Project Plan

Editor: Johannes Klasson

Version 0.1

Status

Reviewed	Johannes Klasson	-
Approved	Martin Nielsen-Lönn	-

PROJECT IDENTITY

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Linköpings Tekniska Högskola, ISY

Group members

Name	**Responsibility**	**Phone**	**E-mail**
Johan Isaksson	Project Leader	070-2688785	johis024@student.liu.se
Johannes Klasson	Document Manager	073-8209003	johkl226@student.liu.se
Jonas Tarasso	Designer	070-5738583	jonta760@student.liu.se
Alexander Yngve	Designer	076-2749762	aleyn573@student.liu.se

Customer: ISY
Contact at customer: Martin Nielsen-Lönn
Course resposible: Atila Alvandpour
Consultant: Martin Nielsen-Lönn

Contents

Document history

Version	**Date**	**Changes**	**Performed by**	**Review by**
0.1	2016-01-31	First draft	Johan Isaksson	

1 Project overview

1.1 Aim and purpose

This project is intended to give knowledge and experience in design and fabrication of CMOS VLSI chips. This includes:

1. Deep insight in physical design of VLSI chips.
2. Knowledge and experience of using professional CAD tools for design, simulation, layout, and verification of VLSI chips.
3. Design of a 'real' and functional chip, starting from the idea and behavioral modeling to detailed circuit design at transistor level, circuit layout, and final verifications.
4. Complete the project using a systematic and professional approach required by industry to run large and complex VLSI projects.

2 Project phases

The project consist of the following five phases:

1. Prestudy
2. High-level system description
3. Top-Down system description
4. Layout
5. Chip assembly

2.1 Phase 1: Prestudy

During the prestudy phase there will be a lot of literature reading and getting a deeper understanding of the project task itself. We will also write the project plan including a time plan.

2.2 Phase 2: High-level system description

The first step in the construction of the chip is to develop the high-level system description, which matches the behavior that the sponsor asked for. This will be done in a hardware descriptive language, which in this case will be Verilog-A, and the design will be simulated to verify that it behaves as intended.

2.3 Phase 3: Top-Down system description

The high-level system description from phase 2 will now be refined to include further details. We will use a top-down methodology as we go from block-level description via gate-level down to a transistor-level implementation. This will be a iterative process as after each new detail we add, we need to simulate and verify the design again. This means that much of the work here will be simulations.

2.4 Phase 4: Layout

Now we will start to build the design from the bottom. Transistors will be used to build small cells, and these cells will then be used in bigger blocks, and so on. This means that the design will be built in a bottom-up fashion. After each step along the way, the design needs to be simulated to verify that each step work correctly.

2.5 Phase 5: Chip assembly

After the layout of the top cell is done, there is still some work to do. We need to add some circuits so that the block can communicate with the off-chip hardware, and after this, the final simulations need to be done.

3 Organisational plan for the project

The project was ordered by the customer, who also delivers the requirement specification and decides if it is fulfilled or not. All contact with the customer and other external parties is handled by the project leader. The project leader shall also plan the work within the group and make sure the group is working towards its common goal. The actual work is not only on the shoulders of the project leader, but on all group members, which play an equal part in the realization of the project. There is also a supervisor available for expert help during the course of the project. Figure 1 illustrates the organisational structure.

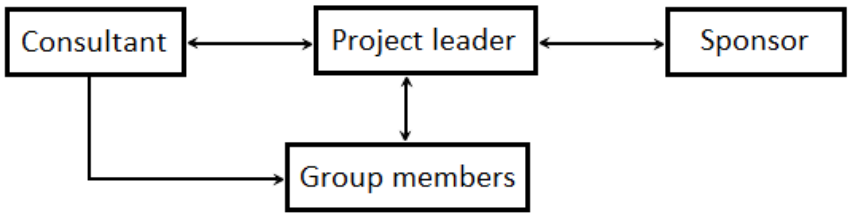

Figure 1 – Organisational plan

3.1 Terms for cooperation within the group

The group has agreed on the following terms:

- All members must be well prepared for meetings.
- Notify the group in time if one can't attend a meeting. In case of illness, this should be reported immediately.
- One shall attend the meetings the group has agreed on.
- If you are unsure of something, you should first seek answers on your own or ask the group. After this external sources may be consulted.
- If a group member doesn't contribute to the project, the rest of the group shall discuss this with the supervisor.

4 Documentation

The documentation listed in table 1 shall be delivered to the sponsor.

Document	Description	Date
Project plan	This is an aid for the project group, describing some basics needed for the collaboration of the project group. This will also include a time plan.	2016-01-31
High-level design report	It should include the complete block level description of the project. Simulation results that verifies the desired functionality should be included. An updated time plan and a time report should be included as well.	2016-02-19
Transistor design report	It should include the complete block level description of the project. Simulation results that verifies the desired functionality should also be included. An updated time plan a, a time report, PAD assignments and an early test plan should be included as well.	2016-03-18
Final report	Block level from the two previous reports should be included along with simulation results of the final design. A final time report, an evaluation plan and a PAD list should also be included. A short evaluation of the projecy should be included as well.	2016-05-27

Table 1 – Documentation

5 Milestones

The milestones are ordered such that the most basic functionality is implemented first. A milestone is considered finished when its functionality is well tested and documented.

Below is the milestones for the project:

#	Description	Date
1	Project selection	2016-01-19
2	Pre-study, project planning and discussion with supervisor	2016-01-31
3	High-level modeling design and simulation result (report)	2016-02-19
4	Gate/transistor level design and simulations result (report)	2016-03-18
5	Layout, DRC, parsitic extraction, LVS, post-layout simulations, modification and chip evaluations	2016-05-18
6	Delivery of the completed chip	2016-05-23
7	Final report and oral presentation	2016-05-27

6 Aktiviteter

Nedan följer de aktiviteter som ska utföras i projektet.

6.1 Utbildning

Följande utbildning krävs för att påbörja projektet.

#	Description	Dependenies	Hours	Date
1	Konvexa kvadratiska optimeringsproblem		70	iteration 1
2	Karush Kunn Tucker bivillkor		42	iteration 1
3	Lagrangemultiplikatorer		14	iteration 1
4	Active set-metoden	1, 2, 3	70	iteration 1
5	Lös enkelt testproblem för hand	4	7	iteration 1
6	Grundutbildning i Latex		7	iteration 1
7	Grundutbildning i Git		7	iteration 1
8	Grundutbildning i Trello		7	iteration 1
9	Grundutbildning i Gurobi		7	iteration 1
10	Grundutbildning i Matlab		7	iteration 1

6.2 Filsystem

Aktiviteter som ska utföras för hantering av in- och utdata från QuadOpt.

#	Description	Dependenies	Hours	Date
11	Definiera filformat och filstruktur		10	iteration 1
12	Implementera inmatning av data till programmet	11	10	iteration 2
13	Implementera utmatning av data från programmet	11	10	iteration 2
14	Utför test av filhanteringssystemet	12, 13	4	iteration 2

6.3 Huvudalgoritm

Aktiviter som ska utföras till implementation av optimeringsalgoritmen.

#	Description	Dependenies	Hours	Date
15	Implementera datastrukturer		35	iteration 1
16	Implementation av matrisaritmetik (multiplikation/addition)	15	20	iteration 1
17	Implementera optimeringsalgoritmen	16	100	iteration 1,2
18	Göra interna tester för att se att problemet går att lösa	17	20	iteration 1,2
19	Optimering av algoritmen		140	iteration 2,3

6.4 Planering

#	Description	Dependenies	Hours	Date
20	Möte varje vecka		200	iteration 1,2,3

6.5 Gränssnitt

#	Description	Dependenies	Hours	Date
21	Definiera gränssnitt mellan modulerna		30	iteration 1
22	Skapa ett gränssnitt (Matlab/terminal)	21	15	iteration 2
23	Definiera och implementera layout för GUI:t		70	iteration 1
24	Definiera och implementera inmatningssyntax för GUI:t		140	iteration 1
25	Hantera inmatning av matriser i GUI:t		105	iteration 2
26	Implementera generering av C-kod i GUI:t		245	iteration 2
27	Koppla samman GUI med lösaren		35	iteration 2
28	Testa gränssnitten	22	50	iteration 2

6.6 Byggsystem

Ett byggsystem krävs för att smidigt kompilera C-koden till de plattformar som gruppen valt att utveckla till.

#	Description	Dependenies	Hours	Date
29	Implementering av kompilering till Linux		14	iteration 3
30	Implementering av kompilering till Windows		14	iteration 3
31	Implementering av kompilering till Mac		7	iteration 3
32	Fixa struktur på Git		1	iteration 1

6.7 Gurobi

För att kunna se hur snabb algoritmen är krävs det ett jämförbart program. Vi har valt att jämföra Quadopt med det kommersiella programmet Gurobi.

#	Description	Dependenies	Hours	Date
33	Testa med Gurobi	9	15	iteration 3
34	Jämför test med egen algoritm	28	15	iteration 3

6.8 Dokumentation

#	Description	Dependenies	Hours	Date
35	Testplan		35	iteration 1
36	Kvalitetsplan		14	iteration 1
37	Arkitektur		35	iteration 1
38	Teknisk dokumentation	Gränssnitt, huvudalgoritm och filsystem är klart	30	iteration 3
39	Användarhandledning	Gränssnitt och GUI är klara	10	iteration 3

7 Project Termination

The project is considered done when the chip design files are delivered and the final report and presentations are done.