TSEK06
Project Plan

Group 5

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Document history

Version	**Date**	**Changes**	**Performed by**
P1A	2016-01-31	First draft	Johan Isaksson
P1B	2016-02-02	Fixed some small misspellings and typos.	Johan Isaksson

1 Project overview

1.1 Aim and purpose

This project is intended to give knowledge and experience in design and fabrication of CMOS VLSI chips. This includes:

1. Deep insight in physical design of VLSI chips.
2. Knowledge and experience of using professional CAD tools for design, simulation, layout, and verification of VLSI chips.
3. Design of a 'real' and functional chip, starting from the idea and behavioral modeling to detailed circuit design at transistor level, circuit layout, and final verifications.
4. Complete the project using a systematic and professional approach required by industry to run large and complex VLSI projects.

1.2 System overview

The following block diagram, taken directly from the requirements specification, illustrates system that shall be implemented.

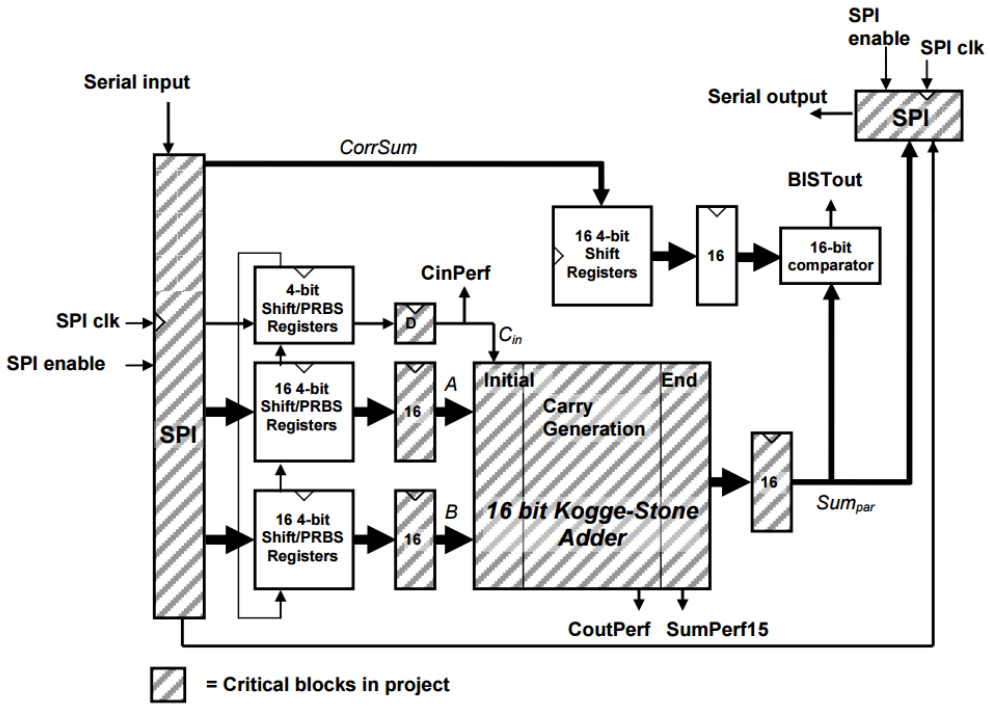

Figure 1 – System block diagram of adder and evaluation circuitry

2 Project phases

The project consist of the following five phases:

1. Prestudy
2. High-level system description

3. Top-Down system description
4. Layout
5. Chip assembly

2.1 Phase 1: Prestudy

During the prestudy phase there will be a lot of literature reading and getting a deeper understanding of the project task itself. We will also write the project plan including a time plan.

2.2 Phase 2: High-level system description

The first step in the construction of the chip is to develop the high-level system description, which matches the behavior that the sponsor asked for. This will be done in a hardware descriptive language, which in this case will be Verilog-A, and the design will be simulated to verify that it behaves as intended.

2.3 Phase 3: Top-Down system description

The high-level system description from phase 2 will now be refined to include further details. We will use a top-down methodology as we go from block-level description via gate-level down to a transistor-level implementation. This will be a iterative process as after each new detail we add, we need to simulate and verify the design again. This means that much of the work here will be simulations.

2.4 Phase 4: Layout

Now we will start to build the design from the bottom. Transistors will be used to build small cells, and these cells will then be used in bigger blocks, and so on. This means that the design will be built in a bottom-up fashion. After each step along the way, the design needs to be simulated to verify that each step work correctly.

2.5 Phase 5: Chip assembly

After the layout of the top cell is done, there is still some work to do. We need to add some circuits so that the block can communicate with the off-chip hardware, and after this, the final simulations need to be done.

3 Organisational plan for the project

The project was ordered by the sponsor, who also delivers the requirement specification and decides if it is fulfilled or not. All contact with the sponsor and other external parties is handled by the project leader. The project leader shall also plan the work within the group and make sure the group is working towards its common goal. The actual work is not only on the shoulders of the project leader, but on all group members, which play an equal part in the realization of the project. There is also a consultant available for expert help during the course of the project. Figure 2 illustrates the organisational structure.

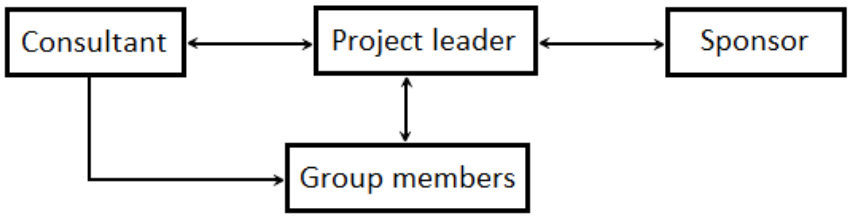

Figure 2 – Organizational structure for the project

3.1 Terms for cooperation within the group

The group has agreed on the following terms:

- All members must be well prepared for meetings.
- Notify the group in time if one can't attend a meeting. In case of illness, this should be reported to the group immediately.
- One shall attend the meetings the group has agreed on.
- If you are unsure of something, you should first seek answers on your own or ask the group. After this external sources may be consulted.
- If a group member doesn't contribute to the project, the rest of the group shall discuss this with the consultant.

4 Documentation

The documentation listed in table 1 shall be delivered to the sponsor.

Document	Description	Date
Project plan	This is an aid for the project group, describing some basics needed for the collaboration of the project group. This will also include a time plan.	2016-01-31
High-level design report	It should include the complete block level description of the project. Simulation results that verifies the desired functionality should be included. An updated time plan and a time report should be included as well.	2016-02-19
Transistor design report	It should include the complete block level description of the project. Simulation results that verifies the desired functionality should also be included. An updated time plan a, a time report, PAD assignments and an early test plan should be included as well.	2016-03-18
Final report	Block level from the two previous reports should be included along with simulation results of the final design. A final time report, an evaluation plan and a PAD list should also be included. A short evaluation of the project should be included as well.	2016-05-27

Table 1 – Documentation to be delivered

5 Milestones

The milestones are ordered such that the most basic functionality is implemented first. A milestone is considered finished when its functionality is well tested and documented.

Below is the milestones for the project:

#	Description	Date
1	Project selection	2016-01-19
2	Pre-study, project planning and discussion with supervisor	2016-01-31
3	High-level modeling design and simulation result (report)	2016-02-19
4	Gate/transistor level design and simulations result (report)	2016-03-18
5	Layout, DRC, parsitic extraction, LVS, post-layout simulations, modification and chip evaluations	2016-05-18
6	Delivery of the completed chip	2016-05-23
7	Final report and oral presentation	2016-05-27

6 Activities

This chapter describes activities and tasks needed for each of the modules/subsystems in this project.

6.1 SPI

The following activities should be carried out to implement the Serial Peripheral unit.

#	Description	Dependenies	Hours	Date
1	Define structure of the SPI unit		10	phase 2
2	Implement counters in Verilog-A	1	10	phase 2
3	Implement control logic in Verilog-A	1	10	phase 2
4	Implement 1:4 decoder in Verilog-A	1	10	phase 2
5	Integrate to high level design of SPI	2,3,4	10	phase 2
44	Implementation of test bench for SPI	5	5	phase 2
6	Simulation and test of high level design	5	5	phase 2
7	Implement transistor level design of the SPI unit	5	30	phase 3
8	Simulation and test of transistor design	7	20	phase 3
9	Implement layout level design of SPI unit	8	30	phase 4
10	Simulation and test of layout	9	20	phase 4

6.2 Number generator

The following activities should be carried out to implement a number generator using pseudo random bit sequence (PRBS).

#	Description	Dependenies	Hours	Date
11	Define structure the generator		10	phase 2
12	Implement linear feedback shift registers in Verilog-A	11	10	phase 2
13	Integrate to high level design of the generator	12	10	phase 2
45	Implementation of test bench for generator	13	5	phase 2
14	Simulation and test of the high level design	13	5	phase 2
15	Implement transistor level design of the generator	14	15	phase 3
16	Simulation and test of the transistor	15	10	phase 3
17	Implement layout level design of generator unit	16	15	phase 4
18	Simulation and test of layout	17	10	phase 4

6.3 Kogge-Stone adder

The following activities should be carried out to implement the adder.

#	Description	Dependenies	Hours	Date
19	Define structure of the adder		10	phase 2
20	Implement Generate calculation logic in Verilog-A	19	10	phase 2
21	Implement Propagate calculation logic in Verilog-A	19	10	phase 2
22	Implement Sum calculation logic in Verilog-A	19	10	phase 2
23	Integrate to high level design of the adder	20,21,22	20	phase 2
46	Implementation of test bench for the adder	23	10	phase 2
24	Simulation and test of the high level design	23	10	phase 2
25	Implement transistor level design of the adder	24	40	phase 3
26	Simulation and test of the transistor design	25	20	phase 3
27	Implement layout level design of adder unit	26	40	phase 4
28	Simulation and test of layout	27	20	phase 4

6.4 Comparator

The following activities should be carried out to implement the the output comparator.

#	Description	Dependenies	Hours	Date
29	Define the structure of the comparator		5	phase 2
30	Implement bit comparator in Verilog-A	29	5	phase 2
31	Integrate to high level design of the comparator	30	10	phase 2
47	Implementation of test bench for the comparator	30	5	phase 2
32	Simulation and test of the high level design	31	5	phase 2
33	Implement transistor level design of the comparator	32	10	phase 3
34	Simulation and test of the transistor design	33	20	phase 3
35	Implement layout level design of adder unit	34	10	phase 4
36	Simulation and test of layout	35	10	phase 4

6.5 System integration

The following activities should be carried out to integrate the modules together.

#	Description	Dependenies	Hours	Date
41	High level integration	5,13,23,31	15	phase 2
48	Implementation of test bench for the complete system	37	20	phase 2
42	Transistor level integration	5,13,23,31	10	phase 3
43	Layout level integration	5,13,23,31	15	phase 4

6.6 Chip assembly

The following activity should be carried out to be able to manufacture the chip.

#	Description	Dependenies	Hours	Date
37	Off-chip hardware interface	10,18,27,36	20	phase 5

6.7 Documentation

The following activity should be carried out to provide satisfactory documentation.

#	Description	Dependenies	Hours	Date
38	Documentation and presentation		60	phase 2,3,4,5

6.8 Planning

The following activities should be carried out for administrative work.

#	Description	Dependenies	Hours	Date
39	Meetings		60	phase 2,3,4,5
40	Buffer time		80	phase 2,3,4,5

7 Project Termination

The project is considered done when the chip design files are delivered and the final report and presentations are done.