Planning

Project: 16 bit Kogge-Stone ad

Project group: 5	**Date: 160204**	**Reviewed:**
Customer: Martin Nielsen-Lön	**Version: P1B**	Johannes Klasson
Course: TSEK06	**Author: JI**	

ACTIVITIES		TIME	WHO	TIME PLAN (week number)																		
no	Description	hours	Initials	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
1	Define structure of the SPI unit	10	JI, JK		9,5																	0,5
2	Implement counters in Verilog-A	10	JI, JK		4																	6
3	Implement control logic in Verilog-A	10	JI, JK			10																0
4	Implement 1:4 decoder in Verilog-A	10	JI, JK			5,																4,5
5	Integrate to high level design of SPI	10	JI, JK			17																−7
6	Simulation and test of high level design (SPI)	5	JI, JK				13															−8
7	Implement transistor level design of the SPI unit	30	JI, JK					15	15													0
8	Simulation and test of transistor design (SPI)	20	JI, JK							20												0
9	Implement layout level design of SPI unit	30											25	25								−2
10	Simulation and test of layout (SPI)	20													20							0
11	Define structure of the generator	10	AY		0																	10
12	Implement linear feedback shift registers in Verilog-A	10	AY			0																10
13	Integrate to high level design of the generator	10	AY			0																10
14	Simulation and test of the high level design (generator)	5	AY				0															5
15	Implement transistor level design of the generator unit	15	JI, JK					10	5													0
16	Simulation and test of the transistor design (generator)	10	JI, JK							10												0
17	Implement layout level design of generator unit	15											10	5								0
18	Simulation and test of layout (generator)	10													10							0
19	Define structure of the adder	10	JT, AY		3																	7
20	Implement Generate calculation logic in Verilog-A	10	JT, AY		1																	9
21	Implement Propagate calculation logic in Verilog-A	10	JT, AY		1																	9
22	Implement Sum calculation logic in Verilog-A	10	JT, AY		1																	9
23	Integrate to high level design of adder	20	JT, AY				17															3
24	Simulation and test of high level design (adder)	20	JT, AY				3,															16,
25	Implement transistor level design of the adder unit	40	JT, AY					20	20													0
26	Simulation and test of the transistor design (adder)	20	JT, AY						10	10												0
27	Implement layout level design of adder unit	40											10	13	15	15						−1
28	Simulation and test of layout (adder)	20															20					0
29	Define structure of the comparator	5	JT		0																	5
30	Implement bit comparator in Verilog-A	5	JI			0																5
31	Integrate to high level design of the comparator	10	JI			2																8
32	Simulation and test of the high level design (comparator)	5	JI				2															3
33	Implement transistor level design of the comparator unit	20	JT, AY					5	5													10
34	Simulation and test of the transistor design (comparator)	10	JT, AY							10												0
35	Implement layout level design of comparator unit	20											15	15								−1
36	Simulation and test of layout (comparator)	10													10							0
37	Off-chip hardware interface	30																15	15			0
38	Documentation and presentation	60		28			35		20	20									10	20		−7
39	Meetings	60			11	0	0	4	4	4			4	4	4	4	4	4	4	4	4	1
40	Buffer time	80						15	10	10			5	5	5	5	5	5	5	10	0	0
41	High level integration	15	JI, JH, JT, AY				14															1
42	Transistor level integration	10								10												0
43	Layout level integration	15														30						−1
44	Implementation of test bench for SPI	5	JH			0																5
45	Implementation of test bench for generator	5	JI		0																	5
46	Implementation of testbench for adder	10	AY		0																	10
47	Implementation of test bench for comparator	5	JT		0																	5
48	Implementation of test bench for the complete system	20					15															5
	Sum, number of hours	755			30,5	34	99	69	89	94	0	0	69	67	64	54	29	24	34	34	4	0