Intel Corporation
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# Cyclone 10 LP I/O Buffer Encrypted HSPICE Model User Guide

For use only with HSPICE version 2009.03 or later

## Final Model

# 1 Introduction

This document is the HSPICE model user guide for all regular output buffers available in the Cyclone 10 LP device. The Cyclone 10 LP I/O is reconfigurable, and provides a combination of various features built into the device. The information in this document enables the user to configure the HSPICE models to his/her requirements.

This document will discuss the naming convention for the HSPICE models, file layout and organization, procedure for setting various output standards, and a list of all HSPICE models for various I/O standards supported by the Cyclone 10 LP device.

Note that throughout this document and the models, the terms HIO and VIO are used. HIO is the horizontal I/O, modeling the left and right banks, and VIO is the Vertical I/O, modeling the top and bottom banks.

### What is included in this kit?

This kit contains the following materials:

1. Encrypted transistor and logic cell library models.
2. Encrypted output buffer circuit models for single ended and differential I/Os.
3. Single ended and differential sample HSPICE decks.

## 2 File Directory Structure

Figure 1 shows the directory structure of the Cyclone 10 LP HSPICE model kit.

```
  Cyclone10 LP
_SPICE_Model_Ver01
   |________ cir
   |
   |________ docs
   |
   |________ lib
   |
   |________ sim
            |________ IV
            |
            |________ TrTf
            |
            |________ LVDS
```

**Figure 1. - Directory Structure of the Cyclone 10 LP HSPICE Modeling Kit**

The contents of each directory are as follows:

**sim:**

This directory contains the top level HSPICE files for all I/O standard simulations. The files that reside here can be modified to simulate any available I/O standard, drive strength, process corner, supply voltage, and/or temperature.

IV – IV curve simulations of the single-ended buffers:

1. HIO_TT_N.sp – HIO IV simulations for TT corner using NMOS pull-down.
2. HIO_TT_P.sp – HIO IV simulations for TT corner using PMOS pull-up.
3. VIO_TT_N.sp – VIO IV simulations for TT corner using NMOS pull-down.
4. VIO_TT_P.sp – VIO IV simulations for TT corner using PMOS pull-up.

TrTf – Transient rise and fall simulations of the single-ended output buffers:

1. HIO_TTL.sp – TTL & CMOS simulations using the horizontal output buffer.
2. HIO_HSTL.sp – HSTL simulations using the horizontal output buffer.
3. HIO_PCI.sp – PCI simulations using the horizontal output buffer.
4. HIO_SSTL.sp – SSTL simulations using the horizontal output buffer.
5. VIO_TTL.sp – TTL & CMOS simulations using the vertical output buffer.
6. VIO_HSTL.sp – HSTL simulations using the vertical output buffer.
7. VIO_PCI.sp – PCI simulations using the vertical output buffer.
8. VIO_SSTL.sp – SSTL simulations using the vertical output buffer.
9. VIO_TTL_SUB.sp – Sample SPICE deck of placing Cyclone 10 LP IO buffer model into the sub-circuit. User can used as an example when having problems to co-simulate Cyclone 10 LP device with other vendor's device

LVDS – Transient and DC simulations of the differential output buffers:

1. HIO_EXTRES_LVDS.sp – Transient simulation using the horizontal external resistor LVDS output buffer.
2. VIO_EXTRES_LVDS.sp – Transient simulation using the vertical external resistor LVDS output buffer.
3. HIO_DEDICATED_LVDS.sp – Transient simulation using the horizontal dedicated differential LVDS output buffer.

**cir:**

This directory contains the encrypted HSPICE netlists for the I/O structures. All netlist file content is encrypted, with the exception of the .subckt definition. Separate circuit files exist for each I/O buffer component for improved simulation runtime, as only the required circuits are instantiated for simulation.

Single Ended and Differential I/O Models:

1. HIO_buffer.inc – Encrypted model of the horizontal input and output buffers.
2. VIO_buffer.inc – Encrypted model of the vertical input and output buffers.
3. HIO_diff_buffer.inc – Encrypted model of the horizontal external resistor LVDS output buffer.
4. VIO_diff_buffer.inc – Encrypted model of the vertical external resistor LVDS output buffer.
5. HIO_deddiff_buffer.inc – Encrypted model of the horizontal dedicated differential LVDS output buffer.

**lib:**

This directory contains the transistor model libraries and drive strength libraries. All files in this directory are listed below:

1. C10LP _tt.inc – Encrypted process model for typical-typical corner.
2. C10LP _ff.inc – Encrypted process model for fast-fast corner.
3. C10LP _ss.inc – Encrypted process model for slow-slow corner.
4. drive_select_HIO.lib – Unencrypted drive strength ram settings for SE HIO.
5. drive_select_VIO.lib – Unencrypted drive strength ram settings for SE VIO.
6. drive_select_LVDS.lib – Unencrypted drive strength ram settings for LVDS.
7. package.lib – Encrypted package model.
8. sample_brd.sp – Unencrypted sample board trace model.
9. IO_load.lib – Unencrypted termination and loading library.

**docs:**

This directory contains the Cyclone 10 LP IO HSPICE model user guide and the release note.

# 3 Single Ended I/O HSPICE Models

Figure 2 shows the general setup for all single ended I/Os HPSICE decks provided in this kit. It contains the transmitter buffer, package parasitic driver terminations, simple topology of a transmission line interconnect, receiver parallel terminations and the receiver buffer. The package parasitic can be changed according to user's requirements for the specific device and package. Depending on the I/O standard, either series or parallel, or both terminations are used at the transmitter end. The following are the description of major sections in the sample single ended IO SPICE deck.

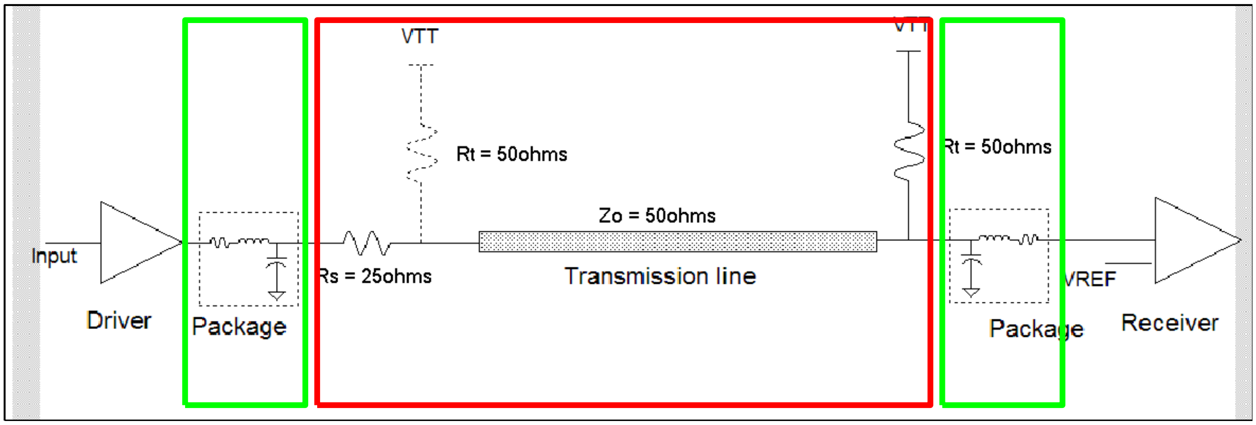

**Figure 2. - Single Ended HSPICE Model Sample Setup**

**HSPICE Optimization/Initialization Header:**

The section "Options and Initial Conditions" defines some of the Synopsys HSPICE tool specific simulation control options. The user may need to adjust the value of these option parameters, depending on the complexity of the topology of the HSPICE circuit. These options improve the DC and transient convergence and ultimately speed up the simulation time. Some of these options are explained below:

```
.options badchr       * Warns when a non-ASCII character is encountered.
.options co=132       * Sets the number of columns for printout.
.options scale=1e-6   * Sets the size multiplier (for L & W).
.options ingold=2     * Sets the output to exponential format.
.options nomod        * Suppresses the printout of model parameters.
.options dv=1.0       * Limits iteration-to-iteration voltage change for
                      * circuit nodes in DC and TRAN analysis.
.options probe        * Limits the postprocessor output to just the
                      * probe/print/plot/graph variables.
.options captab=0     * 1=Reports node capacitances at each operating
                      * point.
.options accurate=1     * 1=Sets the timestep to give better TRAN accuracy.
.options post=2       * Set output display
```

The section "Process/Voltage/Temperature Setting" sets the PVT for Typical-Typical, Slow-Slow, and Fast-Fast corner case analysis. It also defines the path of the encrypted process cell netlist files.

The section “Power Supply connections” defines the global supply voltage (VCC) and global ground (VSS) of the I/O core. The voltage parameter “Vc” defined in this section is a unique voltage level that is used throughout this kit to define all logic ‘1’ control signals. It also defines the IO supply voltage Vccn, IO supply ground Vssn and the pull-up termination voltage for the parallel terminations VTT.

The section “Control Signals” defines the CSR bits connections and the input control signals to the IO buffer.

### Buffer netlist instantiation:

In this section, the single ended Cyclone 10 LP output buffer models (located in the “cir” subdirectory) are instantiated. The instantiations are different depending on the type of buffer.

Vertical I/O:

```
XVIO PIN CODIN COOEB VCCN VSSN VSS VCC VREF
+ RPCDP7 RPCDP6 RPCDP5 RPCDP4 RPCDP3 RPCDP2 RPCDP1 RPCDP0
+ RPCDN7 RPCDN6 RPCDN5 RPCDN4 RPCDN3 RPCDN2 RPCDN1 RPCDN0
+ RPCDNEXTRA RPDLY RNDLY RPCI RPULLUP RPCDSR1 RPCDSR0 RAMBH
+ ROPDRAIN VIO_BUF
```

Horizontal I/O:

```
XHIO PIN CODIN COOEB VCCN VSSN VSS VCC VREF
+ RPCDP7 RPCDP6 RPCDP5 RPCDP4 RPCDP3 RPCDP2 RPCDP1 RPCDP0
+ RPCDN7 RPCDN6 RPCDN5 RPCDN4 RPCDN3 RPCDN2 RPCDN1 RPCDN0
+ RPCDNEXTRA RPDLY RNDLY RPCI RPULLUP RPCDSR1 RPCDSR0 RAMBH
+ ROPDRAIN HIO_BUF
```

In these sub-circuits, the HSPICE node “CODIN” is the data signal input to output buffer. Any input stimulus is applied to this node. Similarly, the node “PIN” is the output node. All of these nodes are defined in detail in Table 1 and Table 2 of the “Control Signals” section of this document.

Also in this section, some files in the “lib” directory are called. These files define all control signal voltage levels to select output buffer drive strength based on the type of I/O standard and the termination resistor and load capacitor values based on the termination scheme. A complete listing of available I/O standards for HIO and VIO can be found in ‘Appendix’ section of this document.

## Package Model:

The package model sub-circuit is instantiated in this section. The package model in the sample SPICE deck is for EP325F324 device. The package model can be changed according to user’s requirements for the specific device and package.

## Transmission Line Interconnect:

This section defines the topology of the target board. This may include transmission lines, interconnect, vias, connectors and cable SPICE sub-circuits. The end user must modify this section to represent the actual board design, or target board environment. The link provided is for reference only.

# 4 Differential I/O HSPICE Models

Figure 3 shows the general setup for the differential I/O. It contains the differential output buffer, package parasitic driver terminations, simple topology of a transmission line interconnect, receiver termination and the differential receiver load. The package parasitic can be changed according to the user's requirements for a specific device and package. The following are the description of major sections in the sample differential IO SPICE deck.

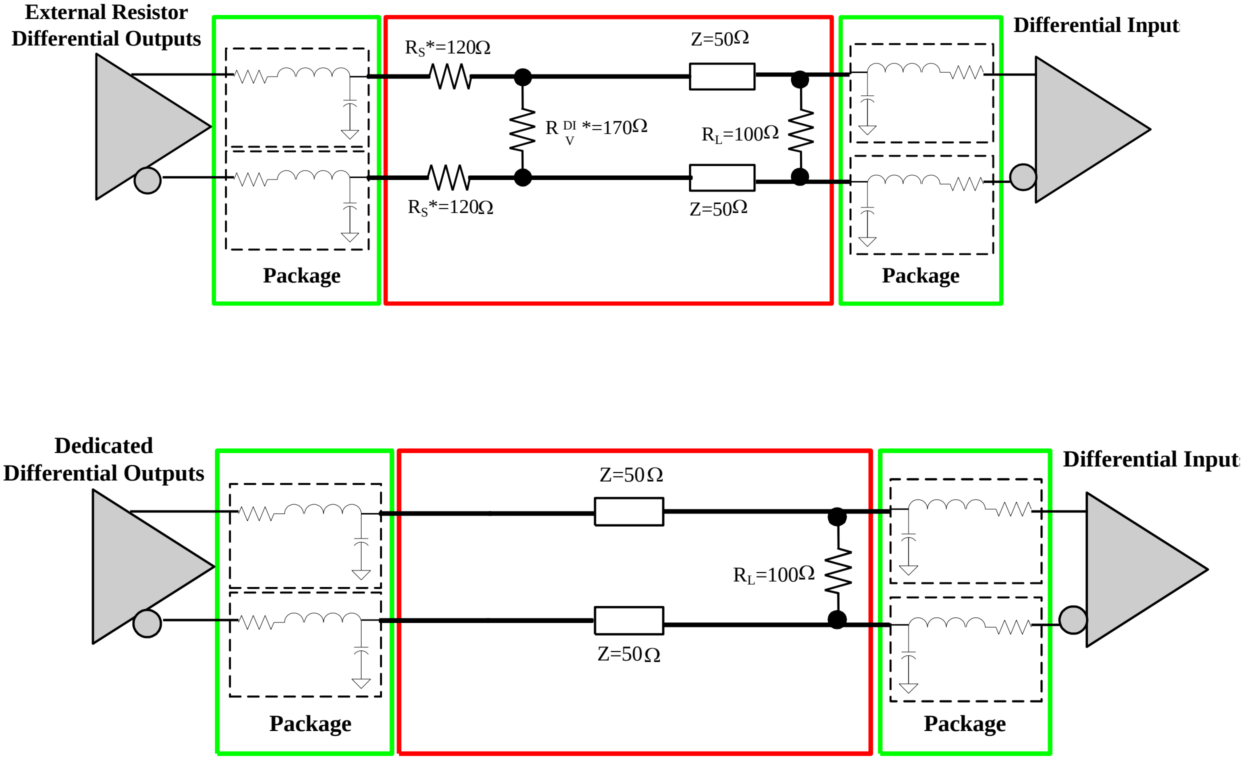

**Figure 3. - External Resistor and Dedicated Differential HSPICE Model Setup**

**HSPICE Optimization/Initialization Header:**

The section "Options and Initial Conditions" defines some of the Synopsys HSPICE tool specific simulation control options. The user may need to adjust the value of these option parameters depending on the complexity of the topology of the HSPICE circuit. These options improve the DC and transient convergence and ultimately speed up the simulation time. Some of these options are explained below:

```
.options badchr       * Warns when a non-ASCII character is encountered.
.options co=132       * Set the number of columns for printout.
.options scale=1e-6   * Sets the size multiplier (for L & W).
.options ingold=2     * Sets the output to exponential format.
.options nomod        * Suppresses the printout of model parameters.
.options dv=1.0       * Limits iteration-to-iteration voltage change for
```

```
                         * circuit nodes in DC and TRAN analysis.
.options probe           * Limits the postprocessor output to just the
                         * probe/print/plot/graph variables.
.options captab=0        * 1=Reports node capacitances at each operating
                         * point.
.options post=2          * Set output display format
.options accurate=1      * 1=Sets the timestep to give better TRAN accuracy.
```

The section “Process/Voltage/Temperature Setting” sets the PVT for the Typical-Typical, Slow-Slow, and Fast-Fast corner case analysis. It also defines the path of the encrypted process cell netlist files.

The section “Power Supply connections” defines the global supply voltage (VCC) and global ground (VSS) of the I/O core. The voltage parameter “Vc” defined in this section is a unique voltage level that is used throughout this kit to define all logic ‘1’ control signals. It also defines the IO supply voltage Vccn, and IO supply ground Vssn.

The section “Control Signals” defines the CSR bits connections and the input control signals to the IO buffer.

**LVDS Output Buffer Netlist Instantiation:**

Cyclone 10 LP supports external resistor LVDS on VIO and HIO. However, dedicated LVDS is supported only on HIO. The Cyclone 10 LP external resistor and dedicated LVDS output buffers are respectively instantiated by the following sub-circuits:

External Resistor LVDS Vertical I/O:

```
XDIFF_VIO PINA PINB CODIN COOEB VCCN VSSN VSS VCC
+ RPCDP7 RPCDP6 RPCDP5 RPCDP4 RPCDP3 RPCDP2 RPCDP1 RPCDP0
+ RPCDN7 RPCDN6 RPCDN5 RPCDN4 RPCDN3 RPCDN2 RPCDN1 RPCDN0
+ RPCDNEXTRA RPCDSR1 RPCDSR0 VIO_DIFF_OUT
```

External Resistor LVDS Horizontal I/O:

```
XDIFF_HIO PINA PINB CODIN COOEB VCCN VSSN VSS VCC
+ RPCDP7 RPCDP6 RPCDP5 RPCDP4 RPCDP3 RPCDP2 RPCDP1 RPCDP0
+ RPCDN7 RPCDN6 RPCDN5 RPCDN4 RPCDN3 RPCDN2 RPCDN1 RPCDN0
+ RPCDNEXTRA RPCDSR1 RPCDSR0 HIO_DIFF_OUT
```

Dedicated LVDS Horizontal I/O:

```
XDEDDIFF_HIO PINA PINB CODIN VCCN VSSN VSS VCC
+ RLVDSA3 RLVDSA2 RLVDSA1 RLVDSA0
+ RLVDSB3 RLVDSB2 RLVDSB1 RLVDSB0 HIO_DEDDIFF_OUT
```

In these sub-circuits, the HSPICE node “CODIN” is the input to the differential output buffer model. Any input stimulus is applied to this node. Similarly, the nodes “PINA” and “PINB” are the output nodes of the differential buffer. All of these ports are defined in detail in Table 3, Table 4 and Table 5 of the “Control Signals” section of this document.

## Package Model:

The package model sub-circuit is instantiated in this section. The package model in the sample SPICE deck is for EP325F324 device. The package model can be changed according to user's requirements for the specific device and package.

## Transmission Line Interconnect:

This section defines the topology of the target board. This may include transmission lines, interconnect, vias, connectors and cable SPICE sub-circuits. The end user must modify this section to represent the actual board design, or target board environment. The link provided is for reference only.

# 5 Control Signals

This section defines the sets of control signals used by the Cyclone 10 LP single ended and differential output buffers. Tables 1 and 2 shows the control signals used by the single ended output buffers. Similarly, Tables 3, 4, and 5 describes the control signals used by the differential output buffer. Section 7 "Setting I/O Standards" describes how to use these parameters to set up the buffer for specific I/O standards.

**Table 1: Control Signals for Vertical Single Ended Output Buffer (VIO_buffer.inc)**

| **HSPICE Node / Control Signal** | **Description** |
|---|---|
| CODIN | Data input to the single ended output buffer from the core. |
| COOEB | Output enable.  Set to '0' to enable, and "vc" to disable. |
| ROPDRAIN | Open-drain.  Set to "vc" to enable, and '0' to disable. |
| PIN | Output of the output buffer. |
| RAMBH | Bus hold enable signal.  Set to "vc" to enable, and '0' to disable. |
| RPCDP[7:0] | Controls the PMOS output transistors.  Set by "drive_select_VIO.lib." |
| RPCDN[7:0] | Controls the NMOS output transistors.  Set by "drive_select_VIO.lib." |
| RPCDNEXTRA | Controls the NMOS output transistors for 3.0V and 3.3V.  Set by "drive_select_VIO.lib." |
| RPCDSR[1:0] | Output slew rate control signal. |
| RPULLUP | Weak pull-up enable.  Set to "vc" to enable, and '0' to disable. |
| RPDLY | Delay bits.  (Not used.) |
| RNDLY | Delay bits.  (Not used.) |
| RPCI | Enable PCI Switch. |
| VREF | External reference voltage for input buffer. |
| VCCN | I/O buffer supply voltage. |
| VSSN | I/O buffer supply ground. |
| VCC | Global supply voltage. |
| VSS | Global supply ground. |

**Table 2: Control Signals for Horizontal Single Ended I/O Buffer (HIO_buffer.inc)**

| **HSPICE Node / Control Signal** | **Description** |
|---|---|
| CODIN | Data input to the single ended output buffer from the core. |
| COOEB | Output enable.  Set to '0' to enable, and "vc" to disable. |
| ROPDRAIN | Open-drain.  Set to "vc" to enable, and '0' to disable. |
| PIN | Output of the output buffer. |
| RAMBH | Bus hold enable signal.  Set to "vc" to enable, and '0' to disable. |
| RPCDP[7:0] | Controls the PMOS output transistors.  Set by "drive_select_HIO.lib." |
| RPCDN[7:0] | Controls the NMOS output transistors.  Set by "drive_select_HIO.lib." |
| RPCDNEXTRA | Controls the NMOS output transistors for 3.0V and 3.3V.  Set by "drive_select_HIO.lib." |

| | |
|---|---|
| RPCDSR[1:0] | Output slew rate control signal. |
| RPULLUP | Weak pull-up enable.  Set to “vc” to enable, and ‘0’ to disable. |
| RPDLY | Delay bits.  (Not used.) |
| RNDLY | Delay bits.  (Not used.) |
| RPCI | Enable PCI Switch. |
| VREF | External reference voltage for input buffer. |
| VCCN | I/O buffer supply voltage. |
| VSSN | I/O buffer supply ground. |
| VCC | Global supply voltage. |
| VSS | Global supply ground. |

**Table 3: Control Signals for External Resistor LVDS Output Buffer (VIO_diff_buffer.inc)**

| **HSPICE Node / Control Signal** | **Description** |
|---|---|
| CODIN | Data input to the differential output buffer from the core. |
| COOEB | Output enable.  Set to ‘0’ to enable, and “vc” to disable. |
| PINA/PINB | Differential output buffer output pins. |
| RPCDP[7:0] | Controls the PMOS output transistors.  Set by “drive_select_VIO.lib.” |
| RPCDN[7:0] | Controls the NMOS output transistors.  Set by “drive_select_VIO.lib.” |
| RPCDSR[1:0] | Output slew rate control signal. |
| RPCDNEXTRA | Controls the NMOS output transistors for 3.0V and 3.3V.  Set by “drive_select_VIO.lib.” |
| VCCN | I/O buffer supply voltage. |
| VSSN | I/O buffer supply ground. |
| VCC | Global supply voltage. |
| VSS | Global supply ground. |

**Table 4: Control Signals for External Resistor LVDS Output Buffer (HIO_diff_buffer.inc)**

| **HSPICE Node / Control Signal** | **Description** |
|---|---|
| CODIN | Data input to the differential output buffer from the core. |
| COOEB | Output enable.  Set to ‘0’ to enable, and “vc” to disable. |
| PINA/PINB | Differential output buffer output pins. |
| RPCDP[7:0] | Controls the PMOS output transistors.  Set by “drive_select_HIO.lib.” |
| RPCDN[7:0] | Controls the NMOS output transistors.  Set by “drive_select_HIO.lib.” |
| RPCDSR[1:0] | Output slew rate control signal. |
| RPCDNEXTRA | Controls the NMOS output transistors for 3.0V and 3.3V.  Set by “drive_select_HIO.lib.” |
| VCCN | I/O buffer supply voltage. |
| VSSN | I/O buffer supply ground. |
| VCC | Global supply voltage. |
| VSS | Global supply ground. |

### Table 5: Control Signals for Dedicated Differential LVDS Output Buffer (HIO_deddiff_buffer.inc)

| HSPICE Node / Control Signal | Description |
|---|---|
| CODIN | Data input to the differential output buffer from the core. |
| PINA/PINB | Differential output buffer output pins. |
| RLVDSA[3:0] | Controls the LVDS pre-emphasis. Set by “drive_select_LVDS.lib.” |
| RLVDSB[3:0] | Controls the LVDS Vod. Set by “drive_select_LVDS.lib. |
| VCCN | I/O buffer supply voltage. |
| VSSN | I/O buffer supply ground. |
| VCC | Global supply voltage. |
| VSS | Global supply ground. |

# 6 Output Slew Rate Settings for SE Output Buffer

This section describes the programmable slew rate settings. The output buffer for Cyclone 10 LP device has a programmable output slew-rate control that the user can configure for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. A slow slew rate can help reduce system noise and overshoot. The slew rate control affects both the rising and falling edges.

There are three slew rate control settings available for each supported I/O standard: slow, medium, and fast. Slew rate control is available for single-ended I/O standards with current strength 8 mA or higher. 3.3-V LVTTL and 3.3-V LVCMOS I/O standards do not support slew rate control. The default slew rate setting for all the I/O standard is the fast setting (RPCDSR [1:0] =10). The slew rate is set to the default for a particular library that does not support programmable slew rate control.

### Setting Output Slew Rate Control

User can select the slew rate setting by using slew_rate_control.lib library.

Example #1: Fast Slew Rate Settings

```
* Fast slew rate
vrpcdsr1   rpcdsr1   0 dc vc
vrpcdsr0   rpcdsr0   0 dc 0
```

Example #2: Medium Slew Rate Settings

```
* Medium slew rate
*vrpcdsr1   rpcdsr1   0 dc 0
*vrpcdsr0   rpcdsr0   0 dc vc
```

Example #3: Slow Slew Rate Settings

```
* Slow slew rate
*vrpcdsr1   rpcdsr1   0 dc 0
*vrpcdsr0   rpcdsr0   0 dc 0
```

# 7 Setting I/O Standards

**Table 6: I/O Standards Supported in the Cyclone 10 LP HSPICE Models**

| Standard | Supply | VIO | HIO |
|---|---|---|---|
| LVTTL/LVCMOS | 3.3V | ✓ | ✓ |
| LVTTL/LVCMOS | 3.0V | ✓ | ✓ |
| LVTTL/LVCMOS | 2.5V | ✓ | ✓ |
| LVTTL/LVCMOS | 1.8V | ✓ | ✓ |
| LVCMOS | 1.5V | ✓ | ✓ |
| LVCMOS | 1.2V | ✓ | ✓ |
| PCI/PCI-X | 3.3V | ✓ | ✓ |
| SSTL2 Class I | 2.5V | ✓ | ✓ |
| SSTL2 Class II | 2.5V | ✓ | ✓ |
| SSTL18 Class I | 1.8V | ✓ | ✓ |
| SSTL18 Class II | 1.8V | ✓ | ✓ |
| 1.8V HSTL Class I | 1.8V | ✓ | ✓ |
| 1.8V HSTL Class II | 1.8V | ✓ | ✓ |
| 1.5V HSTL Class I | 1.5V | ✓ | ✓ |
| 1.5V HSTL Class II | 1.5V | ✓ | ✓ |
| 1.2V HSTL Class I | 1.2V | ✓ | ✓ |
| 1.2V HSTL Class II | 1.2V | ✓ | - |
| External Resistor LVDS | 2.5V | ✓ | ✓ |
| Dedicated LVDS | 2.5V | - | ✓ |

### Setting Single Ended Standards

To set a single ended output standard, the following steps should be taken:

1) Set OEB to ‘0’ to enable the output buffer:

```
VCOOEB COOEB 0 0
```

2) Select the required output standard by using the “drive_select_VIO.lib” or “drive_select_HIO.lib” libraries. For example, to select the “3.3V LVTTL 8mA” output for the VIO, use the following line:

```
.lib ‘../../lib/drive_select_VIO.lib’ p_33ttl_8ma
.lib '../../lib/IO_load.lib' ttl
```

3) Select the required output slew rate settings, default is fast:

```
* Fast slew rate
vrpcdsr1   rpcdsr1   0 dc vc
vrpcdsr0   rpcdsr0   0 dc 0
```

4) Set the VCCN supply to the appropriate voltage for the selected output standard:

```
.param vcn = 3.3
```

### Setting Differential Standards

To set the external resistor differential output buffer, the following steps should be taken:

1) Set OEB to ‘0’ to enable the output buffer:

```
VCOOEB COOEB 0 0
```

2) Select the required output standard by using the “drive_select_VIO.lib” or “drive_select_HIO.lib” libraries. For example, to select the “External Resistor LVDS” output for the VIO, use the following line:

```
.lib ‘../../lib/drive_select_VIO.lib’ p_diff_3_resistor
```

3) Set the VCCN supply to the appropriate voltage for the selected output standard:

```
.param vcn = 2.5
```

To set the dedicated differential LVDS output buffer, the following step should be taken:

1) Set RLVDSA0 to ‘1’ to enable the output buffer:

```
VRLVDSA0 RLVDSA0 0 vc
```

2) Enable or disable pre-emphasis by using the “drive_select_LVDS.lib” library. For example, to enable pre-emphasis, use the following line:

```
.lib ‘../../lib/drive_select_LVDS.lib’ enable_pre_emphasis
```

3) To disable pre-emphasis, use the following line:

```
.lib ‘../../lib/drive_select_LVDS.lib’ disable_pre_emphasis
```

# 8 Scale Factor

The Altera HSPICE models uses scale factor = 1e-6, but other vendors may use scale factor = 1. To be able to use the HSPICE models of various vendors with mixed technology, “Hier_scale” needs to be used to override the .option scale of the two vendors.

Following steps should be taken for mixed technology simulations:

1) If you want to do mixed technology simulations, you will have to override the “.OPTION SCALE” of the two vendors.
2) Enable option “HIER_SCALE.”
3) Ensure that neither vendor is using the parameter "S" in their sub-circuits.
4) At the top-level, add "S=1e-6" AT THE END of the instance call for the vendor instance which requires SCALE=1e-6. (Example: Altera)

Below is an example of how to implement “Hier_scale” in the HSPICE deck:

```
* top-level netlist
.inc vendor1.inc  $ Uses SCALE=1
.inc altera.inc   $ Uses SCALE=1e-6
.option SCALE=1 HIER_SCALE
x1 in wire_in vendor1_outbuf
x2 wire_out out altera_inbuf S=1e-6
w1 wire_in 0 wire_out 0 RLGCmodel=...
...
```

# 9 Co-simulation for Two Different Devices

When performing link simulations using models from multiple devices and/or vendors, users may encounter problems. The most common error message is that there is node redefinition in the encrypted circuit netlist. A solution for this problem is to create sub-circuits for each device and place the encrypted process file and circuit netlists within the sub-circuits. This resolves the node redefinition error. Users can call both sub-circuits through X instantiations at the top level SPICE file and make the appropriate link.

The SPICE template VIO_TTL_sub.sp in the kit provides an example of how to make the sub-circuit for Cyclone 10 LP output buffer and instantiate the sub-circuit through X call from the top level SPICE deck to successfully co-simulate two different devices. It is recommended that the user follow this example to get started.

# 10 Simulation Example - TTL using VIO

This section provides sample HSPICE deck, describing in detail how to successfully simulate board designs that contain Cyclone 10 LP devices. It is recommended that the user follow this example to get started. This example can be easily modified to replace the current board trace with any user specified board design.

**Topology of the HSPICE deck “VIO_TTL.sp”:**

1. Process settings:

   This section defines the process corner for typical (typical-typical), slow (slow-slow), fast best (fast-fast) cases. For typical PVT, the “C10LP_tt.inc” model is used.

   ```
   * Process settings
   .inc '../../lib/C10LP_tt.inc'   * Typical-Typical
   *.inc '../../lib/C10LP_ss.inc'  * Slow-Slow
   *.inc '../../lib/C10LP_ff.inc'  * Fast-Fast
   ```

2. Options and initial conditions:

   This section contains various HSPICE options required to improve the overall simulation quality (such as DC and transient convergence). The user may need to adjust these parameters and/or their values each time the topology of the HSPICE deck is changed.

   ```
   * Simulation options
   .options brief=0
   .options badchr co=132 scale=1e-6 acct ingold=2 nomod dv=1.0
   +        dcstep=1 absv=1e-3 absi=1e-8 probe captab post =2
   ```

3. Temperature setting:

   This section defines the temperature for typical, worst, and best cases. For typical PVT, temp=25C.

   ```
   * Temperature
   *.temp -40
   *.temp 0
   .temp 25
   *.temp 85
   *.temp 100
   ```

4. Supply voltage setting:

   This section defines the operating voltages of the device, for both core and I/O.

   ```
   * Supply Voltages
   .param vcn = 3.3
   .param vc = 1.2
   ```

5. Power supplies:

This section sets the supply voltages used by the I/O buffer.

```
vvccn vccn 0 vcn
vvssn vssn 0 0
vvss  vss  0 0
vvcc  vcc  0 vc
```

6. Constants definition:

   Here the RAM bits and control voltages of the output buffer are set. The majority are parameters that are defined by the “drive_select” libraries.

7. Netlist:

   This section includes the encrypted buffer netlist.

```
.include '../../cir/VIO_buffer.inc'
```

8. Circuit instantiation:

   This section instantiates the output buffer, and defines the nodes connected to the output buffer.

```
XVIO PIN CODIN COOEB VCCN VSSN VSS VCC VREF
+ RPCDP7 RPCDP6 RPCDP5 RPCDP4 RPCDP3 RPCDP2 RPCDP1 RPCDP0
+ RPCDN7 RPCDN6 RPCDN5 RPCDN4 RPCDN3 RPCDN2 RPCDN1 RPCDN0
+ RPCDNEXTRA RPDLY RNDLY RPCI RPULLUP RPCDSR1 RPCDSR0 RAMBH
+ ROPDRAIN VIO_BUF
```

9. Package instantiation:

   This section connects the package model to the output pin of the IO buffer. Different sub-circuit should be instantiated for different device and package.

| **Library Call** | **Sub-circuit Call** |
|---|---|
| pkg_EPSR15_Q148<br>pkg_EPSR15_F169 | PKG_Q148<br>PKG_F169 |

```
.lib '../../lib/package.lib' pkg_EPSR15_Q148
XPKG_Q148 PIN BALL PKG_Q148
```

10. Transient simulation and HSPICE output:

    This section executes the transient simulation for 12ns, outputs the waveforms seen at the listed nodes, and measures the rise and fall time of the waveform at the destination node.

```
* Transient Simulation
.tran 0.02ns 12ns

* Waveform Output Data
```

```
.print tran v(CODIN) v(BALL) v(COOEB) v(PIN)

* Measure Output Data
.mea vmax MAX v(BALL) from=0.1ns to=4ns
.mea vmin MIN v(BALL) from=4ns   to=10ns
.mea tran rise_time trig v(BALL) val='0.2*(vmax-vmin)+vmin' rise=1
+                   targ v(BALL) val='0.8*(vmax-vmin)+vmin' rise=1
.mea tran fall_time trig v(BALL) val='0.8*(vmax-vmin)+vmin' fall=1
+                   targ v(BALL) val='0.2*(vmax-vmin)+vmin' fall=1
```

11. Drive strength settings:

    This final section selects the I/O standard to be simulated, selects the termination scheme to be used, and allows the simulation with other I/O standards and settings by using .alter syntax.

```
* 3.3V LVTTL 4ma
.lib '../../lib/drive_select_VIO.lib' p_33ttl_4ma
.lib '../../lib/IO_load.lib' ttl
.param vcn = 3.3
.param vc  = 1.2
```

# 11 Appendix

**Table 7: Library Calls for Valid VIO Drive Strengths within "drive_select_VIO.lib"**

| Vertical I/O | Valid Drive Strength | Library Call |
|---|---|---|
| 1.2V LVCMOS | 2mA | p_12_2ma |
| 1.2V LVCMOS | 4mA | p_12_4ma |
| 1.2V LVCMOS | 6mA | p_12_6ma |
| 1.2V LVCMOS | 8mA | p_12_8ma |
| 1.2V LVCMOS | 10mA | p_12_10ma |
| 1.2V LVCMOS | 12mA | p_12_12ma |
| 1.5V LVCMOS | 2mA | p_15_2ma |
| 1.5V LVCMOS | 4mA | p_15_4ma |
| 1.5V LVCMOS | 6mA | p_15_6ma |
| 1.5V LVCMOS | 8mA | p_15_8ma |
| 1.5V LVCMOS | 10mA | p_15_10ma |
| 1.5V LVCMOS | 12mA | p_15_12ma |
| 1.5V LVCMOS | 16mA | p_15_16ma |
| 1.8V LVTTL/LVCMOS | 2mA | p_18_2ma |
| 1.8V LVTTL/LVCMOS | 4mA | p_18_4ma |
| 1.8V LVTTL/LVCMOS | 6mA | p_18_6ma |
| 1.8V LVTTL/LVCMOS | 8mA | p_18_8ma |
| 1.8V LVTTL/LVCMOS | 10mA | p_18_10ma |
| 1.8V LVTTL/LVCMOS | 12mA | p_18_12ma |
| 1.8V LVTTL/LVCMOS | 16mA | p_18_16ma |
| 2.5V LVTTL/LVCMOS | 4mA | p_25_4ma |
| 2.5V LVTTL/LVCMOS | 8mA | p_25_8ma |
| 2.5V LVTTL/LVCMOS | 12mA | p_25_12ma |
| 2.5V LVTTL/LVCMOS | 16mA | p_25_16ma |
| 3.0V LVTTL | 4mA | p_30ttl_4ma |
| 3.0V LVTTL | 8mA | p_30ttl_8ma |
| 3.0V LVTTL | 12mA | p_30ttl_12ma |
| 3.0V LVTTL | 16mA | p_30ttl_16ma |
| 3.0V LVCMOS | 4mA | p_30cmos_4ma |
| 3.0V LVCMOS | 8mA | p_30cmos_8ma |
| 3.0V LVCMOS | 12mA | p_30cmos_12ma |
| 3.0V LVCMOS | 16mA | p_30cmos_16ma |
| 3.3V LVTTL | 4mA | p_33ttl_4ma |
| 3.3V LVTTL | 8mA | p_33ttl_8ma |
| 3.3V LVCMOS | 2mA | p_33cmos_2ma |
| 3.0V PCI | | p_pci |
| HSTL12 Class I | 8mA | p_hstl12_8ma |
| HSTL12 Class I | 10mA | p_hstl12_10ma |
| HSTL12 Class I | 12mA | p_hstl12_12ma |
| HSTL12 Class II | 14mA | p_hstl12_14ma |
| HSTL15 Class I | 8mA | p_hstl15_8ma |
| HSTL15 Class I | 10mA | p_hstl15_10ma |
| HSTL15 Class I | 12mA | p_hstl15_12ma |
| HSTL15 Class II | 16mA | p_hstl15_16ma |
| HSTL18 Class I | 8mA | p_hstl18_8ma |
| HSTL18 Class I | 10mA | p_hstl18_10ma |
| HSTL18 Class I | 12mA | p_hstl18_12ma |
| HSTL18 Class II | 16mA | p_hstl18_16ma |

| | | |
|---|---|---|
| SSTL18 Class I | 8mA | p_sstl18c1_8ma |
| SSTL18 Class I | 10mA | p_sstl18c1_10ma |
| SSTL18 Class I | 12mA | p_sstl18c1_12ma |
| SSTL18 Class II | 12mA | p_sstl18c2_12ma |
| SSTL18 Class II | 16mA | p_sstl18c2_16ma |
| SSTL2 Class I | 8mA | p_sstl2c1_8ma |
| SSTL2 Class I | 12mA | p_sstl2c1_12ma |
| SSTL2 Class II | 16mA | p_sstl2c2_16ma |
| 1.2V 25 Ohm OCT-Rs | | p_12_oct_25 |
| 1.2V 50 Ohm OCT-Rs | | p_12_oct_50 |
| 1.5V 25 Ohm OCT-Rs | | p_15_oct_25 |
| 1.5V 50 Ohm OCT-Rs | | p_15_oct_50 |
| 1.8V 25 Ohm OCT-Rs | | p_18_oct_25 |
| 1.8V 50 Ohm OCT-Rs | | p_18_oct_50 |
| 2.5V 25 Ohm OCT-Rs | | p_25_oct_25 |
| 2.5V 50 Ohm OCT-Rs | | p_25_oct_50 |
| 3.0V 25 Ohm OCT-Rs | | p_30_oct_25 |
| 3.0V 50 Ohm OCT-Rs | | p_30_oct_50 |
| 3 External Resistor LVDS, Mini-LVDS, RSDS | | p_diff_3_resistor |

### Table 8: Library Calls for Valid HIO Drive Strengths within “drive_select_HIO.lib”

| Vertical I/O | Valid Drive Strength | Library Call |
|---|---|---|
| 1.2V LVCMOS | 2mA | p_12_2ma |
| 1.2V LVCMOS | 4mA | p_12_4ma |
| 1.2V LVCMOS | 6mA | p_12_6ma |
| 1.2V LVCMOS | 8mA | p_12_8ma |
| 1.2V LVCMOS | 10mA | p_12_10ma |
| 1.5V LVCMOS | 2mA | p_15_2ma |
| 1.5V LVCMOS | 4mA | p_15_4ma |
| 1.5V LVCMOS | 6mA | p_15_6ma |
| 1.5V LVCMOS | 8mA | p_15_8ma |
| 1.5V LVCMOS | 10mA | p_15_10ma |
| 1.5V LVCMOS | 12mA | p_15_12ma |
| 1.5V LVCMOS | 16mA | p_15_16ma |
| 1.8V LVTTL/LVCMOS | 2mA | p_18_2ma |
| 1.8V LVTTL/LVCMOS | 4mA | p_18_4ma |
| 1.8V LVTTL/LVCMOS | 6mA | p_18_6ma |
| 1.8V LVTTL/LVCMOS | 8mA | p_18_8ma |
| 1.8V LVTTL/LVCMOS | 10mA | p_18_10ma |
| 1.8V LVTTL/LVCMOS | 12mA | p_18_12ma |
| 1.8V LVTTL/LVCMOS | 16mA | p_18_16ma |
| 2.5V LVTTL/LVCMOS | 4mA | p_25_4ma |
| 2.5V LVTTL/LVCMOS | 8mA | p_25_8ma |
| 2.5V LVTTL/LVCMOS | 12mA | p_25_12ma |
| 2.5V LVTTL/LVCMOS | 16mA | p_25_16ma |
| 3.0V LVTTL | 4mA | p_30ttl_4ma |
| 3.0V LVTTL | 8mA | p_30ttl_8ma |
| 3.0V LVTTL | 12mA | p_30ttl_12ma |
| 3.0V LVTTL | 16mA | p_30ttl_16ma |
| 3.0V LVCMOS | 4mA | p_30cmos_4ma |
| 3.0V LVCMOS | 8mA | p_30cmos_8ma |
| 3.0V LVCMOS | 12mA | p_30cmos_12ma |
| 3.0V LVCMOS | 16mA | p_30cmos_16ma |
| 3.3V LVTTL | 4mA | p_33ttl_4ma |
| 3.3V LVTTL | 8mA | p_33ttl_8ma |
| 3.3V LVCMOS | 2mA | p_33cmos_2ma |
| 3.0V PCI |  | p_pci |
| HSTL12 Class I | 8mA | p_hstl12_8ma |
| HSTL12 Class I | 10mA | p_hstl12_10ma |
| HSTL15 Class I | 8mA | p_hstl15_8ma |
| HSTL15 Class I | 10mA | p_hstl15_10ma |
| HSTL15 Class I | 12mA | p_hstl15_12ma |
| HSTL15 Class II | 16mA | p_hstl15_16ma |
| HSTL18 Class I | 8mA | p_hstl18_8ma |
| HSTL18 Class I | 10mA | p_hstl18_10ma |
| HSTL18 Class I | 12mA | p_hstl18_12ma |
| HSTL18 Class II | 16mA | p_hstl18_16ma |
| SSTL18 Class I | 8mA | p_sstl18c1_8ma |
| SSTL18 Class I | 10mA | p_sstl18c1_10ma |
| SSTL18 Class I | 12mA | p_sstl18c1_12ma |
| SSTL18 Class II | 12mA | p_sstl18c2_12ma |
| SSTL18 Class II | 16mA | p_sstl18c2_16ma |
| SSTL2 Class I | 8mA | p_sstl2c1_8ma |

| | | |
|---|---|---|
| SSTL2 Class I | 12mA | p_sstl2c1_12ma |
| SSTL2 Class II | 16mA | p_sstl2c2_16ma |
| 1.2V 50 Ohm OCT-Rs | | p_12_oct_50 |
| 1.5V 25 Ohm OCT-Rs | | p_15_oct_25 |
| 1.5V 50 Ohm OCT-Rs | | p_15_oct_50 |
| 1.8V 25 Ohm OCT-Rs | | p_18_oct_25 |
| 1.8V 50 Ohm OCT-Rs | | p_18_oct_50 |
| 2.5V 25 Ohm OCT-Rs | | p_25_oct_25 |
| 2.5V 50 Ohm OCT-Rs | | p_25_oct_50 |
| 3.0V 25 Ohm OCT-Rs | | p_30_oct_25 |
| 3.0V 50 Ohm OCT-Rs | | p_30_oct_50 |
| 3 External Resistor LVDS, Mini-LVDS, RSDS | | p_diff_3_resistor |

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