

## FEATURES

- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit analog-to-digital converter (ADC), 4× oversampling per channel for CVBS, Y/C, and YPrPb modes
- 6 analog video input channels with on-chip antialiasing filter
- Video input support for CVBS (composite), Y/C (S-Video), and YPrPb (component)
- Fully differential, pseudo differential, and single-ended CVBS video input support
- NTSC/PAL/SECAM autodetection
- Short-to-battery (STB) diagnostics on 2 video inputs
- Up to 4 V common-mode input range solution
- Excellent common-mode noise rejection capabilities
- 5-line adaptive 2D comb filter and CTI video enhancement
- Adaptive Digital Line Length Tracking (ADLLT), signal processing, and enhanced FIFO management provide mini-time base correction (TBC) functionality
- Integrated automatic gain control (AGC) with adaptive peak white mode
- Fast switching capability
- Integrated interlaced-to-progressive (I2P) video output converter
- Adaptive contrast enhancement (ACE)
- Down dither (8-bit to 6-bit)
- Rovi (Macrovision) copy protection detection
- MIPI CSI-2 output interface
- Full featured vertical blanking interval (VBI) data slicer with world system teletext (WST) support

Power-down mode available

2-wire, I<sup>2</sup>C-compatible serial interface

Qualified for automotive applications

–40°C to +105°C temperature grade

32-lead, 5 mm × 5 mm, RoHS-compliant LFCSP

## APPLICATIONS

Smartphone/multimedia handsets

Automotive infotainment

DVRs for video security

Media players

## GENERAL DESCRIPTION

The **ADV7282-M** is a versatile one-chip, multiformat video decoder. The **ADV7282-M** automatically detects standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards in the form of composite, S-Video, and component video. The **ADV7282-M** converts these signals into an 8-bit YCrCb 4:2:2 video data stream that is output over a mobile industry processor interface (MIPI®) CSI-2 interface.

The analog video inputs of the **ADV7282-M** accept single-ended, pseudo differential, and fully differential signals. The **ADV7282-M** supports I2P conversion and provides six analog inputs, two STB diagnostic pins, and three general-purpose outputs.

The **ADV7282-M** is programmed via a 2-wire, serial bidirectional port (I<sup>2</sup>C compatible) and is fabricated in a 1.8 V CMOS process. The LFCSP package option makes the decoder ideal for space-constrained portable applications.

## FUNCTIONAL BLOCK DIAGRAM

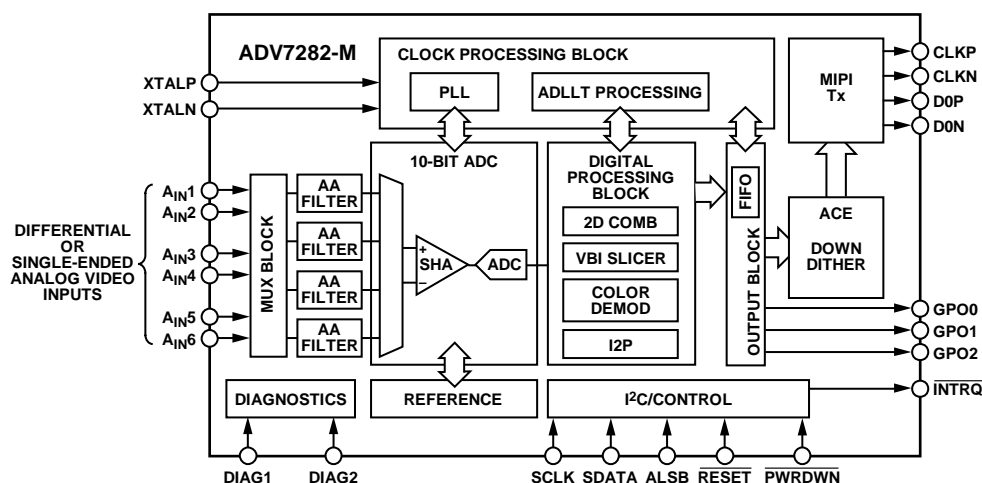


Figure 1.

Rev. 0

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## REVISION HISTORY

8/13—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL SPECIFICATIONS

$A_{VDD}$ ,  $D_{VDD}$ ,  $P_{VDD}$ , and  $M_{VDD}$  = 1.71 V to 1.89 V,  $D_{VDDIO}$  = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
ADC Resolution	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		±0.6		LSB
DIGITAL INPUTS						
Input High Voltage	$V_{IH}$	$D_{VDDIO} = 3.3\text{ V}$	2			V
Input Low Voltage	$V_{IL}$	$D_{VDDIO} = 3.3\text{ V}$			0.8	V
Input Leakage Current	$I_{IN}$	$\overline{\text{RESET}}$ pin	–10		+10	μA
		$\overline{\text{SDATA}}$ , $\overline{\text{SCLK}}$ pins	–10		+15	μA
		$\overline{\text{PWRDWN}}$ , ALSB pins	–10		+50	μA
Input Capacitance	$C_{IN}$				10	pF
CRYSTAL INPUT						
Input High Voltage	$V_{IH}$	XTALN pin	1.2			V
Input Low Voltage	$V_{IL}$	XTALN pin			0.4	V
DIGITAL OUTPUTS						
Output High Voltage	$V_{OH}$	$D_{VDDIO} = 3.3\text{ V}$ , $I_{SOURCE} = 0.4\text{ mA}$	2.4			V
Output Low Voltage	$V_{OL}$	$D_{VDDIO} = 3.3\text{ V}$ , $I_{SINK} = 3.2\text{ mA}$			0.4	V
High Impedance Leakage Current	$I_{LEAK}$				10	μA
Output Capacitance	$C_{OUT}$				20	pF
POWER REQUIREMENTS <sup>1, 2, 3</sup>						
Digital I/O Power Supply	$D_{VDDIO}$		2.97	3.3	3.63	V
PLL Power Supply	$P_{VDD}$		1.71	1.8	1.89	V
Analog Power Supply	$A_{VDD}$		1.71	1.8	1.89	V
Digital Power Supply	$D_{VDD}$		1.71	1.8	1.89	V
MIPI Tx Power Supply	$M_{VDD}$		1.71	1.8	1.89	V
Digital I/O Supply Current	$I_{DVDDIO}$			1.5		mA
PLL Supply Current	$I_{PVDD}$			12		mA
MIPI Tx Supply Current	$I_{MVDD}$			14		mA
Analog Supply Current	$I_{AVDD}$					
Single-Ended CVBS Input				35		mA
Differential CVBS Input		Fully differential and pseudo differential CVBS		69		mA
Y/C Input				60		mA
YPrPb Input				75		mA
Digital Supply Current	$I_{DVDD}$					
Single-Ended CVBS Input				70		mA
Differential CVBS Input		Fully differential and pseudo differential CVBS		70		mA
Y/C Input				70		mA
YPrPb Input				70		mA
POWER-DOWN CURRENTS <sup>1</sup>						
Digital I/O Supply Power-Down Current	$I_{DVDDIO\_PD}$			73		μA
PLL Supply Power-Down Current	$I_{PVDD\_PD}$			46		μA
Analog Supply Power-Down Current	$I_{AVDD\_PD}$			0.2		μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Digital Supply Power-Down Current	I <sub>DVDD_PD</sub>			420		μA
MIPI Tx Supply Power-Down Current	I <sub>MVDD_PD</sub>			4.5		μA
Total Power Dissipation in Power-Down Mode				1		mW

<sup>1</sup> Guaranteed by characterization.

<sup>2</sup> Typical current consumption values are measured with nominal voltage supply levels and an SMPTE bar test pattern.

<sup>3</sup> All specifications apply when the I2P core is activated, unless otherwise stated.

## VIDEO SPECIFICATIONS

A<sub>VDD</sub>, D<sub>VDD</sub>, P<sub>VDD</sub>, and M<sub>VDD</sub> = 1.71 V to 1.89 V, D<sub>VDDIO</sub> = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS <sup>1</sup>						
Differential Phase	DP	CVBS input, modulated 5-step		0.9		Degrees
Differential Gain	DG	CVBS input, modulated 5-step		0.5		%
Luma Nonlinearity	LNL	CVBS input, 5-step		2.0		%
NOISE SPECIFICATIONS						
Signal-to-Noise Ratio, Unweighted	SNR	Luma ramp		57.1		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
Common-Mode Rejection Ratio <sup>2</sup>	CMRR			73		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			–5		+5	%
Vertical Lock Range			40		70	Hz
f <sub>SC</sub> Subcarrier Lock Range				±1.3		kHz
Color Lock-In Time				60		Lines
Synchronization Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed <sup>3</sup>				100		Lines
Fast Switch Speed <sup>4</sup>				100		ms
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy				1		%

<sup>1</sup> These specifications apply for all CVBS input types (NTSC, PAL, and SECAM), as well as for single-ended and differential CVBS inputs.

<sup>2</sup> The CMRR of this circuit design is critically dependent on the external resistor matching on the circuit inputs (see the Input Networks section). The CMRR measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.

<sup>3</sup> Autodetection switch speed is the time required for the [ADV7282-M](#) to detect which video format is present at its input, for example, PAL I or NTSC M.

<sup>4</sup> Fast switch speed is the time required for the [ADV7282-M](#) to switch from one analog input (single-ended or differential) to another, for example, switching from A<sub>IN1</sub> to A<sub>IN2</sub>.

## MIPI VIDEO OUTPUT SPECIFICATIONS

$A_{VDD}$ ,  $D_{VDD}$ ,  $P_{VDD}$ , and  $M_{VDD}$  = 1.71 V to 1.89 V,  $D_{VDDIO}$  = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. The CSI-2 clock lane of the **ADV7282-M** remains in high speed (HS) mode even when the data lane enters low power (LP) mode. For this reason, some measurements on the clock lane that pertain to low power mode are not applicable. Unless otherwise stated, all high speed measurements were performed with the **ADV7282-M** operating in progressive mode and with a nominal 432 Mbps output data rate. Specifications guaranteed by characterization.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
UNIT INTERVAL	UI					
Interlaced Output				4.63		ns
Progressive Output				2.31		ns
DATA LANE LP TX DC SPECIFICATIONS <sup>1</sup>						
Thevenin Output High Level	$V_{OH}$		1.1	1.2	1.3	V
Thevenin Output Low Level	$V_{OL}$		-50	0	+50	mV
DATA LANE LP TX AC SPECIFICATIONS <sup>1</sup>						
Rise Time, 15% to 85%					25	ns
Fall Time, 85% to 15%					25	ns
Rise Time, 30% to 85%					35	ns
Data Lane LP Slew Rate vs. $C_{LOAD}$						
Maximum Slew Rate over Entire Vertical Edge Region		Rising edge			150	mV/ns
		Falling edge			150	mV/ns
Minimum Slew Rate						
400 mV $\leq V_{OUT} \leq$ 930 mV		Falling edge	30			mV/ns
400 mV $\leq V_{OUT} \leq$ 700 mV		Rising edge	30			mV/ns
700 mV $\leq V_{OUT} \leq$ 930 mV		Rising edge	>0			mV/ns
Pulse Width of LP Exclusive-OR Clock		First clock pulse after stop state or last pulse before stop state	40			ns
		All other clock pulses	20			ns
Period of LP Exclusive-OR Clock			90			ns
CLOCK LANE LP TX DC SPECIFICATIONS <sup>1</sup>						
Thevenin Output High Level	$V_{OH}$		1.1	1.2	1.3	V
Thevenin Output Low Level	$V_{OL}$		-50	0	+50	mV
CLOCK LANE LP TX AC SPECIFICATIONS <sup>1</sup>						
Rise Time, 15% to 85%					25	ns
Fall Time, 85% to 15%					25	ns
Clock Lane LP Slew Rate						
Maximum Slew Rate over Entire Vertical Edge Region		Rising edge			150	mV/ns
		Falling edge			150	mV/ns
Minimum Slew Rate						
400 mV $\leq V_{OUT} \leq$ 930 mV		Falling edge	30			mV/ns
400 mV $\leq V_{OUT} \leq$ 700 mV		Rising edge	30			mV/ns
700 mV $\leq V_{OUT} \leq$ 930 mV		Rising edge	>0			mV/ns
DATA LANE HS TX SIGNALING REQUIREMENTS		See Figure 2				
Low Power to High Speed Transition Stage	$t_9$	Time that the D0P pin is at $V_{OL}$ and the D0N pin is at $V_{OH}$	50			ns
	$t_{10}$	Time that the D0P and D0N pins are at $V_{OL}$	40 + (4 $\times$ UI)		85 + (6 $\times$ UI)	ns
	$t_{11}$	$t_{10}$ plus the HS-zero period	145 + (10 $\times$ UI)			ns
High Speed Differential Voltage Swing	$ V_i $		140	200	270	mV p-p
Differential Voltage Mismatch					10	mV
Single-Ended Output High Voltages					360	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Static Common-Mode Voltage Level	t <sub>12</sub>	Time that the <a href="#">ADV7282-M</a> drives the flipped last data bit after sending the last payload data bit of an HS transmission burst	150	200	250	mV
Static Common-Mode Voltage Mismatch					5	mV
Dynamic Common Level Variations					25	mV
50 MHz to 450 MHz					15	mV
Above 450 MHz					0.3 × UI	ns
Rise Time, 20% to 80%			0.15		0.3 × UI	ns
Fall Time, 80% to 20%			0.15		0.3 × UI	ns
High Speed to Low Power Transition Stage			60 + (4 × UI)			ns
					35	ns
					105 + (12 × UI)	ns
	t <sub>13</sub>	Post-end-of-transmission rise time (30% to 85%)				ns
	t <sub>14</sub>	Time from start of t <sub>12</sub> to start of low power state following an HS transmission burst				ns
	t <sub>15</sub>	Time that a low power state is transmitted after an HS transmission burst			100	ns
CLOCK LANE HS TX SIGNALING REQUIREMENTS	t <sub>9</sub>	See Figure 2				
Low Power to High Speed Transition Stage <sup>2</sup>		Time that the CLKP pin is at V <sub>OL</sub> and the CLKN pin is at V <sub>OH</sub>	50			ns
		Time that the CLKP and CLKN pins are at V <sub>OL</sub>	38		95	ns
		Clock HS-zero period	300	500		ns
High Speed Differential Voltage Swing			140	200	270	mV p-p
Differential Voltage Mismatch					10	mV
Single-Ended Output High Voltages					360	mV
Static Common-Mode Voltage Level			150	200	250	mV
Static Common-Mode Voltage Mismatch					5	mV
Dynamic Common Level Variations					25	mV
50 MHz to 450 MHz	V <sub>2</sub>				15	mV
Above 450 MHz					0.3 × UI	ns
Rise Time, 20% to 80%			0.15		0.3 × UI	ns
Fall Time, 80% to 20%			0.15		0.3 × UI	ns
HS TX CLOCK TO DATA LANE TIMING REQUIREMENTS						
Data to Clock Skew						
			0.35 × UI		0.65 × UI	ns

<sup>1</sup> These measurements were performed with C<sub>LOAD</sub> = 50 pF.

<sup>2</sup> The clock lane remains in high speed mode throughout normal operation. These results apply only to the [ADV7282-M](#) during startup.

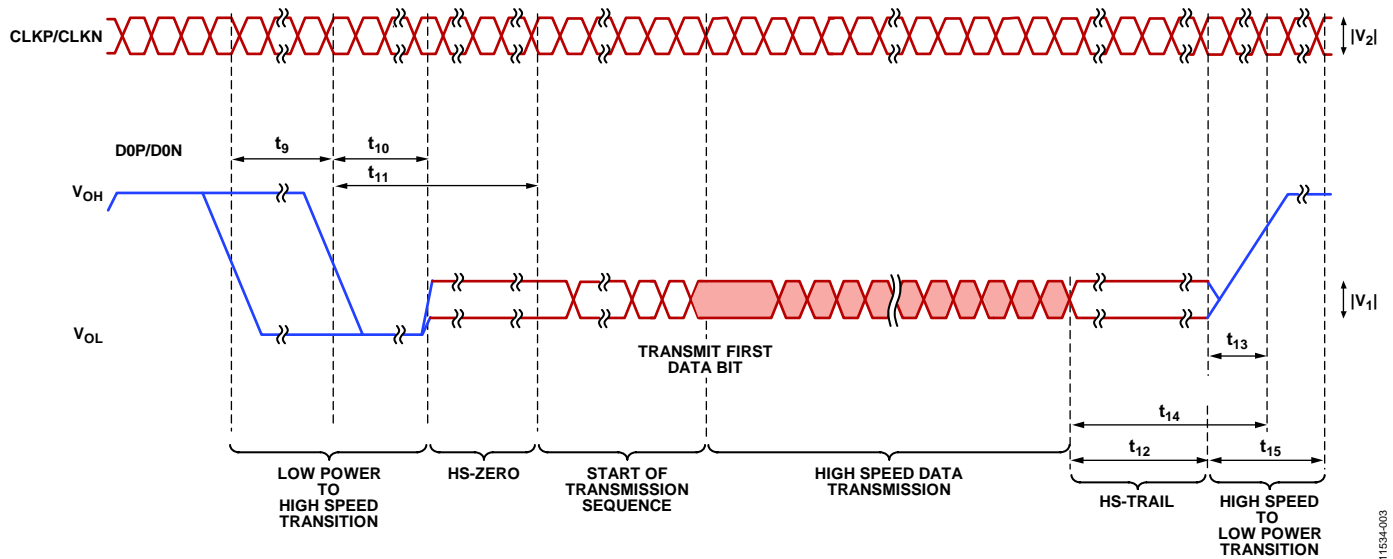


Figure 2. ADV7282-M Output Timing Diagram (Conforms with MIPI CSI-2 Specification)

## ANALOG SPECIFICATIONS

$A_{VDD}$ ,  $D_{VDD}$ ,  $P_{VDD}$ , and  $M_{VDD}$  = 1.71 V to 1.89 V,  $D_{VDDIO}$  = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 4.

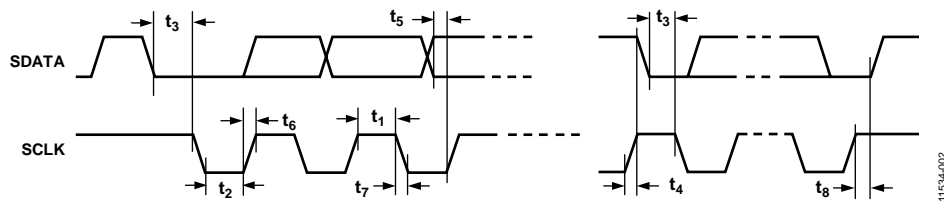
Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor	Clamps switched off		0.1		$\mu\text{F}$
Input Impedance			10		$\text{M}\Omega$
Large Clamp Source Current			0.4		$\text{mA}$
Large Clamp Sink Current			0.4		$\text{mA}$
Fine Clamp Source Current			10		$\mu\text{A}$
Fine Clamp Sink Current			10		$\mu\text{A}$

**CLOCK AND I<sup>2</sup>C TIMING SPECIFICATIONS**

$A_{VDD}$ ,  $D_{VDD}$ ,  $P_{VDD}$ , and  $M_{VDD}$  = 1.71 V to 1.89 V,  $D_{VDDIO}$  = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

**Table 5.**

Parameter	Symbol	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL					
Nominal Frequency			28.63636		MHz
Frequency Stability				±50	ppm
I <sup>2</sup> C PORT					
SCLK Frequency				400	kHz
SCLK Minimum Pulse Width High	$t_1$	0.6			μs
SCLK Minimum Pulse Width Low	$t_2$	1.3			μs
Hold Time (Start Condition)	$t_3$	0.6			μs
Setup Time (Start Condition)	$t_4$	0.6			μs
SDATA Setup Time	$t_5$	100			ns
SCLK and SDATA Rise Times	$t_6$			300	ns
SCLK and SDATA Fall Times	$t_7$			300	ns
Setup Time (Stop Condition)	$t_8$		0.6		μs
RESET INPUT					
RESET Pulse Width		5			ms

Figure 3. I<sup>2</sup>C Timing Diagram

11534-002



## ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
$A_{VDD}$ to DGND	2.2 V
$D_{VDD}$ to DGND	2.2 V
$P_{VDD}$ to DGND	2.2 V
$M_{VDD}$ to DGND	2.2 V
$D_{VDDIO}$ to DGND	4 V
$P_{VDD}$ to $D_{VDD}$	−0.9 V to +0.9 V
$M_{VDD}$ to $D_{VDD}$	−0.9 V to +0.9 V
$A_{VDD}$ to $D_{VDD}$	−0.9 V to +0.9 V
Digital Inputs Voltage	DGND − 0.3 V to $D_{VDDIO} + 0.3$ V
Digital Outputs Voltage	DGND − 0.3 V to $D_{VDDIO} + 0.3$ V
Analog Inputs to Ground	Ground − 0.3 V to $A_{VDD} + 0.3$ V
Maximum Junction Temperature ( $T_J$ max)	140°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions must be taken for handling and assembly.

## THERMAL RESISTANCE

The thermal resistance values in Table 7 are specified for the device soldered onto a 4-layer printed circuit board (PCB) with a common ground plane and with the exposed pad of the device connected to DGND. The values in Table 7 are maximum values.

Table 7. Thermal Resistance for the 32-Lead LFCSP

Thermal Characteristic	Symbol	Value	Unit
Junction-to-Ambient Thermal Resistance (Still Air)	$\theta_{JA}$	32.5	°C/W
Junction-to-Case Thermal Resistance	$\theta_{JC}$	2.3	°C/W

## REFLOW SOLDER

The [ADV7282-M](#) is a Pb-free, environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications and can withstand surface-mount soldering at up to 255°C (±5°C).

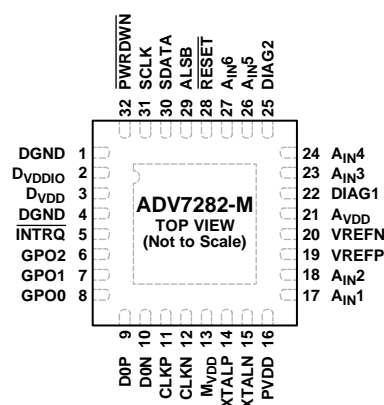
In addition, the [ADV7282-M](#) is backward-compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. THE EXPOSED PAD MUST BE CONNECTED TO DGND.

11934-004

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	DVDDIO	Power	Digital I/O Power Supply (3.3 V).
3	DVDD	Power	Digital Power Supply (1.8 V).
5	INTRQ	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
6 to 8	GPO2 to GPO0	Output	General-Purpose Outputs. These pins can be configured via I <sup>2</sup> C to allow control of external devices.
9	D0P	Output	Positive MIPI Differential Data Output.
10	D0N	Output	Negative MIPI Differential Data Output.
11	CLKP	Output	Positive MIPI Differential Clock Output.
12	CLKN	Output	Negative MIPI Differential Clock Output.
13	MvDD	Power	MIPI Digital Power Supply (1.8 V).
14	XTALP	Output	Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the <b>ADV7282-M</b> . The crystal used with the <b>ADV7282-M</b> must be a fundamental crystal.
15	XTALN	Input	Input Pin for the External 28.63636 MHz Crystal. The crystal used with the <b>ADV7282-M</b> must be a fundamental crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the <b>ADV7282-M</b> , the output of the oscillator is fed into the XTALN pin.
16	PVDD	Power	PLL Power Supply (1.8 V).
17, 18, 23, 24, 26, 27	AIN1 to AIN6	Input	Analog Video Input Channels.
19	VREFP	Output	Internal Voltage Reference Output.
20	VREFN	Output	Internal Voltage Reference Output.
21	AVDD	Power	Analog Power Supply (1.8 V).
22	DIAG1	Input	Diagnostic Input 1.
25	DIAG2	Input	Diagnostic Input 2.
28	RESET	Input	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the <b>ADV7282-M</b> circuitry.
29	ALSB	Input	This pin selects the I <sup>2</sup> C write address for the <b>ADV7282-M</b> . When ALSB is set to Logic 0, the write address is 0x40; when ALSB is set to Logic 1, the write address is 0x42.
30	SDATA	Input/output	I <sup>2</sup> C Port Serial Data Input/Output.
31	SCLK	Input	I <sup>2</sup> C Port Serial Clock Input. The maximum clock rate is 400 kHz.
32	PWRDWN	Input	Power-Down Pin. A logic low on this pin places the <b>ADV7282-M</b> in power-down mode.
	EPAD (EP)		Exposed Pad. The exposed pad must be connected to DGND.

## THEORY OF OPERATION

The **ADV7282-M** is a versatile one-chip, multiformat video decoder. The **ADV7282-M** automatically detects standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards in the form of composite, S-Video, and component video. The **ADV7282-M** converts these signals into an 8-bit YCrCb 4:2:2 video data stream that is output over a MIPI CSI-2 interface.

The MIPI CSI-2 output interface connects to a wide range of video processors and FPGAs. The accurate 10-bit analog-to-digital conversion provides professional quality video performance for consumer applications with true 8-bit data resolution.

The six analog video inputs of the **ADV7282-M** accept single-ended, pseudo differential, and fully differential composite video signals, as well as S-Video and YPrPb video signals, supporting a wide range of consumer and automotive video sources.

In differential CVBS mode, the **ADV7282-M**, along with an external resistor divider, provides a common-mode input range of up to 4 V, enabling the removal of large signal, common-mode transients present on the video lines.

The advanced interlaced-to-progressive (I2P) function allows the **ADV7282-M** to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The **ADV7282-M** uses edge adaptive technology to minimize video defects on low angle lines.

The automatic gain control (AGC) and clamp restore circuitry allows an input video signal peak-to-peak range of 0 V to 1.0 V at the analog video input pins of the **ADV7282-M**. Alternatively, the AGC and clamp restore circuitry can be bypassed for manual settings.

AC coupling of the input video signals provides short-to-battery (STB) protection. STB diagnostics can be performed on two input video signals.

The **ADV7282-M** supports a number of other functions, including 8-bit to 6-bit down dither mode and adaptive contrast enhancement (ACE).

The **ADV7282-M** is programmed via a 2-wire, serial bidirectional port (I<sup>2</sup>C compatible) and is fabricated in a 1.8 V CMOS process. The monolithic CMOS construction of the **ADV7282-M** ensures greater functionality with lower power dissipation. The LFCSP package option makes the decoder ideal for space-constrained portable applications.

## ANALOG FRONT END (AFE)

The analog front end (AFE) of the **ADV7282-M** comprises a single high speed, 10-bit ADC that digitizes the analog video signal before applying it to the standard definition processor (SDP). The AFE uses differential channels to the ADC to ensure high performance in mixed-signal applications and to enable differential CVBS inputs to be connected directly to the **ADV7282-M**.

The AFE also includes an input mux that enables multiple video signals to be applied to the **ADV7282-M**. The input mux allows up to six composite video signals to be applied to the **ADV7282-M**.

Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter.

A resistor divider network is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see the Input Networks section). Fine clamping of the video signal is performed downstream by digital fine clamping within the **ADV7282-M**.

Table 9 lists the three ADC clock rates that are determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, Y/C, and YPrPb modes.

**Table 9. ADC Clock Rates**

Input Format	ADC Clock Rate (MHz) <sup>1</sup>	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video)	114	4×
YPrPb	172	4×

<sup>1</sup> Based on a 28.63636 MHz crystal between the XTALP and XTALN pins.

The fully differential AFE of the **ADV7282-M** provides inherent small and large signal noise rejection, improved electromagnetic interference (EMI) protection, and the ability to absorb ground bounce. Support is provided for both true differential and pseudo differential signals.

## STANDARD DEFINITION PROCESSOR (SDP)

The [ADV7282-M](#) is capable of decoding a large selection of baseband video signals in composite (both single-ended and differential), S-Video, and component formats. The video standards supported by the video processor include

- PAL B, PAL D, PAL G, PAL H, PAL I, PAL M, PAL N, PAL Nc, PAL 60
- NTSC J, NTSC M, NTSC 4.43
- SECAM B, SECAM D, SECAM G, SECAM K, SECAM L

Using the standard definition processor (SDP), the [ADV7282-M](#) can automatically detect the video standard and process it accordingly.

The [ADV7282-M](#) has a five-line adaptive 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the [ADV7282-M](#).

The [ADV7282-M](#) implements the patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as VCRs. ADLLT enables the [ADV7282-M](#) to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs and camcorders.

The [ADV7282-M](#) contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

Adaptive contrast enhancement (ACE) offers improved visual detail using an algorithm that automatically varies contrast levels to enhance picture detail. ACE increases the contrast in dark areas of an image without saturating the bright areas of the image. This feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

Down dithering converts the output of the [ADV7282-M](#) from an 8-bit to a 6-bit output, enabling ease of design for standard LCD panels.

The I2P block converts the interlaced video input into a progressive video output without the need for external memory.

The SDP can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), and teletext data slicing for world system teletext (WST). VBI data is transmitted via the MIPI CSI-2 link as ancillary data packets.

The [ADV7282-M](#) is fully Rovi® (Macrovision®) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

## POWER SUPPLY SEQUENCING

### OPTIMAL POWER-UP SEQUENCE

The optimal power-up sequence for the [ADV7282-M](#) is to first power up the 3.3 V  $D_{VDDIO}$  supply, followed by the 1.8 V supplies ( $D_{VDD}$ ,  $P_{VDD}$ ,  $A_{VDD}$ , and  $M_{VDD}$ ).

When powering up the [ADV7282-M](#), follow these steps. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

1. Assert the  $\overline{PWRDWN}$  and  $\overline{RESET}$  pins (pull the pins low).
2. Power up the  $D_{VDDIO}$  supply.
3. After  $D_{VDDIO}$  is fully asserted, power up the 1.8 V supplies.
4. After the 1.8 V supplies are fully asserted, pull the  $\overline{PWRDWN}$  pin high.
5. Wait 5 ms and then pull the  $\overline{RESET}$  pin high.
6. After all power supplies and the  $\overline{PWRDWN}$  and  $\overline{RESET}$  pins are powered up and stable, wait an additional 5 ms before initiating I<sup>2</sup>C communication with the [ADV7282-M](#).

### SIMPLIFIED POWER-UP SEQUENCE

Alternatively, the [ADV7282-M](#) can be powered up by asserting all supplies and the  $\overline{PWRDWN}$  and  $\overline{RESET}$  pins simultaneously. After this operation, perform a software reset, then wait 10 ms before initiating I<sup>2</sup>C communication with the [ADV7282-M](#).

While the supplies are being established, care must be taken to ensure that a lower rated supply does not go above a higher rated supply level. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

### POWER-DOWN SEQUENCE

The [ADV7282-M](#) supplies can be deasserted simultaneously as long as  $D_{VDDIO}$  does not go below a lower rated supply.

### $D_{VDDIO}$ SUPPLY VOLTAGE

For correct operation of the [ADV7282-M](#), the  $D_{VDDIO}$  supply must be from 2.97 V to 3.63 V.

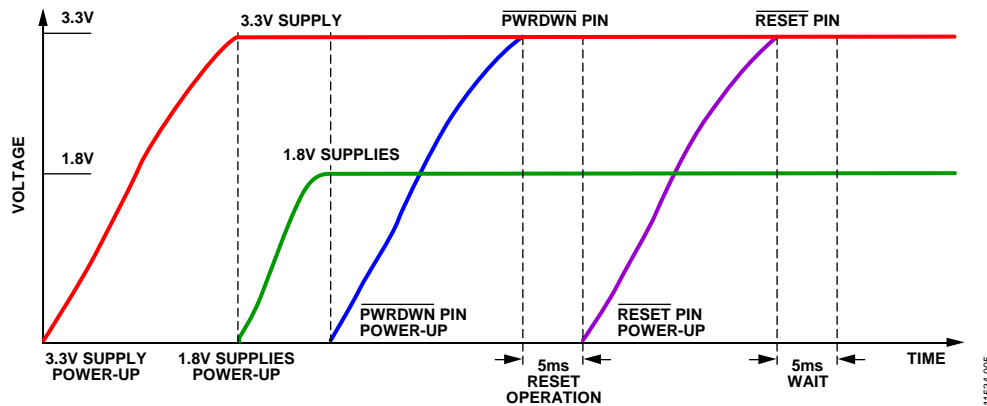


Figure 5. Optimal Power-Up Sequence

## INPUT NETWORKS

An input network (external resistor and capacitor circuit) is required on the  $A_{INX}$  input pins of the [ADV7282-M](#). The components of the input network depend on the video format selected for the analog input.

### SINGLE-ENDED INPUT NETWORK

Figure 6 shows the input network to use on each  $A_{INX}$  input pin of the [ADV7282-M](#) when any of the following video input formats is used:

- Single-ended CVBS
- YC (S-Video)
- YPrPb

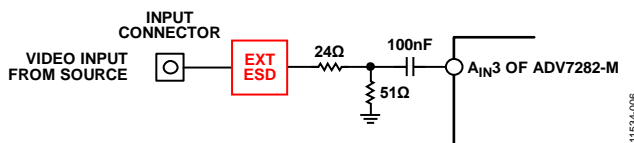


Figure 6. Single-Ended Input Network

The 24  $\Omega$  and 51  $\Omega$  resistors supply the 75  $\Omega$  end termination required for the analog video input. These resistors also create a resistor divider with a gain of 0.68. The resistor divider attenuates the amplitude of the input analog video and scales the input to the ADC range of the [ADV7282-M](#). This allows an input range to the [ADV7282-M](#) of up to 1.47 V p-p. Note that amplifiers within the ADC restore the amplitude of the input signal so that signal-to-noise ratio (SNR) performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the  $A_{INX}$  pin of the [ADV7282-M](#). The clamping circuitry within the [ADV7282-M](#) restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the [ADV7282-M](#).

### DIFFERENTIAL INPUT NETWORK

Figure 7 shows the input network to use when differential CVBS video is input on the  $A_{INX}$  input pins of the [ADV7282-M](#).

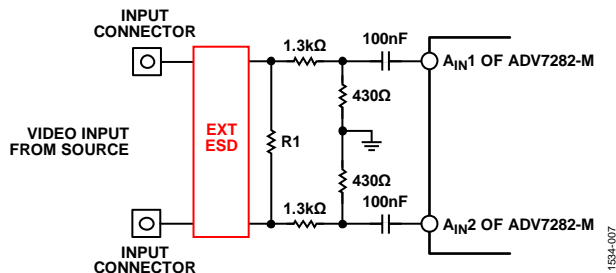


Figure 7. Differential Input Network

Fully differential video transmission involves transmitting two complementary CVBS signals. Pseudo differential video transmission involves transmitting a CVBS signal and a source ground signal.

Differential video transmission has several key advantages over single-ended transmission, including the following:

- Inherent small signal and large signal noise rejection
- Improved EMI performance
- Ability to absorb ground bounce

Resistor R1 provides the RF end termination for the differential CVBS input lines. For a pseudo differential CVBS input, a value of 75  $\Omega$  is recommended for R1. For a fully differential CVBS input, a value of 150  $\Omega$  is recommended for R1.

The 1.3 k $\Omega$  and 430  $\Omega$  resistors create a resistor divider with a gain of 0.25. The resistor divider attenuates the amplitude of the input analog video, but increases the input common-mode range of the [ADV7282-M](#) to 4 V p-p. Note that amplifiers within the ADC restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the  $A_{INX}$  pin of the [ADV7282-M](#). The clamping circuitry within the [ADV7282-M](#) restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the [ADV7282-M](#).

The combination of the 1.3 k $\Omega$  and 430  $\Omega$  resistors and the 100 nF ac coupling capacitors limits the current flow into the [ADV7282-M](#) during short-to-battery (STB) events (see the Short-to-Battery Protection section).

To achieve optimal performance, the 1.3 k $\Omega$  and 430  $\Omega$  resistors must be closely matched; that is, all 1.3 k $\Omega$  and 430  $\Omega$  resistors must have the same resistance tolerance, and this tolerance must be as low as possible.

### SHORT-TO-BATTERY PROTECTION

In differential mode, the [ADV7282-M](#) is protected against short-to-battery (STB) events by ac coupling capacitors (see Figure 7). The input network resistors are sized to reduce the current flow during an STB event, thus preventing damage to the resistors. The R1 resistor is protected because no current or limited current flows through it during an STB event.

The [ADV7282-M](#) provides two STB diagnostic pins that can be used to generate an interrupt when an STB event occurs. For more information, see the Short-to-Battery (STB) Diagnostics section.

## INPUT CONFIGURATION

The input format of the [ADV7282-M](#) is specified using the INSEL[4:0] bits (see Table 10). These bits also configure the SDP core to process CVBS, differential CVBS, Y/C (S-Video), or component (YPrPb) format. The INSEL[4:0] bits are located in the user sub map of the register space at Address 0x00[4:0]. For more information about the registers, see the Register Maps section.

The INSEL[4:0] bits specify predefined analog input routing schemes, eliminating the need for manual mux programming and allowing the user to route the various video signal types to the decoder. For example, if the CVBS input is selected, the remaining channels are powered down.

**Table 10. Input Format Specified by the INSEL[4:0] Bits**

INSEL[4:0] Bit Value	Video Format	Analog Inputs
00000	CVBS	CVBS input on A <sub>IN1</sub>
00001	CVBS	CVBS input on A <sub>IN2</sub>
00010	CVBS	CVBS input on A <sub>IN3</sub>
00011	CVBS	CVBS input on A <sub>IN4</sub>
00100	Reserved	Reserved
00101	Reserved	Reserved
00110	CVBS	CVBS input on A <sub>IN5</sub>
00111	CVBS	CVBS input on A <sub>IN6</sub>
01000	Y/C (S-Video)	Y input on A <sub>IN1</sub> ; C input on A <sub>IN2</sub>
01001	Y/C (S-Video)	Y input on A <sub>IN3</sub> ; C input on A <sub>IN4</sub>
01010	Reserved	Reserved
01011	Y/C (S-Video)	Y input on A <sub>IN5</sub> ; C input on A <sub>IN6</sub>
01100	YPrPb	Y input on A <sub>IN1</sub> ; Pb input on A <sub>IN2</sub> ; Pr input on A <sub>IN3</sub>
01101	Reserved	Reserved
01110	Differential CVBS	Positive input on A <sub>IN1</sub> ; Negative input on A <sub>IN2</sub>
01111	Differential CVBS	Positive input on A <sub>IN3</sub> ; Negative input on A <sub>IN4</sub>
10000	Reserved	Reserved
10001	Differential CVBS	Positive input on A <sub>IN5</sub> ; Negative input on A <sub>IN6</sub>
10010 to 11111	Reserved	Reserved



## SHORT-TO-BATTERY (STB) DIAGNOSTICS

The **ADV7282-M** senses an STB event via the DIAG1 and DIAG2 pins. The DIAG1 and DIAG2 pins can sense an STB event on either the positive or negative differential input because of the negligible voltage drop across Resistor R1.

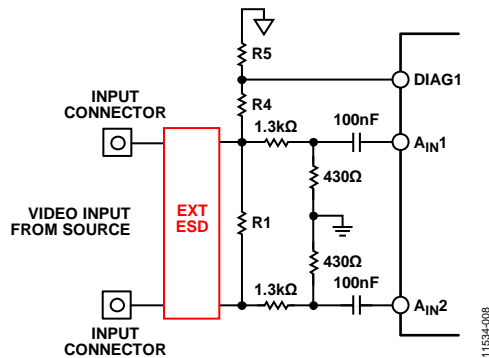


Figure 8. Diagnostic Connections

Resistors R4 and R5 divide down the voltage at the input connector to protect the DIAGx pin from an STB event. The DIAGx pin circuitry compares this voltage to a programmable reference voltage, known as the diagnostic slice level. When the diagnostic slice level is exceeded, an STB event has occurred.

When the DIAGx pin voltage exceeds the diagnostic slice level voltage, a hardware interrupt is triggered and indicated by the INTRQ pin. A readback register is also provided, which allows the user to determine the DIAGx pin on which the STB event occurred.

Use Equation 1 to find the trigger voltage for a selected diagnostic slice level.

$$V_{STB\_TRIGGER} = \frac{R5 + R4}{R5} \times DIAGNOSTIC\_SLICE\_LEVEL \quad (1)$$

where:

$V_{STB\_TRIGGER}$  is the minimum voltage required at the input connector to trigger the STB interrupt on the **ADV7282-M**.  
 $DIAGNOSTIC\_SLICE\_LEVEL$  is the programmable reference voltage.

Table 12. DIAG1 Pin Configuration (Address 0x5D)

Bit Name	Bits (Address 0x5D)	Value	Description
DIAG1_SLICE_LEVEL[2:0]	[4:2]	See Table 11	Set the diagnostic slice level for DIAG1
DIAG1_SLICER_EN	5	1	Enable the diagnostic circuitry for DIAG1
DIAG1_SLICER_PWRDN	6	0	Power up the diagnostic circuitry for DIAG1

Table 13. DIAG2 Pin Configuration (Address 0x5E)

Bit Name	Bits (Address 0x5E)	Value	Description
DIAG2_SLICE_LEVEL[2:0]	[4:2]	See Table 11	Set the diagnostic slice level for DIAG2
DIAG2_SLICER_EN	5	1	Enable the diagnostic circuitry for DIAG2
DIAG2_SLICER_PWRDN	6	0	Power up the diagnostic circuitry for DIAG2

## PROGRAMMING THE STB DIAGNOSTIC FUNCTION

By default, the STB diagnostic function is disabled on the **ADV7282-M**. To enable the diagnostic function, follow the instructions in this section.

### DIAG1 Pin

The DIAG1\_SLICE\_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG1 pin (see Table 11). These bits are located in the user sub map at Address 0x5D[4:2]. When a voltage greater than the diagnostic slice level is seen on the DIAG1 pin, an STB interrupt is triggered on the **ADV7282-M**.

To ensure that the diagnostic functionality on the DIAG1 pin works correctly, set the bits listed in Table 12.

Table 11. Diagnostic Slice Level Settings

DIAG1_SLICE_LEVEL[2:0] or DIAG2_SLICE_LEVEL[2:0]	Diagnostic Slice Level
000	75 mV
001	225 mV
010	375 mV
011 (default)	525 mV
100	675 mV
101	825 mV
110	975 mV
111	1.125 V

### DIAG2 Pin

The DIAG2\_SLICE\_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG2 pin (see Table 11). These bits are located in the user sub map at Address 0x5E[4:2]. When a voltage greater than the diagnostic slice level is seen on the DIAG2 pin, an STB interrupt is triggered on the **ADV7282-M**.

To ensure that the diagnostic functionality on the DIAG2 pin works correctly, set the bits listed in Table 13.



## ADAPTIVE CONTRAST ENHANCEMENT (ACE)

The [ADV7282-M](#) can increase the contrast of an image depending on the content of the picture, allowing bright areas to be made brighter and dark areas to be made darker. The optional ACE feature enables the contrast within dark areas to be increased without significantly affecting the bright areas. The ACE feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

The ACE function is disabled by default. To enable the ACE function, execute the register writes shown in Table 14. To disable the ACE function, execute the register writes shown in Table 15.

**Table 14. Register Writes to Enable the ACE Function**

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x80	Enable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter user sub map

**Table 15. Register Writes to Disable the ACE Function**

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x00	Disable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter user sub map

## I2P FUNCTION

The advanced interlaced-to-progressive (I2P) function allows the [ADV7282-M](#) to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The [ADV7282-M](#) uses edge adaptive technology to minimize video defects on low angle lines.

The I2P function is disabled by default. To enable the I2P function, use the recommended scripts from Analog Devices, Inc.

## MIPI CSI-2 OUTPUT

The decoder in the [ADV7282-M](#) outputs an ITU-R BT.656 data stream. The ITU-R BT.656 data stream is connected into a CSI-2 Tx module. Data from the CSI-2 Tx module is fed into a D-PHY physical layer and output serially from the device.

The output of the [ADV7282-M](#) consists of a single data channel on the D0P and D0N lanes and a clock channel on the CLKP and CLKN lanes.

Video data is output over the data lanes in high speed mode. The data lanes enter low power mode during the horizontal and vertical blanking periods.

The clock lanes are used to clock the output video. After the [ADV7282-M](#) is programmed, the clock lanes exit low power mode and remain in high speed mode until the part is reset or powered down.

The [ADV7282-M](#) outputs video data in an 8-bit YCrCb 4:2:2 format. When the I2P core is disabled, the video data is output in an interlaced format at a nominal data rate of 216 Mbps. When the I2P core is enabled, the video data is output in a progressive format at a nominal data rate of 432 Mbps (see the I2P Function section for more information).

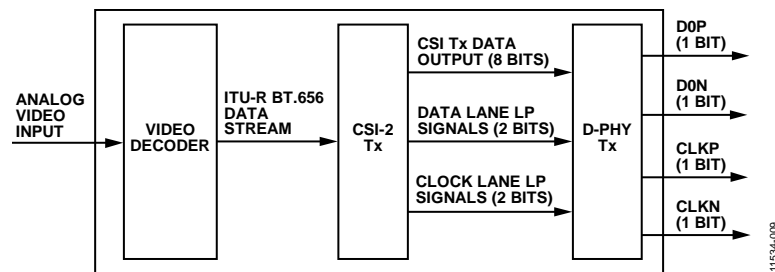


Figure 9. MIPI CSI-2 Output Stage of the [ADV7282-M](#)

## I<sup>2</sup>C PORT DESCRIPTION

The **ADV7282-M** supports a 2-wire, I<sup>2</sup>C-compatible serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the **ADV7282-M** and the system I<sup>2</sup>C master controller. The I<sup>2</sup>C port of the **ADV7282-M** allows the user to set up and configure the decoder and to read back captured VBI data.

The **ADV7282-M** has a number of possible I<sup>2</sup>C slave addresses and subaddresses (see the Register Maps section). The main map of the **ADV7282-M** has four possible slave addresses for read and write operations, depending on the logic level of the ALSB pin (see Table 16).

**Table 16. Main Map I<sup>2</sup>C Address for the **ADV7282-M****

ALSB Pin	R/W Bit	Slave Address
0	0	0x40 (write)
0	1	0x41 (read)
1	0	0x42 (write)
1	1	0x43 (read)

The ALSB pin controls Bit 1 of the slave address. By changing the logic level of the ALSB pin, it is possible to control two **ADV7282-M** devices in an application without using the same I<sup>2</sup>C slave address. The LSB (Bit 0) specifies either a read or write operation: Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

To control the device on the bus, a specific protocol is followed.

1. The master initiates a data transfer by establishing a start condition, which is defined as a high to low transition on SDATA while SCLK remains high, and indicates that an address/data stream follows.
2. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/W bit). The bits are transferred from MSB to LSB.
3. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge (ACK) bit.

4. All other devices withdraw from the bus and maintain an idle condition. In the idle condition, the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address.

The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The **ADV7282-M** acts as a standard I<sup>2</sup>C slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/W bit. The device has subaddresses to enable access to the internal registers; therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register individually without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the **ADV7282-M** does not issue an acknowledge and returns to the idle condition.

If the highest subaddress is exceeded in auto-increment mode, one of the following actions is taken:

- In read mode, the register contents of the highest subaddress continue to be output until the master device issues a no acknowledge, which indicates the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into a subaddress register. A no acknowledge is issued by the **ADV7282-M**, and the part returns to the idle condition.

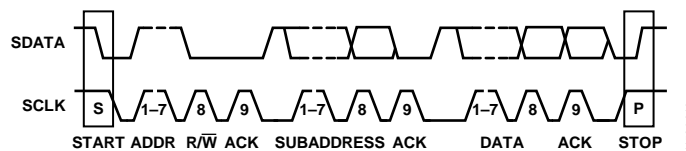


Figure 10. Bus Data Transfer

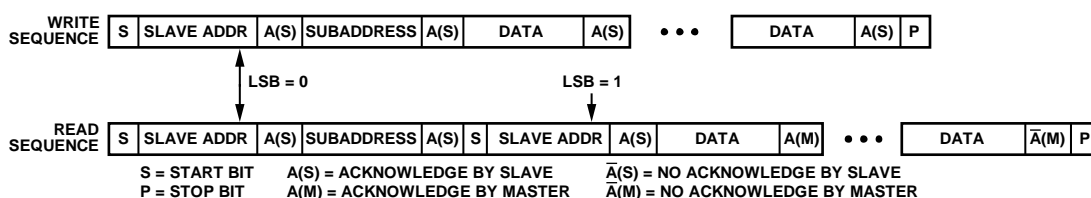


Figure 11. Read and Write Sequence

## REGISTER MAPS

The **ADV7282-M** contains three register maps: the main register map, the VPP register map, and the CSI register map (see Figure 12).

### Main Map

The I<sup>2</sup>C slave address of the main map of the **ADV7282-M** is set by the ALSB pin (see Table 16). The main map allows the user to program the I<sup>2</sup>C slave addresses of the VPP and CSI maps. The main map contains three sub maps: the user sub map, the interrupt/VDP sub map, and User Sub Map 2. These three sub maps are accessed by writing to the SUB\_USR\_EN bits (Address 0x0E[6:5]) within the main map (see Figure 12 and Table 17).

### User Sub Map

The user sub map contains registers that program the analog front end and digital core of the **ADV7282-M**. The user sub map has the same I<sup>2</sup>C slave address as the main map. To access the user sub map, set the SUB\_USR\_EN bits in the main map (Address 0x0E[6:5]) to 00.

### Interrupt/VDP Sub Map

The interrupt/VDP sub map contains registers that can be used to program internal interrupts, control the INTRQ pin, and decode vertical blanking interval (VBI) data.

The interrupt/VDP sub map has the same I<sup>2</sup>C slave address as the main map. To access the interrupt/VDP sub map, set the SUB\_USR\_EN bits in the main map (Address 0x0E[6:5]) to 01.

### User Sub Map 2

User Sub Map 2 contains registers that control the ACE, down dither, and fast lock functions. It also contains controls that set the acceptable input luma and chroma limits before the **ADV7282-M** enters free run and color kill modes.

User Sub Map 2 has the same I<sup>2</sup>C slave address as the main map. To access User Sub Map 2, set the SUB\_USR\_EN bits in the main map (Address 0x0E[6:5]) to 10.

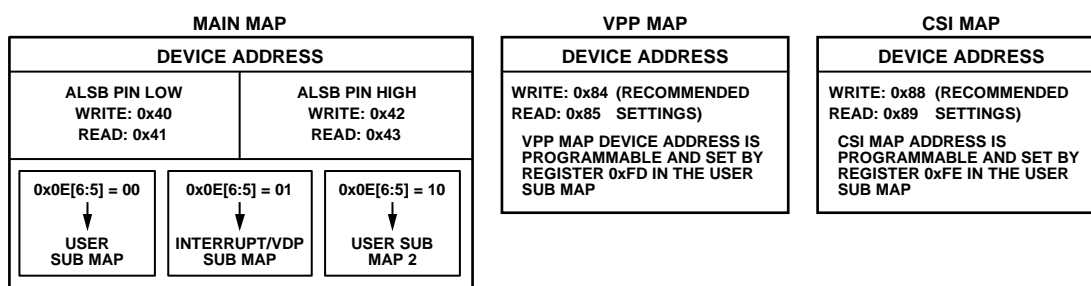


Figure 12. Register Map and Sub Map Access

11534-012

Table 17. I<sup>2</sup>C Register Map and Sub Map Addresses

ALSB Pin	R/W Bit	Slave Address	SUB_USR_EN Bits (Address 0x0E[6:5])	Register Map or Sub Map
0	0 (write)	0x40	00	User sub map
0	1 (read)	0x41	00	User sub map
0	0 (write)	0x40	01	Interrupt/VDP sub map
0	1 (read)	0x41	01	Interrupt/VDP sub map
0	0 (write)	0x40	10	User Sub Map 2
0	1 (read)	0x41	10	User Sub Map 2
1	0 (write)	0x42	00	User sub map
1	1 (read)	0x43	00	User sub map
1	0 (write)	0x42	01	Interrupt/VDP sub map
1	1 (read)	0x43	01	Interrupt/VDP sub map
1	0 (write)	0x42	10	User Sub Map 2
1	1 (read)	0x43	10	User Sub Map 2
X <sup>1</sup>	0 (write)	0x84	XX <sup>1</sup>	VPP map
X <sup>1</sup>	1 (read)	0x85	XX <sup>1</sup>	VPP map
X <sup>1</sup>	0 (write)	0x88	XX <sup>1</sup>	CSI map
X <sup>1</sup>	1 (read)	0x89	XX <sup>1</sup>	CSI map

<sup>1</sup> X and XX mean don't care.

**VPP Map**

The video postprocessor (VPP) map contains registers that control the I2P core (interlaced-to-progressive converter).

The VPP map has a programmable I<sup>2</sup>C slave address, which is programmed using Register 0xFD in the user sub map of the main map. The default value for the VPP map address is 0x00; however, the VPP map cannot be accessed until the I<sup>2</sup>C slave address is reset. The recommended I<sup>2</sup>C slave address for the VPP map is 0x84.

To reset the I<sup>2</sup>C slave address of the VPP map, write to the VPP\_SLAVE\_ADDRESS[7:1] bits in the main register map (Address 0xFD[7:1]). Set these bits to a value of 0x84 (I<sup>2</sup>C write address; I<sup>2</sup>C read address is 0x85).

**CSI Map**

The CSI map contains registers that control the MIPI CSI-2 output stream from the [ADV7282-M](#).

The CSI map has a programmable I<sup>2</sup>C slave address, which is programmed using Register 0xFE in the user sub map of the main map. The default value for the CSI map address is 0x00; however, the CSI map cannot be accessed until the I<sup>2</sup>C slave address is reset. The recommended I<sup>2</sup>C slave address for the CSI map is 0x88.

To reset the I<sup>2</sup>C slave address of the CSI map, write to the CSI\_TX\_SLAVE\_ADDRESS[7:1] bits in the main register map (Address 0xFE[7:1]). Set these bits to a value of 0x88 (I<sup>2</sup>C write address; I<sup>2</sup>C read address is 0x89).

**SUB\_USR\_EN Bits, Address 0x0E[6:5]**

The [ADV7282-M](#) main map contains three sub maps: the user sub map, the interrupt/VDP sub map, and User Sub Map 2 (see Figure 12). The user sub map is available by default. The other two sub maps are accessed using the SUB\_USR\_EN bits. When programming of the interrupt/VDP map or User Sub Map 2 is completed, it is necessary to write to the SUB\_USR\_EN bits to return to the user sub map.

## PCB LAYOUT RECOMMENDATIONS

The **ADV7282-M** is a high precision, high speed, mixed-signal device. To achieve maximum performance from the part, it is important to use a well-designed PCB. This section provides guidelines for designing a PCB for use with the **ADV7282-M**.

### ANALOG INTERFACE INPUTS

When routing the analog interface inputs on the PCB, keep track lengths to a minimum. Use 75  $\Omega$  trace impedances when possible; trace impedances other than 75  $\Omega$  increase the chance of reflections.

### POWER SUPPLY DECOUPLING

It is recommended that each power supply pin be decoupled with 100 nF and 10 nF capacitors. The basic principle is to place a decoupling capacitor within approximately 0.5 cm of each power pin. Avoid placing the decoupling capacitors on the opposite side of the PCB from the **ADV7282-M** because doing so introduces inductive vias in the path.

Place the decoupling capacitors between the power plane and the power pin. Current should flow from the power plane to the capacitor and then to the power pin. Do not apply the power connection between the capacitor and the power pin. The best approach is to place a via near, or beneath, the decoupling capacitor pads down to the power plane (see Figure 13).

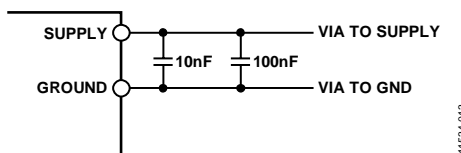


Figure 13. Recommended Power Supply Decoupling

It is especially important to maintain low noise and good stability for the  $P_{VDD}$  pin. Careful attention must be paid to regulation, filtering, and decoupling. It is highly desirable to provide separate regulated supplies for each circuit group ( $A_{VDD}$ ,  $D_{VDD}$ ,  $D_{VDDIO}$ ,  $M_{VDD}$ , and  $P_{VDD}$ ).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This disparity can result in a measurable change in the voltage supplied to the analog supply regulator, which can, in turn, produce changes in the regulated analog supply voltage. This problem can be mitigated by regulating the analog supply, or at least the  $P_{VDD}$  supply, from a different, cleaner power source, for example, from a 12 V supply.

Using a single ground plane for the entire board is also recommended. Experience has shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

### VREFN AND VREFP PINS

Place the circuit associated with the VREFN and VREFP pins as close as possible to the **ADV7282-M** and on the same side of the PCB as the part.

### DIGITAL OUTPUTS ( $\overline{INTRQ}$ , GPO0 TO GPO2)

Minimize the trace length that the digital outputs must drive. Longer traces have higher capacitance, requiring more current and, in turn, causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a 30  $\Omega$  to 50  $\Omega$  series resistor can suppress reflections, reduce EMI, and reduce current spikes inside the **ADV7282-M**. If series resistors are used, place them as close as possible to the pins of the **ADV7282-M**. However, try not to add vias or extra length to the output trace in an attempt to place the resistors closer.

If possible, limit the capacitance that each digital output must drive to less than 15 pF. This recommendation can be easily accommodated by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the **ADV7282-M**, creating more digital noise on the power supplies.

### EXPOSED METAL PAD

The **ADV7282-M** has an exposed metal pad on the bottom of the package. This pad must be soldered to ground. The exposed pad is used for proper heat dissipation, noise suppression, and mechanical strength.

### DIGITAL INPUTS

The digital inputs of the **ADV7282-M** are designed to work with 1.8 V signals (3.3 V for  $D_{VDDIO}$ ) and are not tolerant of 5 V signals. Extra components are required if 5 V logic signals must be applied to the decoder.

### MIPI OUTPUTS (DOP, DON, CLKP, CLKN)

It is recommended that the MIPI output traces be kept as short as possible and on the same side of the PCB as the **ADV7282-M** device. It is also recommended that a solid plane (preferably a ground plane) be placed on the layer adjacent to the MIPI traces to provide a solid reference plane.

MIPI transmission operates in both differential and single-ended modes. During high speed transmission, the pair of outputs operates in differential mode; in low power mode, the pair operates as two independent single-ended traces. Therefore, it is recommended that each output pair be routed as two loosely coupled 50  $\Omega$  single-ended traces to reduce the risk of crosstalk between the two traces in low power mode.

## TYPICAL CIRCUIT CONNECTION

Figure 14 provides an example of how to connect the [ADV7282-M](#). For detailed schematics of the [ADV7282-M](#) evaluation board, contact a local Analog Devices field applications engineer or an Analog Devices distributor.

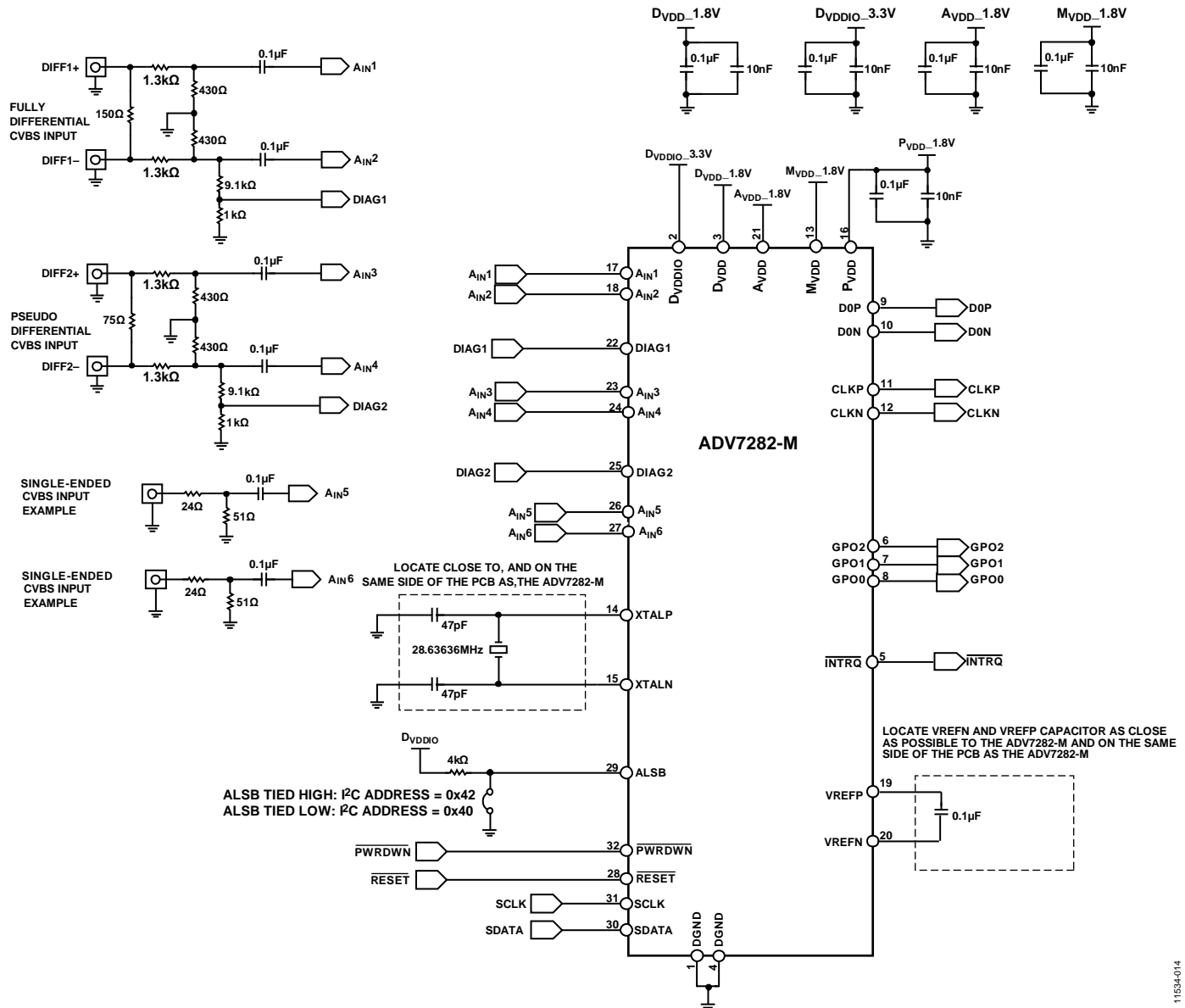
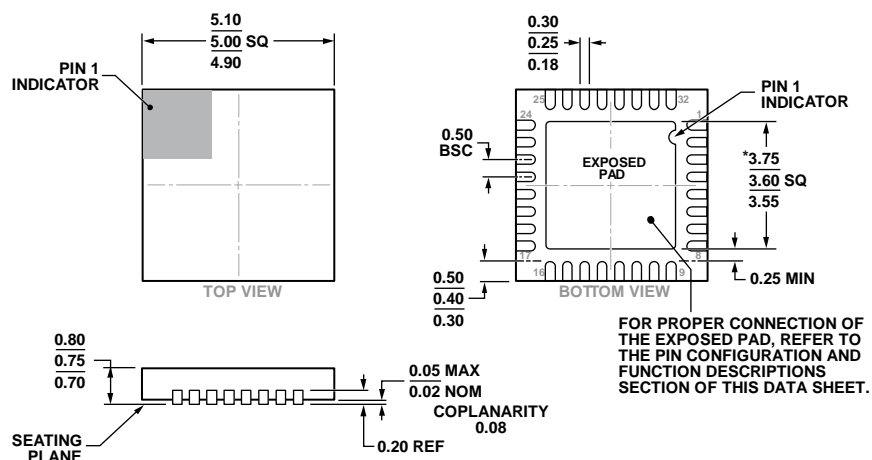


Figure 14. Typical Connection Diagram



## OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5  
WITH THE EXCEPTION OF THE EXPOSED PAD DIMENSION.

Figure 15. 32-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
5 mm x 5 mm Body, Very Very Thin Quad  
(CP-32-12)  
Dimensions shown in millimeters

08-16-2010-B

## ORDERING GUIDE

Model <sup>1, 2</sup>	Temperature Range	Package Description	Package Option
ADV7282WBCPZ-M	-40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7282WBCPZ-M-RL	-40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
EVAL-ADV7282MEBZ	-40°C to +105°C	Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The [ADV7282W](#) models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**NOTES**

## NOTES

## NOTES

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).