Rockchip RV1103 Datasheet

Revision History

Date	Revision	Description
2022-04-27	1.1	Update MSL information and package thermal characteristics
2022-04-06	1.0	Initial released

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Chapter 1 Introduction

1.1 Overview

RV1103 is a highly integrated vision processor SoC for IPC, especially for AI related applications.

It is based on a single-core ARM Cortex-A7 32-bit core which integrates NEON and FPU. There is a 32KB I-cache and 32KB D-cache and 128KB unified L2 cache.

The build-in NPU supports INT4/INT8/INT16 hybrid operation and computing power is up to 0.5TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RV1103 introduces a totally new generation hardware-based maximum 4-Megapixel ISP (image signal processor). It implements a lot of algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehaze, gamma correction and so on. Cooperating with two MIPI CSI (or LVDS), users can build a system that receives video data from 2 camera sensors simultaneous.

The video encoder embedded in RV1103 supports H.265/H.264 encoding. It also supports multi-stream encoding. With the help of this feature, the video from the camera can be encoded with higher resolution and stored in local memory and transferred to another lower resolution video to cloud storage at the same time. To accelerate video processing, an intelligent video engine with 22 calculation units is also embedded. RV1103 has a build-in 16-bit DRAM DDR2 capable of sustaining demanding memory bandwidths. It also integrated build-in POR, audio codec and MAC PHY.

1.2 Feature

The features listed below which may or may not be present in actual product, may be subject to the third-party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Application Processor

- Single core ARM Cortex-A7
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD
- Separately Integrated Neon and FPU
- 32KB L1 I-Cache and 32KB L1 D-Cache
- Unified 128KB L2 Cache for Cortex-A7
- TrustZone technology support
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
 - BootRom
 - ◆ Support system boot from the following device:
 - SPI interface
 - SD/MMC interface
 - Support system code download by the following interface:
 - USB interface
 - UART interface
 - 256KB Share Memory
 - 8KB PMU SRAM
 - RV1103G1 SIP 512Mb DDR2
- External off-chip memory
 - SD/MMC Interface
 - ♦ Compatible with SD3.0, MMC ver4.51
 - ◆ Data bus width is 4bits
 - Flexible Serial Flash Interface (FSPI)

- ◆ Support transfer data from/to serial flash device
- ◆ Support 1bit, 2bits or 4bits data bus width

1.2.3 System Component

- MCU
 - MCU in VD_CORE integrate 16KB Cache
 - Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC for CPU also connect to MCU
 - Integrated Debug Controller with JTAG interface
- CRU (clock & reset unit)
 - Support total 4 PLLs to generate all clocks
 - One oscillator with 24MHz clock input
 - Support clock gating control for individual components
 - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU (power management unit)
 - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
 - Lots of wakeup sources in different mode
 - Support 3 separate voltage domains, VDD ARM, VDD LOGIC, VDD PMU.

Timer

- Support 2 secure timers with 64bits counter and interrupt-based operation
- Support 6 non-secure timers with 64bits counter and interrupt-based operation
- Support two operation modes: free-running and user-defined count for each timer
- Support timer work state checkable

PWM

- Support 12 on-chip PWMs (PWM0~PWM11) with interrupt-based operation
- Programmable pre-scaled operation to bus clock and then further scaled
- Embedded 32-bit timer/counter facility
- Support capture mode
- Support continuous mode or one-shot mode
- Provides reference mode and output various duty-cycle waveform
- Optimized for IR application for PWM3, PWM7, PWM11

Watchdog

- 32-bit watchdog counter
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
 - ◆ Generate a system reset
 - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- One Watchdog for non-secure application
- One Watchdog for secure application

Interrupt Controller

- Support 121 SPI interrupt sources input from different components inside RV1103
- Support 16 software-triggered interrupts
- Input interrupt level is fixed, high-level sensitive or rising edge sensitive
- Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC

- Micro-code programming-based DMA
- Linked list DMA function is supported to complete scatter-gather transfer
- Support data transfer types including memory-to-memory, memory-to-peripherals, peripherals-to-memory
- Totally three embedded DMA controllers for peripheral system
- Each DMAC features:
 - Support 8 channels
 - ◆ 32 hardware requests from peripherals
 - ◆ 2 interrupt output
 - Support TrustZone technology and programmable secure state for each DMA channel

Secure System

- Embedded one cipher engines
 - ◆ Support Link List Item (LLI) DMA transfer
 - ◆ Support SHA-1, SHA-256/224, MD5 with hardware padding
 - ◆ Support HMAC of SHA-1, SHA-256, MD5 with hardware padding
 - ◆ Support AES-128, AES-192, AES-256 encrypt and decrypt cipher
 - ♦ Support DES and TDES cipher
 - ◆ Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/GCM/CBC-MAC/CMAC mode
 - ◆ Support DES/TDES ECB/CBC/OFB/CFB mode
 - ♦ Support up to 4096 bits PKA mathematical operations for RSA/ECC/SM2
- Support generating random numbers, one secure only engine, another one security configurable
- Support secure OTP
- Support secure debug
- Support secure OS
- Except CPU, the other masters in the SoC can also support security and non-security mode by software-programmable
- Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
- System SRAM (share memory), part of space is addressed only in security mode
- External DDR space can be divided into 16 parts, each part can be softwareprogrammable to be enabled by each master

Mailbox

- One Mailbox in SoC to service CPU and MCU communication
- Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
- Provide 32 lock registers for software to use to indicate whether mailbox is occupied

Decompression

- Support for decompressing GZIP files
- Support for decompressing data in DEFLATE format
- Support for decompressing data in ZLIB format
- Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process

1.2.4 Video CODEC

- Video Encoder
 - H.265/HEVC Main Profile, level 5.0
 - H.264/AVC High Profile, level 5.0
 - Support multi-channel encoding with performance up to 4-megapixel@30fps

■ JPEG baseline, up to 4-megapixel @60fps in standalone mode, resolution up to 8192 x 8192

- Bitrate up to 60Mbps
- Six bit rate control modes (CBR, VBR, FIXQP, AVBR, QPMAP, and CVBR)
- Support YUV420 and YUV400 format input
- Intelligent encoding mode
- 8-area OSD
- YUV/RGB video source with crop, rotation and mirror
- Ultra-low delay encoding

1.2.5 Neural Process Unit

- Neural network acceleration engine with processing performance up to 0.5 TOPS
- Support integer 4, integer 8 and integer 16 operation
- Support creating simple custom operators
- Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, etc.

1.2.6 Rockchip Intelligent Video Engine (RKIVE)

- GMM
 - Support 1 to 5 gaussian model
- BGM (base on codebook)
 - Support 3 codebook model
- Canny
 - Staging buffer stride require 64 pixel align
 - Support 3X3 and 5x5 template coefficient
- CCL
 - Support max to 254 connected regions
 - Support 4-connected and 8-connected region
- Stcorner
 - Support max to 500 corner sort output
- LK
 - Support max to 500 corner input
 - Support 1~4 optical flow layers
- Integral
 - Require all the buffer base is 16bytes align
- LBP
 - Support simple and absolute value comparison mode
- Filter
 - Support 3X3 and 5x5 mode
- Sobel
 - Support 3X3 and 5x5 mode
- Morph
 - Support eroding and dilating mode
- Denoise Filter
 - Support minimum/median/maximum 3 types filter
- DMA
 - Support direct copy mode
 - Support interval copy mode
- CSC
 - Support rgb2yuv, yuv2rgb, rgb2hsv, yuv2hsv
 - Support 601 and 709 format, full and limit range
- Hist/eghist
 - Support hist only, eqhist only, hist + eqhist 3 types mode
- Logic OP
 - Support logic and, logic or, logic xor, add, sub, absolute difference
- Mag and Ang
 - Calculation of the image gradient magnitude and direction
- Morph

- Support eroding and dilating mode
- NCC
 - Calculation of the image normalized cross-correlation
- Cast
 - Data linear transformation
- Sad
 - Support sad size is 4x4, 8x8 and 16x16
- Threshold
 - Convert grayscale into a binary image
- Map
 - Support 8bit to 8bit and 8bit to 16bit map operation

1.2.7 Graphics Engine

- 2D Graphics Engine
 - Input data:
 - ◆ ARGB/RGB888/RGB565/RGB4444/RGB5551
 - ◆ YUV420/YUV422/YVYU422/YVYU420/YUV422SP10bit/YUV420SP10bit
 - Output data:
 - ◆ ARGB/RGB888/RGB565/RGB4444/RGB5551
 - ♦ YUV420/YUV422/YUV400/Y4/YVYU422/YVYU420
 - Pixel Format conversion, BT.601/BT.709
 - Dither operation
 - Max resolution: 8192x8192 source, 4096x4096 destination
 - Scaling
 - ◆ Down-scaling: Average filter
 - ◆ Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
 - ◆ Arbitrary non-integer scaling ratio, from 1/16 to 16
 - Rotation
 - ◆ 0, 90, 180, 270-degree rotation
 - ◆ x-mirror, y-mirror
 - ◆ Mirroring and rotation co-operation
 - BitBLT
 - Block transfer
 - ◆ Color palette/Color fill, support with alpha
 - ◆ Transparency mode (color keying/stencil test, specified value/value range)
 - ◆ Two source BitBLT
 - ◆ A+B=B only BitBLT, A support rotate & scale when B fixed
 - ◆ A+B=C second source (B) has same attribute with (C) plus rotation function
 - Alpha Blending
 - ◆ Comprehensive per-pixel alpha(color/alpha channel separately)
 - Fading
 - ◆ Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
 - ◆ Support DST Full CSC convert for YUV2YUV
 - OSD Automatic Inversion
 - Supports OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
 - ◆ Support SRC0 and OSD overlay
 - Support square mosaic patterns to cover rectangular mosaic areas

1.2.8 Video Input Interface

- MIPI Interface
 - Two MIPI CSI DPHY
 - ◆ Each MIPI DPHY V1.2, 2lanes, 1.5Gbps per lane
 - ◆ Support to combine 2 DPHY together to one 4lanes

1.2.9 Image Signal Processor

- Maximum input: 4M @30fps
- Minimum input: 256x256

 3A: Include Auto Enhance (AE)/Histogram, Auto Focus (AF), and Auto White Balance (AWB) statistics output

- EXPANDER: Sensor expander
- BLC: Black Level Correction
- DPCC: Static/Dynamic Defect Pixel Cluster Correction
- PDAF: Phase Detection Auto Focus
- LSC: Lens Shading Correction
- Bayer-2DNR: Spatial Bayer-raw Noise Reduction
- Bayer-3DNR: Temporal Bayer-raw Noise Reduction
- CAC: Chromatic Aberration Correction
- HDR-MGE: 2-Frame Merge into High-Dynamic Range
- HDR-DRC: HDR Dynamic Range Compression, Tone mapping
- GIC: Green Imbalance Correction
- DeBayer: Advanced Adaptive Demosaic
- CCM/CSM: Color Correction Matrix, RGB2YUV, etc.
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and effect enhancement
- 3DLUT: 3D-LUT Color Palette for Customer
- LDCH: Lens Distortion Correction only in the Horizontal direction
- YUV-2DNR: Spatial YUV Noise Reduction
- Sharp: Image sharpening and boundary filtering
- CMSK: Privacy cover and mask
- Gain: Image local gain
- Multi-sensor reuse ISP, 4 sensors for maximum
- Bus interface: 32bit AHB configuration, 128bit AXI R/W
- Low power, auto-gating for each block
- MI R/W burst group to improve memory utilization
- MI 3+2 path output, MP stepless scaling, SP/BP scaling under 1080p, MPDS/SPDS fixed 1/16 downscaling

1.2.10 Audio Interface

- Audio Codec
 - Support two 24-bits ADC channels with 90dB SNR for stereo recording from microphone
 - Support one 24-bits DAC channels with 90dB SNR for stereo playback
 - Support differential and single-ended microphone or line input
 - Sampling rate of 8KHz/12KHz/16KHz/24KHz/32KHz/44.1kHz/48KHz/96KHz

1.2.11 Connectivity

- SDIO interface
 - Compatible with SDIO3.0 protocol
 - 4-bit data bus widths
- MAC 10/100M Ethernet controller and embedded PHY
 - Support one Ethernet controllers
 - Support 10/100-Mbps data transfer rates with the RMII interfaces
 - Support both full-duplex and half-duplex operation
- USB 2.0
 - Compatible with USB 2.0 specification
 - Support one USB 2.0 Host/Device
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
 - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
 - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a
- SPI interface
 - Support 2 SPI Controllers (SPI0-SPI1)

- Support two chip-select output
- Support serial-master and serial-slave mode, software-configurable
- I2C Master controller
 - Support 5 I2C Master(I2C0-I2C4)
 - Support 7bits and 10bits address mode
 - Software programmable clock frequency
 - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400k bits/s in the Fast-mode
- UART interface
 - Support 6 UART interfaces (UART0-UART5)
 - Embedded two 64-byte FIFO for TX and RX operation respectively
 - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
 - Standard asynchronous communication bits such as start, stop and parity
 - Support different input clock for UART operation to get up to 4Mbps baud rate
 - Support auto flow control mode for all UART

1.2.12 Others

- Multiple groups of GPIO
 - All of GPIOs can be used to generate interrupt
 - Support level trigger and edge trigger interrupt
 - Support configurable polarity of level trigger interrupt
 - Support configurable rising edge, falling edge and both edge trigger interrupt
 - Support configurable pull direction (a weak pull-up and a weak pull-down)
 - Support configurable drive strength
- Temperature Sensor (TS-ADC)
 - Support User-Defined Mode and Automatic Mode
 - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
 - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable
 - In Automatic Mode, the temperature of system reset can be configurable
 - -40~125°C temperature range and 1°C temperature resolution
- Successive approximation ADC (SARADC)
 - 10-bit resolution
 - Up to 1MS/s sampling rate
 - 2 single-ended input channels
- OTP
 - Support 8K bits Size, 7K bits for secure application
 - Support Program/Read/Idle mode
- Package Type
 - RoHS QFN88 (body: 9mm x 9mm pin pitch 0.35mm)

1.3 Block Diagram

The following diagram shows the basic block diagram.

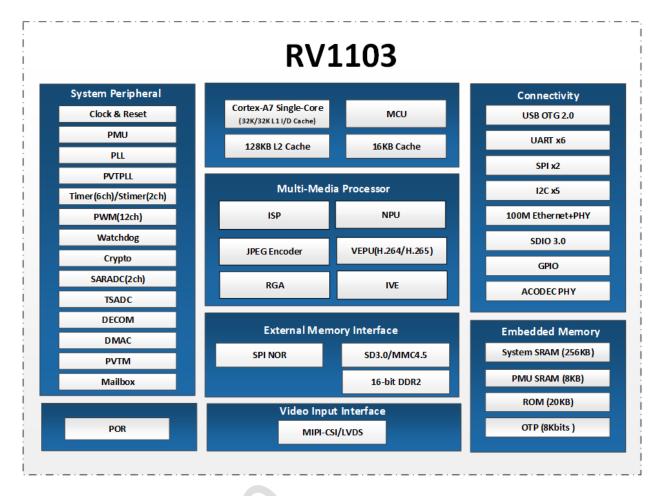


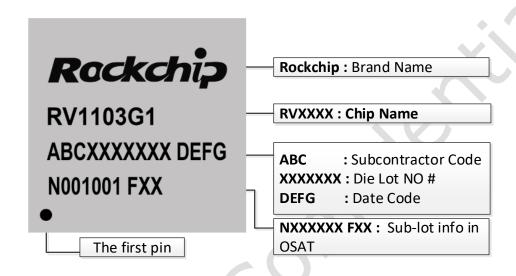
Fig.1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Q'ty Device Feature	
RV1103G1	RoHS	QFN88	2600 pcs by tray	Cortex A7 + MCU + 512Mb DDR2

2.2 Top Marking



2.3 Package Dimension

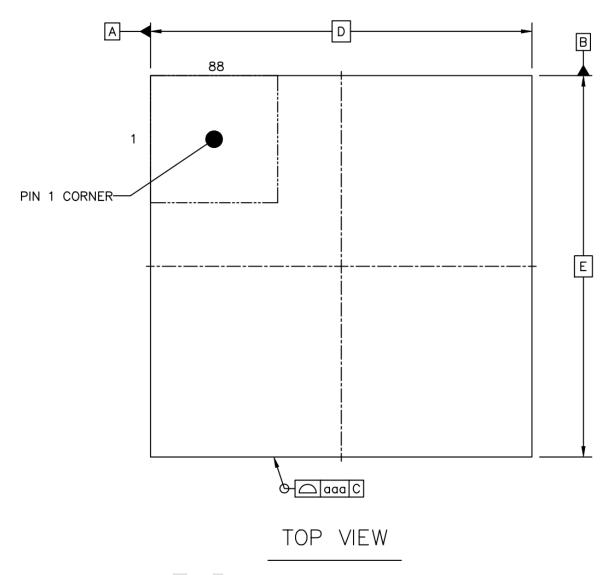


Fig.2-1 Package Top View

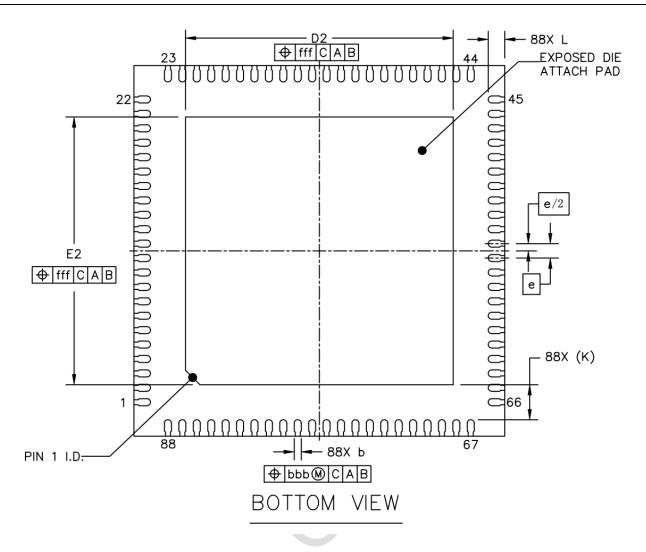


Fig.2-2 Package Bottom View

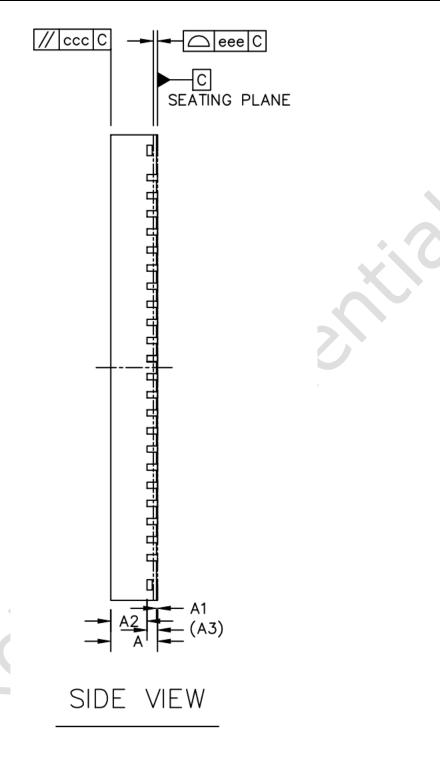


Fig.2-4 Package Side View

		SYMBOL	MIN	NOM	MAX		
TOTAL THICKNESS		А	0.85	0.9	0.95		
STAND OFF	A1	0	0.02	0.05			
MOLD THICKNESS		A2		0.70			
L/F THICKNESS		А3		0.203 REF			
LEAD WIDTH		b	0.12	0.17	0.22		
BODY SIZE	×	D	9 BSC				
DODT SIZE	Y	E	9 BSC				
LEAD PITCH		е	0.35 BSC				
EP SIZE	×	D2	6.4	6.5	6.6		
LI SIZE	Y	E2	6.4	6.5	6.6		
LEAD LENGTH		L	0.3	0.4	0.5		
LEAD TIP TO EXPOSED	PAD EDGE	K	0.85 REF				
PACKAGE EDGE TOLERA	ANCE	aaa	0.1				
MOLD FLATNESS		ccc	0.1				
COPLANARITY		eee	0.08				
LEAD OFFSET	bbb	0.07					
EXPOSED PAD OFFSET		fff		0.1			

Fig.2-5 Package Dimension

2.4 MSL Information

Moisture sensitivity Level: MSL3

2.5 Pin Number List

Table 2-1 Pin Number Order Information

Pin Name	Pin	Pin Name	Pin
MIPI_CLK0_OUT/GPIO3_C4_d	1	OSC_XIN	45
GPIO3 C5 d	2	OSC XOUT	46
PWM7 IR M2/MIPI CLK1 OUT/GPIO3 C6 d	3	OSC AVDD1V8/PLL AVDD1V8	47
I2C4_SCL_M2/UART5_TX_M2/ GPIO3_C7_d	4	PWM0 M0/CPU AVS/GPIO1 A2 d	48
I2C4_SDA_M2/UART5_RX_M2/ GPIO3_D0_d		JTAG CPU TCK M1/UART2 TX M1/JTAG HPMCU TCK	49
	5	M0/GPIO1_B2_d	
DVDD_1	6	JTAG_CPU_TMS_M1/UART2_RX_M1/JTAG_HPMCU_TMS_ M0/GPIO1_B3_u	50
GPIO4_VCC3V3	7	GPIO1_VCC3V3	51
SDMMC0_DET/GPIO3_A1_u	8	PWM10_M1/UART4_RTSN_M1/GPIO1_C6_d	52
SDMMC0_D1/UART2_TX_M0/PWM9_M0/GPIO3_A2_u	9	PWM11_IR_M1/UART4_CTSN_M1/GPIO1_C7_d	53
SDMMC0_D0/UART2_RX_M0/PWM8_M0/GPIO3_A3_u	10	I2C3_SCL_M1/UART5_TX_M1/PWM11_IR_M2/AUD_DSM N/GPIO1 D3 d	54
SDMMC0_CLK/UART5_RTSN_M0/I2C0_SCL_M2/PWM10_M0/GP IO3 A4 d	11	I2C3_SDA_M1/UART5_RX_M1/SPI0_CS1_M0/PWM0_M1/ AUD_DSM_P/GPI01_D2_d	55
SDMMC0_CMD/UART5_CTS_M0/I2C0_SDA_M2/PWM11_IR_M0 /GPIO3 A5 u	12	PWM10_M2/UART5_CTS_M1/UART3_RX_M1/GPIO1_D1_	56
SDMMC0_D3/UART5_TX_M0/JTAG_CPU_TMS_M0/JTAG_HPMCU TMS_M1/GPIO3_A6_u	13	PWM3_IR_M2/UART5_RTS_M1/UART3_TX_M1/GPIO1_D 0 d	57
SDMMC0_D2/UART5_RX_M0/JTAG_CPU_TCK_M0/JTAG_HPMCU	14	DVDD_4	58
_TCK_M1/GPIO3_A7_u		2012 (1/22	
SARADC_IN1/PWM1_M1/GPI4_C1_z	15	GPIO6_VCC	59
SARADC_IN0/GPI4_C0_z	16	PWM9_M1/UART4_TX_M1/SDMMC1_D2_M1/GPIO1_C5_ d	60
SARADC_USB_AVDD1V8	17	PWM8_M1/UART4_RX_M1/SDMMC1_D3_M1/GPIO1_C4_ d	61
USB_DM	18	PWM6_M2/I2C4_SDA_M1/SDMMC1_CMD_M1/SPI0_MIS O M0/GPIO1 C3 d	62
USB_DP	19	PWM5_M2/I2C4_SCL_M1/SDMMC1_CLK_M1/SPI0_MOSI _M0/GPIO1_C2_d	63
USB_AVDD3V3	20	PWM4_M2/SPI0_CLK_M0/SDMMC1_D0_M1/GPI01_C1_d	64
CODEC_LINEOUT	21	PWM2_M2/SPI0_CS0_M0/SDMMC1_D1_M1/GPI01_C0_d	65
CODEC VCM	22	OTP AVDD1V8/ETH AVDD1V8/TSADC AVDD1V8	66
CODEC AVDD1V8	23	ETH PHY RXN	67
CODEC MICOP MICP	24	ETH PHY RXP	68
CODEC MICBIAS	25	ETH PHY TXN	69
CODEC MIC1P MICN	26	ETH PHY TXP	70
GPIO3 VCC	27	ETH AVDD3V3	71
FSPI D3/GPIO4 A6 u	28	ETH EXTR	72
FSPI D0/GPIO4 A4 u	29	DVDD 5	73
FSPI D1/GPIO4 A3 u	30	CPU DVDD	74
FSPI_D2/GPIO4_A2_u	31	DVDD 6	75
FSPI CSO/GPIO4 B0 u	32	MIPI CSI RX D3N/LVDS RX D3N/GPI3 B0 d	76
FSPI_CLK/GPIO4_B0_d	33	MIPI_CSI_RX_D3P/LVDS_RX_D3P/GPI3_B1_d	77
DDR VDDQ 1	34	MIPI CSI RX CK1N/LVDS RX CK1N/GPI3 B2 d	78
DDR VDDQ 1	35	MIPI_CSI_RX_CK1N/LVDS_RX_CK1N/GF13_B2_d MIPI_CSI_RX_CK1P/LVDS_RX_CK1P/GP13_B3_d	79
DVDD 2	36	MIPI_CSI_RX_D2N/LVDS_RX_D2N/GPI3_B4_d	80
DRAM ZQ	37	MIPI CSI RX D2P/LVDS RX D2P/GPI3 B5 d	81
DDR PLL AVDD1V8	38	MIPI CSI RX D1N/LVDS RX D1N/GPI3 B6 d	82
DVDD 3	39	MIPI CSI RX D1P/LVDS RX D1P/GPI3 B7 d	83
DDR_VDDQ_3	40	MIPI_CSI_RX_DIP/LVDS_RX_DIP/GPI3_B7_d MIPI_CSI_RX_CK0N/LVDS_RX_CK0N/GPI3_C0_d	84
TVSS	41	MIPI CSI RX CKOP/LVDS RX CKOP/GPI3 C0 d	85
PWR CTRL M0/PWM1 M0/GPIO0 A4 d	42	MIPI_CSI_RX_CKUP/LVDS_RX_CKUP/GP13_C1_d MIPI_CSI_RX_D0N/LVDS_RX_D0N/GP13_C2_d	86
	42		
PMU_VCC3V3	44	MIPI_CSI_RX_D0P/LVDS_RX_D0P/GPI3_C3_d	87
OSC_PLL_PMU_DVDD	44	MIPI_AVDD1V8/GPIO7_VCC1V8	88
	i	VSS	E-PAD

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CPU_DVDD	0	TBD	V
Supply voltage for LOGIC	DVDD_i(i=1~6)	0	0.99	V
Supply voltage for PMU	OSC_PLL_PMU_DVDD	0	0.99	V
0.9V supply voltage	DVDD_i(i=1~6) OSC_PLL_PMU_DVDD	0	0.99	V
1.8V/3.3V supply voltage	GPIO <i>i</i> _VCC(<i>i</i> =3、4、6, 1.8V/3.3V mode)	0	3.63	V
1.8V supply voltage	OSC_AVDD1V8/PLL_AVDD1V8 DDR_PLL_AVDD1V8 MIPI_AVDD1V8/GPIO7_VCC1V8 SARADC_USB_AVDD1V8 OTP_AVDD1V8/ETH_AVDD1V8/TSADC_A VDD1V8 CODEC_AVDD1V8	0	1.98	V
3.3V supply voltage	GPIO1_VCC3V3 PMU_VCC3V3 USB_AVDD3V3 ETH_AVDD3V3	0	3.63	V
Supply voltage for DDR IO (DDR2 1.8V; DDR3 1.5V)	DDR_VDDQ_i (i=1~3)	0	TBD	V

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Тур	Max	Unit
Voltage for CPU	CPU_DVDD	TBD	0.90	TBD	V
Voltage for LOGIC	DVDD_ <i>i</i> (<i>i</i> =1~6)	0.81	0.90	TBD	٧
Voltage for PMU	OSC_PLL_PMU_DVDD	0.81	0.90	TBD	V
Voltage for PLL Analog (1.8V)	OSC_AVDD1V8/PLL_AVDD1V8	1.62	1.8	TBD	V
Voltage for GPIO (1.8V/3.3V)	GPIO <i>i</i> _VCC(<i>i</i> =3、4、6)	1.62 3.0	1.8 3.3	1.98 3.465	V
Voltage for GPIO (1.8V only)	MIPI_AVDD1V8/GPIO7_VCC1V8	1.62	1.8	1.98	V
Voltage for GPIO (3.3V only)	GPIO1_VCC3V3 PMU_VCC3V3	3.0	3.3	3.465	٧
Voltage for USB/SARADC Analog (1.8V)	SARADC_USB_AVDD1V8	1.62	1.8	1.98	V
Voltage for USB Analog (3.3V)	USB_AVDD3V3	3.0	3.3	3.6	V
Voltage for OTP/MAC Analog (1.8V)	OTP_AVDD1V8/ETH_AVDD1V8/TSADC_AVDD1V8	1.62	1.8	1.98	V
Voltage for MAC Analog (3.3V)	ETH_AVDD3V3	2.97	3.3	3.63	V
Voltage for CODEC Analog	CODEC_AVDD1V8	1.62	1.8	1.98	V
Voltage for MIPI Analog	MIPI_AVDD1V8/GPIO7_VCC1V8	1.62	1.8	1.98	V
Voltage for DDR PHY PLL	DDR_PLL_AVDD1V8	TBD	1.8	TBD	V

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Тур	Max	Unit
	Input Low Voltage	Vil	-0.3	NA	0.8	V

	Parameters	Symbol	Min	Тур	Max	Unit
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
Digital GPIO @3.3V	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
3.31	Pullup Resistor	Rpu	16	25	43	Kohm
	Pulldown Resistor	Rpd	16	25	43	Kohm
	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
Digital GPIO	Output Low Voltage	Vol	-0.3	NA	0.4	V
@1.8V	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	25	43	Kohm
	Pulldown Resistor	Rpd	16	25	43	Kohm

	Parameters	Symbol	Min	Тур	Max	Unit
	Common-mod voltage HS receive mode	VCMRX(DC)	0.8	NA	1.32	V
	Differential input high threshold	VIDTH	NA	NA	70	mV
MIPI_LVDS Combo IO@LVDS	Differential input low threshold	VIDTL	-70	NA	NA	mV
HS receiver mode	Single-ended input high voltage	VIHHS	NA	NA	1.5	V
	Single-ended input low voltage	VILHS	-40	NA	NA	mV
	Differential input impedance	ZID	80	100	125	ohm
	Common-mod voltage HS receive mode	VCMRX(DC)	70	NA	300	mV
	Differential input high threshold	VIDTH	NA	NA	70	mV
	Differential input low threshold	VIDTL	-70	NA	NA	mV
MIPI_LVDS Combo IO@ MIPI HS receiver mode	Single-ended input high voltage	VIHHS	NA	NA	460	mV
	Single-ended input low voltage	VILHS	-40	NA	NA	mV
	Single-ended threshold for HS termination enable	VTERM-EN	NA	NA	450	mV
	Differential input impedance	ZID	80	100	125	ohm
	Logic 1 input voltage	VIH	880	NA	NA	mV
MIPI_LVDS Combo IO@ MIPI	Logic 0 input voltage, not in ULP State	VIL	NA	NA	550	mV
LP receiver mode	Logic 0 input voltage, ULP State	VIL-ULPS	NA	NA	300	mV
	Input hysteresis	VHYST	25	NA	NA	mV
MIPI LVDS	Logic 1 input voltage	VIH	1.2	NA	1.58	V
Combo IO@ 1.8V	Logic 0 input voltage, not in ULP State	VIL	NA	NA	0.6	V
TTL RX mode	Input hysteresis	VHYST	25	NA	NA	mV

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Тур	Max	Unit
	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
, v	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
D: :: 1 0070		Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
Digital GPIO @3.3V	High level input current		Vin = 3.3V, pulldown enabled	NA	NA	10	uA
		Vin = 0V, pullup disabled	NA	NA	10	uA	
	Low level input current	Iil	Vin = 0V, pullup enabled	NA	NA	10	uA

	Parameters	Symbol	Test condition	Min	Тур	Max	Unit
	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
Digital GPIO	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
@1.8V			Vin = 1.8V, pulldown enabled	NA	NA	10	uA
		Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
	Low level input current		Vin = 0V, pullup enabled	NA	NA	10	uA

Note: VDDO and DVDD are both IO power Supply

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Para	Parameters		Test condition	Min	Тур	Max	Unit			
	Input clock frequency(Frac)	F _{in}	Fin = FREF @1.8V/0.99V	10	NA	800	MHz			
	VCO operating range	F _{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	475	NA	1900	MHz			
	Output clock frequency	Fout	Fout = Fvco/POSTDIV @3.3V/0.99V	9	NA	1900	MHz			
	Lock time	T _{It}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	1000	1500	Input clock cycles			

Table 3-6 Electrical Characteristics for FRAC PLL

Para	Parameters		Test condition	Min	Тур	Max	Unit
	Input clock frequency(Frac)	Fin	Fin = FREF @1.8V/0.99V	1	NA	1200	MHz
	VCO operating range	F _{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	950	NA	3800	MHz
	Output clock frequency	Fout	Fout = Fvco/POSTDIV @3.3V/0.99V	19	NA	3800	MHz
	Lock time	Tıt	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

- ① REFDIV is the input divider value;
 ② FBDIV is the feedback divider value;
- ③ POSTDIV is the output divider value

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-7 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Тур	Max	Unit
	•	Transmitter	•			
Output varietanes	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
Output resistance	ROUT	HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
	VIVI	HS mode	0.175	0.2	0.225	V
		Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
Differential output signal high	VOH	Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
		Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
Differential output signal low	VOL	Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
		Receiver				
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV

Parameters	Symbol	Test condition	Min	Тур	Max	Unit
		HS mode	NA	+-25	NA	mV
		Classic mode	0.8	1.65	2.5	V
Receiver common mode	RCM	HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	٧
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for MIPI CSI interface

Table 3-8 HS Receiver AC specifications (for MIPI mode)

Parameters	Symbol	Min	Тур	Max	Unit
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	NA	NA	100	mV
Common-mode interference 50MHz – 450MHz	ΔVCMRX(LF)	-50	NA	50	mV
Common-mode termination	CCM	NA	NA	60	pF

Table 3-9 LP Receiver AC specifications (for MIPI mode)

Parameters	Symbol	Min	Тур	Max	Unit
Input pulse rejection	eSPIKE	NA	NA	300	V.ps
Minimum pulse width response	TMIN-RX	20	NA	NA	ns
Peak interference amplitude	VINT	NA	NA	200	mv
Interference frequency	fINT	450	NA	NA	MHz

Table 3-10 HS Receiver AC specifications (for LVDS mode)

Parameters	Symbol	Min	Тур	Max	Unit
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	NA	NA	100	mV
Common-mode interference 50MHz – 450MHz	ΔVCMRX(LF)	-50	NA	50	mV
Common-mode termination	CCM	NA	NA	50	pF

3.8 Electrical Characteristics for Audio CODEC interface

Table 3-11 Electrical Characteristics for Audio CODEC

Test conditions: AVDD = 1.8V, DVDD = 0.8V, TA = 25°C, 1KHz Sine Input, Fs = 48KHz

Parameters	Symbol	Test condition	Min	Тур	Max	Units
	Or	perating Condition	on	•	<u>.</u>	•
Analog Supply	AVDD		1.62	1.8	1.98	V
Digital Supply	DVDD		0.81	0.9	0.99	V
	ſ	Microphone Bias				
Bias Voltage	V _{MICB}		0.8*AVDD	NA	0.975*AVDD	V
Bias Current	I _{MICB}		NA	NA	3	mA
	Microp	hone Gain Boos	t PGA			
Programmable Gain	G _{BST}		0	NA	20	dB
Gain Step Size			NA	20	NA	dB
Input Decistance	D	G _{BST} =0dB	NA	44	NA	ΚΩ
Input Resistance	R _{IN}	G _{BST} =20dB	NA	8	NA	ΚΩ
Input Capacitance	C _{IN}		NA	10	NA	pF
		ALC PGA				
Programmable Gain	G _{ALC}		-9	NA	37.5	dB
Gain Step Size			NA	1.5	NA	dB
		ADC				

Parameters	Symbol	Test condition	Min	Тур	Max	Units
Signal to Noise Ratio	SNR	A-weighted	NA	92	NA	dB
Total Harmonic Distortion	THD	-3dBFS input	NA	-80	NA	dB
Channel Separation			NA	80	NA	dB
Power Supply Rejection	PSRR	1KHz	NA	80	NA	dB
Digital Filter Pass Band Ripple			0.1	0.125	0.125	
	D	AC Line Output				
Programmable Gain	G _{DRV}		-39	NA	6	dB
Gain Step Size			NA	1.5	NA	dB
Signal to Noise Ratio	SNR	A-weighted	NA	93	NA	dB
Total Harmonic Distortion	THD	-3dBFS output 600Ω load	NA	-84	NA	dB
Power Supply Rejection	PSRR	1KHz	NA	55	NA	dB
	Pov	wer Consumption	า		X	
Standby			NA	0.01	NA	mA
Mono Recording			NA	2.5	NA	mA
Mono Playback		Quiescent output	NA	2.5	NA	mA

3.9 Electrical Characteristics for SARADC

Table 3-12 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Тур	Max	Unit
Resolution			NA	10	NA	bit
Effective Number of Bit	ENOB		NA	9	NA	bit
Differential Non-Linearity	DNL		-1	NA	+1	LSB
Integral Non-Linearity	INL		-2	NA	+2	LSB
Reference voltage	VREFP		NA	1.8	NA	V
Input Capacitance	C _{IN}		NA	8	NA	pF
Sampling Rate	fs		NA	NA	1	MS/s
Spurious Free Dynamic Range	SFDR	f _S =1MS/s f _{OUT} =1.17KHz	NA	61	NA	dB
Signal to Noise and Harmonic Ratio	SNDR		NA	56	NA	dB

3.10 Electrical Characteristics for TSADC

Table 3-13 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Тур	Max	Unit
Accuracy from -40°C to 125°C	TJACC		NA	NA	±3	°C
Sensing Temperature Range	T _{RANGE}		-40	NA	125	°C
Resolution	T _{LSB}		NA	0.6	NA	$^{\circ}$

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125°C.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	θ_{JA}	32.1	(°C/W)
Junction-to-board thermal resistance	θ_{JB}	12.5	(°C/W)
Junction-to-case thermal resistance	θ_{JC}	9.3	(°C/W)

Note: The JEDEC 2S2P PCB is 4 layers, 114.3mm*76.2mm.