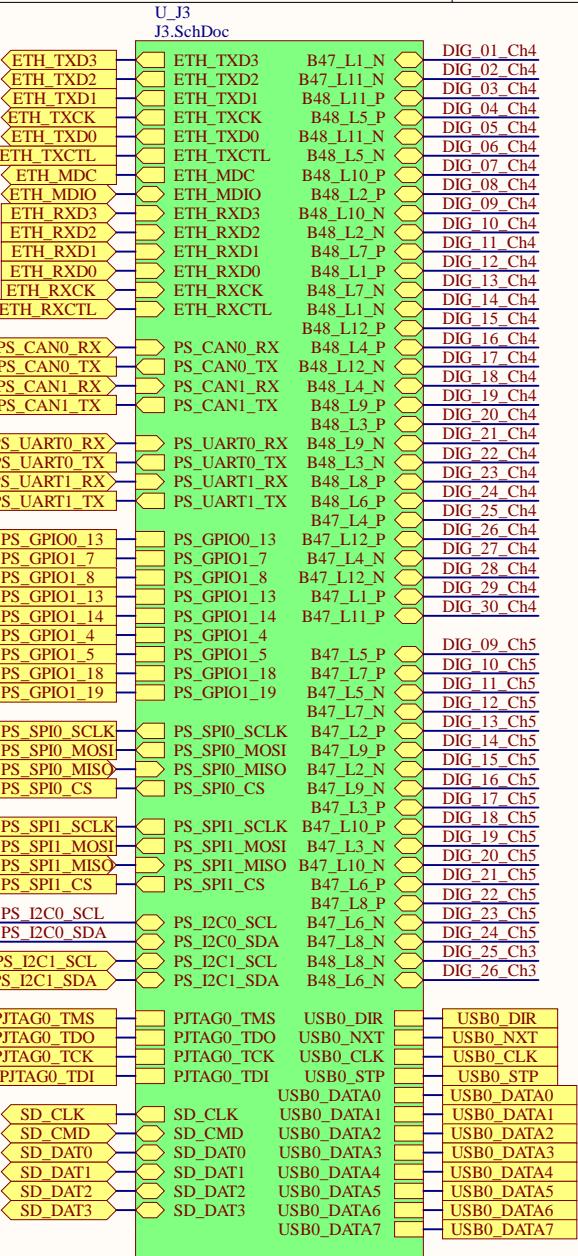
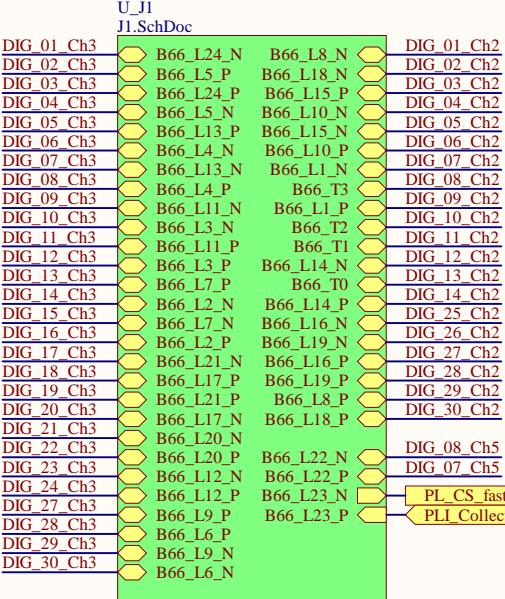
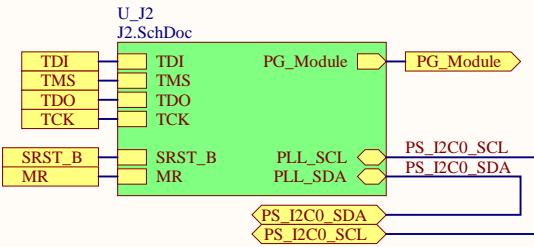
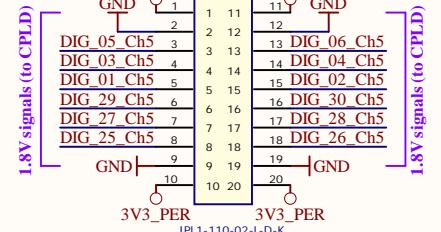


The 5th digital socket is not full connected with FPGA pins. DIG_01...DIG_06 and DIG_25...DIG_30 of this socket can be used externally via this connector.



Title: Board2Board.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	Cannot open file D:\Andrea s_Geiger0
Size: A4	Revision: 3v00		
Date: 07.12.2020	Time: 13:49:48	Sheet 2 of 22	Author: Andreas Geiger
Project: UltraZOhm CarrierBoard.PrjPcb			

A

B

C

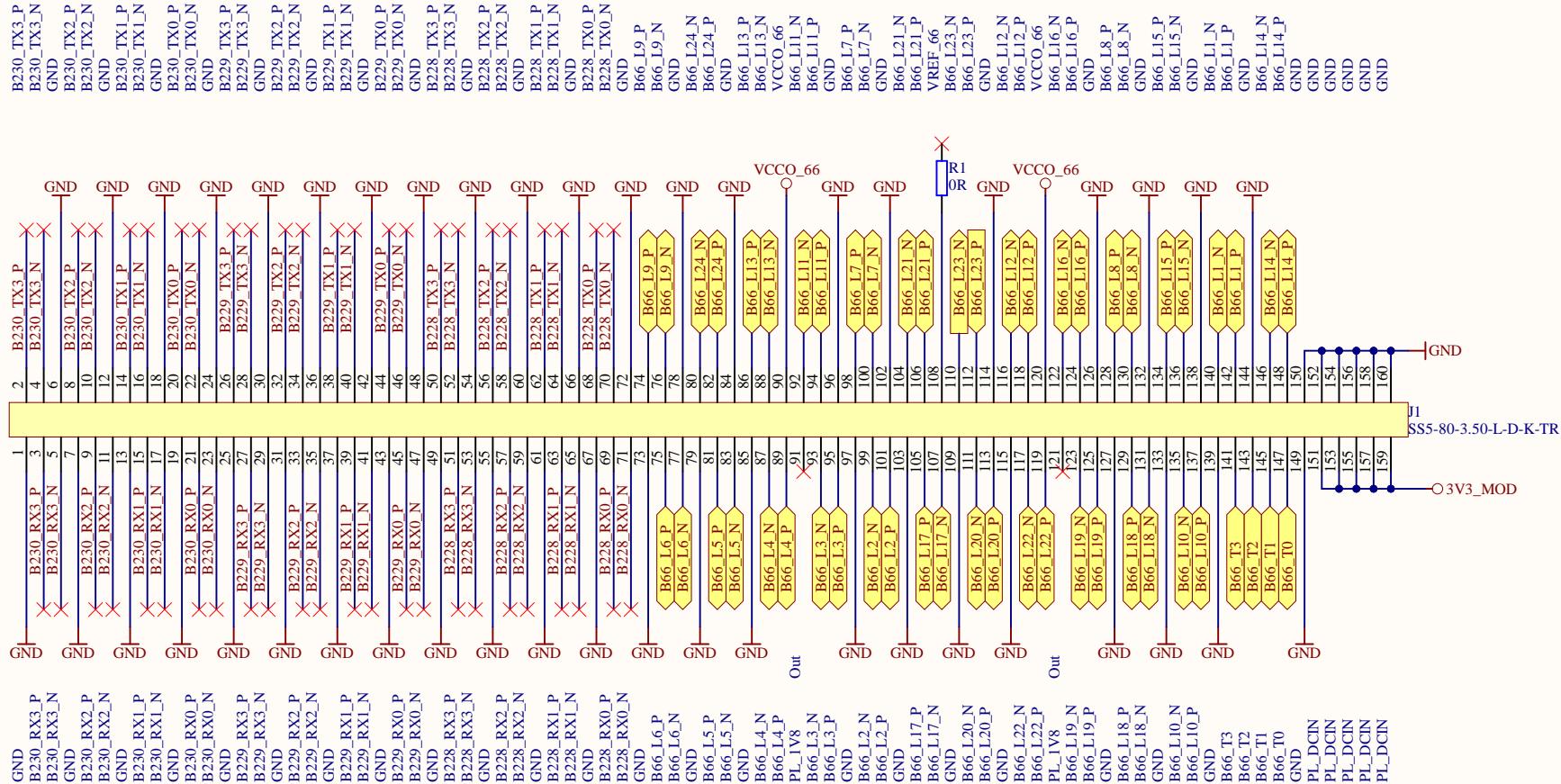
D

A

B

C

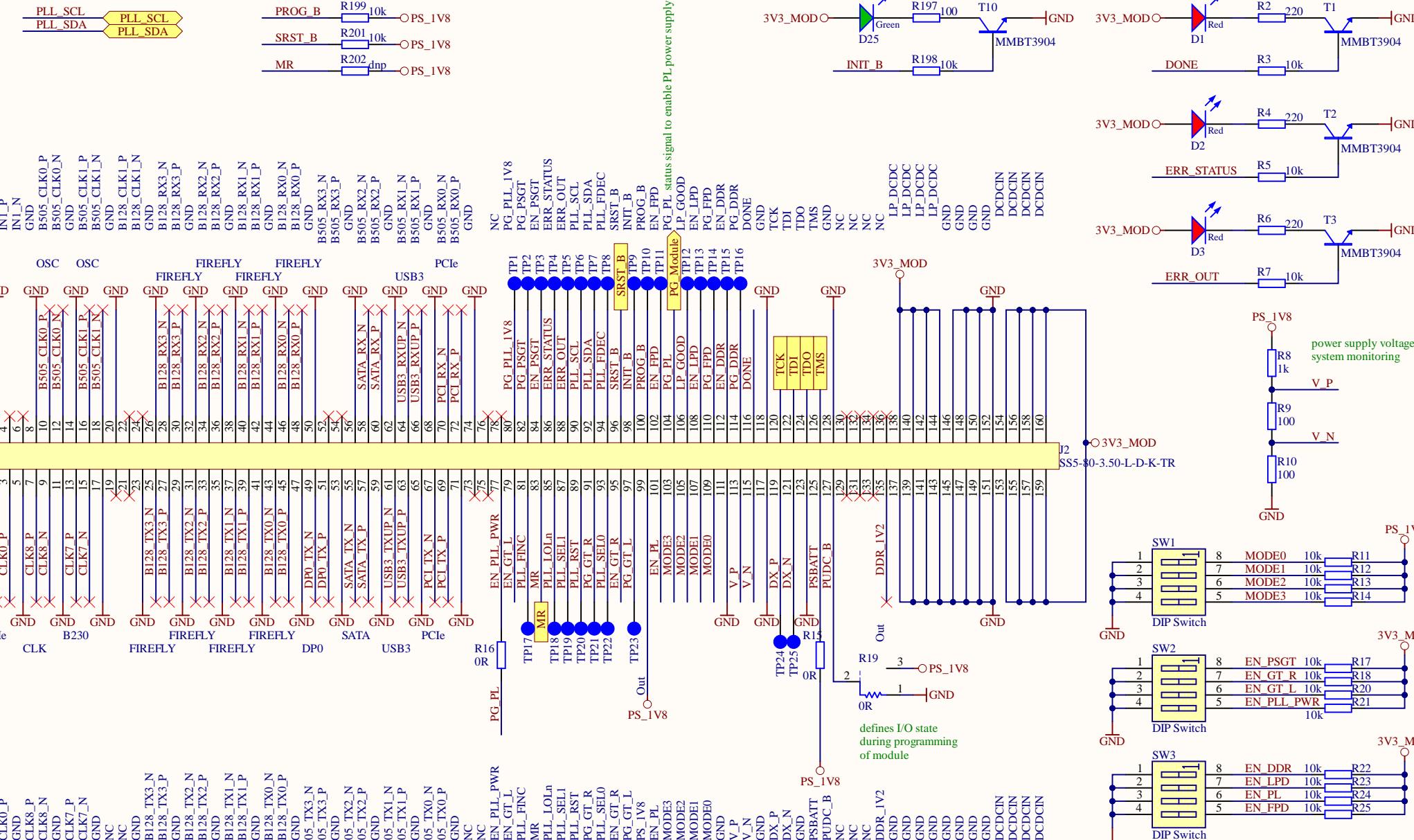
D



1V8 from Trenz U19 -> Not used

1V8 from Trenz U19 -> Not used

Title: J1.SchDoc	Size: A4	Revision: 3v00	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	Cannot open file D:\Andrea s_Geiger0
Date: 07.12.2020	Time: 13:49:48	Sheet 3 of 22	Author: Andreas Geiger	
Project: UltraZOHM CarrierBoard.PriPcb				



Title: J2.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0
Size: A4	Revision: 3v00	Date: 07.12.2020	Time: 13:49:49	
Project: UltraZOHM CarrierBoard.PriPcb	Sheet 4 of 22	Author: Andreas Geiger		

A

B

C

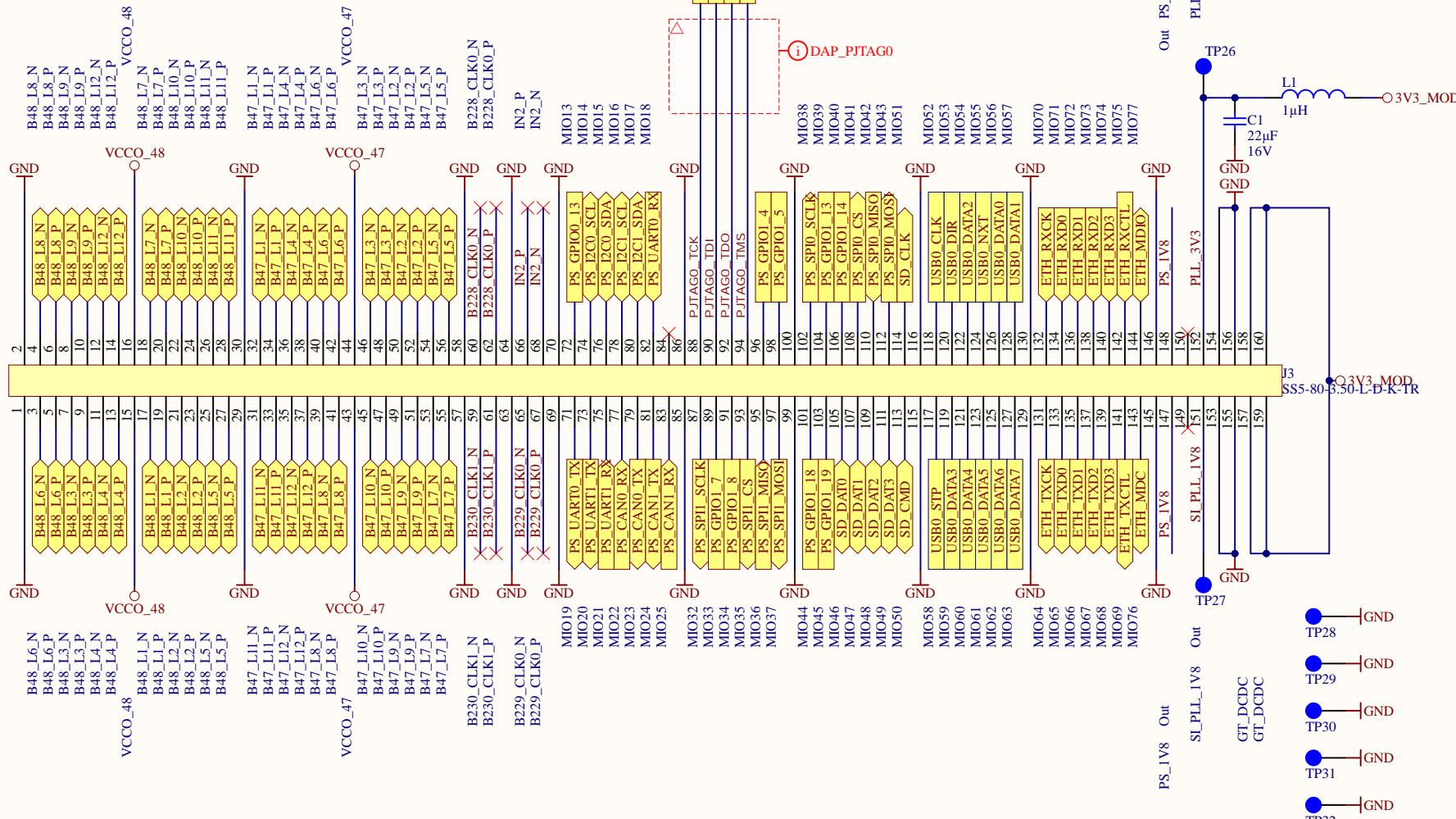
D

A

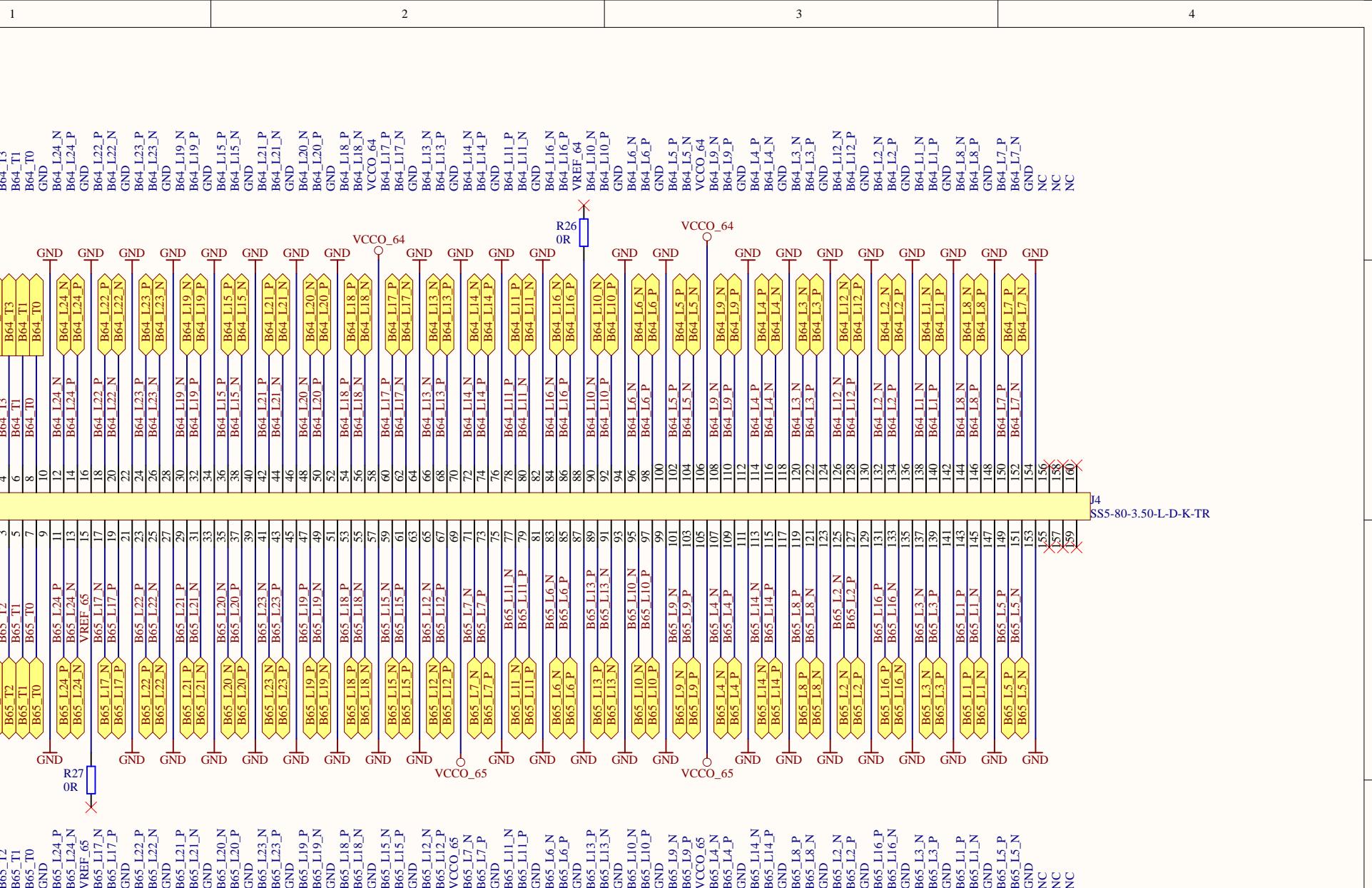
B

C

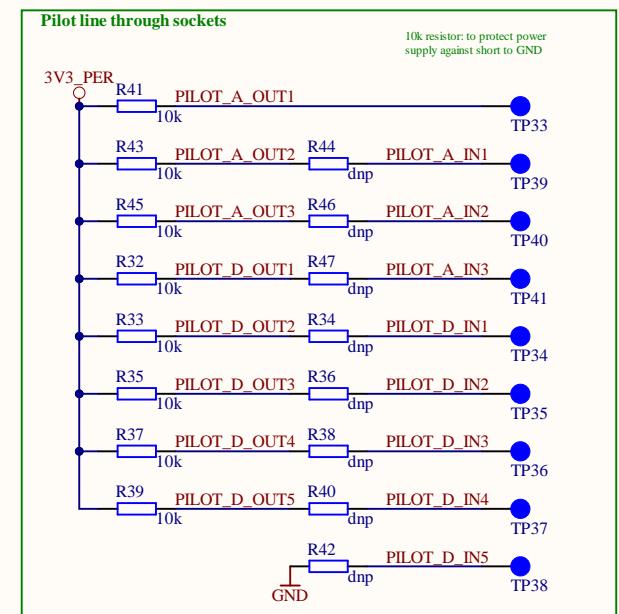
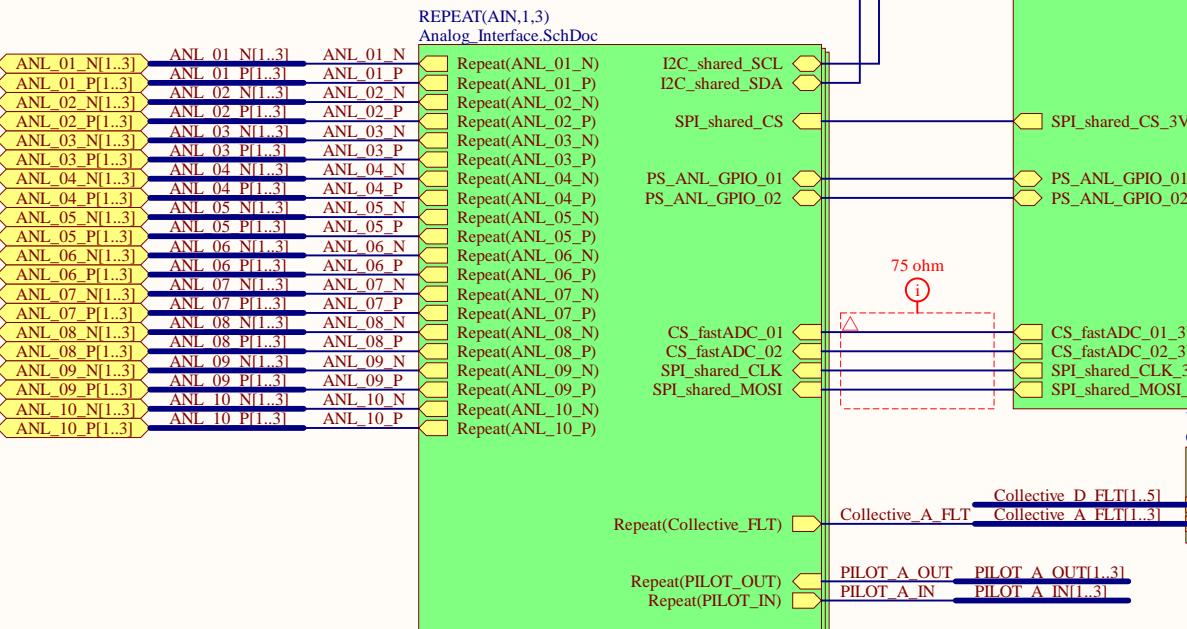
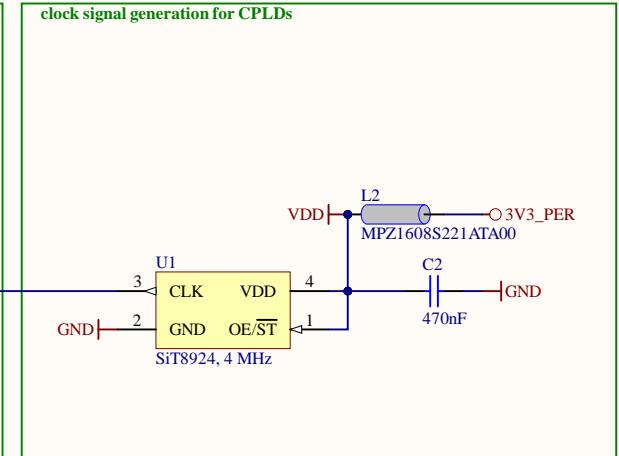
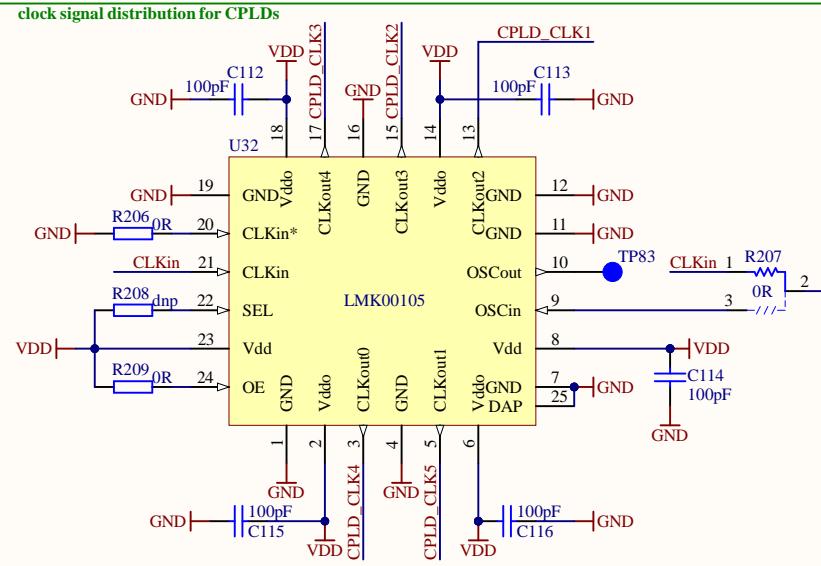
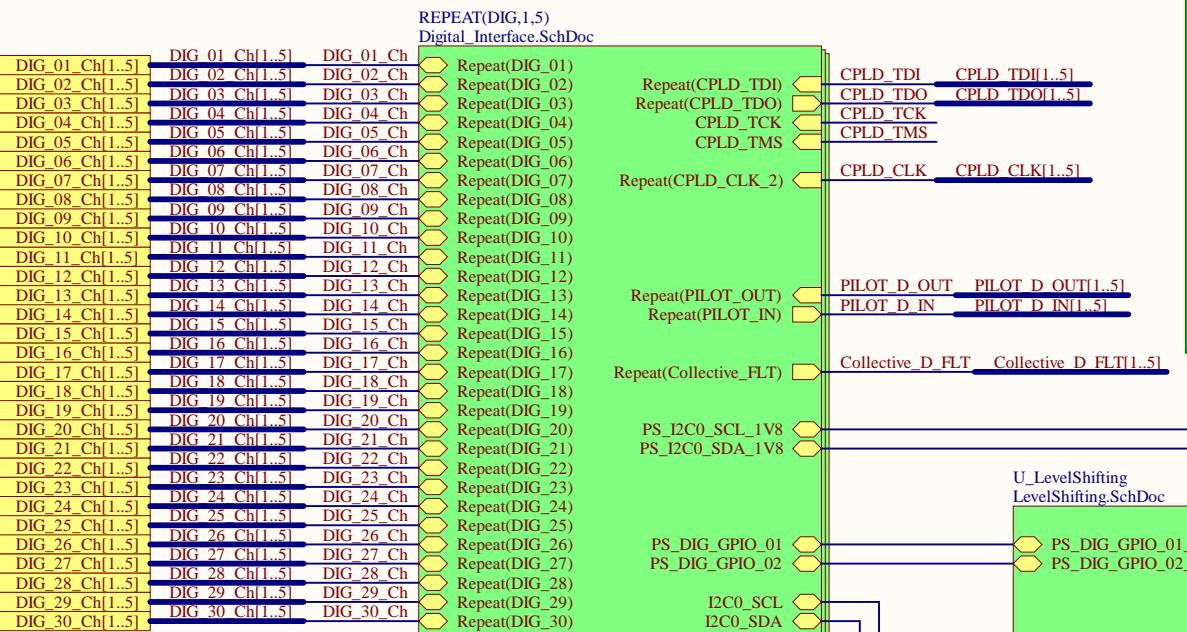
D



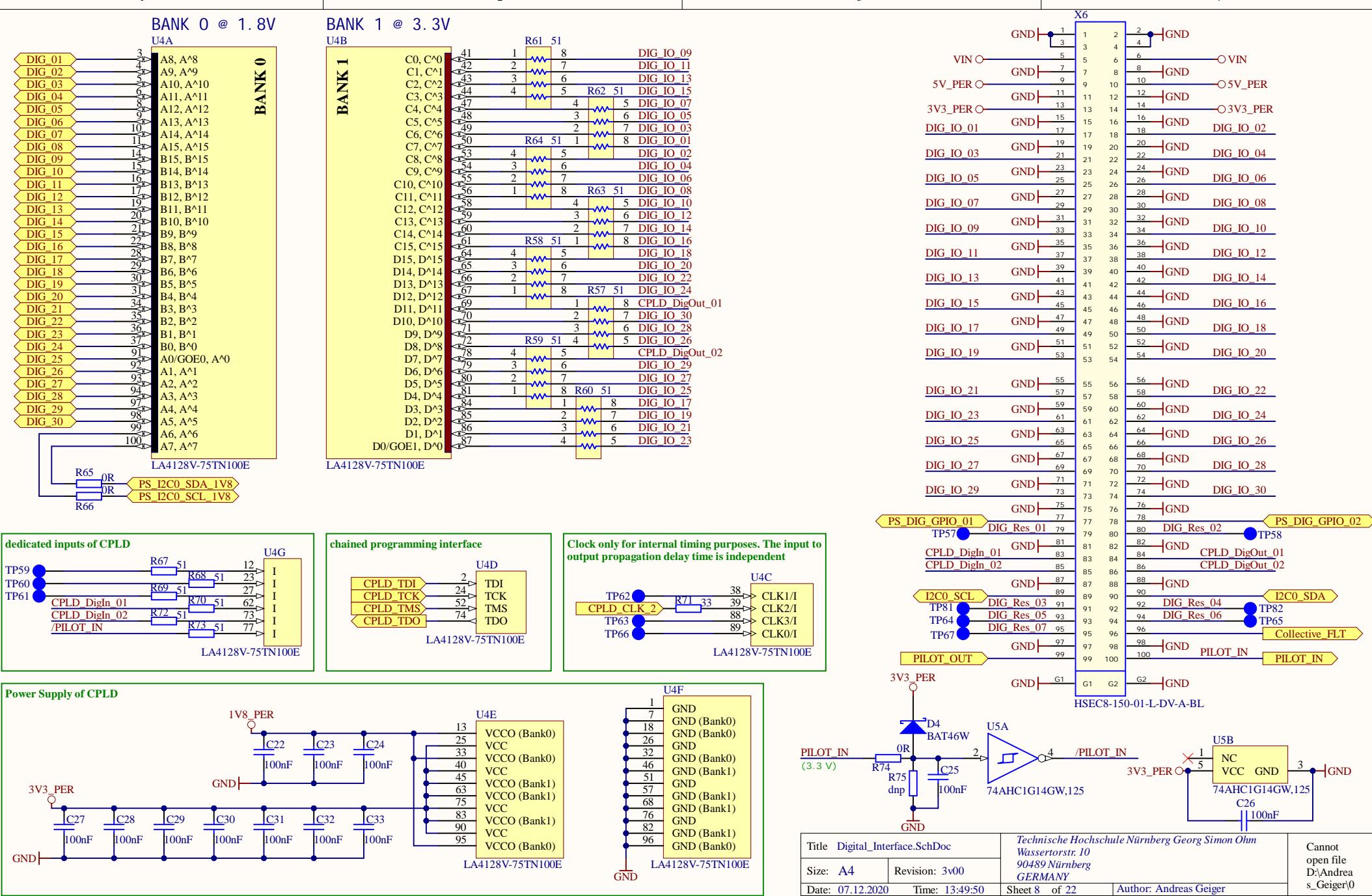
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Size: A4		Revision: 3v00			
Date: 07.12.2020 Time: 13:49:49		Sheet 5 of 22 Author: Andreas Geiger			
Project: UltraZOHM CarrierBoard.PriPcb					



Title J4.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0	
Size: A4		Revision: 3v00			
Date: 07.12.2020		Time: 13:49:49			
Project: UltraZOHM CarrierBoard.PriPcb		Sheet 6 of 22			



Title: Signal_Distribution.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wasserstr. 10 90489 Nürnberg GERMANY	
Size: B	Revision: 3v00	Cannot open file D:\Andrea s_Geiger\0
Date: 07.12.2020	Time: 13:49:49	Sheet 7 of 22 Author: Andreas Geiger
Project: UltraZOHM_CarrierBoard.PrjPcb		



A

B

C

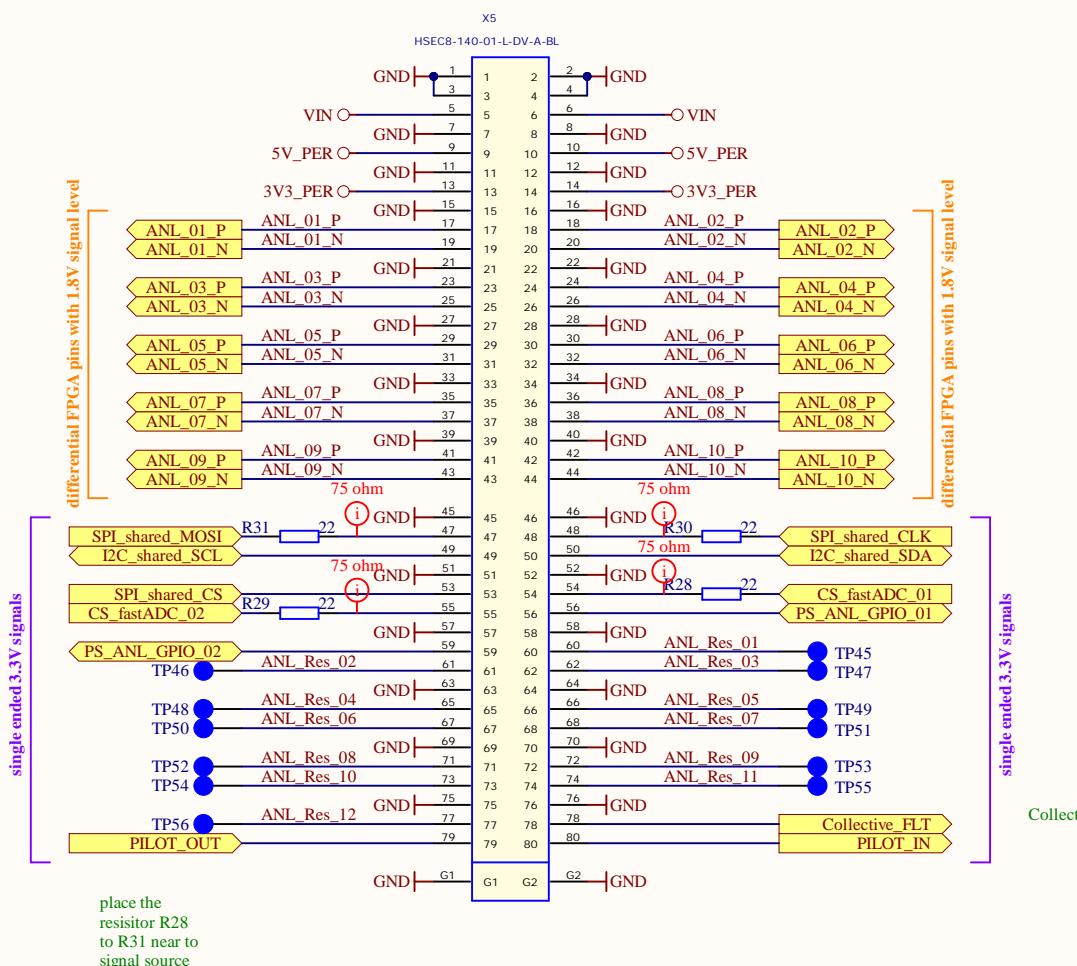
D

A

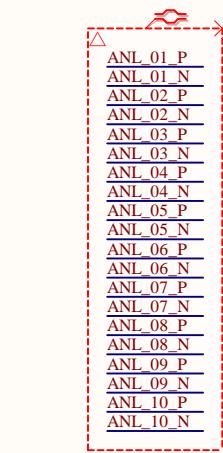
B

C

D



ANL_01_P
ANL_01_N
ANL_02_P
ANL_02_N
ANL_03_P
ANL_03_N
ANL_04_P
ANL_04_N
ANL_05_P
ANL_05_N
ANL_06_P
ANL_06_N
ANL_07_P
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ANL_09_P
ANL_09_N
ANL_10_P
ANL_10_N

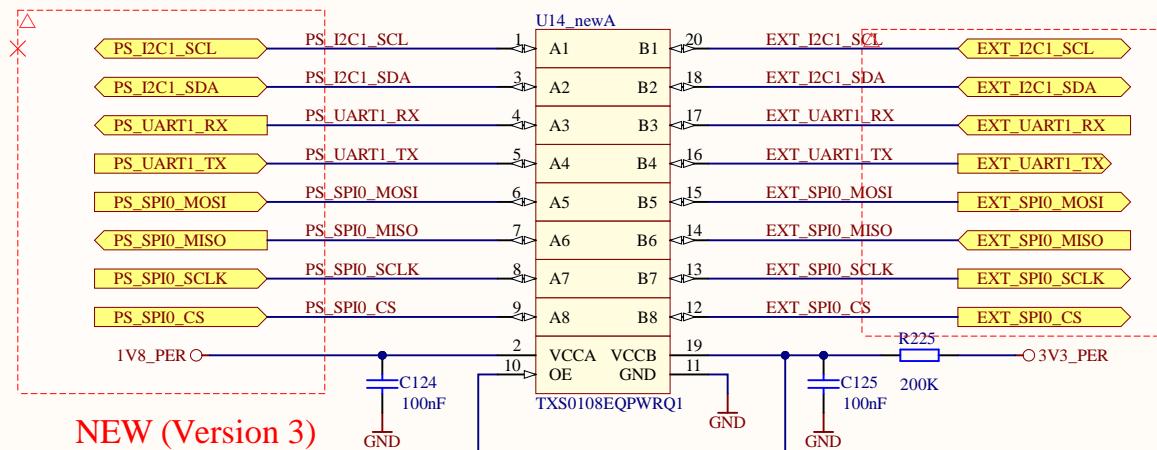


single ended 3.3V signals

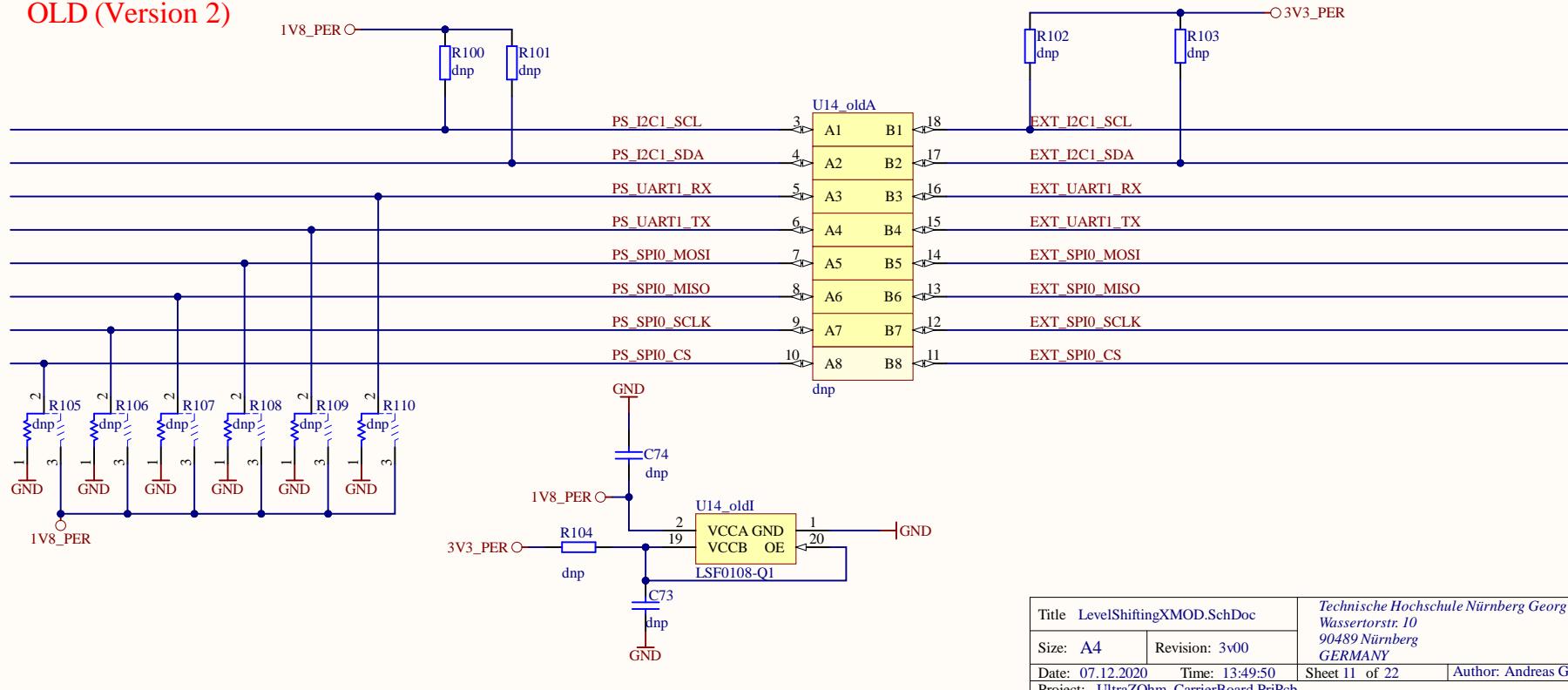
Collective_FAULT goes to all sockets

Title: Analog_Interface.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0
Size: A4	Revision: 3v00			
Date: 07.12.2020		Time: 13:49:50	Sheet 9 of 22	Author: Andreas Geiger
Project: UltraZOHM CarrierBoard.PrjPcb				

Bidirectional Level Shifting 1.8V to 3.3V



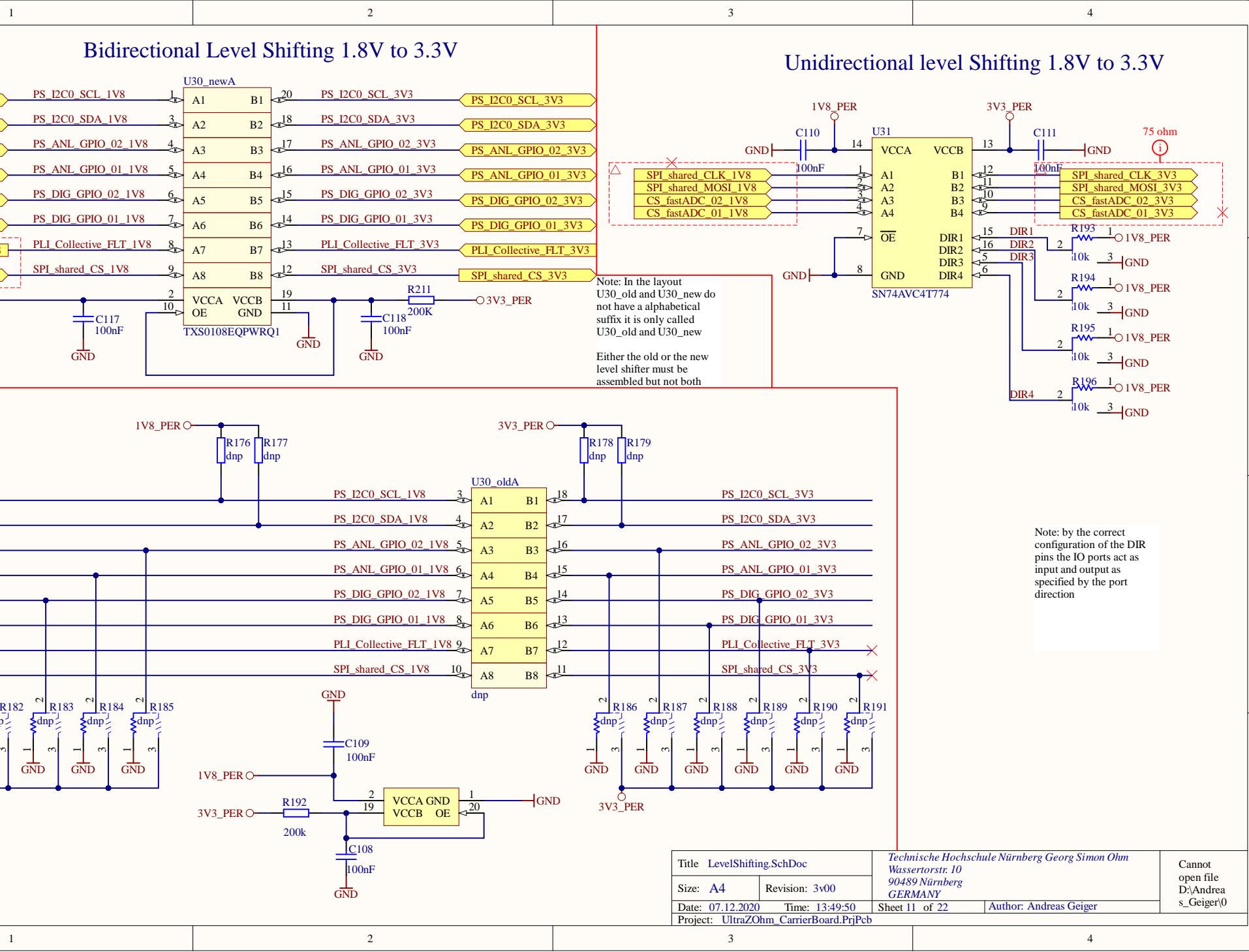
OLD (Version 2)



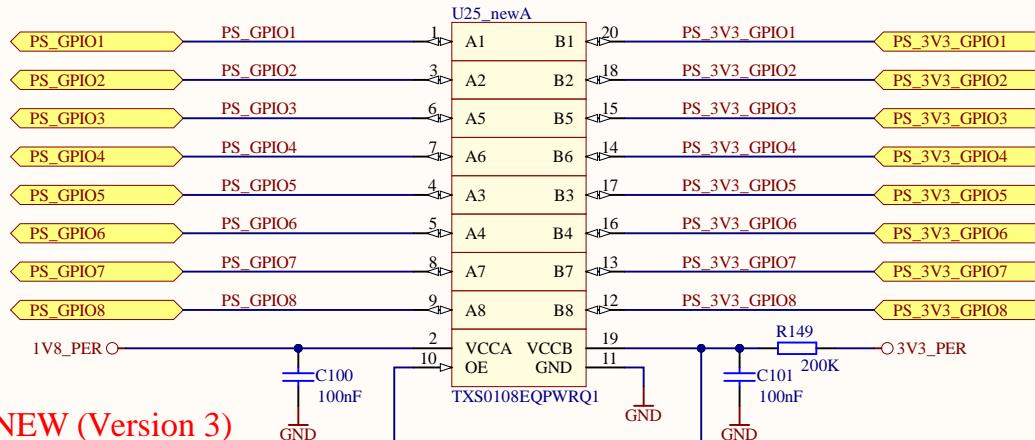
Note: In the layout
U14_old and U14_new do
not have a alphabetical
suffix it is only called
U14_old and U14_new.

Either the old or the new
level shifter must be
assembled but not both

Title: LevelShiftingXMOD.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 3v00	
Date: 07.12.2020	Time: 13:49:50	Sheet 11 of 22
Project: UltraZOHM CarrierBoard.PriPcb	Author: Andreas Geiger	



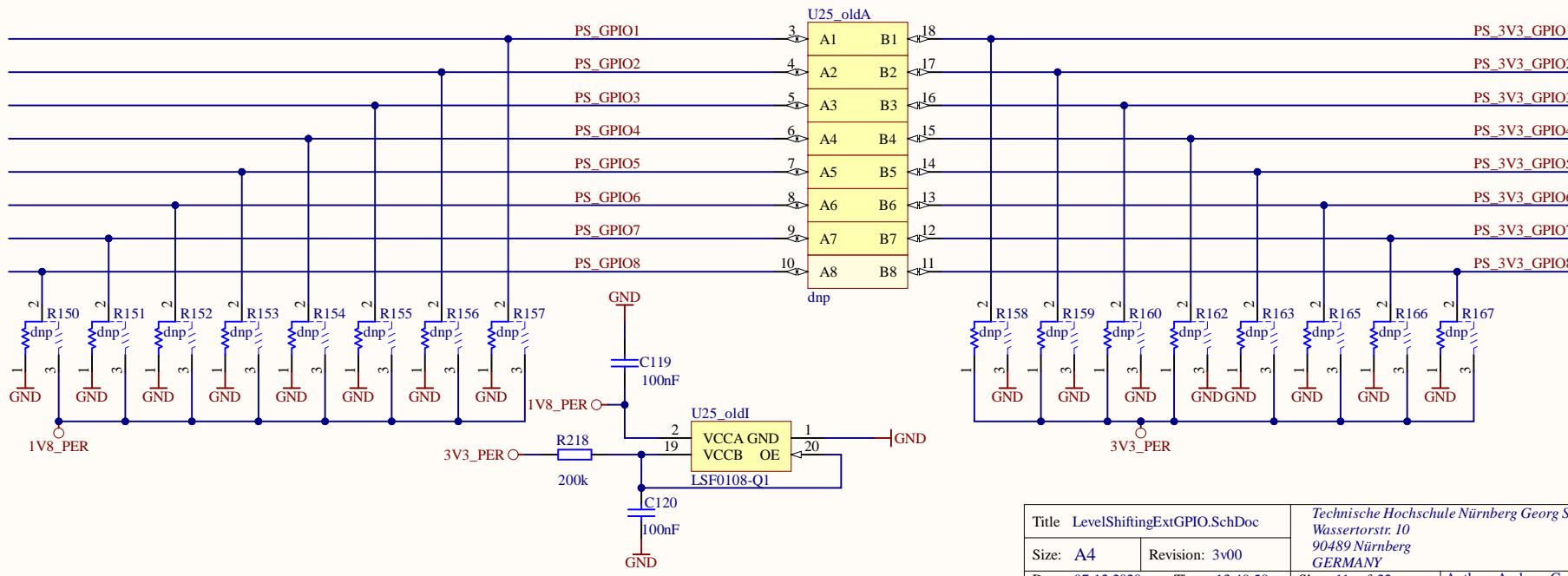
Bidirectional Level Shifting 1.8V to 3.3V



Note: In the layout
U25_old and U25_new do
not have a alphabetical
suffix it is only called
U25_old and U25_new.

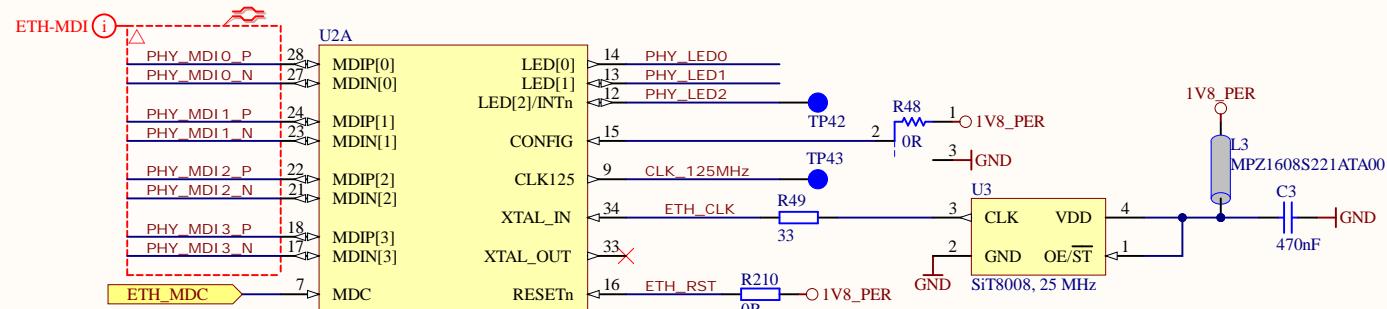
Either the old or the new
level shifter must be
assembled but not both

OLD (Version 2)

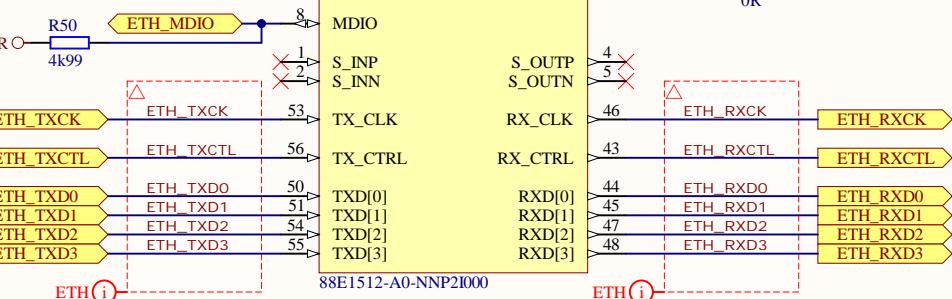


Title: LevelShiftingExtGPIO.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	Cannot open file D:\Andrea s_Geiger0
Size: A4	Revision: 3v00	
Date: 07.12.2020	Time: 13:49:50	Sheet 11 of 22 Author: Andreas Geiger
Project: UltraZOHM CarrierBoard.PriPcb		

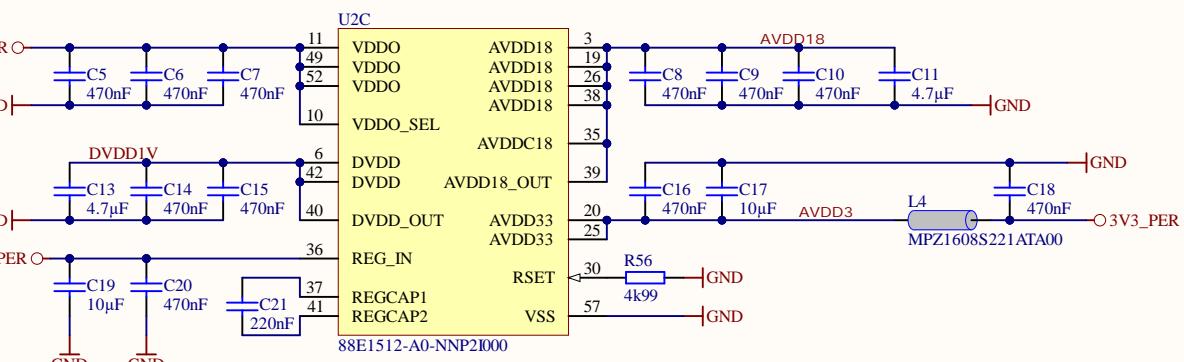
A



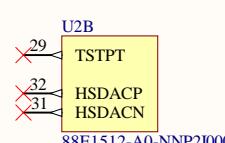
B



C



D



Title ETH-PHY.SchDoc

Size: A4

Revision: 3v00

Technische Hochschule Nürnberg Georg Simon Ohm
Wassertorstr. 10
90489 Nürnberg
GERMANY

Cannot open file
D:\Andrea
s_Geiger0

Date: 07.12.2020

Time: 13:49:50

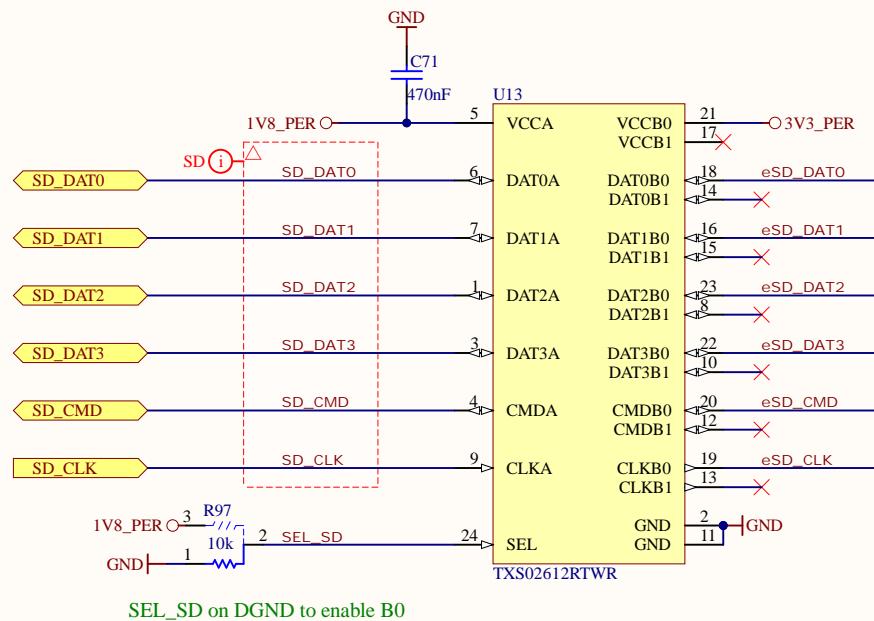
Sheet 12 of 22

Author: Andreas Geiger

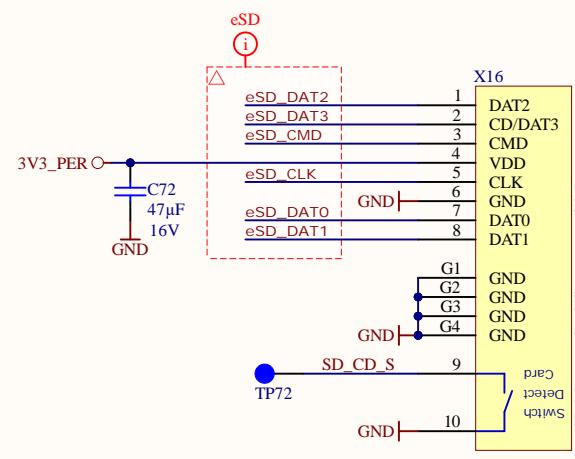
Project: UltraZOhm CarrierBoard.PriPcb

A

Bidirectional Level Shifting 1.8V to 3.3V



SD Card Connector

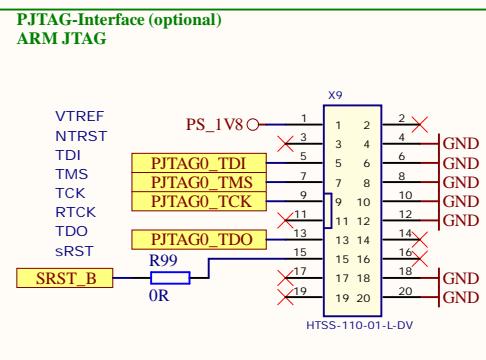
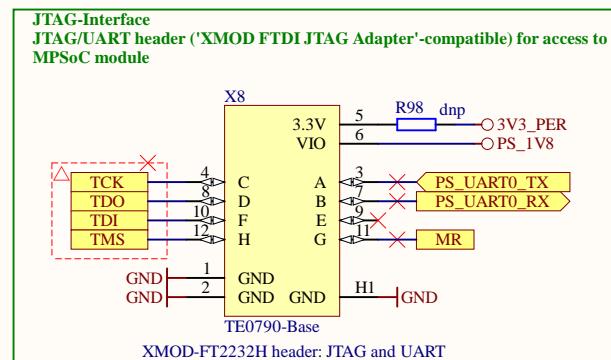


B

C

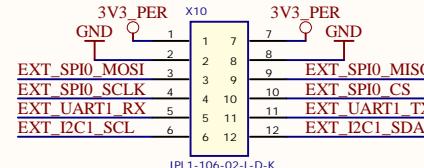
D

Title: SD_Card.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0
Size: A4	Revision: 3v00		
Date: 07.12.2020	Time: 13:49:50	Sheet 13 of 22	Author: Andreas Geiger
Project: UltraZOhm CarrierBoard.PrtPcb			

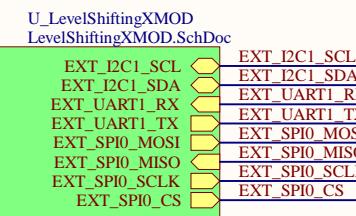


SPI, UART, I2C-Interface (from Processor System)

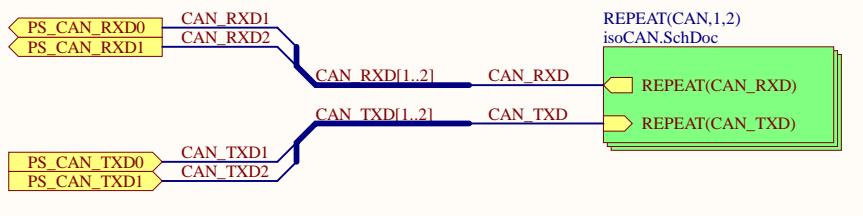
SPI, UART and I2C Connector @ 3.3V level



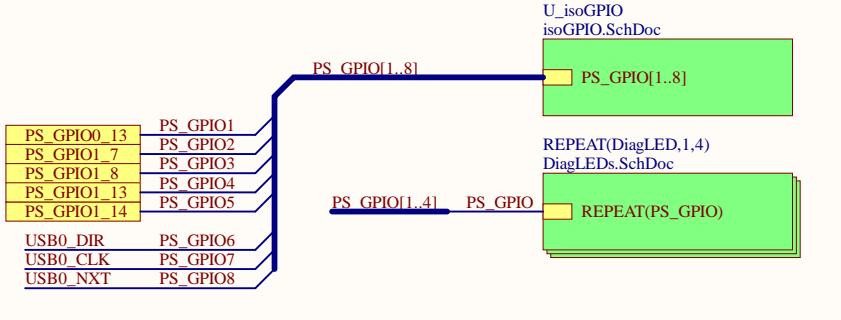
Bidirectional Level Shifting 1.8V to 3.3V



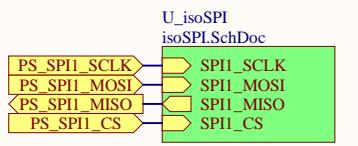
2x Isolated CAN-Interface
(renamed numbering, because multi channel design in Altium Designer starts with index 1 instead of 0)



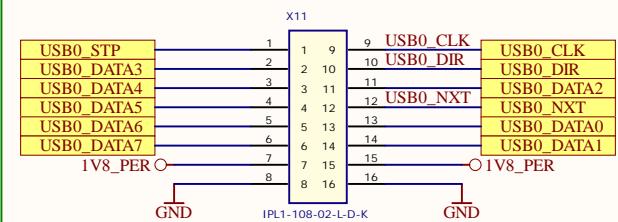
Isolated External GPIO Interface



Isolated SPI-Interface



USB Pins on Header (for use as extension port or pin use as GPIO)

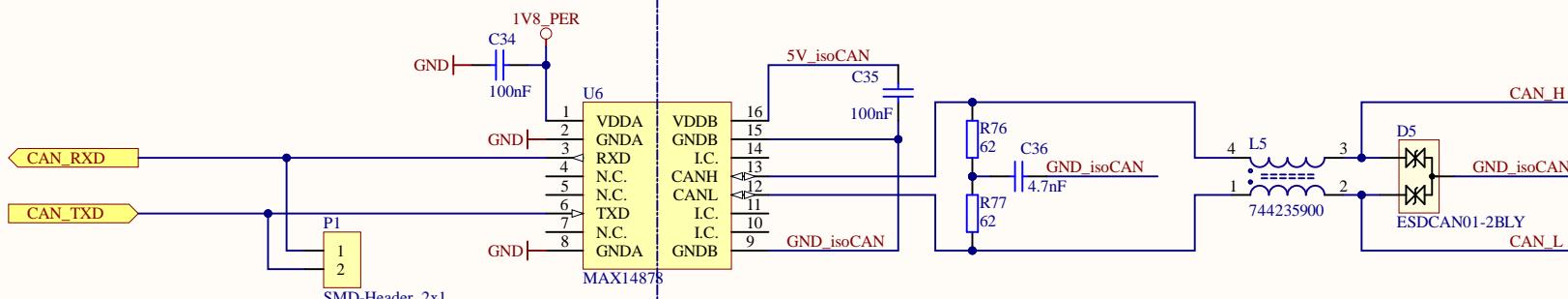


Title XMOD.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0
Size: A4	Revision: 3v00			
Date: 07.12.2020	Time: 13:49:51	Sheet 14 of 22	Author: Andreas Geiger	
Project: UltraZOHM CarrierBoard.PrjPcb				

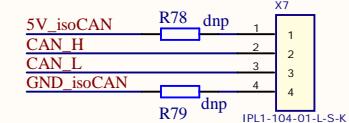
A

LV side

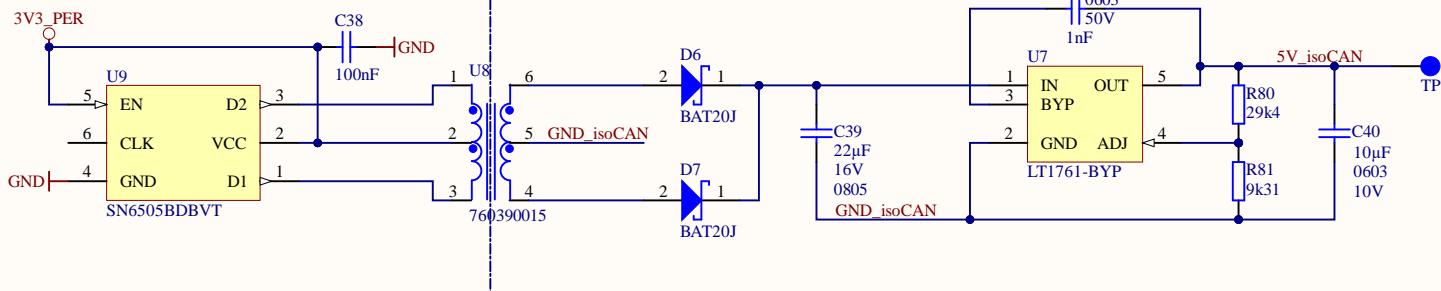
Isolated side



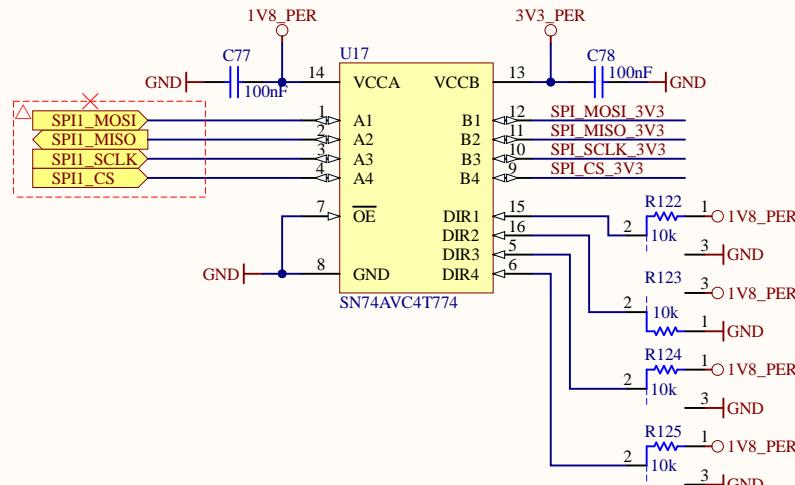
CAN Connector



Isolated Power Supply

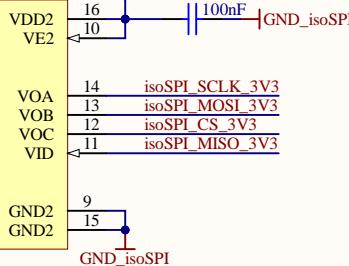


Level Shifting 1.8V to 3.3V

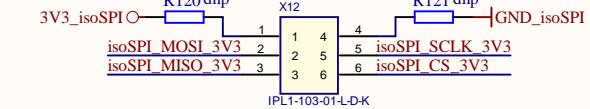


LV side

Isolated side



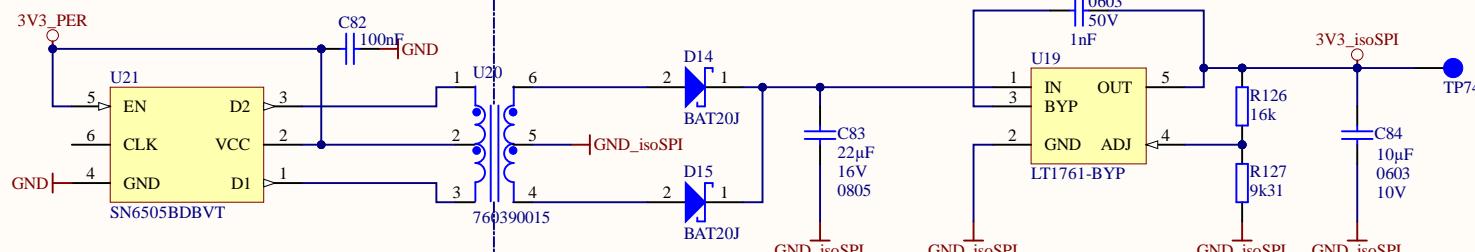
SPI Connector



take ADUM4402 if SoC acts as SPI slave

alternative pin-compatible part: Texas Instruments ISO7741DW

Isolated Power Supply



Bidirectional Level Shifting 1.8V to 3.3V

LV side

Isolated side

IO Protection with TVS-Diode and PTC-Resistor

A

B

C

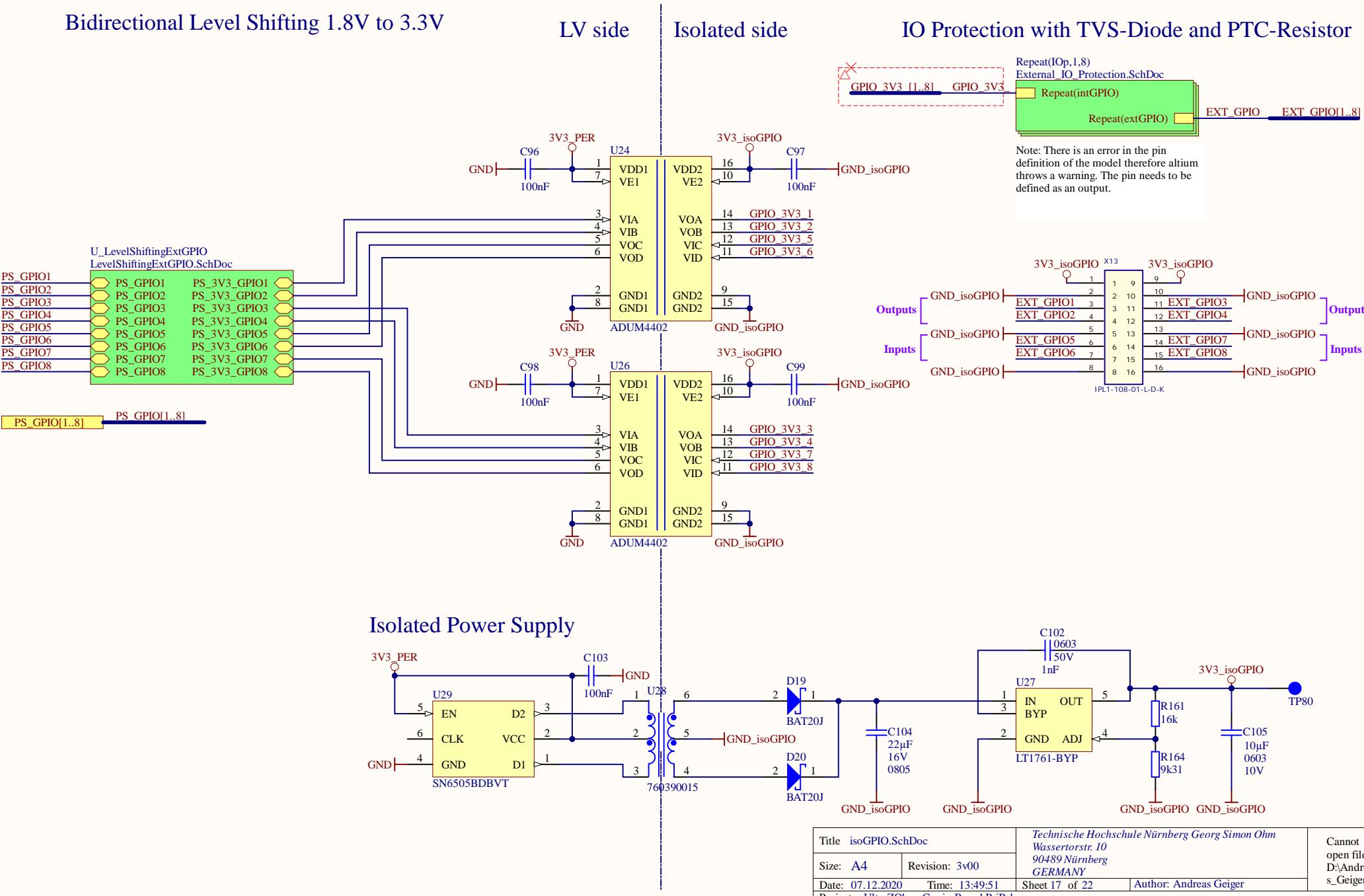
D

A

B

C

D



A

A

B

B

C

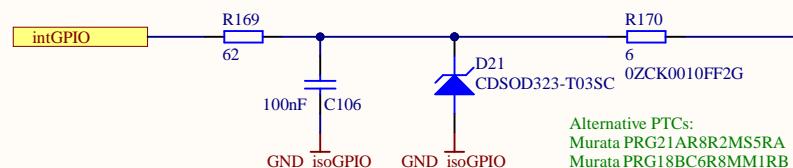
C

D

D

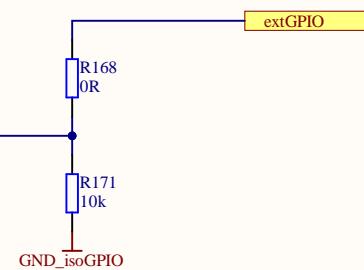
PTC for Overcurrent Protection

this resistor protects the IC-Pin of rest voltage at TVS diode



Alternative PTCs:
Murata PRG21AR8R2MS5RA
Murata PRG18BC6R8MM1RB

Voltage Divider



Title: External_IO_Protection.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0	
Size: A4	Revision: 3v00			
Date: 07.12.2020	Time: 13:49:51			
Project: UltraZOhm CarrierBoard.PriPcb	Sheet 18 of 22			

A

A

B

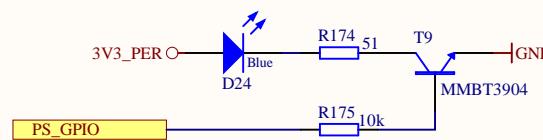
B

C

C

D

D



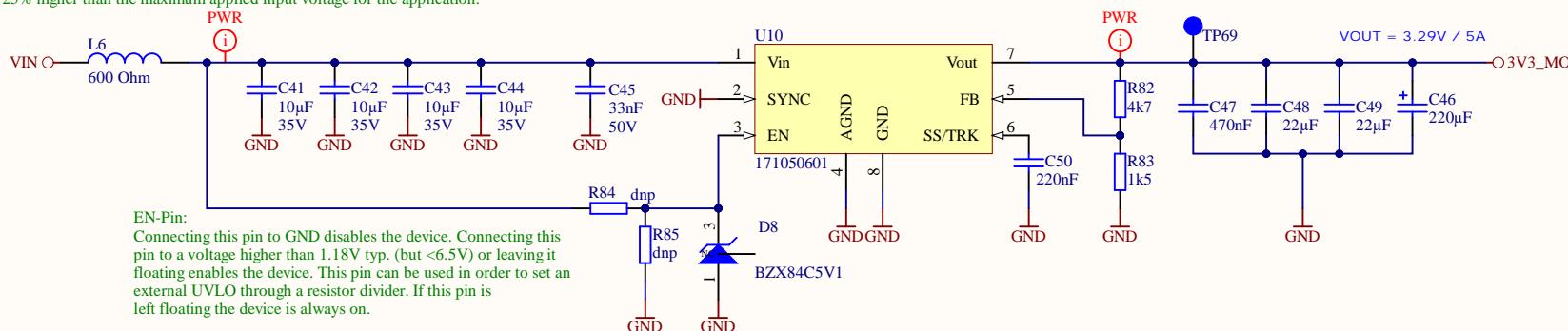
Title: DiagLEDs.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0	
Size: A4	Revision: 3v00			
Date: 07.12.2020	Time: 13:49:51	Sheet 19 of 22		
Project: UltraZOhm CarrierBoard.PrjPcb				

Notes: preferred to use 2x 22 μ F/50V capacitors at Vin, but this design uses 35V caps due to worse availability at distributors.

Datasheet: recommended minimum input capacitance is 22 μ F (including derating) ceramic with voltage rating

at least 25% higher than the maximum applied input voltage for the application.

A

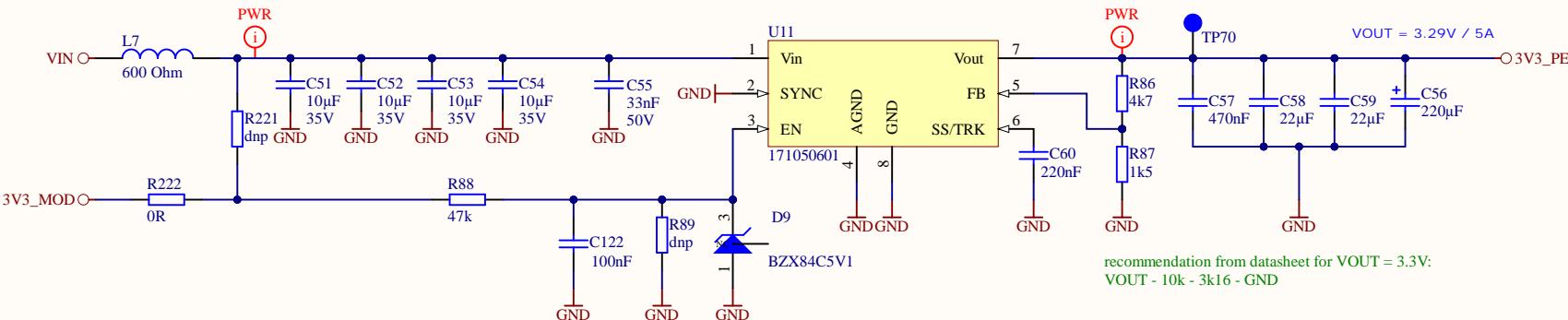


EN-Pin:

Connecting this pin to GND disables the device. Connecting this pin to a voltage higher than 1.18V typ. (but <6.5V) or leaving it floating enables the device. This pin can be used in order to set an external UVLO through a resistor divider. If this pin is left floating the device is always on.

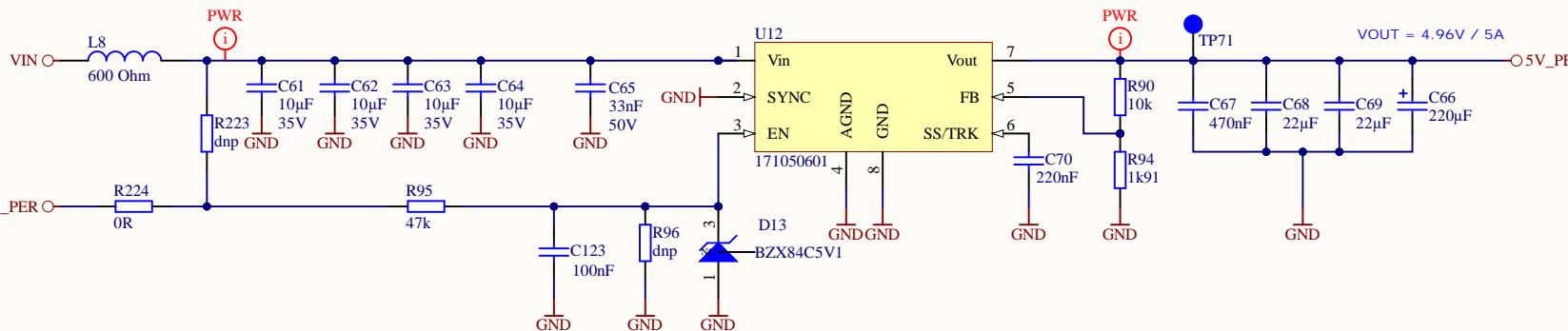
power supply for:
 - Trenz module (PL_1V8, PS_1V8, ...)

B



power supply for:
 - digital and analog sockets
 - SD-Card
 - Ethernet
 - CAN

C



power supply for:
 - digital and analog sockets

D The delay time between the power supplies U10 U11 and U12 is determined by R88 C122 R95 and C123. The delay time can be estimated as follows: $t_{on} = -\tau_{en} * \ln(1 - (U_{en}/U_{max}))$

$\tau_{en} = R*C$

$U_{en} = 1.27V$

U_{max} = output voltage of prior stage (e.g. 3V3)

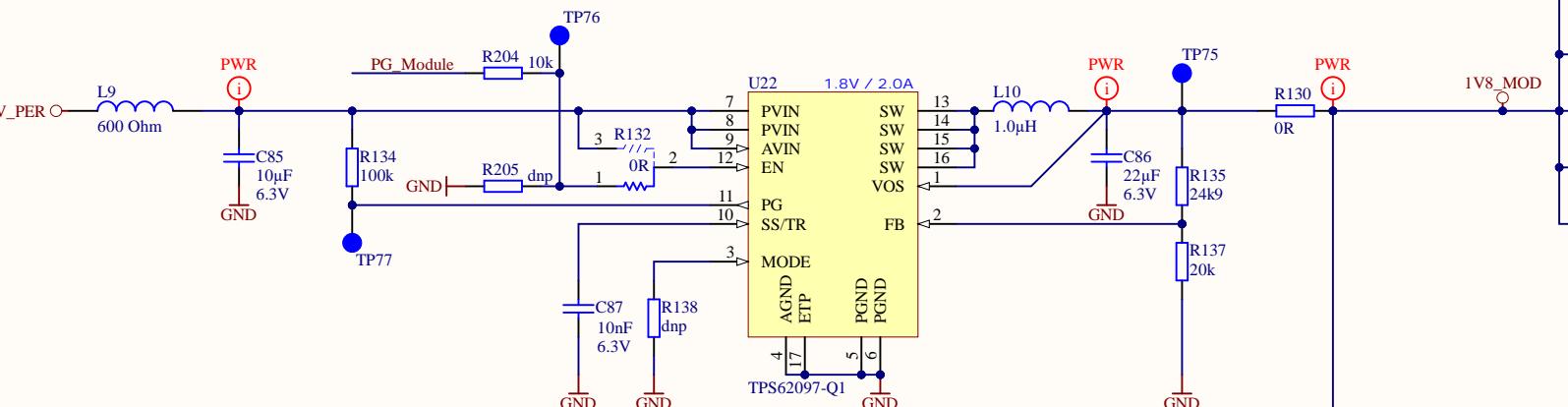
Since the input current of the EN pin is about 21 μ A the real delay time is a bit longer than the calculated value. With the values above there is a delay of about 5ms,

Title: Power_Supply_1.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0
Size: A4	Revision: 3v00		
Date: 07.12.2020	Time: 13:49:51	Sheet 20 of 22	Author: Andreas Geiger
Project: UltraZOHM CarrierBoard.PriPcb			

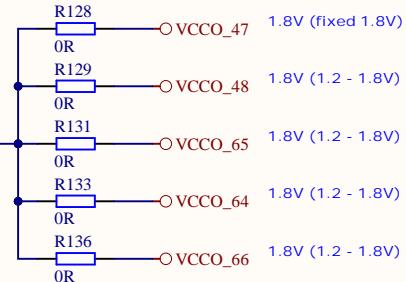
A

PG_Module

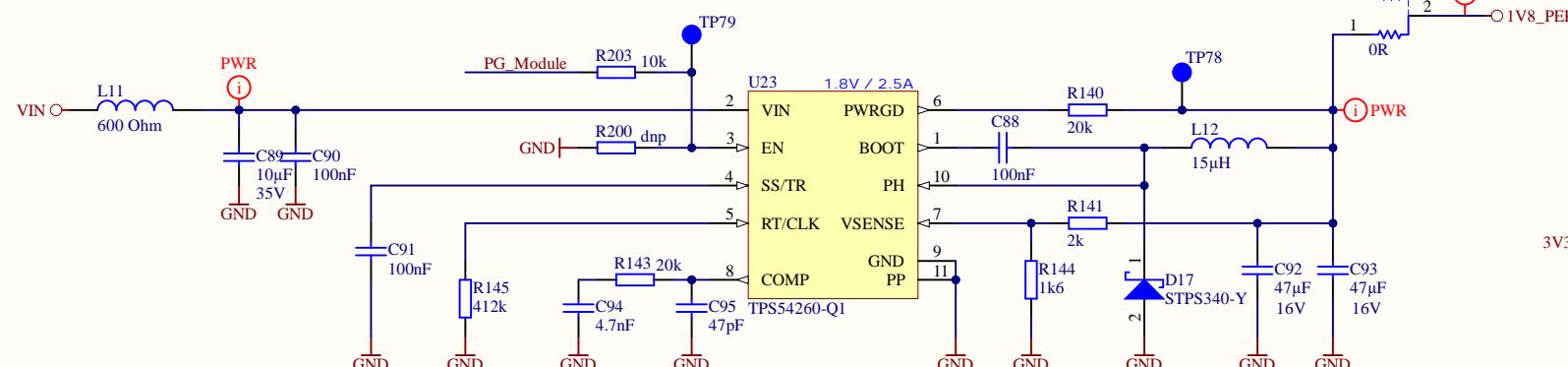
power good signal from Trenz module
to enable banks and peripherals after
module is supplied sufficiently



bank power supply with jumper selectable
(place near to Trenz module!)

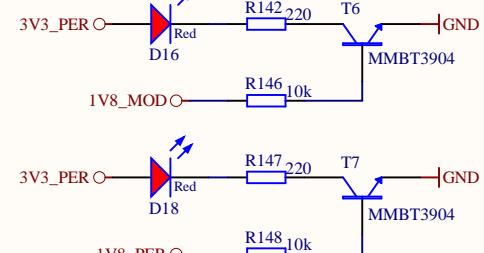


B



power supply for:

- CPLD Banks
- I2C Level Shifter
- Ethernet
- SD-Card Level Shifter
- JTAG Programmer
- CAN Transceiver
- SPI, UART, I2C-Interface Level Shifter
- Isolated SPI Level Shifter
- Isolated GPIO Level Shifter



Reference Design: TE0728

Reference Design: TPS82085SIL (TE0808/POWER.SchDoc) not in stock at distributors...

Title: Power_Supply_2.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		Cannot open file D:\Andrea s_Geiger0
Size: A4	Revision: 3v00		
Date: 07.12.2020	Time: 13:49:51		Sheet 21 of 22 Author: Andreas Geiger
Project: UltraZOHM CarrierBoard.PriPcb			

A

A

B

B

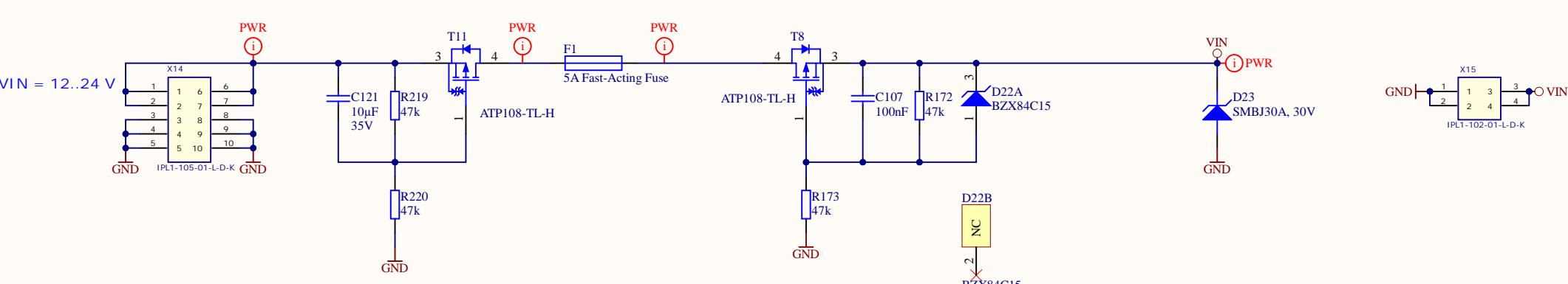
C

C

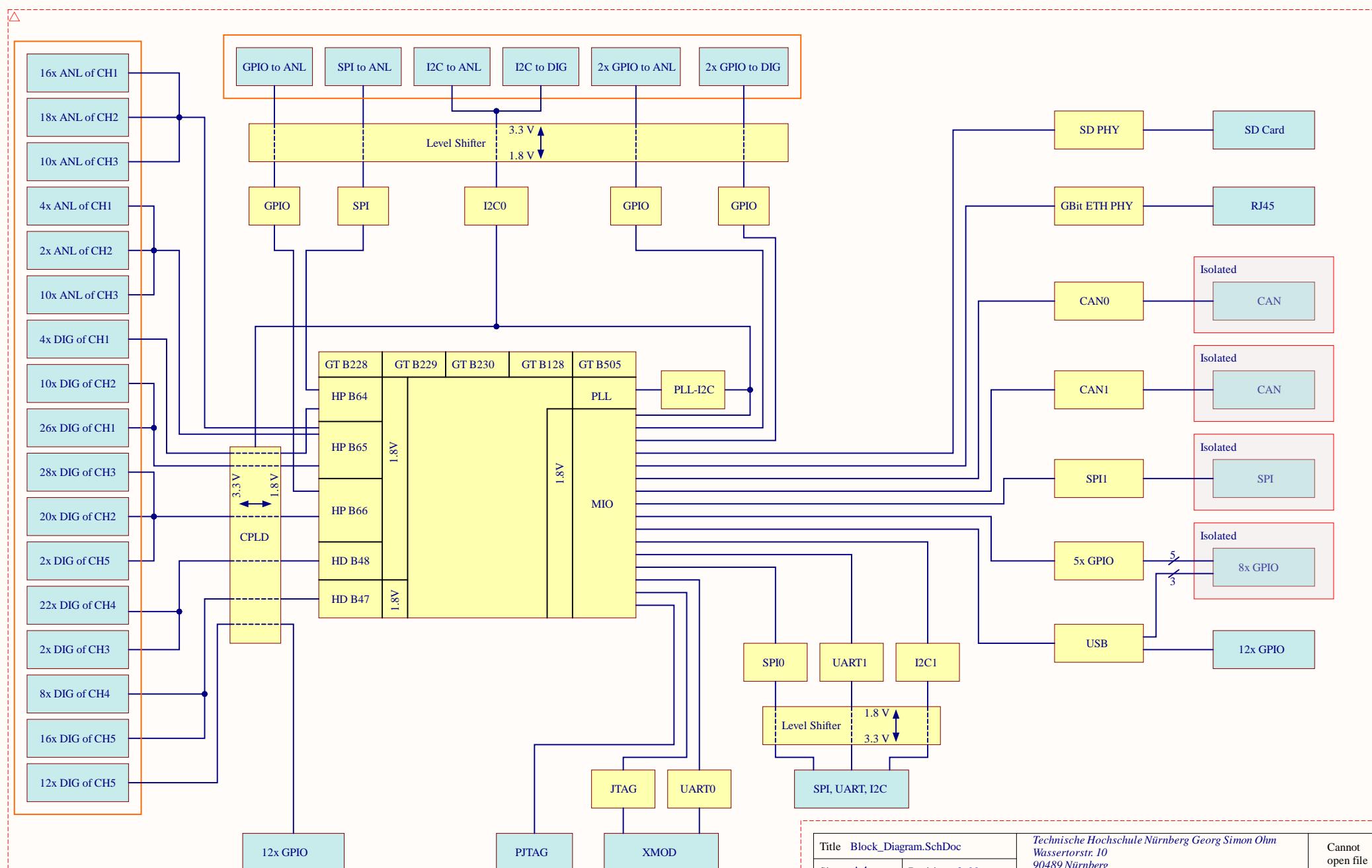
D

D

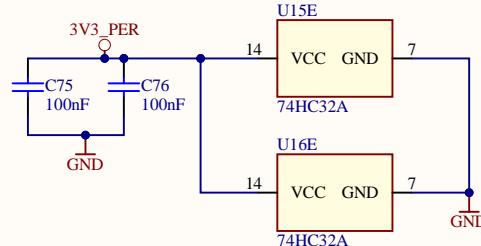
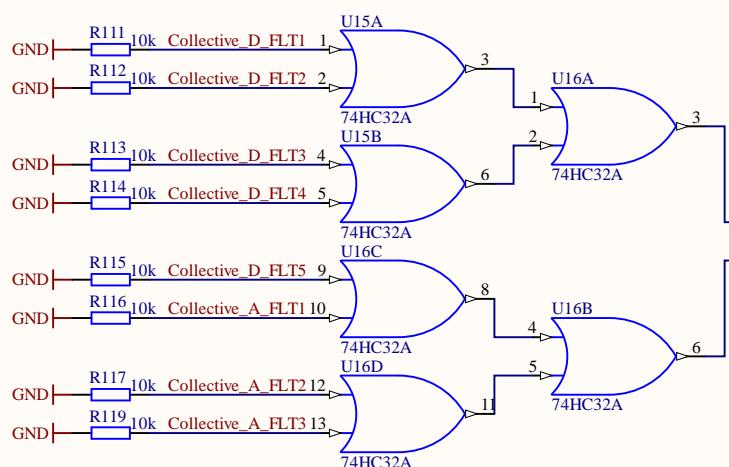
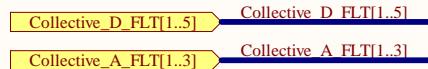
Switch on current limitation Short Circuit Protection Reverse Polarity Protection Overvoltage Protection



Title: Power_Supply_Input.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 3v00	
Date: 07.12.2020	Time: 13:49:51	Sheet 22 of 22 Author: Andreas Geiger
Project: UltraZOhm CarrierBoard.PjPcb		Cannot open file D:\Andreas Geiger\0



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PLI_Collective_FLT_3V3
Note: The collective fault goes to the bidirectional level shifter that's why altium throws a warning (I/O against output)
testpoint for test purposes to force a collective fault error with an external 3.3V probe

Title: Collective_FAULT_logic.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Fürther Straße 250 90429 Nürnberg GERMANY	
Size: A4	Revision: 3v00	
Date: 07.12.2020	Time: 13:49:51	Sheet of
Project: UltraZOHM_CarrierBoard.PnjPcb		Author: Andreas Geiger