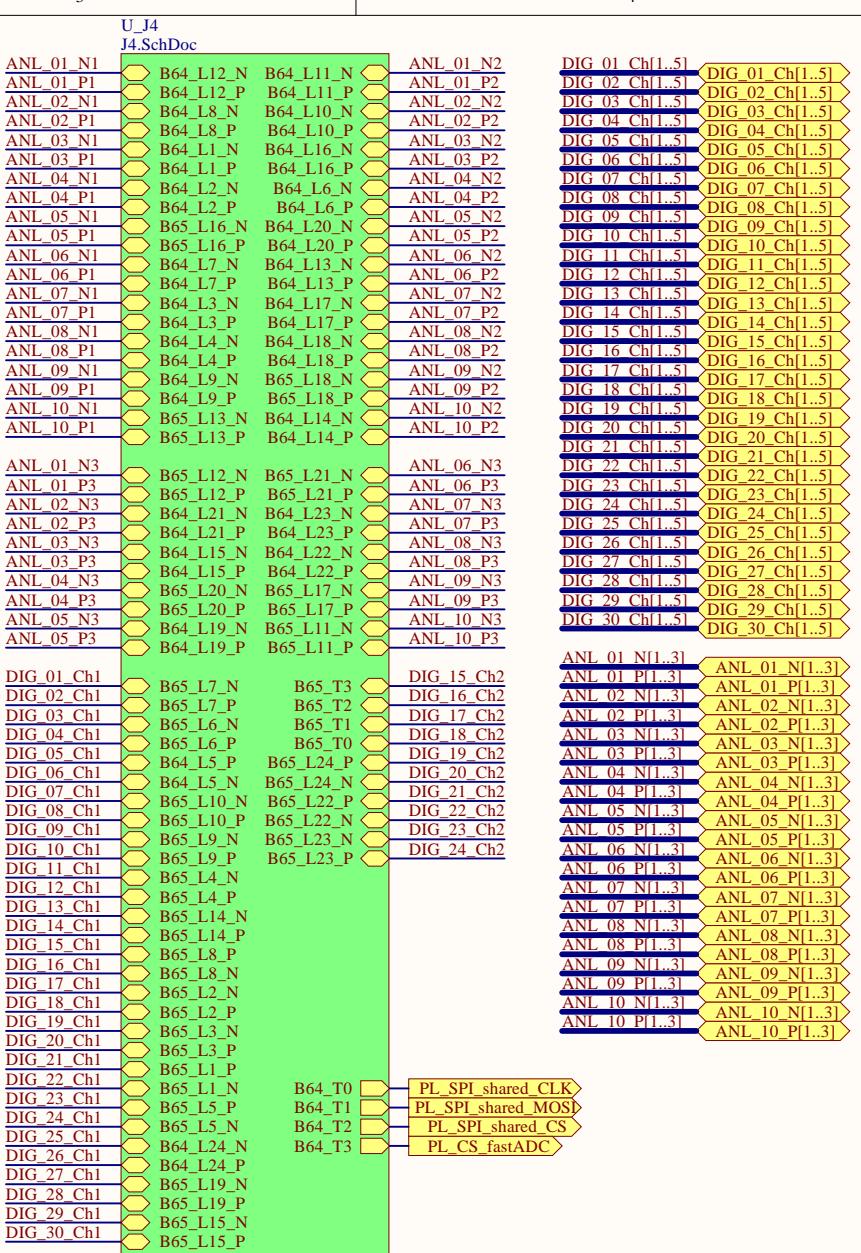
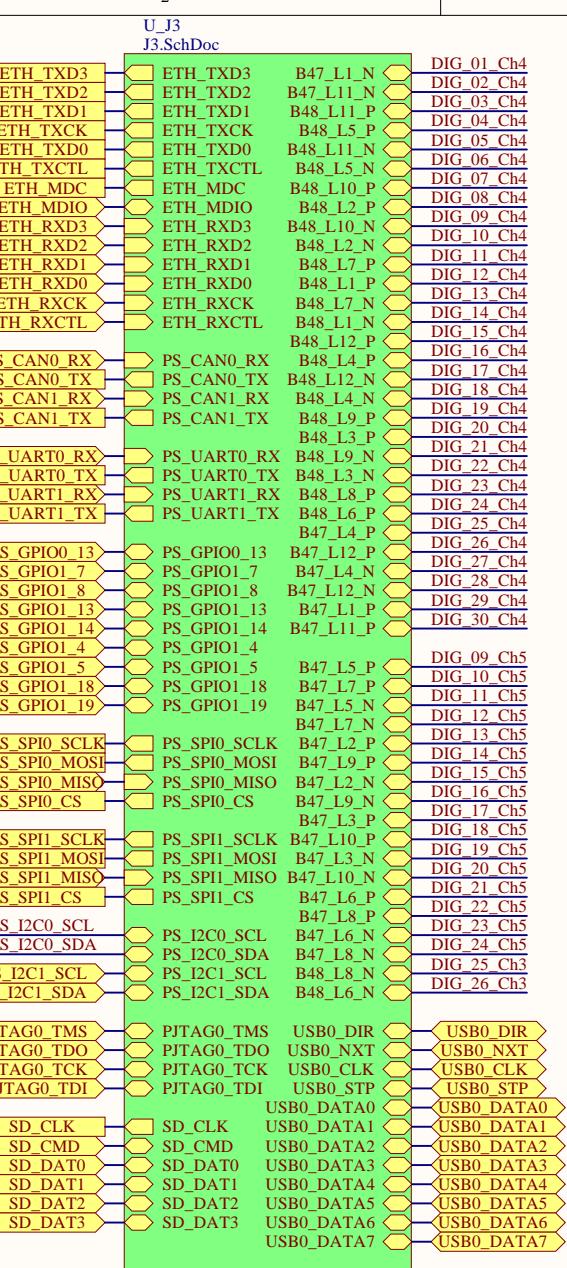
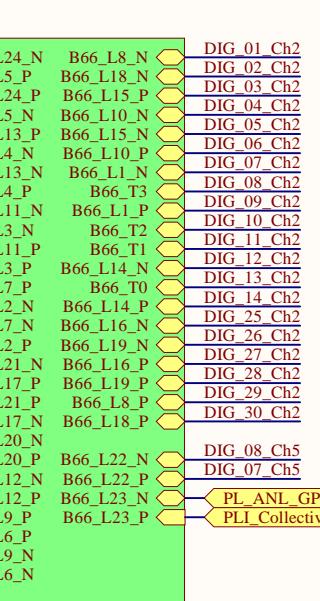
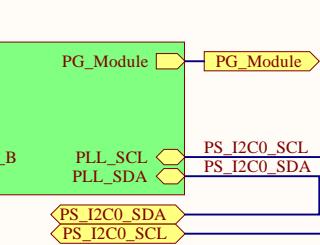
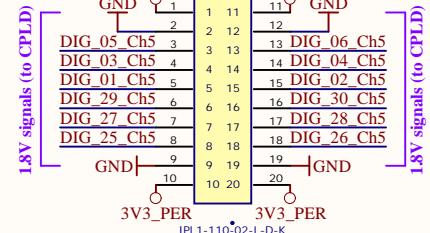


The 5th digital socket is not full connected with FPGA pins. DIG_01...DIG_06 and DIG_25...DIG_30 of this socket can be used externally via this connector.



Title Board2Board.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wasserstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:10	Sheet 2 of 23	Author: Andreas Geiger
Project: UltraZOHM_CarrierBoard.PriPcb			



A

B

C

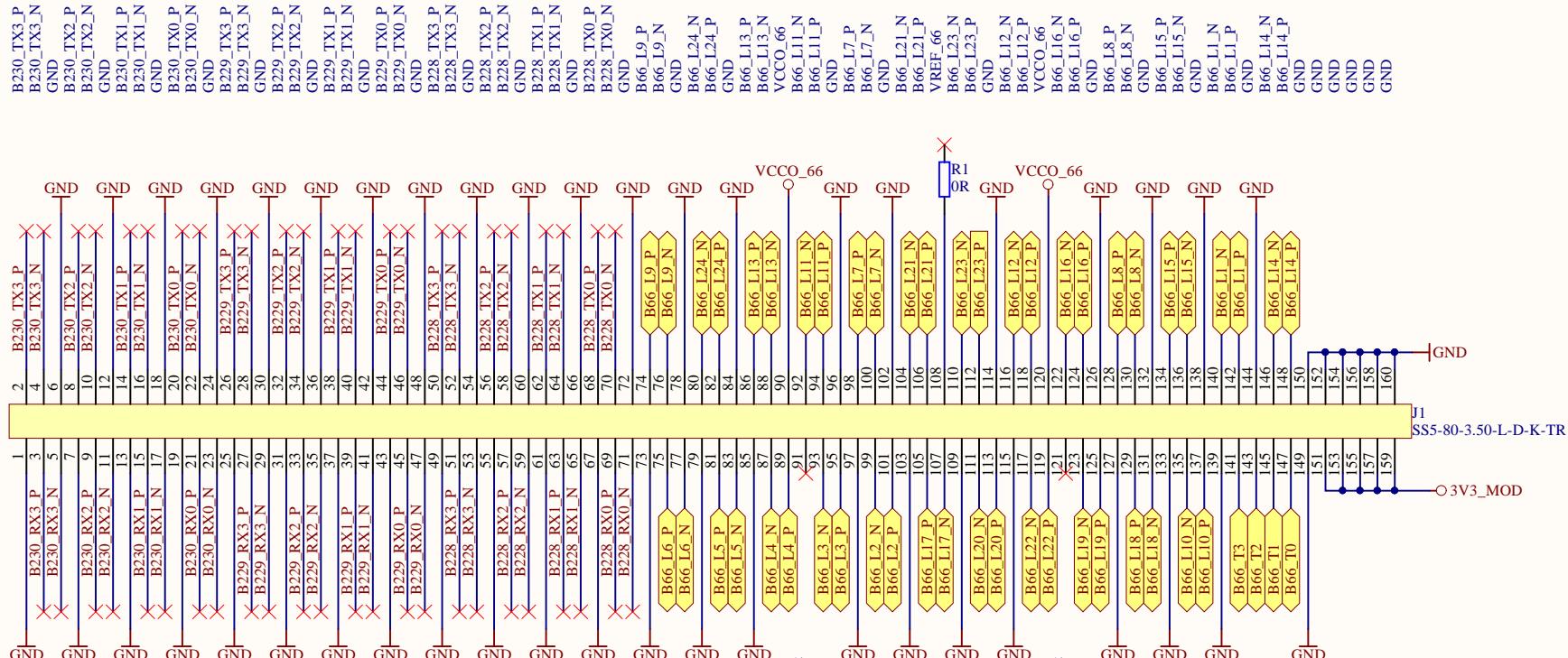
D

A

B

C

D

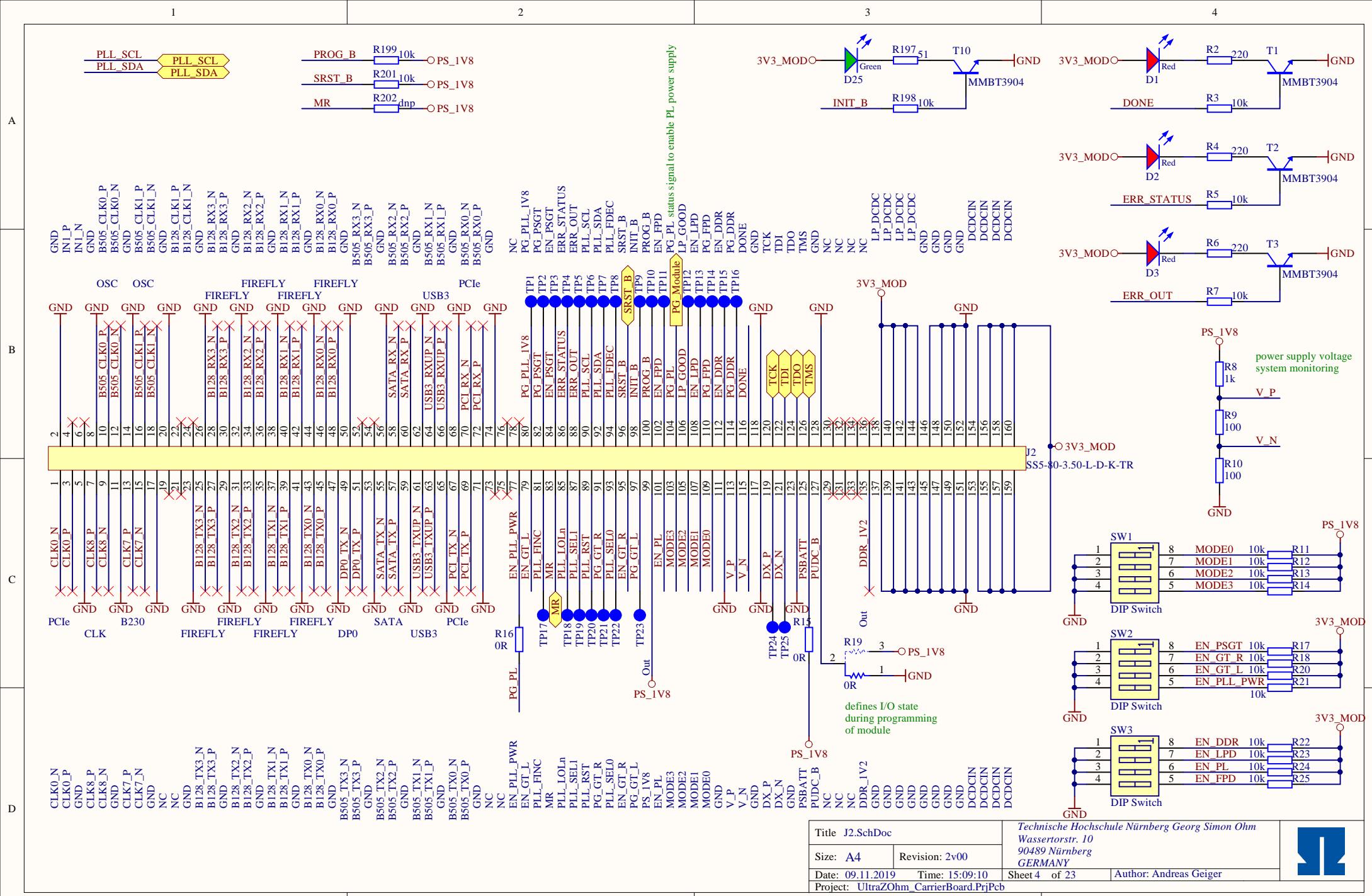


IV8 from Trenz U19 -> Not used

IV9 from Trenz U19 -> Not used

Title J1.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:10	Sheet 3 of 23	Author: Andreas Geiger
Project: UltraZOHM_CarrierBoard.PriPcb			





A

B

C

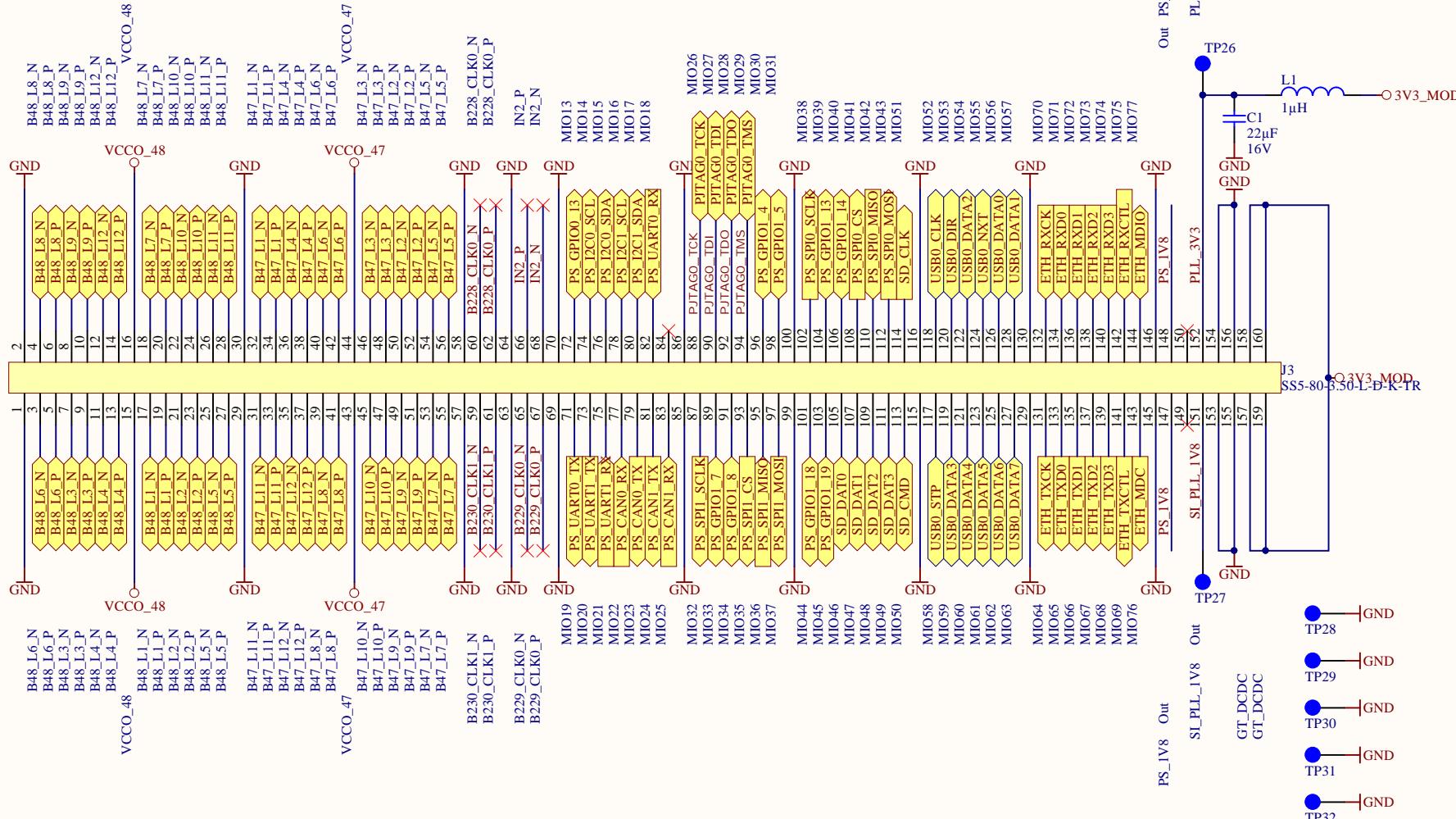
D

A

B

C

D



Title J3.SchDoc	
Size: A4	Revision: 2v00
Date: 09.11.2019	Time: 15:09:11
Project: UltraZOHM_CarrierBoard.PriPcb	Author: Andreas Geiger

Technische Hochschule Nürnberg Georg Simon Ohm
Wasserstr. 10
90489 Nürnberg
GERMANY



A

B

C

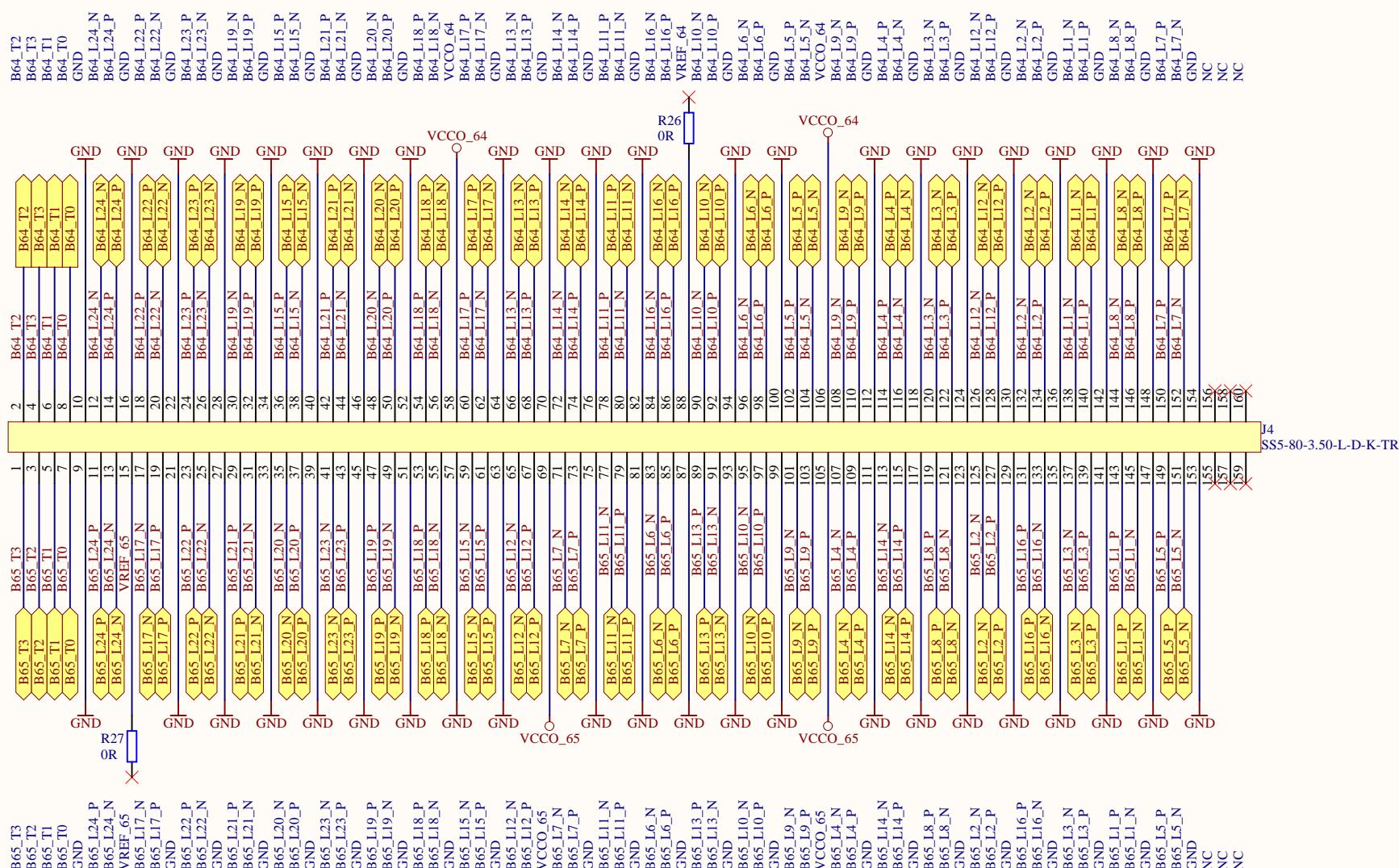
D

A

B

C

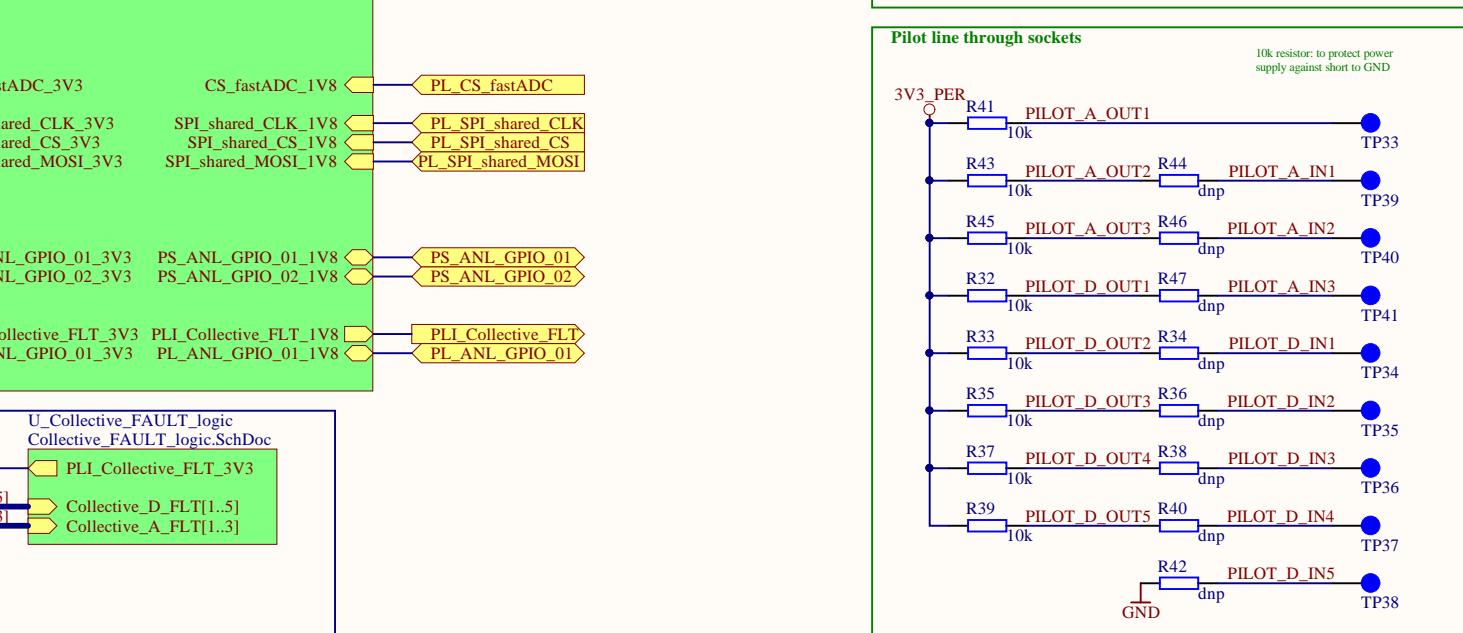
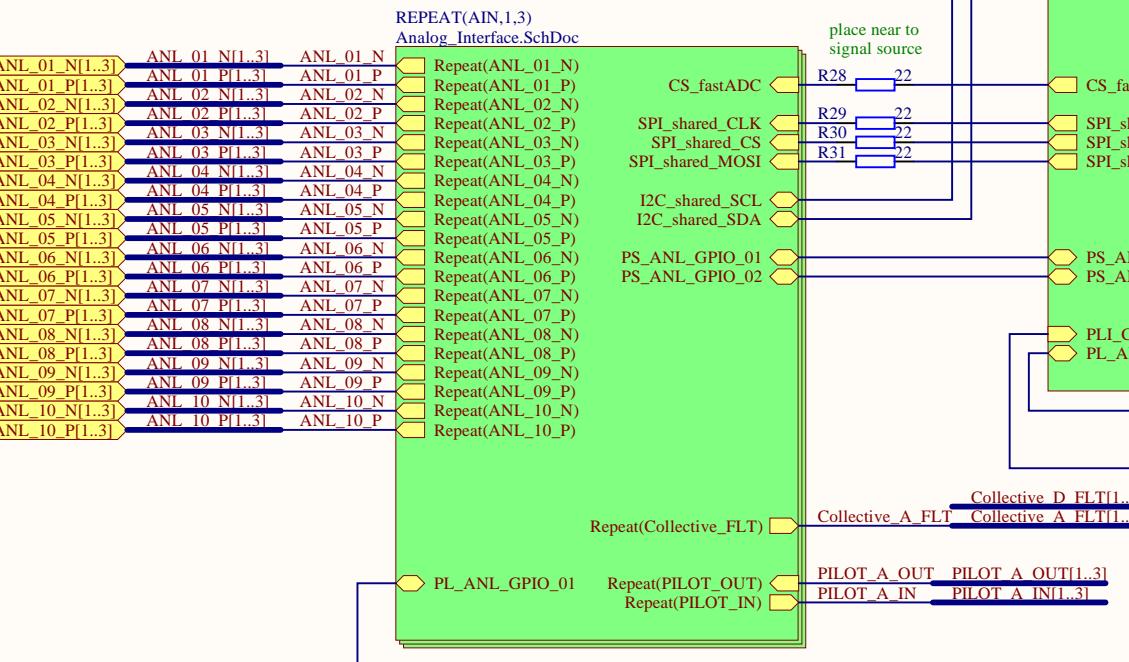
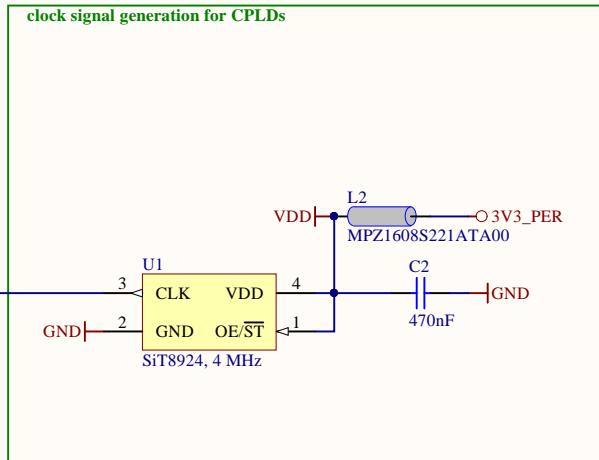
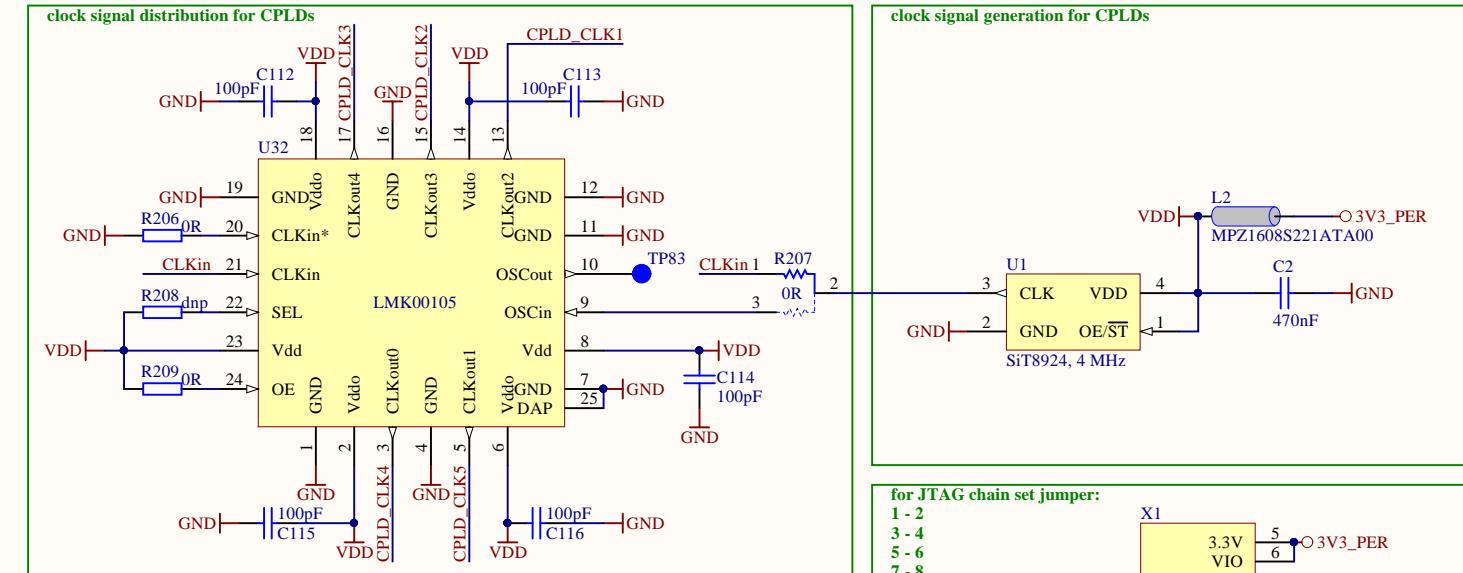
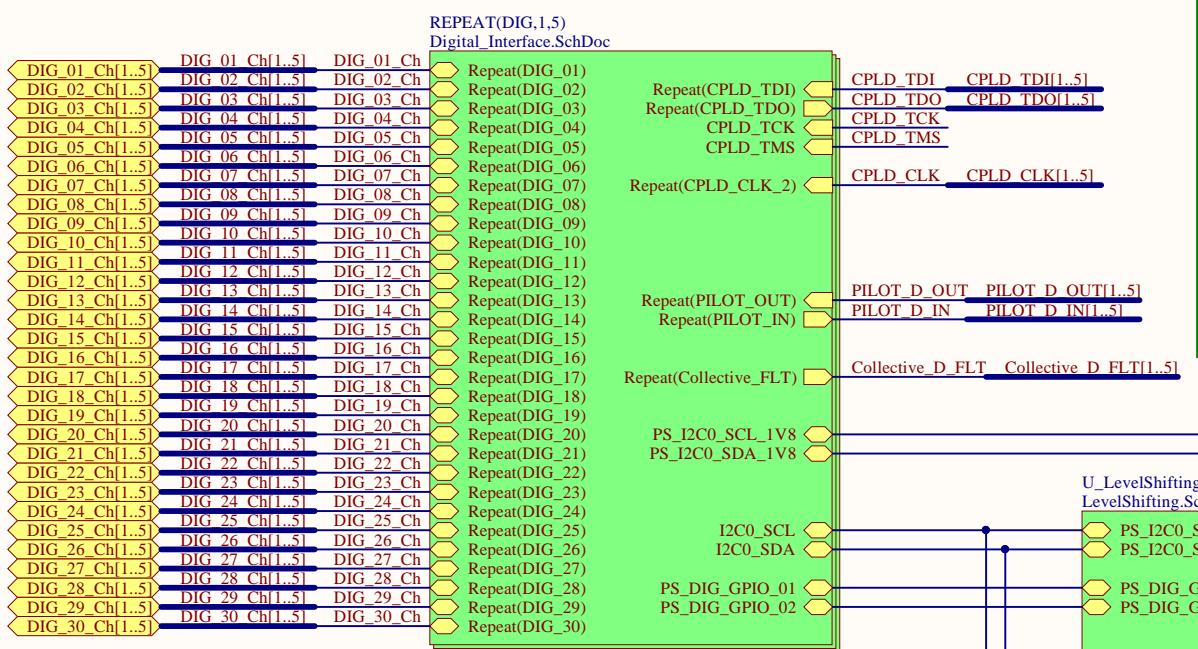
D



Title J4.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wasserstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00	Author: Andreas Geiger	
Date: 09.11.2019	Time: 15:09:11	Sheet 6 of 23	
Project: UltraZOHM_CarrierBoard.PriPcb			



A



Title: Signal_Distribution.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm	
Size: B	Revision: 2v00	Wassertorstr. 10	
		90489 Nürnberg	
		GERMANY	
Date: 09.11.2019	Time: 15:09:11	Sheet 7 of 23	Author: Andreas Geiger
Project: UltraZOHM_CarrierBoard.PriPcb			



BANK 0 @ 1.8V

U4A
 DIG_01 A8, A^8
 DIG_02 A9, A^9
 DIG_03 A10, A^10
 DIG_04 A11, A^11
 DIG_05 A12, A^12
 DIG_06 A13, A^13
 DIG_07 A14, A^14
 DIG_08 A15, A^15
 DIG_09 B15, B^15
 DIG_10 B14, B^14
 DIG_11 B13, B^13
 DIG_12 B12, B^12
 DIG_13 B11, B^11
 DIG_14 B10, B^10
 DIG_15 B9, B^9
 DIG_16 B8, B^8
 DIG_17 B7, B^7
 DIG_18 B6, B^6
 DIG_19 B5, B^5
 DIG_20 B4, B^4
 DIG_21 B3, B^3
 DIG_22 B2, B^2
 DIG_23 B1, B^1
 DIG_24 B0, B^0
 DIG_25 A0/GOE0, A^0
 DIG_26 A1, A^1
 DIG_27 A2, A^2
 DIG_28 A3, A^3
 DIG_29 A4, A^4
 DIG_30 A5, A^5
 A6, A^6
 A7, A^7

LA4128V-75TN100E
 R65 OR
 PS_I2C0_SDA_1V8
 PS_I2C0_SCL_1V8
 R66

BANK 1 @ 3.3V**BANK 1**

U4B
 C0, C^A0 R61 51 1 8 DIG_IO_09
 C1, C^A1 2 7 DIG_IO_11
 C2, C^A2 3 6 DIG_IO_13
 C3, C^A3 4 5 R62 51 5 DIG_IO_07
 C4, C^A4 17 4 3 6 DIG_IO_05
 C5, C^A5 49 2 7 DIG_IO_03
 C6, C^A6 50 8 R64 51 1 8 DIG_IO_01
 C7, C^A7 53 4 5 DIG_IO_02
 C8, C^A8 54 3 6 DIG_IO_04
 C9, C^A9 55 2 7 DIG_IO_06
 C10, C^A10 56 1 8 R63 51 5 DIG_IO_08
 C11, C^A11 58 4 3 6 DIG_IO_10
 C12, C^A12 59 2 7 DIG_IO_12
 C13, C^A13 60 1 8 R58 51 1 8 DIG_IO_16
 C14, C^A14 61 2 7 DIG_IO_14
 C15, C^A15 64 4 5 DIG_IO_18
 D15, D^A15 65 3 6 DIG_IO_20
 D14, D^A14 66 2 7 DIG_IO_22
 D13, D^A13 67 1 8 R57 51 5 DIG_IO_24
 D12, D^A12 69 2 7 DIG_IO_01
 D11, D^A11 70 1 8 R60 51 7 DIG_IO_30
 D10, D^A10 71 3 6 DIG_IO_28
 D9, D^A9 72 2 7 DIG_IO_26
 D8, D^A8 73 1 8 R59 51 4 5 DIG_IO_29
 D7, D^A7 74 3 6 DIG_IO_27
 D6, D^A6 75 2 7 DIG_IO_25
 D5, D^A5 76 1 8 R61 51 8 DIG_IO_17
 D4, D^A4 77 2 7 DIG_IO_19
 D3, D^A3 78 1 8 R62 51 6 DIG_IO_21
 D2, D^A2 79 2 7 DIG_IO_23
 D1, D^A1 80 3 6 DIG_IO_19
 D0/GOE1, D^A0 81 4 5 DIG_IO_23

LA4128V-75TN100E

dedicated inputs of CPLD

TP59 R67 51 12 I U4G
 TP60 R68 51 23 I
 TP61 R69 51 27 I
 CPLD_DigIn_01 R70 51 62 I
 CPLD_DigIn_02 R72 51 73 I
 /PILOT_IN R73 51 77 I
 LA4128V-75TN100E

chained programming interface

U4D
 CPLD_TDI 2 TDI
 CPLD_TCK 24 TCK
 CPLD_TMS 52 TMS
 CPLD_TDO 74 TDO
 LA4128V-75TN100E

Clock only for internal timing purposes. The input to output propagation delay time is independent

U4C
 CPLD_CLK_2 38 CLK1/I
 TP62 R/I 33 39 CLK2/I
 TP63 88 CLK3/I
 TP66 89 CLK0/I
 LA4128V-75TN100E

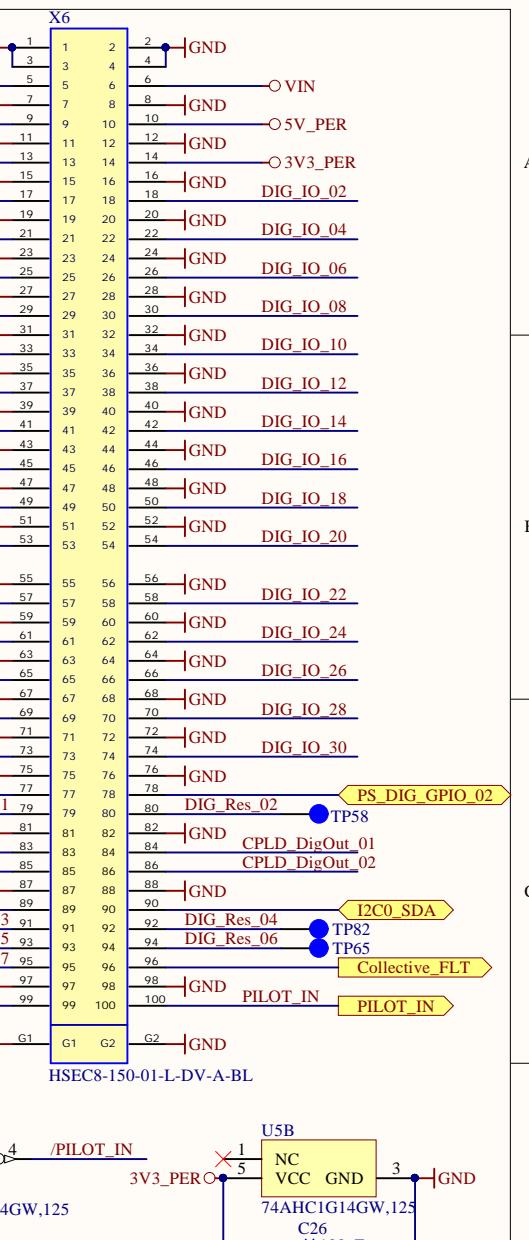
Power Supply of CPLD

1V8_PER
 3V3_PER
 GND
 VCCO (Bank0)
 VCC
 VCCO (Bank0)
 VCC
 VCCO (Bank1)
 VCCO (Bank1)
 VCC
 VCCO (Bank1)
 VCC
 VCCO (Bank0)

U4F
 1 GND
 7 GND (Bank0)
 18 GND (Bank0)
 26 GND
 33 GND (Bank0)
 40 GND (Bank0)
 45 GND (Bank1)
 51 GND (Bank1)
 57 GND (Bank1)
 68 GND (Bank1)
 75 GND (Bank1)
 83 GND (Bank1)
 90 GND (Bank1)
 95 GND (Bank0)

U4E
 13
 25
 33
 40
 45
 51
 57
 68
 75
 83
 90
 95

LA4128V-75TN100E



A

B

C

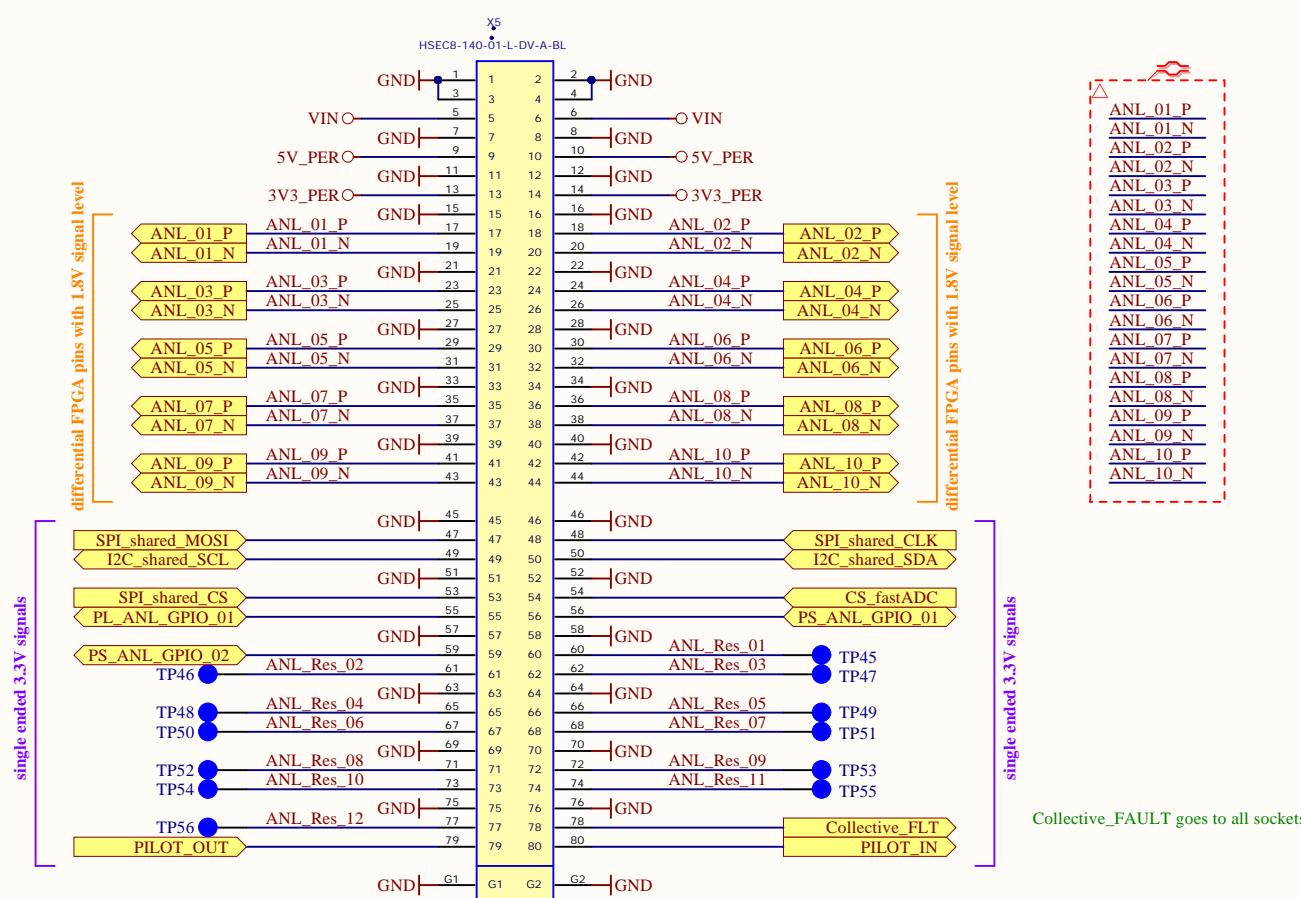
D

A

B

C

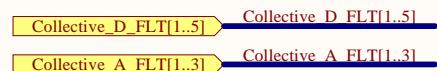
D



Title: Analog_Interface.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:11	Sheet 9 of 23	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PriPcb			

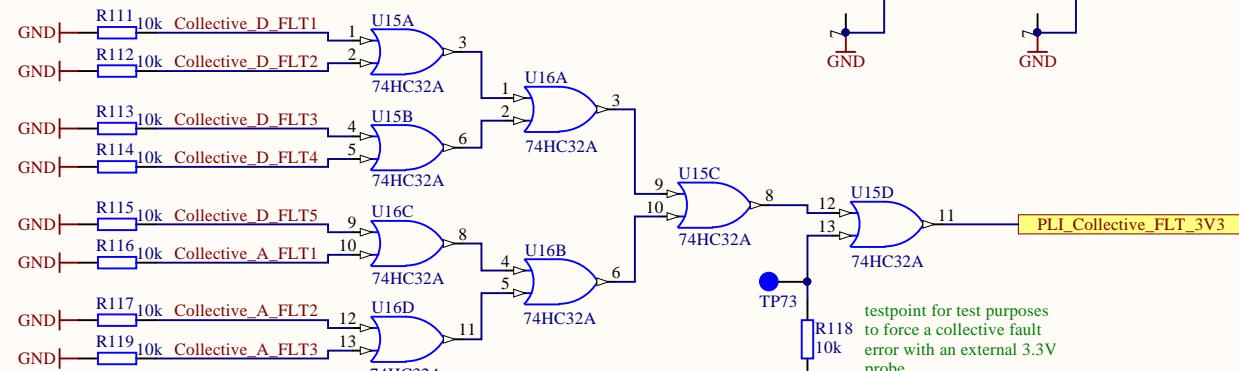
A

A



B

B



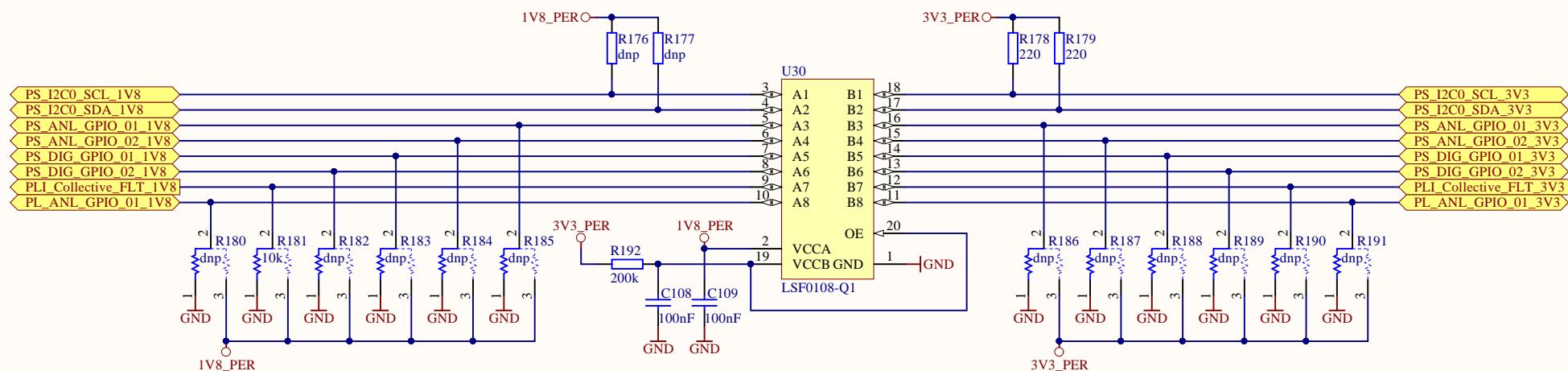
C

C

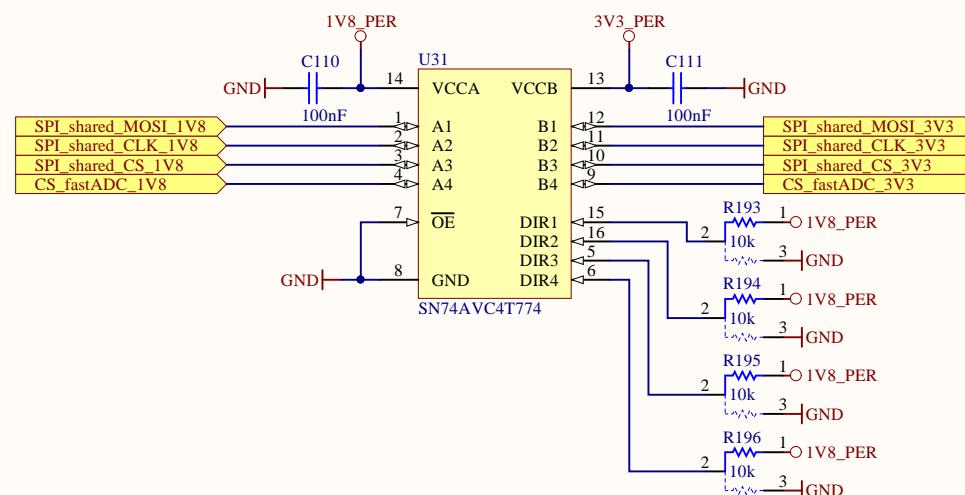
Title: Collective_FAULT_logic.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00	
Date: 09.11.2019	Time: 15:09:12	Sheet 10 of 23
Project: UltraZOhm_CarrierBoard.PriPcb	Author: Andreas Geiger	



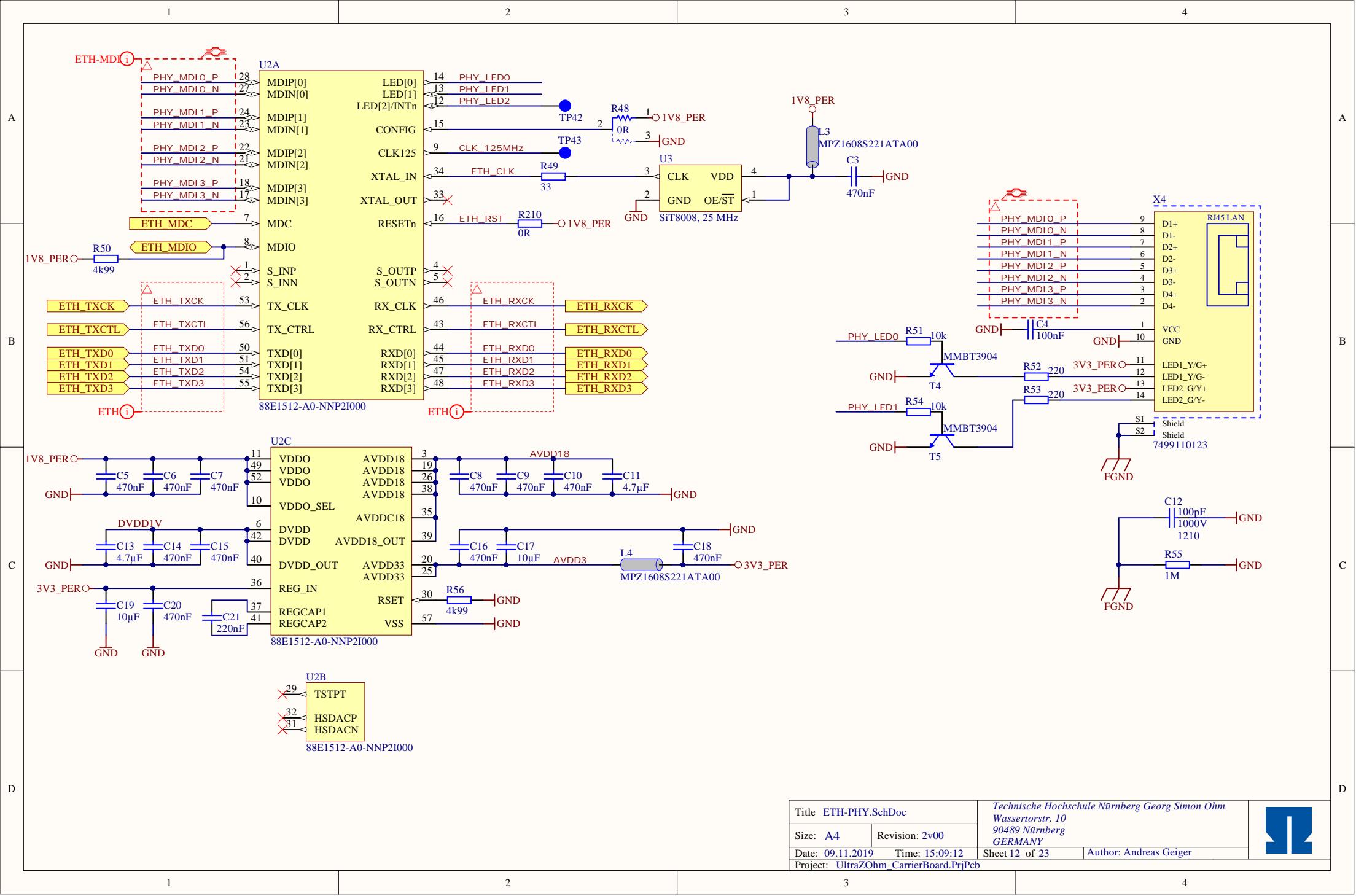
Bidirectional Level Shifting 1.8V to 3.3V



Level Shifting 1.8V to 3.3V



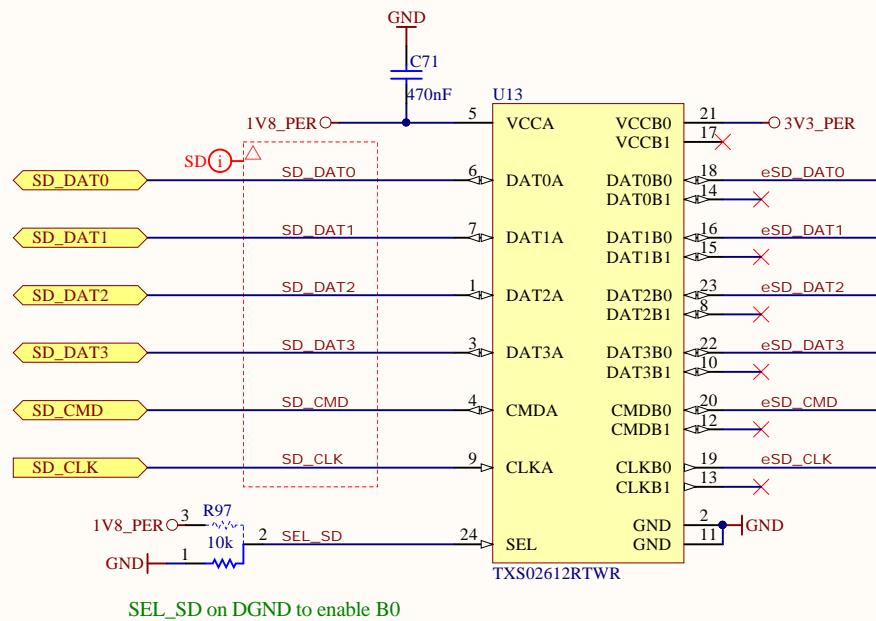
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Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:12	Sheet 11 of 23	Author: Andreas Geiger
Project: UltraZOHM_CarrierBoard.PriPcb			



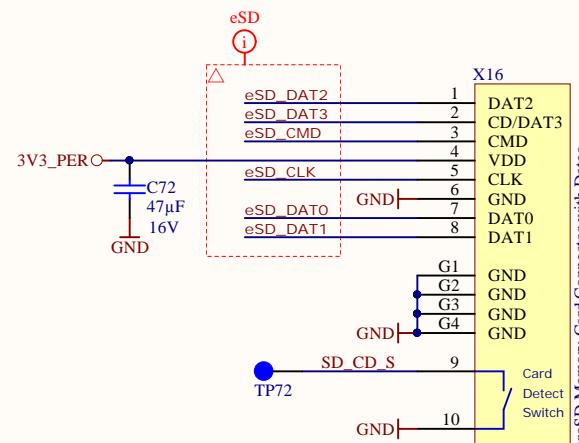
A

A

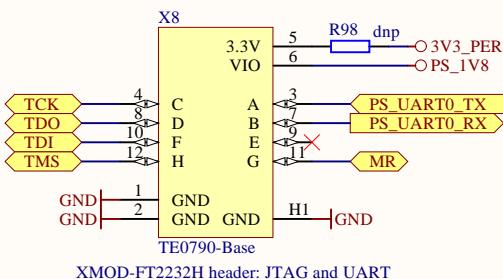
Bidirectional Level Shifting 1.8V to 3.3V



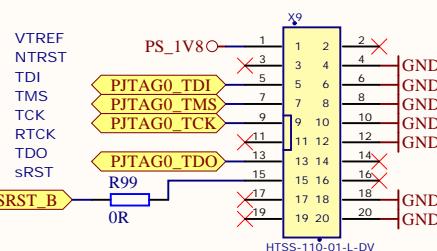
SD Card Connector



JTAG-Interface
JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for access to MPSoC module

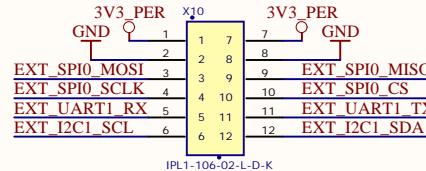


PJTAG-Interface (optional)
ARM JTAG

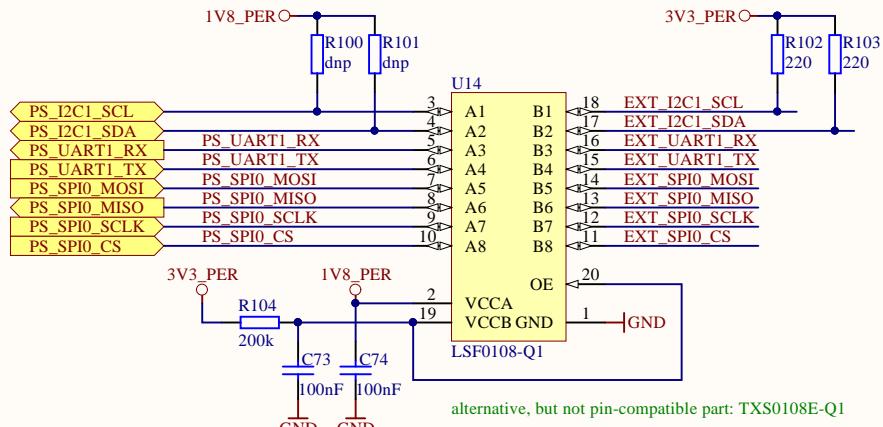


SPI, UART, I2C-Interface (from Processor System)

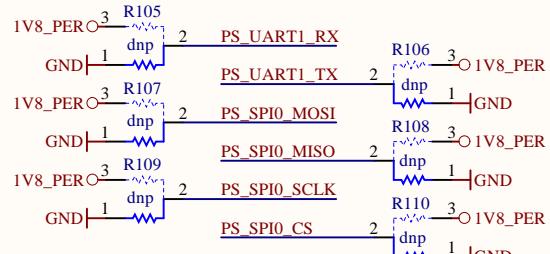
SPI, UART and I2C Connector @ 3.3V level



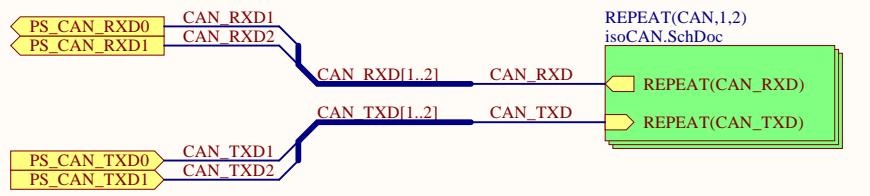
Bidirectional Level Shifting 1.8V to 3.3V



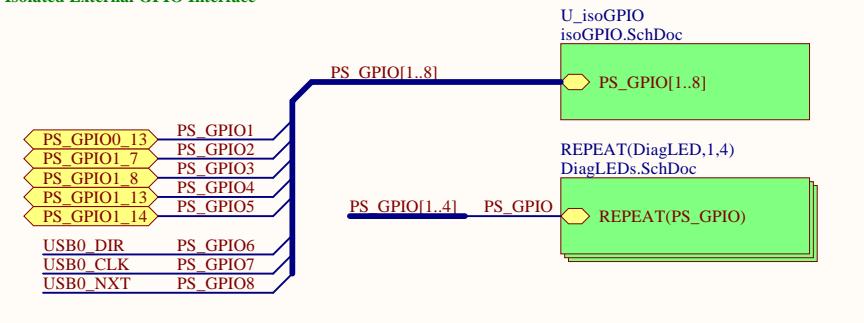
Pull-Up/Pull-Downs @ 1.8V stage



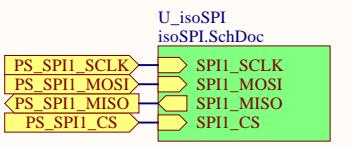
2x Isolated CAN-Interface
(renamed numbering, because multi channel design in Altium Designer starts with index 1 instead of 0)



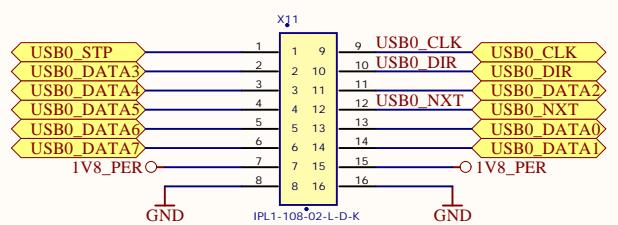
Isolated External GPIO Interface



Isolated SPI-Interface



USB Pins on Header
(for use as extension port or pin use as GPIO)



Title XMOD.SchDoc

Size: A4

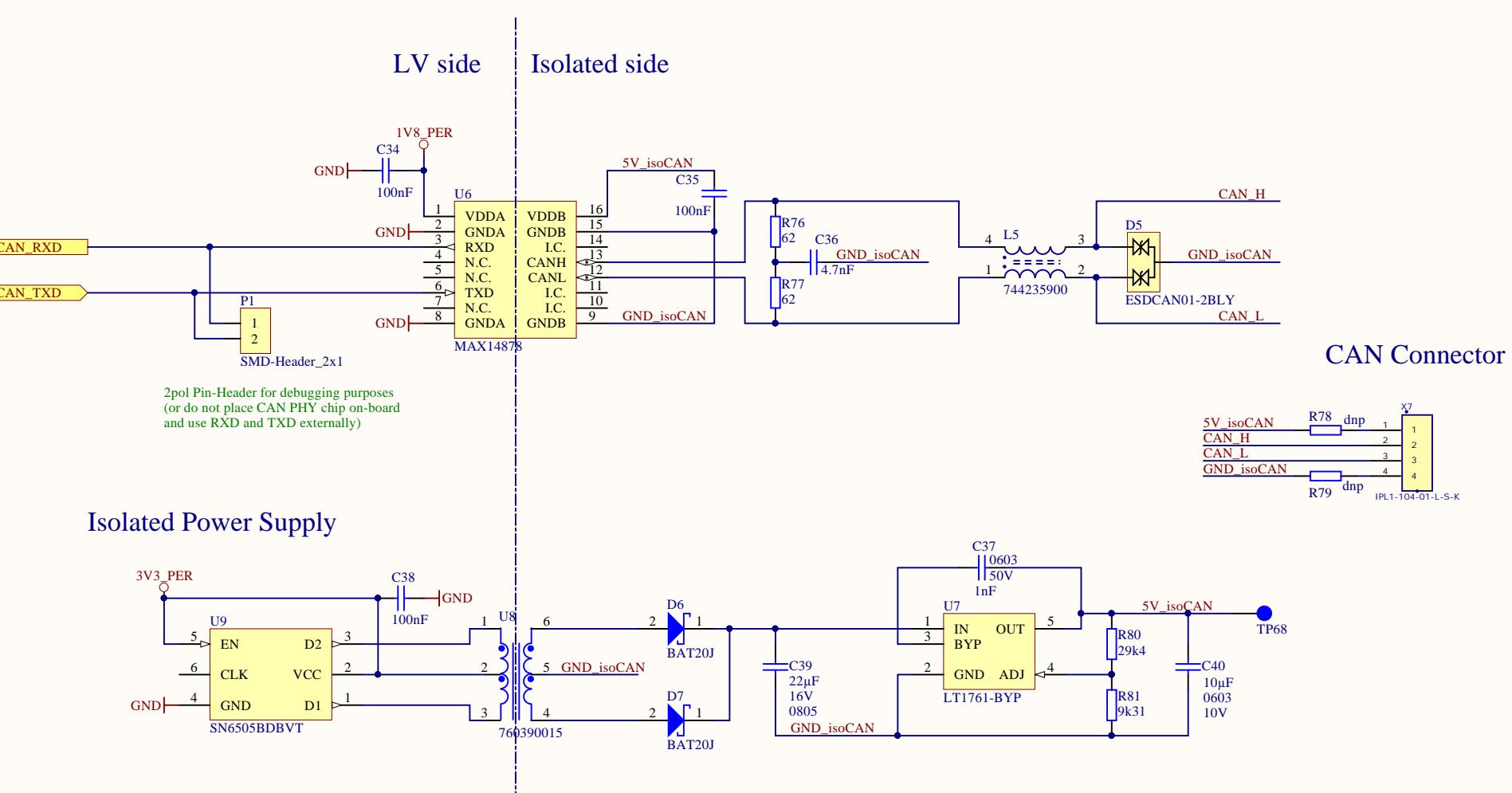
Revision: 2v00

Technische Hochschule Nürnberg Georg Simon Ohm
Wassertorstr. 10
90489 Nürnberg
GERMANY

Date: 09.11.2019 Time: 15:09:12 Sheet 14 of 23 Author: Andreas Geiger

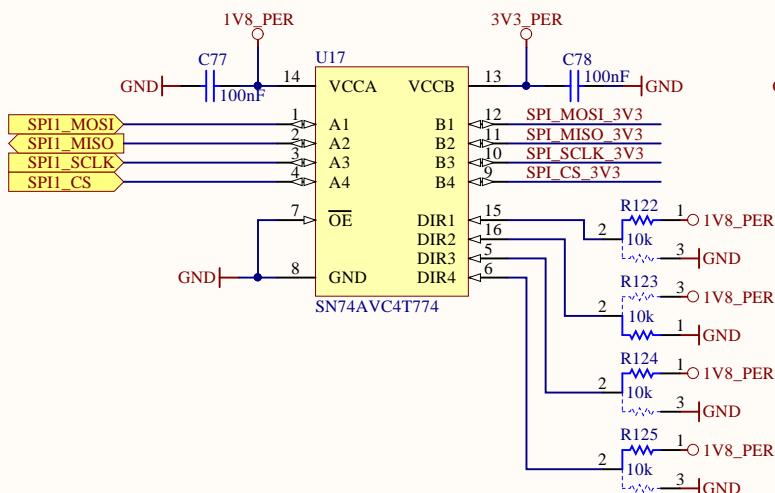
Project: UltraZOHM_CarrierBoard.PnjPcb





Title isoCAN.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:12	Sheet 15 of 23	Author: Andreas Geiger
Project: UltraZOHM_CarrierBoard.PriPcb			

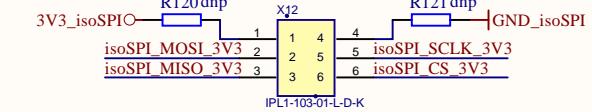
Level Shifting 1.8V to 3.3V



LV side

Isolated side

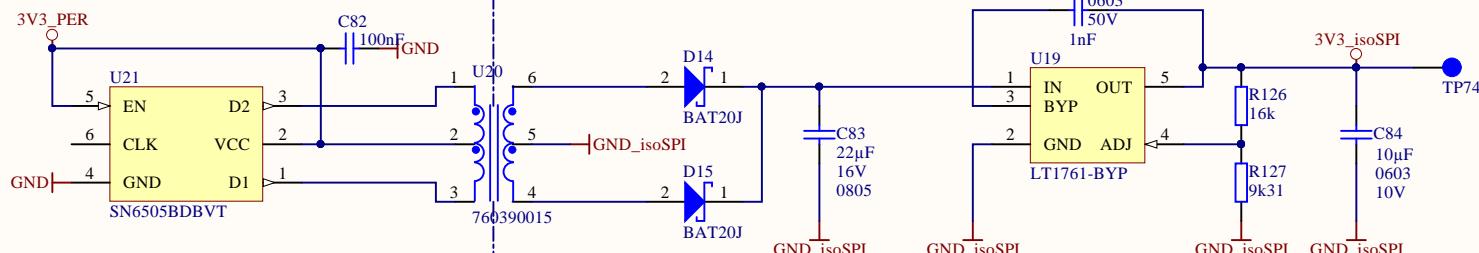
SPI Connector



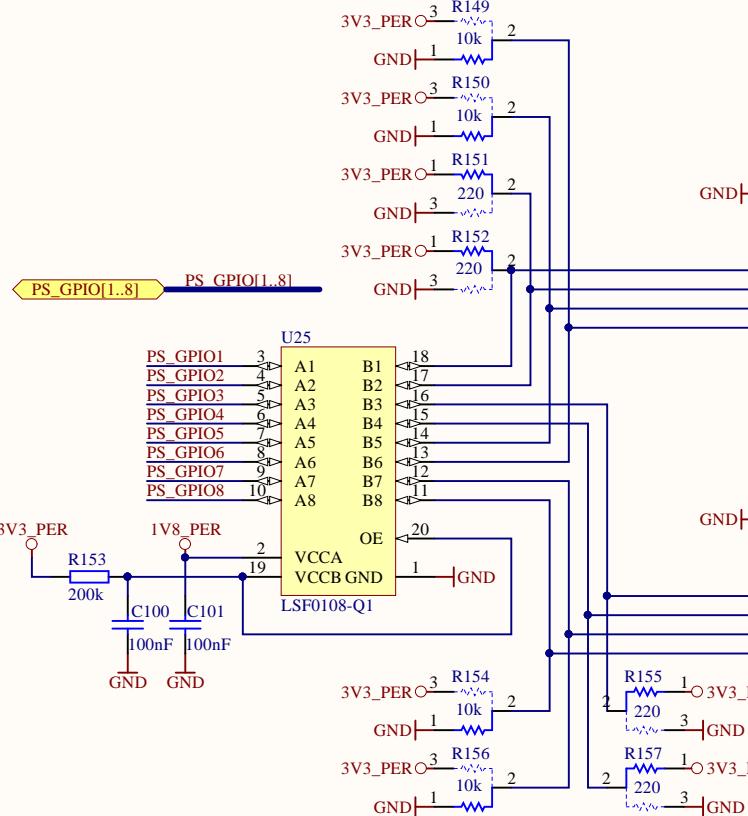
take ADUM4402 if SoC acts as SPI slave

alternative pin-compatible part: Texas Instruments ISO7741DW

Isolated Power Supply



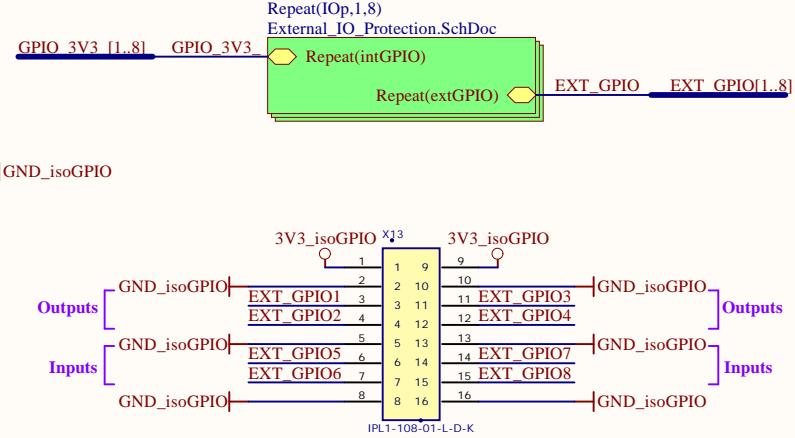
Bidirectional Level Shifting 1.8V to 3.3V



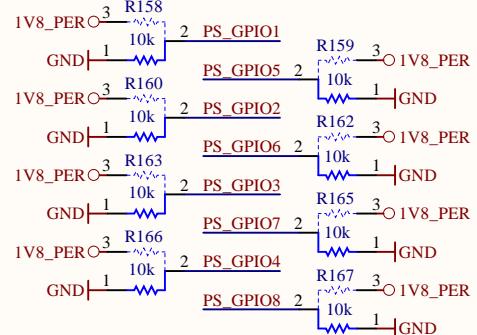
LV side

Isolated side

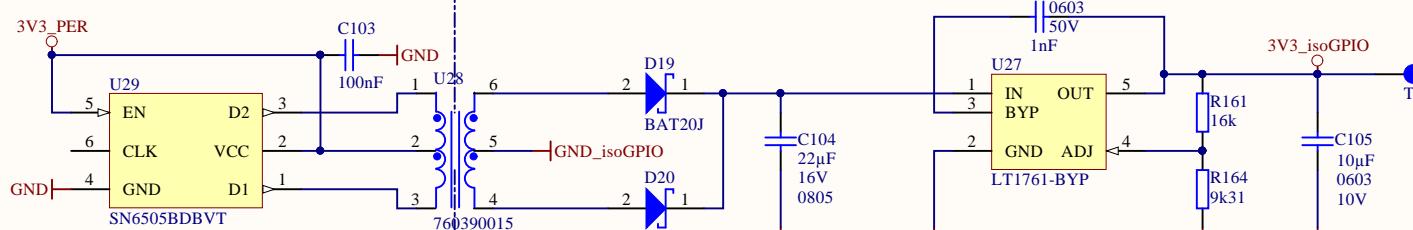
IO Protection with TVS-Diode and PTC-Resistor



Input/Output Pull-Up/Pull-Downs



Isolated Power Supply



Title: isoGPIO.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:12	Sheet 17 of 23	Author: Andreas Geiger
Project: UltraZOHM_CarrierBoard.PriPcb			

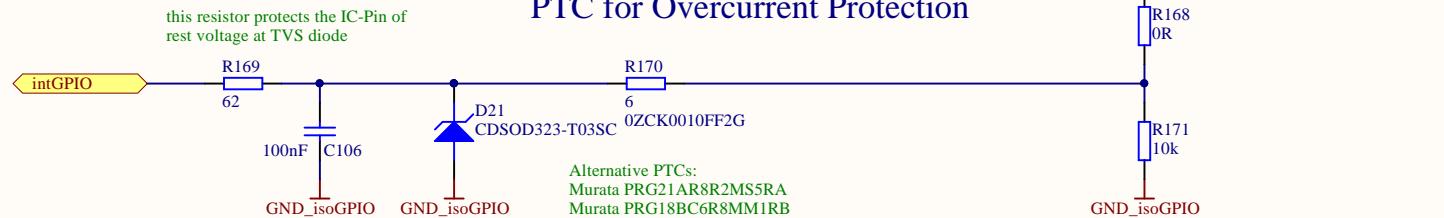


A

A

Voltage Divider

PTC for Overcurrent Protection



B

B

C

C

D

D

Title: External_IO_Protection.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:12	Sheet 18 of 23	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PriPcb			

A

A

B

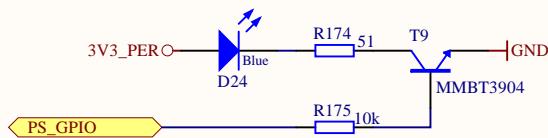
B

C

C

D

D

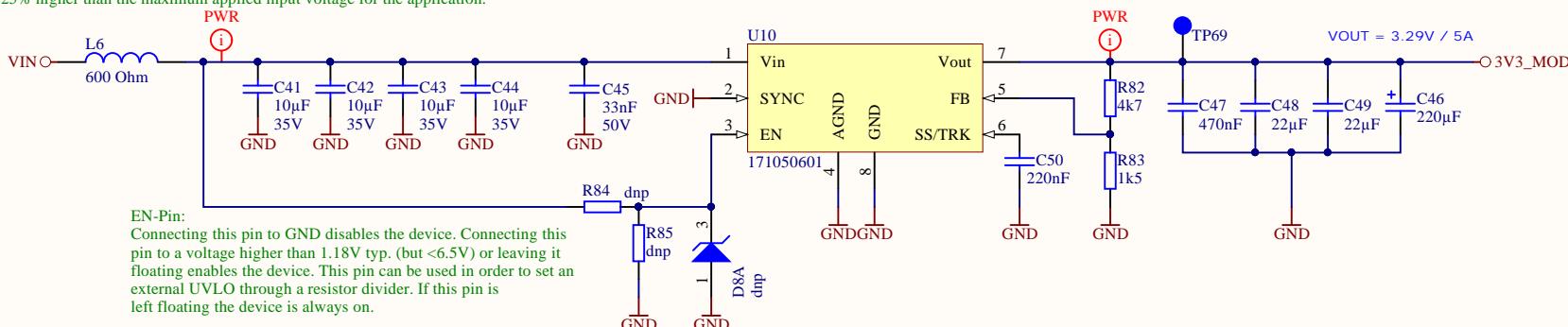


Title: DiagLEDs.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:12	Sheet 19 of 23	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PriPcb			

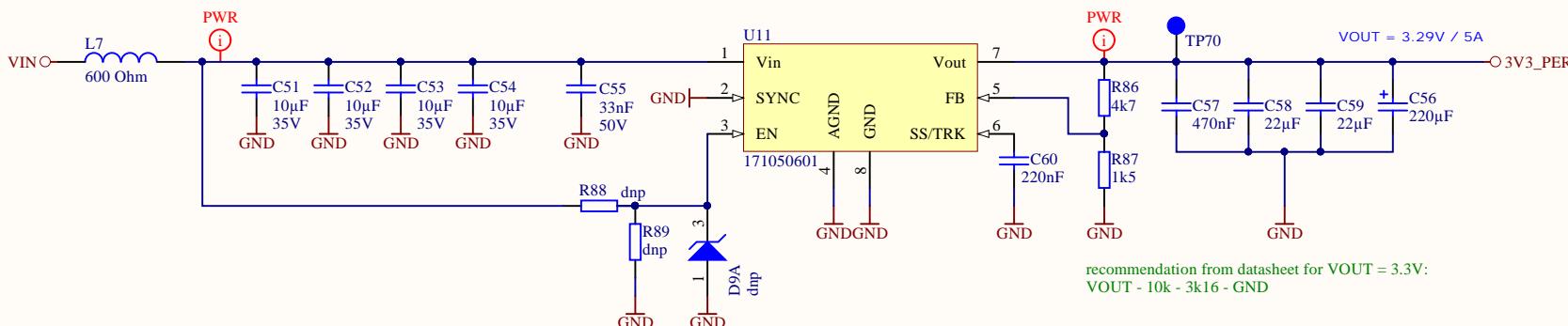
Notes: preferred to use 2x 22 μ F/50V capacitors at Vin, but this design uses 35V caps due to worse availability at distributors.

Datasheet: recommended minimum input capacitance is 22 μ F (including derating) ceramic with voltage rating

at least 25% higher than the maximum applied input voltage for the application.

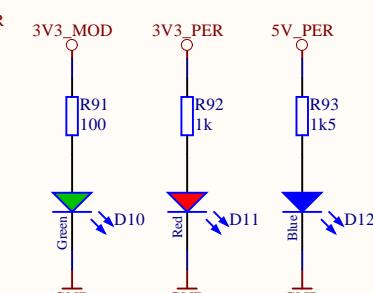
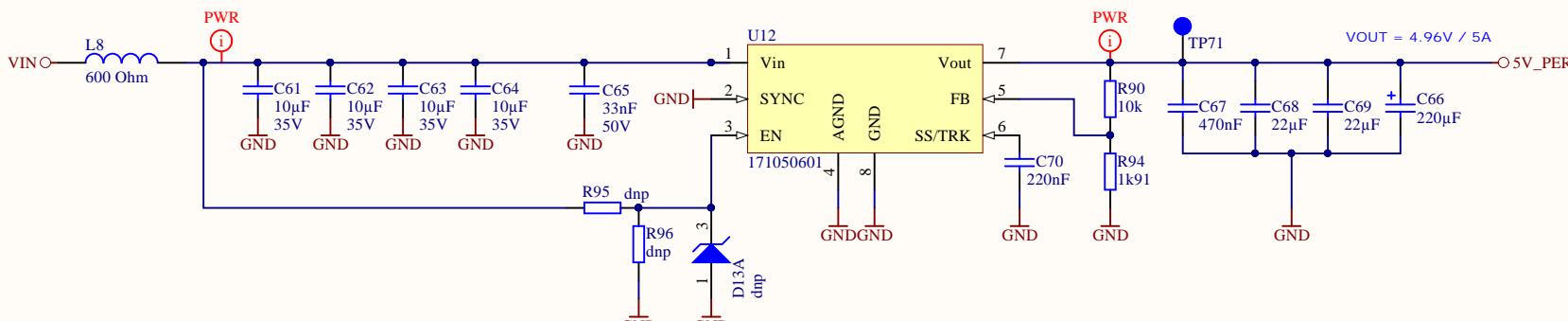


power supply for:
 - Trenz module (PL_1V8, PS_1V8, ...)



power supply for:
 - digital and analog sockets
 - SD-Card
 - Ethernet
 - CAN

power supply for:
 - digital and analog sockets



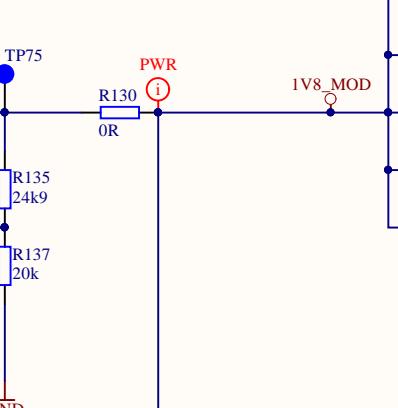
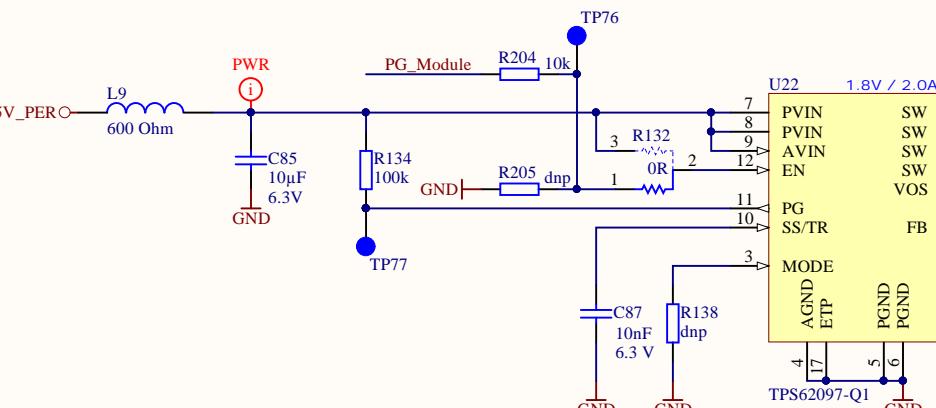
Title: Power_Supply_1.SchDoc	Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00	
Date: 09.11.2019	Time: 15:09:12	Sheet 20 of 23
Project: UltraZOHM_CarrierBoard.PriPcb	Author: Andreas Geiger	



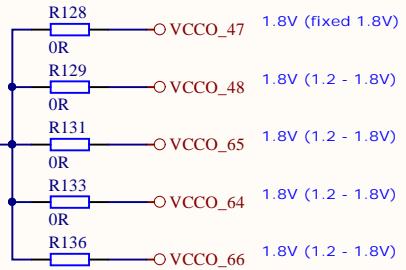
A

PG_Module

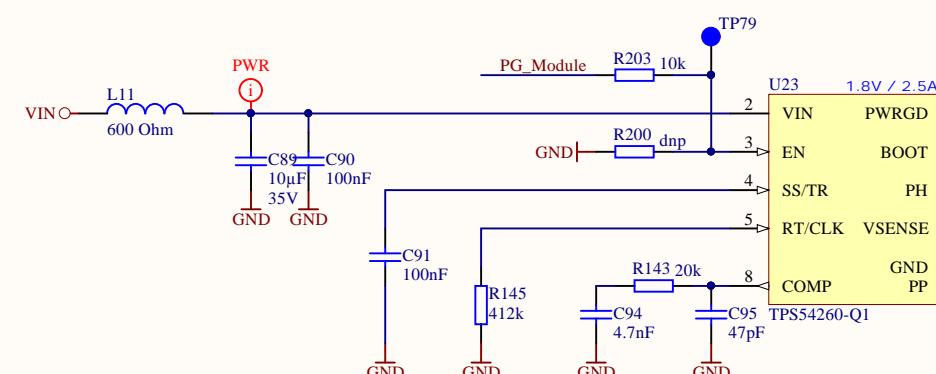
power good signal from Trenz module
to enable banks and peripherals after
module is supplied sufficiently



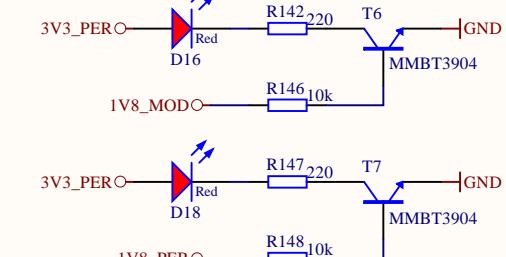
bank power supply with jumper selectable
(place near to Trenz module!)



B



power supply for:
 - CPLD Banks
 - I2C Level Shifter
 - Ethernet
 - SD-Card Level Shifter
 - JTAG Programmer
 - CAN Transceiver
 - SPI, UART, I2C-Interface Level Shifter
 - Isolated SPI Level Shifter
 - Isolated GPIO Level Shifter



Reference Design: TE0728

Reference Design: TPS82085SIL (TE0808/POWER.SchDoc) not in stock at distributors...

Title Power_Supply_2.SchDoc

Size: A4 Revision: 2v00

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90489 Nürnberg
GERMANY

Date: 09.11.2019 Time: 15:09:13

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Author: Andreas Geiger

Project: UltraZOhm_CarrierBoard.PriPcb



A

A

B

B

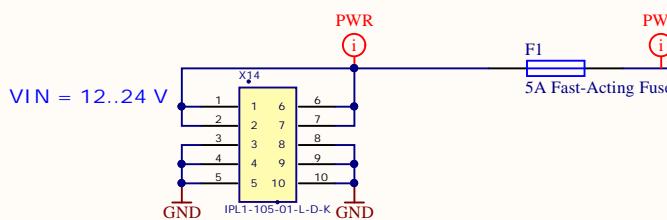
C

C

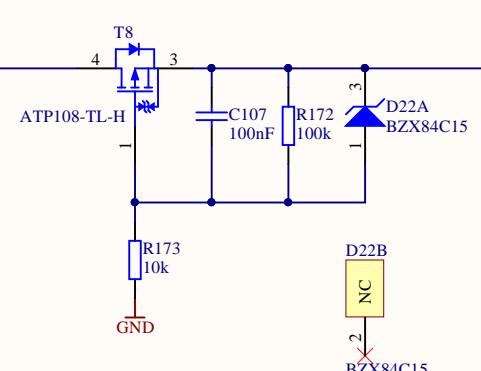
D

D

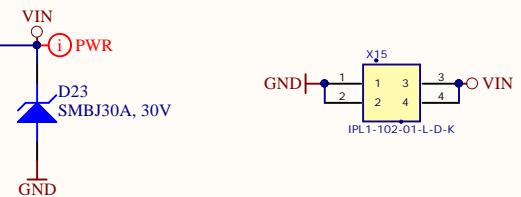
Short Circuit Protection



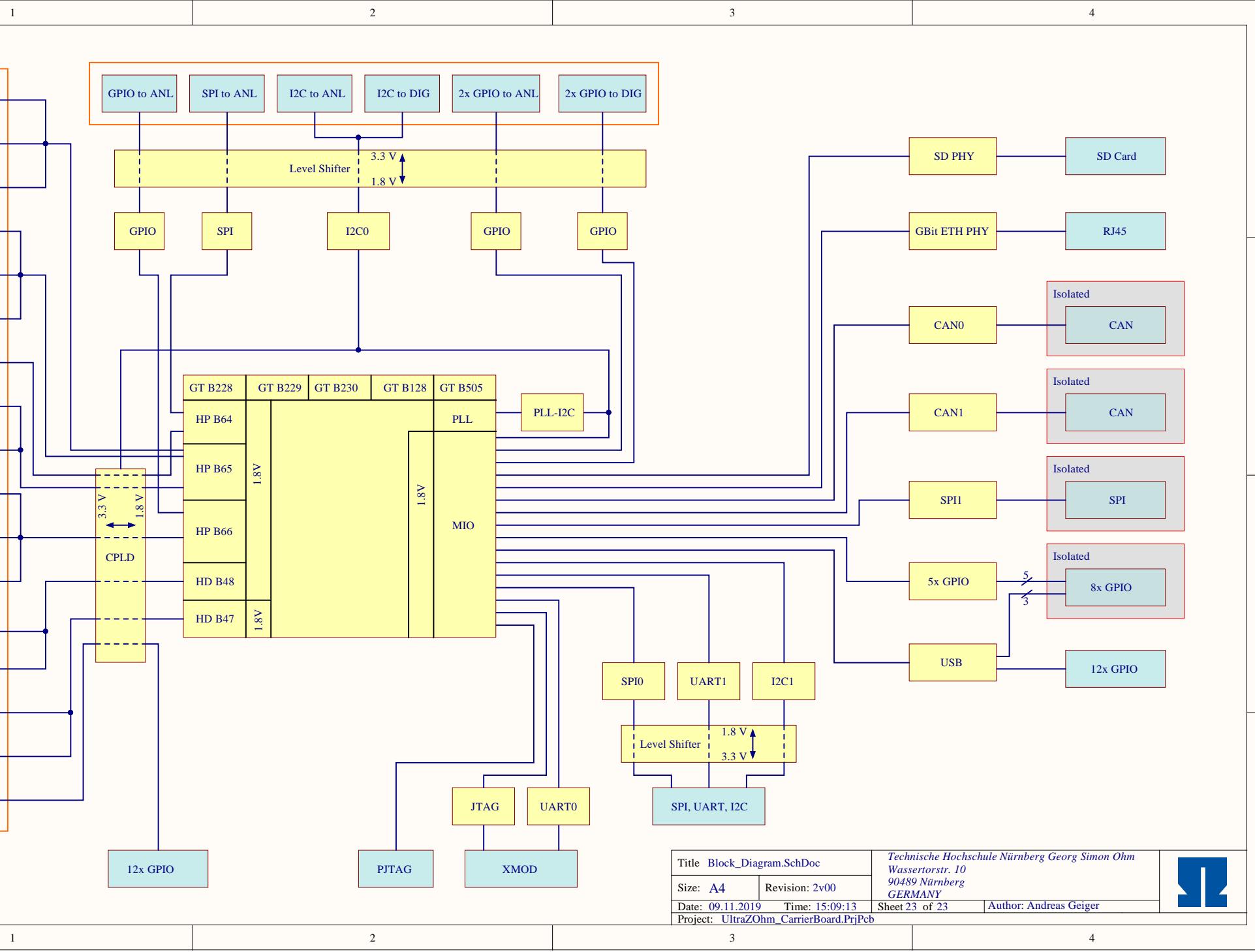
Reverse Polarity Protection



Overvoltage Protection



Title Power_Supply_Input.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:13	Sheet 22 of 23	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PriPcb			



Title: Block_Diagram.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:13	Sheet 23 of 23	Author: Andreas Geiger
Project: UltraZOHM_CarrierBoard.PriPcb			

