

1. What could not reduce miss rate?
 - a) Decreasing the number of cache levels
 - b) Increasing the associativity of cache
 - c) Increasing the number of cache levels
2. What could reduce miss rate?
 - a) Increasing the number of cache levels
 - b) Increasing the associativity of cache
 - c) Increasing the size of cache blocks
 - d) all of them
3. What could reduce miss rate?
 - a) Decreasing the number of cache levels
 - b) Small cache size
 - c) Giving priority to reads before writes
4. What could reduce miss rate?
 - a) Increasing the number of cache levels
 - b) Increasing the total size of cache.
 - c) Increasing the size of cache blocks
 - d) all of them
5. Choose the right word to the place of three dots (...):
A valid bit shows that ...:
 - a) A block consists data
 - b) A block is going to be written
 - c) A block is not going to be written
6. Choose the right word to the place of three dots (...):
A dirty bit shows that ...:
 - a) A block consists data
 - b) A block doesn't consist data
 - c) A block is going to be written
7. Choose the right word to the place of three dots (...):
...shows how often the instruction is executed:
 - a) stall

- b) throughput
 - c) time per instruction
8. Choose the right word to the place of three dots (...):
Inter core i7 L1 cache has ...
- a) one cache for both data and instruction
 - b) one cache for data and one cache for instruction
 - c) two caches for both data and instruction
9. Average Memory Access Time (AMAT) is equal :
- a) $hit\ rate + miss\ rate * miss\ penalty$
 - b) $hit\ rate * miss\ rate + miss\ penalty$
 - c) $hit\ rate + miss\ rate$
10. Choose the right word to the place of three dots (...):
In Allocate writing (Write-Allocate) ...
- a) the data is read from RAM and loaded into the cache. Then, cache is updated with CPU instruction and dirty bit is set to 1. Finally, the evicted block is written to RAM.
 - b) the data is written on through to memory, not being load into cache.
 - c) the data is written directly to cache and memory immediately.

Answers:

- 1) a
- 2) d
- 3) c
- 4) d
- 5) a
- 6) c
- 7) b
- 8) b
- 9) a
- 10) a