40G UDP Parser

Problem:

To parse UDP packet and perform sum/min/max for integers in the payload at 40Gbits/sec and return the result

Design Constraints:

- Design operates at 160Mhz
- Input and Output bus-width is 256 bits (32 Bytes) following AXI4-Streaming
- Each packet including header(Ethernet/IP/UDP) is 2000 Bytes
- First two bytes of data indicate what operation to perform on rest of 32-bit (4 byte) integers (0-sum, 1-max, 2-min)
- There should be a valid output for end of each packet

Packet Header Fields

Ethernet header

```
uint48_t dstAddr;
uint48_t srcAddr;
uint8_t l3Type;
uint8_t length;
```

IPv4 Header

```
uint4_t version;
uint4_t hLength;
uint8_t tos;
uint16_t length;
uint16_t identification;
uint16_t flagsOffset;
uint8_t ttl;
uint8_t protocol;
uint16_t chksum;
uint32_t srcAddr;
uint32_t dstAddr;
```

UDP Header

```
uint16_t sport;
uint16_t dport;
uint16_t len;
uint16_t chksum;
```

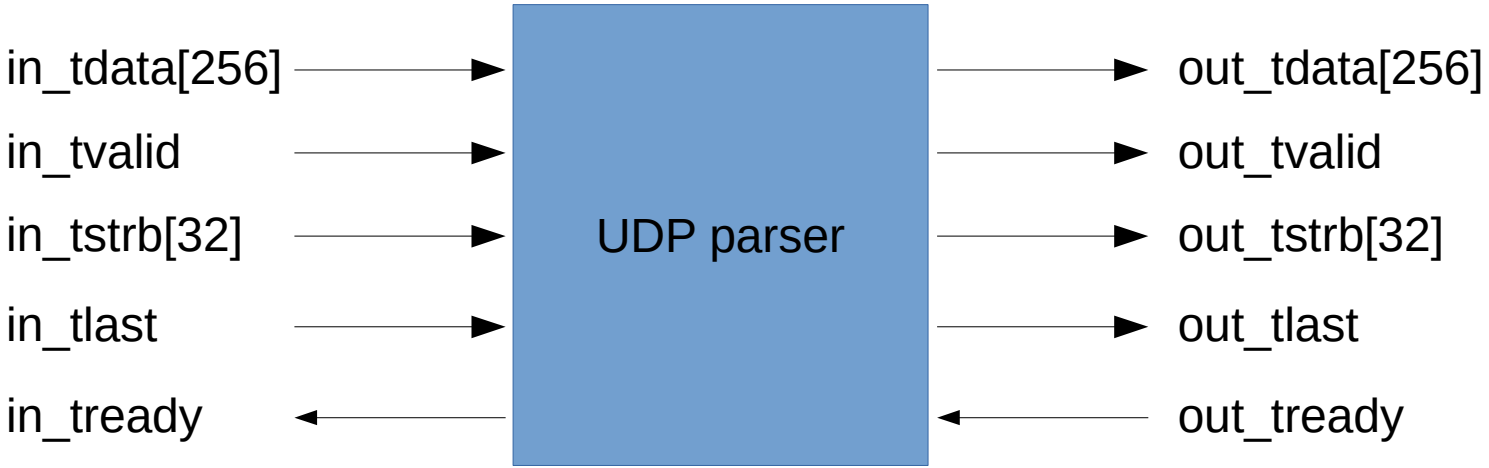
Data

```
uint16_t Operation;
uint32_t [488:0] Data;
```

Summary:

Packet Header : 42 Bytes
Op Command : 2 Bytes
Data : 1956 Bytes

Design block diagram with I/O signals



Packet header format

32 bytes

Ethernet Header (14)		IPv4 Header (18)	
IPv4 Header (2)	UDP Header (8)	Operation (2)	Data (20)
Data (32)			
Data (32)			
……..			
Data (16)			

Note : This packet is streamed from top row to bottom row and consider MSB is in left side. Last row will have only 16 bytes of data as total is 2000 bytes.

Deliverables

- State diagram for the whole design
- Verilog HDL code for whole design (use shift register method and high level codes as much as possible)
- Self checking test bench for simulation
- Test results
- Synthesized design