International Islamic University Islamabad

Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

Digital System Design

DESIGN OF BCD TO EXCESS 3 CODE

Open-Ended Lab Report

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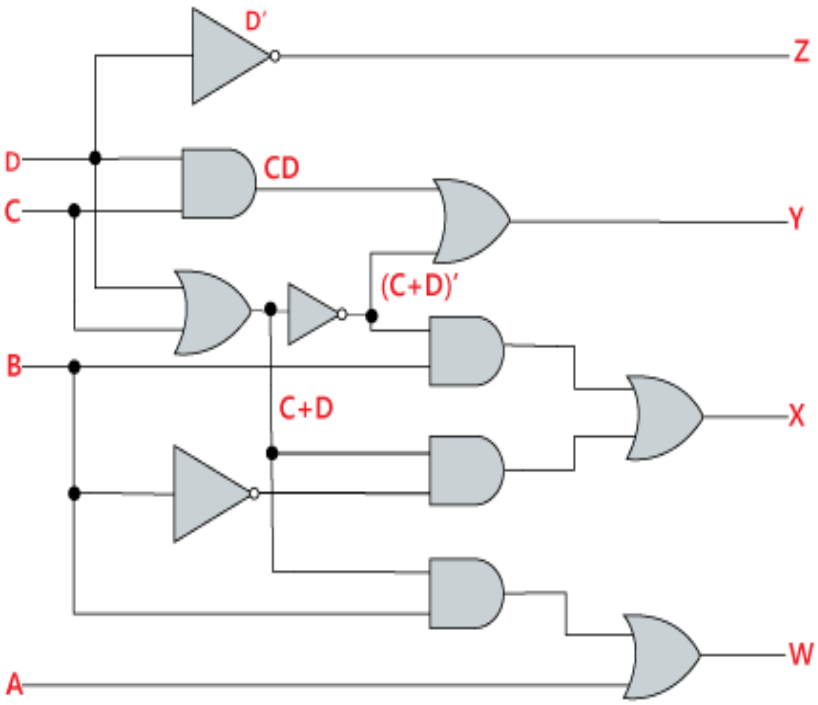
✓ INTRODUCTION:

The Excess-3 binary code is an example of a self-complementary BCD code. A self-complementary binary code is a code which is always complimented in itself. By replacing the bit 0 to 1 and 1 to 0 of a number, we find the 1's complement of the number. The sum of the 1'st complement and the binary number of a decimal is equal to the binary number of decimal 9. The process of converting BCD to Excess-3 is quite simple from other conversions. The Excess-3 code can be calculated by adding 3, i.e., 0011 to each four-digit BCD code. Below is the truth table for the conversion of

BCD to Excess-3 code. In the below table, the 0-9 decimal digits will convert into excess three codes.

We will do our project using a MEALY STATE MACHINE, whose state diagram is given below.

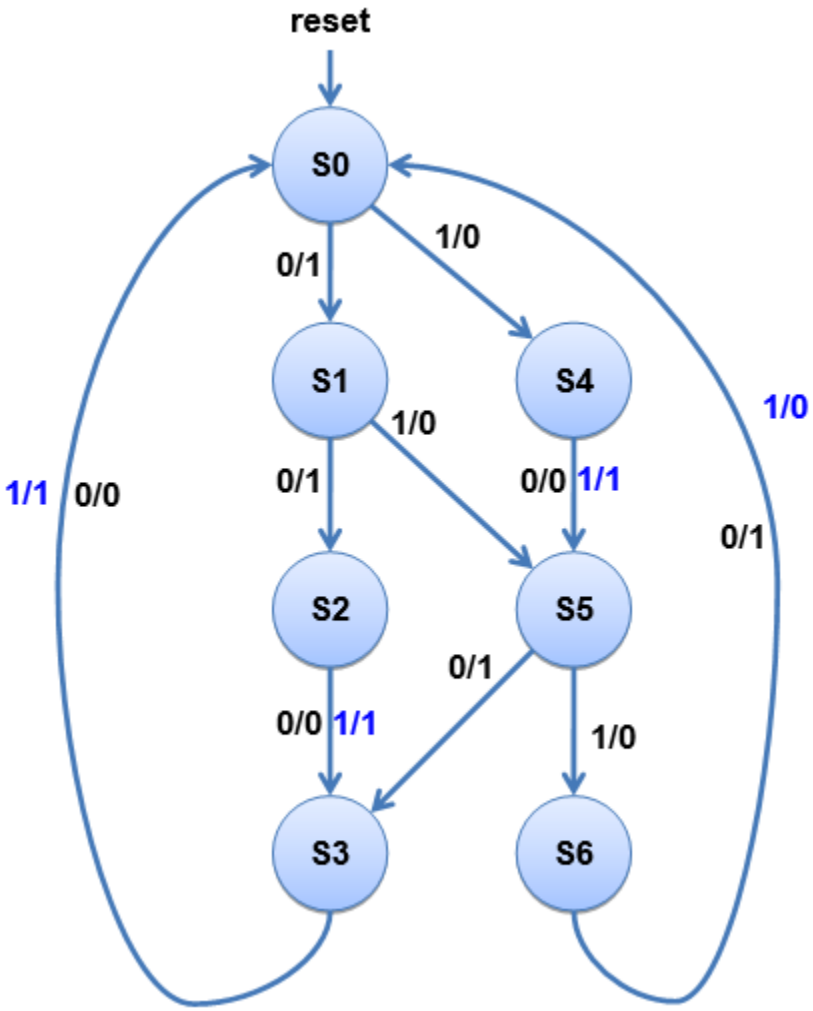
Proposed Methodology/ Circuit Diagram:



Conversion Table

Decimal Digit	BCD Code	Excess-3 Code
0	0000	0011
1	0001	0100
2	0010	0101
3	0011	0110
4	0100	0111
5	0101	1000
6	0110	1001
7	0111	1010
8	1000	1011
9	1001	1100

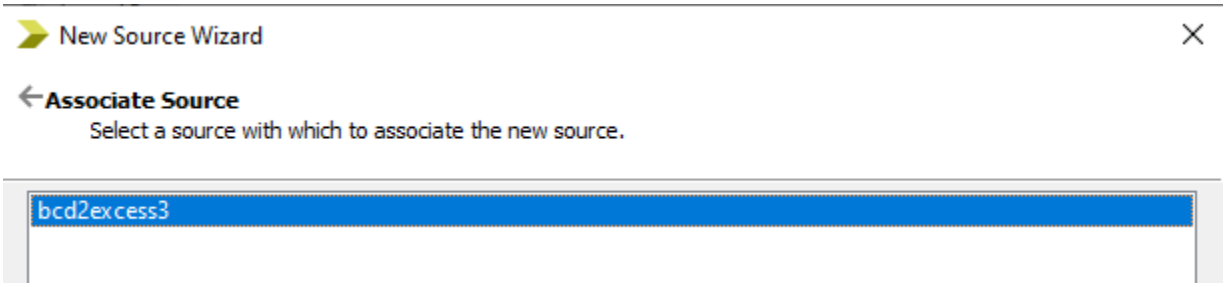
State Diagram :



✓ METHOD:

1. Xilinx Software:

Xilinx ISE (Integrated Synthesis Environment) is a discontinued software tool from Xilinx for synthesis and analysis of HDL designs, which primarily targets development of embedded firmware for Xilinx FPGA and CPLD integrated circuit (IC) product families. Xilinx solutions enable smarter, connected, and differentiated systems, integrating the highest levels of software-based intelligence with hardware optimization and any-to-any connectivity. Xilinx serves the aerospace and defense industry with commercial, industrial, military, and space grade products.



✓ WORKING ON XILINX:

By introducing the BCD TO EXCESS THREE and before practically implementation of thiswe perform all our logic and algorithms on Xilinx .
All the steps, simulations,test bench's, outputs are given in below both in pictorial way as well as in form of written code .

1. Verilog Code:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    18:44:58 06/07/2022
// Design Name:
// Module Name:    bcd2excess3
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module bcd2excess3(y, x, state, clk, reset);
    output y, state; input x, clk, reset;
    parameter  S0 = 3'd0,  S1 = 3'd1,  S2 = 3'd2,  S3 = 3'd3,  S4 = 3'd4, S5 = 3'd5, S6 = 3'd6;
    reg[2: 0] state, nxtstate;  reg y;
    always @ (posedge clk or negedge reset)
    if (reset== 0) state  <=  S0;  else state  <=  nxtstate;
    always @ (state or x)    begin

     case (state)

    S0:  if (x)      begin       nxtstate = S4;       y = 0;        end

     else         begin       nxtstate = S1;       y = 1;        end

     S1:    if (x)      begin       nxtstate = S5;       y = 0;        end

```

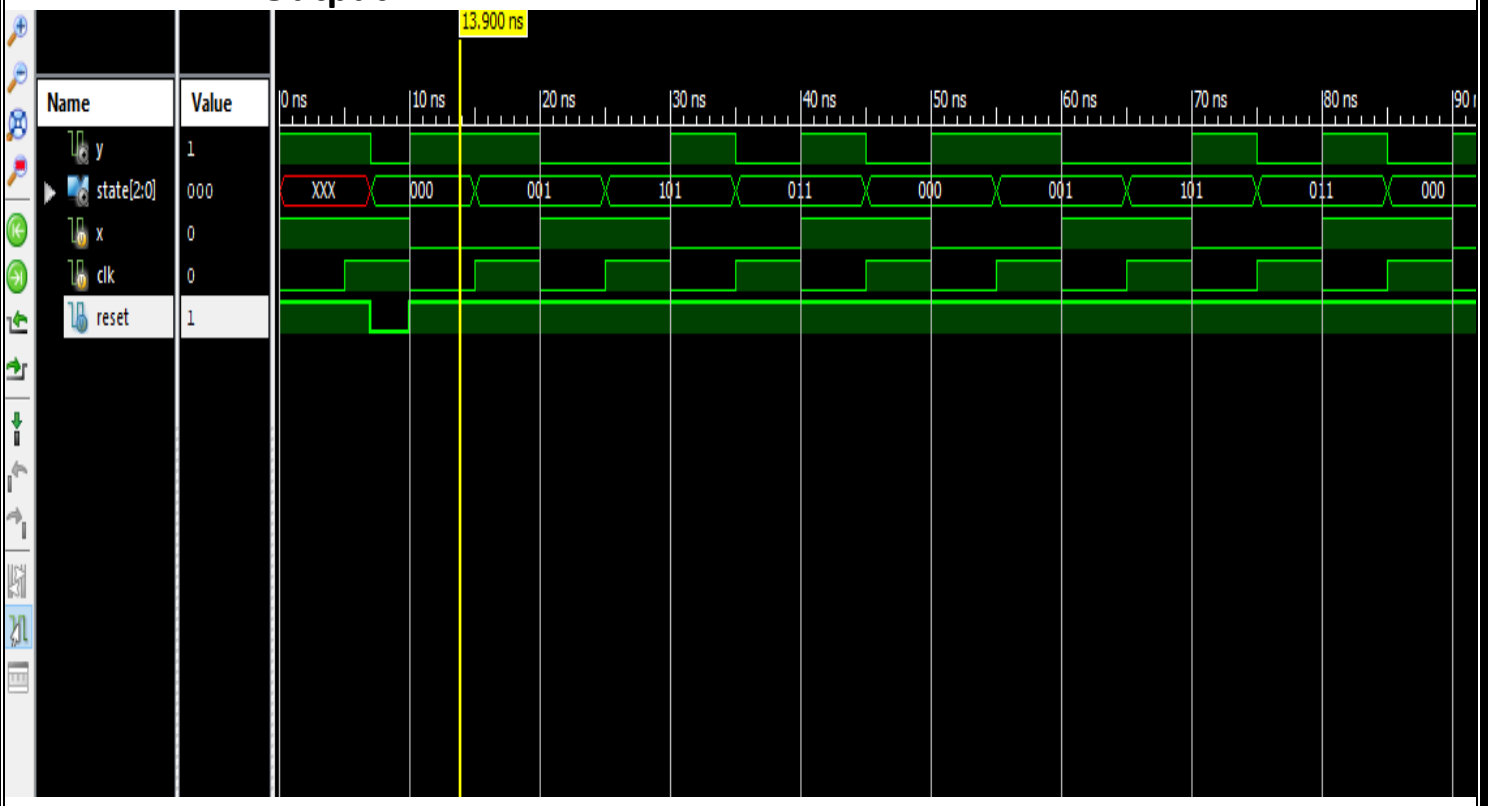
```
37      else          begin       nxtstate = S2;       y = 1;        end
38
39        S2:              begin    nxtstate = S3;       y = x;        end
40
41        S3:     begin    nxtstate = S0;       y = x;        end
42
43       S4:      begin    nxtstate = S5;       y = x;        end
44
45       S5:   if (x)   begin    nxtstate = S6;       y = 0;        end
46
47      else   begin nxtstate = S3;       y = 1;        end
48
49        S6:     begin    nxtstate = S0;       y = ~x;       end
50         default:  begin nxtstate = 3'dx;    y = x;        end
51         endcase
52         end
53         endmodule
```

1. Test bench:

```
1   `timescale 1ns / 1ps
2
3   ////////////////////////////////////////////////////////////////////////////////
4   // Company:
5   // Engineer:
6   //
7   // Create Date:   20:49:03 06/07/2022
8   // Design Name:   bcd2excess3
9   // Module Name:   U:/sem 6/dsd/usmanmajeed/tsb.v
10  // Project Name:  usmanmajeed
11  // Target Device:
12  // Tool versions:
13  // Description:
14  //
15  // Verilog Test Fixture created by ISE for module: bcd2excess3
16  //
17  // Dependencies:
18  //
19  // Revision:
20  // Revision 0.01 - File Created
21  // Additional Comments:
22  //
23  ////////////////////////////////////////////////////////////////////////////////
24
25  module tsb;
26
27     // Inputs
28     reg x;
29     reg clk;
30     reg reset;
```

```
31
32      // Outputs
33      wire y;
34      wire [2:0] state;
35
36      // Instantiate the Unit Under Test (UUT)
37      bcd2excess3 uut (
38          .y(y),
39          .x(x),
40          .state(state),
41          .clk(clk),
42          .reset(reset)
43      );
44      initial begin
45       reset = 1; #7 reset = 0; #3 reset = 1;
46
47  end
48            initial  begin    clk = 0;
49      repeat (20)         #5 clk = ~clk;
50      end
51      initial    begin      x = 1;
52      repeat (10)           #10 x = ~x;
53                    end
54  endmodule
55
```

1. Output:



1. Refrences:

- www.FPGA4FUN.com
- www.FPGA4STUDENTS.com
- www.ijmetr.com