Umang Garg

umang@ucsb.edu +1-805-724-9299

Linkedin Github Scholar

U.C. Santa Barbara, CA

TECHNICAL SKILLS

Languages: Python, C/ C++, MATLAB, Verilog/ Systemverilog, Assembly, HTML, RTL

Developer Tools/ Frameworks: Pytorch, Numpy, Pandas, Linux, Vivado Tool Suites, Cadence Virtuoso, DRC, LVS, PEX, Simulink, Arduino, Labview, GIT, Ansys HFSS, Zynq libraries, FPGAs, emerging memory.

PROJECTS

Rational AI multi-agent design for PACMAN | Python, DSA, Heuristics **Feb '21 - March '21**

- Designing multi-adversary-aware intelligent Pacman AI agent: reflex-based, Minimax, Expectimax models.
- Goal-tailored heuristic modelling. Implemented greedy search, α-β pruning, iterative deepening to time-limit.

Unsupervised SNN Learning for Digit Recognition | SNNTorch | Verilog **Jan 2021**

- Implemented end-to-end neural network in digital RTL-logic with in-situ **online STDP learning** support.
- New local unsupervised learning mechanisms Inter-synaptic traces mechanisms tested. Lateral inhibition etc.

Parallel time-domain Compute-in-memory (CIM) Spiking NN | Pytorch, Virtuoso **Sept - Dec '21**

- Collaborated and developed time-domain parallel spiking paradigm: **83x EDP improvement** over SOTA.
- Reimagined dataflow for better weight reuse. Tested on Fashion-MNIST, NMNIST, CIFAR-10 datasets.

Accelerating Auditory Recognition on edge- FPGA | Verilog, CompArch **Sept - Dec '21**

- Implemented hardware accelerator for audio recognition, achieving **10x improvement** over CPU.
- Employed **Algo-HW co design** techniques: mixed precision processing, multiplier tree, pipeline, Max pool.

Developing 'TETRIS' firmware on Xilinx FPGA | Embedded C, QPNano, Vivado **Sept - Dec '21**

- Used QPNano **Hierarchical FSM** for designing game states on Xilinx Artix-A7 board on Vivado.
- Interfaced SPI LCDs and push buttons for interactive gameplay; ensured correct **interrupt handling**.

Hyperspectral Aerial-Vehicle Anomaly detection at Edge | MATLAB, Virtuoso **May '19 - Aug '19**

- Worked on hyperspectral aerial anomaly detection techniques and multi-band flexible-grain filter design.
- Co-integrated anomaly detection unit with hypersectral imager for system-constrained perception.

INDUSTRY EXPERIENCE

QpiAI Technologies | *Design Engineer* Dec '20 – Jul '21 | *Bangalore, India*

- Developed "Auxiliary Pulse Cancellation" code, boosting qubit fidelity times by 10x. **2 US patents.**
- Filed **US patent** proposing an extensively scalable in-silco solution for magnetic field control for qubits.
- Designed a rail-to-rail cryogenic Variable gain amplifier: deployed as **standalone IP** for qubit control.

EDUCATION

University of California, Santa Barbara (UCSB) Sept 2021 – Present

M.S. in Computer Engineering, Dept. of ECE; GPA: 3.90 *Santa Barbara, CA*

Birla Institute of Science and Technology, Pilani Aug 2016 – May 2020

B.E. in Electronics and Instrumentation; GPA - 8.4 *Pilani, India*

RELEVANT COURSEWORK

Graduate: Data Structures and Algorithms, Artificial Intelligence, Adv. Deep Neural Networks (*upcoming*), Software-HW Co-Design, Embedded Systems, Neuromorphic Computing, Probabilistic Computing

UnderGraduate: Analog and Digital VLSI Design, Computer Architecture, RF Microelectronics

PATENTS and PUBLICATIONS

Publication [1]. Time-domain Parallel Compute-in-memory Spiking Neural Network Architecture and acceleration

Patent [2]. Method and System for designing hybrid quantum-classical architecture (Q-arc) in quantum computers for individual qubit control in distributed fashion. *(3 additional major-Conference publications and 2 more patents)*