# Umang Mishra

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## Education

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| 2024-26 | Master of Technology, Communication System Engineering (ECE)<br>National Institute of Technology Jamshedpur | CGPA: 8.20 |
| 2020-24 | Bachelor of Technology, Electronics & Communication Engineering<br>Dr. APJ Abdul Kalam Technical University, Lucknow | CGPA: 7.61 |
| 2020 | AISSCE(12th), CBSE<br>Vishwa Bharati Public School, New Delhi | Percentage: 82.6% |
| 2018 | AISSE(10th), CBSE<br>Vishwa Bharati Public School, New Delhi | Percentage: 89.2% |

## Experience

- **Technical Intern at NXP Semiconductors** **July 2025 - Present**
  - As a Firmware Automotive Security Technical Intern at NXP Semiconductors, I work on writing and maintaining embedded system code focused on automotive security.
  - My role involves developing secure firmware modules, debugging low-level hardware-software interactions, and ensuring robust implementation of security features in real-time embedded environments to meet automotive safety standards.
- **Teaching Assistant at NIT Jamshedpur** **August 2024 - July 2025**
  - Assisted faculty in teaching, mentoring, lab supervision, grading, and providing technical guidance in electronics, programming, and research activities.
- **Research Intern at DRDO** **July 2023 - August 2023**
  - Designed a small signal analog model of passive components using Monolithic Microwave IC technology and Advanced Design System software for defence applications.

## Projects

- **Synchronous FIFO Design and Simulation using Verilog**
  - Designed and simulated a synchronous FIFO (First-In-First-Out) buffer for efficient data transfer in hardware systems.
- **AI-Based Fault Detection in VLSI Circuits**
  - Implemented an AI model using Python to detect faults in Verilog-based digital circuits, enhancing reliability and accelerating debugging in VLSI verification processes.
- **Automated Testbench Generator using Python**
  - Designed a Python-based tool to auto-generate Verilog/SystemVerilog testbenches from RTL modules, streamlining verification workflows and reducing manual effort in functional simulation.
- **Design of Cascode Amplifier and Common Source Amplifier using Cadence Virtuoso**
  - Designed and simulated a Common Source Amplifier using MOSFETs to achieve high voltage gain and moderate input impedance. Conducted performance analysis and optimisation using Cadence Virtuoso.
- **Design of PWM generator circuit using Cadence Virtuoso**
  - Designed a high-performance PWM generator circuit using Cadence Virtuoso with 90 nm CMOS technology, focusing on low power consumption and signal accuracy.
- **Efficient Multiplier Design using Booth's Algorithm**
  - Implemented Booth's algorithm in Verilog to perform high-speed signed multiplication with minimized partial products. Verified functionality through simulation and achieved efficient hardware utilization using Xilinx Vivado.
- **Power Estimation using ML in RTL Designs**
  - Designed an ML model using Python to predict power consumption of RTL blocks, enabling early-stage power estimation and optimization in VLSI design workflows in System Verilog.
- **Designed a CAN Bus-Based Vehicle Monitoring System**
  - Developed a CAN-based vehicle monitoring system using ATmega328P. Implemented interrupt-driven communication, message filtering, and real-time data display to simulate multi-ECU interactions effectively using C and a microcontroller.
- **UWB Array Antenna**
  - Designed a planar ultra-wideband antenna using a stripline feeding network with an operating frequency 6-8.5GHz in CST Studio.
- **Digital Potentiometer Control via I2C Protocol**
  - Controlled an audio signal's gain using an I2C-interfaced digital potentiometer, implementing smooth level adjustments via Embedded C and microcontroller-based real-time communication.

- **4-bit ALU using FPGA**
  - Designed a 4-bit ALU on FPGA performing basic arithmetic and logic operations like addition, subtraction, AND, OR using Verilog.
- **Implementation of a Coin-Based Vending Machine using Xilinx Vivado**
  - Designed a Finite state machine-based vending machine in Verilog to dispense products based on user input and coin detection. Implemented and verified functionality using Xilinx Vivado with testbenches for various input scenarios.
- **Design and Implementation of 7-Segment Display using FPGA**
  - Implemented a 7-segment display controller using Verilog to display decimal digits from binary input. Deployed and tested the design on an FPGA using Xilinx Vivado for real-time visual output.
- **CMOS-Based Ring Oscillator**
  - Designed a ring oscillator circuit using CMOS inverters and analysed frequency characteristics.
- **Dual Port RAM using Verilog**
  - Designed Synchronous Dual Port RAM, enabling simultaneous Read and Write Operation from two independent ports.
- **16:1 Multiplexer using Verilog**
  - Designed a 16:1 multiplexer (MUX) using a behavioural 4:1 MUX as a building block in a structural modelling approach.
- **Voice Activity Detection using MATLAB**
  - Utilised an energy-based method to detect voice activity in audio signals by analysing audio signals and implemented frame-based energy calculations to determine speech presence and showcase frame energy and voice activity.
- **Wireless EV Charger**
  - Developed a cutting-edge wireless charging system for electric vehicles (EVs), eliminating the need for physical cables and connectors with 80% electrical power efficiency.
- **Unmanned Aerial Vehicle**
  - Designed & developed a basic drone prototype using off-the-shelf components, implemented flight control algorithms using a mission planner, enabling stable flight manoeuvres, altitude hold, and primary autonomous navigation with a range of 800m with 98% efficiency.
- **Trip Pay (MSME)**
  - Designed a **GoI-funded** mobility solutions hardware for connecting customers to drivers and commercial vehicles.
  - Incorporated GPS tracking and IoT connectivity to deliver real-time updates on traffic conditions and public transportation schedules.

## Technical Skills

- **Languages:** C, C++, Python, Verilog
- **Tools:** Cadence Virtuoso, Xilinx Vivado, Synopsys EDA Tools, EDA Playground
- **Frameworks:** MATLAB, Simulink
- **Operating System:** Windows, LINUX
- **Area of Interests:** Embedded Systems, VLSI, Digital Electronics, Signal Processing, Wireless Comm.

## Certifications

- Electronic Devices
  (All India Council of Technical Education)
- Digital System Design
  (All India Council of Technical Education)
- Introduction to Internet of Things & Embedded Systems
  (Coursera)

## Academic Achievements

- Qualified **GATE-2024** in **Electronics and Communication**.
- Qualified **JEE (MAIN) 2020**

## Extra-Curricular

- Training & Placement Coordinator, Internship Coordinator of NIT Jamshedpur
- President, Technical Head, Technical Subhead of Aeronautical Society, IPEC, AKTU
- Core member at UDBHAV, 2024(Annual Techno-Cultural Fest), IPEC.