

# Umang Mishra

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## Education

|         |  |                   |
|---------|--|-------------------|
| 2024-26 | Master of Technology, Communication System Engineering (ECE)<br>National Institute of Technology Jamshedpur                              | CGPA: 8.20        |
| 2020-24 | <a href="#">Bachelor of Technology, Electronics &amp; Communication Engineering</a><br>Dr. APJ Abdul Kalam Technical University, Lucknow | CGPA: 7.61        |
| 2020    | <a href="#">AISSCE(12th)</a> , CBSE<br>Vishwa Bharati Public School, New Delhi   | Percentage: 82.6% |
| 2018    | <a href="#">AISSE(10th)</a> , CBSE<br>Vishwa Bharati Public School, New Delhi  | Percentage: 89.2% |

## Experience

- **Technical Intern at NXP Semiconductors**
  - As a Firmware Automotive Security Technical Intern at NXP Semiconductors, I work on writing and maintaining embedded system code focused on automotive security.
  - My role involves developing secure firmware modules, debugging low-level hardware-software interactions, and ensuring robust implementation of security features in real-time embedded environments to meet automotive safety standards.
- **Research Intern at DRDO**
  - Designed a small signal analog model of passive components using Monolithic Microwave IC technology and Advanced Design System software for defence applications.

## Projects

- **Synchronous FIFO Design and Simulation using Verilog**
  - Designed and simulated a synchronous FIFO (First-In-First-Out) buffer for efficient data transfer in hardware systems.
- **Implementation of a Coin-Based Vending Machine using Xilinx Vivado**
  - Designed a Finite state machine-based vending machine in Verilog to dispense products based on user input and coin detection. Implemented and verified functionality using Xilinx Vivado with testbenches for various input scenarios.
- **Design and Implementation of 7-Segment Display using FPGA**
  - Implemented a 7-segment display controller using Verilog to display decimal digits from binary input. Deployed and tested the design on an FPGA using Xilinx Vivado for real-time visual output.
- **Efficient Multiplier Design using Booth's Algorithm**
  - Implemented Booth's algorithm in Verilog to perform high-speed signed multiplication with minimised partial products. Verified functionality through simulation and achieved efficient hardware utilisation using Xilinx Vivado.

## Technical Skills

- **Languages:** C, C++, Python, MySQL, Verilog
- **Tools:** Cadence Virtuoso, Xilinx Vivado, EDA Playground
- **Frameworks:** MATLAB, Simulink
- **Operating System:** Windows, LINUX
- **Area of Interests:** Embedded Systems, Digital Electronics, VLSI, Analog Electronics.

## Certifications

- [Electronic Devices](#)  
(All India Council of Technical Education)
- [Digital System Design](#)  
(All India Council of Technical Education)
- [Introduction to Internet of Things & Embedded Systems](#)  
(Coursera)

## Academic Achievements

- Qualified **GATE-2024** in **Electronics and Communication**.
- Qualified **JEE (MAIN) 2020**

## Extra-Curricular

- President, Aeronautical Society, IPEC, AKTU
- [Core member at UDBHAV, 2024\(Annual Techno - Cultural Fest\), IPEC.](#)