
ERRATA EMBER® EM351, EM357

The document describes issues that pertain to the Ember EM351 and EM357 ICs.

This Errata refers to the following releases of the chip data sheet:

- 120-035X-000 revision G

The EM351 and EM357 chips have the following issues:

1 SYSRESETREQ causes lockup when asserted in full clock mode

There is a bug in the chip, which means that when using external debuggers the chip may lock up in certain CPU clock modes. Affected modes are operating the CPU at 24 MHz derived from the 24 MHz crystal, or 12 MHz derived from the high frequency RC oscillator. If an external debugger tool asserts SYSRESETREQ, the chip will lock up and require a pin reset or power cycle.

SYSRESETREQ is an ARM Cortex

☐ signal that ca

This error condition applies to operation with a debugger; it does not affect devices in the field.

Affected Conditions

This issue is present in revisions A and B of silicon.

Workaround

Silicon Labs has confirmed by tests, and by discussion with IAR, that the IAR ARM debugger does not assert SYSRESETREQ, and therefore will not exhibit this issue. Other debuggers have not yet been tested, and therefore may exhibit this issue.

It is recommended to use the IAR toolchain for debugging the EM351 and EM357.

Customers should not write to the SCS_AIRCR register directly from application code. The EmberZNet HAL reset APIs should be used instead which ensure that the chip is in a safe clock mode prior to triggering the reset.

2 ARM® Cortex™-M3 Errata

ARM published an Errata for the Cortex-M3, which can be found on ARM's public website.

<http://infocenter.arm.com/help/topic/com.arm.doc.eat0420d/Cortex-M3-Errata-r2p1-v3.pdf>

The version of the Cortex-M3 in the EM35x chips is r1p1.

There are 6 “category 2” errata in this release. “Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.”

429964: Async not generated if no trace in previous session

ETM is not implemented in the EM35x chips, so does not apply.

429965: Trigger packets sometimes not inserted in trace stream

ETM is not implemented in the EM35x chips, so does not apply.

563915: Event Register is not set by interrupts and debug

Ember software uses the WFI instruction instead of the WFE instruction when sleeping, therefore is not affected.

602117: LDRD with base in list may result in incorrect base register when interrupted or faulted

Ember software supports the IAR EWARM toolchain. Versions 5.30 and later do not utilize the affected instructions.

740455: SVC and BusFault/MemManage may occur out of order

Ember software does not currently use the SVC instruction, therefore is not affected.

752419: Interrupted loads to SP can cause erroneous behaviour

No compilers currently available for Cortex-M3 generate code that would be affected. Users should review any application code they have written in assembler and apply the workaround if necessary. Ember software does not include any assembly affected by this problem.

There are also some “category 3” errata: “Behavior that was not the originally intended behavior but should not cause any problems in applications.”

Affected Conditions

These issues are present in revisions A and B of silicon.

Workaround

Silicon Labs has confirmed.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page for ZigBee products:
www.silabs.com/zigbee-support and register to submit a technical support request

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories, Silicon Labs, and Ember are registered trademarks of Silicon Laboratories Inc.

Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.

