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"Design and Implementation of Lock-In Amplifier for Bioimpedance Measurement"

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ABSTRACT

Bioimpedance analysis is a non-invasive, low cost and a commonly used approach for body composition measurements and assessment of clinical condition. Presently, various methods are available for the measurement of bioimpedance. However, traditional bioimpedance measurement methods experience various problems in terms of speed, bandwidth and accuracy for extracting the cellular impedance information. The lock-in method is one of the most frequently used methods for regeneration of measured signal, to determine the modulus and phase of the bioimpedance. High noise immunity of the lock-in demodulation technology allows one to obtain the signals corresponding to amount of the cellular constituents in one person, from bioimpedance variations.

In this report, Optimized Technique to implement Synchronous Demodulator is presented. Various block parameters of proposed design were analyzed. Block wise simulation and testing was done on FPGA Spartan 3E kit using Hardware Co-Simulation. Selection of various block parameters was justified quantitatively and qualitatively. For Simulation and Testing purpose Sine wave of 1 kHz Frequency, 0.1 $V_{(p-p)}$ was used with added noise of different frequency from 50 Hz to 3 kHz , 0.01 $V_{(p-p)}$. Optimization for working voltage Range and Noise level of -45 to -50 dB was achieved with the filter order of 4. Results were compared with sampled analog technology based synchronous demodulator IC i.e. ADA 2200.

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1. INTRODUCTION

Bioimpedance measurement has great potential in biomedical field. Fingerprint recognition system is now not only used in high security application but also used in consumer applications. According to a Researchers led by Stephanie Schuckers, 90% of security systems can be easily fooled with fake fingers made out of Play-Doh[1]. One of the possible solution to this problem is bioimpedance based detector[2]. As number of people having access to modern medical facilities are increasing there is a great need to develop robust and quick detection and diagnostic tools for them. Over the past few years biomedical sciences have shown considerable growth in detection, diagnosis as well as prevention of major diseases. But there is always scope of improvement. There is a requirement of cheap and hand-held non-invasive methods for detection of various biomedical parameters like Heart Rate, Cerebral Monitoring and so on especially in the field of diagnosis. Invasive techniques especially cerebral ones (brain) carry some amount of infection risk. There are some methods like X-ray, MRI etc. which are non-invasive and accurate but the instruments required are costly and bulky [3]. Bioimpedance measurement is one such tool in our arsenal which can revolutionize the medical world. It is a noninvasive, low cost and a commonly used approach for body composition measurements and assessment of clinical condition. Bioimpedance measurement is robust and gives instantaneous results about a patient given proper instruments are used. But, there are many challenges to overcome before its benefits can be reaped.

1.1 Overview

The focus of this project is to implement a lock in amplifier for bioimpedance modulator. Lock-in method is one of the most used methods for the reconstruction of measured signals applied in the bioimpedance measurements to determine modulus and phase of the bioimpedance signal[3].

A lock-in amplifier extracts a signal of interest at a known frequency from an aggregate output signal, which can include significant noise levels at other frequencies. A typical application of a lock-in amplifier is for the purpose of increasing the signal-to-noise ratio

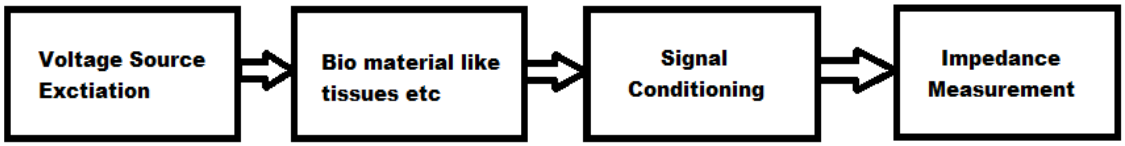


Fig. 1.1 : Basic Block Diagram of Bioimpedance Devices[3]

of the any measuring system, by synchronizing the output signal to the input signal at a particular (known) frequency; subsequent filtering of other frequencies removes noise at those frequencies, hence increasing the signal-to-noise ratio. Lock-in amplifiers can be used in this manner to measure impedance, taking advantage of the reduced noise enabled by single frequency measurements [3].

There are some parameters that need to be considered while designing a bioimpedance modulator.

1) The source excitation needs to be in the range of few millivolts to a few microvolts [4].
2) The current through the body during the measurement should be lower than few milli-amperes [4].

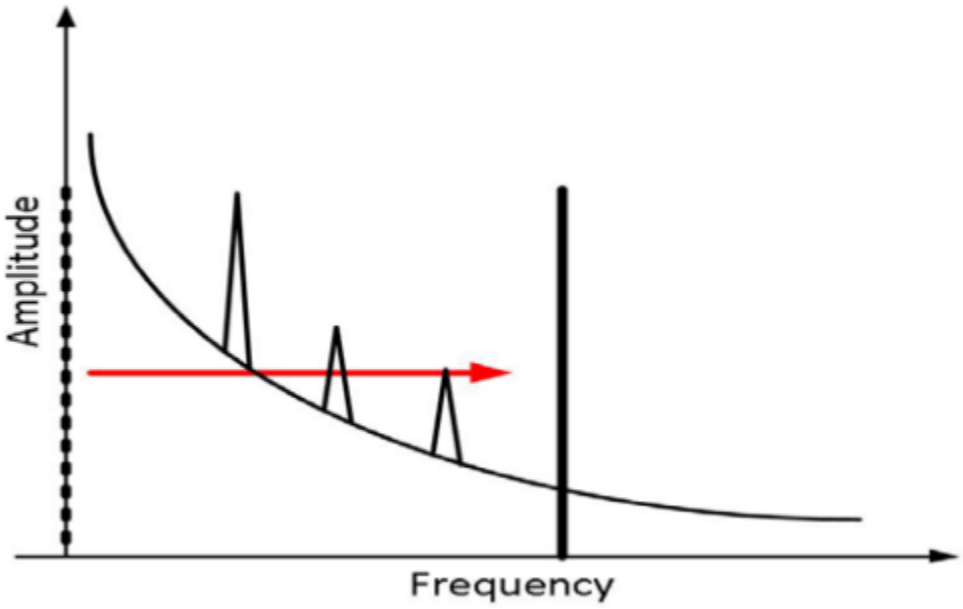
1.2 Motivation

The motivation lies with the extensive research that is going on in the area of biomedical sciences Out of many applications of bioimpedance measurement one of them is a handheld, non-invasive device that can measure important parameters of body like heart rate instantaneously. It would benefit the doctors, patients and even the common man as they would be able to check the important parameters of body instantaneously at home itself. But a major problem in bioimpedance measurement is that we cannot use high voltage source for taking measurement as it will damage the sensitive tissues of the body [3]. High source voltage is required to improve the SNR and ensure faithful results. We need an effective way to isolate low voltage signal from noise as the SNR is very low. This is a bit challenging part as it demands accurately extracting signals which are even smaller than noise levels like measuring very small resistance, measuring light absorption etc.[5]

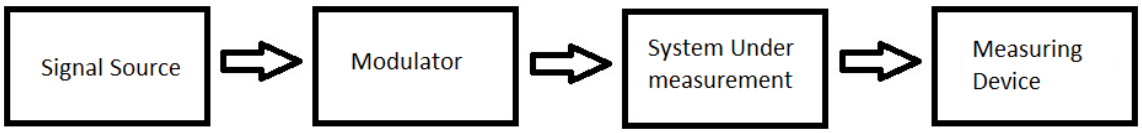
In synchronous detection, the signal source is modulated at higher frequencies away from low frequency noise to improve signal to noise ratio. Signal is then measured through a

suitable measuring device which is a lock-in amplifier in this case [5]. The concept of synchronous detection in a lock-in amplifier can be used to greatly improve the accuracy of handheld measuring systems. In many electrical and electronic systems noise increases as we move towards zero frequency. For example, there is a 1/f noise in Operational amplifiers. Asynchronous detection which was traditionally used in biomedical measurements exhibits following issues.

1) The strength of source excitation used to measure bioimpedance is comparable to noise power which made its extraction by asynchronous detection highly error prone [5]
2) The components required for asynchronous detection like Amplifiers has to be low noise and highly precise which increases the cost of the system [5]



(a)



(b)

Fig. 1.2: (a) Modulating the Signal to Move it away from Noise Sources [5] (b) Basic Block Diagram of Synchronous Detection [5]

Synchronous detection take measurement at higher frequencies and then the lock-in amplifier extracts the required signal information thereby reducing noise. Such variation of noise with frequency is shown in Fig. 1.2.

1.3 Problem Statement

The work targets the design and implementation of synchronous detection based Lock in Amplifier for bioimpedance measurement.

The specific objectives of the project are as follows:

1) Error free and reliable extraction of very low signal voltages (few microvolt (uV) to millivolt (mV)) with phase as well as amplitude information.
2) Removal of noise from signal by extracting the signal at a specified frequency away from any known noise source.
3) Design and implementation of lock-in amplifier which can achieve the above two objectives reliably. It would be specifically tuned for bioimpedance measurement only.

To achieve above mentioned objectives we are going to fulfill following tasks:

1) To implement the design of lock-in amplifier on system generator and simulate the results.
2) To determine useful range of frequencies for bio impedance measurement and optimize the design of lock-in amplifier for these range of frequencies.
3) To implement the auto generated code on FPGA and analyze the implemented hardware.

1.4 Organization of the Report

The report starts with an introduction to bioimpedance and the importance of measuring it in biomedical field in chapter 1. It introduces the significance of lock in amplifier and states its application in bioimpedance measurement. Chapter 2 mainly deals with Bioimpedance measurement techniques. It also gives the description of human body components and cellular constituents as well as basics of bioimpedance measurements and detailed description of techniques for classification of measurement systems. The chapter 3 deals with the proposed design for Lock in Amplifier and description of the blocks used. Chapter 4 contains simulation of each block separately and as a whole circuit. It also contains optimization related methods and comparisons. Chapter 5 shows the implementation of system on FPGA. In the end, Conclusion and Future work is presented

2. BIOIMPEDANCE MEASUREMENT TECHNIQUES

Bioimpedance analysis is a broadly applied approach used in body composition measurements and healthcare assessment systems. The essential fundamentals of Bioimpedance measurement in the human body and a variety of methods are used to interpret the obtained information. In addition there is a wide spectrum of utilization of Bioimpedance in healthcare facilities such as disease prognosis and monitoring of body vital status. Thus, with such a broad applications, here in this section fundamentals of Bioimpedance and its techniques will be presented.

2.1 Introduction

The human body as a volume is composed generally of **F**at **M**ass (FM) which is considered as a non-conductor of electric charge and is equal to the difference between **B**ody **W**eight (Wt_{body}) and **F**at **F**ree **M**ass (FFM), as shown in Eq. (2.1); and FFM, which is considered as the conducting volume that helps the passing of electric current due to conductivity of electrolytes dissolved in body water. Fig. 2.1 shows basic body compartments of human

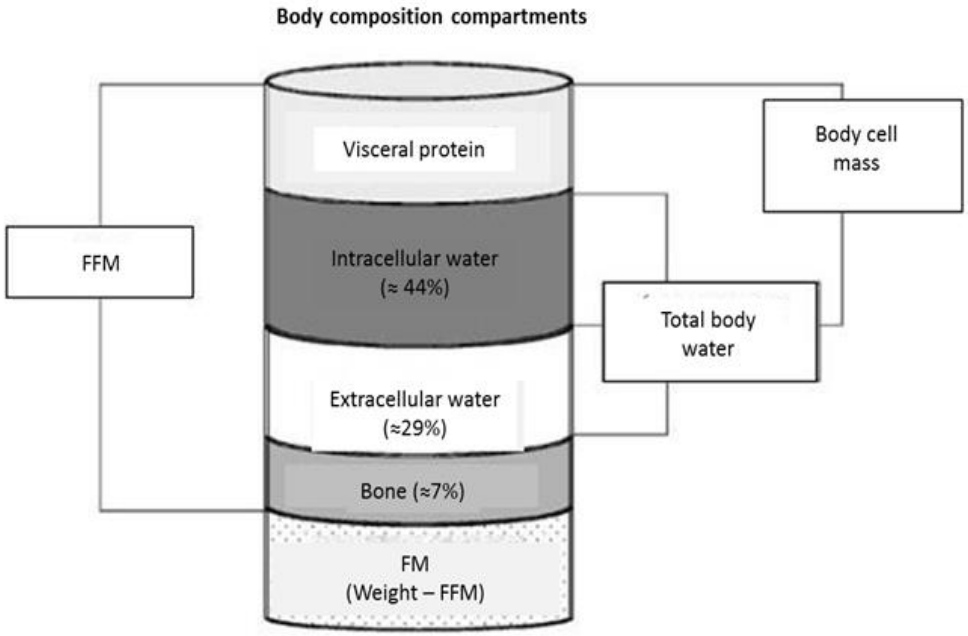


Fig. 2.1: Human Body Constituents [7]

body volume. Studies show that water, known as **T**otal **B**ody **W**ater (TBW) is the major compound of FFM and is equal to 73.2% in normal hydration subjects, as in Equation (2.2) [6]:

$$FM = Wt_{body} - FFM \quad (2.1)$$

$$TBW = 0.73\ FFM \quad (2.2)$$

In Bioimpedance measurements, the human body is divided into five inhomogeneous segments, two for upper limbs, two for lower limbs and one for the trunk. In the five compartment module, the human body is composed of FM and FFM which consists of bone minerals and **B**ody **C**ell **M**ass (BCM) that include protein and total body water that consists of **E**xtracellular **F**luid (ECF) and **I**ntracellular **F**luid (ICF) [4]. Fig. 2.2, shows the five segments and compartments of human body.

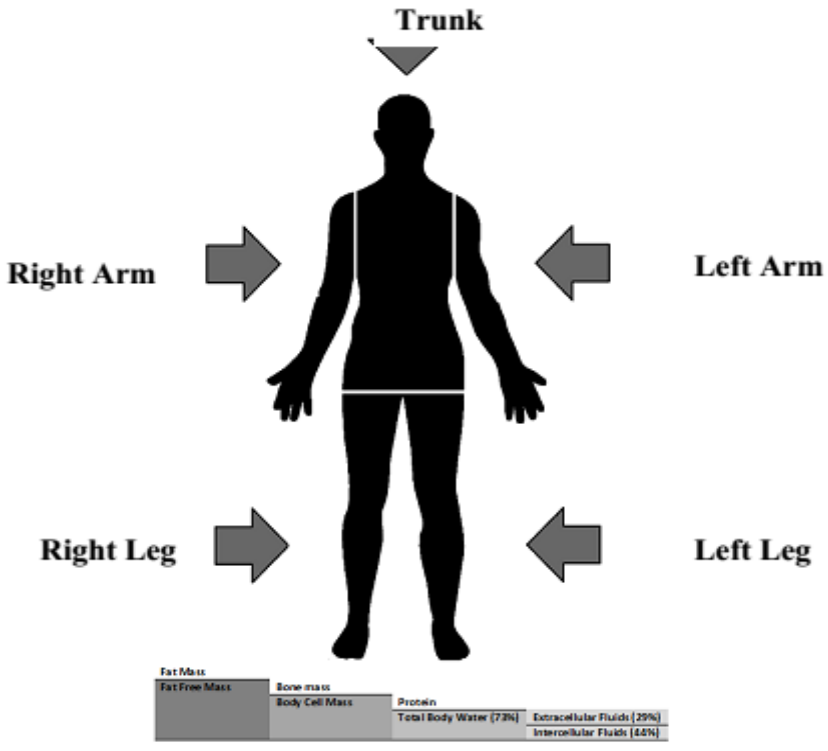


Fig. 2.2: Main Body Segments and Compartments[7]

2.2 Fundamentals of the Bioimpedance Measurements

Impedance (Z), from an electrical point of view, is the obstruction to the flow of an alternating current and, hence, is dependent on the frequency of the applied current, defined in impedance magnitude (|Z|) and phase angle (φ) as shown in Eq. (2.3)-(2.5) [8]. As shown

in Fig. 2.3, Bioimpedance is a complex quantity composed of resistance (R) which is caused by total body water and reactance (X_c) that is caused by the capacitance of the cell membrane[4][9]:

$$Z=R+ j\ X_c \tag{2.3}$$

$$|Z| = \sqrt{R^2 + X_c^2} \tag{2.3}$$

$$\Phi = \tan^{-1}\left(\frac{X_c}{R}\right) \tag{2.4}$$

Body composition estimation using Bioimpedance measurements is based on determination of body volume (V_b) through the basic means of resistance measurement. Value of Resistance gives the ratio of length (L) to surface area (A) then body volume (V_b) can be obtained by substituting the surface area (A) with the numerator and denominator of the length (L), as in Eq. (2.6):

$$V_b = \rho \frac{L^2}{R} \tag{2.5}$$

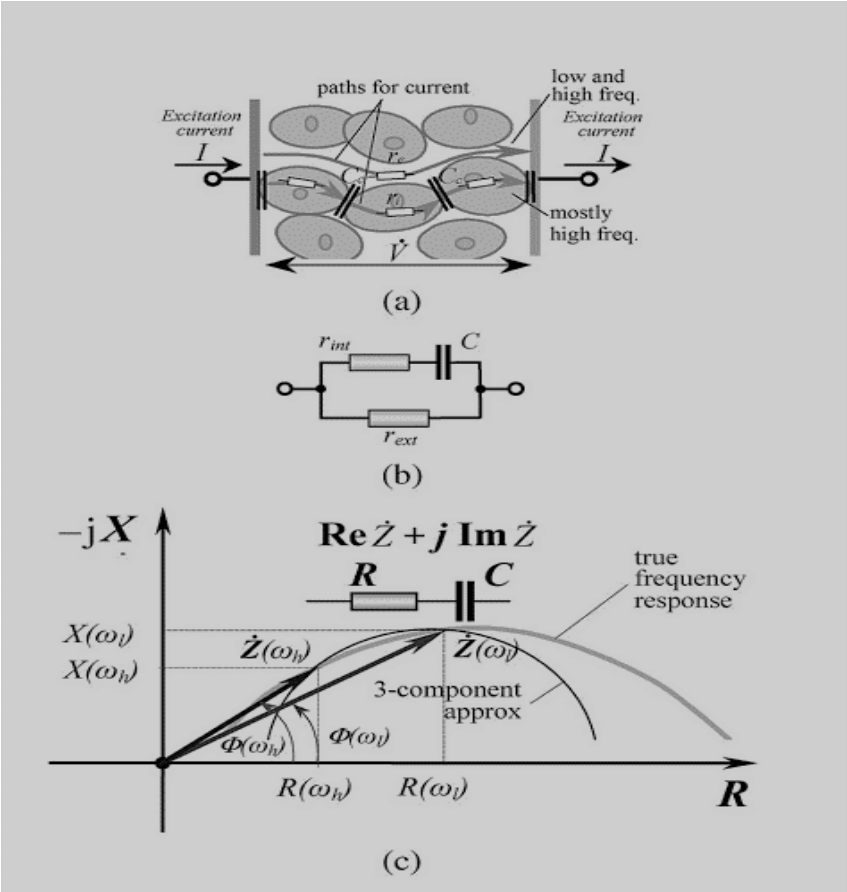


Fig. 2.3: (a) Formation of the electrical Bioimpedance (b) The three component equivalent (c) The Phasor Diagram of the static complex impedance between a pair of electrodes for two frequencies, Low ω_l and ω_h [3]

2.3 Frequency Based Bioimpedance Analysis

Analysis of Bioimpedance information obtained at 50 KHz electric current is known as **S**ingle-**F**requency **B**ioimpedance **A**nalysis (SF-BIA). SF-BIA is the most used and is one of the earliest proposed methods for the estimation of body compartments, It is based on the inverse proportion between assessed impedance and TBW, that represents the conductive path of the electric current [4][10].

Analysis of Bioimpedance that is obtained at more than two frequencies is known as **M**ultiple-**F**requency **B**ioimpedance **A**nalysis (MF-BIA). MF-BIA is based on the finding that the ECF and TBW can be assessed by exposing it to low and high frequency electric currents, respectively. Thomasset [11] has proposed TBW and ECF estimation using 100 and 1 kHz based on the Cole model [12]. However, in later years, Jaffrin *et al*. [13] stated that technically a Bioimpedance analyzer should use frequency range between 5–1000 kHz. Simpson *et al.* [14] state that low frequency in MF-BIA is generally less than 20 KHz and high frequency is more than 50 KHz. Hannan *et al.* [13] report that parameters measured using a frequency of less than 5 KHz and more than 200 KHz fluctuate around the actual value and conclude that estimated TBW is more accurate using the MF-BIA than the BIS method with the same predicted values of ECF for both methods. Patel *et al.* [15] reported that in diseased subjects, TBW prediction using SF-BIA gave more precise results than MF-BIA. In general, the MF-BIA method predicts ECF more precisely than the SF-BIA method; however in elderly diseased subjects the MF-BIA method shows less sensitivity in detecting fluid shifts between ECF and ICF [16].

Analysis of Bioimpedance data obtained using a broad band of frequencies is known as **B**io **i**mpedance **S**pectroscopy (BIS). The BIS method is based on the determination of resistance at zero frequency (R_0) and resistance at infinity frequency (R_{inf}) that is then used to predict ECF and TBW, respectively [7].

2.4 Methods of Cellular Impedance Measurements

There are several impedance measurement approaches developed for testing electrical components or materials. However, applications in cell assays make stricter demands of measurement instruments. In cellular impedance measurements, low noise excitation sources, high sensitive acquisition circuits are required, as well as current limitation for keeping cellular viability, and subsequent signal processing for calculating cellular

impedance from the measured data. Lock-in amplifiers and impedance analyzers are usually applied in cell impedance measurements.

2.4.1 Lock-In Amplifiers

Lock-In amplifiers are commonly utilized for measuring the small signal from any cellular action or response. It applies **P**hase-**S**ensitive **D**etection (PSD) technique, where a reference signal is used to recover a narrow-band response from broadband noise [17]. The technique is suitable for separating the response of a system to an applied stimulus from the noise background, which is widely applied in many scientific fields for many years [18][19]. By measuring the coherent system response from an excitation AC signal, the lock-in technique can detect even minute changes in magnitude and phase, so it can be used to characterize the impedance of samples under test [20].

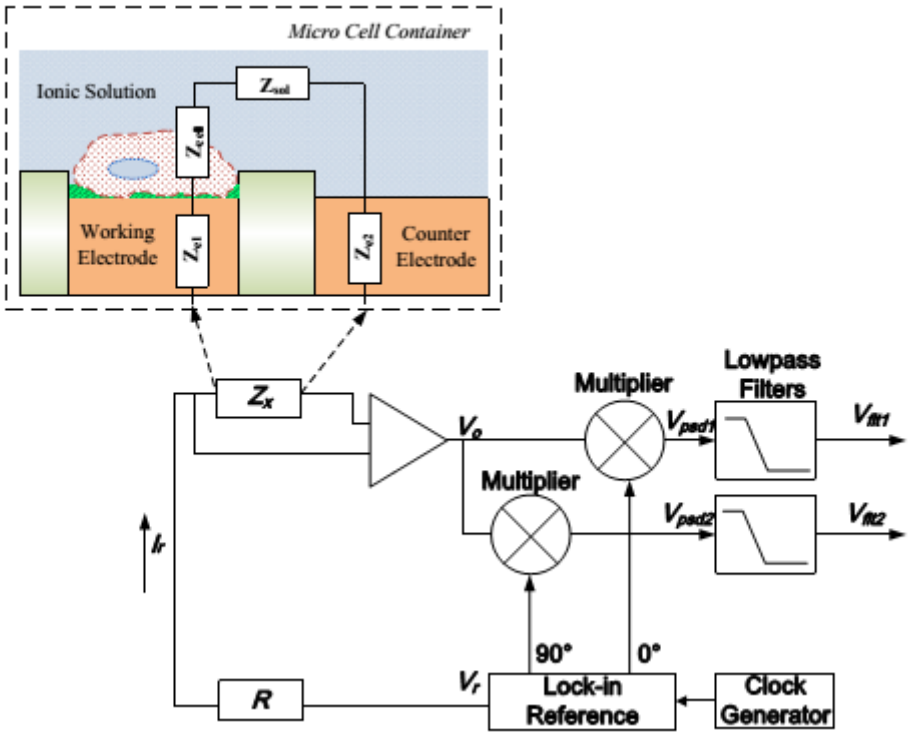


Fig. 2.4: Principal Diagram of Lock-In Amplifier based Cell Measurements [29]

Typically, the lock-in-amplifier based cell impedance measurements are conducted in the following procedures. A constant AC voltage is applied to cell- electrolyte-electrode system and a current limiting resistor. Therefore the cell will not be influenced by electrical stimulation during the impedance measurement [21]. The resulting electric potential between the working electrode and the counter electrode is measured. In order to

avoid cell damage, the amplitude of current passed through the cell has to be limited to the nano amperes.

As shown in Fig. 2.4, typically, a reference current (I_r) is generated from a lock in reference is injected in to an unknown impedance (Z_x) that produces the resulting voltage (V_0) with a modification of the signal phase and magnitude. The reference current and resulting voltage (V_0) can be expressed as follows:

$$I_r = A_{ri} \text{ Sin } (\omega t) \tag{2.6}$$

$$V_0 = A_0 \text{ Sin } (\omega_r t + \theta) \tag{2.7}$$

Where A_{ri} is the amplitude of the reference current, A_0 is the amplitude of the resulting voltage, ω_r is the frequency of the reference current. Θ is the phase difference between I_r and V_0. Thus complex impedance Z_x at frequency ω_r can be defined as

$$\overline{z_x(\omega_r)} = \left|\frac{A_0}{Ari}\right| \angle\theta \tag{2.8}$$

In order to solve Eq. (2.9) amplitude A_0 and θ has to be measured. The lock in system detects the resulting voltage and multiplies it with the in phase (0^o) and the quadrature (90^o) Components of the lock in reference respectively. The lock in reference can be expressed as:

$$V_r = A_r \text{ Sin } (\omega_r t) \tag{2.9}$$

Hence the outputs of the two multipliers (V_{psd1} and V_{psd2}) are simply product of the two sine waves.

$$\begin{aligned} V_{psd1} &= A_0 A_r \sin(\omega_r t + \theta) \sin(\omega_r t) \\ &= \frac{1}{2} A_0 A_r \cos(\theta) - \frac{1}{2} A_0 A_r \cos(2\omega_r t + \theta) \end{aligned} \tag{2.10}$$

$$\begin{aligned} V_{psd2} &= A_0 A_r \sin(\omega_r t + \theta) \sin(\omega_r t + 90^o) \\ &= \frac{1}{2} A_0 A_r \sin(\theta) + \frac{1}{2} A_0 A_r \sin(2\omega_r t + \theta) \end{aligned} \tag{2.11}$$

The AC components of the Eq. (2.11) and (2.12) are filtered by the low pass filter to estimate the DC values. Hence, the two DC filtered signals obtained are as follows,

$$V_{flr1} = \frac{1}{2} A_0 A_r \cos(\theta) \tag{2.12}$$

$$V_{flr2} = \frac{1}{2} A_0 A_r \sin(\theta) \tag{2.13}$$

If A_r equals 2, the amplitude A_0 and phase difference θ can be calculated from Eq. (2.13) and (2.14) as follows:

$$A_0 = \sqrt{{V_{flr1}}^2 + {V_{flr2}}^2} \tag{2.14}$$

$$\Theta = \tan^{-1}\left(\frac{V_{flr2}}{V_{flr1}}\right) \tag{2.15}$$

Therefore impedance Z_x can be calculated.

Conventionally, the lock-in technique demands sophisticated analog circuits to realize the phase-sensitive detection and filtering [21][22]. Most of the previous analog-based commercial lock-in instruments only achieved a narrow measurement bandwidth range from DC to few hundred kHz with limited dynamic range. The major challenges of analog lock-in technique are bandwidth, output offsets, harmonic rejection and limited dynamic reservation. With the rapid development of the digital technology, scientists have been trying to find a digital method to overcome the deficiencies of the analog lock-in technique. Modern digital lock-in technique can be used to remove large amounts of the analog circuitry by performing signal processing digitally[23][24]. This capability provides many additional benefits including increased reliability, accuracy and flexibility [25]. The SNR of the lock-in amplifier is high enough to detect tiny changes of the impedance of a single cell. Therefore many lock-in instruments were applied in cellular impedance-based experiments recently [26]-[27]. However, the major deficiency of the lock-in method is the measurement speed determined by the time constant of the low pass filters (whatever in analog parts or digital algorithm) . In order to derive the DC component from the filtered signal, the **Root Mean Square** (RMS) voltage calibration has to be performed [28] which takes more time to process. Hence the lock-in amplifier cannot meet the time requirements of real-time biological impedance measurements, especially in impedance-based tomography applications.

2.4.2 Impedance Analyzers

Impedance analyzers are useful instruments for testing various components and materials in different conditions. It measures impedance at spot frequencies or within a range of frequencies. The auto balancing bridge method is commonly used in commercial impedance analyzers. The general principle diagram of the auto balancing bridge method

is shown in Fig. 2.5. The two arms of this bridge are formed by two symmetrical voltage generators and by the impedances to be compared.

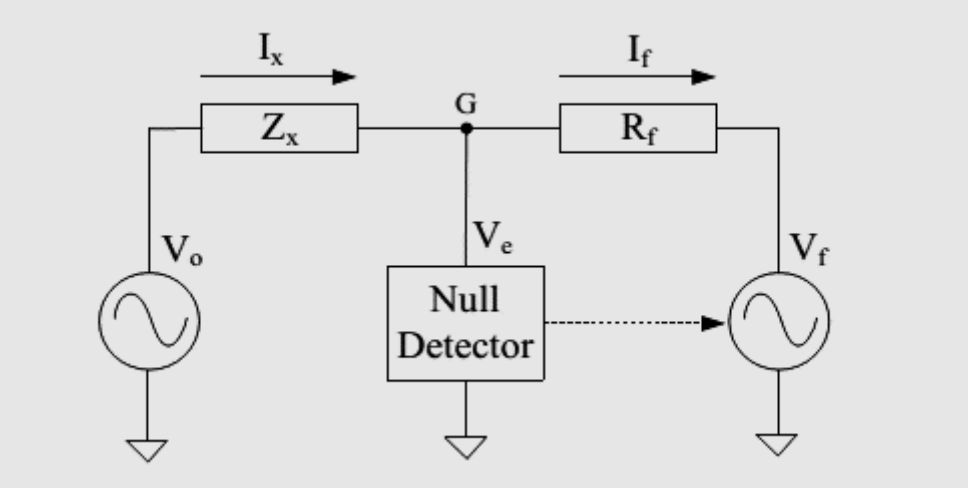


Fig. 2.5: Principal Diagram of Auto Balancing Bridge [29]

In this bridge, V_0 and V_f are two sinusoidal voltage sources, with the same frequency ω_0, but with different amplitudes and phase shifts. The reference voltage source V_0 has a constant amplitude A_0 and zero phase shift, whereas V_f has a variable amplitude A_f and the phase shift φ. The V_0 and V_f can be expressed as follows.

$$V_0=A_0 \sin(\omega_0 t) \tag{2.16}$$

$$V_f = A_f \sin(\omega_0 t + \varphi) \tag{2.17}$$

Where A_f and φ can be controlled to balance the bridge. The other two unknown elements of the bridge are the unknown impedance Z_x, and the reference impedance Z_f. For, Simplicity Z_f is chosen to be resistive i.e. $Z_f = R_f$. When the current flowing through the reference resistor R_f is not balanced with the one through the object under test Z_x, an imbalance current $(I_x - I_f)$ will cause an imbalance voltage V_e at the terminal G. The null detector detects this voltage and adjusts both the magnitude and phase of the V_f to nullify the imbalance voltage on the terminal G. In an ideal situation, when the bridge is balanced ($V_e = 0$), the current I_f will be equal to the current I_x. The following Eq. (2.19) is derived.

$$\frac{V_0}{Z_x} = \frac{V_f}{R_f} \tag{2.18}$$

The unknown impedance at the frequency ω_0 is given by

$$Z_x = \frac{V_o}{V_f} R_f = R_f \frac{A_o}{A_f} \angle \varphi \tag{2.19}$$

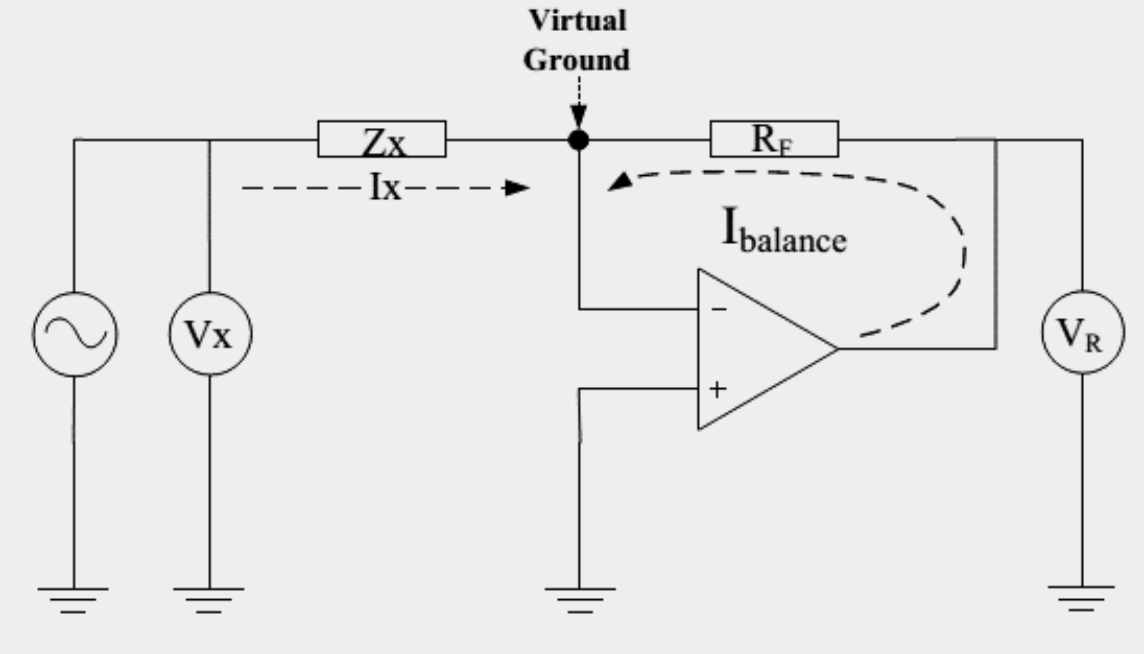


Fig. 2.6: The Simple Negative Feedback Operational Amplifier Architecture [29]

Normally, a negative feedback operational amplifier architecture is suitable for its I-V converter in low frequency range typically below 100 KHz. The general circuit is shown in Fig. 2.6. The current flowing through the measured sample (Z_x), due to operation amplifier's "virtual short" effect. The negative pin of the amplifier always maintains the same potential with the positive input pin. Consequently, when the positive input pin connected to ground, the potential on the negative pin is zero volts because the current through R_f balances the one flowing through the Z_x. The complex impedance of the Z_x can be measured with a measurement circuit consisting of the two voltmeters (V_x and V_r). The voltmeter V_x measures the applied voltage on the object and voltmeter V_r measures the applied voltage on the R_f and then calculated balance current which equals resulting current.

In practice, the performances of the operational amplifier (offset voltage, bandwidth, gain, *etc.*) will decrease versus the increasing of operating frequencies. At higher frequency, the auto-balance function normally realized by more complex circuit including null detector, phase detector, vector modulator, *etc.* as shown in Fig. 2.7.

When an unbalanced current is detected by the null detector, the phase detectors in the next stage separate the current into quadrature vector components. The phase detector output

signals go through loop filters and are applied to the vector modulator to drive the 0° /-90° component signals. The 0° /-90° component signals are compounded and the resultant signal is fed back through a range resistor (R_r) to cancel the current flowing through the test object. Even if the balancing control loop has phase errors, the unbalance current component, due to the phase errors, is also detected and fed back to cancel the error in the range resistor current [30].

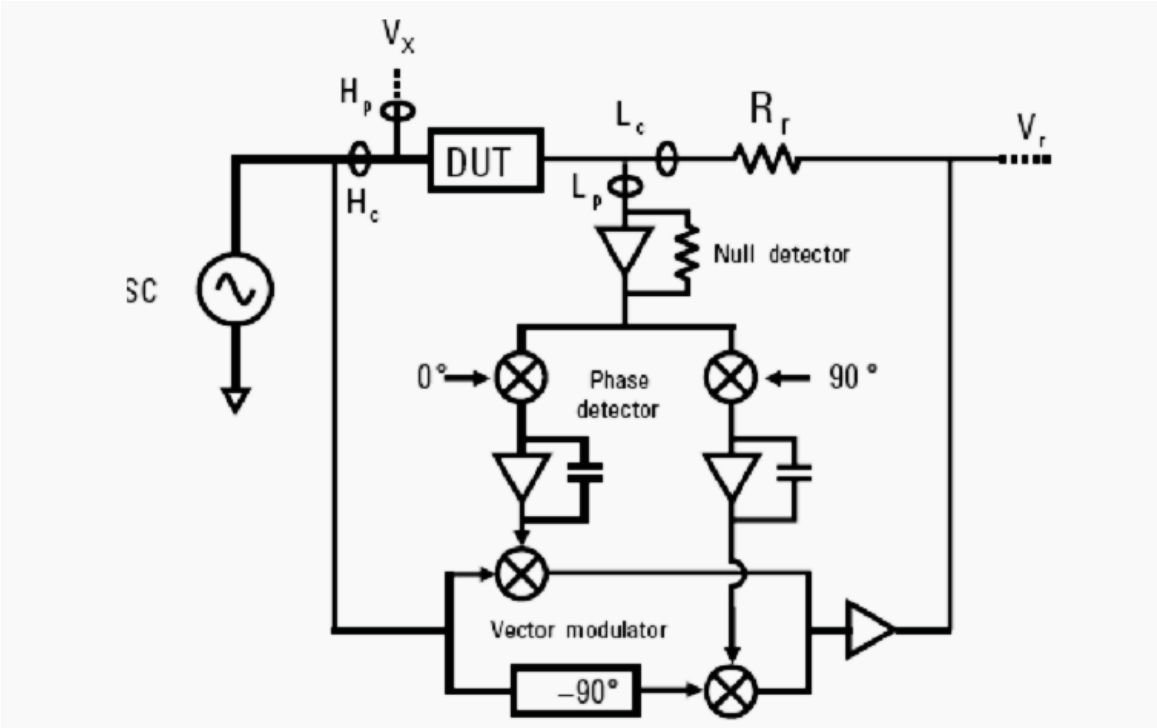


Fig. 2.7: High Frequency Auto Balancing Bridge Circuit [30]

This architecture is widely applied in most commercial impedance analyzers (eg. Solartron 1260A, Agilent 4294A, HIOKI 3532 *etc.*). It can be used in a broad frequency range (covering millihertz to hundreds of megahertz) with high measurement accuracy and a wide impedance measurement range. However, there are some deficiencies in this method:

1. It is difficult to design an analog circuit for obtaining reference quadrature signals with the rigid amplitude and phase balances. Any imbalance between the pair of quadrature signals leads to the deviation of the decomposed signal.

2. The harmonic frequency of the reference signal will affect the detection accuracy.

3. The analog circuit should feature high linearity to maintain the accuracy in a wide frequency range.

4. The performance of analog circuit will be degraded by temperature drift and device degradation.

In high frequency applications (beyond 1 MHz), this method shows better bandwidth performance than other solutions. However, as a tradeoff for its high accuracy, the slow measurement speed, sophisticated analog parts, bulky volume and high cost restrict its convenience in some cellular applications such like cell-based biosensor, multi-channel drug screening and large scale cell culture. Moreover, as a rule of thumb, more analogue components in the circuitry introduce more instability issues, and the performances of the analogue circuits (such as linearity, bandwidth, noise, *etc.*) are easily influenced by noise, temperature drift and device degradation [29].

2.4.3 Electrical Impedance Tomography Technology

Electrical **I**mpedance **T**omography (EIT) is a developing medical imaging technology that is calling the attention of the researchers due to its low-cost, wealth of information and non-invasive nature[31][32]. EIT technique normally applied to display the spatial distribution of the conductivity distribution inside a human body[33][34][35].

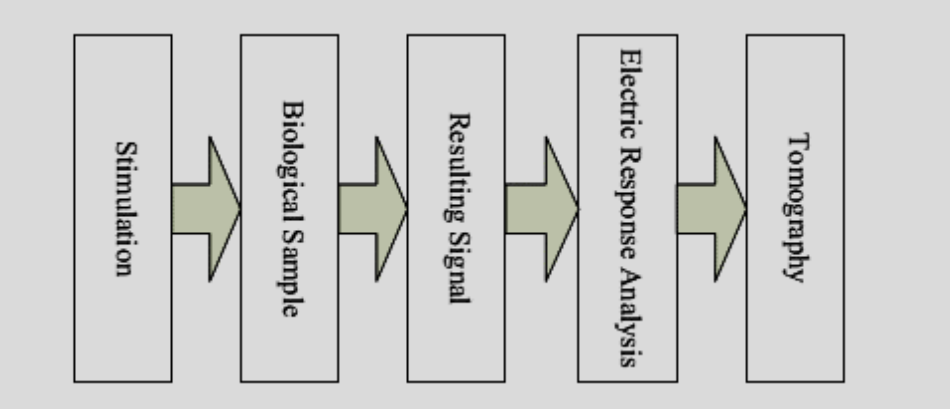


Fig. 2.8: Work Flow of EIT [29]

In an EIT system, an excitation is applied to electrodes on the body surface, cause an electromagnetic field appearing within the volume. The resulting electrical potentials are measured and used to calculate the impedance distribution between electrodes[36][37]. Finally, an image reconstruction process is applied to display this distribution of the interior of a body for medical use. Simplified Work flow of EIT is shown in Fig. 2.8. The advantages in portability, low cost and safety suggests that the EIT technique becomes a novel imaging solution [38].

A summary of recent impedance based setups can be found in the Appendix A.

2.5 Applications of the Bioimpedance Analysis

From the above discussion it is clear that electrical bio-impedance carries information about the physiological performance of living tissue. Bio-impedance based methods have obtained a recognized position among the clinical methods of non-invasive diagnosis of cardiovascular system. Now-a-days Bioimpedance methods have already replaced the EMG based diagnosis systems because of its accuracy and good performance. Bio-impedance is also an important measurement for iontophoretic drug delivery, non-invasive method for penetration of ionized drug through skin. The above all are in-vivo applications of bio-impedance. There are also lots of applications of bio-impedance method for in-vitro analysis[39]. For more clinical applications refer Appendix B.

3. LOCK IN AMPLIFIER: PROPOSED DESIGN

In this chapter, in starting traditional lock-in amplifier circuit is demonstrated block wise. Introduction to each block and block used to simulate it on Xilinx System Generator is given in brief. To design Lock-In amplifier for bioimpedance measurement and simulate it on Spartan 3E kit and Xilinx System Generator, Circuit was modified as per the requirement and limitation of Spartan 3E kit. Based on the limitation and constraints of technique and maximum allowable current that can be passed through body, range of input and output for circuit has been decided.

3.1 Important Parameters

The following parameters have been incorporated for design purpose, which are applicable for general applications in bioimpedance measurements, voltage ranges in millivolts, input operating current range: AC 100 μA to 5 mA and DC few micro ampere and frequency ranges from 1 kHz to several MHz are used. Taking in account these basic constraints, following parameters have been set as basis for our design:

- Input operating frequency: 1 kHz
- Output Voltage Signal Range: 0.1 to 1 $V_{(p-p)}$
- Filter Order: 4
- Noise Rejection: 40-50 dBm

3.2 Basic Circuit and Analysis

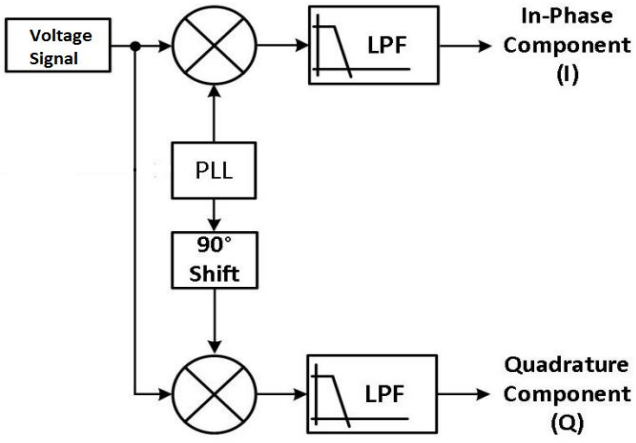


Fig. 3.1: Design Circuit of Lock-In Amplifier [5]

The Fig. 3.1 shows a generalized block diagram of the demodulator circuit to be implemented. There is an input signal given to the two multipliers, and a reference signal is given to another input to other multiplier from Digital Phase Lock Loop normally and to other one with 90^{o} phase shift of Digital Phase Lock Loop. The signal is then passed through a Low Pass Filter and we get the required I and Q component as our output. Every block of DPLL, Multiplier LPF are described in following sections.

3.2.1 Digital Phase Lock Loop (DPLL)

The techniques that are being controlled by **P**hase **L**ock **L**oop (PLL) have been proposed since 1970s. Fig. 3.2 shows general block diagram for all kinds of available PLL. In addition, proof regarding their highly accurate speed control has been provided. When digital signals have to be synchronized, Digital PLL is not a new field. In a PLL, often the output of Digital Phase Detector is passed through an analog filter, to provide a controlled analog signal to **V**oltage **C**ontrolled **O**scillator (VCO) and these are called **C**lassical **D**igital **PLL**s (CDPLLs) [40].

Further, new class of PLL has emerged called the **A**ll-**D**igital **P**LL (ADPLL) which consists of a digital phase detector, a digital filter and a numerically controlled oscillator. The system consists of exclusively logical devices and the signals within the system are also digital signals [40].

The ADPLL has the advantage of using only digital circuits, getting away from the problems that usually accompany analog circuits: parts spread, parasitic capacitors, temperature drift and aging. Another advantage of the ADPLL is the fact that it can be implemented by using reconfigurable devices, making the testing and prototyping very easy [40].

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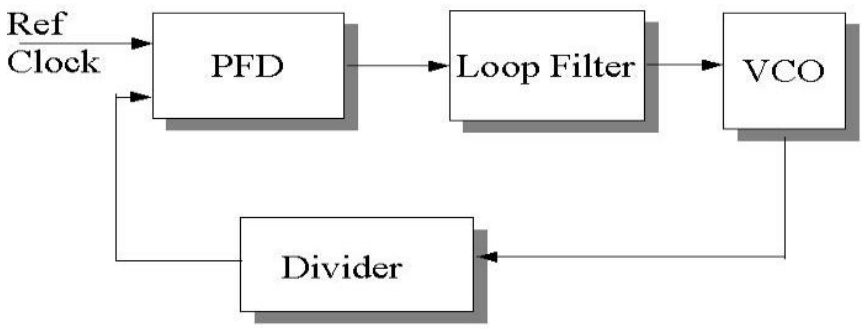


Fig. 3.2: General PLL Block Diagram [41]

A method for designing an ADPLL for speed control is presented. The details of the original circuitry acquiring the phase error are emphasized [40].

A. Designing of Phase Frequency Detector (PFD)

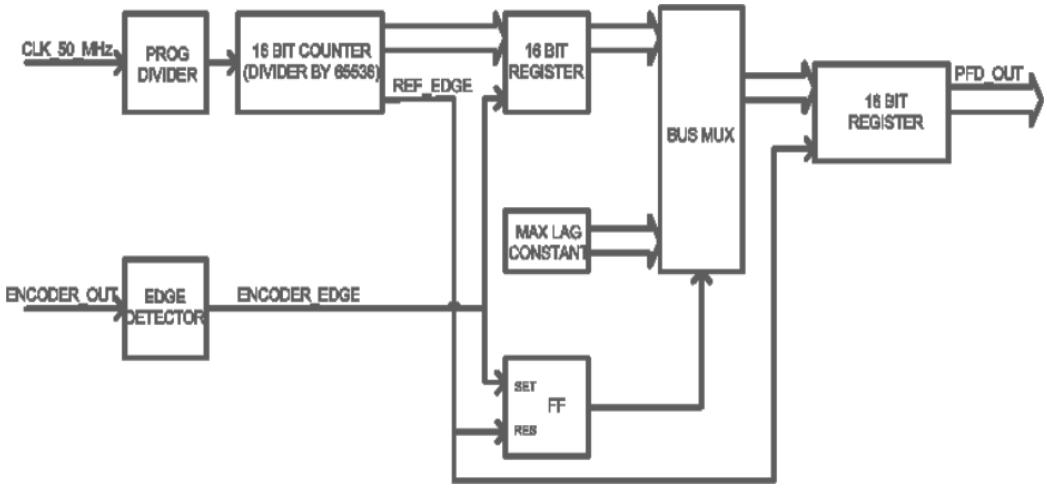


Fig. 3.3: Block Diagram of Phase Frequency Detector (PFD) [40]

Block diagram of PFD is given in Fig. 3.3 whose each and every element function is described. Looking at the second stage, the divided frequency signal is the reference signal. The second divider is used also to measure the phase difference: the encoder output rising edge will save the contents of the counter into a register. In this way, the higher the phase difference between the reference and the encoder signal, the higher will be the value saved from the counter [40].

The 16 bit number can be seen as a signed number, this way providing information about the direction of the phase error when the rising edge of the encoder output comes in the first half - period of the reference signal, the number saved from the counter will be smaller than 8000 H, which means the MSB will be 0. This corresponds to a “lag” between the controlled signal and the reference signal. The magnitude of the “lag” is given by the rest of the bits [40].

B. Loop Filter

In filter if output is denoted by u[k] and the input as e[k] then a relation to compute u[k] can be given by Eq. (3.1)- (3.3) [40].

$$\frac{U(z)}{E(z)} = \frac{K_p E(z) + (K_t T - K_p) z^{-1}}{1 - z^{-1}} \tag{3.1}$$

$$\Rightarrow \quad U(z) - z^{-1}U(z) = K_p E(z) + \left(K_t T - K_p\right) z^{-1} E(z) \tag{3.2}$$

$$\Rightarrow \quad n[k] = n[k-1] + K_p \varepsilon[k] + \left(K_t T + K_p\right) \varepsilon[k-1] \tag{3.3}$$

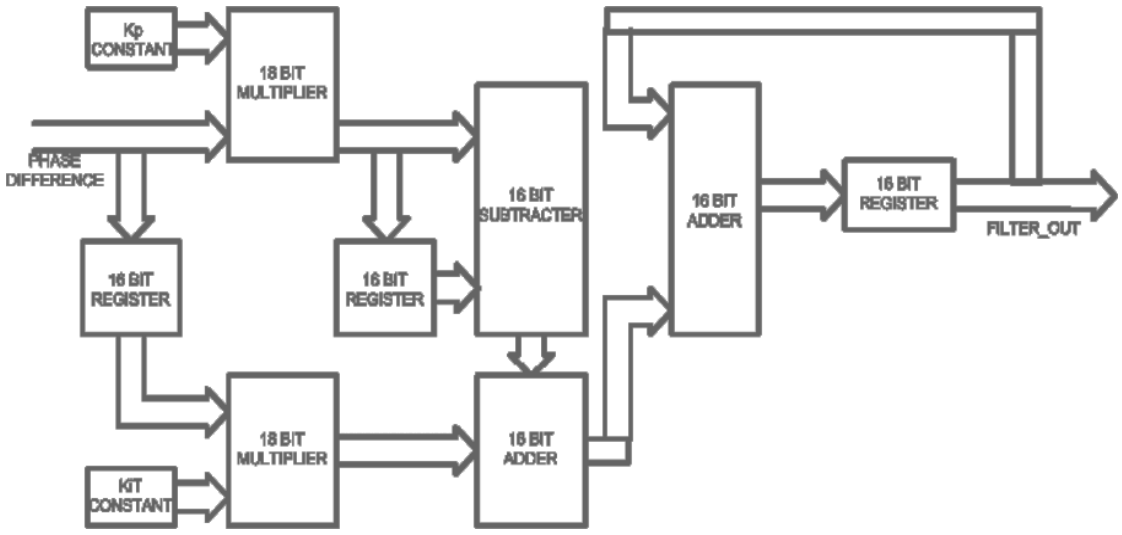


Fig. 3.4: Block Diagram of Loop Filter [40]

The filter to be designed has to be a digital filter as the phase error has been converted to a digital number as shown in Fig. 3.4. This implementation separates the proportional and integral gain paths and allows easy experimentation with different gain factors. It consumes more resources of the FPGA, but it is better for prototyping and experiments. Taking into account that the multiplication factors are less than one and the PFD output is an integer value, integer multiplication is applied after scaling down the values. The scaling is done by an appropriate number of right shifts. This scaling means the filter is effectively ignoring some of the bits of the error signal. This increases the stability of the system, at the expense of a slowly oscillating stationary regime: the error never gets effectively to zero [40].

3.2.2 Numerically Controlled Oscillator (NCO)

Numerically Controlled Oscillator also known as Direct Digital Synthesizer (NCO) is an important component in many Digital Communication Systems such as Digital Radio and Modems, Software Defined Radios, Digital Down/Up converters for Cellular and PCS base stations. A common method for digitally generating a complex or real valued sinusoid employs a Look-Up table based scheme. NCO is a technology of Frequency synthesis; It is developed the using third generation of Frequency synthesis technology. The technique is gaining popularity as a method of generating sinusoidal signals and modulated signals in digital systems[41],

A. Basic Principle of Numerically Controlled Oscillator

NCO is a technology to generate a frequency- and phase tunable output signal with a precision fixed-frequency clock. In time domain, the output frequency, f_{out} of NCO is a function of the system clock, f_{clk}. Without regard to the quantization error of NCO bit truncation, the ideal output of NCO can be given by Eq. (3.4) [42].

$$\boldsymbol{N_{out}(n) = \cos\left(\frac{2\pi f_{out} n}{f_{clk}} + \emptyset_o\right)(n = 1, 2, 3, 4 \ldots\ldots)} \quad (3.4)$$

Basically NCO consists of a Phase accumulator followed by a lookup table which contains pre-computed sine and cosine values. The f_{clk} is a high precision clock, used to synchronize the various components. The phase accumulator steps through and accesses each of the lookup table's memory address and outputs the phase (0-2π). The phase increment varies with the frequency turning words, Fr [41].

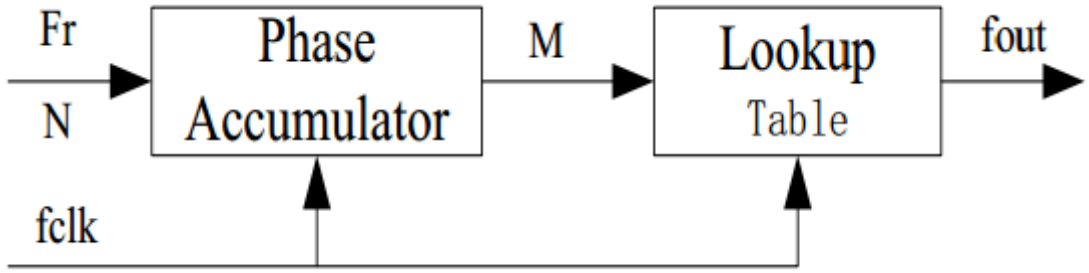


Fig. 3.5: Block Diagram of Loop Filter[41]

B. Xilinx System Generator Implementation of NCO

For implementation of NCO in Xilinx System generator is done through LogiCORE^{IP} DDS compiler core. It consists of a phase generator and a sine/cos lookup table.

C. Implementation of NCO using Xilinx LogiCOREIP DDS Compiler Core

A common method for digitally generating a complex or real valued sinusoid employs a lookup table scheme. The lookup table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the lookup table to the desired output waveform. A simple user interface accepts system-level parameters such as the desired output frequency and spur suppression of the generated waveforms[43].

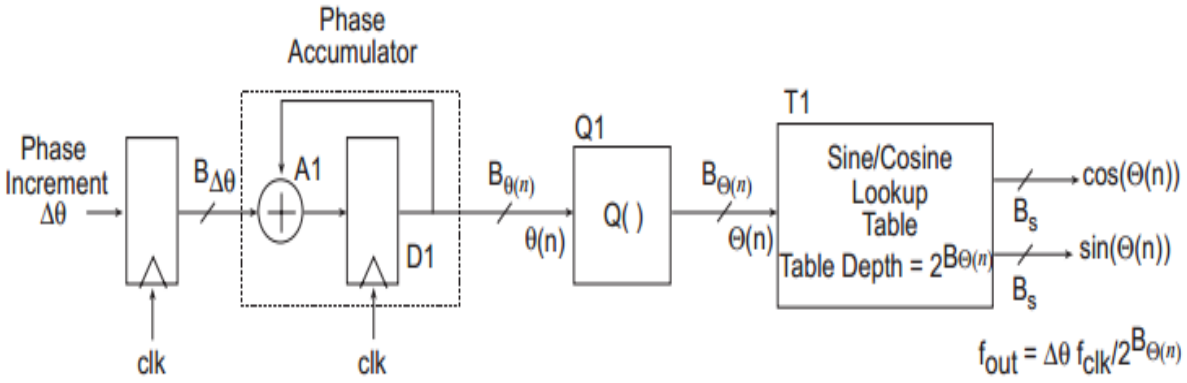


Fig. 3.6: Simplified View of DDS Core[43]

The integrator (components D1 and A1) computes a phase slope that is mapped to a sinusoid (possibly complex) by the lookup table T1. The quantizer Q1, which is simply a slicer, accepts the high-precision phase angle and generates a lower precision representation of the angle denoted as in the figure. This value is presented to the address port of a lookup table that performs the mapping from phase-space to time. The fidelity of a signal formed by recalling samples of a sinusoid from a lookup table is affected by both the phase and amplitude quantization of the process. The depth and width of the lookup table affect the signal's phase angle resolution and the signal's amplitude resolution [43].

The output frequency of DDS can be given Eq. (3.5) as [43]

$$\boldsymbol{f_{out}} = \frac{\boldsymbol{f_{clk}\Delta\theta}}{\boldsymbol{2^{B_{\theta(n)}}}} \tag{3.5}$$

Where F_{clk} is the system clock. $\Delta\Theta$ is the phase increment and $B_{\Theta(n)}$ is the number of bits in the phase increment value.

The frequency resolution of DDS can be given Eq. (3.5) as [43]

$$\boldsymbol{\Delta f} = \frac{\boldsymbol{f_{clk}}}{\boldsymbol{2^{B_{\theta(n)}}}} \tag{3.5}$$

The phase increment of DDS can be given Eq. (3.6) as [43]

$$\boldsymbol{\Delta\theta} = \frac{\boldsymbol{2^{B_{\theta(n)}} f_{out}}}{\boldsymbol{f_{clk}}} \tag{3.6}$$

Spurious Free Dynamic Range of the NCO for no noise shaping is given by Eq. (3.7) and for Taylor series noise shaping is given by Eq. (3.8) [43]

$$SFDR = 6 * Output\ Width \tag{3.7}$$

$$SFDR = (6 - 1) * Output\ Width \tag{3.8}$$

3.2.2 Multiplier

Multiplication is an essential arithmetic operation. Initially ALU's adders were used to perform the multiplication. As the applications of Array multipliers were introduced the clock rates increased as well as timing constraints became more important parameters. Ever since then methods to implement multiplication are proposed which are more sophisticated. As known the use of multiplication operation in digital computing and digital electronics is very intense especially in the field of multimedia and digital signal processing (DSP) applications. There are mainly three stages to perform multiplication: The first stage mainly consists of generating the partial products which are generated through an array of AND gates; Second stage consist of reducing the partial products by the use of partial product reduction schemes; and finally the product is obtained by adding the partial products[44].

As shown in Fig. 3.7 the in-built multiplier blocks in Xilinx Block set system generator provides us readily available blocks for multipliers which can be used. It can be used in our circuits with variable bit length.

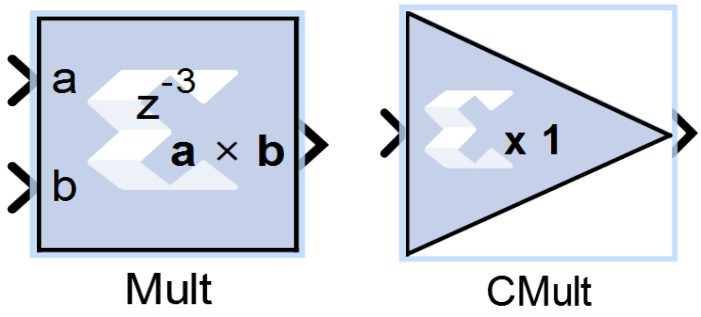


Fig. 3.7: Basic Xilinx Blocks of Multiplier in System Generator[44]

3.2.3 Low Pass Filters (LPF)

This section deals with designing a low pass filter with the aim to remove the higher frequency ($2*f_c$) components as well as noise after we demodulate our input modulated signal. LPF also helps to extract DC component. This DC component contains both phase as well as magnitude information of the signal to be measured. Since the processing is being done in digital domain we are going to implement a digital filter. There are two ways to implement a digital filter [45].

1) Infinite Impulse Response Filters (IIR filters)

An IIR filter is a LTI system that has infinite impulse response. Only causal IIR filters are physically realizable. The system output is [weighted by impulse response h (t)] a linear combination is input signals. Its equation can be described in Eq. (3.4) [45]: -

$$y(n) = \sum_{k=0}^{\infty} h(k)x(n-k) \tag{3.4}$$

Here we can see that the sum involved is a weighted sum of all past inputs and the present input. Basically it has infinite memory. IIR filters are less complex, easier to design and faster to compute. Also it has lower side lobes in stop band than FIR for same parameters. But a major drawback is that a physically realizable IIR filter cannot have linear phase response. In fact, while designing IIR filters we only focus on magnitude response and accept whatever phase response the particular method of designing gives us [45]. So, basically we have no control over phase response of IIR filters.

2) Finite Impulse Response Filters (FIR filters)

These filters have a finite impulse response i.e. its response is zero after a certain time interval. The system output is a weighted sum of only a finite number of past inputs and present input. Its equation can be described in Eq. (3.5) [45]

$$y(n) = \sum_{k=0}^{M-1} h(k)x(n-k) \tag{3.5}$$

FIR filters are more complex to implement and are slower to commute. But we can have a linear phase response from an FIR filter.

IIR filters lose their stability at higher orders but FIR filters are always stable even at higher orders. Besides they are particularly useful when exact linear phase response is required [46]. It is to be noted that we also require phase measurement for calculating Bioimpedance so phase response of the filters used are also important. But one of the major drawback of FIR filters is that they are more complex and hence difficult to implement than IIR filters. The general block diagram of an FIR filter is given in Fig. 3.8 [45].

It can be evaluated using multiply accumulate but it would require L multiply accumulate cycles to compute the next input. Thus, in a conventional multiply accumulate method with a limited number of multiply accumulate engines, as the filter length is increased, the system sample rate should decrease[46]. Basically we have to divide the system clock by n

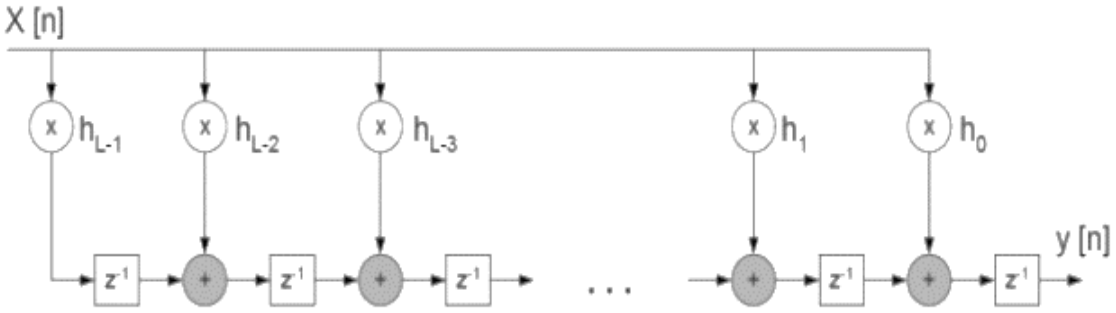


Fig. 3.8: Direct Form Implementation of FIR Filter [46]

times for n^{th} order low pass filter. This assumption is supported by ADA 2200 IC which uses divide by 8 decimation Low Pass Filter on board.

Another problem arises out of it. Let us assume that we are taking measurements at 1 MHz frequency. Su we will at least a sample rate of 4 MHz at the output of Low Pass Filter. Now it is a decimation by 8 filter so we have an input sampling rate of around 32 MHz (4*8). So, we require an ADC of at least 32 MHz sampling rate and a system clock of 32 MHz. Designing a circuit for such high frequencies adds to complexity of system.

For the Area efficient implementation of the low pass filter, Distributed Arithmetic architecture provides best possible solution.

3.2.4 Distributed Arithmetic Architecture

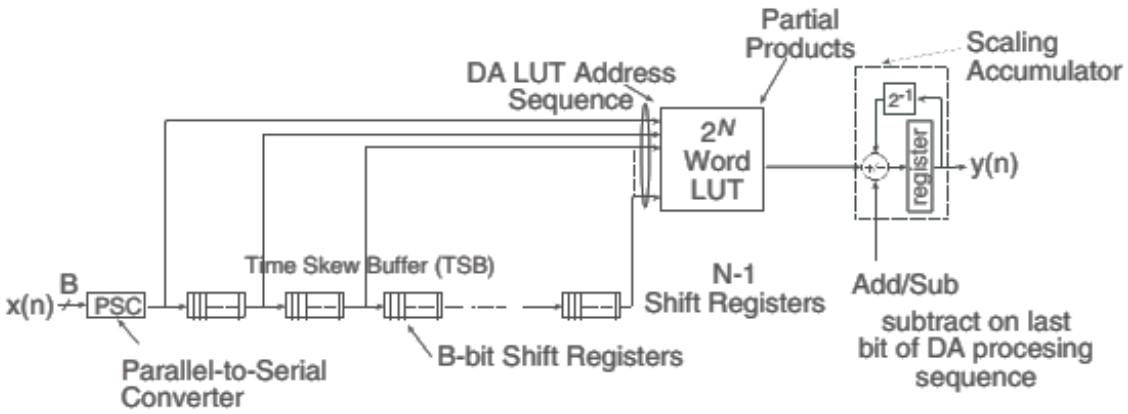


Fig. 3.9: Serial Distributed Arithmetic FIR Filter [47]

In their most obvious and direct form, DA-based computations are bit-serial in nature – serial distributed arithmetic (SDA) FIR. Extensions to the basic algorithm remove this

potential throughput limitation. The advantage of a distributed arithmetic approach is its efficiency of mechanization. The basic operations required are a sequence of table look-ups, additions, subtractions, and shifts of the input data sequence. All of these functions efficiently map to FPGAs. Input samples are presented to the input parallel-to-serial shift register (PSC) at the input signal sample rate. As the new sample is serialized, the bit-wide output is presented to a bit-serial shift register or time-skew buffer (TSB). The TSB stores the input sample history in a bit-serial format and is used in forming the required inner-product computation. The TSB is itself constructed using a cascade of shorter bit-serial shift registers. The nodes in the cascade connection of TSBs are used as address inputs to a look-up table. This LUT stores all possible partial products over the filter coefficient space.

3.2.5 Phase Shifter

Phase Shifter needs to be implemented to get a 90^o phase shifted version of cosine function. But there are a number of drawbacks of phase shifter

1) The phase shifter can be implemented only for a single frequency.
2) Phase shifter requires a designing another filter which is taxing in terms of hardware.
3) Moreover, many architectures are now designed in such a way that they give normal and 90 degree phase shifted output, which is the desired output, and hence it becomes illogical to use a separate phase shifter. In our case NCO already gives 90^o phase shift signal.

3.3 New Proposed Architecture of Lock-In Amplifier

There are various challenges that can be faced while designing a DPLL block.

1) DPLL is a feedback circuit which makes it difficult to implement.
2) DPLL can destabilize if the reference frequency gets out of range due to noise and other external factors.
3) The phase detector and loop detector are difficult to design.

Due to the above mentioned drawbacks a new architecture is being proposed in Fig 3.10. The advantages of the prosed circuit are as follows: -

1) Since the signal is generated in FPGA itself there is no issue of frequency and phase shifting of input signal

2) It removes the need of DPLL and 90^0 phase shifter in the circuit thereby reducing complexity.

NCO replaces 90^o phase shifter. The advantages of using NCO to generate both sine and cosine waves are

1) NCO gives perfect 90^o phase difference between sine wave and cosine wave which is difficult to implement using phase shifter.
2) NCO can give a 90^o phase shift for any frequency as opposed to a single frequency in phase shifter.
3) It is less taxing in terms on hardware as the same NCO architecture can be used to implement both signals.

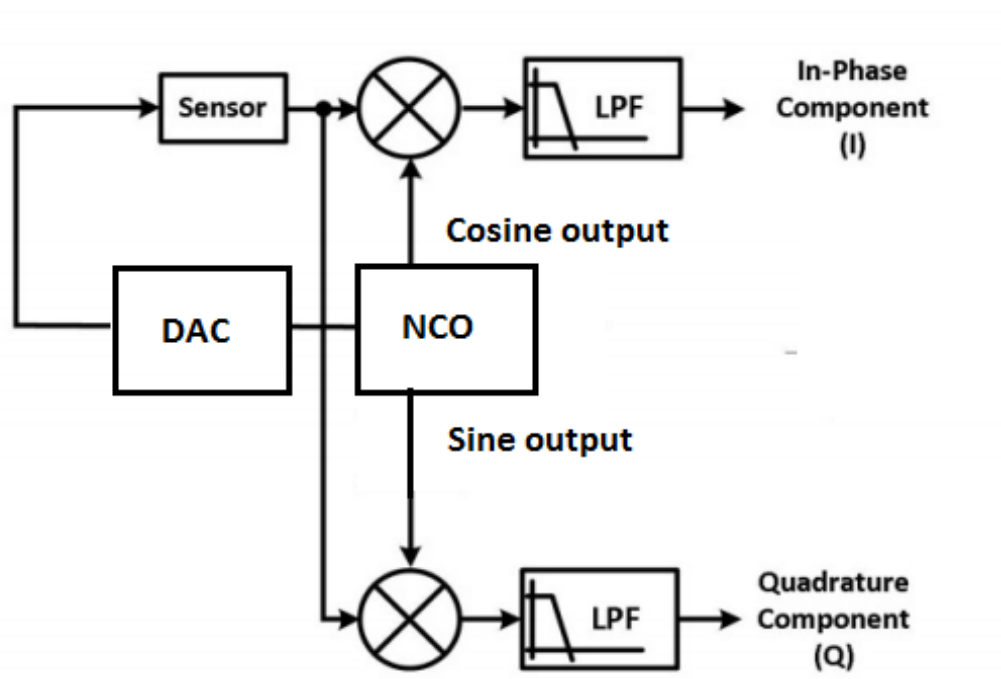


Fig. 3.10: New Purposed Architecture

Here, the output of NCO is converted to analog form through the use of Digital to Analog Convertor and given to sensor as excitation. Besides the same NCO is giving both sine and cosine output. The working of rest of the blocks are the same.

4. SIMULATION AND RESULTS

In this chapter, Work that has been done to implement whole circuit of Lock-In Amplifier for Bioimpedance measurement has been shown block wise and whole as a circuit.

Adopted methodology is as following:

1. The main purpose of block wise simulation, implementation and whole circuit simulation was to optimize area, complexity and speed. The parameters for which we are designing has been shown in Chapter 3.
2. For the simulation purpose, MATLAB - Simulink 2012b and ISE Design suite 14.3 was used.
3. Whole circuit, Firstly block wise on system generator was simulated and required important blocks were tested on the Spartan FPGA 3E kit.
4. Optimization of Block parameters were done with all constraints applied.
5. Selection of all parameters and method used was justified qualitatively and quantitatively. Data of which is included in tabular form in this chapter.
6. After Simulating and testing important blocks, all blocks were integrated on System Generator and results were collected.
7. Collected results were checked against the design specifications to see whether optimization goals were met or not.
8. Collected results were compared with the existing ADA 2200 IC.

4.1 Low Pass Filter

For the low pass filter simulation, Xilinx LogiCORE^{TM} FIR compiler v5.0 was used which provides a common interface for users to generate highly parameterizable area efficient high performance FIR filters utilizing either Multiply- Accumulate (MAC) or Distributed Arithmetic (DA) Architecture [47]. To simulate FIR Low Pass Filter, A Sine wave of variable frequency was generated and passed through FIR Compiler to check results. FDATool, Scope, Gateway In, Gateway Out, Convert and Constant as various supporting blocks from either Simulink built in library or Xilinx Block Set has been used. FIR compiler offer various pins to for signal processing. Pins that are of interests are only din (Data

Input), nd (New Data), dout (Data Out), rfd (Ready for Data) and rdy (Output Ready). So, only these pins were connected in simulation. FIR compiler also provides various parameters to implement filter on hardware such as Filter Architecture, Coefficient Structure, Coefficient type, Coefficient Width, Quantization, Optimization Goal and Filter Type. Experimentation has been done with different combinations of these parameter keeping in mind pros and cons of different value or method selected. To provide frequency parameters or coefficients, FDATool is used. Extensive work on FDATool has been done to get the best possible response as per the specifications required.

4.1.1 FDATool

With the help of FDATool, Various different order Low Pass Filters were realized using different methods such as Window, Equiripple, Maximally Flat etc. Various factors affecting magnitude response such as roll off factor, passband gain, attenuation at cut off frequency, ripple factor etc. were examined. Different hardware complexity related factors such as order, no. of adders, no. of multipliers filter length etc. were also checked against design constraints.

Following are the parameters used for the simulation and testing purposes.

- Direct Form FIR Filter Low pass Filter
- Order: 4
- Design Method: Blackman window
- Cutoff Freq.: 600 Hz
- Sampling Freq.: 4000 Hz
- Filter Co eff.: [0, 0.0811, 0.4189, 0.4189, 0.0811, 0] taken up to 4 points

Although comparison for all available options was done, Table 4.1 shows comparison of some magnitude responses with different methods and parameters that seemed most promising option. For the Selected Method and parameters following magnitude response was obtained.

Magnitude Response:

- Gain at 600 Hz: -2.1 dB
- Roll off Factor: -45 dB
- Filter Length/Taps: 6
- Number of Multipliers: 4
- Number of Adders: 3

Fig. 4.1 shows annotated magnitude response of selected order 4 Blackman FIR Filter.

Table 4.1: Comparison of Different order FIR low pass filter implementation

FIR Type	Other Specifications	Fs (Hz)	Fc (Hz)	Attenuation at 600 Hz	Passband Gain (dB)	Roll off Factor (dB/ Octave)	Order	Filter Structure	Filter length	No. of Adders	No. of Multipliers	Ripple max amplitude
Window	**Blackman**	4000	600	-1.47	-0.09	-7.6	3	Direct Form 1	5	2	3	-40
		4000	600	-2.1	0	-45	4	Direct Form 1	6	3	4	-40
		4000	600	-0.014	-2.8	-24	5	Direct Form 1	7	4	5	-45
	Kaiser	4000	600	-6.74	-0.44	-64	4	Direct Form 1	5	4	5	-21
		4000	600	-8.3	-0.02	-45	5	Direct Form 1	6	5	6	-27
		4000	600	-0.01	-8.1	-48	6	Direct Form 1	7	6	7	-27
Equiripple		4000	600	-3.5	2.376	-38	5	Direct Form 1	6	5	6	-27
		4000	600	-0.02	-3.17	-38	6	Direct Form 1	7	6	7	-10
		4000	600	-3.42	2.21	-61	4	Direct Form 1	5	4	5	-9.74
Least Square		4000	600	-4.2	-0.03	-18	6	Direct Form 1	7	6	7	-21
		4000	600	-4.73	1.2	-65	4	Direct Form 1	5	4	5	-24

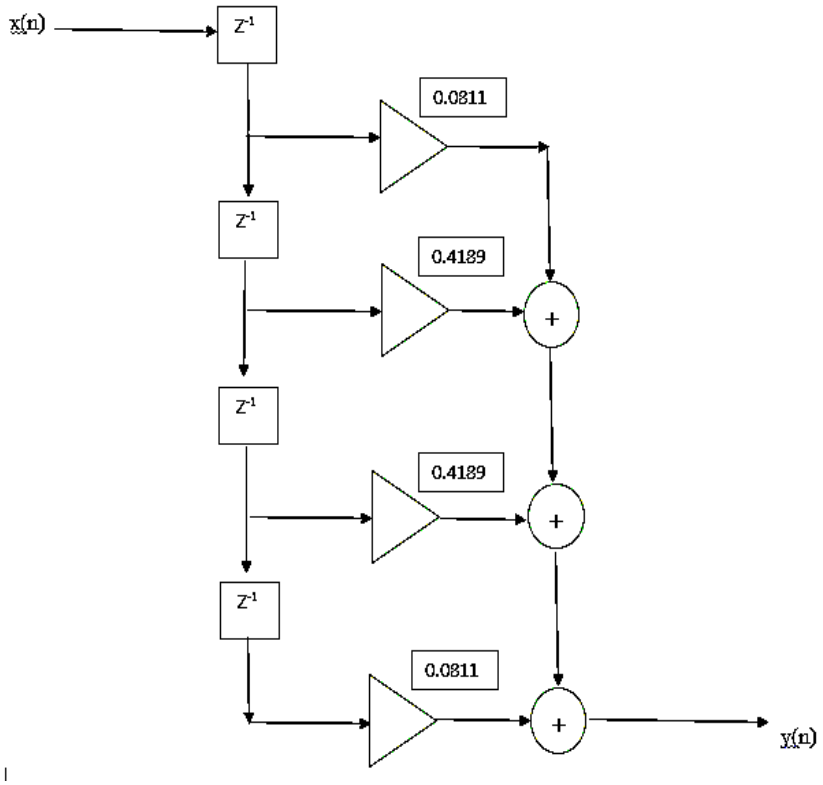


Fig. 4.1: Realization of Blackman Filter

4.1.2 Implementation of Blackman Filter using Xilinx LogiCORETM FIR compiler v5.0

As mentioned earlier, FIR compiler also provides various parameters and options to implement filter on hardware such as Filter Architecture, Coefficient Structure, Coefficient type, Coefficient Width, Quantization, Optimization Goal and Filter Type. For simulation purposes we can provide coefficients to FIR Filter Complier using FDATool token or directly feeding coefficients into it. In our experimentation, FDATool was used to provide coefficient vector. FIR compiler also provides, different filter type implementation such as single rate, multi rate, decimation, interpolation, poly phase etc. For obvious reasons, Single rate filter type has been chosen. Distributed Arithmetic was chosen as filter architecture, since it only needs one adder, shifter and memory to store coefficients. Coefficient structure was chosen to be inferred, so in case we need to change specifications, Filter compiler can change implementation style appropriately. In Quantization option of FIR compiler, Quantization only option was used since other option integer quantization can only be used with integer coefficients and Maximum Dynamic range scales all the

coefficients. In FIR compiler design optimization goal was set to be area. Our main motive of experimentation was to optimize coefficient width since it directly affects speed and area. After simulation for various different coefficient widths, coefficient width of 8 and fractional bits width 7 was chosen. Coefficient width was chosen such that it induced

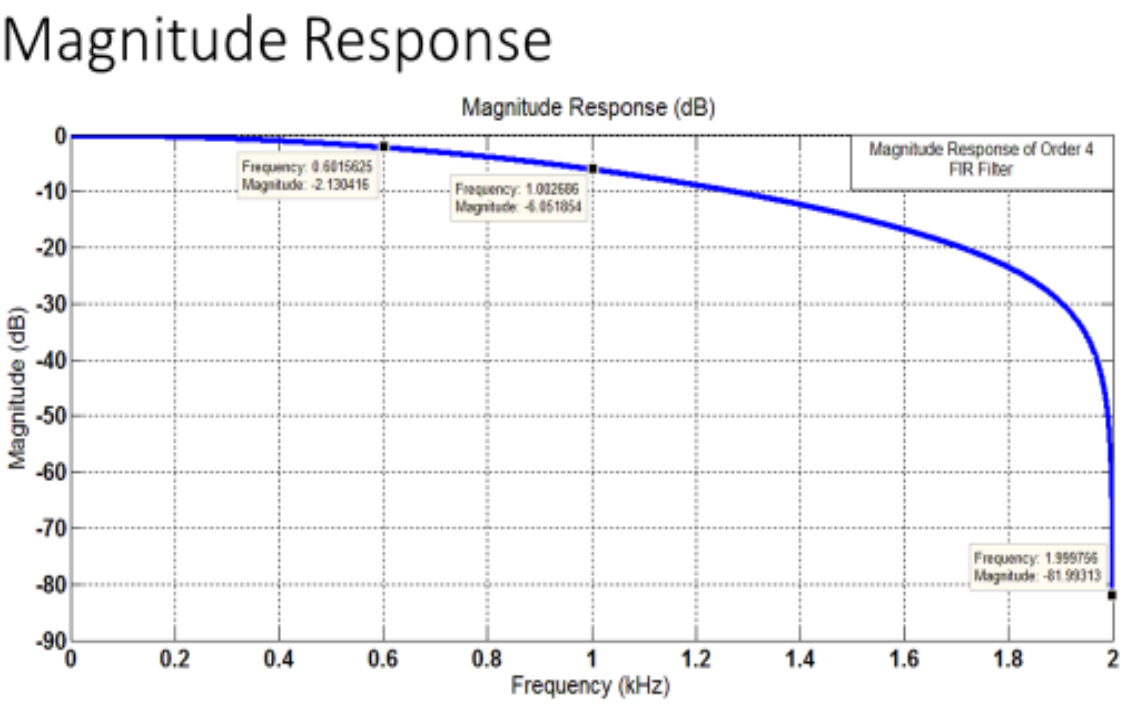


Fig. 4.2: Magnitude Response of order 4 Blackman FIR Filter

minimum quantization error. Fig. 4.3 shows all available parameters and selected options in FIR compiler as summary. Table 4.2 shows comparison for different coefficient widths and its effect on output.

Table 4.2: Coefficients and Bit Optimization of Blackman Filter

Coefficient Width	Fractional Bits	Maximum Amplitude of Noise (dB)	Signal Strength (dB)	DC (dB)
13	12	-42	12.6	-22.4
12	11	-41.8	12.6	-22.375
11	10	-41.91	12.6	-22.4
10	9	-43.2	12.6	-22.5
9	8	-41.9	12.6	-22.4

8	7	-41.9	12.6	-22.4
7	6	-41.9	12.6	-22.4
6	5	-39.69	12.4	-22.7
5	4	-41.3	12.68	-22.8
4	3	-42.88	13.5	-23.5
3	2	-43	12.33	-25.2

As we can see from the table that practically, coefficient width change from 13_12 to 3_2 doesn't show any effect on output spectrum, possibly because of noise introduced. But theoretically coefficient width below 8 shows significant quantization error which has been tabulated for comparison in Table 4.3. From practical and theoretical perspective 8_7 coefficient width provides best possible result under hardware constraints and lower quantization error. So, Coefficient width 8_7 has been chosen for simulation and testing purpose.

4.1.3 Implementation of FIR Low Pass Filter in System Generator

Fig. 4.4, shows complete design of FIR Low Pass Filter in System Generator. In which Constant provides nd pin (New Data) high (1) signal so, FIR compiler continuously accepts the data. Gateway In and Gateway Out define the input and output port of Xilinx Blockset

Table 4.3: Quantization of Number Represented in Fixed Point Format

Bit Number	**Range of Numbers**	**Quantization Step**	**Max Quantization Error**	**Number of Exact Decimal Points**
4	(-1, +1)	0.125	0.0625	1
8	(-1, +1)	0.0078125	0.0078125	2
16	(-1, +1)	3.0517578125*10-5	1.52587890625*10-5	4
32	(-1, +1)	4.6566128730774*10-10	2.3283064365387*10-10	9
64	(-1, +1)	1.0842021724855*10-19	5.4210108624275*10-20	19

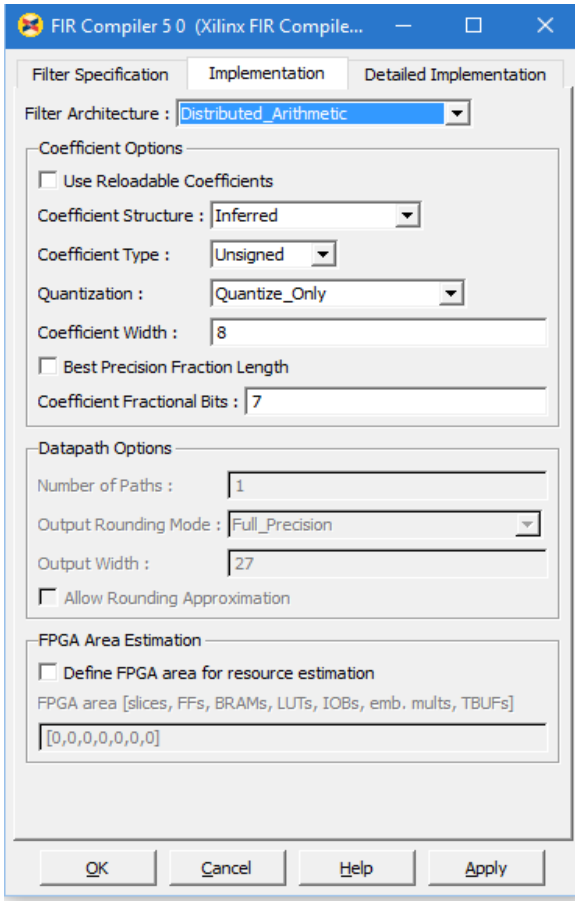


Fig. 4.3: FIR Compiler Implementation

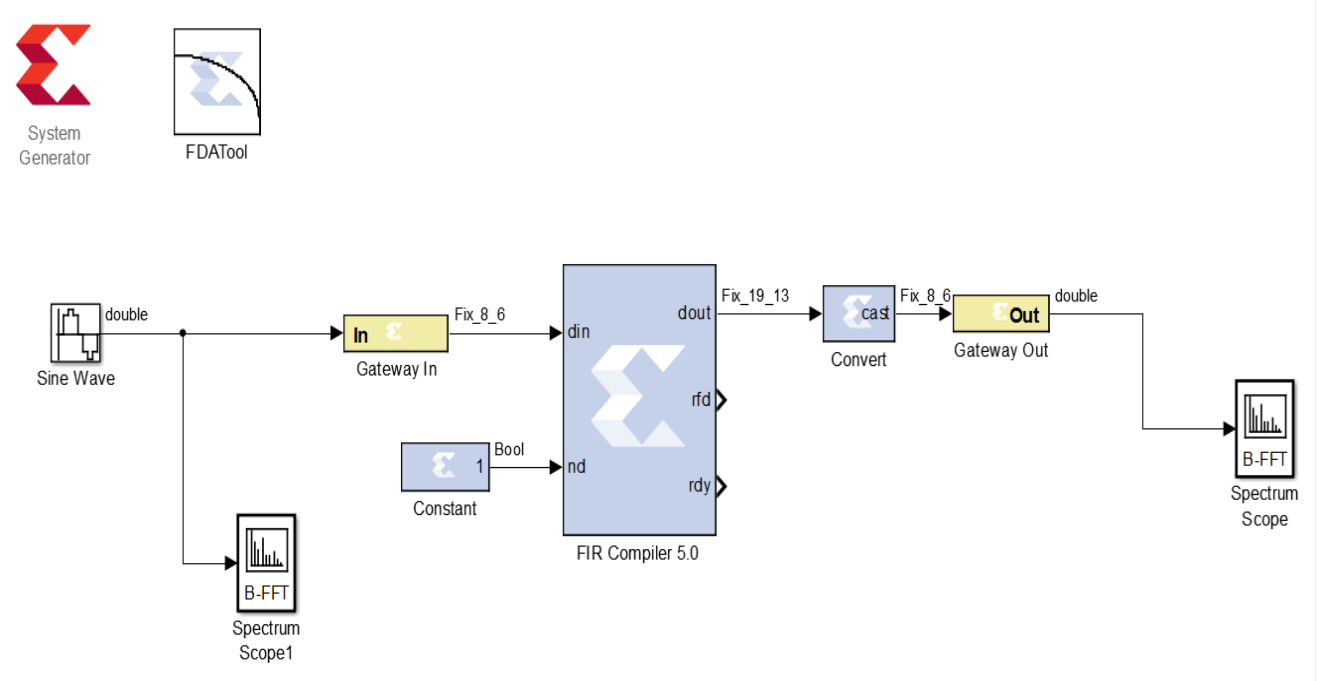


Fig. 4.4: System Generator Block Diagram of FIR Low pass Filter

Implemented on FPGA. Convert block does the data representation conversion for its

display on Scope. For testing purpose, output was checked for 500 Hz sine wave. Output is shown in Fig. 4.5.

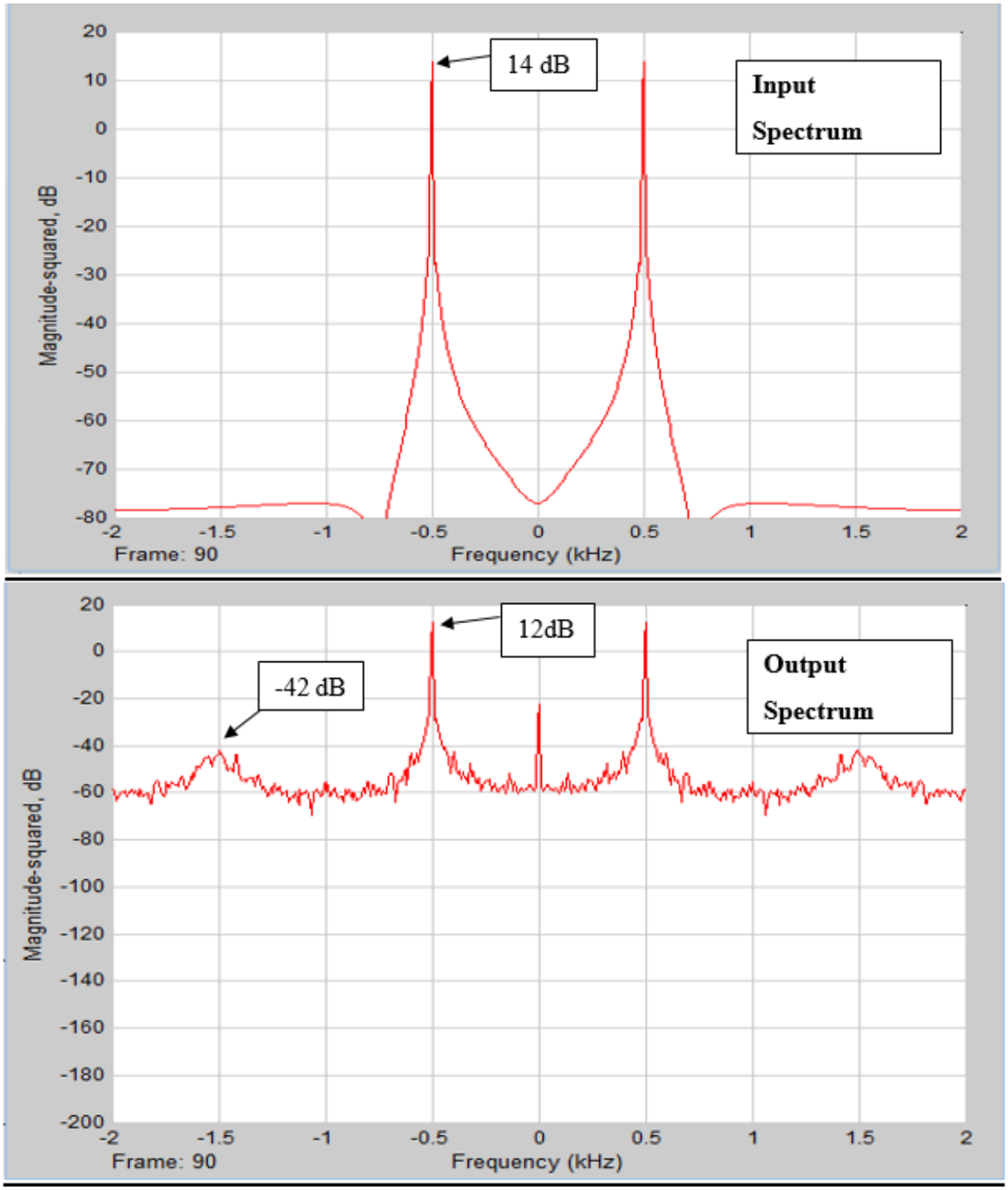


Fig. 4.5: Input Output Spectrum for 500 Hz Sine Wave

4.2 Implementation of NCO

Specifications of NCO:

- Output Frequency = 1 kHz (for testing purposes)
- Magnitude of output = $2V_{p\text{-}p}$
- Assumed System Clock = 10 MHz

- Frequency Resolution: - 0.001% Hz = 0.1 Hz (for 1 kHz)
- Spurious Free Dynamic Range = 50-66 dB

Different values of Frequency resolution corresponding to Phase width ($B_{\Theta(n)}$) for frequency output of 1 kHz at 10 MHz system clock is given in Table 4.4. Fig. 4.6 shows the system generator implementation of NCO. After analyzing different values of $B_{\Theta(n)}$, value of phase width was chosen to be of 24 bit. The phase increment value corresponding to this value is 1677.72, which corresponds to an input the value of 1*10-5.

Table 4.4: Frequency Resolution vs Phase Width

S.no	No of Bits ($B_{\Theta(n)}$)	Frequency resolution (Δf)
1	16	152.17
2	24	0.596
3	32	$5.59e^{-3}$

Output width is chosen to be 12 bit because

- The practical values of most low cost ADC is 12bit.
- It has an SFDR of 66db.

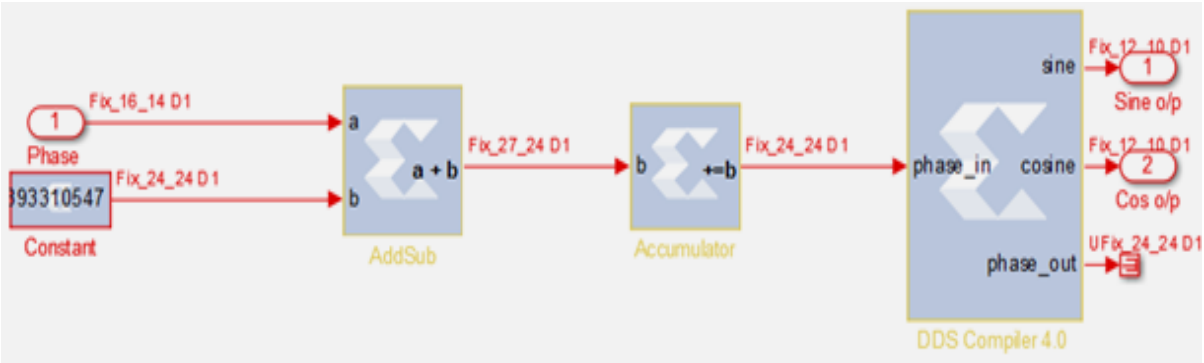


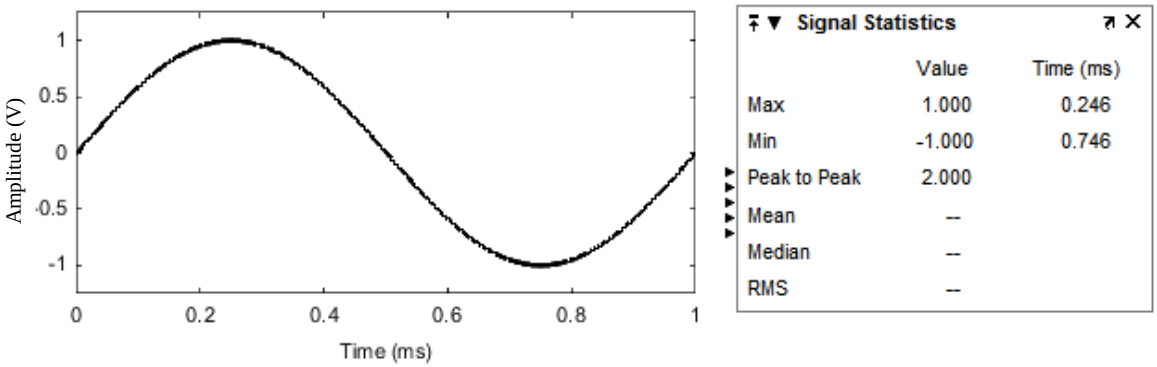
Fig. 4.6: System Generator Implementation of NCO

Port 1 is the input to the NCO which increases or decreases the frequency of output wave. It is put to zero when we require a 1 kHz frequency. The accumulator accumulates the phase and send the current phase of output sinusoid to the DDS compiler.

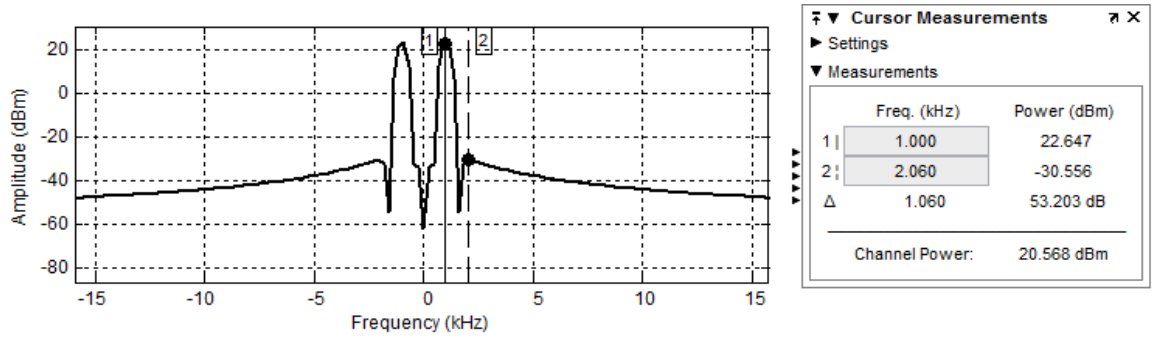
4.2.1 Simulation Results of NCO

The time domain and frequency domain analysis of NCO is given in Fig. 4.7 (a) and Fig. 4.7 (b) respectively. The results are as follows:

1) The amplitude of generated sine wave is $2V_{p-p}$.
2) The maximum amplitude is obtained at 0.246 ms and 0.746 ms which is very near to the expected value of 250 ms and 750 ms respectively. The output frequency corresponding to these values is 1.004 kHz.
3) SFDR of output sine wave is 53.203 dB which is within the range of 50-66 dB.



(a)



(b)

Fig. 4.7: (a) Time Domain Analysis of NCO (b) Frequency Spectrum of NCO

4.3 Complete Design and Simulation of Lock-In Amplifier

For the integration of different blocks having different data rates and sampling rates, Down sampler, Assert, Delay have been used and for the numerical computation on the input signal Add-Sub, Mult (Multiplier), Square Root blocks from the Xilinx Systems Block Library have been used. All these block have simple functionalities that do not need any explanation. Complete block diagram of system is shown in Fig. 4.8. For the simulation purpose, Sine wave of 1 kHz, 0.1 V $_{(p-p)}$ excitation signal was used with added noise of different frequency with amplitude of 0.01 V $_{(p-p)}$ to check the reliability of the circuit. Input- Output Waveforms are shown in Fig. 4.9 to 4.15.

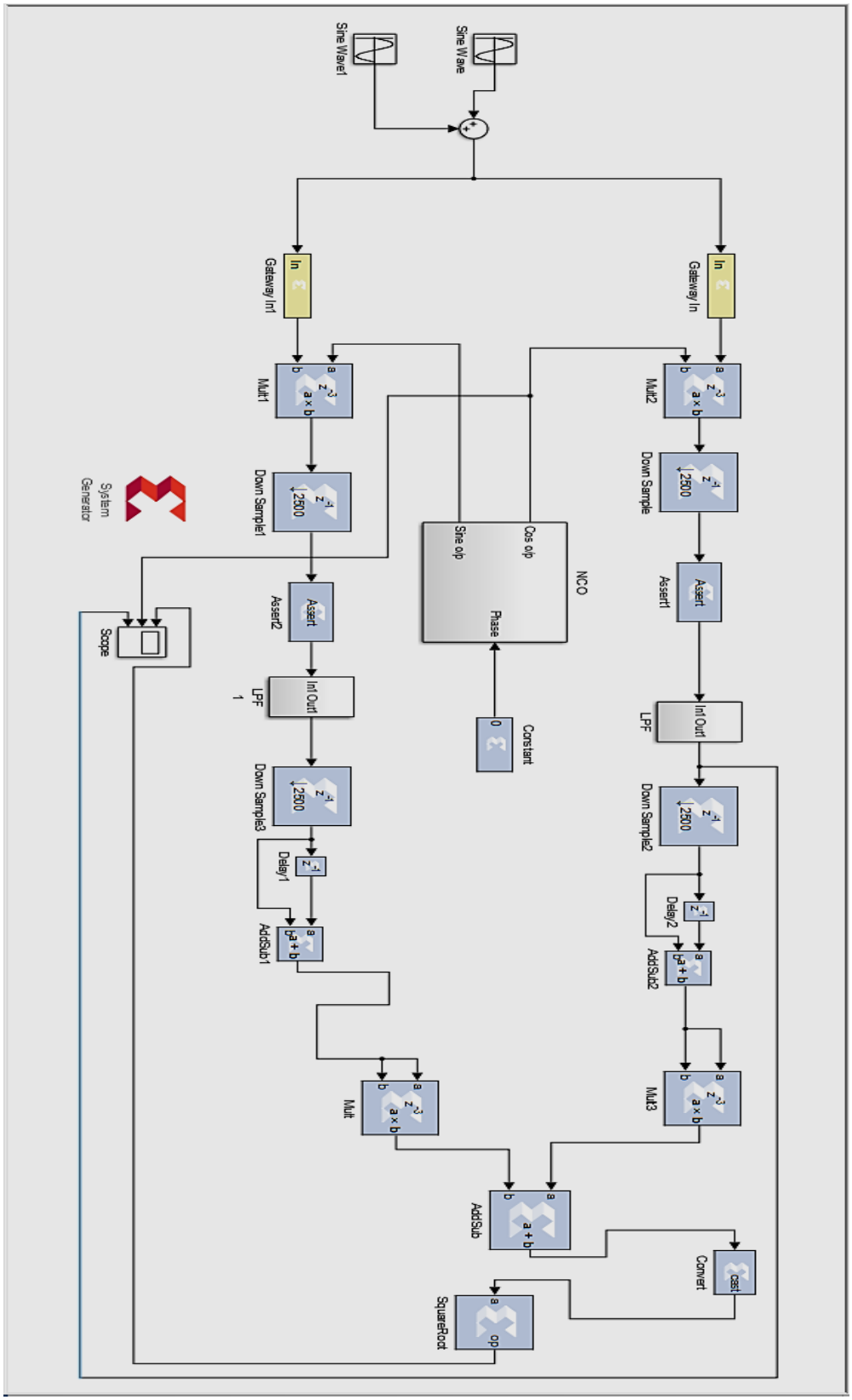


Fig. 4.8: System Generator Implementation of Lock-In Amplifier

It has been observed from MATLAB- Simulink and System Generator simulations that magnitude values of output signals ($\sqrt{I^2 + Q^2}$) are fairly DC for any input signal frequency above 2 kHz which as can be observed from Fig. 4.14 and 4.15. 2 kHz is the stopband end frequency.

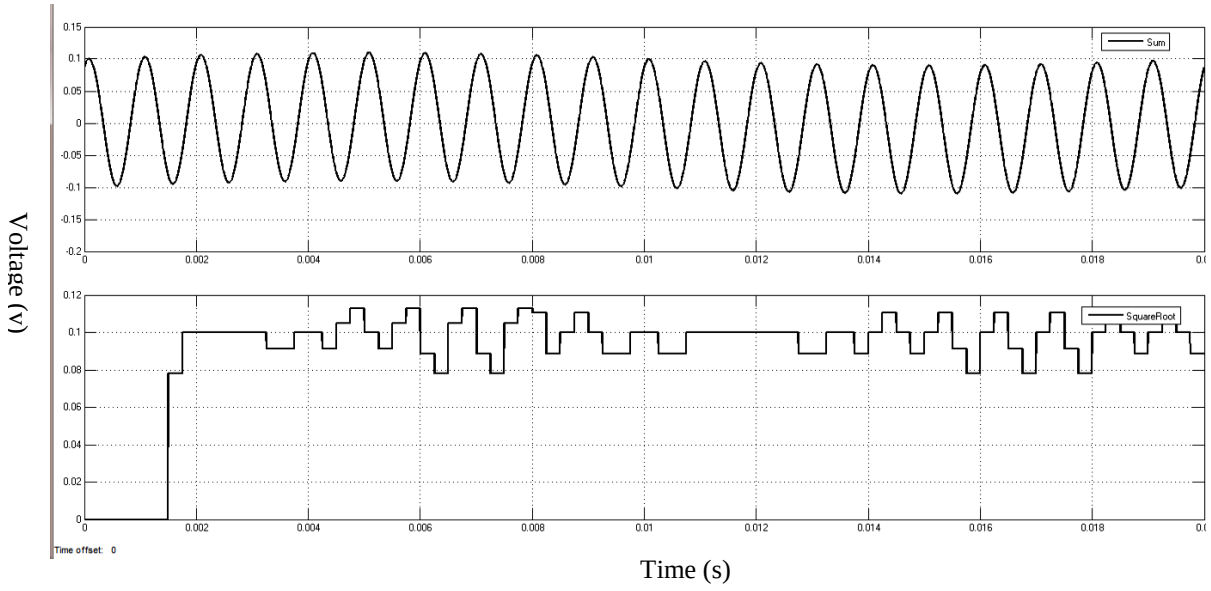


Fig. 4.9:Input and output Waveforms of Complete Design for Input Signal Frequency 1 kHz and Noise Frequency 50 Hz

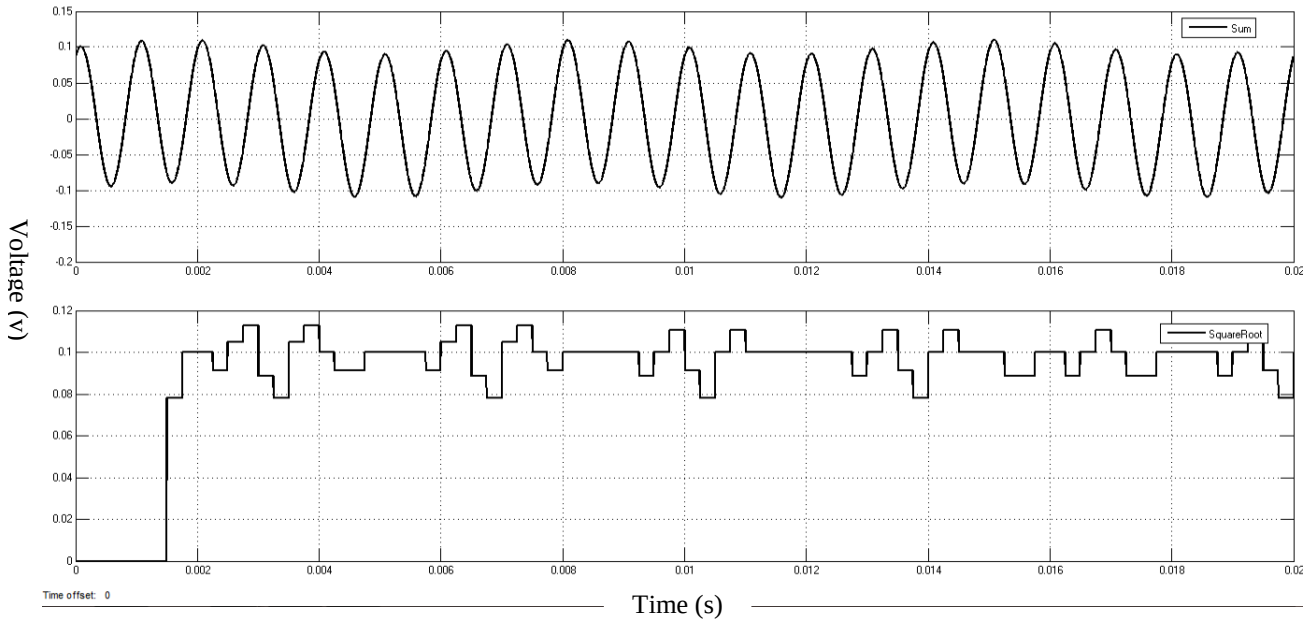


Fig. 4.10: Input and output Waveforms of Complete Design for Input Signal Frequency 1 kHz and Noise Frequency 150 Hz

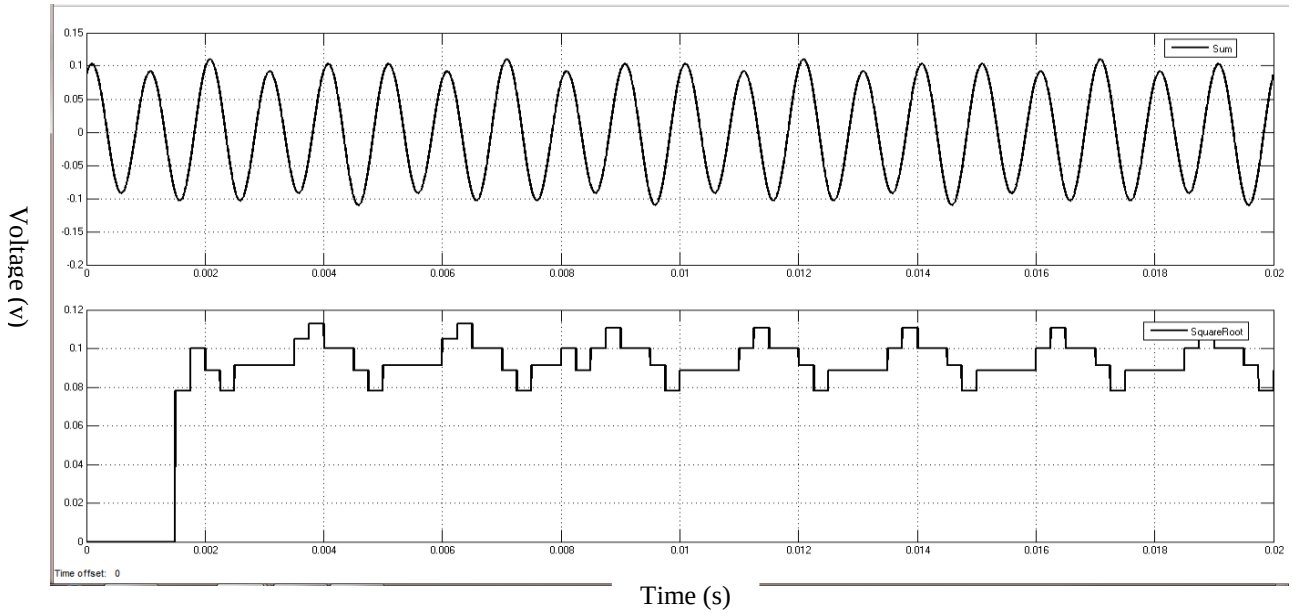


Fig. 4.11:Input and output Waveforms of Complete Design for Input Signal Frequency 1 kHz and Noise Frequency 600 Hz

As it can be seen from the following figures from 4.14 and 4.15, above 2 kHz frequency, magnitude output obtained is nearly DC around 100 mV. For noise frequencies below 2 kHz, maximum voltage fluctuations of ΔV= 40 mV as it can be seen from the Fig. 4.9 to 4.12.

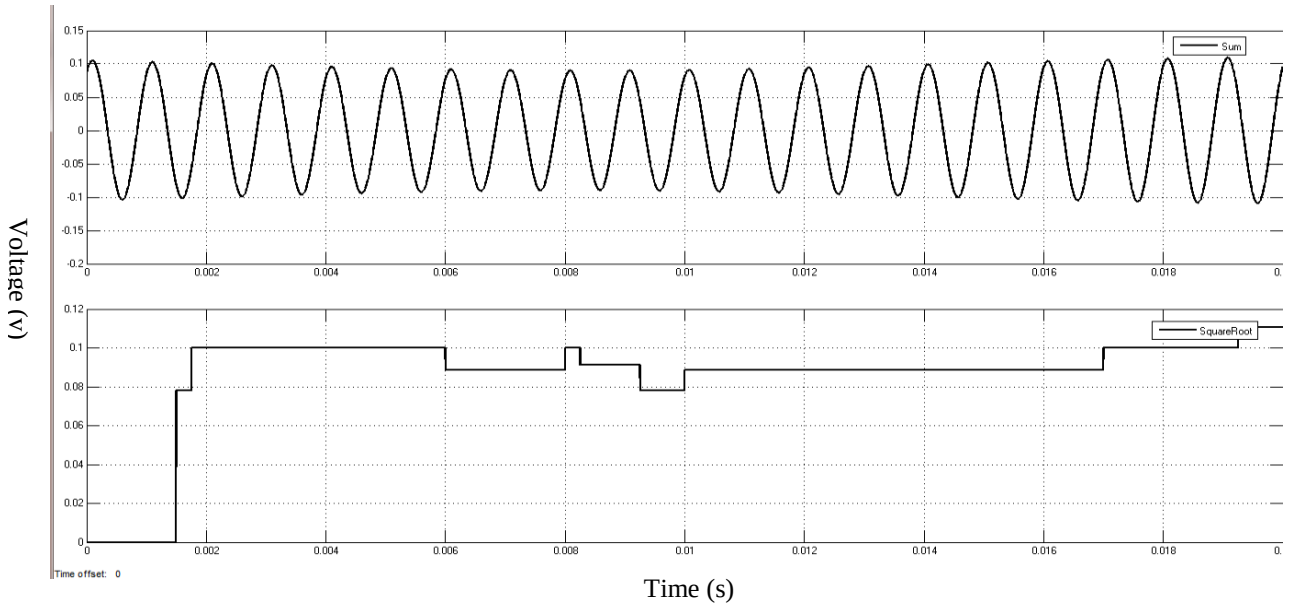


Fig. 4.12: Input and output Waveforms of Complete Design for Input Signal Frequency 1 kHz and Noise Frequency 960 Hz

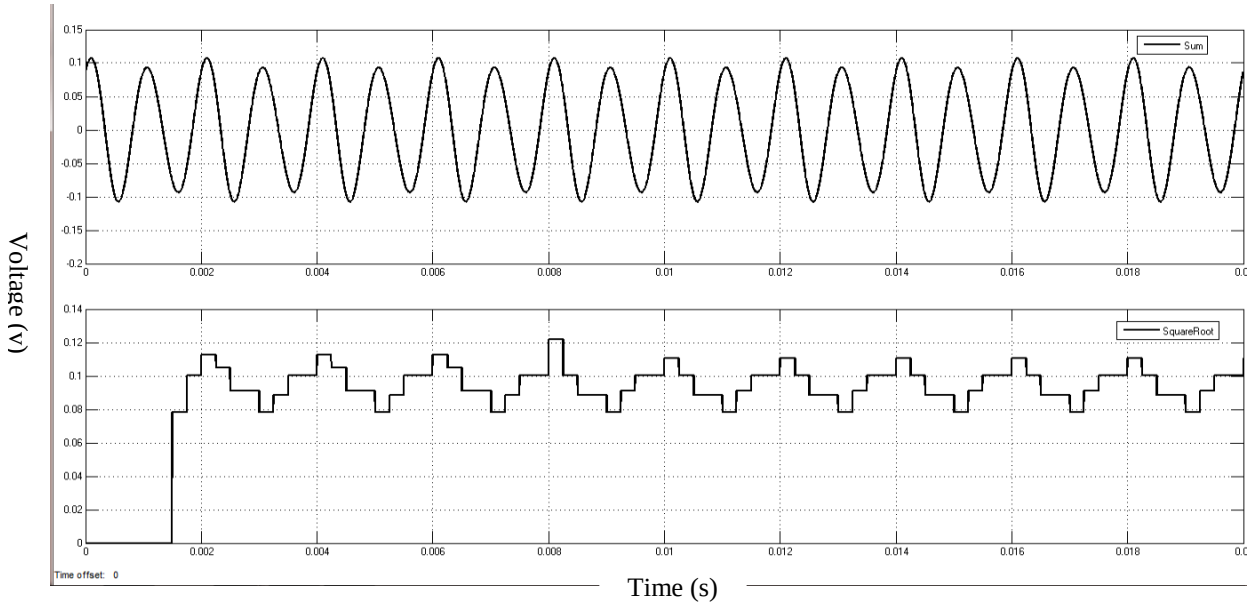


Fig. 4.13: Input and output Waveforms of Complete Design for Input Signal Frequency 1 kHz and Noise Frequency 1.5 kHz

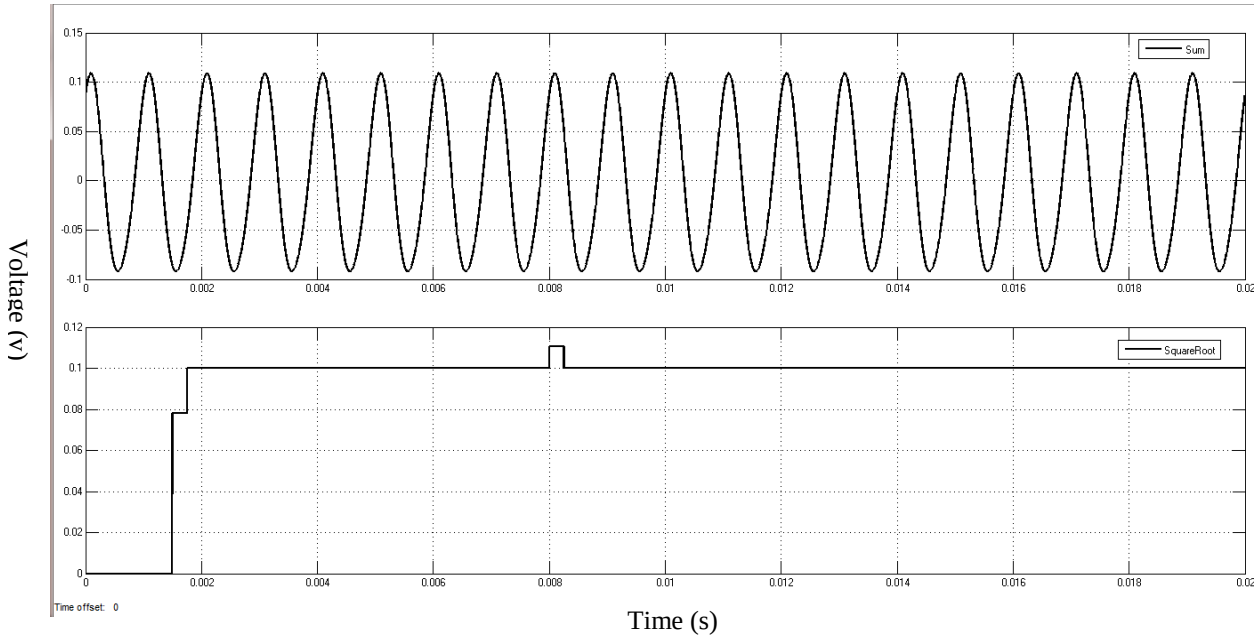


Fig. 4.14: Input and output Waveforms of Complete Design for Input Signal Frequency 1 kHz and Noise Frequency 2 kHz

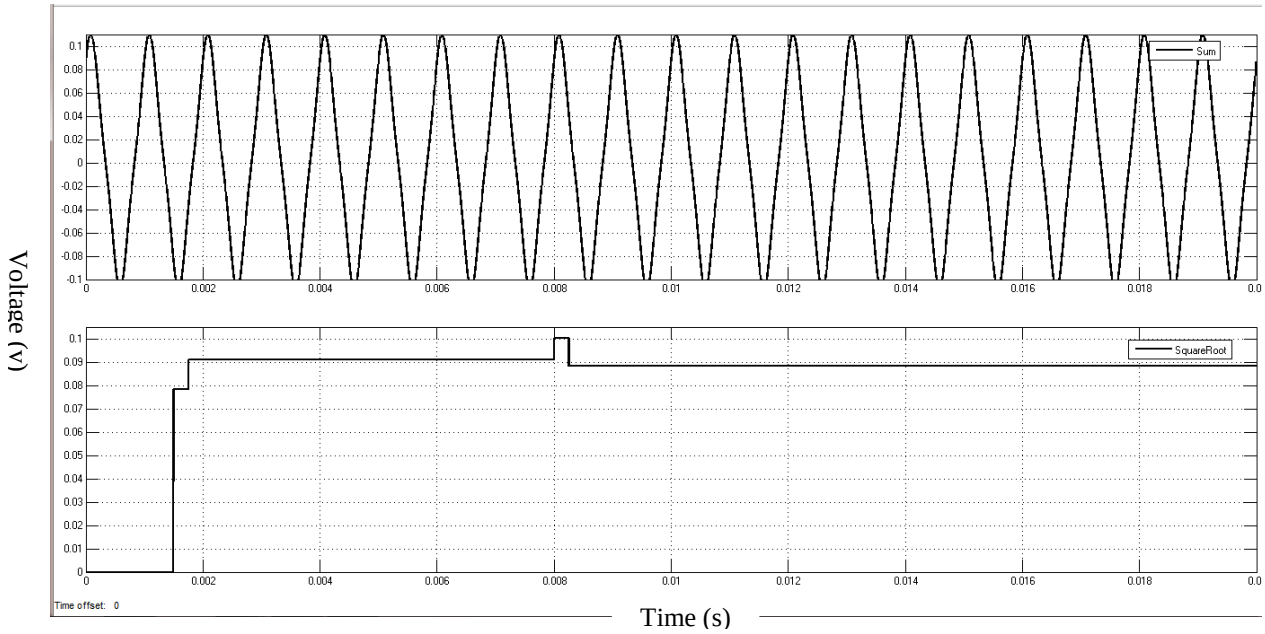


Fig. 4.15: Input and output Waveforms of Complete Design for Input Signal Frequency 1 kHz and Noise Frequency 3 kHz

Obtained Proposed System Parameters:

- Input operating frequency: 1 kHz
- Output Voltage Signal Range: 0.1 to 1 $V_{(p-p)}$
- Filter Order: 4
- Max filter ripple amplitude: -42dBm
- Noise levels in output: 45-60dBm

5. FPGA IMPLEMENTATION

For implementation and testing purpose, Hardware Co-simulation has been used to verify outputs from FPGA. The Simulink graphical language allows an abstraction of the design through the use of available System Generator blocks and subsystems. Using hardware co-simulation, an effective reduction in time can be obtained in control design and hardware implementation. In addition, the software provides for the hardware simulation and hardware-in-the-loop verification, referred to as hardware co-simulation, from within this environment. Compared to HDL based method, this is a better approach. It is a far more cost efficient methodology in comparison to others. The ability of quick and direct realization of the control system design as a real-time embedded system greatly facilitates the design process [48].

Given below are the steps that are followed for implementation and testing:

1. Generate Board support package[48].

- Open the required design file (.mdl).
- New compilation target has to be created.
- Use of Spartan 3E kit has been made and hence, clock frequency of the board is 50MHz and clock pin location is C9.
- For Boundary Scan and IR Length, the board is simply connected and the respective values have been detected.
- Finally, the target device has been selected as Spartan3e (xc3s500e -4 fg320).

2. Generate Hardware Model[48]

- Open the model file for the simulated block.
- Double click and open the system generator token.
    - Compilation: HDL Co-Simulation -> s3e_starter
    - Synthesis tool: XST
    - Hardware description language: VHDL
- Click Generate button in System Generator token for generating the Hardware model.

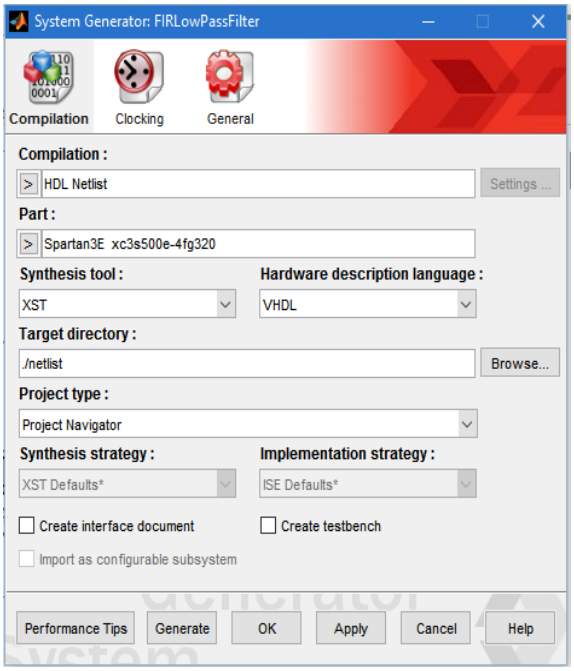


Fig. 5.1: System Generator Token Setting

3. Connect Hardware Model and perform JTAG Co-Sim [48].

- Connect hardware run time model.
- Specify Xilinx Platform USB as download cable in Hardware Co-Simulation block.
- Now, start the simulation to verify the hardware-in-the-loop.

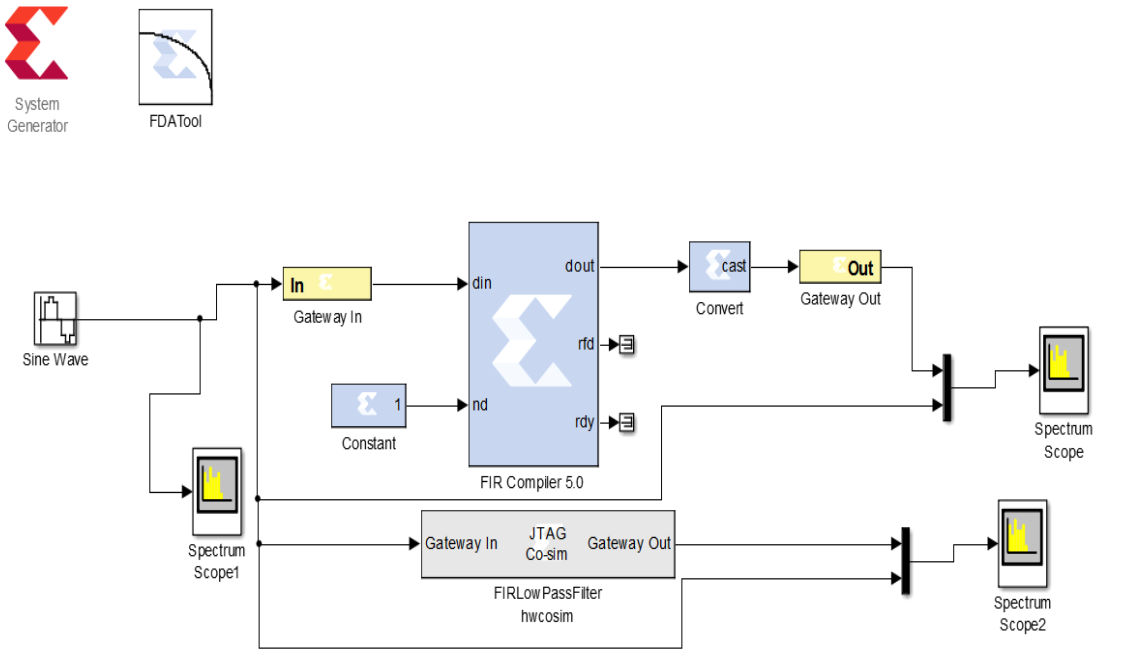


Fig. 5.2: Filter Block Hardware Co- Simulation using JTAG

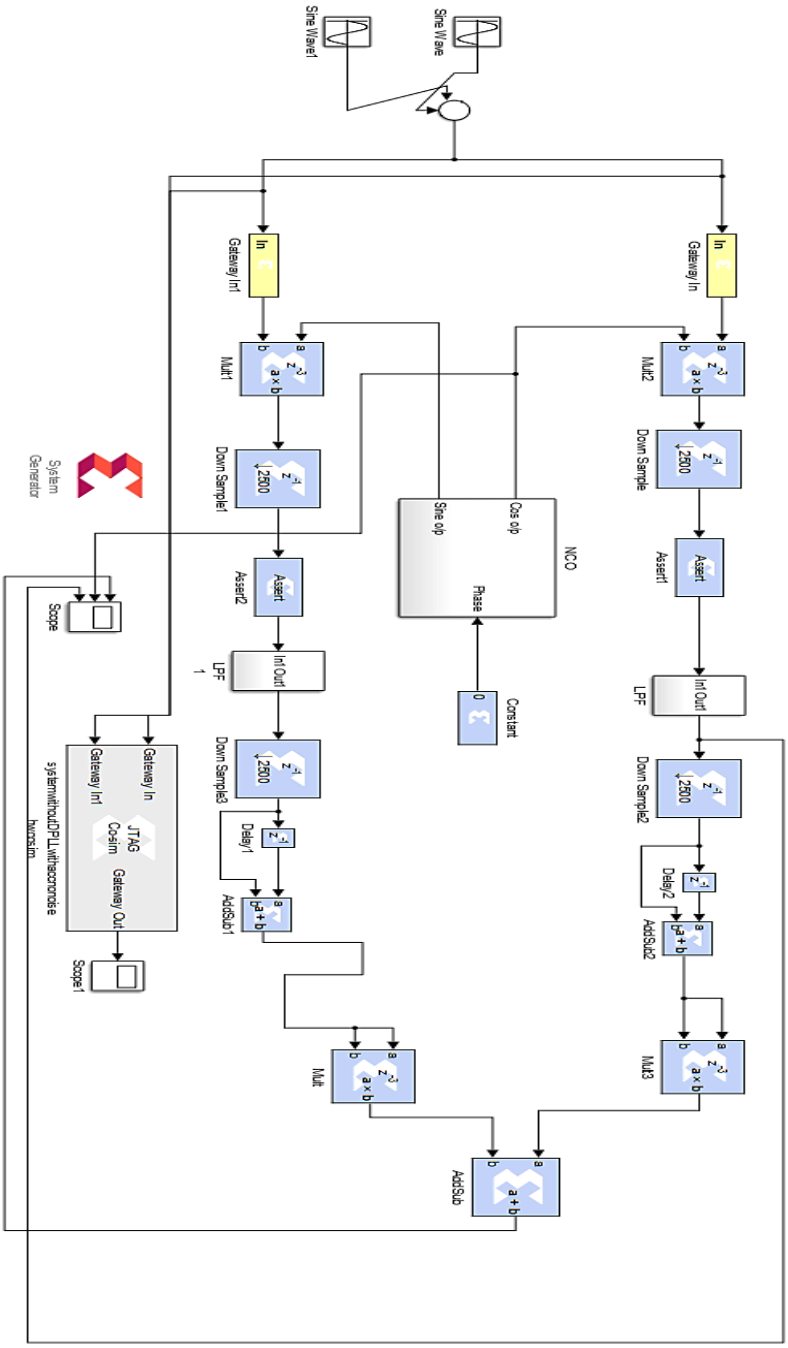


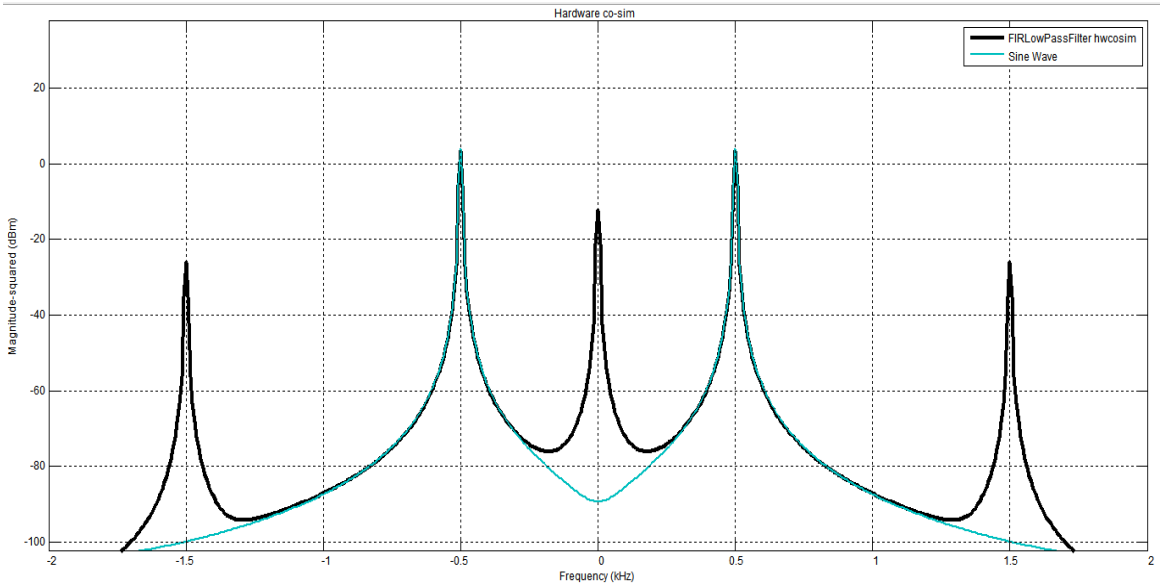
Fig. 5.3: Hardware Co-Simulation of the entire system

5.1 Hardware Co-Simulated Output:

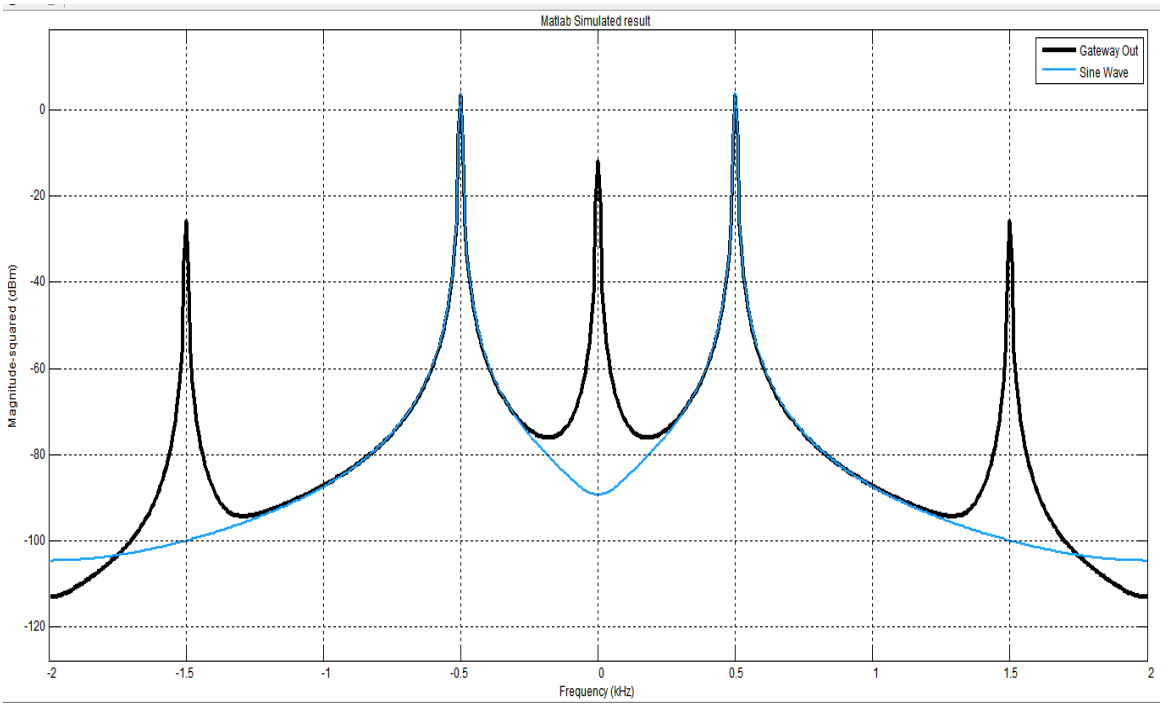
As it can be observed from the graphs, the outputs from the hardware-in-the-loop verification fairly emulate the MATALB - Simulink and System Generator simulation.

- **Filter Block Level Simulation**

The MATLAB simulation and Hardware Co-Simulation results are given in Fig. 5.4 to 5.6 for Filter block.



(a)



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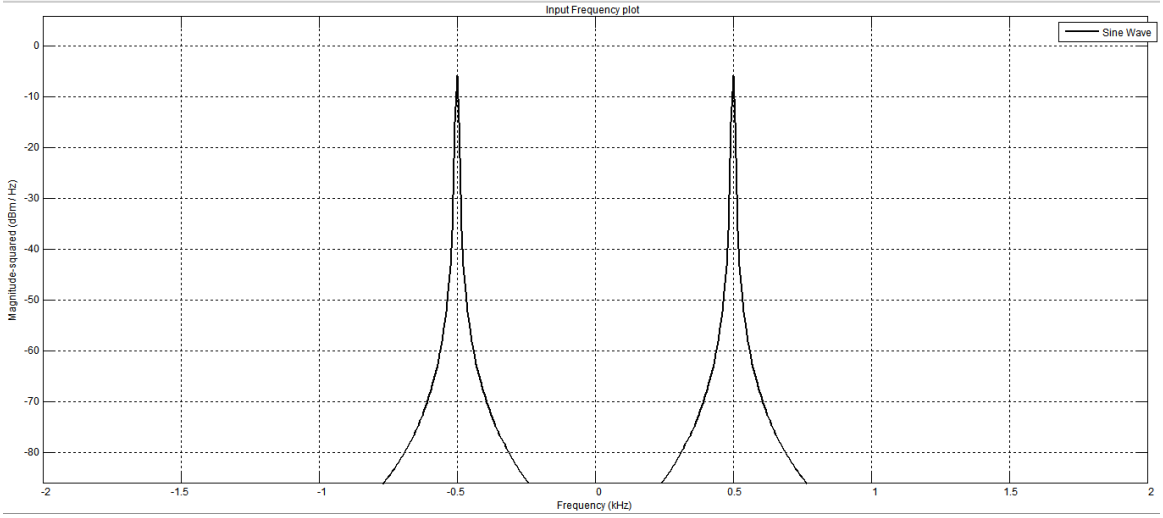
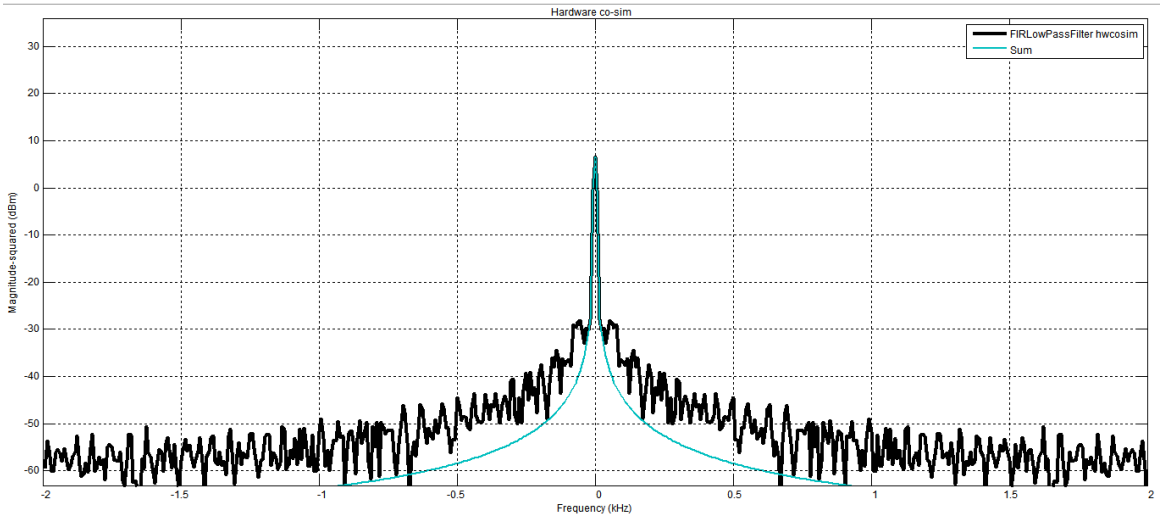
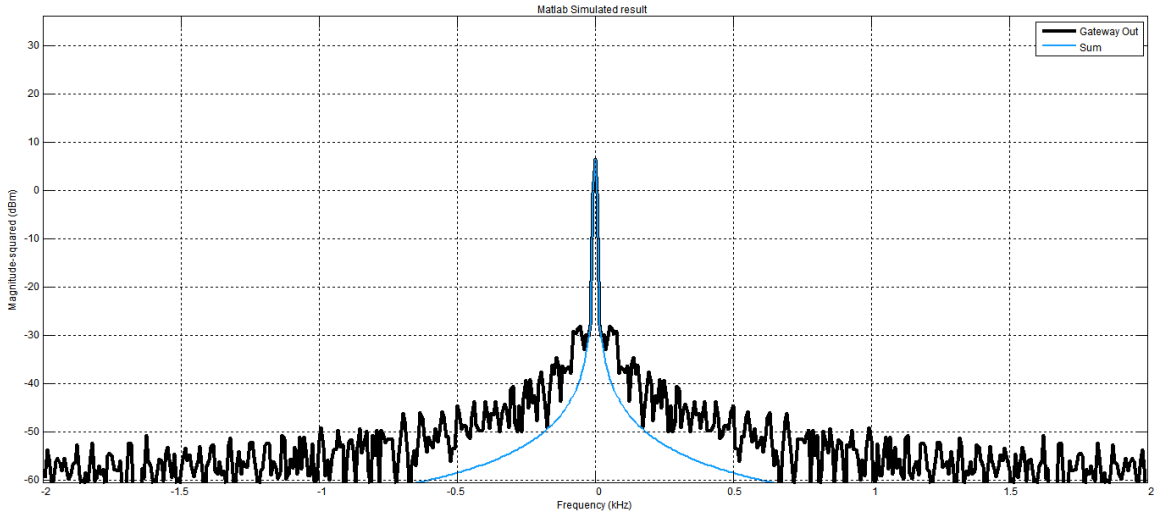


(c)

Fig. 5.4: For Single Freq. input of 500 Hz (a) Hardware co-simulated (b) MATLAB Simulated Output (c) Input Spectrum



(a)



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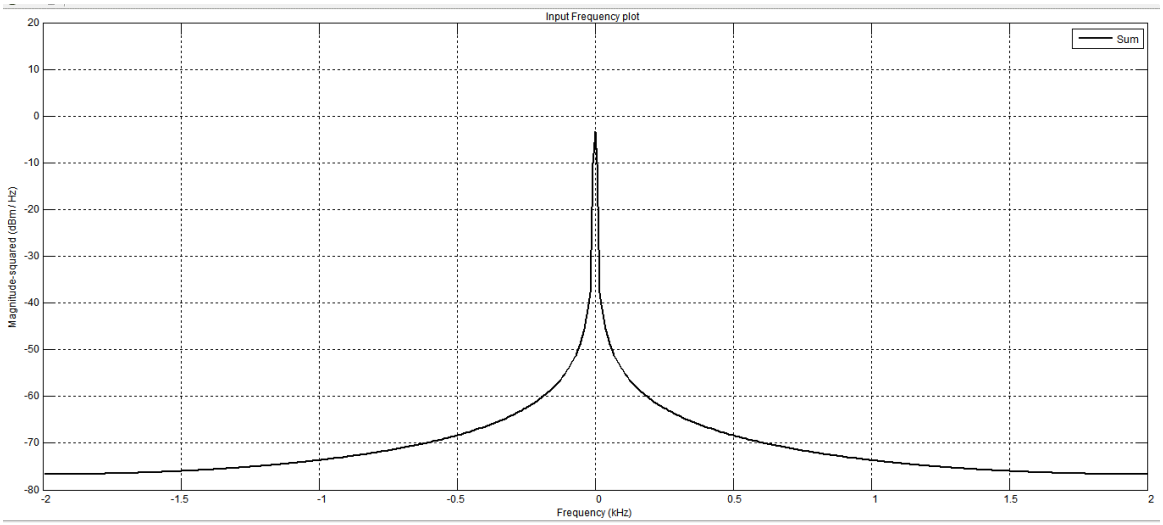
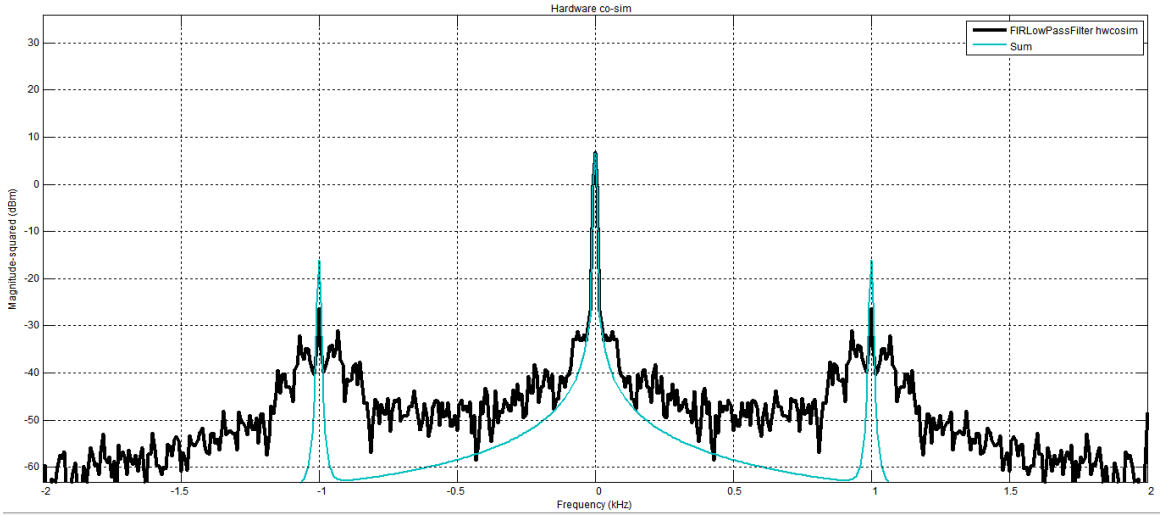
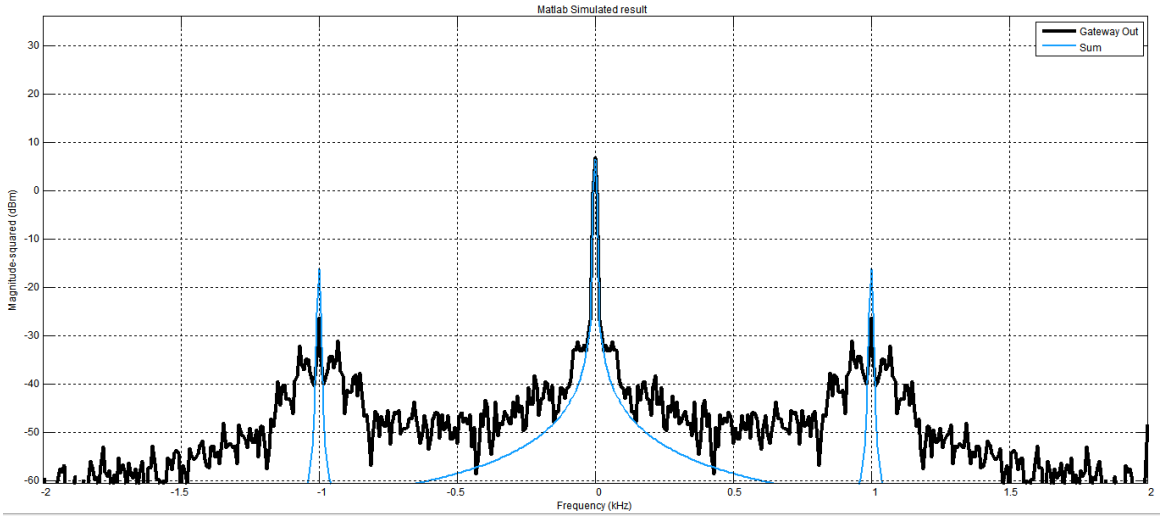


(c)

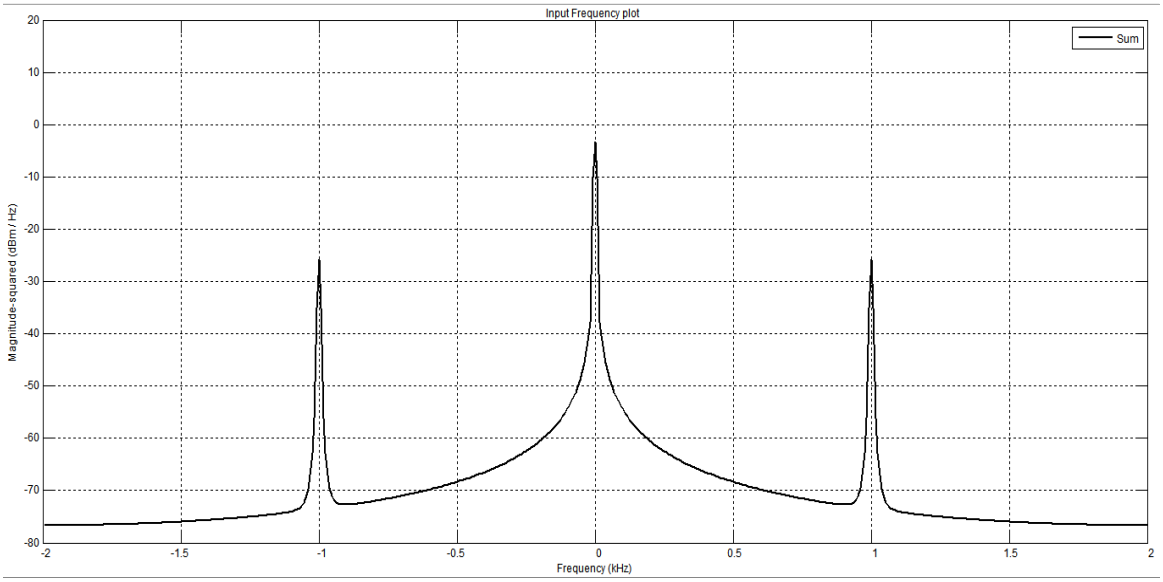
Fig. 5.5: Input Message Frequency of 2 Hz, Noise Signal Frequency 2 kHz (a) Hardware Co- Simulated Spectrum (b) MATLAB Simulated Output Spectrum (c) Input Spectrum



(a)



(b)

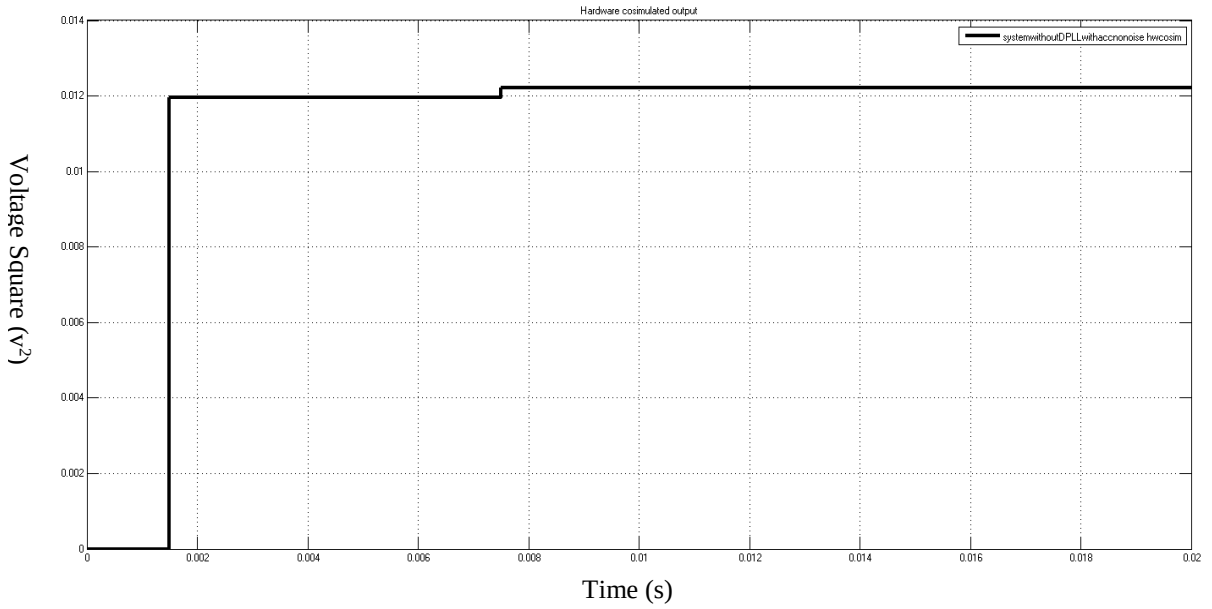


(c)

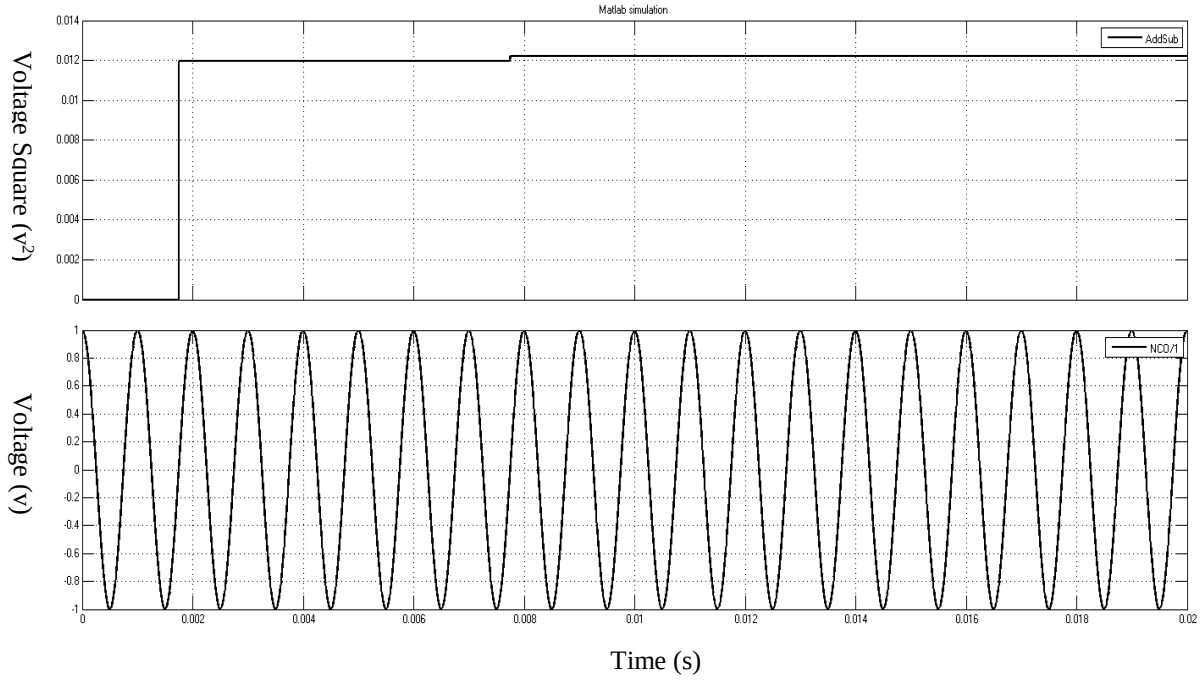
Fig. 5.6: Input Message Frequency of 2 Hz, Noise Signal Frequency 1 kHz (a) Hardware Co- Simulated Spectrum (b) MATLAB Simulated Output Spectrum (c) Input Spectrum

- **<u>Full System Level</u>**

The MATLAB simulation and Hardware Co-Simulation results are given in figures from 5.7 to 5.9 for Full System block.

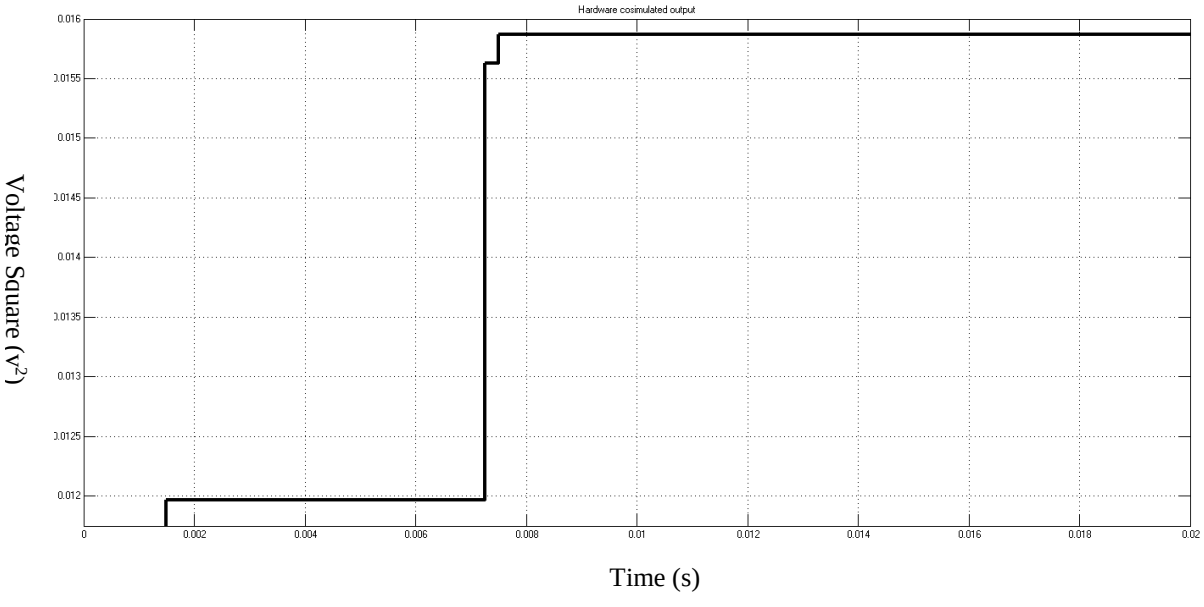


(a)

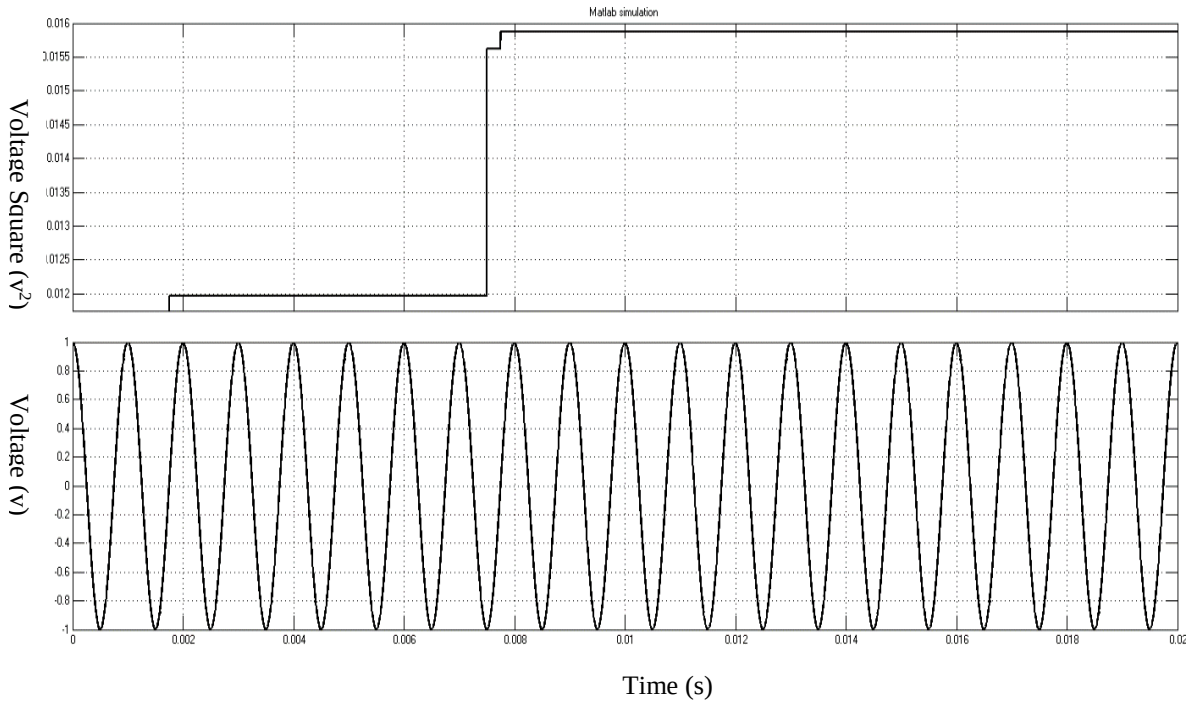


(b)

Fig. 5.7: Full System Simulation for Input Frequency of 1 kHz and Noise Frequency of 2 kHz (a) Hardware Co-Simulation Waveforms (b) MATLAB Simulated Waveforms

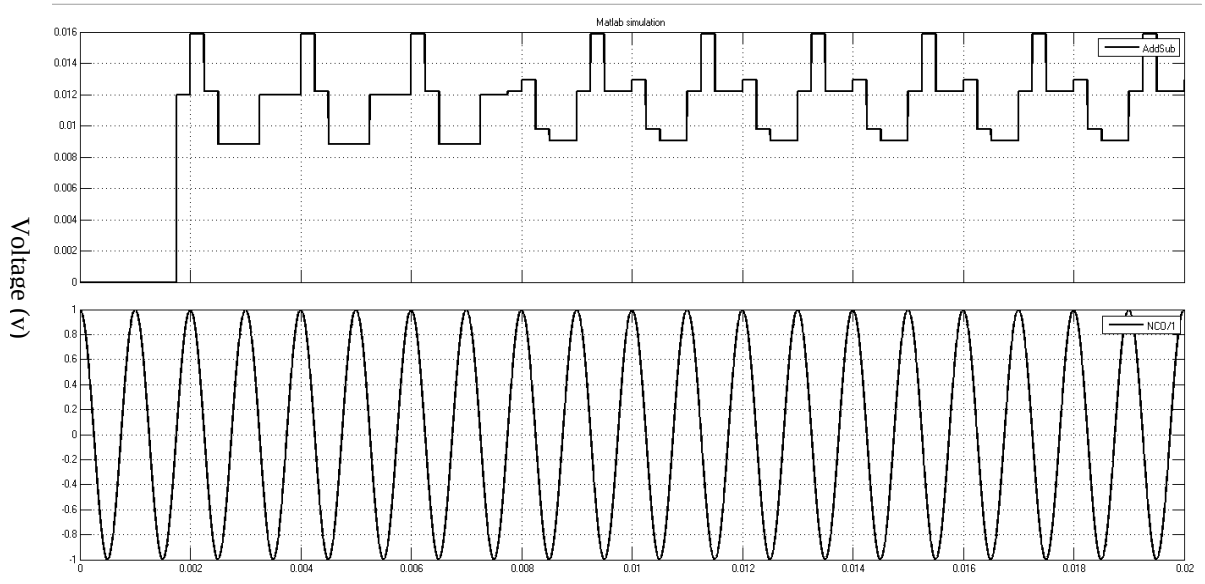


(a)

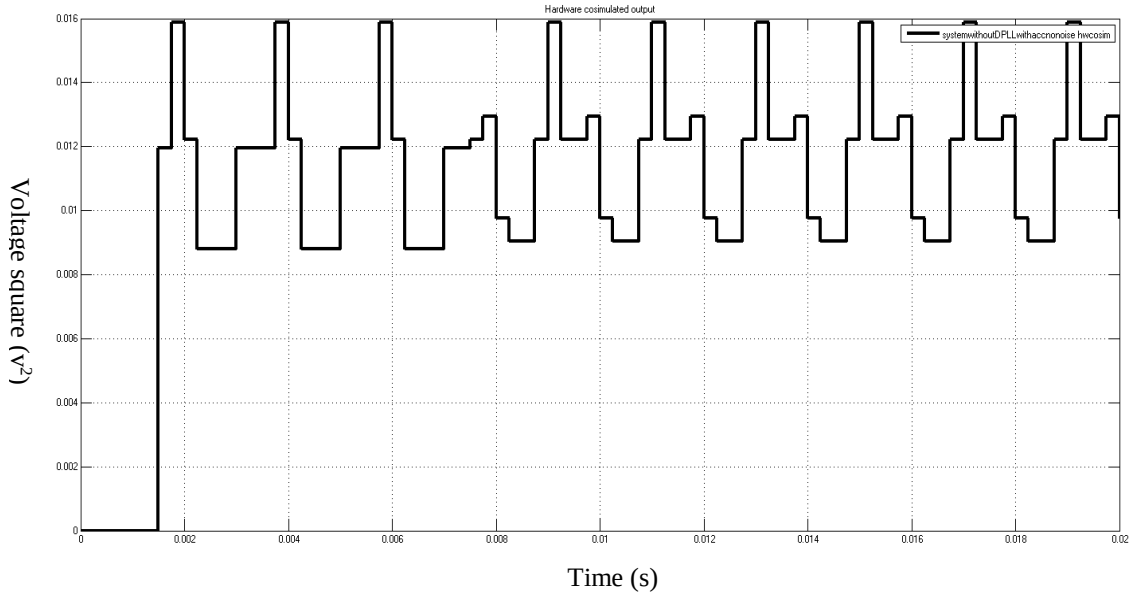


(b)

Fig. 5.8: Full System Simulation for Input Frequency of 1 kHz and Noise Frequency of 3 kHz (a) Hardware Co-Simulation Waveforms (b) MATLAB Simulated Waveforms



(a)



(b)

Fig. 5.9: Full System Simulation for Input Frequency of 1 kHz and Noise Frequency of 500 Hz (a) MATLAB Simulated Waveforms (b) Hardware Co- Simulated Waveforms

Following results have been obtained:

1. Noise signals that have been visualized in the output are in the range -45 to -60 dBm.
2. Gain of the DC signal: 8 to 2 dBm.
3. The I square and Q square results show nearly a DC signal above 2 kHz noise frequency and below 2 kHz fluctuation in the DC voltage has been observed around 7.5 mV for a 100 mV input and 10 mV noise amplitude signal, which is the same as observed in MATLAB Simulation.

5.2 Summary

In a nut shell, we have observed the MATLAB Simulation and Hardware Co-Simulation output and concluded the above results. The ADA2200 is a very popular sampled analog technology[1] synchronous demodulator used for signal conditioning in industrial, medical, and communications applications. The ADA2200 is an analog input, sampled analog output device. The signal processing is performed entirely in the analog domain by charge sharing among capacitors, which eliminates the effects of quantization noise and rounding errors

[49]. Hereby, we compare the output of our proposed design and ADA 2200 output parameters.

Table 5.1: Comparison between current state of art and proposed design

Parameter	ADA 2200	Proposed Design
Filter Order	8	4
Working Voltage Range$_{(p-p)}$	0.3V – 3V	0.1V - 1V
Filter Quality Factor	1.9	0.8571
Programmability	Yes	No
Noise Level	-55 to -60dB	-45 to -50 dB
Stopband Ripple Level	-55dB	-42dB

CONCLUSION AND FUTURE WORK

The possibility of using Lock-in amplifier in removing noise and getting correct measurements for bioimpedance have been explored. Different methods of measuring bioimpedance like single frequency measurements, multi-frequency measurements and spectroscopy have been studied.

A synchronous demodulator has been designed, optimized and tested with hardware co-simulation on FPGA kit. A digital circuit is the output that has advantages over circuit complexity over its analog counterpart ADA2200.The filter order required for the low pass filter is 4, which is a development over the analog circuit which uses an 8^{th} order filter. Also the input voltage range is improved with proposed circuit working on voltages as low as 100mv. Also the filter ripple magnitude and final noise levels in the output are comparable to ADA2200. While the proposed circuit is better on many terms as compared to the given state of the art IC, there are also a few limitations and tradeoffs that could not be resolved.

- The transition band of the filter designed is too wide due to the design constraints of frequency as well as reducing complexity of the circuit.
- The proposed circuit is not programmable and is based to work on a single excitation frequency.
- The sampling frequency of the system is limited by the method of filter design, NCO design constraints as well as the on board ADC and DAC provided on FPGA kit.

Future work:

Various tradeoffs have been taken under consideration as the circuit simplicity and optimum reliability has been given priority. Optimizations can be made to the proposed circuit for better accuracy and results than the one obtained however at the cost of increased circuit complexity.

- Better filter response can be obtained with steep transition band and lesser ripple in stop band by increasing the order of the filter.

- Extensive use of memory blocks can be done to make filter programmable and to work for a band of frequencies.
- Implementation can be done on a better or higher version of FPGA board that has advanced facilities like square root support, support for floating point operations, ADC and DAC with higher bit precision etc.
- At the cost of increased memory and increased processing at the block level, the word length of the coefficients and input data can be increased to give even better accuracy and low quantization noise.

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LIST OF ACRONYMS/ ABBREVIATIONS

ADPLL	All-Digital PLL
BCM	Body Cell Mass
BIA	Bio-Impedance Analysis
BIS	Bioimpedance Spectroscopy
CDPLL	Classical Digital PLL
CSD	Canonic Signed Digit
ECF	Extra Cellular Fluid
EIT	Electrical Impedance Tomography
FFM	Fat Free Mass
FIR	Finite Impulse Response
FM	Fat Mass
IC	Integrated Circuit
ICF	Intra Cellular Fluid
IIR	Infinite Impulse Response
MF-BIA	Multiple Frequency-Bioimpedance Analysis
NCO	Numerically Controlled Oscillator
PLL	Phase Lock Loop
PSD	Phase Sensitive Detection
RMS	Root Mean Square
SF-BIA	Single Frequency-Bioimpedance Analysis
TBW	Total Body Water
VCO	Voltage Controlled Oscillator
W_t Body	Body Weight

Appendix A

A summary of recent impedance-based setups.

(Courtesy: Li, N. (2014). Development of real time cellular impedance analysis system. University of Sussex.)

Author/Year	Method Type	Amplitude/ Frequency	Electrodes Quantity	Electrode Space
Antonio Affanni,2012(Cheng et.al. 2013)	LCR meter (HP E4980a, Agilent Technology, USA)	0.1-V ac voltage frequency range of 1 kHz–2 MHz,	Single	250 µm
Shree Narayanana,2010(Narayan an et al., 2010)	Impedance analyzer, (HP 4192A, Agilent Technology, USA)	Shree Narayanana,2010(Narayan an et al., 2010)	Multi-(20)	45 µm
Fareid Asphahani,2011 , (Asphahani et al., 2011)	Lock-in amplifier. (SR810, Stanford Research Systems,USA)	10 mV sine wave frequency range of 500 Hz to 20 kHz	Multi-(32)	20 µm
Cornelia Hildebrandt,2010(Hildebra ndt et al., 2010)	Impedance analyzer (4294, Agilent Technologies,USA)	10mV frequency range of 100 Hz to 1MHz.	Multi-(16)	1 mm
Jhih-Lin Hong,2012 (Hong et al., 2012)	Impedance analyzer (6440B, Wayne Kerr Precision Component Analyzer,UK)	0.2–1.0 V frequency range of 20– 101 kHz.	Single	10 um
Stolwijk, Judith A.,2011 (Stolwijk et al., 2011)	Stolwijk, Judith A.,2011 (Stolwijk et al., 2011)	AC signal with amplitude of 70 mV at 4 kHz	Single	250 um
Qingjun Liu,2009(Liu *et al.*, 2009b)	Impedance analyzer (VersaSTAT3,Princeton Applied Research, USA)	sinusoidal AC voltage of 10mV amplitude (peak-to-peak) frequency range of 1Hz to 1MHz.	Multi-(10 x 10)	80 um

Nirankar N. Mishra,2005 (Mishra et al., 2005)	An function generator (HP3325A, Agilent Technology, USA) and A data acquisition system (PowerLab 4/20, ADInstruments, USA)	amplitude of 50.5mV frequency range of 1k to 8 kHz	Single	100 um
Lei Wang,2010 (Wang *et al.*, 2010a)	DAQ card (PCI-6110, National Instruments, USA)	frequency range of 5k– 250 kHz	Single	60 um
H.S. Kim,2009 (Kim et al., 2009)	H.S. Kim,2009 (Kim et al., 2009)	500 mV frequency range of 40 Hz to 10 MHz.	Single	4 um
Dana Krinke, 2009 (Robitzki et al., 2009)	Impedance analyzer (4294A, Agilent Technologies, USA)	alternating voltage of 10mV frequency range of 100Hz to 500 kHz	Multi	NA

Appendix B

Applications of bioimpedance analysis in clinical status monitoring and diagnosis of diseases.

(Courtesy: Khalil, S., Mohktar, M., & Ibrahim, F. (2014). The Theory and Fundamentals of Bioimpedance Analysis in Clinical Status Monitoring and Diagnosis of Diseases. Sensors, 14(6), 10895–10928. http://doi.org/10.3390/s140610895)

Organ Systems	Diseases	BIA Parameters	Remarks	Authors
Pulmonary system	Lung cancer, stages IIIB and IV	R and X_c (BIVA)	Reactance components decrease in patients (phase angle <4.5). *Clinical Study.*	Toso *et al.*, 2000
	Pulmonary edema monitoring	R (SFBIA)	Mean resistivity for left and right lung (1205 ± 163, 1200 ± 165 Ω·cm) and system reproducibility (2%). *Research Study.*	Zlochiver *et al.*, 2007
Cardiovascular system	Fluid accumulation after cardiac surgery.	Ht^2/Z (MFBIA)	Significant increase in segmental trunk bioimpedance after surgery due to fluid accumulation. *Clinical Study.*	Bracco *et al.*, 1998
Circulatory system	Volaemic status and hyponatraemia	TBW (SFBIA)	In elderly hyponatraemic patients, TBW assessment using BIA method was correlated with dilution of deuterium oxide (R = 0.68). *Clinical Study.*	Hoyle *et al.*, 2011
	Hydration status and hyponatraemia in elderly	TBW (SFBIA)	Assessment of hydration status in elderly hyponatraemic patients using BIA method was more accurate than clinical procedures (Cohen's kappa coefficient = 0.52). *Clinical Study.*	Cumming *et al.*, 2014
Renal system	Chronic hemodialysis	ECF (BIS)	ECF to weight ratio of hypertensive patient's increase from that of normal patients (24.29 ± 3.56% *vs.* 21.50 ± 2.38). *Clinical Study.*	Chen *et al.*, 2002
	Dry weight in kidney failure.	ECF (BIS)	ECF/Wt is 0.239 and 0.214 L/kg for male and female healthy subjects. *Clinical Study.*	Chamney *et al.*, 2002
	Hydration states monitoring in hemodialysis patients	Calf-BIS (BIS)	Normalized resistivity ($\mu = \rho$ /BMI) increased from	Zhu *et al.*, 2007 , 2008

			17.9 ± 3 to 19.1 ± 2.3 × 10^{-2} $\Omega^3 \cdot Kg^{-1}$, and weight was reduced from 78.3 ± 28 to 77.1 ± 27 kg in Post-dialysis. *Research Study.*	
	Dry weight assessment hemodialysis patients	Calf-BIS (BIS)	Dry weight assessed by cBIS underestimate left ventricular mass and blood pressure while antihypertensive medication remains unchanged. *Clinical Study.*	Seibert *et al.*, 2013
	Body fluids estimation in hemodialysis patients	ECF, ICF and TBW (BIS)	Correlation between proposed equation corrected for BMI and the references (mean ± SD) was −0.4 ± 1.4 L for ECF, 0.2 ± 2.0 L for ICF and −0.2 ± 2.3 L for TBW. *Clinical Study.*	Moissl *et al.*, 2006
	Dry weight assessment HD patients	R and X_c (BIVA)	BIVA method shows significant different in vectors in post dialysed patients. *Clinical Study.*	Atilano *et al.*, 2012
Neural system	Alzheimer's disease	R and X_c (BIVA)	BCM decreased in patients for men, T^2 (Hotelling's statistic) = 12.8 and for women, T^2 = 34.9. *Clinical Study.*	Buffa *et al.*, 2010
	Anorexia nervosa (eating disorder)	FM, FFM, TBW and ECF (BIS)	The BCM to Ht^2 ratio was found to be significantly changed between diseased and controls subjects. *Clinical Study.*	Moreno *et al.*, 2008
	Anorexia nervosa (eating disorder)	R and X_c (BIVA)	Gradually increasing in BCM and decreasing in ECF during treatments. *Clinical Study.*	Haas *et al.*, 2012
Muscular system	Body composition changes monitoring during exercise training	FFM and FM (MFBIA)	BIA method underestimates FM (−3.42 kg) and overestimated FFM (3.18 kg); and undetected small shift in body composition due to exercise training. *Clinical Study.*	Sillanpää *et al.*, 2013
Immunology system	Comparison between SFBIA and MFBIA in HIV patients	ECF and TBW (BIS)	Insignificant differences in TBW and ECF estimation using SFBIA, MFBIA and BIS methods. *Clinical Study.*	Paton *et al.*, 1998
	Dengue haemorrhagic fever estimation in children	ECF and ICF (BIS)	(ECF/ICF) increase with increasing dengue virus infections severity in children. *Clinical Study.*	Libraty *et al.*, 2002

	Cancer patients	TBW (SFBIA)	Change in TBW using BIA method (Ht^2/R_{50}) correlate with deuterium dilution in underweight and normal-weight cancer patients ($R^2 = 0.43$ and SEE = 1.22 L). *Clinical Study.*	Simons *et al.*, 1999
	Early diagnosis and risk analysis of dengue	R, C, φ and Xc (SFBIA)	Reactance variations among dengue patients during defervescence of feverintervalis an indicator for classifying risk category in the DHF patients. *Clinical Study.*	Ibrahim *et al.*,
Other diseases	Critically ill subjects	FM, TBW and ECF (BIS)	Body composition using BIS method show slightly more significant in estimation of FM, TBW and ECF among healthy and diseased subjects. *Clinical Study.*	Pichler *et al.*, 2013
	Gastrointestinal disease	R, Xc, Fc, FFM, TBW, ECF and ICF (BIS)	In critically diseased subjects, Fc and ECF increased, Xc decreased, and TBW and ICF remain the same. *Clinical Study.*	Cox-Reijven *et al.*, 2003

Appendix C

Courtesy of:

[1] S. Al-Araji, Z. Hussain, and M. Al-Qutayri, "Chapter 2 Digital Phase Lock Loops," in Digital phase lock loops: Architectures and Applications, Springer, 2006, pp. 15–16.

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All Digital Phase Locked Loop

The Analog PLLs (APLLs) are still widely used, but Digital PLLs (DPLLs) are attracting more attention for the significant advantages of digital systems over their analog counterparts. These advantages include superiority in performance, speed, reliability, and reduction in size and cost. DPLLs alleviated many problems associated with APLLs. The following is a brief comparison [1]:

1. APLLs suffer from the sensitivity of the voltage-controlled oscillator (which decides the center frequency) to temperature and power supply variations, hence the need for initial calibration and periodic adjustments. DPLLs do not suffer from such a problem [1][2].

2. The most familiar error detectors used in APLLs utilize analog multipliers (balanced modulators) which are sensitive to DC drifts, a problem that does not exist in DPLLs [1].

3. DPLLs can operate at very low frequencies that create problems in APLLs. These problems are related to the operation of the analog low-pass filter in extracting the lower frequency component, as it needs larger time for better frequency resolution, and this will reduce the locking-speed [1].

4. Self-acquisition of APLLs is often slow and unreliable, while DPLLs, a basic block diagram is shown in Figure 2.1, have faster locking speeds. This is due to the basic operation of the analog low-pass filter and the analog multiplier in the phase detector (PD)[1].

An All-Digital Phase-Locked Loop (ADPLL) is one of the many types of phase locked loop (PLL) in which all the components that are being used are digital in nature. Thus these types of PLL have the advantage of being realizable in an FPGA. The use of digitized components gives it flexibility and the parameters of the components can be changed on the field itself. Also, the use of digitized components provides immunity from factors such as temperature dependency and parasitic capacitances which are otherwise very much prominent in analog devices. The digital nature of the components also helps in noise immunity thus improving the functionality of the circuit [1].

ADPLL Structure

The basic structure of an all-digital phase-locked loop has been shown in figure 6. The phase detection system for the ADPLL consists of the Hilbert Transform and the CORDIC algorithm as the phase detection system, the PI controller as the loop filter and the CORDIC algorithm is the rotation mode as the Digitally Controlled Oscillator (DCO). The advantage of the phase detection system comprising of Hilbert filter and the CORDIC algorithm in vectoring mode is that it not only has a good working range and a better resolution but is also FPGA realizable [3].

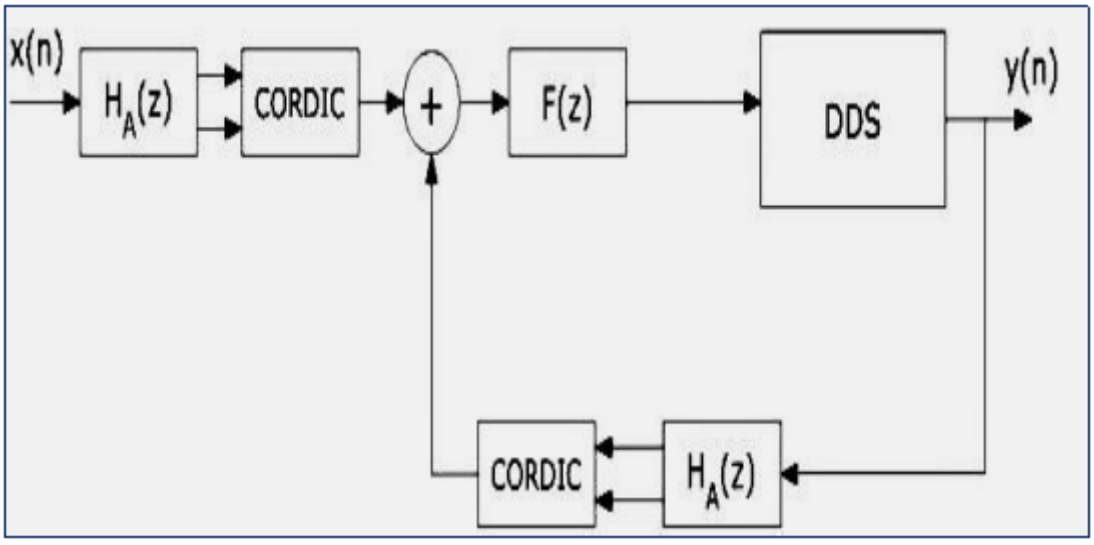

Fig. C.1: ADLL Architecture [4]

Phase Detection System

The phase detection system of the ADPLL comprises of two parts or blocks. The first part is the Hilbert filter block which works on the concept of generation of an analytic signal in order to generate an imaginary part as well as a real part from an input signal. The second part consists of the CORDIC algorithm in its vectoring mode of operation which computes

the value of instantaneous phase by calculating the arctangent value of the imaginary part by the real part.

Hilbert Transform

Hilbert transform works on the principle of generation of an analytic signal in order to calculate the phase information of a signal. In an analytic signal no negative frequency components exist i.e. there are no spectral components in the range $-\pi<\Omega<0$. The analytic signal is made up of two parts, the real part which is simply the input signal that is coming in, and the second part is the imaginary part. The imaginary part actually is the Hilbert transform of the real part i.e. the input that is coming in. Any real sinusoid represented by A cos ($\omega t + \phi$) and on generation of phase quadrature component A sin ($\omega t + \phi$) to serve as imaginary part concerts a positive sinusoidal represented by A exp $\{j(\omega t + \phi)\}$. If a signal is complicated and consists of many sinusoids, a filter is implemented in that case which shifts each of the components by a quarter cycle. Such filters are known as Hilbert Transform Filters. This type of filter should introduce a phase shift of $-\pi/2$ at each positive frequency and a phase shift of $\pi/2$ at each negative frequency. The filter should ideally have a magnitude of one. The discrete Hilbert transform's frequency response is given by [3],

$$H_H(e^{j\Omega}) = \begin{cases} -j \; for \; 0 < \Omega < \pi \\ j \; for -\pi < \Omega < 0 \\ 0 \; for \; \Omega = 0 \end{cases} \quad (C.1)$$

Thus for an input signal x(n), the analytic signal is given by,

$$\underline{x(n)} = x(n) + j\,H\{x(n)\} \quad (C.2)$$

In order to obtain the phase information of the signal, the arctangent value of the imaginary part by the real part is calculated using the CORDIC algorithm given by [3],

$$\Phi(t) = \arctan \frac{Im(\underline{x(n)})}{Real(\underline{x(n)})} \quad (C.3)$$

Cordic Algorithm

CORDIC stands for COrdinate Rotation Digital Computer which is an algorithm proposed by Volder to compute elementary trigonometric functions. CORDIC may be performed in two different modes - rotation mode and vectoring mode both of which are used in this project. The output of the Hilbert transform is fed to the CORDIC algorithm which

computes the instantaneous phase of the signal at every instant of time. The use of CORDIC algorithm reduces the complexity of the system as they use no multipliers at all [4].

In this method the coordinate of an input vector is rotated by constant angles until its angle is reduced to zero. The operation of planar rotation for a vector A with coordinates (X_j, Y_j) is given by the equation in the matrix form [4]

$$\begin{bmatrix} x_j \\ y_j \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} x_i \\ y_i \end{bmatrix} \tag{C.4}$$

The calculation of this rotation involves trigonometric functions sin and cos. The rotation of this vector through an angle θ is executed iteratively in steps. The rotation equation now can be transformed into [4]

$$\begin{bmatrix} x_{n+1} \\ y_{n+1} \end{bmatrix} = cos\theta_n \begin{bmatrix} 1 & -tan\theta_n \\ tan\theta_n & 1 \end{bmatrix} \begin{bmatrix} x_n \\ y_n \end{bmatrix} \tag{C.5}$$

where the angle steps θ_n are selected such that the tangent of the step is a power of 2 thereby replacing multiplication operation by shifting and addition. The angle parameter for each step is given by [4]

$$\theta_n = \arctan(\frac{1}{2^n}) \tag{C.6}$$

Such that the total rotation is equal to the rotation angle θ of the input vector:

$$\sum_{n=0}^{\infty} S_n\theta_n = \theta \tag{C.7}$$

Where S_n = {- 1 , +1 } in respect to addition or subtraction.

Now, the equation for rotation is modified to

$$\begin{bmatrix} x_{n+1} \\ y_{n+1} \end{bmatrix} = cos\theta_n \begin{bmatrix} 1 & -S_n 2^{-n} \\ S_n 2^{-n} & 1 \end{bmatrix} \begin{bmatrix} x_n \\ y_n \end{bmatrix} \tag{C.8}$$

In the above equation $cos\theta_n$ can be taken to be a constant K which can be computed later and the introduction of terms of power of 2 replace the multiplication operation by shifting and addition. The value of the rotation parameter S_n is decided by the residue Z defined as the difference between total rotation to be done and sum of all the rotations already performed and is given by the equation [4]

$$Z_{n+1} = \theta - \sum_{i=0}^{n} \theta_i = \theta - \sum_{i=0}^{n} \arctan\left(\frac{1}{2^n}\right) \tag{C.9}$$

And the value of the rotation parameter is

$$S_n = \begin{cases} -1 \; if \; Z_n < 0 \\ 1 \; if \; Z_n \geq 0 \end{cases} \tag{C.10}$$

Each iteration of the CORDIC algorithm increases the resolution of the output by one bit. Therefore since the iterations never go to infinity, N pre-computed arctan values can be stored in a look-up table (LUT) to be referenced, where N is the number of iterations to be performed [4].

For the rotation mode of operation of the CORDIC we drive Z to zero thereby performing:

$$\begin{bmatrix} X_j \\ Y_j \\ Z_j \end{bmatrix} = \begin{bmatrix} P(X_i \cos Z_i - Y_i \sin Z_i) \\ P(Y_i \cos Z_i + X_i \sin Z_i) \\ 0 \end{bmatrix} \tag{C.11}$$

With the initial values of $X_i = 1/P$, $Y_i = 0$ and $Z_i = \theta$ at the end of iteration we get,

$$\begin{bmatrix} X_j \\ Y_j \\ Z_j \end{bmatrix} = \begin{bmatrix} \cos\theta \\ \sin\theta \\ 0 \end{bmatrix} \tag{C.12}$$

The rotation mode of CORDIC algorithm is used to work as a DDS for this ADPLL. For the instantaneous phase detection of the input waveform and the DDS output we make use of the CORDIC algorithm in its vectoring mode. There to meet our requirement we drive Y coordinate to 0 such that the final vector lies on the X-axis there by providing us the value of the angle rotated in performing the operation. The result thus obtained is [4]:

$$\begin{bmatrix} X_j \\ Y_j \\ Z_j \end{bmatrix} = \begin{bmatrix} P\sqrt{X_i^2 + Y_i^2} \\ 0 \\ Z_i + \arctan(\frac{Y_i}{X_i}) \end{bmatrix} \tag{C.13}$$

Again with, $X_i = X$, $Y_i = Y$ and $Z_i = 0$, we obtain,

$$\begin{bmatrix} X_j \\ Y_j \\ Z_j \end{bmatrix} = \begin{bmatrix} P\sqrt{X^2 + Y^2} \\ 0 \\ \arctan(\frac{Y}{X}) \end{bmatrix} \tag{C.14}$$

Here, neglecting the amplification factor P the magnitude and the phase value are given by X_j and Z_j correspondingly as required.

Loop Filter

The basic functionality of a loop filter is to stabilize the complete PLL. It does that by suppressing the unwanted higher frequency signals and allowing the low frequency signals through it such that only the required signals gets passed and not its harmonics which may cause erroneous results as the DDS will try generating the signals of the higher frequencies as well. Thus the work of the loop filter is very crucial and its parameters must be set according to the precise need of the system for the correct functioning and stability of the system [5].

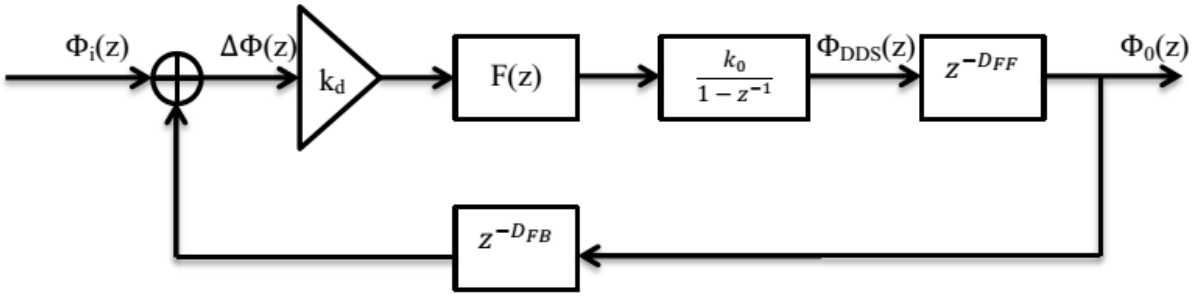

Fig. C.2: Phase Model of ADPLL [5]

Here, D_{FF} and D_{FB} represent the feed-forward path and feedback path processing delays required for pipelining respectively. And the DDS has been represented by the transfer function of the phase accumulator with gain k_o. The gain of the complete phase detection system has been represented by k_d. The phase-error transfer function of the ADPLL is [5]

$$E(z) = \frac{1-z^{-1}}{1-z^{-1}+k_d k_0 F(Z) z^{-(D_{FB}+D_{FF})}} \qquad \text{(C.15)}$$

In order to get the transfer function of the loop filter we can set the error transfer function *E(z)* to be equal to any desired $E_d(z)$ which is causal and hence realizable thereby finding *F(z)* from the equation. $E_d(z)$ has to be chosen such that it satisfies the basic requirements of the ADPLL one of them being the phase-error reducing down to zero with increasing time leading us to [5]

$$\lim_{z\to 1}(z-1)E(z) = 0 \qquad \text{(C. 16)}$$

Other desirable properties of the loop filters include low settling time and a filtering behavior such that the input to output transfer function $H(z) = \frac{\emptyset_0(z)}{\emptyset_I(z)}$ has low pass behavior.

This ADPLL makes use of a PI controller as loop filter *F(z)* which satisfies the required properties. The transfer function for a PI controller is [5]

$$u(s) = (K_P + K_I \frac{1}{s})e(s) \tag{C.17}$$

this is discretized using bilinear transformation done by substituting,

$$s \leftarrow \frac{1}{T_s}(1 - Z^{-1}) \tag{C.18}$$

This results in the IIR filter

$$F_{PI}(z) = \frac{b_0 + b_1 z^{-1}}{1 - z^{-1}} \tag{C.19}$$

where the coefficients

$$b_0 = K_P + K_I T_s \tag{C.20}$$

$$b_1 = -K_P \tag{C.21}$$

and $T_s = 1/ f_s$ as the sample period.

With the help of the analog PLL model we can find the coefficients' value using the damping factor ζ and the natural radian frequency $\omega_n = 2\pi f_n$. Thus the coefficients can be obtained using continuous parameters as [5],

$$b_0 = \frac{(2\zeta + \omega_n T_s) w_n}{K_0 K_d} \tag{C.22}$$

$$b_1 = -\frac{2\zeta w_n}{K_0 K_d} \tag{C.23}$$

Direct Digital Synthesizer

Direct Digital Synthesizer is a type of frequency synthesizer that generates required waveforms when provided with the necessary inputs. DDS finds a very important use in ADPLL as it is responsible to generate the output of the complete structure depending upon the calculations and processing already done by the phase detection system and loop filter. This block produces the final output of the ADPLL [4].

The DDS consists of a Reference Clock generator that provides the clock required by the complete system to operate. The Numerically Controlled Oscillator (NCO) generates a discrete output of the required waveform (in this case a sine waveform) whose period and hence the frequency is controlled by the stored word at the frequency control register. The

discrete binary output of the NCO is converted to analog waveform using a Digital to Analog Converter (DAC). The reconstruction low pass filter is used to filter out the higher order harmonics produced due to DAC [4].

This ADPLL model was synthesized using two different DDSs - CORDIC algorithm in the rotation mode and an LUT based sine waveform generator was also used. Both these methods find application but in different requirements. Since there is no strict memory constraint in case of using an FPGA a LUT based DDS can be used which produces faster result with very less delay. But when this ADPLL has to be fabricated onto a chip reducing memory and thus the cost of the hardware becomes a target which can be augmented using the CORDIC based DDS which stores very less values compared to the LUT based DDS. In addition to that, use of a CORDIC based DDS facilitates easy increase in the resolution of output since only the iteration number needs to be changed. Whereas in case of an LUT based DDS increasing the resolution becomes very tedious due to the fact that the complete LUT needs to be replaced by another LUT that stores values of the sine waveform in higher precision. Hence the use of the DDS is very application specific [4].
LUT based DDS: In this method the values of the first quadrant of sine waveform is stored in an LUT. The values of the remaining quadrants can be found out by either inverting the result or inverting the argument and adding $\pi/2$ or doing both depending on the value of the phase accumulator [4].
CORDIC algorithm based DDS: this method used the CORDIC algorithm in the rotation mode which is already discussed.

Simulink Implementation of ADPLL

For the illustration purpose, ADPLL model was simulated in Simulink as shown in Fig. C.3. Input-Output waveforms for 1 MHz frequency is shown in Fig. C.4. After transient time, output waveform tracks input waveform.

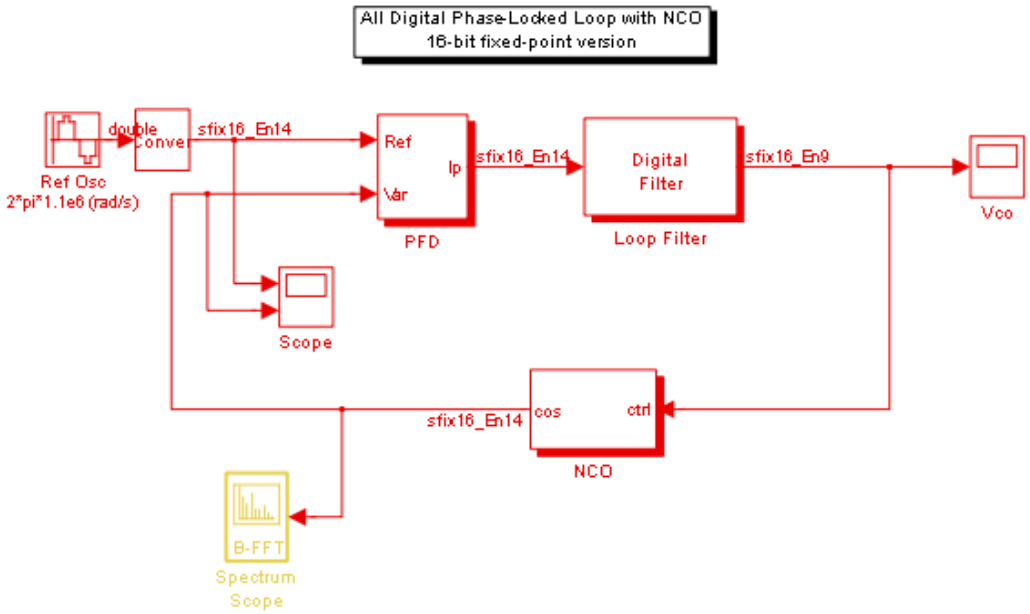

Fig. C.3: Simulink ADPLL Model

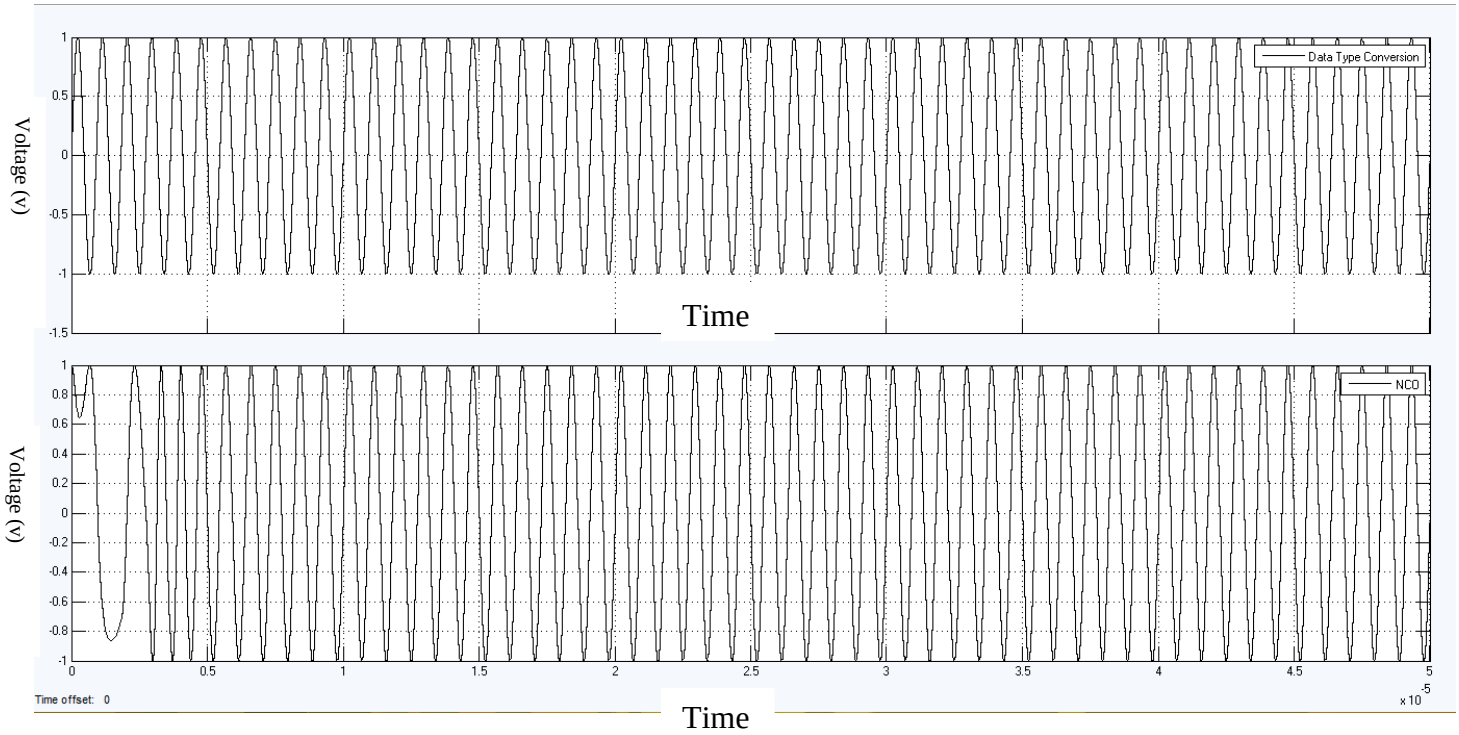

Fig. C.4: Input Output Waveforms for 1 MHz Input Frequency