MILITARY COLLEGE OF SIGNALS
FINAL EXAM
BESE 16 – B
CE 230 Digital Logic Design

Instructor: Dr. Imran Siddiqi **Time: 2.5 hours**
Max Marks: 50

FUNCTION IMPLEMENTATION

(6)

Question # 1

Given the Boolean function:

$$F(A,B,C,D) = \sum(0,4,8,9,10,11,12,14)$$

Using 4 variable k-map, simplify and implement the above function using the following two-level forms:

i. AND-OR-INVERT
ii. OR-AND-INVERT
iii. NOR-NOR

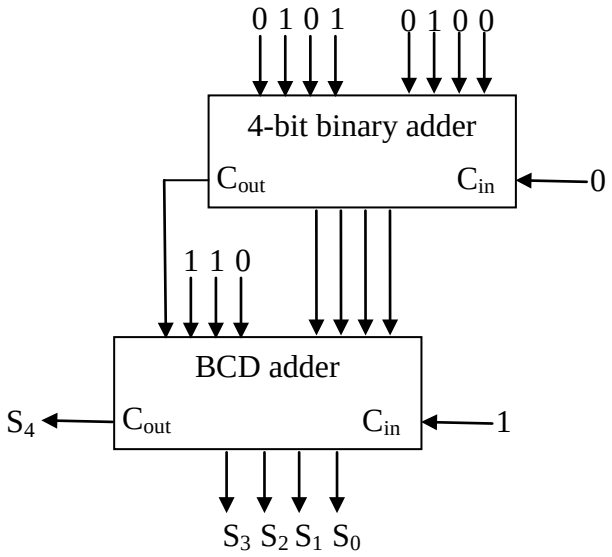
COMBINATIONAL LOGIC

(5+2+4)

Question # 2

a. Design a combinational circuit with three inputs *a,b,c* and three output *x,y,z* such that the output is 1's complement of the input. Simplify the Boolean expressions for *x,y* and *z* and show the circuit design.

b. What is the output ($S_4S_3S_2S_1S_0$) of the following circuit?



c. A combinational circuit is defined by the following functions:

$$F1(x,y,z) = xy' + x'z$$
$$F2(x,y,z) = \sum(0,4,6)$$
$$F3(x,y,z) = \prod(0,4,6)$$

i. Implement the circuit using a decoder and external gates.
ii. Which external gates will you need if the decoder you are using is constructed with NAND gates?

(4+4)

Question # 3

a. A 4x1 multiplexer has inputs *x* and *y* connected to the select lines S_1 and S_0 respectively. The data inputs I_0 to I_3 are as follows:
$I_0=z;\ I_1=z';\ I_2=0;\ I_3=1$

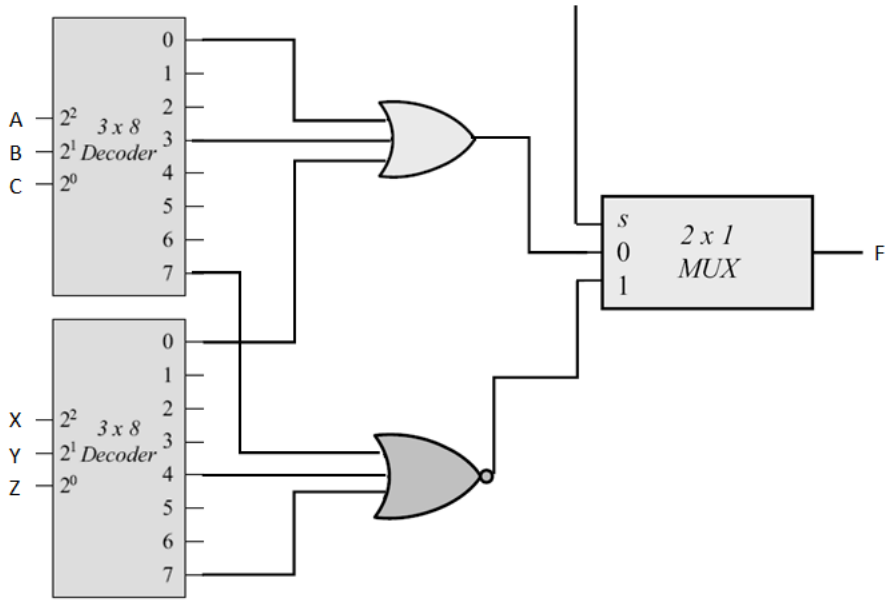
Find the Boolean function *F(x,y,z)* that the multiplexer implements.

b. Implement the full adder using two 8x1 MUXes. Connect *x,y* and C_{in} to the selection lines and 1 or 0 to the data lines.

(3+3)

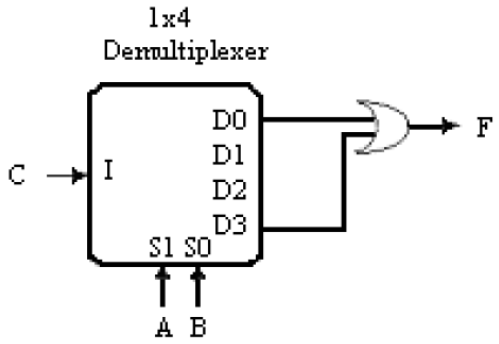
Question # 4

a. Consider the following circuit with two decoders and one MUX.



i. What is the output *F* if the select input *s = 0*.
ii. What is the output *F* if the select input *s = 1*.
iii. Write the Boolean expression for *F* in terms of *A,B,C,X,Y,Z* and *s*. *s* could be either 0 or 1.

b. For the given circuit show the truth table for inputs A, B, C and output F.



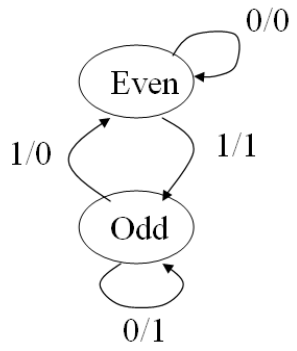
SEQUENTIAL LOGIC

(6+4+2)

Question # 5

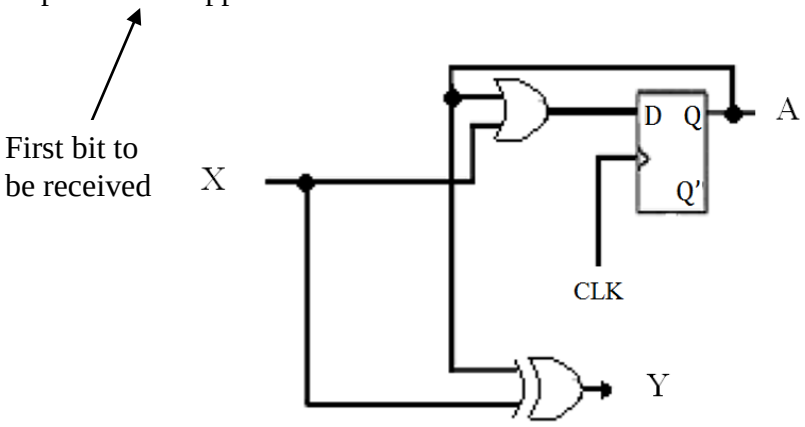
a. Design a sequential circuit that detects the pattern '0010' in a string of bits coming through an input line.

b. It is required to design a state machine that outputs a '0' if an even number of 1's have been received and outputs a '1' otherwise. This can be achieved with the Mealy machine shown below:



Convert it into Moore machine and show the state tables for both the machines.

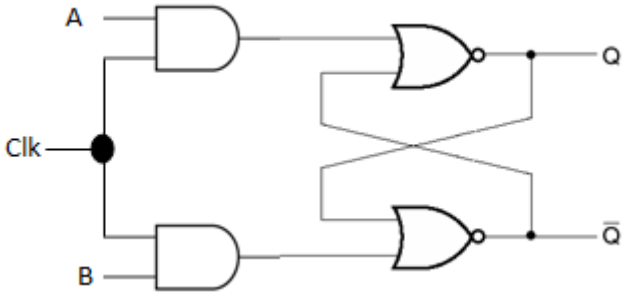
c. Assuming that the flip flop given below is initially cleared, what is the output Y if the serial input 0110 is applied to X.



(3+4)

Question # 6

a. Consider the following latch.



Show the characteristic table for this latch. The table should include the following:

Clk	A	B	Q(t+1)
…	…	…	…
…	…	…	…

b. Reduce the number of states in the following state table. Starting at state '*a*' what is the output sequence if the input sequence 1001 is applied to the original state table before reduction.

	Next State		Output	
Present state	x=0	x=1	x=0	x=1
a	*f*	*b*	0	0
b	*d*	*c*	1	0
c	*f*	*e*	0	1
d	*g*	*a*	1	1
e	*d*	*e*	0	1
f	*g*	*a*	1	1

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