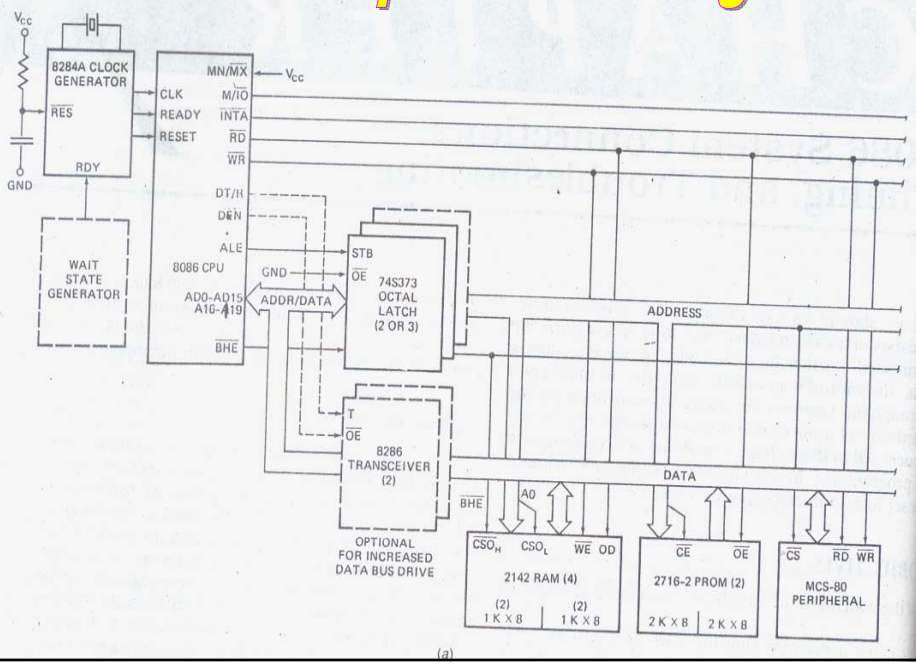
8086/8088 Hardware Specifications

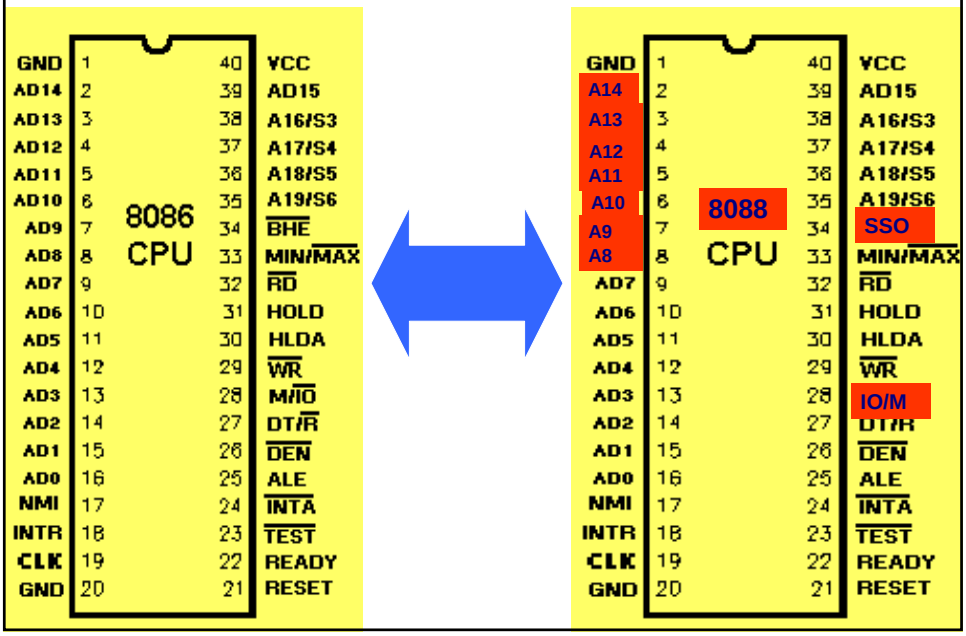
Lecture 05

Asst Prof Athar Mohsin

8086- Simple Block diagram



Pin layout 8086/8088



Pin layout

- Virtually no difference
  - Both are 40 pin
  - 16 bit microprocessors
  - Maj difference is the width of data bus
  - Another Difference is one of the control signal

16 bit data bus	8 bit data bus
AD0-AD15	AD0-AD7
M/IO pin	IO/$\overline{M}$ pin
BHE pin	$\overline{SSO}$ pin

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Pin Functions

- AD7-AD0 (8088): Multiplexed Address and Data bus
  - Memory address or port numbers when ALE is active(1)
  - Data when ALE is inactive (0)
  - High impedance state during hold acknowledge
- A15- A8 (8088): address appears throughout the entire bus cycle
- AD15-AD0 (8086): Multiplexed Address/ Data bus contains
  - Address information or IO port numbers when ALE is active
  - Data when ALE is inactive
  - High impedance during hold ack

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Pin Functions

- A19-A16/S6-S3: Address and status pins are multiplexed and contains
  - Address bus bits with ALE
  - Status bits without ALE
    - S6 always at logic 0
    - S5 indicate condition of 1 flag bit
    - S3 & S4 indicates which segment is accessed during the current bus cycle
- RD: this strobe becomes a logic 0 during reception of data from memory or IO
- READY: when HIGH execute instructions and when LOW, WAIT states are inserted

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Pin Functions

- INTR: used to request hardware interrupt
- NMI: Nonmaskable Interrupt:
  - causes a type 2 interrupt at the end of the current instruction
- RESET: Reset the processor, if remains high for a minimum of four clock
- CLK: to provide basic timings for the processor
- NM/MX: used to select the minimum and maximum mode of operation

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Clock Generator (8284A)

- 8086 requires clock signals from an external clock, to synchronize the internal operations, it provide fol main functions:
  - Clock Generation
  - RESET synchronization
  - READY synchronization
  - Peripheral Clock signal
    - CLK pin provide clock input signal to 8086 and other components
    - PCLK: provide clock signal to peripheral eqpt in the system
- 8284A has a 14.7456 MHz crystal connected to it
  - The clock signal is produced by Freq of the crystal divided by three (14.7456/3)
  - The actual freq for 8086 is 4.915 MHz
  - The PCLK freq is half of the clock freq so it is 2.45 MHz

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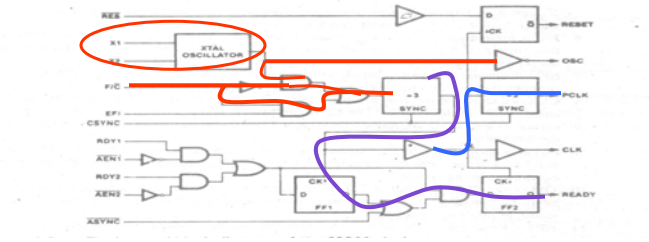
Clock Operation



- Crystal Oscillator has two inputs X1 and X2
  - Oscillator will generate the signal of the same freq as the crystal
  - The generated signal will be fed to AND gate and to an Inverting buffer to provide output signal
  - When F/C is at logic 0 the oscillator output is fed to divide by three counter
- The output of divide by 3 counter generate the timings for
  - ready synchronization, divide by 2 counter and CLK signal
- A divide by 2 counter cascaded with the divide by 3 provide divide by 6 output as PCLK

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Bus Buffering

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Buses

- Three buses required to interface memory and I/O:
  - Address bus , To provide the memory and I/O with the addresses and the port numbers
  - Data Bus , Transfers data to and from memory and I/O in the system
  - Control bus, To provide the control information to the memory and the I/o

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8086/88 Buses

- Control, Data and Address buses
- Data and Address buses are multiplexd once leave the 8086 labeled as ADDR/DATA
  - To save pins
  - Lower 16 bits of addresses are multiplexed on the data bus
  - To access the memory or port 8086 sends out lower 16 bits of address on data bus
  - Latches holds the address during the read / write operation and output on ALE signal

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Buses

- Demultiplexing is the technique of extracting the information form these multiplexed pins
- Why to demultiplex the pins?
  - Memory and port requires that address must remain valid throughout read and write operation
  - If not demultiplexed, address changes at the memory and I/O

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Buffered System

- If more than 10 unit load is attached to any bus pin, then the system should be buffered
- A fully buffered 8086 system requires
  - Demultiplexed address pins are buffered by three address latches
  - Data bus has two Octal bidirectional bus buffers
  - Control bus signals M/IO, RD and WR has a buffer

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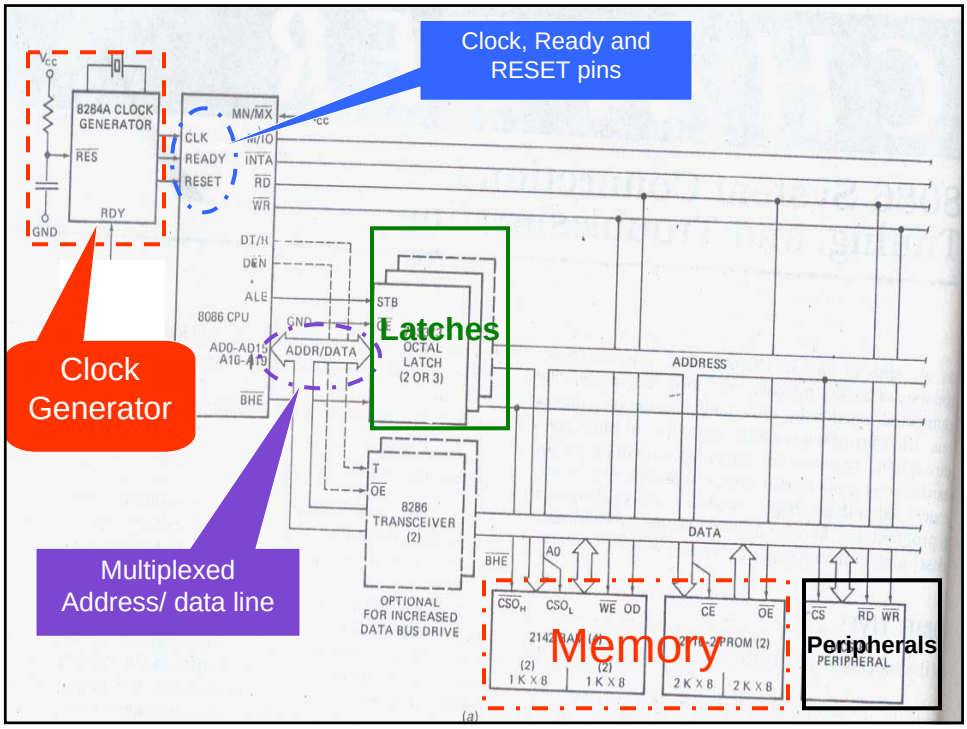

8286 - Transceiver

- Bidirectional three state buffer
  - Not req for smaller system
  - Req when more devices are added
- To ensure proper fast and speedy supply of current high speed drive buffers are used
- These are bi directional because
  - They send out and read in the data on the data bus
- These should have three state output:
  - so that data can be floated during a bus operation

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DT/R Signal

- Data Transmit and Receive DT/R' signal sets the direction in which the data will pass through the buffers
  - When DT/R' is asserted high the buffers will setup to transmit data from 8086 to ROM, RAM or port
  - When DT/R' is asserted low the buffers will setup to allow the data from ROM, RAM or port to 8086
- DEN' signal is asserted to enable the three state output on data bus buffers

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Basic 8086 system Timings

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Timing

- One clock cycle is called a “State”
  - Measured from falling edge of one clock pulse to the falling edge of next clock pulse
  - Time for a state is determined by the frequency of the clock signal
- Basic microprocessor operation is called a “ Machine Cycle”
  - Machine cycle consists of several states
- The time a microprocessor requires to fetch and execute an entire instruction is referred as “instruction cycle”
  - Consists of one or more machine cycle

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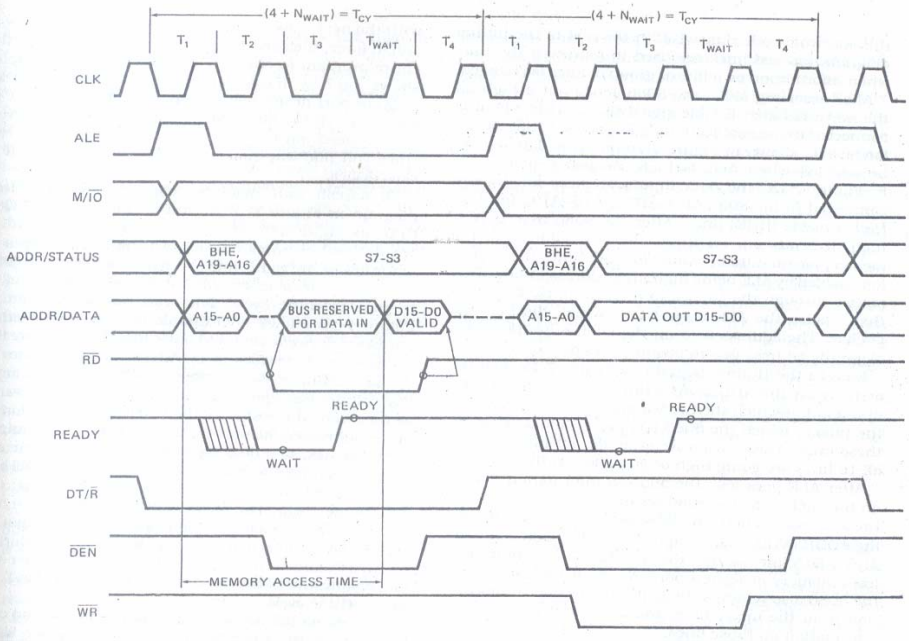
Basic 8086 Timings



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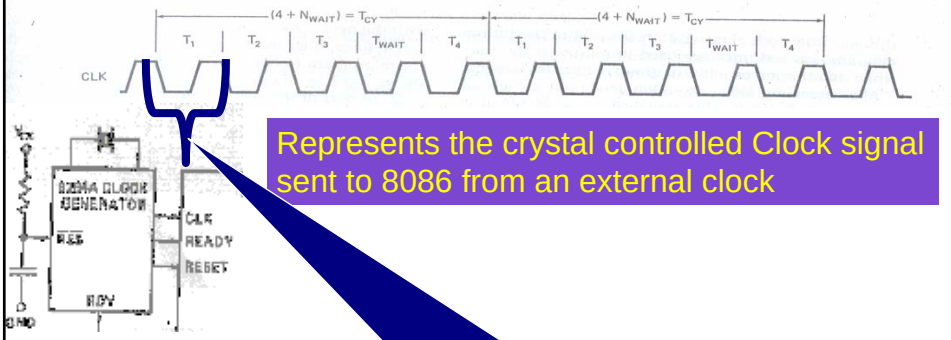
Clock Weaveform



Represents the crystal controlled Clock signal sent to 8086 from an external clock

The time of a state is determined by the frequency of clock signal

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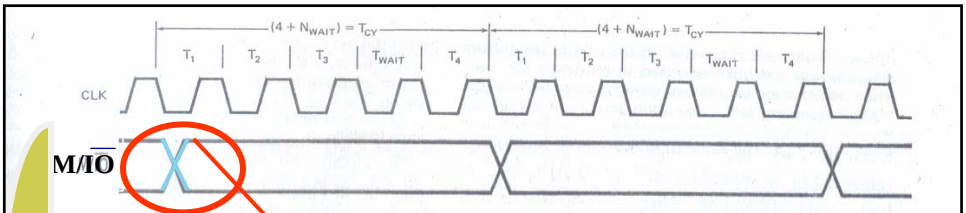

During T1 of read machine cycle the 8086 first asserts M/IO signal

- 8086 assert M/$\overline{IO}$ high to read from memory
- 8086 assert M/$\overline{IO}$ low to read from port

The cross indicates the time at which the signal become valid for this machine cycle.

Crossed waveform as signal may be going low or going high for a read cycle

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M/IO signal

- 8086 asserts M/IO
  - High if the read is from memory
  - Low if the read is from a port

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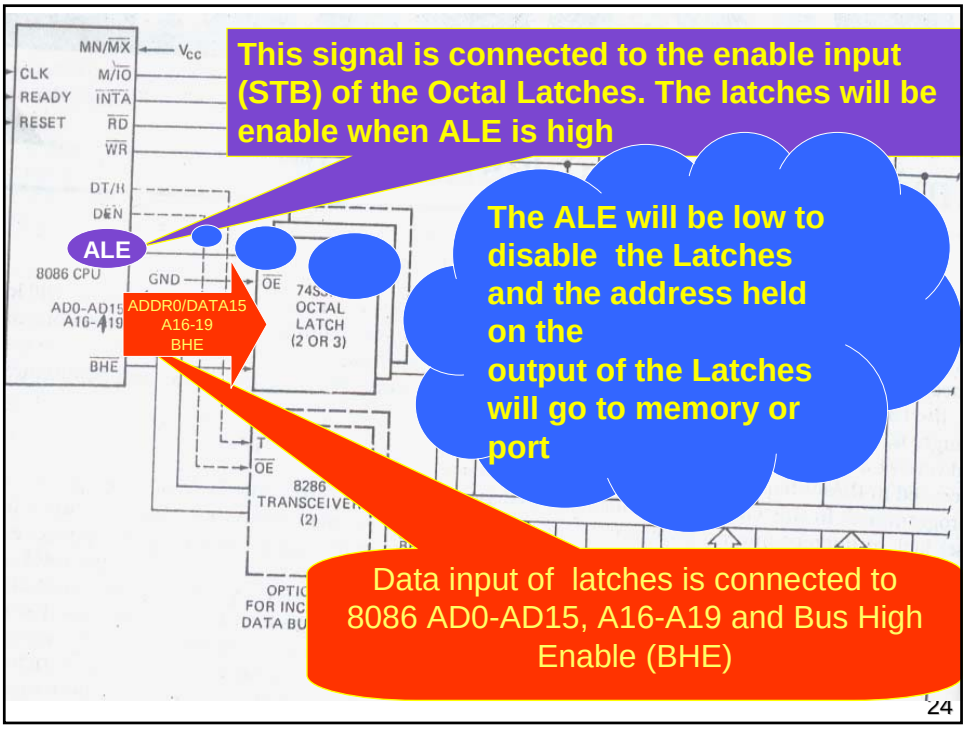

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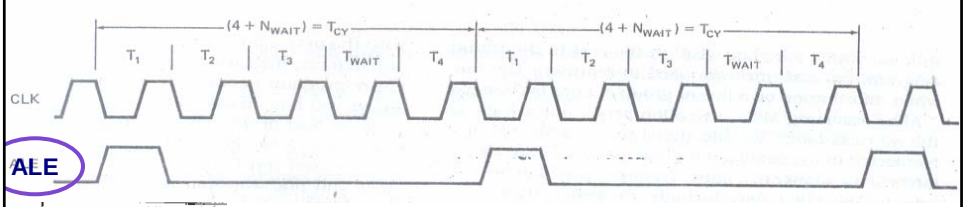

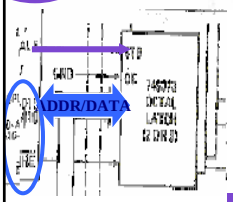

After asserting M/IO, 8086 sends out a high on Address Latch Enable Signal (ALE)

After asserting ALE high, 8086 sends out the address of the memory location for a read operation

since the ALE is high and Latches are enabled, the Address information will pass through the output

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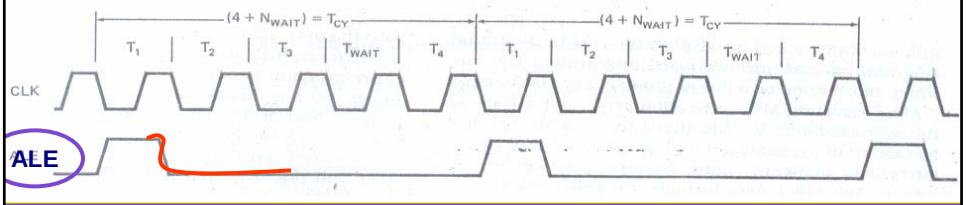

8086 then make the ALE output low, which disable the latch

The address held on the latch output will travel on the address bus to the memory or port

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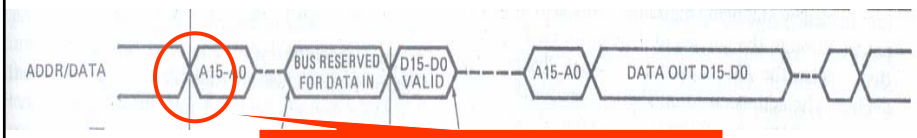
Activity on ADDR/DATA lines



Cross represents the time at which 8086 has placed a valid address

After ALE goes low
The address information is held on the latches
8086 will no Longer needs to send out the address.

8086 floats the AD0-AD15 lines so that these may be used for input data from memory or port

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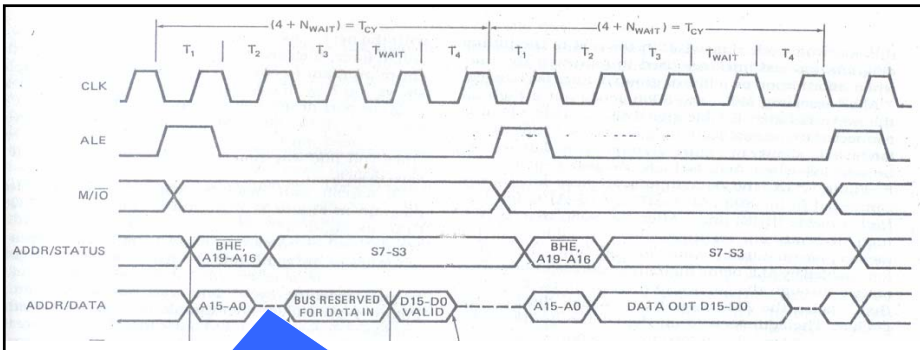

Dashed line shows the 8086 floating condition

8086 floats the AD0-AD15 lines so that these may be used for input data from memory or port

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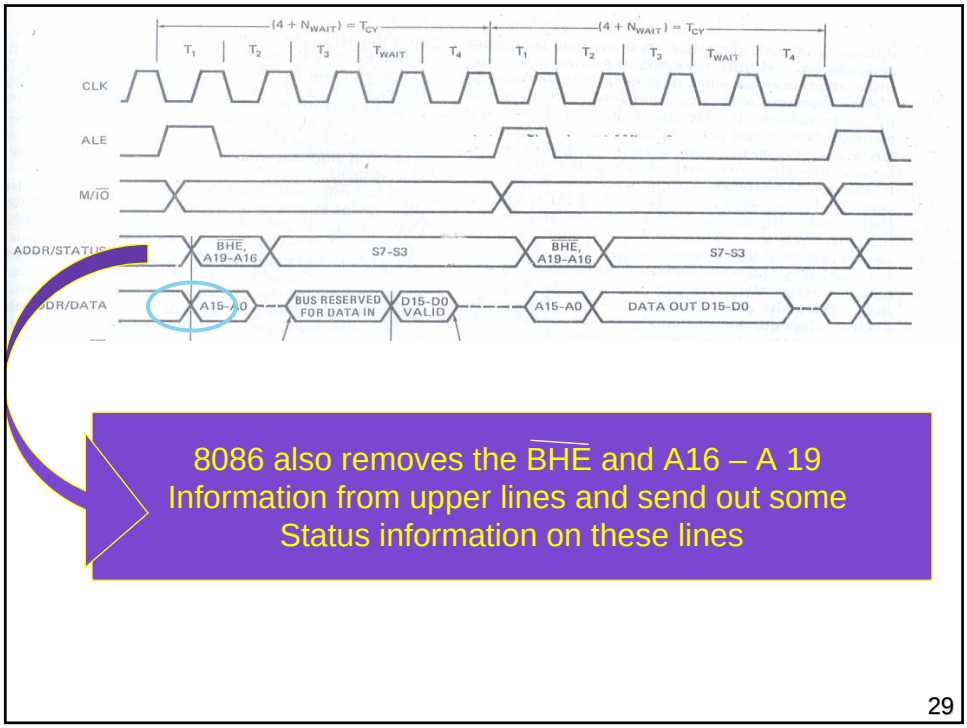
$(4 + N_{WAIT}) = T_{CY}$
$(4 + N_{WAIT}) = T_{CY}$
T_1 T_2 T_3 T_{WAIT} T_4 T_1 T_2 T_3 T_{WAIT} T_4
CLK
ALE
M/IO
ADDR/STATUS
BHE, A19-A16
S7-S3
BHE, A19-A16
S7-S3
ADDR/DATA
A15-A0
BUS RESERVED FOR DATA IN
D15-D0 VALID
A15-A0
DATA OUT D15-D0
8086 also removes the BHE and A16 – A 19 Information from upper lines and send out some Status information on these lines

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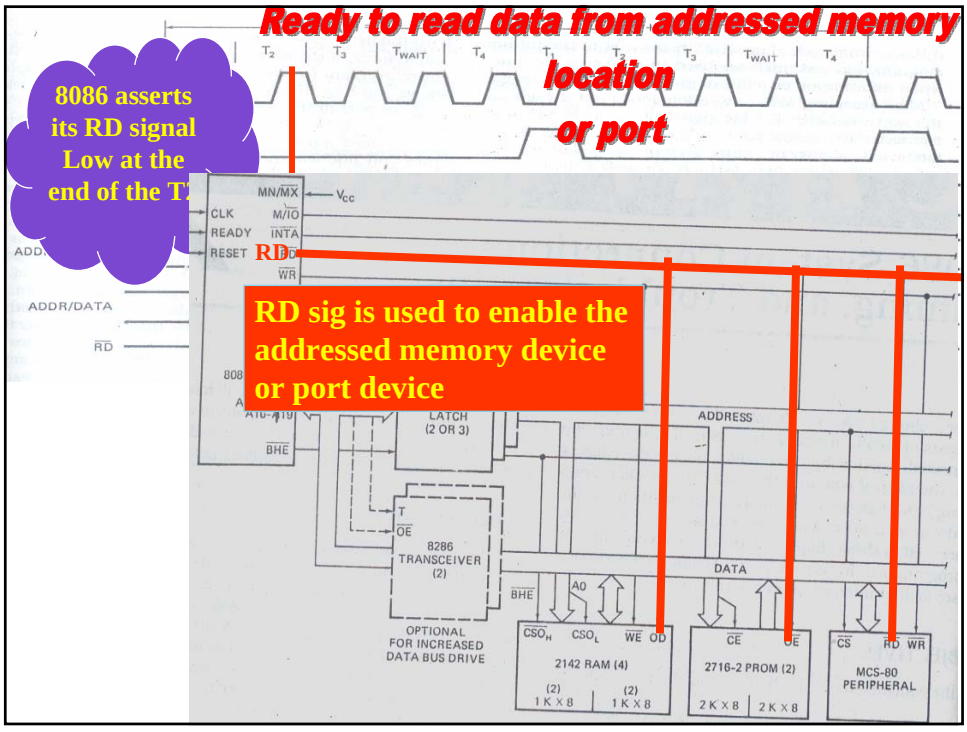
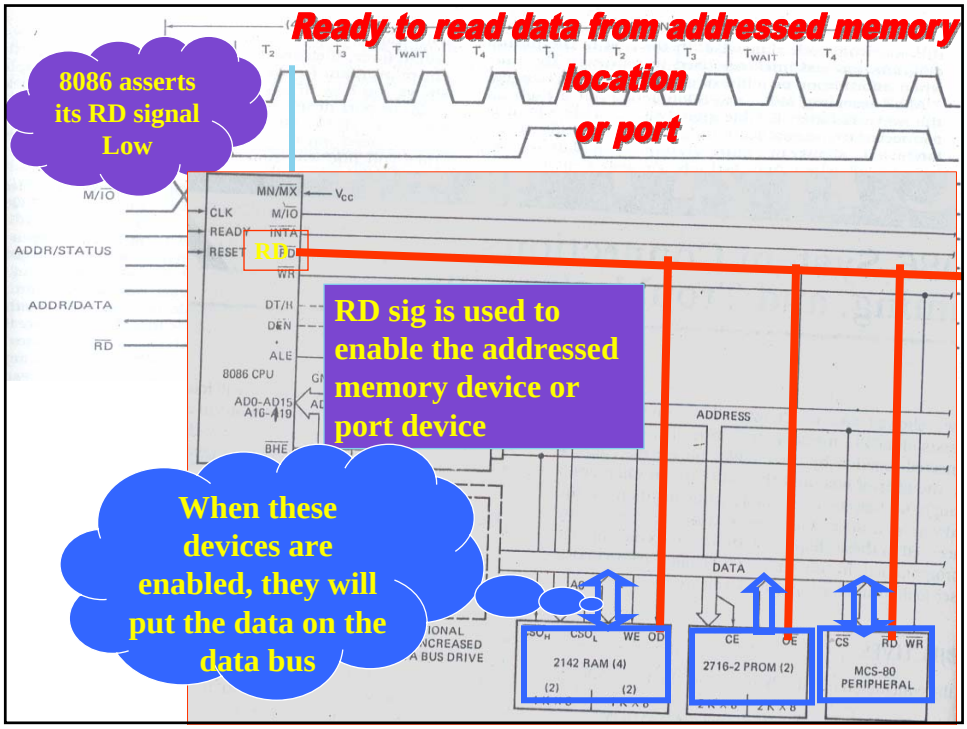
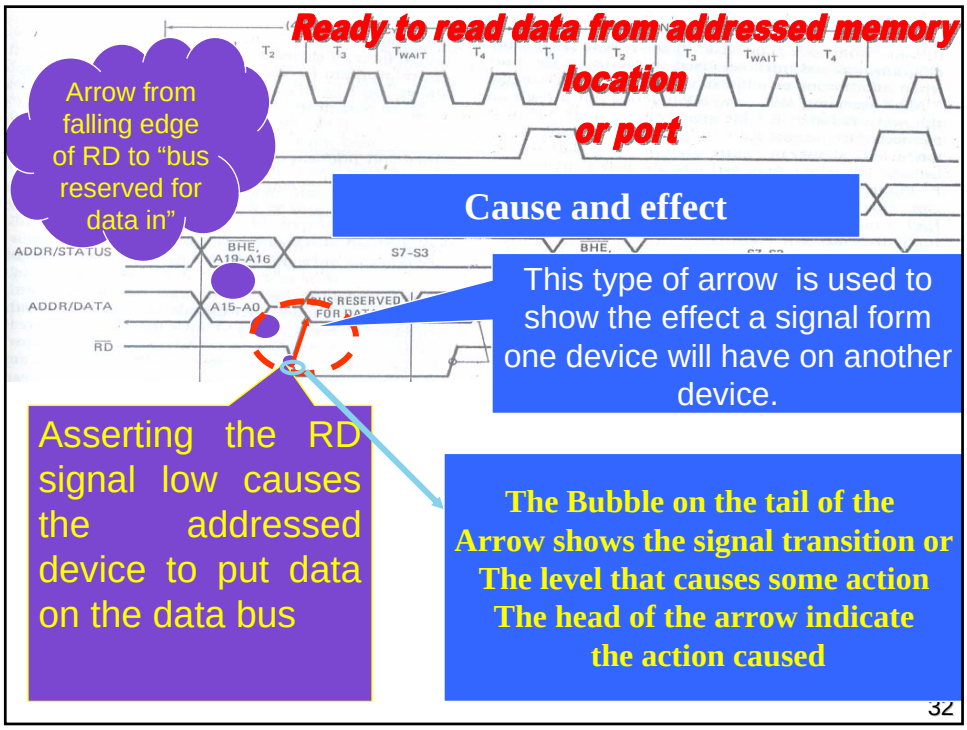

Ready to read data from addressed memory location or port
8086 asserts its RD signal Low at the end of the T
ADDR/DATA
RD
RD sig is used to enable the addressed memory device or port device
MN/MX
V_{CC}
CLK
M/IO
READY
INTA
RESET
WR
BHE
LATCH (2 OR 3)
ADDRESS
8286 TRANSCEIVER (2)
OPTIONAL FOR INCREASED DATA BUS DRIVE
DATA
A0
CSO_H CSO_L WE OD
2142 RAM (4)
(2) 1 K X 8
(2) 1 K X 8
CE OE
2716-2 PROM (2)
2 K X 8
2 K X 8
CS RD WR
MCS-80 PERIPHERAL


Ready to read data from addressed memory location or port
8086 asserts its RD signal Low
RD sig is used to enable the addressed memory device or port device
When these devices are enabled, they will put the data on the data bus
ADDR/STATUS
ADDR/DATA
RD
8086 CPU
ADDRESS
DATA
2142 RAM (4)
2716-2 PROM (2)
MCS-80 PERIPHERAL


Ready to read data from addressed memory location or port
Arrow from falling edge of RD to "bus reserved for data in"
Cause and effect
This type of arrow is used to show the effect a signal form one device will have on another device.
Asserting the RD signal low causes the addressed device to put data on the data bus
The Bubble on the tail of the Arrow shows the signal transition or The level that causes some action The head of the arrow indicate the action caused
ADDR/STATUS
ADDR/DATA
RD
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RD signal

- **RD signal is used to enable the addressed memory or port device**
- **RD signal low turns ON the addressed memory or port, which then output the desired data on the data bus**
- **To complete the cycle the 8086 brings the RD line high, that cause the addressed memory to floats its output on the data bus**

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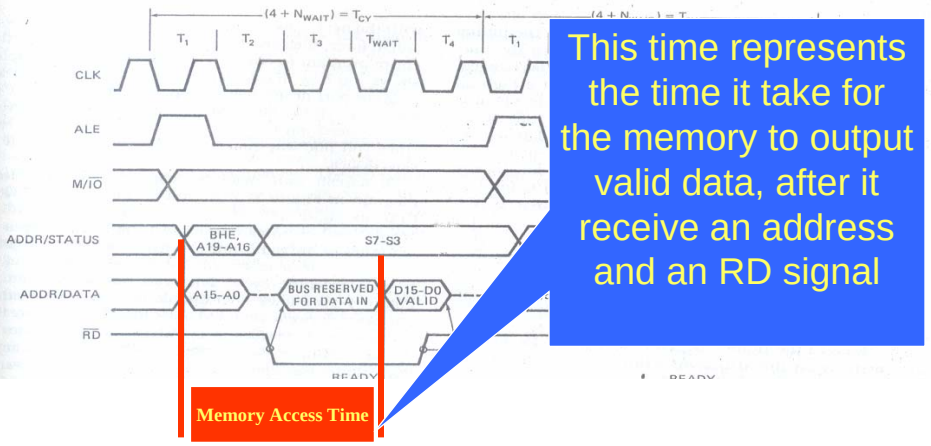
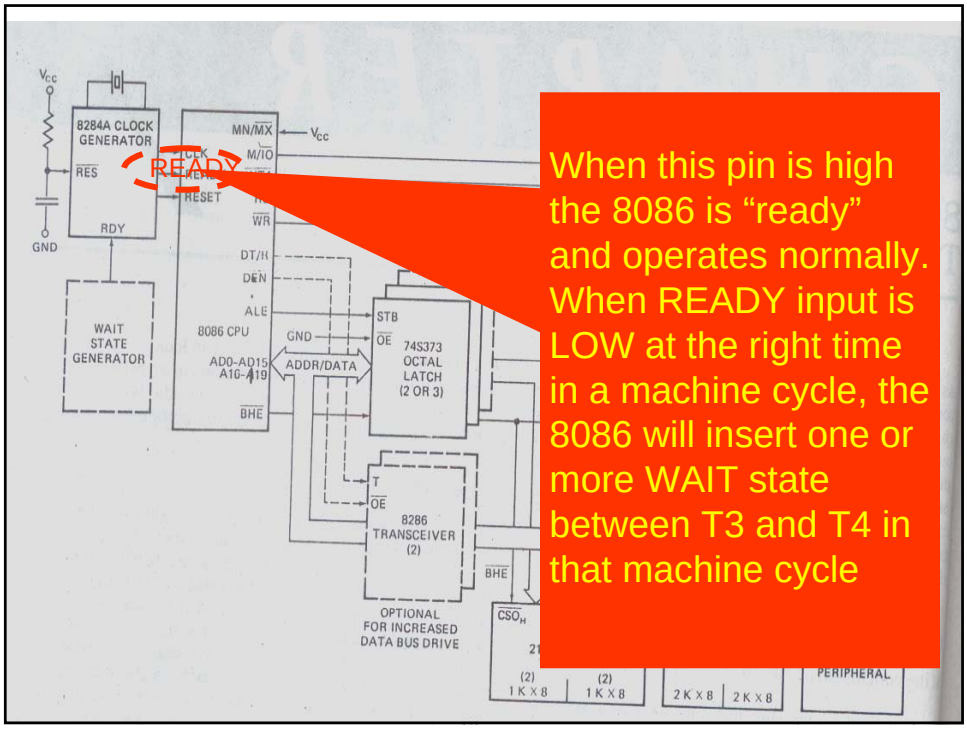
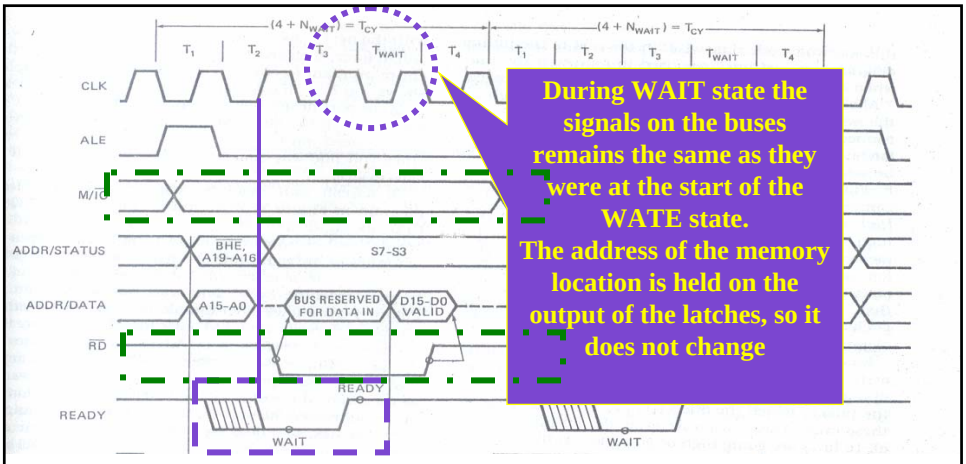


This time represents the time it take for the memory to output valid data, after it receive an address and an RD signal

If the access time for a memory device is too long, the memory will not have valid data on its output during a machine cycle, so 8086 will not receive it correctly and take the data as garbage, and go on to next machine cycle





The control bus signals, M/IO, RD remains the same during WAIT state

The memory or port will has at least one more clock cycle To get its data output

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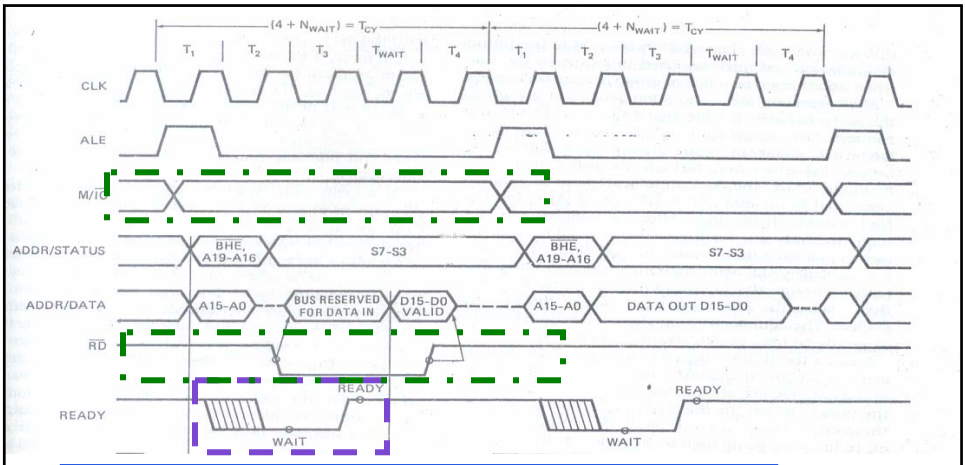

If , READY input is made high again during T3 or during the WAIT state then after one WATE state the 8086 will go on with the regular T4 machine cycle

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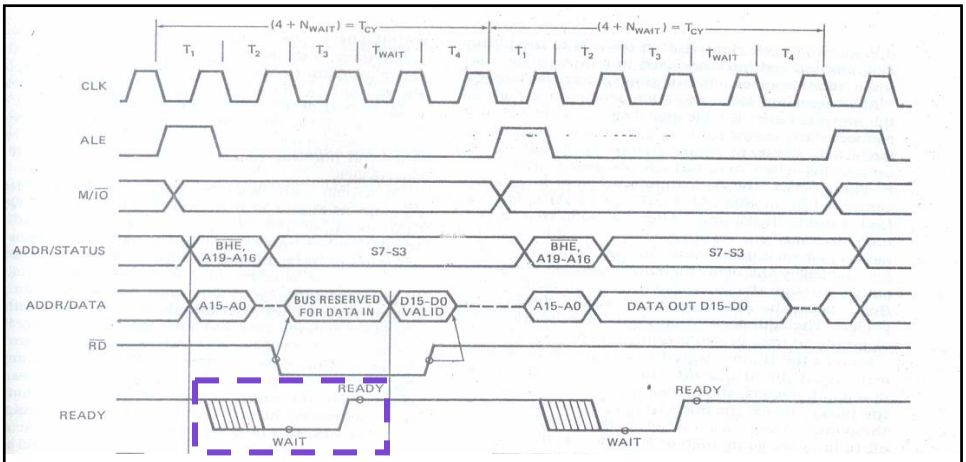

If , READY input is still low at the end of WATE state then 8086 will insert another WAIT state until the READY input Is made high again

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WAIT State

- Inserting the wait state freezes the action on the buses
- WAIT state give an extra clock cycle to the addressed device to put valid data
- WAIT state is inserted to accommodate the operation of slower devices (like ROM)
- NO WAIT state is inserted in a read machine cycle for reading data from a faster device (like RAM)

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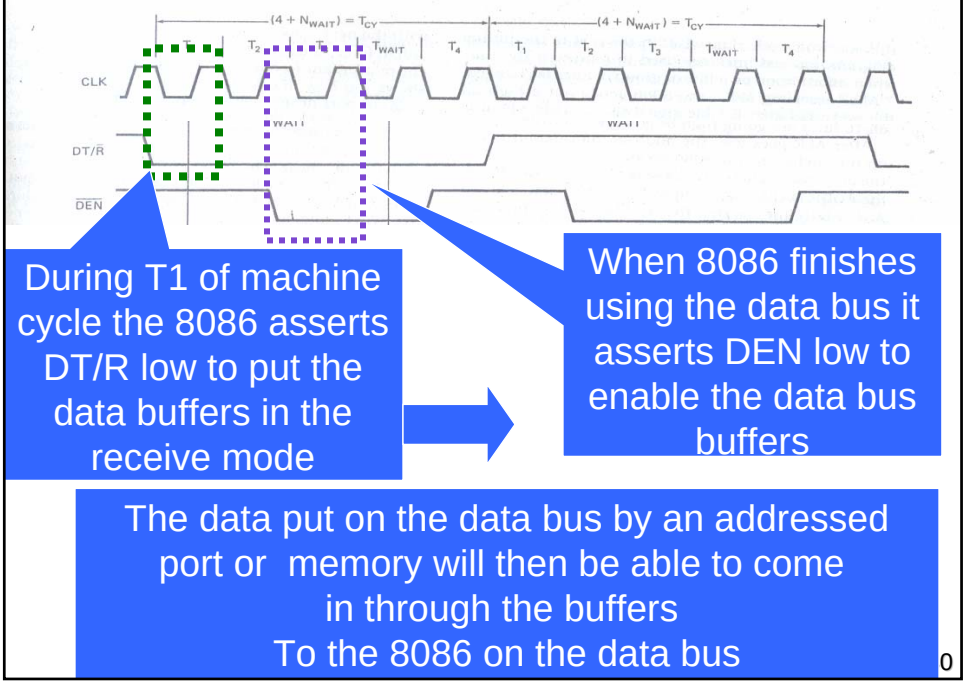

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DEN & DT/R Signals

- DEN signal Enable the buffers at the appropriate time in the machine cycle
- DT/R signal is connected to the buffers will set them for input during a read operation or set them for output during a write operation

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