Solution-Final Exam
BESE 15 (A)
COMPUTER ORGANIZATION AND ARCHITECTURE

Faculty Member: Dr. Hammad Afzal **Time:** 150 Mins
Max Marks: 50

Part 1 (10)

Answer: 1

False

Answer: 2

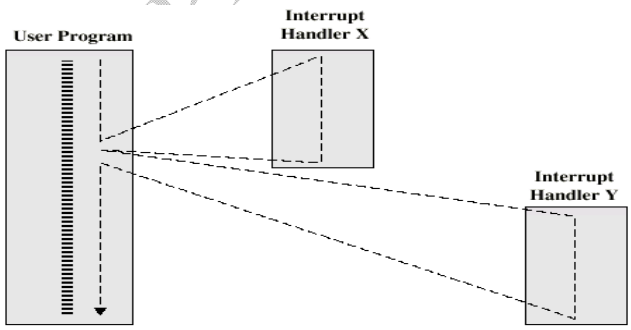
Two approaches that can be used to handle multiple interrupts are:

i. Disable Interrupts
ii. Define priorities

Disable interrupts (Sequential Handling of multiple interrupts)

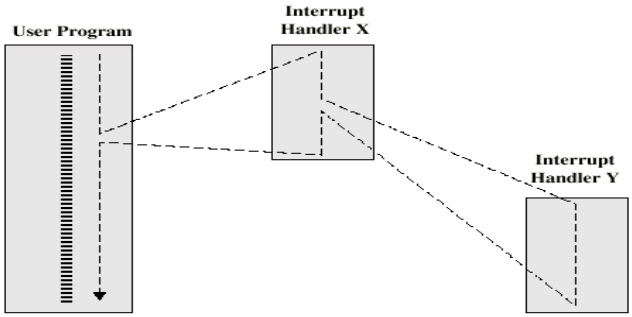
In this mode, processor will ignore further interrupts whilst processing one interrupt. Interrupts remain pending and are checked after first interrupt has been processed.

Interrupts are handled in sequence as they occur.



Define Priorities (Nested Interrupts)

In this mode, the low priority interrupts can be interrupted by higher priority interrupts. When higher priority interrupt has been processed, processor returns to previous interrupt



The main disadvantage of sequential handling is that, interrupts from other I/O module which require immediate response (e.g. processing of data) may be delayed that can result in data loss. For example, if an interrupt from printer is being handled, and there is an input data on communication module (Modem), processor will only handle the request from Modem only after finishing the processing of interrupt from Printer that may result in data loss. This shortcoming of sequential mode is catered for in Nested Interrupts.

Answer: 3

Program interrupt is generated by some condition that occurs as a result of an instruction execution.

Example conditions are:

Arithmetic overflow, Division by zero, attempt to execute an illegal machine instruction, or reference outside a user's allowed memory space.

Answer: 4

Some registers are required as part of the digital structure of a CPU; for example, the *instruction register*, the *memory address register*, the *memory data register*, and registers used to implement computer arithmetic. These are invisible registers – invisible in the sense that they cannot be directly accessed by the programmer – there are no instructions that operate directly or explicitly on these internal registers.

Visible registers are those that can be accessed by the programmer –the address and data register, and the status register. The program counter is not directly visible although it can be accessed indirectly. A visible register is part of its architecture.

Answer: 5

The devices connected to buses have a wide variety of characteristics. At one end we have the keyboard and mouse; at the other end of the spectrum we have high-speed memory. No single bus can handle such a range of devices economically.

Typical systems have a high-speed bus that operates at the highest possible rate to link the processor and memory. They may have a slower bus that links the processor to peripherals such as SCSI cards.

Part 2 (17)

Answer: 6

Main memory is used to hold data and programs and to hold intermediate values during a calculation.

(Part of) Operating System is also held in Main Memory, however, at this level, we would rather not make distinction between an OS and a normal program that comprises of data and instructions.

Answer: 7

Random access

An element in a random access memory can be accessed in (approximately) the same time it takes to access any other element in the memory. More importantly, random access implies that you do not have to read other elements before you can access the one you want.

Non-volatile

A memory is non-volatile if it retains its data when the power supply is removed. Typically, magnetic memory and flash memory is non-volatile.

Access time

The access time of a memory is the time taken to locate an element and read from data it.

EPROM

EPROM is erasable and programmable read only memory. It is a form of read-mostly memory that can be programmed with data occasionally (for example, during an upgrade). It is non-volatile ROM and the data is retained when the power is removed. Data can be erased by exposing the memory to UV light.

Answer: 8

8Mbytes/sec

Answer: 9

RAM means *random access memory* which means that it takes the same time to access any cell chosen at random. Random access memory contrasts, with sequential access memory (e.g. disk) where the access time depends on the physical location of the data – because you have to access the memory sequentially until you locate what you want.

ROM is read only memory and indicates that the memory can be read from (once its contents have been written for the first time) but not written to. The opposite of ROM is read/write memory.

Thus we have two pairs of contrasting definitions (or opposites) RAM and sequential memory, and ROM and read/write memory.

For historical reasons, RAM has been contrasted with ROM (i.e., RAM is used to indicate read/write rather than random access). This is, of course, nonsense! Unfortunately, the definition has stuck and Ram means both read/write and random access depending on the context. Consequently, ROM is also RAM because it is random access (the only aspect of ROM that is included in the definition is read-only). However, RAM is not ROM because RAM either means random access or read/write.

Answer: 10

Flash memory is a read-mostly form of non-volatile semiconductor memory that can be written to (relatively slowly) and accessed rapidly.

Flash memory is part of the EPROM and EEPROM group of semiconductor non-volatile RAM. The storage principle is the injection of a charge on an insulated electrode. This charge allows or prevents the passage of electrons through a narrow semiconductor channel. The charge is injected during the writing process and can be removed electronically to erase data.

Flash memory is used to store system software such as a computer's BIOS when the software is required immediately on power-up (independently of hard disks or CD ROMs). Moreover, the BIOS is not normally changed but it can be updated to reflect product improvements and enhancements.

Flash memory is closer to EEPROM, as data can be erased and written on it easily, whereas in PROM, data can be written only once by user using a special PROM programming device and then it can only be read.

Answer: 11

CD-ROM

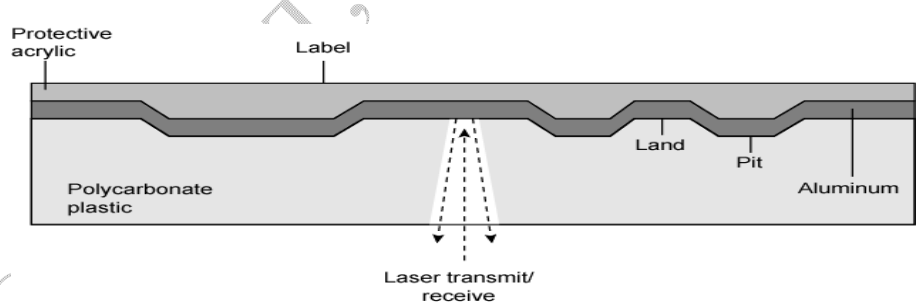
The CD-ROM is polycarbonate coated with highly reflective coat, usually aluminium.

Writing

Data is stored as pits and is written using high intensity Laser. Pits and Lands represent 1s and 0s or vice versa. Usually dies are made which are then used to imprint on other disks.

Read

Data is read by reflecting laser whose intensity is varied with smooth *lands* and pits.



CD-RW

Write and Read

The material used in CD-RW has property of Phase Change (From Crystalline to Amorphous). Two phase states have different reflectivity, i.e. in crystalline form, the reflected intensity of laser is more as compared to that in amorphous form, Therefore 1s and 0s are stored using the two phase states.

Answer: 12

5 bits of Code

Calculations are skipped only here. Students are expected to clearly demonstrate the calculations to support their answer, using formula

$$2^K-1<=M+K$$

Answer: 13

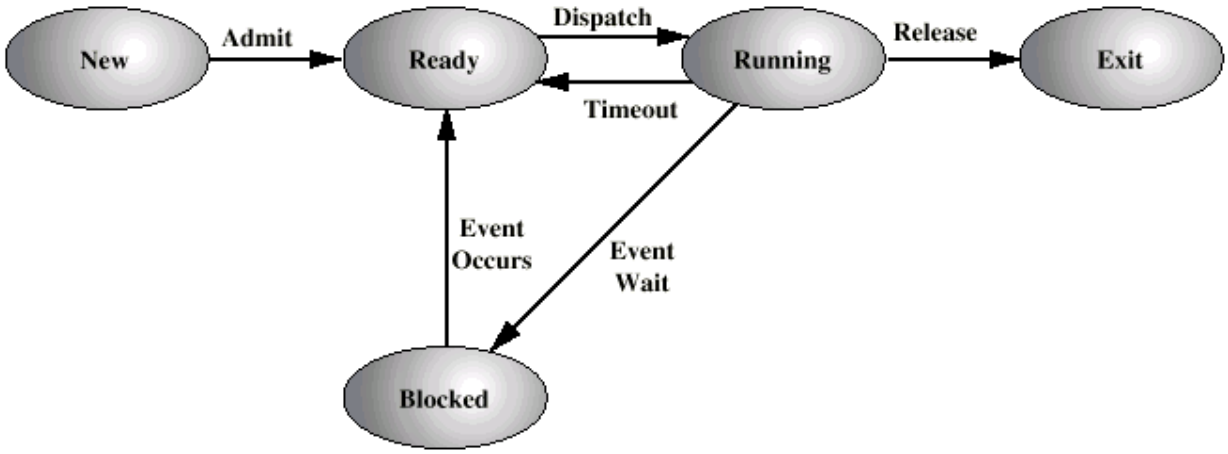
RPS is a technique/method whereby the processor sense (look) for a specified sector, and then receives the sector number required to access the record. The performance of system can be improved (increasing speed) by freeing the I/O Channel after Seek Command. The I/O channel and processor can do some other task meanwhile I/O Channel reconnects once the data to be read is under the head.

RPS Miss:

If the data to be read has reached under the head, but control unit or I/O Channel (that was released after Seek Command to improve the efficiency) is busy, then RPS Miss occurs. In this case, another rotation of disk will take place so that I/O Channel or Control Unit can be freed from other tasks meanwhile.

Part 3 (10)

Answer: 14



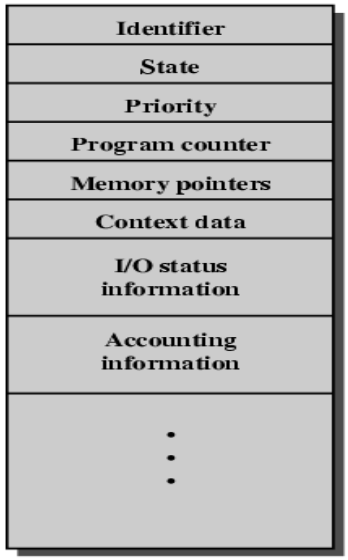
Running: Process is being executed by Processor.

Ready: Process is ready to be executed by processor and is waiting in Short-Term Queue.

Blocked: Process is in Intermediate Queue, waiting for some external event (for example, I/O operation).

Answer: 15

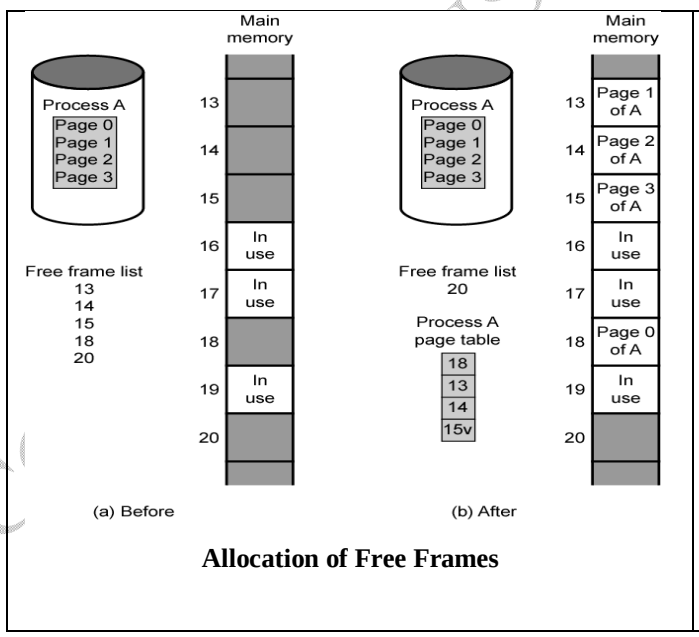
A process control block is the information the operating system holds on each process. Essentially, a process control block must contain at least enough information for a process to be resumed. Consequently, it must contain the process's program counter (and the stack pointer if the process maintains one), the process's working registers, and the process's status word (it's C,Z,V,N flags). A process control block may also contain operating system information such as the state of the process, its priority, the next process in a linked list of processes, and so on.



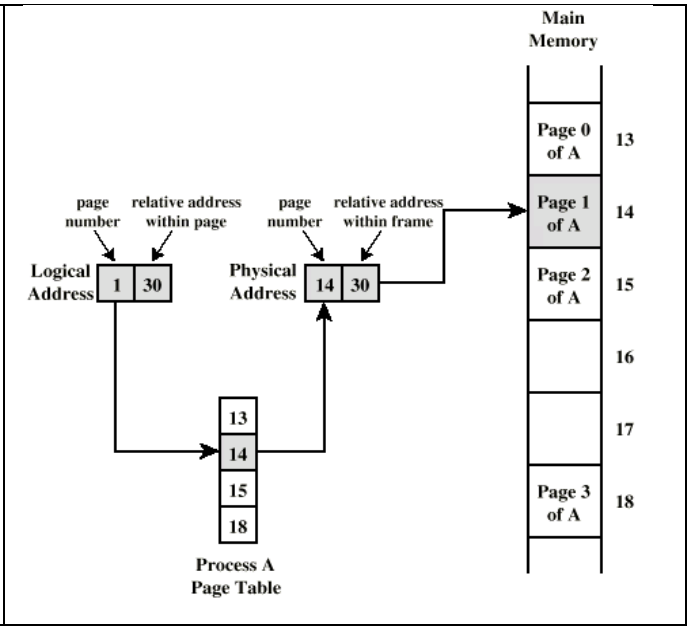
PCB Diagram

Answer: 16

A physical address is the actual address of a memory element within the computer's memory. The size of a computer's physical memory space is the size of the memory implemented by the computer. Physical address space is the address space made up of all the memory locations that can be accessed by the computer. In a simple computer (i.e., without memory management) the logical and physical address space are the same. In a computer with a modern operating system and a memory management unit, the operating system controls the allocation of logical address space to processes and the memory management unit maps logical address space onto the physical address space. The concept of Physical and Logical address can be elaborated by the following diagrams.



Allocation of Free Frames



Answer: 17

Virtual memory allows programs and data to reside partially on disk and to be swapped in when needed. When the computer's physical memory is full, it is necessary to swap data out to disk and bring in new data. The operating system and memory management unit do this together. A similar process takes place when the cache memory is full – old data has to be swapped out to make way for new data.

Answer: 18

Page: 1. Processes are split into equal sized small chunks called Pages.

2. A partition (proportion) of secondary memory that is transferred to main memory as a block;

Frame: A partition of RAM into which pages are loaded;

Page fault: Reference to a memory address that is not contained in RAM

Part 4 (13)

Answer: 19

Spatial locality refers to the tendency of execution to involve a number of memory locations that are clustered. **Temporal locality** refers to the tendency for a processor to access memory locations that have been used recently.

Answer: 20

Assumptions

- 64KB of cache size, and one block of memory contains 4 words, each word comprising of a single byte.

Direct Mapping

- No of lines in Cache: 64K/4=16K
- 2^{14}=16k

Therefore,

- Number of bits required for Word = 2 since 2^2=4 distinct Words can be addressed.
- Number of bits required for Line = 14 since 2^{14}=16k distinct Lines can be addressed.
- Number of bits required for Tag = 24-2-14=8

For 666666

0110	0110	0110	0110	0110	0110

0110 0110	0001 1001 1001 1001	10

66h	1999h	2h

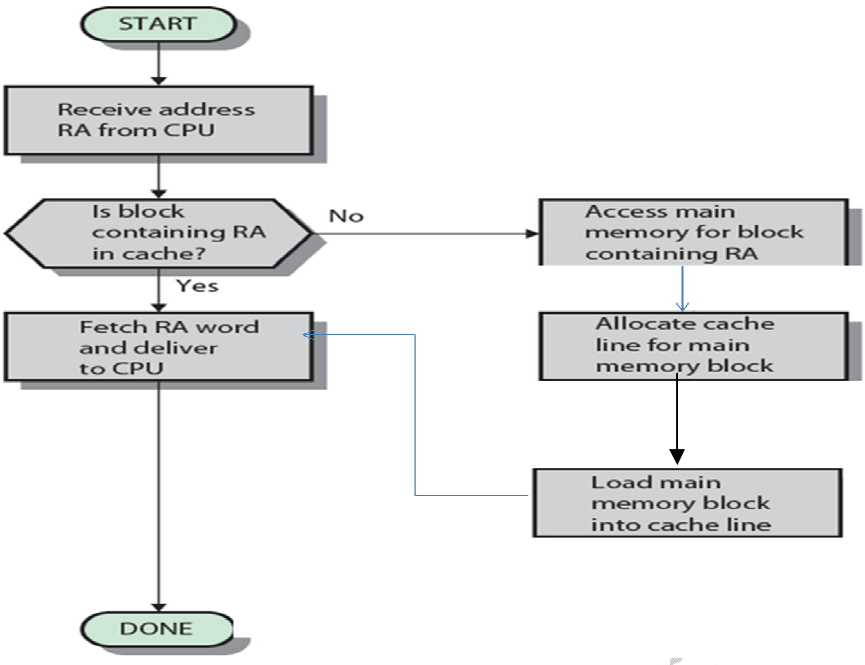
For BBBBBB

1011	1011	1011	1011	1011	1011

1011 1011	0010 1110 1110 1110	11

BBh	2EEEh	3h

Answer: 21



Answer: 22

Write Policy is required for Cache as more than one device may have access to memory. For example, an I/O module. If word is altered only in cache, corresponding memory word is invalid vice versa.

In Write Through Policy, all writes go to main memory as well as cache. Multiple CPUs can monitor main memory traffic to keep local (to CPU) cache up to date. However, there are some disadvantages as well in this technique, for example, lots of memory traffic as memory is constantly updated as there are any changes in Cache.

Answer: 23

The classification between Unified and Split Cache is based on the principle of "One cache for data and instructions or two, one for data and one for instructions". In unified Cache, Data and Instruction are on same Cache, whereas, in Split Cache, Data is stored on one cache, and Instructions are stored in other Cache.

Advantages of unified cache: In this mode, only one cache is to be designed and implemented. Load of instruction and data fetch is automatically balanced using the algorithms (based on Spatial and Temporal Locality)

Advantages of split cache: This mode eliminates cache contention between instruction fetch/decode unit and execution unit. Performance is significantly improved in pipelining.