

Solution of Mid Term Exams

BESE 15 (A)

Computer Organization and Architecture

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Part 1 (5 Marks)

1. False. Vacuum tubes were used in First Generation. (1)
2. Von-Neumann architecture. (1)
3. Instruction Register: (2)

The register that holds the value of currently executing instruction after it is fetched from the memory.

Program Counter.

The register that holds the value of the memory location from where the next instruction to be executed is fetched.

4. The law is named after Intel co-founder Gordon E. Moore, who described the trend in his research paper in 1965. The paper noted that number of components in integrated circuits (transistors in particular) had doubled every year from the invention of the integrated circuit in 1958 until 1965 and predicted that the trend would continue "for at least ten years. (1)

Part 2 (15 Marks)

1. False. It is part of operating system (1)
2. Processor grants authority to an I/O module to read and write to memory, so that I/O memory transfer can occur without tying up processor. During such transfer, I/O module issues read or write commands to memory, relieving the processor of responsibility for exchange. This is called **Direct Memory Access (DMA)** (2)
3. Interrupt: (3)

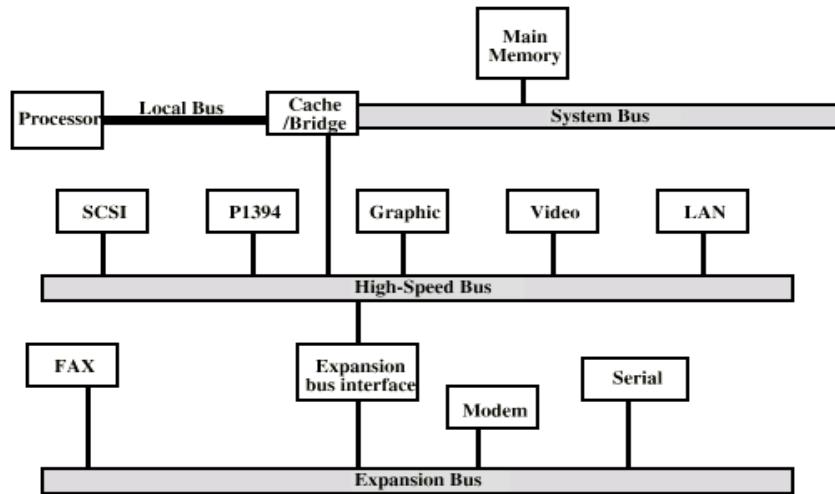
Interrupt is mechanism by which other modules (e.g. I/O, memory) may interrupt normal sequence of processing.

- i. Program
- ii. Timer
- iii. I/O
- iv. Hardware Failure

4.

- a) $2^{24}=16\text{Mbytes}$ (1)
- b) PC at least 24 bits (1)
- c) IR at most 32 bits (1)

5. Multi-bus architecture: (3)



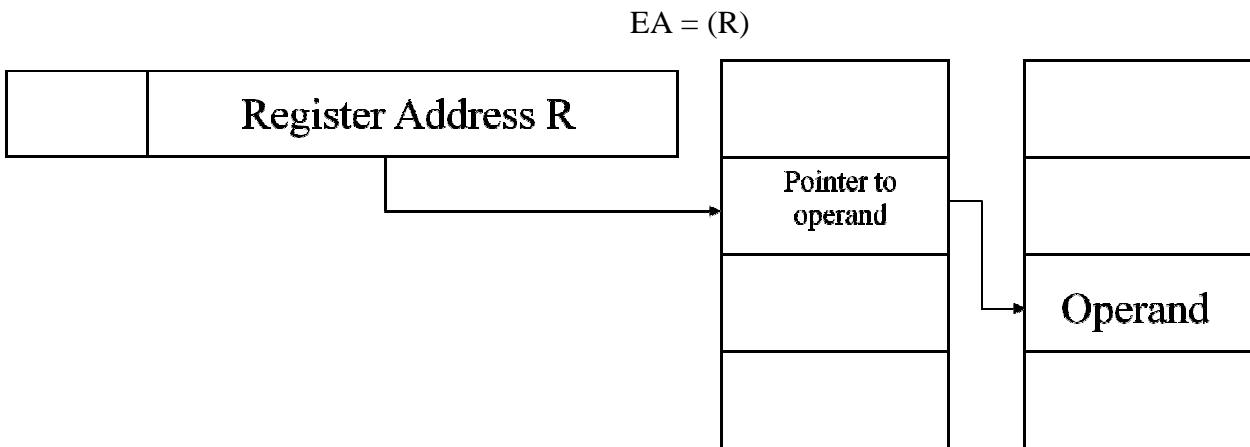
6. If more than two modules (I/O, Processor etc) control the bus at same time, their signals will overlap and become garbled. Hence **Arbitration** is required that makes sure that only one module controls the bus at one time.

- a. Centralized Arbitration (a dedicated device or CPU controls arbitration).
- a) Distributed Arbitration (each module can claim the bus and has chip logic in it) (1+2)

Part 3 (10 Marks)

1. $2^4=16$ (1)
2. Branch to memory location X if result (of most recently executed instruction) is positive. (1)
3.
 - a) 20
 - b) 40
 - c) 60
 - d) 70
4. (2)

- a) The address in instruction points to one of the registers R, and the contents of R then point to the memory cell that contains the operand. Register Indirect Addressing Mode is similar to the Indirect Addressing Mode.



(2)

b) **Advantages and Disadvantages of**

Register Indirect Addressing Mode vs Register Direct Addressing Mode

- As the address in instruction points to the register that contains the effective address of operand, therefore, the smaller size of instruction does not limit the addressable locations where operand can be stored. The number of addressable memory locations will be equal to 2^k where k is the size of register.
- One memory access is involved; therefore it is slower than Register Direct Addressing Mode.
- Register direct mode has very limited address space due to fewer numbers of registers that can hold the operand.

Advantages and Disadvantages of

Register Indirect Addressing Mode vs Indirect Addressing Mode

- There are much fewer numbers of registers as compared to the addressable memory locations, therefore, less space is required to store instruction (Instruction size is small).
- One fewer memory access than indirect addressing, hence faster execution.