Lab # 1: Simulation of Processor Fetch & Execute Cycle

OBJECTIVE

The objective of this lab is to simulate processor fetch & execute cycle without interrupts.

BACKGROUND

A program consists of a set of instructions stored in memory. Processor reads (fetches) instructions from memory and executes each instruction one by one. The basic instruction cycle is shown below:

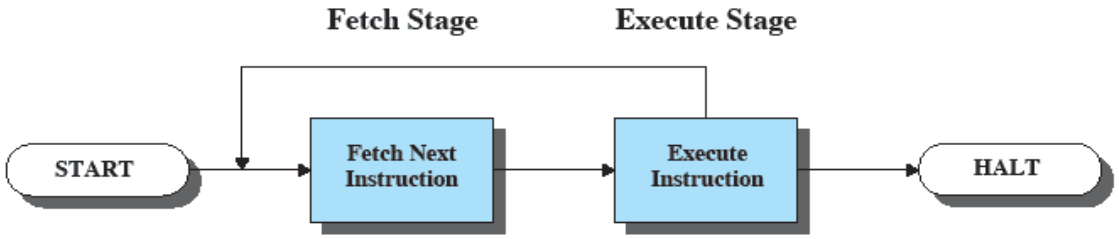

Figure 1.2 Basic Instruction Cycle

Main steps of basic instruction cycle are given below:

1. Load the address of first instruction to be executed in Program Counter Register (PC).
2. Fetch the instruction from the address specified by PC into the Memory Address Register (MAR).
3. Increment PC by 1.
4. Load the instruction from the address given by MAR into the Memory Data Register (MDR).
5. Load the instruction from MDR into Instruction Register (IR).
6. Decode the instruction.
7. Execute the instruction.
8. Go to step 1.

TASK

Simulate the processor fetch-execute cycle for following program instructions:

Address	Contents	Decoded Operation
000	00035	
001	00040	
002		
003	0001	Load the value (00035) from address 000
004	0101	Add 5 to the value
005	0010	Store the result at address 002

You can simulate this task in C++ or C#. As an output, show the status of CPU registers at each step of the fetch & execute instruction cycle.

For reference, consult following websites:

1. http://homepages.feis.herts.ac.uk/~msc_ice/fe2/#
2. http://homepages.ius.edu/rwisman/c335/html/hw1.htm

Important Note: Copied code will be given no credit.