Thin-Film Capacitor, MOSFET, and Resistor Fabrication & Integration

1. Introduction to 741 Op Amp:

Working Theory:

The 741 Op Amp is a differential amplifier, meaning it amplifies the voltage difference between two input signals while rejecting any common-mode noise. This makes it ideal for clean and accurate signal processing. Internally, the Op Amp has multiple stages working together: the input differential amplifier handles the initial signal, while the intermediate gain and output stages boost the signal and prepare it for driving various loads. A compensation capacitor is included to stabilize the Op Amp's performance and prevent it from oscillating at higher frequencies. Its internal circuitry is optimized for linear operation across frequencies up to around 100 kHz.

One of the key advantages of the 741 is that it can handle both AC and DC signals thanks to its direct-coupled internal stages. The open-loop gain of the Op Amp is extremely high (up to 200,000), but in practice, we usually add external feedback to control the gain and tailor it to specific applications. While it operates linearly within its supply voltage limits, it's important to ensure the output doesn't hit saturation or cut-off regions, as this would distort the signal.

Applications:

Signal Amplification: The 741 can provide linear amplification with minimal distortion.

Active Filters: It is reliable for designing low-pass, high-pass, and band-pass filters. These circuits are common in communication systems and audio processing.

Waveform Generators: The 741 can be used in circuits to generate sine, triangle, or square waves, which makes it useful for oscillators and timing circuits.

Analog Computation: It is often used to build circuits that perform mathematical functions like addition, subtraction, integration, and differentiation, which are useful in control systems and analog computing.

Comparators: Although not as fast as dedicated comparators, the 741 can still be used for applications like threshold detection or zero-crossing.

2. Background of Si-MOSFET:

What is Si-MOSFET:

Si-MOSFET is a Silicon Metal-Oxide Semiconductor Field Effect Transistor. The “Si” indicates that the substrate or semiconductor material is made of Silicon. Two examples of Si-MOSFETs are NMOS and PMOS transistors. Since the two types of transistors are similar but functionally opposite, we only really need to understand one to understand the other. NMOS transistors have a substrate material that is made of Silicon doped with a group III element, most commonly Boron. Two N-wells form the Source and Drain regions, while the Gate is made either of a metal material or polysilicon deposited above an insulating layer of Silicon Dioxide (SiO_2). When a voltage is applied to the Gate, an electric field is formed between the electrode of the Gate and the substrate, hence the “Field Effect.” These transistors can either be the “enhancement” type or “depletion” type with the enhancement type being the most

common. The two modes of operation refer to how the transistor behaves before a voltage is applied between the Gate and Source, where the enhancement type is normally off while the depletion type is normally on.

Working Principle:

With the enhancement type of NMOS transistors, when a positive voltage V_{DS} (that is the Drain is at a higher potential than the Source, as the Source is connected to the substrate terminal (or the Body) which is tied to ground) is applied, no current will flow until a positive voltage is applied at the Gate. In this scenario, the transistor is said to be in “cutoff.” When a positive voltage is applied at the Gate terminal, holes will collect on the Gate electrode and repel the holes in the p-type substrate beneath the Gate. At the same time, free electrons are attracted to and collect at the interface, creating a channel between the Source and Drain. Once the voltage applied at the Gate reaches a threshold voltage, current will begin to flow in the induced n-channel. As the V_{DS} voltage is increased (with the Gate voltage held constant), the resistance in the channel decreases while the current increases proportionally. This is called the “Triode,” “Ohmic,” or “Linear” region in which the MOSFET behaves as a voltage-controlled resistance. Increasing V_{DS} beyond this point will expand the depletion region between the N-well and p-type substrate near the Drain which narrows the channel until the channel is pinched off, in which case, the MOSFET enters the saturation region. The amount of current flowing in the channel will essentially be held constant; increasing V_{DS} will have no effect on the current. To increase the saturation current, the Gate voltage must be increased.

The depletion type of NMOS transistors are opposite to the enhancement type. The n-channel is already established and current will flow between the Drain and Source when V_{DS} is applied even though no Gate voltage has been applied (it is normally on). Applying a negative voltage to the Gate shrinks the channel which then turns the transistor off.

3. Fabrication Process of Si-MOSFET:

Process Diagram:

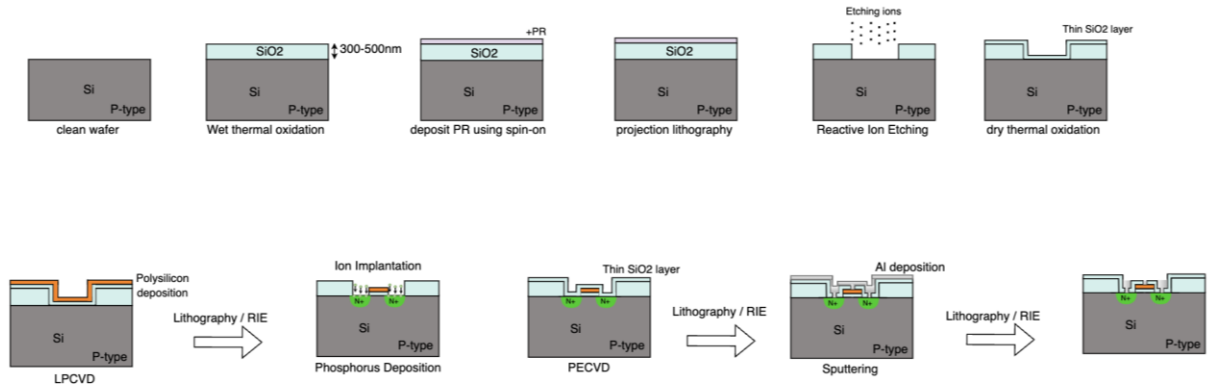


Figure: Fabrication Process Diagram of Si-MOSFET

Process Technologies:

Substrate Preparation: Lightly doped p-type silicon wafer. The reason for choosing the p-type substrate is for forming n-channel MOSFETs, where the channel formed by inversion requires a p-type base. To ensure a pristine surface, the wafer undergoes

RCA cleaning, a multi-step process designed to remove organic and metallic contaminants. The SC-1 cleaning stage uses a solution of DI water, hydrogen peroxide, and ammonium hydroxide to oxidize and lift organic particles from the surface, followed by an HF dip to remove the native oxide layer. This ensures that subsequent layers are deposited on an uncontaminated silicon surface. SC-2 cleaning employs hydrochloric acid, hydrogen peroxide, and DI water to eliminate metallic residues while passivating the silicon surface to prevent recontamination. After cleaning, Chemical Mechanical Polishing (CMP) is performed to planarize the wafer, creating a smooth surface that enhances photolithography accuracy and ensures uniform deposition during the subsequent steps.

Field Oxide Formation: This process is done by Thermal Oxidation around 1000-1100℃. The purpose of this process is to grow a thick (~300-500 nm) SiO_2 layer for isolating devices. For this process, we chose the wet thermal oxidation process for having faster and thicker oxide growth. This oxidation process produces dense, uniform oxide with good electric insulation and better oxide quality than deposited oxides. The SiO_2 layer acts as a shield, protecting the whole substrate from any damage.

Photoresist and Photolithography: Photoresist is light sensitive and acid-resistant inorganic polymer and its properties change on exposure to UV light. In this case, we are using the positive photoresist which becomes soluble in a developer solution when exposed to UV light. We chose positive photoresist because it has better resolution with small features. This process includes coating the wafer with the photoresist, exposing it to UV light and developing the pattern. This process is for getting high resolution patterning down to nanometer scale and for defining the transistor layer accurately. We

choose the ‘Projection Lithography’ process which is known as ‘Stepper’ too. Because it is capable of resolving the feature sizes down to 100 nm and below, it is a non-contact method that means the mask does not touch the wafer, avoiding damage and contamination. It has better alignment accuracy, reduces overlay errors between layers (gate, source, drain, contacts).

Etching (Oxide Patterning): Silicon Dioxide (SiO_2) grown by the thermal oxidation must be patterned to define active areas, gate regions, for that we need to do etching. We prefer to choose the Reactive Ion Etching (RIE), a type of dry, plasma-assisted etching. We are not using the wet etching because it uses HF, it has poor anisotropic behavior causing undercutting which won’t be suitable for fine features. For Etch chemistry we are using CF_4 ,

$$CF_4 + e^- \rightarrow CF_3 + F + e^-$$

$$SiO_2 + 4F \rightarrow SiF_4(gas) + O_2$$

So here we are getting the SiF_4 (Silicon Tetrafluoride) as a byproduct which is volatile meaning it evaporates and gets pumped away in the chamber. This is important for clean etching without residue. While doing etching we need to consider the fact of Etch profile which refers to the shape of the sidewalls after etching. Since we are doing the RIE, we aim for an anisotropic (vertical) etch profile. This prevents undercutting and keeps pattern fidelity. And this is critical when defining gate lengths or oxide trenches for accurate alignment. The wafer temperature is controlled via electrostatic chuck with backside helium cooling. Typical Temp(~20°C to 80°C). Lower temperature prevents

photoresist damage and keeps etch rate stable. And for clean native oxide or residue before main etch starts, we go through a process called Breakthrough step. It ensures uniform etching and avoids delays or surface defects.

Gate Oxide Formation: The gate oxide formation is done by using the Dry Thermal Oxidation. Since we need to grow a very thin SiO_2 as a gate oxide. The reaction happens around ~900℃-1000℃. The Dry Oxidation produces high quality and reliable oxide interface for gate control which is critical for threshold voltage stability.

Polysilicon Gate Deposition: This process is for depositing a layer of undoped (or lightly doped) polysilicon over the thin gate oxide. This will become the gate electrode of the MOSFET. The deposition process we prefer to use is LPCVD (Low Pressure Chemical Vapor Deposition) because it offers excellent conformality, film purity and process control all of which are essential for reliable gate structures in MOSFETs. Other methods like PVD (sputtering) or PECVD (Plasma CVD) either lack step coverage or result in lower quality films. Silane (SiH_4) is decomposed at ~500℃-700℃under low pressure to deposit a uniform, high quality polysilicon film.

$$SiH_4 \rightarrow Si(solid) + 2H_2$$

We are using Silane as it is a simple chemistry and for having cleaner film. It has a good deposition rate and yields uniform and conformal films. We could have used Dichlorosilane($SiCl_2H_2$). But it is basically used for epitaxial silicon deposition and also it generates corrosive HCL by products. It is often used in more advanced or high temperature epi processes.

Gate Pattering: We are etching the polysilicon gate layer after it's deposited by LPCVD and patterned with photoresist. The method we used for etching is Reactive Ion Etching (RIE) which is Plasma based anisotropic dry etching. We are using this etching because it has anisotropic behavior, it has a high selectivity and it is compatible with PR masks. The common chemistry for this is

$$Si\ (solid) + 2Cl_2 \rightarrow SiCl_4\ (gas)$$

Here Polysilicon reacts with Cl radicals to form $SiCl_4$ which is volatile and easily removed by vacuum pumping. This process produces anisotropic vertical sidewalls, essential for accurate gate length control. Wafer temperature is maintained around 20-80℃ to preserve photoresist integrity. A breakthrough step using low power $Cl_{2\ plasma}$ is applied to clean native oxide before the main etch. Liftoff is not used since this is a subtractive etch process and photoresist is stripped after etching.

Source/Drain Doping: The technique we use for doping is Ion Implantation. Since we are dealing with NMOS the dopant element we use Phosphorus (P). The reason for choosing Phosphorus is it has light mass so easy to implant and it has high diffusivity. We can do the implantation at room temperature followed by annealing.

Annealing: We use Rapid Thermal Annealing (RTA) ~1100℃ for 10~30 seconds. The purpose of this is to repair lattice damage from ion implantation and activate dopants (driving them to substitutional lattice sites). We particularly use RTA for fast and localized heating to prevent unwanted diffusion and it is superior to furnace annealing for shallow junctions.

Sidewall Spacer Formation: Sidewall spacers are the thin, insulating layer deposited on the sides of the polysilicon gate. Sidewall spacer formation in MOSFET is crucial for controlling the short channel effect, reducing the gate leakage voltage and improving device performance by offsetting ion implantation profiles from the gate edge and adjusting the channel length. We prefer to use Plasma Enhanced Chemical Vapor Deposition (PECVD). The reason behind choosing this deposition method is, it works at low temperature (300-400°C), conformal and fast. After gate and doping steps, the wafer cannot be exposed to high temperature because high temperature will cause dopant diffusion and degrade fine structure. The deposition reaction is:

$$SiH_4 + N_20 \rightarrow SiO_2 + NH_3 \text{ (gas)}$$

After deposition , an anisotropic RIE etch back is performed to remove horizontal oxide , leaving oxide only on gate sidewalls. The resulting sidewall spacers help define lightly doped drain regions and provide gate to source / drain isolation.

Interlayer Dielectric Deposition: The purpose of this process is to electrically insulate the gate, source, drain from the metal interconnects. It prevents short circuits, capacitive coupling and leakage paths. We use the PECVD deposition as it happens in a low temperature, covering topography from gates, spacers and diffusion contacts. It provides good film uniformity. The same chemical reaction is happening in this process mentioned in step 10.

Contact Hole Etching: The goal of this process is to open vertical holes in the interlayer dielectric (SiO_2) to expose the source, drain and gate regions , so metal

contacts can be formed. We are using Reactive Ion Etching (RIE) - a dry anisotropic etching. The chemical reaction is as follow:

$$CF_4 + e^- \rightarrow CF_3 + F + e^-$$

$$SiO_2 + 4F \rightarrow SiF_4(gas) + O_2$$

The etch profile is highly anisotropic (vertical sidewalls). Wafer temperature is controlled at ~20-70℃to protect the photoresist. A breakthrough step using a low power plasma is performed first to clean native oxide and residues.

Metallization: Here we are depositing a metal layer to make ohmic contacts to source, drain and gate. We prefer to choose sputtering because it is low cost, standard and fast. We choose to deposit Aluminum(Al) since it is a good conductor, easy to deposit and pattern, does not require a diffusion barrier, forms low resistance ohmic contact to silicon. This sputtering process works by bombarding a metal target (Al) with Argon (Ar^+) plasma ions. This physically knocks atoms off the target and then they deposit on the wafer.

Metal Pattering: We are applying photoresist on top of the aluminum layer. Using photolithography to define the interconnect pattern. Then etching away unwanted aluminum areas. We prefer to use Contact Photolithography. And then we choose wet etching over dry etching since Aluminum etches quickly, cleanly with simple wet chemistry . The etch profile is isotropic which is acceptable for metals where the linewidths are relatively large.

Passivation Layer Deposition: After metallization, a passivation layer is deposited to protect the chip from moisture, ionic contamination , mechanical damage, and

corrosion. Again we use PECVD to deposit the Silicon Nitride (Si_3N_4) at ~300-400℃. The chemical reaction is:

$$3SiH_4 + 4NH_3 \rightarrow Si3N_4 + 12H_2$$

The resulting Si_3N_4 layer provides excellent chemical resistance and moisture protection. And then selective etching is performed afterward to open windows for wire bonding.

4. Thin Film Capacitor:

Introduction:

Capacitors are a crucial component in analog and digital circuits, used for energy storage, filtering, and signal coupling. The primary objective was to create a metal-insulator-metal (MIM) capacitor with high capacitance density, stable dielectric properties, and reliable performance.

Materials:

Thin-film capacitors can be fabricated using a variety of materials for each component—substrate, electrodes, and dielectric—depending on the desired electrical properties and compatibility with the fabrication process. The choice of materials impacts factors like capacitance density, leakage currents, reliability, and integration ease. Here are some common materials for thin-film capacitors along with the materials selected for this project:

Substrate: this serves as the foundation for the capacitor and influences mechanical stability and integration. Commonly used materials include lightly doped silicon (p-type

or n-type) for semiconductor-based capacitors and glass or ceramic for standalone thin-film capacitors.

Dielectric Layer: The dielectric material plays a crucial role in determining the capacitor's electrical properties, such as capacitance density, breakdown voltage, and leakage current. Common dielectric materials include silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), and tantalum pentoxide (Ta_2O_5). Each offers unique advantages; for example, HfO_2 and Ta_2O_5 provide high dielectric constants, enhancing capacitance density. For this project, we chose silicon dioxide (SiO_2) due to its excellent insulating properties, high breakdown voltage, and integration compatibility with standard silicon processes.

Bottom Electrode: The bottom electrode must be highly conductive, adhere well to the substrate, and offer compatibility with the dielectric material. Potential materials include aluminum (Al), titanium (Ti), tungsten (W), molybdenum (Mo), or platinum (Pt). Aluminum is commonly used due to its excellent conductivity, ease of deposition, and compatibility with standard semiconductor workflows. For this project, aluminum was chosen for the bottom electrode, deposited via sputtering to ensure uniformity and strong adhesion to the substrate.

Top Electrode: Similar to the bottom electrode, the top electrode requires a highly conductive material to ensure efficient charge transfer. Common materials include aluminum, copper (Cu), titanium, or platinum. Aluminum is again preferred in this project due to its high conductivity, cost-effectiveness, and straightforward etching properties.

The top electrode will also be aluminum, deposited via sputtering and patterned to form the desired capacitor structure.

Passivation Layer: The passivation layer protects the capacitor from environmental contamination, such as moisture and ionic intrusion, and provides mechanical durability. Typical materials include silicon nitride ($Si_3 N_4$), silicon oxynitride (SiON), or polyimide. For this project, we selected silicon nitride ($Si_3 N_4$) because of its superior moisture resistance, chemical stability, and reliability. The $Si_3 N_4$ layer will be deposited via Plasma Enhanced Chemical Vapor Deposition (PECVD).

Fabrication Process:

Substrate Preparation: The fabrication process starts with a lightly doped p-type silicon wafer, which serves as the substrate for the capacitor. To ensure a pristine surface, the wafer undergoes RCA cleaning, a multi-step process designed to remove organic and metallic contaminants. The SC-1 cleaning stage uses a solution of DI water, hydrogen peroxide, and ammonium hydroxide to oxidize and lift organic particles from the surface, followed by an HF dip to remove the native oxide layer. This ensures that subsequent layers are deposited on an uncontaminated silicon surface. SC-2 cleaning employs hydrochloric acid, hydrogen peroxide, and DI water to eliminate metallic residues while passivating the silicon surface to prevent recontamination. After cleaning, Chemical Mechanical Polishing (CMP) is performed to planarize the wafer, creating a smooth surface that enhances photolithography accuracy and ensures uniform deposition during the subsequent steps.

Field Oxide Formation: This process is done by Thermal Oxidation around 1000-1100℃. The purpose of this process is to grow a thick (~300-500 nm) SiO_2 layer for isolating devices. For this process, we chose the wet thermal oxidation process for having faster and thicker oxide growth. This oxidation process produces dense, uniform oxide with good electric insulation and better oxide quality than deposited oxides. The SiO_2 layer acts as a shield, protecting the whole substrate from any damage.

Bottom Electrode Formation: A layer of aluminum is deposited onto the oxide layer to form the conductive bottom electrode. This deposition is achieved through sputtering, a reliable technique that provides uniform coverage across the wafer and ensures strong adhesion to the oxide. Aluminum is chosen for its high electrical conductivity and compatibility with silicon-based processes, making it ideal for capacitor applications. To define the bottom electrode pattern, a positive photoresist is applied to the aluminum layer and spin-coated to ensure uniform thickness. Using a UV mask, the desired regions are exposed to ultraviolet light, rendering the exposed areas soluble in the developer solution. After development, wet etching is performed using phosphoric acid to selectively remove aluminum from unwanted areas. This process results in precisely patterned bottom electrodes, which are crucial for ensuring the functionality and alignment of the final device.

Dielectric Layer Formation: The dielectric layer is formed by growing a thin layer of silicon dioxide (SiO_2) on the substrate using dry thermal oxidation at ~900–1000°C. Silicon dioxide is selected as the dielectric material due to its excellent insulating properties, low leakage current, and high breakdown voltage, all of which are critical for

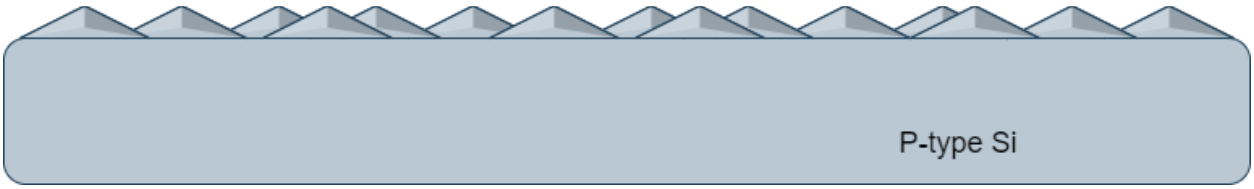
capacitor performance. The oxidation process ensures a uniform and high-quality insulating layer that effectively separates the capacitor's electrodes. Following oxidation, CMP is applied once again to planarize the dielectric layer. This step removes surface irregularities caused by the growth process, ensuring a flat and smooth oxide layer that is essential for achieving accurate photolithography and minimizing defects in the subsequent top electrode deposition.

Top Electrode Formation: A second layer of aluminum is deposited onto the dielectric layer to form the capacitor's top electrode. This deposition is also carried out using sputtering, providing excellent conformal coverage and maintaining strong electrical conductivity. The top electrode pattern is defined through photolithography, where a positive photoresist is applied to the aluminum layer and exposed to UV light through a mask that specifies the contact pad and electrode regions. After development, the exposed photoresist reveals the areas to be etched. Wet etching with phosphoric acid removes unwanted aluminum, leaving a clean and precisely patterned top electrode. Proper alignment with the bottom electrode is critical during this step to ensure that the capacitor achieves the desired capacitance and electric field uniformity.

Passivation Layer Deposition: To protect the capacitor from environmental factors such as moisture, ionic contamination, and mechanical damage, a passivation layer of silicon nitride ($Si_3 N_4$) is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) at ~300–400°C. Silicon nitride is an ideal choice due to its excellent chemical resistance and durability, ensuring the long-term reliability of the device. After deposition, photolithography is employed to define the bonding pad windows in the

passivation layer. The positive photoresist applied to the nitride layer is patterned using UV exposure through a mask, and after development, the exposed regions are etched using Reactive Ion Etching (RIE). The anisotropic etching provided by RIE ensures clean and precise openings in the passivation layer, enabling access to the bonding pads for electrical connections without compromising the underlying capacitor structure.

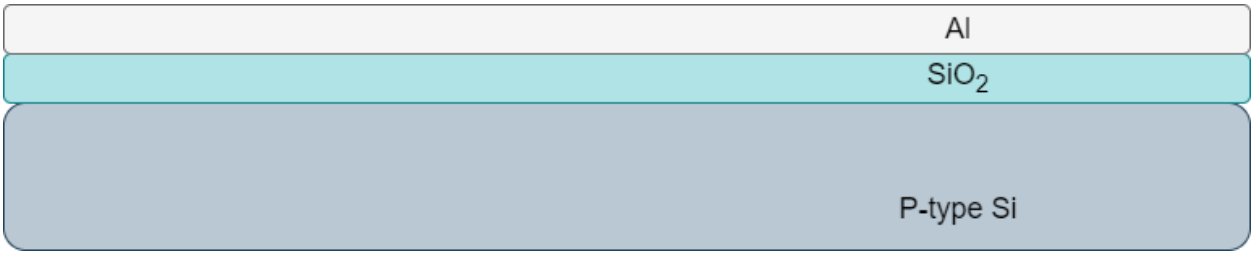
Process Diagram:



Raw Silicon substrate.

Silicon substrate after RCA cleaning and CMP.

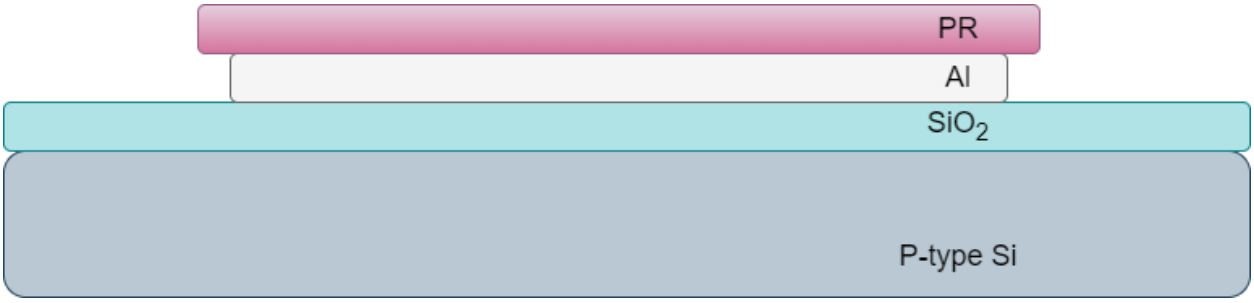
Silicon Dioxide insulating layer.



First Aluminum sputtered layer.

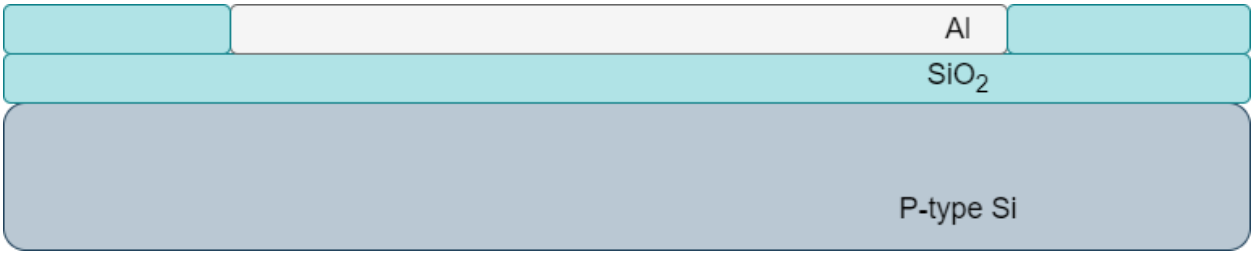
Photoresist layer.

Photoresist after the development step.



Wet etching of bottom electrode.

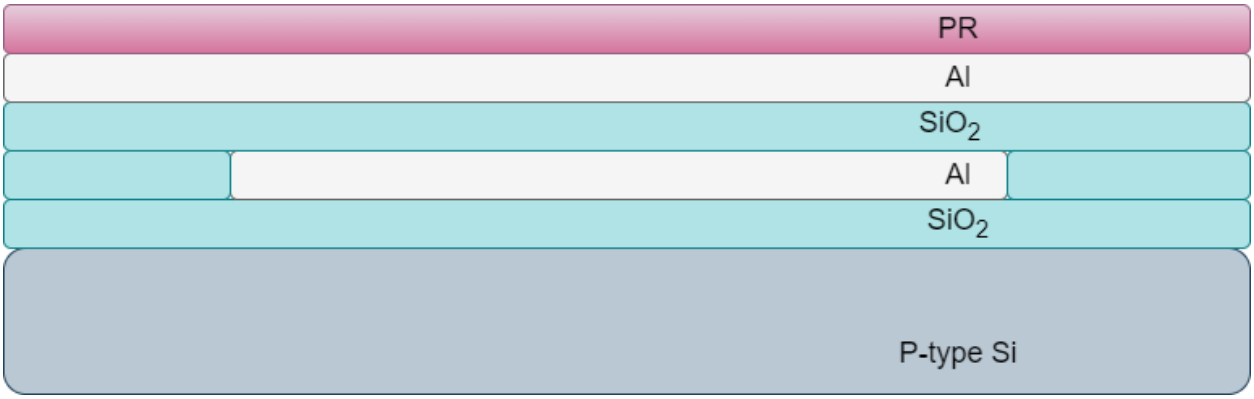
Insulation build up after removing the photoresist.



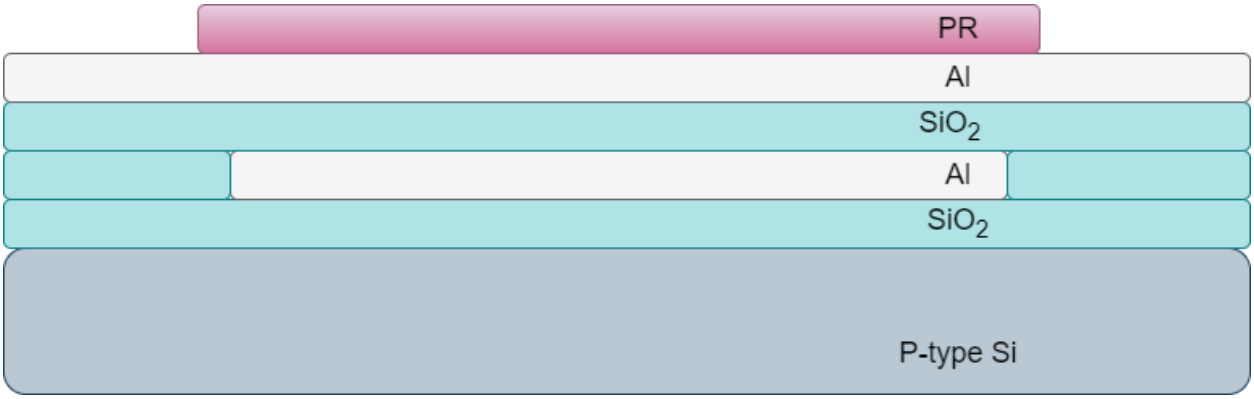
After CMP.

Dielectric layer after additional CMP.

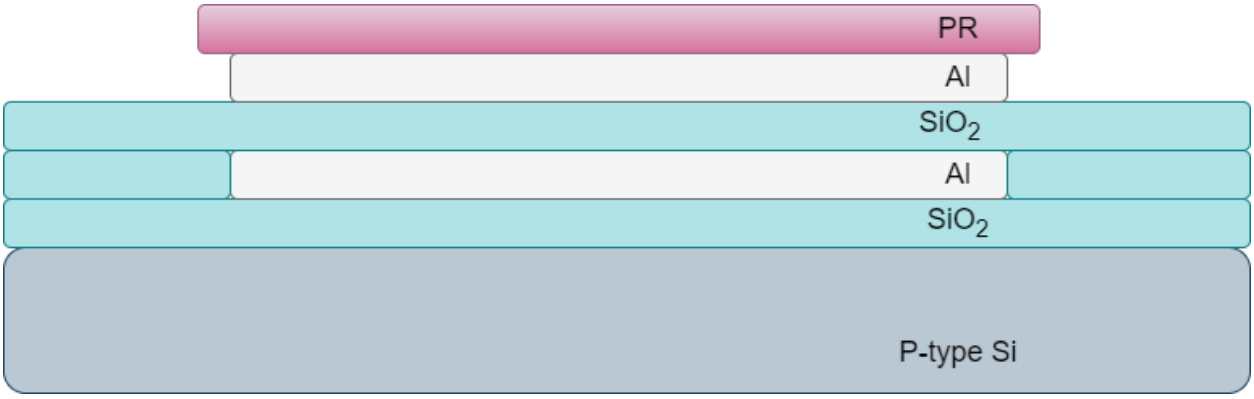
Second aluminum sputtered layer.



Photoresist layer.

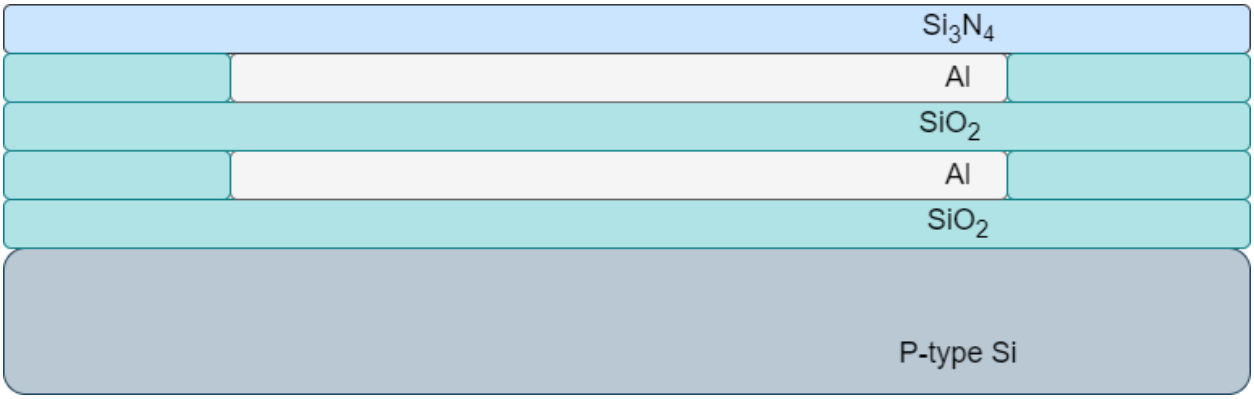


Photoresist after the development step.

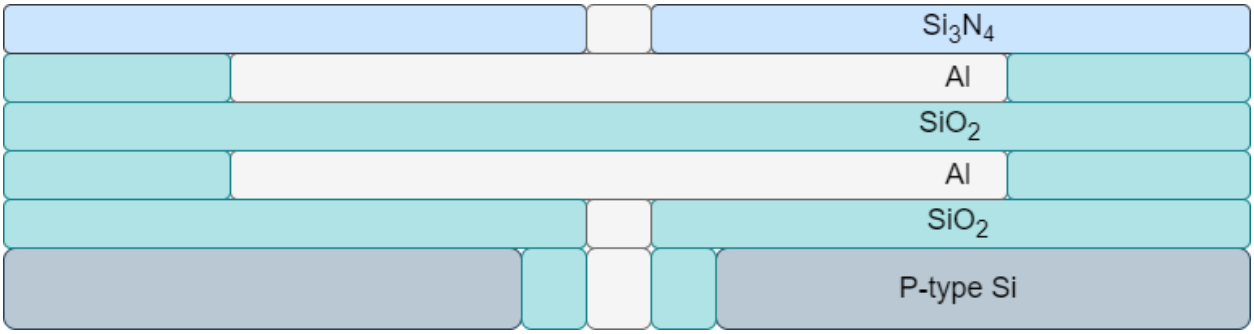


Wet etching of the top electrode.

Insulation build up after removing the photoresist.



Silicon Nitride passivation layer.



Backend processing for topside and backside vias/bond pads.

5. Thin Film Resistor:

Introduction:

Thin film and chip resistors are designed to limit the flow of electrical current within a circuit. The term “thin” refers to the extremely fine layer of resistive material, which ranges from a few nanometers to microns in thickness, deposited onto a ceramic or glass substrate.Thin film size usually varies from 0.001 um to 0.1 um. Thin film resistors offer higher precision, better stability, and superior temperature coefficients compared to thick film resistors, making them ideal for applications that require high accuracy.

Materials:

In the fabrication of thin-film resistors, the first essential step is the selection of a suitable substrate material. Typically, materials like Alumina ($Al_2 O_3$) or Silicon (Si) are chosen based on the required mechanical strength, electrical insulation, and thermal properties. Alumina is preferred when excellent electrical insulation and mechanical toughness are needed, as it is a very strong and durable ceramic. Silicon, on the other hand, is selected for applications requiring high thermal conductivity of semiconductor integration. The substrate provides the base support structure for all subsequent layers, making its selection critical for ensuring the stability, reliability, and performance of the final resistor.

Coming to the deposition, commonly used resistive materials include Nickel-Chromium (NiCr) alloys, Tantalum Nitride (TaN), and Silicon-Chromium (SiCr). Nickel-Chromium (NiCr) is widely used due to its excellent temperature stability and corrosion resistance,

making it ideal for precision applications. Tantalum Nitride (TaN) offers superior moisture and chemical resistance compared to NiCr, making it better suited for harsh environments. Silicon-Chromium (SiCr), while slightly less stable than NiCr in temperature variations, provides higher achievable resistance values, which is beneficial when very high resistances are needed. Each material is selected based on the specific performance requirements of the resistor.

Once almost all fabrication steps are completed, metallic contacts or leads made from materials such as aluminum (Al), titanium (Ti), or gold (Au) are attached to the resistor terminals.

Fabrication Process:

1. **Substrate Selection:**

   First, a ceramic material like alumina ($Al_2 O_3$) or sometimes silicon is selected based on mechanical strength, electrical insulation, and thermal properties. When we compare alumina ($Al_2 O_3$) and silicon (Si) for making thin-film resistors, they have some important differences. Alumina is a very good insulator, meaning it does not let electricity pass through it, while silicon is a semiconductor, so it can let a little bit of electricity flow. For heat, silicon is better because it can spread heat much faster than alumina. Alumina is very strong and tough, like a hard ceramic, and it does not break easily. Silicon is also strong but can be more brittle and break under stress. Both materials can have a very smooth surface, which is important for making thin films. Alumina can be polished very smooth, while silicon is naturally smooth after special treatments.

In our design we will be using Alumina since overall it is a much better.In our design, we will be using Alumina (Al_2O_3) as the substrate because it provides excellent electrical insulation, mechanical strength, and sufficient thermal conductivity for most thin-film resistor applications. Unlike silicon, which can conduct some current due to its semiconducting nature, alumina is a pure insulator, ensuring no leakage paths that could affect resistor accuracy. Additionally, its tough ceramic structure makes it highly resistant to mechanical stress, vibrations, and cracking — important for robust and long-term reliability. While silicon offers better thermal conductivity, alumina's thermal performance is still adequate, and it is more cost-effective and easier to handle in standalone resistor manufacturing. Therefore, alumina is a more suitable and practical choice for discrete precision thin-film resistors.

2. **Surface Polishing:**

In our thin-film resistor design, we are using Chemical Mechanical Polishing (CMP) because it provides the ultra-smooth and flat surface required for high-quality thin-film deposition. CMP combines mechanical abrasion with chemical etching using a slurry that contains both abrasive particles and reactive chemicals. The substrate is pressed against a rotating polishing pad while slurry is dispensed, enabling controlled material removal through both friction and chemical reaction. This process ensures the elimination of microscopic surface defects, scratches, and irregularities that could otherwise interfere with thin-film uniformity or adhesion. CMP is widely used for both alumina and silicon

substrates and is the industry standard for achieving the surface planarity needed in nanometer-scale film fabrication.

3. **Cleaning:**

After polishing, the substrate is chemically cleaned to eliminate any remaining particles, organic residues, or metal contaminants that could interfere with thin-film deposition. This is typically done using RCA cleaning, a two-step wet cleaning method. The first step, RCA-1 (SC-1), uses a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and water , heated to ~75–80°C. It removes organic contaminants and particles by oxidizing and lifting them off the surface. The second step, RCA-2 (SC-2), uses hydrochloric acid (HCl), hydrogen peroxide, and water in a 1:1:6 ratio to dissolve and remove metallic ions and prevent redeposition.These steps ensure the substrate surface is ultra-clean, allowing the thin film to adhere uniformly and preventing defects in the resistor.

4. Deposition of Thin Film:

A very thin layer of resistive material is coated onto the substrate. The material used to make thin film resistors are Nickel-Chromium (NiCr), Tantalum Nitride (TaN), and Silicon-Chromium (SiCr) due to their specific properties. NiCr is widely used because it offers very stable resistance across temperature changes and resists corrosion, making it ideal for precision applications. TaN is preferred in harsh environments because it provides excellent resistance to moisture and

chemicals. SiCr, while slightly less stable in temperature variation, is useful for applications requiring very high resistance values, as it can achieve greater resistivity than NiCr. Each material is selected based on the performance needs of the resistor.

In our design, we use sputtering as the preferred deposition method because it is highly compatible with both the Nickel-Chromium (NiCr) resistive material and the Alumina (Al_2O_3) substrate. Sputtering allows precise and uniform deposition of NiCr, which is essential for achieving consistent resistance values and excellent temperature stability. Since NiCr is a metallic alloy, sputtering is ideal because it does not rely on chemical reactions (as in PCVD) and can deposit alloy films with accurate composition and strong adhesion. Additionally, alumina is a robust ceramic that can withstand the physical bombardment involved in sputtering without damage. The strong film-to-substrate bonding achieved during sputtering ensures high durability and long-term stability of the resistor. Furthermore, the vacuum environment in sputtering minimizes contamination, resulting in high-purity films — critical for precision resistor performance. Overall, sputtering provides a reliable, clean, and controlled method for fabricating NiCr-based thin-film resistors on alumina substrates.

5. **Patterning:**

Once the thin resistive film NiCr is deposited, it must be patterned to define the exact shape and size of the resistor. This is done using a process called

photolithography, which allows for precise and repeatable micro-scale patterning on the substrate surface.

In photolithography, a photoresist (a light-sensitive polymer) is uniformly applied over the thin film using a technique like spin coating. The wafer is then exposed to ultraviolet (UV) light through a photomask that contains the desired resistor layout. The areas of the photoresist exposed to the light undergo a chemical change. A developer solution is then used to remove either the exposed or unexposed areas (depending on whether a positive or negative photoresist is used), revealing the thin film underneath in those regions.

Once the pattern is developed, the wafer undergoes an etching process to remove the exposed areas of the resistive film — thereby transferring the pattern into the actual material.

6. **Formation of Contacts:**

Attaching the metal contacts (leads or pads) to the resistor body.The contacts are often sputtered, plated, or attached through special metal deposition or soldering processes. Common contact materials include aluminum (Al), titanium (Ti), or gold (Au).

But here we will be using gold (Au) contacts at the ends of the resistive film to provide reliable electrical connections. Since gold offers excellent conductivity, chemical stability, and strong resistance to oxidation, it is an ideal material for precision resistors, especially in high-reliability or corrosive environments. The

gold contacts are applied using the sputtering technique, where high-energy argon ions in a vacuum chamber bombard a solid gold target, causing gold atoms to eject and deposit uniformly onto the desired contact areas of the substrate. This method ensures precise thickness control, strong adhesion, and uniform coverage, making it well-suited for fine-patterned thin-film resistor applications.

7. **Trimming and Calibration:**

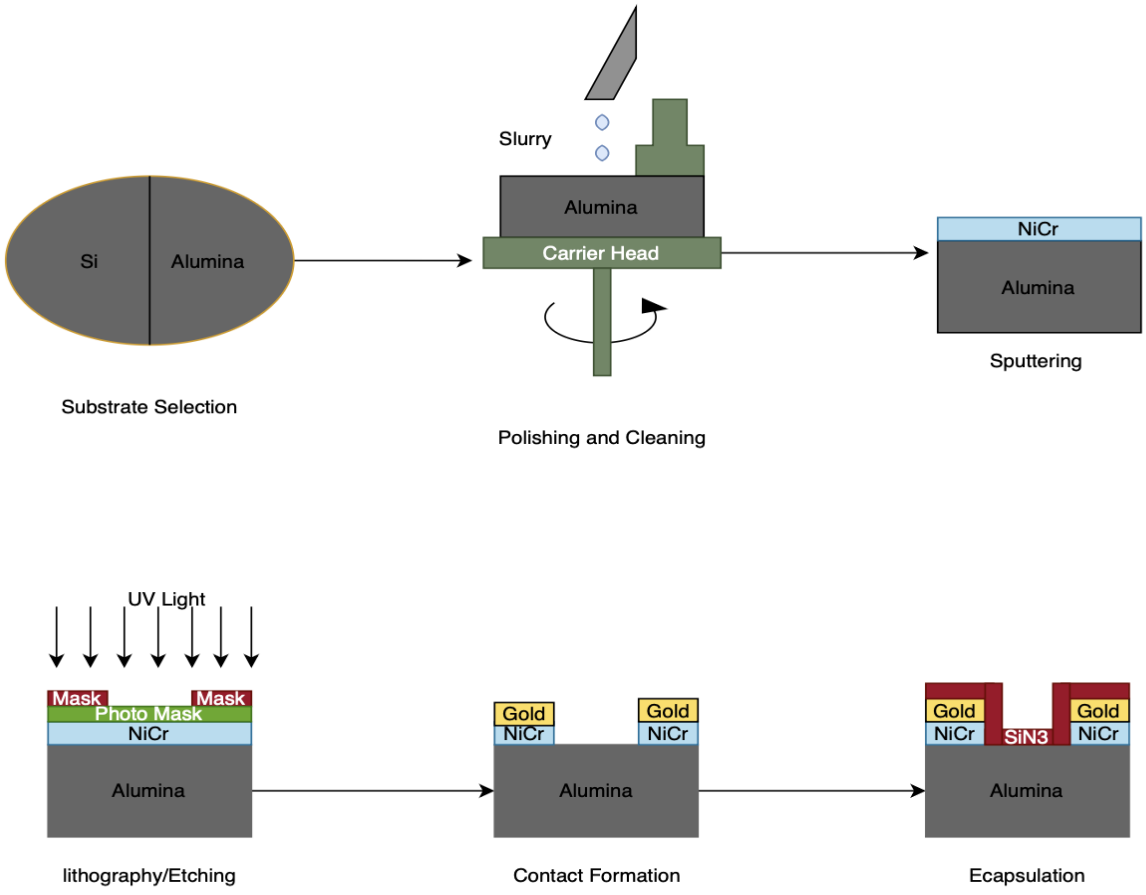
   After the initial construction, the resistor's resistance value is fine-tuned through trimming processes. This involves selectively removing parts of the resistor film to adjust its resistance to the desired specification. Laser trimming is used to remove the excess resistive material. During this process live readings are taken to reach the accurate value. If the resistance is low it is calibrated but if the resistance is too high it is discarded.

8. **Encapsulation:**

   Finally, the resistor is encapsulated with a conformal coating to protect it from environmental factors such as moisture, chemicals, or physical damage. This ensures the life and stable performance of the resistor in a variety of applications. Since your design prioritizes long-term reliability and protection against moisture, corrosion, and physical wear, Si_3N_4 is the better choice. It forms a dense, strong, and chemically resistant barrier, ideal for precision, high-stability resistors used in harsh or varying environments.

Furthermore, Si_3N_4 is chosen due to its excellent barrier properties against moisture and chemicals, as well as its high mechanical strength, which protects the resistor from scratches and external damage. This encapsulation step is critical to ensuring the lifespan, performance

Process Diagram:



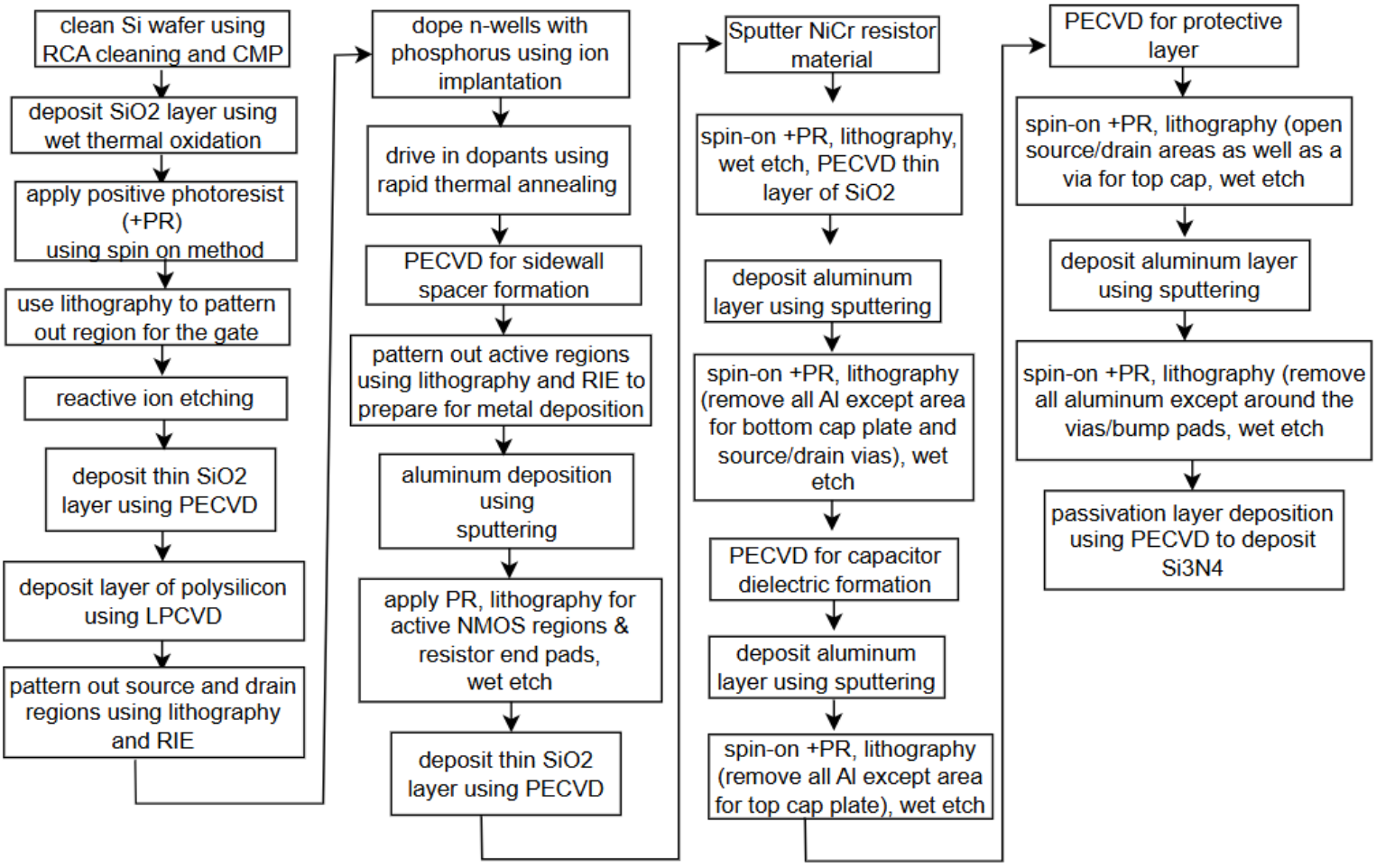
6. Process Integration:

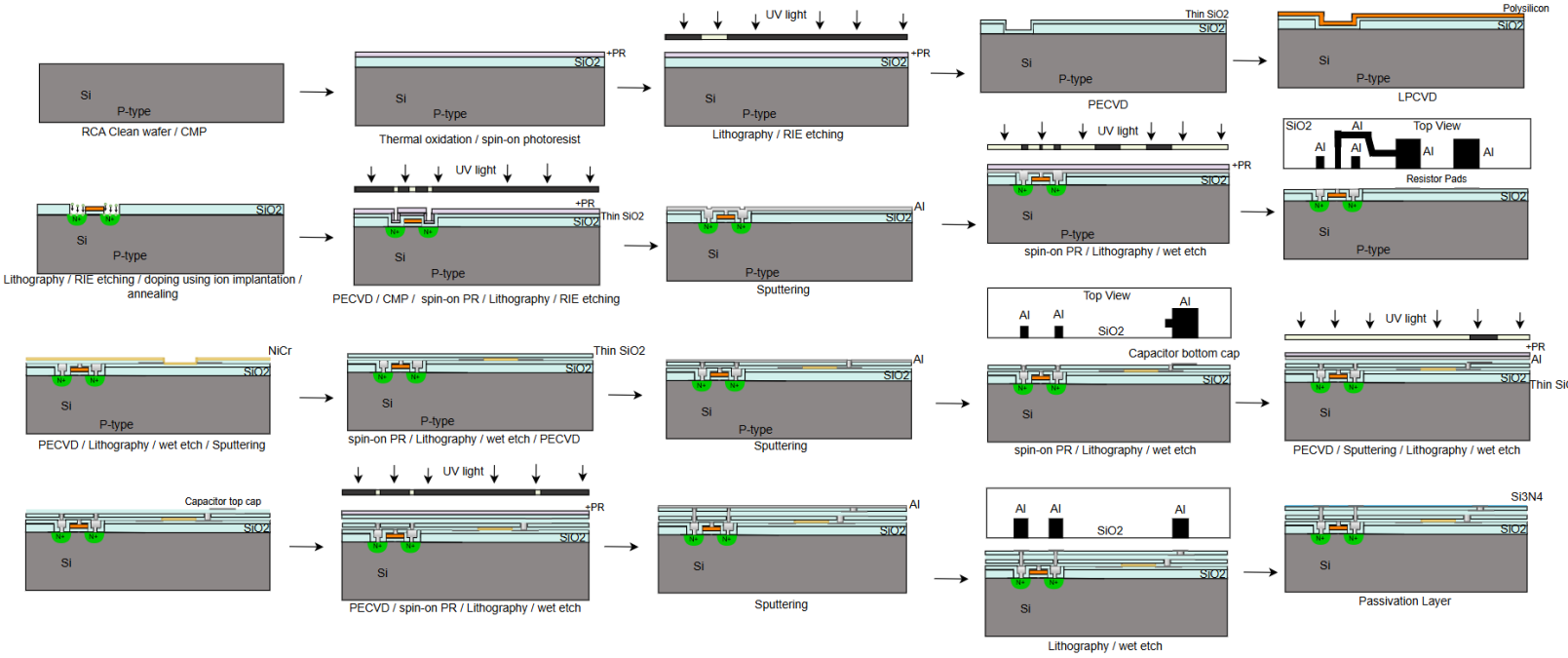
Integration Flow: Thin film components are temperature sensitive. Since the NMOS fabrication process requires the highest temperature, we will begin by building the transistor first, followed by the resistor then the capacitor. The NMOS is fabricated as stated in the above section for MOSFET fabrication process up until the metal patterning where aluminum is deposited and etched to form vias to the gate, source, and drain. Along with patterning the active regions of the transistor, we also pattern the ends of the resistor, leaving a gap in between the pads. At this time, we also connect the gate terminal to the first pad of the resistor. After growing a thin, protective SiO2 layer using PECVD, only the area between the resistor pads is exposed to UV light using the lithography mask. This defines the region where the resistor material will be deposited. Once the area has been etched, a thin layer of NiCr is sputtered on the surface of the wafer. Lithography and etching is once again performed, but this time, the pattern is reversed; only the area where the resistor sits will be hardened and everything else is exposed to UV light. Another thin layer of SiO2 is grown using PECVD and lithography and etching is then performed to open up vias where the source and drain are, as well as at the second resistor pad where the capacitor bottom plate will connect to. An aluminum layer is sputtered on, then the lithography mask will define the capacitor bottom plate. The capacitor dielectric material is then grown (SiO2 using PECVD) and aluminum is sputtered onto the surface. The top electrode of the capacitor is then formed using lithography and etching followed by another layer of SiO2. The final layer of aluminum is deposited using sputtering, and the bond pads for the source, drain, and top electrode of the capacitor are formed using lithography and

etching. Finally, a passivation layer is deposited across the wafer, and pad openings are defined and etched to expose the source, drain, and capacitor top plate pads for bonding.

Transmission Lines and Vias: Transmission lines and vias were added in between processes. The transmission line connecting the gate of the NMOS to the resistor was added during the etching process while etching out the active regions of the NMOS. The transmission line connecting the other resistor pad to the bottom electrode of the capacitor was added through a via connection. The source and drain areas as well as a via for the top electrode of the capacitor were etched out. These regions form the bond pads that will later be used to solder components onto.

Integration Diagram:




Si
P-type
RCA Clean wafer / CMP
SiO2
+PR
Thermal oxidation / spin-on photoresist
UV light
Lithography / RIE etching
Thin SiO2
PECVD
Polysilicon
LPCVD
Lithography / RIE etching / doping using ion implantation / annealing
PECVD / CMP / spin-on PR / Lithography / RIE etching
Al
Sputtering
spin-on PR / Lithography / wet etch
Top View
Resistor Pads
NiCr
PECVD / Lithography / wet etch / Sputtering
spin-on PR / Lithography / wet etch / PECVD
Capacitor bottom cap
PECVD / Sputtering / Lithography / wet etch
Capacitor top cap
PECVD / spin-on PR / Lithography / wet etch
Lithography / wet etch
Si3N4
Passivation Layer