An **application-specific integrated circuit** (**ASIC** [/ˈeɪsɪk/](https://en.wikipedia.org/wiki/Help:IPA/English)) is an [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) (IC) chip customized for a particular use, rather than intended for general-purpose use. For example, a chip designed to run in a [digital voice recorder](https://en.wikipedia.org/wiki/Digital_voice_recorder) or a high-efficiency [bitcoin miner](https://en.wikipedia.org/wiki/Bitcoin_mining) is an ASIC. [Application-specific standard product](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#Application-specific_standard_product) (ASSP) chips are intermediate between ASICs and industry standard integrated circuits like the [7400 series](https://en.wikipedia.org/wiki/7400_series) or the [4000 series](https://en.wikipedia.org/wiki/4000_series).[[1]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-:0-1) ASIC chips are typically [fabricated](https://en.wikipedia.org/wiki/Semiconductor_device_fabrication) using [metal-oxide-semiconductor](https://en.wikipedia.org/wiki/Metal-oxide-semiconductor) (MOS) technology, as [MOS integrated circuit](https://en.wikipedia.org/wiki/MOS_integrated_circuit) chips.[[2]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-computerhistory1967-2)

As feature sizes have shrunk and design tools improved over the years, the maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 [logic gates](https://en.wikipedia.org/wiki/Logic_gate) to over 100 million. Modern ASICs often include entire [microprocessors](https://en.wikipedia.org/wiki/Central_processing_unit), [memory](https://en.wikipedia.org/wiki/Memory) blocks including [ROM](https://en.wikipedia.org/wiki/Read-only_memory), [RAM](https://en.wikipedia.org/wiki/Random-access_memory), [EEPROM](https://en.wikipedia.org/wiki/EEPROM), [flash memory](https://en.wikipedia.org/wiki/Flash_memory) and other large building blocks. Such an ASIC is often termed a SoC ([system-on-chip](https://en.wikipedia.org/wiki/System-on-chip)). Designers of digital ASICs often use a [hardware description language](https://en.wikipedia.org/wiki/Hardware_description_language) (HDL), such as [Verilog](https://en.wikipedia.org/wiki/Verilog) or [VHDL](https://en.wikipedia.org/wiki/VHDL), to describe the functionality of ASICs.[[1]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-:0-1)

[Field-programmable gate arrays](https://en.wikipedia.org/wiki/Field-programmable_gate_array) (FPGA) are the modern-day technology for building a [breadboard](https://en.wikipedia.org/wiki/Breadboard) or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs or lower production volumes, FPGAs may be more cost effective than an ASIC design, even in production. The [non-recurring engineering](https://en.wikipedia.org/wiki/Non-recurring_engineering) (NRE) cost of an ASIC can run into the millions of dollars. Therefore, device manufacturers typically prefer FPGAs [for prototyping](https://en.wikipedia.org/wiki/FPGA_prototyping) and devices with low production volume and ASICs for [very large production volumes](https://en.wikipedia.org/wiki/Mass_production) where NRE costs can be [amortized](https://en.wikipedia.org/wiki/Amortized_cost) across many devices.

**History**

Early ASICs used [gate array](https://en.wikipedia.org/wiki/Gate_array) technology. By 1967, [Ferranti](https://en.wikipedia.org/wiki/Ferranti) and Interdesign were manufacturing early [bipolar](https://en.wikipedia.org/wiki/Bipolar_transistor) gate arrays. In 1967, [Fairchild Semiconductor](https://en.wikipedia.org/wiki/Fairchild_Semiconductor) introduced the Micromatrix family of bipolar [diode–transistor logic](https://en.wikipedia.org/wiki/Diode%E2%80%93transistor_logic) (DTL) and [transistor–transistor logic](https://en.wikipedia.org/wiki/Transistor%E2%80%93transistor_logic) (TTL) arrays.[[2]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-computerhistory1967-2)

[Complementary metal-oxide-semiconductor](https://en.wikipedia.org/wiki/Complementary_metal-oxide-semiconductor) (CMOS) technology opened the door to the broad commercialization of gate arrays. The first CMOS gate arrays were developed by Robert Lipp,[[3]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-3)[[4]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-4) in 1974 for International Microcircuits, Inc. (IMI).[[2]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-computerhistory1967-2)

[Metal-oxide-semiconductor](https://en.wikipedia.org/wiki/Metal-oxide-semiconductor) (MOS) [standard cell](https://en.wikipedia.org/wiki/Standard_cell) technology was introduced by Fairchild and [Motorola](https://en.wikipedia.org/wiki/Motorola), under the trade names Micromosaic and Polycell, in the 1970s. This technology was later successfully commercialized by [VLSI Technology](https://en.wikipedia.org/wiki/VLSI_Technology) (founded 1979) and [LSI Logic](https://en.wikipedia.org/wiki/LSI_Logic) (1981).[[2]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-computerhistory1967-2)

A successful commercial application of gate array circuitry was found in the low-end 8-bit [ZX81](https://en.wikipedia.org/wiki/ZX81) and [ZX Spectrum](https://en.wikipedia.org/wiki/ZX_Spectrum) [personal computers](https://en.wikipedia.org/wiki/Personal_computer), introduced in 1981 and 1982. These were used by [Sinclair Research](https://en.wikipedia.org/wiki/Sinclair_Research) (UK) essentially as a low-cost [I/O](https://en.wikipedia.org/wiki/Input/output) solution aimed at handling the [computer's graphics](https://en.wikipedia.org/wiki/Computer_graphics).

Customization occurred by varying a metal interconnect mask. Gate arrays had complexities of up to a few thousand gates; this is now called [mid-scale integration](https://en.wikipedia.org/wiki/Mid-scale_integration). Later versions became more generalized, with different [base dies](https://en.wikipedia.org/wiki/Die_(integrated_circuit)) customized by both metal and [polysilicon](https://en.wikipedia.org/wiki/Polycrystalline_silicon) layers. Some base dies also include [random-access memory](https://en.wikipedia.org/wiki/Random-access_memory) (RAM) elements.

## Standard-cell designs

Main article: [Standard cell](https://en.wikipedia.org/wiki/Standard_cell)

In the mid-1980s, a designer would choose an ASIC manufacturer and implement their design using the design tools available from the manufacturer. While third-party design tools were available, there was not an effective link from the third-party design tools to the [layout](https://en.wikipedia.org/wiki/Integrated_circuit_layout) and actual semiconductor process performance characteristics of the various ASIC manufacturers. Most designers used factory-specific tools to complete the implementation of their designs. A solution to this problem, which also yielded a much higher density device, was the implementation of [standard cells](https://en.wikipedia.org/wiki/Standard_cell).[[5]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-MichaelJohnSebastianSmith-5) Every ASIC manufacturer could create functional blocks with known electrical characteristics, such as [propagation delay](https://en.wikipedia.org/wiki/Propagation_delay), capacitance and inductance, that could also be represented in third-party tools. Standard-cell design is the utilization of these functional blocks to achieve very high gate density and good electrical performance. Standard-cell design is intermediate between [§ Gate-array and semi-custom design](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#Gate-array_and_semi-custom_design) and [§ Full-custom design](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#Full-custom_design) in terms of its non-recurring engineering and recurring component costs as well as performance and speed of development (including [time to market](https://en.wikipedia.org/wiki/Time_to_market)).

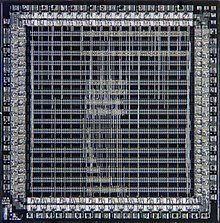
By the late 1990s, [logic synthesis](https://en.wikipedia.org/wiki/Logic_synthesis) tools became available. Such tools could compile [HDL](https://en.wikipedia.org/wiki/Hardware_description_language) descriptions into a gate-level [netlist](https://en.wikipedia.org/wiki/Netlist). Standard-cell [integrated circuits](https://en.wikipedia.org/wiki/Integrated_circuit) (ICs) are designed in the following conceptual stages referred to as [electronics design flow](https://en.wikipedia.org/wiki/Design_flow_(EDA)), although these stages overlap significantly in practice:

1. [**Requirements engineering**](https://en.wikipedia.org/wiki/Requirements_engineering): A team of design engineers starts with a non-formal understanding of the [required functions](https://en.wikipedia.org/wiki/Requirement) for a new ASIC, usually derived from [requirements analysis](https://en.wikipedia.org/wiki/Requirements_analysis).
2. [**Register-transfer level**](https://en.wikipedia.org/wiki/Register-transfer_level) **(RTL) design**: The design team constructs a description of an ASIC to achieve these goals using a [hardware description language](https://en.wikipedia.org/wiki/Hardware_description_language). This process is similar to writing a computer program in a [high-level language](https://en.wikipedia.org/wiki/High-level_programming_language).
3. [**Functional verification**](https://en.wikipedia.org/wiki/Functional_verification): Suitability for purpose is verified by functional verification. This may include such techniques as [logic simulation](https://en.wikipedia.org/wiki/Logic_simulation) through [test benches](https://en.wikipedia.org/wiki/Test_bench), [formal verification](https://en.wikipedia.org/wiki/Formal_verification), [emulation](https://en.wikipedia.org/wiki/Hardware_emulation), or creating and evaluating an equivalent pure [software](https://en.wikipedia.org/wiki/Software) model, as in [Simics](https://en.wikipedia.org/wiki/Simics). Each verification technique has advantages and disadvantages, and most often several methods are used together for ASIC verification. Unlike most [FPGAs](https://en.wikipedia.org/wiki/Field-programmable_gate_array), ASICs cannot be [reprogrammed](https://en.wikipedia.org/wiki/Reconfigurable_computing) once [fabricated](https://en.wikipedia.org/wiki/Semiconductor_device_fabrication) and therefore ASIC designs that are not completely correct are much more costly, increasing the need for full [test coverage](https://en.wikipedia.org/wiki/Test_coverage).
4. **Logic synthesis**: [Logic synthesis](https://en.wikipedia.org/wiki/Logic_synthesis) transforms the RTL design into a large collection called of lower-level constructs called standard cells. These constructs are taken from a [standard-cell library](https://en.wikipedia.org/wiki/Library_(electronics)) consisting of pre-characterized collections of [logic gates](https://en.wikipedia.org/wiki/Logic_gate) performing specific functions. The standard cells are typically specific to the planned manufacturer of the ASIC. The resulting collection of standard cells and the needed electrical connections between them is called a gate-level [netlist](https://en.wikipedia.org/wiki/Netlist).
5. **Placement**: The gate-level netlist is next processed by a [placement](https://en.wikipedia.org/wiki/Placement_(EDA)) tool which places the standard cells onto a region of an [integrated circuit die](https://en.wikipedia.org/wiki/Die_(integrated_circuit)) representing the final ASIC. The placement tool attempts to find an [optimized](https://en.wikipedia.org/wiki/Mathematical_optimization) placement of the standard cells, subject to a variety of specified constraints.
6. **Routing**: An electronics [routing](https://en.wikipedia.org/wiki/Routing_(electronic_design_automation)) tool takes the physical placement of the standard cells and uses the netlist to create the [electrical connections](https://en.wikipedia.org/wiki/Electrical_connection) between them. Since the [search space](https://en.wikipedia.org/wiki/Optimization_problem#Search_space) is large, this process will produce a "sufficient" rather than "[globally optimal](https://en.wikipedia.org/wiki/Global_optimum)" solution. The output is a file which can be used to create a set of [photomasks](https://en.wikipedia.org/wiki/Photomask) enabling a [semiconductor fabrication facility](https://en.wikipedia.org/wiki/Semiconductor_fabrication_plant), commonly called a 'fab' or 'foundry' to [manufacture](https://en.wikipedia.org/wiki/Manufacturing) physical [integrated circuits](https://en.wikipedia.org/wiki/Integrated_circuit). Placement and routing are closely interrelated and are collectively called [place and route](https://en.wikipedia.org/wiki/Place_and_route) in electronics design.
7. **Sign-off**: Given the final layout, [circuit extraction](https://en.wikipedia.org/wiki/Circuit_extraction) computes the [parasitic resistances and capacitances](https://en.wikipedia.org/wiki/Parasitic_element_(electrical_networks)). In the case of a [digital circuit](https://en.wikipedia.org/wiki/Digital_circuit), this will then be further mapped into [delay information](https://en.wikipedia.org/wiki/Propagation_delay) from which the circuit performance can be estimated, usually by [static timing analysis](https://en.wikipedia.org/wiki/Static_timing_analysis). This, and other final tests such as [design rule checking](https://en.wikipedia.org/wiki/Design_rule_checking) and [power analysis](https://en.wikipedia.org/wiki/Power_analysis) collectively called [signoff](https://en.wikipedia.org/wiki/Signoff_(electronic_design_automation)) are intended to ensure that the device will function correctly over all extremes of the process, voltage and temperature. When this testing is complete the [photomask](https://en.wikipedia.org/wiki/Photomask) information is released for [chip fabrication](https://en.wikipedia.org/wiki/Chip_fabrication).

These steps, implemented with a level of skill common in the industry, almost always produce a final device that correctly implements the original design, unless flaws are later introduced by the physical fabrication process.[[6]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-6)

The design steps, also called [design flow](https://en.wikipedia.org/wiki/Design_flow_(EDA)), are also common to standard product design. The significant difference is that standard-cell design uses the manufacturer's cell libraries that have been used in potentially hundreds of other design implementations and therefore are of much lower risk than full custom design. Standard cells produce a [design density](https://en.wikipedia.org/wiki/Transistor_density) that is cost effective, and they can also integrate [IP cores](https://en.wikipedia.org/wiki/Semiconductor_intellectual_property_core) and [static random-access memory](https://en.wikipedia.org/wiki/Static_random-access_memory) (SRAM) effectively, unlike gate arrays.

## Gate-array and semi-custom design

[](https://en.wikipedia.org/wiki/File:S-MOS_Systems_ASIC_SLA6140.jpg)

Microscope photograph of a gate-array ASIC showing the predefined logic cells and custom interconnections. This particular design uses less than 20% of available logic gates.

[Gate array](https://en.wikipedia.org/wiki/Gate_array) design is a manufacturing method in which diffused layers, each consisting of [transistors](https://en.wikipedia.org/wiki/Transistor) and other [active devices](https://en.wikipedia.org/wiki/Active_element), are predefined and [electronics wafers](https://en.wikipedia.org/wiki/Wafer_(electronics)) containing such devices are "held in stock" or unconnected prior to the [metallization](https://en.wikipedia.org/wiki/Metallizing) stage of the [fabrication process](https://en.wikipedia.org/wiki/Fabrication_process). The [physical design](https://en.wikipedia.org/wiki/Physical_design_(electronics)) process defines the interconnections of these layers for the final device. For most ASIC manufacturers, this consists of between two and nine metal layers with each layer running perpendicular to the one below it. Non-recurring engineering costs are much lower than full custom designs, as [photolithographic](https://en.wikipedia.org/wiki/Photolithography) masks are required only for the metal layers. Production cycles are much shorter, as metallization is a comparatively quick process; thereby accelerating [time to market](https://en.wikipedia.org/wiki/Time_to_market).

Gate-array ASICs are always a compromise between rapid design and [performance](https://en.wikipedia.org/wiki/Computer_performance) as mapping a given design onto what a manufacturer held as a stock wafer never gives 100% [circuit utilization](https://en.wikipedia.org/wiki/Circuit_utilization). Often difficulties in [routing](https://en.wikipedia.org/wiki/Routing_(electronic_design_automation)) the interconnect require migration onto a larger array device with consequent increase in the piece part price. These difficulties are often a result of the layout [EDA](https://en.wikipedia.org/wiki/Electronic_design_automation) software used to develop the interconnect.

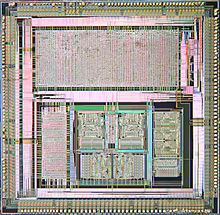
Pure, logic-only gate-array design is rarely implemented by circuit designers today, having been almost entirely replaced by [field-programmable](https://en.wikipedia.org/wiki/Field-programmability) devices. Most prominent of such devices are [field-programmable gate arrays](https://en.wikipedia.org/wiki/Field-programmable_gate_array) (FPGAs) which can be programmed by the user and thus offer minimal tooling charges non-recurring engineering, only marginally increased piece part cost, and comparable performance.

Today, gate arrays are evolving into [structured ASICs](https://en.wikipedia.org/wiki/Structured_ASIC_platform) that consist of a large [IP core](https://en.wikipedia.org/wiki/IP_core) like a [CPU](https://en.wikipedia.org/wiki/Central_processing_unit), [digital signal processor](https://en.wikipedia.org/wiki/Digital_signal_processor) units, [peripherals](https://en.wikipedia.org/wiki/Peripheral), standard [interfaces](https://en.wikipedia.org/wiki/Computer_bus), integrated [memories](https://en.wikipedia.org/wiki/Computer_memory), [SRAM](https://en.wikipedia.org/wiki/Static_random-access_memory), and a block of [reconfigurable](https://en.wikipedia.org/wiki/Reconfigurable_computing), uncommitted logic. This shift is largely because ASIC devices are capable of integrating large blocks of [system](https://en.wikipedia.org/wiki/Systems_engineering) functionality, and [systems on a chip](https://en.wikipedia.org/wiki/System_on_a_chip) (SoCs) require [glue logic](https://en.wikipedia.org/wiki/Glue_logic), [communications subsystems](https://en.wikipedia.org/wiki/Communications_system) (such as [networks on chip](https://en.wikipedia.org/wiki/Network_on_a_chip)), [peripherals](https://en.wikipedia.org/wiki/Peripheral) and other components rather than only [functional units](https://en.wikipedia.org/wiki/Functional_unit) and basic interconnection.

In their frequent usages in the field, the terms "gate array" and "semi-custom" are synonymous when referring to ASICs. [Process engineers](https://en.wikipedia.org/wiki/Process_engineering) more commonly use the term "semi-custom", while "gate-array" is more commonly used by logic (or gate-level) designers.

## Full-custom design

Main article: [Full custom](https://en.wikipedia.org/wiki/Full_custom)

[](https://en.wikipedia.org/wiki/File:VLSI_VL82C486_Single_Chip_486_System_Controller_HV.jpg)

Microscope photograph of custom ASIC (486 chipset) showing gate-based design on top and custom circuitry on bottom

By contrast, full-custom ASIC design defines all the photolithographic layers of the device.[[5]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-MichaelJohnSebastianSmith-5) Full-custom design is used for both ASIC design and for standard product design.

The benefits of full-custom design include reduced area (and therefore recurring component cost), [performance](https://en.wikipedia.org/wiki/Computer_performance) improvements, and also the ability to integrate [analog](https://en.wikipedia.org/wiki/Analog_signal) components and other [pre-designed](https://en.wikipedia.org/wiki/Semiconductor_intellectual_property_core)—and thus fully verified—components, such as [microprocessor](https://en.wikipedia.org/wiki/Microprocessor) cores, that form a [system on a chip](https://en.wikipedia.org/wiki/System_on_a_chip).

The disadvantages of full-custom design can include increased manufacturing and design time, increased non-recurring engineering costs, more complexity in the [computer-aided design](https://en.wikipedia.org/wiki/Computer-aided_design) (CAD) and [electronic design automation](https://en.wikipedia.org/wiki/Electronic_design_automation) systems, and a much higher skill requirement on the part of the design team.

For digital-only designs, however, "standard-cell" cell libraries, together with modern CAD systems, can offer considerable performance/cost benefits with low risk. Automated layout tools are quick and easy to use and also offer the possibility to "hand-tweak" or manually optimize any performance-limiting aspect of the design.

This is designed by using basic logic gates, circuits or layout specially for a design.

## Structured design

Main articles: [Structured ASIC platform](https://en.wikipedia.org/wiki/Structured_ASIC_platform) and [Platform-based design](https://en.wikipedia.org/wiki/Platform-based_design)

*Structured ASIC design* (also referred to as "*platform ASIC design*") is a relatively new trend in the semiconductor industry, resulting in some variation in its definition. However, the basic premise of a structured ASIC is that both manufacturing cycle time and design cycle time are reduced compared to cell-based ASIC, by virtue of there being pre-defined metal layers (thus reducing manufacturing time) and pre-characterization of what is on the silicon (thus reducing design cycle time).

Definition from Foundations of Embedded Systems states that

In a "structured ASIC" design, the logic mask-layers of a device are predefined by the ASIC vendor (or in some cases by a third party). Design differentiation and customization is achieved by creating custom metal layers that create custom connections between predefined lower-layer logic elements. "Structured ASIC" technology is seen as bridging the gap between field-programmable gate arrays and "standard-cell" ASIC designs. Because only a small number of chip layers must be custom-produced, "structured ASIC" designs have much smaller non-recurring expenditures (NRE) than "standard-cell" or "full-custom" chips, which require that a full mask set be produced for every design.

— Foundations of Embedded Systems

[[7]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-7)

This is effectively the same definition as a gate array. What distinguishes a structured ASIC from a gate array is that in a gate array, the predefined metal layers serve to make manufacturing turnaround faster. In a structured ASIC, the use of predefined metallization is primarily to reduce cost of the mask sets as well as making the design cycle time significantly shorter.

For example, in a cell-based or gate-array design the user must often design power, clock, and test structures themselves. By contrast, these are predefined in most structured ASICs and therefore can save time and expense for the designer compared to gate-array based designs. Likewise, the design tools used for structured ASIC can be substantially lower cost and easier (faster) to use than cell-based tools, because they do not have to perform all the functions that cell-based tools do. In some cases, the structured ASIC vendor requires that customized tools for their device (e.g., custom physical synthesis) be used, also allowing for the design to be brought into manufacturing more quickly.

## Cell libraries, IP-based design, hard and soft macros

[Cell libraries](https://en.wikipedia.org/wiki/Library_(electronics)) of logical primitives are usually provided by the device manufacturer as part of the service. Although they will incur no additional cost, their release will be covered by the terms of a [non-disclosure agreement](https://en.wikipedia.org/wiki/Non-disclosure_agreement) (NDA) and they will be regarded as intellectual property by the manufacturer. Usually their physical design will be pre-defined so they could be termed "hard macros".

What most engineers understand as "[intellectual property](https://en.wikipedia.org/wiki/Intellectual_property)" are [IP cores](https://en.wikipedia.org/wiki/Semiconductor_intellectual_property_core), designs purchased from a third-party as sub-components of a larger ASIC. They may be provided in the form of a [hardware description language](https://en.wikipedia.org/wiki/Hardware_description_language) (often termed a "soft macro"), or as a fully routed design that could be printed directly onto an ASIC's mask (often termed a "hard macro"). Many organizations now sell such pre-designed cores – CPUs, Ethernet, USB or telephone interfaces – and larger organizations may have an entire department or division to produce cores for the rest of the organization. The company [ARM](https://en.wikipedia.org/wiki/ARM_(company)) (Advanced [RISC](https://en.wikipedia.org/wiki/Reduced_instruction_set_computer) Machines) *only* sells IP cores, making it a [fabless manufacturer](https://en.wikipedia.org/wiki/Fabless_manufacturing).

Indeed, the wide range of functions now available in structured ASIC design is a result of the phenomenal improvement in electronics in the late 1990s and early 2000s; as a core takes a lot of time and investment to create, its [re-use](https://en.wikipedia.org/wiki/Code_reuse) and further development cuts product cycle times dramatically and creates better products. Additionally, [open-source hardware](https://en.wikipedia.org/wiki/Open-source_hardware) organizations such as [OpenCores](https://en.wikipedia.org/wiki/OpenCores) are collecting free IP cores, paralleling the [open-source software](https://en.wikipedia.org/wiki/Open-source_software) movement in hardware design.

Soft macros are often process-independent (i.e. they can be fabricated on a wide range of manufacturing processes and different manufacturers). Hard macros are process-limited and usually further design effort must be invested to migrate (port) to a different process or manufacturer.

## Multi-project wafers

Some manufacturers offer multi-project wafers (MPW) as a method of obtaining low cost prototypes. Often called shuttles, these MPW, containing several designs, run at regular, scheduled intervals on a "cut and go" basis, usually with very little liability on the part of the manufacturer. The contract involves the assembly and packaging of a handful of devices. The service usually involves the supply of a physical design database (i.e. masking information or pattern generation (PG) tape). The manufacturer is often referred to as a "silicon foundry" due to the low involvement it has in the process.

## Application-specific standard product

[](https://en.wikipedia.org/wiki/File:Kyocera_FS-C5200DN_-_interface_board_-_Renesas_M66591GP-4189.jpg)

[Renesas](https://en.wikipedia.org/wiki/Renesas_Electronics) M66591GP: USB2.0 Peripheral Controller

An **application-specific standard product** or **ASSP** is an [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) that implements a specific [function](https://en.wikipedia.org/wiki/Function_(engineering)) that appeals to a wide market. As opposed to ASICs that combine a collection of functions and are designed by or for one [customer](https://en.wikipedia.org/wiki/Customer), ASSPs are available as off-the-shelf components. ASSPs are used in all industries, from automotive to communications.[[*citation needed*](https://en.wikipedia.org/wiki/Wikipedia:Citation_needed)] As a general rule, if you can find a [design](https://en.wikipedia.org/wiki/Design) in a data [book](https://en.wikipedia.org/wiki/Book), then it is probably not an ASIC, but there are some exceptions.[[*clarification needed*](https://en.wikipedia.org/wiki/Wikipedia:Please_clarify)]

For example, two ICs that might or might not be considered ASICs are a controller chip for a PC and a chip for a [modem](https://en.wikipedia.org/wiki/Modem). Both of these examples are specific to an application (which is typical of an ASIC) but are sold to many different system vendors (which is typical of standard parts). ASICs such as these are sometimes called application-specific standard products (ASSPs).

Examples of ASSPs are encoding/decoding chip, standalone USB interface chip, etc.

[IEEE](https://en.wikipedia.org/wiki/IEEE) used to publish an ASSP magazine,[[8]](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit#cite_note-8) which was renamed to IEEE Signal Processing Magazine in 1990.

## See also

* [Application-specific instruction-set processor](https://en.wikipedia.org/wiki/Application-specific_instruction-set_processor) (ASIP)
* [Complex programmable logic device](https://en.wikipedia.org/wiki/Complex_programmable_logic_device) (CPLD)
* [Electronic design automation](https://en.wikipedia.org/wiki/Electronic_design_automation) (EDA or ECAD)
* [Field-programmable gate array](https://en.wikipedia.org/wiki/Field-programmable_gate_array) (FPGA)
* [Multi-project chip](https://en.wikipedia.org/wiki/Multi-project_chip) (MPC)
* [Very-large-scale integration](https://en.wikipedia.org/wiki/Very-large-scale_integration) (VLSI)
* [System-on-a-chip](https://en.wikipedia.org/wiki/System_on_a_chip) (SoC)
* [Hardware acceleration](https://en.wikipedia.org/wiki/Hardware_acceleration) for an overview of computing based primarily in hardware