**Second Level Address Translation** (**SLAT**), also known as **nested paging**, is a [hardware-assisted virtualization](https://en.wikipedia.org/wiki/Hardware-assisted_virtualization) technology which makes it possible to avoid the overhead associated with software-managed [shadow page tables](https://en.wikipedia.org/wiki/Shadow_page_tables).

[AMD](https://en.wikipedia.org/wiki/AMD) has supported SLAT through the Rapid Virtualization Indexing (RVI) technology since the introduction of its third-generation [Opteron](https://en.wikipedia.org/wiki/Opteron) processors (code name Barcelona). [Intel](https://en.wikipedia.org/wiki/Intel)'s implementation of SLAT, known as Extended Page Table (EPT), was introduced in the [Nehalem microarchitecture](https://en.wikipedia.org/wiki/Nehalem_(microarchitecture)) found in certain [Core i7](https://en.wikipedia.org/wiki/Core_i7), [Core i5](https://en.wikipedia.org/wiki/Core_i5), and [Core i3](https://en.wikipedia.org/wiki/Core_i3) processors.

[ARM](https://en.wikipedia.org/wiki/ARM_architecture)'s virtualization extensions support SLAT, known as Stage-2 page-tables provided by a Stage-2 [MMU](https://en.wikipedia.org/wiki/Memory_management_unit). The guest uses the Stage-1 MMU. Support was added as optional in the ARMv7ve architecture and is also supported in the ARMv8 (32-bit and 64-bit) architectures.

Overview[[edit](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=1)]

Modern processors use the concepts of [physical memory](https://en.wikipedia.org/wiki/Physical_memory) and [virtual memory](https://en.wikipedia.org/wiki/Virtual_memory); running processes use virtual addresses and when an instruction requests access to memory, the processor translates the virtual address to a physical address using a [page table](https://en.wikipedia.org/wiki/Page_table) or [translation lookaside buffer](https://en.wikipedia.org/wiki/Translation_lookaside_buffer) (TLB). When running a virtual system, it has allocated virtual memory of the host system that serves as a physical memory for the guest system, and the same process of address translation goes on also within the guest system. This increases the cost of memory access since the address translation needs to be performed twice – once inside the guest system (using software-emulated [shadow page table](https://en.wikipedia.org/wiki/Shadow_page_tables)), and once inside the host system (using hardware page table).

In order to make this translation more efficient, processor vendors implemented technologies commonly called SLAT. By treating each guest-physical address as a host-virtual address, a slight extension of the hardware used to walk a non-virtualized page table (now the guest page table) can walk the host page table. With [multilevel page tables](https://en.wikipedia.org/wiki/Multilevel_page_table) the host page table can be viewed conceptually as *nested* within the guest page table. A hardware page table walker can treat the additional translation layer almost like adding levels to the page table.

Using SLAT and multilevel page tables, the number of levels needed to be walked to find the translation doubles when the guest-physical address is the same size as the guest-virtual address and the same size pages are used. This increases the importance of caching values from intermediate levels of the host and guest page tables. It is also helpful to use large pages in the host page tables to reduce the number of levels (e.g., in x86-64, using 2 [MB](https://en.wikipedia.org/wiki/MiB) pages removes one level in the page table). Since memory is typically allocated to virtual machines at coarse granularity, using large pages for guest-physical translation is an obvious optimization, reducing the depth of look-ups and the memory required for host page tables.

## Implementations[[edit](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=2)]

### Rapid Virtualization Indexing**[**[**edit**](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=3)**]**

Rapid Virtualization Indexing (RVI), known as Nested Page Tables (NPT) during its development, is an [AMD](https://en.wikipedia.org/wiki/AMD) second generation [hardware-assisted virtualization](https://en.wikipedia.org/wiki/Hardware-assisted_virtualization) technology for the processor [memory management unit](https://en.wikipedia.org/wiki/Memory_management_unit) (MMU).[[1]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-1)[[2]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-2)

A [VMware](https://en.wikipedia.org/wiki/VMware) research paper found that RVI offers up to 42% gains in performance compared with software-only (shadow page table) implementation.[[3]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-vmware-3) Tests conducted by [Red Hat](https://en.wikipedia.org/wiki/Red_Hat) showed a doubling in performance for [OLTP](https://en.wikipedia.org/wiki/OLTP) benchmarks.[[4]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-4)

RVI was introduced in the third generation of [Opteron](https://en.wikipedia.org/wiki/Opteron) processors, [code name Barcelona](https://en.wikipedia.org/wiki/AMD_K10).[[5]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-5)

### Extended Page Tables**[**[**edit**](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=4)**]**

Extended Page Tables (EPT) is an Intel second-generation [x86 virtualization](https://en.wikipedia.org/wiki/X86_virtualization) technology for the [memory management unit](https://en.wikipedia.org/wiki/Memory_management_unit) (MMU). EPT support is found in Intel's [Core i3](https://en.wikipedia.org/wiki/Core_i3#Core_i3), [Core i5](https://en.wikipedia.org/wiki/Core_i5#Core_i5), [Core i7](https://en.wikipedia.org/wiki/Core_i7#Core_i7) and [Core i9](https://en.wikipedia.org/wiki/Core_i9#Core_i9) CPUs, among others.[[6]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-6) It is also found in some newer [VIA](https://en.wikipedia.org/wiki/VIA_Technologies) CPUs.

EPT is required in order to launch a logical processor directly in [real mode](https://en.wikipedia.org/wiki/Real_mode), a feature called "unrestricted guest" in Intel's jargon, and introduced in the [Westmere microarchitecture](https://en.wikipedia.org/wiki/Westmere_(microarchitecture)).[[7]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-7)[[8]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-8)

According to a VMware evaluation paper: "EPT provides performance gains of up to 48% for MMU-intensive benchmarks and up to 600% for MMU-intensive microbenchmarks", although it can actually cause code to run slower than a software implementation in some [corner cases](https://en.wikipedia.org/wiki/Corner_case).[[9]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-9)

### Stage-2 page-tables**[**[**edit**](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=5)**]**

Stage-2 page-table support is present in ARM processors that implement exception level 2 (EL2).

## Support in software[[edit](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=6)]

[Hypervisors](https://en.wikipedia.org/wiki/Hypervisor) that support SLAT include the following:

* [Hyper-V](https://en.wikipedia.org/wiki/Hyper-V) for [Windows Server 2008 R2](https://en.wikipedia.org/wiki/Windows_Server_2008_R2), [Windows 8](https://en.wikipedia.org/wiki/Windows_8) and later.[[10]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-10) The Windows 8 (and later Microsoft Windows) Hyper-V actually requires SLAT.[[11]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-11)[[12]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-12)
* Hypervisor.framework, a native [macOS](https://en.wikipedia.org/wiki/MacOS) hypervisor, available since macOS 10.10[[13]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-13)
* [KVM](https://en.wikipedia.org/wiki/Kernel-based_Virtual_Machine), since version 2.6.26 of the [Linux kernel mainline](https://en.wikipedia.org/wiki/Linux_kernel_mainline)[[14]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-14)[[15]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-15)
* [Parallels Desktop for Mac](https://en.wikipedia.org/wiki/Parallels_Desktop_for_Mac), since version 5[[16]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-16)
* [VirtualBox](https://en.wikipedia.org/wiki/VirtualBox), since version 2.0.0[[17]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-17)
* [VMware ESX](https://en.wikipedia.org/wiki/VMware_ESX), since version 3.5[[3]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-vmware-3)
* [VMware Workstation](https://en.wikipedia.org/wiki/VMware_Workstation). The VMware Workstation 14 (and later VMware Workstation) actually requires SLAT.[[18]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-18)
* [Xen](https://en.wikipedia.org/wiki/Xen), since version 3.2.0[[19]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-19)
* [Qubes OS](https://en.wikipedia.org/wiki/Qubes_OS) — SLAT mandatory[[20]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-20)
* [bhyve](https://en.wikipedia.org/wiki/Bhyve)[[21]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-21)[[22]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-22) — SLAT mandatory and slated to remain mandatory
* vmm, a native hypervisor on [OpenBSD](https://en.wikipedia.org/wiki/OpenBSD) — SLAT mandatory[[23]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-23)[[24]](https://en.wikipedia.org/wiki/Second_Level_Address_Translation#cite_note-24)

Some of the above hypervisors actually require SLAT in order to work at all (not just faster) as they do not implement a software shadow page table; the list is not fully updated to reflect that.

## See also[[edit](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=7)]

* [AMD-V](https://en.wikipedia.org/wiki/AMD-V) (codename Pacifica) – the first-generation AMD hardware virtualization support
* [Page table](https://en.wikipedia.org/wiki/Page_table)
* [VT-x](https://en.wikipedia.org/wiki/VT-x)

## References[[edit](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=8)]

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## External links[[edit](https://en.wikipedia.org/w/index.php?title=Second_Level_Address_Translation&action=edit&section=9)]

* [Method and system for a second level address translation in a virtual machine environment](http://www.freepatentsonline.com/7428626.html) (patent)
* [Second Level Address Translation Benefits in Hyper-V R2](http://www.virtualizationadmin.com/articles-tutorials/microsoft-hyper-v-articles/general/second-level-address-translation-benefits-hyper-v-r2.html)
* [Virtualization in Linux KVM + QEMU](http://www.cse.iitb.ac.in/~puru/courses/autumn12/cs695/classes/kvm-overview.pdf) (PDF)