Preliminary Data Sheet

SSV6060P

Single-Chip 802.11 b/g/n MAC/BB/Radio with SPI_MASTER Interface

General Description

The SSV6060P is a low-power single chip device providing for the highest level of integration for internet of thing embedded systems. It is designed to support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~MCS7, 20MHz, 800ns and 400ns guard interval.

It includes a 2.4 GHz WLAN CMOS efficient power amplifier (PA) and an internal low noise amplifier (LNA). The Radio Frequency Front-end is single-ended bi-directional input and output.

The SSV6060P has additional LDOs and DCDC buck convertor that could provide noise isolation for digital and analog supplies and excellent power efficient with minimum BOM cost.

The SSV6060P provides multiple peripheral interfaces including SPI_ MASTER, UART_DATA, UART_DEBUG, I2C_MASTER, SPI_DEBUG, etc.

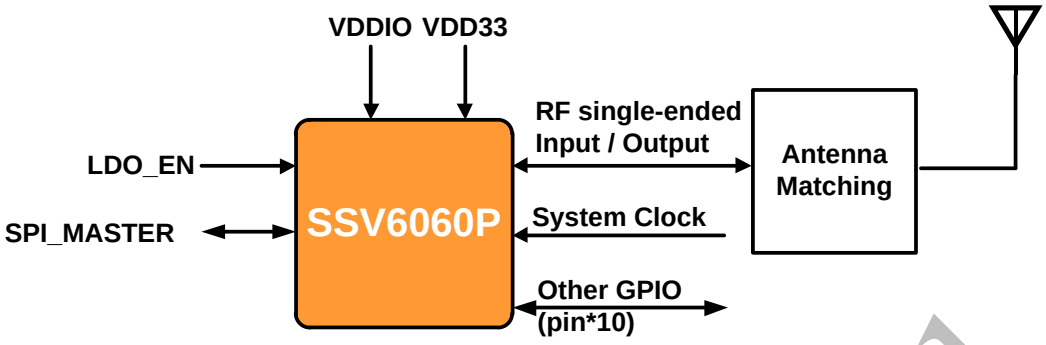
The only external clock source needed for SSV6060P based designs is a high speed crystal or oscillator. A variety of reference clocks are supported which include 19.2, 20, 24, 26, 38.4, 40 and 52 MHz

SSV6060P Features

- All CMOS IEEE 802.11 b/g/n single chip
- Single stream 802.11n provides highest throughput and superior RF performance for embedded system
- Advanced 1x1 802.11n features:
  - Full / Half Guard Interval
  - Frame Aggregation
  - Reduced Inter-frame Space (RIFS)
  - Space Time Block Coding (STBC)
  - Greenfield mode
- Integrated WLAN CMOS efficient power amplifier with internal power detector and closed loop power calibration

Device Package

6 x 6 mm, 0.4mm pitch QFN-48



SSV6060P System Block Diagram

Liability Disclaimer

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Revision History

Version	Date	Owner	Description
0.1	2015/06/18	HY Liao/ Chengyu Wang	Initial draft
0.2	2015/08/14	HY Liao/ Chengyu Wang	
0.3	2015/09/18	Chengyu Wang	
0.4	2015/11/02	Chengyu Wang	

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1: SYSTEM OVERVIEW

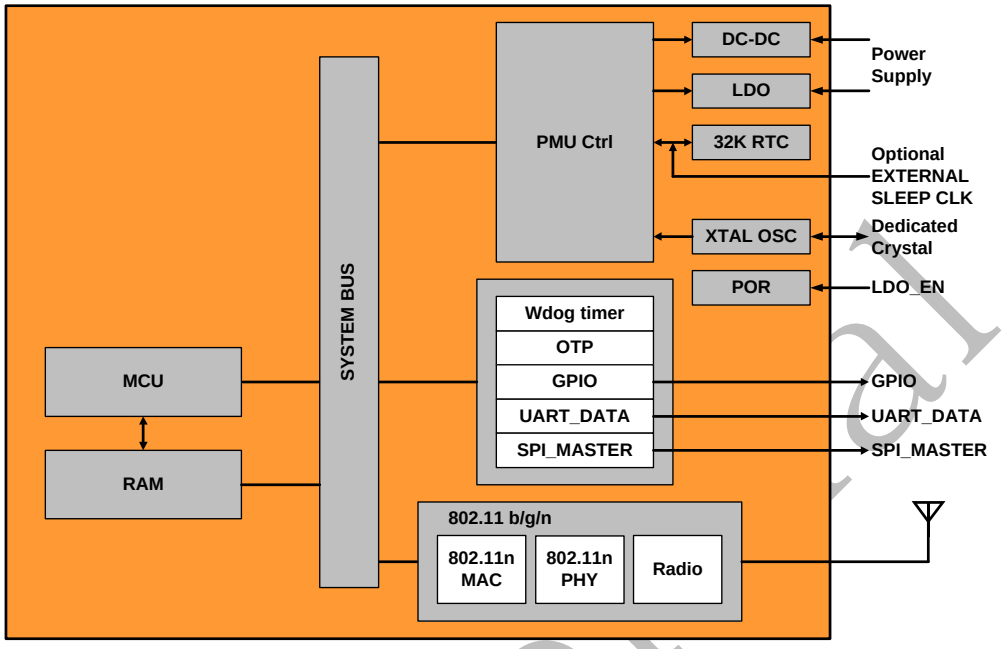


Figure 1-1: SSV6060P Block Diagram

1.1 General Description

The SSV6060P WLAN is designed to support IEEE 802.11 b/g/n single stream with the state of-the-art design techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The SSV6060P WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and achieve extreme low power consumption at sleep state to extend the battery life. The SSV6060P WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.

1.2 MAC Features

- 802.11 b/g/n/e/i/d
- WLAN/BT coexistence mechanisms
- 802.11n features
  - A-MPDU Tx & Rx
  - Support immediate Block-Ack
- AP/STA mode
  - Soft-AP
- Rate adaption mechanism

- WFA features
  - WEP/TKIP/WPA/WPA2
  - WMM/WMM PS
  - WPS 1.0 and 2.0
- WiFi Direct(P2P)

1.3 PHY features

- 802.11b, 11g, and 802.11n 1T1R
- Short Guard Interval
- Greenfield mode
- RIFS in RX mode
- STBC in RX mode
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle no-idealities effects from CMOS RF block

1.4 CPU

- 32-bit micro-controller
- Support 192 KB Instruction SRAM with Data SRAM in total.

1.5 GPIO

The SSV6060P has 10 GPIO pins with direct software access. These GPIO pins are GPIO_8, GPIO_1, GPIO_2, GPIO_3, GPIO_5, GPIO_6, GPIO_15, GPIO_18, GPIO_19 and GPIO_20. Many are multiplexed with other functions such as the host interface, UART_DEBUG, UART_DATA, I2C_MASTER, PWM, etc. Each GPIO supports the following configurations via software programming:

- Internal pull down option
- Input available for sampling by a software register
- Open-drain output driver

1.6 System Clocking and Reset

The SSV6060P has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

1.7 Design for Test

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2: POWER SUPPLIES AND POWER MANAGEMENT

2.1 General Description and PMU Power Connection

The power management unit (PMU) contains Under-Voltage Lockout (UVLO) circuit, Low Dropout Regulators (LDOs), buck DC-DC converter and reference bandgap circuit.

The PMU integrated multi-LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line / load regulation, ripple rejection and output noise.

The input voltage of the buck converter is 3.3V. Its output voltage is 1.6V and feeds into the input power of the RF circuit and DLDO which has 1.2V output voltage for all digital circuits.

There is only one PALDO for Tx PA, ANTSEL IO power with output voltage of 3.3V. There is also one dedicated LDO which provides 3.3V output voltage for RF blocks.

Figure 2-1 shows the typical power connection for SSV6060P. DLDO and some RF circuits are powered by the buck converter output. The VDDIO is a power input which may be 1.8V, 2.5V or 3.3V from the host side. The connection structure is shown in the figure below.

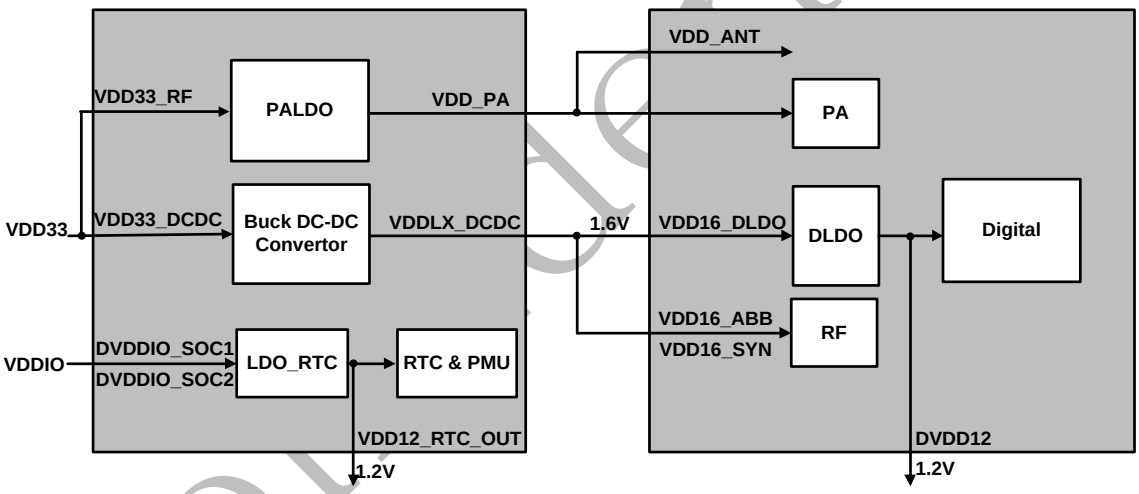


Figure 2-1: SSV6060P Power Connection

2.2 Under-Voltage Lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the battery is below pre-defined threshold. It ensures that SSV6060P is powered on with the battery in good condition. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself to prevent further discharging.

2.3 PALDO

PA_LDO converts the supply input to a 3.3V supply for using WLAN transmitter circuits including PA. It is optimized for high-performance and adequate quiescent current.

2.4 DLDO

The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.6V input to 1.2V output which suits the digital circuits. The input is typically connected to the buck's output.

2.5 Buck Converter

The regulator is a DC-DC step-down converter (buck converter) to source 300mA (max.) with 2.0V to 1.5V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

2.6 Power Management Control

There are three power modes that SSV6060P operates when it is initialized: HOST_OFF, ACTIVE mode and SLEEP mode. There are two intermediate system transition modes: FW_DOWNLOAD and WARM_UP mode. The following are the brief introduction to each mode.

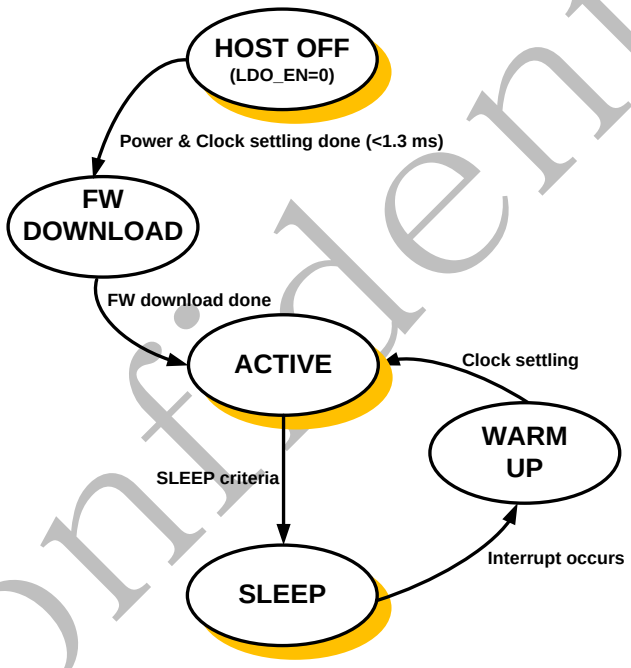


Figure 2-2: SSV6060P Power State

Table 2-1: SSV6060P Power State Description

State	Description
HOST OFF	When **LDO_EN** pin is de-asserted and logically low, the chip is brought to this state immediately.
	Sleep clock and internal power supply is disabled.
	After **LDO_EN** pin is asserted, the internal power and clock will be settled down within 1.3 ms.
FW DOWNLOAD	States for firmware download after power and clock is settled down.
SLEEP	The host controller can determine when to enter sleep to turn off most circuit in SSV6060P. All the RF, DPLL circuits are turned off. In sleep mode, the system could be awakened after the sleep time is expired or by an external wake up signal from the host controller.
	All internal states are maintained and the Crystal oscillator is disabled.
WARM UP	The system transitions from SLEEP to ACTIVE. The crystal or oscillator is brought up and the PLL is enabled.
ACTIVE	The high speed clock is operational and sent to each block by the clock control register.
	The RF circuit is enabled to transmit or receive data, and the whole system is under normal operation.

2.7 Power-on Sequence

Figure 2-3 shows the power-on sequence of the SSV6060P from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the SSV6060P or pulsed low to induce a subsequent reset. After LDO_EN is assert and host starts the power-on sequence of the SSV6060P. From that point, the typical SSV6060P power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

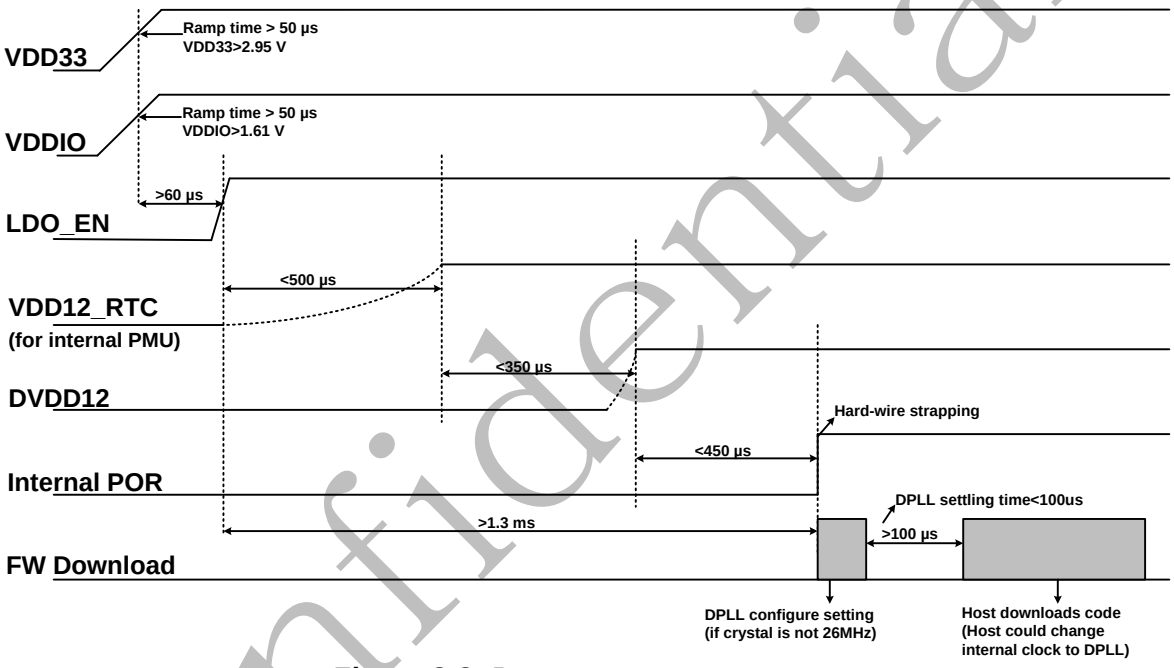


Figure 2-3: Power-on sequence

2.8 Reset Control

The SSV6060P **LDO_EN** pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SSV6060P is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SSV6060P turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

4: DC CHARACTERISTICS

3.1 Absolute Maximum Ratings

The absolute maximum ratings in Table 4-1 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 4-1: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
VDD16_ABB	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD16_SYN	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD_ANT	VDD input for external components I/O control	-0.3 to 3.6	V
EFUSE_VDD	VDD input for EFUSE burn-in. Pull low when read mode	-0.3 to 2.75	V
DVDDIO_SOC1	VDD input for GPIO pins	-0.3 to 3.6	V
DVDD12	VDD output for internal digital circuit	-0.3 to 1.32	V
VDD16_DLDO	VDD input for digital circuit	-0.3 to 3.6	V
VDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V
VDD12_RTC_OUT	VDD output for internal RTC circuit	-0.3 to 1.43	V
DVDDIO_SOC2	VDD input for GPIO pins (same level as DVDDIO_SOC1)	-0.3 to 3.6	V
VDD33_RF	VDD input for RF circuit	-0.3 to 3.6	V
VDD_PA	VDD output for internal PA	-0.3 to 3.6	V

3.2 Environmental Ratings

The environmental ratings are shown in Table 4-2

Table 4-2 Environmental Ratings

Characteristic	Conditions/Comments	Value	Units
Ambient Temperature (T_A)	Functional operation	-20 to +85	˚C
Storage Temperature	-	-40 to +125	˚C
Relative Humidity	Storage	Less than 60	%
	Operation	Less than 85	%

3.3 PMU Under Voltage Lock-out (UVLO) Characteristics

Table 4-3 PMU UVLO characteristics

Symbol (domain)	Description	Min.	Typ.	Max.	Unit
Under Voltage Lock-Out (UVLO)					
Under voltage rising threshold of VBAT	VDD33: pin VDD33_DCDC & VDD33_RF		2.95		V
Under voltage falling threshold of VBAT	VDD33: pin VDD33_DCDC & VDD33_RF		2.85		V
Under voltage rising threshold of DVDDIO	DVDDIO: pin DVDDIO_SOC1 & DVDDIO_SOC2		1.6		V
Under voltage falling threshold of DVDDIO	DVDDIO: pin DVDDIO_SOC1 & DVDDIO_SOC2		1.5		V

3.4 Electrostatic Discharge Specifications

This is an ESD sensitive product! Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Table 4-4: ESD Specifications

Pin Type	Test Condition	ESD Rating	Unit
Human Body Mode (HBM)	refers to MIL-STD-883G Method 3015.7	Pass ±2.5	KV
Machine Mode (MM)	refers to JEDEC EIA/JESD22-A115	Pass ±250	V

3.5 Recommended Operating Conditions and DC Characteristics

Table 4-5: Recommended Operating Conditions and DC Characteristics

Symbol (domain)	Description	Min.	Typ.	Max.	Unit
VDD16_ABB	VDD input for analog 1.6V		1.6		V
VDD16_SYN	VDD input for analog 1.6V		1.6		V
VDD_ANT	VDD input for external components I/O control		3.3		V

EFUSE_VDD	VDD input for EFUSE burn-in. Pull low when read mode	2.25	2.5	2.75	V
DVDDIO_SOC1	VDD input for GPIO pins	1.71	1.8/2.5/3.3	3.46	V
DVDD12	VDD output for internal digital circuit		1.2		V
VDD16_DLDO	VDD input for digital circuit's LDO		1.6		V
VDD33_DCDC	VDD input for DCDC		3.3		V
VDD12_RTC_OUT	VDD output for internal RTC circuit		1.3		V
DVDDIO_SOC2	VDD input for GPIO pins (same level as DVDDIO_SOC1)	1.71	1.8/2.5/3.3	3.46	V
VDD33_RF	VDD input for RF circuit		3.3		V
VDD_PA	VDD output for internal PA		3.3		V

5: FREQUENCY REFERENCES

5.1 Crystal Oscillator Specifications

Table 5-1: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
Crystal load Capacitance	–	–	10		pF
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm

5.2 External Clock-Requirements and Performance

Table 5-1: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
OSCIN Input Voltage	AC-couple analog signal	400	–	1500	mV_{PP}
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm
Duty Cycle	26MHz clock	40	50	60	%
Phase Noise (802.11b/g)	26MHz clock at 1KHz offset	–	–	–119	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–129	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–134	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–139	dBc/Hz
Phase Noise (802.11n 2.4GHz)	26MHz clock at 1KHz offset	–	–	–125	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–135	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–140	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–145	dBc/Hz

6: Electrical Specifications

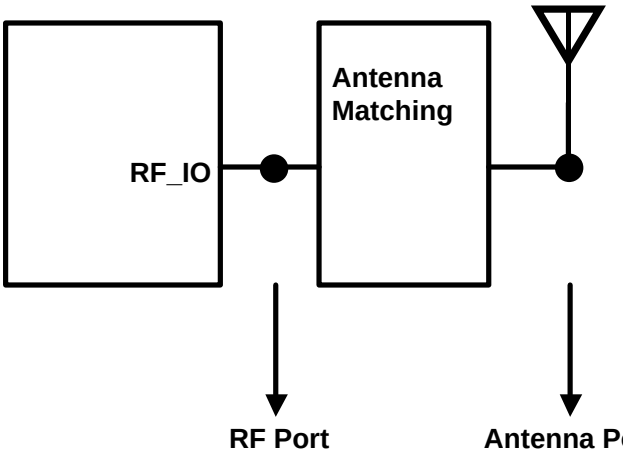


Figure 6-1: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the Antenna Port unless otherwise specified.

6.1 WLAN RF Performance Specifications

Table 6-1: WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-95.5		dBm
	CCK, 2 Mbps		-93.5		dBm
	CCK, 5.5 Mbps		-91.0		dBm
	CCK, 11 Mbps		-88.0		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.5		dBm
	OFDM, 9 Mbps		-90.0		dBm
	OFDM, 12 Mbps		-88.0		dBm
	OFDM, 18 Mbps		-86.0		dBm
	OFDM, 24 Mbps		-82.5		dBm
	OFDM, 36 Mbps		-79.5		dBm
	OFDM, 48 Mbps		-74.5		dBm
	OFDM, 54 Mbps		-73.5		dBm
Rx Sensitivity (HT20) Greenfield 800nS GI Non-STBC	HT20, MCS0		-91.0		dBm
	HT20, MCS1		-88.0		dBm
	HT20, MCS2		-86.0		dBm
	HT20, MCS3		-81.5		dBm
	HT20, MCS4		-79.0		dBm
	HT20, MCS5		-74.5		dBm
	HT20, MCS6		-73.5		dBm
	HT20, MCS7		-72.5		dBm
RX Adjacent Channel Rejection (CCK)	CCK, 1 Mbps (30 MHz offset)		41		dB

	CCK, 11 Mbps (25 MHz offset)		41		dB
RX Adjacent Channel Rejection (OFDM)	OFDM, 6 Mbps (25 MHz offset)		39		dB
	OFDM, 54 Mbps (25 MHz offset)		23		dB
RX Adjacent Channel Rejection (HT20)	HT20, MCS0 (25 MHz offset)		38		dB
	HT20, MCS7 (25 MHz offset)		21		dB
TX Output Power	CCK, 1-11 Mbps		19		dBm
	OFDM, 54 Mbps		16		dBm
	HT20, MCS7		15		dBm

7: System Power Consumption

Note: All results are measured at the antenna port and VBAT is 3.3V and DCDC buck convertor is enabled.

Table 7-1: System Power Consumption

WLAN Operational Modes	Typ.	Unit
OFF[a]	4	uA
Rx, CCK, 1 Mbps	60	mA
Rx, OFDM, 54 Mbps	66	mA
Rx, HT20, MCS7	67	mA
Sleep	200	uA
Rx Power Saving, DTIM= 1	1.2	mA
Tx, CCK, 1 Mbps, 19dBm	282	mA
Tx, OFDM, 54 Mbps, 16dBm	218	mA
Tx, HT20, MCS7, 15dBm	223	mA

a. Test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V

8: Pin Descriptions

This section contains a listing of the signal descriptions (see Figure 8-1 for the SSV6060P QFN package pin-out)

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name, indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 6-1:

IA	Analog input signal
I	Digital input signal
IO	Digital bidirectional signal
IOA	Analog bidirectional signal
O	Digital output signal
P	Power signal
G	Ground signal

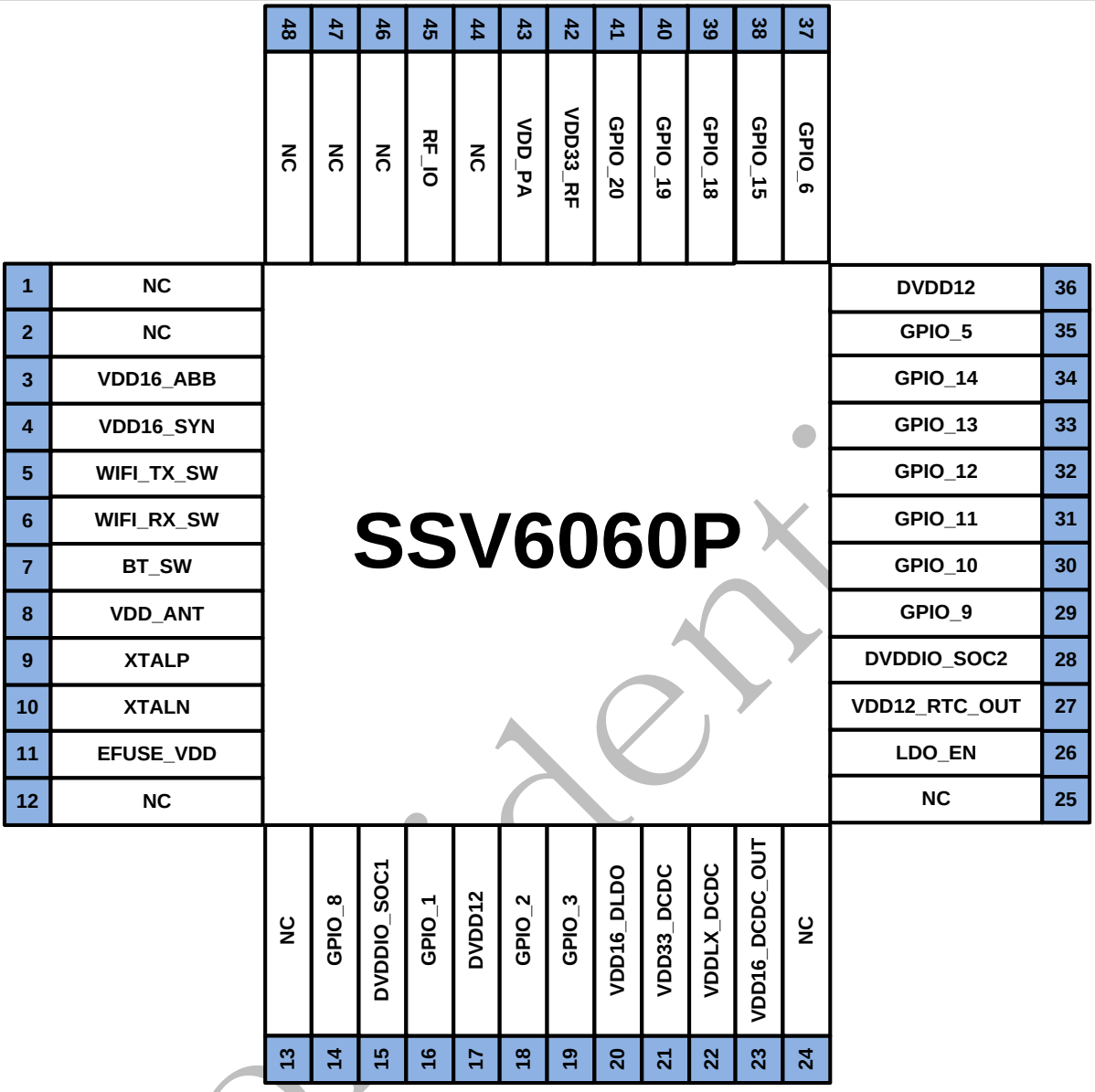


Figure 8-1: SSV6060P QFN Pin Assignment (top view)

Table 8-1: SSV6060P Package Pin-out

No.	Name	Description	Type (default)
1	**NC**	No connection	NC
2	**NC**	No connection	NC
3	**VDD16_ABB**	Analog 1.6V supply	P
4	**VDD16_SYN**	Analog 1.6V supply	P
5	**WIFI_TX_SW**	Control signal for external WiFi Tx switch or WiFi switch (**WIFI_SW**)	I
6	**WIFI_RX_SW**	Control signal for external WiFi Rx switch	I
7	**BT_SW**	Control signal for external BT switch	I
8	**VDD_ANT**	External components control I/O supply	P
9	**XTALP**	Crystal input	IA
10	**XTALN**	Crystal input or external reference clock input	IA
11	**EFUSE_VDD**	EFUSE burn-in supply	P
12	**NC**	No connection	NC
13	**NC**	No connection	NC
14	**GPIO_8**	GPIO pin	O
15	**DVDDIO_SOC1**	SOC1 GPIO I/O supply	P
16	**GPIO_1**	GPIO pin	O
17	**DVDD12**	Digital 1.2V supply	P
18	**GPIO_2**		I
19	**GPIO_3**		I
20	**VDD16_DLDO**	Digital 1.6V supply	P
21	**VDD33_DCDC**	DCDC 3.3V supply	P
22	**VDDLX_DCDC**	Buck converter feedback	P
23	**VDD16_DCDC_OUT**	Buck converter 1.6V output	P
24	**NC**	No connection	NC
25	**NC**	No connection	NC
26	**LDO_EN**	Reset signal to power down the SSV6060P	I
27	**VDD12_RTC_OUT**	RTC 1.2V supply	P
28	**DVDDIO_SOC2**	SOC2 GPIO I/O supply	P
29	**GPIO_9**	SPI_MASTER_MOSI	
30	**GPIO_10**	SPI_MASTER_CSN	
31	**GPIO_11**	SPI_MASTER_NC	
32	**GPIO_12**	SPI_MASTER_WP	
33	**GPIO_13**	SPI_MASTER_MISO	
34	**GPIO_14**	SPI_MASTER_CLK	
35	**GPIO_5**		I
36	**DVDD12**	Digital 1.2V supply	P
37	**GPIO_6**		I
38	**GPIO_15**		O
39	**GPIO_18**		O
40	**GPIO_19**		I
41	**GPIO_20**	GPIO pin	O
42	**VDD33_RF**	RF 3.3V supply	P

43	**VDD_PA**	PA supply	P
44	**NC**	No connection	NC
45	**RF_IO**	2.4 GHz RF input & output port	IOA
46	**NC**	No connection	NC
47	**NC**	No connection	NC
48	**NC**	No connection	NC

Table 8-2 shows the others GPIO hardware functions except HOST control interface pins. These functions could be selected by GPIO register setting.

There are two UART functions which are UART_DATA and UART_DEBUG. UART_DATA mode has four pins with flow control: UART_DATA_RTS, UART_DATA_CTS, UART_DATA_RXD and UART_DATA_TXD. On the other hands, UART_DEBUG has only two pins: UART_DEBUG_TXD and UART_DEBUG_RXD.

Table 8-2: SSV6060P GPIO Hardware Function

Pin Name	GPIO hardware function	
GPIO_8	PWM_HW	
GPIO_1	I2C_MASTER_SCL	UART_DEBUG_TXD
GPIO_2		
GPIO_3	I2C_MASTER_SDA	UART_DEBUG_RXD
GPIO_5	UART_DATA_RTS	UART_DEBUG_TXD
GPIO_6	UART_DATA_CTS	UART_DEBUG_RXD
GPIO_15		
GPIO_18		
GPIO_19	UART_DATA_RXD	
GPIO_20	UART_DATA_TXD	

Table 8-3 shows GPIO pins' default output status. The GPIO pins have programmable IO selection shown column 3. The default output status of these GPIO pins are shown in column 4 and 6.

Table 8-3: SSV6060P GPIO default output status

Pin Name	Programmable IO Selection	Output Status (before POR)	Default IO Type (after POR)	Output Status (after POR)
GPIO_8	I/O/IO	weakly pulled low	I	weakly pulled low

GPIO_1	I/O/IO	weakly pulled low	O	Low
GPIO_2	I/O/IO	None	I	None
GPIO_3	I/O/IO	None	I	None
GPIO_5	I/O/IO	weakly pulled high	I	weakly pulled high
GPIO_6	I/IO	None	I	None
GPIO_15	I/O/IO	None	O	Low
GPIO_18	I/O/IO	High	O	High
GPIO_19	I/O/IO	None	I	None
GPIO_20	I/O/IO	weakly pulled low	O	Low

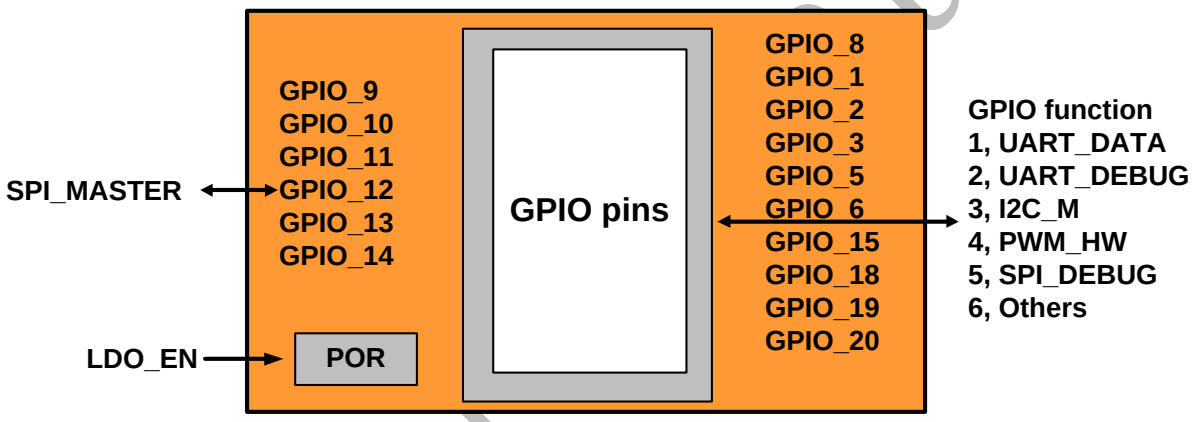
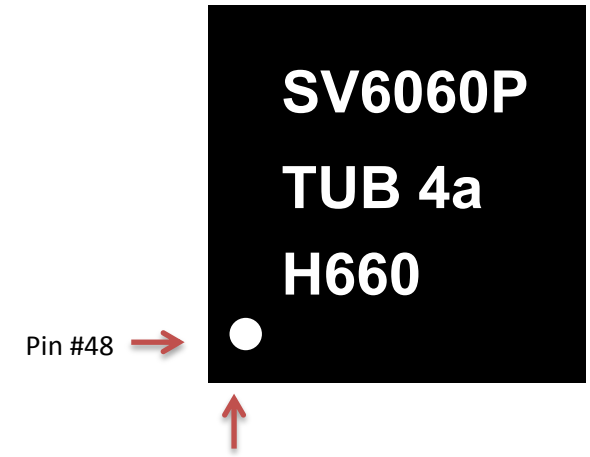


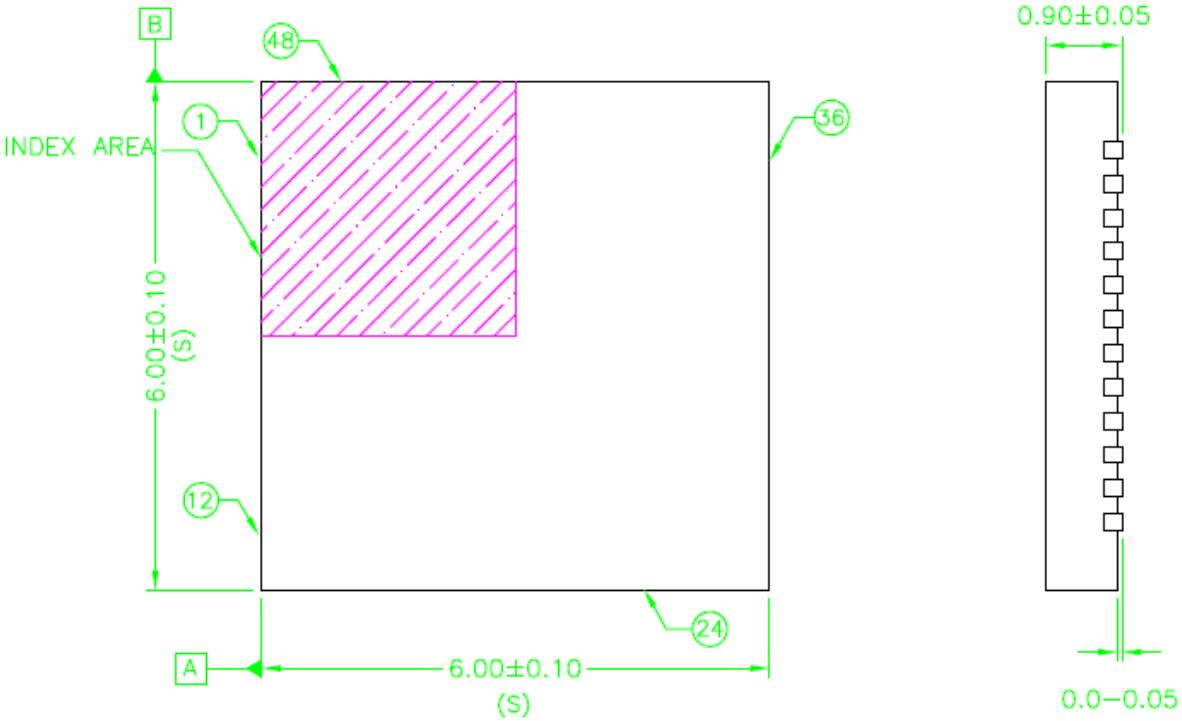
Figure 8-1: SSV6060P GPIO usage

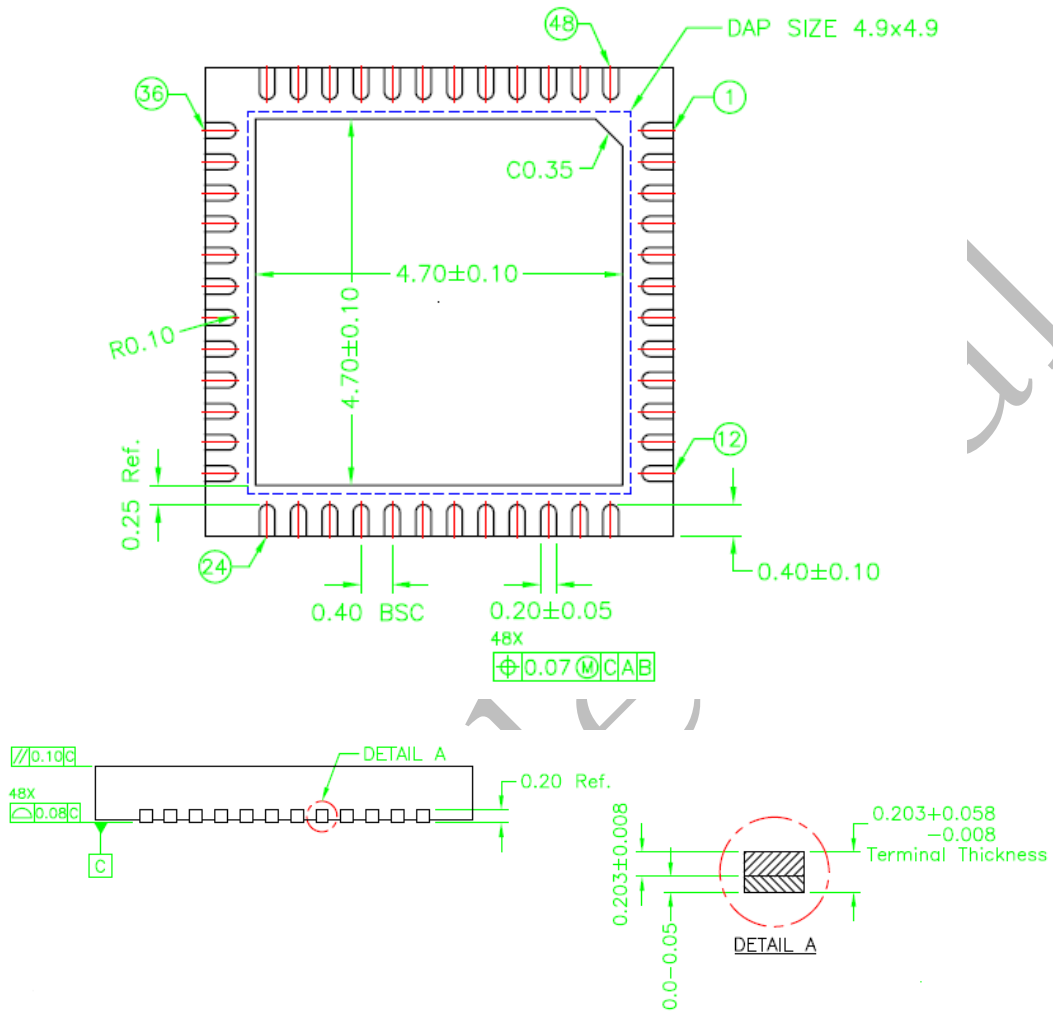
9: PACKAGE INFORMATION

6 x 6 mm (body size), 0.4mm pitch QFN-48

Marking format (top view)







NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. L/F STOCK# FR9012 (PPF)

Figure 9-1: SSV6060P QFN 6 x 6 mm Package Dimensions

10: ORDERING INFORMATION

Part Number	Package
SSV6060P	QFN 48, 6x6 mm