HDL Code Generation Check Report for 'untitled1' open model 'untitled1'
Generated on 2022-06-11 22:48:38

HDL check for 'untitled1' complete with 3 errors, 0 warnings, and 0 messages.

The following table describes blocks for which errors, warnings or messages were reported.

Simulink Blocks and resources	Level	Description
untitled1/TmpGroundAtBPSK Modulator BasebandInport1	Error	Signals of type 'Double' will not generate synthesizable HDL. For synthesizable HDL code, set the "Library" option to "Native Floating Point". For non-synthesizable and simulation-only HDL code, set the "Check for presence of reals in generated HDL code" diagnostic to "Warning" or "None".
untitled1/BPSK Modulator Baseband	Error	The block does not support mixing double, single, half, and/or non-real types at the ports. Use either all the same floating point type or no floating point types.
untitled1/BPSK Modulator Baseband	Error	HDL code generation for PSK Modulation is not supported for Double and Single data types. Convert the data types to fixed-point.