Design Rule Verification Report

Date:	7/5/2020
Time:	12:02:22 PM
Elapsed Time:	00:00:00
Filename:	C:\Users\Public\Documents\Altium\Projects\Bluetooh_Project\PCB1.PcbDoc

Warnings:	0
Rule Violations:	0

Summary

Warnings	**Count**
Total	**0**

Rule Violations	**Count**
Clearance Constraint (Gap=0mm) (OnLayer('Keep-Out Layer')),(OnLayer('Keep-Out Layer'))	0
Clearance Constraint (Gap=0.2mm) (All And Not OnLayer('Keep-Out Layer')),(All And Not OnLayer('Keep-Out Layer'))	0
Clearance Constraint (Gap=0.254mm) (InNamedPolygon('Ground')),(IsVia And AsMM(HoleDiameter) >= 3)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.3mm) (Max=1mm) (Preferred=0.3mm) (All)	0

Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) (Entries=4) (All)	0
Hole Size Constraint (Min=0.55mm) (Max=3.2mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.05mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.01mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.01mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	**0**