Solutions to *The Art of Electronics 3rd Edition*

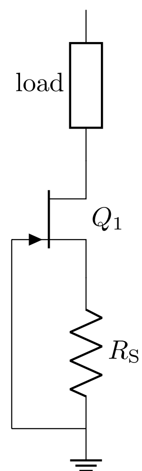
April 14, 2024

Contents

Solutions for Chapter 3

Exercise 3.1

Figure 1.1: JFET current source



From Figure 3.21 of the book, one can see that a drain current equal to 1 mA corresponds to a gate-source voltage of −0.6 V. Therefore:

$$\boxed{R_S = \frac{0.6\,\mathrm{V}}{1\,\mathrm{mA}} = 600\,\Omega}$$

Exercise 3.2

At $V_{GS} = V_{G0}$:

$$r_{GS} = r_{G0} = \frac{1}{2k\left(V_{G0} - V_{th}\right)}$$

The ratio between r_{DS} and R_{G0} returns:

$$\boxed{\frac{r_{DS}}{r_{G0}} = \frac{2k\left(V_{G0} - V_{th}\right)}{2k\left(V_{GS} - V_{th}\right)}}$$

Exercise 3.3

Being g_{m} the differential conductance of the FET operated in aturation region, it can be expressed as:

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}} = \frac{\partial}{\partial V_{\mathrm{GS}}} k \left(V_{\mathrm{GS}} - V_{\mathrm{th}}\right)^2 = 2k \left(V_{\mathrm{GS}} - V_{\mathrm{th}}\right)$$

Therefore:

$$\boxed{g_{\mathrm{m}} = \frac{1}{r_{\mathrm{DS}}}}$$

Exercise 3.4

(a) The voltage change across the drain-gate capacitance when the JFET is switched on ($V_{\mathrm{DS}} = 0\,\mathrm{V}$) is equal to 50 V-(0 V-10 V)=60 V. Considering a maximum current across this capacitance equal to 1 A:

$$\boxed{t_{\mathrm{ON}} = \frac{60\,\mathrm{V}\,200\,\mathrm{pF}}{1\,\mathrm{A}} = 12\,\mathrm{ns}}$$

(b) Since the current is equal to the charge over time, we have:

$$\boxed{t_{\mathrm{ON}} = \frac{40\,\mathrm{nC}}{1\,\mathrm{A}} = 40\,\mathrm{ns}}$$

Exercise 3.5

The 1 pF drain-source capacitance happens to be in series with the 10 kΩ load resistance. The capacitive reactance is:

$$X_{\mathrm{DS}} = \frac{1}{2\pi 1\,\mathrm{MHz}\,1\,\mathrm{pF}} = 160\,\mathrm{k\Omega}$$

Therefore, the feedthrough is given by:

$$\boxed{20\log_{10}\frac{10\,\mathrm{k\Omega}}{10\,\mathrm{k\Omega} + 160\,\mathrm{k\Omega}} = -25\,\mathrm{dB}}$$

Exercise 3.6

In this case, the output 10 kΩ resistance is in parallel with the 50 Ω R_{ON} resistance. Their equivalent resistance is about 50 Ω. Similarly to the previous exercise, the feedthorugh is given by:

$$\boxed{20\log_{10}\frac{50\,\Omega}{50\,\Omega + 160\,\mathrm{k\Omega}} = -70\,\mathrm{dB}}$$

Exercise 3.7

Figure 1.2: Zero ohm R_{ON}

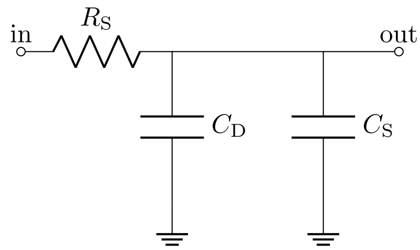
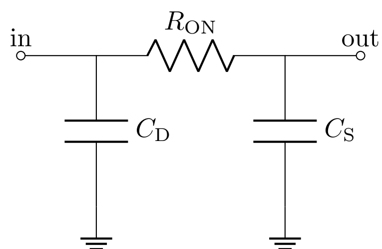


Figure 1.3: $75\,\Omega$ R_{ON}



For this exercise we assume that the load resistance of $100\,\mathrm{k}\Omega$ does not load the circuit.

(a) The circuit is that of Figure 1.2. Since $C_{\mathrm{D}} = C_{\mathrm{S}} = C_{\mathrm{T}} = 8\,\mathrm{pF}$, there is a single pole at the frequency f_{p}:

$$\boxed{f_{\mathrm{p}} = \frac{1}{4\pi R_{\mathrm{S}} C_{\mathrm{T}}} \approx 1\,\mathrm{MHz}}$$

(b) In this case the circuit is depicted in Figure 1.3. The circuit has one pole at DC and another pole at f_{p}:

$$\boxed{f_{\mathrm{p}} = \frac{1}{2\pi R_{\mathrm{ON}} C_{\mathrm{T}}} \approx 265\,\mathrm{MHz}}$$

Exercise 3.8

Figure 1.4: OFF-OFF

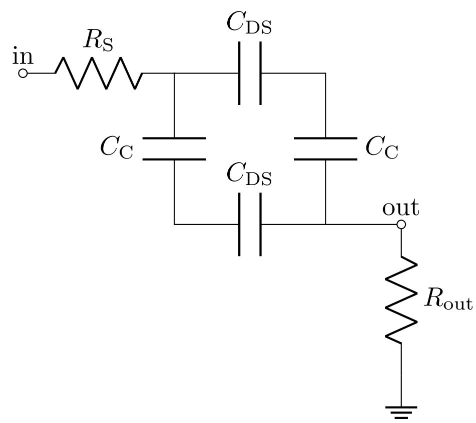


Figure 1.5: OFF-ON

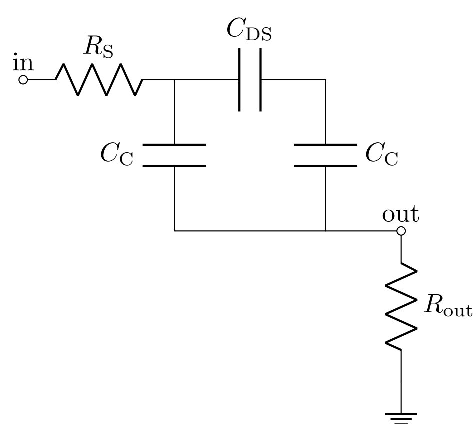


Figure 1.6: ON-OFF

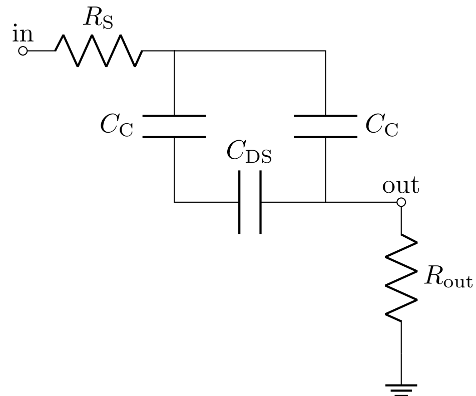
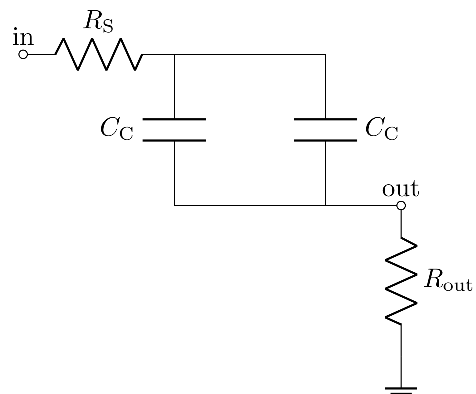


Figure 1.7: ON-ON



(a) In this case the reference circuit is depicted in Figure 1.4. The cross-coupling is given by:

$$\boxed{20\log_{10}\frac{R_{out}}{R_{out}+R_S+0.5(X_C+X_{DS})}=-10.75\,\mathrm{dB}}$$

being $X_C=\frac{1}{2\pi f\,C_C}=320\,\mathrm{k}\Omega$ and $X_{DS}=\frac{1}{2\pi f\,C_{DS}}=160\,\mathrm{k}\Omega$

(b) In this case the reference circuit is depicted in Figure 1.5. The cross-coupling is given by:

$$\boxed{20\log_{10}\frac{R_{out}}{R_{out}+R_S+\frac{X_C(X_C+X_{DS})}{2X_C+X_{DS}}}=-9.6\,\mathrm{dB}}$$

(c) In this case the reference circuit is depicted in Figure 1.6. The cross-coupling is the same as before

(d) In this case the reference circuit is depicted in Figure 1.7. The cross-coupling is given by:

$$\boxed{20\log_{10}\frac{R_{out}}{R_{out}+R_S+0.5X_C}=-8.6\,\mathrm{dB}}$$

Exercise 3.9

(a) Considering the different combinations of resistors, the $-3\,\mathrm{dB}$ frequencies can be computed as:

$$\boxed{f_{\mathrm{3dB,n}} = \frac{n\,G_{\mathrm{10k}}}{2\pi C} \quad n = 1\ldots 15}$$

where $C = 0.01\,\mathrm{\mu F}$ and $G_{\mathrm{10k}} = 0.1\,\mathrm{mS}$

(b) The glitch amplitude voltage can be computed as:

$$\boxed{\Delta V = \frac{20\,\mathrm{pC}}{C} = 2\,\mathrm{mV}}$$

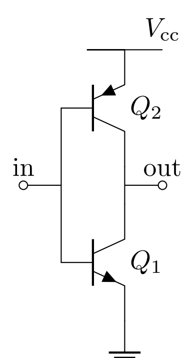
Exercise 3.10

The peak output current that the buffer has to provide can be given as the peak time derivative of the output voltage across the $10\,\mathrm{nF}$ capacitor multiplied by its value:

$$\boxed{I_{\mathrm{p}} = 10\,\mathrm{nF}\left.\frac{dV}{dt}\right|_{\mathrm{p}} = 10\,\mathrm{nF}\,2\pi 10\,\mathrm{kHz}\,1\,\mathrm{V} = 0.6\,\mathrm{mA}}$$

Exercise 3.11

Figure 1.8: BJT-based inverter logic circuit



The circuit of Figure 1.8 represents the complementary bjt inverter. It's easy to see that without a proper bias, if the input is grounder (low level) the V_{BE} of the pnp transistor is equal to V_{cc} which is likely to damage the transistor in a very short time

Exercise 3.12

Figure 1.9: Logic AND symbols

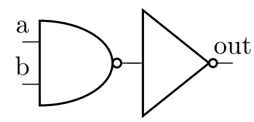
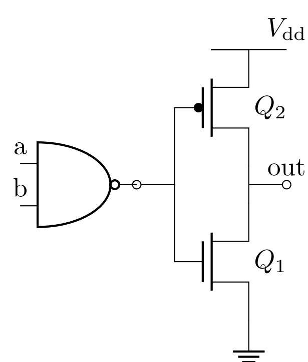


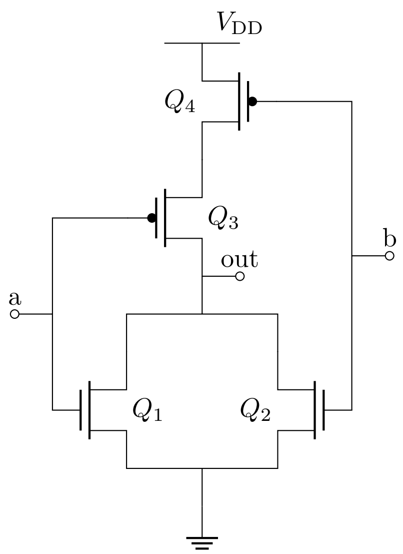
Figure 1.10: Logic AND symbol and circuit



In order to transform a NAND port into an AND port, we can use a NOT port as shown in Figures 1.9 and 1.10

Exercise 3.13

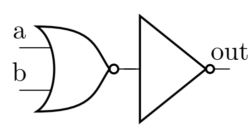
Figure 1.11: NOR circuit



The solution is presented in Figure 1.11

Exercise 3.14

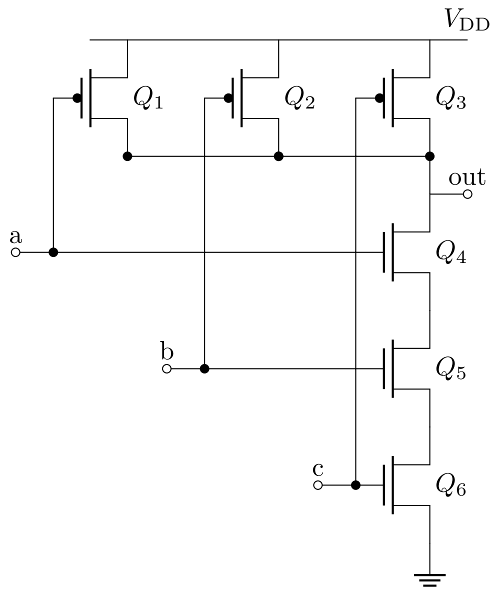
Figure 1.12: Logic OR symbols



The OR circuit can be easily obtained by cascading a NOT circuit to the NOR circuit designed in exercise 3.13.

Exercise 3.15

Figure 1.13: Three ports NAND circuit



The solution is represented in Figure 1.13. The gate comply with the following truth table

a	b	c	out
1	1	1	0
1	1	0	1
1	0	0	1
1	0	1	1
0	0	1	1
0	1	0	1
0	1	1	1
0	0	0	1

Exercise 3.16

As soon as the voltage across R_5 gets higher than the V_{EB} threshold of Q3, a current starts flowing from its emitter to its collector. As long as Q1 does not saturate, its collector current is fixed (current sink) and Q3 collector current flows into R_2. This increases V_{SG} of Q2 until it becomes higher than its threshold $V_{\text{SG}}^{\text{th}}$ The maximum allowed current $I_{\text{S}}^{\max}$ can be computed as it follows:

$$I_{\text{C}}^{\text{Q1}} = \frac{3.3\,\text{V} - 0.65\,\text{V}}{15\,\text{k}\Omega} = 0.18\,\text{mA}$$

Therefore:

$$V_{\text{SG}}^{\text{th}} = (I_{\text{C}}^{\text{Q1}} - I_{\text{C}}^{\text{Q3}})R_2 - R_5 I_{\text{lim}}$$

Since:

$$I_{\text{C}}^{\text{Q3}} = I_{\text{S}} e^{\frac{I_{\text{lim}} R_5}{V_{\text{T}}}}$$

One can obtain, by substituting $I_{\mathrm{C}}^{\mathrm{Q3}}$ in the expression for $V_{\mathrm{SG}}^{\mathrm{th}}$:

$$V_{\mathrm{SG}}^{\mathrm{th}} = (I_{\mathrm{C}}^{\mathrm{Q1}} - I_{\mathrm{S}} e^{\frac{I_{\mathrm{lim}} R_5}{V_{\mathrm{T}}}}) R_2 - R_5 I_{\mathrm{lim}}$$

This equation can be solved numerically and it gives $I_{\mathrm{lim}} = 1.25\,\mathrm{A}$ if $V_{\mathrm{SG}}^{\mathrm{th}} = 5\,\mathrm{V}$ or $I_{\mathrm{lim}} = 1.29\,\mathrm{A}$ if $V_{\mathrm{SG}}^{\mathrm{th}} = 0\,\mathrm{V}$. In both cases, the V_{EB} of Q3 is approximately it diode voltage drop 0.65 V. Therefore, I_{lim} can be approximately obtained is a easire way as:

$$\boxed{I_{\mathrm{lim}} = \frac{0.65\,\mathrm{V}}{R_5} = 1.3\,\mathrm{V}}$$

Exercise 3.17

From the exercise data we have the following requirements:

- Q2 $V_{\mathrm{SD}}^{\mathrm{max}} = 175\,\mathrm{V}$
- $V_{\mathrm{CE}}^{\mathrm{max}} = 175\,\mathrm{V}$
- $V^{\mathrm{LED}} = 38\,3.2\,\mathrm{V} = 121.6\,\mathrm{V}$
- Q2 $I_{\mathrm{SD}}^{\mathrm{max}} = 0.5\,\mathrm{A}$

From Table at page 202 we see that the p-channel MOSFET FQP9P25 is suitable. Looking at the datasheet we see that the $V_{\mathrm{GS}}^{\mathrm{th}} = -5\,\mathrm{V}$ and $R_{\mathrm{ON}} = 0.62\,\Omega$. Aiming for a V_{GS} about $-10\,\mathrm{V}$, we can compute the ratio of R_2 and R_1 as:

$$\frac{R_2}{R_1} = \frac{10\,\mathrm{V}}{3.3\,\mathrm{V} - 0.65\,\mathrm{V} = 3.77}$$

Since the minimum supply voltage is equal to 155 V, we have to account for a resistor in series with the led equal to:

$$\frac{155\,\mathrm{V} - 121.6\,\mathrm{V}}{0.5\,\mathrm{A}} = 67\,\Omega$$

From the previous exercise, if we want to limit the drain current through Q2 at 0.5 A, we should use a resistor R_5 equal to

$$R_5 = \frac{0.65\,\mathrm{V}}{0.5\,\mathrm{A}} = 1.3\,\Omega$$

For the transistor Q1, from Table 2.1 at page 74 we choose the model MPSA92 whose maximum collector current is equal to 30 mA and maximum power 625 mW. The maximum power thorugh Q1 can be obtained as:

$$P^{Q1} = V_{\mathrm{CE}} I_{\mathrm{C}} = [175\,\mathrm{V} - I_{\mathrm{C}}(R_1 + R_2)] I_{\mathrm{C}} \leq 625\,\mathrm{mW}$$

Since:

$$I_{\mathrm{C}} = \frac{3.3\,\mathrm{V} - 0.65\,\mathrm{V}}{R_1}$$

Accounting for a Q1 power of 500 mW:

$$R_1 = 860\,\Omega$$

and

$$R_2 = 3.77\,R_1 = 3.2\,\mathrm{k}\Omega$$

The maximum power dissipated by Q2 can be easily computed accounting for a maximum drain current ($I_{\mathrm{D}}^{\mathrm{Q2}}$) equal to 0.5 A:

$$P^{\mathrm{Q2}} = {I_{\mathrm{D}}^{\mathrm{Q2}}}^2 R_{\mathrm{ON}} = 155\,\mathrm{mW}$$

Finally, from the datasheet of the FQP9P25 MOSFET, for a single 10 ms pulse, the tehermal impedance from junction to case is equal to $0.3\,°\mathrm{C}\,\mathrm{W}^{-1}$. Supposing that the case thermal capacitance is such as the case temperature is not affected by the 10 ms pulse, the junction temperature increase will be equal to:

$$\Delta T^{\mathrm{Q2}} = 0.3\,°\mathrm{C}\,\mathrm{W}^{-1}\,155\,\mathrm{mW} = 0.04\,°\mathrm{C}$$

However, if we account for a continous 10 ms pulse with 0.5 duty cycle, the tehermal impedance from junction to case becomes equal to $0.5\,°\mathrm{C}\,\mathrm{W}^{-1}$. If we neglect the case thermal capacitance, the junction temperature increase will be equal to:

$$\Delta T^{\mathrm{Q2}} = (0.5\,°\mathrm{C}\,\mathrm{W}^{-1} + 1.04\,°\mathrm{C}\,\mathrm{W}^{-1})\,155\,\mathrm{mW} = 0.24\,°\mathrm{C}$$

where $1.04\,°\mathrm{C}\,\mathrm{W}^{-1}$ is the thermal resistance from case to ambient as given in the datasheet.

Exercise 3.18 TODO: write solution