Solutions to *The Art of Electronics 3rd Edition*

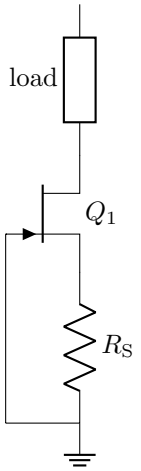
February 17, 2024

Contents

Solutions for Chapter 3

Exercise 3.1

Figure 1.1: JFET current source



From Figure 3.21 of the book, one can see that a drain current equal to 1 mA corresponds to a gate-source voltage of $-0.6\,\mathrm{V}$. Therefore:

$$\boxed{R_S = \frac{0.6\,\mathrm{V}}{1\,\mathrm{mA}} = 600\,\Omega}$$

Exercise 3.2

At $V_{GS} = V_{G0}$:

$$r_{GS} = r_{G0} = \frac{1}{2k\,(V_{G0} - V_{th})}$$

The ratio between r_{DS} and R_{G0} returns:

$$\boxed{\frac{r_{DS}}{r_{G0}} = \frac{2k\,(V_{G0} - V_{th})}{2k\,(V_{GS} - V_{th})}}$$

Exercise 3.3

Being g_m the differential conductance of the FET operated in aturation region, it can be expressed as:

$$g_\mathrm{m} = \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{GS}} = \frac{\partial}{\partial V_\mathrm{GS}} k \left(V_\mathrm{GS} - V_\mathrm{th}\right)^2 = 2k \left(V_\mathrm{GS} - V_\mathrm{th}\right)$$

Therefore:

$$\boxed{g_\mathrm{m} = \frac{1}{r_\mathrm{DS}}}$$

Exercise 3.4

(a) The voltage across the drain-gate capacitance when the JFET is switched on ($V_\mathrm{DS} = 0\,\mathrm{V}$) is equal to 50 V-10 V=40 V. Considering a maximum current across this capacitance equal to 1 mA:

$$\boxed{t_\mathrm{ON} = \frac{40\,\mathrm{V}\,200\,\mathrm{pF}}{1\,\mathrm{mA}} = 8\,\mu\mathrm{s}}$$

(b) Since the current is equal to the charge over time, we have:

$$\boxed{t_\mathrm{ON} = \frac{40\,\mathrm{nC}}{1\,\mathrm{mA}} = 40\,\mu\mathrm{s}}$$

Exercise 3.5

The 1 pF drain-source capacitance happens to be in series with the 10 kΩ load resistance. The capacitive reactance is:

$$X_\mathrm{DS} = \frac{1}{2\pi 1\,\mathrm{MHz}\,1\,\mathrm{pF}} = 160\,\mathrm{k\Omega}$$

Therefore, the feedthrough is given by:

$$\boxed{20\log_{10}\frac{10\,\mathrm{k\Omega}}{10\,\mathrm{k\Omega} + 160\,\mathrm{k\Omega}} = -25\,\mathrm{dB}}$$

Exercise 3.6

In this case, the output 10 kΩ resistance is in parallel with the 50 Ω R_ON resistance. Their equivalent resistance is about 50 Ω. Similarly to the previous exercise, the feedthorugh is given by:

$$\boxed{20\log_{10}\frac{50\,\Omega}{50\,\Omega + 160\,\mathrm{k\Omega}} = -70\,\mathrm{dB}}$$

Exercise 3.7

Figure 1.2: Zero ohm R_{ON}

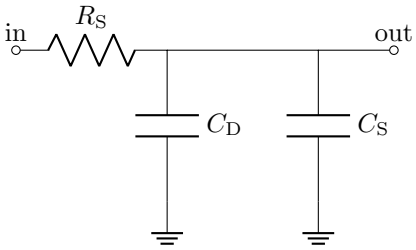
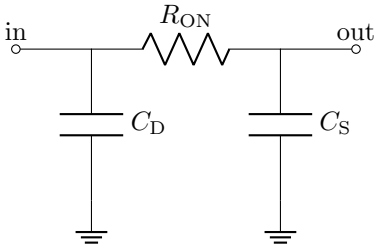


Figure 1.3: $75\,\Omega$ R_{ON}



For this exercise we assume that the load resistance of $100\,\mathrm{k}\Omega$ does not load the circuit.

(a) The circuit is that of Figure 1.2. Since $C_{\mathrm{D}} = C_{\mathrm{S}} = C_{\mathrm{T}} = 8\,\mathrm{pF}$, there is a single pole at the frequency f_{p}:

$$\boxed{f_{\mathrm{p}} = \frac{1}{4\pi R_{\mathrm{S}} C_{\mathrm{T}}} \approx 1\,\mathrm{MHz}}$$

(b) In this case the circuit is depicted in Figure 1.3. The circuit has one pole at DC and another pole at f_{p}:

$$\boxed{f_{\mathrm{p}} = \frac{1}{2\pi R_{\mathrm{ON}} C_{\mathrm{T}}} \approx 265\,\mathrm{MHz}}$$

Exercise 3.8

Figure 1.4: OFF-OFF

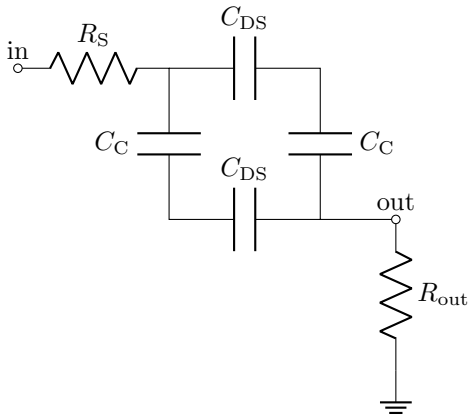


Figure 1.5: OFF-ON

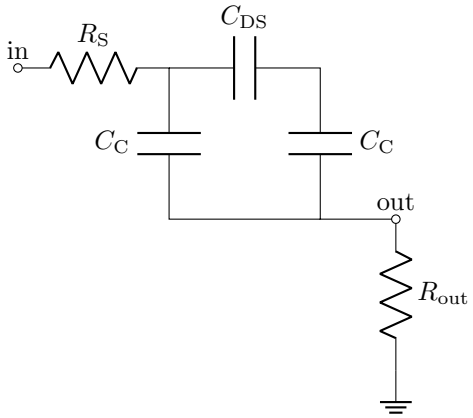


Figure 1.6: ON-OFF

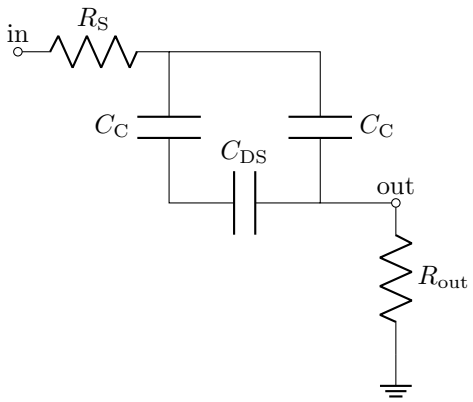
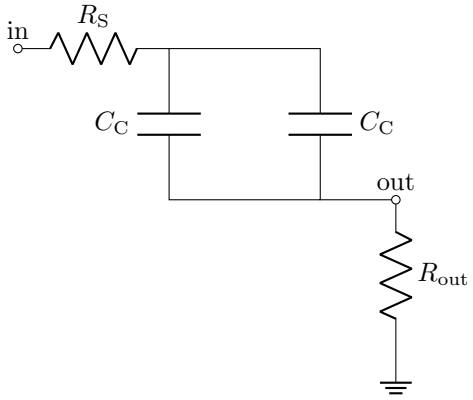


Figure 1.7: ON-ON



(a) In this case the reference circuit is depicted in Figure 1.4. The cross-coupling is given by:

$$\boxed{20\log_{10}\frac{R_{out}}{R_{out}+R_S+0.5(X_C+X_{DS})}=-10.75\,\text{dB}}$$

being $X_C=\frac{1}{2\pi f C_C}=320\,\text{k}\Omega$ and $X_{DS}=\frac{1}{2\pi f C_{DS}}=160\,\text{k}\Omega$

(b) In this case the reference circuit is depicted in Figure 1.5. The cross-coupling is given by:

$$\boxed{20\log_{10}\frac{R_{out}}{R_{out}+R_S+\frac{X_C(X_C+X_{DS})}{2X_C+X_{DS}}}=-9.6\,\text{dB}}$$

(c) In this case the reference circuit is depicted in Figure 1.6. The cross-coupling is the same as before

(d) In this case the reference circuit is depicted in Figure 1.7. The cross-coupling is given by:

$$\boxed{20\log_{10}\frac{R_{out}}{R_{out}+R_S+0.5X_C}=-8.6\,\text{dB}}$$

Exercise 3.9

(a) Considering the different combinations of resistors, the $-3\,\mathrm{dB}$ frequencies can be computed as:

$$\boxed{f_{3\mathrm{dB,n}} = \frac{n\,G_{10\mathrm{k}}}{2\pi C} \quad n = 1 \ldots 15}$$

where $C = 0.01\,\mu\mathrm{F}$ and $G_{10\mathrm{k}} = 0.1\,\mathrm{mS}$

(b) The glitch amplitude voltage can be computed as:

$$\boxed{\Delta V = \frac{20\,\mathrm{pC}}{C} = 2\,\mathrm{mV}}$$

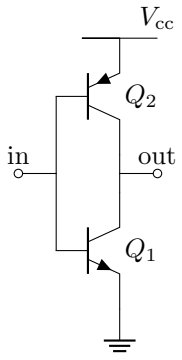
Exercise 3.10

The peak output current that the buffer has to provide can be given as the peak time derivative of the output voltage across the 10 nF capacitor multiplied by its value:

$$\boxed{I_\mathrm{p} = 10\,\mathrm{nF}\left.\frac{dV}{dt}\right|_\mathrm{p} = 10\,\mathrm{nF}\,2\pi 10\,\mathrm{kHz}\,1\,\mathrm{V} = 0.6\,\mathrm{mA}}$$

Exercise 3.11

Figure 1.8: BJT-based inverter logic circuit



The circuit of Figure 1.8 represents the complementary bjt inverter. It's easy to see that without a proper bias, if the input is grounder (low level) the V_{BE} of the pnp transistor is equal to V_{cc} which is likely to damage the transistor in a very short time

Exercise 3.12

Figure 1.9: Logic AND symbols

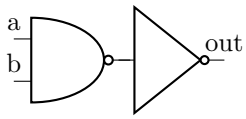
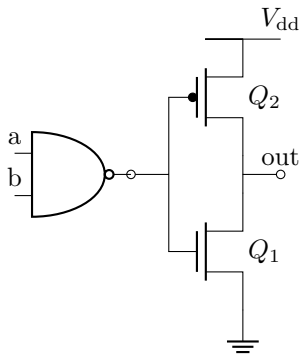


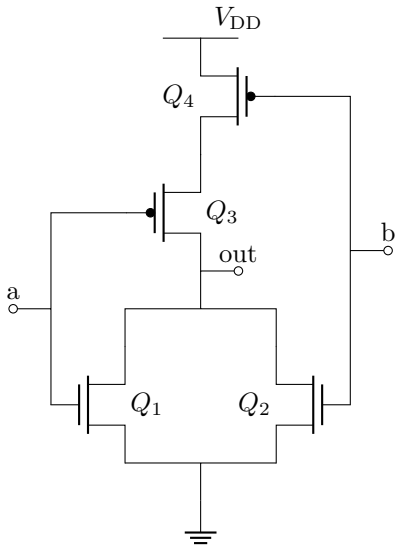
Figure 1.10: Logic AND symbol and circuit



In order to transform a NAND port into an AND port, we can use a NOT port as shown in Figures 1.9 and 1.10

Exercise 3.13

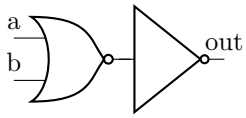
Figure 1.11: NOR circuit



The solution is presented in Figure 1.11

Exercise 3.14

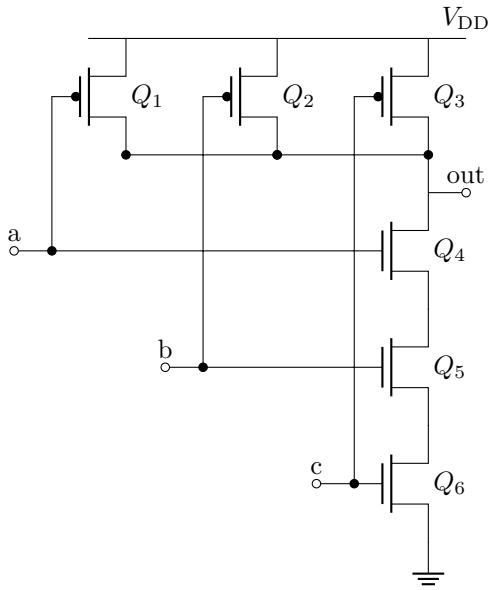
Figure 1.12: Logic OR symbols



The OR circuit can be easily obtained by cascading a NOT circuit to the NOR circuit designed in exercise 3.13.

Exercise 3.15

Figure 1.13: Three ports NAND circuit



The solution is represented in Figure 1.13. The gate comply with the following truth table

a	b	c	out
1	1	1	0
1	1	0	1
1	0	0	1
1	0	1	1
0	0	1	1
0	1	0	1
0	1	1	1
0	0	0	1

Exercise 3.16 TODO: write solution

Exercise 3.17 TODO: write solution

Exercise 3.18 TODO: write solution