LHCb Upgrade: Periphery Electronics Processing Interface for the Upstream Tracker

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On behalf of the LHCb Collaboration

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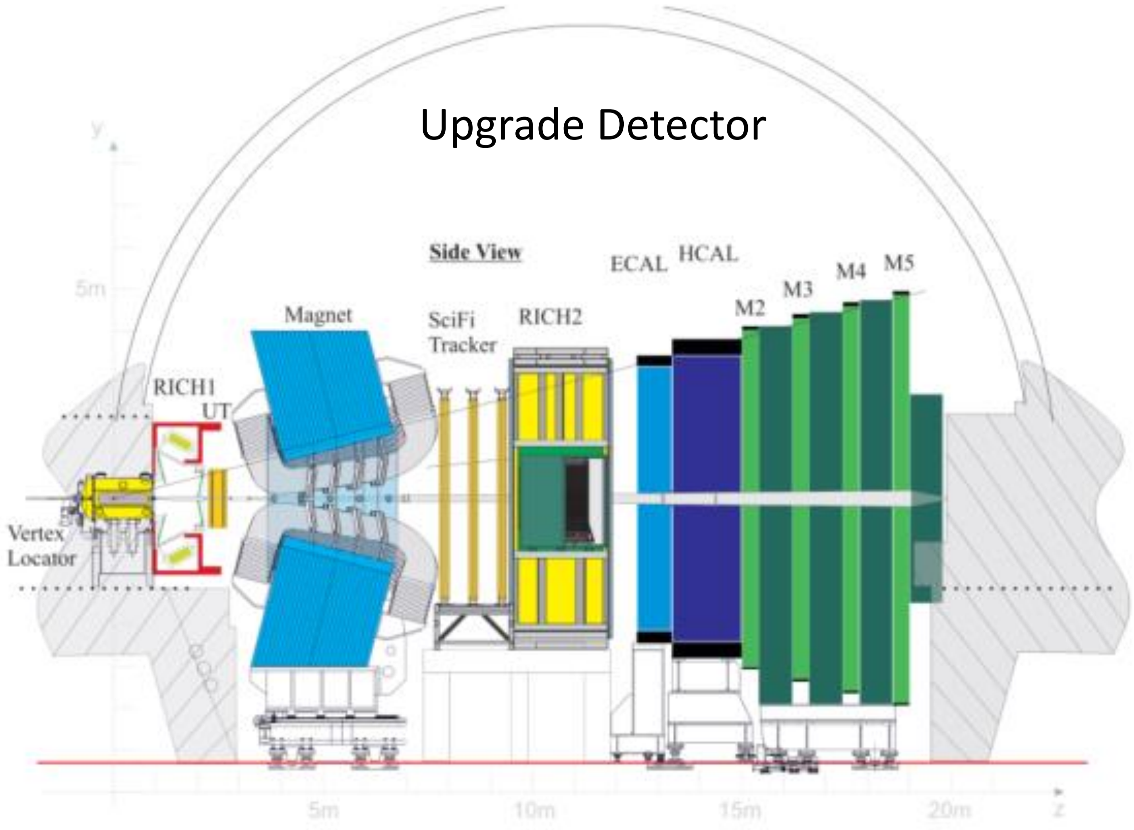
LHCb Detector Upgrade

- Flavor physics factory, with excellent vertexing and tracking
- Aim for reduced statistical uncertainties for precision measurements → more data
- LHC will increase instantaneous luminosity by factor of 5 for run 3
- Need to replace hardware/electronics to be capable of a full 40 MHz readout (for every 25 ns bunch crossing), as well as higher radiation tolerance
  - 40 MHz software trigger replaces current 1 MHz, which is limited by “level 0” hardware trigger
  - Upstream Tracker: 40 MRad for components near beam pipe, 100 kRad for electronics surrounding subdetector

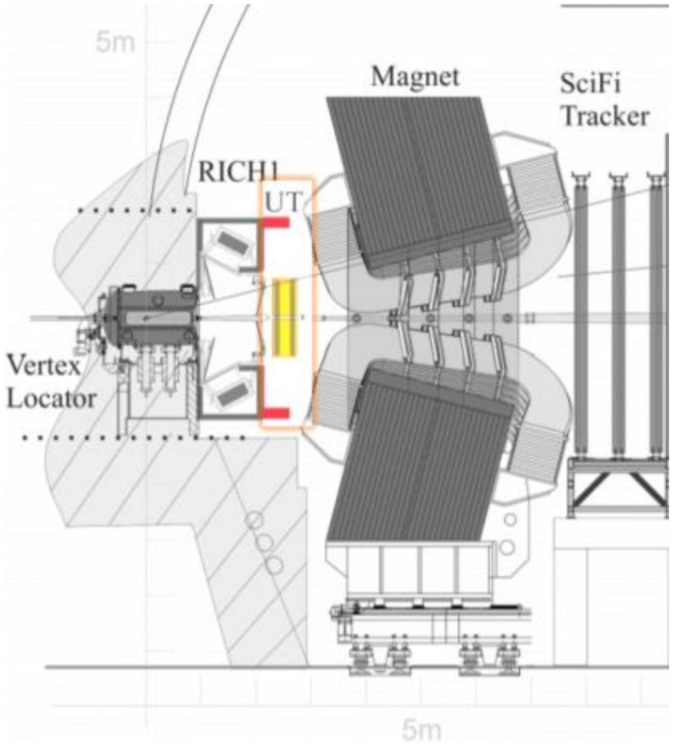


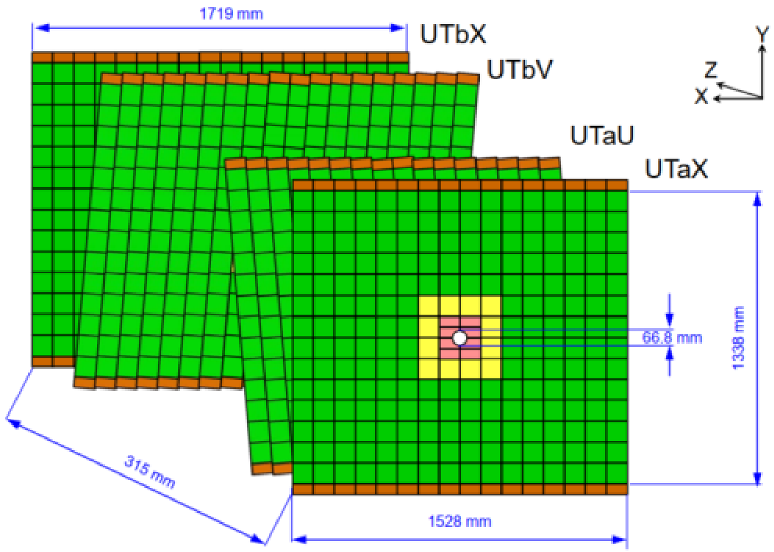
9 fb^{-1} — Upgrade I — Goal: 50 fb^{-1}

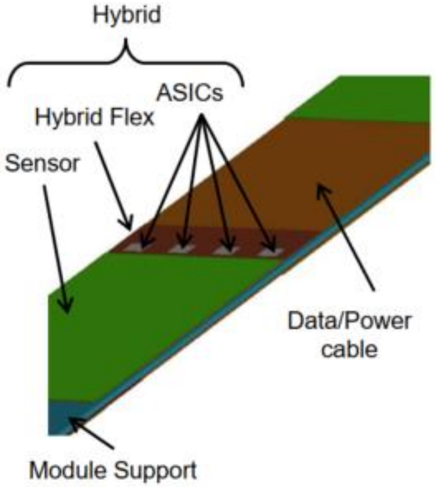
Run 1	LS1	Run 2	LS2	Run 3	LS3	Run 4
2010 2011 2012	2013 2014	2015 2016 2017 2018	2019 2020 2021	2022 2023 2024	2025 2026 2027	2028 2029 2030

Upstream Tracker (UT) Overview

- Major US contribution to LHCb hardware
- 4 planes composed of vertical staves with Si microstrip sensors and front-end (FE) electronics
  - FE Electronics- SALT (Si ASIC for LHCb Tracker) ASICs
    - 4192 of them, up to 8 per sensor, with 128 input channels and up to 5 output SLVS e-links @ 320 Mbps each
    - Digitization and zero suppression



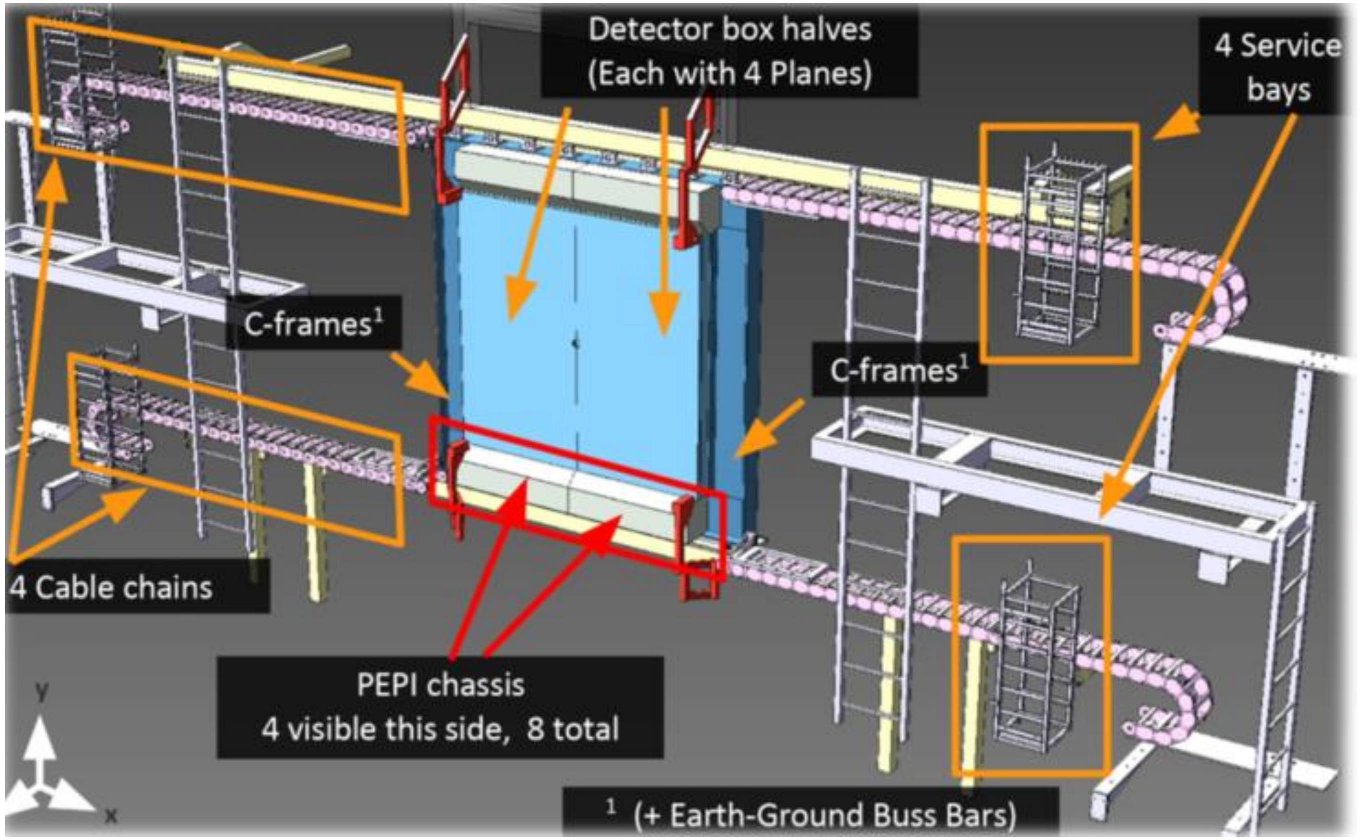




Physical Layout

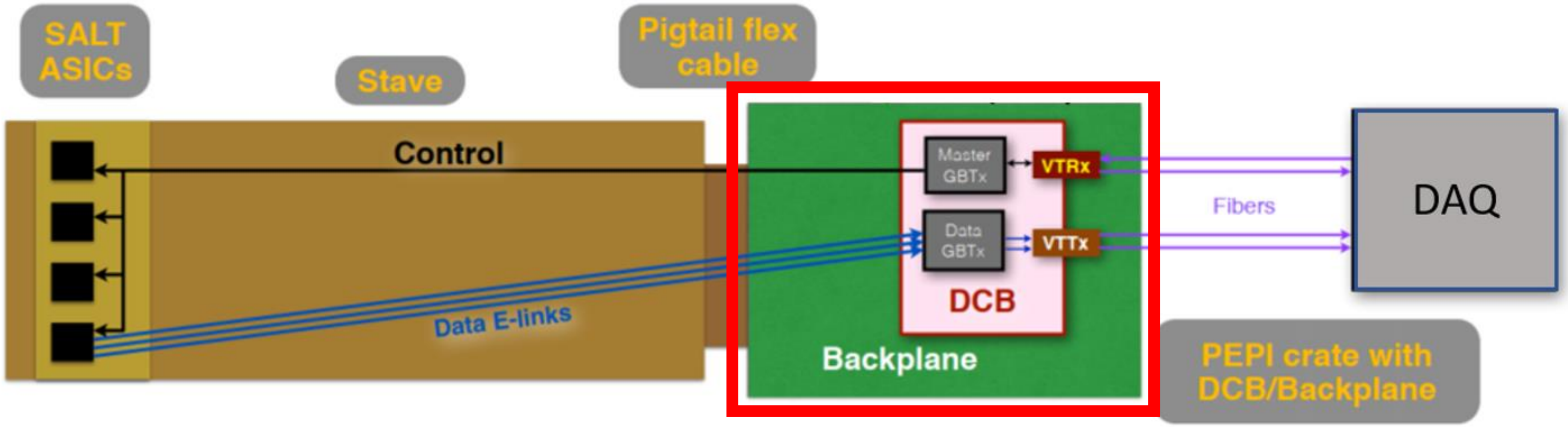
ASICs→hybrid flex→‘pigtail’ flex cables→backplanes (BP)→data control boards (DCBs)→DAQ

- BPs and DCBs inside periphery electronics processing interface (PEPI)
- 8 PEPI boxes- each with 3 BP and up to 12 DCBs per BP
- Service Bay Crates contain low voltage regulators (LVR) for powering PEPI and hybrids, while remotely sensing voltages



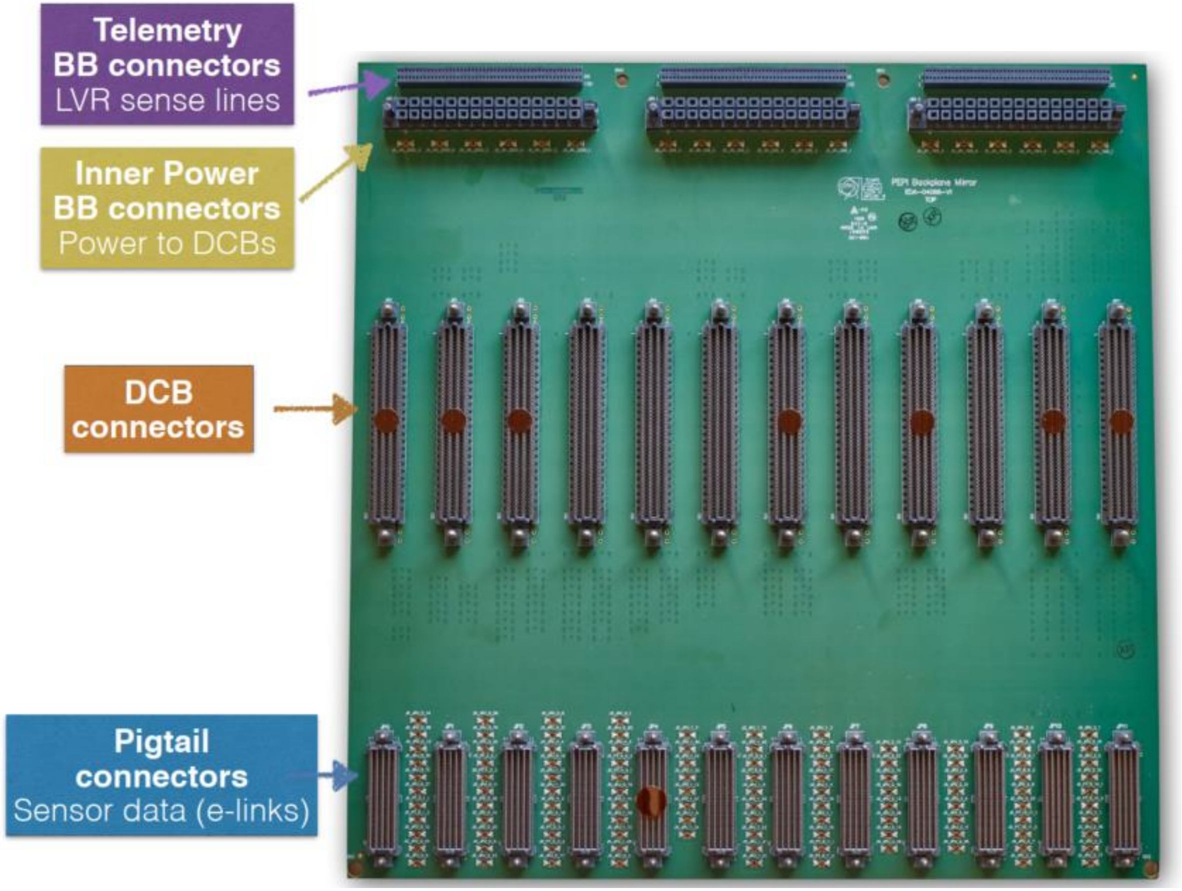
PEPI Functionality

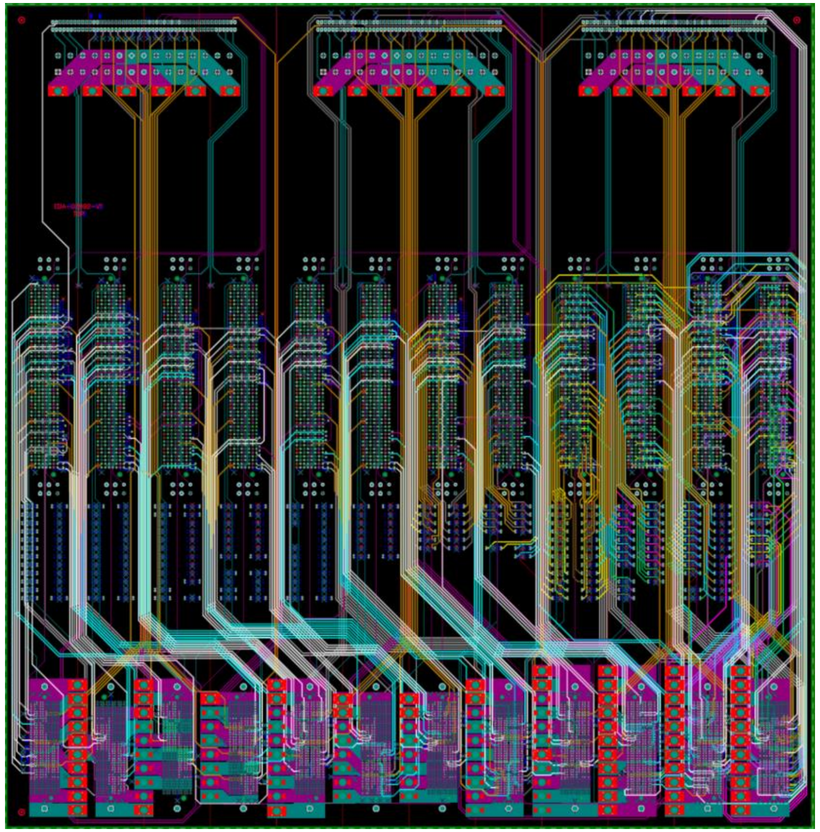
- Backplanes route data and control signals to and from DCBs
- DCBs have data input in digital form and optically relay it to LHCb DAQ
  - 6 Data GBTx chips per DCB, each with data from multiple FE ASICs, that serialize sensor data, then send it out at 4.8 Gbps
  - 248 DCBs x 6 GBTx/DCB x 4.8 Gbps/GBTx = 7.1 Tbps throughput
- DCBs also perform various other roles via single master GBTx chip: communication between DAQ and other components
  - Monitoring and slow control
    - Monitoring electronics temperatures
    - Configuring FE ASICs
  - Timing and fast control
    - Communicate clock to FE ASICs
    - FE resets
    - Bunch crossing vetos



Backplanes

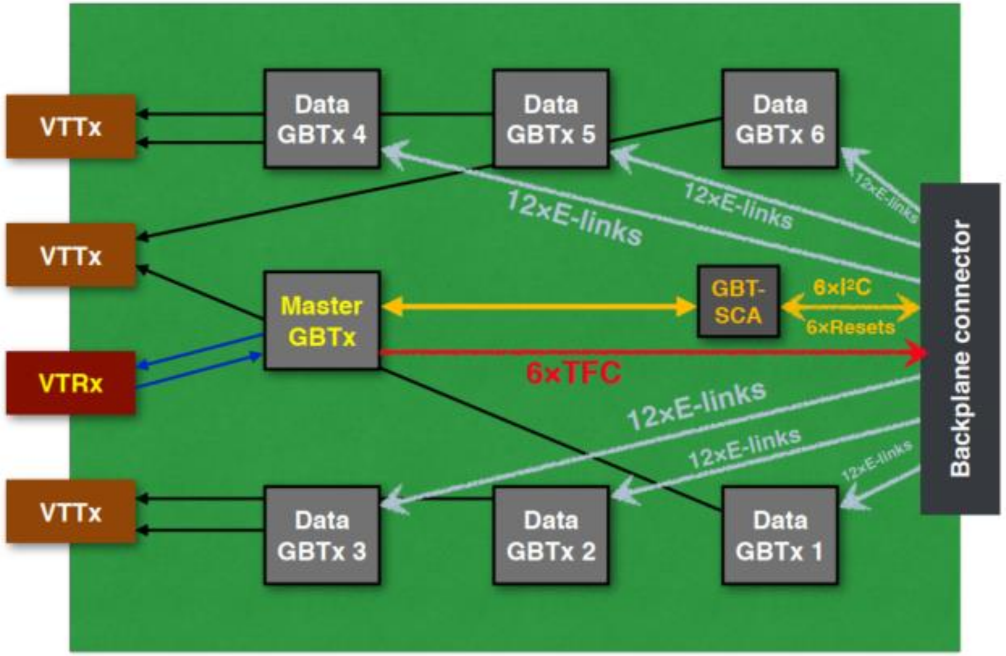
- Due to space constraints, backplane is ultra-dense, with 28 layers -- at the limit of manufacturability





DCBs

- GBTx: high speed serializer/deserializer
  - Total speed 5.1 Gbps
  - 6 data GBTx and 1 master GBTx
- VTTx/VTRx: optical transmitter/transceiver modules
  - Also operate at 5.1 Gbps
- GBT-SCA: experiment slow control/monitoring
- These components all rad-hard and designed by CERN

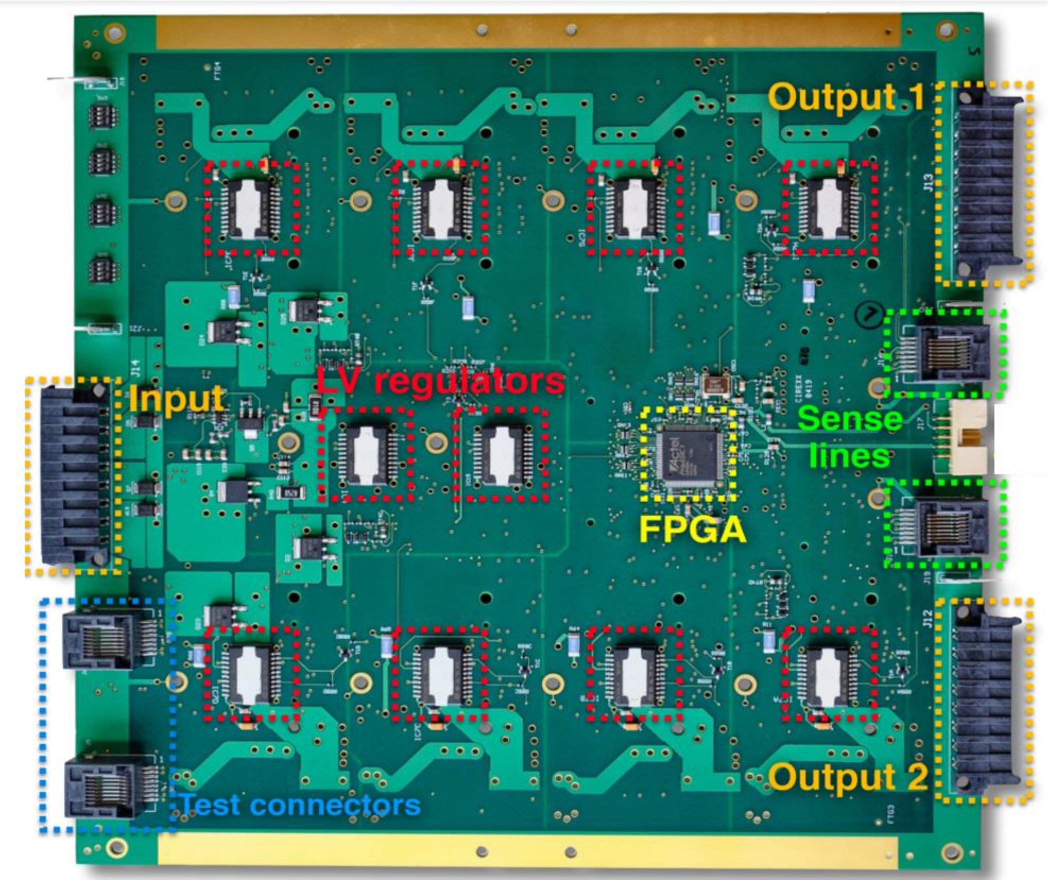


- Critical to achieve high fidelity data transmission
  - Verified up to 10^{15} bits with pseudo-random bit sequence

Eye diagram measurement on the DCB with 4.8 Gbps input to the VTTx

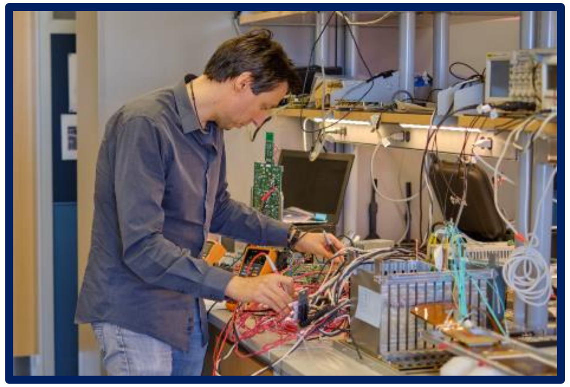
LVRs

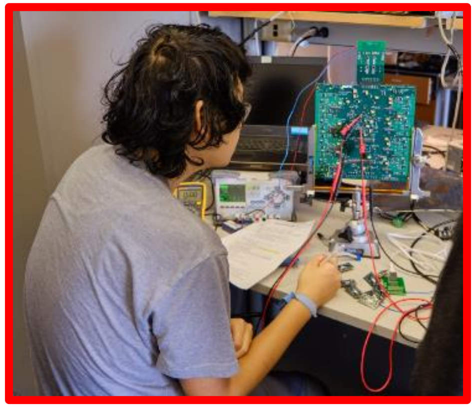
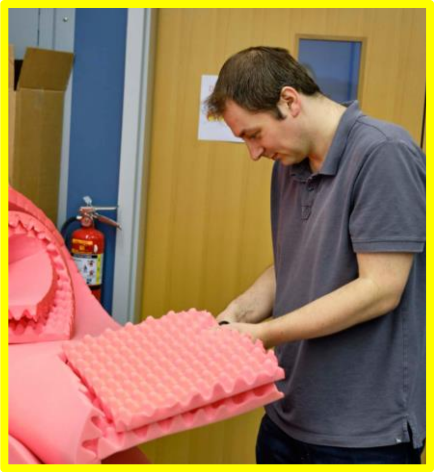
- LVRs provide LV power to PEPI and staves, with sense lines to ensure precise (better than 5%) remote voltage regulation
  - LV regulator part number LHC4913PDU, rad-hard and designed by CERN
  - Sense lines accommodate fully differential remote sensing, beyond the functionality granted via LV regulator chips



Project Status

- All boards for detector QA'd and burned in at UMD, undergoing testing at CERN now
  - 248 DCBs, 268 LVRs, 24 backplanes for full detector
- Next goal will be commissioning- plan to begin taking data next February

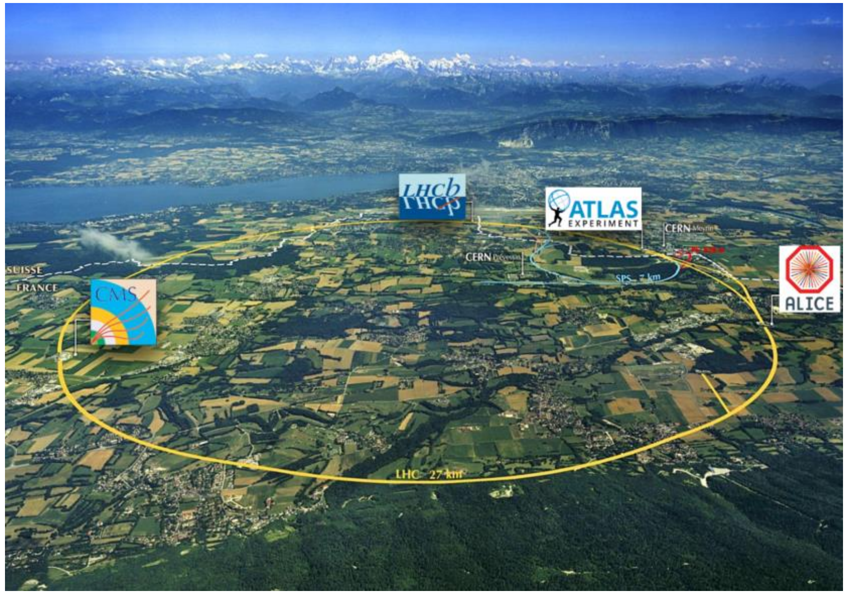

Summary

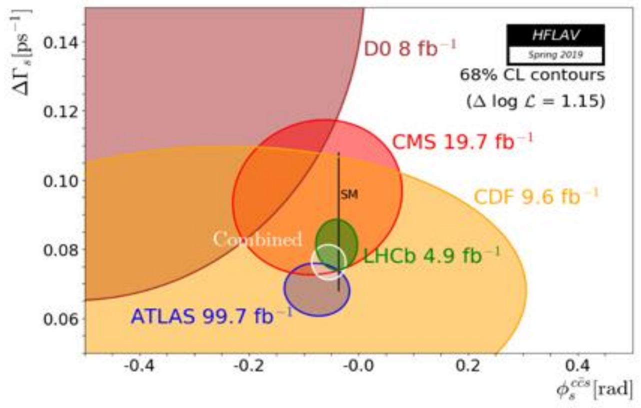
- LHCb detector upgrading to a 40 MHz trigger, with corresponding hardware upgrades, in run 3, resulting in 5 fb^{-1} of data to be taken per year
- UT is critical for tracking and will be an important part of the upgrade
- PEPI electronics serialize and optically transmit sensor data and relay control signals, LVRs provide LV power and remote sensing for PEPI and staves: boards for full detector are now at CERN being QA’d

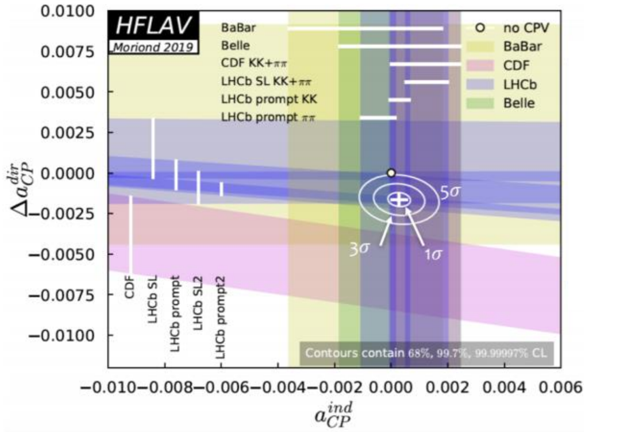
Backup Slides

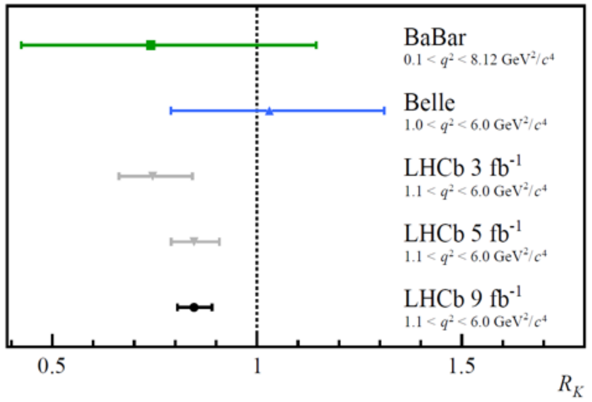
LHCb Physics Motivation

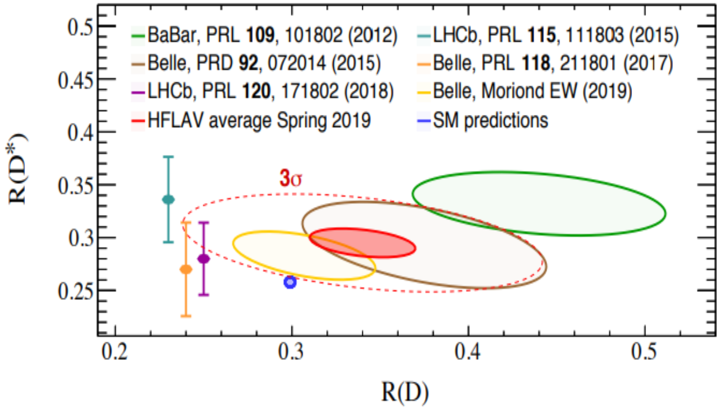
- Flavor physics: focus on *b*,*c* quark rich data
- Physics objectives, searches for new physics
  - CP violation measurements
  - Lepton flavor universality violations
  - Hadron discovery/spectroscopy
  - Evidence for exotic particles





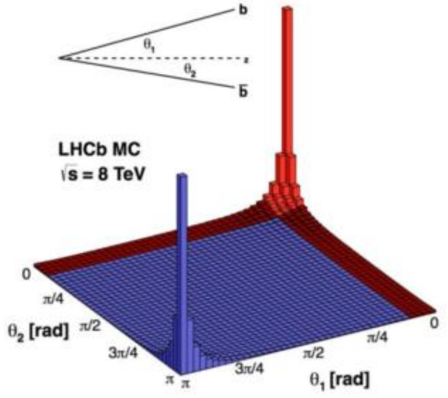


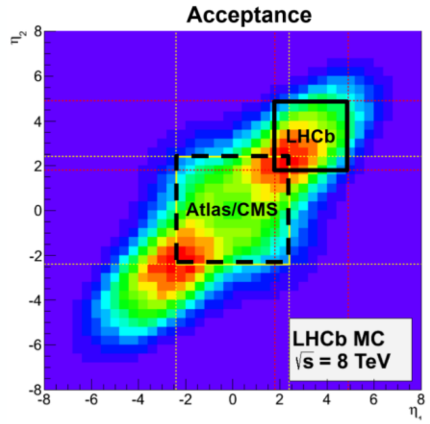




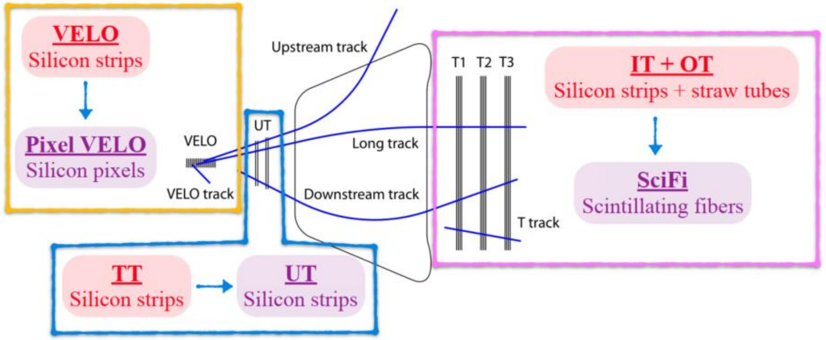
LHCb Detector Overview

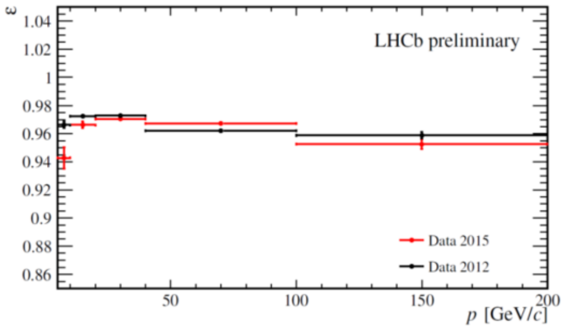
- Flavor physics factory: beauty, charm particles produced primarily in highly-boosted CM frame, hence LHCb single-arm forward detector
  - 25% of $b\bar{b}$ production within ~4% solid angle $(2 < \eta < 5)$
- Excellent vertexing and tracking are cornerstones of many LHCb precision measurements
  - 96% reconstruction efficiency for long tracks (runs 1,2)



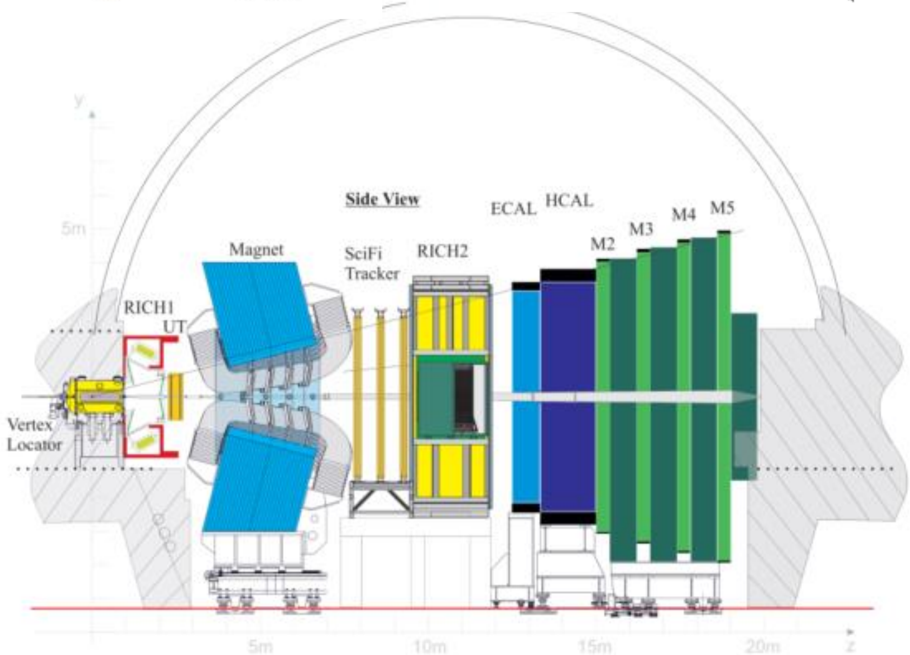


Runs 1,2,3 tracking system



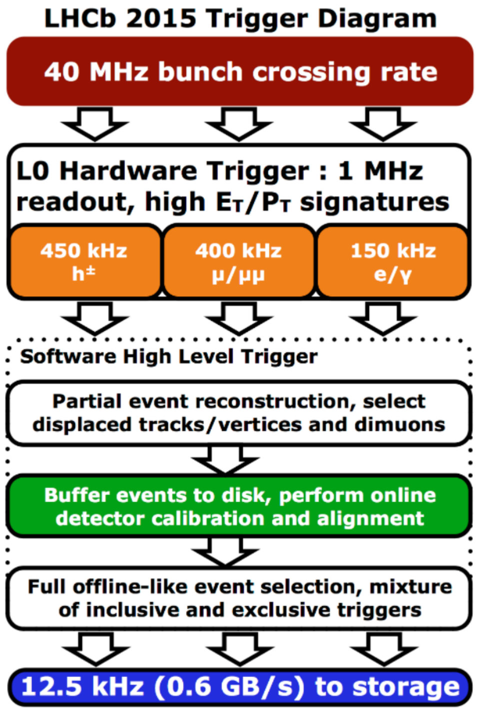


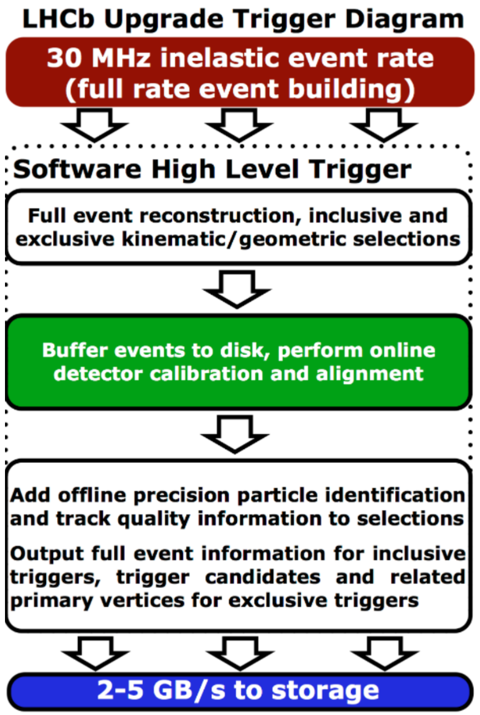
Track reco efficiency for long tracks in 2012, 2015

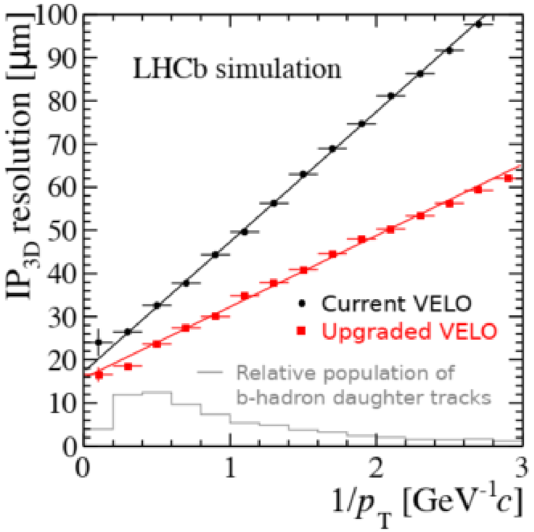


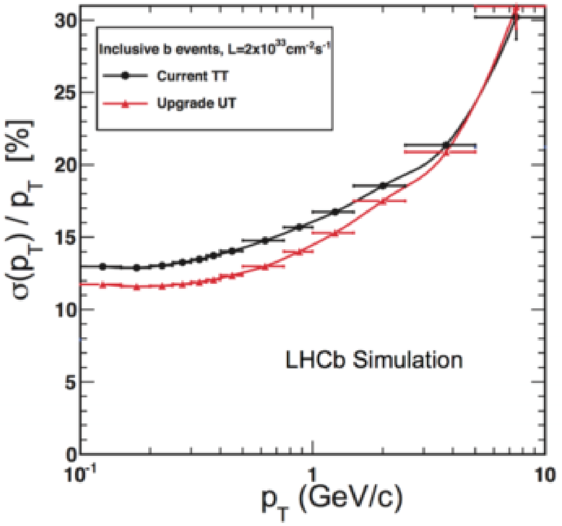
Trigger and Performance Upgrade

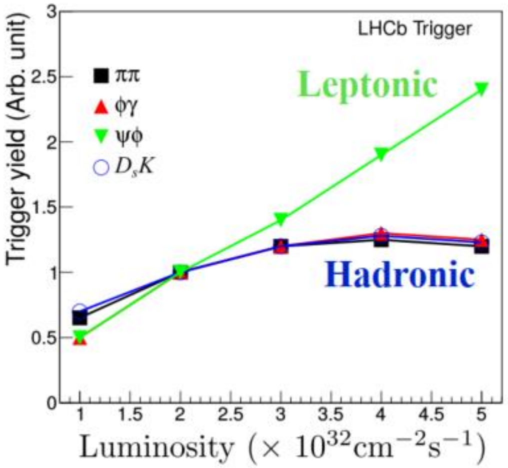
- Updated fully software trigger for full 40 MHz readout removes “level 0” hardware trigger limitation
- Improve tracking to speed up reconstruction time
  - Better impact parameter resolution, p_T resolution, reduction in ghost rate

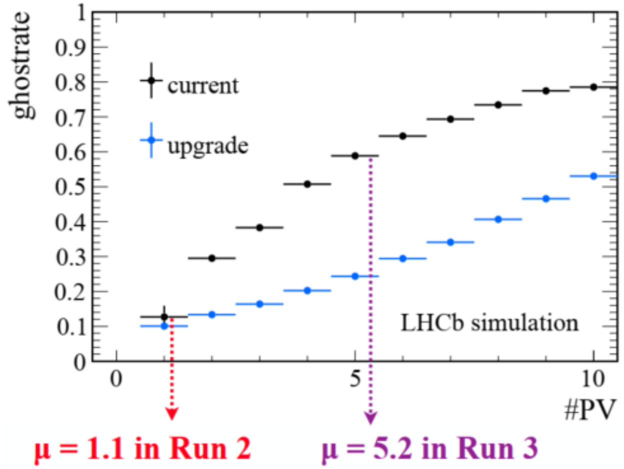












Upstream Tracker (UT) Overview [More Detail]

- First major US contribution to LHCb hardware
  - Replaces Tracker Turicensis from runs 1,2 detector
    - Finer granularity, closer to the beam, reduced material budget, 40 MHz readout
- Placed between VELO and dipole magnet
  - Crucial for (fast) triggering, long-lived (outside VELO) charged particle reconstruction, reducing ghost tracks
- 4 planes composed of vertical staves with Si microstrip sensors and front-end (FE) electronics
  - Rotated U,V planes provide stereo information
  - FE Electronics- SALT (Si ASIC for LHCb Tracker) ASICs
    - 4192 of them, up to 8 per sensor, with 128 input channels and up to 5 output SLVS e-links @ 320 Mbps each
    - Analog shaping, digitization, pedestal subtraction, mean common mode subtraction, zero suppression, serialization