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LVR user's manual

Low Voltage Regulator board for the Upstream Tracker (UT) of the LHCb detector

Firmware tag: 2.03

LVR switches and SPI interface

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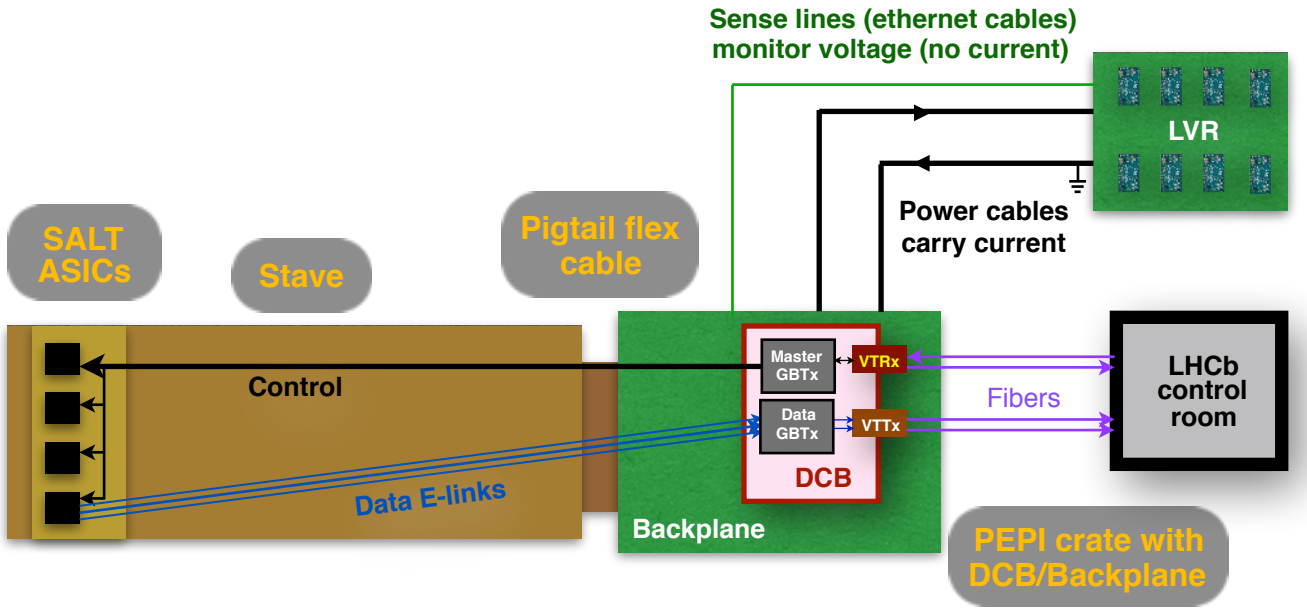
Overview and documentation

The **Low Voltage Regulator boards (LVRs)** provide precisely regulated DC voltages and stable currents. These boards are located about 10 meter away from the Upstream Tracker in the service bay areas where the radiation levels are about 20 krad of TID for ten years. These boards are based on the radiation-hard ST Microelectronics LHC4913PDU chips. Remote sense circuits that accommodate both common and difference mode voltage shifts across the load cables provide precision remote sense capability that keeps the voltage levels at their set values to within better than 5%.

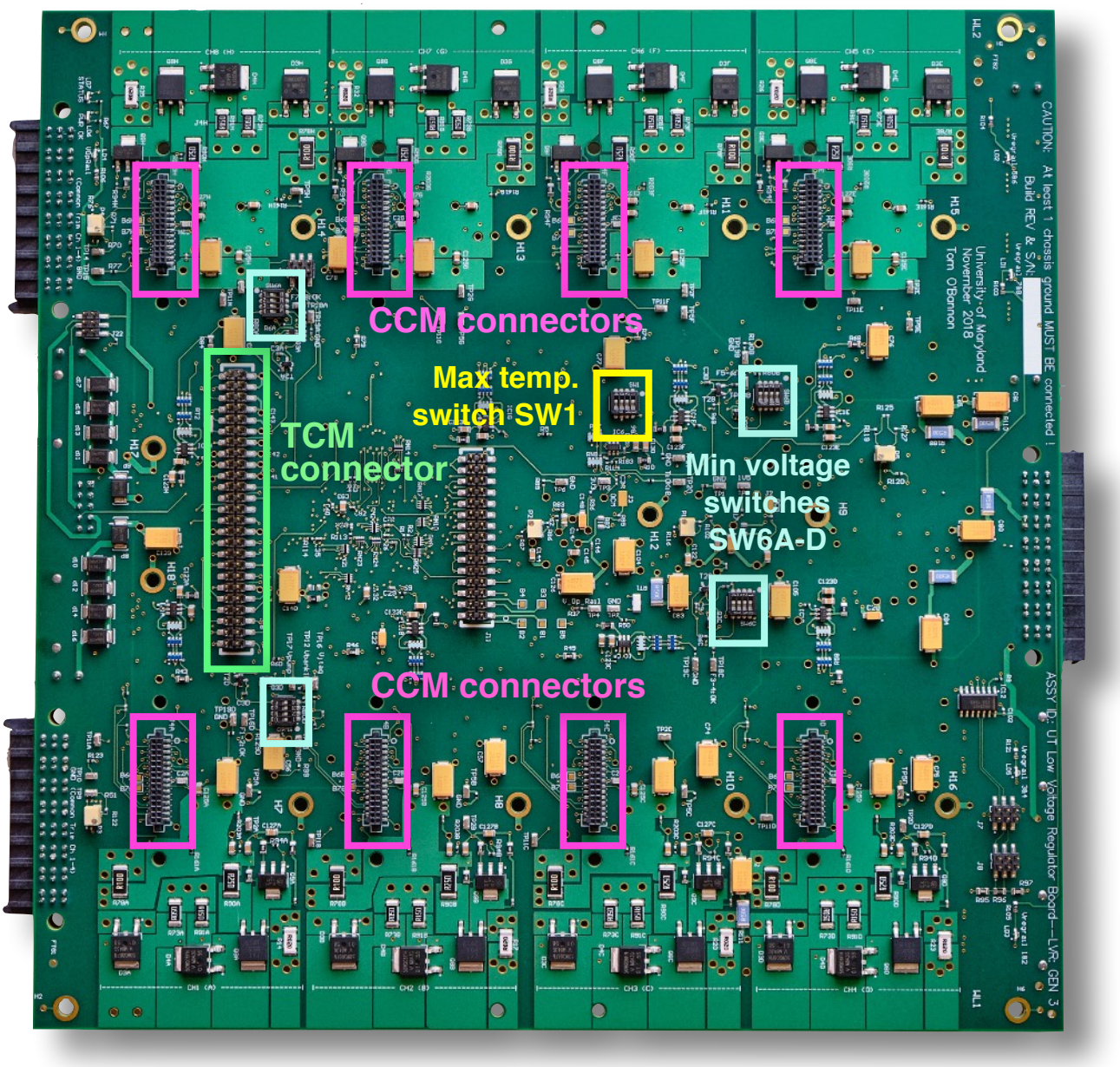
Key documentation can be found at

- Latest version of this manual: http://flavor.physics.umd.edu/research/ut/lvr_manual.pdf
- Firmware project and .stp files: https://github.com/umd-lhcb/lvr_fw
- Schematics: https://github.com/umd-lhcb/electronic-projects/raw/master/lvr/schematic_lvr.pdf
- Altium project: https://github.com/umd-lhcb/electronic-projects/raw/master/lvr/2019-09-05_lvr_project.zip
- Bill of materials (BOM): https://github.com/umd-lhcb/electronic-projects/raw/master/lvr/2019-09-05_lvr_bom.xlsx
- Gerber (manufacturing) files): https://github.com/umd-lhcb/electronic-projects/raw/master/lvr/2019-09-05_lvr_gerber.zip
- High resolution photos: https://umd.box.com/s/haufw3fllsfhzq0ndg74z22ls4mxqwnt



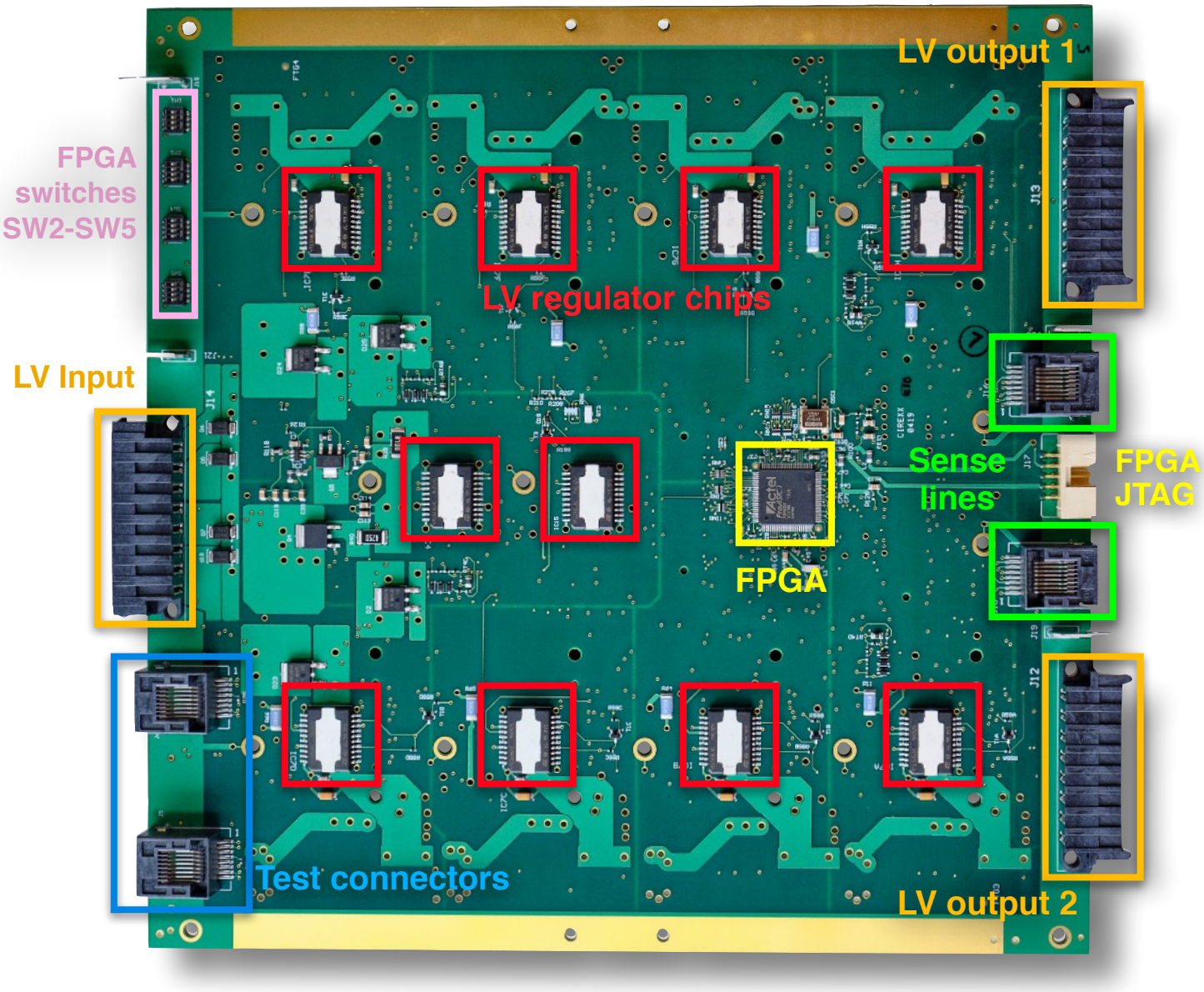
LVR top view (CCM/TCM side)

The CCMs and TCM are connected on this side.



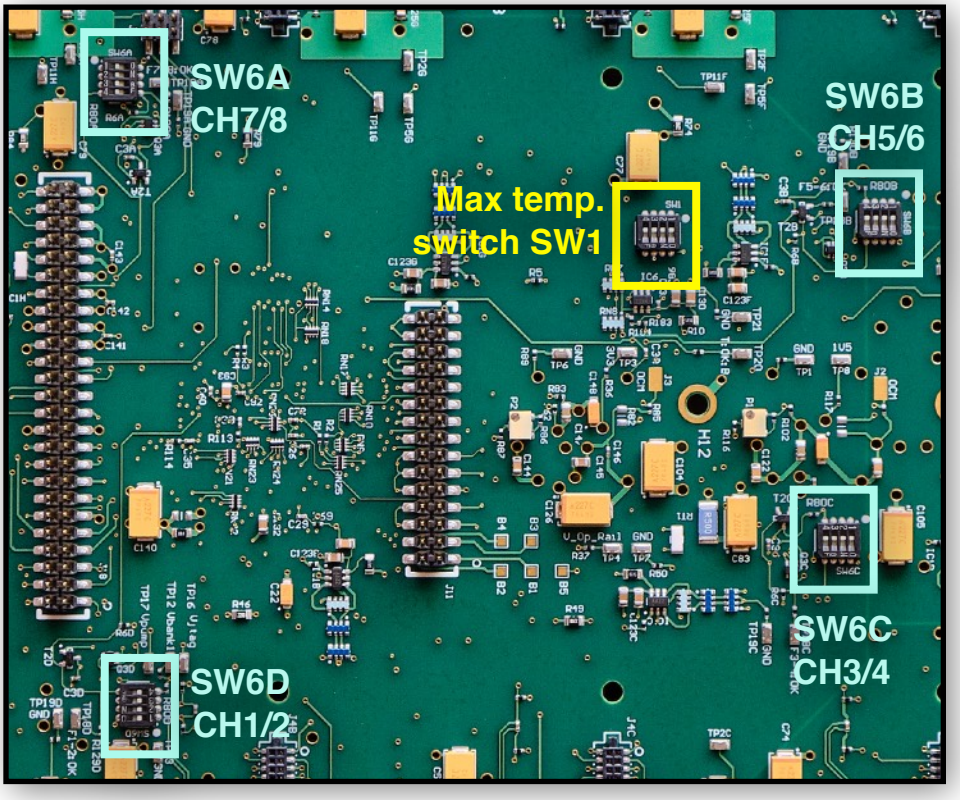
LVR bottom view (FPGA side)

This side is pressed against the LVR heat spreader.



Functionality of switches

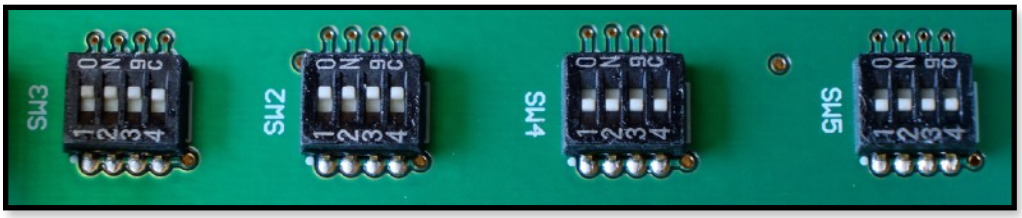
Top (CCM/TCM side) switches



SW1 controls **max temperature** (toggles 1-4)
30°C: **1101**
55°C: **1001**
70°C: **0001**

SW6A-D control the **undervoltage lockout**.
Toggles 1-3 set min voltage needed:
3.9V: **111**
4.6V: **101, 001**
5.1V: **110, 010**
5.4V: **100**
5.9V: **000**
Toggle 4 is a lockout override

Bottom (FPGA side) switches



Toggles are ON away from the edge of the board (up in the picture), as labeled on the switch

SW3	SW2	SW4	SW5
1 CH1 enabled	**1** CH5 enabled	**1** CH2 slave	**1** Channels ON at turn-on
2 CH2 enabled	**2** CH6 enabled	**2** CH4 slave	**2** Duty cycle mode
3 CH3 enabled	**3** CH7 enabled	**3** CH6 slave	**3** No CRC checking
4 CH4 enabled	**4** CH8 enabled	**4** CH8 slave	**4** *Unused*

SPI interface

The table below defines the 32-bit input commands (**STD**), and the three possible responses (**STD**, **WORD2**, **WORD3**). Color code is **Control - Monitoring - Configuration**

Bits	31-28	27-24	23-20	19-16	15-12	11-8	7-4	3-0
STD	COMMAND & CRC	CRC	STATUS	UVL	READY8-5	READY4-1	ON8-5	ON4-1
WORD2	"00" & CRC	CRC	EN8-5	EN4-1	SLAVE	FW2	FW1	FW0
WORD3	"00" & CRC	CRC	0	0	0	0	0	SW5

The definition of the components in the **STD** structure are

STD word	Bit	W/R	Description
COMMAND	31 30	W/R	"00" → Read **STD** word (this table except the first two bits) "01" → Read **WORD2** in following SPI command "10" → Read **WORD3** in following SPI command "11" → Write
CRC	29	R	6-bit CRC with $x^6 + x^5 + x^2 + x + 1$ polynomial applied on the other 26 bits of **STD**, ie, `CRC[STD(31-30) & STD(23-0)]` SPI reads return `CRC["00" & STD(23-0)]` in this field
	28	R	
	27	R	
	26	R	
	25	R	
	24	R	
STATUS	23	R	Previous command timed out (3.22 ms after first edge)
	22	R	Previous command had bad parity bit
	21	R	Over-temperature state
	20	W/R	Low duty cycle (pulse mode)
UVL	19	R	Input voltage below threshold for channels 7/8
	18	R	Input voltage below threshold for channels 5/6
	17	R	Input voltage below threshold for channels 3/4
	16	R	Input voltage below threshold for channels 1/2
READY8-5	15-12	W/R	Channels 8-5 READY
READY4-1	11-8	W/R	Channels 4-1 READY
ON8-5	7-4	W/R	Channels 8-5 ON
ON4-1	3-0	W/R	Channels 4-1 ON

WORD2 is a 32-bit word sent after **COMMAND** = **01**. The definition of its components is

- **SLAVE**: Whether channels 2, 4, 6, or 8 are set to slave by SW4.
- **EN8-1**: Whether channels 8 down to 1 are enabled by switches SW2 and SW3.
- **FW2/1/0**: The firmware version. For instance, **FW2** = 2, **FW1** = 0, and **FW0** = 3 would mean version 2.03.

WORD3 is a 32-bit word sent after **COMMAND** = **10**. The definition of its components is

- **SW5**: Values of SW5 switch configuring channel startup, duty cycle, and CRC checking.

Technical details of SPI protocol

Data is sampled on the rising edges of the SPI clock, and shifted on the falling edges.

The nominal frequency for the SPI protocol is 312.5 kHz, but frequencies between 10 kHz and 1 MHz should work. There is a timeout after 3.22 ms of receiving the first edge of the SPI command, corresponding to the slowest frequency of about 10 kHz. If a timeout occurs, the SPI state machine goes back to waiting for a command and reports the timeout in the next SPI communication.

If the CRC is invalid for the word, "write" commands are ignored and the bad CRC is reported in the next SPI communication. CRC is not checked for "read" commands. The attribute SYN_RADHARDLEVEL is set to "TMR".

LVR behavior

The LVR channels can be in one of three states: **OFF**, **STANDBY**, or **ON**.

- Going from **OFF** to **ON** requires a turn-on sequence that takes about 20 ms to complete.
  - ➡ To set a channel to **ON** you need to set both the **READY** and **ON** bits to 1. A channel cannot be **ON** without being **READY**.
- The **STANDBY** state outputs ~130 mV, so basically no power, and allows us to go to **ON** immediately.
  - ➡ To set a channel to **STANDBY** you set the **READY** bit to 1 and the **ON** bit to 0.

The status of the 8 channels can be controlled by the SPI interface, but several constraints override the SPI commands:

- Channels not enabled by switches SW2 and SW3 cannot become **READY**.
- If the LVR is over the maximum temperature set by SW1, or the input voltage is under the minimum voltage set by SW6A-D, the associated channels cannot become **READY**.
- If a channel is set to slave by SW4, its **READY** and **ON** states are controlled by its master. The master channel number is the slave's minus one, eg, if channel 4 is a slave, its states are controlled by channel 3.

Examples of SPI commands

The following would the responses by an LVR with the following characteristics:

➡ It has firmware 2.03 and was just turned-on

➡ It has all toggles in SW5 set to 0 (by default channels start **OFF**, no duty cycle, CRC is checked)

➡ All channels in SW2 and SW3 are enabled (all toggles set to ON)

➡ Channel 4 is set to slave in SW4 (toggle 2 set to ON, rest to OFF)

➡ The temperature is ok, but the input voltage is insufficient for channels 1/2

#	Input to LVR from SOL40	Output from LVR	Comments
1	00 00 00 00	3F 01 00 00	**READ**: all channels start **OFF**. The 1 indicates and CH1/2 have insufficient input voltage. 3F is the CRC
2	CC 00 FF F7	3F 01 00 00	**WRITE**: turn all channels but CH4 **ON** and set CH4 to **STANDBY**. We read the status of the channels before turning them **ON**
3	00 00 00 00	1A 01 FC FC	**READ**: CH1/2 cannot turn **ON** because insufficient input voltage. CH4 turned on because if follows its master CH3
4	40 00 00 00	1A 01 FC FC	**REQUEST WORD2**
5	80 00 00 00	2F FF 22 03	**REQUEST WORD3/READ WORD2**: FF indicates all channels are enabled, the first 2 that CH4 is a slave, and 203 that the firmware version is 2.03
6	00 00 00 00	00 00 00 00	**READ WORD3**: The last 0 indicates all toggles in SW5 are set to OFF (default turn on OFF, no duty cycle, CRC is checked)
7	00 00 00 00	1A 01 FC FC	**READ**
8	00 00 00 00	33 21 00 00	**READ**: all channels are now **OFF** due to **over-temperature** as Indicated by bit 21 (the 2 in 21)
9	00 00 00 00	1A 01 FC FC	**READ**: over-temperature no more, so channels turned back **ON**
10	C0 00 00 00	1A 01 FC FC	**WRITE**: turn all channels **OFF**. Note the **bad CRC**
11	00 00 00 00	02 41 FC FC	**READ**: channels were not turned **OFF** because of the bad parity bit in previous command, indicated by the 4 in 41