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LVR user's manual

Low Voltage Regulator board for the Upstream Tracker (UT) of the LHCb detector

Firmware tag: 2.02

LVR switches and SPI interface

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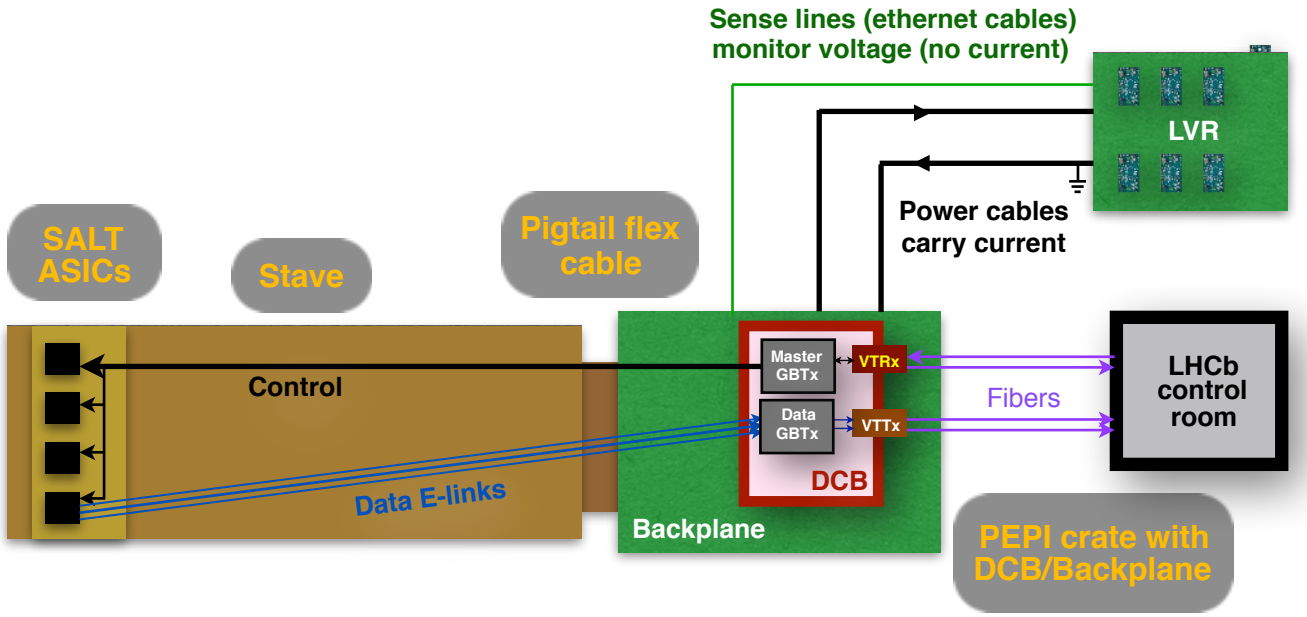
Overview and documentation

The **Low Voltage Regulator boards (LVRs)** provide precisely regulated DC voltages and stable currents. These boards are located about 10 meter away from the Upstream Tracker in the service bay areas where the radiation levels are about 20 krad of TID for ten years. These boards are based on the radiation-hard ST Microelectronics LHC4913PDU chips. Remote sense circuits that accommodate both common and difference mode voltage shifts across the load cables provide precision remote sense capability that keeps the voltage levels at their set values to within better than 5%.

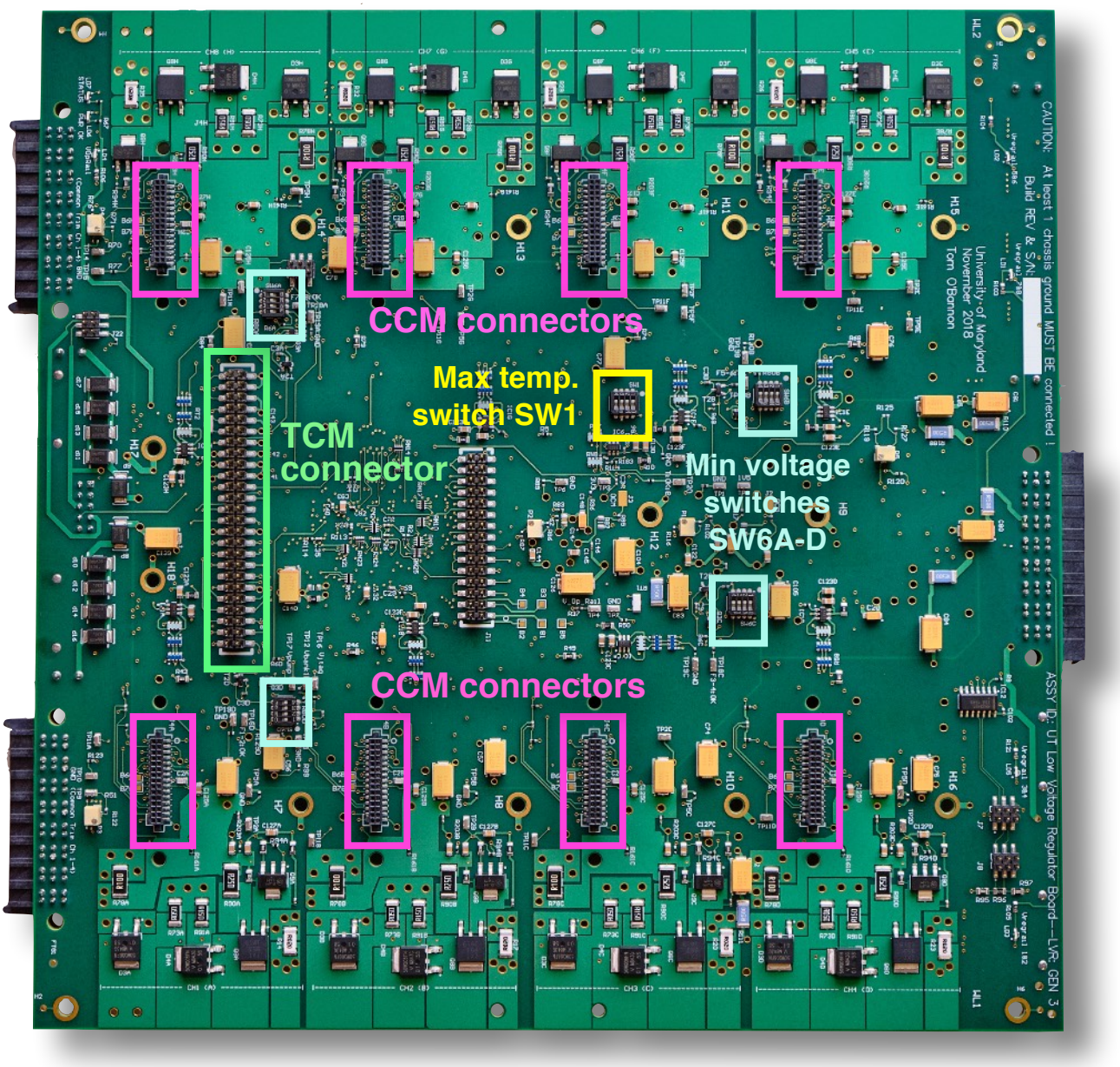
Key documentation can be fount at

- Latest version of this manual: http://flavor.physics.umd.edu/research/ut/lvr_manual.pdf
- Firmware project and .stp files: https://github.com/umd-lhcb/lvr_fw
- Schematics: https://github.com/umd-lhcb/electronic-projects/raw/master/lvr/schematic_lvr.pdf
- Altium project: https://github.com/umd-lhcb/electronic-projects/raw/master/lvr/2019-09-05_lvr_project.zip
- Bill of materials (BOM): https://github.com/umd-lhcb/electronic-projects/raw/master/lvr/2019-09-05_lvr_bom.xlsx
- Gerber (manufacturing) files): https://github.com/umd-lhcb/electronic-projects/raw/master/lvr/2019-09-05_lvr_gerber.zip
- High resolution photos: https://umd.box.com/s/haufw3fllsfhzq0ndg74z22ls4mxqwnt



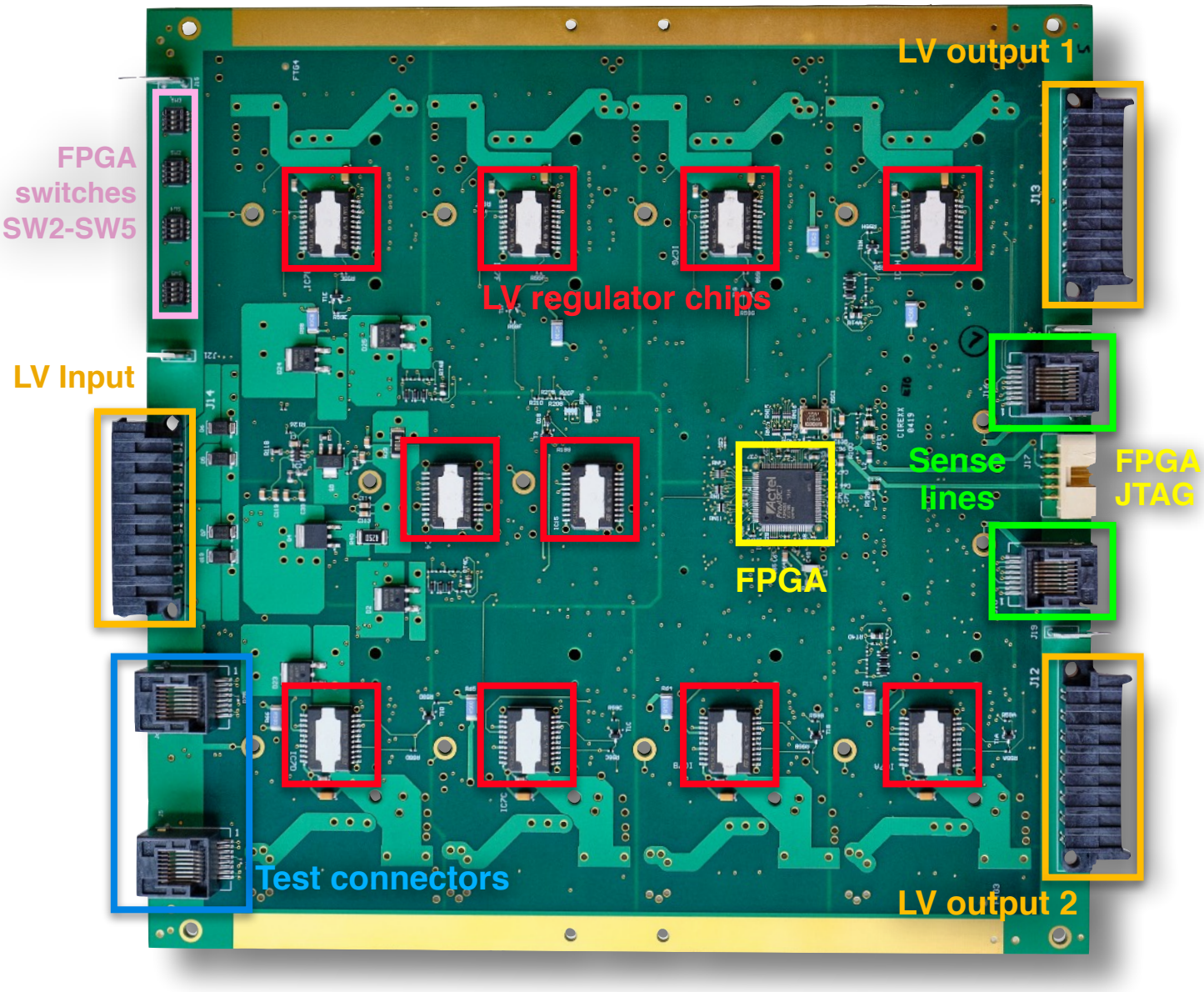
LVR top view (CCM/TCM side)

The CCMs and TCM are connected on this side.



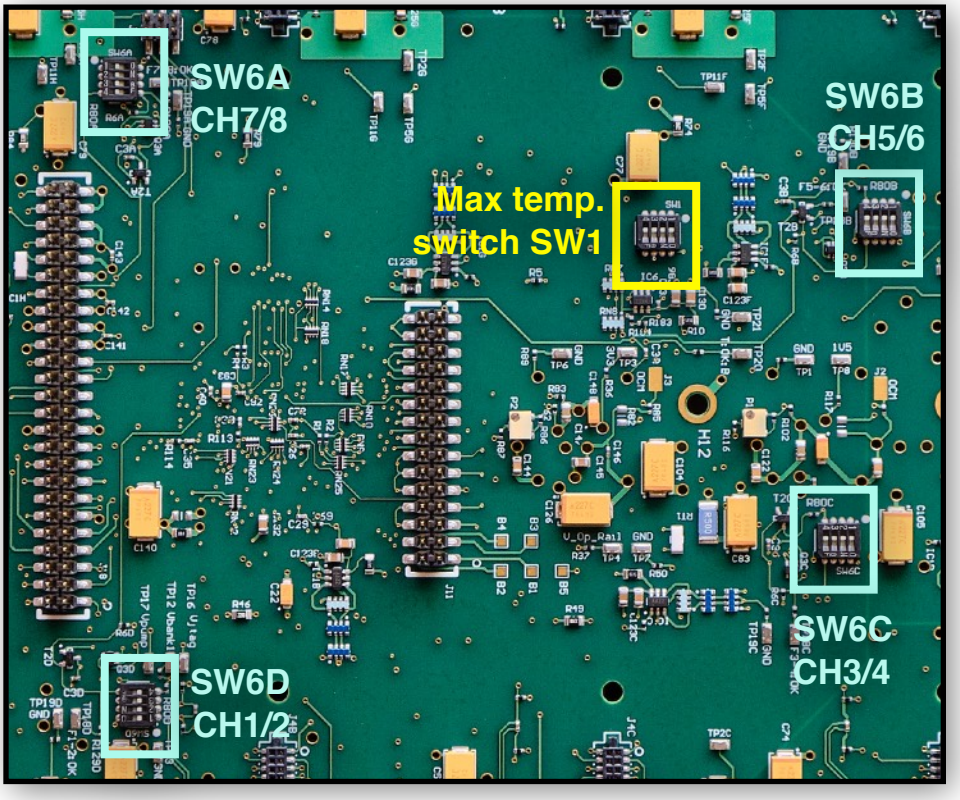
LVR bottom view (FPGA side)

This side is pressed against the LVR heat spreader.



Functionality of switches

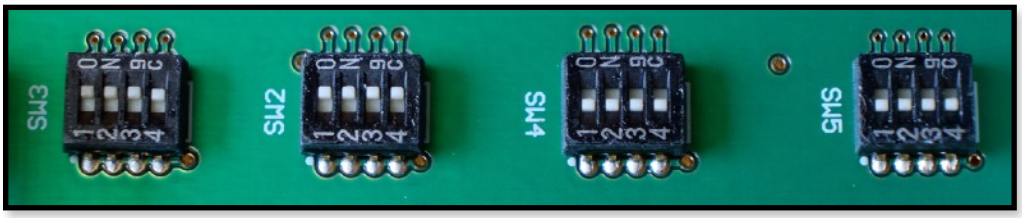
Top (CCM/TCM side) switches



SW1 controls **max temperature** (toggles 1-4)
30°C: **1101**
55°C: **1001**
70°C: **0001**

SW6A-D control the **undervoltage lockout**.
Toggles 1-3 set min voltage needed:
3.9V: **111**
4.6V: **101, 001**
5.1V: **110, 010**
5.4V: **100**
5.9V: **000**
Toggle 4 is a lockout override

Bottom (FPGA side) switches



Toggles are ON away from the edge of the board (up in the picture), as labeled on the switch

SW3	SW2	SW4	SW5
1 CH1 enabled	**1** CH5 enabled	**1** CH2 slave	**1** Duty cycle mode
2 CH2 enabled	**2** CH6 enabled	**2** CH4 slave	**2** Channels ON at turn-on
3 CH3 enabled	**3** CH7 enabled	**3** CH6 slave	**3** *Unused*
4 CH4 enabled	**4** CH8 enabled	**4** CH8 slave	**4** *Unused*

SPI interface

The LVR responds to 32-bit SPI commands following the structure of the **STD** word defined in the table below. The response follows the same **STD** structure unless **COMMAND** = **001**, in which case it returns **WORD2** in the following SPI command.

Bits	31-28	27-24	23-20	19-16	15-12	11-8	7-4	3-0
STD	**PAR & COMMAND**	**STATUS**	**SLAVE**	**UVL**	**READY8-5**	**READY4-1**	**ON8-5**	**ON4-1**
WORD2	0	0	**EN8-5**	**EN4-1**	0	**FW2**	**FW1**	**FW0**

The definition of the components in the **STD** structure are

STD word	Bit number	Write/ Read	Description
PAR & COMMAND	31	R	Parity bit, ie, **XOR(STD(30-0))**
	30 29 28	W/R	"000" → Read parameters in this table "001" → Read **WORD2** in the following SPI command "111" → Write
STATUS	27	R	Previous command timed out
	26	R	Previous command had bad parity bit
	25	R	Over-temperature state
	24	W/R	Low duty cycle (pulse mode)
SLAVE	23	R	Channel 8 is in slave mode
	22	R	Channel 6 is in slave mode
	21	R	Channel 4 is in slave mode
	20	R	Channel 2 is in slave mode
UVL	19	R	Input voltage below threshold for channels 7/8
	18	R	Input voltage below threshold for channels 5/6
	17	R	Input voltage below threshold for channels 3/4
	16	R	Input voltage below threshold for channels 1/2
READY8-5	15-12	W/R	Channels 8-5 READY
READY4-1	11-8	W/R	Channels 4-1 READY
ON8-5	7-4	W/R	Channels 8-5 ON
ON4-1	3-0	W/R	Channels 4-1 ON

WORD2 is a 32-bit word sent after **COMMAND** = **001**. The definition of its components is

❖ **EN8-1**: Whether channels 8 down to 1 are enabled by switches SW2 and SW3.

❖ **FW2/1/0**: The firmware version. For instance, **FW2** = 2, **FW1** = 0, and **FW0** = 1 would mean version 2.01.

Technical details of SPI protocol

The nominal frequency for the SPI protocol is 312.5 kHz, but frequencies between 10 kHz and 1 MHz should work.

Data is sampled on the rising edges of the SPI clock, and shifted on the falling edges.

LVR behavior

The LVR channels can be in one of three states: **OFF**, **STANDBY**, and **ON**.

❖ Going from **OFF** to **ON** requires a turn-on sequence that takes about 20 ms to complete.

➡ To set a channel to **ON** you need to set both the **READY** and **ON** bits to 1. A channel cannot be **ON** without being **READY**.

❖ The **STANDBY** state outputs ~130 mV, so basically no power, and allows us to go to **ON** immediately.

➡ To set a channel to **STANDBY** you set the **READY** bit to 1 and the **ON** bit to 0.

The status of the 8 channels can be controlled by the SPI interface, but a number of constraints override the SPI commands:

❖ Channels not enabled by switches SW2 and SW3 cannot become **READY**.

❖ If the LVR is over the maximum temperature set by SW1, or the input voltage is under the minimum voltage set by SW6A-D, the associated channels cannot become **READY**.

❖ If a channel is set to slave by SW4, its **READY** and **ON** states are controlled by its master. The master channel number is the slave's minus one, eg, if channel 4 is a slave, its states are controlled by channel 3.

Examples of SPI commands

The following would the responses by an LVR with the following characteristics:

➡ It has firmware 2.02 and was just turned-on

➡ It has all toggles in SW5 set to 0 (no duty cycle and by default channels start **OFF**)

➡ All channels in SW2 and SW3 are enabled

➡ Channel 4 is set to slave in SW4

➡ The temperature is ok, but the input voltage is insufficient for channels 1/2

#	Input to LVR from SOL40	Output from LVR	Comments
1	00 00 00 00	00 21 00 00	**READ**: all channels start **OFF**. The 21 indicates CH4 is a slave and CH1/2 have insufficient input voltage
2	70 00 FF F7	00 21 00 00	**WRITE**: turn all channels but CH4 **ON** and set CH4 to **STANDBY**. We read the status of the channels before turning them **ON**
3	00 00 00 00	00 21 FC FC	**READ**: CH1/2 cannot turn **ON** because insufficient input voltage. CH4 turned on because if follows its master CH3
4	90 00 00 00	00 21 FC FC	**REQUEST WORD2**
5	00 00 00 00	00 FF 02 02	**READ WORD2**: The FF indicates all channels are enabled and the 202 that the firmware version is 2.02
6	00 00 00 00	00 21 FC FC	**READ**
7	00 00 00 00	82 21 00 00	**READ**: all channels are now **OFF** due to **over-temperature**
8	00 00 00 00	00 21 FC FC	**READ**: over-temperature no more, so channels turned back **ON**
9	70 00 00 00	00 21 FC FC	**WRITE**: turn all channels **OFF**. Note the **bad parity bit**
10	00 00 00 00	84 21 FC FC	**READ**: channels were not turned **OFF** because of the bad parity bit in previous command, indicated by the 4