Mahavir Education Trust's
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UG Program in Electronics & Telecommunication Engineering

PC CONTROLLED SCROLLING MESSAGE DISPLAY

By

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INTRODUCTION:

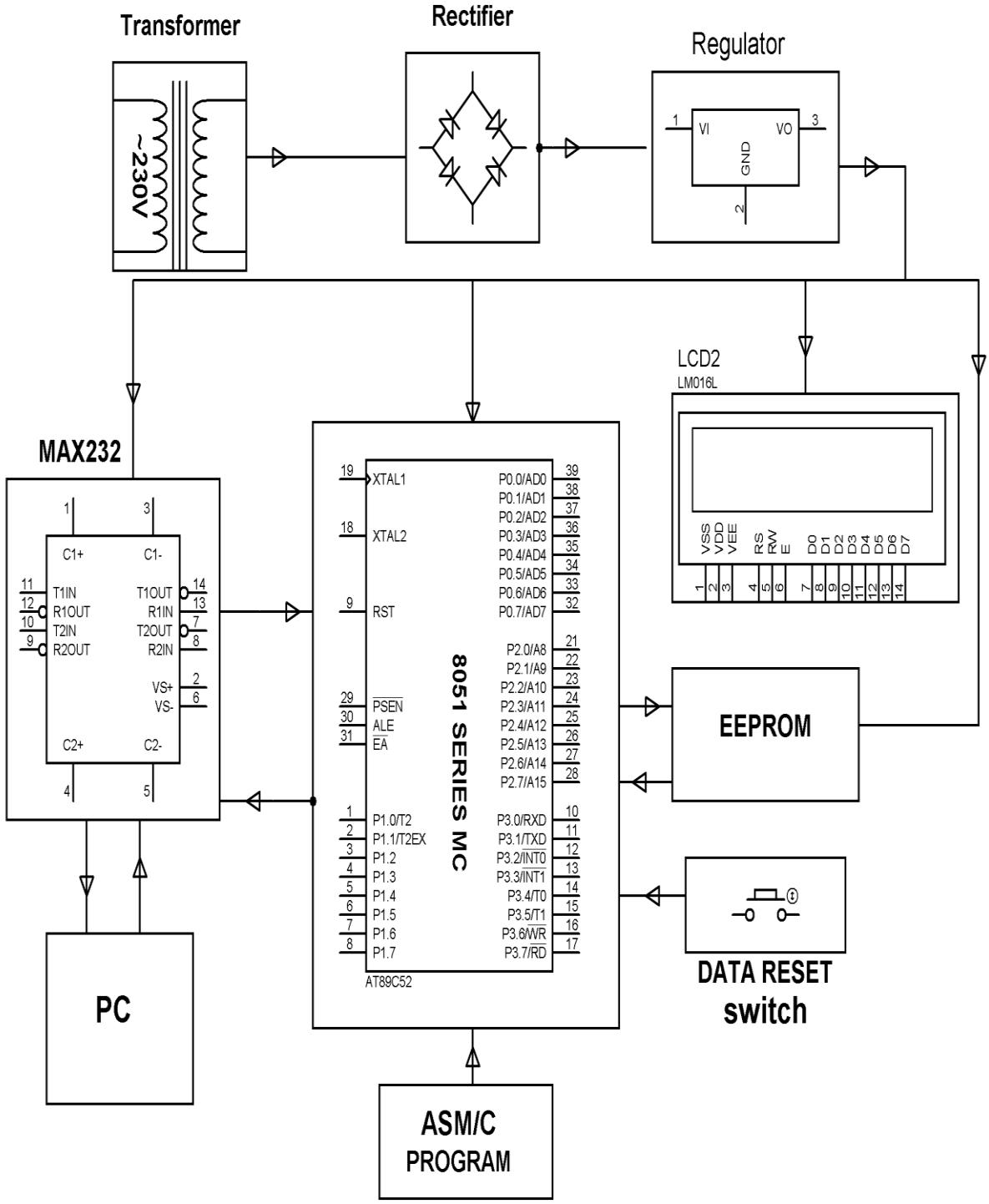
This project is designed to develop a PC controlled scrolling message display for notice board. It can also be used to display latest information anywhere such as colleges, shops, railway stations and other places. The information is transmitted using PC.

Traditionally notice board is all about sticking information, but sticking various notices day-to-day is a difficult process. A person is required separately to take care of this notice board. This system displays notices through a PC on notice boards.

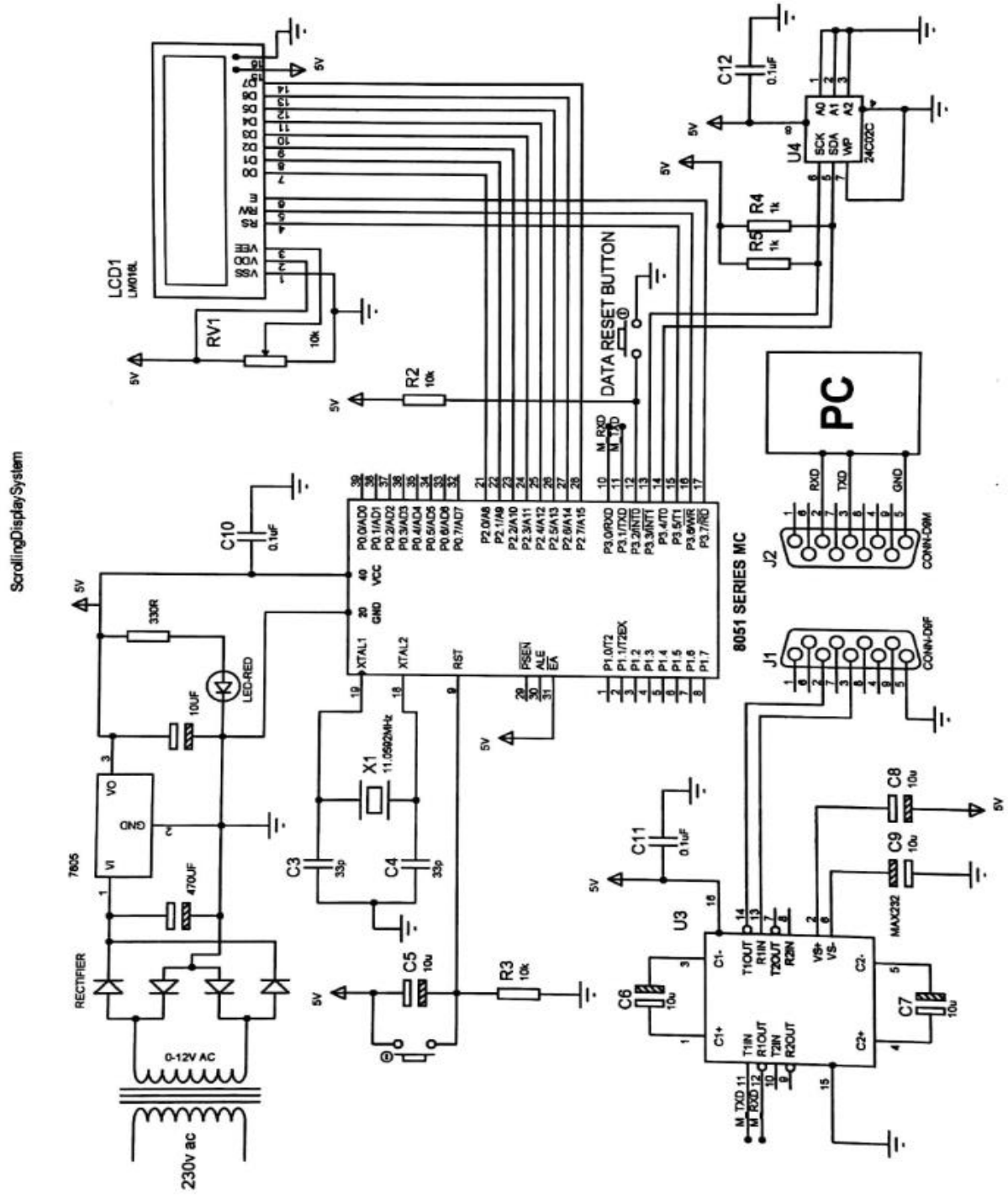
This system can be implemented in many important places where latest information can be displayed. For example if implemented in colleges all information for students can be displayed. It is very convenient for students and college management to display any information. This system can also be implemented in railway stations and airports to display information regarding the train and flight timings. This system reduces the wastage of papers. The information is sent through a PC, which is interfaced to a 8051 family microcontroller through MAX232 interface IC. An external memory connected to the microcontroller stores the information. An LCD is connected to the microcontroller to display the message in a continuous scrolling manner.

The project works only on operating systems having hyper terminal (E.g. Windows XP). The computer must have a RS232 serial port.

BLOCK DIAGRAM



CIRCUIT DIAGRAM



WORKING

This project is designed to develop a PC controlled scrolling message display. The information is transmitted using PC. The PC is interfaced to microcontroller through MAX232 IC and DB9 connector as explained above. An external memory (24C02) is used to store the information. It is interfaced with MC using SCL & SDA pins for reading and writing the data from the EEPROM. HyperTerminal is used to type the message and when enter is pressed a after typing the string the message is received by the MC and is displayed on a 16X2 LCD interfaced to the MC by scrolling the text entered. The information sent through PC is displayed on a LCD interfaced with the microcontroller.

OPERATION PROCEDURE

- Connect DB9 connector to PC and MC transmitter unit.
- Open HyperTerminal from the start menu (start> program> accessories> communications> HyperTerminal)
- Press interrupt button if the scrolling data is to be changed.
- “Enter the string1” is displayed on HyperTerminal
- Enter string and press enter
- “Enter the string2” is displayed on HyperTerminal
- Enter string and press enter
- OK is displayed on HyperTerminal.

PROGRAM CODE

```
#include<reg52.h>

sbit RS=P3^7;
sbit RW=P3^6;
sbit EN=P3^5;
sbit BUSY=P2^7;

sbit sda=P3^4;
sbit sclk=P3^3;

bit string_ovflg=0x10;
bit int0_flag=0x11;

#define LCDDATA P2

char ch,b,General_buf[50];
```

```
void lcd_init();

void lcd_cmd(unsigned char);

void lcd_data(unsigned char);

void lcd_string(unsigned char*);

void delay(unsigned int);

void delay1(unsigned int);

void Display_String1();

void Display_String2();


void Display_Strings1();

void Display_Strings2();

void BusyCheck();

void LCDCMD(unsigned char CMD);

void init_LCD();

void LCDData(unsigned char Data);

void send_string(char*s);

void send_to_mem(char s_address,char s_data);
```

```
void start_s_eeprom();

void send_byte_s_eeprom(char s_byte);

void acknowledge();

void stop_s_eeprom();

void wait();

void copy_string1();

void copy_string2();

void Read_string1();

void Read_string2();

char get_from_mem(char s_address);

char get_byte_s_eeprom();

void delay2();

void clear1stline();

void clear2ndline();

void clear_string1();

void clear_string2();

void Enter_strings();
```

```
void rs232_init();
{
    TMOD=0X20;
    TH1=0XFD;
    SCON=0X50;
    TR1=1;
}
void init0_ISR(void) interrupt 2;
{
    Enter_strings();
}
void Enter_strings()
{
    char p;
    LCDCMD(0X01);
    LCDCMD(0X80);
    lcd_string("ScrollingMessage");
    LCDCMD(0xC0);
```

```
lcd_string("Display System");
send_string("Enter String1:");
rs232_init();
p=0;
while(1)
{
        while(RI==0);
        RI=0;
        ch=SBUF;
        if(ch==0x0d)
        {
                General_Buf[p]='\0';
                delay2();
                clear_string1();
                copy_string1();
                break;
        }
        else
```

```
        {
                General_Buf[p]=ch;
        }
}
LCDCMD(0X01);
LCDCMD(0X80);
lcd_string("ScrollingMessage");
LCDCMD(0xC0);
lcd_string("Display System");
send_string("Enter String2:");
rs232_init();
p=0;
while(1)
{
        while(RI==0);
        RI=0;
        ch=SBUF;
        if(ch==0x0d)
```

```
        {
                General_Buf[p]='\0';
                delay2();
                clear_string2();
                copy_string2();
                break;
        }
        else
        {
                General_Buf[p]=ch;
        }
}
SBUF=0X0d;
while(TI==0);
TI=0;

SBUF=0X0a;
while(TI==0);
```

```
        TI=0;


        SBUF='O';
        while(TI==0);
        TI=0;


        SBUF='K';
        while(TI==0);
        TI=0;


        Read_string1();
        Read_string2();
        LCDCMD(0X01);
}
void send_string(char*s)
{
        SBUF=0X0d;
        while(TI==0);
```

```
TI=0;


SBUF=0X0a;
while(TI==0);
TI=0;


while(*s!='\0')
{
        SBUF=*s;
        while(TI==0);
        TI=0;
        s++;
}
SBUF=0X0d;
while(TI==0);
TI=0;


SBUF=0X0a;
```

```
        while(TI==0);
        TI=0;
}


void delay3()
{
        int f,g;
        for(f=0;f<30;f++)
        {
                for(g=0;g<2000;g++);
        }
}
void main()
{
        Init_LCD();
        EX0=1
        EA=1;
        LCDCMD(0X01);
```

```
        LCDCMD(0X80);
        lcd_string("ScrollingMessage");
        LCDCMD(0xC0);
        lcd_string("Display System");
        delay3();
        while(1)
        {
                Read_String1();
                Display_String1();
                Read_String2();
                Display_String2();
        }
}
void Display_String1()
{
        char k,l,m,pos=0x8f,count=1;
        LCDCMD(0x01);
        for(k=0;k<16;k++)
```

```
{
        LCDCMD(pos);
        for(I=0;I<count;I++)
        {
                LCDData(General_Buf[I]);
        }
        pos--;
        count++;
        delay(200);
}
count=16;
pos=0x80;
m=0;
while(1)
{
        clear1stline();
        LCDCMD(pos);
        I=0;
```

```
        while(I<count)
        {
            if(General_Buf[I+m]=='\0')
            {
                string_ovflg=1;
                break;
            }
            LCDData(General_Buf[I+m]);
            I++;
        }
        if(string_ovflg==1)
        {
            break;
        }
        delay(200);
    }
    pos=0x80;
    for(k=0;k<16;k++)
```

```
        {
                clear1stline();
                LCDCMD(pos);
                I=0;
                while(I<count)
                {
                        LCDData(General_Buf[I]);
                        I++;
                }
                count--;
                delay(200);
        }
}

void Display_String2()
{
        char k,l,m,pos=0xcf,count=1;
        LCDCMD(0x01)
```

```
for(k=0;k<16;k++)
{
        LCDCMD(pos);
        for(I=0;I<count;I++)
        {
                LCDData(General_Buf[I]);
        }
        pos--;
        count++;
        delay(200);
}
count=16;
pos=0xc0;
 while(1)
{
        clear2ndline();
        LCDCMD(pos);
        I=0;
```

```
        while(I<count)
        {
            if(General_Buf[I+m]=='\0')
            {
                string_ovflg=1;
            }
            LCDData(General_Buf[I+m]);
            I++;
        }
        if(string_ovflg==1)
        {
            break;
        }
        delay(200);
    }
    pos=0xc0;
    for(k=0;k<16;k++)
    {
```

```
            clear2ndline();
            LCDCMD(pos);
            I=0;
            while(I<count)
            {
                  LCDData(General_Buf[I]);
                  I++;
            }
            count--;
            delay(200);
      }
}

void clear1stline()
{
      LCDCMD(0x80);
      for(b=0;b<16;b++)
      {
```

```
            LCDData(' ');
        }
}
void clear2ndline()
{
        LCDCMD(0xc0);
        for(b=0;b<16;b++)
        {
            LCDData(' ');
        }
}
void LCDCMD(unsigned char CMD)
{
        LCDDATA=CMD;
        RS=0;
        RW=0;
        EN=1;
        EN=0;
```

```
}
void LCDData(unsigned char Data)
{
	LCDDATA=Data;
	RS=1;
	RW=0;
	EN=1;
	EN=0;
}
void lcd_string(char*s1)
{
	while(*s1!='\0')
	{
		LCDData(*s1);
		s1++;
	}
}
void Init_LCD()
```

```
{
        LCDCMD(0X38);
        LCDCMD(0X06);
        LCDCMD(0X0C);
        LCDCMD(0X02);
}
void delay(unsigned int i)
{
        unsigned int j,k;
        for(j=0;j<i:j++)
        {
                for(k=0;k<1000;k++)
                {
                        ;
                }
        }
}
```

```
void delay2()

{

        unsigned int u,v;

        for(u=0;u<2;u++)

        for(v=0;v<2000;v++);

}

void clear_string1()

{

        char x;

        for(x=0;x<50;x++)

        {

                send_to_mem((0x10+x,' ');

                delay2();

        }

}


void clear_string2()

{
```

```
        char x;
        for(x=0;x<50;x++)
        {
                send_to_mem((0x50+x,' ');
                delay2();
        }
}
void copy_string1()
{
        char x,Temp_cnt;
        Temp_cnt=get_from_mem(0x01);
        delay2();
        for(x=0;x<=Temp_cnt;x++)
        {
                send_to_mem((0x10+x),General_Buf[x]);
                delay2();
        }
}
```

```
void copy_string2()
{
    char x,Temp_cnt;
    Temp_cnt=get_from_mem(0x02);
    delay2();
    for(x=0;x<=Temp_cnt;x++)
    {
        send_to_mem((0x50+x),General_Buf[x]);
        delay2();
    }
}
void Read _string1()
{
    char y,Temp,Temp_cnt;
    for(y=0;y<50;y++)
    {
        General_Buf[y]='\0';
    }
```

```
        Temp_cnt=get_from_mem(0x08);
        delay2();
        for(y=50;y>Temp_cnt;y--)
        {
                Temp=get_from_mem(0x20+y);
                General_Buf[y]=Temp;
                delay2();
        }
}
void Read _string2()
{
        char y,Temp,Temp_cnt;
        for(y=0;y<50;y++)
        {
                General_Buf[y]='\0';
        }
        Temp_cnt=get_from_mem(0x05);
        delay2();
```

```
        for(y=50;y>Temp_cnt;y--)
        {
                Temp=get_from_mem(0x60+y);
                General_Buf[y]=Temp;
                delay2();
        }
}
char get_from_mem(char s_address)
{
        char i=0;
        start_s_eeprom();
        send_byte_s_eeprom(0x0A);
        acknowledge();
        send_byte_s_eeprom(s_address);
         acknowledge();

        start_s_eeprom();
        send_byte_s_eeprom(0xA1);
```

```
        acknowledge();
        i=get_byte_s_eeprom();
        acknowledge();
        stop_s_eeprom();
        acknowledge();
        return(i);
}

char get_byte_s_eeprom()
{
        char temp,temp_h,i;
        temp=0;
        sda=1;
        sclk=0;
        for(i=7;i>=0;i--)
        {
                sclk=1;
                if(sda==1)
```

```
            {
                temp=temp|temp_h>>i;
            }
        }
        reurn(temp);
}


void send_to_mem(char s_address,char s_data)
{
        start_s_eeprom();
        send_byte_s_eeprom(0xA0);
        acknowledge();
        send_byte_s_eeprom(s_address);
        acknowledge();
        send_byte_s_eeprom(s_data);
        acknowledge();
        stop_s_eeprom();
```

```
        acknowledge();
}
void start_s_eeprom()
{
        sda=1;
        sclk=1;
        wait();
        sda=0;
        sclk=0;
}
void send_byte_s_eeprom(char s_byte)
{
        char temp=s_byte;
        char i;
        for(i=7;i>=0;i--)
        {
                temp=s_byte;
                temp=temp<<i;
```

```
            temp=temp|0x01;


            if(temp==0)
                  sda=0;
            else
                  sda=1;
      }
}
void acknowledge()
{
      sclk=0;
      wait();
      sclk=0;
}
void stop_s_eeprom()
{
      sda=0;
      sclk=1;
```

```
        wait();

        sda=1;

        sclk=0;


}


void wait();

{

        char i;

        for(i=0;i<=200;i++)

        i++;

}
```

APPLICATIONS

- Used in public transports like trains, busses, etc.
- Used in airports for displaying schedules.
- Used in noticeboards.
- Used for advertisement purposes in shopping malls.
- Used to display information
  - Share markets
  - Hospitals
  - Libraries
  - Educational Institutes
- Used as a sub-part in various electronic circuits
  - 8051 & 8086 practice kits for students.
  - Other devices that require user communication.

ADVANTAGES

- Messages displayed are more attractive and catchy to eye.
- Seems to be a modern way of communication.
- Has been a efficient way for sharing information.

LIMITATIONS

- LCD consumes more power as that compared with LEDs
- Requires hyper-terminal for user inputs.

FUTURE SCOPE

- The system can be used as reference for developing other communication based projects.
- Various other advanced controllers can be used for making the project more efficient and much more user friendly.
- LEDs may be used instead of LCD as LEDs have more advantages as compared to LCD.

REFERENCES

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www.electronicsforu.com

www.brighthubengineering.com

www.atmel.com

www.beyondlogic.org

www.wikipedia.org

www.howstuffworks.com

www.alldatasheets.com

www.circuitstoday.com

TEXTBOOKS REFERRED

"The 8051 Microcontroller and Embedded systems" by Muhammad Ali Mazidi and Janice Gillispie Mazidi , Pearson Education.

ATMEL 89S52 Data Sheets.

COMPONENT LIST

Component Name	Quantity	Cost
RESISTORS		
22R	1	
330R	1	
10K	6	
10K PRESET	1	
1K	4	
CAPACITORS		
470uF/35V	1	
10uF/63V	2	
33pF Ceramic	2	
Integrated Circuits		
AT89S52	1	
24C02	1	
7805	1	
IC BASES		
40-PIN BASE	1	
8-PIN BASE	1	
16-PIN BASE	1	
DIODES		
1N4007	4	
RED-LED	3	
MISCELLANOUS		
CRYSTAL 11.0592MHz	1	
TRANSFORMER 0-12V	1	
2-PIN PUSH BUTTON	1	
LCD 16X2	1	
HEAT SINK	1	
SCREW NUT FOR HEAT-SINK	1	
FEMALE BURGE 16-PIN	1	
MALE BURGE 16-PIN	1	
FEMALE BURGE 2-PIN	1	
MALE BURGE 2-PIN	1	
12V RELAY	2	
PCB CONNECTOR 2-PIN	3	
POWER CORD	1	
PLAIN PCB	1	
SOLDERING LEAD (50gm)	1	

DATASHEETS

AT89S52

Features

- Compatible with MCS®-51 Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 10,000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option

8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

1. Description

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

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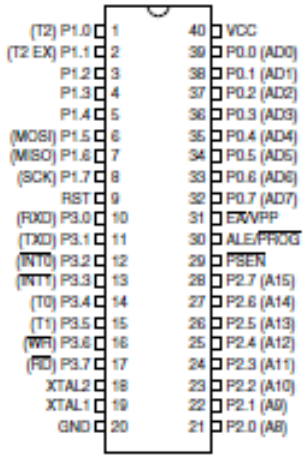
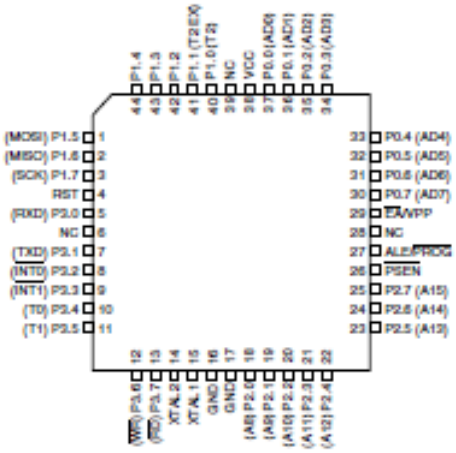
2. Pin Configurations

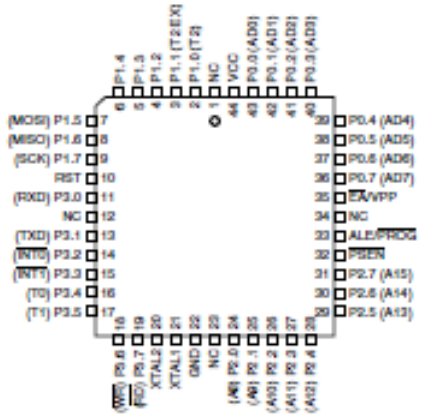
2.1 40-lead PDIP



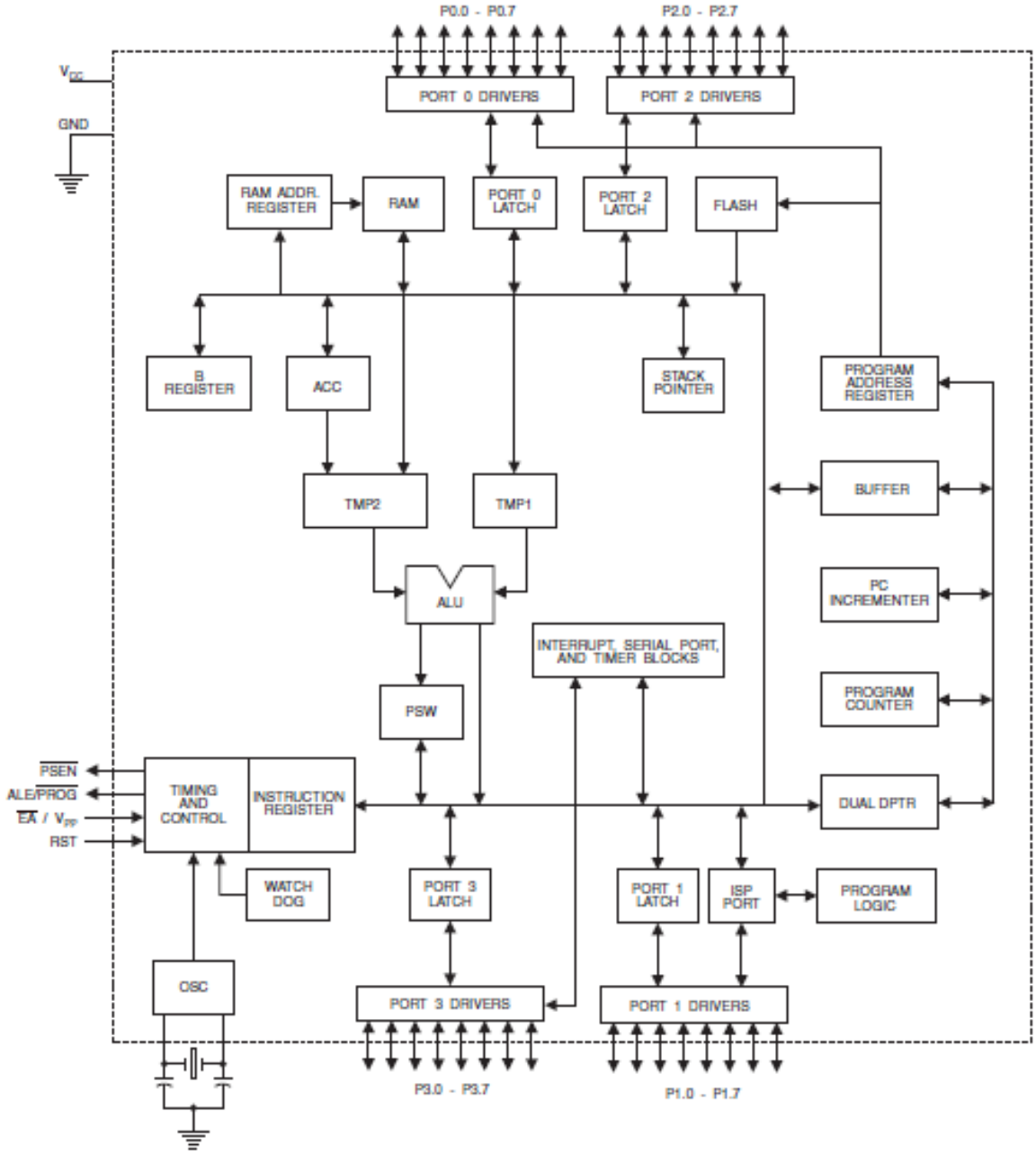
2.2 44-lead TQFP



2.3 44-lead PLCC



3. Block Diagram



4. Pin Description

4.1 VCC

Supply voltage.

4.2 GND

Ground.

4.3 Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

4.4 Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

4.5 Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

4.6 Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

4.7 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

4.8 ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

4.9 $\overline{\text{PSEN}}$

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

4.10 $\overline{\text{EA}}$/VPP

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

4.11 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

4.12 XTAL2

Output from the inverting oscillator amplifier.

5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 5-2) and T2MOD (shown in Table 10-2) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 5-1. AT89S52 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

Table 5-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 5-3. AUXR: Auxiliary Register

AUXR	Address = 8EH						Reset Value = XXX00XX0B	
	Not Bit Addressable							
	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion	
DISALE	Disable/Enable ALE	
	DISALE	Operating Mode
	0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1	ALE is active only during a MOVX or MOVC instruction
DISRTO	Disable/Enable Reset out	
	DISRTO	
	0	Reset pin is driven High after WDT times out
	1	Reset pin is input only
WDIDLE	Disable/Enable WDT in IDLE mode	
	WDIDLE	
	0	WDT continues to count in IDLE mode
	1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 5-4. AUXR1: Auxiliary Register 1

AUXR1	Address = A2H						Reset Value = XXXXXXX0B	
	Not Bit Addressable							
	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion	
DPS	Data Pointer Register Select	
	DPS	
	0	Selects DPTR Registers DP0L, DP0H
	1	Selects DPTR Registers DP1L, DP1H

6. Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

6.1 Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

6.2 Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

7. Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

7.1 Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When

WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

7.2 WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

8. UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

9. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

10. Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 5-2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 10-1. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 10-1. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

10.1 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 10-1.

10.2 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 10-2). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 10-1. Timer in Capture Mode

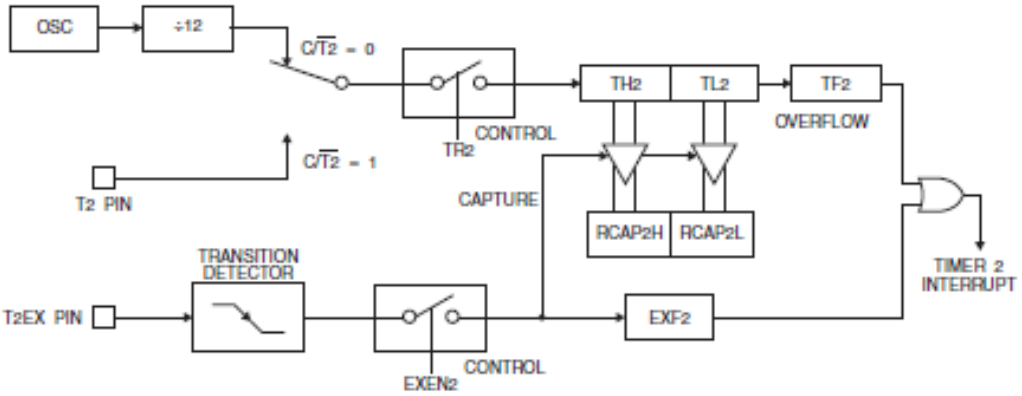


Table 10-2. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	T2OE	DCEN

Symbol	Function
–	Not implemented, reserved for future
T2OE	Timer 2 Output Enable bit
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter

Figure 10-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 10-2. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 10-2. Timer 2 Auto Reload Mode (DCEN = 0)

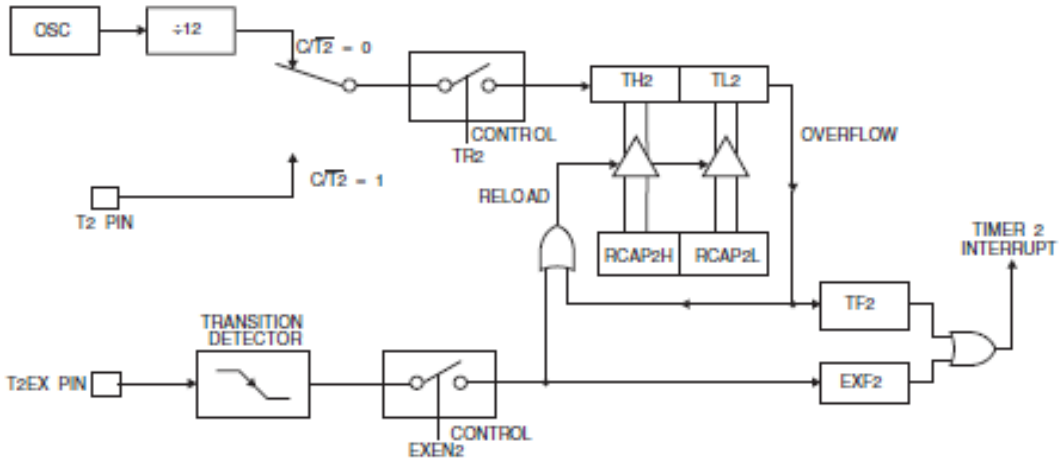
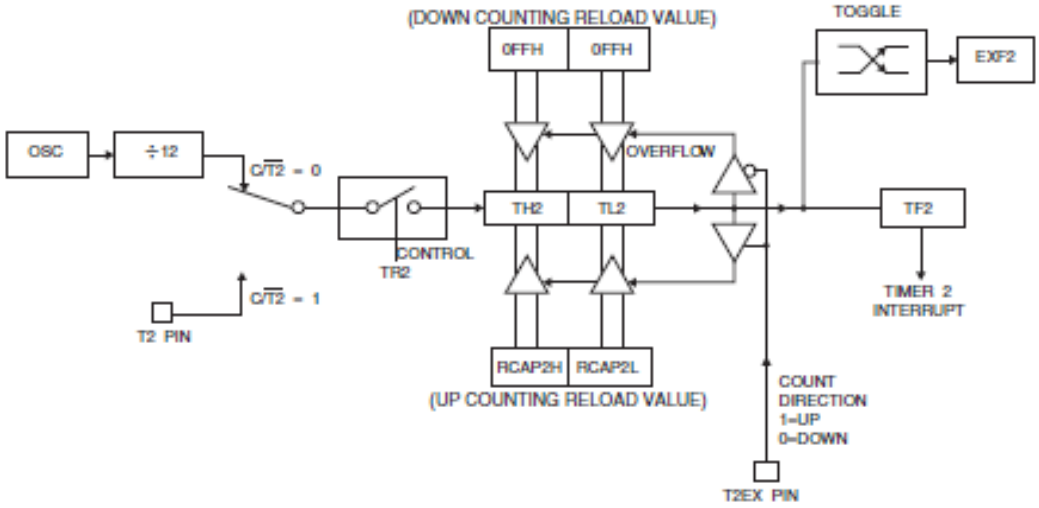


Figure 10-3. Timer 2 Auto Reload Mode (DCEN = 1)



11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 5-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 11-1.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

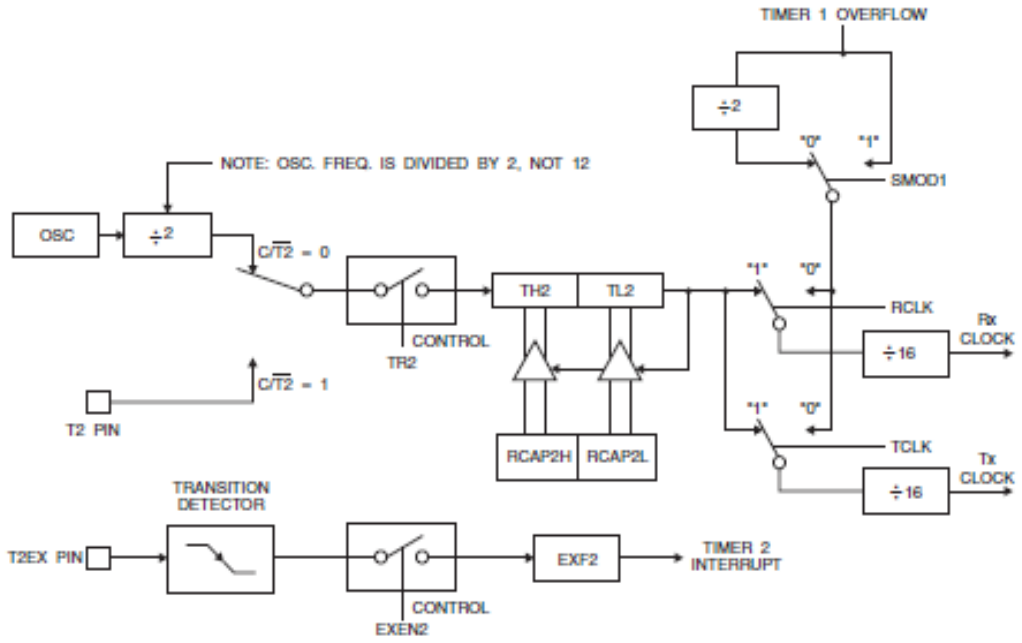
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - \text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 11-1. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 11-1. Timer 2 in Baud Rate Generator Mode



12. Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 12-1. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

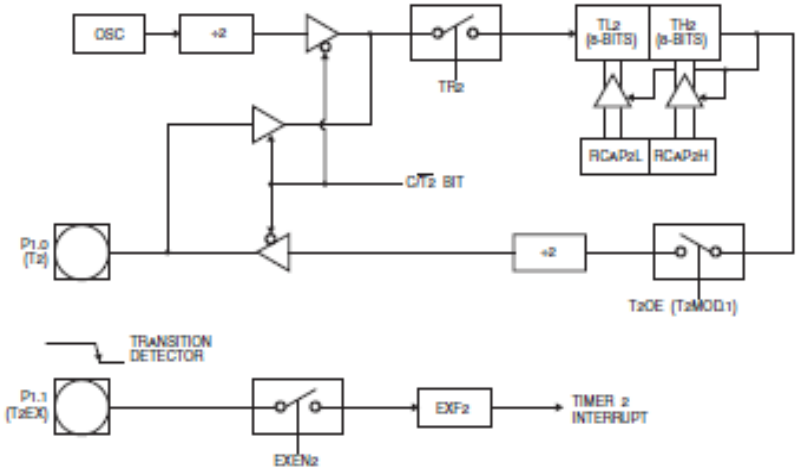
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 12-1. Timer 2 in Clock-Out Mode



13. Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 13-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 13-1 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 13-1. Interrupt Enable (IE) Register

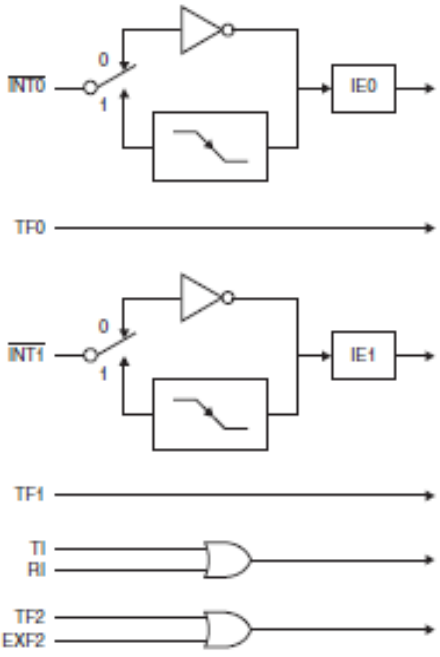
(MSB)							(LSB)
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

Figure 13-1. Interrupt Sources



14. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 16-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 16-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

15. Idle Mode

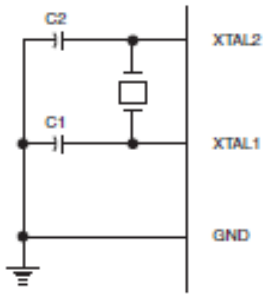
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

16. Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 16-1. Oscillator Connections



Note: 1. C1, C2 = 30 pF ±10 pF for Crystals
= 40 pF ±10 pF for Ceramic Resonators

Figure 16-2. External Clock Drive Configuration

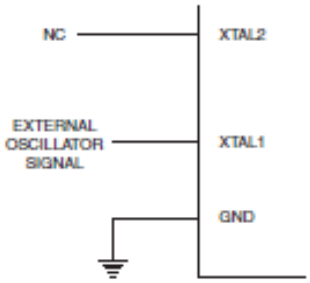


Table 16-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

17. Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 17-1.

Table 17-1. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

18. Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the "Flash Programming Modes" (Table 22-1) and Figure 22-1 and Figure 22-2. To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{pp}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates AT89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

19. Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

20. Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

1. Set XTAL1 to "L" (if a crystal is not used).
2. Set RST to "L".
3. Turn V_{CC} power off.

Data Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

21. Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 24-1.

22. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 22-1. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

Notes:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 22-1. Programming the Flash Memory (Parallel Mode)

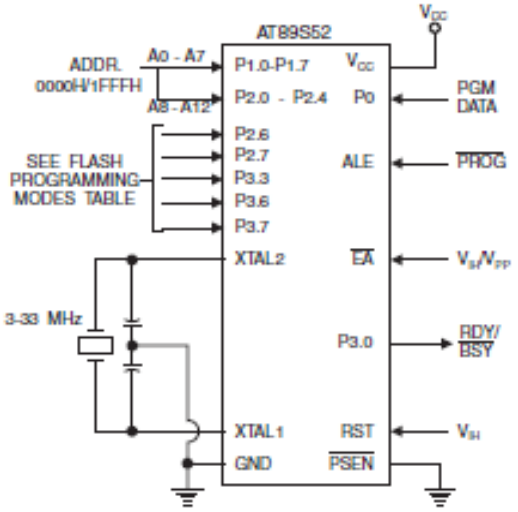
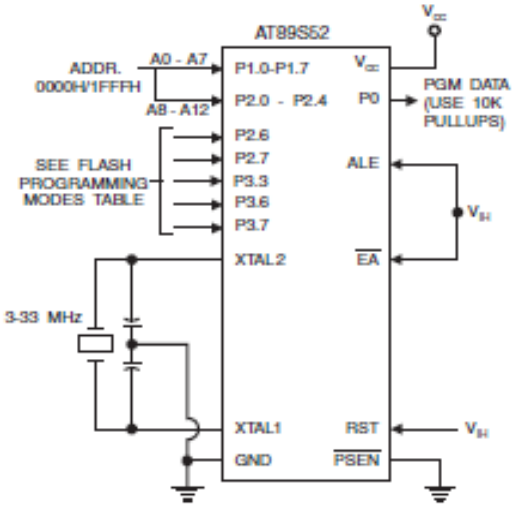


Figure 22-2. Verifying the Flash Memory (Parallel Mode)



23. Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHAX}	Address Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHDX}	Data Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48 t_{CLCL}		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		48 t_{CLCL}	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		48 t_{CLCL}	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	48 t_{CLCL}	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 23-1. Flash Programming and Verification Waveforms – Parallel Mode

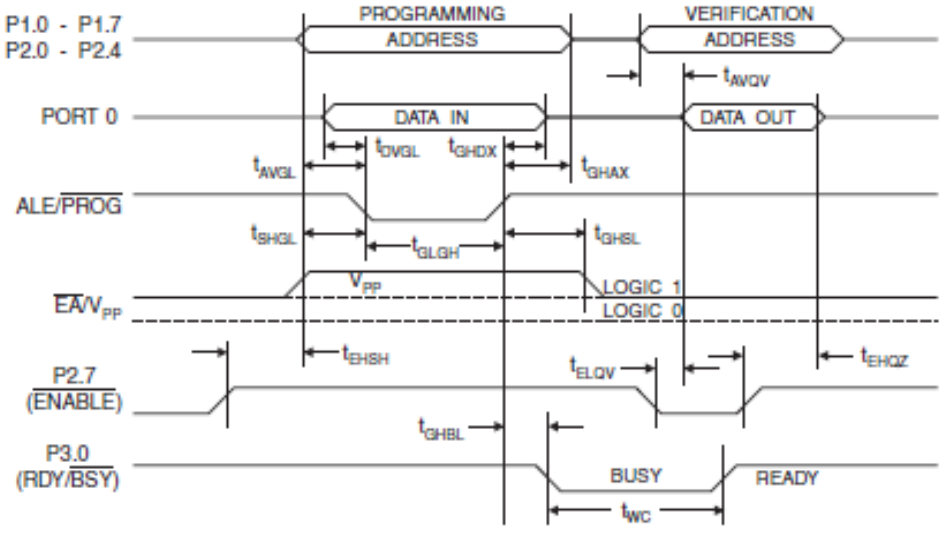
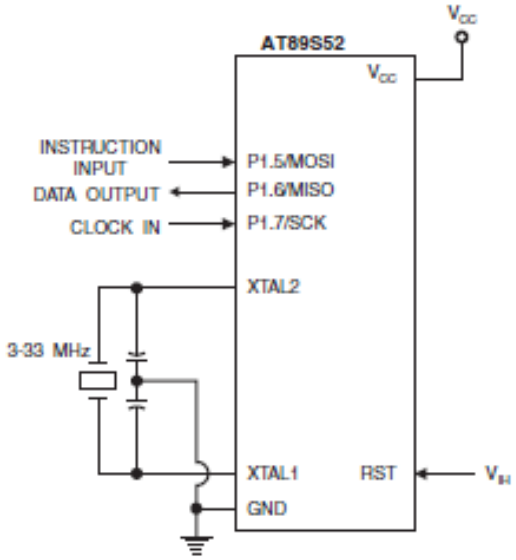


Figure 23-2. Flash Memory Serial Downloading



24. Flash Programming and Verification Waveforms – Serial Mode

Figure 24-1. Serial Programming Waveforms

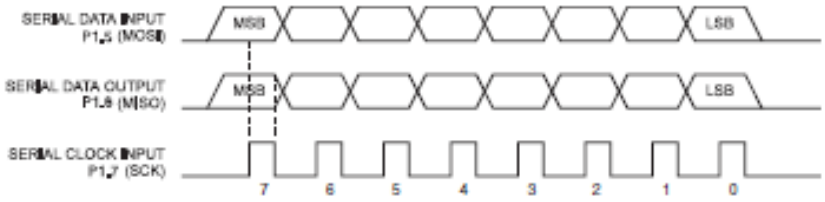


Table 24-1. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[1]	1010 1100	1110 00B2B1	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxxLB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes	0010 1000	xxx A12 A11 A10 A9 A8	0000 0000	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note: 1. B1 = 0, B2 = 0 ---> Mode 1, no lock protection
B1 = 0, B2 = 1 ---> Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 ---> Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 ---> Mode 4, lock bit 3 activated

} Each of the lock bit modes needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

25. Serial Programming Characteristics

Figure 25-1. Serial Programming Timing

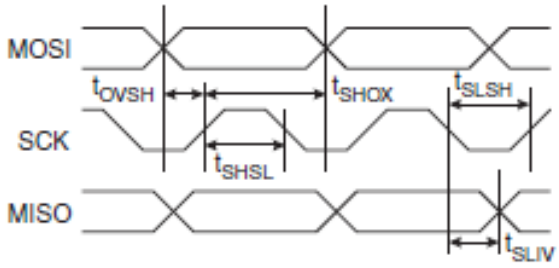


Table 25-1. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

26. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

27. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-300	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

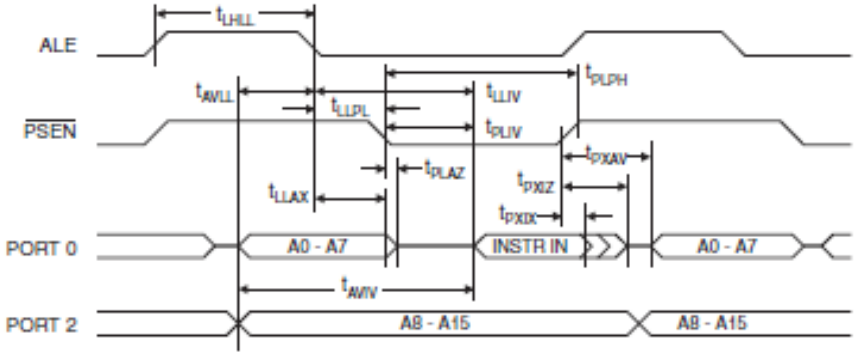
28. AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

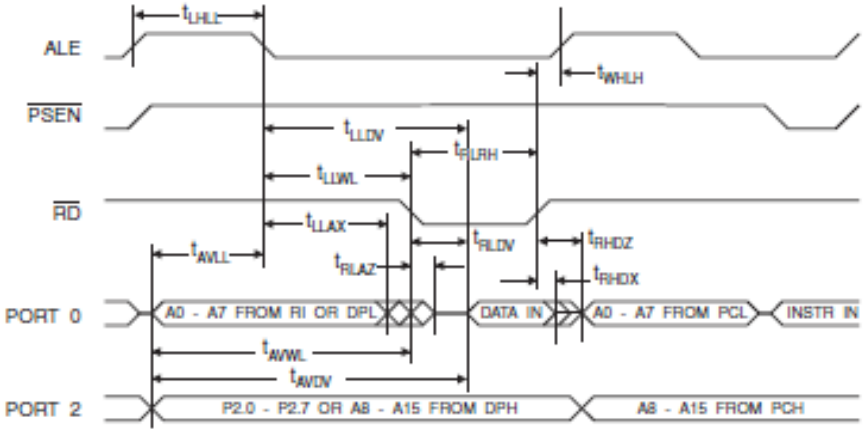
28.1 External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

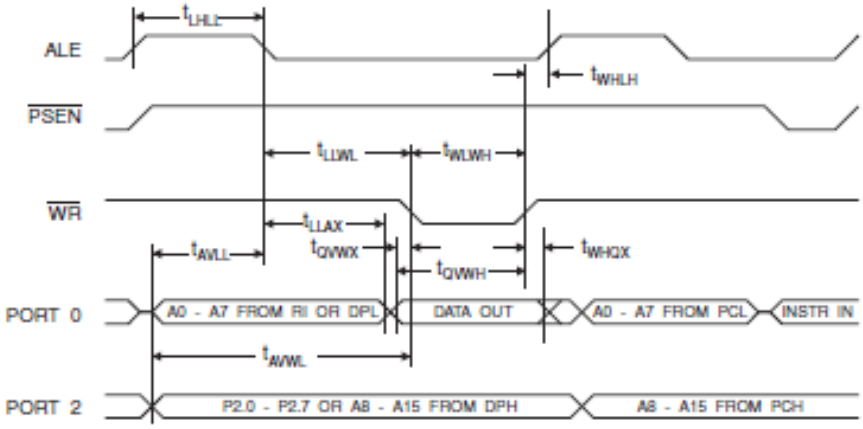
29. External Program Memory Read Cycle



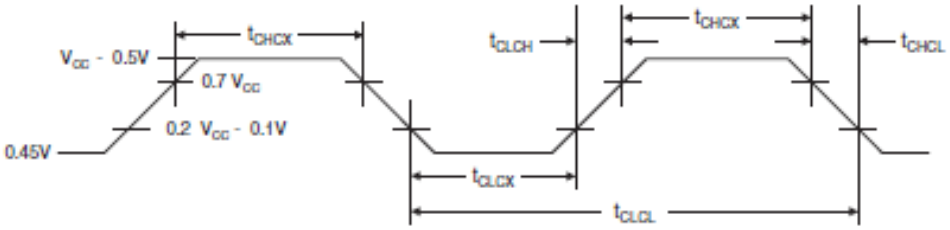
30. External Data Memory Read Cycle



31. External Data Memory Write Cycle



32. External Clock Drive Waveforms



33. External Clock Drive

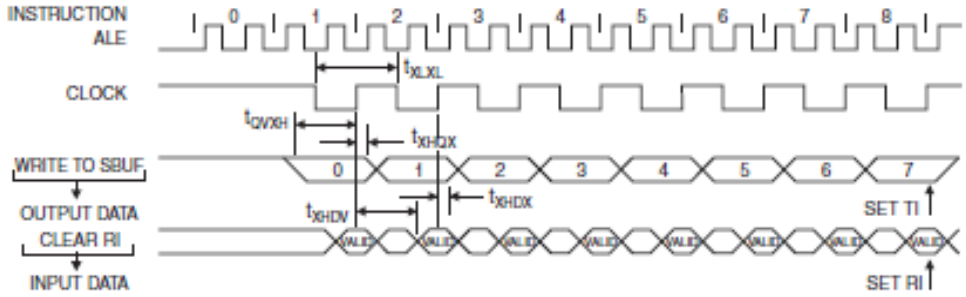
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

34. Serial Port Timing: Shift Register Mode Test Conditions

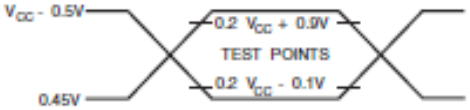
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		12 t_{CLCL}		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		10 t_{CLCL}-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		2 t_{CLCL}-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		10 t_{CLCL}-133	ns

35. Shift Register Mode Timing Waveforms

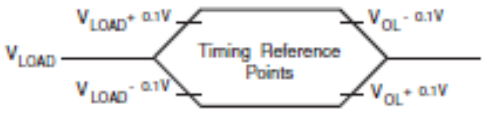


36. AC Testing Input/Output Waveforms[1]



Note: 1. AC inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

37. Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

38. Ordering Information

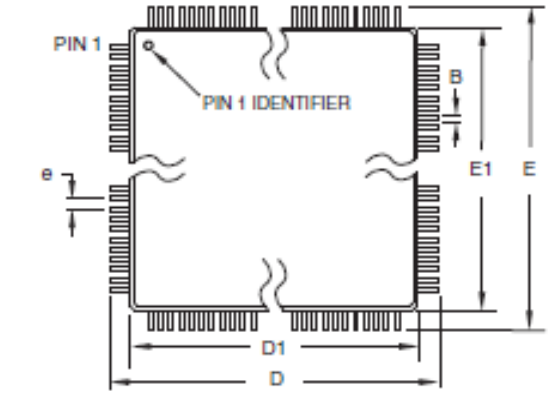
38.1 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AU AT89S52-24JU AT89S52-24PU	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S52-33AU AT89S52-33JU AT89S52-33PU	44A 44J 40P6	Industrial (-40° C to 85° C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

39. Packaging Information

39.1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

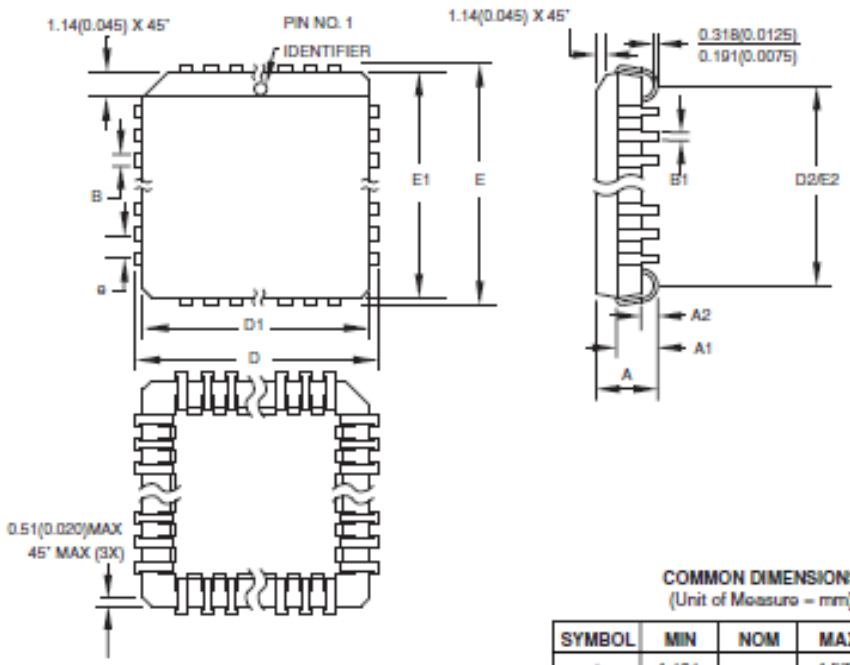
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

39.2 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure – mm)

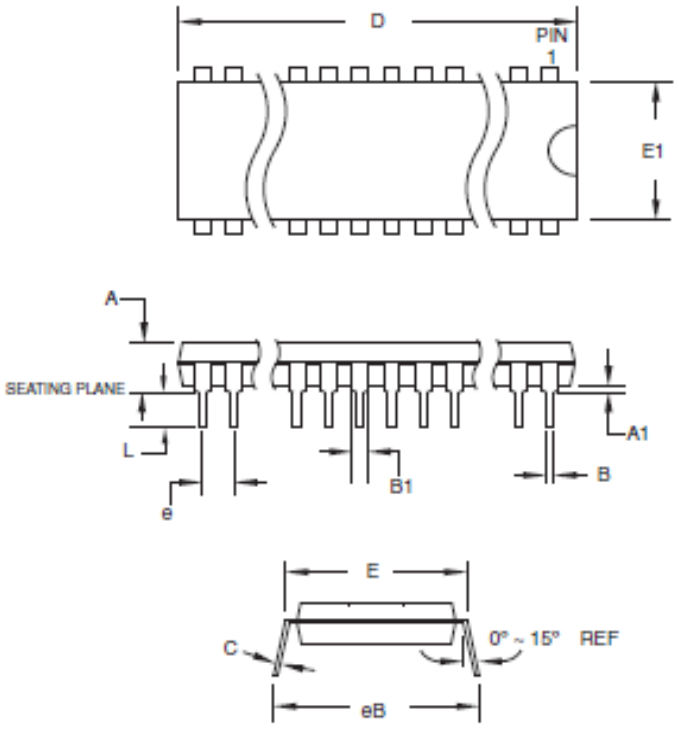
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

2325 Orchard Parkway San Jose, CA 95131	TITLE **44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	DRAWING NO. 44J	REV. B

39.3 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

EEPROM

Features

- Low-voltage and Standard-voltage Operation
  - V_{CC} = 1.7V to 5.5V
- Internally Organized 256 x 8 (2K)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1MHz (5V), 400kHz (1.7V, 2.5V, 2.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-byte Page (2K) Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Green (Pb/Halide-free/RoHS Compliant) Package Options
- Die Sales: Wafer Form and Tape and Reel

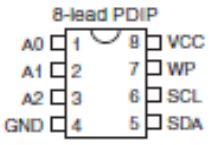
Description

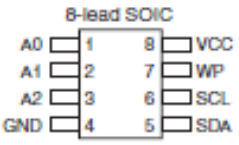
The Atmel® AT24C02C provides 2048-bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256-words of 8-bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C02C is available in space-saving 8-lead PDIP, 8-lead TSSOP, 8-lead JEDEC SOIC, 8-lead UDFN, 5-lead SOT23 and 8-ball VFBGA packages and is accessed via a two-wire serial interface.

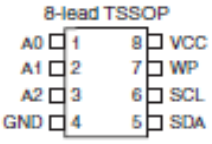
Table 0-1. Pin Configuration

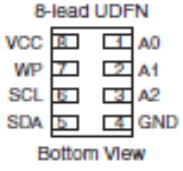
Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
VCC	Power Supply

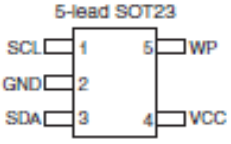
Note: For use of 5-lead SOT23, the software A2, A1, and A0 bits in the device address word must be set to zero to properly communicate

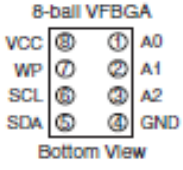












Two-wire Serial Electrically Erasable and Programmable Read-only Memory

2K (256 x 8)

Atmel AT24C02C

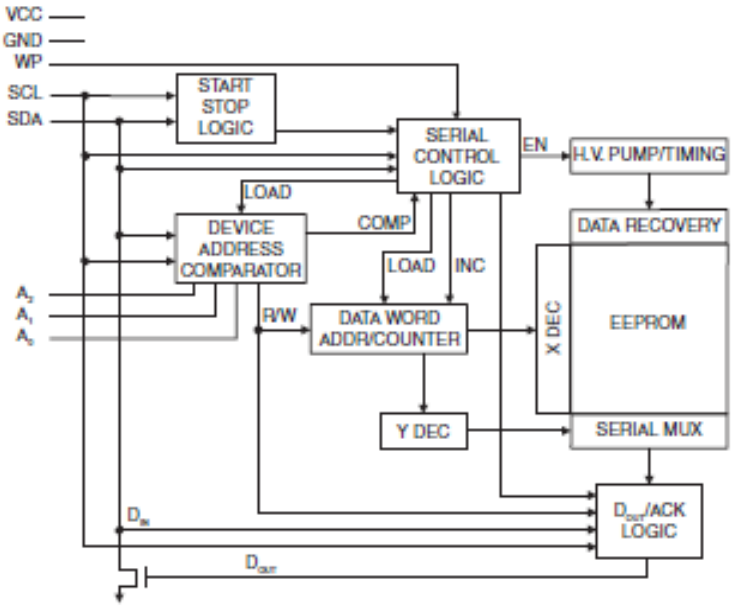
8700D–SEEPR–8/10

Absolute Maximum Ratings

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 0-1. Block Diagram



1. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the Atmel® AT24C02C. As many as eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

WRITE PROTECT (WP): AT24C02C has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when connected to ground (GND). When the write protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in Table 1-1.

Table 1-1. Write Protect

WP Pin Status	Part of the Array Protected
	Atmel 24C02C
At V_{CC}	Full (2K) Array
At GND	Normal Read/Write Operations

2. Memory Organization

Atmel AT24C02C, 2K SERIAL EEPROM: Internally organized with 32 pages of 8-bytes each, the 2K requires an 8-bit data word address for random word addressing.

Table 2-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +1.7V to +5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested

Table 2-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.7		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested

Table 2-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = +1.7V to +5.5V, CL = 1TTL Gate and 100pF (unless otherwise noted)

Symbol	Parameter	1.7, 2.5, 2.7		5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_I	Noise Suppression Time		50		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Setup Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Setup Time	100		100		ns
t_R	Inputs Rise Time[1]		0.3		0.3	µs
t_F	Inputs Fall Time[1]		300		100	ns
$t_{SU.STO}$	Stop Setup Time	0.6		.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance[1]	5.0V, 25-C, Byte Mode	1 Million				Write Cycles

Note: 1. This parameter is ensured by characterization only

3. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 5-2 on page 8). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 5-3 on page 8).

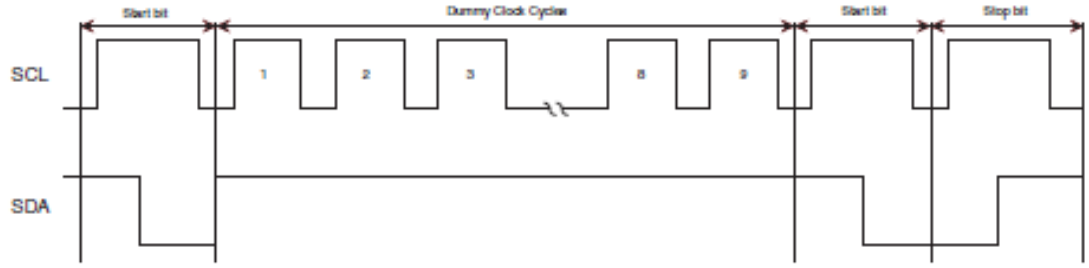
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5-3 on page 8).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The Atmel® AT24C02C features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

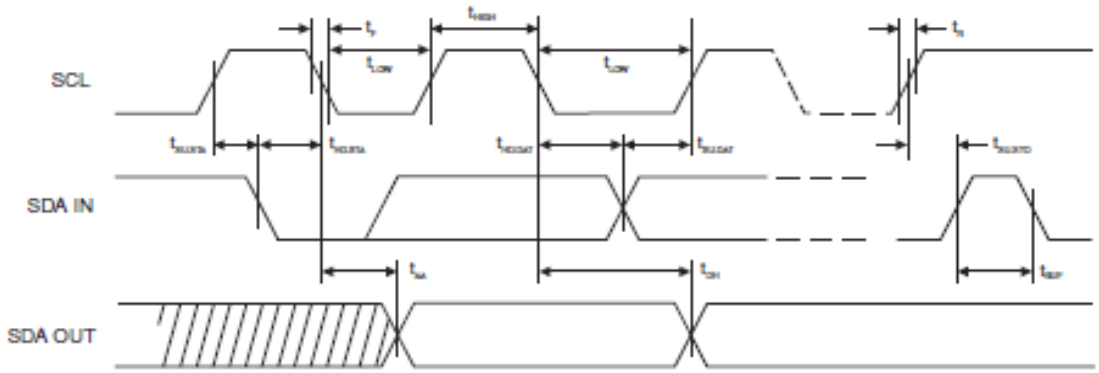
2-Wire Software Reset: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps: (a) Create a start bit condition, (b) clock 9 cycles, (c) create another start bit followed by stop bit condition as shown below. The device is ready for next communication after above steps have been completed.

Figure 3-1. Software reset



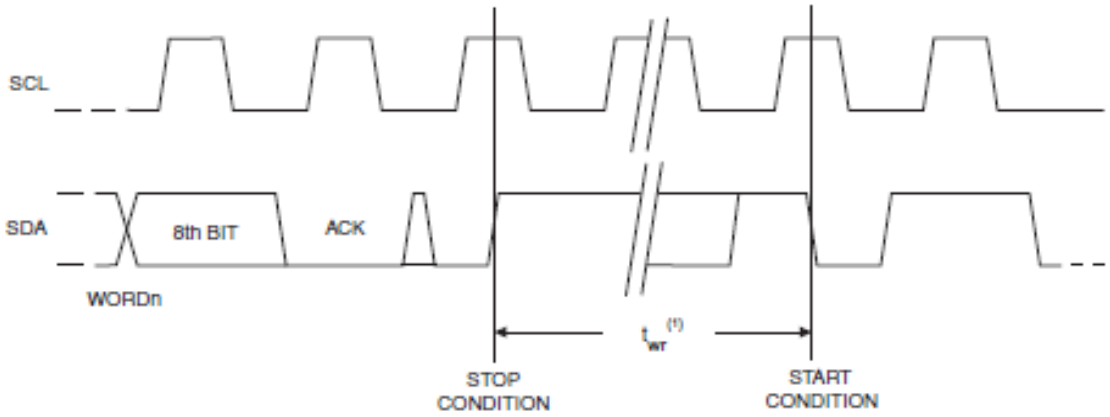
4. Bus Timing

Figure 4-1. SCL: Serial Clock, SDA: Serial Data I/O



5. Write Cycle Timing

Figure 5-1. SCL: Serial Clock, SDA: Serial Data I/O



Notes: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle

Figure 5-2. Data Validity

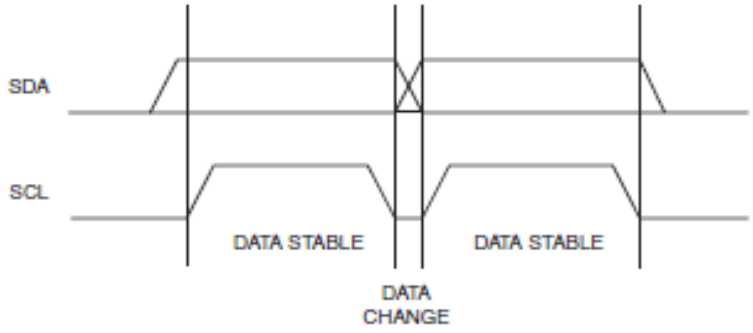


Figure 5-3. Start and Stop Definition

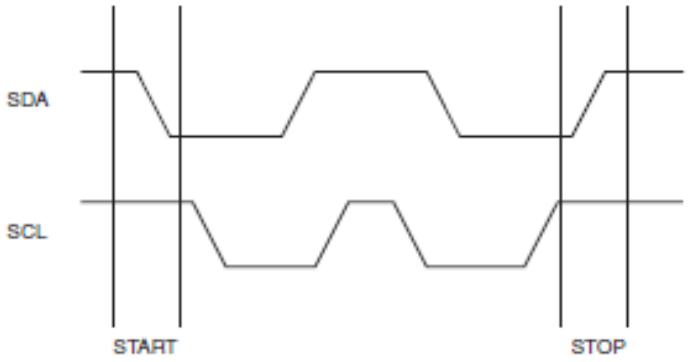
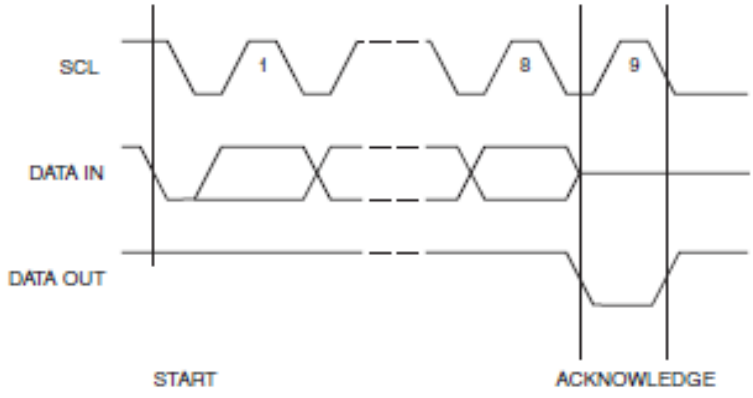


Figure 5-4. Output Acknowledge



6. Device Addressing

The 2K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 8-1).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next three bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These three bits must compare to their corresponding hard-wired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

7. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8-2 on page 10).

PAGE WRITE: The 2K EEPROM is capable of an 8-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 8-3 on page 10).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

8. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the

first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 8-4 on page 11).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8-5 on page 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8-6 on page 11).

Figure 8-1. Device Address

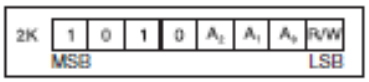


Figure 8-2. Byte Write

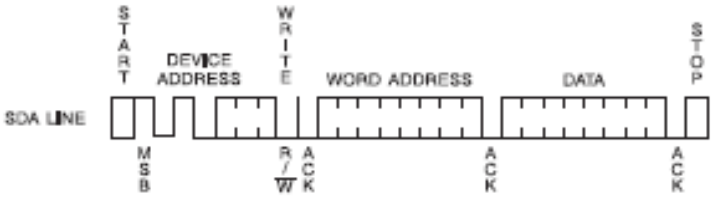


Figure 8-3. Page Write

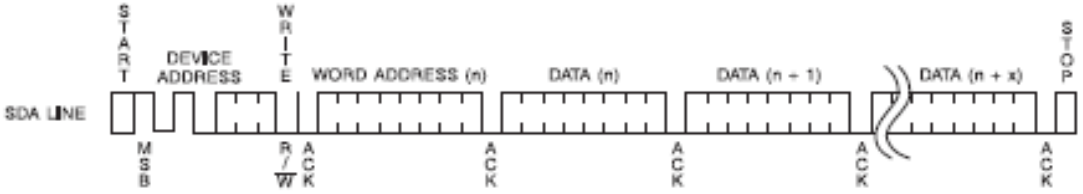


Figure 8-4. Current Address Read

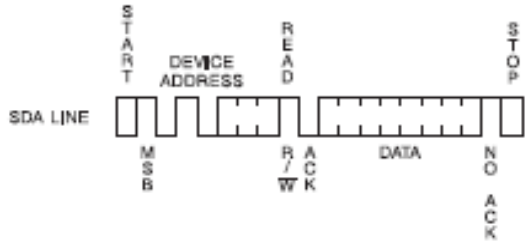


Figure 8-5. Random Read

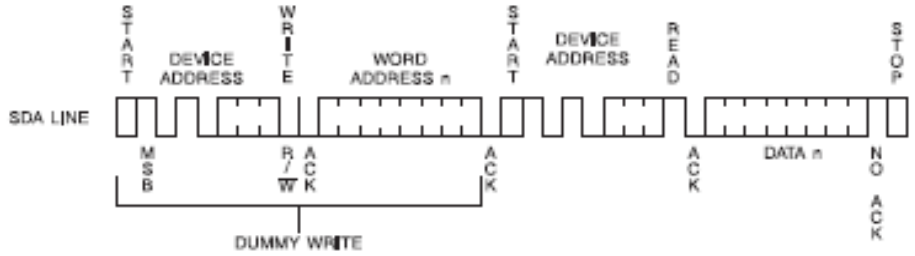
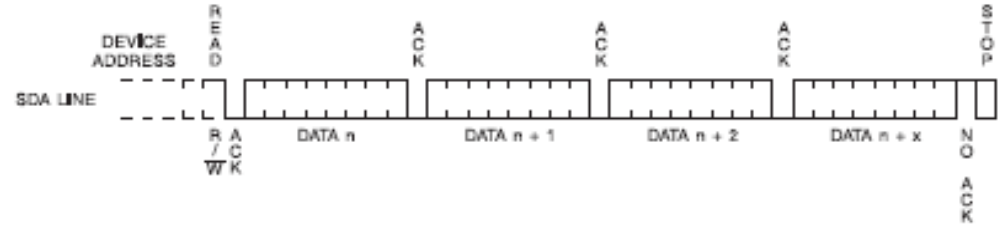
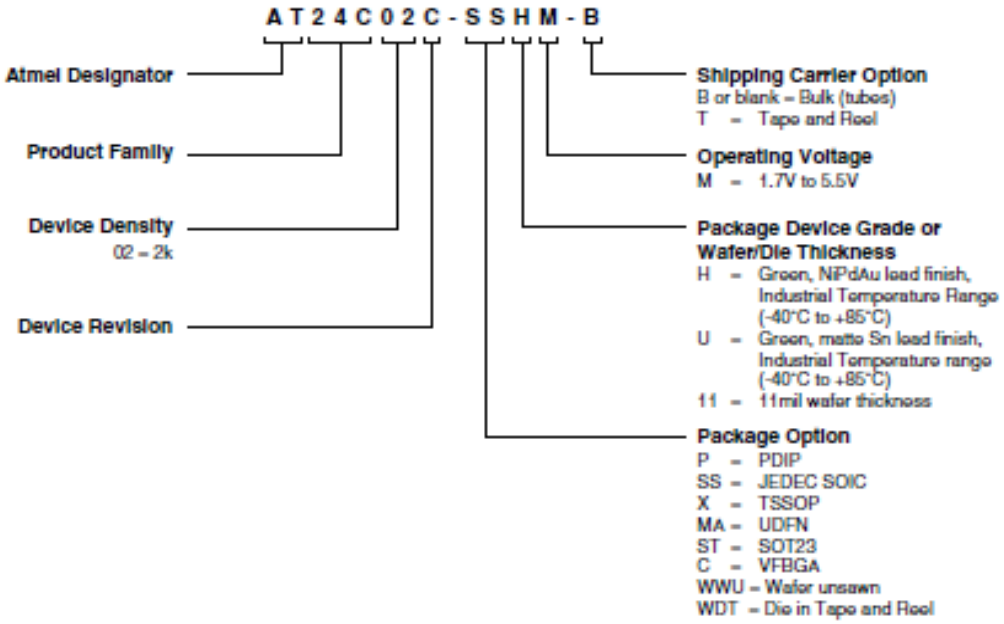


Figure 8-6. Sequential Read

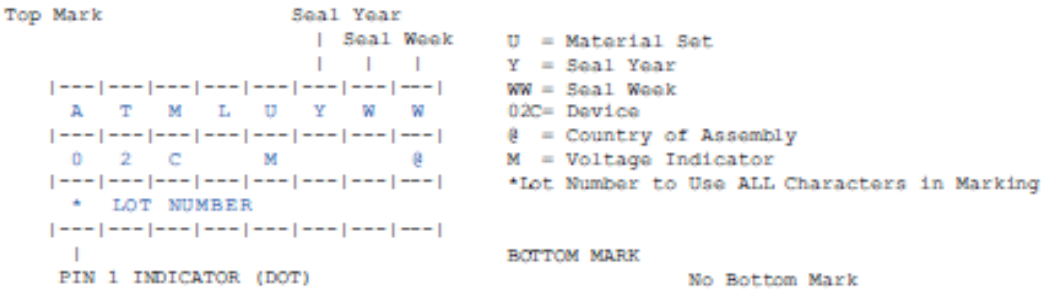


9. Ordering Code Detail

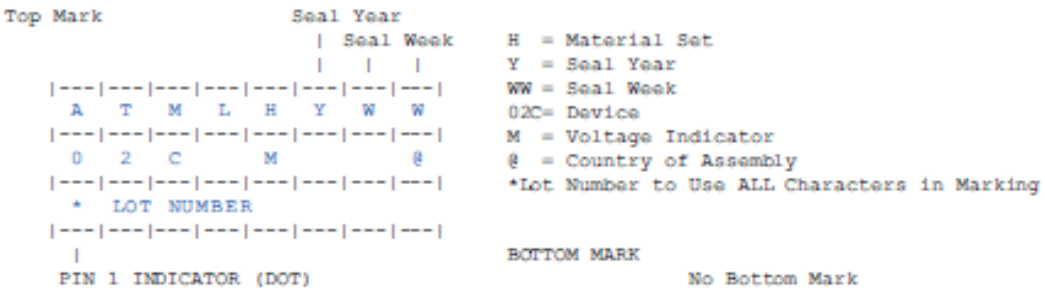


10. Part Markings

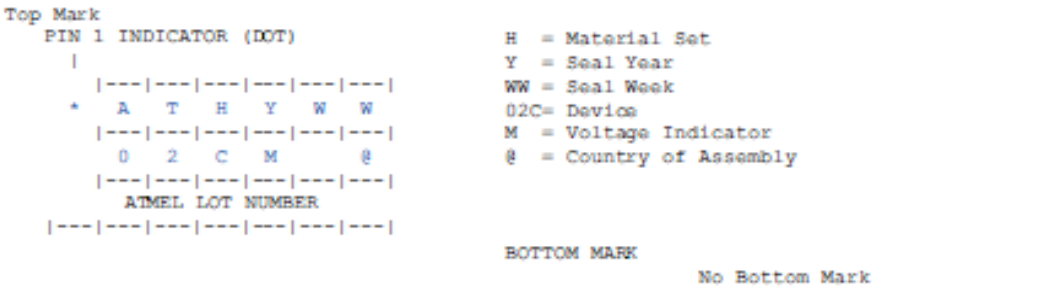
Atmel AT24C02C-PUM



Atmel AT24C02C-SSHM



Atmel AT24C02C-XHM



Atmel AT24C02C-MAHM

Top Mark

```
|---|---|---|
  0   2   C
|---|---|---|
  H   M   @
|---|---|---|
  Y   T   C
|---|---|---|
  *
  | PIN 1 INDICATOR (DOT)
```

02C= Device
H = Material Set
M = Voltage Indicator
@ = Country of Assembly
Y = Year of Assembly
TC = Trace Code

Atmel AT24C02C-STUM

Top Mark

```
                |---|---|---|---|---|
Line 1 -------->  2   C   M   B   U
                |---|---|---|---|---|
                  *
                  |
                PIN 1 INDICATOR (DOT)
```

2C = Device
M = Voltage Indicator
B = Write Protection
U = Material Set

Bottom Mark

```
|---|---|---|---|
  Y   M   T   C
|---|---|---|---|
```

Y = One Digit Year Code
M = Seal Month
TC = Trace Code

Atmel AT24C02C-CUM

Top Mark

```
Line 1 -------> 02CU
Line 2 -------> YMTC
                |<--PIN 1 THIS CORNER
```

02C= Device
U = Material Set
Y = One Digit Year Code
M = Seal Month
TC = Trace Code

11. Ordering Codes

Atmel AT24C02C Ordering Information

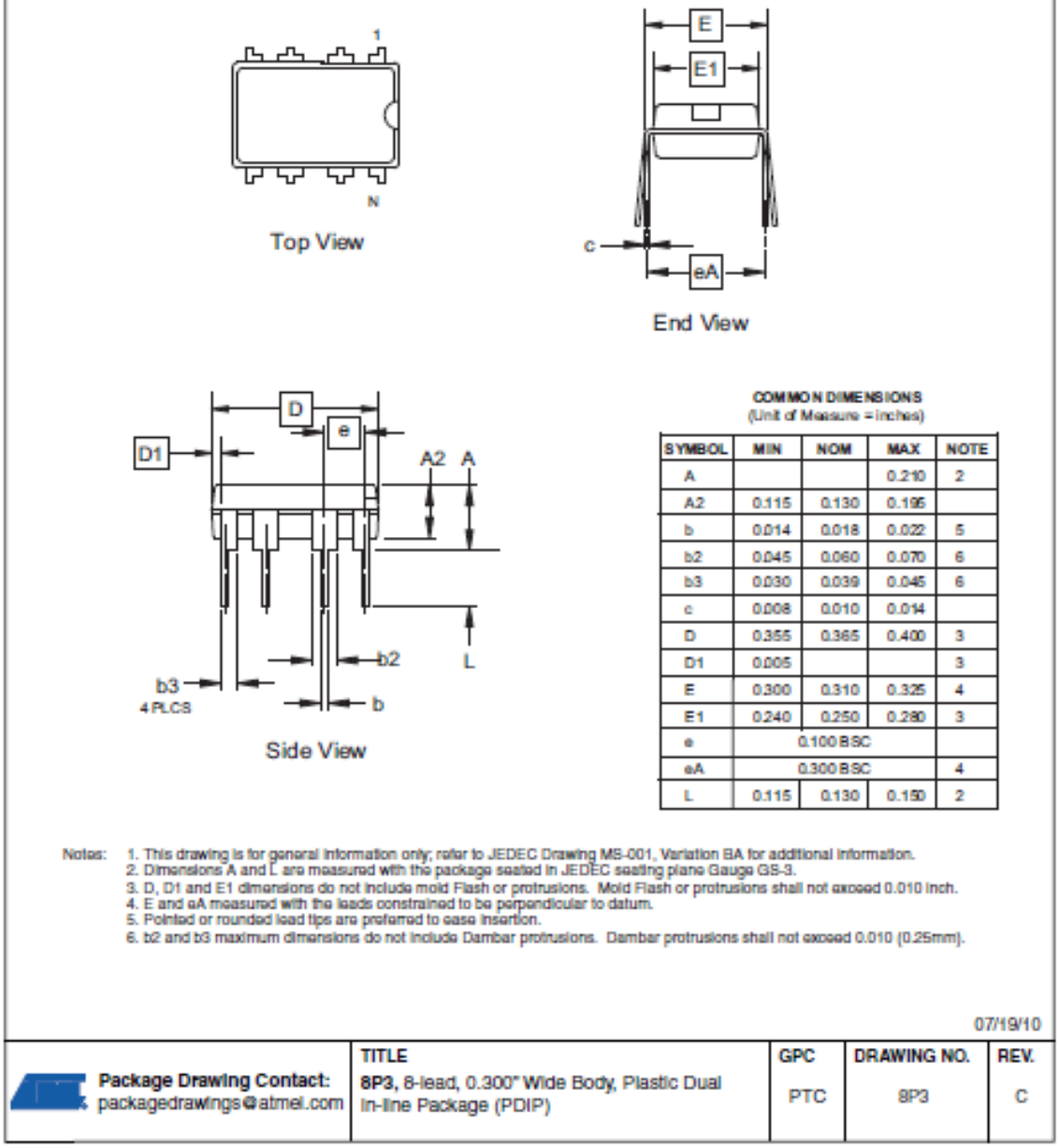
Ordering Code	Voltage	Package	Operation Range
AT24C02C-PUM (Bulk form only)	1.7V to 5.5V	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT24C02C-SSHM-B[1] (NiPdAu Lead Finish)	1.7V to 5.5V	8S1	
AT24C02C-SSHM-T[2] (NiPdAu Lead Finish)	1.7V to 5.5V	8S1	
AT24C02C-XHM-B[1] (NiPdAu Lead Finish)	1.7V to 5.5V	8A2	
AT24C02C-XHM-T[2] (NiPdAu Lead Finish)	1.7V to 5.5V	8A2	
AT24C02C-MAHM-T[2] (NiPdAu Lead Finish)	1.7V to 5.5V	8Y6	
AT24C02C-STUM-T[2]	1.7V to 5.5V	5TS1	
AT24C02C-CUM-T[2]	1.7V to 5.5V	8U3-1	
AT24C02C-WWU11[3]	1.7V to 5.5V	Die Sale	Industrial Temperature (–40°C to 85°C)

Notes: 1. "-B" denotes bulk
2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP, UDFN, SOT23, and VFBGA = 5K per reel
3. For Wafer sales, please contact Atmel Sales

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch, Dual No Lead Package (UDFN)
5TS1	5-lead, 2.90mm x 1.60mm Body, Plastic Thin Shrink Small Outline Package (SOT23)
8U3-1	8-ball, die Ball Grid Array Package (VFBGA)

12. Packaging Information

8P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = Inches)

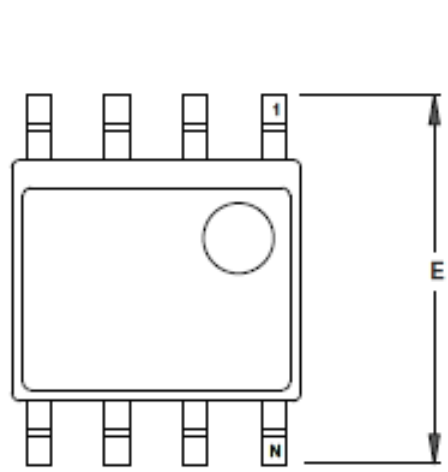
SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25mm).

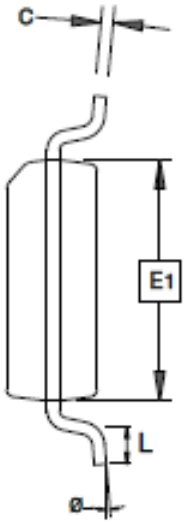
07/19/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8P3, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	PTC	8P3	C

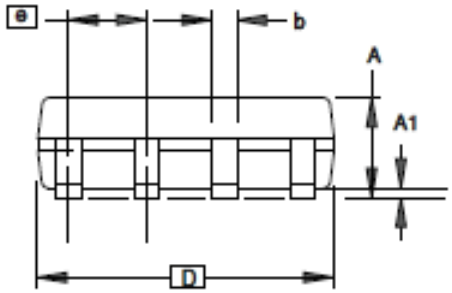
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

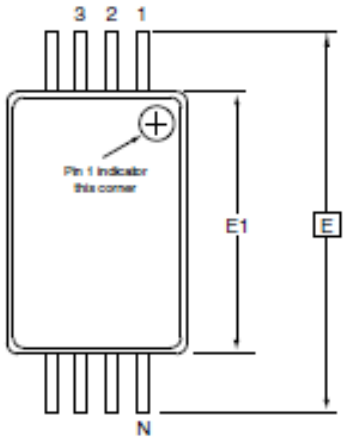
COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

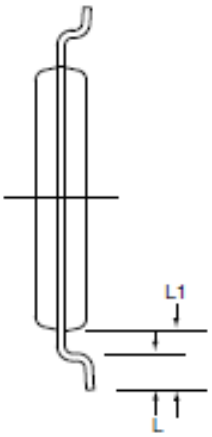
5/19/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	SWB	8S1	F

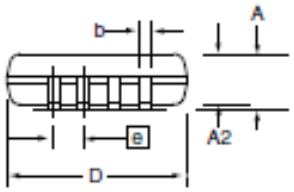
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

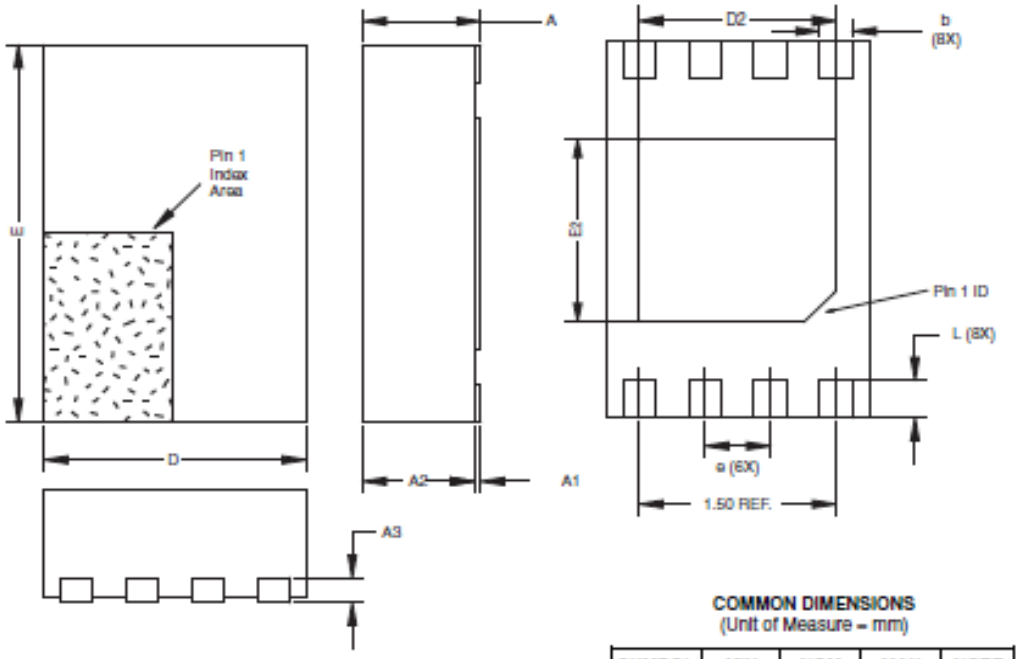
SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/19/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8A2, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8A2	E

8Y6 - UDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

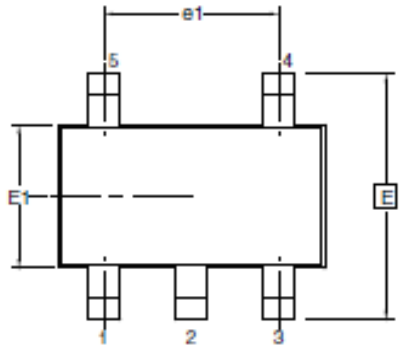
SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	–	–	1.40	
A	–	–	0.60	
A1	0.00	0.02	0.05	
A2	–	–	0.55	
A3		0.20 REF		
L	0.20	0.30	0.40	
e		0.50 BSC		
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

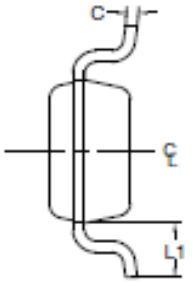
11/21/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8Y6, 8-lead, 2.0x3.0mm Body, 0.50mm Pitch, UltraThin Mini-MAP, Dual No Lead Package (Sawn)(UDFN)	YNZ	8Y6	E

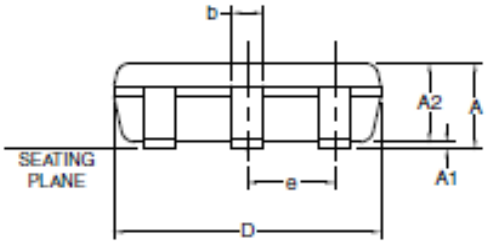
5TS1 – SOT23



Top View



End View



Side View

Notes:
1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.15mm per end. Dimensions E1 does not include interlead flash or protrusion. Interlead flasg or protrusion shall not exceed 0.15mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.80mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07mm.
5. This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

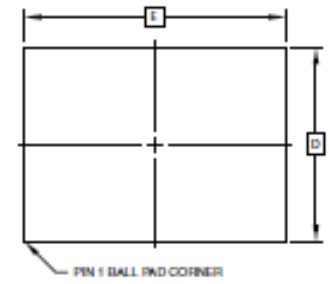
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.10	
A1	0.00	–	0.10	
A2	0.70	0.90	1.00	
c	0.08	–	0.20	3
D		2.90 BSC		1, 2
E		2.80 BSC		1, 2
E1		1.60 BSC		1, 2
L1		0.60 REF		
e		0.95 BSC		
e1		1.90 BSC		
b	0.30	–	0.50	3, 4

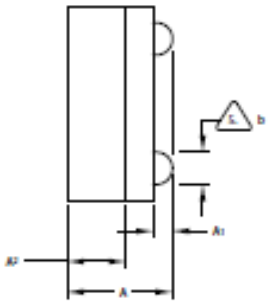
11/05/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	5TS1, 5-lead, 1.60mm Body, Plastic Thin Shrink Small Outline Package (Shrink SOT)	TSZ	5TS1	B

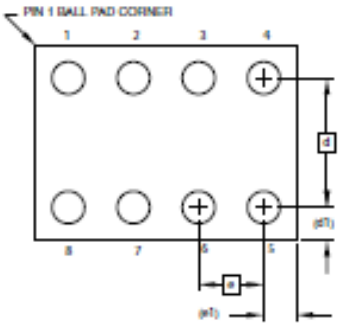
8U3-1 – VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW
8 SOLDER BALLS

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D		1.50 BSC		
E		2.0 BSC		
e		0.50 BSC		
e1		0.25 REF		
d		1.00 BSC		
d1		0.25 REF		

Notes:
1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

07/14/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8U3-1, 8-ball, 1.50 x 2.00mm Body, 0.50 pitch, VFBGA Package (dBGA2)	GXU	8U3-1	D

13. Revision History

Doc. Rev.	Date	Comments
8700D	08/2010	Changed AT24C02C-XHM Part Marking from C02CM@ to 02CM @
8700C	07/2010	Ordering Information: - Changed Atmel AT24C02C-TSUM-T to Atmel AT24C02C-STUM-T - Changed Atmel AT24C02CY6-MAHM-T to Atmel AT24C02C-MAHM-T - Changed Atmel AT24C02CU3-CUM-T to Atmel AT24C02C-CUM-T Catalog Numbering Scheme, changed TS = SOT23 to ST = SOT23 Part Marking SOT23: - Changed 2CMWU to 2CMBU - Changed W = Write Protection Feature to B = Write Protection Part Marking PDIP and SOIC: Added @ = Country of Assembly Part Marking TSSOP: Replaced and removed bottom mark Part Marking UDFN: Added HM@ Remove Preliminary Status Changed t_i Max 40 to 50 in Table AC Characteristics
8700B	02/2010	Corrected Catalog Numbering Scheme and Ordering Information
8700A	12/2009	Initial Document Release

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www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

8700D–SEEPR–8/10

LCD

HITACHI

LM016L·LM016XMBL

- 16 character x 2 lines
- Controller LSI HD44780 is built-in (See page 79).
- +5V single power supply
- Display color: LM016L : Gray
  LM016XMBL : New-gray

MECHANICAL DATA (Nominal dimensions)

Module size	84W x 44H x 10.5T (max.) mm
Effective display area	61W x 15.8H mm
Character size (5 x 7 dots)	2.96W x 4.86H mm
Character pitch	3.55 mm
Dot size	0.56W x 0.66H mm
Weight	about 35 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	6.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temeprature (Ta)	0	50 40*°C
Storage temperature (Tstg)	−20	70 60*°C

* Shows the value of type LM016XMBL.

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (V_{IH})	2.2 V min.
Input "low" voltage (V_{IL})	0.6 Vmax.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 Vmax.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 3.0 mA max.

POWER SUPPLY FOR LCD DRIVE (Recommended) (V_{DD}-V_O)

Duty = 1/16

Range of $V_{DD}-V_O$	1.5~5.25 V
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA ..... See page 7

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	–	0V — Power supply
2	V_{DD}	–	+5V — Power supply
3	V_O	–	– — Power supply
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

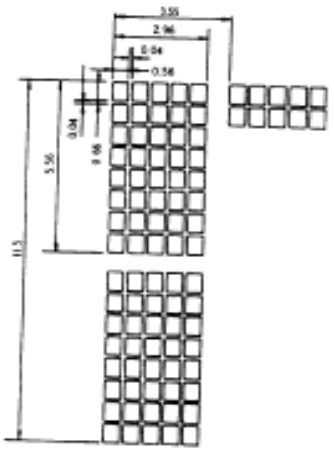


Fig. 1 Display pattern

Unit: mm

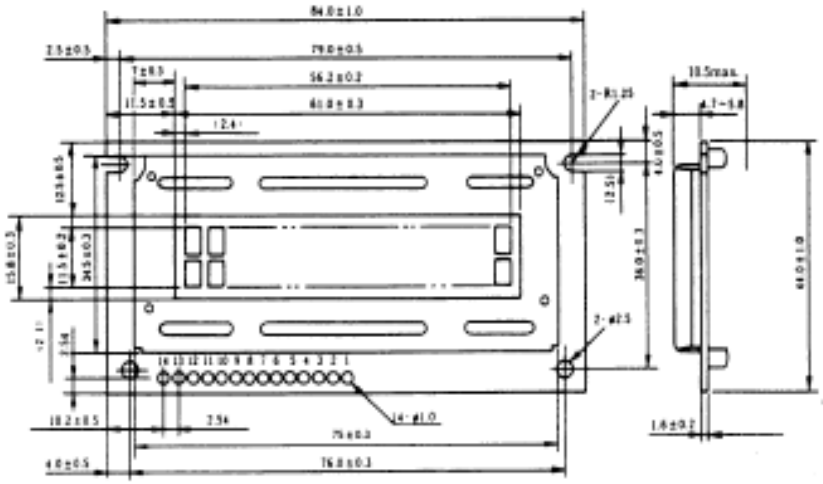


Fig. 2 External dimensions

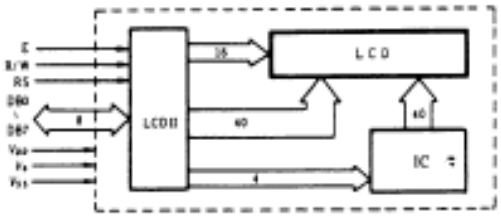


Fig. 3 Block diagram

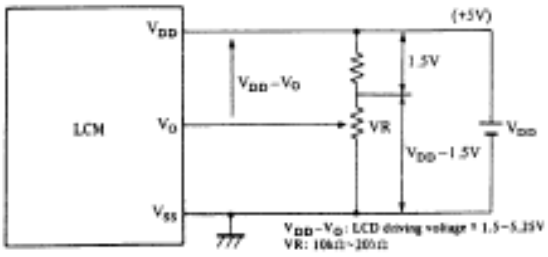


Fig. 4 Power supply

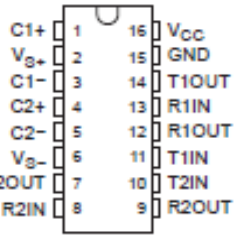
MAX 232

MAX232, MAX232I
DUAL EIA-232 DRIVERS/RECEIVERS

SLLS047L – FEBRUARY 1989 – REVISED MARCH 2004

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0-μF Charge-Pump Capacitors
- Operates Up To 120 kbit/s
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15-kV HBM) and 0.1-μF Charge-Pump Capacitors is Available With the MAX202
- Applications
  - TIA/EIA-232-F, Battery-Powered Systems, Terminals, Modems, and Computers

MAX232 . . . D, DW, N, OR NS PACKAGE
MAX232I . . . D, DW, OR N PACKAGE
(TOP VIEW)



description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	MAX232N	MAX232N
	SOIC (D)	Tube of 40	MAX232D	MAX232
		Reel of 2500	MAX232DR	
	SOIC (DW)	Tube of 40	MAX232DW	MAX232
		Reel of 2000	MAX232DWR	
	SOP (NS)	Reel of 2000	MAX232NSR	MAX232
−40°C to 85°C	PDIP (N)	Tube of 25	MAX232IN	MAX232IN
	SOIC (D)	Tube of 40	MAX232ID	MAX232I
		Reel of 2500	MAX232IDR	
	SOIC (DW)	Tube of 40	MAX232IDW	MAX232I
		Reel of 2000	MAX232IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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Function Tables

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	H
H	L

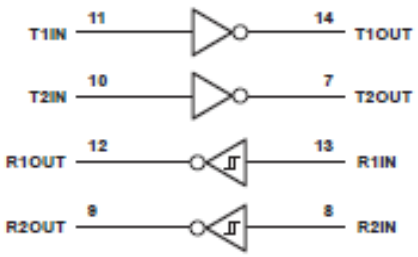
H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	H
H	L

H = high level, L = low level

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 6 V
Positive output supply voltage range, V_{S+} ..... V_{CC} − 0.3 V to 15 V
Negative output supply voltage range, V_{S-} ..... −0.3 V to −15 V
Input voltage range, V_I: Driver ..... −0.3 V to V_{CC} + 0.3 V
Receiver ..... ±30 V
Output voltage range, V_O: T1OUT, T2OUT ..... V_{S-} − 0.3 V to V_{S+} + 0.3 V
R1OUT, R2OUT ..... −0.3 V to V_{CC} + 0.3 V
Short-circuit duration: T1OUT, T2OUT ..... Unlimited
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package ..... 73°C/W
DW package ..... 57°C/W
N package ..... 67°C/W
NS package ..... 64°C/W
Operating virtual junction temperature, T_J ..... 150°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (T1IN,T2IN)		2			V
V_{IL}	Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage				±30	V
T_A	Operating free-air temperature	MAX232	0		70	°C
		MAX232I	−40		85	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5 V, All outputs open, T_A = 25°C		8	10	mA

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND		5	7		V
V_{OL}	Low-level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND			−7	−5	V
r_o	Output resistance	T1OUT, T2OUT	V_{S+} = V_{S-} = 0,	V_O = ±2 V	300			Ω
I_{OS}§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0				200	µA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 2			30	V/µs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/µs
	Data rate	One TOUT switching		120		kbit/s

NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	I_{OH} = −1 mA		3.5			V
V_{OL}	Low-level output voltage‡	R1OUT, R2OUT	I_{OL} = 3.2 mA				0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V		0.2	0.5	1	V
r_i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5,	T_A = 25°C	3	5	7	kΩ

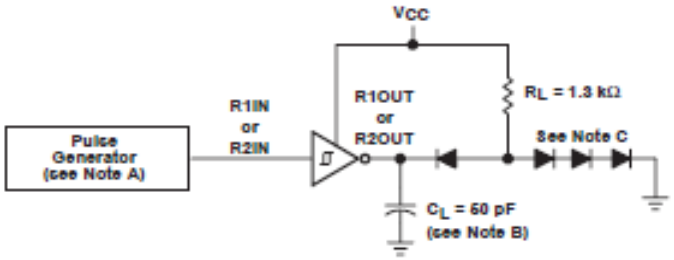
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4 and Figure 1)

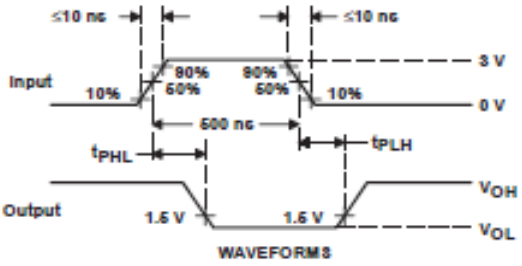
PARAMETER		TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	500	ns

NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

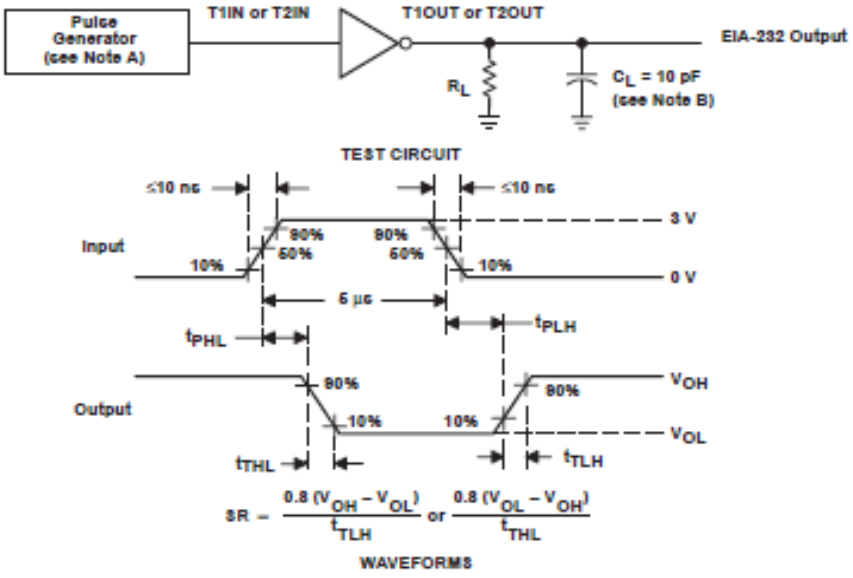


WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

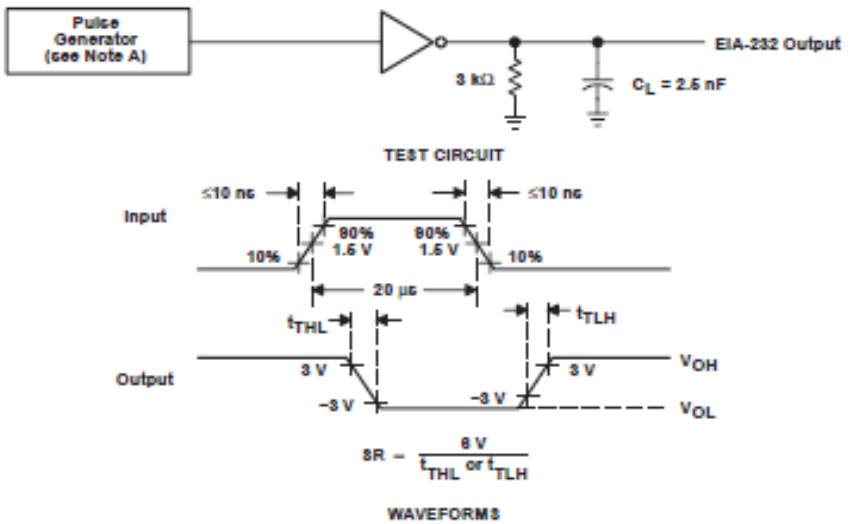
Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

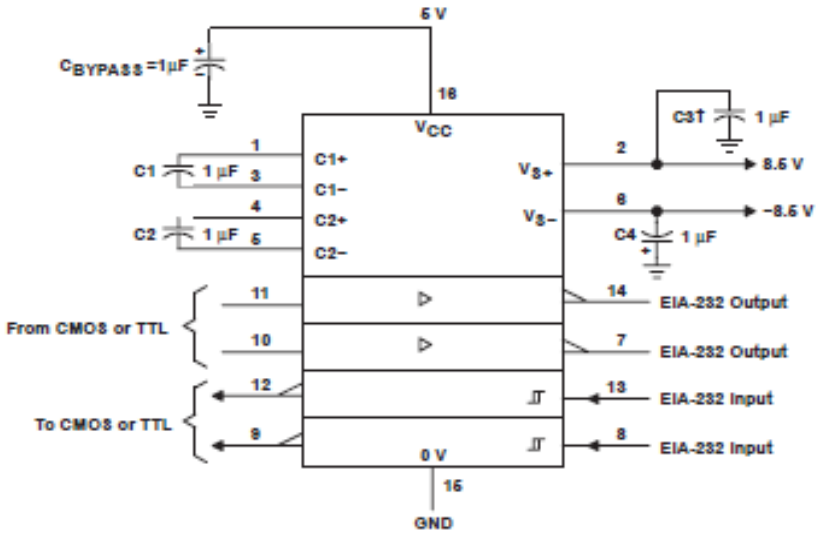
Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-µs Input)



NOTE A: The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.
B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-µF capacitors shown, the MAX202 can operate with 0.1-µF capacitors.

Figure 4. Typical Operating Circuit

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PACKAGE OPTION ADDENDUM

18-Jul-2006

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MAX232D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:

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PACKAGE OPTION ADDENDUM

18-Jul-2006

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. – The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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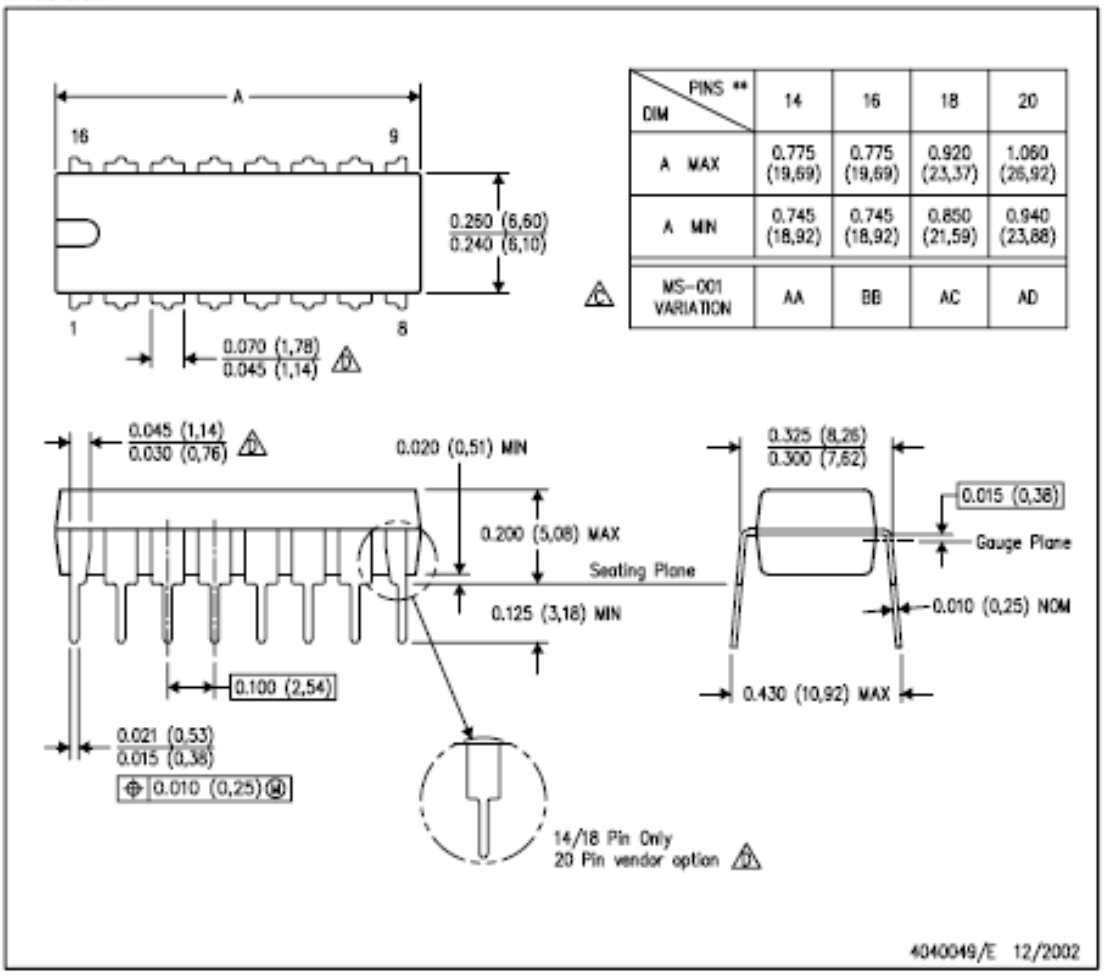
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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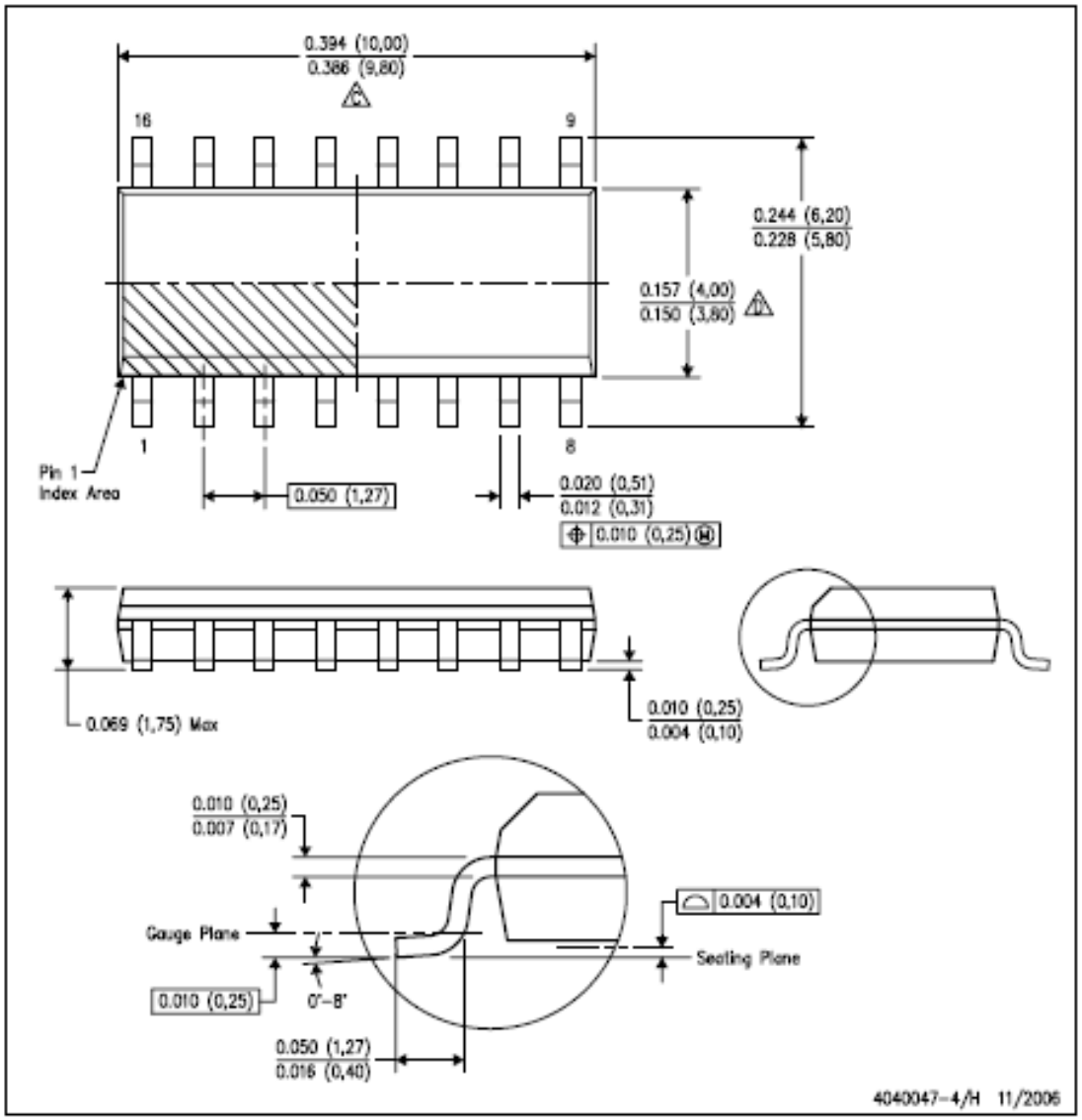
MECHANICAL DATA

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

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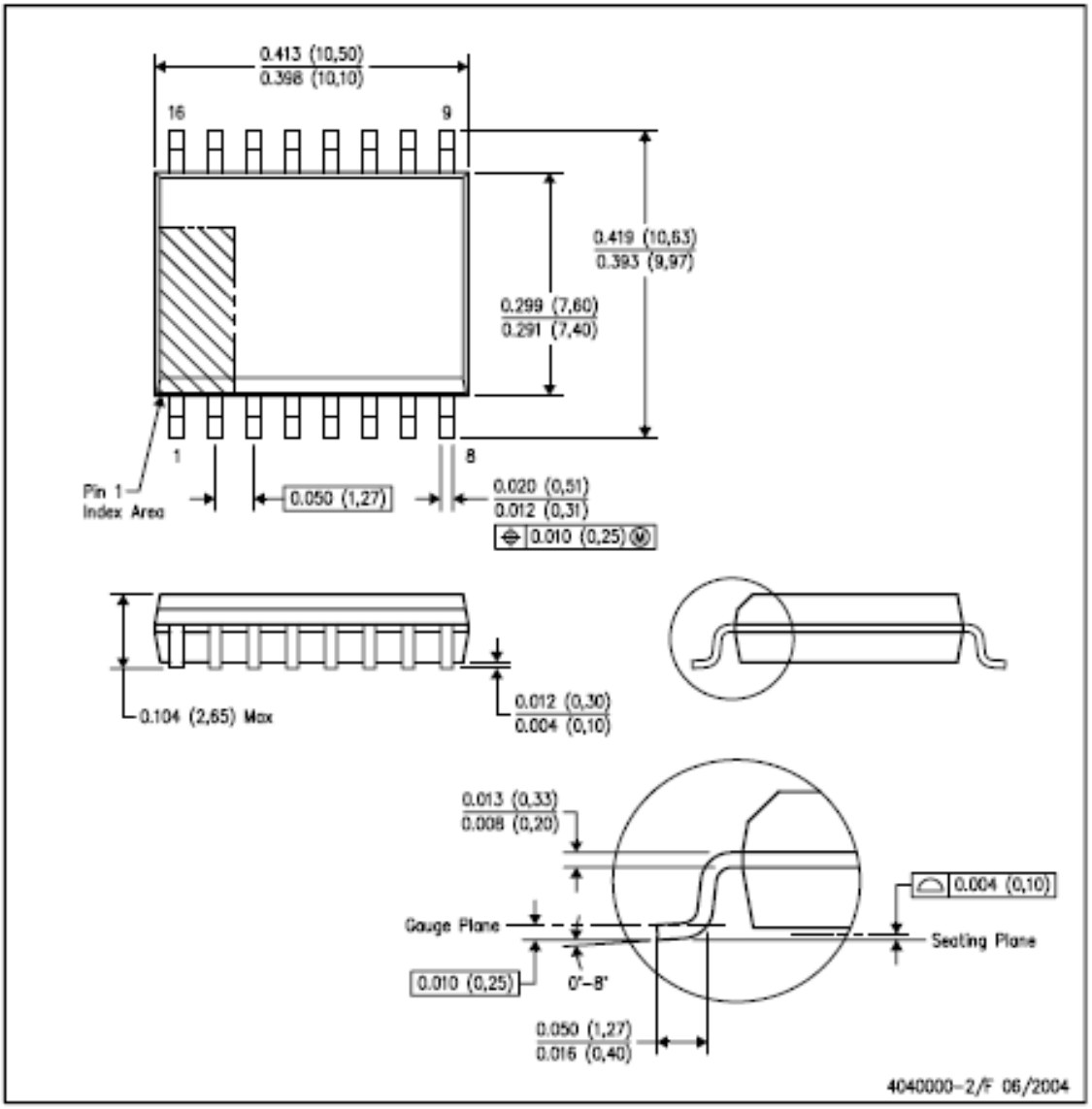
MECHANICAL DATA

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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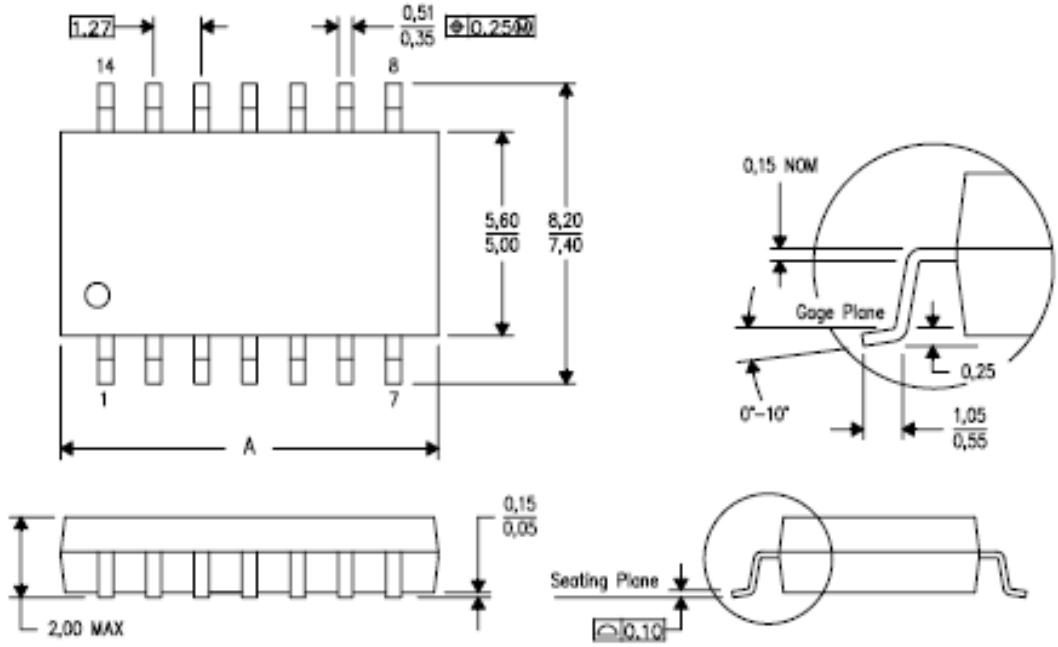
MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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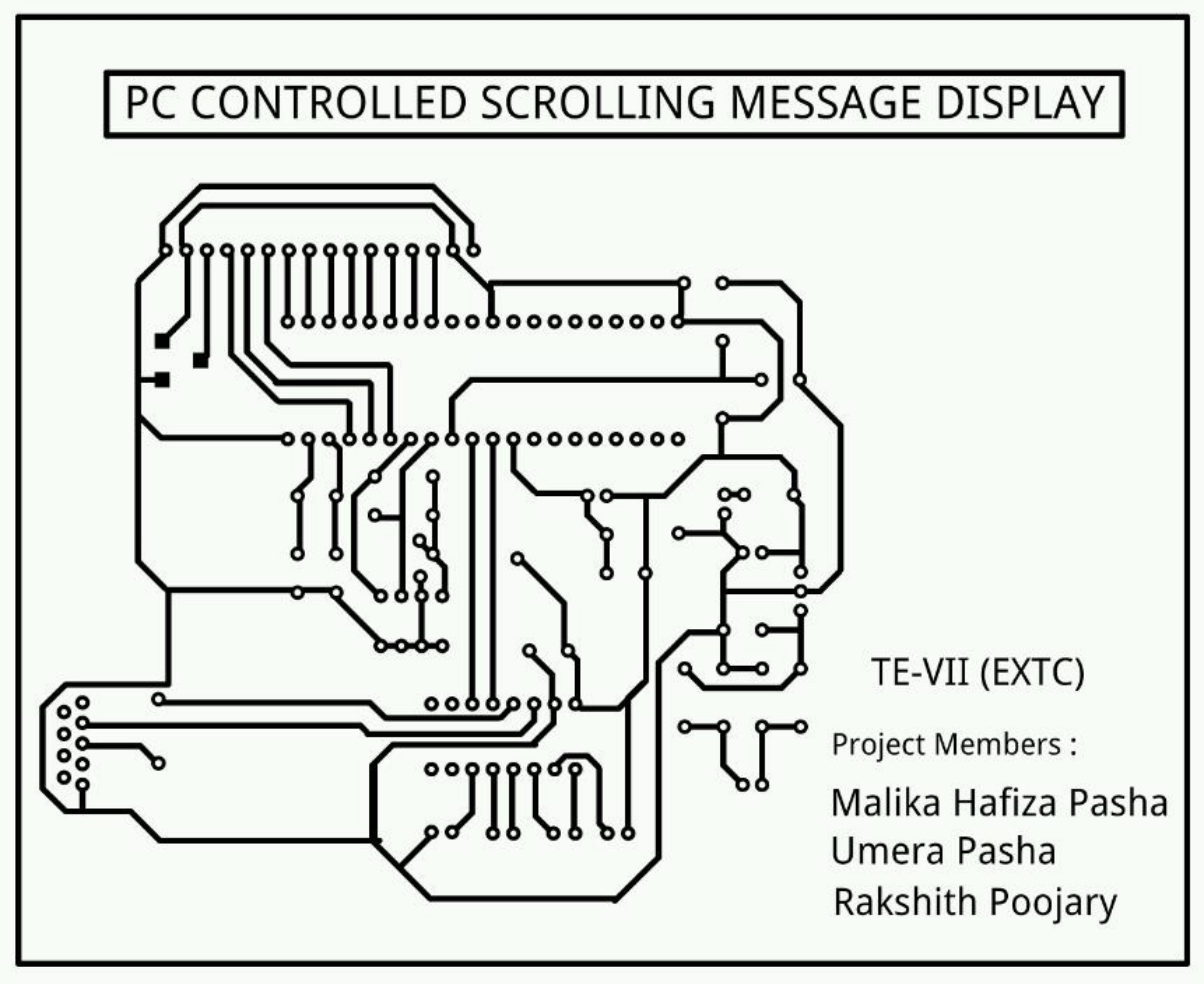
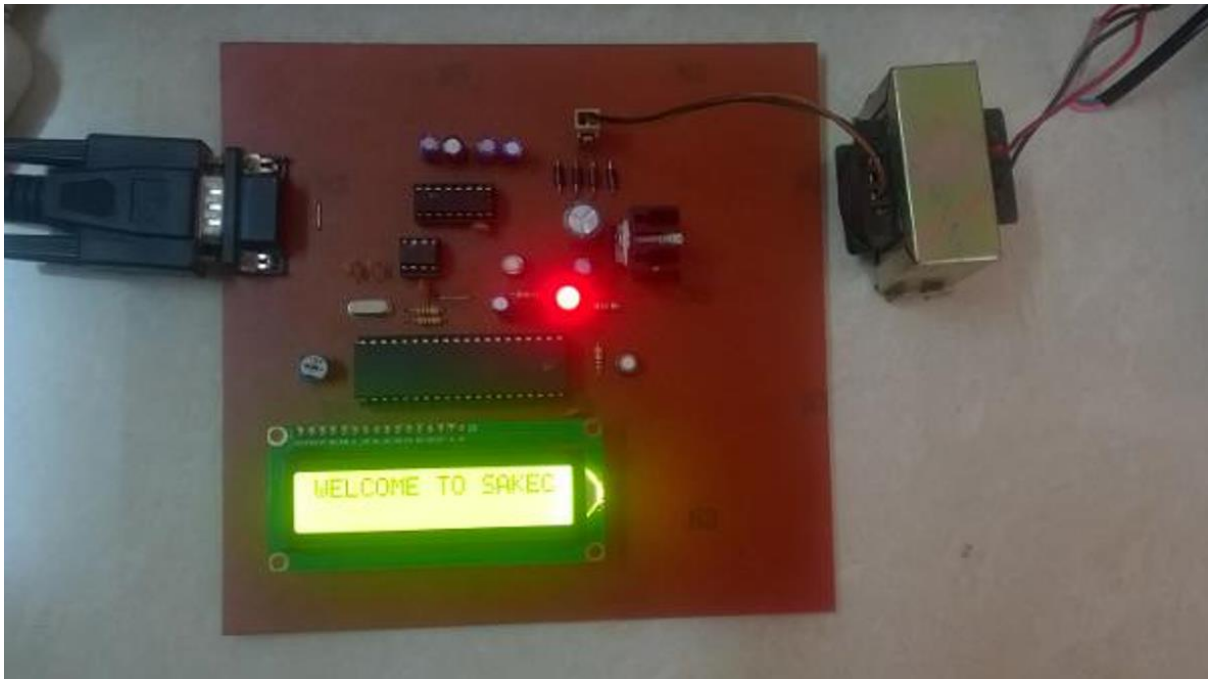
PCB LAYOUT:


PC CONTROLLED SCROLLING MESSAGE DISPLAY
TE-VII (EXTC)
Project Members :
Malika Hafiza Pasha
Umera Pasha
Rakshith Poojary

FINAL OUTPUT:



CONCLUSION:

This project made us familiar with the vast application of PC controlled scrolling message display. We have applied our theoretical knowledge and have simultaneously gained practical experience, thus satisfying the basic objective of the "Project".

With this project we have realized the importance of planning and organization of work involved. Assigning different members of our Project Team and yet ensuring co-ordination amongst all has enabled us to complete the project in time.

We have been very fortunate to get the appropriate guidance as and when required from our Project Guide and we once again thank them for the same.