Taylor & Francis
Taylor & Francis Group

Journal of Information and Optimization Sciences

ISSN: 0252-2667 (Print) 2169-0103 (Online) Journal homepage: https://www.tandfonline.com/loi/tios20

A design of low leakage cache memory cell for high performance processors

Monica Gupta, Kirti Gupta & Neeta Pandey

To cite this article: Monica Gupta, Kirti Gupta & Neeta Pandey (2019) A design of low leakage cache memory cell for high performance processors, Journal of Information and Optimization Sciences, 40:2, 279-290, DOI: 10.1080/02522667.2019.1578089

To link to this article: https://doi.org/10.1080/02522667.2019.1578089

Published online: 08 Mar 2019.

Journal of Information & Optimization Sciences
ISSN 0252-2667 (Print), ISSN 2169-0103 (Online)
Vol. 40 (2019), No. 2, pp. 279–290
DOI : 10.1080/02522667.2019.1578089

Taylor & Francis
Taylor & Francis Group

A design of low leakage cache memory cell for high performance processors

Monica Gupta *
Kirti Gupta †
Bharati Vidyapeeth's College of Engineering
Paschim Vihar
New Delhi 110063
India

Neeta Pandey §
Delhi Technological University
Shahbad Daulatpur
New Delhi 110042
India

Abstract

The noises, when augmented with leakage, destabilize the data stored in cache (SRAM). So, a novel 7T cache memory cell with reduced leakages and improved read and write performance is proposed to address the mentioned issue. The proposed cell with its unique read assist circuit provides SNM-free read operation. It also provides improved write ability by performing a differential write operation. The performance of the proposed cell is compared with the Standard-6T and Dual-V_T 7T (DVT-7T) cells at 32nm technology node in the subthreshold region by SPICE simulations. The proposed structure shows significant improvement over other cells in terms of Read Static Noise Margin (RSNM), Write Static Noise Margin (WSNM), Data Retention Voltage (DRV), critical write time (T_{crit}), read current (I_{read}) and standby leakage current (I_{leak}) values. In addition it uses three MOS transistor based latch structure to reduce area overhead. The Proposed-7T structure improves RSNM, WSNM, Iread and Ileak over Standard-6T cell. Similarly, performance improvement is observed in RSNM, WSNM, I_{read}, T_{crit}('0'), T_{crit}('1') and I_{leak} in comparison to the DVT-7T cell. A super cut-off CMOS scheme to reduce leakages further has been employed in the paper. A process corner analysis has been done to capture the effect of process variation on the performance of cells.

Keywords: *Differential write, SNM-free read, Subthreshold, Low leakage, 7T SRAM, Cache*

*E-mail: monica.gupta.me@gmail.com (Corresponding Author)
†E-mail: kirtigupta22@gmail.com
§E-mail: neetapandey@dce.ac.in

1. Introduction

A Cache memory (CPU memory) is a faster static random access memory (SRAM) which a processor accesses more often than the other memories for carrying out its complex computational work. But due to the growing need of high density cache to speed up the working mechanism of the processor, the device scaling on SRAM cell is done which increases the number of cells per unit chip area [1]. Due to the presence of large number of cells on a constrained chip area, the problem of excessive leakages and high power consumption has emerged as the main area of concern during standby mode. To curtail these problems, supply scaling on smaller devices is implemented but it again leads to degraded read and write performance in Standard-6T SRAM cell [2].

The read-write conflict issue and destructive read problem inherent in the architecture of Standard-6T SRAM cell has led to the design of various improvised dual-port structures with separate read and write port. One such structure is Dual-V_T 7T (DVT-7T) SRAM cell [3] with single ended read and write ports. A decoupled read port provides SNM-free (static noise margin - free) read operation but show degraded write and leakage performance in comparison to Standard-6T cell. Various leakage reduction techniques [4] [5] [6] have been proposed in the literature to combat the leakage specific problems to a certain extent above and near subthreshold region. But the improvement achieved through such techniques is limited so the other improved topologies are proposed. The dual-port 7T SRAM structure proposed in [7] uses an inherently slow single ended write operation. Also the presence of grounded transistor in latch structure increases the leakages in the standby mode. Therefore, a new more effective structure with improved performance is proposed in the paper.

This paper is organized as follows. The Section II discusses some existing cell topologies while Section III presents the architecture of the Proposed-7T SRAM cell and describes its operation. The performance of the new cell is discussed in Section IV and Section V summarizes this paper.

2. Existing cell topologies

An SRAM array is made up of several cells arranged over multiple rows and columns to store binary information. Each cell can store one bit of binary information. There are numerous circuit realizations for the

SRAM cell. The cells are classified according to the number of transistors used in their implementation. Some of the circuits are discussed below.

2.1 *Standard-6T cell*

A conventional six transistor SRAM cell is shown in Fig. 1(a). The two pull-down and two pull-up transistors (PUL-PDL, PUR-PDR) are used to form the latch while the other two transistors (ACL, ACR) are used to access the internal nodes (Q, QB) during read and write operation.

Due to the direct access of internal nodes (Q, QB) during read operation the cell becomes vulnerable to external noise. This leads to degraded read static noise margins (RSNM) which increases the tendency of cell towards destructive read operation. Similarly, to enhance the current conducting ability during write operation, the access transistors (ACL, ACR) must be made more powerful than the pull-up transistors (PUL, PUR). This is not a concern for cell operating at high voltages but in the region below threshold voltage, the effect of process variations becomes much more important specifically at worst Slow-Fast (SF) corner. At this corner the pull-up PMOS transistors have higher current conducting ability than the access NMOS transistors leading to the complete malfunction during write operation.

2.2 *Dual-V_T 7T cell(DVT-7T) [3]*

To address the issues associated with Standard-6T cell, an improvised Dual-V_T 7T (DVT-7T) SRAM cell was proposed in [3] as shown in Fig. 1(b) where V_T is the threshold voltage of the MOS transistor. It consists of the basic two cross-coupled inverters (PUR-PDR, PUL-PDL) to store one bit of information. The dual threshold voltage (DVT) transistors are used to form the latch. A MOS transistor with high -V_T (HVT) has low leakage current and also reduces the power consumption during write operation in subthreshold region. The cell provides single ended read through a decoupled read circuit consisting of transistors, M1 and M2. The advantage of such an arrangement is that the latch and the read circuit can be sized independent of each other, removing the read-write conflict issue. Also it provides separate path for read current to flow resolving the destructive read problem. The cell provides single ended write operation via NMOS access transistor, ACL.

There are various drawbacks associated with this cell. The read assist circuit uses a stack of two NMOS transistors [4] which degrades the read current during read operation. This in turn leads to the degraded Ion/

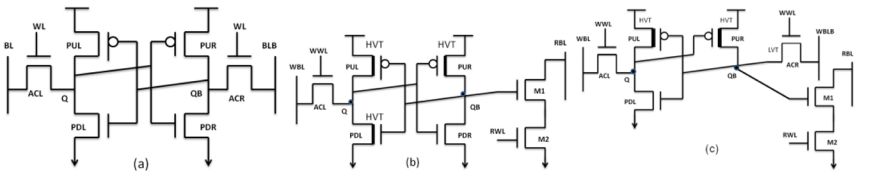

Figure 1

Schematic of (a) Standard-6T cell (b) DVT-7T[3] cell (c) Proposed-7T cell

Ioff ratio of the SRAM cell. Thus reducing the number of cells that can be connected to the pair of bitlines and increasing the number of peripherals required to implement an SRAM array. Similarly it has deteriorated write ability due to the presence of high-V_T transistors on the write critical path. It provides single ended write which is slow and degrades the write ability of the cell further. The implementation of Dual-V_T technique on a cell requires placement of smaller devices in close proximity to each other which is both difficult and expensive. So, it becomes essential to propose a new design for SRAM cell which can offer improved read stability, write ability and reduced leakages. A novel design to deal with these issues is presented next.

3. Proposed-7T cell

The constraints on the performance of the 6T cell at low voltages are overcome by the Proposed-7T cell. The structure of Proposed-7T SRAM cell is shown in Fig. 1(c). It consists of the novel three transistor based latch structure formed by transistors (PUR, PUL, and PDL) for bit storage. It uses read bitline (RBL), read assist circuit (M1, M2) and read word line (RWL) for performing single ended read operation. The control signal, write word line (WWL) along with the write bitlines (WBL-WBLB) are used for performing a faster differential write operation. The WBLB is kept low at all times (read and hold mode) except when writing '1' at node QB. To reduce the impact of leakages on the cell voltages, the PUL and PUR transistors are HVT (high $-V_T$) implemented. Also to provide robust hold '1' state ACR is LVT (low-V_T) implemented.

3.1 *Read mode*

The read word line (RWL) acts as a switch to connect read bitline (RBL) to the cell ground in the read mode. When QB is '1' (Q='0') then the transistor M1 turns ON and conducts heavy read current through

M1 and M2 due to improved W/L ratio of the read circuit. So, RBL discharges quickly through M2. This drop in voltage of RBL is sensed by sense amplifier. Similarly, if QB is '0' (Q='1') then the transistor M1 stays OFF and there is no change in the voltage of RBL. Due to the presence of separate discharge path for the read current (through M1 and M2) the RSNM is equal to the HSNM.

3.2 *Write mode*

This cell employs faster differential write operation using two complementary write bitlines (WBL, WBLB) and a write word line (WWL). The bitlines are driven in opposite direction to ease the writing process. For a write '1' operation, with WWL = '1', ACL turns ON and due to very high V_{DS} quickly charges the node Q towards logic high. Simultaneously, node QB discharges quickly through ON access transistor ACR towards ground. The proposed cell provides improved write ability at low power consumption (till 400mV) with no much area overhead.

3.3 *Hold mode*

In this state WWL and RWL go low to isolate the internal nodes from noises through external bitlines. Since only the leakages can change the voltages at the internal nodes in this mode therefore the immunity of cell against noise is maximum in this state [4][5]. In Proposed-7T structure the transistors which generate the leakage current are either sized minimum or are HVT implemented. To reduce the leakages further, a leakage reduction technique namely Super cut-off CMOS scheme [6] has been implemented on the proposed cell. In this technique, the voltage at the gate of the OFF MOS transistors that is ACL and ACR are increased negatively (no precise control needed) till there is no problem due to gate-oxide reliability or until gate tunneling current (GIDL) remains negligible.

4. Simulation results and discussions

The Standard-6T, DVT-7T [3] and Proposed-7T cells are implemented at 32nm technology node in the subthreshold region. The comparison among the cells have been done on the basis of read static noise margin (RSNM), read current (I_{read}), critical write time (T_{crit}), write static noise margin (WSNM), hold static noise margin (HSNM), data retention voltage (DRV) and standby leakage current (I_{leak}). All the SPICE simulations are carried out at a supply voltage (V_{DD}) of 0.4 V and temperature (T) of 27°C.

Table 1

SRAM cell transistors dimension

SRAM Cell	MOS Transistors with W/L ratio ($\lambda = 0.018\mu m$)
Standard-6T	PUL,PUR : **3λ/2λ** ; PDL,PDR : **8λ/2λ** ; ACL,ACR : **4λ/2λ**
DVT-7T [3]	PUL,PUR,M1,M2 : **3λ/2λ** ; ACL : **4λ/2λ** ; PDL,PDR : **8λ/2λ**
Proposed-7T	PUL,PUR : **3λ/2λ** ; M1,M2 : **4λ/2λ** ; ACL : **6λ/2λ** ; PDL,ACR : **8λ/2λ**

The dimensions, i.e., width to length ratio (W/L) of all the transistors are specified in the Table 1 in lambda (λ) as per lambda rule of layout specification.

4.1 *Read mode*

The SRAM cells are implemented to operate in the read mode. To estimate the read static noise margin, a butterfly curve is plotted for each cell [8]. The read current is calculated with respect to the internal node and RBL.

4.1.1 Read Static Noise margin (RSNM) [8]

From the plots shown in Fig. 2, it can be observed that the proposed cell provides 63.4% and 12.5% higher RSNM compared to Standard-6T and DVT-7T cells respectively. This shows that during read operation the stored data remains *more* resistant to noise in the proposed cell compared to Standard-6T and DVT-7T cells.

4.1.2 Read Current (I_{read}) [7][9]

The variation of the read current with supply voltage and temperature is shown in Fig. 3. It can be noted that the proposed cell provides 8.9%

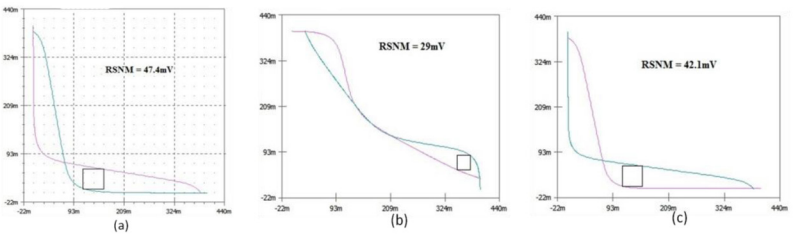

Figure 2

RSNM at V_{DD} = 0.4 V for (a) Proposed-7T cell (b) Standard-6T cell and (c) DVT-7T cell

and 151.3% higher read current than Standard-6T and DVT-7T cells in the subthreshold region. This validates that the RBL discharges faster in proposed cell as compared to the other two cells under similar operating conditions. The result also shows the sturdiness of the proposed cell against varying conditions like V_{DD} and T.

The Monte Carlo analysis with 500 MC runs is carried out to inspect the consequence of process variations on the read current of all the three SRAM cells. The results are shown in Fig. 4 and 5 for high supply voltage (strong inversion) and low supply voltage (weak inversion) respectively. The process variations are considered as threshold voltage variations which include random dopant fluctuations (RDF), transistor parameter deviations etc. As can be seen in Fig. 4 and 5, the process parameter variation degrades the read current of all the SRAM cells but the effect is

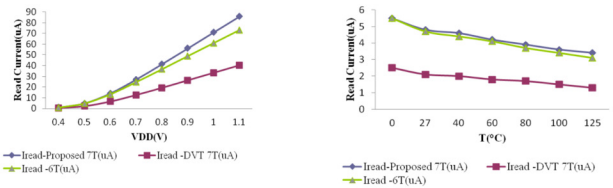

Figure 3

I_{read} of Proposed-7T, Standard-6T and DVT-7T cells under (a) V_{DD} (V) variations at 27°C and (b) T (°C) variations at V_{DD}=0.4V

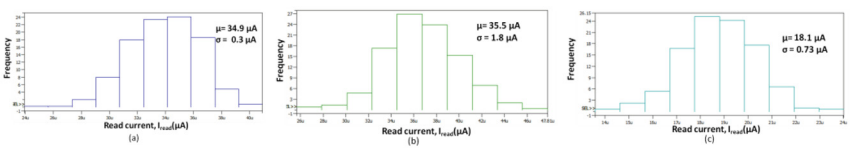

Figure 4

I_{read} distribution for (a) Proposed-7T cell, (b) Standard-6T cell and (c) DVT-7T cell due to process parameter variation at strong inversion (V_{DD} = 0.8 V).

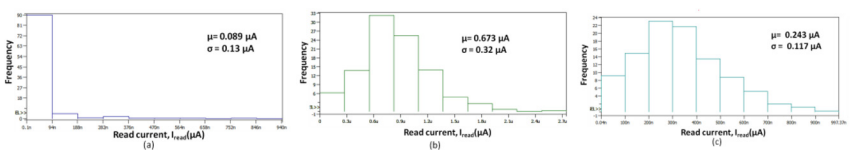

Figure 5

I_{read} distribution for (a) Proposed-7T cell, (b) Standard-6T cell and (c) DVT-7T cell due to process parameter variation at weak inversion (V_{DD} = 0.4 V).

more evident on Standard-6T and DVT-7T as only in few cases the read current goes below one standard deviation for Proposed-7T cell.

4.2 *Write mode*

All the SRAM cells are implemented to operate in the write mode. The use of high-V_T pull-up transistors results in the tremendous improvement in the noise immunity of the proposed cell in terms of WSNM [8]. The actual write ability of the cells in the dynamic environment is estimated using critical write time, T_{crit} [7].

4.2.1 Write Static Noise margin (WSNM) [8]

The WSNM is evaluated using butterfly curve as shown in Fig. 6. It is apparent from the graph that the proposed cell improves the WSNM by 21% and 16.4% in comparison to Standard-6T and DVT-7T near subthreshold region. The result confirms the robust performance of proposed cell during write operation.

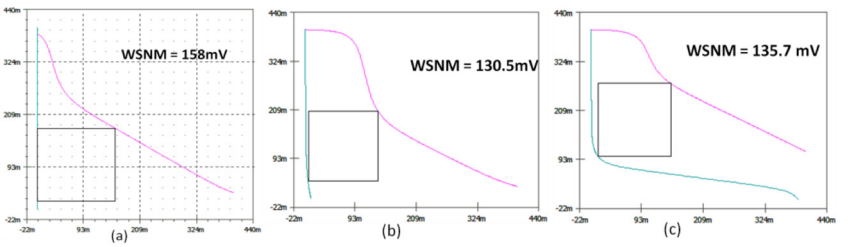

Figure 6

WSNM at V_{DD} = 0.4 V for (a) Proposed-7T cell (b) Standard-6T cell and (c) DVT-7T cell

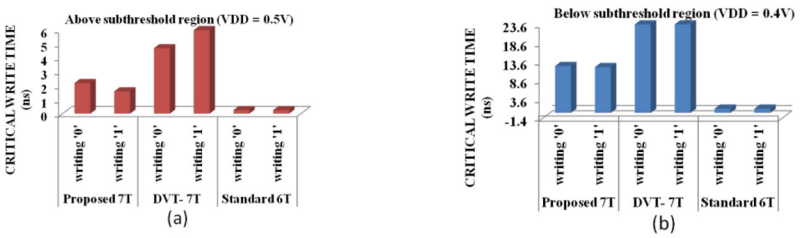

Figure 7

T_{crit} '0' and '1' for all cells (a) V_{DD} = 0.5 V (above subthreshold region) (b) V_{DD} = 0.4 V (below subthreshold region) at T=27 °C.

4.2.2 Critical write time (T_{crit}) [7]

The T_{crit} which is defined as the minimum width of the pulse that needs to be applied at the WL terminal for the write operation to be successful is shown in Fig. 7 and 8. The write '0' and write '1' cases are considered separately in Fig. 7. The proposed cell shows 71.6% and 48.3% improvement in write '0' time and write '1' time over DVT-7T cell at V_{DD} = 0.4V while it shows 53.2% and 73.3% improvement in the same at V_{DD} = 0.5V. When compared to Standard-6T cell it shows a slight increase in both write '1' and write '0' time . It is due to the nonexistence of pull down NMOS transistor below node QB and use of high-V_T pull-up transistors in latch structure.

Fig. 8 shows that for the proposed cell, the time required for the write operation to finish is highest at the TT corner and lowest at the FF corner for both near and below subthreshold region. It is worth mentioning that the proposed cell provides substantially improved performance at all corners even at the most problematic SF corner compared to TT corner. The write '0' time is higher than write '1' time under both operating conditions because of the presence of LVT implemented access transistor ACR which quickly discharges node QB towards '0' during write '1' operation at node Q.

It is apparent from the graphs that write '1' operation at FS corner takes much lesser time than at TT corner. This is because at FS corner the conductivity of NMOS transistor is more than that of PMOS transistor. The pull-up transistor PUL is OFF during this cycle and ACL conducts heavy current to write '1' at node Q.

4.3 *Hold mode*

All the three SRAM cells are implemented to operate in the HOLD mode. Three important parameters, namely HSNM [8], DRV [9] and I_{leak} [9] are estimated to ensure the stability of data in the cell. The performance of Proposed-7T, Standard-6T and DVT-7T [3] are compared on the basis of the specified parameters.

4.3.1 Hold Static Noise margin (HSNM) [8]

HSNM is an estimate of the immunity of the cell against static noise in hold mode.

The improved value of HSNM for proposed cell translates into a more stable data when stored in this cell compared to DVT-7T cell. Fig. 9 shows 12.5% higher HSNM compared to DVT-7T cell in subthreshold region. The sturdiness of data in hold mode for Proposed-7T cell is lesser than that of Standard-6T cell.

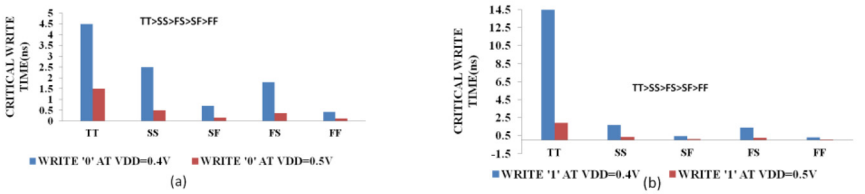

Figure 8

Corner analysis on T_{crit} for Proposed-7T at VDD = 0.5 V (near subthreshold region) and V_{DD} = 0.4 V(subthreshold region) (a) Write '0' time and (b) Write '1' time.

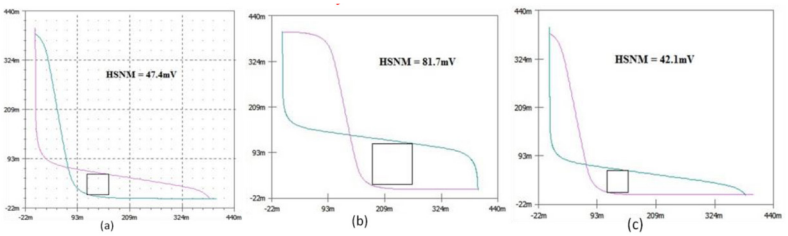

Figure 9

HSNM at V_{DD} = 0.4 V for (a) Proposed-7T cell (b) Standard-6T cell and (c) DVT-7T cell

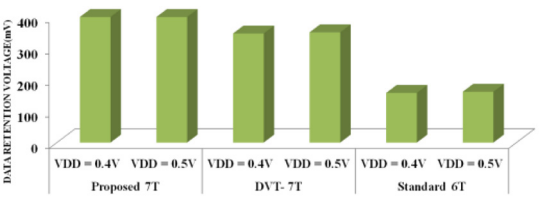

Figure 10

DRV at V_{DD} = 0.4 V and 0.5 V for Proposed-7T, Standard-6T and DVT-7T cells

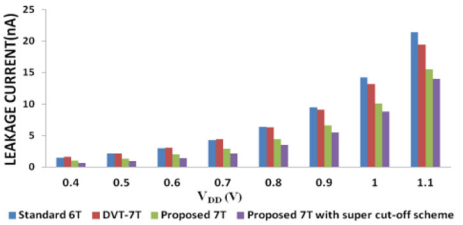

Figure 11

I_{leak} for Proposed-7T(with and without Super cut-off scheme), Standard-6T and DVT-7T cells

4.3.2 Data Retention Voltage (DRV) [9]

DRV is the least supply voltage required by the SRAM cell to retain the stored data. This parameter is used to reduce the static power dissipation of the cell. The DRV of cell shows slightly high value compared to DVT-7T cell at V_{DD} = 0.4 V and 0.5V while the value is quite high compared to Standard-6T cell as shown in Fig. 10.

4.3.3 Standby leakage current (I_{leak}) [9]

The variation of the leakage current with supply voltage is shown in Fig. 11. The cell shows 32% and 37.5% reduction in leakages when compared to Standard-6T cell and DVT-7T cell respectively in the subthreshold region (V_{DD}=0.4V). To further reduce the leakage current in the subthreshold region, a new approach namely Super cut-off scheme [6] has been applied. It overdrives the access transistor in standby mode by applying -80 mV at control signal terminal, WWL. A reduction of 54% and 57.8% can be seen from the graph as compared to Standard-6T cell and DVT-7T cells respectively at VDD = 0.4 V.

5. Conclusion

In this paper, a novel 7T SRAM cell with enhanced read and write performance in subthreshold region is presented. The cell has separate read and write ports to solve read-write conflict issue. It shows significant improvement in noise immunity of the cell in terms of static noise margins. A unique read assist circuit leads higher read current to improve read performance. The use of three MOS transistors in latch realization of SRAM is suggested to reduce area overhead and provide robust hold-'0' state in the proposed cell. The Proposed-7T cell shows tremendous improvement in RSNM, WSNM, I_{read} , T_{crit} and leakages. The leakages are further reduced by employing the Super cut-off scheme on the Proposed-7T cell. All the SPICE simulations are performed at 32 nm CMOS technology node.

References

[1] Gonzalez, R., Gordon, B. , Horowitz, M.: Supply and threshold voltage scaling for low power CMOS. IEEE J. Solid-State Circuits, Vol. 32, 1210–1216(1997).

[2] Olivera, F., Petraglia, A.: Analytic boundaries for 6T-SRAM design in standby mode. 29th Symposium on Integrated Circuits and Systems Design (SBCCI), 1-6(2016).

[3] Tawfik, S., A., Kursun, V.: Low power and robust 7T dual-Vt SRAM circuit. Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 1452–1455(2008).

[4] Narendra, S., Borkar, S., De, V., Antoniadis, D., Chandrakasan, A. : Scaling of stack effect and its application for leakage reduction. Int. Symp. Low Power Electronic and Design, 195-200(2001).

[5] Zhang, L., Chen, W., Ma, Y., Zheng, J., Mao, L.: Leakage power reduction techniques of 55nm SRAM cells. IETE technical review, 135-144(2015).

[6] Kawaguchi, H., Nose, K., Sakurai, T.: A super cut-off CMOS (SCCMOS) scheme for 0.5 V supply voltage with picoampere stand-by current. IEEE J. Solid-State Circuits, 1498–1501(2000).

[7] Gupta, S., Gupta, K., Pandey, N.: A 32-nm Subthreshold 7T SRAM Bit Cell With Read Assist. IEEE T. Very Large Scale Integration (VLSI) Systems, 3473-3483(2017).

[8] Wang, J., Nalam, S., Calhoun, B., H.: Analyzing static and dynamic write margin for nanometer SRAMs. Proc. 13th Int. Symp. Low Power Electron. Design (ISLPED), 129-134(2008).

[9] Edri, N., Fraiman, S., Teman, A., Fish, A.: Data retention voltage detection for minimizing the standby power of SRAM arrays. Proc. IEEE 27th Conv. Elect. Electron. Eng. Israel (IEEEI), 1-5(2012).