Name: Umesh

Roll Number : 2018UEC2030

ECE – 1 (2018-2022)

Subject Code: ECC20

Subject: VLSI

6th Semester

Index

NAME : UMESH

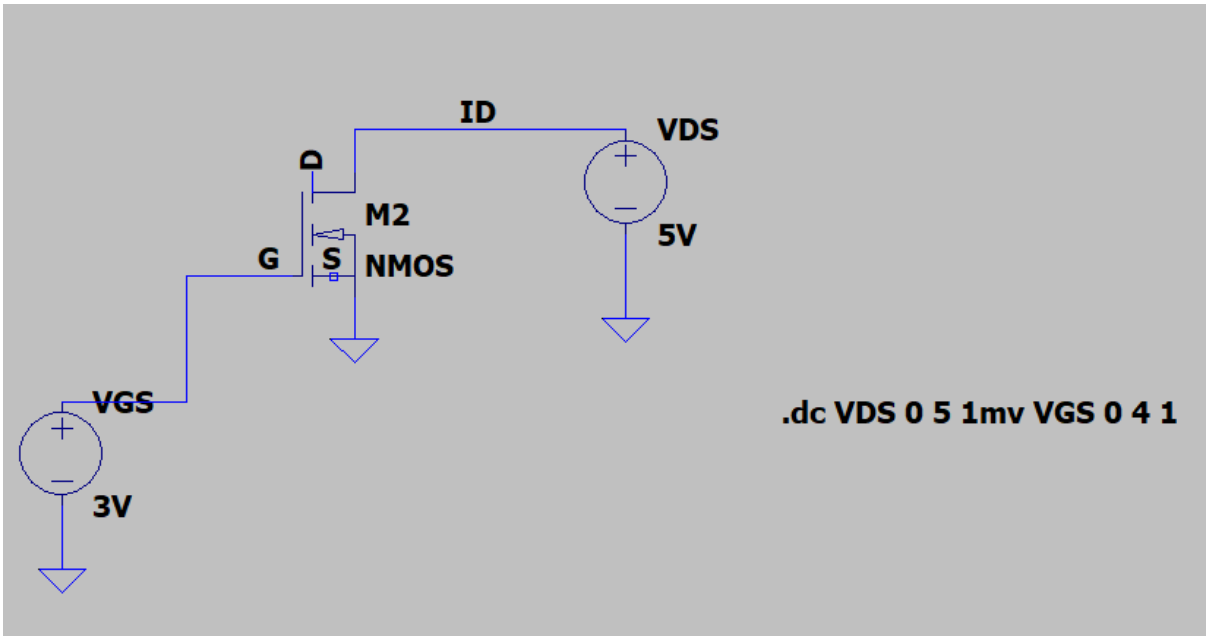
2018UEC2030

SUBJECT: VLSI(ECC20)

EXPERIMENT:1

AIM: TO PLOT THE DC,AC,TRANSIENT CHARACTERISTIC OF NMOS AND PMOS .

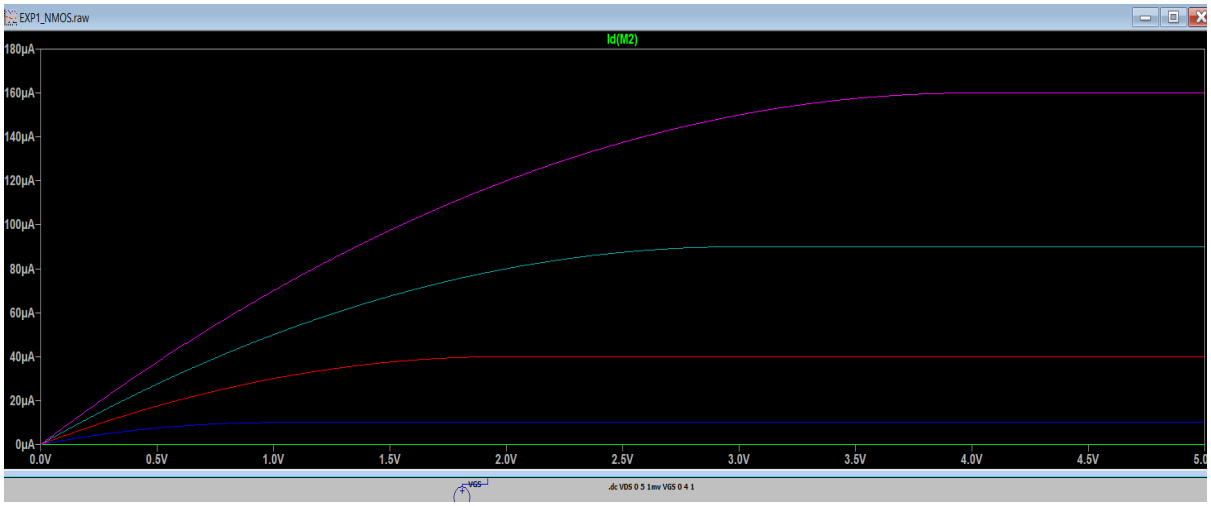
FOR NMOS:



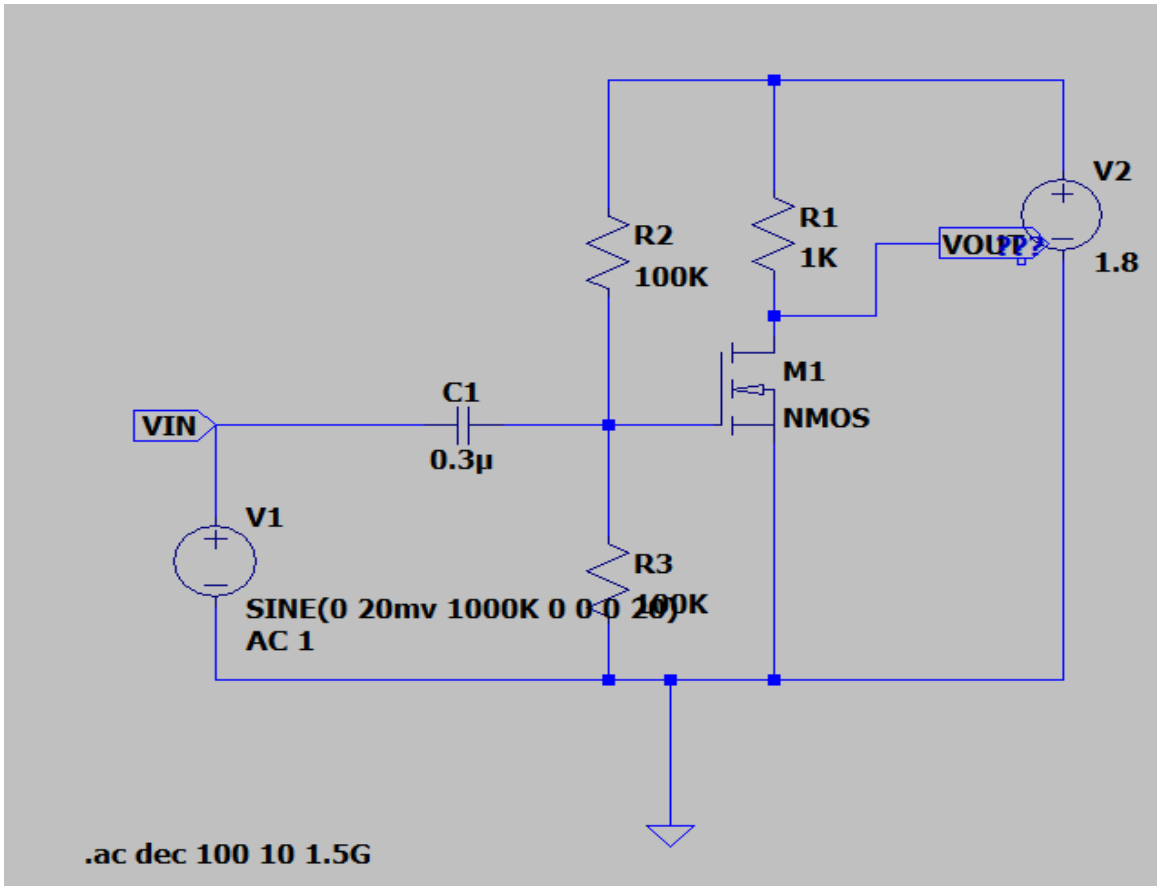
DC Analysis:

.dc VDS 0 5 1mv VGS 0 4 1

GRAPH I(VDS) VS VDS

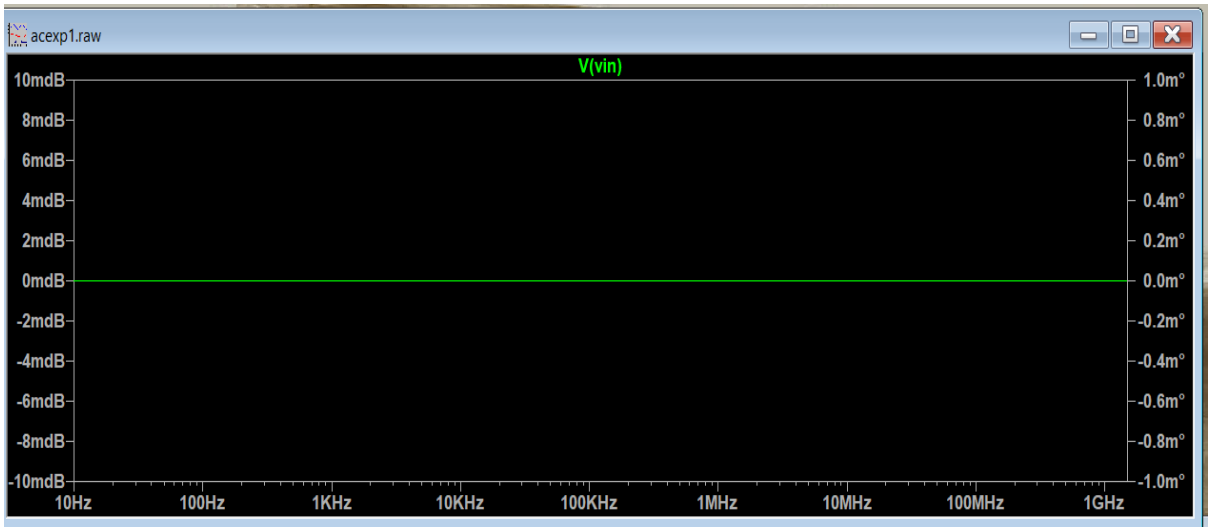


FOR AC ANALYSIS:

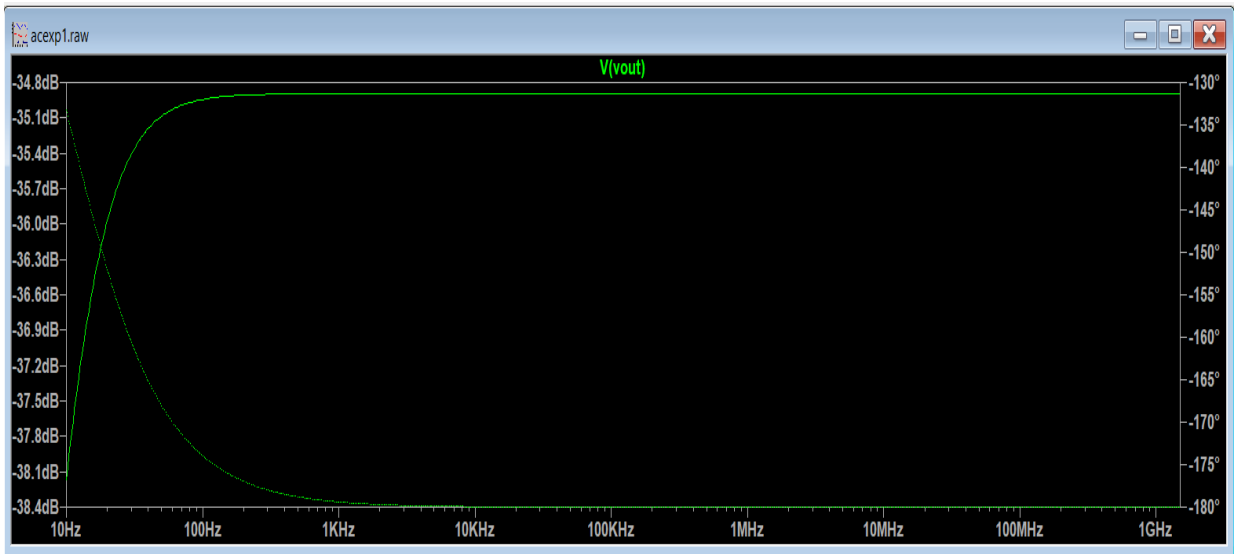


.ac dec 100 10 1.5G

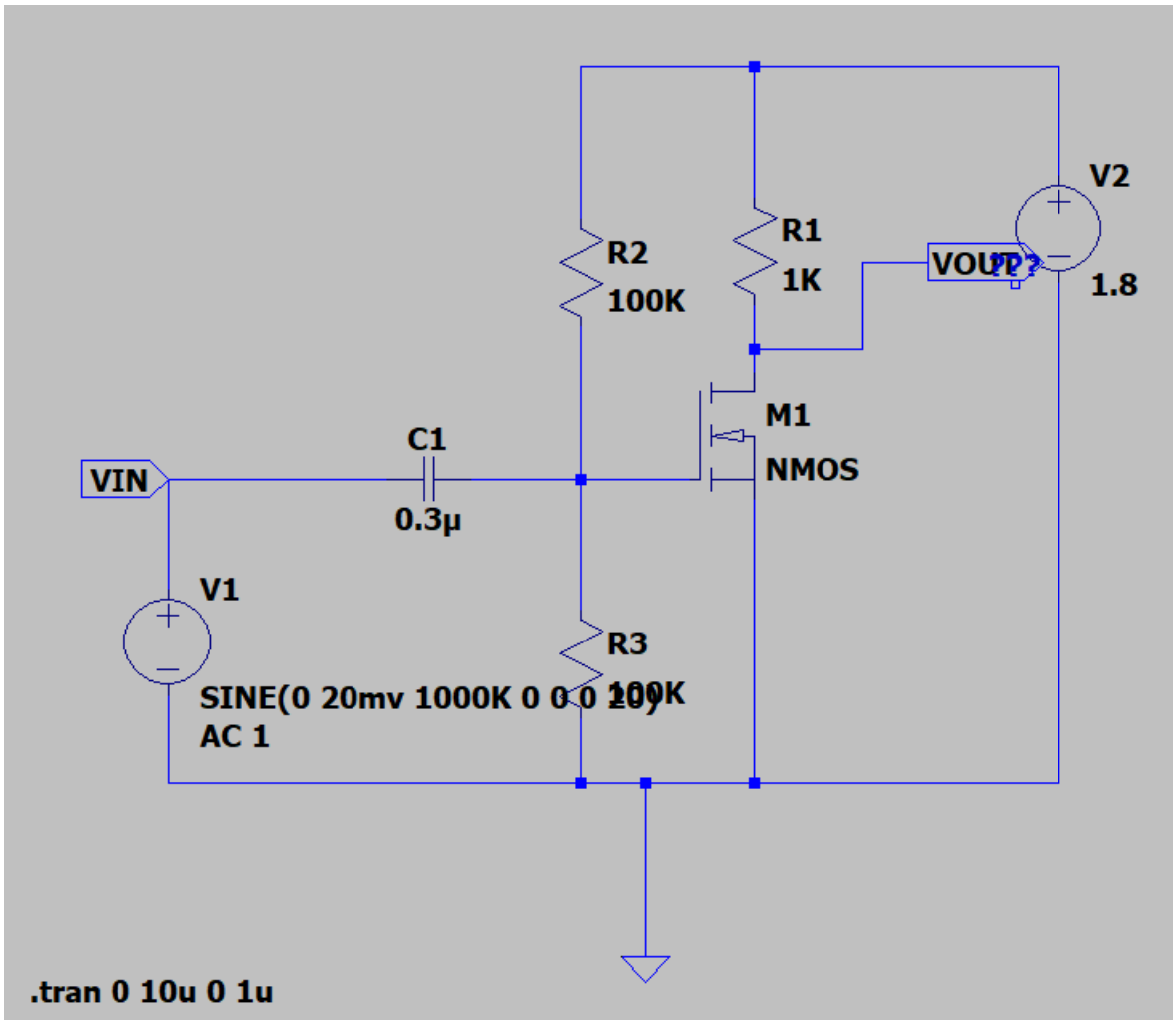
Vin:



Vout:

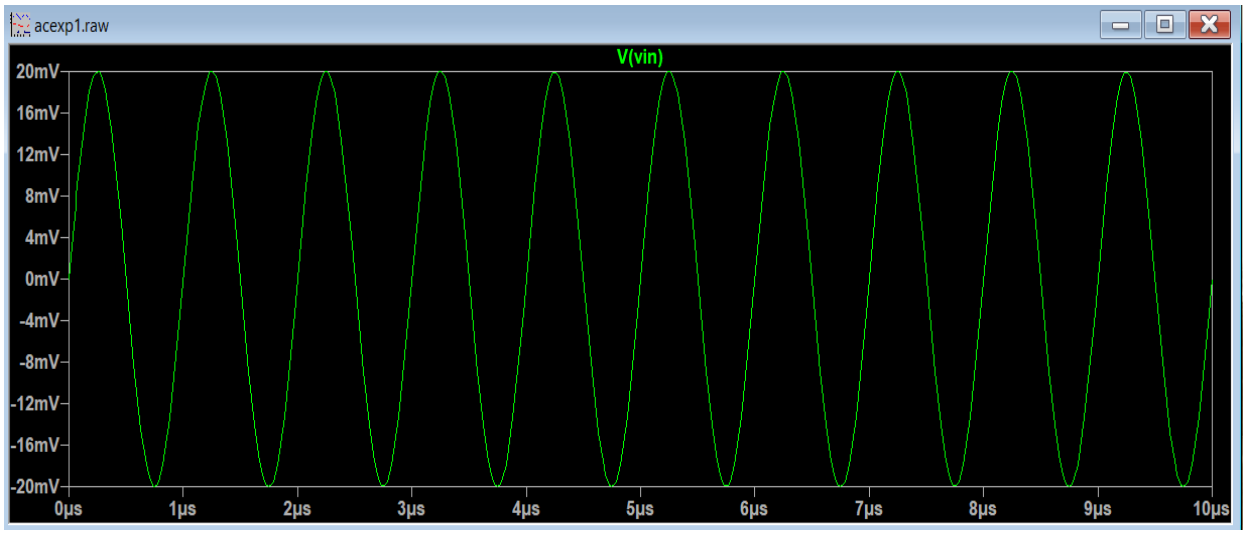


FOR TRANSCIENT ANALYSIS:

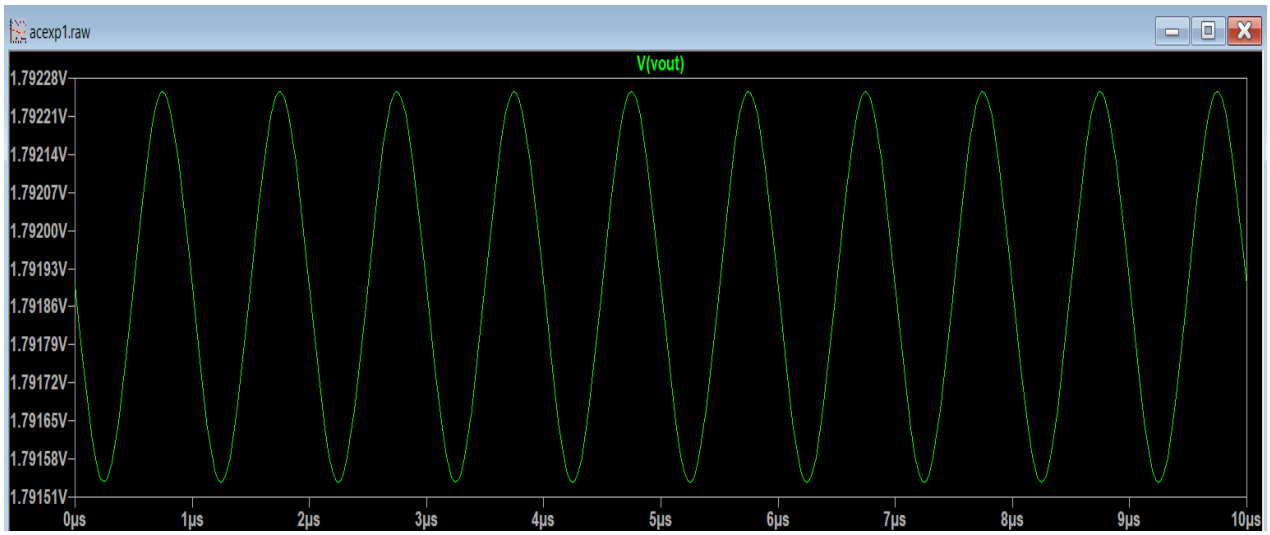


.tran 0 10u 0 1u

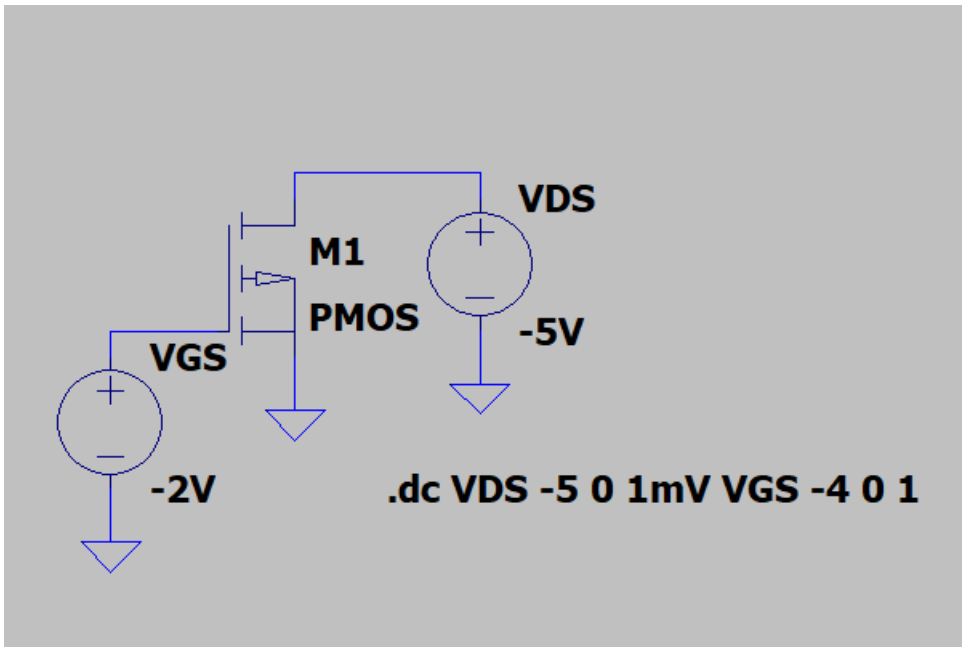
vin



Vout:

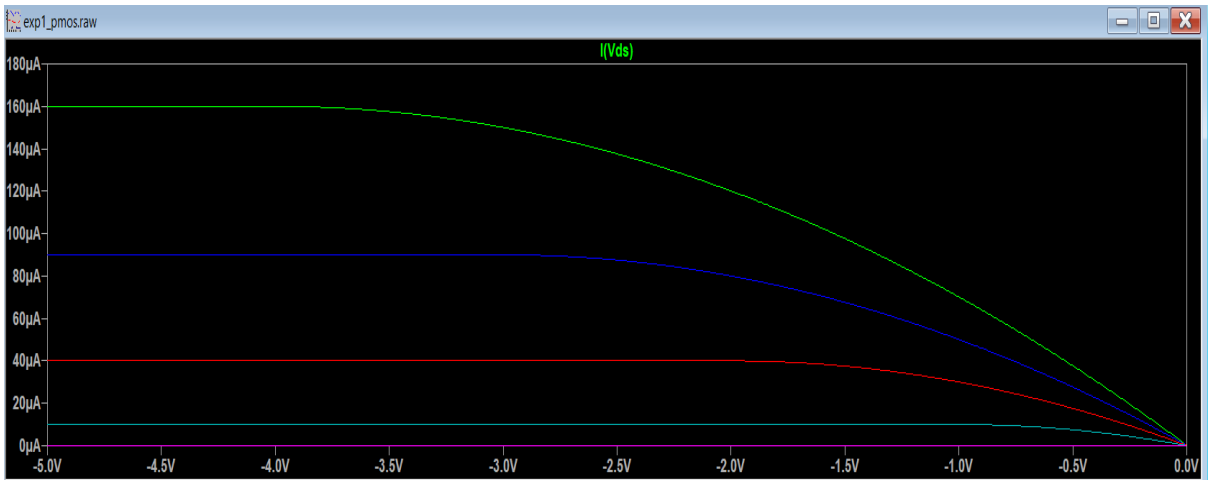


For PMOS:

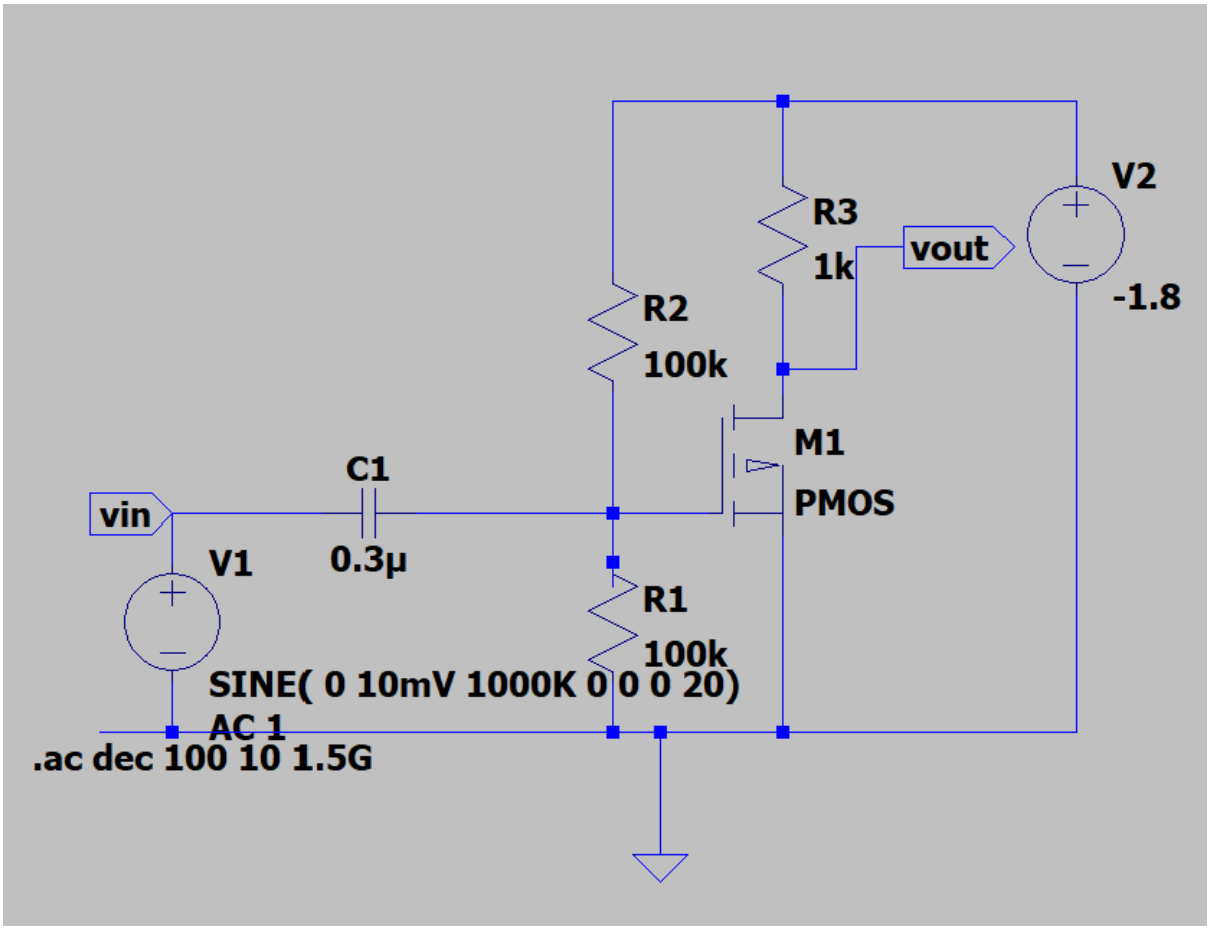


FOR DC ANALYSIS:

.dc VDS -5 0 1mV VGS -4 0 1

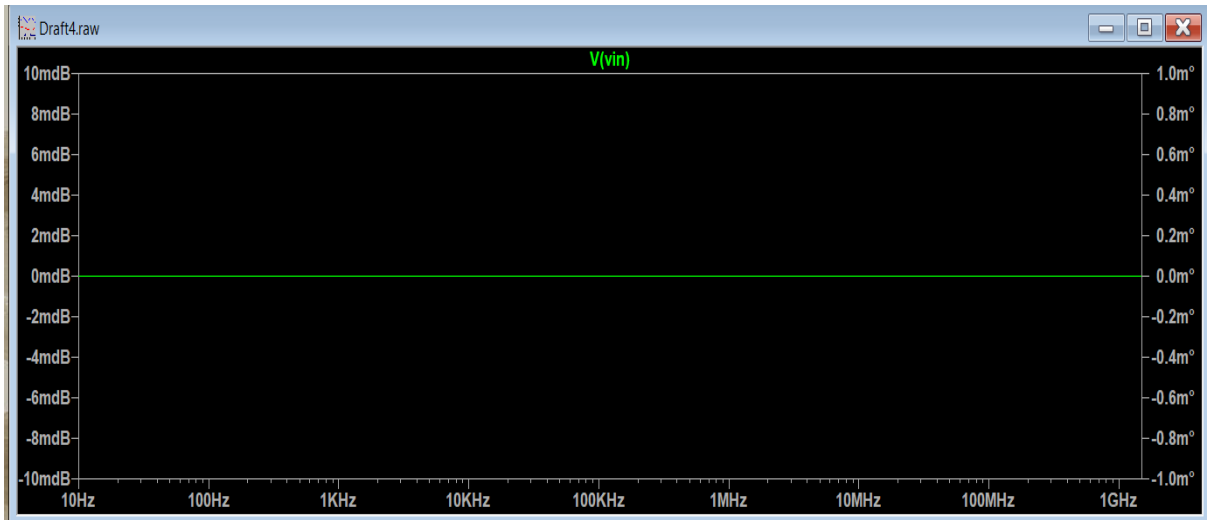


FOR AC ANALYSIS:

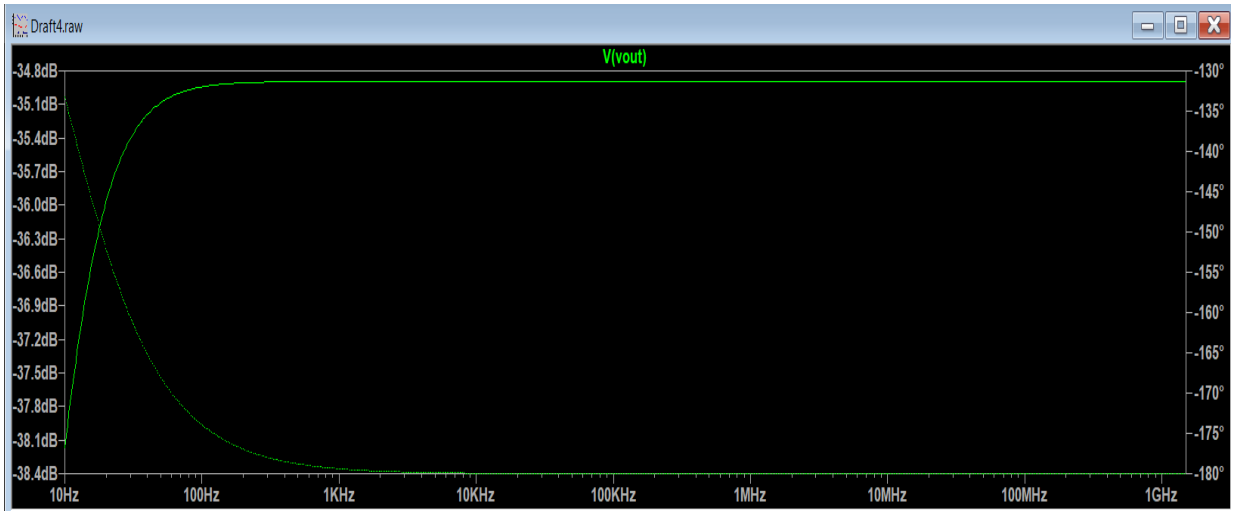


.ac dec 100 10 1.5G

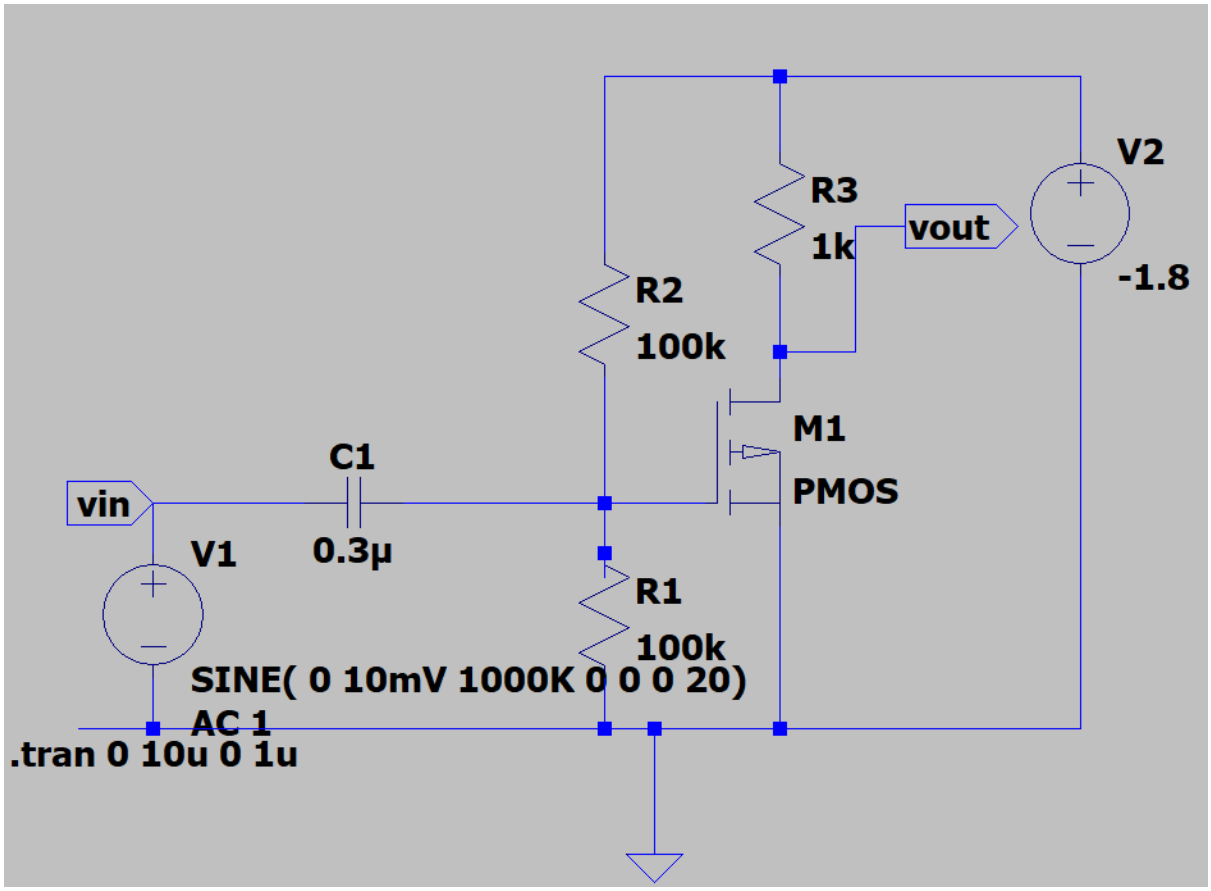
Vin:


Draft4.raw
V(vin)
10mdB
8mdB
6mdB
4mdB
2mdB
0mdB
-2mdB
-4mdB
-6mdB
-8mdB
-10mdB
1.0m°
0.8m°
0.6m°
0.4m°
0.2m°
0.0m°
-0.2m°
-0.4m°
-0.6m°
-0.8m°
-1.0m°
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
100MHz
1GHz

Vout:

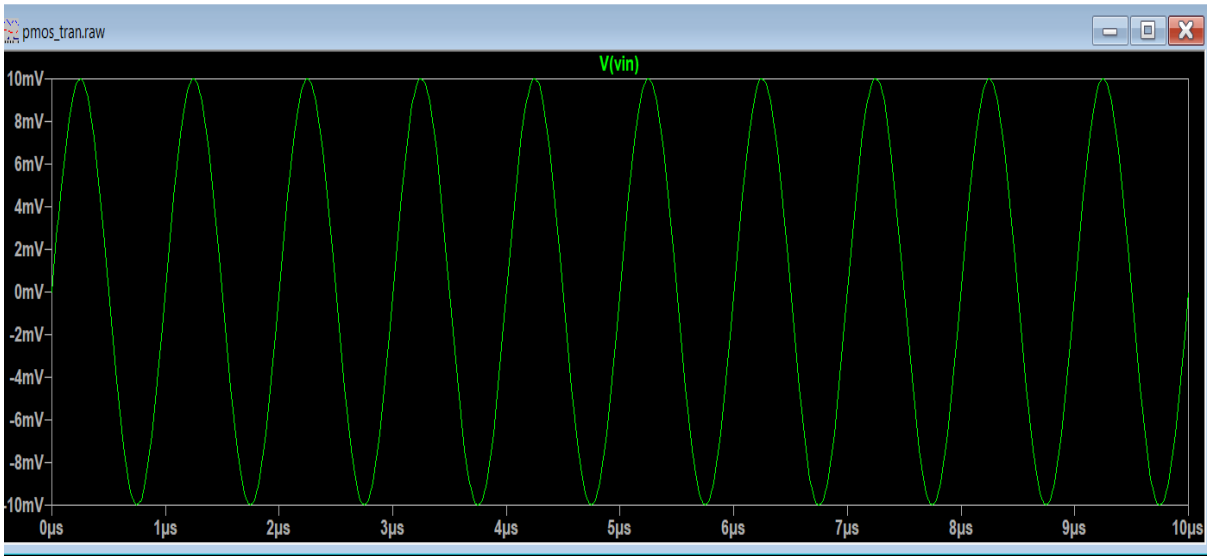

Draft4.raw
V(vout)
-34.8dB
-35.1dB
-35.4dB
-35.7dB
-36.0dB
-36.3dB
-36.6dB
-36.9dB
-37.2dB
-37.5dB
-37.8dB
-38.1dB
-38.4dB
-130°
-135°
-140°
-145°
-150°
-155°
-160°
-165°
-170°
-175°
-180°
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
100MHz
1GHz

For transient analysis:

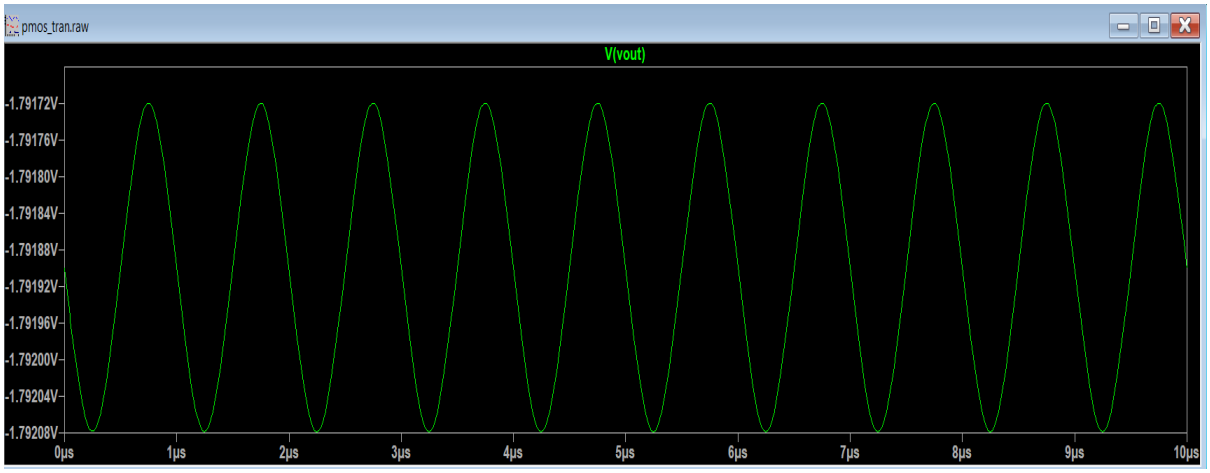


.tran 0 10u 0 1u

Vin:


pmos_tran.raw
V(vin)
10mV
8mV
6mV
4mV
2mV
0mV
-2mV
-4mV
-6mV
-8mV
-10mV
0µs
1µs
2µs
3µs
4µs
5µs
6µs
7µs
8µs
9µs
10µs

Vout:


pmos_tran.raw
V(vout)
-1.79172V
-1.79176V
-1.79180V
-1.79184V
-1.79188V
-1.79192V
-1.79196V
-1.79200V
-1.79204V
-1.79208V
0µs
1µs
2µs
3µs
4µs
5µs
6µs
7µs
8µs
9µs
10µs

RESULTS:

Different types of response of MOSFET circuits for DC, AC and Transient Analysis using

LTSpice were studied, simulated, plotted and observed. The results were similar to

what was expected theoretically with minor errors.

PRECAUTIONS AND SOURCES OF ERROR:

1. Code should be correct.

2. The correct elements should be used.

3. Values should be defined as used in the experiment.

4. Incorrect values can lead to incorrect results.

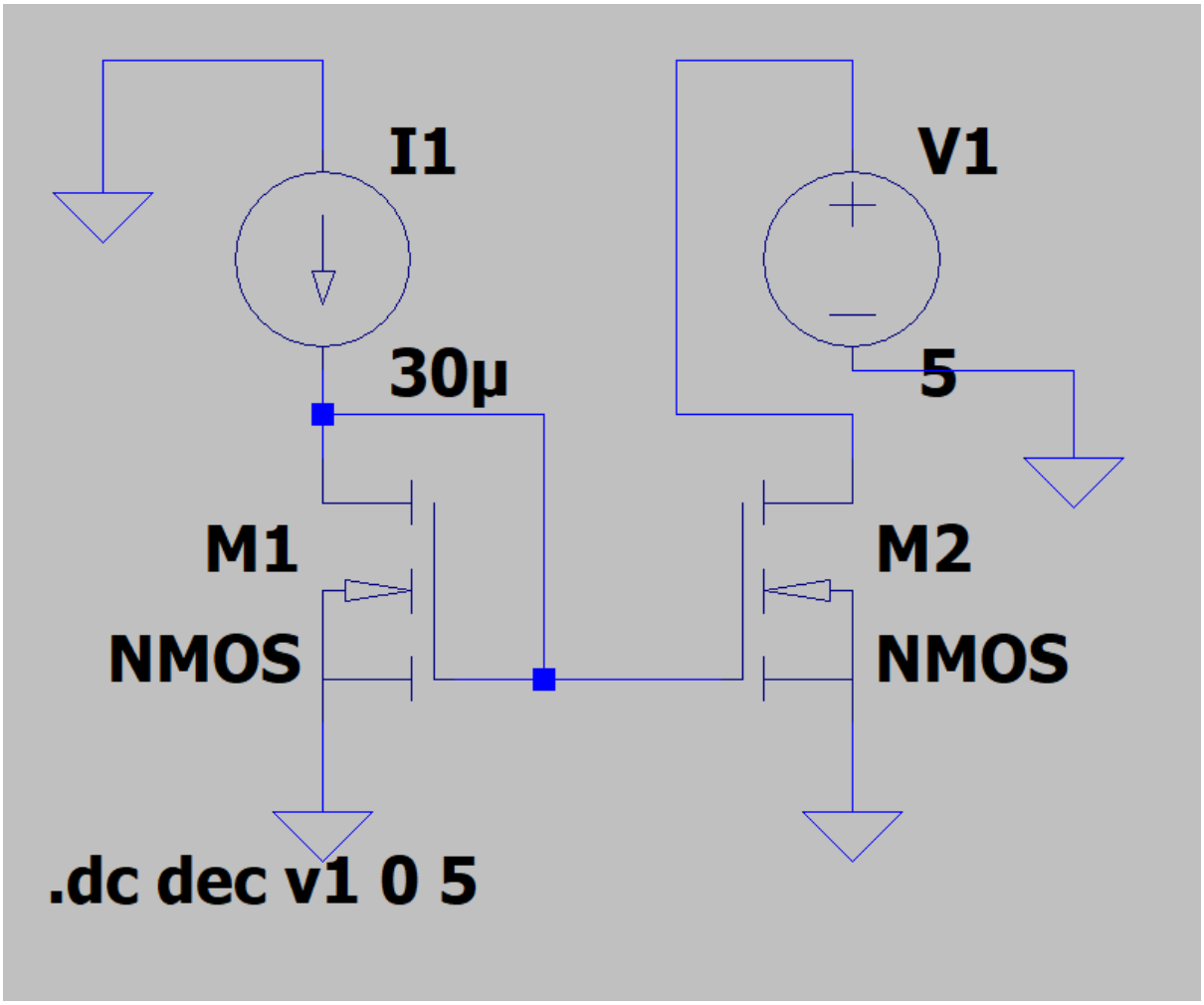
NAME: UMESH

ROLL NO. :2018UEC2030

EXPERIMENT:2

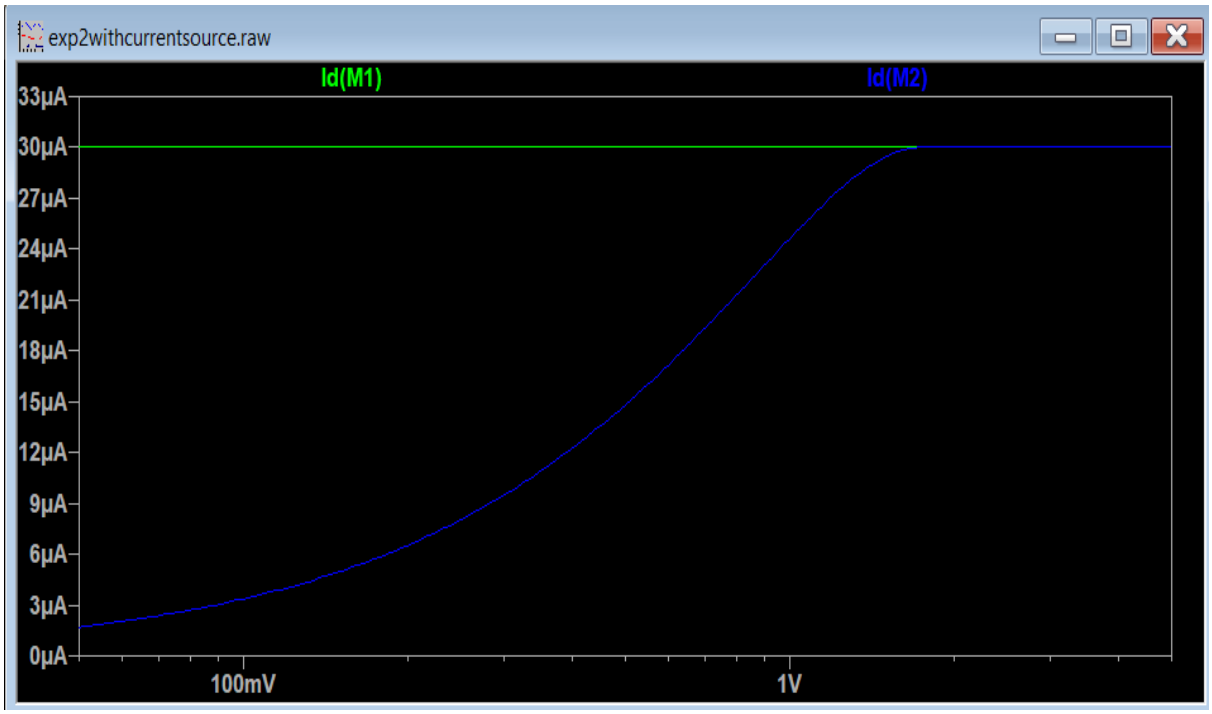
AIM: To simulate the simple MOS current mirror and cascode and Wilson current. Verify it's operation and find out Vmin

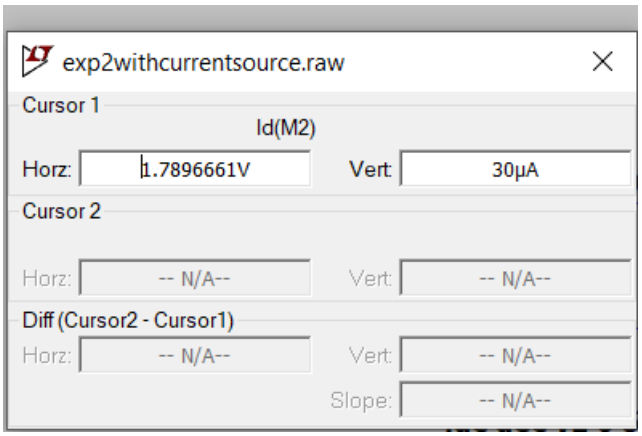
<u>WITH DIRECT CURRENT SOURCE</u>



.dc dec v1 0 5

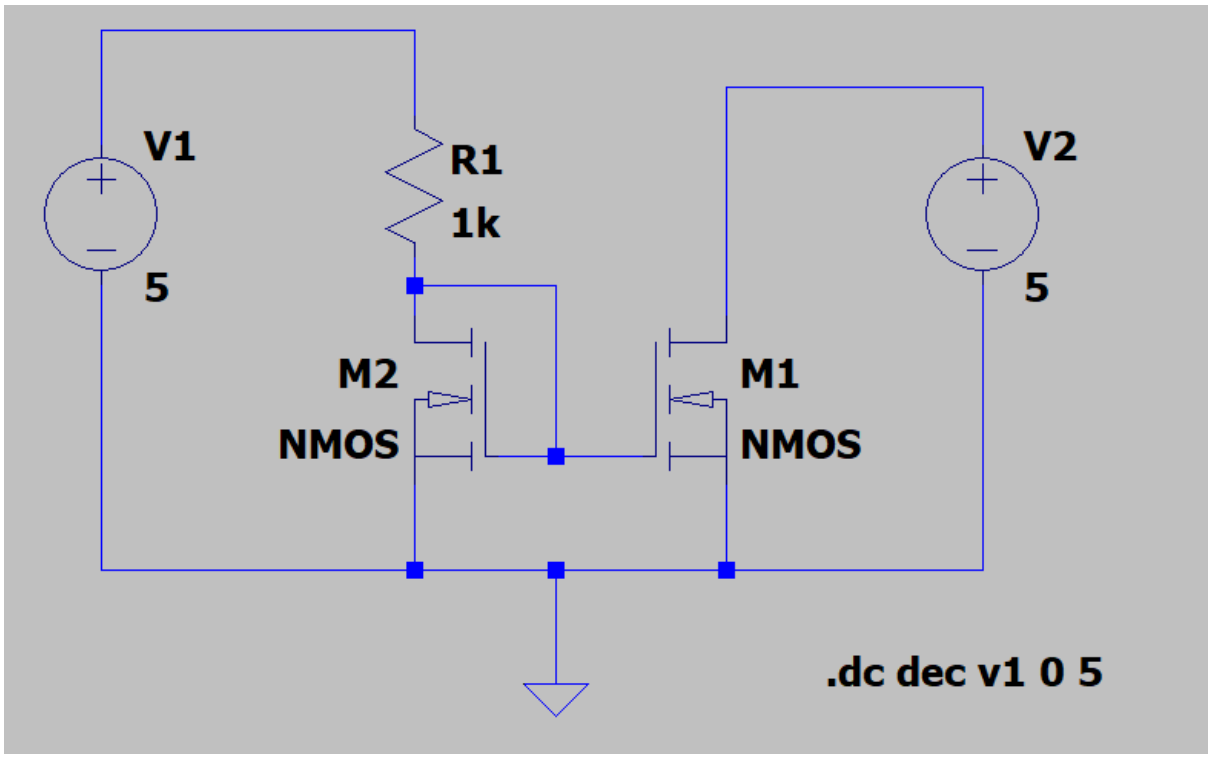
Output





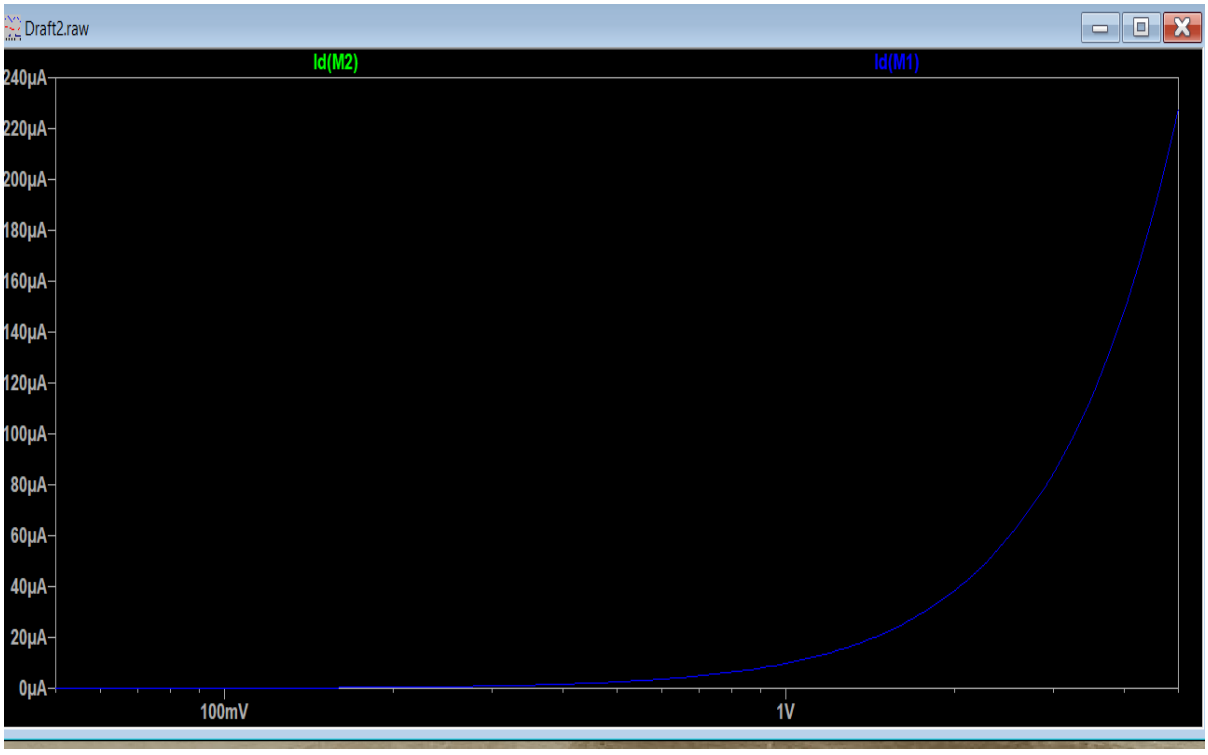
We get voltage: 1.7896661v

Now using voltage source with resistance

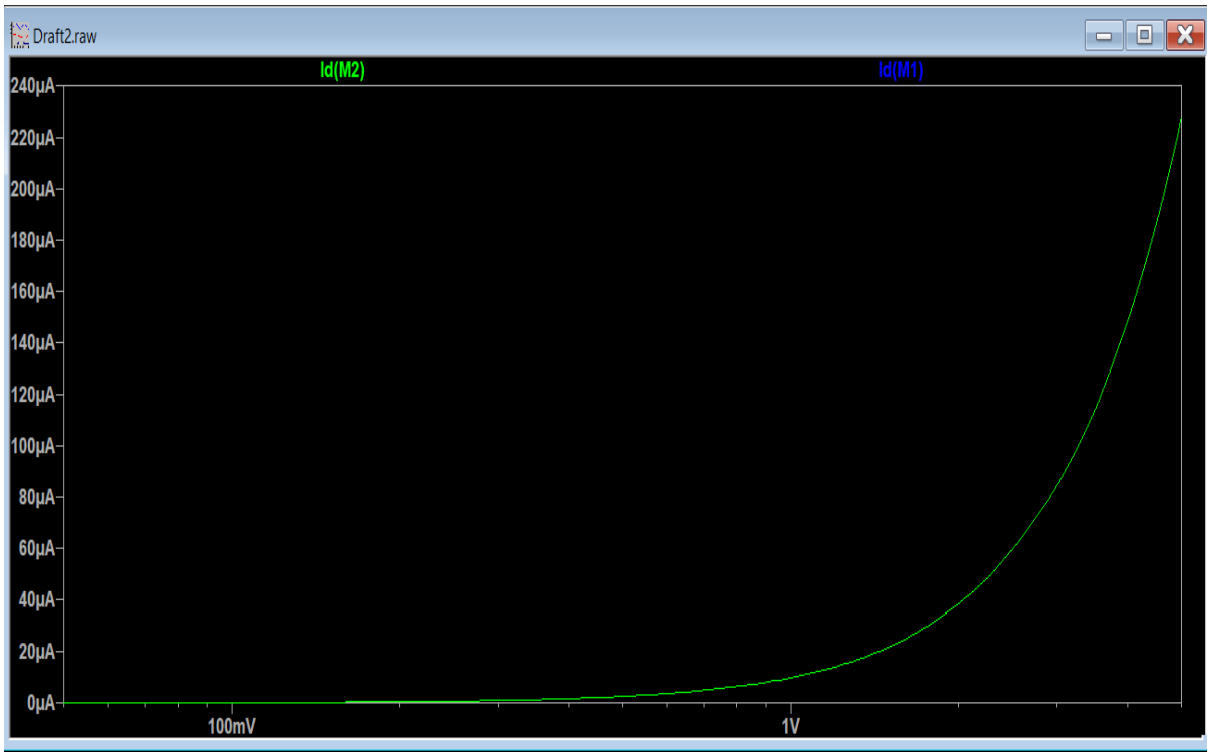


Input current:

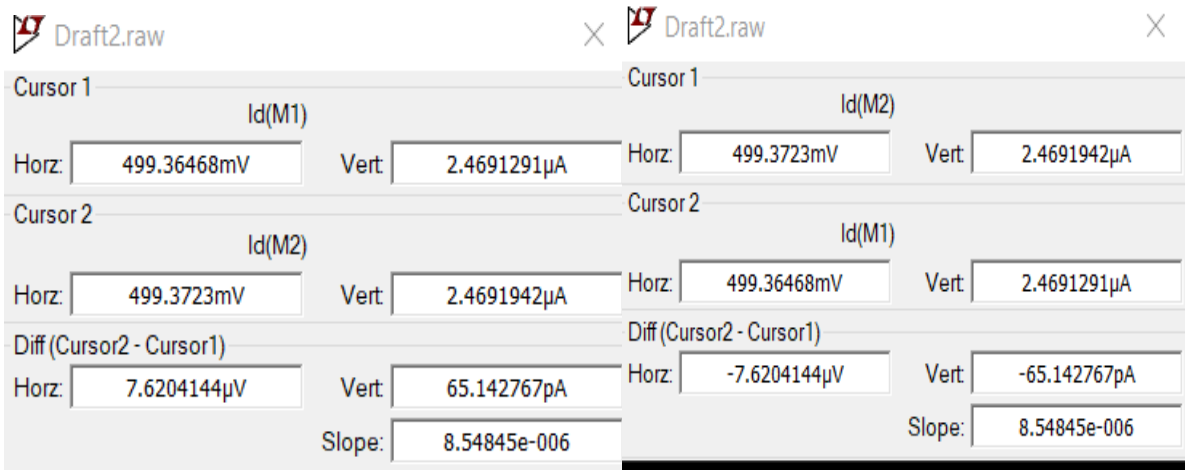
For idm1



For idm2

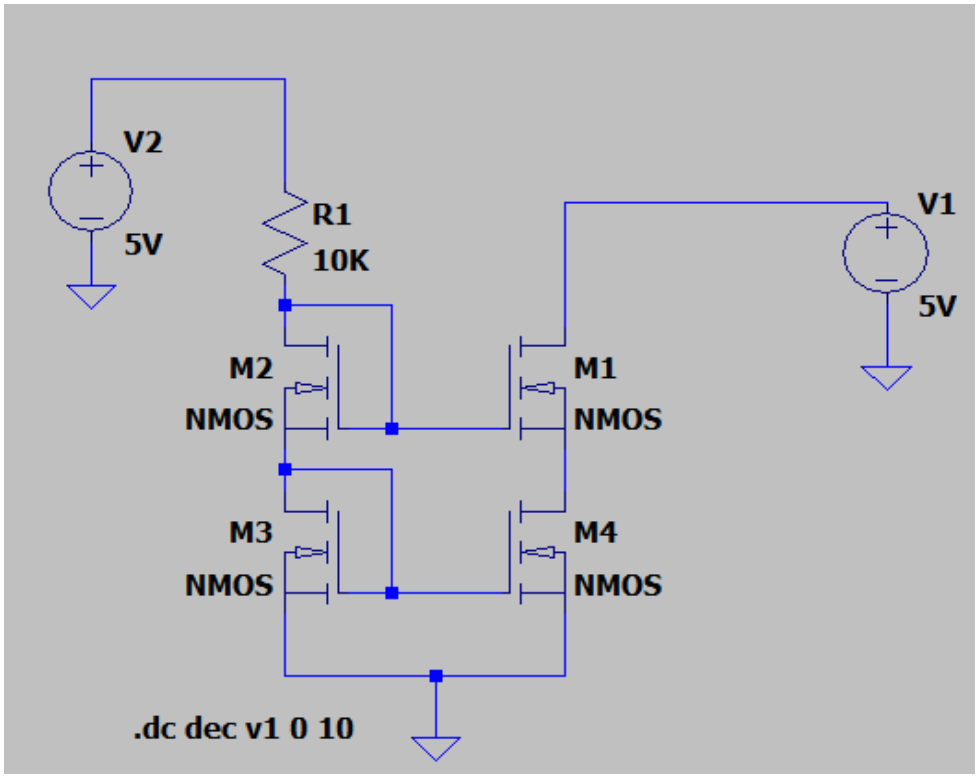


Both are currents mirror.because both are identical

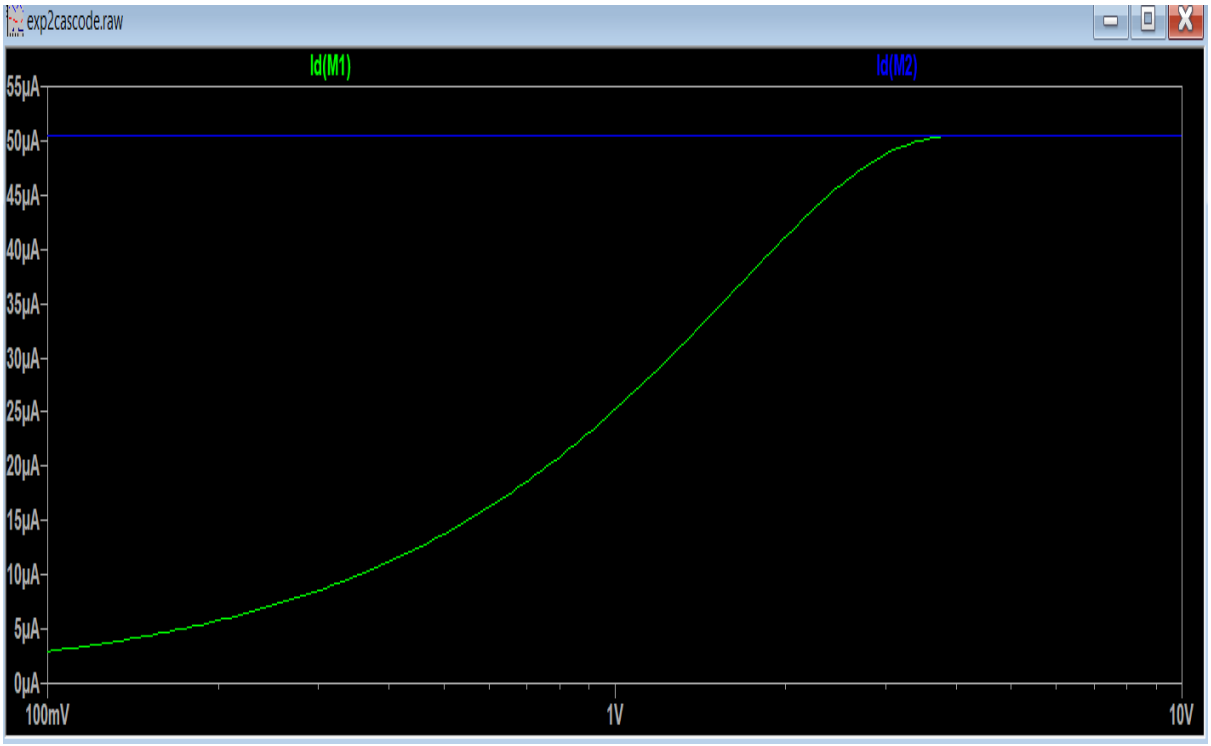


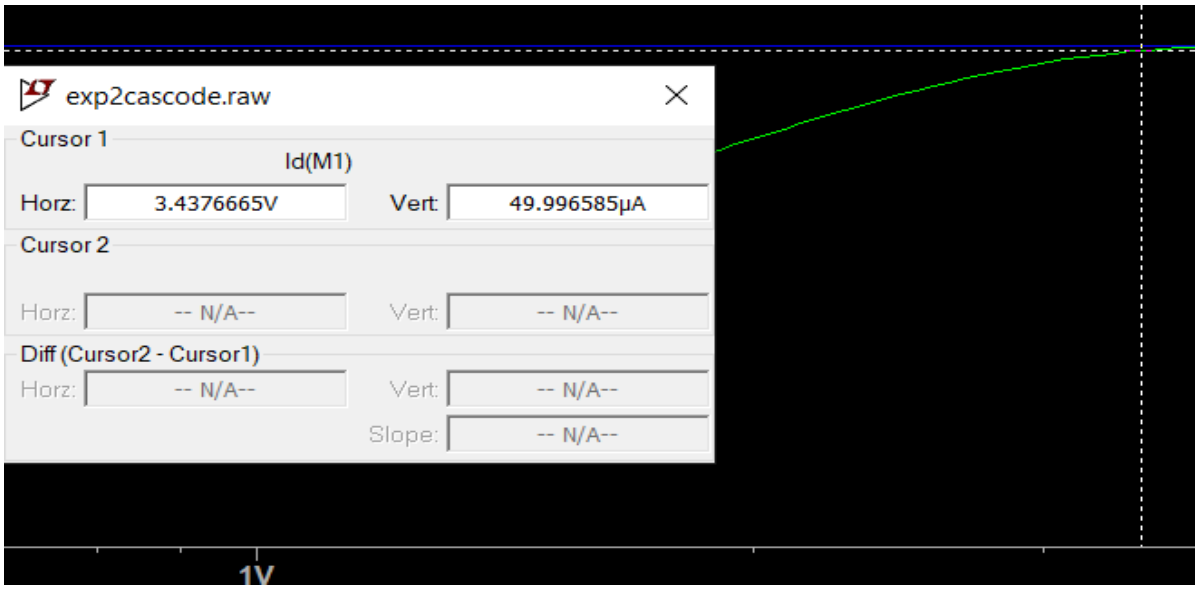
Vmin=499.3723mV

For cascode



Output currents graph

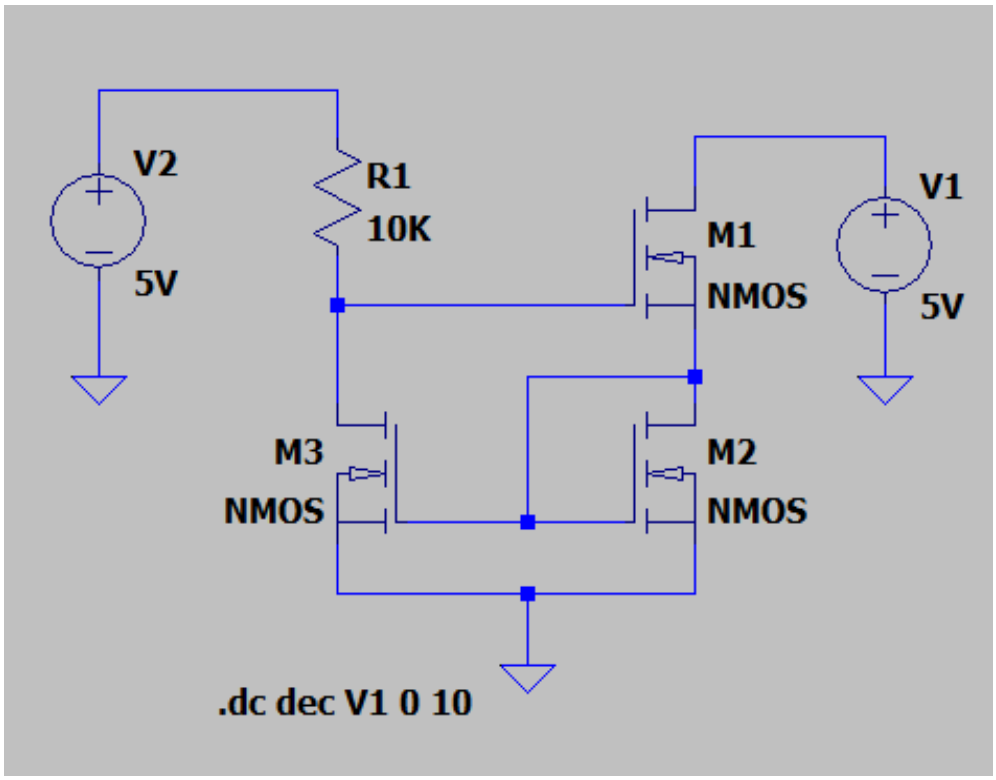


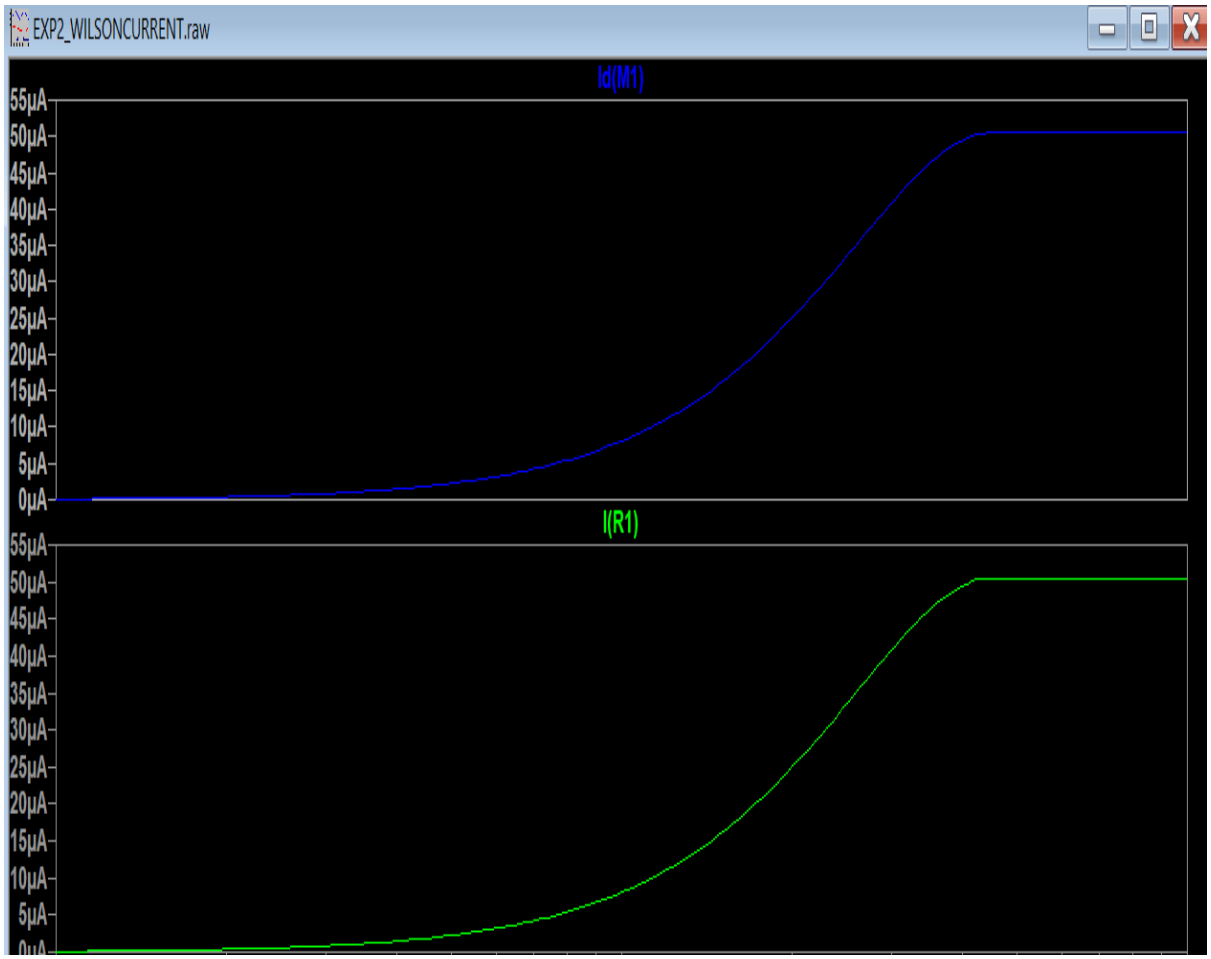


Vmin=3.4376665v

Iin =50Ua and our Iout is approximately equal to 49.996585uA

<u>FOR WILSON CURRENT MIRROR</u>





RESULT:

ALL GRAPHS OF MOS CURRENT MIRRORS and cascode And Wilson current mirror HAVE A MINIMUM POINT of voltage WHERE WE GET EQUAL CURRENT (Iin=Iout) which is shown in above figures.

1)Vmin for 1 mos current mirror using current source directly, vmin=1.7896661v

2) Vmin for 2 mos current mirror using voltage source with resistance, Vmin=499.3723mV

3)Vmin for cascode mos current mirror is Vmin=3.4376665v

PRECAUTIONS :

1) MAY BE YOUR CIRCUIT IS WORKING PROPERLY
2) YOUR CIRCUIT MAY NOT BE GROUNDED

NAME:UMESH

ROLL NO.: 2018UEC2030

ECE SECTION 1

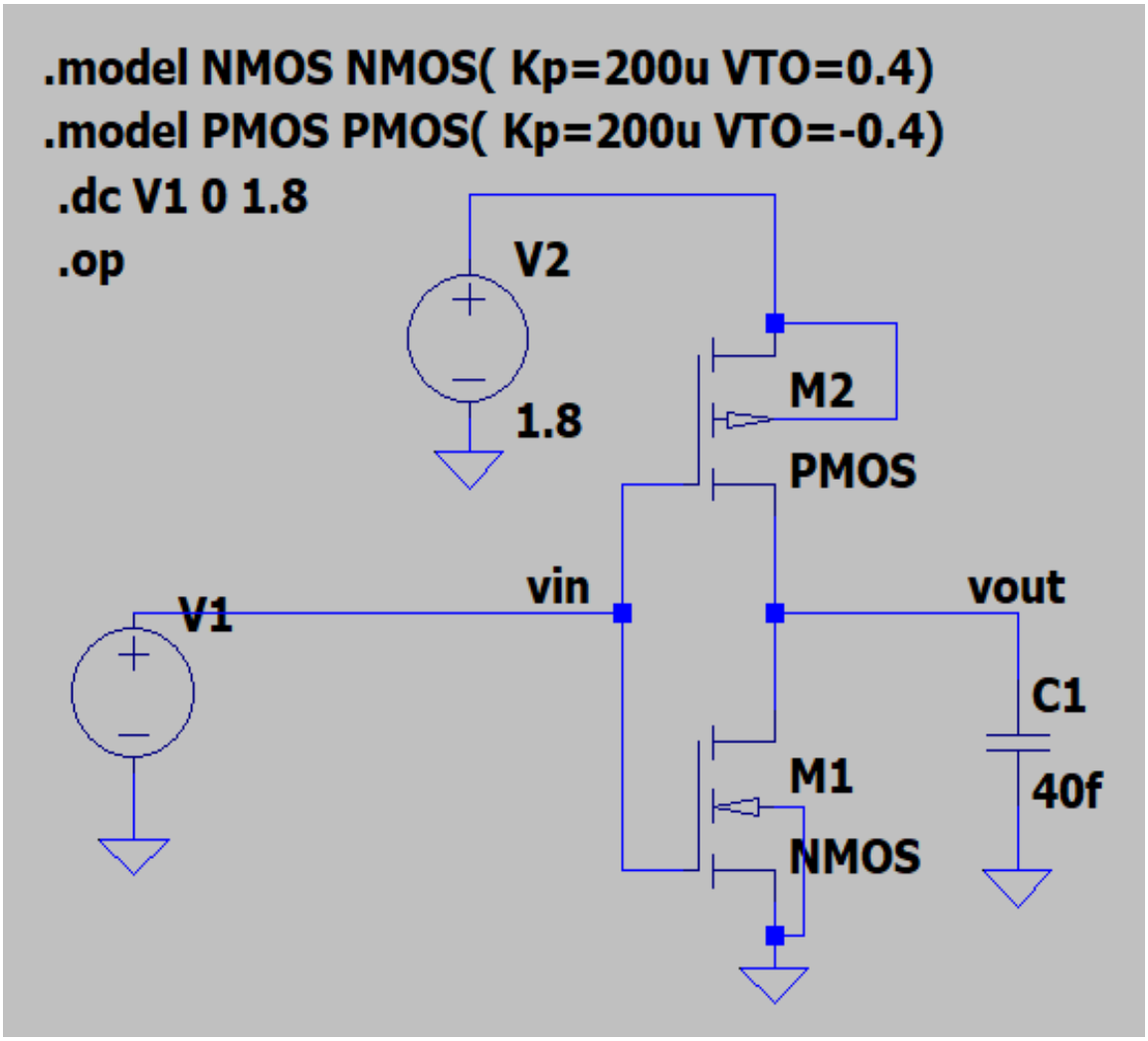
VLSI EXPERIMENT NO. 3

COURSE CODE: ECC20

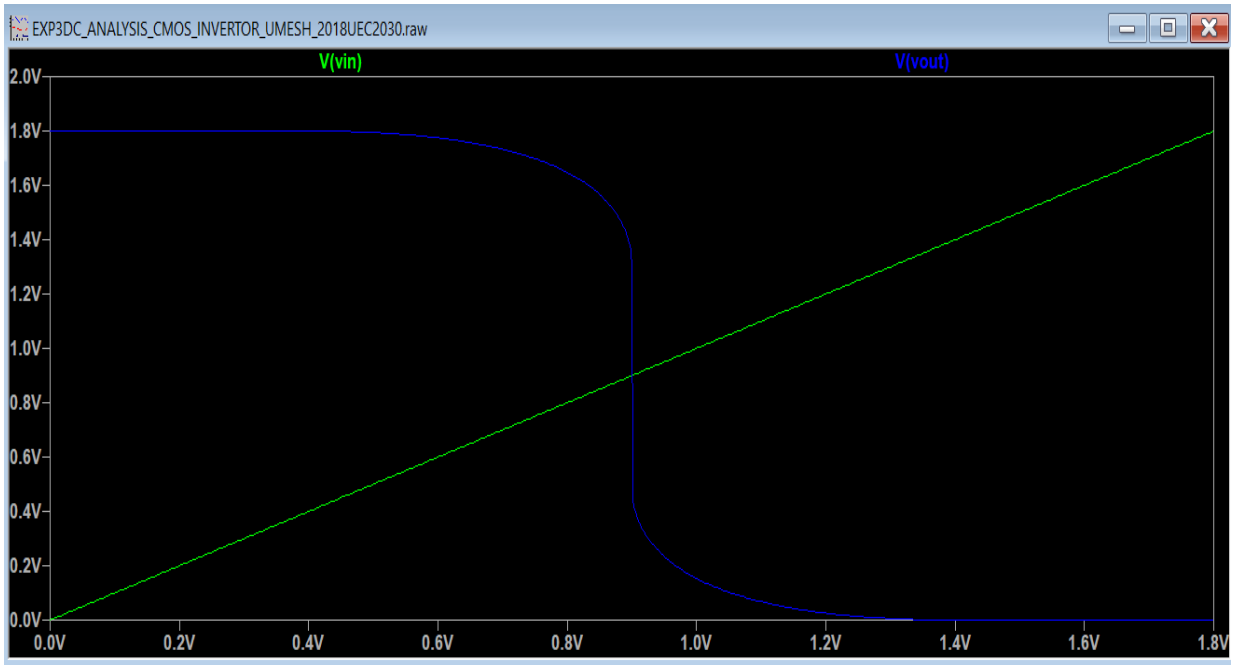
EXPERIMENT 3

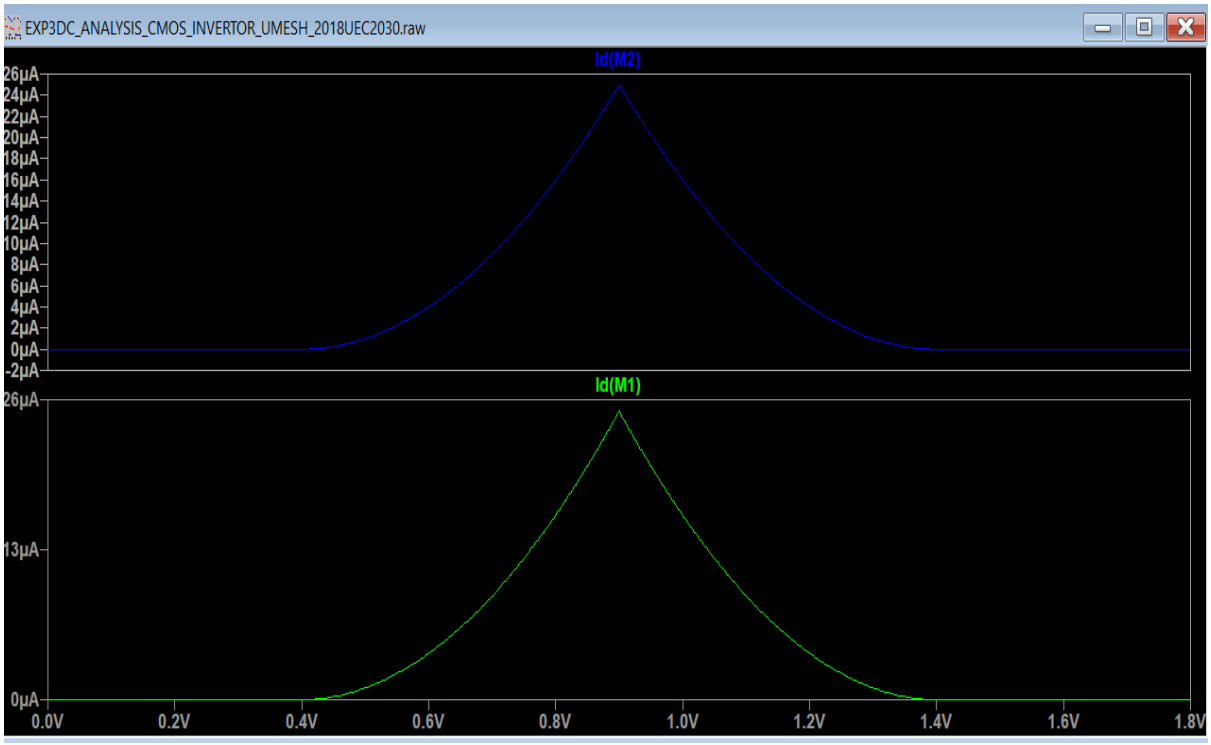
AIM: To Study, Simulate, Plot and Observe CMOS Inverter Characteristics using DC and Transient Analysis.

DC ANALYSIS



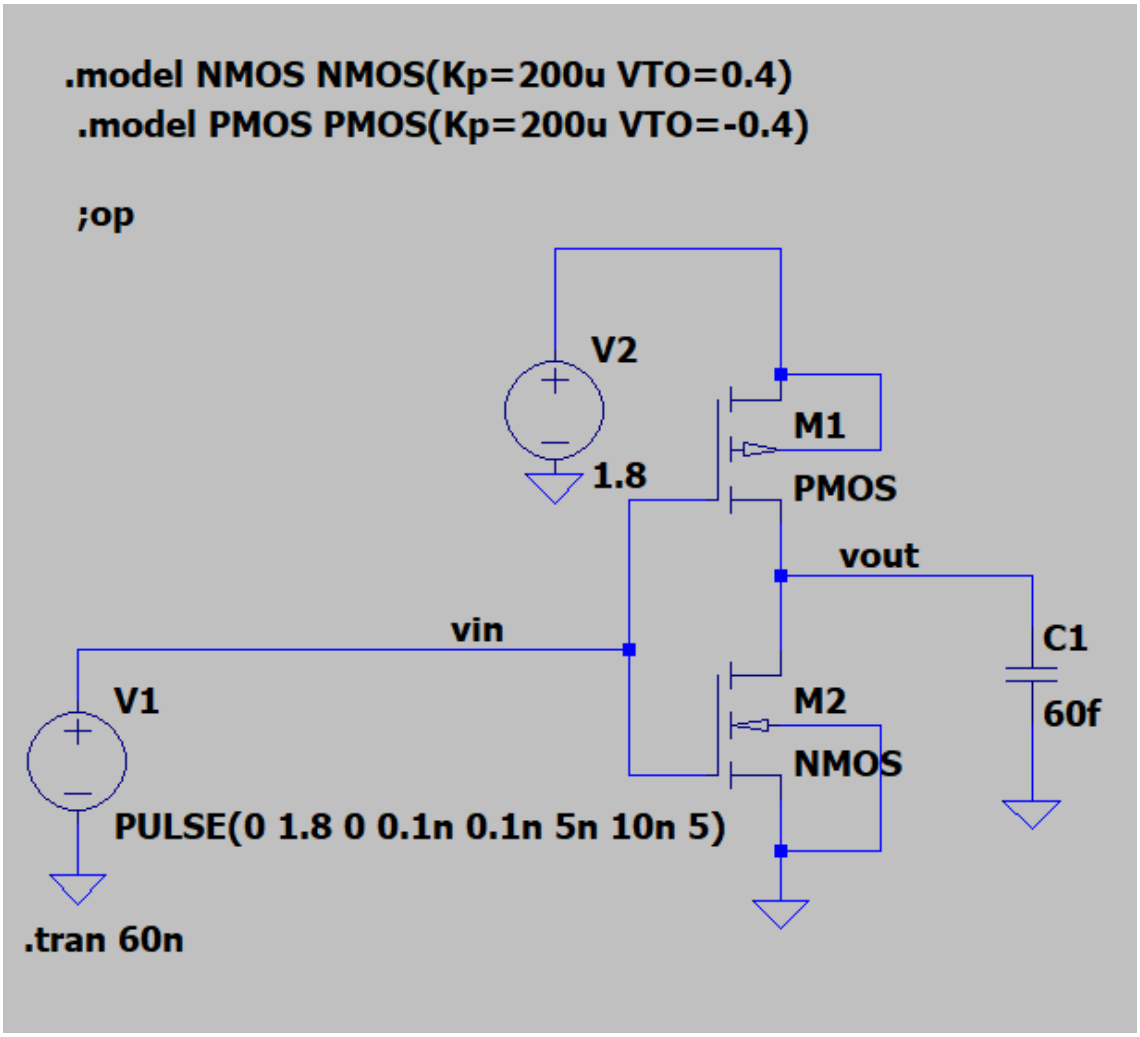
OUTPUTS


EXP3DC_ANALYSIS_CMOS_INVERTOR_UMESH_2018UEC2030.raw
V(vin)
V(vout)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0.0V
0.2V
0.4V
0.6V
0.8V
1.0V
1.2V
1.4V
1.6V
1.8V

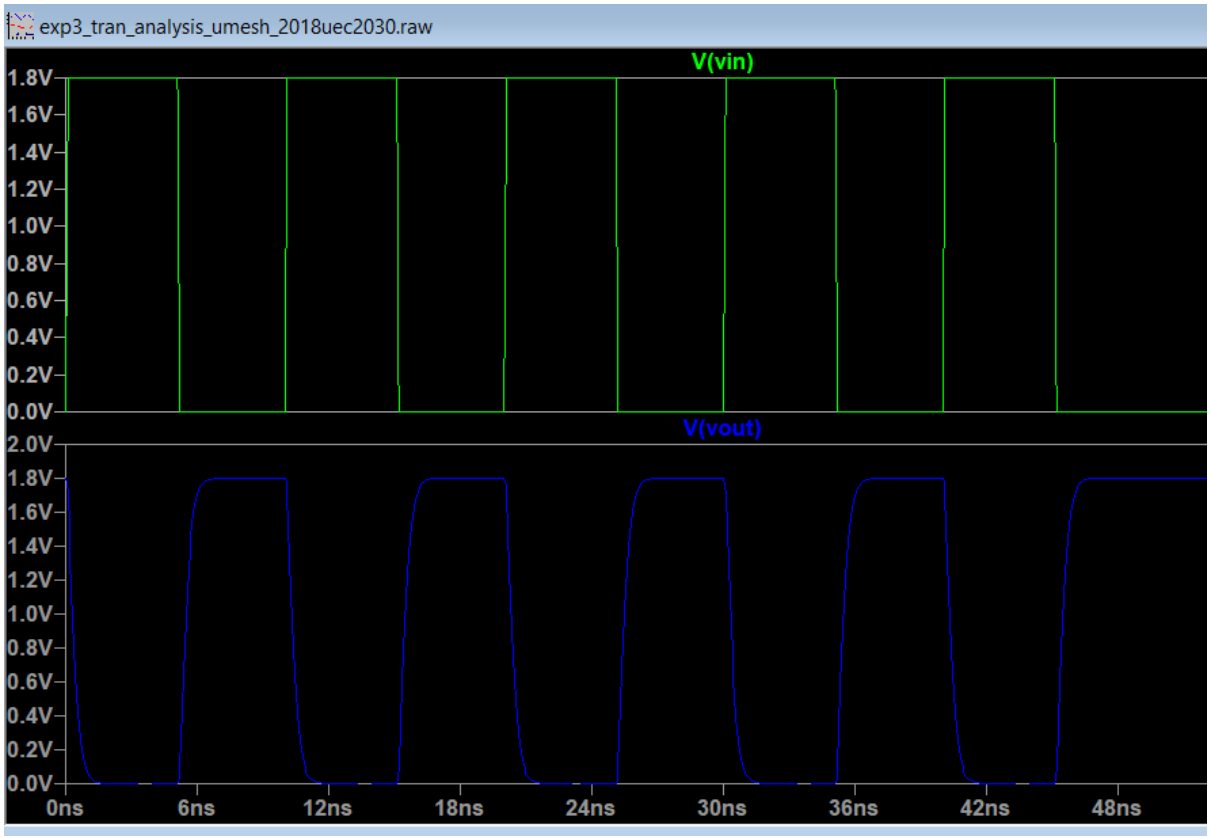

EXP3DC_ANALYSIS_CMOS_INVERTOR_UMESH_2018UEC2030.raw
Id(M2)
26µA
24µA
22µA
20µA
18µA
16µA
14µA
12µA
10µA
8µA
6µA
4µA
2µA
0µA
-2µA
Id(M1)
26µA
13µA
0µA
0.0V
0.2V
0.4V
0.6V
0.8V
1.0V
1.2V
1.4V
1.6V
1.8V

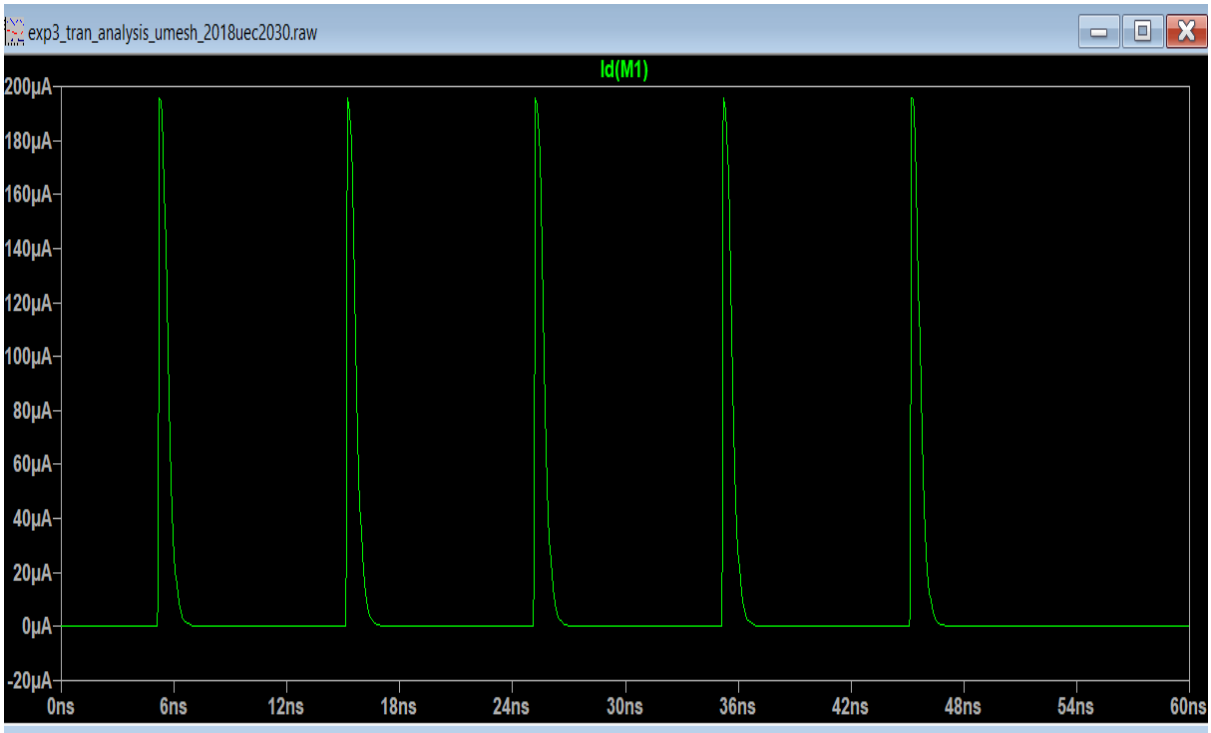
```
--- Operating Point ---

V(vout):        1.8             voltage
V(vin):         0               voltage
V(n001):        1.8             voltage
Id(M2):         3.60731e-012    device_current
Ig(M2):         -0              device_current
Ib(M2):         6.43112e-021    device_current
Is(M2):         -3.60731e-012   device_current
Id(M1):         3.61e-012       device_current
Ig(M1):         0               device_current
Ib(M1):         -1.81e-012      device_current
Is(M1):         -1.8e-012       device_current
I(C1):          3.6e-026        device_current
I(V2):          -3.61e-012      device_current
I(V1):          0               device_current
```

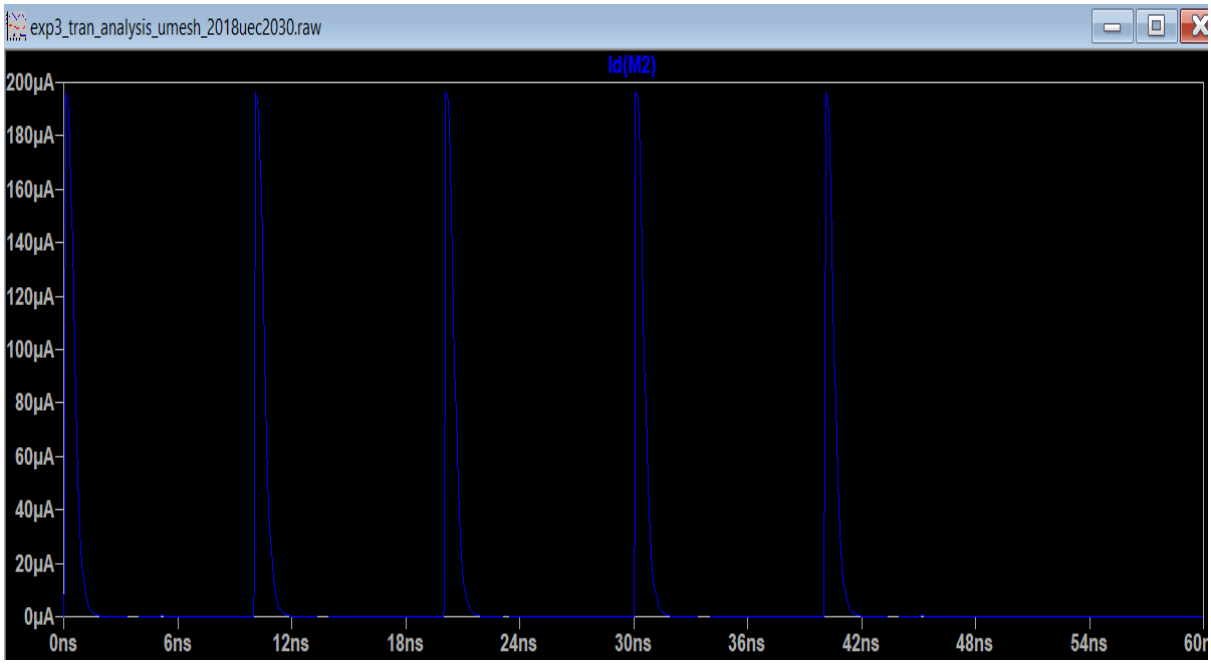
Transient Analysis



Outputs:


exp3_tran_analysis_umesh_2018uec2030.raw
V(vin)
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(vout)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0ns
6ns
12ns
18ns
24ns
30ns
36ns
42ns
48ns


exp3_tran_analysis_umesh_2018uec2030.raw
Id(M1)
200µA
180µA
160µA
140µA
120µA
100µA
80µA
60µA
40µA
20µA
0µA
-20µA
0ns
6ns
12ns
18ns
24ns
30ns
36ns
42ns
48ns
54ns
60ns




```
       --- Operating Point ---

V(vout):        1.8             voltage
V(vin):         0               voltage
V(n001):        1.8             voltage
Id(M2):         3.60731e-012    device_current
Ig(M2):         -0              device_current
Ib(M2):         6.43112e-021    device_current
Is(M2):         -3.60731e-012   device_current
Id(M1):         3.61e-012       device_current
Ig(M1):         0               device_current
Ib(M1):         -1.81e-012      device_current
Is(M1):         -1.8e-012       device_current
I(C1):          9e-026          device_current
I(V2):          -3.61e-012      device_current
I(V1):          0               device_current
```

RESULTS:

Outputs of CMOS Inverter Characteristics using DC and Transient Analysis were

studied, simulated, plotted and observed. The results were similar to what was

expected theoretically with minor errors

.

PRECAUTIONS AND SOURCES OF ERROR:

1. Code should be correct.

2. The correct elements should be used.

3. Values should be defined as used in the experiment.

4. Incorrect values can lead to varying results from what is expected.

5. Different elements can also cause varying results slightly.

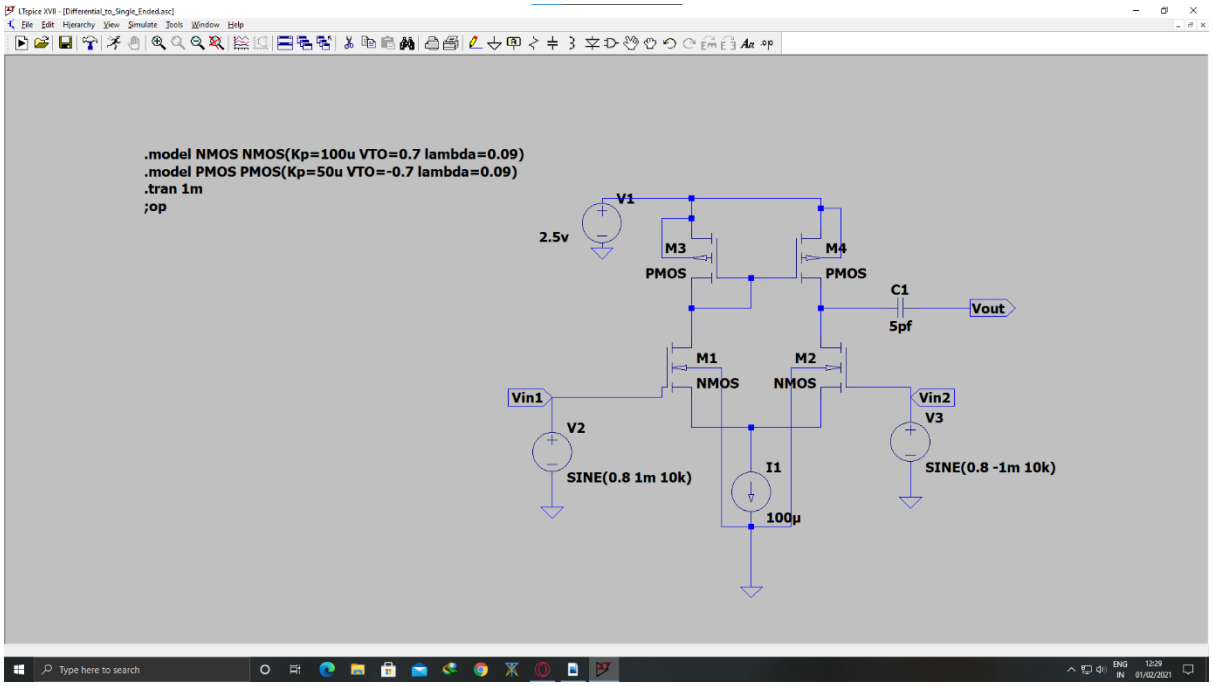
NAME: UMESH
ROLL NUMBER: 2018UEC2030
CLASS/SECTION: Electronics and Communication Engineering 1
SUBJECT: VLSI (ECC20)
DATE: 28/01/2021

EXPERIMENT 4

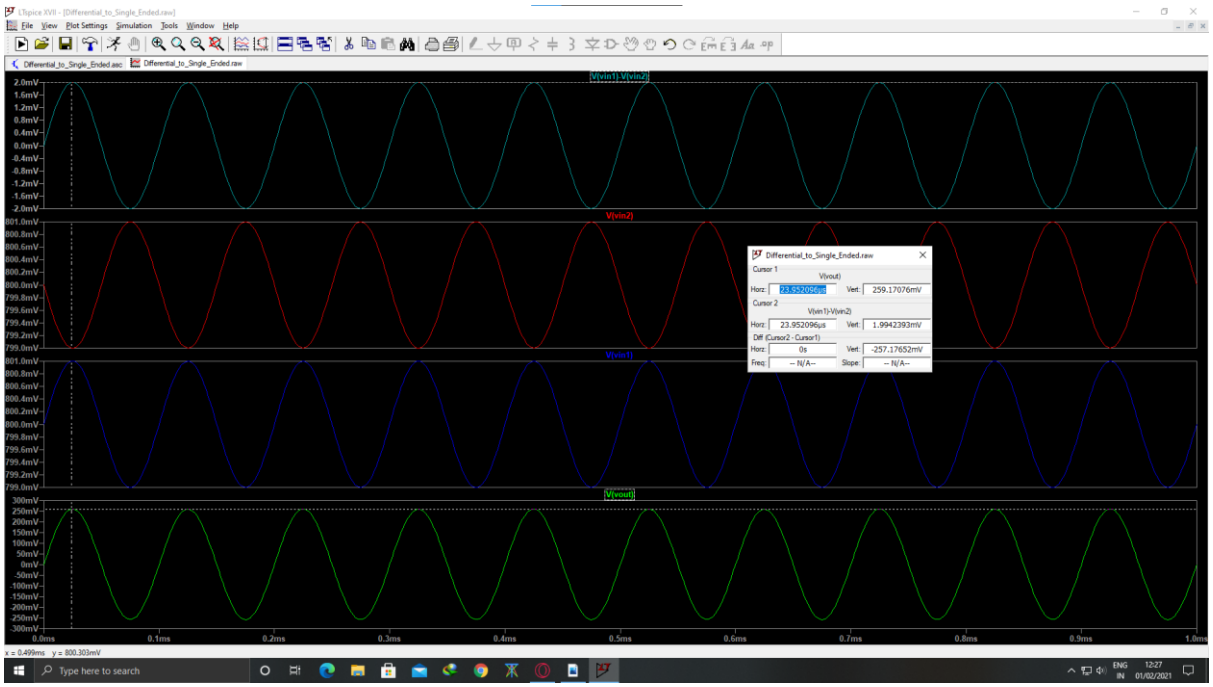
AIM:
To Study, Simulate, Plot and Observe output of Single Ended Differential Amplifier and Single Ended Differential Amplifier in Cascode Configuration.

Single Ended Differential Amplifier

Circuit:



Output:

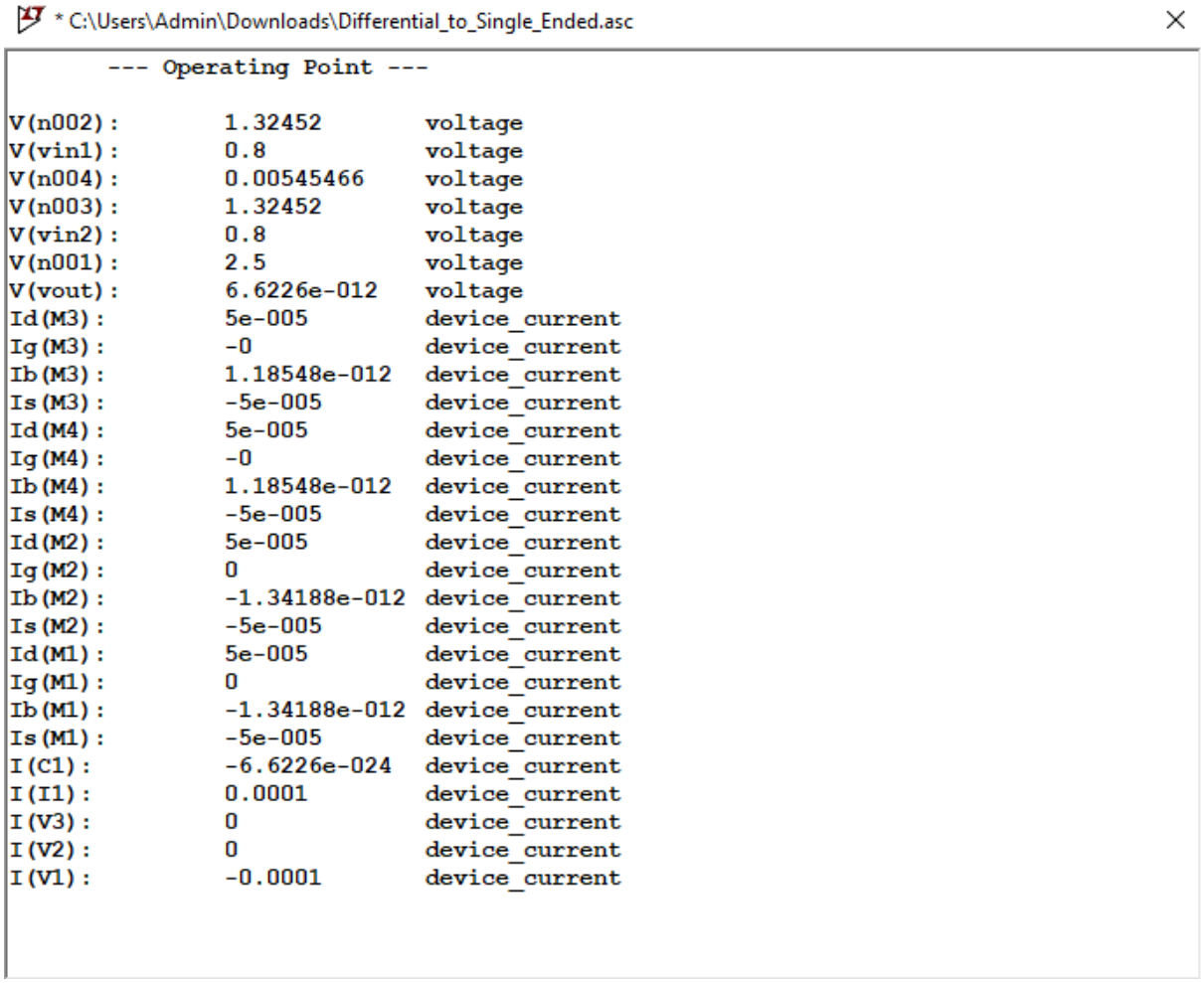


V(vin1)-V(vin2) = 1.994 mV

V(out) peak = 259.170mV

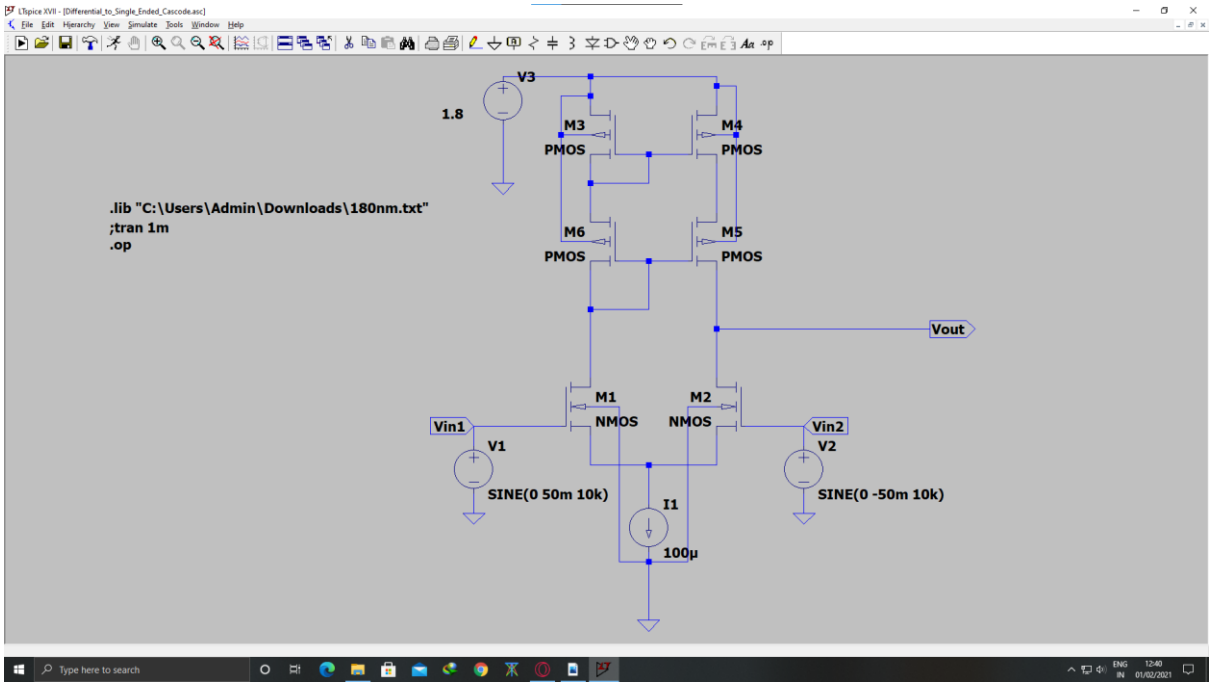
Gain = 259.170/1.994 = 129.975

Operating Bias Point Windows Solution:

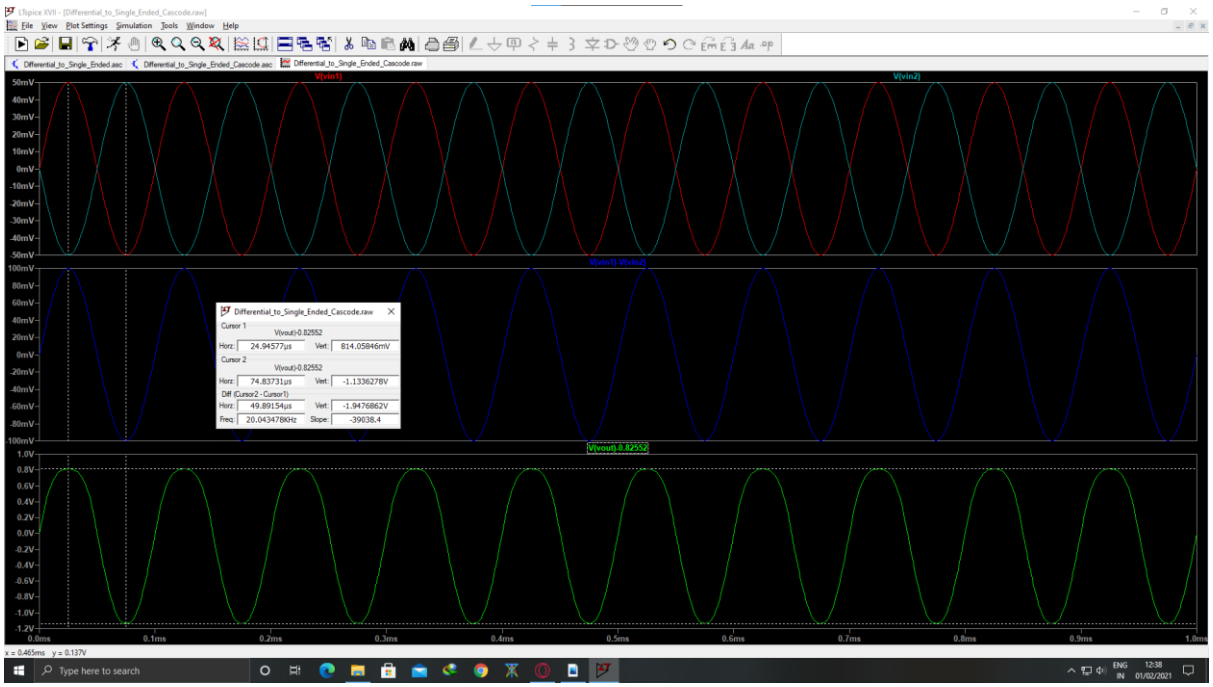


Single Ended Differential Amplifier in Cascode Configuration

Circuit:



Output:

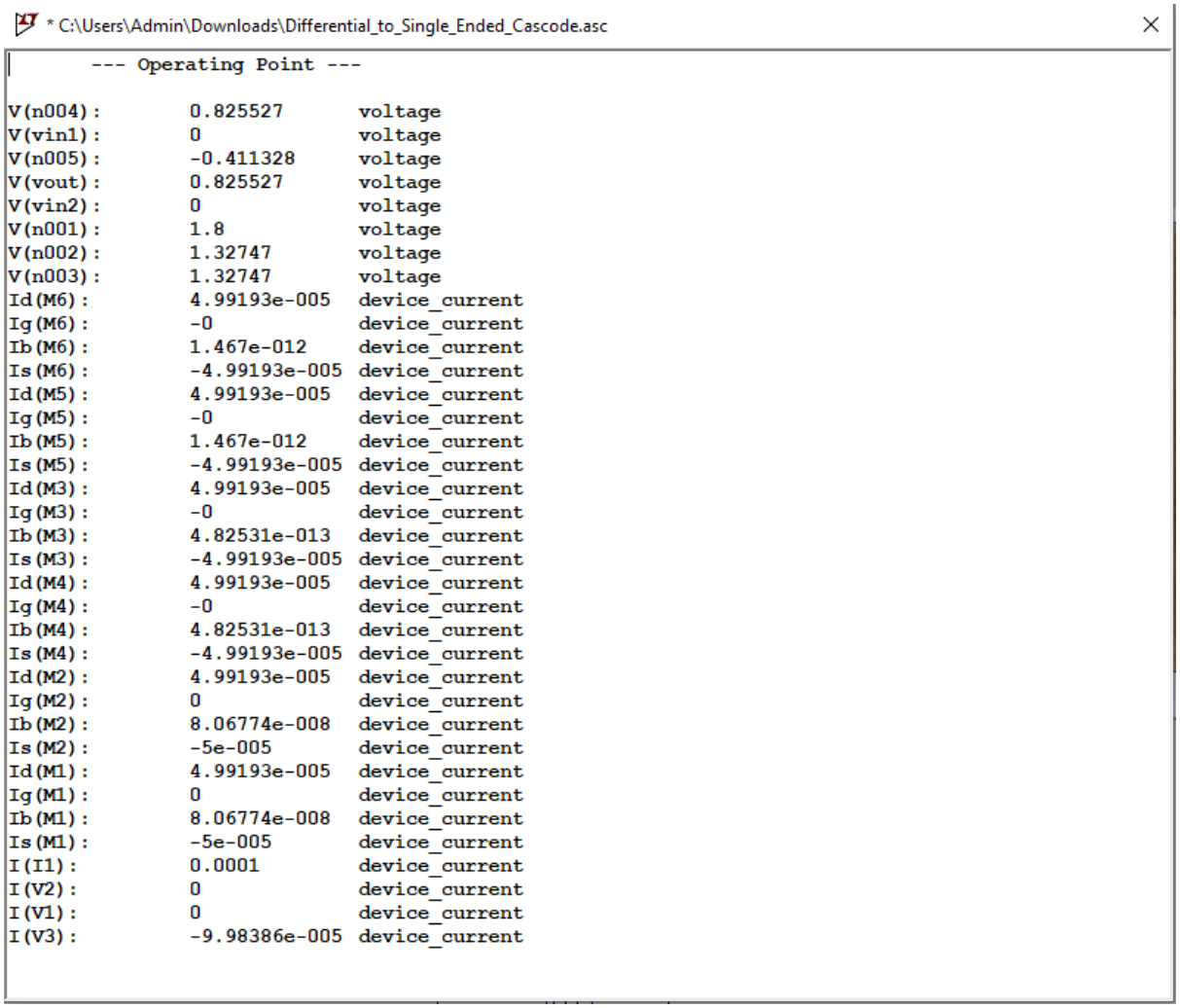


Peak to Peak Vin1 – Vin2 = 200 mV

Peak to Peak Vout = 814.058 – (-1133.628) = 1947.686 mV

Gain = 1947.686/200 = 9.738

Operating Bias Point Windows Solution:



RESULTS:

Outputs of Single Ended Differential Amplifier and Single Ended Differential Amplifier in Cascode Configuration, were studied, simulated, plotted and observed. The results were similar to what was expected theoretically with minor errors.

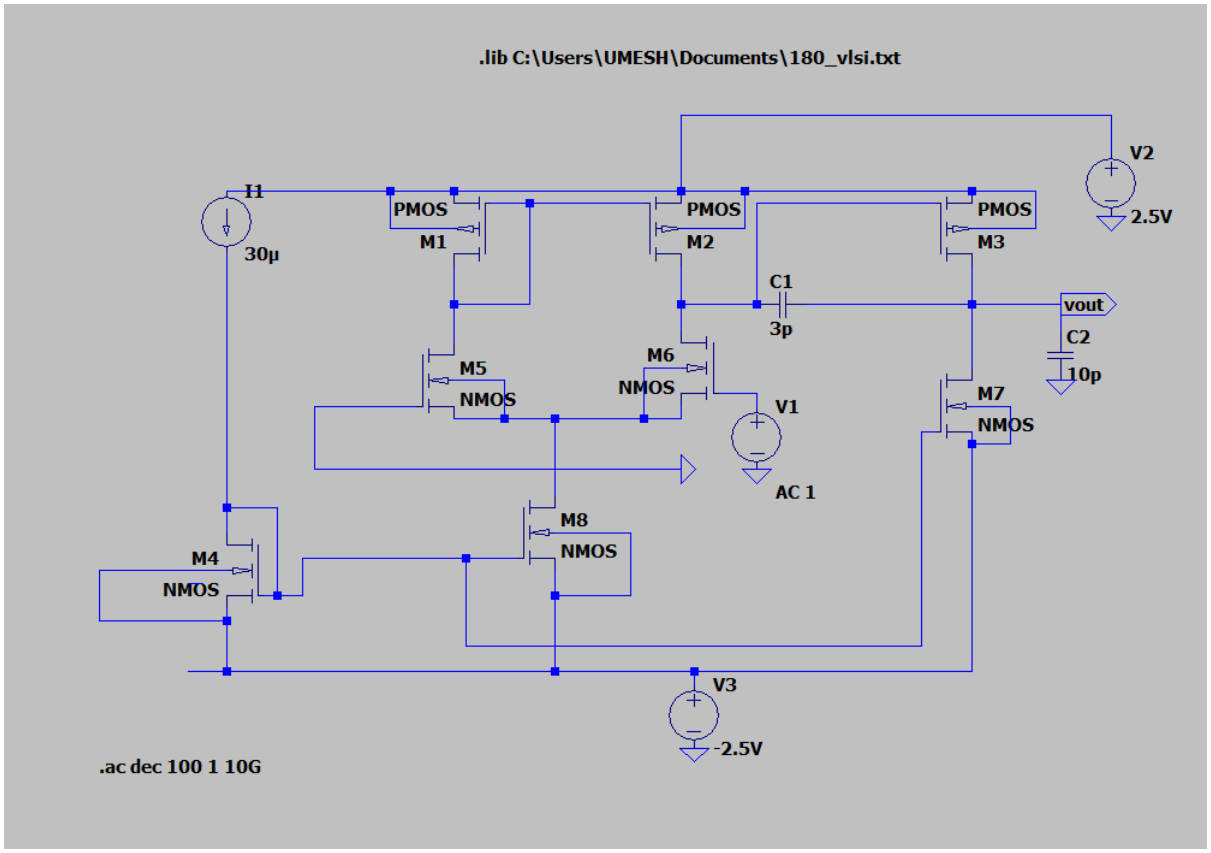
PRECAUTIONS AND SOURCES OF ERROR:

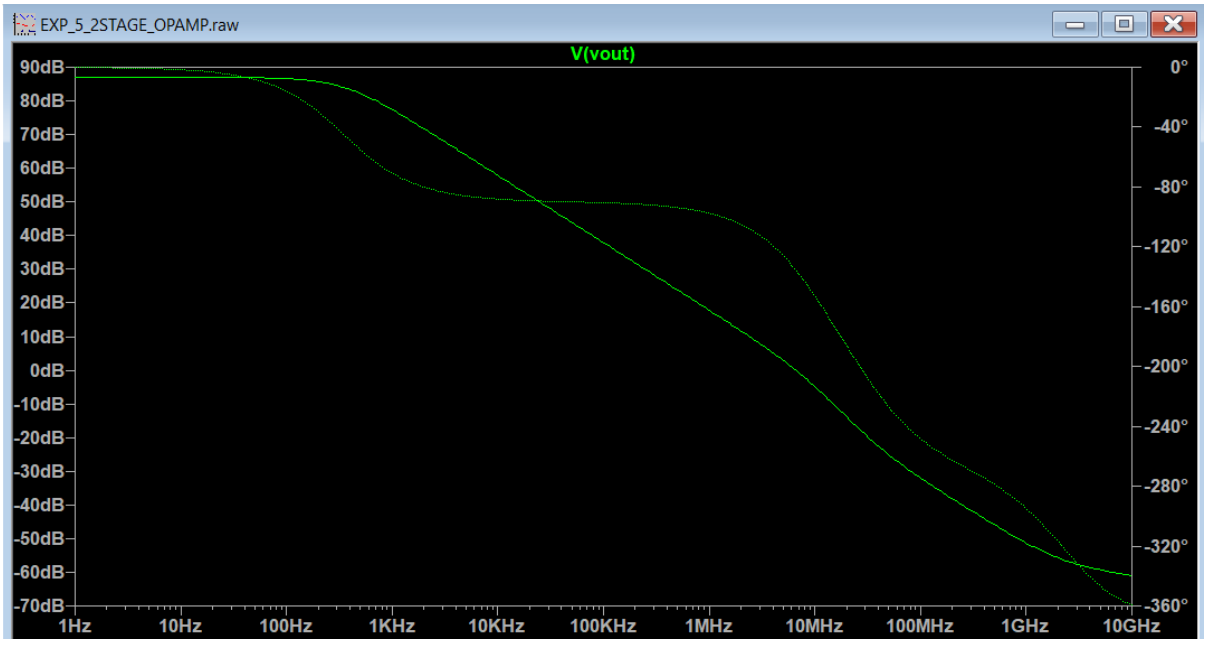
1. Code should be correct.
2. The correct elements should be used.
3. Values should be defined as used in the experiment.
4. Incorrect values and parameters of MOSFETs can lead to incorrect results.

NAME:UMESH

2018UEC2030

AIM: 2 STAGE OPAMP **EXPERIMENT:5**





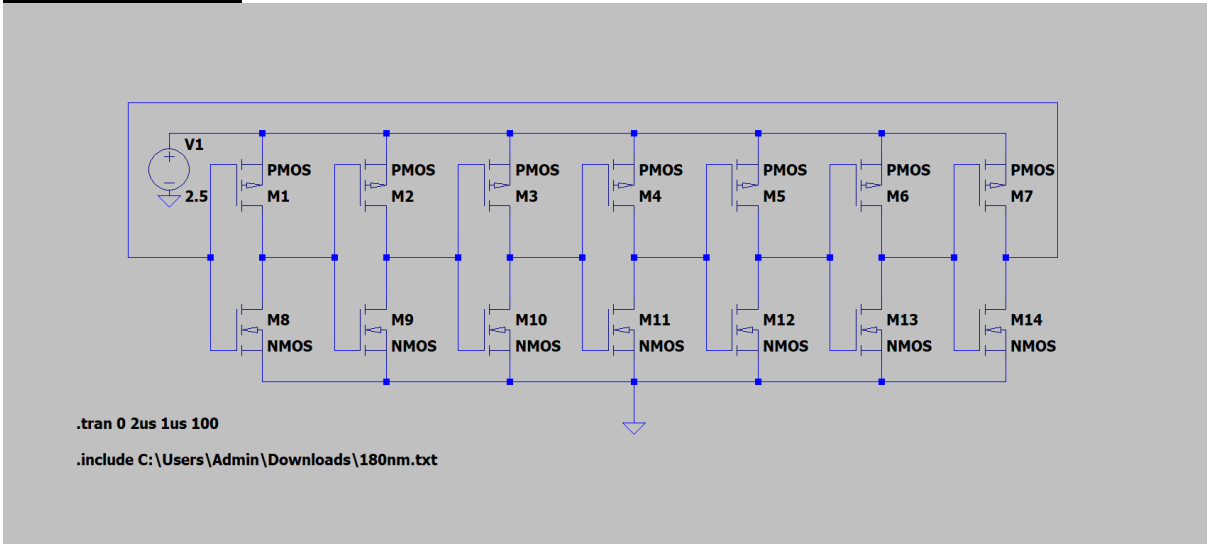
Name: UMESH
Date: 05/04/2021
Roll No: 2018UEC2030
Branch/Sec: ECE-1

Experiment-6

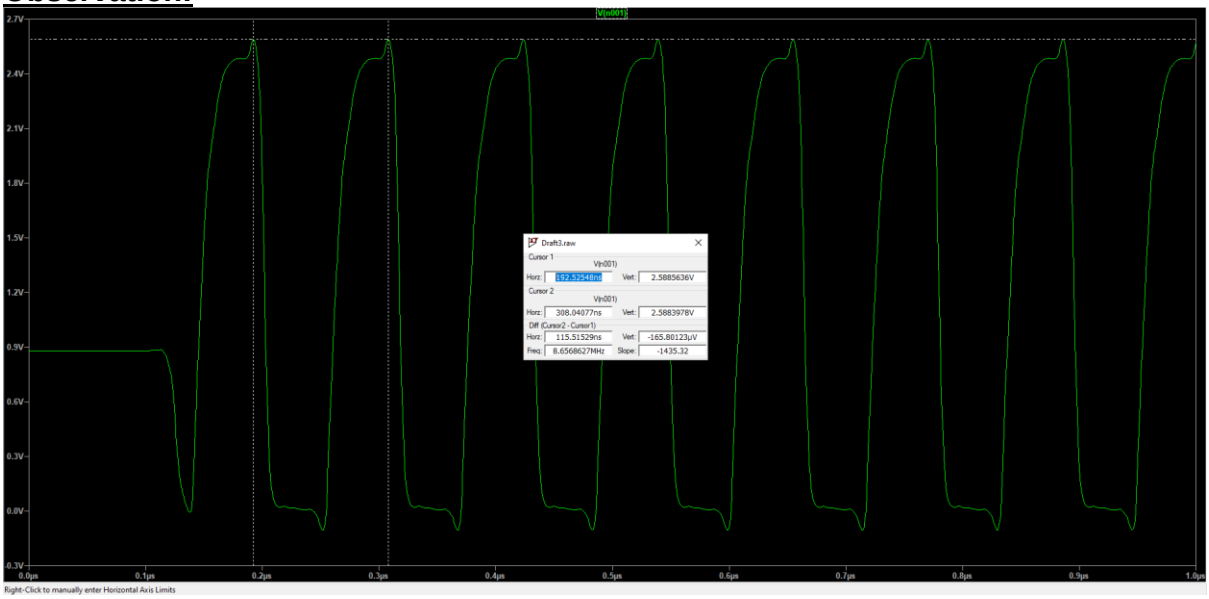
Aim of the experiment:

To Study, Simulate, Plot and Observe output of CMOS Invertor Based Oscillator Configuration.

Circuit Diagram:



Observation:

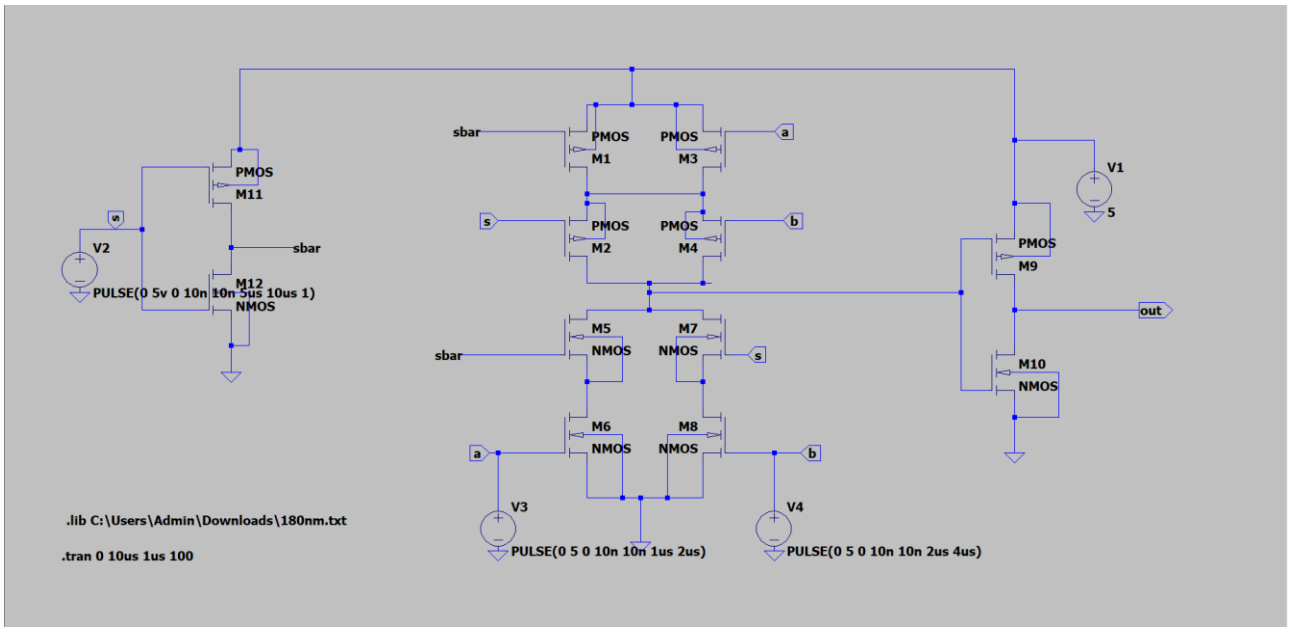


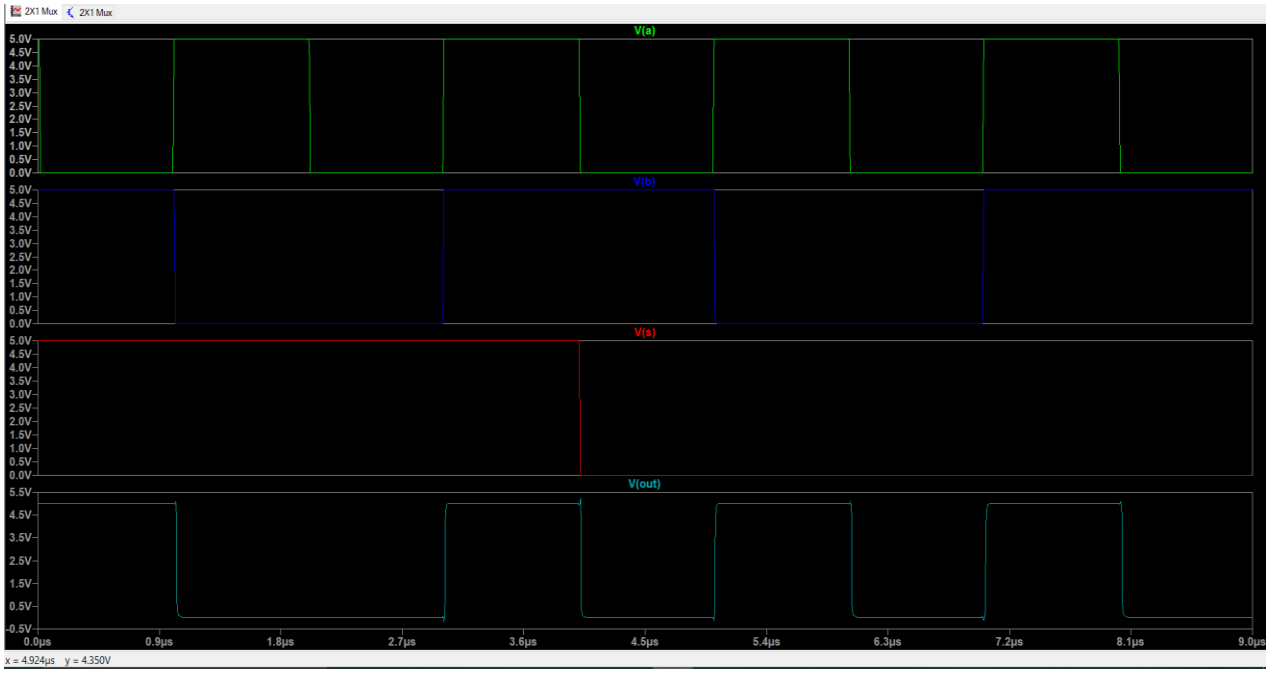
Results: Output of CMOS Invertor based Oscillator was studied, simulated, plotted and observed. The results were similar to what was expected theoretically with minor errors.

EXPERIMENT-7

Name: UMESH
Roll No: 2018UEC2030

AIM: To implement 2X1 MUX using CMOS Logic

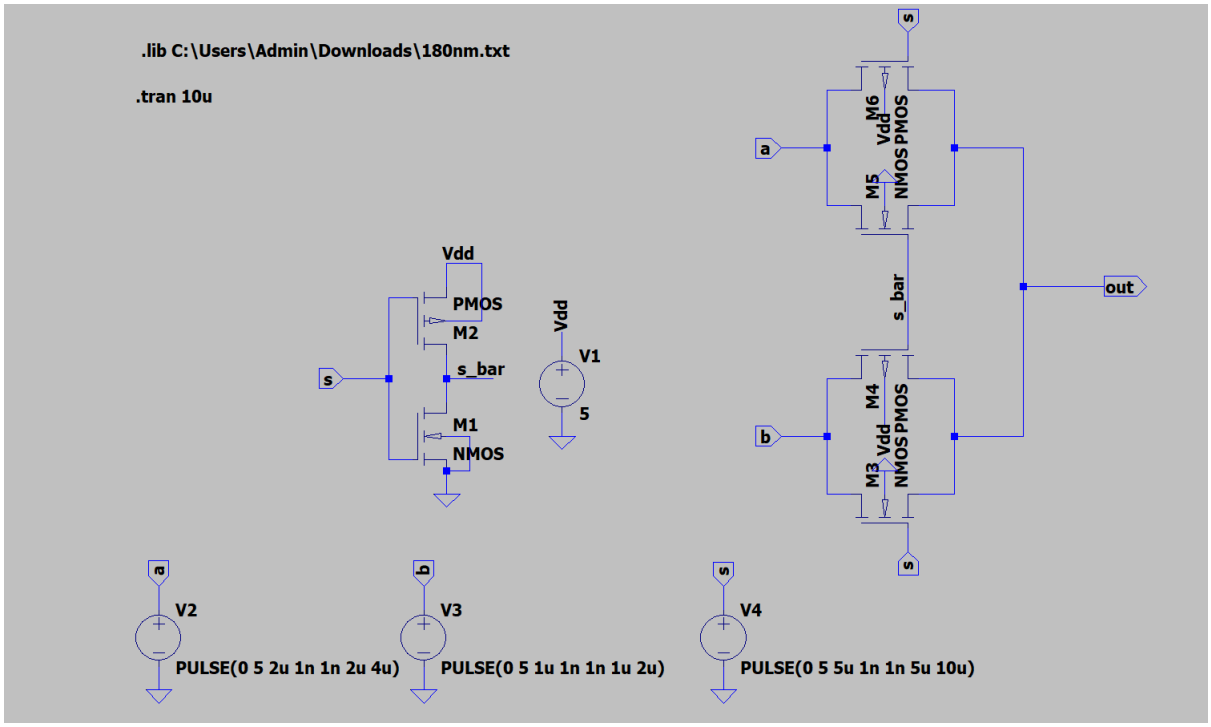


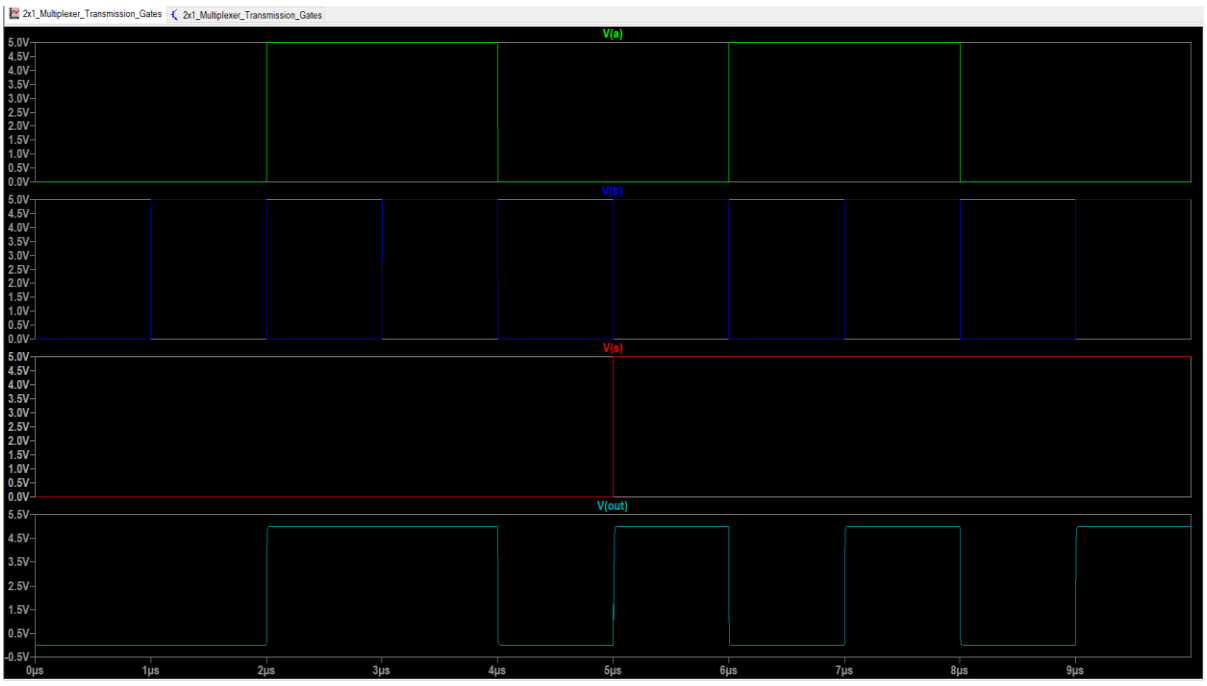


EXPERIMENT-8

Name: Umesh
Roll no: 2018UEC2030

AIM: 2X1 MUX using Transmission Gate





Experiment-9

Name: Umesh

Roll no: 2018UEC2030

AIM: 3 input XOR