

Experiment No.:
Title: DC analysis of MOSFET amplifier.

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM: -To design, build single stage CS amplifier & verify dc operating point.

APPARATUS/REQUIREMENTS: -

For Hardware Experiment:

Sr. No.	Description	Specification	Quantity
1.	E-MOSFET	2N7000	1
2.	DMM	--	4
3.	Resistor	1k, 15k	4
4.	Connecting Wires	--	--
5.	Power Supply	0-30V	1

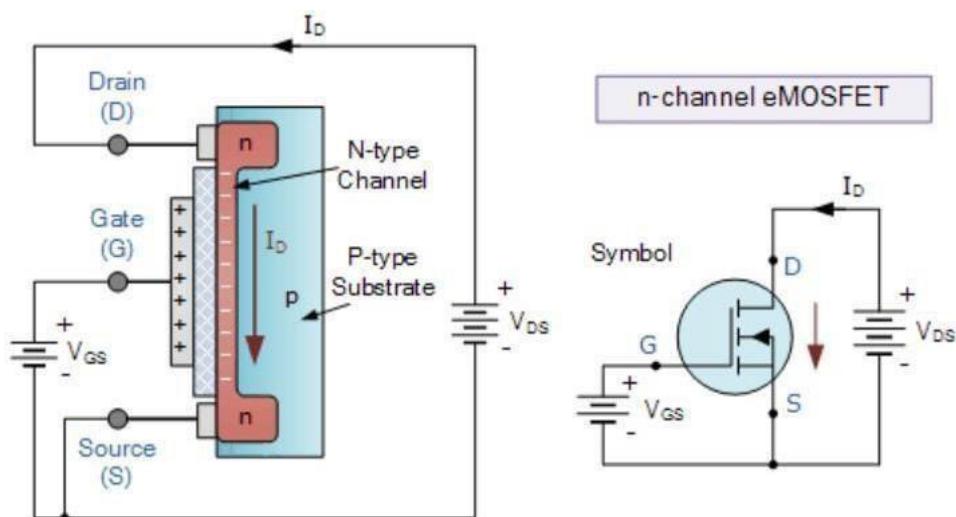
For Software Experiment:

Sr. No.	Description	Specifications	Quantity
1.	Personal Computer	With Windows OS. P4 or advanced processor	1
2.	Multisim Software	--	1

THEORY:-

Metal Oxide Semiconductor Field Effect Transistor, or MOSFET for short, is an excellent choice for small signal linear amplifiers as their input impedance is extremely high making them easy to bias. But for a MOSFET to produce linear amplification, it has to operate in its saturation region, unlike the Bipolar Junction Transistor. But just like the BJT, it too needs to be biased around a centrally fixed Q-point.

MOSFETS conduct through a conductive region or path called “the channel”. We can make this conductive channel wider or smaller by applying a suitable gate potential. An electric field induced around the gate terminal by the application of this gate voltage affects the electrical characteristics of the channel, thus the name *field-effect transistor*.



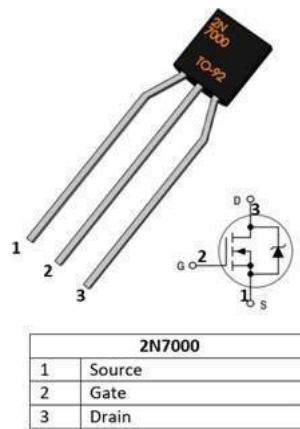
We can see that for the n-channel MOSFET (NMOS) above the substrate semiconductor material is *p-type*, while the source and drain electrodes are *n-type*. The supply voltage will be positive. Biasing the gate terminal positive attracts electrons within the p-type semiconductor substrate under the gate region towards it.

This overabundance of free electrons within the p-type substrate causes a conductive channel to appear or grow as the electrical properties of the p-type region invert, effectively changing the p-type substrate into a n-type material allowing channel current to flow.

The reverse is also true for the p-channel MOSFET (PMOS), where a negative gate potential causes a build of holes under the gate region as they are attracted to the electrons on the outer side of the metal gate electrode. The result is that the n-type substrate creates a p-type conductive channel.

So for our n-type MOS transistor, the more positive potential we put on the gate the greater the build-up of electrons around the gate region and the wider the conductive channel becomes. This enhances the electron flow through the channel allowing more channel current to flow from drain to source leading to the name of **Enhancement MOSFET**.

Pin Configuration of 2N7000 MOSFET



DC Biasing the MOSFET

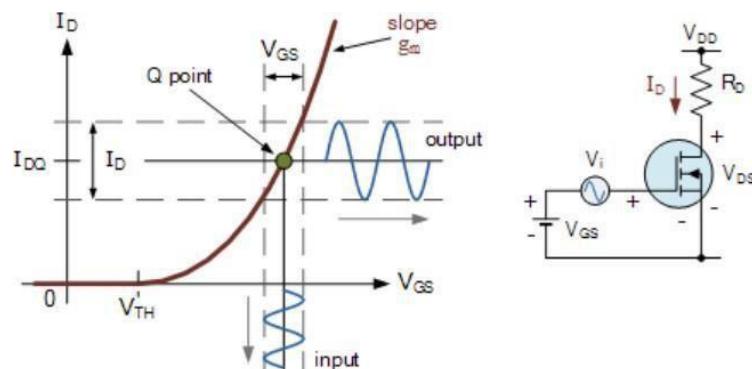
The universal voltage divider biasing circuit is a popular biasing technique used to establish a desired DC operating condition of bipolar transistor amplifiers as well as MOSFET amplifiers. The advantage of the voltage divider biasing network is that the MOSFET, or indeed a bipolar transistor, can be biased from a single DC supply. But first we need to know where to bias the gate for our MOSFET amplifier.

A MOSFET device has three different regions of operation. These regions are called the: *Ohmic/Triode region*, *Saturation/Linear region* and *Pinch-off point*. For a MOSFET to operate as a linear amplifier, we need to establish a well-defined quiescent operating point, or Q-point, so it must be biased to operate in its saturation region. The Q-point for the MOSFET is represented by the DC values, I_D and V_{GS} that position the operating point centrally on the MOSFETs output characteristics curve.

As we have seen above, the saturation region begins when V_{GS} is above the V_{TH} threshold level. Therefore, if we apply a small AC signal which is superimposed on to this DC bias at the gate input, then the MOSFET will act as a linear amplifier as shown.

The common-source NMOS circuit above shows that the sinusoidal input voltage, V_i is in series with a DC source. This DC gate voltage will be set by the bias circuit. Then the total gate-source voltage will be the sum of V_{GS} and V_i .

The DC characteristics and therefore Q-point (quiescent point) are all functions of gate voltage V_{GS} , supply voltage V_{DD} and load resistance R_D .



The MOS transistor is biased within the saturation region to establish the desired drain current which will define the transistors Q-point. As the instantaneous value of V_{GS} increases, the bias point moves up the curve as shown allowing a larger drain current to flow as V_{DS} decreases.

This simple enhancement-mode common source MOSFET amplifier configuration uses a single supply at the drain and generates the required gate voltage, V_G using a resistor divider. We remember that for a MOSFET, no current flows into the gate terminal and from this we can make the following basic assumptions about the MOSFET amplifiers DC operating conditions.

$$\begin{aligned} V_{DD} &= I_D R_D + V_{DS} + I_D R_S \\ &= I_D (R_D + R_S) + V_{DS} \end{aligned}$$

$$\therefore R_D + R_S = \frac{V_{DD} - V_{DS}}{I_D}$$

Then from this we can say that:

$$R_D = \frac{V_{DD} - V_D}{I_D} \quad \text{and} \quad R_S = \frac{V_S}{I_D}$$

And the MOSFETs gate-to-source voltage, V_{GS} is given as:

$$V_{GS} = V_G - I_S R_S$$

And;

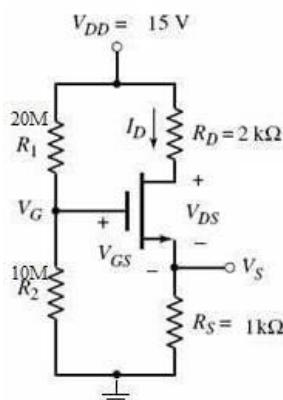
$$I_D = k(V_{GS} - V_{TH})^2$$

As we have seen above, for proper operation of the MOSFET, this gate-source voltage must be greater than the threshold voltage of the MOSFET, that is $V_{GS} > V_{TH}$. Since $I_S = I_D$, the gate voltage, V_G is therefore equal too:

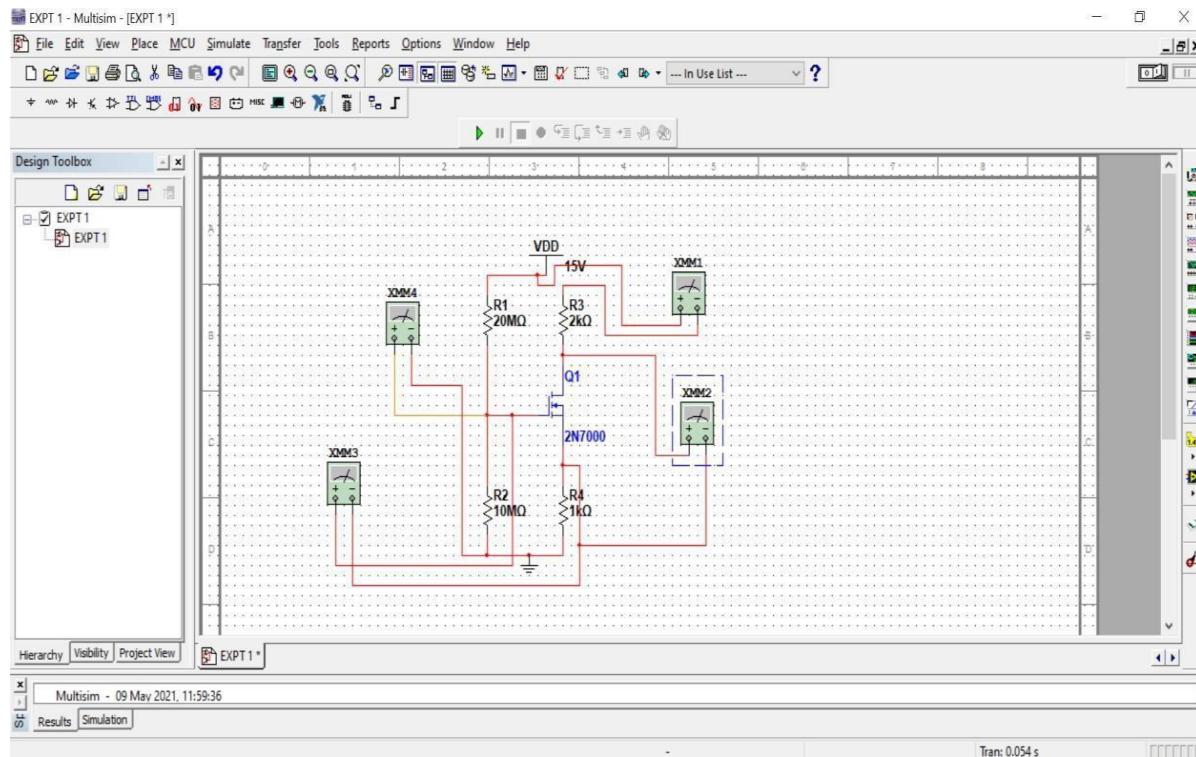
MOSFET Amplifier Gate Bias Voltage

$$V_G = V_{DD} \left(\frac{R_2}{R_1 + R_2} \right)$$

CIRCUIT DIAGRAM:



CIRCUIT DIAGRAM /SIMULATION:



PROCEDURE:-

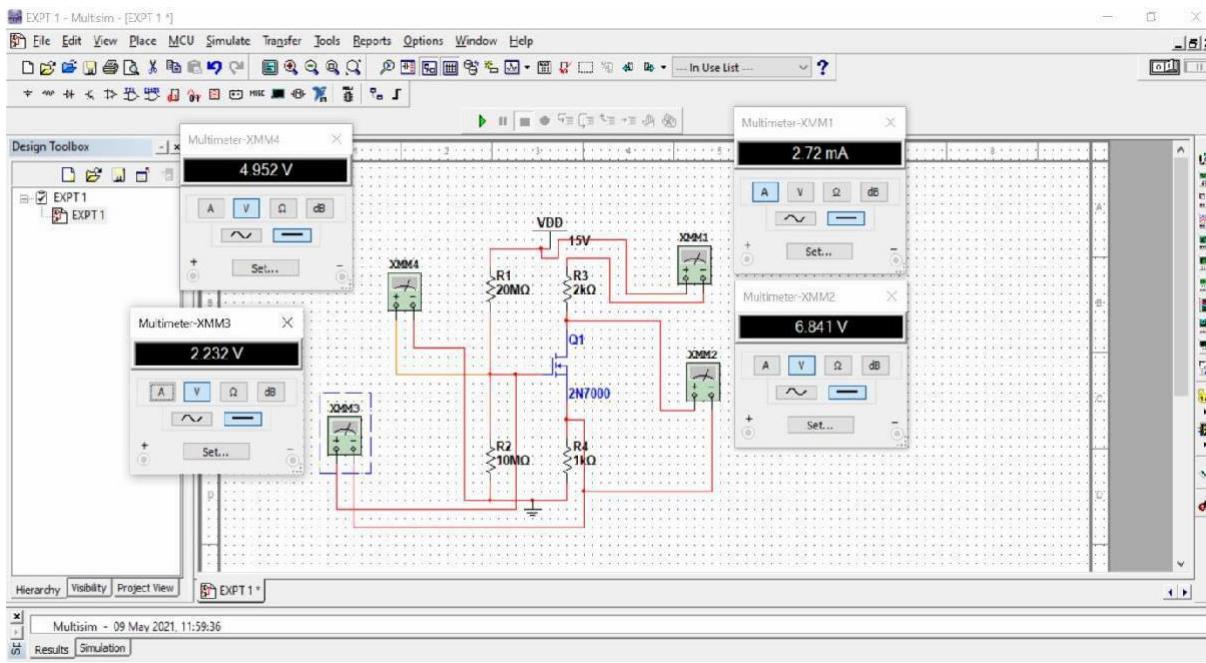
For Hardware Experiment:

- Make Connections as per the circuit diagram.
- VDD supply is given to drain terminal of MOSFET.
- Measure drain current ID using milli-ammeter and VDS using voltmeter across drain and source terminals of MOSFET.
- Compare theoretical and practical values of ID and VDS.

For Software Experiment:

- Start PC and Open Multisim Software.
- Go to file menu and open new file and draw the circuit diagram (Program) and save it.
- Go to simulate menu and run the program.
- If any errors correct them.
- Observe the input and output waveforms by double clicking XMMs.

OBSERVATIONS:-



- Observed values of ID=2.72 mA and VDS=6.841V.

CALCULATIONS:-

Sample Calculation:

$$VG = VDD \left(\frac{R2}{R1+R2} \right) = 15 \left(\frac{10}{30} \right) = 5V.$$

Likewise, all the values of currents and voltages can be calculated using above formulae.

RESULT:-

Sr. No.	Practical Values	Theoretical Values
ID		
VDS		
VGS		
VG		

CONCLUSION:-

Experiment No.:
Title: AC analysis of MOSFET amplifier.

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM: -To build & test single stage CS amplifier, plot frequency response. Calculate Av, Ri, Ro & bandwidth

APPARATUS/REQUIREMENTS: -

Sr. No.	Description	Specifications	Quantity
1.	Personal Computer	With Windows OS. P4 or advanced processor	1
2.	Multisim Software	--	1

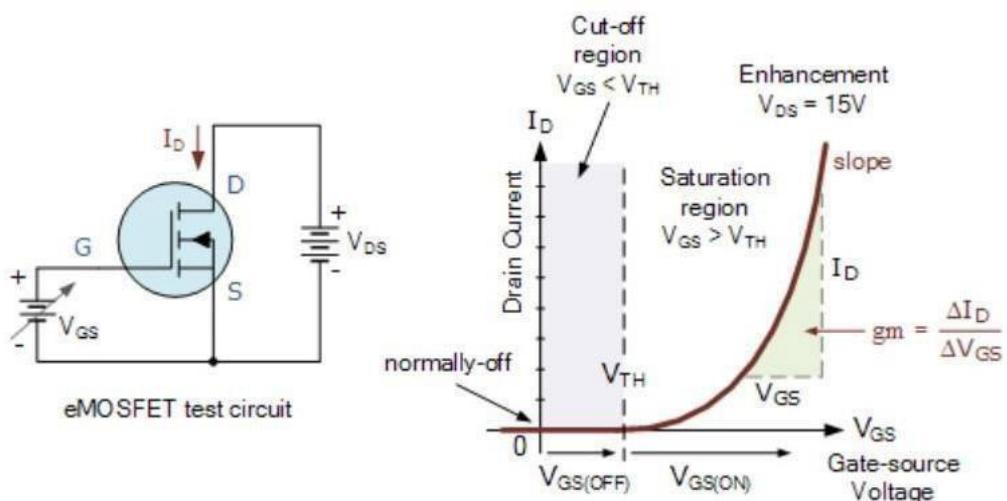
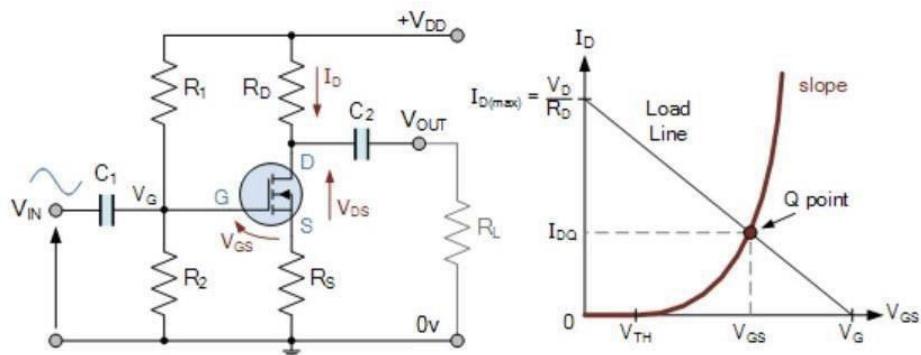
THEORY:-

Basic Common Source MOSFET Amplifier

If we apply a small time-varying signal to the input, then under the right circumstances the mosfet circuit can act as a linear amplifier providing the transistors Q-point is somewhere near the center of the saturation region, and the input signal is small enough for the output to remain linear. Consider the basic MOSFET amplifier circuit below.

With a fixed V_{DS} drain-source voltage connected across the eMOSFET we can plot the values of drain current, I_D with varying values of V_{GS} to obtain a graph of the mosfets forward DC characteristics. These characteristics give the transconductance, g_m of the transistor.

This transconductance relates the output current to the input voltage representing the gain of the transistor. The slope of the transconductance curve at any point along it is therefore given as: $g_m = I_D/V_{GS}$ for a constant value of V_{DS} .



$$gm = \frac{\Delta I_D}{\Delta V_{GS}}$$

This ratio is called the transistors static or DC transconductance which is short for “transfer conductance” and is given the unit of Siemens (S), as its amps per volt. Voltage gain of a mosfet amplifier is directly proportional to the transconductance and to the value of the drain resistor.

The main goal of a MOSFET amplifier, or any amplifier for that matter, is to produce an output signal that is a faithful reproduction of its input signal but amplified in magnitude. This input signal could be a current or a voltage, but for a mosfet device to operate as an amplifier it must be biased to operate within its saturation region.

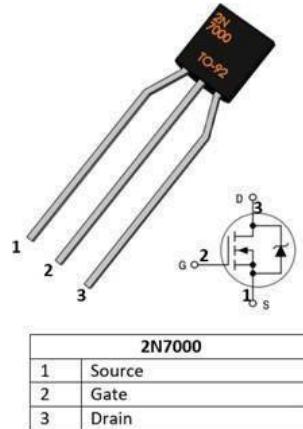
There are two basic types of enhancement-mode MOSFETs, n-channel and p-channel and in this mosfet amplifier tutorial we have looked at the n-channel enhancement MOSFET is often referred to as an NMOS, as it can be operated with positive gate and drain voltages relative to the source as opposed to the p-channel PMOS which is operated with negative gate and drain voltages relative to the source.

The saturation region of a MOSFET device is its constant-current region above its threshold voltage, V_{TH} . Once correctly biased in the saturation region the drain current, I_D varies as a result of the gate-to-source voltage, V_{GS} and not by the drain-to-source voltage, V_{DS} since the drain current is called saturated.

In an enhancement-mode MOSFET, the electrostatic field created by the application of a gate voltage enhances the conductivity of the channel, rather than deplete the channel as in the case of a depletion-mode MOSFET.

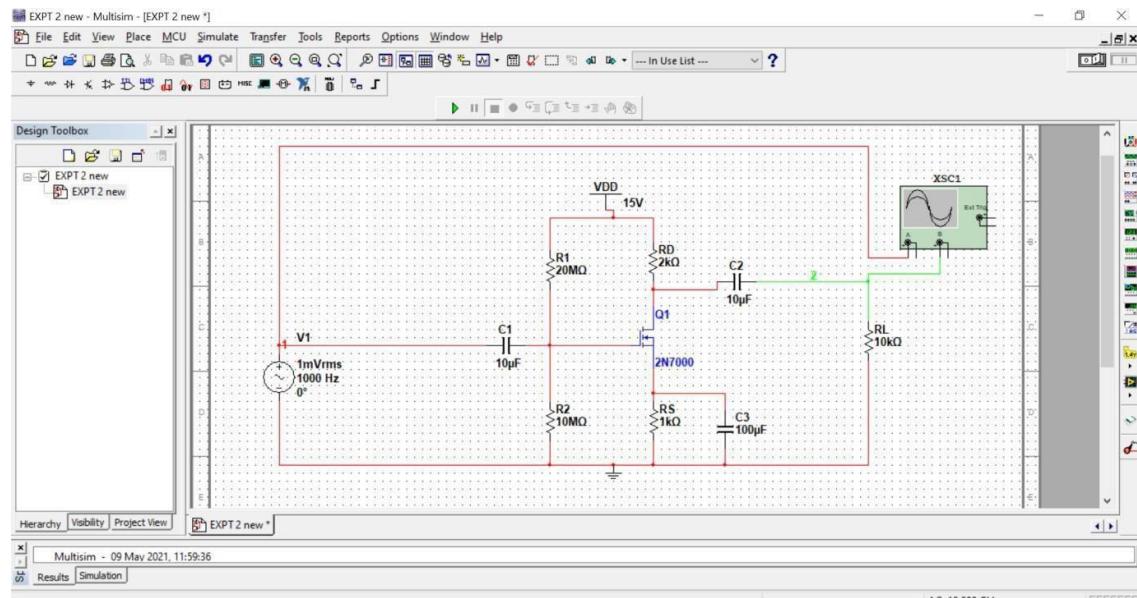
The threshold voltage is the minimum gate bias required to enable the formation of the channel between the source and the drain. Above this value the drain current increases in proportion to $(V_{GS} - V_{TH})^2$ in the saturation region allowing it to operate as an amplifier.

Pin Configuration of 2N7000 MOSFET

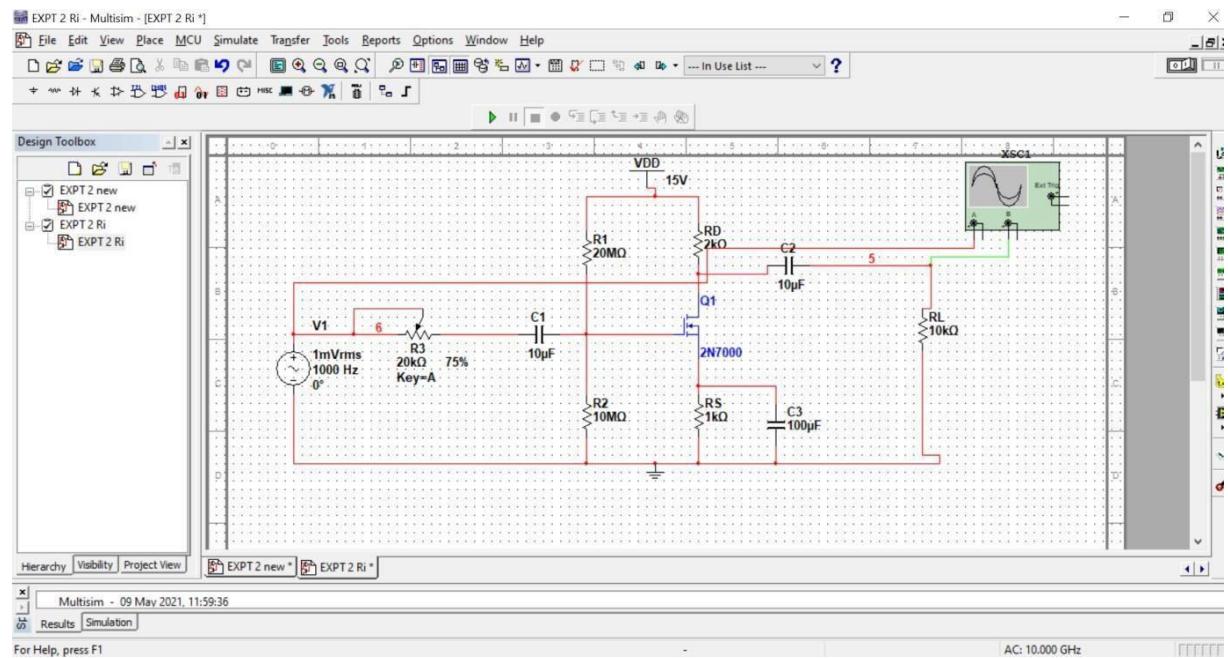


CIRCUIT DIAGRAM /SIMULATION:

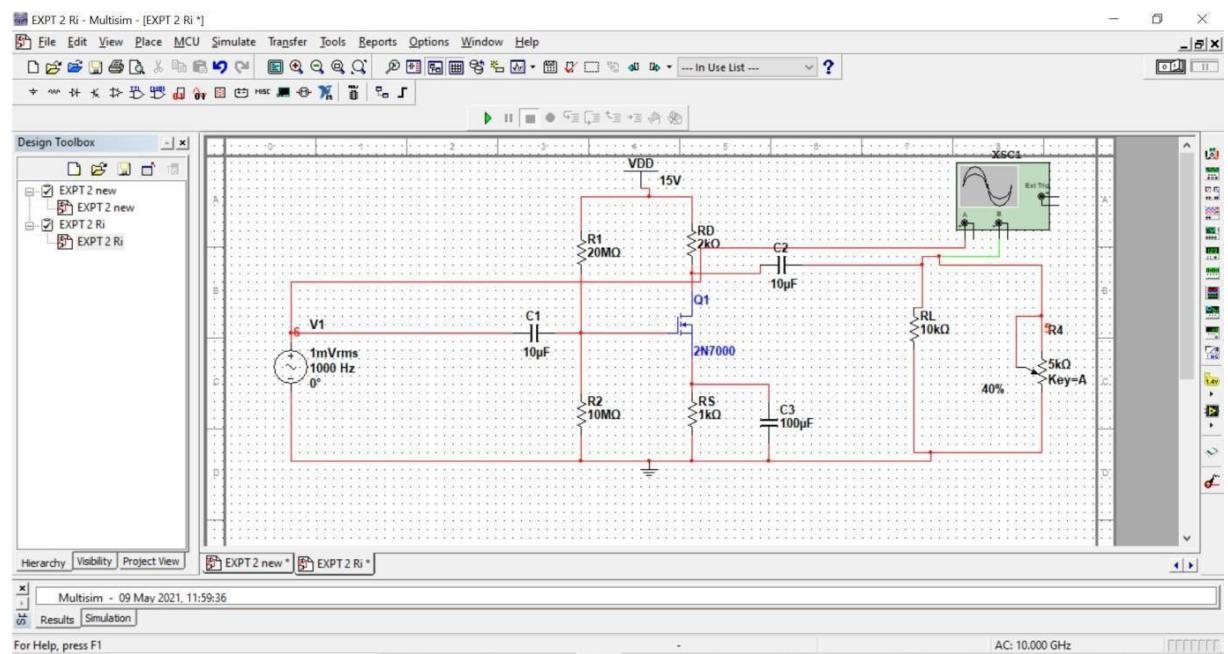
A. Frequency Response



B. Calculation of R_i



C. Calculation of R_o



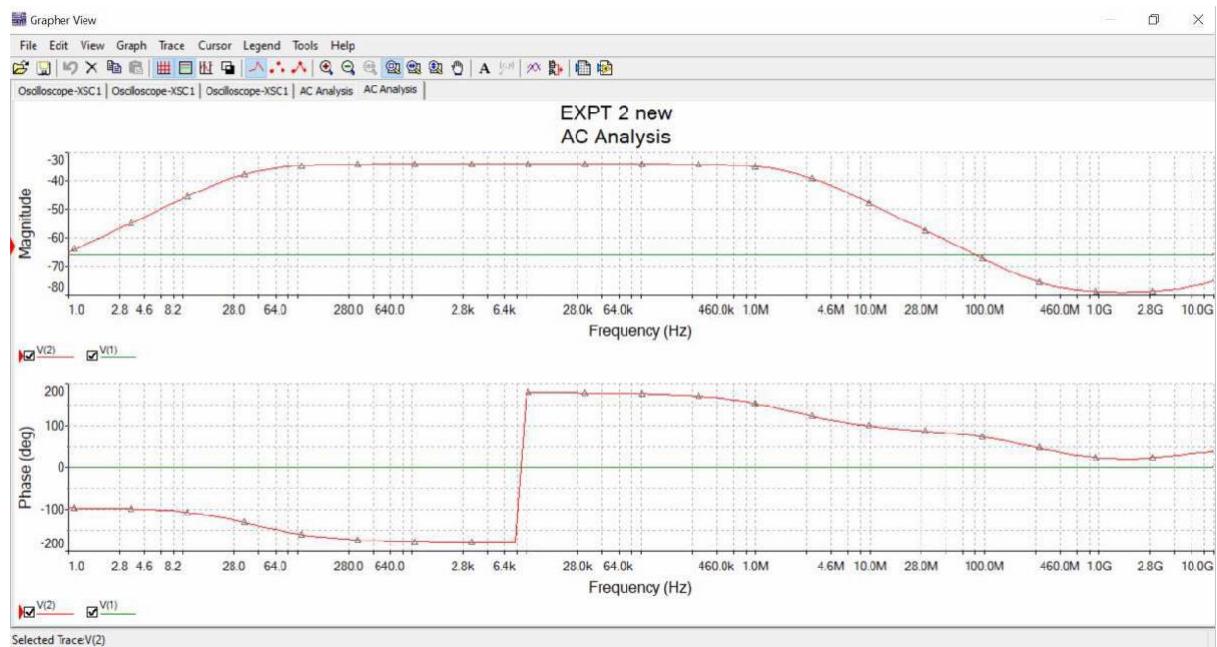
PROCEDURE:-

- Start PC and Open Multisim Software.
- Go to file menu and open new file and draw the circuit diagram (Program) and save it.
- Go to simulate menu and select Analyses in that select AC analysis select decibel scale and select parameters i.e input and output voltages. We will get frequency response. From that we can find bandwidth

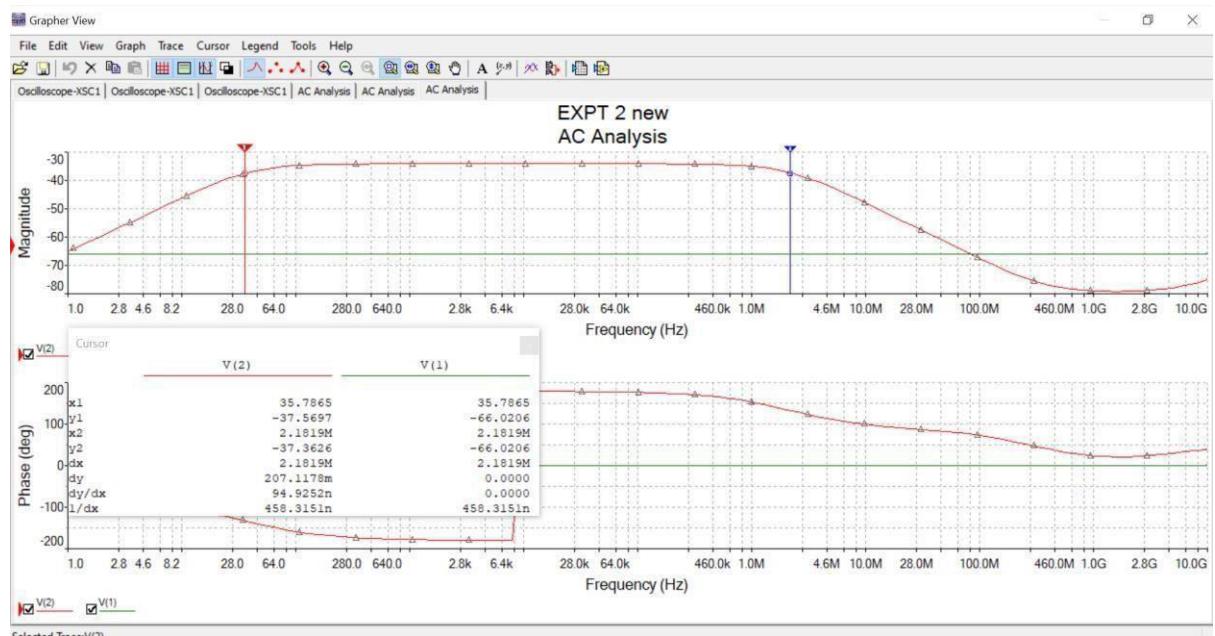
- To find R_{in} place one pot in series with input capacitor.
- To find R_o place one pot across load.

OBSERVATIONS: -

A. Frequency Response:



B. Bandwidth:



$$F_l = 35.7 \text{ Hz}$$

$$F_h \text{ is } 2.18 \text{ MHz}$$

$$\text{Band width} = \text{BW} = F_h - F_l = 2.18 \text{ MHz}$$

CALCULATIONS:-

- Band width= BW = $F_h - F_l = 2.18\text{MHz}$.
- Gain = $V_o / V_{in} = 78.68$
- $R_i = 4\text{Mohm}$
- $R_o = 3\text{kohm}$

RESULT:-

Sr. No.	Parameter	Practical Value	Theoretical value
1	A_v		
2	R_{in}		
3	R_o		
4	BW		

CONCLUSION:-

Experiment No.:
Title: Adjustable voltage regulator

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM:- Design and implement an adjustable voltage regulator using three terminal voltage regulator IC.

APPARATUS/REQUIREMENTS: -

Sr. No.	Description	Specification	Quantity
1.	3-terminal Voltage Regulator IC LM317	Output 1.25-37V	1
2.	DMM	--	2
3.	Capacitors	0.1uF, 10uF	2
4.	Resistor (R1)	240ohm,	1
5.	Connecting Wires	--	-
6.	Power Supply	0-30V	1
7	POT (R2)	10kohm	1

THEORY:-

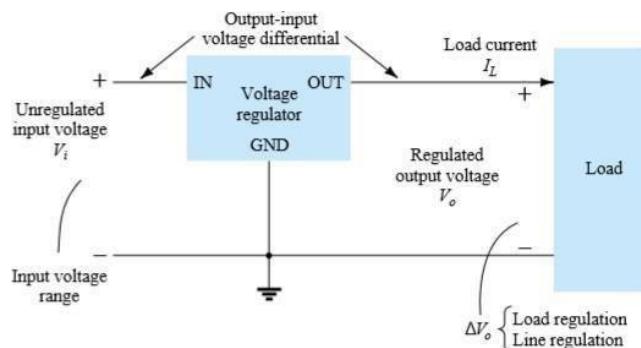
IC VOLTAGE REGULATORS

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an

adjustable set voltage. A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to desired amplitude, then rectifying that ac voltage, filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli-amperes to tens of amperes, corresponding to power ratings from milli-watts to tens of watts.

Three-Terminal Voltage Regulators

Figure shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage, V_i , applied to one input terminal, a regulated output dc voltage, V_o , from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).



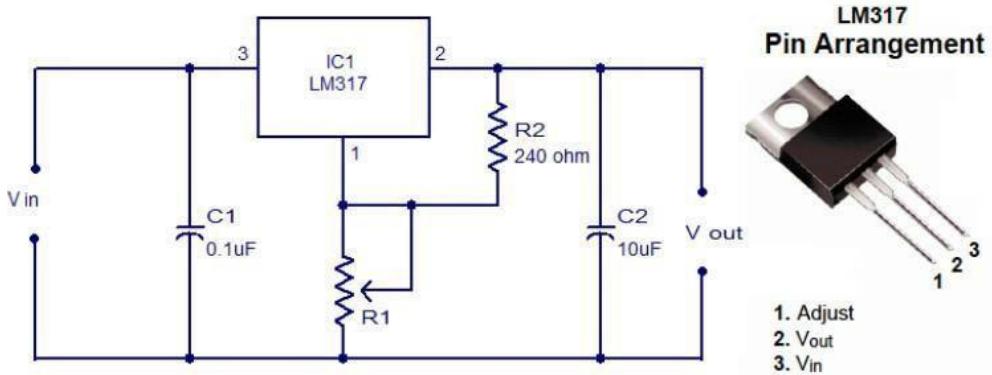
Adjustable Positive Voltage Regulators

Voltage regulators are also available in circuit configurations that allow the user to set the output voltage to a desired regulated value. The LM317, for example, can be operated with the output voltage regulated at any setting over the range of voltage from +1.2 to +37 V. Maximum unregulated permissible input voltage to these regulators IC is provided by the manufacturer in data sheets (Mostly this value is 57V_{DC}). In this regulator, minimum input unregulated DC voltage required is minimum 2 to 3Volts greater than the desired output regulated voltage. Figure shows how the regulated output voltage of an LM317 can be set. Resistors R_1 and R_2 set the output to any desired voltage over the adjustment range (1.2 to 37 V). The output voltage desired can be calculated using typically $R_1=240\Omega$ by following equation-

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{adj} R_2$$

with typical IC values of

$$V_{ref} = 1.25 \text{ V} \quad \text{and} \quad I_{adj} = 100 \mu\text{A}$$



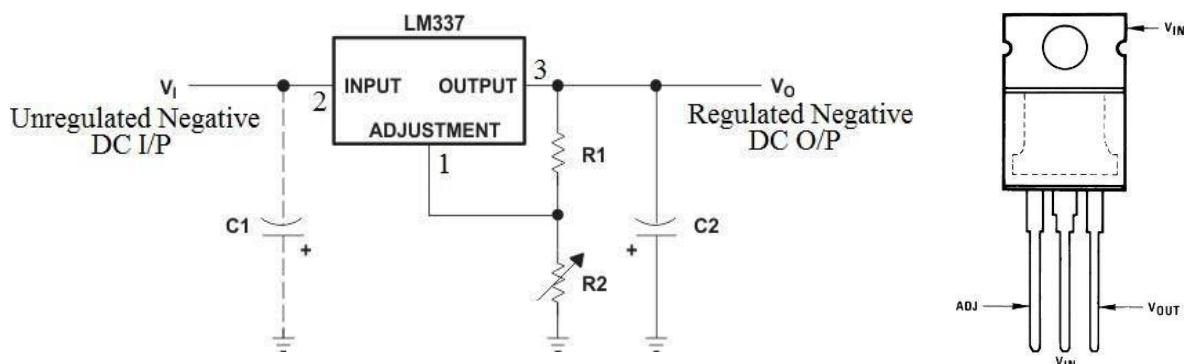
Adjustable Negative Voltage Regulators

Voltage regulators are also available in circuit configurations that allow the user to set the output voltage to a desired negative regulated value. The LM337, for example, can be operated with the output voltage regulated at any setting over the range of voltage from -1.2 to -37 V. Maximum unregulated permissible input voltage to these regulators IC is provided by the manufacturer in data sheets (Mostly this value is -57V_{DC}). In this regulator, minimum input unregulated DC voltage required is minimum -2 to -3Volts greater than the desired output regulated voltage. Figure shows how the regulated output voltage of an LM337 can be set. Resistors \$R_1\$ and \$R_2\$ set the output to any desired voltage over the adjustment range (-1.2 to -37 V). The output voltage desired can be calculated using typically \$R_1 = 240\Omega\$ by following equation-

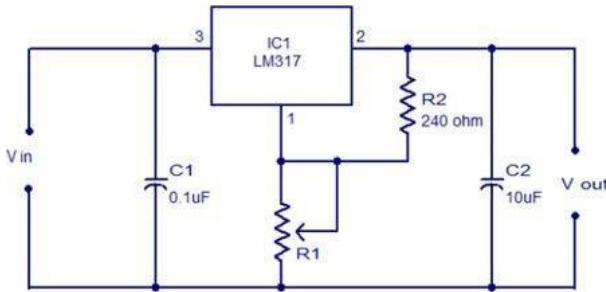
$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{adj} R_2$$

with typical IC values of

$$V_{ref} = 1.25 \text{ V} \quad \text{and} \quad I_{adj} = 100 \text{ } \mu\text{A}$$



CIRCUIT DIAGRAM:-



PROCEDURE:-

- Make Connections as per the circuit diagram.
- Input supply is given to pin no. 3 of IC 317.
- By adjusting the value of R₂, output is measured at pin no. 2.
- This measured output is compared with required output.

OBSERVATIONS:-

- Output voltage varies with value of R₂.
- Output voltages are always less than input voltage by 1.5-2.5V.
- When R₂ = 5kohm, Vin =30V then Vo=26.9V.

CALCULATIONS:-

If we keep R₂ at 5kohm and calculate value of output voltage is

$$V_o = V_{ref} [1 + R_2 / R_1] + I_{adj} R_2$$

$$V_{ref} = 1.25V$$

$$R_1 = 240\text{ ohm}$$

$$R_2 = 5\text{kohm}$$

$$I_{adj} = 100\mu\text{A}$$

Then

$$V_o = 1.25 [1 + 5000/240] + 100\mu\text{A} * 5000$$

$$V_o = 1.25 [1 + 20.833] + 0.5 = 27.8V$$

RESULT:-

Theoretical Value of output voltage is 27.8V and Practical value is 26.9V

CONCLUSION:-

We have implemented adjustable voltage regulator using ICL317. And calculated practical value of output voltage and theoretical value of output voltage and compared them. Hence by changing value of R₂ we can vary output voltage hence we can call this circuit as adjustable voltage regulator.

Experiment No.:

Title: Wein bridge oscillator.

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM:-To implement Wein bridge oscillator using OPAMP.

APPARATUS/REQUIREMENTS: -

Sr. No.	Description	Specifications	Quantity
1.	Personal Computer	With Windows OS. P4 or advanced processor	1
2.	Multisim Software	--	1

THEORY:-

A Wien-Bridge Oscillator is a type of phase-shift oscillator which is based upon a Wien-Bridge network (Figure 1a) comprising of four arms connected in a bridge fashion. Here two arms are purely resistive while the other two arms are a combination of resistors and capacitors. In particular, one arm has resistor and capacitor connected in series (R_1 and C_1) while the other has them in parallel (R_2 and C_2). This indicates that these two arms of the network behave identical to that of high pass filter or low pass filter, mimicking the behavior of the circuit shown by Figure1.

In this circuit, at high frequencies, the reactance of the capacitors C_1 and C_2 will be much less due to which the voltage V_0 will become zero as R_2 will be shorted. Next, at low frequencies, the reactance of the capacitors C_1 and C_2 will become very high.

However even in this case, the output voltage V_0 will remain at zero only, as the capacitor C_1 would be acting as an open circuit. This kind of behavior exhibited by the Wien-Bridge network makes it a lead-lag circuit in the case of low and high frequencies, respectively.

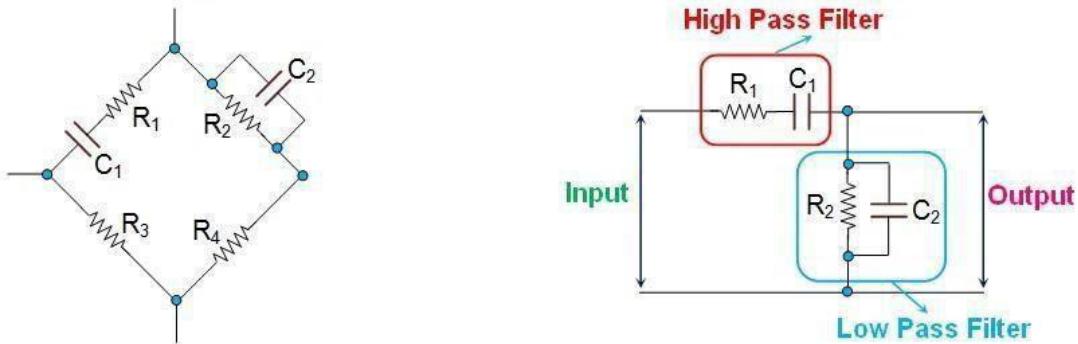


Figure 1 (a) Wien-Bridge Network (b) Two arms of the Wien-Bridge Network

Wien Bridge Oscillator Frequency Calculation

$$f_r = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

if $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$\text{then } f_r = \frac{1}{2\pi RC}$$

Further, at this frequency, the phase-shift between the input and the output will become zero and the magnitude of the output voltage will become equal to one-third of the input value. In addition, it is seen that the Wien-Bridge will be balanced only at this particular frequency.

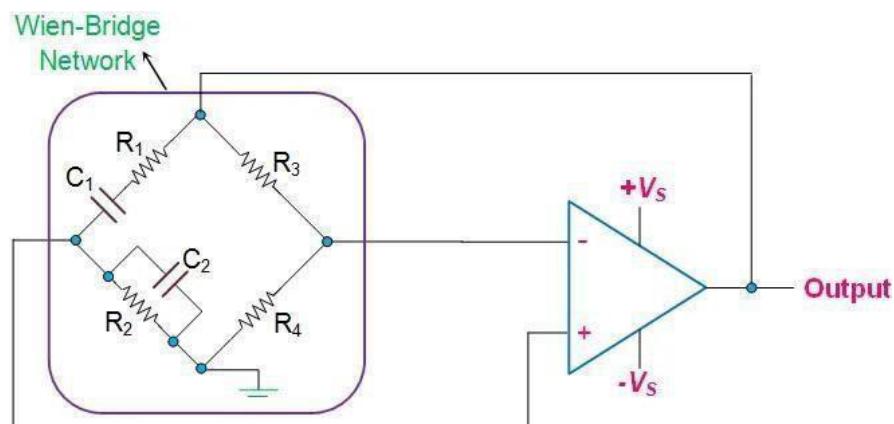
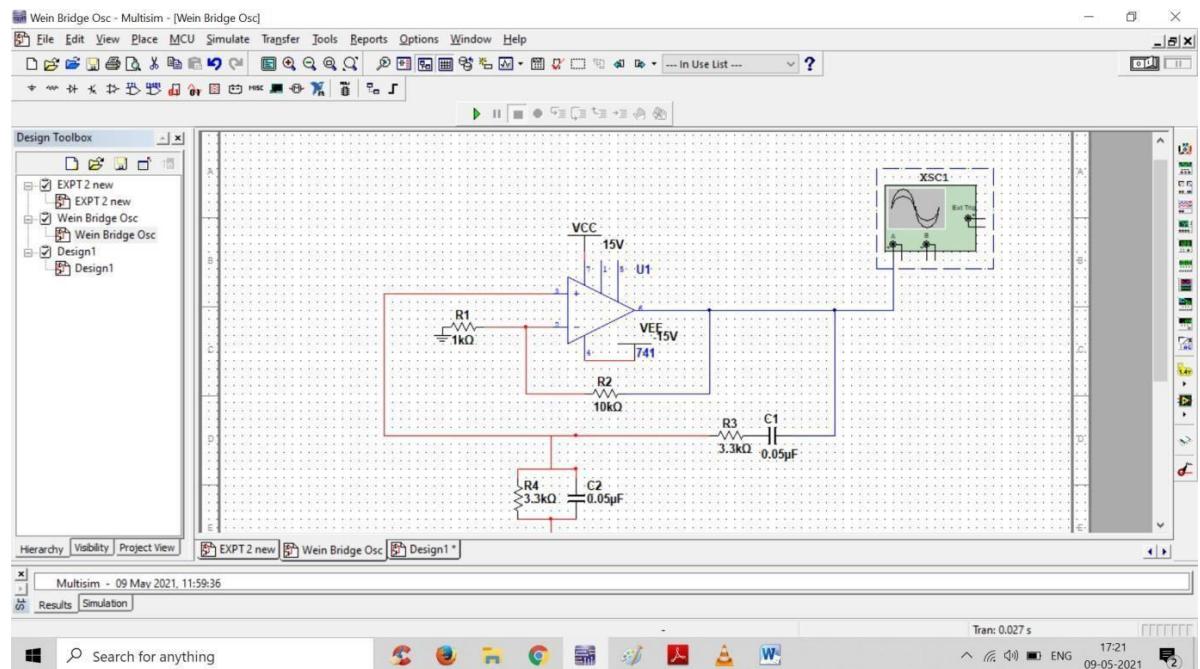


Figure Wien-Bridge Oscillator Using an Op-Amp

Wien-Bridge networks are low frequency oscillators which are used to generate audio and sub-audio frequencies ranging between 20 Hz to 20 KHz. Further, they provide stabilized, low distorted sinusoidal output over a wide range of frequency which can be selected using decade resistance boxes. In addition, the oscillation frequency in this kind of circuit can be varied quite easily as it just needs variation of the capacitors C_1 and C_2 . However these oscillators require large number of circuit components and can be operated up to a certain maximum frequency only.

CIRCUIT DIAGRAM/ Software Implementation:



PROCEDURE:-

1. Start PC and Open Multisim Software.
2. Go to file menu and open new file and draw the circuit diagram (Program) and save it.
3. Go to simulate menu and run the program.
4. If any errors correct them.
5. Observe the input and output waveforms by double clicking XCS.(Oscilloscope).

OBSERVATIONS: -



- Time period of output waveform is 2msec.

CALCULATIONS:-

We have;

$$F_r = \frac{1}{2\pi RC}$$

For R= 3.3k and C=0.05uF
 We get; $= \frac{1}{2\pi * 3.3k * 0.05u} = 482Hz$

$$Fr = \frac{2\pi * 3.3k * 0.05u}{1} = 482Hz$$

Practical value of fr= 1/time period= 1/2msec=500Hz.

RESULT: -

CONCLUSION: -

Experiment No.:-
Title: Practical Integrator

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM: -To design, build & test integrator using Op-amp for given frequency f_a (1kHz).

APPARATUS/REQUIREMENTS: -

For Hardware Experiment:

Sr. No.	Description	Specification	Quantity
1.	OP AMP IC	uA 741	1
2.	CRO	--	1
3.	Resistor	1k, 15k	3
4.	Capacitor	0.01uF	1
5.	Connecting Wires	--	--
6.	Dual Power Supply	+15V & -15V	1
7.	Function Generator	--	1
8.	CRO Probes	--	2

For Software Experiment:

Sr. No.	Description	Specifications	Quantity
1.	Personal Computer	With Windows OS. P4 or advanced processor	1
2.	Multisim Software	--	1

THEORY:-

As its name implies, the Integrator Amplifier is an operational amplifier circuit that performs the mathematical operation of Integration. A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C .

The Following fig. shows the op-amp as integrator.

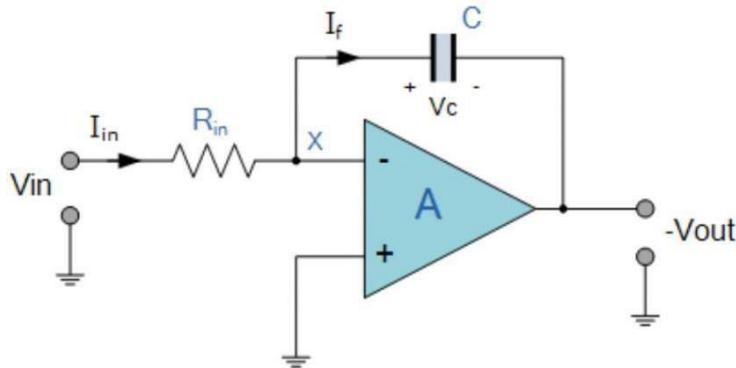


Fig. Op-amp as integrator

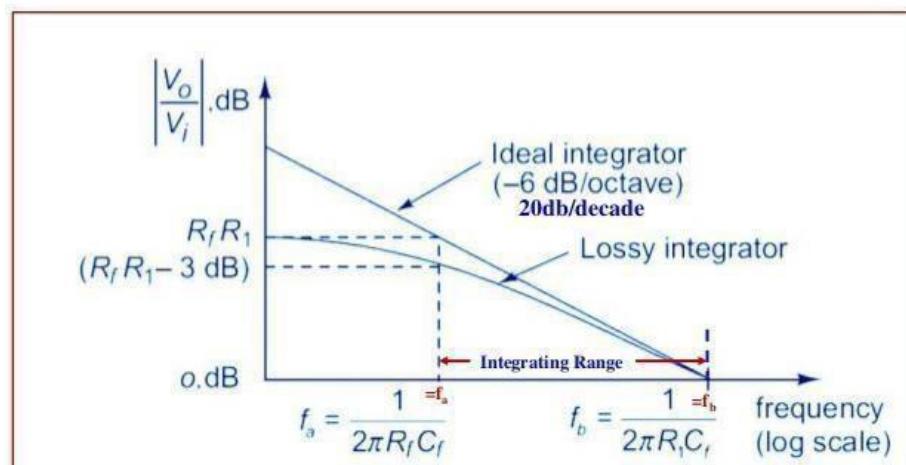
the expression for the output voltage is given as,

$$V_{out} = - (1/RF C) \int V_s dt$$

Here the negative sign indicates that the output voltage is 180 degrees out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $RF C$. That is, $T \geq RF C$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

Frequency response of practical integrator is;



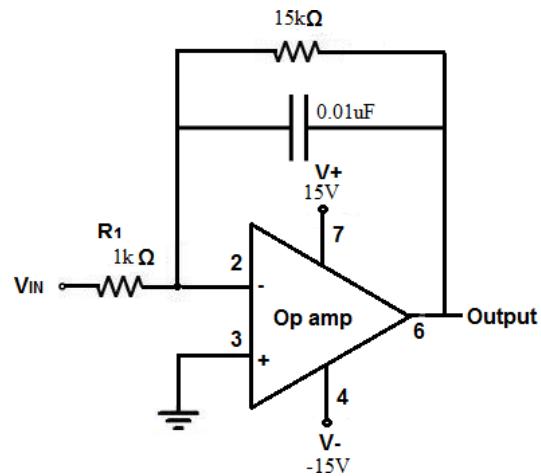
Frequency Response of an Ideal & Lossy Integrator

Cut off frequency of integrator is given by

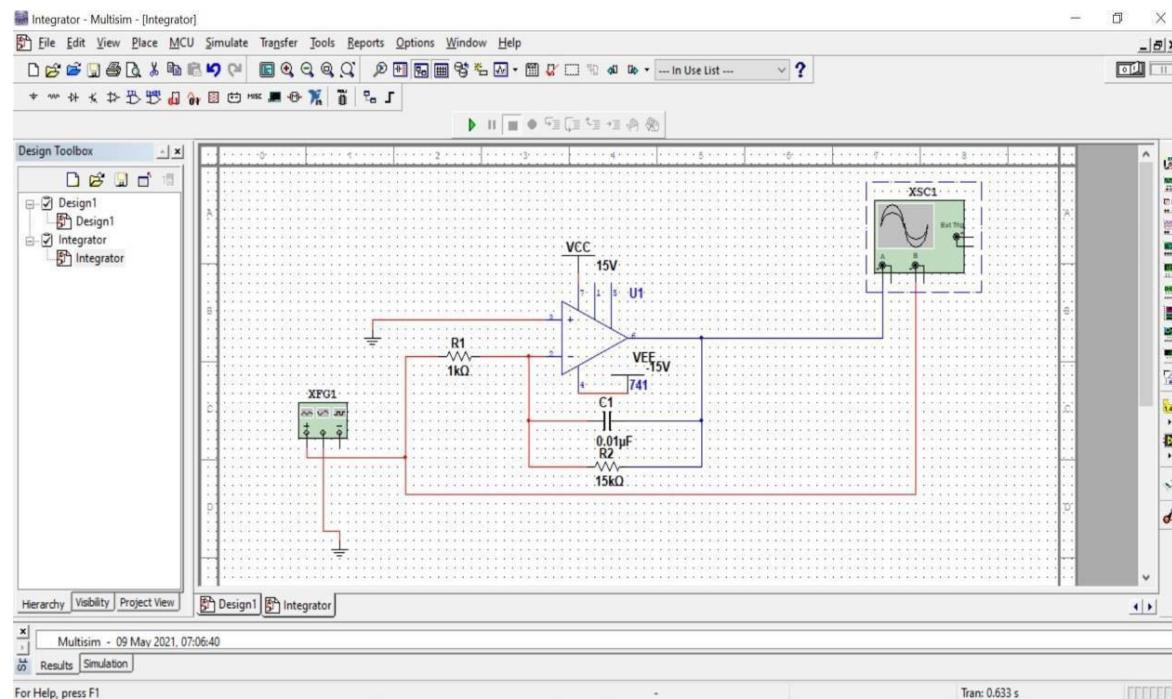
$$\frac{1}{2\pi R C}$$

$$F_a = \frac{1}{2\pi f C}$$

CIRCUIT DIAGRAM:



CIRCUIT DIAGRAM /SIMULATION:



PROCEDURE: -

For Hardware Experiment:

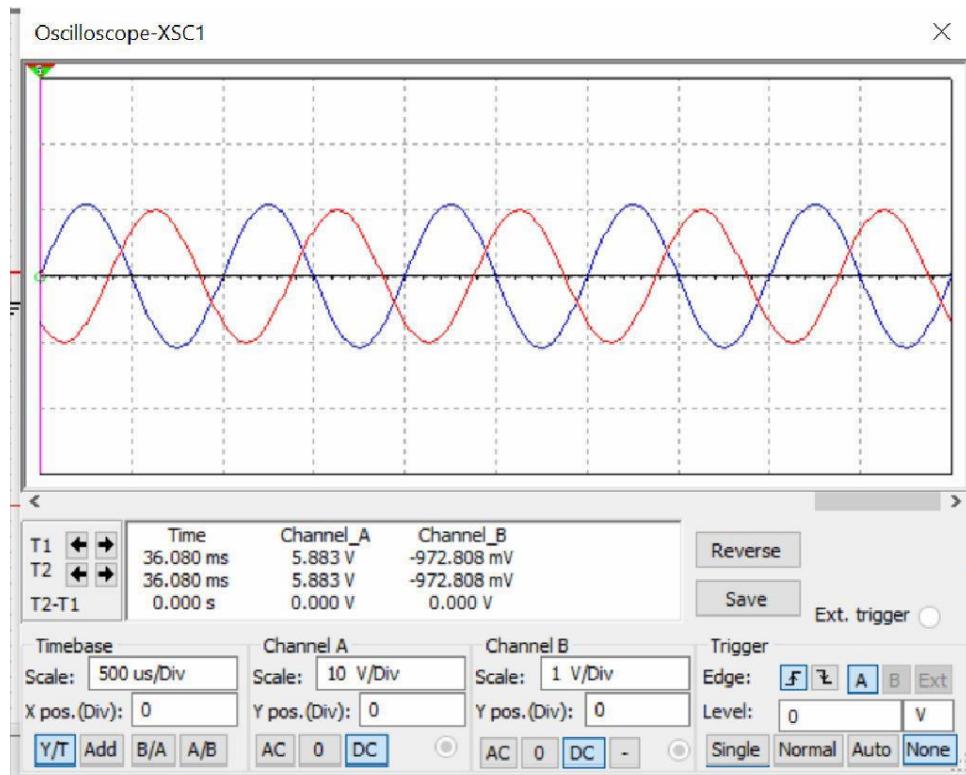
- Make Connections as per the circuit diagram.
- + Vcc and - VEE supply is given to the power supply terminal of the Op-Amp IC.
- By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
- The output voltage is obtained in the CRO and the input and output voltage waveforms are observed and plotted.

For Software Experiment:

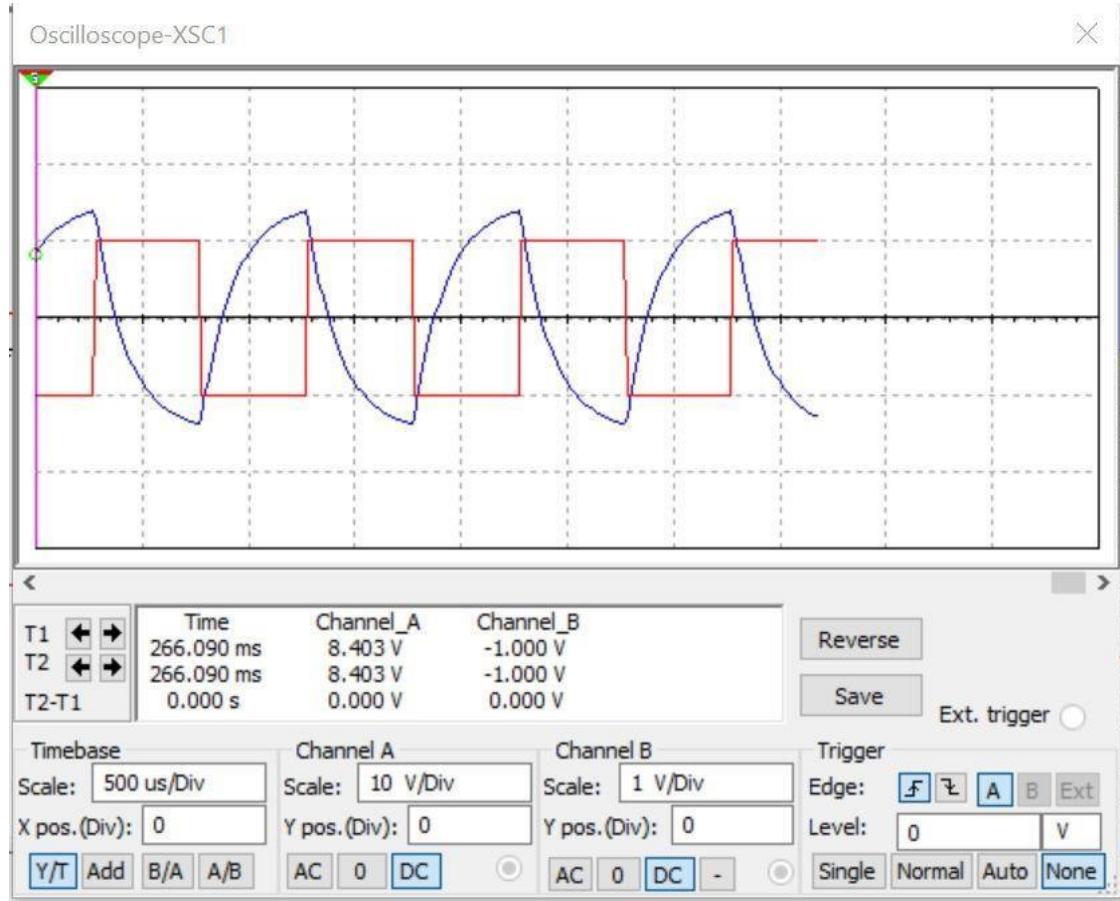
- Start PC and Open Multisim Software.
- Go to file menu and open new file and draw the circuit diagram (Program) and save it.
- Go to simulate menu and run the program.
- If any errors correct them.
- Observe the input and output waveforms by double clicking XCS. (Oscilloscope).

OBSERVATIONS: -

A. When input is sine wave:



B. When input is square wave:



CALCULATIONS:-

Design:

Cut off frequency of integrator is given by $\frac{1}{2\pi R C}$

For $F_a = 1\text{Kz}$, Let $C_f = 0.01\mu\text{F}$
Then above equation;

Rearranging

$$1k \frac{1}{2\pi R_f 0.01\mu} = \frac{1}{1}$$

After solving we get $R_f = \frac{1}{2\pi * 1k * 0.01\mu}$

$$R_f = 15.923k$$

Assuming

$$R_f = 15k$$

RESULT:-

CONCLUSION:-

Experiment No.:-
Title: 3-bit R-2R ladder DAC

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM: -To design, build & test 2 or 3-bit R-2R ladder DAC using multisim.

APPARATUS/REQUIREMENTS: -

Sr. No.	Description	Specifications	Quantity
1.	Personal Computer	With Windows OS. P4 or advanced processor	1
2.	Multisim Software	--	1

THEORY:-

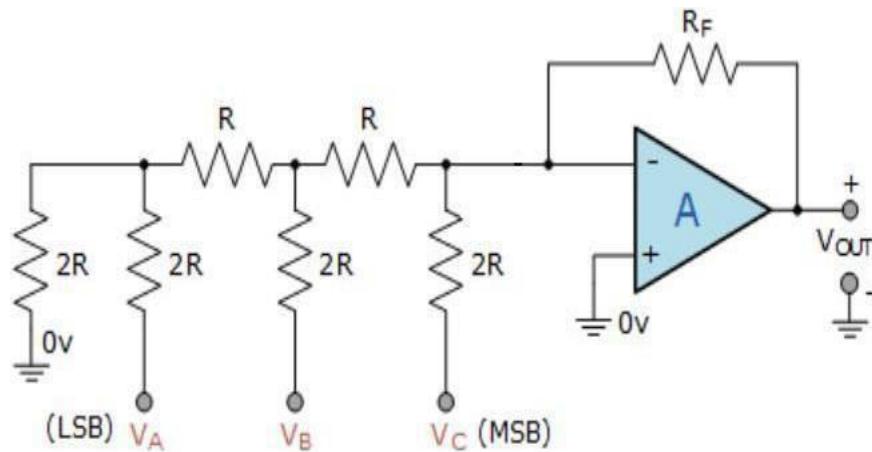
The R-2R resistive ladder network uses just two resistor values, one which is the base value “R” and the other which has twice the value, “2R” of the first resistor no matter how many bits are used to make up the ladder network. So, for example, we could just use a $1\text{k}\Omega$ resistor for the base resistor “R”, and therefore a $2\text{k}\Omega$ resistor for “2R” (or multiples thereof as the base value of R is not too critical), thus 2R is always twice the value of R, that is $2R = 2*R$. This means that it is much easier to maintain the required accuracy of the resistors along the ladder network compared to the previous weighted resistor DAC. But what is a “R-2R resistive ladder network” anyway.

R-2R Resistive Ladder Network

As its name implies, the “ladder” description comes from the ladder-like configuration of the resistors used within the network. A R-2R resistive ladder network provides a simple means of converting digital voltage signals into an equivalent analogue output. Input voltages are

applied to the ladder network at various points along its length and the more input points the better the resolution of the R-2R ladder. The output signal as a result of all these input voltage points is taken from the end of the ladder which is used to drive the inverting input of an operational amplifier.

Then a R-2R resistive ladder network is nothing more than long strings of parallel and series connected resistors acting as interconnected voltage dividers along its length, and whose output voltage depends slowly on the interaction of the input voltages with each other. Consider the basic 4-bit R-2R ladder network (3-bits because it has four input points) below.



The generalized analog output voltage equation can be given as

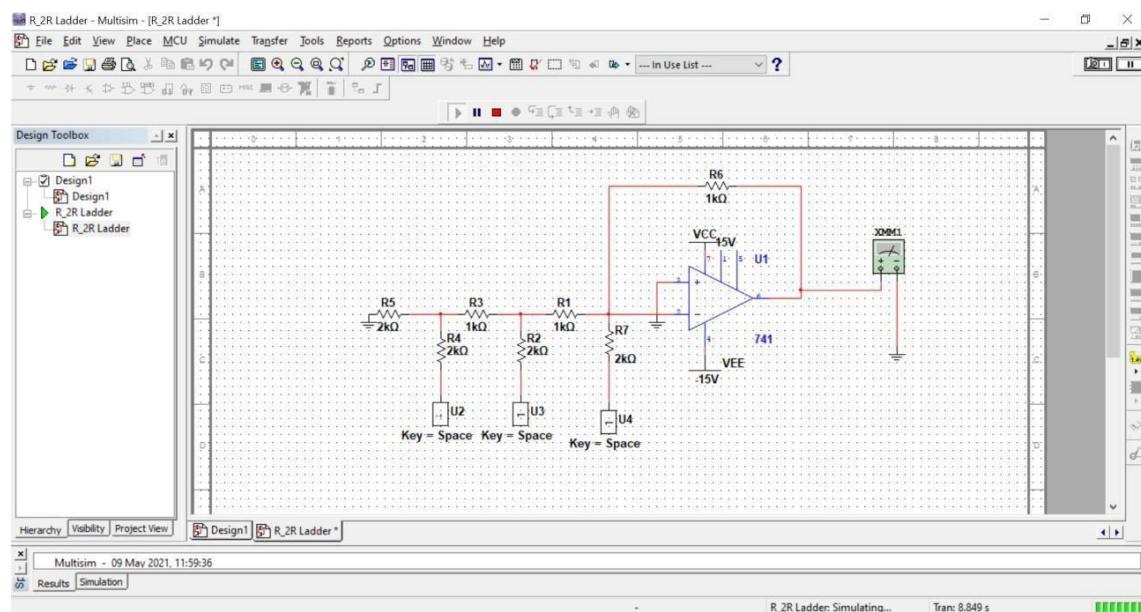
$$\begin{aligned}
 V_o &= -V_R \frac{R_f}{R} \left[\frac{B_1}{2^1} + \frac{B_2}{2^2} + \frac{B_3}{2^3} + \dots + \frac{B_n}{2^n} \right] \\
 \therefore V_o &= -V_R \frac{R_f}{R \times 2^n} [B_1 2^{n-1} + B_2 2^{n-2} + B_3 2^{n-3} + \dots + B_n 2^0] \\
 \therefore V_o &= -V_R \frac{R_f}{R \times 2^n} [B_1 2^{n-1} + B_2 2^{n-2} + B_3 2^{n-3} + \dots + B_n 2^0]
 \end{aligned}$$

For 3bit DAC

$$V_o = \frac{[V_C * 2^2 + V_B * 2^1 + V_A * 2^0]}{R * 2^3}$$

Here VC is MSB and VA is LSB.

CIRCUIT DIAGRAM /SIMULATION:-



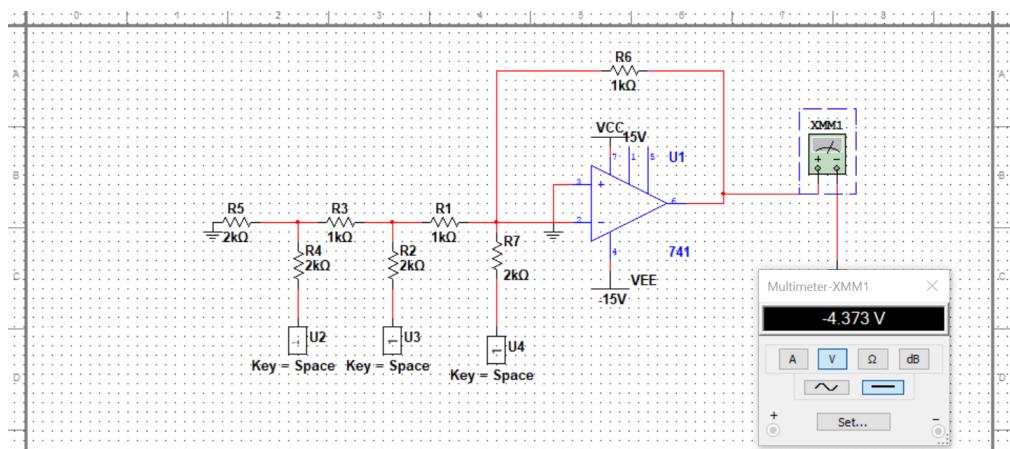
PROCEDURE:-

For Software Experiment:

- Start PC and Open Multisim Software.
- Go to file menu and open new file and draw the circuit diagram (Program) and save it.
- Go to simulate menu and run the program.
- If any errors correct them.
- Observe the input and output waveforms by double clicking XCS. (Oscilloscope).

OBSERVATIONS:-

C. When input 111



Observation Table:

Sr. No	Binary Input (VC, VB, VA)	Output Voltage
1		
2		
3		
4		
5		
6		
7		
8		

CALCULATIONS: -

We have $R=R_f=1k$, $V_R = 5V$

$$V_o = -V \frac{R_f}{R * 2^3} [V_C * 2^2 + V_B * 2^1 + V_A * 2^0]$$

Therefore;

$$V_o = -\frac{1}{8} [V_C * 4 + V_B * 2 + V_A * 1]$$

C

$$V_o = -5 \frac{1}{8} [V_C * 4 + V_B * 2 + V_A * 1]$$

$$V_o = -\frac{5}{8} [V_C * 4 + V_B * 2 + V_A * 1]$$

When $VCVBVA=000$ then

$$V_o = -\frac{5}{8} [0 * 4 + 0 * 2 + 0 * 1] = 0V$$

8

Likewise, we can calculate output voltage for all input combinations.

RESULT:-

Sr. No	Binary Input (VC, VB, VA)	Output Voltage (Observed)	Output Voltage (Theoretical)
1			
2			
3			

4			
5			
6			
7			
8			

CONCLUSION:-

Experiment No.:

Title: Square and Triangular waveform generator

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM:-To design, build & test square and triangular waveform generator using Op-Amp.

APPARATUS/REQUIREMENTS: -

For Software Experiment:

Sr. No.	Description	Specifications	Quantity
1.	Personal Computer	With Windows OS. P4 or advanced processor	1
2.	Multisim Software	--	1

THEORY:-

A. Square Wave Generator

- The Square Wave Generator Using Op amp means the astable multivibrator circuit using op-amp, which generates the square wave of required frequency. The Fig. shows the square wave generator using op amp.

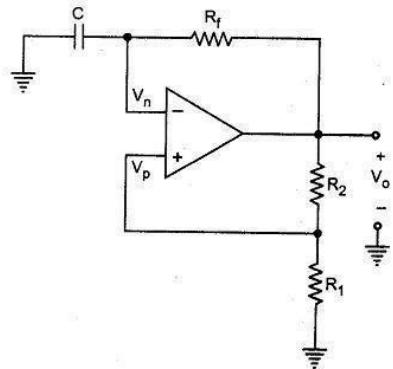


Fig. Square wave generator

- When V_o is at $+V_{sat}$, the feedback voltage is called the upper threshold voltage V_{UT} and is given as,

$$V_{UT} = \frac{R_1 \cdot +V_{sat}}{R_1 + R_2} \quad \dots (1)$$

- When V_o is at $-V_{sat}$, the feedback voltage is called the lower-threshold voltage V_{LT} and is given as

$$V_{LT} = \frac{R_1 \cdot -V_{sat}}{R_1 + R_2} \quad \dots (2)$$

- When power is turn ON, V_o automatically swings either to $+V_{sat}$ or to $-V_{sat}$ since these are the only stable states allowed by the Schmitt trigger. Assume it swings to $+V_{sat}$. With $V_o = +V_{sat}$ we have $-V_p = V_{UT}$ and capacitor starts charging towards $+V_{sat}$ through the feedback path provided by the resistor R_f to the inverting (-) input. This is illustrated in Following fig. As long as the capacitor voltage V_C is less than V_{UT} , the output voltage remains at $+V_{sat}$

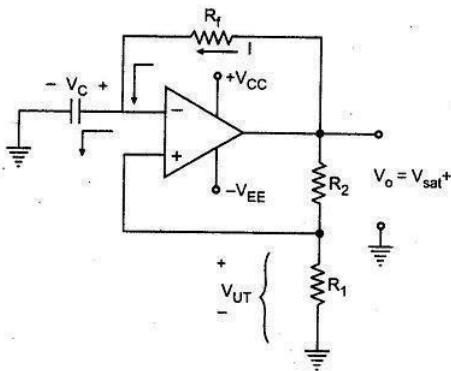


Fig. When $V_o = +V_{sat}$, capacitor charges towards V_{UT}

- As soon as V_C charges to a value slightly greater than V_{UT} , the (-) input goes positive with respect to the (+) input. This switches the output voltage from $+V_{sat}$ to $-V_{sat}$ and we have $V_p = V_{LT}$, which is negative with respect to ground. As V_o switches to $-V_{sat}$, capacitor starts discharging via R_f , as shown in the following Fig.

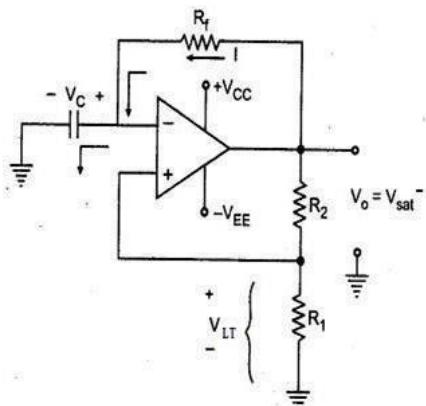


Fig. When $V_o = +V_{sat}$, capacitor charges towards V_{LT}

- The current $I = \frac{V_{sat}}{R_2}$ – discharges capacitor to 0 V and recharges capacitor to V_{LT} . When V_C becomes slightly more negative than the feedback voltage V_{LT} , output voltage V_o switches back to $+V_{sat}$. As a result, the condition in Fig. is reestablished except that capacitor now has an initial charge equal to V_{LT} . The capacitor will discharge from V_{LT} to 0V and then recharge to V_{UT} , and the process is repeating. Once the initial cycle is completed, the waveform become periodic, as shown in the Fig.

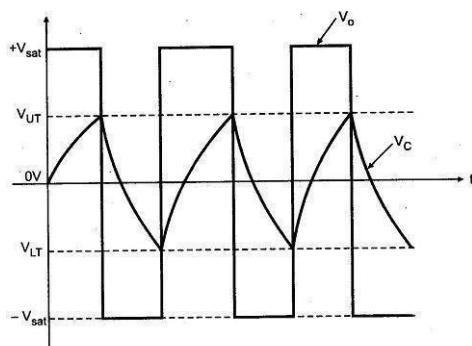


Fig. Waveforms

Frequency of square wave is given by;

$$f_o = \frac{1}{2 R_f C \ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)}.$$

B. Triangular Wave Generator:

- The output of integrator is a Triangular Wave Generator Using Op amp if its input is a square wave. This means that a Triangular Wave Generator Using Op amp can be formed by simply connecting an integrator to the square wave generator as shown in the Fig.

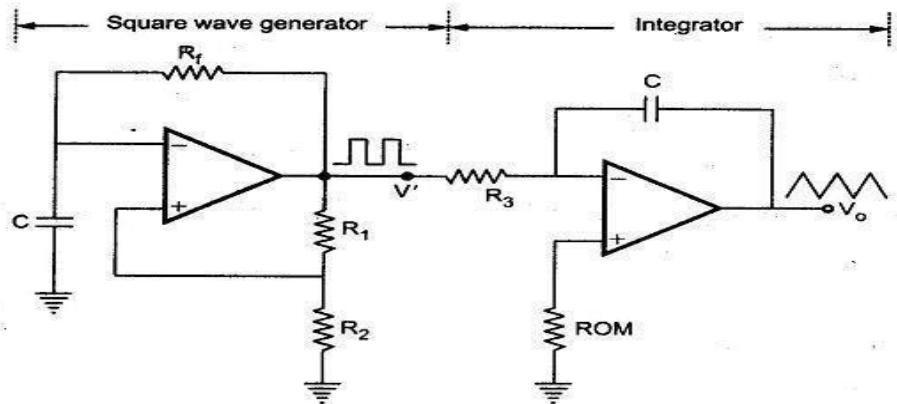


Fig. Triangular wave generator

- Basically, triangular wave is generated by alternatively charging and discharging a capacitor with a constant current. This is achieved by connecting integrator circuit at the output of square wave generator. Assume that V' is high at $+V_{sat}$. This forces a constant current ($+V_{sat} / R_3$) through C (left to right) to drive V_o negative linearly. When V' is low at $-V_{sat}$, it forces a constant current ($-V_{sat} / R_3$) through C (right to left) to drive V_o positive, linearly. The frequency of the triangular wave is same as that of square wave. This is illustrated in Fig. 2.86. Although the amplitude of the square wave is constant ($\pm V_{sat}$), the amplitude of the triangular wave decreases with an increase in its frequency, and vice versa. This is because the reactance of capacitor decreases at high frequencies and increases at low frequencies.
- Figure Shows two waveforms first is output of square wave generator which is then given to integrator. Finally, we get triangular wave as output.

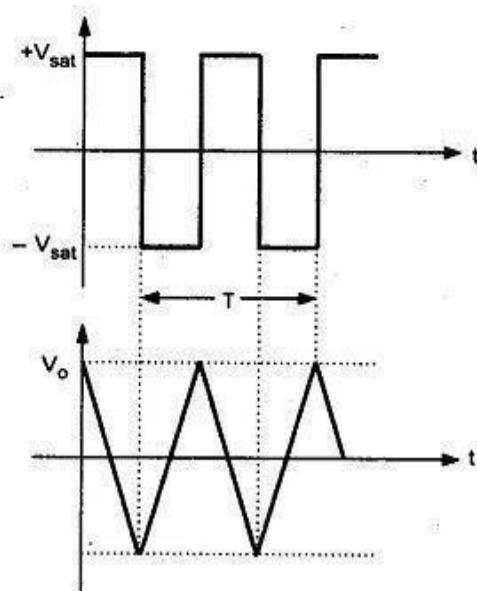
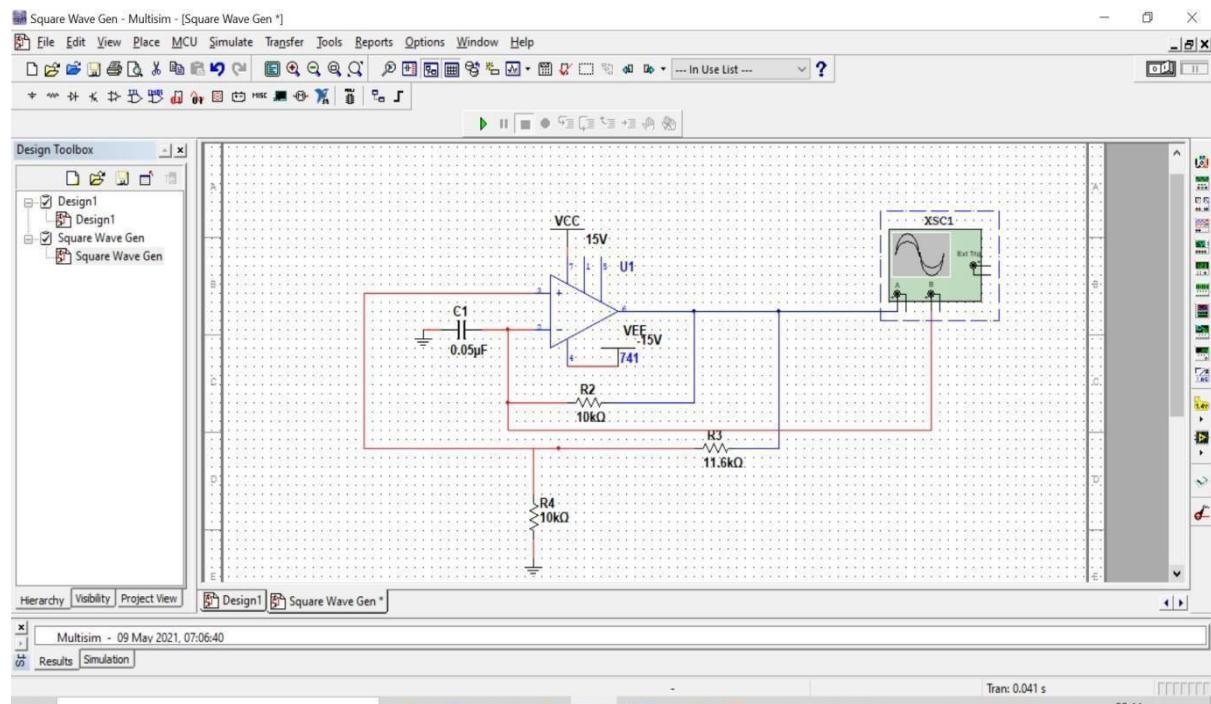


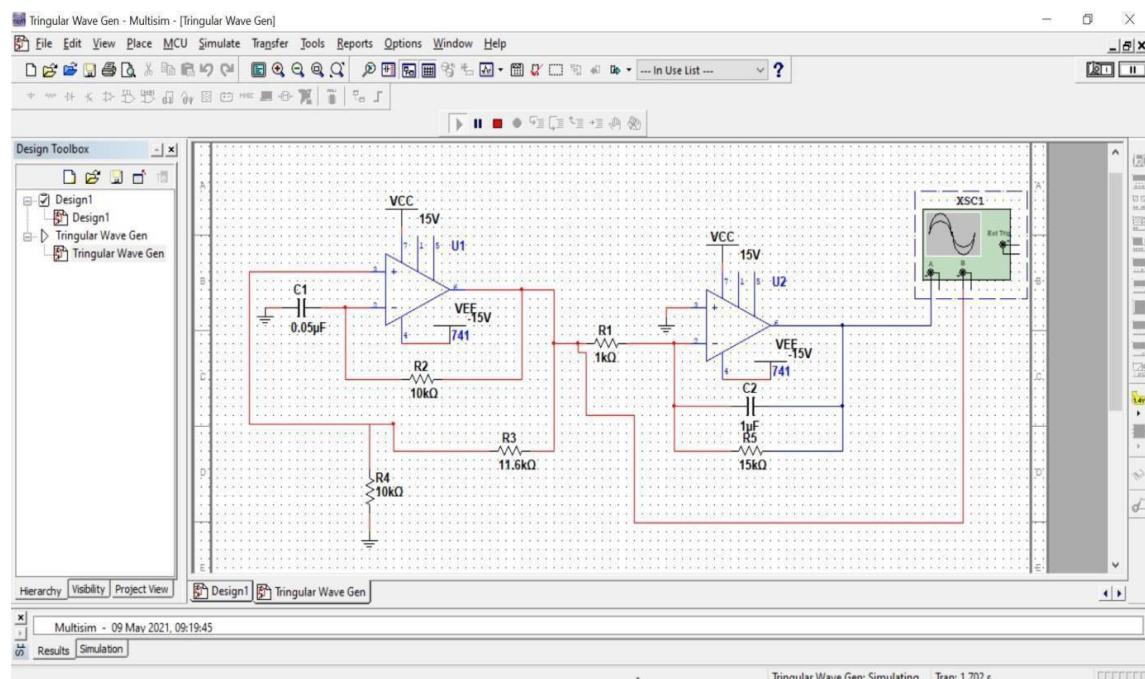
Fig. Waveforms of triangular wave generator

CIRCUIT DIAGRAM:

A. Square Wave Generator:



B. Triangular Wave Generator:



PROCEDURE: -

A. Square Wave Generator:

- Start PC and Open Multisim Software.
- Go to file menu and open new file and draw the circuit diagram (Program) and save it.
- Go to simulate menu and run the program.
- If any errors correct them.
- Observe the input and output waveforms by double clicking XCS. (Oscilloscope).

B. Triangular Wave Generator:

- Start PC and Open Multisim Software.
- Go to file menu and open new file and draw the circuit diagram (Program) and save it.
- Go to simulate menu and run the program.
- If any errors correct them.
- Observe the input and output waveforms by double clicking XCS.(Oscilloscope).

OBSERVATIONS: -

A. Square Wave Generator:



B. Triangular Wave Generator:



- From waveform we get $+V_{sat} = 14V$ and $-V_{sat} = -14V$.
- From waveform we can calculate frequency of square wave as
No. of Divisions per cycle are 2.2
Scale is 500usec/ Div

CALCULATIONS:-

Frequency of square wave is given by;

$$f_0 = \frac{1}{2 R_f C \ln \left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}} \right)}$$

Now;

$+V_{sat} = 14V$ and $-V_{sat} = -14V$, $R_1 = 10k$ and $R_2 = 11.6k$

$$V_{UT} = \frac{R_1 \cdot +V_{sat}}{R_1 + R_2} \quad \dots \quad (1)$$

$$V_{LT} = \frac{R_1 \cdot -V_{sat}}{R_1 + R_2} \quad \dots (2)$$

We get

$$V_{UT} = 6.48V$$

$$V_{LT} = -6.48V$$

Also $R_f = 10k$ and $C = 0.05\mu F$.

We get f_{oas} ;

$$f_o = 1kHz$$

Practical value of Frequency:

Time period of 1 cycle = $500\mu s * 2.2 = 1100\mu s$

Now frequency = $1 / T = 1 / 1100\mu s = 909Hz$

RESULT:-

Practical value of Frequency:

Theoretical value of Frequency:

CONCLUSION:-

Experiment No.:
Title: Schmitt Trigger

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM: -To design, build & test Schmitt trigger using Op-Amp.

APPARATUS/REQUIREMENTS: -

For Hardware Experiment:

Sr. No.	Description	Specification	Quantity
1.	OP AMP IC	uA 741	1
2.	CRO	--	1
3.	Resistor	100ohm, 1k, 56k	3
4.	Connecting Wires	--	--
5.	Dual Power Supply	+15V & -15V	1
6.	Function Generator	--	1
7.	CRO Probes	--	2

For Software Experiment:

Sr. No.	Description	Specifications	Quantity
1.	Personal Computer	With Windows OS. P4 or advanced processor	1
2.	Multisim Software	--	1

THEORY:-

A part of output is fed back to the non-inverting (positive) input of the op-amp, hence called as positive feedback comparator. The inverting Schmitt trigger is shown below,

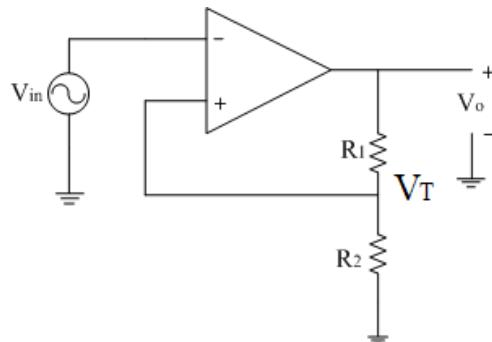


Fig. 1 Circuit diagram

- The triggering point VT is calculated as

$$VT = R_2 / (R_1 + R_2) V_{out}$$
- If $V_{out} = +V_{sat}$, $VT = +ve$
 If $V_{out} = -V_{sat}$, $VT = -ve$

Thus when output is $+V_{sat}$, the upper threshold point is given as

$$V_{UT} = R_2 / (R_1 + R_2) [+V_{sat}]$$

And when output is $-V_{sat}$, the lower threshold point is given as

- $V_{LT} = R_2 / (R_1 + R_2) [-V_{sat}]$
- The operation of the above circuit can be explained with the two conditions

When $V_{in} > VT \therefore V_o = -V_{sat}$

When $V_{in} < VT \therefore V_o = +V_{sat}$

When input voltage V_{in} is less than upper threshold V_{UT} , the output is in positive saturation $+V_{sat}$. When input crosses the upper threshold V_{UT} , output is changed to negative saturation $-V_{sat}$. This output state is maintained till the next threshold level i.e., V_{LT} . When input signal crosses the lower threshold V_{LT} , output is changed to positive saturation.

Thus, output state is changed only when the two thresholds are crossed. This is shown in the transfer characteristics. Between the V_{LT} and V_{UT} , output ($\pm V_{sat}$) remains constant i.e output is not responding to any changes in the input signal. Thus, output is dead between V_{LT} and V_{UT} and called as dead band. It is also referred as hysteresis width, denoted by 'H'.

- Thus, in transfer characteristics we get a rectangle. This is called as hysteresis loop. The graph indicates that the output remains in the state indefinitely until input voltage crosses the any of the threshold levels. The transfer characteristics are shown below.
- This hysteresis loop is also called as a dead band or dead zone because output is not changing (i.e., not responding to input signal)
- The Width of Hysteresis Loop is calculated as

$$H = V_{UT} - V_{LT}$$

$$\therefore H = R_2 / (R_1 + R_2) [+V_{sat}] - R_2 / (R_1 + R_2) [-V_{sat}]$$

$$\therefore H = \frac{(2R_2)}{(R_1 + R_2)} [V_{sat}]$$

$$H = 2VT$$

- The input and output waveforms and transfer characteristics are shown below.

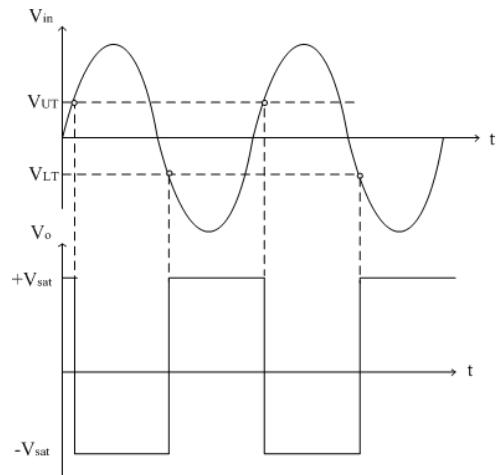


Fig. 2 Input output waveforms

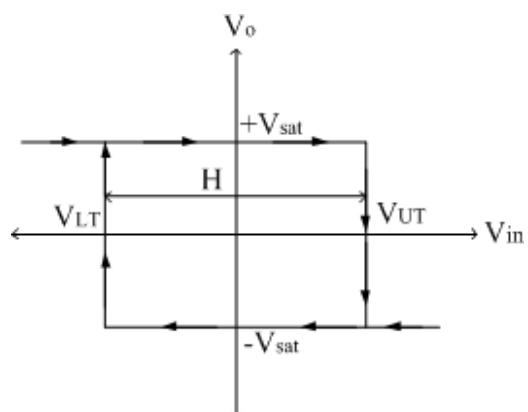
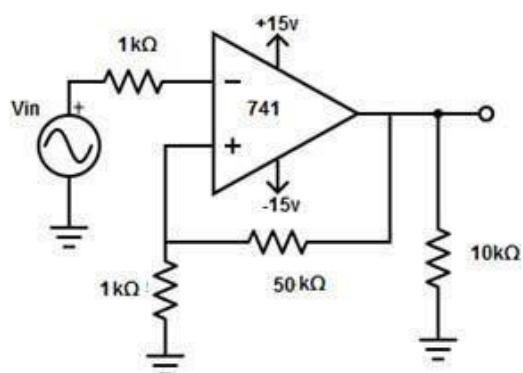
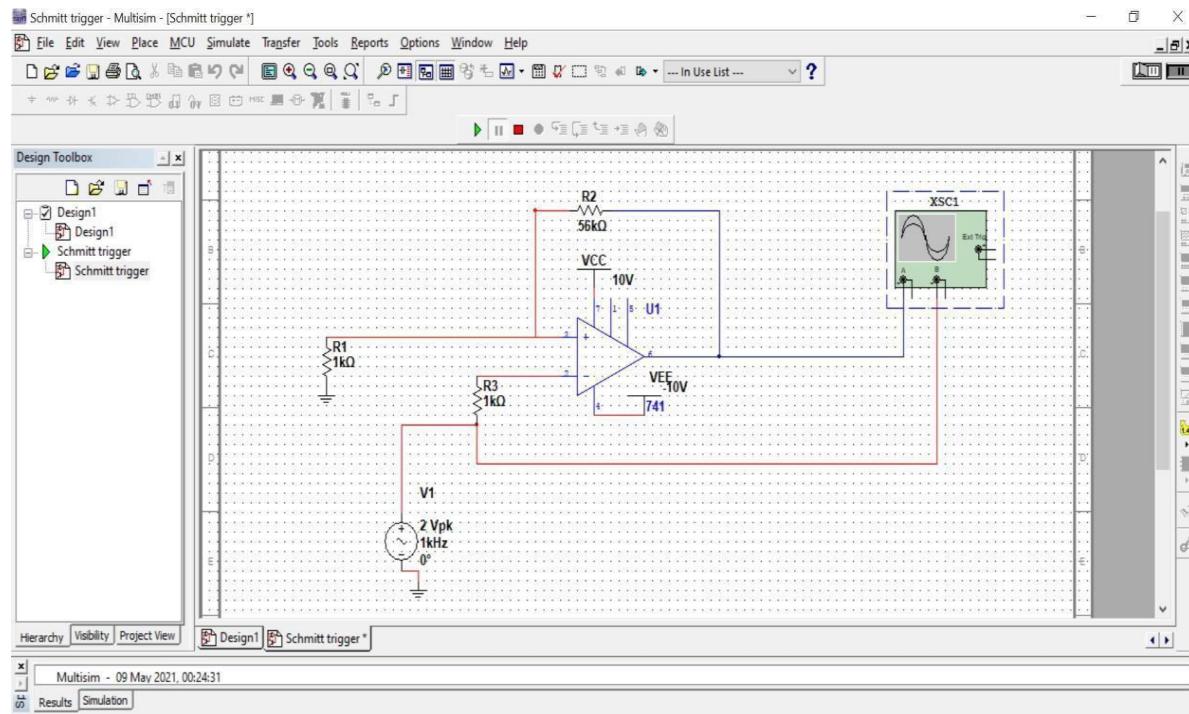


Fig. 2 Hysteresis loop

CIRCUIT DIAGRAM/ Software Implementation:



Simulation:



PROCEDURE:-

For Hardware Experiment:

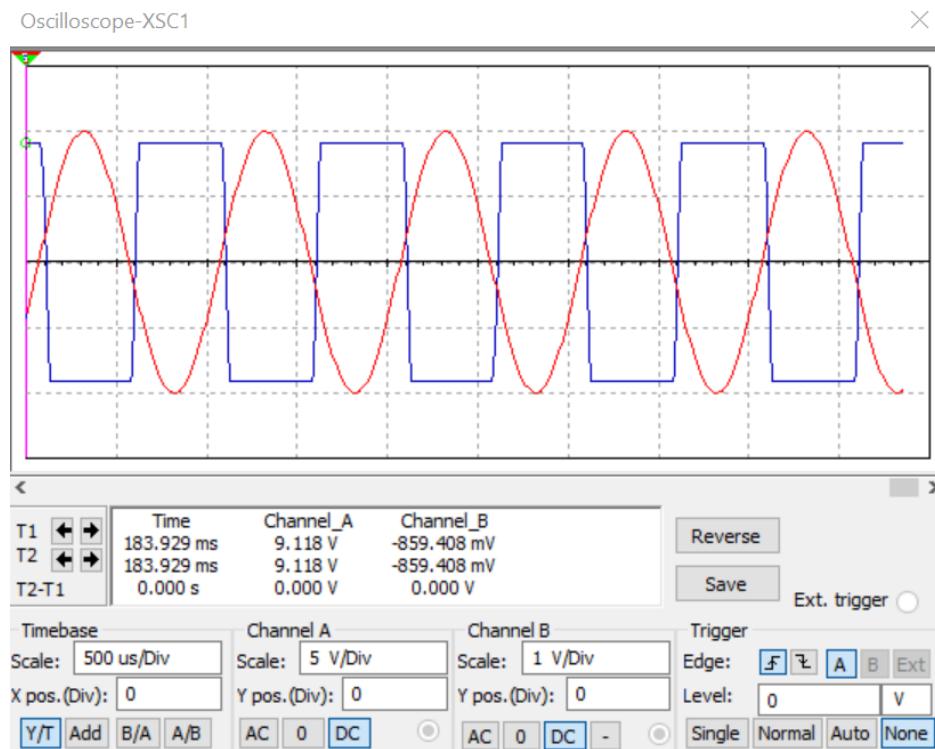
- Make Connections as per the circuit diagram.
- + Vcc and - VEE supply is given to the power supply terminal of the Op-Amp IC.
- By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
- The output voltage is obtained in the CRO and the input and output voltage waveforms are observed and plotted.

For Software Experiment:

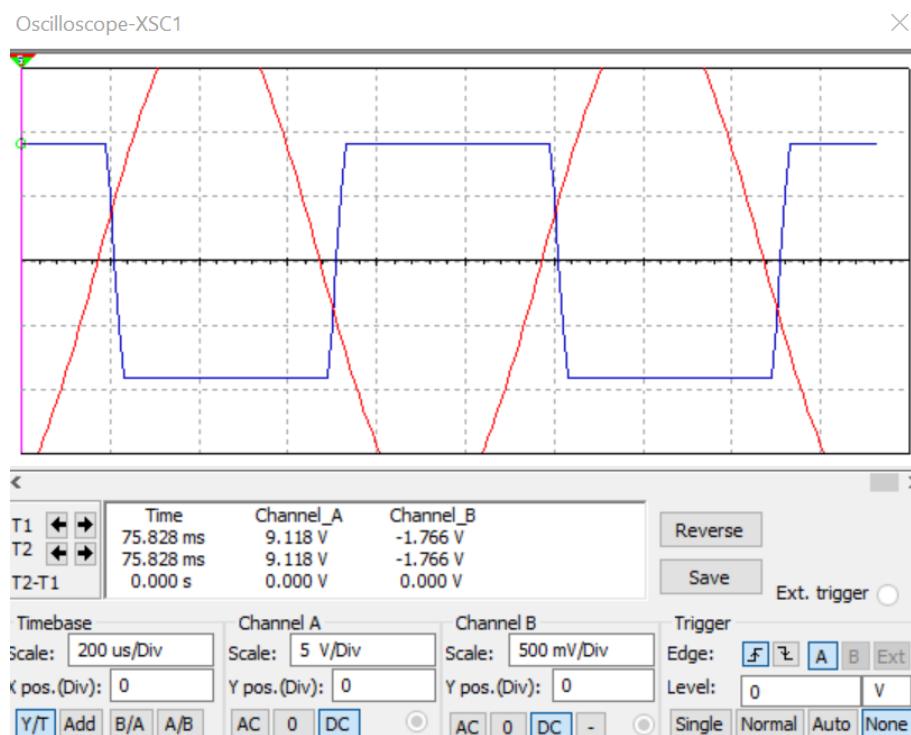
6. Start PC and Open Multisim Software.
7. Go to file menu and open new file and draw the circuit diagram (Program) and save it.
8. Go to simulate menu and run the program.
9. If any errors correct them.
10. Observe the input and output waveforms by double clicking XCS.(Oscilloscope).

OBSERVATIONS:-

A. Input Output Waveforms:



B. Threshold Voltage observation:



CALCULATIONS: -

$$V_{UT} = R_2 / (R_1 + R_2) [+V_{sat}]$$

$$V_{LT} = R_2 / (R_1 + R_2) [-V_{sat}]$$

By putting values of $R_1 = 56k$ and $R_2 = 1k$ we get;

$$V_{UT} = 0.158V$$

$$V_{LT} = -0.158V$$

$$\text{Hysteresis (H)} = 2V_{UT} = 2 * 0.158 = 0.316 \text{ V}$$

RESULT:-

CONCLUSION:-

Experiment No.:

Title: Instrumentation amplifier

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

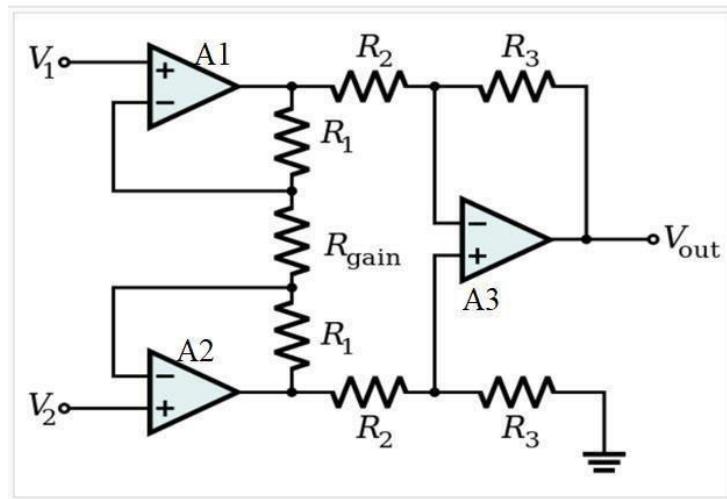
AIM: -To design, build & test three Op amp Instrumentation amplifier for typical application using multisim.

APPARATUS/REQUIREMENTS: -

Sr. No.	Description	Specifications	Quantity
1.	Personal Computer	With Windows OS. P4 or advanced processor	1
2.	Multisim Software	--	1

THEORY: -

Instrumentation amplifier is a kind of differential amplifier with additional input buffer stages. The addition of input buffer stages makes it easy to match (impedance matching) the amplifier with the preceding stage. Instrumentation amplifiers are commonly used in industrial test and measurement application. The instrumentation amplifier also has some useful features like low offset voltage, high CMRR (Common mode rejection ratio), high input resistance, high gain etc. The circuit diagram of a typical instrumentation amplifier using opamp is shown below;



A circuit providing an output based on the difference between two inputs (times a scale factor) is given in the above figure. In the circuit diagram, opamps labeled A1 and A2 are the input buffers. Anyway, the gain of these buffer stages is not unity because of the presence of R₁ and R_g. Op amp labeled A3 is wired as a standard differential amplifier. R₃ connected from the output of A3 to its non-inverting input is the feedback resistor. R₂ is the input resistor. The voltage gain of the instrumentation amplifier can be expressed by using the equation below;

$$A_v = \frac{V_{\text{out}}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{\text{gain}}} \right) \frac{R_3}{R_2}$$

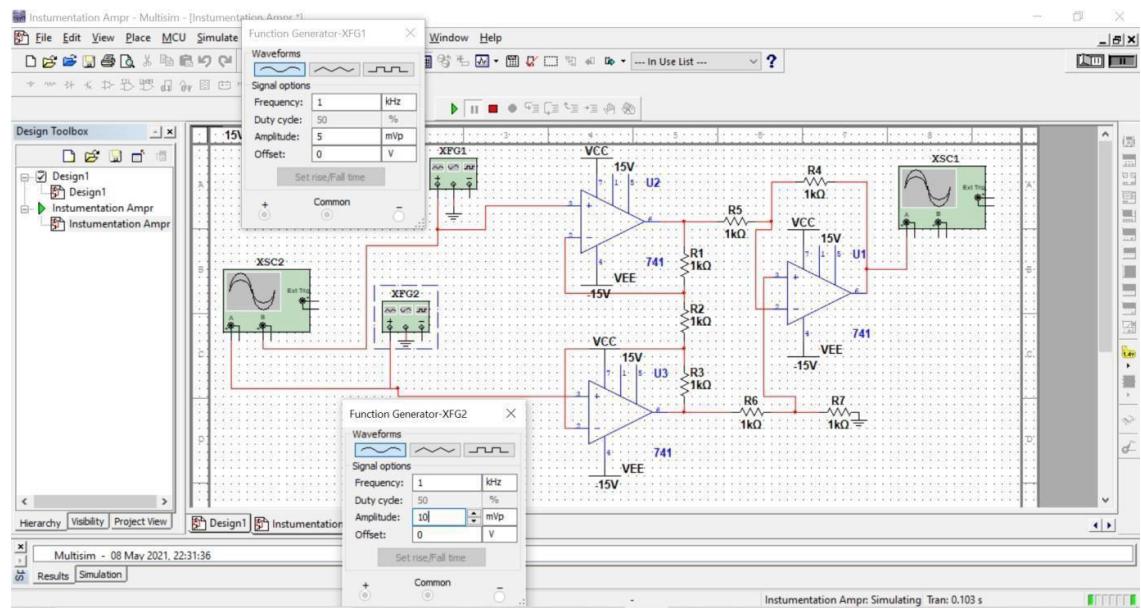
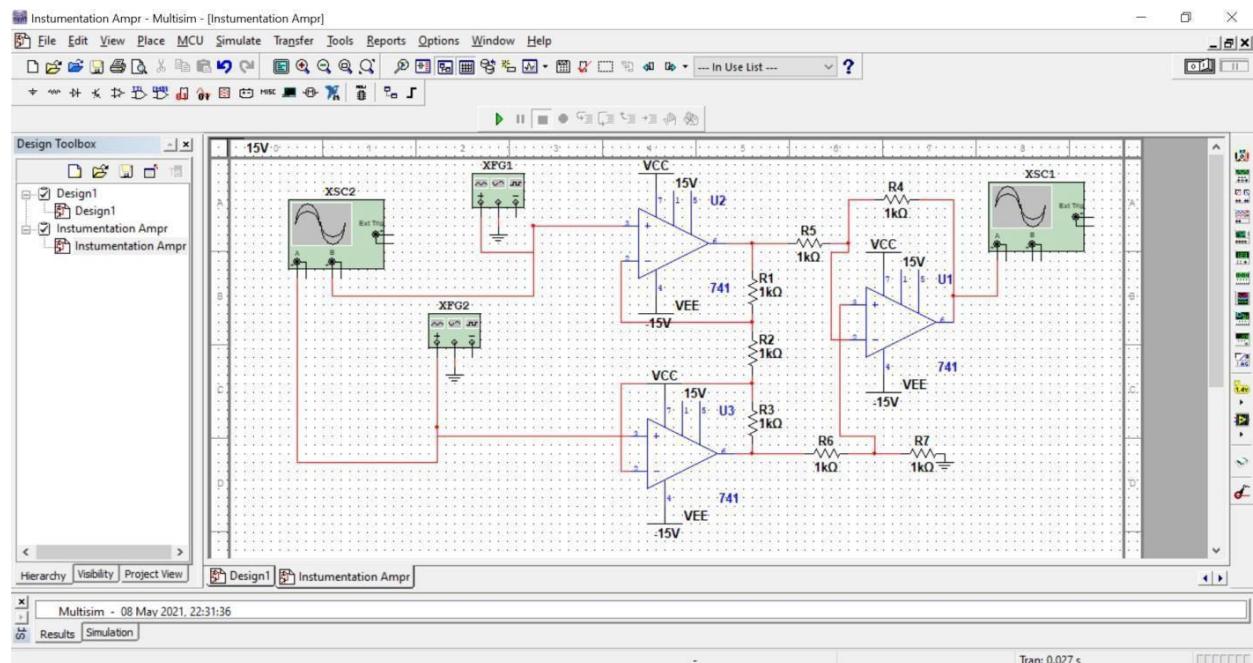
If need a setup for varying the gain, replace *R_{gain}* with a suitable potentiometer. Instrumentation amplifiers are generally used in situations where high sensitivity, accuracy and stability are required. Instrumentation amplifiers can be also made using two opamps, but they are rarely used and the common practice is to make it using three opamps like what is shown here. The only advantages of making an instrumentation amplifier using 2 opamps are low cost and improved CMRR.

High gain accuracy can be achieved by using precision metal film resistors for all the resistances. Because of large negative feedback employed, the amplifier has good linearity, typically about 0.01% for a gain less than 10. The output impedance is also low, being in the range of milli-ohms. The input bias current of the instrumentation amplifier is determined by the op-amps A1 and A2.

PROCEDURE:-

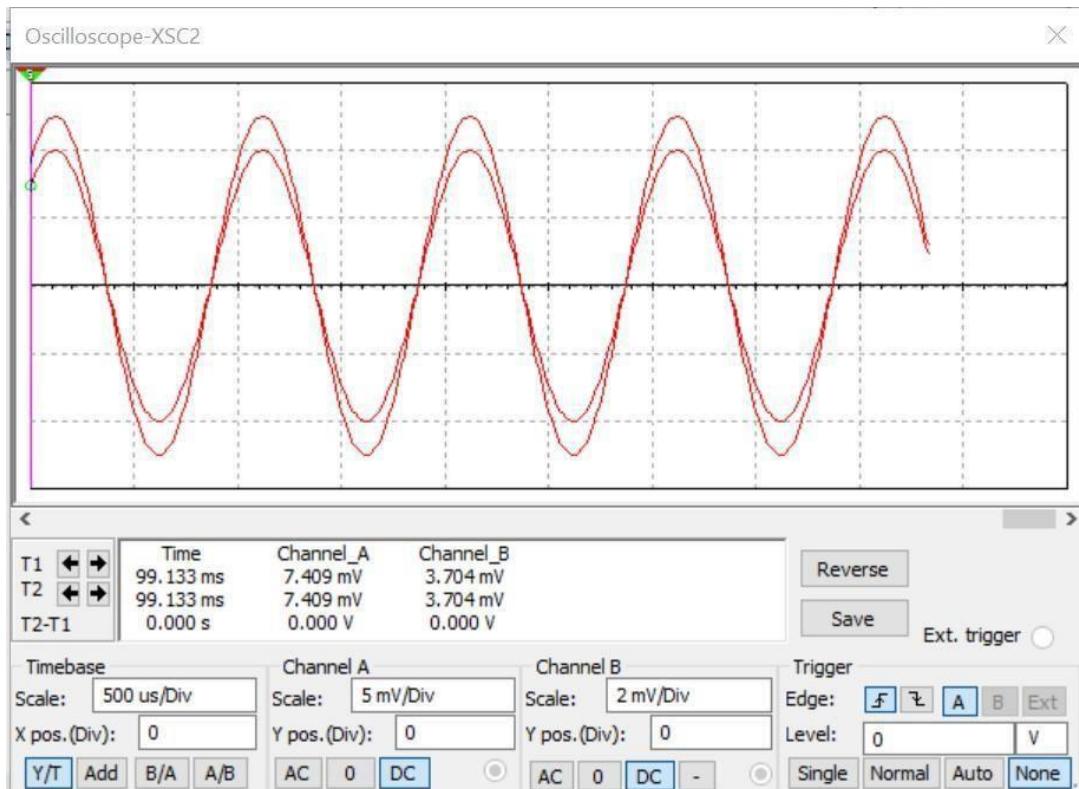
1. Start PC and Open Multisim Software.
2. Go to file menu and open new file and draw the circuit diagram (Program) and save it.
3. Go to simulate menu and run the program.
4. If any errors correct them.
5. Observe the input and output waveforms by double clicking XCS1 & XCS1 (Oscilloscope) on and find gain. And compare this value of gain with theoretical value.

PROGRAM (CIRCUIT DIAGRAM):

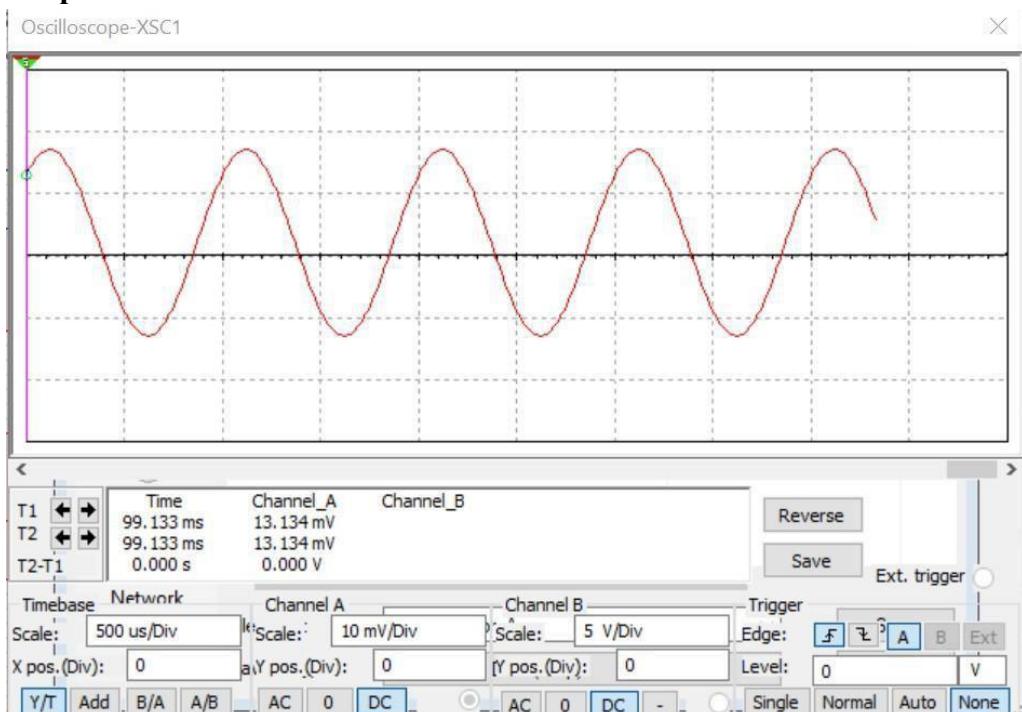


OBSERVATIONS:-

Input Waveform at XCS2



Output Waveforms at XCS2:



CALCULATIONS:-

Theoretical value of gain:

$$A_v = \frac{V_{\text{out}}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{\text{gain}}}\right) \frac{R_3}{R_2}$$

Since all the values of resistors are taken 1k in the simulations. Hence putting in above equation;

$$Av = (1 + (2*1/1)*1)$$

$$Av = 3$$

Practical Value of gain:

$$A_v = \frac{V_{\text{out}}}{V_2 - V_1}$$

Since $V_{\text{out}} = 13.134\text{mV}$, $V_2 = 7.41\text{mv}$ and $V_1 = 3.704\text{mV}$

$$Av = (13.124\text{ mv}) / (7.41\text{mv} - 3.704\text{mV})$$

$$Av = 3.344$$

RESULT:-

CONCLUSION:-

Experiment No.:
Title: OP-AMP Parameters

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM: -To study following Op- amp parameters & compare with specifications given in data sheet.

- a) Input bias current
- b) Input offset current
- c) Input offset voltage
- d) Slew rate
- e) CMRR

THEORY:-

1. Input Offset Current (I_{IO})

Though for an ideal op-amp the input impedance is infinite, it is not so practically. So the IC draws current from the source of the voltage, however small it may be.

The algebraic difference between the currents into the inverting and non-inverting terminals is referred to as input offset current I_{IO} .

$$I_{IO} = |IB_1 - IB_2|$$

This is shown in Fig

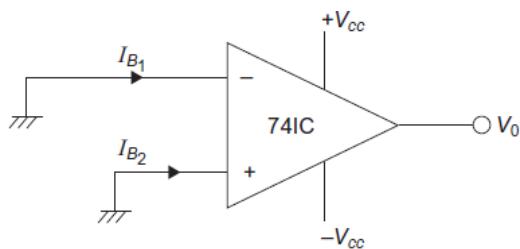


Fig. 1: Input Offset Current

For an ideal op-amp, $I_{IO} = 0$. The typical value for a practical op-amp = 100 nA
 For precision op-amp 741C, the value typically is 6 nA.

2. Input Offset Voltage (V_{io})

If no external **input signal** is applied to the op-amp at the inverting and non-inverting input terminals the output must be zero. That is, if $V_1 = 0$, $V_o = 0$. But as a result of the given biasing supply voltages, $+V_{cc}$ and $-V_{cc}$, a finite bias current is drawn by the op-amp, and as a result of un symmetry on the differential amplifier configuration, the output will not be zero. This is known as **offset**.

Since V_o must be zero when $V_1 = 0$, the input signal must be applied such that the output offset is cancelled and V_o is made zero. This is known as **input offset voltage**.

It is the voltage that must be applied between the two input terminals of an op-amp to nullify output.

This is shown in Fig. . The value for ideal op-amp is $V_{io} = 0$ V. Practical value = 100 uV (typical).

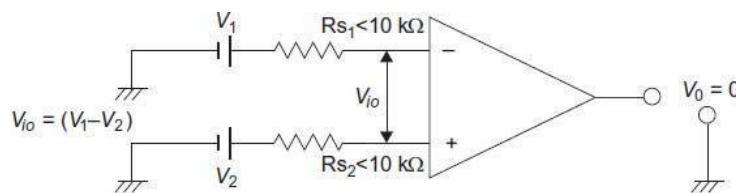


Fig. : Input Offset Voltage

3. Output Bias Current (/B)

This is the average of the currents that flow into the inverting and non-inverting input terminals of the op-amp.

$$I_B = \frac{I_{B_1} + I_{B_2}}{2}$$

4. Common Mode Rejection Ratio [CMRR]

This parameter indicates the capability of the op-amp to reject noise. **The higher the value of CMRR, the better it is.**

CMRR is defined as the ratio of the differential voltage gain, A_d , to the common mode voltage gain, A_{cm} (cm = common mode)

$$CMRR = \frac{A_d}{A_{cm}}$$

The op-amp has a differential voltage amplifier configuration. A_d is usually large. A_{cm} is small. Hence, the value of CMRR is large.

5. Slew Rate (SR)

This is defined as **the maximum rate of change of output voltage per unit time**.

The input capacitance of the op-amp circuit prevents it from responding instantaneously to high frequency signals. If a square wave input or pulse of high frequency is applied as input, at the output the slope of the leading edge and trailing edge is measured and the larger values computed. This gives SR.

$$SR = \left. \frac{\Delta V_o}{\Delta t} \right|_{max} \text{ V}/\mu\text{sec}$$

Ideal value is infinite, Practical value = 0.01 V/ sec.

6. Input Resistance (R_i)

This is **the equivalent resistance of the IC measured at either the inverting or non-inverting input terminal, with the other terminal connected to the ground**.

Ideal value is infinity, Practical value is 2 Mohm.

For JFET op-amps, typical value of R_i is 10^{12} ohm.

7. Power Supply Rejection Ratio (PSRR)

The input offset voltage V_{io} of the op-amp changes if the bias power supply of the op-amp changes. The change of V_{io} with $+V_{cc}$ or $-V_{ee}$ is called the PSRR. The term is also called the **supply voltage rejection ratio (SVRR) or power supply sensitivity (PSS)**.

PSRR is defined as the ratio of change in the input offset voltage V_{io} with a change in one of the bias power supplying V_{cc} , when the other power supply is held constant.

$$PSRR = \frac{\Delta V_{io}}{\Delta V} \text{ } \mu\text{V/V}$$

Ideal value = 0, Practical value = 150 $\mu\text{V/V}$

CONCLUSION:-

Experiment No.:
Title: DIFFERENTIATOR

Name of the Student:

Batch:

Date of Performance:

Date of Submission:

Remark:

Roll. No.	Practical (5)	Oral (5)	Total (10)	Remark	Sign. with date

AIM:

To design a Differentiator circuit for the given specifications using Op-Amp IC 741.

THEORY:

The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1 . The expression for the output voltage is given as,

$$V_o = -R_f C_1 \left(\frac{dV_i}{dt} \right)$$

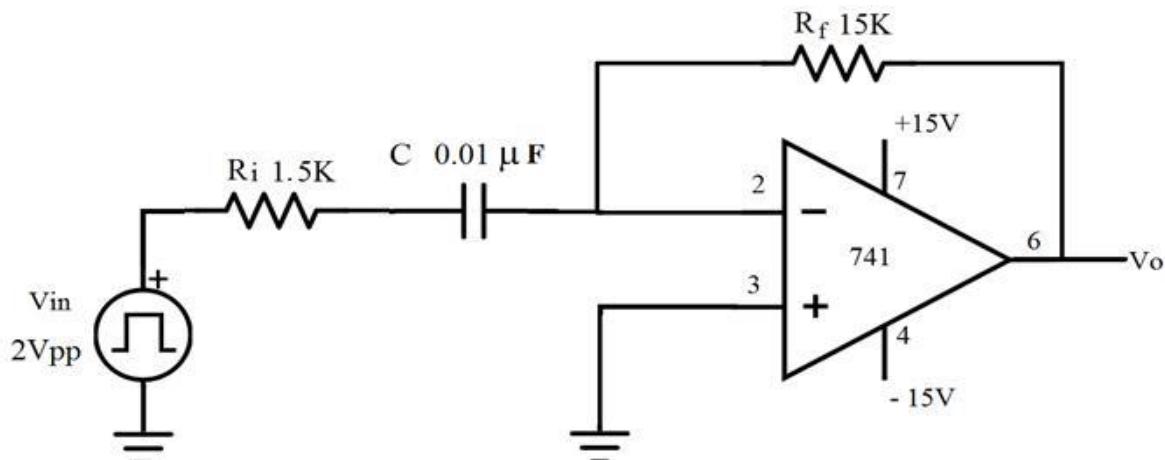
Here the negative sign indicates that the output voltage is 180° out of phase with the input signal. A resistor $R_{comp} = R_f$ is normally connected to the non-inverting input terminal of the op-amp to compensate for the input bias current. A workable differentiator can be designed by implementing the following steps:

1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of $C_1 < 1 \mu F$, calculate the value of R_f .

2. Choose $f_b = 20 f_a$ and calculate the values of R_1 and C_f so that $R_1 C_1 = R_f C_f$.

The differentiator is most commonly used in wave shaping circuits to detect high frequency components in an input signal and also as a rate-of-change detector in FM modulators.

CIRCUIT DIAGRAM OF DIFFERENTIATOR:



DESIGN :

Given $f = 1 \text{ KHz}$

So $T = 1/f = 1\text{ms}$

Design equation is $T = 2\pi R_f C$

Let $C = 0.01\mu\text{F}$

Then $R_f = 15\text{K}\Omega$

Let $R_i = R_f/10 = 1.5\text{K}\Omega$

[To design a differentiator circuit to differentiate an input signal that varies in frequency from 10

Hz to about 1 KHz. If a sine wave of 1 V peak at 1000Hz is applied to the differentiator, draw

its output waveform.]

Given $f_a = 1 \text{ KHz}$

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_f C_1)$

Let us assume $C_1 = 0.1 \mu\text{F}$; then

$R_f = \underline{\hspace{2cm}}$

Since $f_b = 20 f_a$, $f_b = 20 \text{ KHz}$

We know that the gain limiting frequency $f_b = 1 / (2\pi R_1 C_1)$

Hence $R_1 = \underline{\hspace{2cm}}$

Also since $R_1 C_1 = R_f C_f$; $C_f = \underline{\hspace{2cm}}$

Given $V_p = 1 \text{ V}$ and $f = 1000 \text{ Hz}$, the input voltage is $V_i = V_p \sin \omega t$

We know $\omega = 2\pi f$

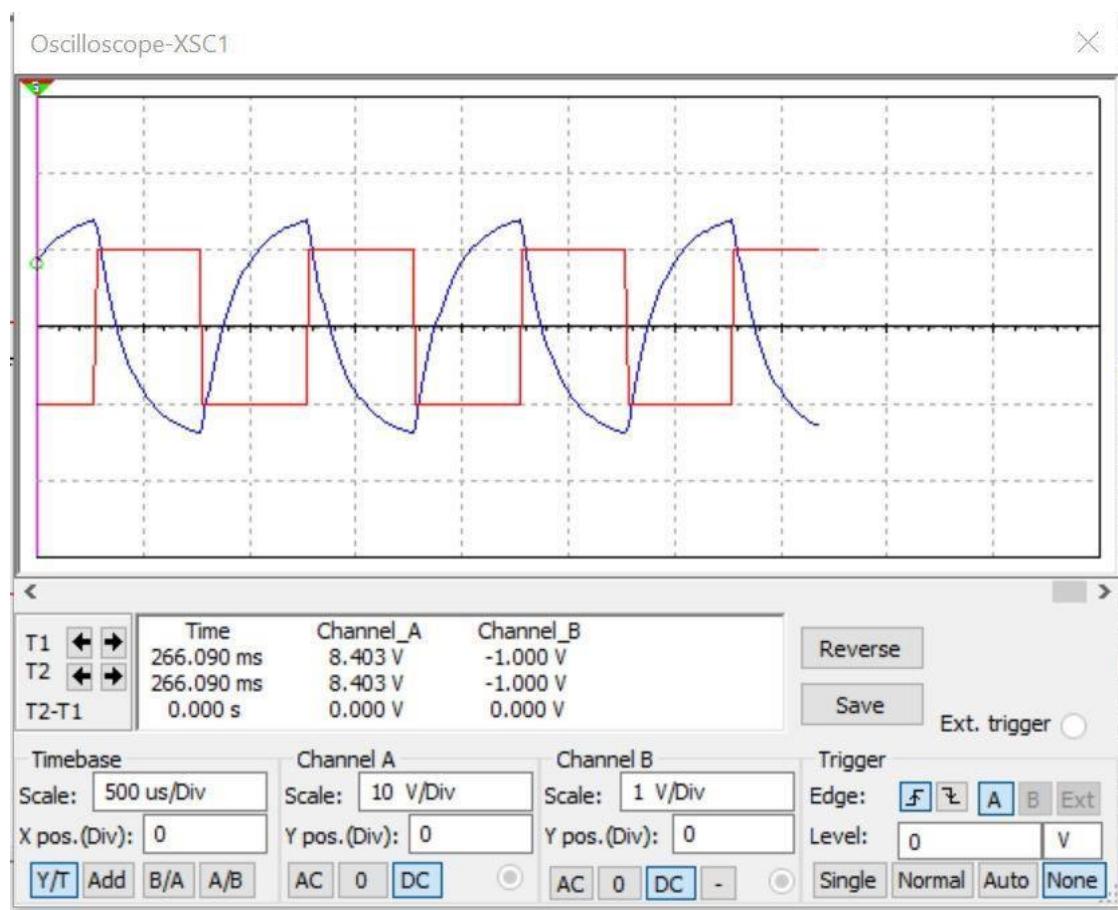
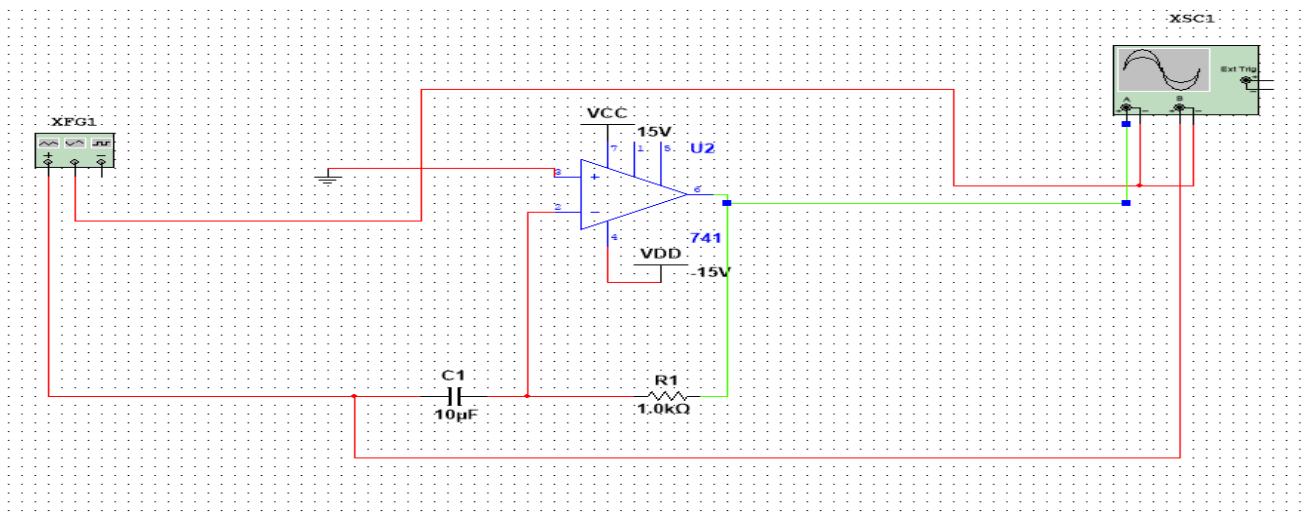
Hence

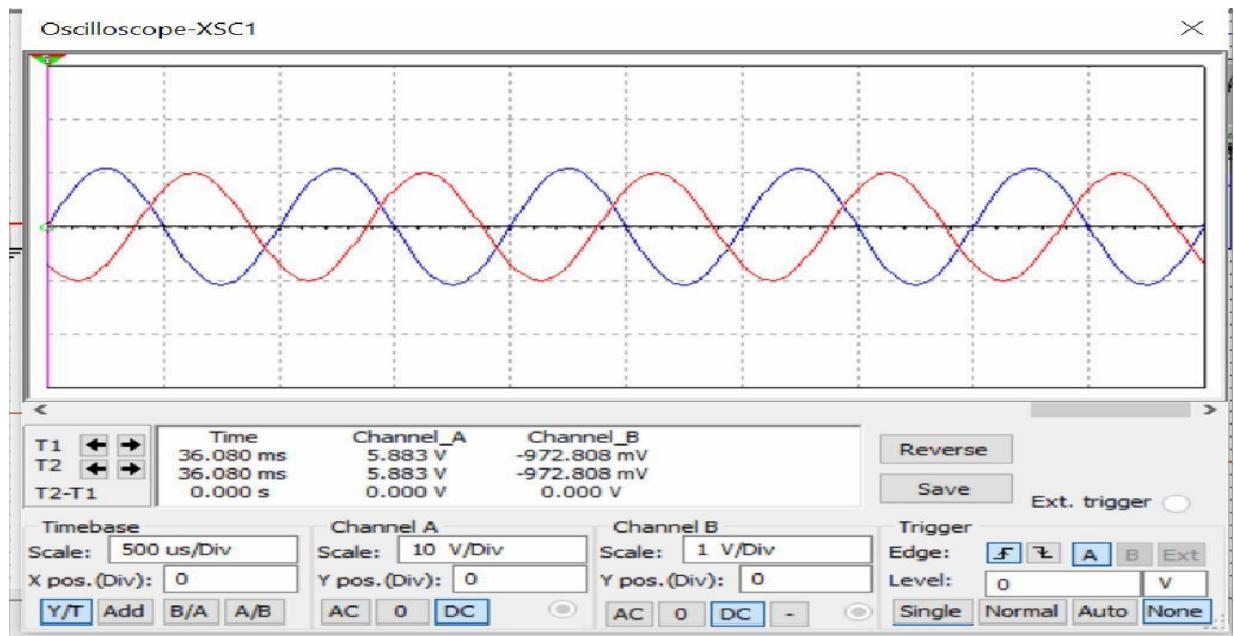
$$V_o = -R_f C_1 (dV_i/dt)$$

$$= -0.94 \cos \omega t$$

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + Vcc and - Vcc supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.





CONCLUSION: