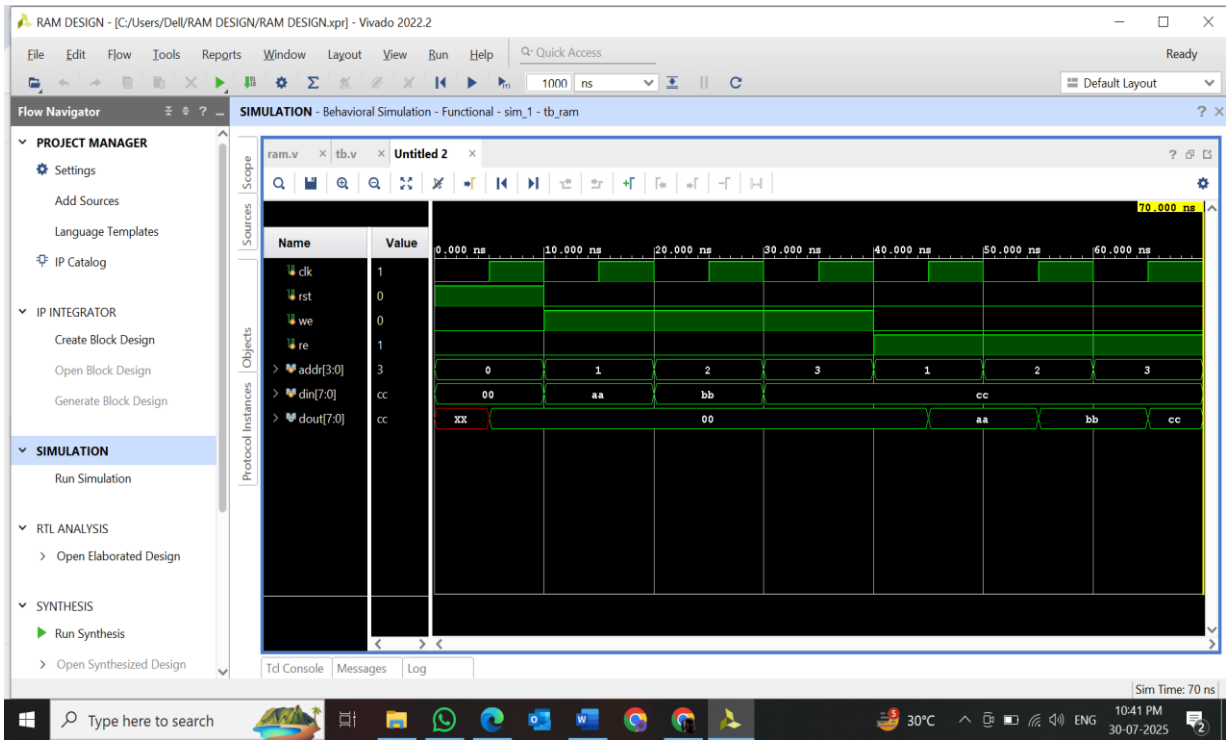
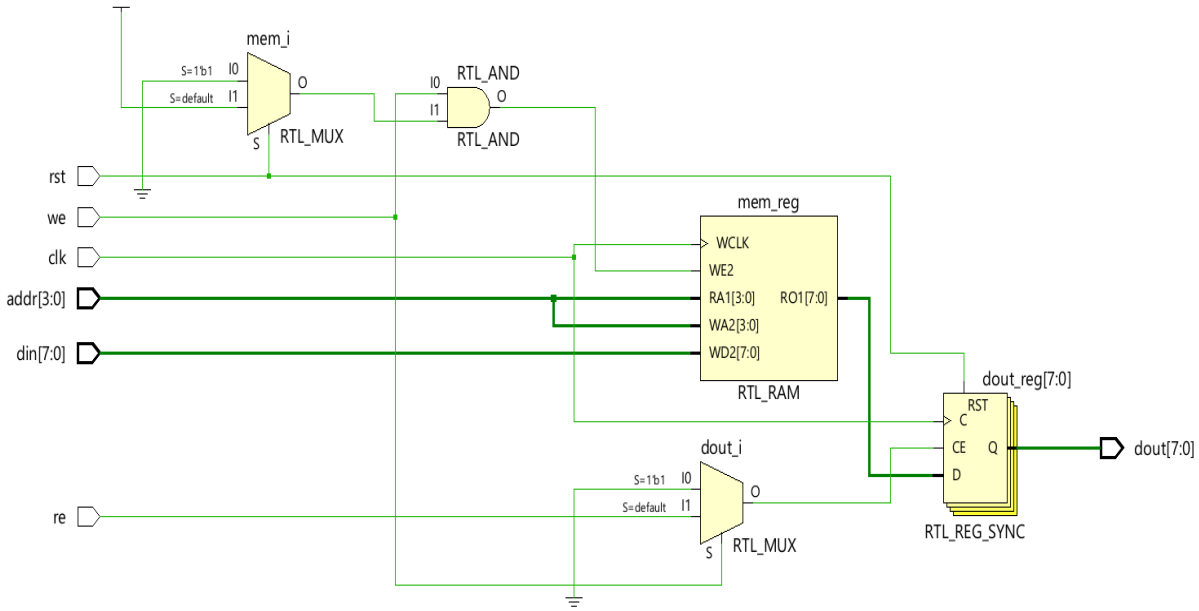
RAM DESIGN:

Waveform:



Elaborated Design:



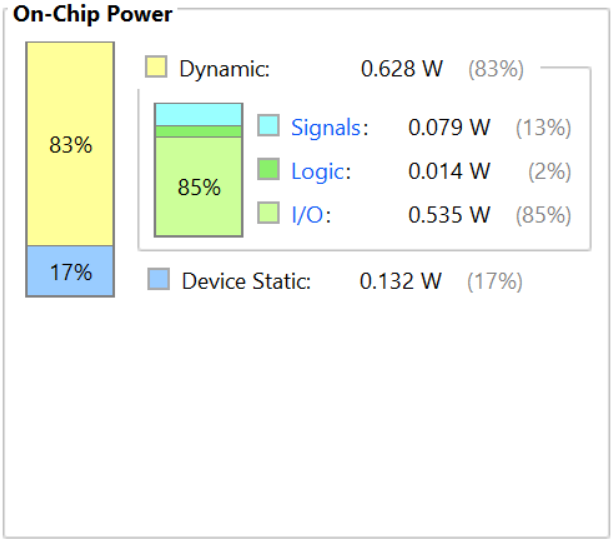
Reports:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.76 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.4°C**
Thermal Margin:	58.6°C (31.0 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Name 1	Slice LUTs (134600)	Slice Registers (269200)	Slice (33650)	LUT as Logic (134600)	LUT as Memory (46200)	Bonded IOB (400)	BUFGCTRL (32)
N ram	10	8	3	2	8	24	1

Name	Port	I/O Std	Vcco	Slew	Drive Strength (...	Off-Chip Termina...	Remaining Margin...	Notes
I/O Bank 0 (0)								
I/O Bank 12 (0)								
I/O Bank 13 (0)								
I/O Bank 14 (8)		LVCMOS18	1.80	SLOW	12	FP_VTT_50		
P24	dout[0]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	85.19	
P23	dout[1]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	85.19	
N19	dout[2]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	85.19	
P19	dout[3]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	85.19	
N24	dout[4]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	85.19	
N23	dout[5]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	85.19	
P21	dout[6]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	85.19	
P20	dout[7]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	85.19	
I/O Bank 15 (0)								
I/O Bank 16 (0)								
I/O Bank 33 (0)								
I/O Bank 34 (0)								
I/O Bank 35 (0)								

Design Timing Summary

Setup

Worst Negative Slack (WNS):	inf
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	80

Hold

Worst Hold Slack (WHS):	inf
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	80

Pulse Width

Worst Pulse Width Slack (WPWS):	NA
Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA

There are no user specified timing constraints.