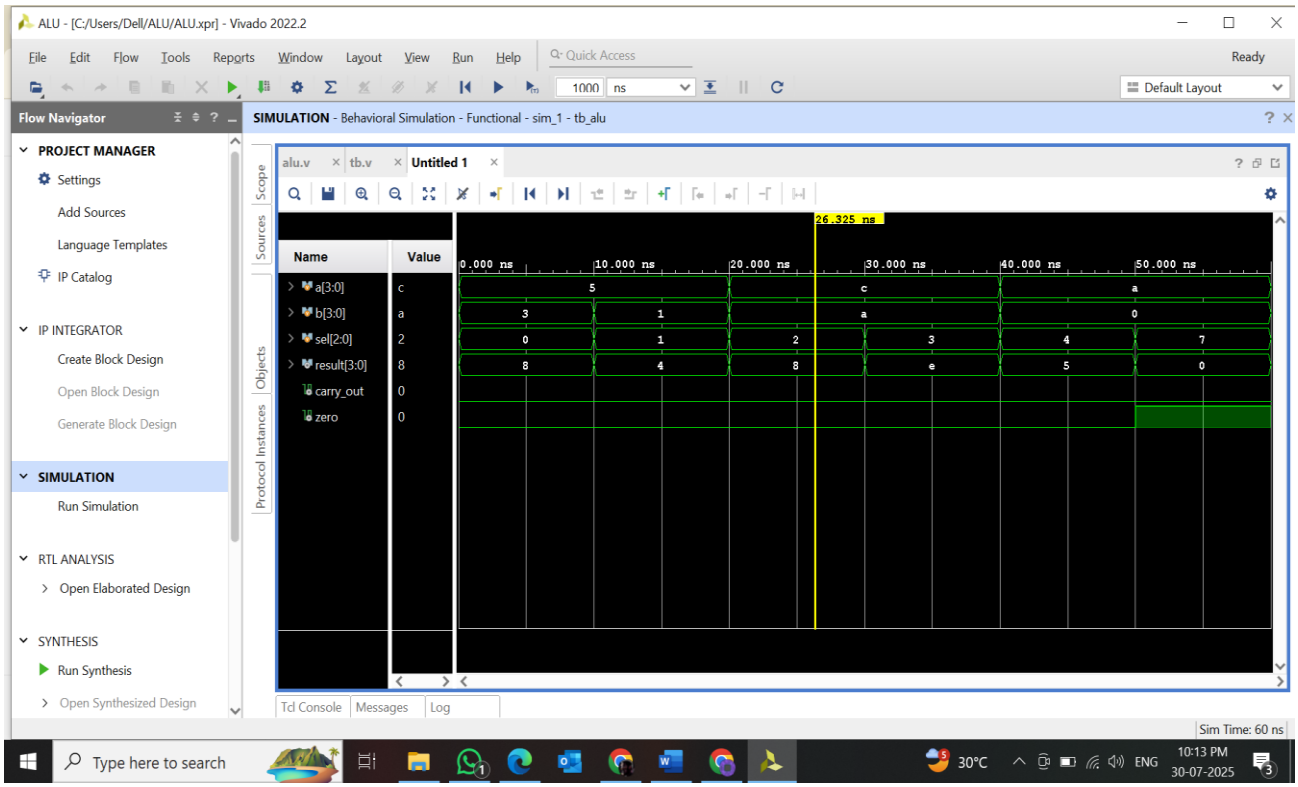
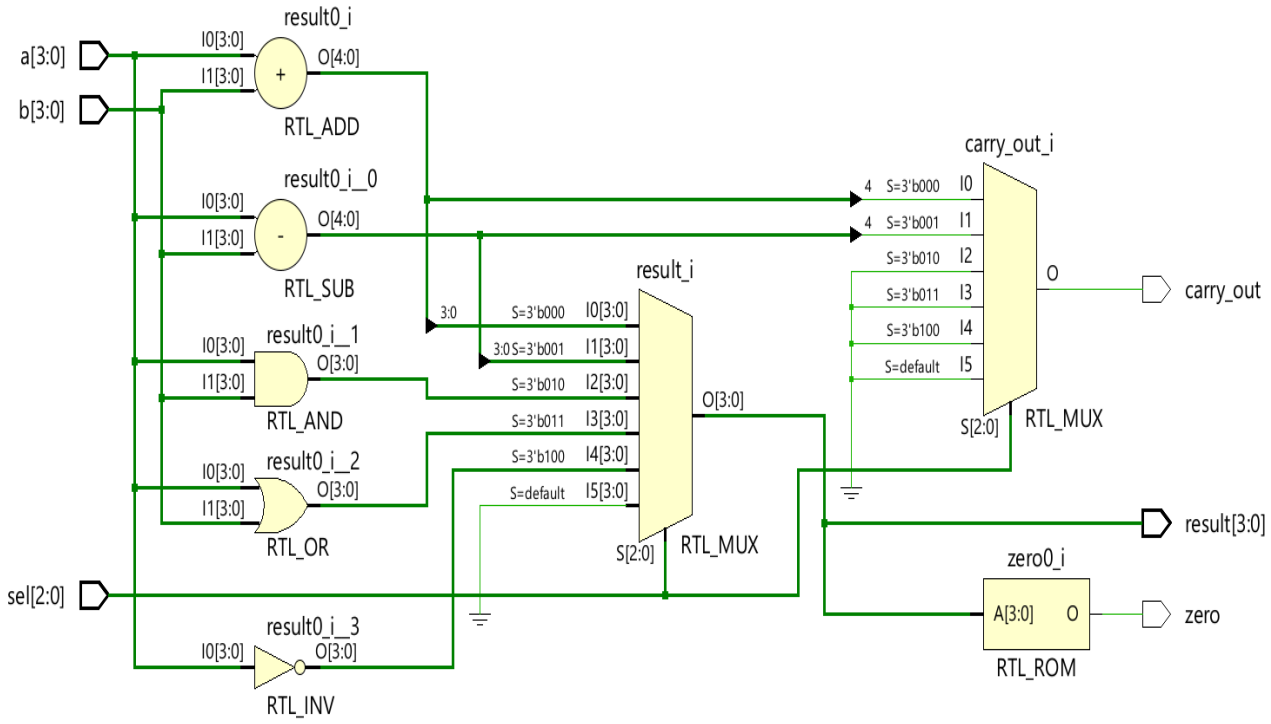
ARITHMETIC LOGIC UNIT(ALU):

Waveform:



Elaborated Design:



Reports:

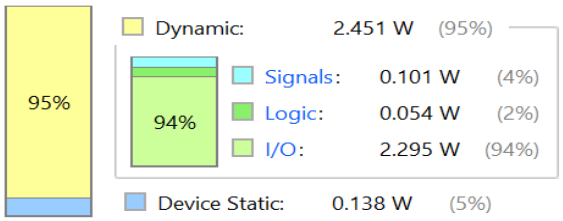
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.589 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**29.8°C**
Thermal Margin:	55.2°C (29.2 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power



Name	Slice LUTs (134600)	Slice (33650)	LUT as Logic (134600)	Bonded IOB (400)
N alu	11	4	11	17

Design Timing Summary

Setup

Worst Negative Slack (WNS):	inf
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	6

Hold

Worst Hold Slack (WHS):	inf
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	6

Pulse Width

Worst Pulse Width Slack (WPWS):	NA
Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA

There are no user specified timing constraints.

Name	Port	I/O Std	Vcco	Slew	Drive Strength (...	Off-Chip Termina...	Remaining Margin...	Notes
I/O Bank 0 (0)								
I/O Bank 12 (0)								
I/O Bank 13 (0)								
I/O Bank 14 (6)		LVCMOS18	1.80	SLOW	12	FP_VTT_50		
P24	carry_out	LVCMOS18	1.80	SLOW	12	FP_VTT_50	88.89	
P25	result[0]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	88.89	
R25	result[1]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	88.89	
R21	result[2]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	88.89	
R20	result[3]	LVCMOS18	1.80	SLOW	12	FP_VTT_50	88.89	
P23	zero	LVCMOS18	1.80	SLOW	12	FP_VTT_50	88.89	
I/O Bank 15 (0)								
I/O Bank 16 (0)								
I/O Bank 33 (0)								
I/O Bank 34 (0)								
I/O Bank 35 (0)								