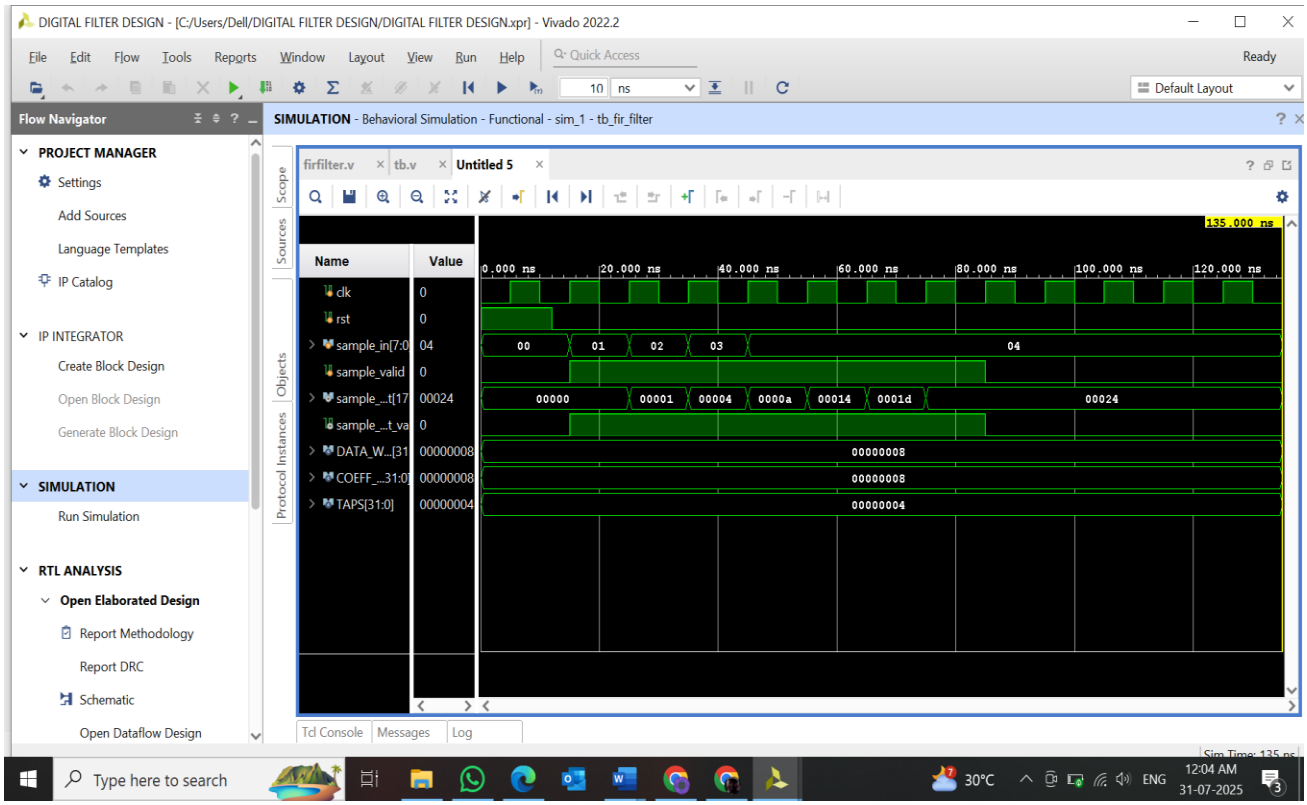
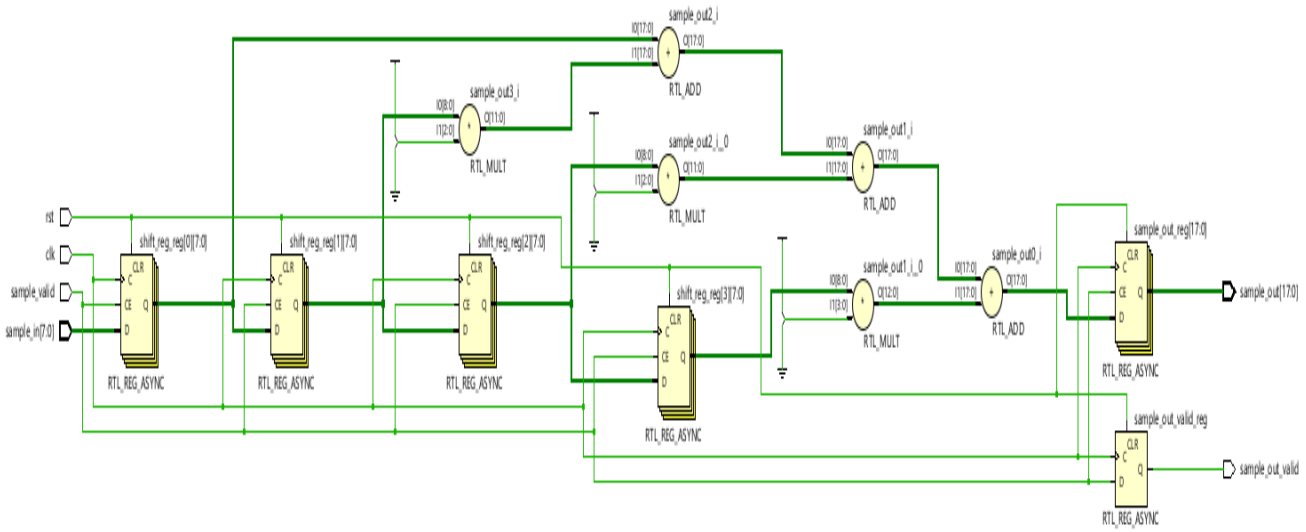
DIGITAL FILTER DESIGN:

Waveform:



Elaborated Design:



Reports:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	171	Total Number of Endpoints:	171	Total Number of Endpoints:	NA

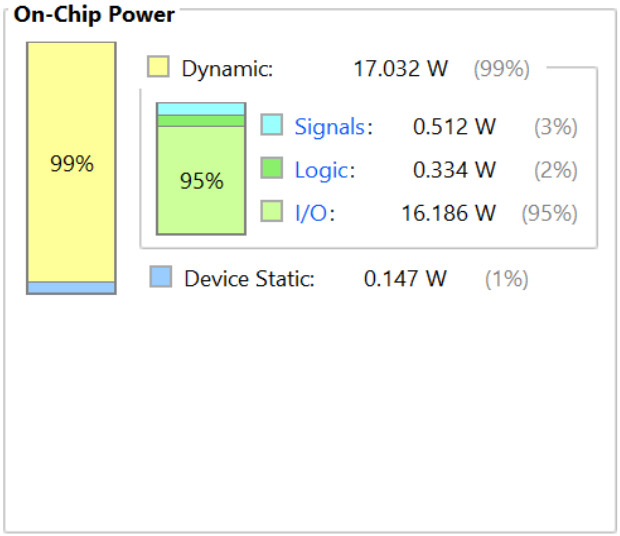
There are no user specified timing constraints.

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**17.179 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**57.4°C**
Thermal Margin:	27.6°C (14.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Name 1	Slice LUTs (41000)	Slice Registers (82000)	Slice (10250)	LUT as Logic (41000)	Bonded IOB (300)	BUFGCTRL (32)
N fir_filter	42	51	18	42	30	1