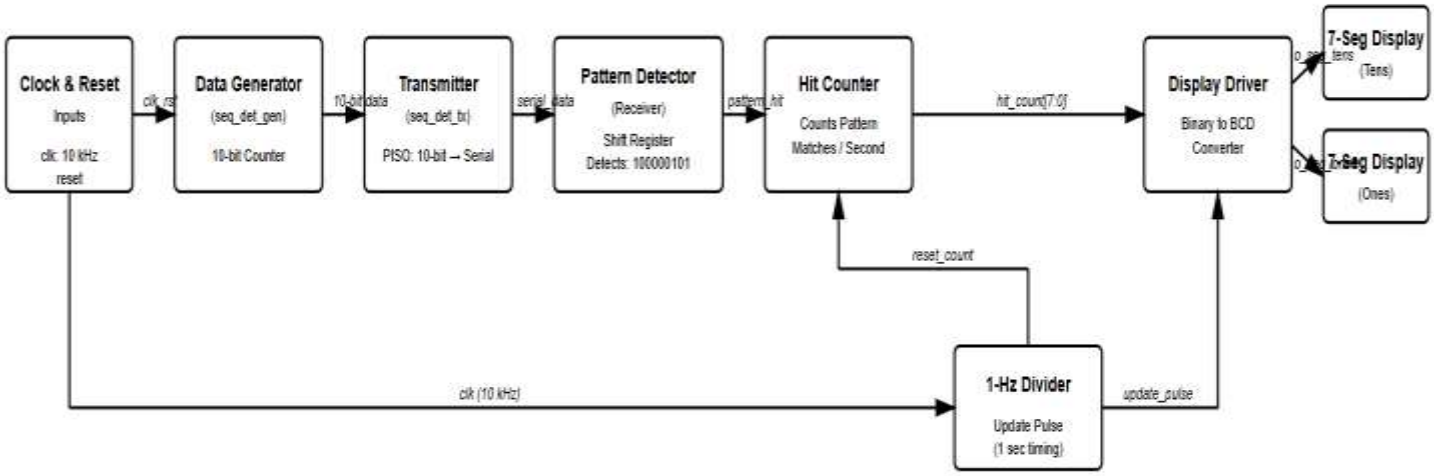
HAPPY BIRTHDAY DESIGN PROBLEM

The Problem Statement has been already shared with specifications. This Report is made for the evaluation criteria.

1.Understanding and Block Diagram Development:

- **Transmits** a continuous 10-bit counter sequence (data generator + PISO transmitter).
- **Receives** the serial bitstream and **detects a 9-bit "birthday" pattern** (month+date).
- **Counts** how many times that pattern appears every second.
- **Displays** the count on **two seven-segment displays** (ones and tens).



2. Implementation Status:

Component	Module Name	Function	Implementation Status
Data Generator	seq_det_gen	10-bit counter producing serial frames	✔ Implemented
Transmitter (PISO)	seq_det_tx	Parallel-to-Serial data transmission	✔ Implemented

Receiver (Pattern Detector)	seq_det_rx	Detects 9-bit pattern 100000101	✔ Implemented
Hit Counter	(inside seq_det_rx)	Counts detected patterns per second	✔ Implemented
1-Hz Divider	(inside seq_det_rx)	Divides 10 kHz clock to 1 Hz	✔ Implemented
Display Driver	bcd_to_7seg	Converts binary to 7-segment display format	✔ Implemented
Top Module Integration	happy_birthday_top	Connects all blocks & outputs hit count	✔ Implemented
Testbench	tb_happy_birthday_top	Simulates full system behavior	✔ Implemented and validated

3.Code Quality:

https://drive.google.com/drive/folders/1cR7-EkucXS3Xh7xAJjfZQS7zuJppcRrU?usp=drive_link

Project Folder - Vivaodo

Module Descriptions:

Module	**Function**	**Clock/Timing correctness**
seq_det_gen	10-bit counter, increments once per transmitted frame (10 bits).	Since i_count_valid pulses once every 10 clocks (via tx_done), you get 1 kHz frame rate at 10 kHz clock.
seq_det_tx	Serially transmits 10-bit word, 1 bit per clock.	Perfectly matches generator timing. One full word = 10 clocks.
seq_det_tx_top	Integrates generator + transmitter, triggers new word every 10 clocks.	Continuous 1 kHz frame flow.
seq_det_rx	Receives serial stream, checks for 9-bit pattern, counts hits every "1 s" (10 000 clocks).	Your divider sec_div == 9999 gives 1 Hz from 10 kHz — i.e., a 1 s display refresh.
bcd_to_7seg	Converts 4-bit BCD digits to segment pattern.	No timing dependence.
happy_birthday_top	Top integration: connects TX + RX + display logic.	Clean interface, no clock-domain mismatch.
tb_happy_birthday_top	Drives 10 kHz simulation clock (#50 delay → 100 µs period).	Perfect simulation for the same 10 kHz system.