DESIGN AND IMPLEMENTATION OF RADIX-4 BOOTH ALGORITHM

FRONT-END PART

RTL DESIGN

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1. INTRODUCTION

The Booth multiplication algorithm is a fundamental technique used to perform signed multiplication efficiently. Radix-2 Booth is a classic approach; however, its performance becomes a bottleneck in high-speed digital systems. To overcome this, the Radix-4 Booth algorithm has been developed to optimize speed, reduce switching activity, and improve overall resource usage in digital multipliers.

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2. OBJECTIVE

- To analyze and implement a **Radix-4 Booth multiplier**.
- To compare it with the **Radix-2 Booth algorithm** in terms of speed, area, and resource utilization.
- To target **FPGA implementation** for hardware acceleration in DSP and embedded systems.

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3. NEED FOR ENHANCEMENT

Parameter	**Radix-2 Booth**	**Radix-4 Booth**
Operations/Cycle	1 bit per cycle	2 bits per cycle
Speed	Slower	Faster
Partial Products	More	Fewer
Switching Activity	Higher	Lower
Power Consumption	Higher	Lower (in optimized design)
Area	Moderate	Slightly more, but optimized

Why Radix-4?

Radix-4 examines 3 bits at a time (X[i+1], X[i], X[i−1]), allowing it to encode and skip more bits per step. This reduces the number of partial products by ~50%, improving performance.

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4. Design Methodology

- Implemented in **Verilog HDL**.
- Targeted on **FPGA platform**.
- Used **signed 8-bit** multiplicand and multiplier.
- Simulation and verification done using **Vivado Simulator**.
- Resource synthesis report obtained using **Vivado**.

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5. Advantages of Radix-4 Booth Algorithm

- **Reduced Partial Products:** Operates on 2 bits per cycle instead of 1.
- **Higher Speed:** Suitable for high-speed arithmetic logic units (ALUs).
- **Efficient Pipelining:** Better for pipeline stages in DSPs.
- **Optimized Switching:** Reduces power consumption in optimized hardware.
- **Good FPGA Fit:** Utilizes fewer DSP slices and BRAMs for same operand width.

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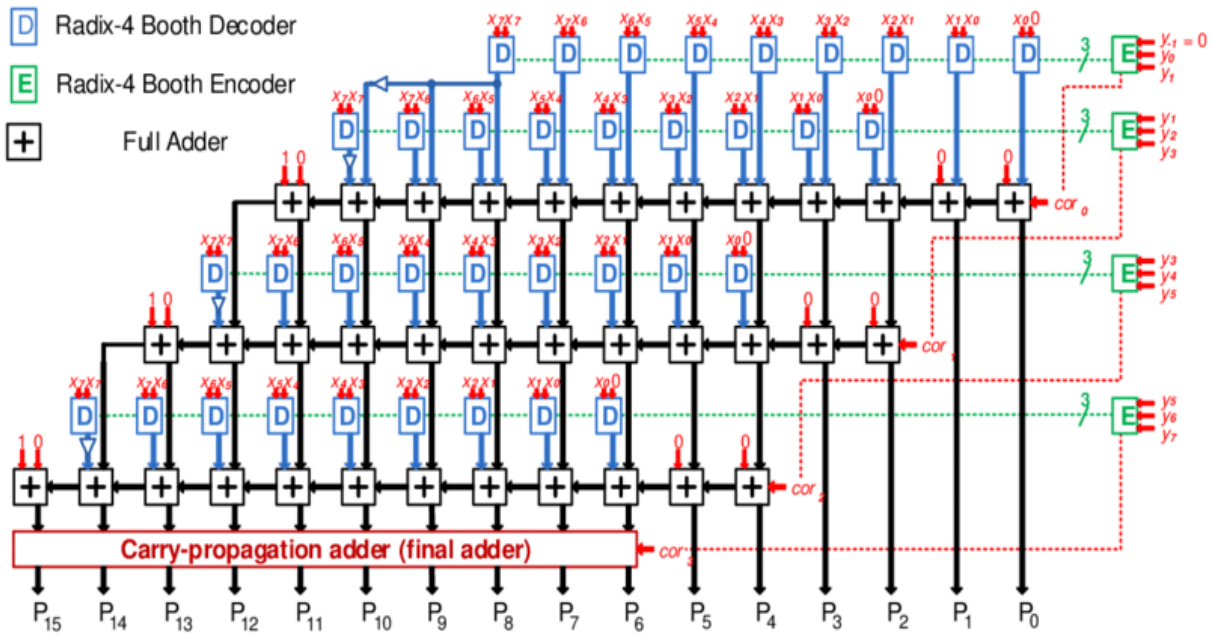
6. Applications

- **Digital Signal Processing (DSP)**
  Fast convolution, filtering, and FFT operations.
- **Image and Video Processing**
  Pixel-wise multiplication, scaling, transformation.
- **Cryptographic Systems**
  Modular multipliers used in RSA/ECC.
- **Embedded Systems and IoT Edge Devices**
  Efficient multipliers in resource-constrained environments.
- **Machine Learning Accelerators**
  Dot-product and matrix-multiplication-heavy operations.

BLOCK DIAGRAM



ALGORITHM WORKING

RADIX-4

RADIX-2

Y_i	Y_{i-1}	Partial Product
0	0	0×Multiplicand
0	1	1×Multiplicand
1	0	-1×Multiplicand
1	1	0×Multiplicand

Partial Product Selection Table

Multiplier Bits		Multiple Selection
X_{i+1} X_i	X_{i-1}	
00	0	+0
00	1	+M
01	0	+M
01	1	+2M
10	0	-2M
10	1	-M

Goal:

Multiply two signed binary numbers using fewer steps by reducing the number of partial products (PPs), increasing speed compared to Radix-2 Booth.

Key Concepts:

- Radix-4 groups **3 bits** of the multiplier at a time:
  X[i+1] X[i] X[i-1]
- Each group **overlaps** with the previous by 1 bit.
- Each group determines a **Booth recoding** to generate partial products:

Group (Xi+1 Xi Xi−1)	Operation	Value
000 / 111	0 × M	0
001 / 010	+1 × M	M
011	+2 × M	2M
100	−2 × M	−2M
101 / 110	−1 × M	−M

- **M** = Multiplicand
- **X** = Multiplier
- This allows skipping over 2 bits at a time → **fewer partial products**

Algorithm Steps:

Step 1: Inputs

- Multiplicand = M (n-bit signed)
- Multiplier = Q (n-bit signed)
- Append 0 to the LSB of multiplier → Q[-1] = 0
- Group multiplier bits in **overlapping triplets**

Step 2: Booth Encoding

- For each group of 3 bits, use Booth table to determine operation.

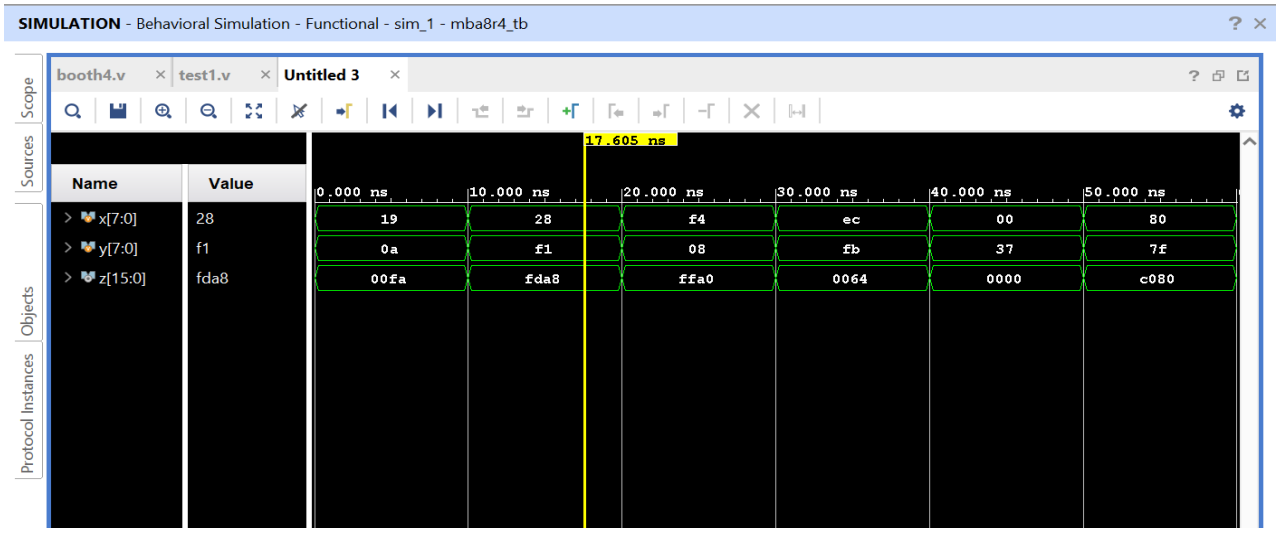
Step 3: Generate Partial Products

- Based on Booth encoding, generate 0, ±M, or ±2M
- Shift appropriately (like multiplying by powers of 4)

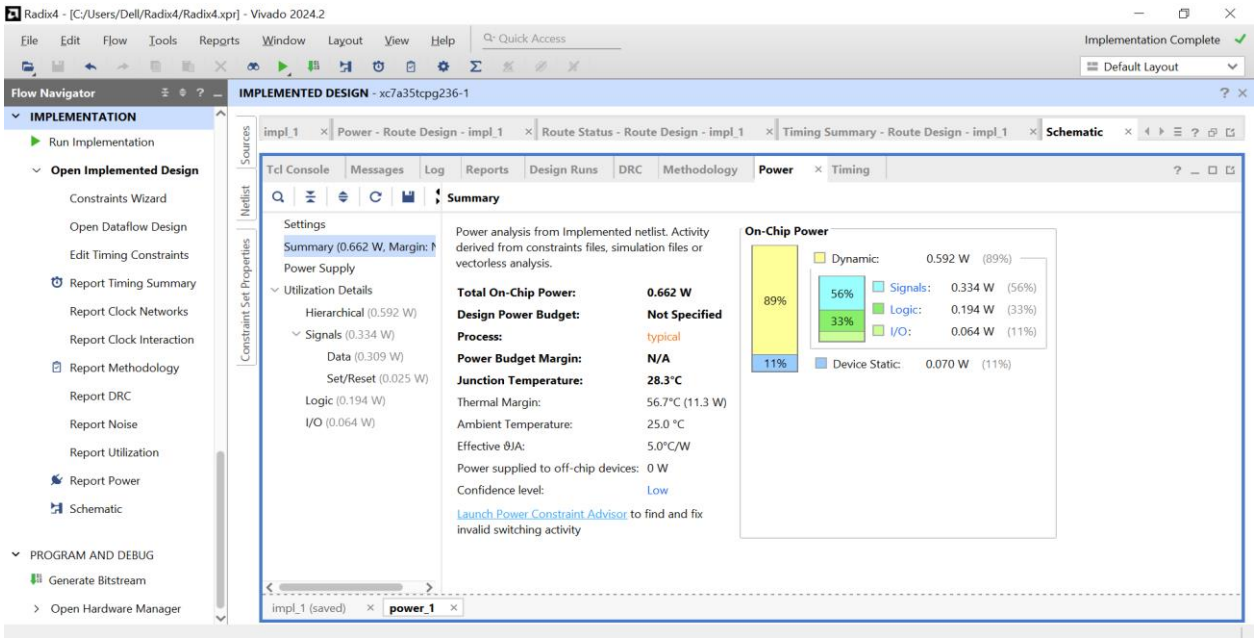
Step 4: Sum Partial Products

- Add up all the shifted partial products using addition or Wallace tree.

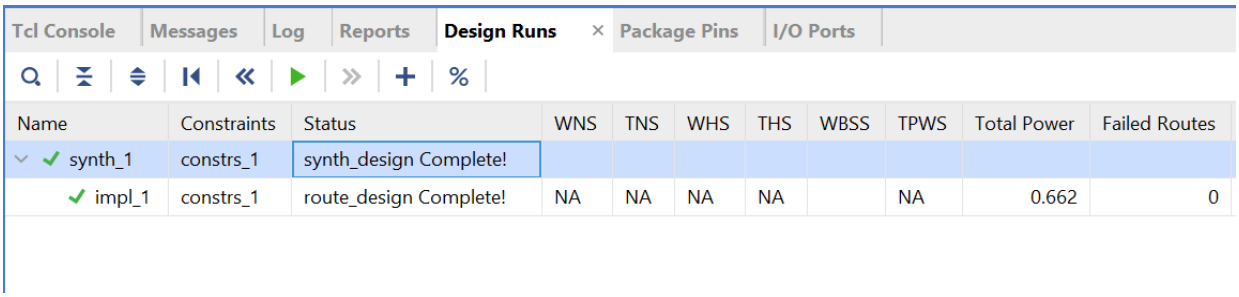
SIMULATION OUTPUT:



POWER REPORT:



SUCCESSFUL SYNTHESIS :



Utilization Design Information

Table of Contents
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1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	86	0	0	20800	0.41
LUT as Logic	86	0	0	20800	0.41
LUT as Memory	0	0	0	9600	0.00
Slice Registers	40	0	0	41600	0.10
Register as Flip Flop	0	0	0	41600	0.00
Register as Latch	40	0	0	41600	0.10
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.
Warning! LUT value is adjusted to account for LUT combining.
Warning! For any ECO changes, please run place_design if there are unplaced instances

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset

0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
40	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-
+-------+-------------+-------------+-------------+

2. Memory

+---------------+------+-------+------------+-----------+-------+
| Site Type | Used | Fixed | Prohibited | Available | Util% |
+---------------+------+-------+------------+-----------+-------+
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00
+---------------+------+-------+------------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

+-----------+------+-------+------------+-----------+-------+
| Site Type | Used | Fixed | Prohibited | Available | Util% |
+-----------+------+-------+------------+-----------+-------+
| DSPs | 0 | 0 | 0 | 90 | 0.00 |
+-----------+------+-------+------------+-----------+-------+

4. IO and GT Specific

+----------------------------+------+-------+------------+-----------+-------+
| Site Type | Used | Fixed | Prohibited | Available | Util% |
+----------------------------+------+-------+------------+-----------+-------+
Bonded IOB	32	0	0	106	30.19
Bonded IPADs	0	0	0	10	0.00
Bonded OPADs	0	0	0	4	0.00
PHY_CONTROL	0	0	0	5	0.00
PHASER_REF	0	0	0	5	0.00

OUT_FIFO	0	0	0	20	0.00
IN_FIFO	0	0	0	20	0.00
IDELAYCTRL	0	0	0	5	0.00
IBUFDS	0	0	0	104	0.00
GTPE2_CHANNEL	0	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	250	0.00
IBUFDS_GTE2	0	0	0	2	0.00
ILOGIC	0	0	0	106	0.00
OLOGIC	0	0	0	106	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	0	0	0	32	0.00
BUFIO	0	0	0	20	0.00
MMCME2_ADV	0	0	0	5	0.00
PLLE2_ADV	0	0	0	5	0.00
BUFMRCE	0	0	0	10	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	20	0.00

6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
PCIE_2_1	0	0	0	1	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT6	42	LUT
LDCE	40	Flop & Latch
LUT5	28	LUT
LUT3	22	LUT
OBUF	16	IO
IBUF	16	IO
LUT4	8	LUT
LUT2	4	LUT

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

Ref Name	Used

```
#-----------------------------------------------------------
# Vivado v2024.2 (64-bit)
# SW Build 5239630 on Fri Nov 08 22:35:27 MST 2024
# IP Build 5239520 on Sun Nov 10 16:12:51 MST 2024
# SharedData Build 5239561 on Fri Nov 08 14:39:27 MST 2024
# Start of session at: Fri Apr 18 11:57:16 2025
# Process ID         : 14620
# Current directory  : C:/Users/Dell/Radix4/Radix4.runs/synth_1
# Command line       : vivado.exe -log mba8r4.vds -product Vivado -mode batch -messageDb
vivado.pb -notrace -source mba8r4.tcl
# Log file           : C:/Users/Dell/Radix4/Radix4.runs/synth_1/mba8r4.vds
# Journal file       : C:/Users/Dell/Radix4/Radix4.runs/synth_1\vivado.jou
# Running On         : DESKTOP-MNO8N4K
# Platform           : Windows Server 2016 or Windows 10
# Operating System   : 19045
# Processor Detail   : Intel(R) Core(TM) i5-6300U CPU @ 2.40GHz
# CPU Frequency      : 2496 MHz
# CPU Physical cores : 2
# CPU Logical cores  : 4
# Host memory        : 8476 MB
# Swap memory        : 3856 MB
# Total Virtual      : 12332 MB
# Available Virtual  : 1570 MB
#-----------------------------------------------------------
source mba8r4.tcl -notrace
Command: synth_design -top mba8r4 -part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: [Synth 8-7079] Multithreading enabled for synth_design using a maximum of 2
processes.
INFO: [Synth 8-7078] Launching helper process for spawning children vivado processes
INFO: [Synth 8-7075] Helper process launched with PID 11488
---------------------------------------------------------------------------------
Starting Synthesize : Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak =
843.652 ; gain = 476.117
---------------------------------------------------------------------------------
Finished Synthesize : Time (s): cpu = 00:00:13 ; elapsed = 00:00:14 . Memory (MB): peak =
949.906 ; gain = 582.371
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:14 ; elapsed = 00:00:15 . Memory
(MB): peak = 949.906 ; gain = 582.371
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
```

```
---------------------------------------------------------------------------------
Loading part: xc7a35tcpg236-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:14 ; elapsed =
00:00:15 . Memory (MB): peak = 949.906 ; gain = 582.371
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a35tcpg236-1
WARNING: [Synth 8-327] inferring latch for variable 'm_reg'
[C:/Users/Dell/Radix4/Radix4.srcs/sources_1/new/booth4.v:24]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:15 ; elapsed = 00:00:15 .
Memory (MB): peak = 949.906 ; gain = 582.371
---------------------------------------------------------------------------------
No constraint files found.
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
        2 Input   16 Bit       Adders := 4
+---XORs :
        2 Input      1 Bit         XORs := 6
        3 Input      1 Bit         XORs := 33
+---Muxes :
        2 Input   16 Bit       Muxes := 8
        2 Input   11 Bit       Muxes := 4
        2 Input    1 Bit       Muxes := 4
        3 Input    1 Bit       Muxes := 4
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
No constraint files found.
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:30 ; elapsed =
00:00:40 . Memory (MB): peak = 1170.477 ; gain = 802.941
```

No constraint files found.

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:30 ; elapsed = 00:00:41 . Memory (MB): peak = 1170.477 ; gain = 802.941

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:30 ; elapsed = 00:00:41 . Memory (MB): peak = 1170.477 ; gain = 802.941

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 . Memory (MB): peak = 1331.062 ; gain = 963.527

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 . Memory (MB): peak = 1331.062 ; gain = 963.527

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 .
Memory (MB): peak = 1331.062 ; gain = 963.527

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 .
Memory (MB): peak = 1331.062 ; gain = 963.527

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 .
Memory (MB): peak = 1331.062 ; gain = 963.527

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 .
Memory (MB): peak = 1331.062 ; gain = 963.527

Start Writing Synthesis Report

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
| |Cell |Count |
+------+-----+------+
1	LUT2	4
2	LUT3	22
3	LUT4	8
4	LUT5	28
5	LUT6	42
6	LDC	40
7	IBUF	16
8	OBUF	16

```
Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |   176|
|2     |  i0     |r4     |    30|
|3     |  k0     |r4_0   |    26|
|4     |  kk     |r4_1   |    31|
|5     |  l0     |r4_2   |    57|
+------+---------+-------+------+
--------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 . Memory
(MB): peak = 1331.062 ; gain = 963.527
--------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 14 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 . Memory
(MB): peak = 1331.062 ; gain = 963.527
Synthesis Optimization Complete : Time (s): cpu = 00:00:39 ; elapsed = 00:00:52 . Memory
(MB): peak = 1331.062 ; gain = 963.527
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.004 . Memory (MB):
peak = 1346.090 ; gain = 0.000
INFO: [Netlist 29-17] Analyzing 40 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak
= 1455.281 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 40 instances were transformed.
  LDC => LDCE: 40 instances

Synth Design complete | Checksum: cb43a75c
INFO: [Common 17-83] Releasing license: Synthesis
20 Infos, 14 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:43 ; elapsed = 00:00:58 . Memory (MB): peak =
1455.281 ; gain = 1088.723
Write ShapeDB Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.014 . Memory
(MB): peak = 1455.281 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint
'C:/Users/Dell/Radix4/Radix4.runs/synth_1/mba8r4.dcp' has been generated.
INFO: [Vivado 12-24828] Executing command : report_utilization -file
mba8r4_utilization_synth.rpt -pb mba8r4_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Fri Apr 18 11:58:31 2025...
```

Report DRC

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1. REPORT SUMMARY

Netlist: netlist
Floorplan: design_1
Design limits: <entire design considered>
Ruledeck: default
Max checks: <unlimited>
Checks found: 3

Rule	Severity	Description	Checks
NSTD-1	Critical Warning	Unspecified I/O Standard	1
UCIO-1	Critical Warning	Unconstrained Logical Port	1
CFGBVS-1	Warning	Missing CFGBVS and CONFIG_VOLTAGE Design Properties	1

2. REPORT DETAILS

NSTD-1#1 Critical Warning
Unspecified I/O Standard
32 out of 32 logical ports use I/O standard (IOSTANDARD) value 'DEFAULT', instead of a user assigned specific value. This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all I/O standards. This design will fail to generate a bitstream unless all logical ports have a user specified I/O standard value defined. To allow bitstream creation with unspecified I/O standard values (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks NSTD-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports: x[7:0], y[7:0], z[15:0].
Related violations: <none>

UCIO-1#1 Critical Warning
Unconstrained Logical Port
32 out of 32 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the

components to which it is connected. To correct this violation, specify all pin locations. This design will fail to generate a bitstream unless all logical ports have a user specified site LOC constraint defined. To allow bitstream creation with unspecified pin locations (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks UCIO-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports: x[7:0], y[7:0], z[15:0].
Related violations: <none>

CFGBVS-1#1 Warning
Missing CFGBVS and CONFIG_VOLTAGE Design Properties
Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

```
set_property CFGBVS value1 [current_design]
#where value1 is either VCCO or GND

set_property CONFIG_VOLTAGE value2 [current_design]
#where value2 is the voltage provided to configuration bank 0
```

Refer to the device configuration user guide for more information.
Related violations: <none>

Power Report

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1. Summary

Total On-Chip Power (W)	0.662
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	0.592
Device Static (W)	0.070
Effective TJA (C/W)	5.0
Max Ambient (C)	81.7
Junction Temperature (C)	28.3
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

On-Chip	Power (W)	Used	Available	Utilization (%)
Slice Logic	0.194	148	---	---
LUT as Logic	0.194	86	20800	0.41
Others	0.000	4	---	---
Register	0.000	40	41600	0.10
Signals	0.334	154	---	---
I/O	0.064	32	106	30.19

| Static Power | 0.070 | | | |
| Total | 0.662 | | | |
+---------------+----------+---------+----------+----------------+

1.2 Power Supply Summary

+----------+----------+----------+----------+----------+----------+----------+----------+

Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) | Powerup (A) | Budget (A) | Margin (A) |

+----------+----------+----------+----------+----------+----------+----------+----------+

Vccint	1.000	0.603	0.592	0.011	NA	Unspecified	NA
Vccaux	1.800	0.013	0.000	0.013	NA	Unspecified	NA
Vcco33	3.300	0.000	0.000	0.000	NA	Unspecified	NA
Vcco25	2.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco18	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vcco15	1.500	0.000	0.000	0.000	NA	Unspecified	NA
Vcco135	1.350	0.000	0.000	0.000	NA	Unspecified	NA
Vcco12	1.200	0.000	0.000	0.000	NA	Unspecified	NA
Vccaux_io	1.800	0.000	0.000	0.000	NA	Unspecified	NA
Vccbram	1.000	0.000	0.000	0.000	NA	Unspecified	NA
MGTAVcc	1.000	0.000	0.000	0.000	NA	Unspecified	NA
MGTAVtt	1.200	0.000	0.000	0.000	NA	Unspecified	NA
Vccadc	1.800	0.020	0.000	0.020	NA	Unspecified	NA

+----------+----------+----------+----------+----------+----------+----------+----------+

2. Settings

2.1 Environment

+----------------------+-------------------------+
Ambient Temp (C)	25.0
ThetaJA (C/W)	5.0
Airflow (LFM)	250
Heat Sink	medium (Medium Profile)
ThetaSA (C/W)	4.6
Board Selection	medium (10"x10")
# of Board Layers	12to15 (12 to 15 Layers)
Board Temperature (C)	25.0
+----------------------+-------------------------+

2.2 Clock Constraints

+-------+--------+-----------------+
| Clock | Domain | Constraint (ns) |
+-------+--------+-----------------+
3. Detailed Reports

3.1 By Hierarchy

+--------+-----------+
| Name | Power (W) |
+--------+-----------+
mba8r4	0.592
i0	0.106
k0	0.086
kk	0.081
l0	0.108
+--------+-----------+
Design Route Status

	: # nets :
# of logical nets.....	: 193 :
# of nets not needing routing.....	: 38 :
# of internally routed nets.....	: 38 :
# of routable nets.....	: 155 :
# of fully routed nets.....	: 155 :
# of nets with routing errors.....	: 0 :

Conclusion

The implementation of Radix-4 Booth algorithm shows a significant improvement in performance over Radix-2, especially in terms of speed and resource efficiency. It proves to be a suitable candidate for modern FPGA-based arithmetic systems, enabling real-time computation in advanced digital applications.