1. (c) Number density of atoms in silicon specimen = 5 × 1028 *atom/m*3 = 5 × 1022 *atom*/*cm*3

Since one atom of indium is doped in 5 × 107 *Si* atom. So number of indium atoms doped per *cm*3 of silicon.



1. (a) The probability of electrons to be found in the conduction band of an intrinsic semiconductor

; where *k* = Boltzmann's constant

Hence, at a finite temperature, the probability decreases exponentially with increasing band gap.

1. (c) When donor impurity (+5 valence) added to a pure silicon (+4 valence), the +5 valence donor atom sits in the place of + 4 valence silicon atom. So it has a net additional + 1 electronic charge. The four valence electron form covalent bond and get fixed in the lattice. The fifth electron (with net – 1 electronic charge) can be approximated to revolve around + 1 additional charge. The situation is like the hydrogen atom for which energy is given by . For the case of hydrogen, the permittivity was taken as *ε*0. However, if the medium has a permittivity *εr*, relative to *ε*0, then 

For *Si*, *εr* = 12 and for *n* = 1, 

1. (c) The forward current 



1. (a,b,d) At 0 *K*, a semiconductor becomes a perfect insulator. Therefore at 0 *K*, if some potential difference is applied across an insulator or a semiconductor, current is zero. But a conductor will become a superconductor at 0 *K*. Therefore, current will be infinite. In reverse biasing at 300 *K* through a *P-N* junction diode, a small finite current flows due to minority charge carriers.
2. (a) Since diode in upper branch is forward biased and in lower branch is reversed biased. So current through circuit ; here = diode resistance in forward biasing = 0

⇒ .

1. (a) The voltage drop across resistance = 8 – 0.5 = 7.5 *V*

∴ Current 

1. (c) ⇒=217100Å.
2. (b) The diode in lower branch is forward biased and diode in upper branch is reverse biased

∴ .

1. (b) The current through circuit 

∴ voltage drop across resistance = 1.5 – 0.5 = 1 *V*

⇒ .

1. (d) In common emitter configuration current gain

= – 48.78.

1. (c) Voltage gain 

⇒ *Vout* = *Vin* × Voltage gain

⇒ *Vout* = *Vin* × Current gain × Resistance gain

= *Vin* × *β* × = 

1. (a) 



 so semiconductor is *N*-type

Also conductivity 

⇒

⇒ *ρ* = 0.34 Ω-*m*.

1. (b) 
2. (a) At knee point voltage across the diode is 0.7*V*.

Hence voltage across resistance *R* is 5 – 0.7 = 4.3 *V*.

⇒ using *V = iR* ⇒ 4.3 = 1 × 10–3 × *R* ⇒ *R* = 4.3 *k*Ω.

1. (d) In positive half cycle one diode is in forward biasing and other is in reverse biasing while in negative half cycle their polarity reverses, and direction of current is opposite through *R* for positive and negative half cycles so out put is not rectified.

Since *R*1 and *R*2 are different hence the peaks during positive half and negative half of the input signal will be different.

1. (b) In half wave rectifier 
2. (a) In common base mode *α* = 0.98, *R* = 5 *k*Ω, *R*in= 70Ω

∴ voltage gain 

Power gain = Current gain × Voltage gain

= 0.98 × 70 = 68.6

1. (a) = 10.6 Å.
2. (c) (i) *VA* = –10*V* and V*B* = –5*V*

Diodes *D*1 and *D*3 are reveres biased and *D*2 is forward biased.

*R*

*R*

*R*

*A*

*B*





– 10 *V*

– 5 *V*

**.**

(ii) When *VA* = – 5*V* and *VB* = – 10*V*

Diodes *D*2 is reverse biased *D*1 and *D*3 are forward biased

*R*

*R*

*R*

*A*

*B*





– 5 *V*

– 10 *V*

****=*R*.

(iii) In this case equivalent resistance between *A* and *B* is also *R*.

Hence (ii) = (iii) < (i).

1. (b) According to the given polarity, diode *D*1 is forward biased while *D*­2 is reverse biased. Hence current will pass through *D*1 only.

So current 

1. (a) Diode is in forwards biasing hence the circuit can be redrawn as follows

30*V*

10Ω

10Ω

10Ω

*VAB*

Parallel





1. (d) The diode *D* will conduct for positive half cycle of *a.c.* supply because this is forward biased. For negative half cycle of *a.c.* supply, this is reverse biased and does not conduct. So out put would be half wave rectified and for half wave rectified out put



1. (d)  



∴ 

1. (a) As we know current density *J* = *nqv*

⇒  and 

⇒  ⇒  ⇒ 

1. (b) Consider the case when *Ge* and *Si* diodes are connected as show in the given figure.

Equivalent voltage drop across the combination *Ge* and *Si* diode = 0.3 *V*

⇒ Current 

∴ Out put voltage *V*0 = *Ri*= 5 *k*Ω × 2.34 *mA* = 11.7 *V*

Now consider the case when diode connection are reversed. In this case voltage drop across the diode's combination = 0.7 *V*

⇒ Current 

∴ 

Hence charge in the value of *V*0 = 11.7 –11.3 = 0.4 *V*

1. (b) For the positive half cycle of input the resulting network is shown below

*Vi*

10 *V*

0

*T*/2

*t*

*D*1

*D*2

2*k*Ω

2*k*Ω

2*k*Ω

+

–

*V*0

+

–

⇒

2*k*Ω

+

–

2*k*Ω

2*k*Ω

⇒ (*V*0)max = 

1. (d) The equivalent circuit can be redrawn as follows

12*k*Ω

10 *V*

*i*1

14*k*Ω

2*k*Ω

*i*2

*i*

From figure it is clear that current drawn from the battery  and 

1. (c)  ⇒ 

By using 

1. (a)  

Since 2% electrons are absorbed by base, hence 98% electrons reaches the collector *i.e.* *α* = 0.98

⇒ 

Also current amplification factor

1. (b)

*A*

*B*

(*A* + *B*)

*G*1

*G*2

*G*3

*Y*



*A*

*B*



The given output equation can also be written as

 (De morgan’s theorem)



This is the expression for XOR gate.

1. (c)

*Y*

*X*



*R*



*X*

*Y*

*Q*

*P*

The truth table can be written as

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *X* | *Y* |  |  |  |  |  |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 |

Hence *X* = 1, *Y* = 0 gives output *R* =1

1. (d)

*A*

*B*



NOR







= *AB*

NOT

NOT

NOT

Hence option (d) is correct.

1. (b) The truth table of the circuit is given

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | *C* |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |

Output *Z* of single three input gate is that of AND gate.

1. (c) Output of upper OR gate = *W* + *X*

Output of lower OR gate = *W* + *Y*

Net output *F* = (*W + X*) (*W + Y*)

= *WW* + *WY* + *XW* + *XY* (Since *WW* = *W*)

= *W*(1 *+ Y*) + *XW* + *XY* (Since 1 + *Y*= 1)

= *W* + *XW* + *XY* = *W* (1 + *X*) + *XY* = *W* + *XY*

1. (b) 

From  ⇒ 

⇒ 

= 75 *K* (*ip*/*K*)1/3

Because *ip* was in *mA*, *gm* is substituted as 5 *m*℧

⇒ ⇒ 

Cut off grid voltage 

1. (d) 



∴ *ohms*

1. (d) The dynamic plate resistance is 

Now for a vacuum diode 

⇒ 

⇒  ⇒ 

1. (d) 

Differentiating this equation *w.r.t.* *V­p*

 or ⇒ 

1. (b) 
2. (c) The emission current 

For the two surfaces *A*1 = *A*2, *S*1 = *S*2, *T*1 = 800 *K*, 

Therefore, = (2)2 = 4 ⇒ 

1. (a) The first data gives value of plate resistance 

Also  and 

⇒ 

1. (a) 

⇒ 

⇒ 

⇒ 

Comparing the given equation of *Ip* with standard equation  we get *μ* = 10

Also from *μ* = *rp* × *gm* ⇒ 

⇒ 

1. (b) 

From ⇒ 

⇒ 

1. (a) . Peak value of output signal  ⇒ 

⇒ *r.m.s.* value of current through the load



1. (c) 

Voltage gain 

∴ Output signal voltage



Signal power in load 

1. (a) 

⇒ 4 = *k*(200 – 10 × 4)3/2 = *k* × (160)3/2 ….(i)

and  ….(ii)

From equation (i) and (ii) we get



1. (a) At  and 

At  for constant plate current *i.e.* 

From 

⇒  ⇒ 

∴ change in plate voltage 

Change in grid voltage 

So, 

1. (b) The slope of anode characteristic curve 



The slope of mutual characteristic curve = *gm*

= 1 × 10–3 *A/V*.

.

1. (b) Voltage gain .

–

+

*Rf*

*Vi*

*V*o

*Ri*