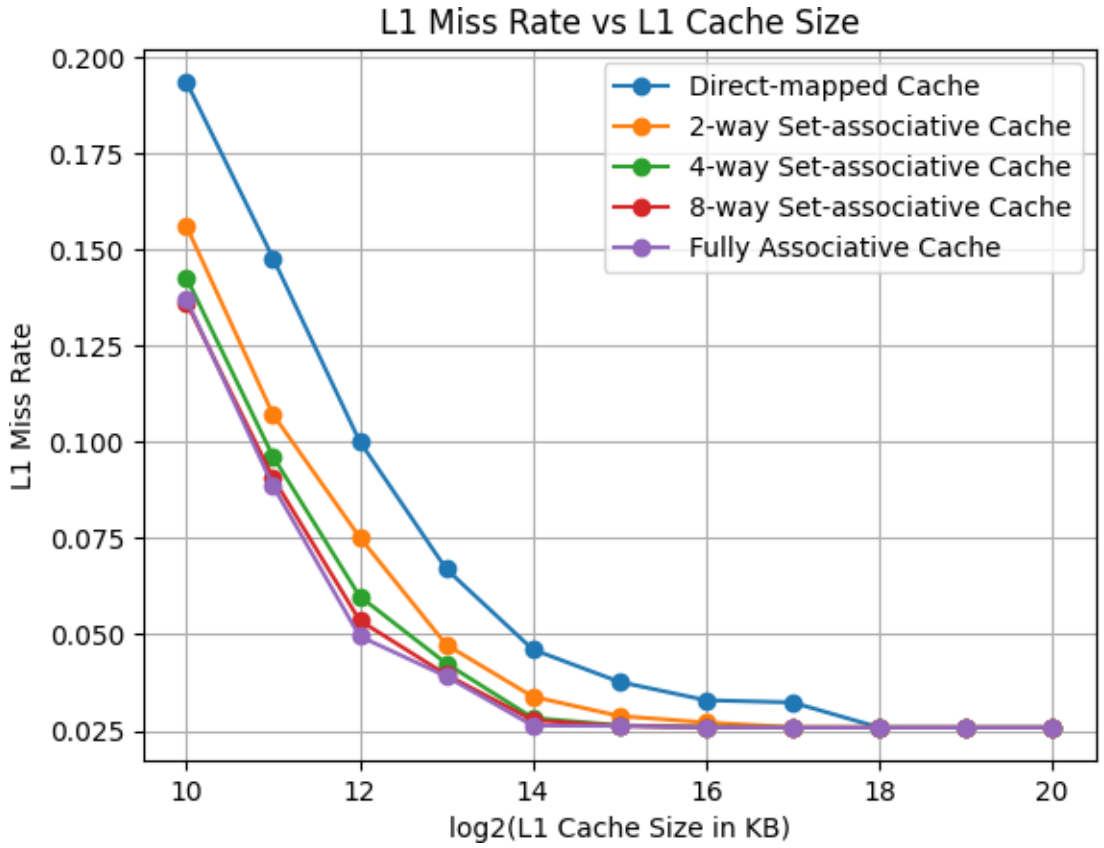
Results:

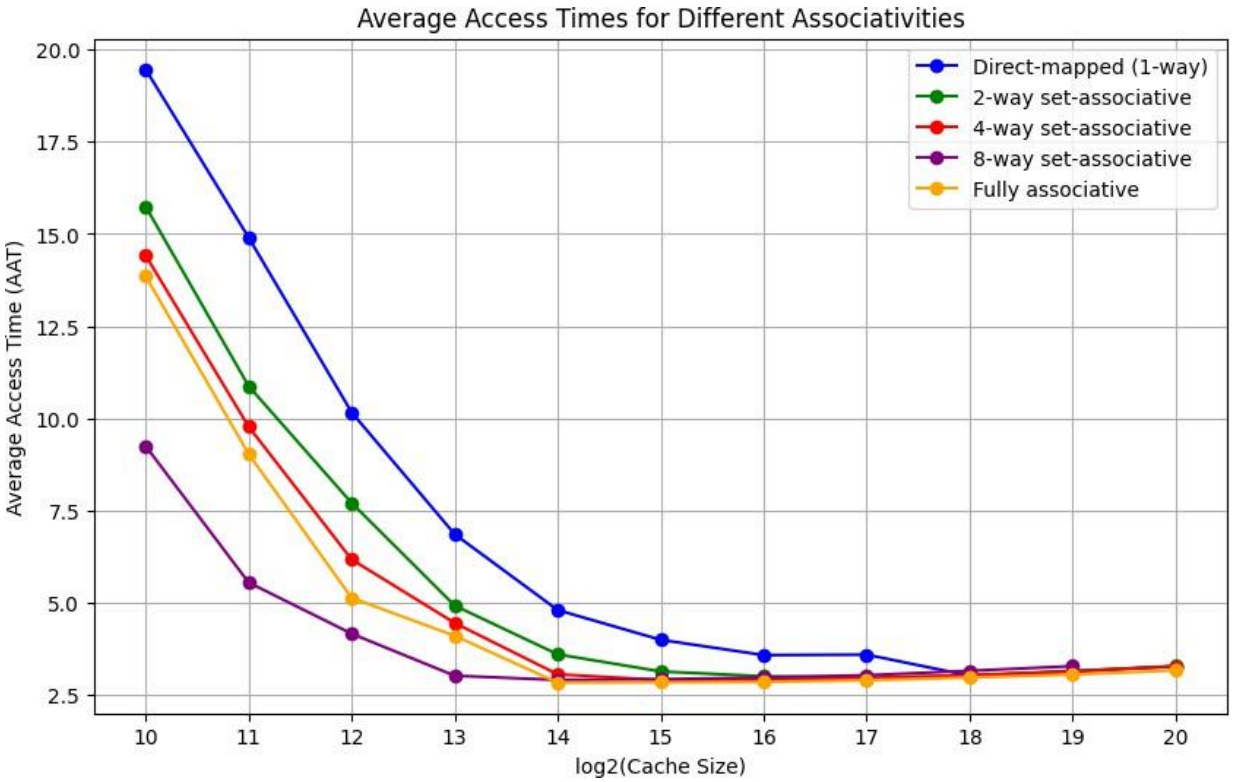
GRAPH 1:

The Total number of simulations is 55



- The graph shows a clear pattern: miss rates go down as cache size goes up, emphasizing how important enough cache capacity is to reduce data retrieval delays.
- To determine the compulsory miss rate, analyze the miss rate at the smallest cache size (1KB) and log2(Cache Size) = 10 to gain insight into how the cache's initial size affects necessary data requests.
- By carefully examining the graph, it is possible to estimate the mandatory miss rate, which provides important information for optimizing cache configurations by balancing associativity and size. The conflict miss rate for 1-way is 0.16755; The conflict miss rate for 2-way is 0.13031; The conflict miss rate for 4-way is 0.11679; The conflict miss rate for 8-way is 0.11037; The conflict miss rate for Fully associative is 0.11114

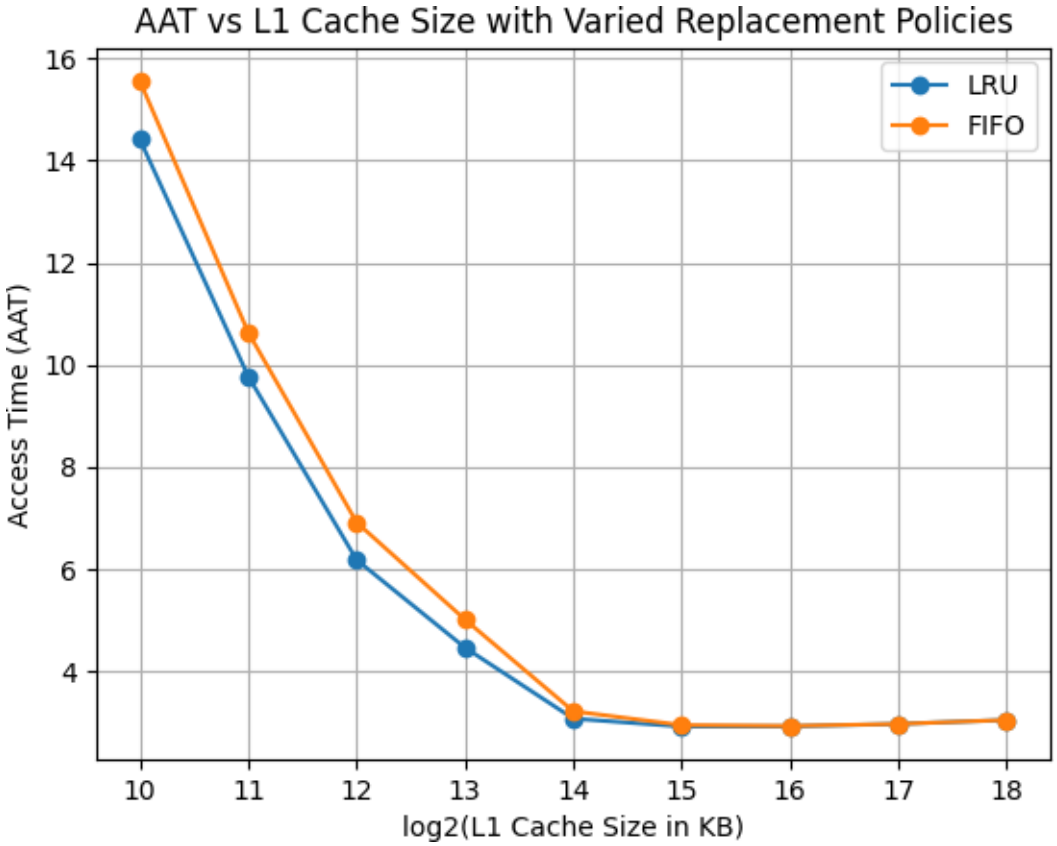
GRAPH 2:



- The best configuration for the lowest AAT is: Associativity: Fully Cache Size: 16384 KB Minimum AAT Value: 2.839608
- The fully associative cache is the recommended option for a memory hierarchy with only an L1 cache and BLOCKSIZE of 32 since it consistently yields optimal AAT.

Graph 3:

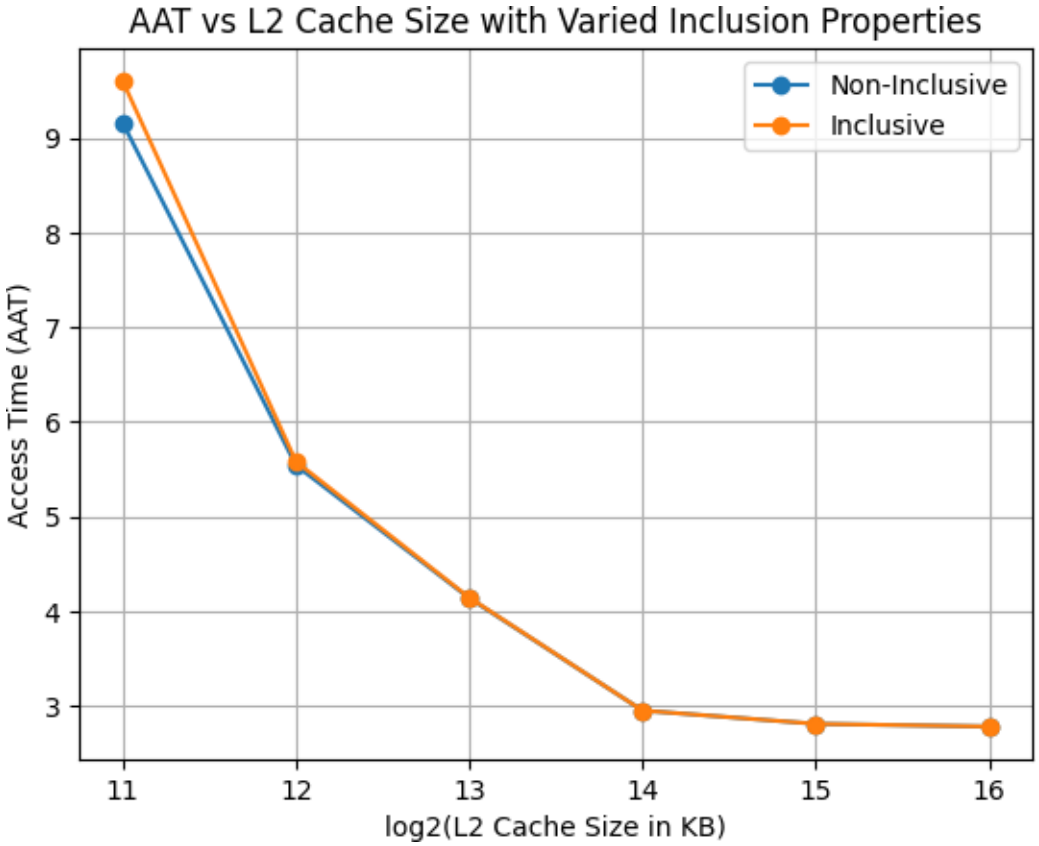
The Total number of simulations is 18



- Across a range of L1 cache sizes, the graph consistently shows that the Least Recently Used (LRU) replacement policy achieves lower Access Time (AAT) in comparison to the First-In-First-Out (FIFO) policy. This demonstrates how well LRU performs within the constraints of the experiment.
- For both replacement policies, there is a discernible and consistent decrease in AAT as the L1 cache size grows. But the LRU policy always performs better than FIFO, highlighting how well it reduces access time and indicating that it is best suited for this memory hierarchy arrangement.
- The best AAT for LRU: 2.91125 at log2(Cache Size) = 15
  The best AAT for FIFO: 2.922481 at log2(Cache Size) = 16
  LRU replacement policy yields the best (lowest) AAT overall.

Graph 4:

The Total number of simulations is 18



- When the cache size increases, the inclusive L2 cache design consistently outperforms the non-inclusive one in terms of Average Access Time (AAT) decline.
- The continuous downward trend in the AAT difference between inclusive and non-inclusive designs implies that the inclusive attribute always guarantees better performance, which results in lower AAT as the L2 cache size grows.