FPGASID Register Description

Version 20190727

Index

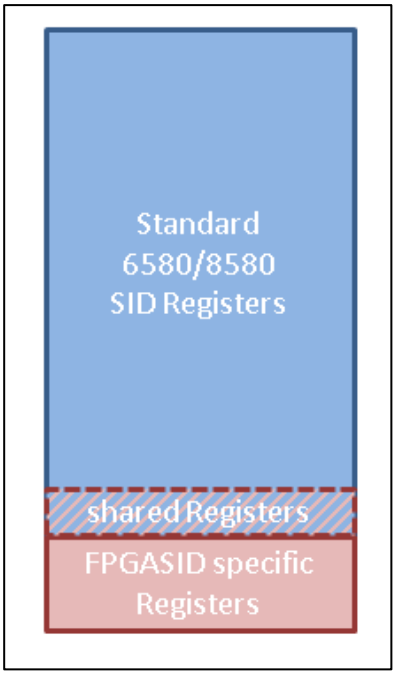
FPGASID Register Description

Extended Register Set

To achieve the utmost compatibility, the FPGASID registers are mapped to the same address-offset locations as the standard MOS6581 or MOS8580 registers. However some extensions are made to the register set to support extra features of FPGASID. These extensions are located in an unused space of the register set in order to keep compatibility with existing software.

Registers with offset addresses $00 to $18 are organized exactly in the same way as standard SID registers. Registers $19 to $1F are used for FPGASID configuration. Please note that this includes also registers $19 to $1C, that are also part of the standard SID register set and that are shared with the FPGASID register set.

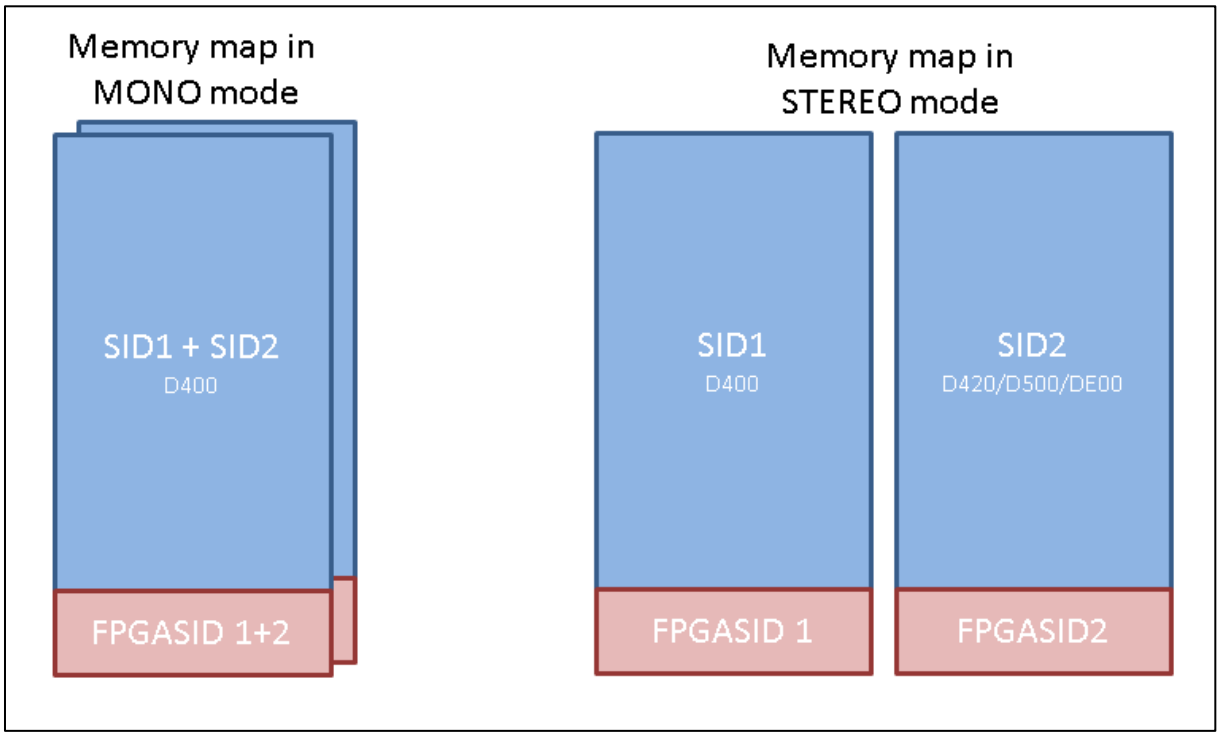
FPGASID has a mechanism to switch the FPGASID specific registers into a special mode that allows FPGASID control. In normal operation mode all FPGASID specific registers are write-protected making it impossible to accidentally overwrite the FPGASID configuration by existing software.



Extended Register Set

Memory Map Modes

To allow stereo operation, FPGASID incorporates two full register sets controlling two independent SID instances. These two SID instances can be mapped into memory in two fundamental modes: MONO mode and STEREO mode.



Memory map configuration modes

Mono Mode

When FPGASID is configured in MONO mode, both register sets are mapped to the same memory location $D400. Writing to a register in the range of $D400 and $D41F will write the value into both register sets at the same time. Reading from the memory location from $D400 to $D41F will return the value read out from the SID 1 register set. In this configuration the SID 2 register set cannot be read. This is the default configuration.

Stereo Mode

When FPGASID is configured in STEREO mode, the register sets of SID1 and SID2 are mapped to different memory locations. SID 1 will always be mapped to $D400. SID 2 can be mapped to any of the following locations: $D420, $D500 or $DE00. In this configuration both SID instances are completely independent and can be written with different values. SID 2 can be read out by reading the memory locations $D420 to $D43F and $D500 to $D51F. Reading from $DE00 to $DE1F is not possible due to potential address collisions with modules connected to the expansion port.
This is the most flexible configuration mode but it also has the downside that it is hard to keep track of which registers get written especially when the mode is changed between MONO and STEREO back and forth.

Operation modes

FPGASID can operate in three basic operation modes: Normal mode, configuration mode and diagnostics mode.

Normal mode

In **normal mode** FPGASID behaves like a standard SID chip or a set of two SID chips when the configuration is in STEREO mode. In this mode the configuration of FPGASI cannot be changed.

Configuration mode

In **configuration** mode FPGASID opens all configuration registers for write access. The configuration can be changed. It still operates mostly like one or two standard SIDs. Only the SID's read registers are no longer available.
The Configuration mode comes in three flavors:

1. The 'normal' configuration mode allows writing the configuration of both SID instances. When the FPGASID is configured to mono mode, both SID instances will be mapped to the $D400 address space. This will make it impossible to write the configuration registers of both SID instances independently.
2. The 'SID1 mode' allows writing of the first SID's configuration but write protects the second SID's registers.
3. In 'SID2 mode' the configuration registers of the second SID instance are mapped to the address space $D428…$D42F and the registers of the first SID instance are write protected. This allows accessing the SID2 registers even in mono mode where both SIDs are mapped to the $D400 address space.

Diagnostics mode

In **diagnostics mode** FPGASID is still a fully operational SID or a pair of SIDs. But read access to the SIDs registers returns some diagnostic information.

Flash mode

In **flash mode** FPGASID does no longer operate as a SID. The registers are remapped to registers used to access the internal flash memory of the FPGASID. In this mode the firmware of the FPGA can be updated and the flashed configuration can be altered.

Changing the operation mode

The basic FPGASID operation mode is changed by writing a special magic cookie value into the POTX/POTY registers of the first SID instance at address $D419 and $D41A. Writing the POTX/Y registers of the second SID instance does not have any effect.
In standard SIDs these registers are read-only registers. Writing to them does not have any effect. So it is unlikely that any existing software is writing the cookie value into these registers.

To activate the various operation modes the following magic cookie values have to be used:

Mode	Magic Cookie value	Low Byte	High Byte
Configuration normal	$6581	$81 / 129	$65 / 101
Configuration SID1	$6580	$80 / 128	$65 / 101
Configuration SID2	$6582	$82 / 130	$65 / 101
Diagnostics	$ABEE	$EE / 238	$AB / 171
Flash	$F7A5	$A5 / 165	$F7 / 247
Normal	anything else	anything else	anything else

Register Map Overview

FPGASID Register map

Offset #	$	D400	D420	D500	DE00	normal operation / config mode bit7 128	bit6 64	bit5 32	bit4 16	bit3 8	bit2 4	bit1 2	bit0 1	diag mode	flash mode[6] bit7 128	bit6 64	bit5 32	bit4 16	bit3 8	bit2 4	bit1 2	bit0 1
0	0	54272	54304	54528	56832	frequency voice 1 low								$1D	wait	x	x	erase ok	write ok	read ok	00: idle, 01: busy erase 10: busy write, 11: busy read	
1	1	54273	54305	54529	56833	frequency voice 1 high								$F5	erase page number							
2	2	54274	54306	54530	56834	pulse width voice 1 low								CPLD revision	write protect bits: 11111 = protect, 00000 = write					sector erase number		
3	3	54275	54307	54531	56835	x	x	x	x	pulse width voice 1 high				FPGA revision	address bits 7...0					set to $1D to set write mode		
4	4	54276	54308	54532	56836	v1 noise	v1 pulse	v1 saw	v1 triangle	v1 test	v1 ring	v1 sync	v1 gate	UNIQUEID0	address bits 15...8					set to $F5 to set write mode		
5	5	54277	54309	54533	56837	attack voice 1				decay voice 1				UNIQUEID1	0: read 1: write	1: addr auto increment	set register to $AB to set write mode in bit 7				address bit 16	
6	6	54278	54310	54534	56838	sustain voice 1				release voice 1				UNIQUEID2	data low							
7	7	54279	54311	54535	56839	frequency voice 2 low								UNIQUEID3	data mid low							
8	8	54280	54312	54536	56840	frequency voice 2 high								UNIQUEID4	data mid hi							
9	9	54281	54313	54537	56841	pulse width voice 2 low								UNIQUEID5	data high							
10	A	54282	54314	54538	56842	x	x	x	x	pulse width voice 2 high				UNIQUEID6								
11	B	54283	54315	54539	56843	v2 noise	v2 pulse	v2 saw	v2 triangle	v2 test	v2 ring	v2 sync	v2 gate	UNIQUEID7								
12	C	54284	54316	54540	56844	attack voice 2				decay voice 2				Φ2 frequency								
13	D	54285	54317	54541	56845	sustain voice 2				release voice 2				PCA revision[6]								reconfigure
14	E	54286	54318	54542	56846	frequency voice 3 low								select_pins	JTAG Pin 7	JTAG Pin 6	select_pins readout					C128 detect
15	F	54287	54319	54543	56847	frequency voice 3 high								readout config A SID1 digifix	readout config A SID1 digifix							
16	10	54288	54320	54544	56848	pulse width voice 3 low								readout config A SID1 stereo	readout config A SID1 stereo							
17	11	54289	54321	54545	56849	x	x	x	x	pulse width voice 3 high				readout config A SID1 mode	readout config A SID1 mode							
18	12	54290	54322	54546	56850	v3 noise	v3 pulse	v3 saw	v3 triangle	v3 test	v3 ring	v3 sync	v3 gate	readout config A SID2 digifix	readout config A SID2 digifix							
19	13	54291	54323	54547	56851	attack voice 3				decay voice 3				readout config A SID2 stereo	readout config A SID2 stereo							
20	14	54292	54324	54548	56852	sustain voice 3				release voice 3				readout config A SID2 mode	readout config A SID2 mode							
21	15	54293	54325	54549	56853	x	x	x	x	x	filter low			readout config B SID1 digifix	readout config B SID1 digifix							
22	16	54294	54326	54550	56854	filter high								readout config B SID1 stereo	readout config B SID1 stereo							
23	17	54295	54327	54551	56855	resonance				ext	voice3	voice2	voice1	readout config B SID1 mode	readout config B SID1 mode							
24	18	54296	54328	54552	56856	voice3 off	hp	bp	lp	volume				readout config B SID2 digifix	readout config B SID2 digifix							
25	19	54297	54329	54553	56857	read: paddle x / identify ? $1D : CPLD revision[3] write: magic low, $80 = config SID1 mode, $81 = config mode, $82 = config_swap_mode, $EE = diag mode, $A5 = flash mode, else disable								readout config B SID2 stereo write: $EE = diag mode	set to $A5 to enable flashing mode			readout config B SID2 stereo				
26	1A	54298	54330	54554	56858	read: paddle y / identify ? $F5 : FPGA revision write: magic high, $65 = config mode, $AB = diag mode, $F7 = flash mode, else disable								readout config B SID2 mode write: $AB = diag mode	set to $F7 to enable flashing mode			readout config B SID2 mode				
27	1B	54299	54331	54555	56859	oscillator 3 / reserved for future use								config index A	config index A							
28	1C	54300	54332	54556	56860	envelope 3 / 6581 filter bias[9]								config index B	config index B							
29	1D	54301	54333	54557	56861	write: digifix value (can be used for sample playback) read: identify ? digifix value : current sample value of EXTIN input values are signed: -128=$FF, -1=$80, 0=$00, +1=$01, +127=$7F								config filter bias A SID1 / SID 2[9]	readout config A SID1 filter bias[9]					readout config A SID2 filter bias[9]		
30	1E	54302	54334	54558	56862	identify[10] 0: rev+digi 1: F51D	disable v3	disable v2	disable v1	output mode[11] 0: two signals 1: one signal	addr 2nd SID[2]: 1 = DE00	000 = D400 1 = D500	1 = D420	config filter bias B SID1 / SID 2[9]	readout config B SID1 filter bias[9]					readout config B SID2 filter bias[9]		
31	1F	54303	54335	54559	56863	Source EXTIN: 00: analog input 01: disabled 10: other SID 11: digifix (8580)	writeregs readback: 00: bitrot 6581 01: always read value 10: always read $00 11: bitrot 8580			reg delay[4]: 0: 6581 1: 8580	mixed wave: 0: 6581 1: 8580	crunchy DAC: 0: on (6581) 1: off (8580)	Filter Mode: 0: 6581 1: 8580									

Footnotes:

Reset value is $00 for all registers!

[2]: register exists only in first SID. Second SID function reserved

[3]: available since CPLD-revision >= 3, FPGA-revision >=3

[4]: available from FPGA-revision 4 onwards

[5]: available from FPGA-revision 5 onwards

[6]: available from FPGA-revision 6 onwards

[9]: available from FPGA-revision 9 onwards

[10]: SID1 identify=1:disable LEDs for heartbeat; SID2 identify=1:disable LEDs for voices;

[11]: from FW revision 0A onwards

Register $00/0 – Frequency Voice 1 low

Normal mode
Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 1 frequency.

Configuration mode
Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 1 frequency.

Diagnostics mode
Reading this register returns the low-byte $1D of the identifier $F51D.
Writing this register sets the low-byte of the voice 1 frequency.

Flash mode
Reading this register returns the Status information of the flash memory
Writing this register does not have an effect.

Register $01/1 – Frequency Voice 1 high

Normal mode
Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 1 frequency.

Configuration mode
Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 1 frequency.

Diagnostics mode
Reading this register returns the high-byte $F5 of the identifier $F51D.
Writing this register sets the high-byte of the voice 1 frequency.

Flash mode
Reading returns the value that has been written previously.
Writing this register sets the page number for page erase operation

Register $02/2 – Pulse Width Voice 1 low

Normal mode
Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 1 pulse width.

Configuration mode
Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 1 pulse width.

Diagnostics mode
Reading this register returns the CPLD revision.
Writing this register sets the low-byte of the voice 1 pulse width.

Flash mode

Reading returns the value that has been written previously.
Writing this register sets the sector number for sector erase operation and the sector protect bits.

Register $03/3 – Pulse Width Voice 1 high

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 1 pulse-width.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 1 pulse-width.

Diagnostics mode

Reading this register returns the FPGA revision.
Writing this register sets the high-byte of the voice 1 pulse-width.

Flash mode

Reading returns the value that has been written previously.
Writing this register sets the 8 lowest word address bits for read or write

Register $04/4 – Voice 1 Control

Normal mode

Reading returns the value that has been written previously.
Writing this register sets control bits of voice 1:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
noise	pulse	saw	triangle	test	ring	sync	gate

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets control bits of voice 1 (see above).

Diagnostics mode

Reading this register returns the bits 0 to 7 of the FPGASID unique ID.
Writing this register sets the high-byte of the voice 1 pulse-width.

Flash mode

Reading returns the value that has been written previously.
Writing this register sets the 8 middle word address bits for read or write

Register $05/5 – Attack Decay Voice 1

Normal mode

Reading returns the value that has been written previously.
Writing this register sets voice 1's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Configuration mode

Reading returns the value that has been written previously.

Writing this register sets voice 1's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Diagnostics mode

Reading this register returns the bits 8 to 15 of the FPGASID unique ID.
Writing this register sets voice 1's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Flash mode

Reading returns the value that has been written previously.
Writing this register sets the highest word address bit for read or write, enables auto addres increment mode and selects between read and write mode.

Register $06/6 – Sustain Release Voice 1

Normal mode

Reading returns the value that has been written previously.
Writing this register sets voice 1's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets voice 1's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Diagnostics mode

Reading this register returns the bits 16 to 23 of the FPGASID unique ID.
Writing this register sets voice 1's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Flash mode

Reading returns bits 0…7 of the flash memory word addressed with the read/write address registers.
Writing this register sets bits 0…7 of the flash memory word to be written.

Register $07/7 – Frequency Voice 2 low

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 2 frequency.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 2 frequency.

Diagnostics mode

Reading this register returns the bits 24 to 31 of the FPGASID unique ID.
Writing this register sets the low-byte of the voice 2 frequency.

Flash mode

Reading returns bits 8…15 of the flash memory word addressed with the read/write address registers.
Writing this register sets bits 8…15 of the flash memory word to be written.

Register $08/8 – Frequency Voice 2 high

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 2 frequency.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 2 frequency.

Diagnostics mode

Reading this register returns the bits 32 to 39 of the FPGASID unique ID.
Writing this register sets the high-byte of the voice 2 frequency.

Flash mode

Reading returns bits 16…23 of the flash memory word addressed with the read/write address registers.
Writing this register sets bits 16…23 of the flash memory word to be written.

Register $09/9 – Pulse Width Voice 2 low

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 2 pulse width.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 2 pulse width.

Diagnostics mode

Reading this register returns the bits 40 to 47 of the FPGASID unique ID.
Writing this register sets the low-byte of the voice 2 pulse width.

Flash mode

Reading returns bits 24…31 of the flash memory word addressed with the read/write address registers.
Writing this register sets bits 24…31 of the flash memory word to be written.

Register $0A/10 – Pulse Width Voice 2 high

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 2 pulse-width.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 2 pulse-width.

Diagnostics mode

Reading this register returns the bits 48 to 55 of the FPGASID unique ID.
Writing this register sets the high-byte of the voice 2 pulse-width.

Flash mode
Reading or writing this register does not have any effect

Register $0B/11 – Voice 2 Control

Normal mode
Reading returns the value that has been written previously.
Writing this register sets control bits of voice 2:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
noise	Pulse	saw	Triangle	test	ring	sync	gate

Configuration mode
Reading returns the value that has been written previously.
Writing this register sets control bits of voice 2 (see above).

Diagnostics mode
Reading this register returns the bits 56 to 63 of the FPGASID unique ID.
Writing this register sets the high-byte of the voice 2 pulse-width.

Flash mode
Reading or writing this register does not have any effect

Register $0C/12 – Attack Decay Voice 2

Normal mode
Reading returns the value that has been written previously.
Writing this register sets voice 2's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Configuration mode
Reading returns the value that has been written previously.
Writing this register sets voice 2's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Diagnostics mode
Reading this register returns 6502 bus clock (Φ2) frequency in units of 12.5 kHz. Since the frequency resolution is very coarse, it is recommended to read this register multiple times. Then use an average of all values read, to obtain a more accurate value.
Writing this register sets voice 2's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Flash mode
Reading or writing this register does not have any effect

Register $0D/13 – Sustain Release Voice 2

Normal mode
Reading returns the value that has been written previously.
Writing this register sets voice 2's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Configuration mode
Reading returns the value that has been written previously.

Writing this register sets voice 2's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Diagnostics mode

Reading this register is reserved for future use.
Writing this register sets voice 2's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Flash mode

Reading this register returns 0.
Writing bit 0 of this register with 1 triggers the reconfiguration of the FPGA.

Register $0E/14 - Frequency Voice 3 low

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 3 frequency.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 3 frequency.

Diagnostics mode

Reading this register returns information about the C128-signal, the configuration mode switch position and the result of the C128 auto detection.
Writing this register sets the low-byte of the voice 3 frequency.

Flash mode

Reading this register returns information about the C128-signal, the configuration mode switch position and the result of the C128 auto detection.
Writing this register does not have any effect.

Register $0F/15 – Frequency Voice 3 high

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 3 frequency.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 3 frequency.

Diagnostics mode

Reading this register returns the stored digifix register value for SID1, configuration A.
Writing this register sets the high-byte of the voice 3 frequency.

Flash mode

Reading this register returns the stored digifix register value for SID1, configuration A.
Writing this register does not have any effect.

Register $10/16 – Pulse Width Voice 3 low

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 3 pulse width.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the low-byte of the voice 3 pulse width.

Diagnostics mode

Reading this register returns the stored stereo register value for SID1, configuration A.
Writing this register sets the low-byte of the voice 3 pulse width.

Flash mode

Reading this register returns the stored stereo register value for SID1, configuration A.
Writing this register does not have any effect.

Register $11/17 – Pulse Width Voice 3 high

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 3 pulse-width.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the high-byte of the voice 3 pulse-width.

Diagnostics mode

Reading this register returns the stored mode register value for SID1, configuration A.
Writing this register sets the high-byte of the voice 3 pulse-width.

Flash mode

Reading this register returns the stored mode register value for SID1, configuration A.
Writing this register does not have any effect.

Register $12/18 – Voice 3 Control

Normal mode

Reading returns the value that has been written previously.
Writing this register sets control bits of voice 3:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
noise	pulse	saw	Triangle	test	ring	sync	gate

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets control bits of voice 3 (see above).

Diagnostics mode

Reading this register returns the stored digifix register value for SID2, configuration A.
Writing this register sets the high-byte of the voice 3 pulse-width.

Flash mode

Reading this register returns the stored digifix register value for SID2, configuration A.
Writing this register does not have any effect.

Register $13/19 – Attack Decay Voice 3

Normal mode

Reading returns the value that has been written previously.
Writing this register sets voice 3's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets voice 3's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Diagnostics mode

Reading this register returns the stored stereo register value for SID2, configuration A.
Writing this register sets voice 3's attack value in register bits 4 to 7 and decay setting in bits 0 to 3.

Flash mode

Reading this register returns the stored stereo register value for SID2, configuration A.
Writing this register does not have any effect.

Register $14/20 – Sustain Release Voice 3

Normal mode

Reading returns the value that has been written previously.
Writing this register sets voice 3's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets voice 3's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Diagnostics mode

Reading this register returns the stored mode register value for SID2, configuration A.
Writing this register sets voice 3's sustain value in register bits 4 to 7 and release setting in bits 0 to 3.

Flash mode

Reading this register returns the stored mode register value for SID2, configuration A.
Writing this register does not have any effect.

Register $15/21 – Filter Frequency low

Normal mode

Reading returns the value that has been written previously.
Writing this register to bits 0 to 2 sets the 3 least significant bits of the filter cutoff frequency value.

Configuration mode

Reading returns the value that has been written previously.
Writing this register to bits 0 to 2 sets the 3 least significant bits of the filter cutoff frequency value.

Diagnostics mode

Reading this register returns the stored digifix register value for SID1, configuration B.
Writing this register to bits 0 to 2 sets the 3 least significant bits of the filter cutoff frequency value.

Flash mode

Reading this register returns the stored digifix register value for SID1, configuration B.
Writing this register does not have any effect.

Register $16/22 – Filter Frequency high

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the 8 most significant bits of the filter cutoff frequency value.

Configuration mode

Reading returns the value that has been written previously.
Writing sets the filter resonance in bits 4 to 7 and the 8 most significant bits of the filter cutoff frequency value.

Diagnostics mode

Reading this register returns the stored stereo register value for SID1, configuration B.
Writing this register sets the 8 most significant bits of the filter cutoff frequency value.

Flash mode

Reading this register returns the stored stereo register value for SID1, configuration B.
Writing this register does not have any effect.

Register $17/23 – Filter Resonance / Select

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the Filter resonance and the filter channel selection:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Filter Resonance				EXTIN	VOICE 3	VOICE 2	VOICE 1

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the Filter resonance and the filter channel selection (see above).

Diagnostics mode

Reading this register returns the stored mode register value for SID1, configuration B.
Writing this register sets the Filter resonance and the filter channel selection (see above).

Flash mode

Reading this register returns the stored mode register value for SID1, configuration B.

Writing this register does not have any effect.

Register $18/24 – Filter Mode / Volume

Normal mode

Reading returns the value that has been written previously.
Writing this register sets the filter mode and the volume:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VOICE3 off	**highpass**	**bandpass**	lowpass			Volume	

Configuration mode

Reading returns the value that has been written previously.
Writing this register sets the filter mode and the volume (see above).

Diagnostics mode

Reading this register returns the stored digifix register value for SID2, configuration B.
Writing this register sets the filter mode and the volume (see above).

Flash mode

Reading this register returns the stored digifix register value for SID2, configuration B.
Writing this register does not have any effect.

Register $19/25 – POTX and Magic

Normal mode

Reading this register returns the current position of the POTX paddle.
Writing this register sets the low-byte of the magic cookie.

Configuration mode

Reading this register depends on the identify bit (Bit 7 in register $1F/31):
When identify == 0: reading returns the CPLD revision
When identify == 1: reading returns $1D/29
Writing this register sets the low-byte of the magic cookie.

Diagnostics mode

Reading this register returns the stored stereo register value for SID2, configuration B.
Writing this register sets the low-byte of the magic cookie.

Flash mode

Reading this register returns the stored stereo register value for SID2, configuration B.
Writing this register sets the low-byte of the magic cookie.

Register $1A/26 – POTY and Magic

Normal mode

Reading this register returns the current position of the POTY paddle.
Writing this register sets the high-byte of the magic cookie.

Configuration mode

Reading this register depends on the identify bit (Bit 7 in register $1F/31):

When identify == 0: reading returns the FPGA revision
When identify == 1: reading returns $F5/253
Writing this register sets the high-byte of the magic cookie.

Diagnostics mode

Reading this register returns the stored mode register value for SID2, configuration B.
Writing this register sets the high-byte of the magic cookie.

Flash mode

Reading this register returns the stored mode register value for SID2, configuration B.
Writing this register sets the high-byte of the magic cookie.

Register $1B/27 - Reserved

Normal mode

Reading this register returns the current waveform value of voice 3
Writing this register is reserved for future use.

Configuration mode

Reading this register is reserved for future use.
Writing this register is reserved for future use.

Diagnostics mode

Reading this register returns the configuration list index for configuration A.
Writing this register is reserved for future use.

Flash mode

Reading this register returns the configuration list index for configuration A.
Writing this register is reserved for future use.

Register $1C/28 – Filter Bias

Normal mode

Reading this register returns the current envelope value of voice 3
Writing this register is reserved for future use.

Configuration mode

Reading this register returns the 6581 filter bias.
Writing this register sets the 6581 filter bias:
Bits 0…3 are treated as a signed value and can be used to set the filter bias in a range of -8 to +7. The neutral setting is 0. Negative values lead to lower filter cutoff frequencies whilst positive values increase the filter cutoff frequencies.
Note: *There is a big audible difference between filter bias settings in firmware revision 09 against firmware revision 0A. Older revisions do not support this feature.*

Diagnostics mode

Reading this register returns the configuration list index for configuration B.
Writing this register is reserved for future use.

Flash mode

Reading this register returns the configuration list index for configuration B.
Writing this register is reserved for future use.

Register $1D/29 – Digifix and Sampling

Normal mode

Reading this register is reserved for future use.
Writing this register is reserved for future use.

Configuration mode

Reading this register returns the current sample value at the EXTIN input. This register can be used to sample analog audio signals from the EXTIN input of FPGASID. The values are updated at a rate of 1MHz. The sample values are in signed twos-complement format and range from -128 to +127. An internal anti-aliasing filter limits the audio bandwidth to about 32 kHz.

Note: E*xternal low pass filter is required for sampling*

Since the sampling auf audio on a C64 will most likely run on a sample rate less than 32 kHz, it is strongly recommended to use an external low pass filtering with a cutoff frequency of about half of the sample rate. This will eliminate the aliasing artefacts caused by the sampling process.

Note: *Take care of the limited signal dynamic range*

The sampling is done with 8 bits only which limits the signal dynamic range to 48dB. Most nowadays audio sources have a higher dynamic range. To achieve good results it is recommended to apply audio compression to the signal to reduce the dynamic range and set the input signal level carefully to use the full range of the FPGASID AD-Converter (+/- 1.5V = 3Vss) without clipping.

Writing this register sets the digifix value that will be used when digifix-mode is enabled by bits 6/7 of Register $1F/31. The digifix value is configured in twos-complement format ranging from -128 to +127. This register can also be used for sample playback when digifix mode is enabled.

Note: L*ow pass filter is required for sample playback*

Sample playback on a C64 will most likely run on a rather low sample rate less than 32 kHz. It is strongly recommended to apply low pass filtering with a cutoff frequency of about half of the sample rate to eliminate aliasing artefacts caused by the sampling process. This filtering can be done by the internal SID filter. However better results can be achieved by external filtering with a steep filter response.

Diagnostics mode

Reading this register returns the 6581 filter bias of SID1 and SID2 for configuration A.
Writing this register is reserved for future use.

Flash mode

Reading this register returns the 6581 filter bias of SID1 and SID2 for configuration A.
Writing this register is reserved for future use.

Register $1E/30 – Stereo Configuration

Normal mode

Reading this register is reserved for future use.
Writing this register is reserved for future use.

Configuration mode

Reading returns the value that has been written previously

Writing this register controls these configuration bits:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3		Bits 2 to 0	
identify 0: revisions 1: F51D	disable voice 3	disable voice 2	disable voice 1	output mode	addr 2nd SID: 1 = DE00	000 = D400 1 = D500	1 = D420

Bits 0 to 2 are only available in SID1. Writing them in SID2 does not have any effect.

Bit 7 - Identify:

Set the read behavior of register $19/25 and $1A/26. This bit allows software identification of a FPGASID device in a defined and reliable way.
To do this enable configuration mode by writing the magic cookie, then set the identify bit. Finally read out registers $19/25 and $1A/26 and check the result for the value $F51D. When the value matches, FPGASID is identified.

In Firmware revisions >= 0A the identify bit has a second function: It will control the debug LEDs of the FPGASID and allows disabling the heartbeat or voice gate visualization.
SID1 identify == 1 will turn off idle blinking of LEDs (heartbeat),
SID2 identify == 1 will turn off voice gate visualization of LEDs
In order to set both bits individually, a STEREO mode has to be (temporarily) selected to make the identify bits accessible without modifying the corresponding bit of the other SID.

Bits 6, 5 and 4 - Pseudo stereo configuration:

Setting a bit disables (mutes) a single voice.
Pseudo Stereo is configured by muting different voices in SID 1 and SID 2. To achieve this FPGASID has to be temporarily switched to STEREO mode to allow independent configuration of SID 1 and SID 2. Then set a single bit so mute one voice in SID 1 and another bit to mute another voice in SID 2. The third voice will be available on both SIDs. Then switch back to MONO mode. The unmuted voice will be audible on both SIDs and appear in the middle while the other two voices are muted on either of the two SIDs and will appear left and right. The result is a stereo playback of a tune that has been made for only one single SID.

Bit 3 – Output mode

Note: *This bit is only available for SID 1. The function of this bit in SID 2 is reserved.*
The output mode bit can be used to mix the output signals of both SIDs into one single mono signal even when the configuration is set to STEREO mode. This can be useful in an environment where only one audio channel is used:
output mode == 0: SID1 audio output and SID2 audio output are separated.
output mode == 1: SID1 audio output and SID2 audio output are mixed together to a mono signal.

Bits 2, 1 and 0 – Stereo Mode

Note: *These bits are only available for SID 1. The function of these bits for SID 2 is reserved.*
These bits configure the stereo mode and the address location of the second SID.
When all three bits are set to 0, MONO mode is active and STEREO mode is disabled.
When one or more bits are set, SID 2 is mapped to the corresponding address space. Multiple bits can be set causing SID 2 to appear at multiple memory locations.
Note: *Please use the memory location DE00 with caution:*
Many external modules connected to the expansion port are using this memory location for other purposes. So use DE00 only when you are sure that this address location is unused. Nevertheless

DE00 is used by some external SID cartridges so setting this bit will enable FPGASID to replace such a cartridge.
SID 1 will always be mapped to address $D400.
Note: *Reset of internal state when switching back to mono:*
When the address mode is switched back to mono (bits are all 0), an internal reset of some SID states is triggered - This is done to achieve a perfect synchronization of both SIDs in mono mode. But it can also make it necessary to re-initialize the SID and restart the waveforms and envelopes especially when the switching occurs while the SIDs are actively generating sound.

Diagnostics mode

Reading this register returns the 6581 filter bias of SID1 and SID2 for configuration B.
Writing this register is reserved for future use.

Flash mode

Reading this register returns the 6581 filter bias of SID1 and SID2 for configuration B.
Writing this register is reserved for future use.

Register $1F/31 – SID Type

Normal mode

Reading this register is reserved for future use.
Writing this register is reserved for future use.

Configuration mode

Reading returns the value that has been written previously
Writing this register controls these configuration bits:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Source EXTIN: 00: analog input 01: disabled 10: other SID 11: digifix (8580)		writeregs readback: 00: bitrot 6581 01: always read value 10: always read $00 11: bitrot (8580)		reg delay: 0: 6581 1: 8580	mixed wave: 0: 6581 1: 8580	crunchy DAC: 0: on (6581) 1: off (8580)	Filter Mode: 0: 6581 1: 8580

Bit 7 and 6 – Source EXTIN:

Set the source that is being used for EXTIN.
To use the analog EXTIN input of FPGASID, set the value 00.
To disable the EXTIN input and cut off potential noise signals, set 01.
To route the output of the SID 2 to EXTIN of SID 1, set the value 10 in SID1
To route the output of the SID 1 to EXTIN of SID 2, set the value 10 in SID2
To use the digifix value written in register $1D/29, set 11.

Bits 5 and 4 – Register read mode:

A standard SID does not allow reading of the write registers. When such a register is read, the original SID returns the value that has been written to the SID chip last, regardless of which register the value was written to. The readout value disappears shortly after the write operation. After this time the value $00 is read (“bit rotting” or “bit fade”). 6581 and 8580 chips have different timings of this effect.

FPGASID can simulate the behavior of the original SID or it can allow reading all registers, which can be helpful for debugging.

To mimic the original 6581 bit rotting behavior set to 00.
To disable reading and return 0 on read attempts, set to 01.
To allow full reading of all registers, set to 10.
To mimic the original 8580 bit rotting behavior set to 11.

Bit 3 – Register delay mode

Set this bit to enable 8580 register delay mode. Clear the bit to switch back to 6581 mode.
This is important to allow most SID-type detection routines to detect the correct SID type.

Bit 2 – Mixed waveform mode

Set this bit to enable 8580 mixed waveforms. Clear this bit to enable 6581 waveforms.

Bit 1 – Crunchy DAC mode

Set this bit to disable nonlinear (“crunchy”) DACs as used for 8580.
Clear this bit to enable nonlinear DACs used for 6581.

Bit 0 – Analog Filter mode

Set this bit switch to 8580 analog filter circuit simulation. Clear the bit to switch to 6581 analog filter circuit simulation.

Diagnostics mode

Reading this register is reserved for future use.
Writing this register is reserved for future use.

Flash mode

Reading this register is reserved for future use.
Writing this register is reserved for future use.

Example Configurations

The following examples are demonstrated by small basic programs because BASIC is considered to be the most common programming language on Commodore computers. Of course the functionality can also be implemented in other languages.
All examples are written for the Commodore 64.

Full Software-Reset

Resetting FPGASID is not as trivial as one might think. Caused by the various register and memory configurations it is required to reset some registers in the correct order to achieve that all registers are cleared. Before clearing FPGASID should be switched to MONO mode in order to avoid that some of the SID 2 registers are forgotten.
Here is a commented BASIC program that is clearing really everything:

```
10 rem reset fpgasid the comprehensive
20 rem way. this method disables stereo
30 rem mode before resetting. it also
40 rem resets the oscillator phases
50 rem with the test bits to re-sync
60 rem both sids.
70 :
100 si=54272
105 :
110 rem set magic cookie
120 poke si+25,129:poke si+26,101
125 :
130 rem switch to mono
140 poke si+30,0
145 :
150 rem set magic cookie again to
151 rem assure that sid2 gets updated
152 poke si+25,129:poke si+26,101
153 :
155 rem set all test bits. this will
160 rem re-sync the oscillators for
170 rem perfect mono mode.
180 poke si+4,8
181 poke si+11,8
182 poke si+18,8
185 :
190 rem now write zero to all registers
200 rem start at register 31 and count
210 rem down to 0. this will clear the
220 rem magic cookie after the fpgasid
230 rem specific registers have been
235 rem written
240 for i=31 to 0 step -1
250 : poke si+i,0
260 next
265 :
270 rem now the fpgasid is reset to
280 rem default values. it will operate
290 rem in 6581 mono mode.
```

6581 mode

6581 mode is the default mode after reset. So to switch to 6581 mode simply reset the FPGASID following the steps in the Full Software Reset chapter. When the state of the SID configuration is known to be 8580, then the FPGASID can be set back to 6581 mode with the following Program.

```
100 si=54272
105 :
110 rem set magic cookie
120 poke si+25,129:poke si+26,101
125 :
130 rem switch to 6581
140 poke si+31,0
145 :
150 rem clear magic cookie
160 poke si+25,0:poke si+26,0
165 :
```

In MONO mode this is enough. However, when FPGASID is in STEREO mode, the second SID can be switched to 6581 mode as well:

```
170 rem when fpgasid is in stereo mode
180 rem we set sid 2 to 6581 mode as
190 rem well. (if not nobody cares)
200 s2=54272+32 :rem sid 2 at d420
201 rem s2=54272+256:rem sid 2 at d500
202 rem s2=54272+2560:rem sid 2 at de00
205 :
210 rem set magic cookie
220 poke s2+25,129:poke s2+26,101
225 :
230 rem switch to 6581
240 poke s2+31,0
245 :
250 rem clear magic cookie
260 poke s2+25,0:poke s2+26,0
```

Please note the different base address values in lines 200 to 202 depending on the stereo configuration. When multiple addresses are configured, it is enough to configure SID 2 at one of these addresses.

8580 mode

Here you find the same program as before. But now we switch both SIDs that are already in STEREO mode to 8580 mode:

```
100 si=54272
105 :
110 rem set magic cookie
120 poke si+25,129:poke si+26,101
125 :
130 rem switch to 8580
140 poke si+31,63
145 :
150 rem clear magic cookie
160 poke si+25,0:poke si+26,0
165 :
170 rem when fpgasid is in stereo mode
180 rem we set sid 2 to 8580 mode as
190 rem well. (if not nobody cares)
200 s2=54272+32  :rem sid 2 at d420
201 rem s2=54272+256 :rem sid 2 at d500
202 rem s2=54272+2560:rem sid 2 at de00
205 :
210 rem set magic cookie
220 poke s2+25,129:poke s2+26,101
225 :
230 rem switch to 8580
240 poke s2+31,63
245 :
250 rem clear magic cookie
260 poke s2+25,0:poke s2+26,0
```

As you can see, it is always a good idea to clear the magic cookie value after changing the configuration. When you do so, the FPGASID specific registers are protected and cannot be accidently overwritten by other software.

Plain Stereo Mode

Plain stereo mode means, that SID 1 and SID 2 are configured to two different memory addresses. Then existing programs, that require two SIDs to operate in stereo, can use both SIDs independently. The first SID 1 will always be located at address D400. The second SID 2 can be switched to D420, D500, DE00 and all combinations of these three addresses. The address DE00 should be avoided because this address range can easily collide with modules connected to the expansion slot. Luckily only very few existing programs are using that address. In this example we configure the second SID to D420 and D500, but not to DE00:

```
100 si=54272
110 rem set magic cookie
120 poke si+25,129:poke si+26,101
130 rem switch to stereo
140 poke si+30,3 : rem d420 + d500
150 rem clear magic cookie
160 poke si+25,0:poke si+26,0
170 rem also clear magic cookie for sid2
180 poke si+32+25,0:poke si+32+26,0
```

Please note that in the end (lines 170-180) we have to clear the magic cookie for the second SID separately because in stereo mode both SIDs are completely independent.

Pseudo Stereo 6581 + 8580

Despite the word ‘stereo’ in its name, in this special mode the FPGASID is configured to MONO mode, so all existing SID tunes that are made for a single SID chip will work. To achieve a pseudo stereo effect, Both SIDs will be configured to different SID types. This leads to a pseudo stereo effect especially for SID-tunes that are using a lot of filter effects.
Be careful: The program expects FPGASID to be in MONO mode. When it should be in STEREO mode, the magic cookie in line 120 would only be written to SID 1. So best would be to reset the SID before doing this:

```
10 rem pseudo stereo by switching sid1
20 rem to 6581 mode and sid 2 to 8580
30 rem mode. best suitable for mono sid
40 rem tunes with a lot of filtering
50 rem effects
60 :
100 s1=54272:s2=s1+32
105 :
110 rem set magic cookie
120 poke s1+25,129:poke s1+26,101
125 :
130 rem switch to stereo so we can
135 rem configure both sids
136 rem independently
140 poke s1+30,1:rem enable sid2 @ d420
145 :
150 rem switch sid 1 to 6581
160 poke s1+31,0
165 :
170 rem switch sid 2 to 8580
180 poke s2+31,63
185 :
190 rem now switch back to mono
200 poke s1+30,0
205 :
210 rem clear magic cookie
220 poke s1+25,0:poke s1+26,0
225 :
230 rem now sid1 is in 6581 mode
240 rem while sid2 is in 8580 mode
250 rem the result is a nice stereo
260 rem effect on all mono tunes
```

Pseudo Stereo Phase Shift

Another interesting way of achieving a pseudo stereo effect is to shift the oscillator phases of both SIDs against each other. This can be done by setting the oscillator frequencies of each SID to a different frequency which will move the phases away from each other in a more or less random way. Again, in the beginning, we expect to be in MONO mode:

```
10 rem set pseudo stereo mode using the
20 rem phase method. works best when
30 rem the sid tune is not using test
40 rem bits to resync the phases
50 :
100 s1=54272: s2=s1+32
105 :
110 rem set magic cookie
120 poke s1+25,129:poke s1+26,101
129 :
130 rem switch to stereo so we can
135 rem configure both sids
136 rem independently
140 poke s1+30,3
145 :
150 rem set sid 1 frequencies
160 poke s1+1,10
161 poke s1+8,20
162 poke s1+15,30
165 :
170 rem set sid 2 frequencies
180 poke s2+1,123
181 poke s2+8,234
182 poke s2+15,255
183 :
190 rem now switch back to mono
200 poke s1+30,0
205 :
210 rem clear magic cookie
220 poke s1+25,0:poke s1+26,0
225 :
230 rem now both sids have their
235 rem oscillators running at
240 rem different frequencies which
250 rem reliably randomises the
255 rem starting phases of the next
260 rem sid tune
```

Pseudo Stereo Voice based

Finally pseudo stereo can be configured by distributing the different voices to both channels. In our example we put voice 1 to SID 1 (left), voice 2 to SID 2 (right) and voice 3 to both SIDs (middle). Again we expect to be in MONO mode:

```
10 rem pseudo stereo using the voice
20 rem method. since this method
30 rem distributes the voices on both
40 rem channels, it gives good results
50 rem with all mono sid-tunes
60 :
100 s1=54272:s2=s1+32
105 :
110 rem set magic cookie
120 poke s1+25,129:poke s1+26,101
125 :
130 rem switch to stereo so we can
135 rem configure both sids
136 rem independently
140 poke s1+30,1:rem enable sid2 @ d420
145 :
150 rem set sid 2 to disable voice 1
160 poke s2+30,16*1
165 :
170 rem set sid 1 to disable voice 2
180 rem in the same time switch back
190 rem to mono mode
200 poke s1+30,16*2
205 :
210 rem clear magic cookie
220 poke s1+25,0:poke s1+26,0
225 :
230 rem now sid1 only plays voice 1&3
240 rem while sid2 plays only voice 2&3
250 rem the result is a nice stereo
260 rem effect on all mono tunes
```

Please note that register $1E/30 does not only control the voice muting but also the stereo addressing. So it may become quite tricky to configure these registers correctly in both SIDs without accidently switching back to mono mode too early. The safe way to do this is to always read-modify-write this register. The alternative way shown here heavily depends on the order in which the registers are written.

Digifix Setup

Here we show how the Digifix value can be used in 8580 mode to allow the playback of digi-samples using the classic volume register method. Original 8580 SIDs usually do not playback this kind of digis. So a workaround has been become popular where the external audio input EXTIN is applied with a DC offset by connecting a resistor between EXTIN and GND or VCC. The digifix mechanism inside FPGASID is exactly duplicating this behavior by applying a fixed offset to the EXTIN input. The level of this offset is configurable. A value of 100 is a good choice (see line 160).

```
100 si=54272
105 :
110 rem set magic cookie
120 poke si+25,129:poke si+26,101
125 :
130 rem switch to 8580+digifix
140 poke si+31,255
145 :
150 rem set digifix value
160 poke si+29,100
165 :
170 rem clear magic cookie
180 poke si+25,0:poke si+26,0
190 :
```