East West University

Presentation On

Implement a Memory Hierarchy Simulator to Analyze Cache Performance in C

Md. Saiful Islam
ID: 2022-3-60-045

Umme Mukaddisa
ID: 2022-3-60-317

Memory Hierarchy

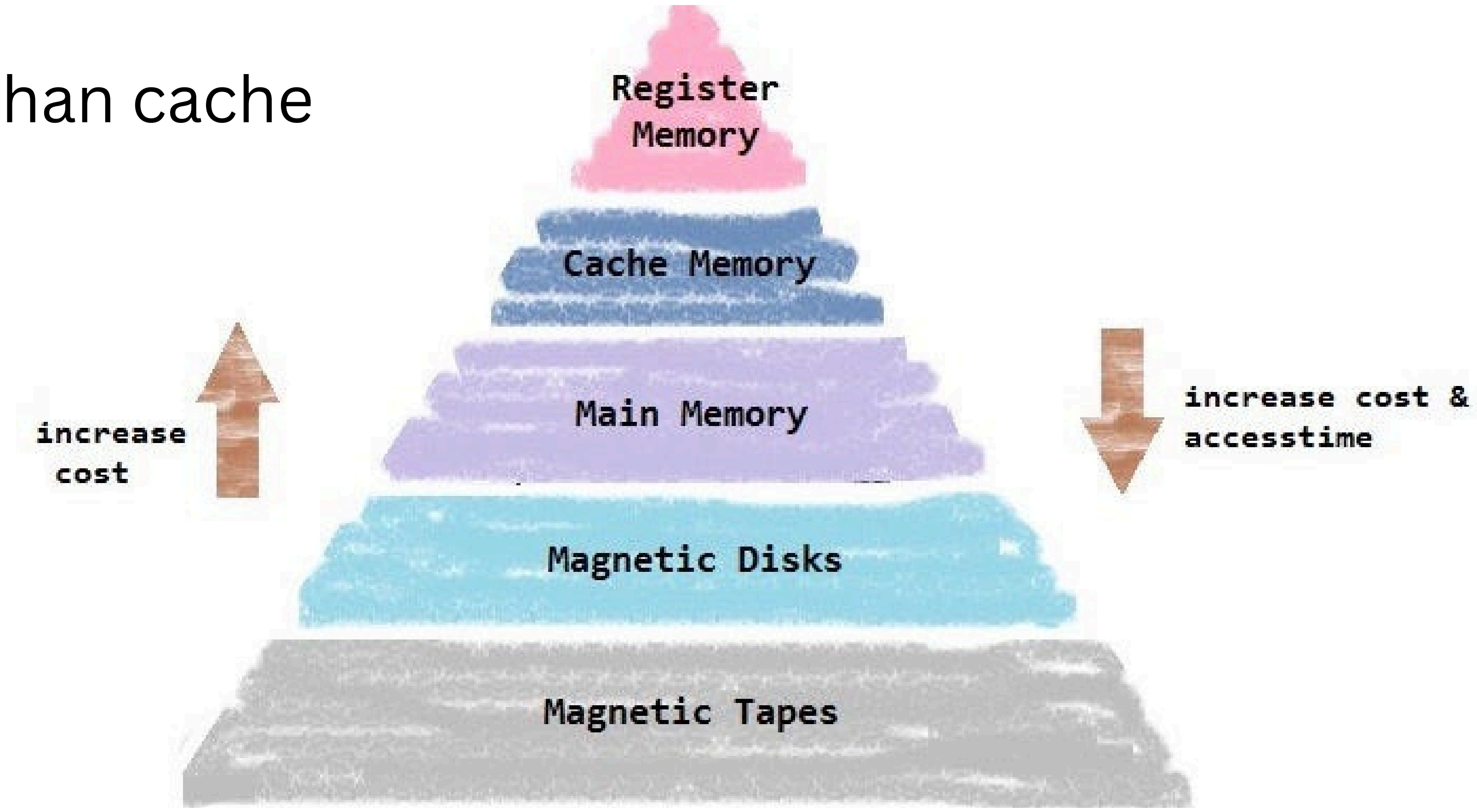
The memory hierarchy is the arrangement of various types of storage in a computer based on access speed. This levels can also be distinguished by their performance & controlling technologies.

1. **Registers** (In CPU)
2. **Internal or, Main Memory** (RAM , May include one or, more levels of **Cache**)
3. **External Memory**(Backing store)

Memory Hierarchy - Diagram

Internal or, main memory

It is the primary memory of a computer system. It is slower than cache memory but faster than secondary storage (hard-disk).



Cache Memory

It is the fastest type of memory & is located closest to the CPU. There are typically three levels of cache memory **L1, L2 & L3**, with each level having a larger capacity & slower access speed than the previous level.

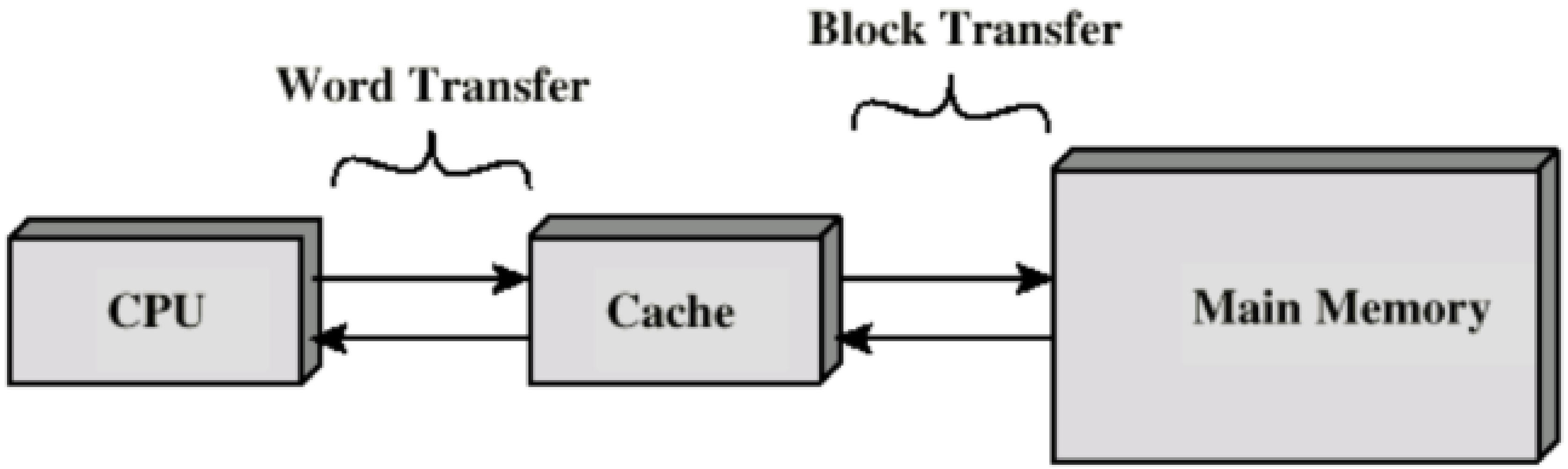
Register Memory

Registers are the fastest & smallest type of memory, located in CPU. They store small amounts of data that are frequently accessed by the CPU.

What is Cache?

Cache memory gives the fastest memory, at the same time provide s a large memory size. It sits between normal main memory (slower and relatively larger) & CPU.

When the processor attempts to read a word of memory, a check is made to determine if the word is in the cache. If so, the word is delivered to the processor. If not, a block of main memory consisting of some fixed number of words is read into the cache and then it is delivered to processor.



Cache Memory Mapping Technique

- **Direct Mapping**

Each block from main memory has only one possible place in the cache organization in this technique.

- **Associative Mapping**

In the associate mapping of the main memory block can be done with any of the cache block.

- **Set Associative Mapping**

It is the combination of advantages of both direct & associative mapping.

Cache used in this project

The simulator models a 3-level memory hierarchy with direct-mapped caches at both L1 & L2, followed by main memory.

L1 Cache (Level 1)

Structure: Direct, associative & set associative (**2 way set**) mapping
Blocks: 16
Block Size: 16 bytes (4words * 4 bytes)
Access Time: 1 cycle
Characteristics:

- Fastest and smallest cache level
- Simple address mapping
- Higher miss rate due to fixed block placement

L2 Cache (Level 2)

Structure: Direct, associative & set (**4 way set**) associative mapping
Blocks: 64 (4* more than L1)
Block Size: 16 bytes
Access Time: 10 cycles
Characteristics:

- Larger & slower than L1
- Reduces miss rate significantly
- Inclusive of L1 (contains all L1 data)

Main Memory for this simulation project

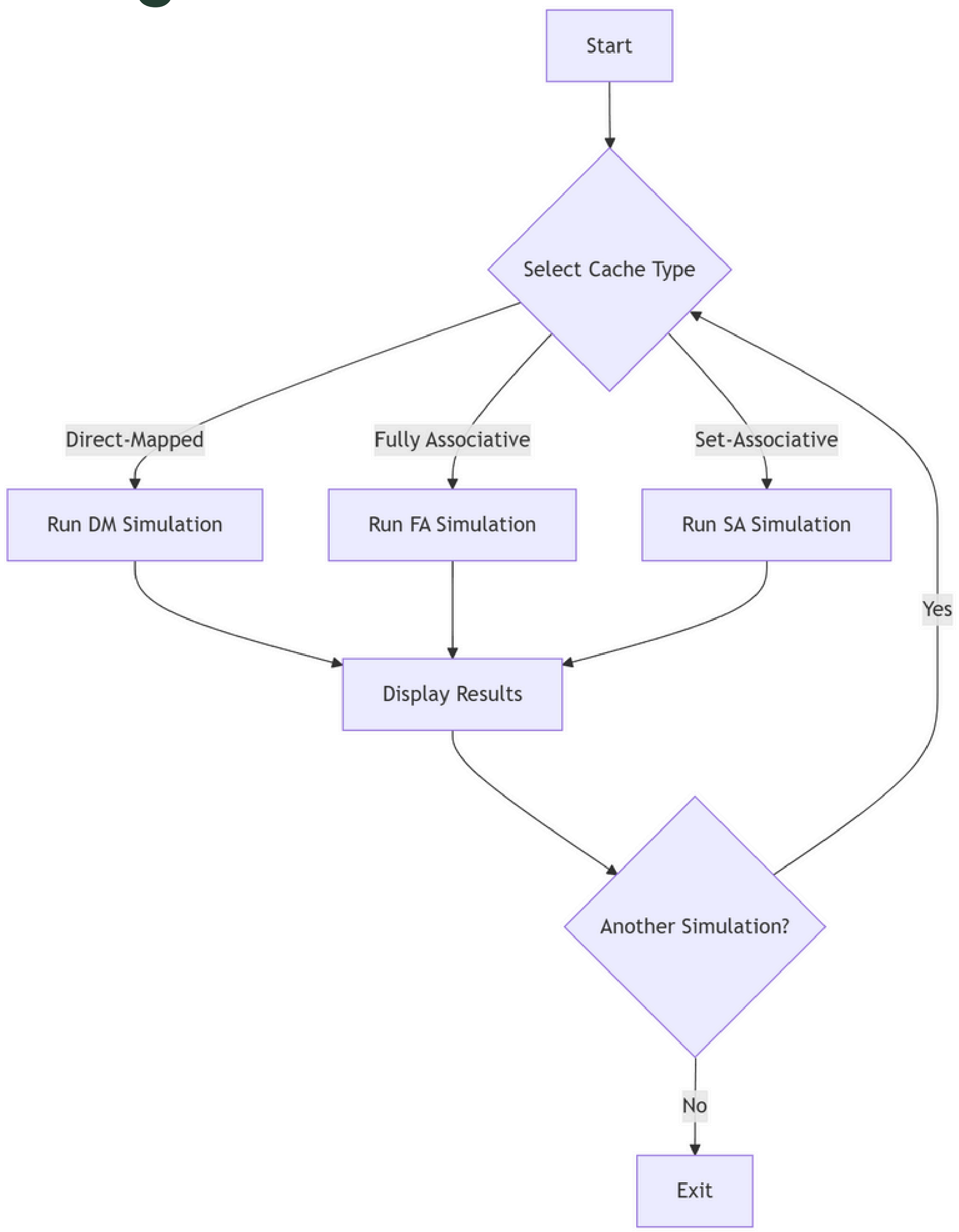
Main Memory

Model: Byte-addressable array
Blocks: 256
Block Size: 16 bytes
Access Time: 100 cycle
Characteristics:

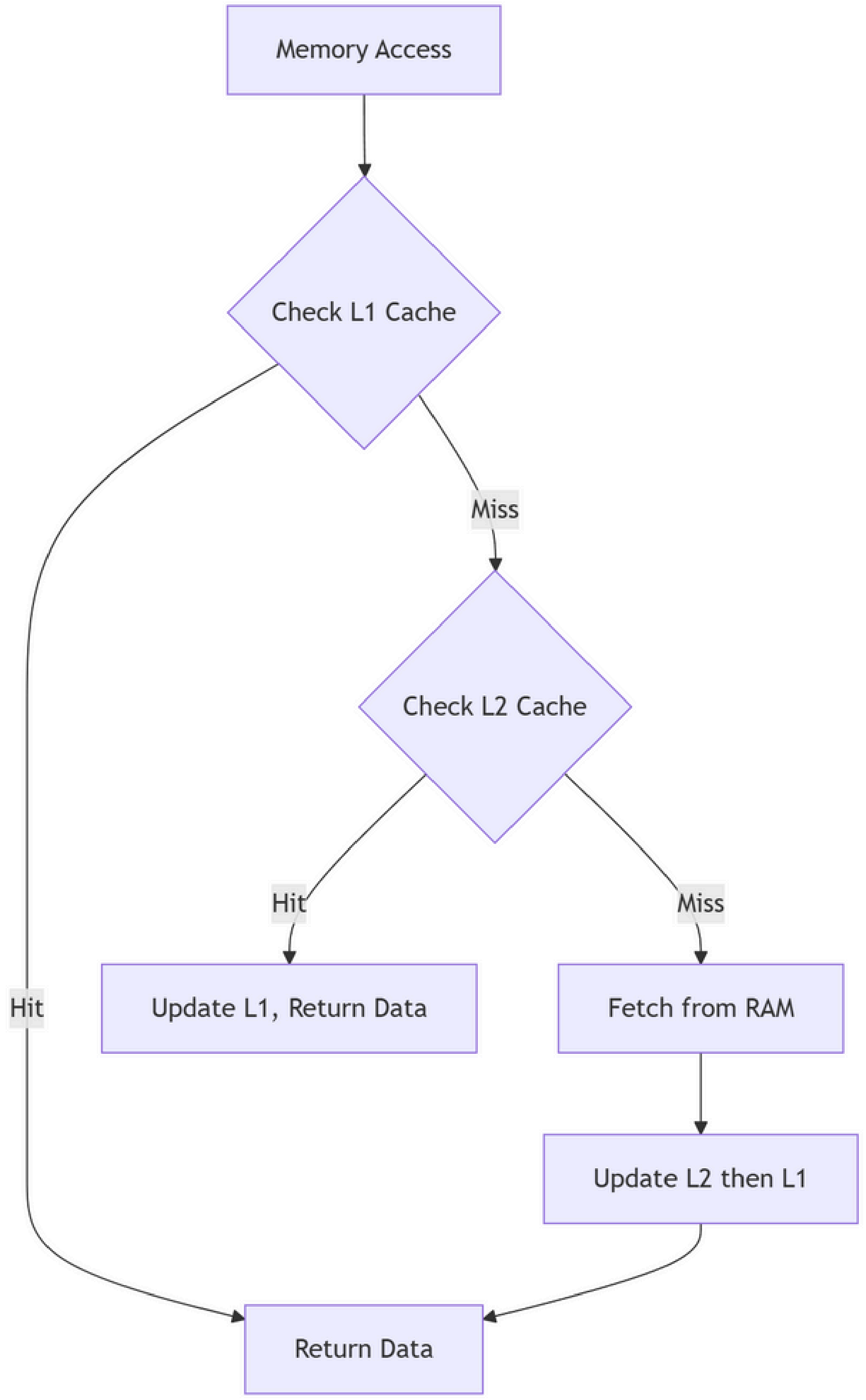
- Simulates DRAM timing
- Accessed only after L2 cache miss
- Transfer data in cache block sizes

Flowchart

Main Program Flow

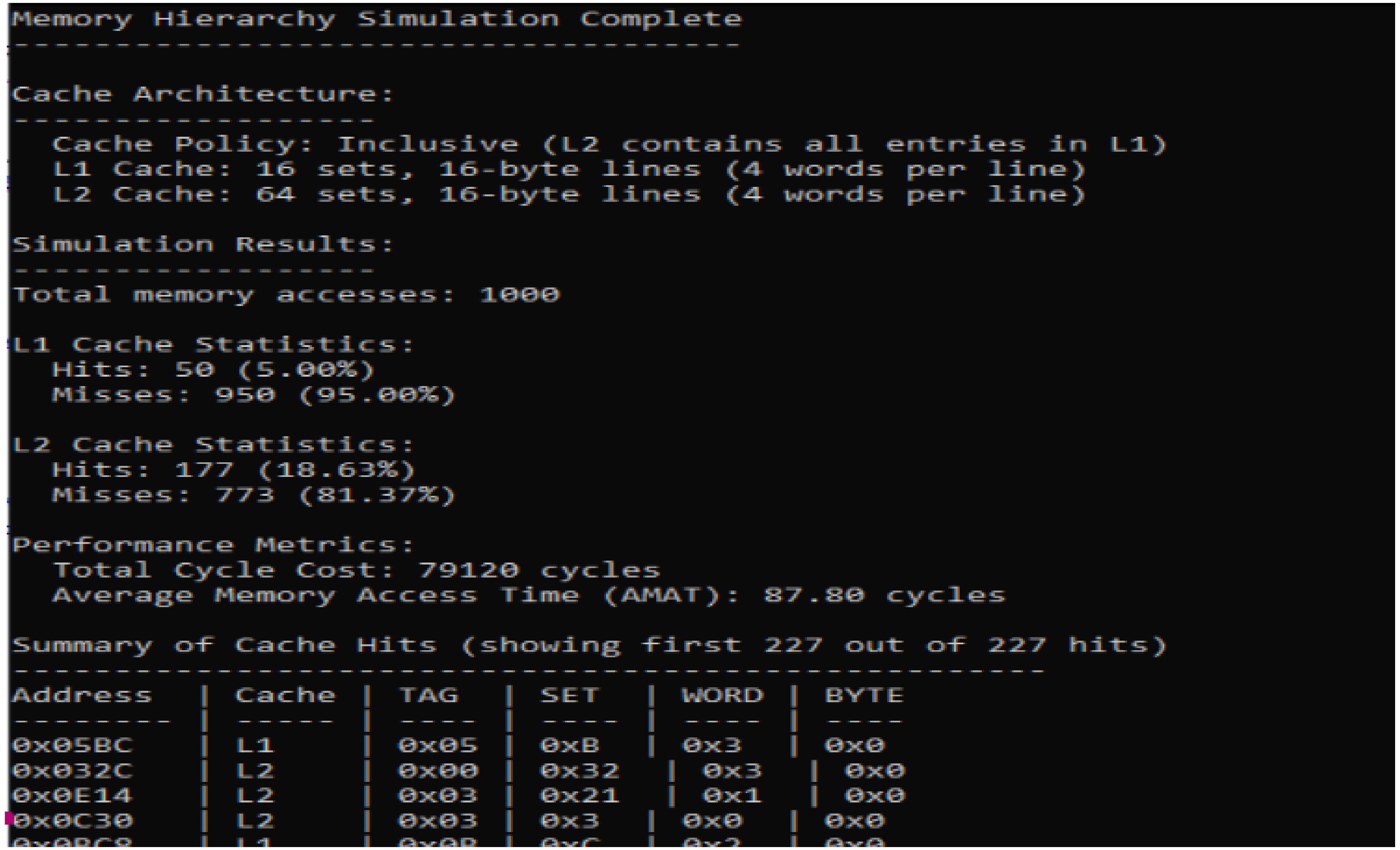


Cache Access Flow



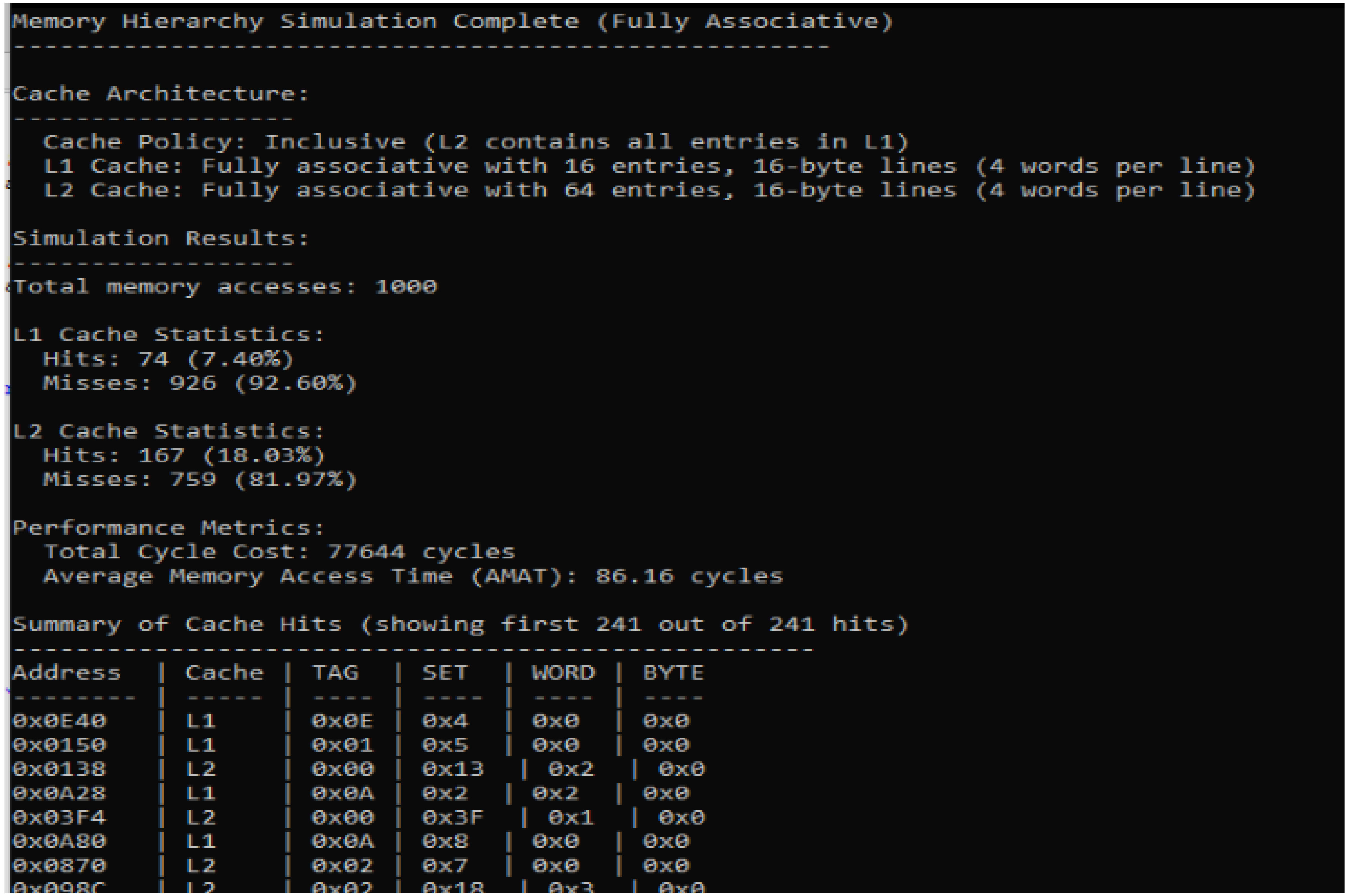
Performance Result

Direct Mapping (1000 random addresses)



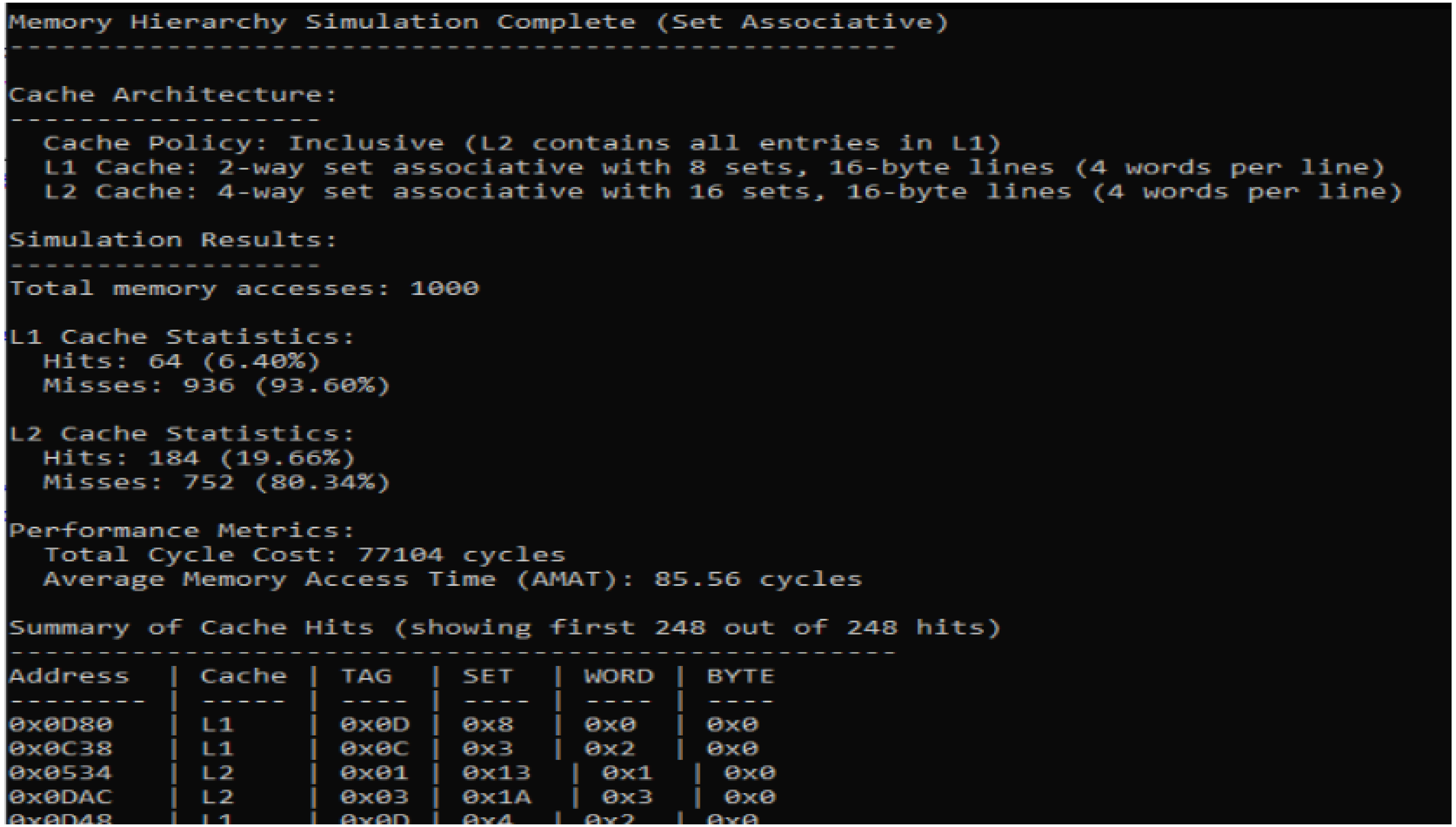
```
Memory Hierarchy Simulation Complete
------------------------------------

Cache Architecture:
------------------
  Cache Policy: Inclusive (L2 contains all entries in L1)
  L1 Cache: 16 sets, 16-byte lines (4 words per line)
  L2 Cache: 64 sets, 16-byte lines (4 words per line)

Simulation Results:
------------------
Total memory accesses: 1000

L1 Cache Statistics:
  Hits: 50 (5.00%)
  Misses: 950 (95.00%)

L2 Cache Statistics:
  Hits: 177 (18.63%)
  Misses: 773 (81.37%)

Performance Metrics:
  Total Cycle Cost: 79120 cycles
  Average Memory Access Time (AMAT): 87.80 cycles

Summary of Cache Hits (showing first 227 out of 227 hits)
---------------------------------------------------
Address    | Cache   | TAG    | SET    | WORD  | BYTE
--------   | -----   | ----   | ----   | ----  | ----
0x05BC     | L1      | 0x05   | 0xB    | 0x3   | 0x0
0x032C     | L2      | 0x00   | 0x32    | 0x3   | 0x0
0x0E14     | L2      | 0x03   | 0x21    | 0x1   | 0x0
0x0C30     | L2      | 0x03   | 0x3    | 0x0   | 0x0
0x0BC8     | L1      | 0x0B   | 0xC    | 0x2   | 0x0
```

Associative Mapping (1000 random addresses)



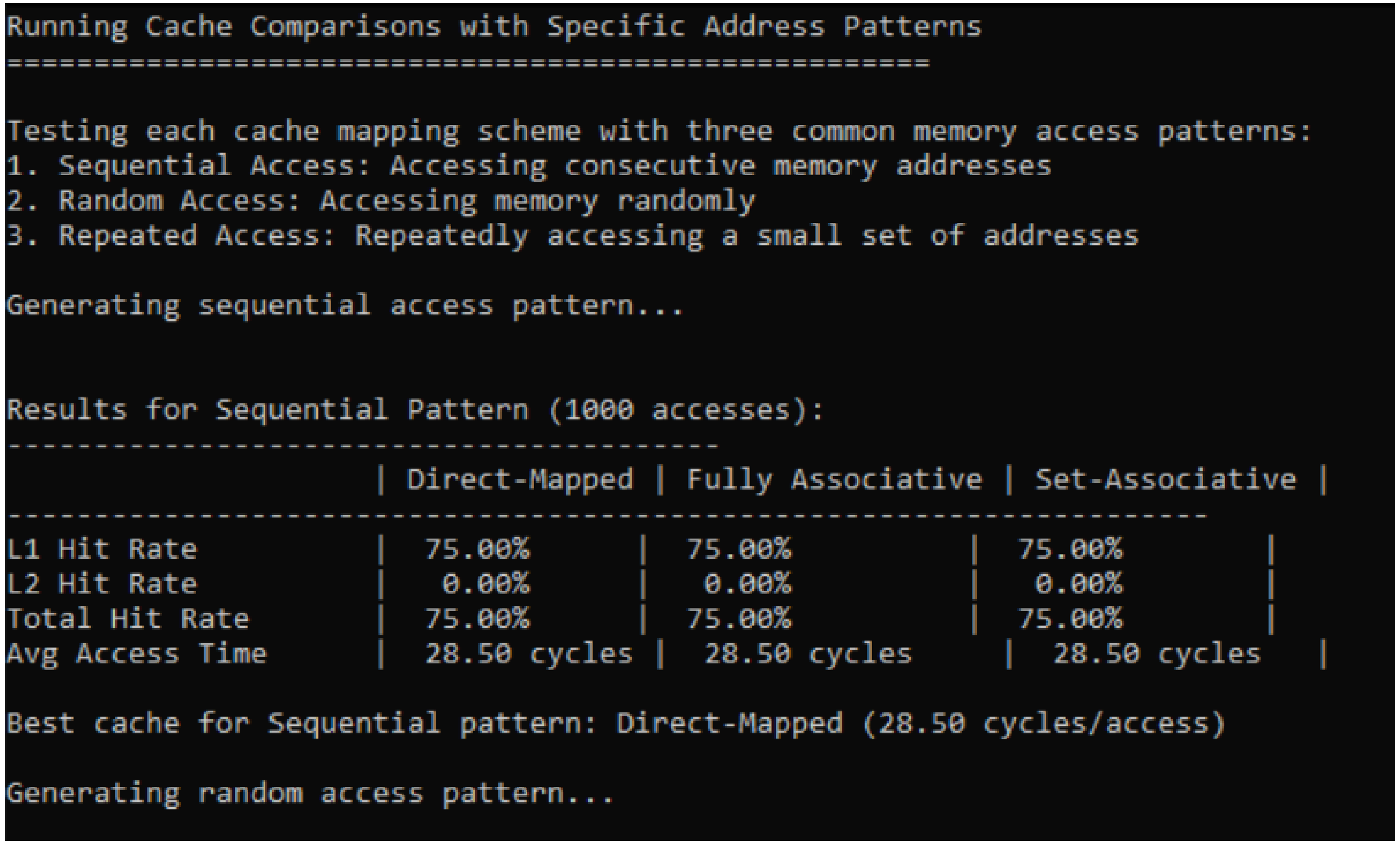
```
Memory Hierarchy Simulation Complete (Fully Associative)
----------------------------------------------------

Cache Architecture:
------------------
  Cache Policy: Inclusive (L2 contains all entries in L1)
  L1 Cache: Fully associative with 16 entries, 16-byte lines (4 words per line)
  L2 Cache: Fully associative with 64 entries, 16-byte lines (4 words per line)

Simulation Results:
------------------
Total memory accesses: 1000

L1 Cache Statistics:
  Hits: 74 (7.40%)
  Misses: 926 (92.60%)

L2 Cache Statistics:
  Hits: 167 (18.03%)
  Misses: 759 (81.97%)

Performance Metrics:
  Total Cycle Cost: 77644 cycles
  Average Memory Access Time (AMAT): 86.16 cycles

Summary of Cache Hits (showing first 241 out of 241 hits)
---------------------------------------------------
Address    | Cache  | TAG  | SET  | WORD | BYTE
--------   | -----  | ---- | ---- | ---- | ----
0x0E40     | L1     | 0x0E | 0x4  | 0x0  | 0x0
0x0150     | L1     | 0x01 | 0x5  | 0x0  | 0x0
0x0138     | L2     | 0x00 | 0x13  | 0x2  | 0x0
0x0A28     | L1     | 0x0A | 0x2  | 0x2  | 0x0
0x03F4     | L2     | 0x00 | 0x3F  | 0x1  | 0x0
0x0A80     | L1     | 0x0A | 0x8  | 0x0  | 0x0
0x0870     | L2     | 0x02 | 0x7  | 0x0  | 0x0
0x098C     | L2     | 0x02 | 0x18  | 0x3  | 0x0
```

Set Associative Mapping (1000 random addresses)

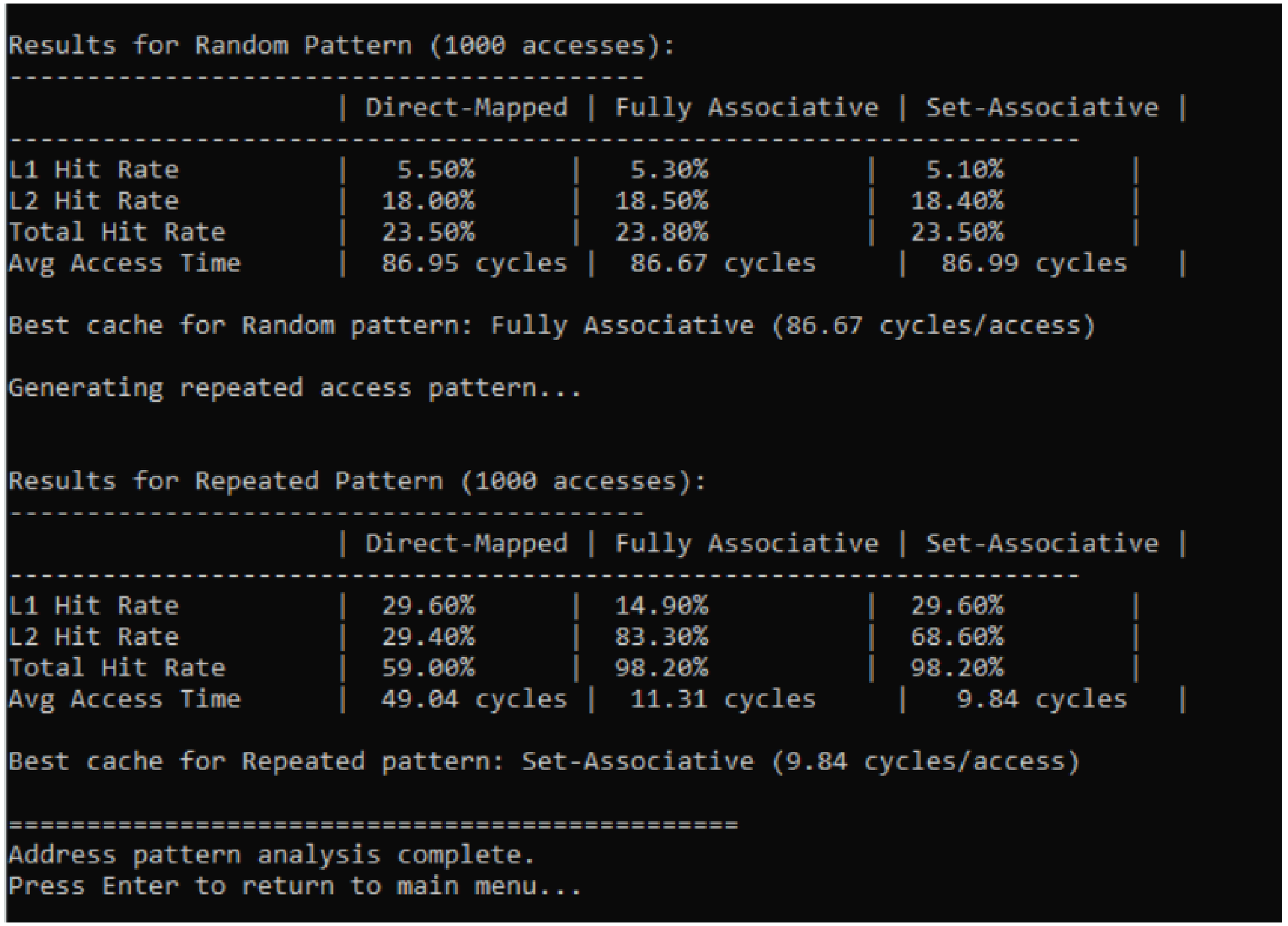


```
Memory Hierarchy Simulation Complete (Set Associative)
---------------------------------------------------

Cache Architecture:
------------------
  Cache Policy: Inclusive (L2 contains all entries in L1)
  L1 Cache: 2-way set associative with 8 sets, 16-byte lines (4 words per line)
  L2 Cache: 4-way set associative with 16 sets, 16-byte lines (4 words per line)

Simulation Results:
------------------
Total memory accesses: 1000

L1 Cache Statistics:
  Hits: 64 (6.40%)
  Misses: 936 (93.60%)

L2 Cache Statistics:
  Hits: 184 (19.66%)
  Misses: 752 (80.34%)

Performance Metrics:
  Total Cycle Cost: 77104 cycles
  Average Memory Access Time (AMAT): 85.56 cycles

Summary of Cache Hits (showing first 248 out of 248 hits)
---------------------------------------------------
Address    | Cache | TAG  | SET  | WORD | BYTE
--------   | ----- | ---- | ---- | ---- | ----
0x0D80     | L1    | 0x0D | 0x8  | 0x0  | 0x0
0x0C38     | L1    | 0x0C | 0x3  | 0x2  | 0x0
0x0534     | L2    | 0x01 | 0x13  | 0x1  | 0x0
0x0DAC     | L2    | 0x03 | 0x1A  | 0x3  | 0x0
0x0D48     | L1    | 0x0D | 0x4  | 0x2  | 0x0
```

Comparative Analysis Result



```
Running Cache Comparisons with Specific Address Patterns
=====================================================

Testing each cache mapping scheme with three common memory access patterns:
1. Sequential Access: Accessing consecutive memory addresses
2. Random Access: Accessing memory randomly
3. Repeated Access: Repeatedly accessing a small set of addresses

Generating sequential access pattern...


Results for Sequential Pattern (1000 accesses):
-----------------------------------------
                     | Direct-Mapped | Fully Associative | Set-Associative |
--------------------------------------------------------------------------
L1 Hit Rate          |  75.00%      |  75.00%          |  75.00%        |
L2 Hit Rate          |   0.00%      |   0.00%          |   0.00%        |
Total Hit Rate       |  75.00%      |  75.00%          |  75.00%        |
Avg Access Time      |  28.50 cycles |  28.50 cycles     |  28.50 cycles   |

Best cache for Sequential pattern: Direct-Mapped (28.50 cycles/access)

Generating random access pattern...
```



```
Results for Random Pattern (1000 accesses):
-----------------------------------------
                     | Direct-Mapped | Fully Associative | Set-Associative |
--------------------------------------------------------------------------
L1 Hit Rate          |   5.50%      |   5.30%          |   5.10%        |
L2 Hit Rate          |  18.00%      |  18.50%          |  18.40%        |
Total Hit Rate       |  23.50%      |  23.80%          |  23.50%        |
Avg Access Time      |  86.95 cycles |  86.67 cycles     |  86.99 cycles   |

Best cache for Random pattern: Fully Associative (86.67 cycles/access)

Generating repeated access pattern...


Results for Repeated Pattern (1000 accesses):
-----------------------------------------
                     | Direct-Mapped | Fully Associative | Set-Associative |
--------------------------------------------------------------------------
L1 Hit Rate          |  29.60%      |  14.90%          |  29.60%        |
L2 Hit Rate          |  29.40%      |  83.30%          |  68.60%        |
Total Hit Rate       |  59.00%      |  98.20%          |  98.20%        |
Avg Access Time      |  49.04 cycles |  11.31 cycles     |   9.84 cycles   |

Best cache for Repeated pattern: Set-Associative (9.84 cycles/access)

==============================================
Address pattern analysis complete.
Press Enter to return to main menu...
```

Conclusion

This project successfully simulated a memory hierarchy consisting of L1 & L2 caches along with main memory, allowing detailed analysis of cache behavior under various conditions. By implementing address breakdown, cache mapping techniques & realistic latency values, the simulator provided insights into how memory access patterns affect performance metrics such as hit rate, miss rate & average memory access time (AMAT).

Through experimentation with different access patterns—sequential, random, and repeated—the project demonstrated the importance of spatial & temporal locality in optimizing cache efficiency. The results highlight the trade-offs between cache size, speed, and complexity, which are essential considerations in modern processor design.

Overall, the simulator serves as an educational tool to better understand how caches works & how different architectural decisions can impact overall system performance.

THANK YOU