MIDDLE EAST TECHNICAL UNIVERSITY
ELECTRICAL AND ELECTRONICS ENGINEERING

EE 463 STATIC POWER CONVERSION-I HOMEWORK 3 REPORT

Prepared By

Hüseyin Umut Suna
Student ID: 2516938

Muhammed Raşid Gökcen
Student ID: 2443091

Instructor

Ogün Altun

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Introduction

This report focuses on the design of a duty controlled full bridge isolating converter. The aim of the study is to design a power converter with a rated output power of 250 W, operating from a 100 V input source and providing a regulated 24 V output voltage with limited peak-to-peak ripple.

In the first part of the report, the main electrical parameters of the converter are determined. The transformer turns ratio is calculated, followed by the design of the output filter components. The values of the output inductor and capacitor are obtained based on the given current and voltage ripple requirements.

In the second part, the magnetic design of the system is addressed. Suitable transformer and inductor cores are selected from manufacturer datasheets, and the corresponding number of turns are calculated. Important design constraints such as flux density, current density, fill factor, and saturation limits are checked to verify that the selected magnetic components operate safely and efficiently.

Overall, this report aims to demonstrate a complete and practical design approach for the given converter, using basic analytical calculations and reasonable engineering judgments.

Q1

The converter is a duty controlled full bridge isolating converter. Given values are:

$$P_o = 250\,\mathrm{W}, \quad V_{in} = 100\,\mathrm{V}, \quad V_o = 24\,\mathrm{V},$$

$$f_s = 200\,\mathrm{kHz}, \quad D = 0.45,$$

and the output voltage ripple is limited to 1% peak-to-peak.

(a)

Because a center-tapped full-wave rectifier is used, the output filter sees two pulses in one switching period. Therefore, an equivalent duty cycle can be written as

$$D_{eq} = 2D.$$

During the on-time, the voltage applied to the output inductor is the reflected secondary voltage:

$$V_x = \left(\frac{N_s}{N_p}\right) V_{in}.$$

The output stage behaves like an ideal buck converter, so

$$V_o = D_{eq} V_x = (2D)\left(\frac{N_s}{N_p}\right) V_{in}.$$

Solving for the turns ratio,

$$\frac{N_s}{N_p} = \frac{V_o}{2DV_{in}} = \frac{24}{0.9 \cdot 100} \approx 0.267.$$

$$\boxed{\frac{N_s}{N_p} \approx 0.267 \quad \text{(per half-secondary)}}$$

(b)

The output current is

$$I_o = \frac{P_o}{V_o} = \frac{250}{24} \approx 10.42\,\text{A}.$$

The inductor current ripple is chosen as 10% of the output current:

$$\Delta I_L^{pp} = 0.1 I_o \approx 1.04\,\text{A}.$$

Since there are two pulses per switching period,

$$f_{eq} = 2f_s = 400\,\text{kHz}, \quad D_{eq} = 0.9.$$

For an ideal buck converter,

$$\Delta I_L^{pp} = \frac{(V_x - V_o)D_{eq}}{L f_{eq}}.$$

The reflected input voltage is

$$V_x = \frac{V_o}{D_{eq}} = \frac{24}{0.9} \approx 26.67\,\text{V},$$

so

$$V_x - V_o \approx 2.67\,\text{V}.$$

Solving for the inductance,

$$L = \frac{(V_x - V_o)D_{eq}}{\Delta I_L^{pp} f_{eq}} \approx 5.76\,\mu\text{H}.$$

$$\boxed{L \approx 5.76\,\mu\text{H}}$$

(c)

The allowed output voltage ripple is

$$\Delta V_o^{pp} = 0.01 V_o = 0.24\,\text{V}.$$

For a CCM buck converter (ignoring ESR), the output voltage ripple is

$$\Delta V_o^{pp} = \frac{\Delta I_L^{pp}}{8 C f_{eq}}.$$

Solving for the capacitance,

$$C = \frac{\Delta I_L^{pp}}{8 f_{eq} \Delta V_o^{pp}} \approx 1.36\,\mu\text{F}.$$

$$\boxed{C \approx 1.36\,\mu\text{F}}$$

In practice, a larger low-ESR capacitor would be selected.

Q2

(a)

For the transformer, a ferrite core is selected from the Magnetics catalog. An **ETD39** core is chosen because it is suitable for 200 kHz operation and medium power levels.

Given core parameters:

$$A_e = 125 \text{ mm}^2, \quad V_e = 11500 \text{ mm}^3.$$

The peak flux density is calculated by

$$B_{pk} = \frac{V_{in} D}{2 N_p A_e f_s}.$$

Choosing $N_p = 15$ turns,

$$B_{pk} \approx 0.06 \text{ T},$$

which is well below the typical ferrite limit of 0.2 T.

From Q1,

$$\frac{N_s}{N_p} \approx 0.267,$$

so the secondary turns per half winding are selected as

$$N_s = 4.$$

$$\boxed{N_p = 15, \quad N_{s1} = N_{s2} = 4}$$

(b)

The magnetizing inductance is calculated using the A_L value from the datasheet:

$$L_m = A_L N_p^2.$$

For ETD39,

$$L_m \approx 0.73 \text{ mH}.$$

(c)

The average input current is estimated assuming 90% efficiency:

$$I_{in} \approx \frac{250}{0.9 \cdot 100} \approx 2.78 \text{ A}.$$

The RMS primary current is approximated as

$$I_{p,rms} \approx \frac{I_{in}}{\sqrt{2D}} \approx 2.9 \text{ A}.$$

Each half-secondary conducts for duty D, so

$$I_{s,rms} \approx I_o \sqrt{D} \approx 7.0 \text{ A}.$$

AWG14 is selected for the primary and AWG12 for the secondary. The resulting current densities are below 4 A/mm^2.

The total copper area in the window is approximately

$$A_{cu} \approx 57.7 \text{ mm}^2.$$

The window area is

$$W_a \approx 174.4 \text{ mm}^2.$$

Thus, the fill factor is

$$k_f \approx \frac{57.7}{174.4} \approx 0.33,$$

which satisfies the 30% requirement.

(d)

For the output inductor, a **Kool Mμ** toroidal core (77310A7) is selected because it can handle high DC current without saturation.

Given

$$A_L = 90 \text{ nH/turn}^2.$$

The required inductance is $L = 5.76\,\mu\text{H}$, so

$$N_L = \sqrt{\frac{L}{A_L}} = 8 \text{ turns}.$$

The peak inductor current is

$$I_{pk} \approx 10.94\,\text{A}.$$

From the DC bias curve, the inductance drop at this current is moderate, and the core operates safely below saturation.

(e)

The inductor RMS current is approximately

$$I_L \approx 10.42\,\text{A}.$$

Using $J \leq 4\,\text{A/mm}^2$, AWG13 wire is sufficient. The estimated fill factor is about 54%, which is acceptable, although using two parallel thinner wires would make winding easier.

(f)

A detailed loss calculation would require exact mean length per turn values. However, since the flux density is low and the selected wire sizes have low current density, both transformer and inductor losses are expected to remain below the given 15 W limit. Since all design constraints were satisfied with sufficient margin in the first attempt, no further numerical iteration was required.

Q3)

a)

The duty controlled full bridge isolating converter was designed and simulated using LTspice to verify the operational requirements. The simulation model was constructed using the design parameters derived in the analytical sections (Q1 and Q2) to verify the theoretical performance of the converter. Our schematic can be seen as figure 1 below.

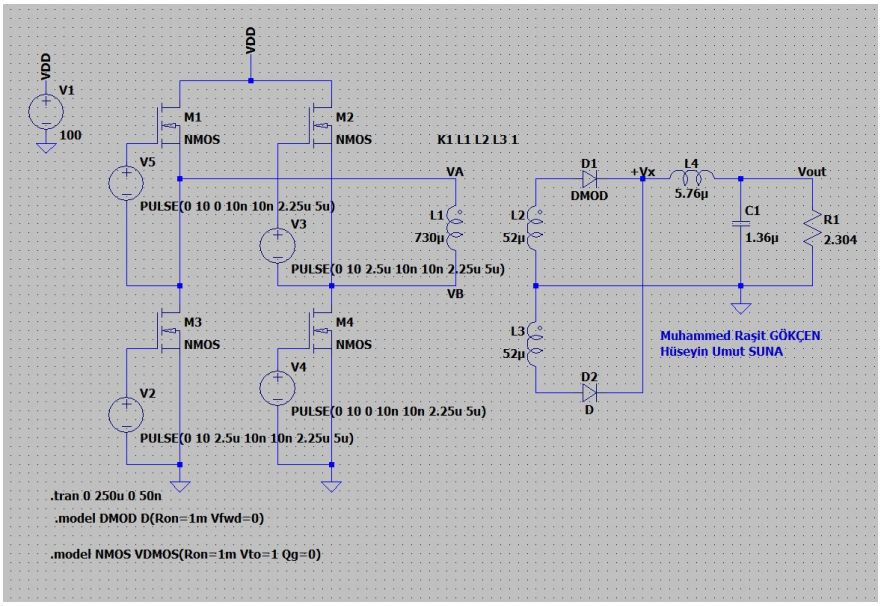

Figure 1: Schematic of Duty Controlled Full Bridge Isolating Converter

Primary Voltage (V_P): As shown in Figure 2, the primary transformer voltage oscillates between +100V and -100V. This confirms the correct push-pull operation, where the two primary switches are driven 180 degrees out of phase. A distinct dead-time is observed at 0V, which is necessary to prevent shoot-through currents.

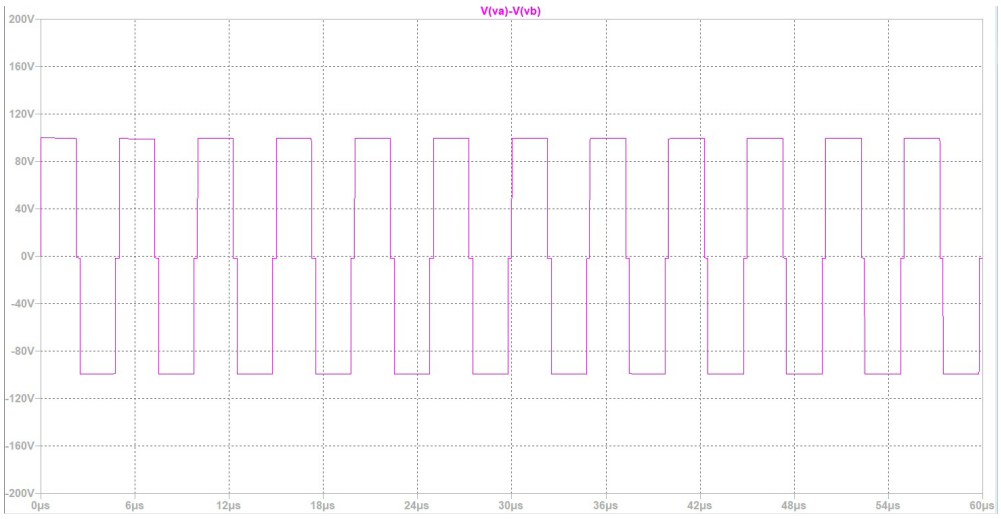

Figure 2: Primary Voltage (V_P)

Output Voltage (V_{out}): As can be seen in Figure 3, the simulation demonstrates a stable output voltage of approximately 24V, which aligns with the design specifications.

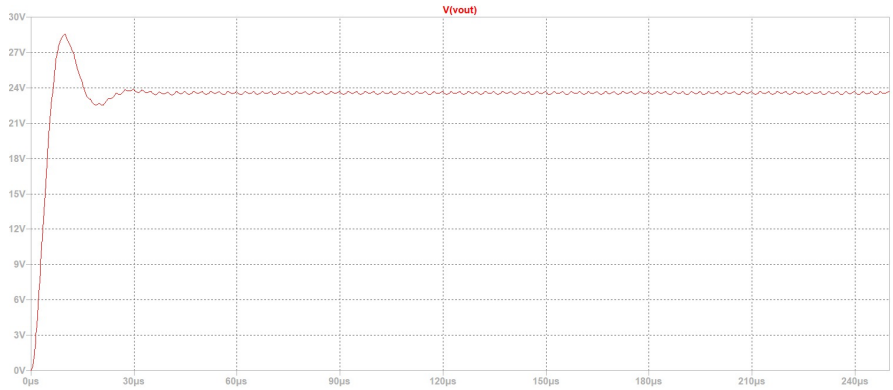

Figure 3: Output Voltage (V_{out})

Secondary Winding Voltage (V_x): The voltage waveform at node V_x (across the secondary winding L_2) is observed to pulse between V and approximately 27V as can be seen on figure 4.

Active State: When the primary side drives the corresponding polarity, the voltage across L_2 rises to its peak 27V, forward-biasing diode D_1 and delivering current to the output filter.

Inactive State: During the alternate half-cycle (when the lower winding L_3 is active) and the dead-time intervals, the voltage at node V_x remains at 0V, as the transformer action drives the other half of the secondary winding.

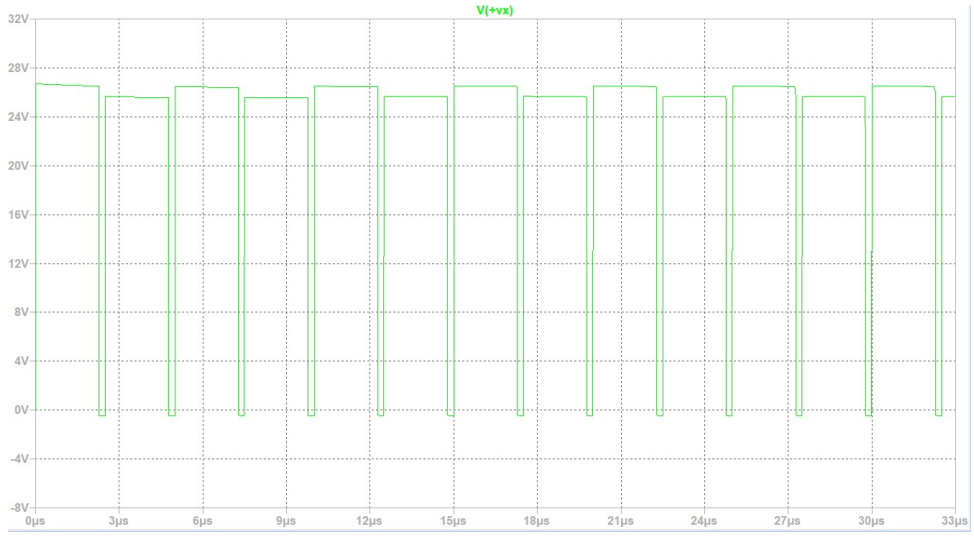

Figure 4: Secondary Winding Voltage (V_x)

Inductor Current (i_L): As presented in Figure 5, the current flowing through the output filter inductor (L_4) exhibits a continuous triangular waveform, confirming that the converter operates in Continuous Conduction Mode (CCM). The current oscillates around a DC average of approximately 10A, which corresponds to the steady-state load requirement, while the linear ramp-up and ramp-down phases represent the energy storage and release cycles during the switching period. This controlled ripple behavior validates the filter design, ensuring that current is delivered to the output capacitor without interruption.

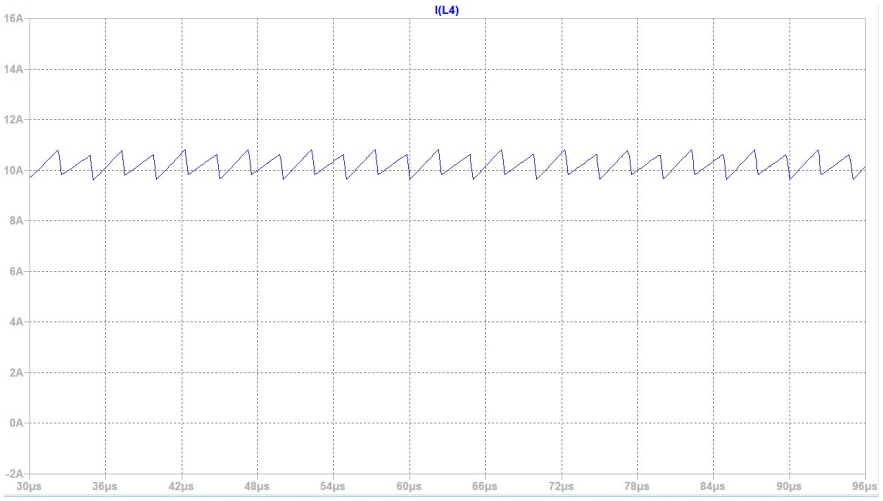

Figure 5: Inductor Current (i_L)

MOSFET Drain-Source Voltage (V_{sw1}): As depicted in Figure 6, the voltage across the primary-side MOSFET (M_1) alternates between a conducting state of 0V and a blocking state of 100V. Since the circuit utilizes a Full-Bridge topology, the maximum voltage stress across each switch is clamped strictly to the DC input voltage (V_{in}). The waveform confirms that during the off-state, the MOSFET blocks exactly 100V, with no significant voltage overshoot observed.

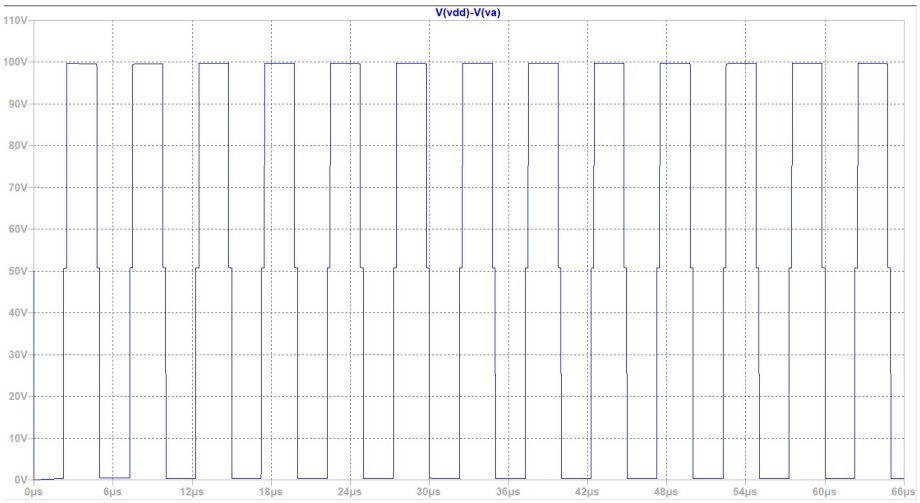

Figure 6: MOSFET Drain-Source Voltage

The simulation results align closely with the theoretical design; however, slight discrepancies are observed due to the inclusion of parasitic elements.

Analytically, the output voltage is calculated as ideal (V_{out}= 2D. n.V_{in}). In the simulation, the presence of cable resistances (R_{cable}) for the inductor and transformer, along with the forward voltage drop of the rectifier diodes and MOSFET on-resistance ($R_{DS(on)}$), results in a slightly lower output voltage than the ideal calculation. This is expected behavior and represents a more realistic model of the converter.

Required Component Ratings:

- Semiconductors (MOSFETs): The simulation shows a peak voltage stress of 100V. To ensure reliability against transient spikes and ringing, a rating of 150V or higher is recommended.
- Rectifier Diodes: The diodes must block the full secondary voltage during the off-states. Based on the secondary peak voltage (≈27V) and reverse ringing, a rating of 60V or 100V is suitable.
- Output Capacitor: The steady-state voltage across the output capacitor is approximately 24V with minimal ripple. A commercial capacitor with a voltage rating of 35V or 50V would provide an adequate safety margin (typically derated by 20-50%).

b)

In a real world scenario, transformers always exhibit leakage inductance (L_{1k}) because magnetic coupling is never 100% efficient.

- In a real circuit, the leakage inductance stores energy ($E = \frac{1}{2}.L_{lk}.I^2$). When a MOSFET turns off, this energy cannot dissipate instantaneously. This forces a sharp voltage spike ($V_{spike} = L_{lk}.\frac{di}{dt}$) across the switch, often significantly exceeding the steady-state voltage.

- This leakage energy resonates with the parasitic capacitance of the MOSFETs, causing high-frequency ringing oscillations on the voltage waveform.

These transient spikes are critical because they can exceed the breakdown voltage (V_{DSS}) of the semiconductors, leading to failure. Therefore, unlike an ideal simulation, a real hardware design must include snubber circuits to clamp these spikes and protect the components.

c)

1. Component Selection
    - MOSFET: IRF640N (200V, 18A, 0.15Ω) Selected for its 200V rating, providing a safe margin over the 100V switching stress
    - Diode: MBR20100CT (100V, 20A, Schottky). Selected for low forward voltage drop (0.8V) and fast switching capability.

2. Power Loss Calculations
    - MOSFET Losses: Conduction: $P_{cond} = {I_{RMS}}^2 \times R_{DS(on)} \approx 1.81^2 A \times 0.15\ \Omega = 0{,}49W$
    - Switching:
    $$P_{sw} = \frac{1}{2} V_{in} \times I_{pri}.\left(t_r + t_f\right).f_w \approx 2.16W$$
    Total Per Switch: $P_{total} = 2.65W$
    - Diode Losses: Total Per Diode: $P_{diode} \approx V_F \times I_{avg} = 0.8V\ \times 5A = 4W$

3. Thermal Analysis & Heatsink Selection
    - Ambient Temperature (T_A): 40˚C. Without a heatsink, the diode junction temperature would reach $T_J = 40 + \left(4W \times 60\ ^\circ\frac{C}{W}\right) = 280\ ^\circ C$, which destroys the device. A heatsink is mandatory.
    - Heatsink Selection: A standard heatsink with $R_{\theta SA} = 10\ ℃/W$ (e.g. Aavid 530614) was selected. With the heatsink, the diode temperature is:

$$T_J = 40\ ℃ + 4W\ \times (2 + 1 + 10)℃/W = 92℃$$

This remains well below the safety limit of 125℃.

d)

To make the converter bidirectional so power can flow back from the output to the input, you need to replace the two diodes on the secondary side with MOSFETs. This changes the circuit into a synchronous rectifier, which allows current to be controlled in both directions instead of just being blocked by the diodes. Comparing this to the first design, the main difference is that the original circuit with diodes is strictly one-way and much simpler to build since diodes work automatically. The modified version with MOSFETs is more complex because it requires extra gate drivers and control logic to switch them at the right times.

However, the modified version is actually more efficient because MOSFETs have very low resistance when they are on, wasting less power than the fixed voltage drop of the diodes.

Conclusion

In this project, a 250W Duty Controlled Full Bridge Converter was designed to regulate a 100V input to a 24V output. The analytical design phase established the key electrical parameters, resulting in a transformer turns ratio of approximately 0.267 and an output filter (5.76μH inductor, 1.36μF capacitor) designed to limit current ripple to 10%. The magnetic design was successfully realized using an ETD39 ferrite core for the transformer ($N_p = 15, N_s = 4$) and a Kool Mu toroidal core for the inductor, ensuring operation within safe flux and current density limits.

The LTspice simulation verified these design choices, confirming stable operation in Continuous Conduction Mode (CCM) with results that aligned closely with the theoretical calculations. Beyond the ideal analysis, the study highlighted practical real-world constraints. Discrepancies in the output voltage were identified because of parasitic component resistances. Furthermore, the thermal analysis proved that while the selected commercial semiconductors (IRF640N and MBR20100CT) are electrically suitable, they require heatsinks to operate safely. Finally, the investigation into leakage inductance and synchronous rectification demonstrated that a physical prototype would require snubber circuits for protection and active switching for bidirectional capability.