

**CS322 ALGORITHM LABORATORY**  
**MINI PROJECT**  
**EXTENDING FUNCTIONALITY OF MARS MIPS ASSEMBLER**  
**SUBMITTED BY: KHUSHI PRASAD ROLL NUMBER: 2001CS38**

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**CACHE:**

They refer to memory storage managed to take advantage of locality of access. They bridge the speed gap between processor and main memory. A cache provides the processor requested data from the memory. If it is not found in the cache, the data item is then stored in the cache from the main memory. However, cache has limited storage.

So, in case of full storage, how to decide which block to replace? There are certain Block Replacement Policies for the same.

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**BLOCK REPLACEMENT POLICIES:**

Mars already provides us with two types of replacement policies - LRU and Random. We have extended this functionality and included 3 more block replacement policies - LFU, FIFO AND LRU-2.

**1. Least Recently Used:**

This algorithm replaces the block that has not been used for the longest period of time. It is based on the observation that blocks that have not been used for a long time will probably remain unused for the longest time and thus, be replaced.

**2. Random:**

This algorithm replaces blocks randomly.

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Following Cache Simulation functionalities have been added:

**1. Least Frequently Used:**

This algorithm replaces the block that has been accessed the least number of times.

### **IMPLEMENTATION:**

Defined 2 new variables:

- accesscount -> one to keep track of the number of times the respective block has been accessed.
- leastAccesscount -> one to keep track of the global minima.

We initialise the variable <accesscount> whenever the respective memory block is accessed.

- When a set is full or it is not in the cache, it is initialised to 1.
- When it is found in the cache, the value of the variable is increased by one.

In case of full set,

- We iterate over all the blocks updating <leastAccesscount> and storing the respective block.
- At the end of the loop, the block that has been accessed the least number of times is replaced.

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## **2. First IN First OUT:**

In this algorithm, the oldest block, which has spent the longest time in memory is chosen and replaced

### **IMPLEMENTATION:**

Define 2 new variables:

- creationtime -> to store the time when the blocks were first used.
- leastRecentCreationtime -> to store the least creation time.

We initialise the variable <creationtime> whenever the respective memory block is accessed.

- When the set is full or the data item is found in cache, the respective variable is initialised to memoryAccesscount.

In case of full set,

- We iterate over all the blocks updating <leastRecentCreationtime> and storing the respective block.
  - At the end of the loop, the block that has been accessed the earliest is replaced.
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### 3. LRU-2:

In this, instead of the most recent access time, we compare the second most recent access time of the block. Generally speaking, LRU-k compares the kth recent access time for comparison and deciding which block has to be replaced in case of a full set.

#### IMPLEMENTATION:

Define 2 new variables:

- secondmostRecentAccesstime -> to store the time when the blocks were used second most recent time.
- leastRecentsecondAccessTime -> to store the least second most access time of all the blocks.

We initialise the variable <secondmostRecentAccesstime> whenever the respective memory block is accessed.

- In case the set is full or the data item is not in the cache, we initialise the respective variable with a large arbitrary number.
- In case the data item is already in the cache and need not be fetched from the memory, we assign the value of the variable <mostRecentAccesstime> to <secondmostRecentAccesstime> and update the value of <mostRecentAccesstime>.

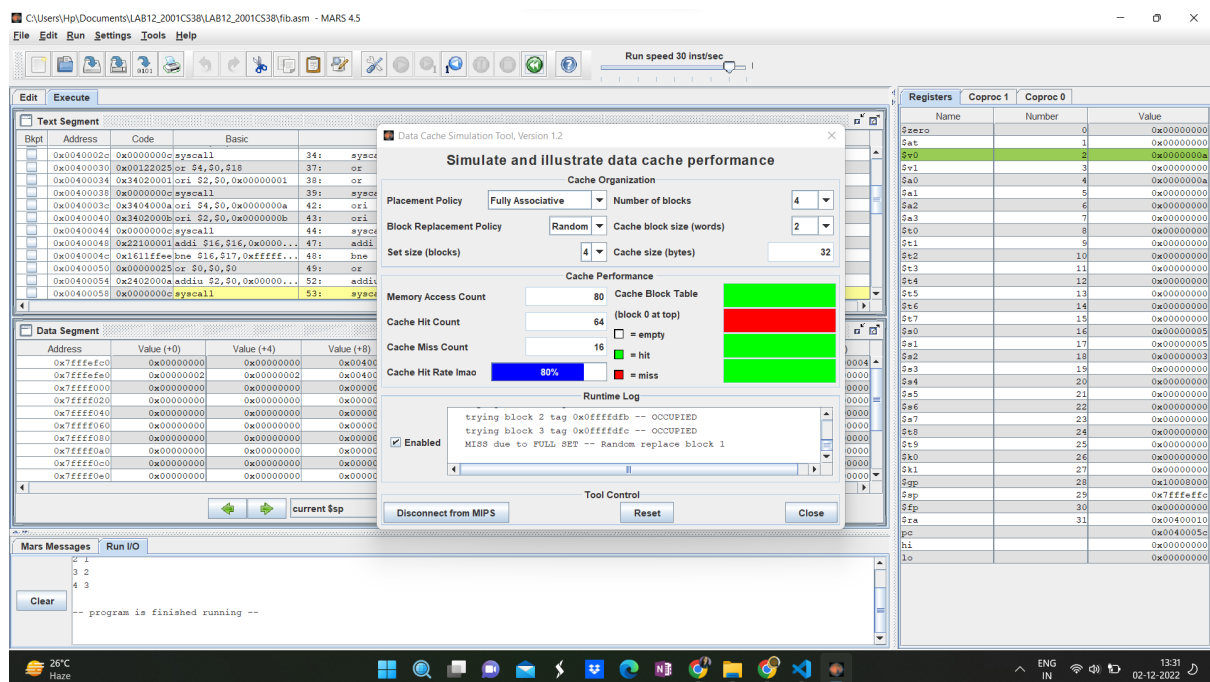
In case of full set,

- We iterate over all the blocks updating <leastRecentsecondAccessTime> and storing the respective block.
  - At the end of the loop, the block with the least second most recent access time is replaced.
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### PERFORMANCE COMPARISON:

We will consider 4 blocks in the cache, where each block can store 2 words each. For performance comparison, we will consider two standard programs - Fibonacci and Factorial of a Number (Recursive Method).

## 1. RANDOM:



## 2. FIFO:



Simulate and illustrate data cache performance

Cache Organization

Placement Policy: Fully Associative Number of blocks: 4

Block Replacement Policy: LRU Cache block size (words): 2

Set size (blocks): 4 Cache size (bytes): 32

Cache Performance

Memory Access Count: 80 Cache Block Table (block 0 at top)

Cache Hit Count: 67

Cache Miss Count: 13

Cache Hit Rate Imao: 84%

Runtime Log

trying block 1 tag 0x0ffffdfe -- OCCUPIED  
trying block 2 tag 0x0ffffdfe -- OCCUPIED  
trying block 3 tag 0x0ffffdfe -- OCCUPIED  
MISS due to FULL SET -- LRU replace block 0; unused since (73)

Tool Control

Disconnect from MIPS Reset Close

Registers

Name	Number	Value
\$zero	0	0x00000000
\$at	1	0x00000000
\$v0	2	0x0000000a
\$v1	3	0x00000000
\$a0	4	0x0000000a
\$a1	5	0x00000000
\$a2	6	0x00000000
\$a3	7	0x00000000
\$a0	8	0x00000000
\$t1	9	0x00000000
\$t2	10	0x00000000
\$t3	11	0x00000000
\$t4	12	0x00000000
\$t5	13	0x00000000
\$t6	14	0x00000000
\$t7	15	0x00000000
\$a0	16	0x00000005
\$a1	17	0x00000005
\$a2	18	0x00000003
\$a3	19	0x00000000
\$a4	20	0x00000000
\$a5	21	0x00000000
\$a6	22	0x00000000
\$a7	23	0x00000000
\$t8	24	0x00000000
\$t9	25	0x00000000
\$t0	26	0x00000000
\$t1	27	0x00000000
\$fp	28	0x10008000
\$fp	29	0x7ffffefc
\$ra	30	0x00400010
\$ra	31	0x0040005c
\$pc		0x00000000
\$hi		0x00000000
\$lo		0x00000000

Mars Messages

Run I/O

Clear

program is finished running --

## 5. LRU 2

Simulate and illustrate data cache performance

Cache Organization

Placement Policy: Fully Associative Number of blocks: 4

Block Replacement Policy: LRU 2.0 Cache block size (words): 2

Set size (blocks): 4 Cache size (bytes): 32

Cache Performance

Memory Access Count: 80 Cache Block Table (block 0 at top)

Cache Hit Count: 67

Cache Miss Count: 13

Cache Hit Rate Imao: 84%

Runtime Log

trying block 2 tag 0x0ffffdfe -- OCCUPIED  
trying block 3 tag 0x0ffffdfe -- OCCUPIED  
MISS due to FULL SET -- LRU-2 replace block 0; second last use at

Tool Control

Disconnect from MIPS Reset Close

Registers

Name	Number	Value
\$zero	0	0x00000000
\$at	1	0x00000000
\$v0	2	0x0000000a
\$v1	3	0x00000000
\$a0	4	0x0000000a
\$a1	5	0x00000000
\$a2	6	0x00000000
\$a3	7	0x00000000
\$t0	8	0x00000000
\$t1	9	0x00000000
\$t2	10	0x00000000
\$t3	11	0x00000000
\$t4	12	0x00000000
\$t5	13	0x00000000
\$t6	14	0x00000000
\$t7	15	0x00000000
\$a0	16	0x00000005
\$a1	17	0x00000005
\$a2	18	0x00000003
\$a3	19	0x00000000
\$a4	20	0x00000000
\$a5	21	0x00000000
\$a6	22	0x00000000
\$a7	23	0x00000000
\$t8	24	0x00000000
\$t9	25	0x00000000
\$t0	26	0x00000000
\$t1	27	0x00000000
\$fp	28	0x10008000
\$fp	29	0x7ffffefc
\$ra	30	0x00400010
\$ra	31	0x0040005c
\$pc		0x00000000
\$hi		0x00000000
\$lo		0x00000000

Mars Messages

Run I/O

Clear

program is finished running --

## ANALYSIS:

REPLACEMENT POLICY	HIT RATE
RANDOM	80%
FIFO	75%

LFU	75%
LRU	84%
LRU-2	84%

FIFO and LFU replacement policies have the worst performance. They have the least cache hit rate. And for FIFO as it is observed, the cache hit rate decreases when the number of blocks is increased. It can be attributed to the fact that FIFO sometimes replaces an active block and brings it back after two or three memory accesses. This takes many times, because it writes in cache and brings it back to main memory in two steps.

LRU is the better algorithm to implement in these conditions. The cache hit rate for LRU is even greater than Random.

## FACTORIAL RECURSIVE CODE:

### 1. RANDOM:

C:\Users\Hp\Documents\LAB12\_2001CS38\LAB12\_2001CS38\fac\_rec.asm - MARS 4.5

File Edit Run Settings Tools Help

Run speed 30 inst/sec

**Simulate and illustrate data cache performance**

Cache Organization

Placement Policy: Fully Associative Number of blocks: 4

Block Replacement Policy: Random Cache block size (words): 2

Set size (blocks): 4 Cache size (bytes): 32

Cache Performance

Memory Access Count: 105

Cache Hit Count: 80

Cache Miss Count: 25

Cache Hit Rate: 76%

Cache Block Table (block 0 at top)

Cache Hit Rate: 76%

Runtime Log

Enabled

Tool Control

Disconnect from MIPS Reset Close

**Registers**

Name	Number	Value
\$zero	0	0x00000000
\$at	1	0x10010000
\$v0	2	0x00000004
\$v1	3	0x00000000
\$a0	4	0x00000000
\$a1	5	0x00000000
\$a2	6	0x00000000
\$a3	7	0x00000000
\$a0	8	0x00000001
\$t1	9	0x10010004
\$t2	10	0x10010008
\$t3	11	0x00000018
\$t4	12	0x00000000
\$t5	13	0x00000000
\$t6	14	0x00000000
\$t7	15	0x00000000
\$a0	16	0x00000018
\$a1	17	0x00000000
\$a2	18	0x00000000
\$a3	19	0x00000000
\$a4	20	0x00000000
\$a5	21	0x00000000
\$a6	22	0x00000000
\$a7	23	0x00000000
\$s8	24	0x00000000
\$s9	25	0x00000000
\$k0	26	0x00000000
\$k1	27	0x00000000
\$gp	28	0x00000000
\$fp	29	0x7fffffc0
\$sp	30	0x00000000
\$ra	31	0x00000034
\$pc		0x00400084
\$hi		0x00000000
\$lo		0x00000018

**Mars Messages** Run I/O

Clear

-- program is finished running --

Positive integer: Positive integer: The value of factorial(4) is 24

-- program is finished running --

### 2. FIFO:

3. LRU:

The screenshot shows the Data Cache Simulation Tool interface. The 'Cache Organization' section is configured with 'Fully Associative' placement policy, 'FIFO' block replacement policy, 4 blocks, and 32 bytes per block. The 'Cache Performance' section shows a memory access count of 105, a cache hit count of 81, a cache miss count of 24, and a cache hit rate of 77%. The 'Runtime Log' shows the following entries:

```

trying block 0 tag 0x02002006 -- OCCUPIED
trying block 1 tag 0x0ffffdfe -- OCCUPIED
trying block 2 tag 0x02002001 -- OCCUPIED
trying block 3 tag 0x02002007 -- HIT

```

The 'Registers' table on the right shows the state of the registers:

Name	Number	Value
\$zero	0	0x00000000
\$at	1	0x10010000
\$v0	2	0x0000000a
\$v1	3	0x00000000
\$a0	4	0x00000000
\$a1	5	0x00000000
\$a2	6	0x00000000
\$a3	7	0x00000000
\$a4	8	0x00000000
\$a5	9	0x10010004
\$a6	10	0x10010008
\$a7	11	0x00000018
\$a8	12	0x00000000
\$a9	13	0x00000000
\$t0	14	0x00000000
\$t1	15	0x00000000
\$t2	16	0x00000018
\$t3	17	0x00000000
\$t4	18	0x00000000
\$t5	19	0x00000000
\$t6	20	0x00000000
\$t7	21	0x00000000
\$t8	22	0x00000000
\$t9	23	0x00000000
\$s0	24	0x00000000
\$s1	25	0x00000000
\$s2	26	0x00000000
\$s3	27	0x00000000
\$s4	28	0x10008000
\$s5	29	0x7ffffefc
\$s6	30	0x00000000
\$s7	31	0x00400034
\$pc		0x00000000
\$hi		0x00000000
\$lo		0x00000018

4. LRU:

The screenshot shows the Data Cache Simulation Tool interface. The 'Cache Organization' section is configured with 'Fully Associative' placement policy, 'LFR' block replacement policy, 4 blocks, and 32 bytes per block. The 'Cache Performance' section shows a memory access count of 105, a cache hit count of 68, a cache miss count of 37, and a cache hit rate of 65%. The 'Runtime Log' shows the following entries:

```

trying block 0 tag 0x02002007 -- HIT
(105) address: 0x1001003c (tag 0x02002007) block range: 0-3
trying block 0 tag 0x02002007 -- HIT

```

The 'Registers' table on the right shows the state of the registers:

Name	Number	Value
\$zero	0	0x00000000
\$at	1	0x10010000
\$v0	2	0x0000000a
\$v1	3	0x00000000
\$a0	4	0x00000000
\$a1	5	0x00000000
\$a2	6	0x00000000
\$a3	7	0x00000000
\$a4	8	0x00000000
\$a5	9	0x10010004
\$a6	10	0x10010008
\$a7	11	0x00000018
\$a8	12	0x00000000
\$a9	13	0x00000000
\$t0	14	0x00000000
\$t1	15	0x00000000
\$t2	16	0x00000018
\$t3	17	0x00000000
\$t4	18	0x00000000
\$t5	19	0x00000000
\$t6	20	0x00000000
\$t7	21	0x00000000
\$t8	22	0x00000000
\$t9	23	0x00000000
\$s0	24	0x00000000
\$s1	25	0x00000000
\$s2	26	0x00000000
\$s3	27	0x00000000
\$s4	28	0x10008000
\$s5	29	0x7ffffefc
\$s6	30	0x00000000
\$s7	31	0x00400034
\$pc		0x00000000
\$hi		0x00000000
\$lo		0x00000018



Run speed at max (no interaction)

File Edit Run Settings Tools Help

Text Segment

Bkpt	Address	Code	Basic
0x00400000	0x3c011001	lui \$1,0x00001001	30: la
0x00400004	0x34200000	ori \$9,\$1,0x00000000	
0x00400008	0x8d040000	lw \$4,0x00000000(\$9)	31: lw
0x0040000c	0x24020004	addiu \$2,\$0,0x00000000	32: li
0x00400010	0x00000000	syscall	33: syscall
0x00400014	0x24020004	addiu \$2,\$0,0x00000000	37: li
0x00400018	0x00000000	syscall	38: syscall
0x0040001c	0x00024021	addu \$8,\$0,\$2	39: move
0x00400020	0x00082021	addu \$4,\$0,\$8	41: move
0x00400024	0x23bffff4	addi \$29,\$29,0xfffff4	42: addi
0x00400028	0xafaf0000	sw \$8,0x00000000(\$29)	43: sw
0x0040002c	0xafbf0008	sw \$31,0x00000008(\$29)	44: sw

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)
0x10010000	0x1001000e	0x1001001f	0x1001001e
0x10010004	0x7420e568	0x65756c61	0x206666
0x10010008	0x00000000	0x00000000	0x00000000
0x1001000c	0x00000000	0x00000000	0x00000000
0x10010010	0x00000000	0x00000000	0x00000000
0x10010014	0x00000000	0x00000000	0x00000000
0x10010018	0x00000000	0x00000000	0x00000000
0x1001001c	0x00000000	0x00000000	0x00000000
0x10010020	0x00000000	0x00000000	0x00000000
0x10010024	0x00000000	0x00000000	0x00000000
0x10010028	0x00000000	0x00000000	0x00000000
0x1001002c	0x00000000	0x00000000	0x00000000

Mars Messages

Reset: reset completed.

Positive integer: Positive integer: The value of factorial(4) is 24

-- program is finished running --

Registers

Name	Number	Value
\$zero	0	0x00000000
\$at	1	0x10010000
\$v0	2	0x0000000a
\$v1	3	0x00000000
\$a0	4	0x00000018
\$a1	5	0x00000000
\$a2	6	0x00000000
\$a3	7	0x00000000
\$a0	8	0x00000001
\$t1	9	0x10010004
\$t2	10	0x10010008
\$t3	11	0x00000018
\$t4	12	0x00000000
\$t5	13	0x00000000
\$t6	14	0x00000000
\$t7	15	0x00000000
\$a0	16	0x00000018
\$a1	17	0x00000000
\$a2	18	0x00000000
\$a3	19	0x00000000
\$a4	20	0x00000000
\$a5	21	0x00000000
\$a6	22	0x00000000
\$a7	23	0x00000000
\$t8	24	0x00000000
\$t9	25	0x00000000
\$t0	26	0x00000000
\$t1	27	0x00000000
\$gp	28	0x10008000
\$gp	29	0x7ffffefc
\$gp	30	0x00000000
\$ra	31	0x00400084
\$pc		0x00000000
\$hi		0x00000000
\$lo		0x00000018

Simulate and illustrate data cache performance

Cache Organization

Placement Policy: Fully Associative

Block Replacement Policy: LRU

Set size (blocks): 4

Cache block size (words): 2

Cache size (bytes): 32

Cache Performance

Memory Access Count: 105

Cache Hit Count: 82

Cache Miss Count: 23

Cache Hit Rate: 78%

Runtime Log

trying block 0 tag 0x02002001 -- OCCUPIED

trying block 1 tag 0x02002006 -- OCCUPIED

trying block 2 tag 0xfffff4 -- OCCUPIED

trying block 3 tag 0x02002007 -- HIT

Tool Control

Disconnect from MIPS

Reset

Close

## 5. LRU 2:

Run speed at max (no interaction)

File Edit Run Settings Tools Help

Text Segment

Bkpt	Address	Code	Basic
0x00400000	0x3c011001	lui \$1,0x00001001	30: la
0x00400004	0x34200000	ori \$9,\$1,0x00000000	
0x00400008	0x8d040000	lw \$4,0x00000000(\$9)	31: lw
0x0040000c	0x24020004	addiu \$2,\$0,0x00000000	32: li
0x00400010	0x00000000	syscall	33: syscall
0x00400014	0x24020004	addiu \$2,\$0,0x00000000	37: li
0x00400018	0x00000000	syscall	38: syscall
0x0040001c	0x00024021	addu \$8,\$0,\$2	39: move
0x00400020	0x00082021	addu \$4,\$0,\$8	41: move
0x00400024	0x23bffff4	addi \$29,\$29,0xfffff4	42: addi
0x00400028	0xafaf0000	sw \$8,0x00000000(\$29)	43: sw
0x0040002c	0xafbf0008	sw \$31,0x00000008(\$29)	44: sw

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)
0x10010000	0x1001000e	0x1001001f	0x1001001e
0x10010004	0x7420e568	0x65756c61	0x206666
0x10010008	0x00000000	0x00000000	0x00000000
0x1001000c	0x00000000	0x00000000	0x00000000
0x10010010	0x00000000	0x00000000	0x00000000
0x10010014	0x00000000	0x00000000	0x00000000
0x10010018	0x00000000	0x00000000	0x00000000
0x1001001c	0x00000000	0x00000000	0x00000000
0x10010020	0x00000000	0x00000000	0x00000000
0x10010024	0x00000000	0x00000000	0x00000000
0x10010028	0x00000000	0x00000000	0x00000000
0x1001002c	0x00000000	0x00000000	0x00000000

Mars Messages

Reset: reset completed.

Positive integer: Positive integer: The value of factorial(4) is 24

-- program is finished running --

Registers

Name	Number	Value
\$zero	0	0x00000000
\$at	1	0x10010000
\$v0	2	0x0000000a
\$v1	3	0x00000000
\$a0	4	0x00000018
\$a1	5	0x00000000
\$a2	6	0x00000000
\$a3	7	0x00000000
\$t0	8	0x00000001
\$t1	9	0x10010004
\$t2	10	0x10010008
\$t3	11	0x00000018
\$t4	12	0x00000000
\$t5	13	0x00000000
\$t6	14	0x00000000
\$t7	15	0x00000000
\$a0	16	0x00000018
\$a1	17	0x00000000
\$a2	18	0x00000000
\$a3	19	0x00000000
\$a4	20	0x00000000
\$a5	21	0x00000000
\$a6	22	0x00000000
\$a7	23	0x00000000
\$t8	24	0x00000000
\$t9	25	0x00000000
\$t0	26	0x00000000
\$t1	27	0x00000000
\$gp	28	0x10008000
\$gp	29	0x7ffffefc
\$gp	30	0x00000000
\$ra	31	0x00400084
\$pc		0x00000000
\$hi		0x00000000
\$lo		0x00000018

Simulate and illustrate data cache performance

Cache Organization

Placement Policy: Fully Associative

Block Replacement Policy: LRU 2.0

Set size (blocks): 4

Cache block size (words): 2

Cache size (bytes): 32

Cache Performance

Memory Access Count: 105

Cache Hit Count: 78

Cache Miss Count: 27

Cache Hit Rate: 74%

Runtime Log

trying block 0 tag 0x02002007 -- HIT

(105) address: 0x1001003c (tag 0x02002007) block range: 0-3

trying block 0 tag 0x02002007 -- HIT

Tool Control

Disconnect from MIPS

Reset

Close

## ANALYSIS:

REPLACEMENT POLICY	HIT RATE
RANDOM	76%

FIFO	77%
LFU	65%
LRU	74%
LRU-2	74%

As observed, LFU has the least Cache Hit rate out of all Replacement Policies. In the above program, the smaller numbers will be used more times as compared to the larger numbers. Thus, in case of a full set, the LFU replacement policy will replace the block containing the larger numbers (of the numbers stored in the cache). But these numbers will also be required further in computation. This will cause an increase in Miss Rate.

In this case, FIFO performs the best and has a Cache Hit Rate greater than the Random Cache Hit Rate. FIFO stores the number nearest to the argument in cache and thus reduces miss rate.

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### **CONCLUSION:**

Thus, from our observation of the above two recursive codes, we can summarise the replacement policies as under:

REPLACEMENT POLICY	COMMENT
RANDOM	
FIFO	Might replace important blocks
LFU	Not Efficient
LRU	Excellent, but difficult to implement, as it requires substantial hardware assistance
LRU-2	Efficiency increases as the size of cache increases

### **Video Link:**

[https://drive.google.com/drive/folders/1VM16\\_2UeBGkK9XlCCpzFHpE3b209zsu1?usp=sharing](https://drive.google.com/drive/folders/1VM16_2UeBGkK9XlCCpzFHpE3b209zsu1?usp=sharing)