Requirement Specification of

Flight Control System Test Unit (FTU)

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1. INTRODUCTION

The FTU is a programmable signal synthesizer, i.e. function generator, provided on-board. The FTU facilitates the User to initiate the generation of synthetic signal of pre-defined characteristics and inject the synthesized signals at pre-defined points of the Control Computer for performing the testing i.e. Flutter test and parameter Estimation / System Identification (PID) test. The synthetic signal characteristics are pre-defined and pre-programmed on Erasable Programmable Read Only Memory (EPROM) / Flash Memory module.

2. SYSTEM DESCRIPTION

The FTU is a programmable signal synthesizer, i.e. function generator, provided on-board to facilitate the User to initiate the generation of synthetic signals of pre-defined characteristics and inject the synthesized signals at pre-defined points of the Control Computer. The synthetic signal characteristics (period/frequency, amplitude etc.) are pre-defined and stored on EPROM / Flash for every test point. The interface block diagram of FTU Control Computer are shown in Figure 1.

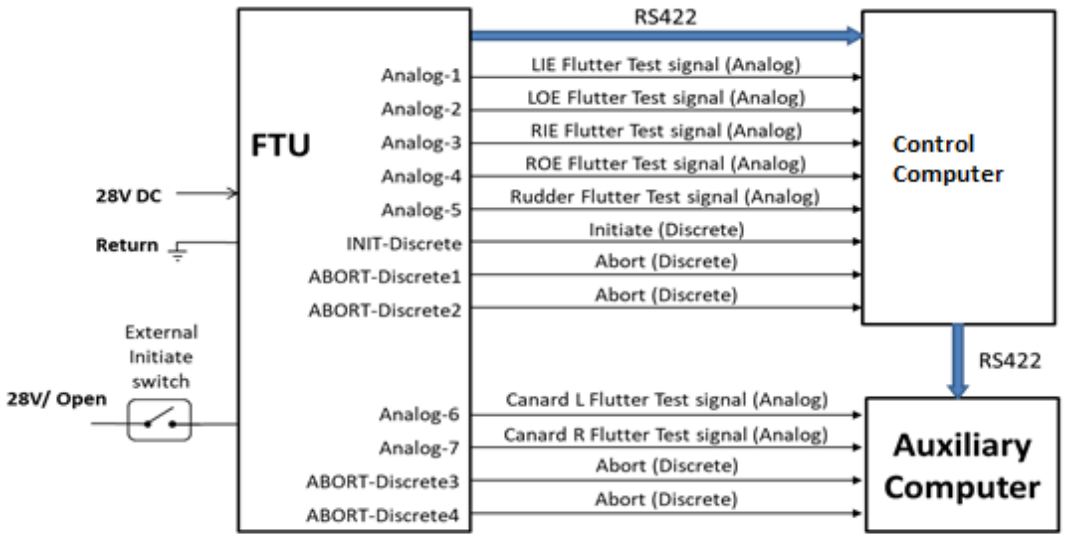


Figure 1

Setting up of the function generator of FTU, for any required Test shall be made User-friendly by control switches and displays utilizing the pre-programmed external EPROM / Flash (Containing the set-up data for a max of 1000 pre-determined tests).

The synthetic signals generated shall be either of the two types:

1. Digital test signal shall be injected into Control Computer, through RS-422 SDL for any one of the axes (i.e. Longitudinal / Lateral / Directional) at a time and for the purpose of PID test and associated testing of the control Law. The PID test signal for only one axis shall be provided at a time (i.e. PITCH or ROLL or YAW).

The digital test signal through RS422 shall be transmitted from FTU to control computer. The required test signal information to Auxiliary Computer shall be transmitted from control computer through RS422 link.

2. Analog test signals shall be injected to control computer for summation with the appropriate actuator commands for the purpose of flutter tests, for a combination of actuators.

3. TOP LEVEL TECHNICAL SPECIFICATIONS

The top level technical specifications of FTU are as given in the following table:

Table 2: TOP LEVEL TECHNICAL SPECIFICATIONS

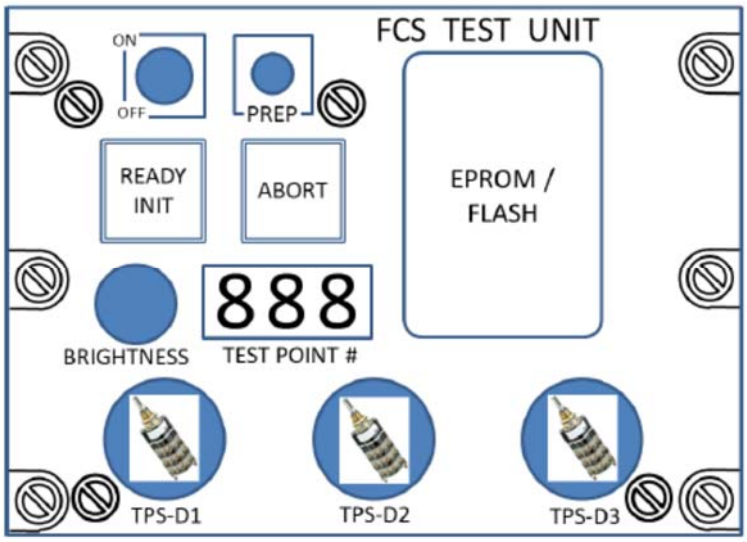
Sl.No	Parameter	Requirement
1	Analog outputs	8 Nos. differential
2	Discrete outputs	5 Nos. (Open / Ground)
3	Discrete Input	External INIT SW (28V / Open)
4	Serial Data Link Output	1 RS-422 SDL (RS-422 SDL, 57600 bps Asynchronous and Simplex).
5	Control switches and displays	Switches: Power ON / OFF, PREP, INIT, ABORT, Three Rotary Switches, Brightness Control Displays: Ready Lamp, ABORT lamp and Three Digit Display
6	No. of Signal Generators	1
7	Frequency	0.1 to 100 Hz
8	No of test points	1000
9	Types of synthesized signals	Square Pulse, Square Doublet, Half Sine Pulse, Full Sine Doublet, 3-2-1-1 Pulse train, Linear Sine Sweep, Logarithmic Sine Sweep and Random Signals
10	Input Power supply	28 Volts (Power <15W)
11	Operating Temperature range	-40° C to +73° C

Sl.No	Parameter	Requirement
12	Storage Temperature range	-55° C to +73° C
13	Weight	< 3.25 Kg
14	Dimension	100 X 146 X 140 mm
15	MTBF	>3000 Hrs
16	Chassis material	Aluminium alloy of BS L168 or equivalent material.
17	Chassis finish	External surfaces to be black anodized as per MIL-A-8625F type-III, Class 2 and internal surfaces to be finished with Al-chrome treatment as per MIL 5541F

Note: FTU hardware and Software design & development process shall follow the existing industrial standards for Aircraft applications.

4. FUNCTIONAL CHARACTERSITICS

4.1. Controls & Displays



The control switches and Displays on FTU front panel is shown in Figure 2.

4.1.1. Power ON / OFF Switch

Power ON / OFF Switch shall enable the User to power ON the FTU with the 28 V DC aircraft power. This switch shall be two positions toggle switch with maintained contact and lever lock in ON direction.

4.1.2. PREP Switch

This switch shall enable the User to enter into Preparation Phase. This switch shall be a spring loaded, momentary contact, push button type. This switch position is monitored by FTU only.

4.1.3. READY Lamp / INIT Switch

INIT Switch shall be used to initiate the test point. The INIT switch shall be a spring loaded, momentary contact, push button switch cum indicator type. The INIT switch position shall be monitored by FTU and INIT discrete signal corresponding to Switch Position to be sent to DFCC through discrete channel. The READY Lamp shall be a GREEN lamp and indicate the status of FTU to the User.

In addition to the above, the FTU test point shall be initiated from an external switch identified on the User Control Grip. To meet this, a 28V/Open discrete input interface shall be provided in FTU. Upon receiving this input, the FTU shall perform the function same as that of INIT switch.

4.1.4. ABORT Lamp / Switch

ABORT Switch shall be used to abort the test point. The ABORT switch shall be a spring loaded, momentary contact, push button switch cum indicator type. The ABORT switch position shall be monitored by FTU and ABORT discrete signals corresponds to Switch Position to be sent to DFCC and Auxiliary Computer through discrete channels. The ABORT lamp shall be a RED Lamp and indicate to the User that the test has been manually aborted.

4.1.5. Three Digit Display

Three digit display shall be used to the test point number / POST status / POST results. This display shall be in green colour and sunlight readable. It displays the selected test point number in the range of '000' to '999'. Display type should be Glass / Ceramic Numeric and Hexadecimal Displays.

4.1.6. Rotary Switches

Three Rotary Switches (TPS-D1, TPS-D2 and TPS-D3) shall be available on FTU to select the test point on Three Digit Display. These switches shall be rotary switches with stable ten positions (0 to 9 positions). The position of these switches shall be monitored by FTU. The selected position of these three switches shall be displayed on the 3 digit display.

4.1.7. Brightness Control

Rotary knob shall be provided in the front panel of FTU to vary the brightness of Three Digit Display, READY and ABORT Lamps.

4.1.8. EPROM / FLASH Socket

EPROM / Flash Socket shall be provided to access EPROM / Flash module.

5. INPUT and OUTPUT Interfaces

The FTU shall have the following external input and output Interfaces:

5.1. Inputs

a. 28V Power Supply

b. External INIT switch (28 V / Open discrete)

5.2. Outputs

a. 8 Analog Channels to transmit Flutter test Signals

b. 1 RS-422 Serial Data Link (SDL) to transmit PREPARE message, PID test signal message and Test Completion message (RS-422 SDL, 57600 bps Asynchronous and Simplex).

c. 1 Discrete Channel to transmit INIT Switch status.

d. 4 Discrete channels to transmit ABORT Switch status

e. Additional spare RS422 channel (Tx & Rx) to be provided.

6. FUNCTIONAL MODES

The FTU shall operate in any one of the following phases:

a) Power on Self-Test Phase

b) Test point Selection Phase

c) Preparation Phase

d) Test in progress Phase

e) Test Completion Phase

f) Abort Phase

The state transition diagram of FTU is showed in Figure 4.

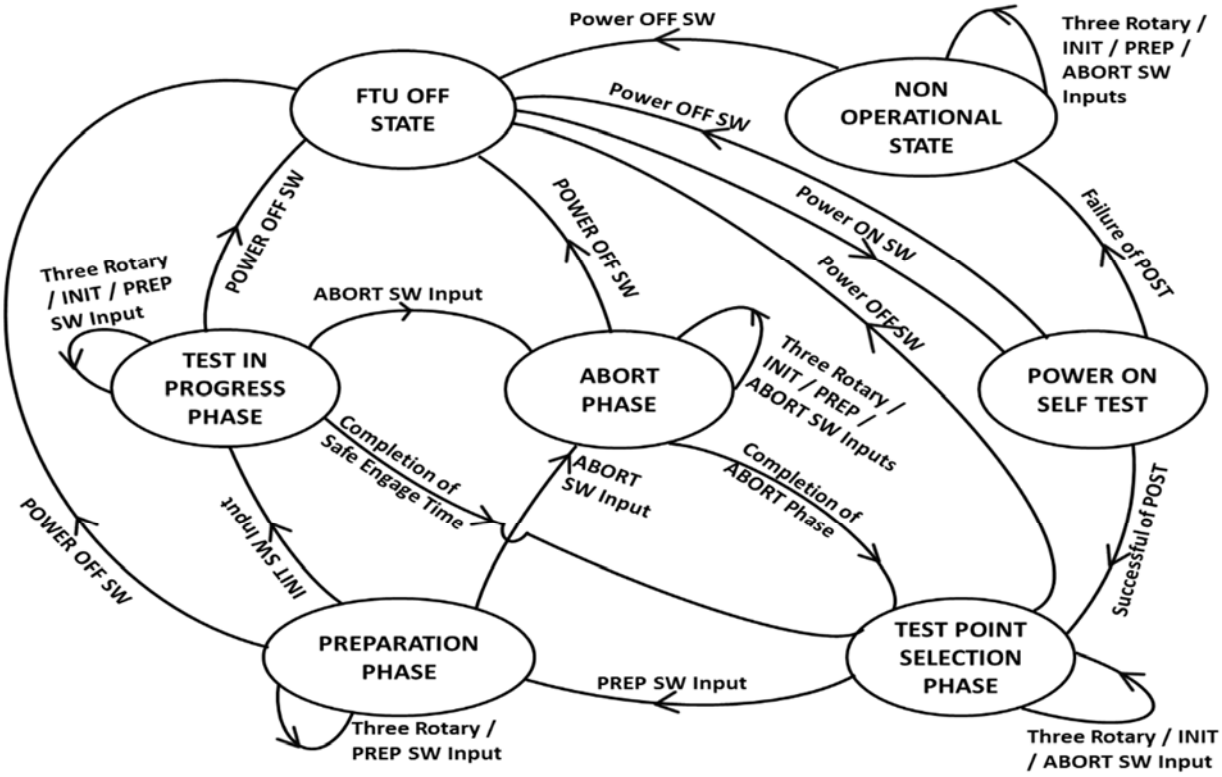


Figure 4: State Transition Diagram of FCS Test Unit

a) POWER ON SELF TEST PHASE (POST)

The FTU shall enter into this phase immediately after power ON. In this phase it checks the health of the unit by the following actions:

- Display numeral '888' on the three digit display, implying the serviceability of the display elements.
- Display the identification of the resident software for about a second on the three digit display (C00-CFF).
- Display the identification of the external EPROM / Flash for about a second on the three digit display (E00-EFF).
- Displays '888' on the three digit display during other hardware self – test of POST.
- Perform self-test of the electronic hardware. I.e. micro controller's on-chip RAM & internal EPROM / Flash, external EPROM / Flash (Checksum), Discrete channels hardware, ABORT & READY Lamps, RS-422 SDL hardware and Analog channels hardware.

- Initialize all the analog channels to 0 volts, discrete channels to High state and RS-422 SDL to High state, immediately after self-test of the respective channel.
- Display the numeral '000' to '999' on the three-digit display as per the selected position of the three rotary switches and keep the READY lamp and ABORT lamp OFF, if the POST is successful and change over to Test Point Selection Phase.
- Display the numeral 'FFF' on the three-digit display, if the POST fails and remain in non-operational state.
- The POST shall be completed in less than 10 seconds.

b) TEST POINT SELECTION PHASE

The FTU shall enter into this phase immediately after successful completion of POST or after execution of Abort phase or Test completion phase. In this phase, it shall;

- Display the selected test point on the three digit display upon operating the three rotary switches.
- Transmit the Test Point Number as per the message structure continuously over the RS-422 SDL as per Table - 3.
- Keep the READY lamp and ABORT lamp OFF.
- Detect the INIT switch operation and keep the READY lamp ON & transmit the corresponding switch status on the respective discrete channels (i.e. setup the discrete channel LOW) till the switch is operated.
- Detect the ABORT switch operation and keep the ABORT lamp ON & transmit the corresponding switch status on the respective discrete channels (i.e. setup the discrete channel LOW) till the switch is operated
- Change over to preparation phase on momentary operation of PREP switch.

Table – 3: TEST POINT NUMBER - MESSAGE STRUCTURE

Byte	Description	Hexadecimal value
0	Start Of Header Character (SOH)	01
1	Message identifier	05
2	Number of Data Bytes	02
3	Test point Number - LS Byte	Variable
4	Test point Number - MS Byte	Variable
5	Checksum-LS Byte	Variable
6	Checksum-MS Byte	Variable
7	End Of Text Character (EOT)	04

c) PREPARATION PHASE

The FTU shall enter into this phase after the momentary operation of PREP switch in Test Point Selection phase. On entering this phase it shall;

- Not respond to the change in position of 3 rotary test point selection switches. FTU shall continue to display the test point selected prior to PREP switch press.

  Note: If for any reason, the required test point is to be changed, the preparation phase has to be first aborted by operating the ABORT switch. After completion of Abort Phase, FTU shall enter into Test Point Selection Phase.
- Read the appropriate test set up data corresponding to the test point from the external EPROM / Flash.
- Transmit the PREPARE message as per the message structure in Table - 4 over the RS-422 SDL.
- Illuminate READY lamp steady after the transmission of PREPARE message.
- Remain in this phase until a test is initiated (by momentary operation of INIT switch) or Aborted (by momentary operation of ABORT switch).

- Change over to Test In Progress phase upon momentary operation of INIT switch (or) Change over to Abort phase upon momentary operation of ABORT switch.

Table -4: PREPARE MESSAGE STRUCTURE

Byte	Description	Hexadecimal value
0	Start Of Header Character(SOH)	01
1	Message identifier	0A
2	Number of Data Bytes	13
3	Test point Number - LS Byte	Variable
4	Test point Number - MS Byte	Variable
5	Signal Injection Point	Variable
6	Slat-Least Significant(LS)Byte	Variable
7	Slat-Most Significant(MS)Byte	Variable
8	Response parameter 1 identifier	Variable
9	Response parameter 1 Limit-LS Byte	Variable
10	Response parameter 1 Limit-MS Byte	Variable
11	Response parameter 2 identifier	Variable
12	Response parameter 2 Limit -LS Byte	Variable
13	Response parameter 2 Limit-MS Byte	Variable
14	Response parameter 3 identifier	Variable
15	Response parameter 3 Limit -LS Byte	Variable
16	Response parameter 3 Limit -MS Byte	Variable
17	Response parameter 4 identifier	Variable
18	Response parameter 4 Limit -LS Byte	Variable
19	Response parameter 4 Limit -MS Byte	Variable
20	Safe Engage Time –LS Byte	Variable
21	Safe Engage Time –MS Byte	Variable
22	Test point signal type, Amplitude, Test Initiation delay, etc… to be transmitted to DFCC shall be finalized in due course.	
23		
24		
25		
26		
27		
28		
29	Checksum-LS Byte	Variable
30	Checksum-MS Byte	Variable
31	End Of Text Character(EOT)	04

d) TEST IN PROGRESS PHASE

The FTU shall enter into this phase after the momentary operation of the INIT switch in Preparation Phase. On entering this phase it shall;

- Set up the INIT discrete channel LOW for duration of 400 msec.
- Provide an Initiation delay (variable) as per Test Point definition in EPROM / Flash before transmitting the synthesized signal (s) and flash the ready lamp at a rate of 10 Hz. Change over to ABORT phase upon momentary operation of ABORT switch.
- Not respond to the change in position of 3 rotary test point selection switches. FTU shall continue to display the test point selected.
- After the initiation delay, transmit the synthesized signal (s) on the appropriate data channel (i.e. PID test signal through RS-422 SDL as per Table-5 / Flutter test signal through Analog channels) for a specified duration as per the test point definition and also Flash the READY lamp at a rate of 1 Hz (to indicate the transmission of the synthetic signals).
- After successful completion of test, transmit the Test complete message as in Table – 6 and change over to Test point Selection phase.
- Change over to Abort phase upon momentary operation of ABORT switch.

Table -5: PID TEST MESSAGE

Byte	Description	Hexadecimal value
0	SOH	01
1	Message Identifier	03
2	Number of data bytes	02
3	PID TEST signal-LS Byte	variable
4	PID Test Signal-MS Byte	variable
5	Checksum-LS Byte	variable
6	Checksum-MS Byte	variable
7	EOT	04

Table - 6: TEST COMPLETION MESSAGE

Byte	Description	Hexadecimal value
0	SOH	01
1	Message Identifier	07
2	Number of data bytes	00
3	Checksum-LS Byte	08
4	Checksum-MS Byte	00
5	EOT	04

e) ABORT PHASE

The FTU enters this phase by momentary operation of ABORT switch in Preparation phase or Test in Progress phase. On entering this phase it shall;

1. On momentary operation of the ABORT switch during Preparation phase or Test in Progress phase during Initiation delay;
   i. Turn OFF the READY lamp
   ii. Setup the ABORT discrete channel LOW for a duration of 300 msec and keep the ABORT lamp 'ON' till the ABORT switch is pressed.
   iii. Change over to Test point Selection phase on completion of the above tasks.
2. On momentary press of the ABORT switch during the signal synthesis;
   i. Turn OFF the READY lamp
   ii. Terminate the generation of the synthetic signal at the first zero-crossing point

Setup the ABORT discrete channel LOW for a duration of 300 msec and keep the ABORT lamp 'ON' till the ABORT switch is operated Change over to Test point Selection phase on completion of the above tasks.

7. TYPES OF SYNTHESIZED SIGNALS

The FTU shall be capable of synthesizing signals of pre-defined characteristics whose specification is as in Table - 7. The synthetic signals at any given time shall be sent to Control Computer through either the RS-422 or ANALOG channel (s), as per the test requirements.

The PID test signal shall be sent on asynchronous RS-422 SDL, operating at 57600bps. The Flutter test signal shall be sent to Control Computer through the analog channels. The analog signals for one or more actuators excitation shall be possible. The actuators shall be excited in any one of the following combinations:

- Inboard and Outboard Elevon shall be excited as pairs with symmetric / anti-symmetric signals.
- Rudder shall be excited independently.
- Canards shall be excited with symmetric / anti-symmetric signal.
- Stabilators shall be excited with symmetric / anti-symmetric signals.
- Ailerons shall be excited with symmetric / anti-symmetric signals.
- Rudder shall be excited with symmetric / anti-symmetric signals.
- Trailing Edge Flaps shall be excited with symmetric / anti-symmetric signals.

- **TABLE - 7: WAVEFORM PARAMERTER SPECIFICATION**

#	Parameter	Value	Resolution	Accuracy
1	Max. amplitude – Pitch Stick Top Input (Digital)	± 12 mm	$5.862 * 10^{-3}$	± 0.6 mm
2	Max. amplitude – Roll Stick Top Input (Digital)	± 12 mm	$5.862 * 10^{-3}$	± 0.6 mm
3	Max. amplitude – Rudder pedal physical input (Digital)	± 30 mm	$1.466 * 10^{-2}$	± 1.5 mm
4	Max. amplitude of Analog Excitation	0.46 Volts (for non-impulse signals)	0.001 Volts	± 0.1 Volts
		0.92 Volts (for impulse signals)	0.001 Volts	± 0.1 Volts
5	Range of Slats Input	0.0 to 1.0	$6.103 * 10^{-4}$	NA
6	Digital Excitation Data Resolution (RS-422)	12 bit	NA	NA
7	Digital Data Rate	12.5 msec	NA	± 150µsec
8	Analog Excitation Data Resolution	12 bit	NA	NA
10	Digital Waveforms period - Range	0.1 to 20 sec	0.0125 sec	± 0.05 sec
11	Analog Waveforms period - Range	0.0125 to 10 sec	0.00125 sec	± 0.08 sec

#	Parameter	Value	Resolution	Accuracy
12	Ramp step of Digital Square Edges	45 mm/sec	NA	± 1mm/ sec
13	Ramp step of Analog Square Edges	27.75 Volts/sec	NA	± 1 Volt/ sec
14	Injection start Delay from INITIATE command	1sec	NA	± 0.05 sec
15	Sweep duration of linear/log. Sine sweep signals	0.1 to 54 sec	NA	± 1 sec
16	Flutter waveform step period*	0.2 to 2 sec	NA	± 0.08 sec
17	Dwell time*	0.1 to 5 sec	NA	± 0.01 sec
18	Time Between Repeats	0 to 53.9875 sec, for all waveforms and linear/ log. Sine sweep with amplitude coeff1=0	NA	± 0.01 sec for analog signals ±0.025 sec for digital signal
		0.025 to 53.9875 sec, for analog signals with amplitude coeff1≠0		

- *Applicable to flutter test – linear sine sweep signal only.

The test signals shall start and stop at the nearest zero crossing point. Table - 8 lists the various excitation combinations with their signal transmission mode.

TABLE – 8: SYNTHESIZED SIGNAL INJECTION

#	Signal injection Point(s)	Transmission Mode
1	Pitch Stick FTU Input (FXP01)	Digital*
2	Roll Stick FTU Input (FXR01)	Digital*
3	Rudder Pedal FTU Input (FXY01)	Digital*
4	Inboard Elevon Symmetric (IE SYM)	Analog**
5	Outboard Elevon Symmetric (OE SYM)	Analog**
6	Inboard Elevon Asymmetric (IE ASYM)	Analog**
7	Outboard Elevon Asymmetric (OE ASYM)	Analog**
8	Inboard & Outboard Elevon Symmetric(IOE SYM)	Analog**
9	Inboard & Outboard Elevon Asymmetric(IOE ASYM)	Analog**
10	Rudder(RUD)	Analog**

*Digital implies that the PID test signal is sent on the RS-422 SDL.

** Analog implies that the flutter test signal is sent on the analog channels.

7.1. Characteristics of signals

The FTU shall be capable of generating the types of waveforms listed below. The waveforms along with its characteristics to be synthesized either as a single

or multiples of the waveform. The following types of signals shall be generated by the FTU:

a) Square pulse
b) Square doublet
c) Half-sine Pulse
d) Full-sine Doublet
e) 3-2-1-1 pulse Train
f) Linear Sine sweep
g) Logarithmic Sine sweep
h) Random

a) Square pulse

This is a square wave commencing from zero input value, building up to the amplitude specified, and returning to zero after the elapse of pulse-width duration. Figure 5 shows the waveform. The waveform shall be a mirror image of the one shown in Figure 5, if the amplitude is specified as a negative value.

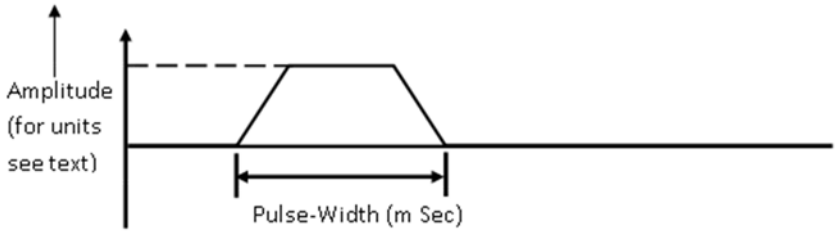


Figure 5: Square Pulse

Parameters: Amplitude in units of mm for PID test signals or volts for flutter test signals.

b) Square Doublet

This is a square wave doublet commencing from zero input value, building up to the +ve amplitude specified for the pulse-width specified, changing to –ve amplitude specified, and returning to zero after the elapse of pulse-width duration. Figure 6 shows the waveform. The waveform shall be a mirror image of the one shown in figure 6, if the amplitude is specified as a negative value.

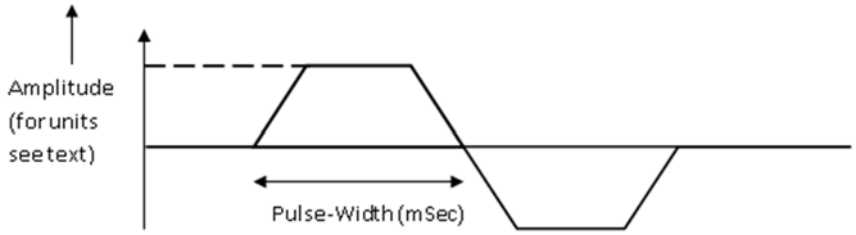


Figure 6: Square Doublet

Parameters: Amplitude in units of mm for PID test signals or volts for flutter test signals.

c) Half-sine Pulse

This is a sine wave commencing from zero input value, building up to the amplitude specified as per sine law and returning to zero for after the frequency specified. Figure 7 shows the waveform. The waveform shall be a mirror image of the one shown in figure 7, if the amplitude is specified as a negative value.

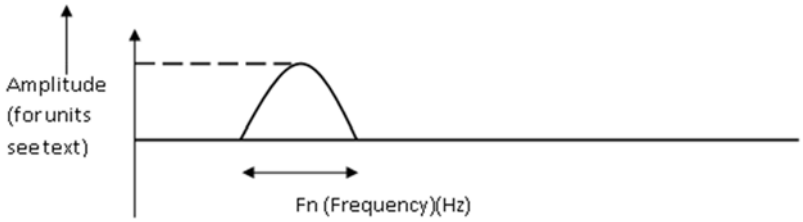


Figure 7: Half-sine Pulse

Parameters: Amplitude in units of mm for PID test signals or volts for flutter test signals.

d) Full-sine Doublet

This is a sine wave commencing from zero input value, building up to the amplitude specified as per sine law and returning to zero for after the frequency specified. Figure 8 shows the waveform. The waveform shall be a mirror image of the one shown in figure 8, if the amplitude is specified as a negative value.

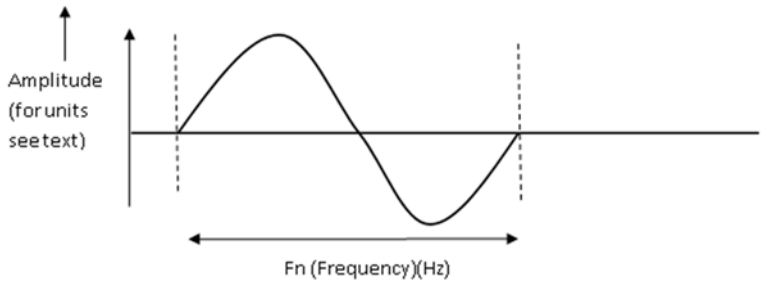


Figure 8: Full-sine Doublet

Parameters: Amplitude in units of mm for PID test signals or volts for flutter test signals.

e) 3-2-1-1 Pulse Train

This is a sequence of four pulses of equal amplitude, each pulse alternating in sign vis-à-vis the previous pulse and the first pulse in the sign of amplitude specified. Figure 9 shows the waveform. The waveform shall be a mirror image of the one shown in figure 9, if the amplitude is specified as a negative value.

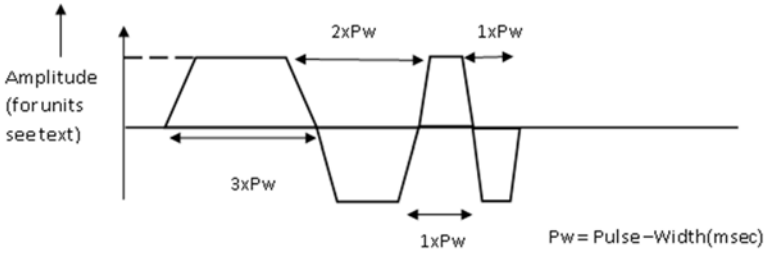


Figure 9: 3-2-1-1 Pulse Train

Parameters: Amplitude in units of mm for PID test signals or volts for flutter test signals.

f) Linear Sine Sweep

This is a sinusoidal signal whose frequency and amplitude varies according to the sweep law defined by:

i. $\omega = \omega_0 + \alpha t$ for digital waveform

Where ω = instantaneous frequency (rad/sec)

ω_0 = initial frequency (rad/sec)

$\alpha = (\omega_f - \omega_0)/\tau$, is the sweep rate (rad/sec/sec)

τ = sweep duration (sec)

ωf = final frequency (rad/sec)

ii. f = f0 + Δf * tk for analog waveform

Where f = instantaneous frequency (Hz)

f0 = initial frequency (Hz)

Δf = frequency step (Hz)

tk = int (t /td) = 0,1,2,.....where td is dwell time (sec)

iii. A(t) = C0+ C1*t

Where A(t) = instantaneous amplitude

C0 & C1 are constants

Parameters:

C0 in units of mm for PID test signals or volts for flutter test signals.

C1 in units of mm/sec for PID test signals or volts/sec for flutter test signals.

Dwell time (td) in units of msec, defines the dwell time of the signal frequency, applicable to flutter test signals.

Frequency (start)(ω0) in units of cycles per sec (Hz).

Frequency (final)(ωf) in units of cycles per sec (Hz).

Frequency step (Δf) in units of cycles per sec (Hz), defines the value of frequency to be stepped up / down, applicable to flutter test signals.

Sweep Duration (τ) in units of msec, defines the total duration of the linear sine sweep signal.

g) Logarithmic Sine Sweep

This is a sinusoidal signal whose frequency and amplitude varies according to the sweep law defined by:

i. ω = ω0 eβt

ii. A(t) = C0 +C1 * t

Where ω is the instantaneous frequency (rad /sec),

ω0 is the initial frequency (rad/sec),

τ is the sweep duration (sec),

β is the sweep rate (rad/sec/sec) = (1/ τ) * ln(ωf / ω0),

ωf is the final frequency (rad/sec).

Parameters: C0 in units of mm for PID test signals or volts for flutter test signals.

C1 in units of mm/sec for PID test signals or volts/sec for flutter test signals.
Frequency (start) (ω0) in units of cycles per sec (Hz).
Frequency (final) (ωf) in units of cycles per sec (Hz).
Sweep Duration (τ) in units of msec.

h) Random Signal

This signal is analog derived from a random number generator using a 16-bit shift Register with Linear Feedback. The Output from the random number generator is fed to a Low pass Butter worth filter, whose output with a peak amplitude of A volts, would be a multilevel analog random signal of 80 Hz bandwidth.

Parameters: Amplitude in units of volts, applicable to a flutter test signals.
Signal Duration in units of msec, applicable to flutter test signals.

i) Multiples of the waveforms

These parameters specify, if any of the test waveform is to be repeated for a number of times. Number of repeats and time between repeats are self-explanatory.

Invert flag, if set to (TRUE) inverts/swaps certain parameters before every repeat.

The following inverts/swaps are carried out for the following waveform types:

(a) Square Pulse – Change Sign of Amplitude.
(b) Square Doublet - Change Sign of Amplitude.
(c) Half- Sine Pulse- Change Sign of Amplitude.
(d) Full- Sign Doublet - Change Sign of Amplitude.
(e) 3-2 1-1 Pulse Train - Change Sign of Amplitude.
(f) Linear Sine Sweep – Swap frequency (start) and frequency (final).
(g) Logarithmic Sine Sweep – Swap frequency (start) and frequency (final).
(h) Not Applicable to random waveforms.

Parameters: Invert Flag in units of Logical Variable (True or False)

Number of Repeats in units of number (Zero for single test)

Time Between repeats in units of msec

Typical Test Case definition:

FTU Test No., Path and Amplitude Levels for Flutter Test Inputs using FTU (Linear Sine Sweep - LSS Analog)

FTU Test No	Signal Type	Signal Injection Point	Amplitude (%of stroke)	C0 (mv)	C1	Start Freq (Hz)	End Freq (Hz)	Freq. Step (Hz)	Dwell Duration (Secs)	Safe engage Time (Secs)
001	LSS	Elevon Symmetric	0.5	65.5	0	5	20	0.5	1	38

FTU Test No., Path and Details of Input for PID Test Points

FTU Test No	Type Of Input	Slat Input	Signal Type	Signal Injection Point	Amplitude	Pulse Width sec	No. of Repeats	Time Between Repeats Sec	Invert Flag	Safe engage Time (Secs)
079	Elevon Pulse Train	0.5	3-2-1-1 Pulse Train	Pitch FXP01	10mm	1	0	0	False	22

Test Case definition for all the 1000 cases shall be provided after finalization.

8. DESIGN OF FCS TEST UNIT

The design of FTU is based on the following aspects:

8.1. Hardware

a. The FTU shall be designed as a real time-embedded system. The hardware shall be built around the microcontroller.

b. The synthesis of the waveforms shall be by an algorithm executed on the microcontroller and Conversion to appropriate test signal shall be by the Hardware.

c. The Hardware of FTU should be designed with modular concept and to be housed inside the mechanical enclosure.

d. Provision shall be made for plugging the EPROM / Flash module through an opening on the front panel.

e. FTU should be designed with a suitable EPROM / Flash to store test set-up data for a max of 1000 pre-determined tests.

f. Mil qualified electronics components shall be used in the design, to greater extent possible. In case of non-availability of Mil-grade components, Automotive / industrial grade components can be used. Components less than the temp range -40° C to +85° C are not allowed in design.

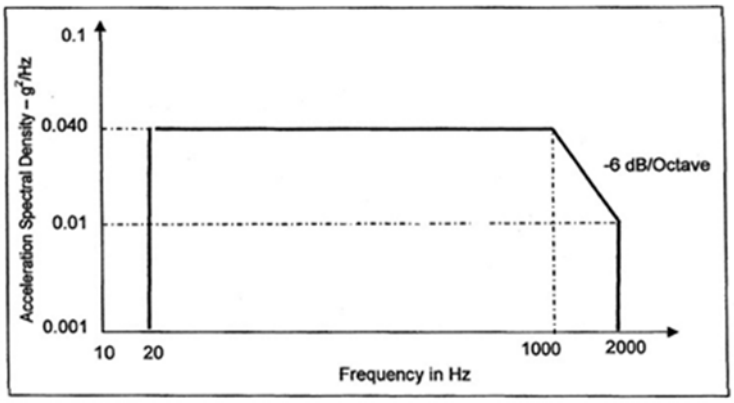
g. The design shall be able to comply the following SOFT test:

i. MIL-STD-704D Test

ii. EMI/EMC (CE101, CE102 , RE101 , RE102)

Type	Test	Description	Frequency Range
Conducted Emission	CE101	Power Leads	30 Hz to 10 KHz
	CE102	Power Leads	10 KHz to 10 MHz
Radiated Emission	RE101	Magnetic Field	30 Hz to 100 KHz
	RE102	Electric Field	

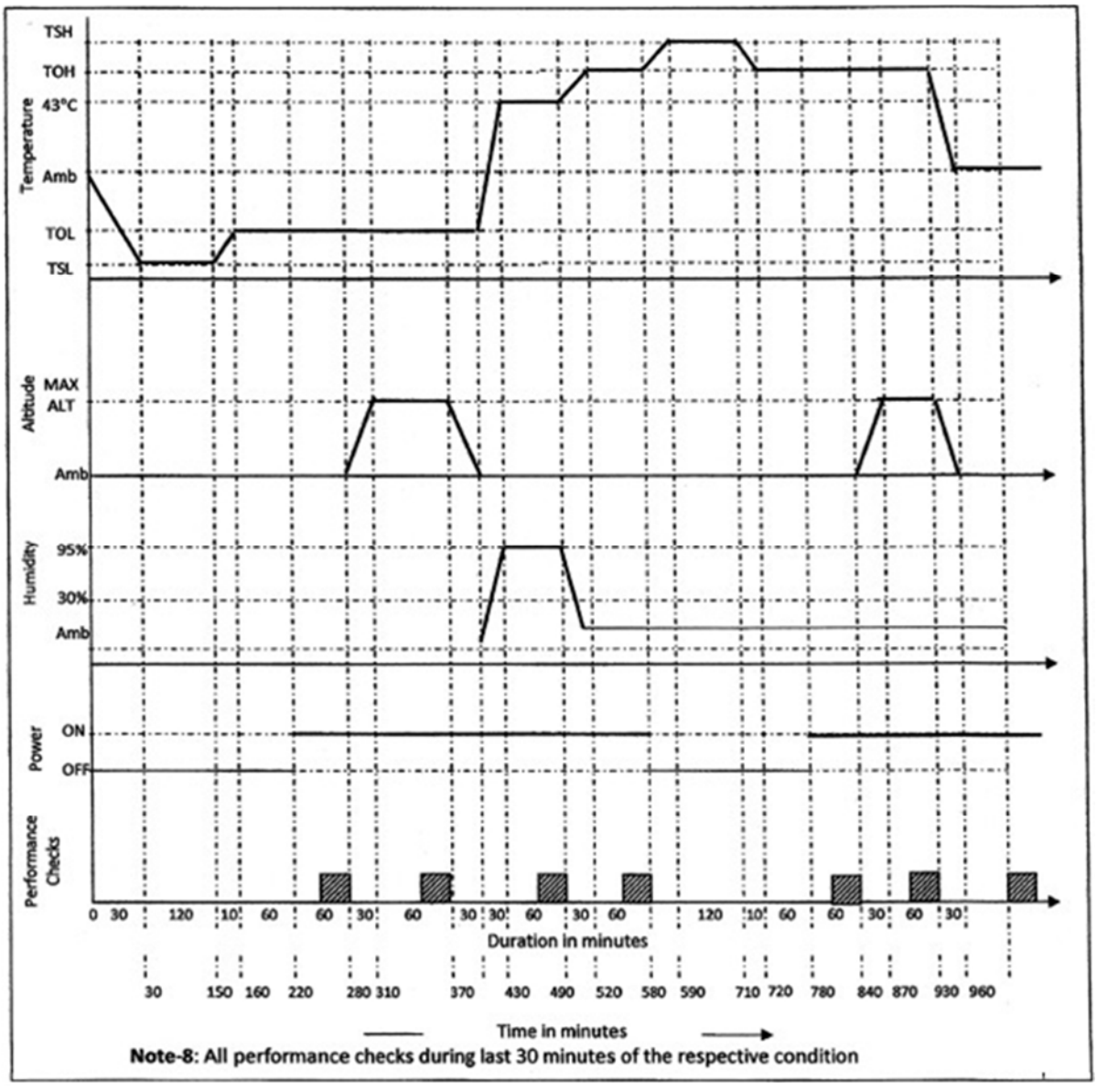
iii. Random Vibration (b.0.04 g2/Hz from 20 Hz to 1000 Hz & falling off at 6 dB/octave from 1000 Hz to 2000 Hz, 15mins / axis in all three axis)



iv. Combined Altitude Temperature Humidity (CATH) Test

(Amb = +25C, TOH = +73C, TOL = -40C, TSH = +73C, TSL = -55C,

Amb. Alt= 3000 feet, Max. Alt=66000 feet.)



Note-8: All performance checks during last 30 minutes of the respective condition

v. Acceleration (Structural) : The FTU shall be subjected to acceleration in 6 directions at 'g' level indicated below in OFF condition for duration of 1 minute / direction.

Direction	'g' level
Fore	3.0
Aft	9.0
Up	13.5
Down	4.5
Lateral Left	6.0
Lateral Right	6.0
Note: Directions are w.r.t. aircraft axis	

vi. Shock test: 20g saw tooth/ 15g half sine pulse of 11 milliseconds duration in all six directions in ON condition.

vii. Crash Safety Test : 40g saw tooth / 30g half sine pulse of 11 milliseconds duration in all six directions in OFF condition

h. Reliability calculations as per the part stress method.

8.2. Printed Circuit Boards

These shall confirm to IPC 2221B & IPC 6012 class 3. The PCB substrate shall be of glass epoxy and be coated with conformal coating to protect the circuits from external environments.

a) PCB should be made with FR4 material.

b) PCB should comply with DRS (design rule check) & LVS (Lay out verses schematic) verification

c) The screening test of populated PCBs shall be conducted as per CEMILAC directive No. 81/2003 released vide letter No. CEMILAC/5390/1, dated 10 January 2004 based on the applicability

d) MIL-STD-454 shall be used as a guideline for printed wiring.

e) MIL-I-46058 shall be used as a guideline for conformal coating

8.3. Software

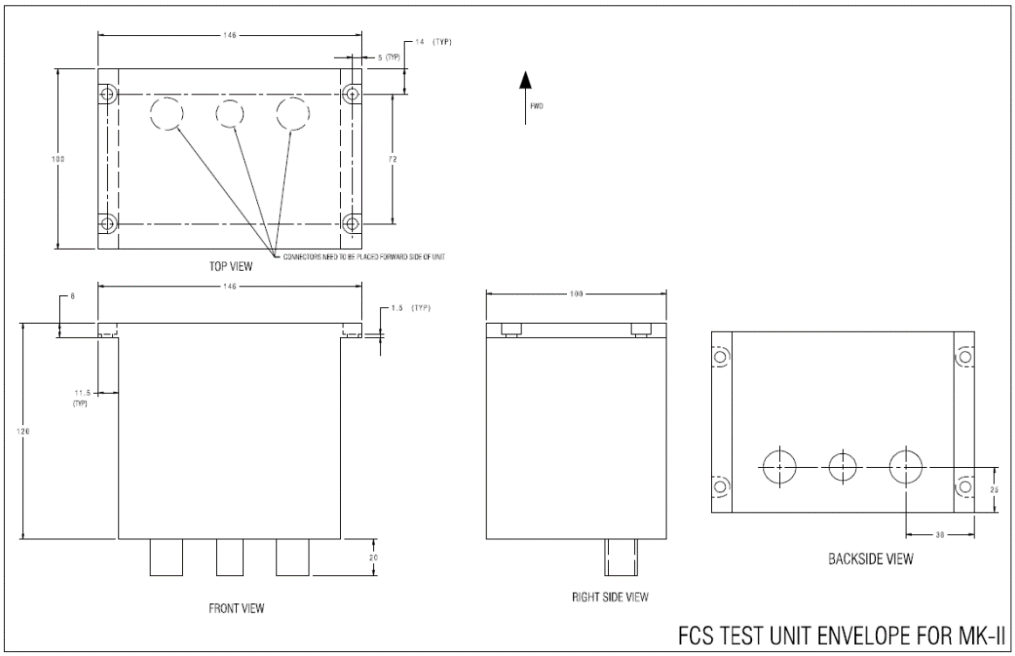
FTU Software design & development process should follow DO-178C (Level C).

The Software performs the following:

a. Power on Self-Test
b. Monitor the switch operation on the panel and schedule / invoke the software modules.
c. Update the test point.
d. Read the Test Data from EPROM / Flash.
e. Communicate the preparation messages.
f. Generate Test Signal as per the selected test requirement.
g. Communicate these signal either through RS-422 channel (for PID test) or through Analog Channel (for flutter test).

8.4. Physical

The external dimension of FTU shall not exceed 100 x 146 x 140 mm (including connector and excluding Switch projections) and its weight shall not exceed 3.25 Kg. Switch projection shall not exceed 30 mm. The FTU shall be installed in cockpit using DZUs fasteners. The dimension of the FTU is as shown in Figure 10.



8.5. Mechanical Chassis

The mechanical chassis shall confirm to the external dimensions. The switches, indicators and EPROM socket are to be accommodated on the front panel. The circular connectors may be positioned in the rear panel, with sufficient clearance between the connectors. The mechanical parts of the chassis shall be made out of aluminum alloy BS L168 or equivalent material. External surfaces to be black anodized as per MIL-A-8625F type-III, Class 2 and internal surfaces to be finished with Al-chrome treatment as per MIL 5541F.

The mechanical chassis shall comprise of front panel, left & right side covers, top & bottom covers and rear covers which shall be fitted / assembled using screws and thread inserts. As a part of structural stability, stress analysis shall be carried out for mechanical chassis. The unit shall be fitted on the platform using 6 DZUS fasteners.

8.6. Power Supply

1) The FTU shall operate satisfactorily when supplied with normal electric power (28V DC) confirming to MIL STD 704D requirement.
2) The FTU Design shall comply to following test:

As per MIL-STD- 704D

Sl. No.	Test	Description
1	LDC101	Load Measurements
2	LDC102	Steady State Limits for Voltage
3	LDC103	Voltage Distortion Spectrum
4	LDC104	Total Ripple
5	LDC105	Normal Voltage Transients
6	LDC201	Power Interrupt
7	LDC301	Abnormal Steady State Limits for Voltage
8	LDC302	Abnormal Voltage Transients

9	LDC401	Emergency Limits for Voltage
10	LDC602	Polarity Reversal

3) The FTU Design shall comply to conducted and radiated emission tests as per MIL-STD-461E:

Type	Test	Description	Frequency Range
Conducted Emission	CE101	Power Leads	30 Hz to 10 KHz
	CE102	Power Leads	10 KHz to 10 MHz
Radiated Emission	RE101	Magnetic Field	30 Hz to 100 KHz
	RE102	Electric Field	10 KHz to 18 GHz

8.7. Electrical Interface

The FTU shall be connected to Control Computer through a signal connector for;

- transmitting Flutter signal on various analog channels
- transmitting Parameter Identification signals on RS422 SDL.
- transmitting discrete signals on discrete channels.

The FTU shall be connected to aircraft DC Power supply through a power connector for receiving the 28V DC.

The details of FTU connectors with the signal details are shown in Table – 9 and Table - 10.

TABLE - 9: DC POWER CONNECTOR (C1) SIGNAL DETAILS

S/N	Signal type	Signal Name
1	DC Power	+28V,DC
2	DC Power	Ret, DC
3	Ground	SGRP Chassis)
4	Spare	-
5		
6		

TABLE – 10: CONNECTOR (C2) SIGNAL DETAILS

#	Signal Type	Signal Name	
		LCA AF Mk2	AMCA
1	Analog1	LIE-Flutter-H	Stabilator Left-Flutter-H
2	Ground	LIE-Flutter-L	Stabilator Left-Flutter-L
3	Analog2	LOE-Flutter-H	Stabilator Right-Flutter-H
4	Ground	LOE-Flutter-L	Stabilator Right-Flutter-L
5	Analog3	RIE-Flutter-H	Aileron Left-Flutter-H
6	Ground	RIE-Flutter-L	Aileron Left-Flutter-L
7	Analog4	ROE-Flutter-H	Aileron Right-Flutter-H
8	Ground	ROE-Flutter-L	Aileron Right-Flutter-L
9	Analog5	Rudder Flutter -H	Rudder Left Flutter -H
10	Ground	Rudder Flutter-L	Rudder Left Flutter-L
11	Analog6	Canard Left Flutter -H	Rudder Right Flutter -H
12	Ground	Canard Left Flutter -L	Rudder Right Flutter-L
13	Analog7	Canard Right Flutter -H	TEF Left Flutter -H
14	Ground	Canard Right Flutter -L	TEF Left Flutter -L
15	Analog8	-	TEF Right Flutter -H
16	Ground	-	TEF Right Flutter -L
17	Digital1	FTU-SDL-H	FTU-SDL-H
18	Digital1	FTU-SDL-L	FTU-SDL-L
19	Digital2	ESDL-H * (RS-422)	ESDL-H * (RS-422)
20	Digital2	ESDL-L * (RS-422)	ESDL-L * (RS-422)
21	Discrete1	INIT Switch Discrete	INIT Switch Discrete
22	Ground	Reference	Reference
23	Discrete2	INIT Switch Discrete (PG1 Switch Input)	INIT Switch Discrete (PG1 Switch Input)
24	Ground	SGRP (Chassis)	SGRP (Chassis)
25	Discrete3	ABORT Switch Discrete	ABORT Switch Discrete
26	Ground	Reference	Reference
27	Discrete4	ABORT Switch Discrete	ABORT Switch Discrete
28	Ground	Reference	Reference
29	Discrete5	ABORT Switch Discrete	ABORT Switch Discrete

#	Signal Type	Signal Name	
		LCA AF Mk2	AMCA
30	Ground	Reference	Reference
31	Discrete6	ABORT Switch Discrete	ABORT Switch Discrete
32	Ground	Reference	Reference
33	Spare	-	-
34	Spare	-	-
35	Spare	-	-
36	Spare	-	-
37	Spare	-	-

*ESDL-H & ESDL-L are RS-422 interface signals shall be used for hardware debugging

Note: For all above connectors (C1, C2), Pin details shall be defined during design stage.

8.8. Cooling Requirement

The FTU shall be designed to operate satisfactorily without any forced air cooling.

9. ACCEPTANCE

The deliverable units shall be subjected to acceptance tests as described below:

9.1. Initial Visual Examination

The FTU shall be inspected for type / part number, serial number etc., and to visually verify compliance to standard workmanship / assembly practices and conformance to drawings. Also weight and physical dimensions shall be measured and recorded.

9.2. Bonding Test

The bonding resistance test should be carried out for the unit and it should be less than 2.5mΩ.

9.3. Insulation Resistance (IR) Checks:

Insulation resistance should be measured between all the power supply pins w.r.t. the chassis of the unit at room temperature. The insulation resistance should be > 50 M ohm at 500V DC.

9.4. Hardware Acceptance Tests

The purpose of this test is to determine the satisfactory functioning of FTU hardware, when supplied with the required DC Power. These tests shall be performed by executing the ATP test software. The following hardware shall be tested during this acceptance tests:

a) Internal EPROM & RAM (On-chip)

b) External EPROM / Flash

c) Analog Channels

d) Discrete Channels

e) RS 422 Serial Data Link

f) Timer

g) Watch Dog Timer

h) Display and Switches

9.5. Documents

All the documents (Design and Engineering) shall be generated in BEL standard formats and BEL approval for the same shall be obtained for Configuration Management.

The following documents are required:

1) Technical Specification Document.
2) Interface Control Document (ICD).
3) Hardware Requirements Document / Hardware Design Document
4) Schematics.
5) Bill of Materials (BOM).
6) Electronics Design analysis documents (SI, PI, Thermal).
7) Power budget analysis.
8) Obsolescence study report.

9) CAD Design file(.brd, .enm .emp .dxf, X-Y location, footprint analysis, gerber, MD, Electrical net, IPC 356A net list, Design Rule Check.
10) Thermal Analysis, Stress Analysis (Static & Dynamic) and Fatigue analysis for Mechanical Design.
11) All applicable drawings (Part drawings, Mechanical and Electrical assembly Drawings. schematics drawings, etc) including Master Drawing Index (MDI) and Bill of Material (BOM) .
12) De-rating analysis document.
13) Mean Time Between Failures (MTBF) Report/ Reliability prediction report.
14) Failure Modes, Effects and Criticality Analysis (FMECA) Report
15) Acceptance Test Procedure (ATP) Document.
16) Acceptance Test Report (ATR) for every deliverable.
17) Source code and configuration files related application software shall be provided in softcopy.
18) DO-178C, Level C certificate along with following Software Documents:
    a. Software Requirement Specification (SRS)
    b. Software Quality Assurance Plan (SQAP)
    c. Software Design & Development Plan
    d. Software Configuration Management Document
    e. Independent Verification & Validation (IV & V) Plan & Test report
    f. Software Design Document (SDD).
    g. Software Configuration Management Plan (SCMP).
    h. Software Test Plan (STP).
    i. Software Test Report (STR).
    j. Version Description Document (VDD).

10. SCOPE OF WORK

The design and development of FTU Mk2 shall have the following scope of work:

1. The Vendor shall design and develop the FTU MK2 as per the Requirement specification. ***However, for this order the Scope is limited to the Development of one number engineering Unit / LRU.***
2. The Vendor shall design and develop the FTU MK2 in Compliance with DDPMAS 2021 (IMTAR – 21, Ver 01).
3. Vendor has to study the Requirement specifications of FTU Mk2 and accordingly the feasibility study, Concept design, architecture design, Component identification, Schematic capture, component selection study report, and bill of material shall be prepared. BEL will review all of above for Finalization of Hardware Design.
4. BEL will review and finalize the Bill of materials after carrying out thorough analysis w.r.to Design for Manufacturability aspects. (Note: Mil qualified electronics components shall be used in the design, to greater extent possible. In case of non-availability of Mil-grade components, Automotive / industrial grade components can be used).
5. The Vendor shall conduct the progressive design review and project status along with BEL. And shall release the MoM and close the action points as per the PDC.
6. The vendor shall incorporate indigenised design / items / components preferably.
7. The Vendor shall develop the application software (Microcontroller) and shall be comply to DO-178C, Level C.
8. The Vendor shall develop test software required for complete functionality of the Modules / LRU to conduct the ATP and SOFT of unit.
9. The Vendor shall design and fabricate the SRUs / modules as per mechanical form factor in this document.
10. The vendor shall procure the components as per BOM, assemble and test the SRUs and LRU functionally as per the ATP document mutually agreed upon using the available test facility. Note: test jig and tester development is not part of the Scope.
11. The vendor shall demonstrate hardware and software integration.

12. The Vendor shall support design iterations in case of not meeting the specification / functionality in the first iteration.

13. ESS / SOFT test facility will be provided by BEL, Vendor shall demonstrate the functionality of the LRU as per Specification.

14. All the documents shall be reviewed and approved by BEL.

15. The Vendor shall provide the complete Design documents, Manufacturing / engineering documents and reports generated during the design and development phase to BEL as per the para 9.5 list of documents in BEL suggested format and also vendor shall provide documents related to design and development which are missed in the above list.

16. BEL will hold the IP right for all the design and development outputs like hardware, software and documents.

11. DELIVERABLES

SN	LIST OF DELIVERABLES	QTY (Nos)	DD
1	One Engineering FTU LRU	1	T0+6 months
2	NRE towards Design, Analysis and Development (Complete Set of documents, source code, drivers and reports files as per para 9.5)	1	NRE towards Design Analysis and Development of FTU

12. FREE ISSUE MATERIAL / SERVICES

Only ESS and EMI facility will be provided for demonstration of FTU functionality.

13. NON DISCLOSURE TERMS:

1. Vendor should execute a Non-Disclosure Agreement (NDA) before taking up the job.

2. As per official secrets act of BEL, the vendor should not share the schematics, BOM and other design documents with any other third party.

3. All the design inputs given for these activity are the Intellectual property of Bharat Electronics Ltd., Bangalore, India. Reproduction, utilization or disclosure to third parties in any form whatsoever is not allowed without written consent of BEL.