UNIFI Reference Design
1500W-120V Single-phase Grid-forming Inverter

Power Electronics and System Group
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December 16, 2024

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1 System Overview

This section shows the block diagram of the single-phase DC/AC inverter reference design for grid-forming (GFM) applications.

1.1 Block Diagram

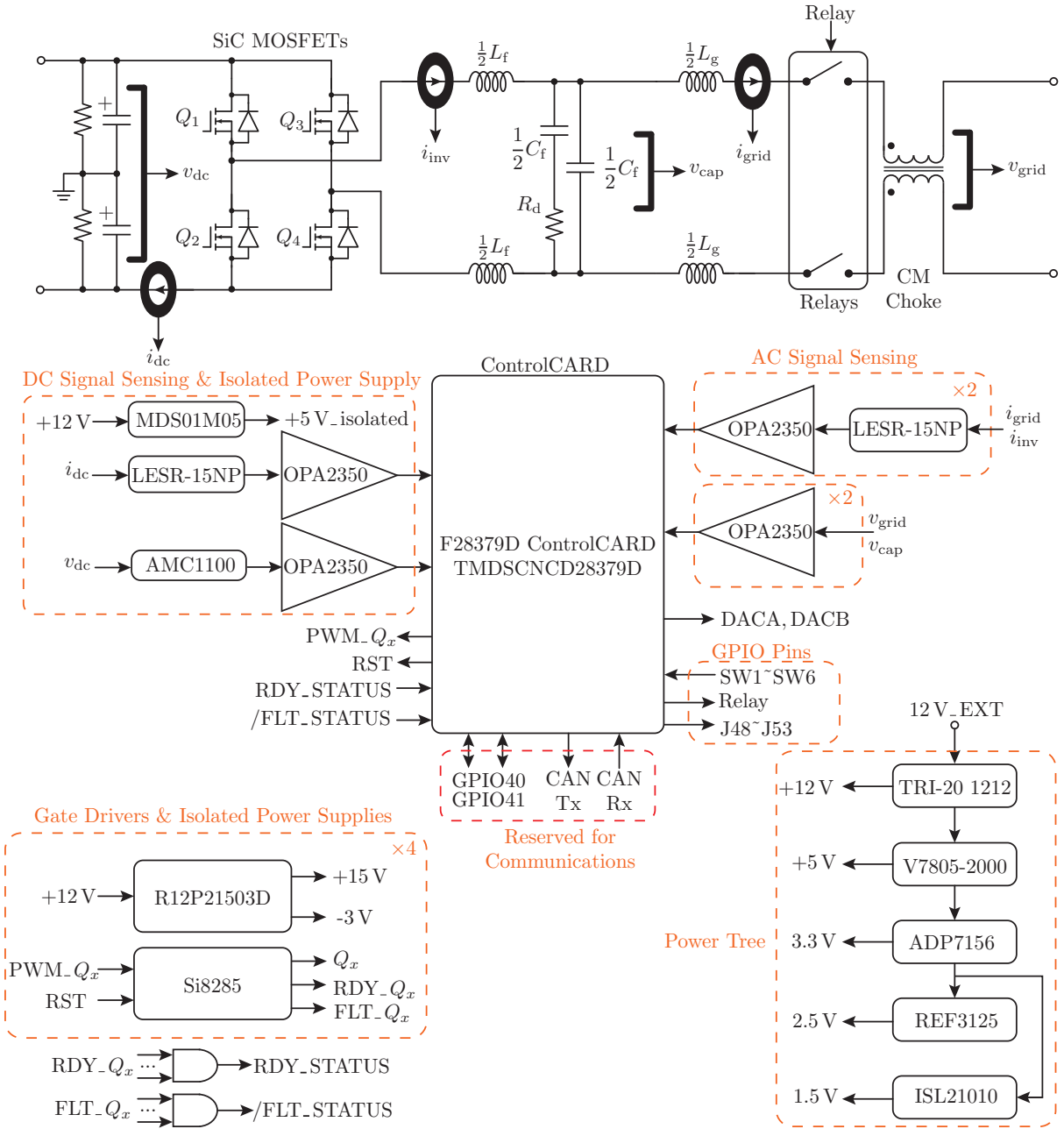

Figure 1: Single-phase GFM inverter block diagram.

The hardware part of the reference design consists of following main sections that intercommunicate:

- A power board comprising the system power tree, the power stage SiC MOSFETs, gate drivers, voltage and current sensing electronics.
- A TMDSCNCD28379D control card to support digital control.

1.2 Key Specifications

Tab. 1 lists some of the critical design specifications of the 1500 W/120 V single-phase grid-forming (GFM) inverter.

Symbol	Parameter	Value	Unit
S_{nom}	Power rating	1500	VA
V_{dc}	Input DC voltage	200	V
V_0	Nominal AC voltage (RMS)	120	V
I_0	Nominal AC current (RMS)	12.5	A
ω_0	Nominal angular frequency	$2\pi 60$	rad/s
f_{sw}	Switching frequency	100	kHz
f_{ctrl}	Control frequency	20	kHz
L_{f}	Filter inductance	300	μH
L_{g}	Output inductance	30	μH
C_{f}	Equivalent filter capacitance	7	μF
R_{d}	Damping resistance	5	Ω

Table 1: Key System Specifications

2 Power Tree

The power tree of this reference design consists of multiple ICs providing the necessary system voltages:

a) An external 12 V power supply is necessary to operate the board. Regulated by TRI 20-1212 isolated DC/DC converter, the 12 V rail powers the relays and R12P21503D isolated bias supplies.

b) 5 V rail regulated from 12 V rail is to power the Control Card.

c) 3.3 V rail regulated from 5 V rail is to power the gate driver digital side and sensing circuits. LED1 is used to indicate the status of 3.3 V rail.

d) 1.5 V and 2.5 V from 3.3 V rail is to the sensing circuits.

e) The isolated bias supplies provide +15 V and -3 V for gate drives.

f) The isolated 5 V from 12 V power rail is to power the DC voltage sensing electronics.

Most of the power rails are shown in Fig. 2. Besides, Each gate driver has an independent R12P21503D isolated bias supply, as shown in Fig. 3, which regulates VCC at +15 V and VEE at -3 V. The DC sensing circuit is also powered by a separate isolated 5 V power supply depicted in Fig. 4.
To test the status of above voltage rails, several test points are added as listed in Tab. 2.

3 ControlCARD Setting

In this reference design, Delfino F28379D controlCARD (TMDSCNCD28379D) from Texas Instruments (TI) is used as the microcontroller. The controlCARD is connected to the main circuit via a 180-pin connector, of which the associated pinmap is given in this section. Fig. 5 illustrates the various components on the card, some of which related to this design are in need of correct configuration.

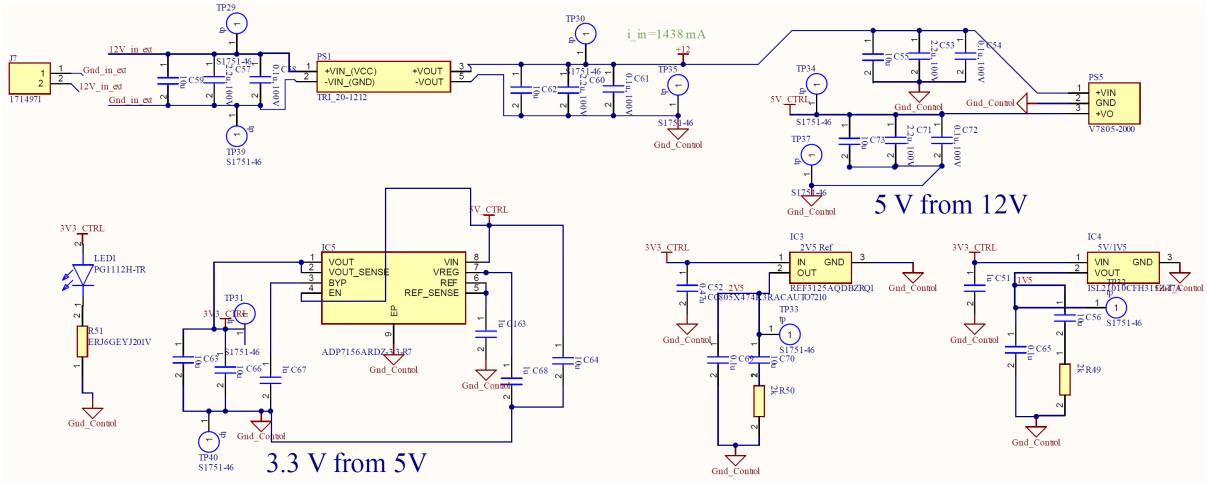

Figure 2: The power rails of the reference design, including +12 V, +5 V, 3.3 V, 2.5 V, and 1.5 V.

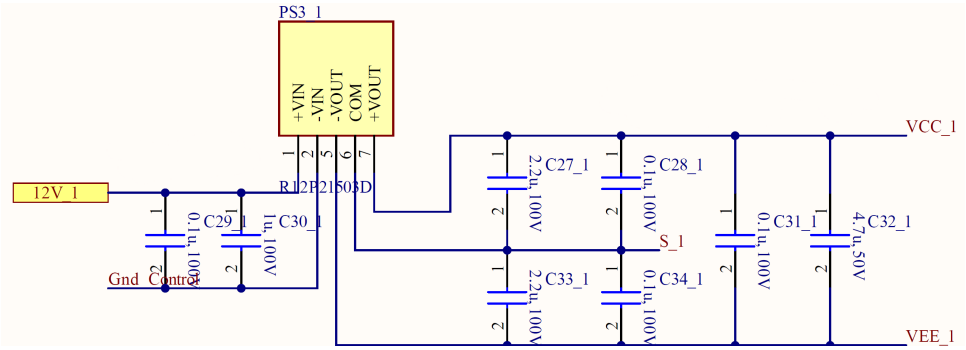

Figure 3: The isolated bias supply regulating +15 V and -3 V in the gate driver circuitry of MOSFET Q1.

3.1 Selected Configuration

a) In the reference design, the manual switch SW4 on the main board connected to GPIO121 is impacted by the jumpers on controlCARD. When controlCARD jumpers J2-J7 are all up, GPIOs 42, 43, 46, 47, 120, and 121 are used for USB PHY connection. Hence, to enbale manual switch SW4 on the mother board, all jumpers J2-J7 on the controlCARD need to be pulled down.

b) In MCU F28379D, the ADC high reference voltage can be set as either 3.3 V or other external voltage reference. In this design, we pick the 3.0 V voltage reference by adjusting the switch on the controlCARD.

   Illustrated in Fig. 5, SW2 and SW3 are ADC VREFHI control switches for ADCA, ADCB and ADCC, ADCD, respectively. When the switch is in the left position, VREFHI uses 3.3 V; In the right position, VREFHI is configured to a precise 3.0 V. Hence, in this design, we keep all switches in SW2, SW3 at the right position.

3.2 Pinmap

The pinmap between the MCU pins and the 180 controlCARD pins (HSEC pins) is shown in Tab. 3.

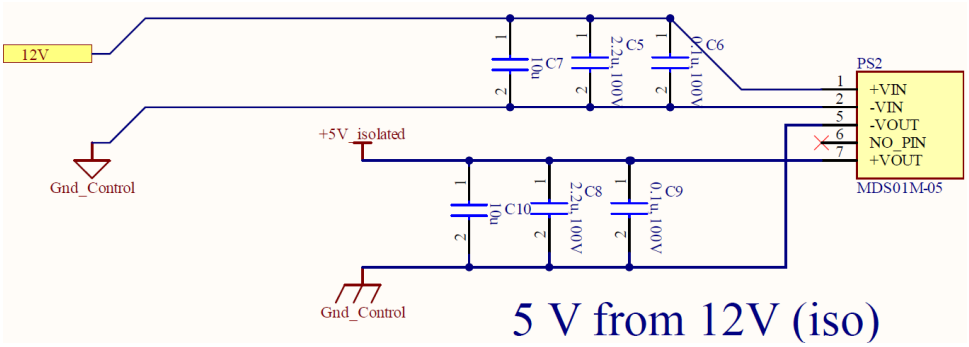

Figure 4: The power supply providing isolated 5 V for DC voltage sensing circuit.

Power rail	12 V_EXT	12 V	5 V	3.3 V	2.5 V	1.5 V
Test point	TP29-39	TP30-35	TP34-37	TP31-40	TP33-40	TP32-40

Table 2: Test points for different power rails

4 *LCL* Filter Design & Implementation

4.1 *LCL* Filter Design

The design constraints taken into consideration in this reference design are listed as follows

a) The resonant frequency of *LCL* filter must satisfy the following inequality

$$10f_0 < f_{\text{res}} = \frac{1}{2\pi}\sqrt{\frac{L_{\text{f}}+L_{\text{g}}}{L_{\text{f}}L_{\text{g}}C_{\text{f}}}} < \frac{1}{2}f_{\text{sw}} \tag{1}$$

b) The current ripple (defined as peak to peak) on inverter-side filter inductor L_{f} should not exceed 10% of maximum current under unipolar PWM. This constraint is picked such that the current ripple is no more than 20% even under bipolar PWM:

$$\Delta I_{\text{pp}} = \frac{V_{\text{dc}}}{4f_{\text{sw}}L_{\text{f}}} \leq 10\% \cdot \sqrt{2}I_0 \tag{2}$$

c) The total voltage drop across the filter inductance, two inductances L_{f}, L_{g} as a whole, should be less than 10% of the nominal voltage:

$$L_{\text{f}} < L_{\text{f}} + L_{\text{g}} < 10\% \cdot \frac{V_0}{\omega_0 I_0} \tag{3}$$

d) The filter capacitance C_{f} is restricted by the reactive power on it such that the reactivce power across capacitance is less than 5% at rated loads:

$$C_{\text{f}} \leq 5\% \cdot \frac{S_{\text{nom}}}{\omega_0 V_0^2} \tag{4}$$

e) The voltage ripple on C_{f} is limited to less than 1%. Approximating the voltage ripple as shown in [1], there comes

$$\Delta V_{\text{pp}} = \frac{\Delta I_{\text{pp}}}{8C_{\text{f}}f_{\text{sw}}} \leq 1\% \cdot \sqrt{2}V_0. \tag{5}$$

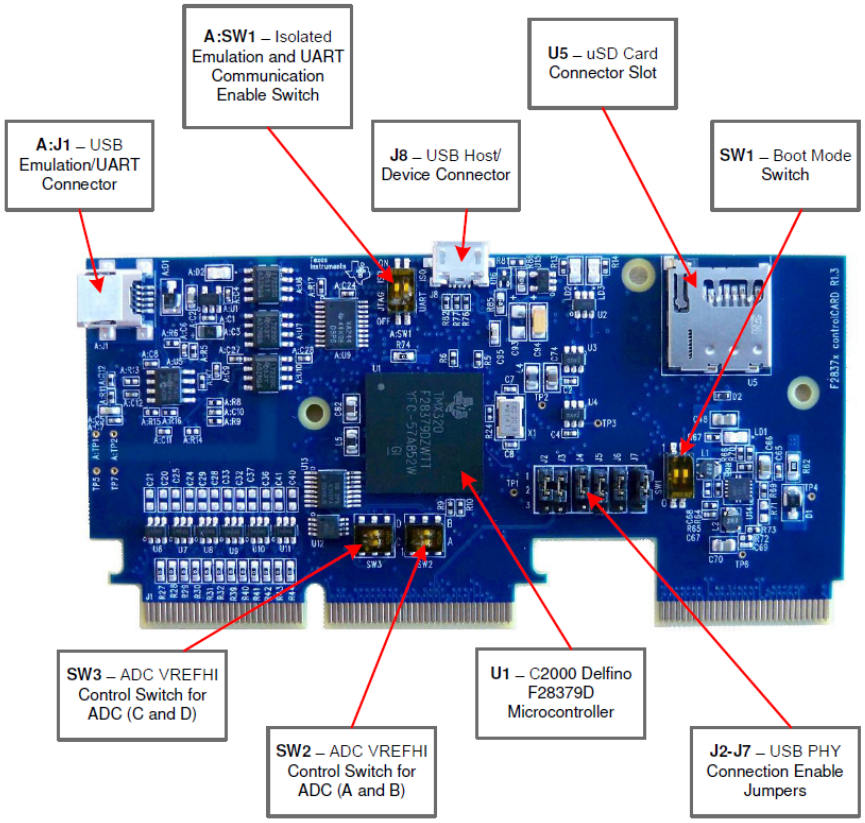

Figure 5: Key components on the controlCARD

f) Grid-side inductance L_{g} should attenuate the output current ripple within 2% [2, 3]. The current ripple can be derived by the transfer function of inverter-side current to output current as

$$\frac{i_{\mathrm{g}}(s)}{i(s)} = \frac{L_{\mathrm{f}}C_{\mathrm{f}}s^2 + 1}{L_{\mathrm{f}}L_{\mathrm{g}}C_{\mathrm{f}}^2 s^4 + (L_{\mathrm{f}} + L_{\mathrm{g}})C_{\mathrm{f}}s^2 + 1}. \tag{6}$$

Since the ripple is at switching frequency, then after some approximation we can obtain the output current ripple as

$$\Delta I_{\mathrm{g,pp}} = \Delta I_{\mathrm{pp}} \cdot \left\| \frac{i_{\mathrm{g}}(j\omega_{\mathrm{sw}})}{i(j\omega_{\mathrm{sw}})} \right\| \approx \frac{Z_{\mathrm{LC}}^2}{\|\omega_{\mathrm{res}}^2 - \omega_{\mathrm{sw}}^2\|}, \quad \text{where} \quad Z_{\mathrm{LC}} = \sqrt{\frac{1}{L_{\mathrm{g}}C_{\mathrm{f}}}}. \tag{7}$$

g) According to IEEE standard for harmonic control in electric power systems, i.e. IEEE 519-2022 [4], voltage THD should be less than 8% and individual harmonic magnitude less than 5%. The current harmonic distortion requirement is also given. The requirements are verified after the design satisfying requirements is obtained.

Considering all above constraints, the LCL filter inductance and capacitance is obtained as listed in Table 1.

4.2 LCL Filter Implementation

In the hardware realization, both two inductances are distributed evenly on each leg to minimize common-mode components as shown in Fig. 6, in which R_{f} and R_{g} are ESRs of those inductors. Besides, a damping resistance R_{d} is also integrated following [5] to obtain a low quality factor as well as a relatively low power loss.

HSEC pin	MCU pin	Name on Schematic
9	DACA	DACA
11	DACB	DACB
12	ADC-B0	I_dc sensing signal
14	ADC-B1	V_dc sensing signal
15	ADC-A2	i_inv_A1 sensing signal
17	ADC-A3	i_grid_A1 sensing signal
31	ADC-C2	V_cap_A1 sensing signal
33	ADC-C3	V_grid_A1, sensing signal
49	PWM1A	PWM_Q1
51	PWM1B	PWM_Q2
53	PWM2A	PWM_Q3
55	PWM2B	PWM_Q4
80	CANRX	Rx
82	CANTX	Tx
89	GPIO-40	GPIO40
91	GPIO-41	GPIO41
121	GPIO-35	Relay_1, relay control output
122	GPIO-36	Gpio48, J48 GPIO output
124	GPIO-38	Gpio49, J49 GPIO output
126	GPIO-61	Gpio50, J50 GPIO output
128	GPIO-63	Gpio51, J51 GPIO output
130	GPIO-65	Gpio52, J52 GPIO output
132	GPIO-67	Gpio53, J53 GPIO output
159	GPIO-90	RST, GPIO output
161	GPIO-92	/FLT_STATUS, GPIO input
163	GPIO-94	RDY_STATUS, GPIO input
160	GPIO-91	SW1, manual switch input
162	GPIO-93	SW2, manual switch input
164	GPIO-133	SW3, manual switch input
166	GPIO-121	SW4, manual switch input
168	GPIO-162	SW5, manual switch input
170	GPIO-164	SW6, manual switch input

Table 3: ControlCARD Pinmap in the reference design

4.3 Magnetic Design of The Filter Inductor

The grid-side inductor uses existing inductor product while the inverter-side inductance is customarily built by the user. On the schematic and PCB layout, only the bobbin mechanically connected onto the board is given. The magnetic wires, cores, and other accessories are assembled additionally.

As explained before, the inverter-side inductor on each leg is $150\,\mu$F. Let maximum operating current be 25 A, maximum magnetic field be at 3 T, the winding fill factor be 0.4, then the inverter-side inductor is obtained by K_c method referring to [1]. After RLC meter test, some modifications may be needed to obtain the final design in Tab. 4.

4.4 Common Mode Choke

Common mode voltage reflects the voltage difference between the power source and the neutral point of a load. In inverters, we take the DC bus midpoint as zero potential reference, but

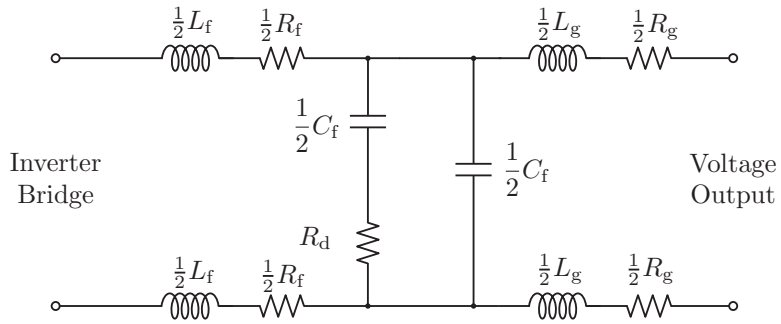

Figure 6: LCL filter implementation with damping resistor and evenly distributed inductances.

Core	TDK PQ 5O/50 DG, ordering code: B65981Q0100K095
Wire	AWG16 magnetic wire
Turn number	40
Air gap	5.04 mm*

Table 4: Key specifications in inverter-side inductor manufacturing. *Note that this core already has sufficient built-in air gaps, so no additional air gap is in need in manufacturing.

on AC side we actually take AC neutral as zero potential reference. These two have different potentials in physical reality and such voltage difference leads to current in between. In the reference design, the common-mode choke SCF47C-400-1R8C040JH, which tolerates 40 A DC current, that is two times of our nominal AC current magnitude, is deployed.

5 Power Stage Design

5.1 Capacitor selection

The DC link capacitor should create a stiff DC bus which provides low impedance path for high frequency currents. Major considerations in selecting capacitors were ripple current, DC bus voltage, DC bus voltage ripple and resonant frequency. For a reasonable energy storage in the DC bus, four metallized polypropylene film capacitors with a DC voltage rating of 800 V and capacitance of 30μF are connected in parallel. Several aluminum electrolytic capacitors rated at 350 V and 680μF are used in series-parallel connection. Multiple ceramic capacitors rated at DC voltage of 630V and capacitance of 47000pF are connected between $V_{\mathrm{dc}+}$ and $V_{\mathrm{dc}-}$.

5.2 Semiconductor device selection

The main switching devices in power stage should block the full input DC voltage. The switch should have high blocking voltage with low on-resistance, high-speed switching with low capacitances and fast intrinsic diode with low reverse recovery. This reference design uses six C3M0030090K discrete devices, based on C3M^{TM} Silicon Carbide (SiC) power MOSFET Technology, which increase power density and switching frequency. This MOSFET has a drain source voltage of of 900 V, continuous drain current of 73 A at 25° C and a drain-source on-state resistance of 30 $m\Omega$.

5.3 Switching frequency

The SiC MOSFETs in the power stage enables the inverter to switch at a higher frequency. This helps to reduce the size of magnetics used in the converter and increases the power density. The

switching frequency chosen for this reference design is 120 kHz. The control frequency is 20 kHz.

5.4 Gate driver design

The gate driver used in this design is the SI8285BC-ISR. It is an isolated, high current gate driver with integrated system safety and feedback functions. These devices are ideal for driving SiC power MOSFETs. The isolated bias supply selected for this gate driver is R12P21503D. This dc-dc converter is designed for high slew rate SiC transistor drivers. It has high isolation voltage and low isolation capacitance.

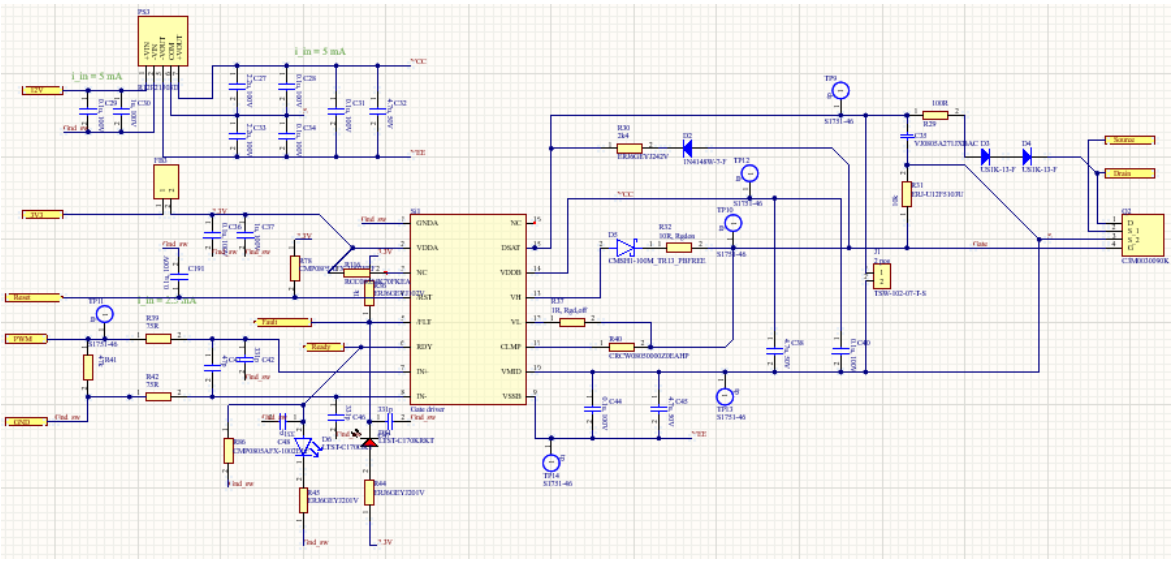

Figure 7: Gate driver schematic.

5.5 Thermal considerations

Three Wakefield Solutions OmniKlip TO-247/TO-264 (OMNI-UNI-41-75) heat sinks are used to cool the FETs. Each heat sink supports two MOSFETs. The 3M™ Thermally conductive adhesive transfer tapes (8810) are used between the FETs and the heat sinks to provide necessary insulation and a good thermal interface.

6 ADC Sensing Circuit Design

As shown in Fig. 1, there are 6 different voltage and current analog signals sensed in the reference design. The six signals are respectively

- Inverter-side inductor current from H-bridge to filter capacitor;
- Output-side inductor current from filter capacitor to AC output terminal;
- Filter capacitor voltage;
- Grid-side voltage after the relay;
- DC input current;
- DC input terminal voltage;

Notably, the ac sensing circuit output i_inv, i_grid, v_cap, V_grid are connected to the signal i_inv_A1, i_grid_A1, v_cap_A1, V_grid_A1 that feeds the controlCARD via external RF cables as shown in the schematic.
In this section, the sensing circuitry input-to-output relations are given, of which the inverted ones direct the ADC-related coding.
The reference voltage used in the MCU in this design is 3.0 V.

6.1 Current Sensing Circuitry

Both the DC input current and two AC outpout current sensing circuitry share the same architecture. Neglecting the filtering circuit, the sensing circuitry is shown in Fig. 8, in which i_{sens} is the current to be sampled and v_{o} is the sensed voltage feeding the MCU pin. TH ADC sensing relation is given by

$$v_{\text{o}} = G_{\text{i,sens}} \frac{R_2}{R_1} i_{\text{sens}} + 1.5 \text{ [V]}, \tag{8}$$

where $G_{\text{i,sens}}$ is the sensitivity of LESR15NP Hall sensor. Referring to its datasheet, it is obtained that $G_{\text{i,sens}} = 41.67\,\text{mV/A}$ given the pin connection applied in this reference design.
In two AC current sensing, the sensing resistance is given by $R_1 = R_2 = 1\,k\Omega$.
In DC current sensing, the sensing resistance is given by $R_1 = 3.3\,k\Omega,\ R_2 = 8.2\,k\Omega$.

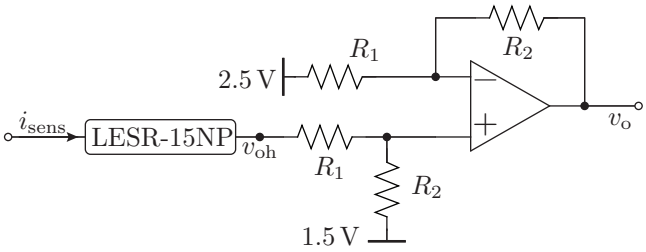

Figure 8: The sensing circuitry shared by DC and AC current sensing.

6.2 AC Voltage Sensing Circuitry

Similarly, the AC voltage sensing circuitry for two AC voltage is shown in Fig. 9. The input-

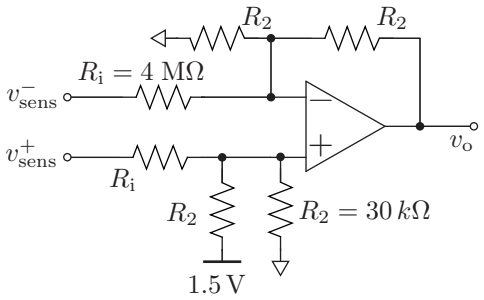

Figure 9: AC voltage sensing circuitry.

to-output relation is derived as

$$v_{\text{o}} = 1.5 + \frac{R_2}{R_{\text{i}}} v_{\text{sens}} \text{ [V]}, \tag{9}$$

where $v_{\text{sens}} = v_{\text{sens}}^+ - v_{\text{sens}}^-$ is the voltage to be sensed.
As shown above, there exist $R_2 = 30\,k\Omega$ and $R_{\text{i}} = 3\,\text{M}\Omega$.

6.3 DC Voltage Sensing Circuitry

The DC input voltage sensing circuitry is shown in Fig. 10. The input-to-output relation is

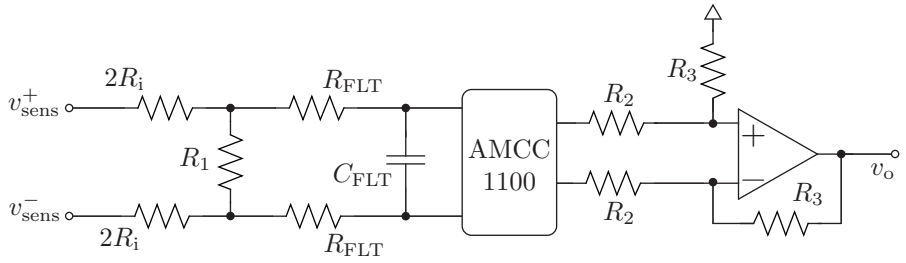

Figure 10: DC voltage sensing circuitry.

derived as

$$v_\text{o} = \frac{R_1}{4R_\text{i} + R_1}\frac{R_3}{R_2}G_\text{amcc}v_\text{sens}\ [\text{V}], \tag{10}$$

where $v_\text{sens} = v^+_\text{sens} - v^-_\text{sens}$ is the voltage to be sensed. $G_\text{amcc} = 8$ is the gain of the differential isolation amplifier AMCC1100 in the circuitry.
In Fig. 10, there exist $R_i = 100\,k\Omega$, $R_2 = 2\,k\Omega$, and $R_3 = 4.3\,k\Omega$.

7 Other Accessories Besides BOM

7.1 MOSFET Installation

Place a thermally conductive tape (3M™ Thermally Conductive Adhesive Transfer Tape 8810) between the heatsink and MOSFET. Use clips (Wakefield Solutions OmniKlip TO-247/TO-264 Heat Sinks) to hold it firmly as shown in Fig. 11.

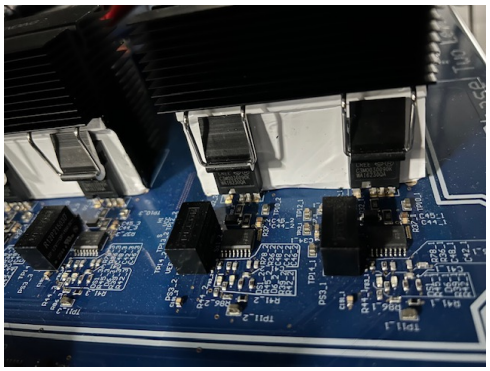

Figure 11: MOSFET and heatsink assembly reference

7.2 Inductor Installation

The user needs to custom build the inverter side inductance. In the schematic and PCB layout, only the bobbin footprint is created. This bobbin needs to be mechanically connected to the PCB. In order to assemble the complete inductor, components like the magnetic wires, cores, shim stock, and Kapton tape are wrapped around the bobbin.

The inductor on the inverter side on each leg is chosen to be $120\,\mu$F. The components used in the final design are listed in Tab. 4. A Kapton tape is used to hold everything in place firmly.

The number of turns needed should be around 48 and can be adjusted to match the required inductance. Measure inductance and R_s using a precision LCR meter. The R_s should be around 1.3 - 1.5 Ohms at 100kHz. Minor modifications based on measurements of the LCR meter are acceptable. Custom inductors when soldered to the appropriate designators on the PCB should look like Fig. 12.

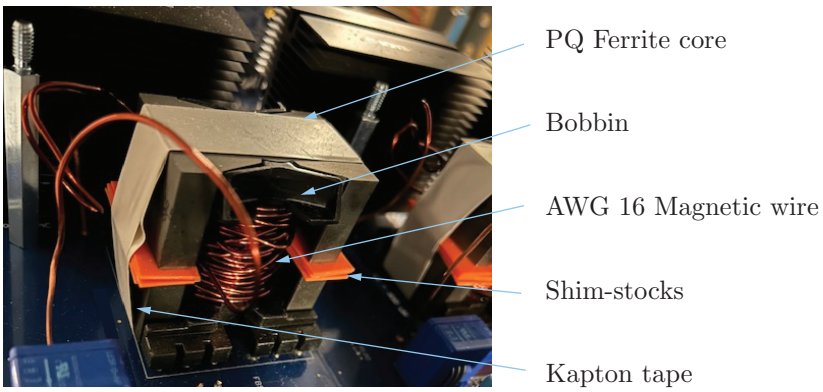

Figure 12: Custom Inductor construction.

7.3 RF Cables

The ac sensing circuit output i_inv, i_grid, v_cap, V_grid are connected to the signal i_inv_A1, i_grid_A1, v_cap_A1, V_grid_A1 that feeds the controlCARD via external RF cables, respectively, as shown in the schematic. Besides, the relay control signal Relay and Relay_1 also need to be connected via RF cables.
In this design, RF cable connectors of signal GPIO40, GPIO41, DACA, and DACB are reserved for customized applications.

7.3.1 Standoffs

User needs to order and assemble Hex Nuts (M5x0.8mm) and M5 Standoffs in the 9 holes provided on the PCB. To protect the components assembled on the PCB, make sure to stack sufficient number of standoffs above and below the PCB.

8 Software Design

To download the Software related files see files and documentation at GitHub - UNIFI Consortium.

9 Design Files

9.1 Schematics

To download the schematics, see the design files at GitHub - UNIFI Consortium.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at GitHub - UNIFI Consortium.

9.3 Altium Project

To download the Altium Designer® project files, see the design files at GitHub - UNIFI Consortium.

9.4 Gerber Files

To download the Gerber files, see the design files at GitHub - UNIFI Consortium.

9.5 Assembly Drawings

To download the assembly drawings, see the design files GitHub - UNIFI Consortium.

9.6 CCS Project

To download the Code Composer Studio® files, see the design files at GitHub - UNIFI Consortium.

References

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[2] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an lcl-filter-based three-phase active rectifier," *IEEE Transactions on industry applications*, vol. 41, no. 5, pp. 1281–1291, 2005.

[3] A. Reznik, M. G. Simões, A. Al-Durra, and S. Muyeen, "LCL filter design and performance analysis for grid-interconnected systems," *IEEE transactions on industry applications*, vol. 50, no. 2, pp. 1225–1232, 2013.

[4] "IEEE standard for harmonic control in electric power systems," *IEEE Std 519-2022 (Revision of IEEE Std 519-2014)*, pp. 1–31, 2022.

[5] P. Channegowda and V. John, "Filter optimization for grid interactive voltage source inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 12, pp. 4106–4114, 2010.