UNIFI Reference Design
5kW Three-phase Grid-forming Inverter

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1 System Overview

This section provides an overview of the three-phase DC/AC inverter hardware reference design, specifically tailored for grid-forming (GFM) applications.

1.1 Block Diagram

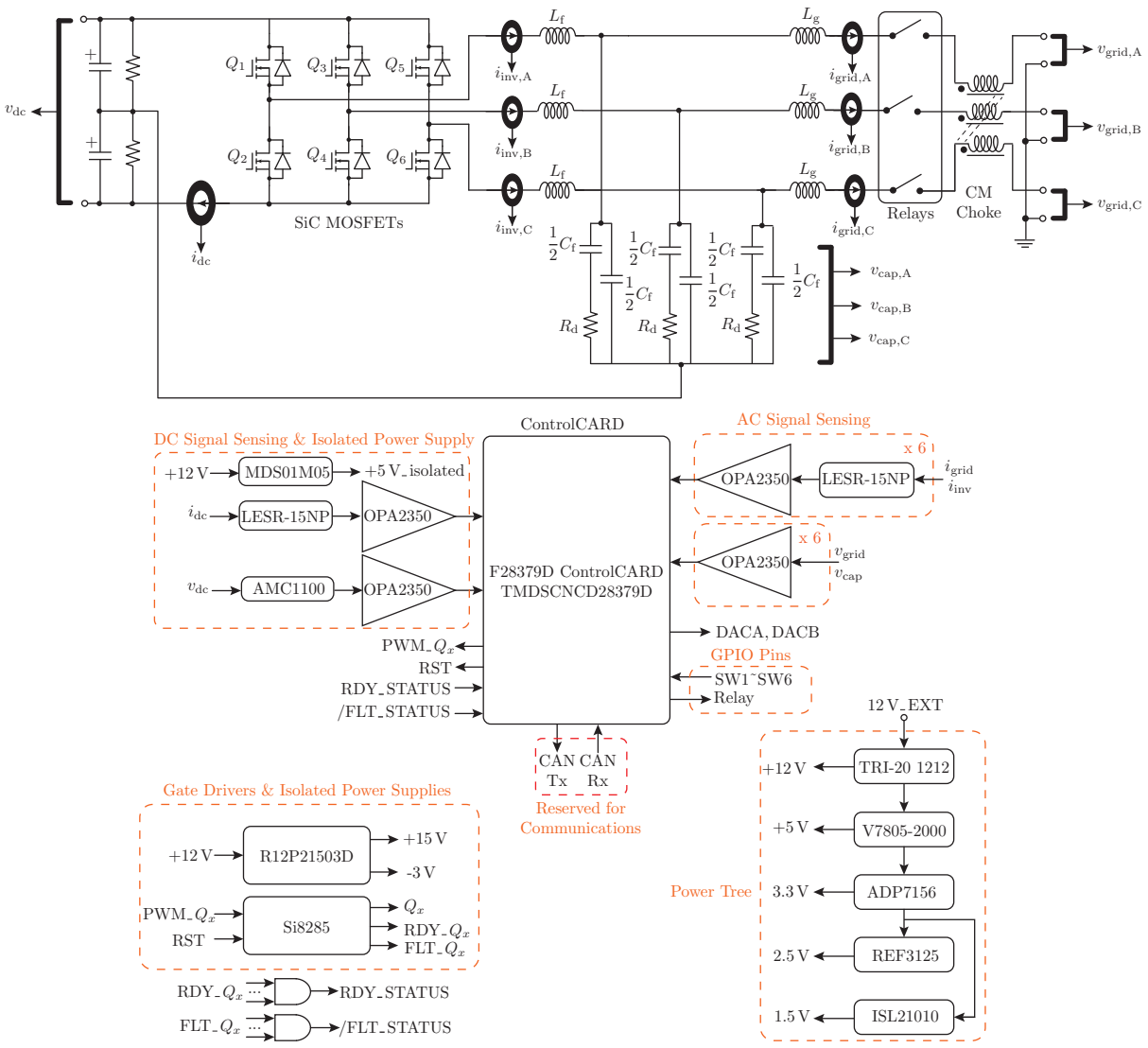

Figure 1: Three-phase GFM inverter block diagram.

The hardware implementation of the reference design includes the following key components, which interact cohesively:

- A power board comprising the system power tree, the power stage SiC MOSFETs, gate drivers, voltage and current sensing electronics.
- A TMDSCNCD28379D control card for supporting digital control operations.

1.2 Key specifications

Tab. 1 lists some of the critical design specifications of the 5000 W/208 V three-phase grid-forming (GFM) inverter.

Symbol	Parameter	Value	Unit
S_{nom}	Power rating	5000	VA
V_{dc}	Input DC voltage	400	V
V_0	Nominal AC voltage (RMS)	208	V
I_0	Nominal AC current (RMS)	13.87	A
ω_0	Nominal angular frequency	$2\pi 60$	rad/s
f_{sw}	Switching frequency	120	kHz
f_{ctrl}	Control frequency	20	kHz
L_{f}	Filter inductance	120	μH
L_{g}	Output inductance	30	μH
C_{f}	Equivalent filter capacitance	7	μF
R_{d}	Damping resistance	5	Ω

Table 1: Key System Specifications

2 Power architecture

The power tree of this reference design consists of multiple ICs providing the necessary system voltages:

a) An external 12 V power supply is necessary to operate the board. Regulated by TRI 20-1212 isolated DC/DC converter, the 12 V rail powers the relays and R12P21503D isolated bias supplies.

b) The isolated bias supplies provide +15 V and -3 V for gate drives.

c) 5 V regulated from 12 V rail is to power the Control Card.

d) 3.3 V, regulated from 5 V rail is to power the gate driver digital side and sensing circuits. LED1 is used to indicate the status of 3.3 V rail.

e) 1.5 V and 2.5 V from 3.3 V rail is to the sensing circuits.

To test the status of above voltage rails, several test points are added as listed in Tab. 2. The power rails, except the bias power output for gate drivers, are shown in Fig. 2. Each gate driver has an independent R12P21503D isolated bias supply, as shown in Fig. 3, which regulates VCC at +15 V and VEE at -3 V.

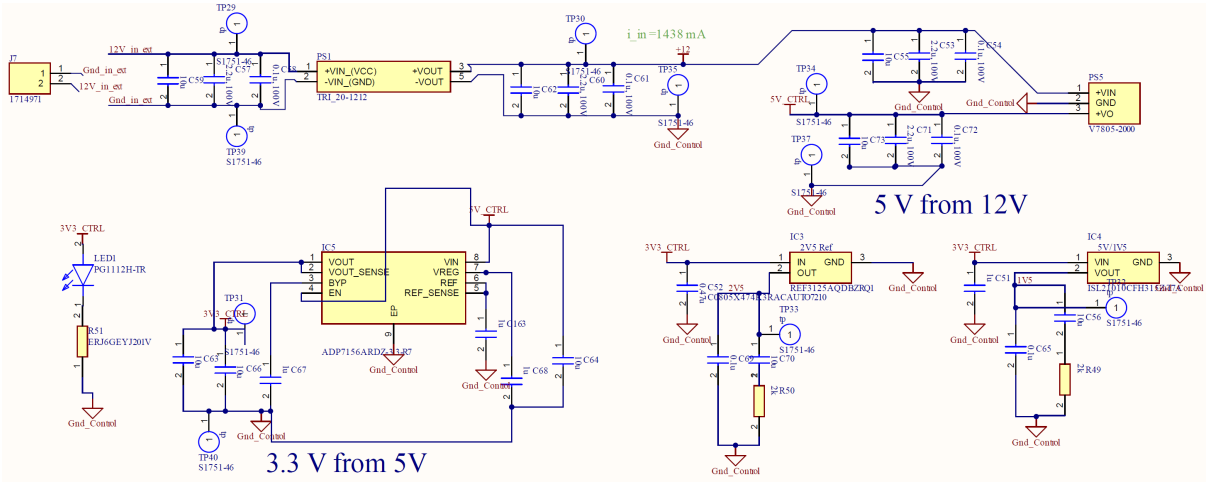

Figure 2: The power rails of the reference design, including +12 V, +5 V, 3.3 V, 2.5 V, and 1.5 V.

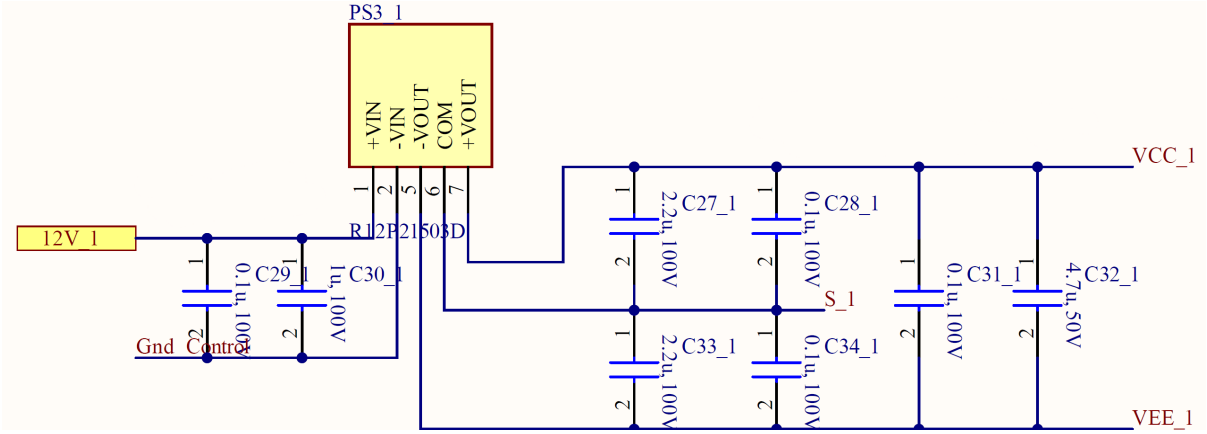

Figure 3: The isolated bias supply regulating +15 V and -3 V in the gate driver circuitry of MOSFET Q1.

Voltage rail	Test point
12 V EXT	TP29, 39
12 V	TP30, 35
5 V	TP34, 37
3.3 V	TP31, 40
2.5 V	TP33, 40
1.5 V	TP32, 40

Table 2: Test points for different power rails

3 ControlCARD setting

In this reference design, Delfino F28379D controlCARD (TMDSCNCD28379D) from Texas Instruments (TI) is used as the microcontroller. The controlCARD is connected to the main circuit via a 180-pin connector, of which the associated pinmap is given in this section. Fig. 4 illustrates the various components on the card. The three-phase inverter board needs a certain configuration to operate.

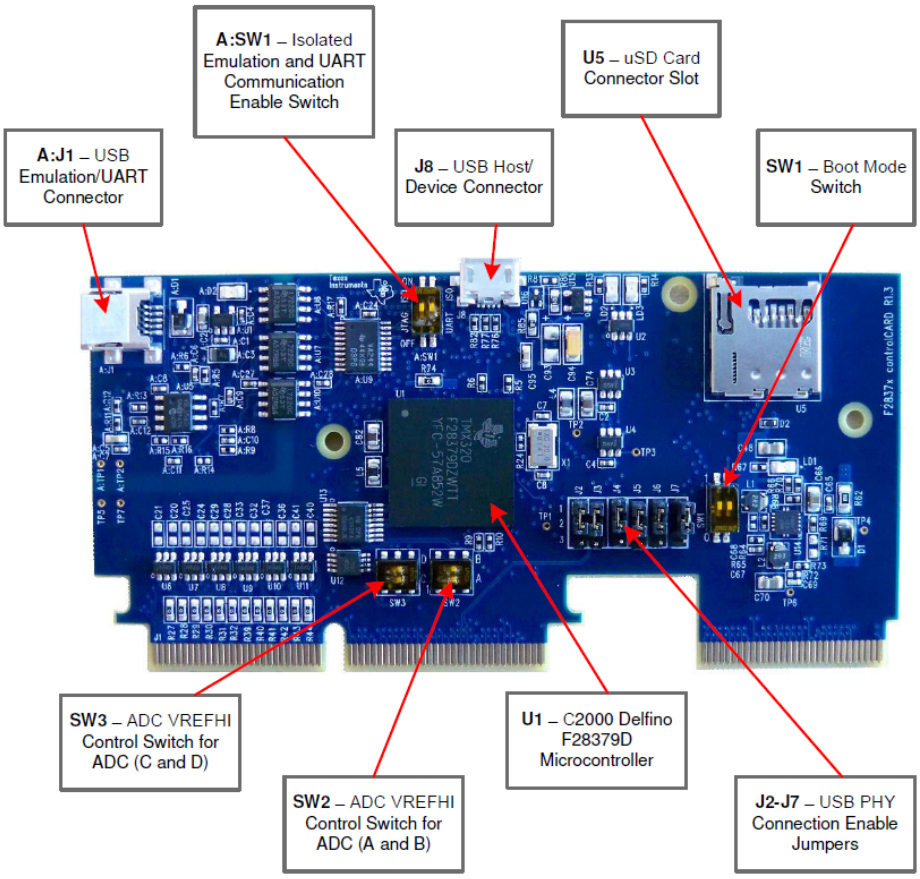

Figure 4: Key components on the controlCARD

3.1 Selected configuration

In MCU F28379D, the ADC high reference voltage can be set as either 3.3 V or other external voltage reference. In this design, we pick the 3.0 V voltage reference by adjusting the switch on the controlCARD. Illustrated in Fig. 4, SW2 and SW3 are ADC VREFHI control switches for ADCA, ADCB and ADCC, ADCD, respectively. When the switch is in the left position, VREFHI uses 3.3 V; In the right position, VREFHI is configured to a precise 3.0 V. Hence, in this design, we keep all switches in SW2, SW3 at the right position.

3.2 Pinmap

The pinmap between the MCU pins and the 180 controlCARD pins (HSEC pins) is shown in Tab. 3.

HSEC pin	MCU pin	Function
9	DACA	DACA
11	DACB	DACB
12	ADC-B0	I_dc sensing signal
14	ADC-B1	V_dc sensing signal
15	ADC-A2	i_inv_A sensing signal
17	ADC-A3	i_grid_B sensing signal
18	ADC-B2	V_cap_A sensing signal
20	ADC-B3	V_cap_B sensing signal
21	ADC-A4	i_inv_C sensing signal
24	ADC-B4	V_cap_C sensing signal
31	ADC-C2	i_grid_A sensing signal
33	ADC-C3	i_grid_B, sensing signal
36	ADC-D3	V_grid_B, sensing signal
37	ADC-C4	i_grid_C, sensing signal
40	ADC-D4	V_grid_C, sensing signal
49	PWM1A	PWM_Q1
50	PWM3A	PWM_Q5
51	PWM1B	PWM_Q2
52	PWM3B	PWM_Q6
53	PWM2A	PWM_Q3
55	PWM2B	PWM_Q4
80	CANRX	Rx
82	CANTX	Tx
121	GPIO-35	Relay_1, relay control output
124	GPIO-49	Gpio49, GPIO output
126	GPIO-50	Gpio50, GPIO output
128	GPIO-51	Gpio51, GPIO output
130	GPIO-52	Gpio52, GPIO output
132	GPIO-52	Gpio52, GPIO output
159	GPIO-90	/FLT_STATUS, GPIO input
160	GPIO-91	SW1, manual switch input
161	GPIO-92	/RDY_STATUS, GPIO input
162	GPIO-93	SW2, manual switch input
163	GPIO-94	RST, GPIO output
164	GPIO-133	SW3, manual switch input
166	GPIO-121	SW4, manual switch input
168	GPIO-162	SW5, manual switch input
170	GPIO-164	SW6, manual switch input

Table 3: ControlCARD Pinmap in the reference design

4 LCL filter design

In grid-connected inverters, a LCL filter is commonly employed. The LCL filter has an ability to provide better attenuation at the switching frequency while maintaining the same or even lower total inductance (i.e., $L_{\mathrm{f}} + L_{\mathrm{g}}$).
The parameters of the LCL filter are calculated based on design constraints and IEEE recommendations in [1], and [2]. A passive damping scheme, as shown in 5, is implemented to address the resonance damping issue. This approach results in a low quality factor and relatively low

power loss. The design procedure for this reference design follows the method outlined in [4]

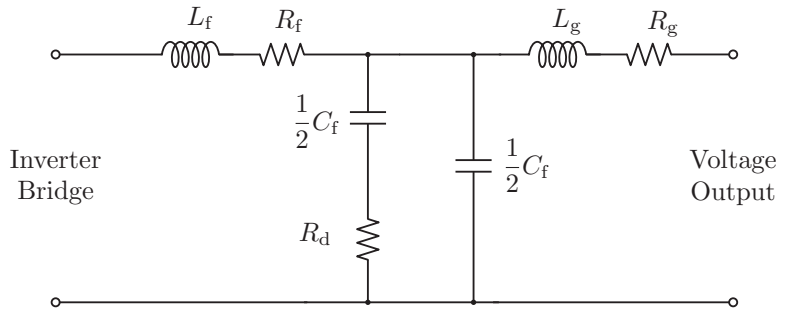

Figure 5: LCL filter implementation with damping resistor, capacitor and inductor.

4.0.1 Design constraints

The design constraints taken into consideration in UNIFI reference design are listed as follows:

1. The resonant frequency of LCL filter is chosen to satisfy, $f_\mathrm{res} = 10\% f_\mathrm{sw}$
2. The maximum current ripple (defined as peak to peak) on inverter-side filter inductor is obtained from nominal value of current as $\Delta I_\mathrm{pp} = 20\% \cdot I_0$.
3. The maximum voltage ripple, ΔV_pp is limited to 1% of the nominal voltage V_0
4. Inverter-side inductance L_f is chosen based on the maximum allowable ripple in the inductor current, as follows:

$$L_\mathrm{f} = \frac{V_\mathrm{dc}}{4 f_\mathrm{sw} \Delta I_\mathrm{pp}}.$$

5. Grid-side inductance L_g can be selected as 10% of the inverter side inductance, L_f
6. The maximum and minimum values of filter capacitance C_max and C_min respectively are obtained as follows:

$$C_\mathrm{max} = \frac{0.05(S_\mathrm{nom}/3)}{V_0^2 \omega_0} \quad \text{and} \quad C_\mathrm{min} = \frac{\Delta I_\mathrm{pp}}{8 f_\mathrm{sw} \Delta V_\mathrm{pp}},$$

   where C_max is decided based on maximum allowable reactive power injection by the filter capacitor and C_min is limited by the maximum permissible ripple in capacitor voltage.

7. The value of filter capacitance C is found using the value of f_res, L_f, and L_g as follows,

$$C = \frac{1}{\omega_\mathrm{res}^2 L_\mathrm{eqv}},$$

   where $L_\mathrm{eqv} = \frac{L_f L_g}{L_f + L_g}$.

8. Damping resistance, R_d is taken equal to the characteristic impedance of the LCL circuit.

Considering all above constraints, the LCL filter inductance and capacitance is obtained as listed in Table 4.

Table 4: Filter Parameters

Symbol	Parameter	Value	Unit
L_{f}	Filter inductance	120	μH
L_{g}	Output inductance	30	μH
C	Equivalent filter capacitance	7	μF
R_{d}	Damping resistor	5	Ω

4.1 Filter inductor design and implementation

The grid-side inductor is off the shelf while the inverter-side inductance is custom built by the user. The grid-side inductor is a leaded power inductors with inductance of 33μH . The inverter-side inductors on each leg are chosen to be 120 μF. The inductance value is majorly based on K_{c} method referring to [3] with minor modifications based on LCR meter measurements. It is built using a PQ - N95 Ferrite core.

4.2 Common mode choke

Common mode voltage reflects the voltage difference between the power source and the neutral point of a load. In inverters, we take the DC bus midpoint as zero potential reference, but on AC side we actually take AC neutral as zero potential reference. These two have different potentials in physical reality and such voltage difference leads to current in between. In this reference design the common-mode choke used is SCF47C-400-1R8C040JH. It tolerates twice of the nominal AC current magnitude (40 A DC current).

5 Power Stage Design

5.1 Capacitor selection

The DC link capacitor should create a stiff DC bus which provides low impedance path for high frequency currents. Major considerations in selecting capacitors were ripple current, DC bus voltage, DC bus voltage ripple and resonant frequency. For a reasonable energy storage in the DC bus, four metallized polypropylene film capacitors with a DC voltage rating of 800 V and capacitance of 30μF are connected in parallel. Several aluminum electrolytic capacitors rated at 350 V and 680μF are used in series-parallel connection. Multiple ceramic capacitors rated at DC voltage of 630V and capacitance of 47000pF are connected between $V_{\mathrm{dc+}}$ and $V_{\mathrm{dc-}}$.

5.2 Semiconductor device selection

The main switching devices in power stage should block the full input DC voltage. The switch should have high blocking voltage with low on-resistance, high-speed switching with low capacitances and fast intrinsic diode with low reverse recovery. This reference design uses six C3M0030090K discrete devices, based on C3M^{TM} Silicon Carbide (SiC) power MOSFET Technology, which increase power density and switching frequency. This MOSFET has a drain source voltage of of 900 V, continuous drain current of 73 A at 25° C and a drain-source on-state resistance of 30 $m\Omega$. The figure 6 shows the schematic of power stage circuit.

5.3 Switching frequency

The SiC MOSFETs in the power stage enables the inverter to switch at a higher frequency. This helps to reduce the size of magnetics used in the converter and increases the power density. The

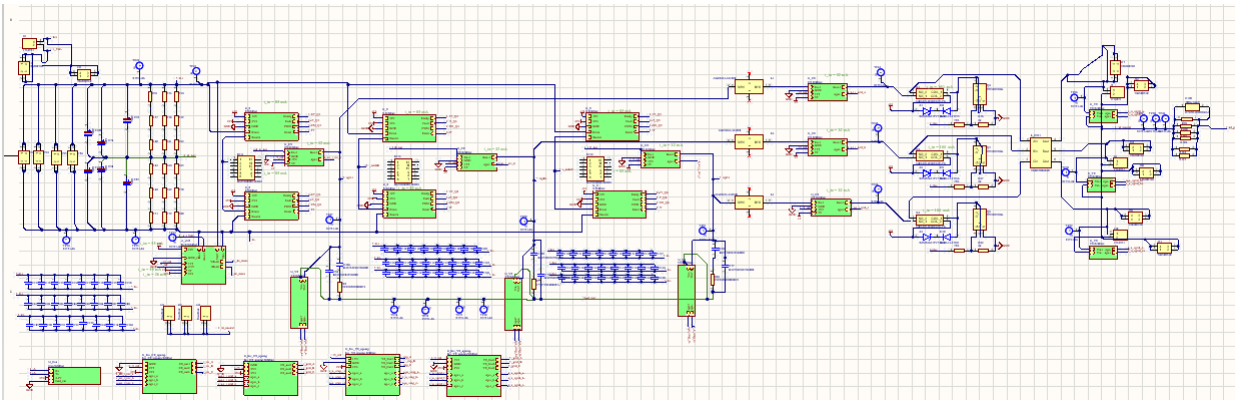

Figure 6: Power stage schematic.

switching frequency chosen for this reference design is 120 kHz. The control frequency is 20 kHz.

5.4 Gate driver design

The gate driver used in this design is the SI8285BC-ISR. It is an isolated, high current gate driver with integrated system safety and feedback functions. These devices are ideal for driving SiC power MOSFETs. The isolated bias supply selected for this gate driver is R12P21503D. This dc-dc converter is designed for high slew rate SiC transistor drivers. It has high isolation voltage and low isolation capacitance.

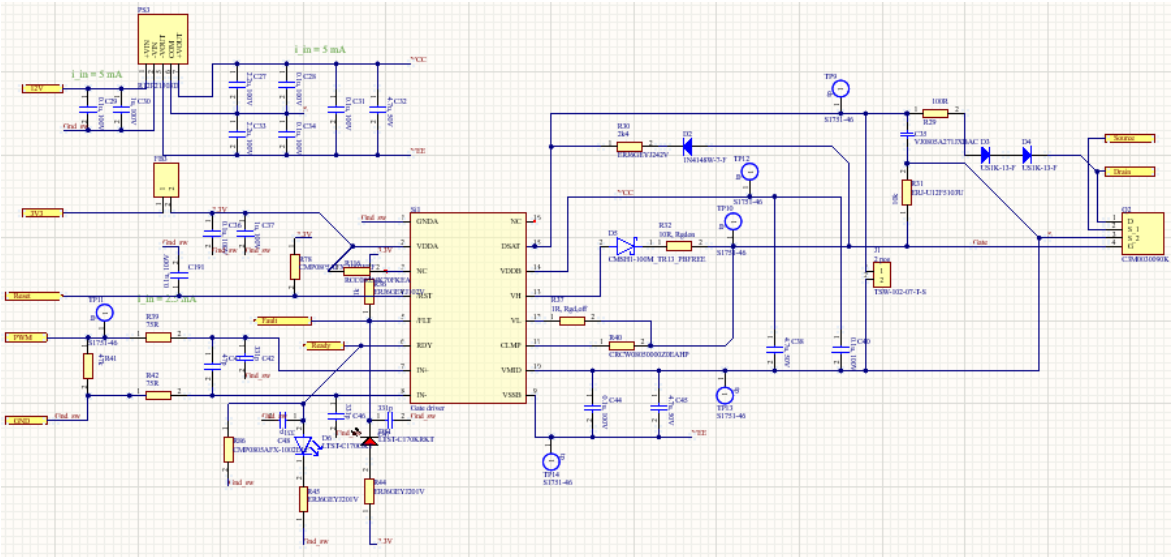

Figure 7: Gate driver schematic.

5.5 Thermal considerations

Three Wakefield Solutions OmniKlip TO-247/TO-264 (OMNI-UNI-41-75) heat sinks are used to cool the FETs. Each heat sink supports two MOSFETs. The 3M™ Thermally conductive adhesive transfer tapes (8810) are used between the FETs and the heat sinks to provide necessary insulation and a good thermal interface.

6 Sensing Circuit Design

As shown in 1, there are multiple voltage and current analog signals sensed in the reference design. These signals are

- Three inverter-side inductor currents from inverter to filter capacitor;
- Three output-side inductor currents from filter capacitor to AC output terminal;
- Three filter capacitor voltages;
- Three grid-side voltages after the relay;
- DC input current;
- DC input terminal voltage;

This section briefly discusses the input-to-output relations of the sensing circuits. Note that the inverted ones direct the ADC-related coding.

6.1 Current Sensing Circuit

Both the DC input current and six AC output current sensing circuitry share the same architecture. Neglecting the filtering circuit, the sensing circuitry is shown in Fig. 8, in which i_{sens} is the current to be sampled and v_{o} is the sensor voltage that feeds the MCU pin. TH ADC sensing relation is given by

$$v_{\text{o}} = G_{\text{i,sens}} \frac{R_2}{R_1} i_{\text{sens}} + 1.5 \text{ [V]}, \tag{1}$$

where $G_{\text{i,sens}}$ is the sensitivity of LESR15NP Hall sensor. Referring to its datasheet, it is obtained that $G_{\text{i,sens}} = 41.67\,\text{mV/A}$ for the pin connection applied in this reference design.
In six AC current sensing, the sensing resistance is given by $R_1 = R_2 = 1\,k\Omega$.
In DC current sensing, the sensing resistance is given by $R_1 = 3.3\,k\Omega,\ R_2 = 8.2\,k\Omega$.

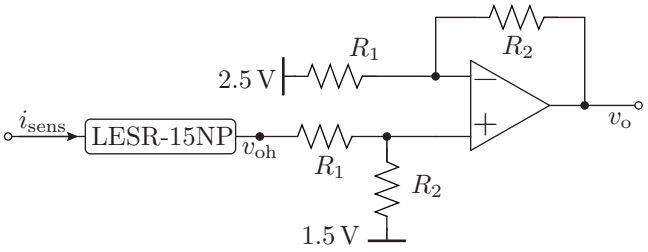

Figure 8: The sensing circuitry shared by DC and AC current sensing.

6.2 AC Voltage Sensing Circuit

Similarly, the AC voltage sensing circuitry for the six AC voltages is shown in Fig. 9. The input-to-output relation is derived as

$$v_{\text{o}} = 1.5 + \frac{R_2}{R_{\text{i}}} v_{\text{sens}} \text{ [V]}, \tag{2}$$

where $v_{\text{sens}} = v_{\text{sens}}^{+} - v_{\text{sens}}^{-}$ is the voltage to be sensed.
As shown above, there exist $R_2 = 30\,k\Omega$ and $R_{\text{i}} = 3\,\text{M}\Omega$.

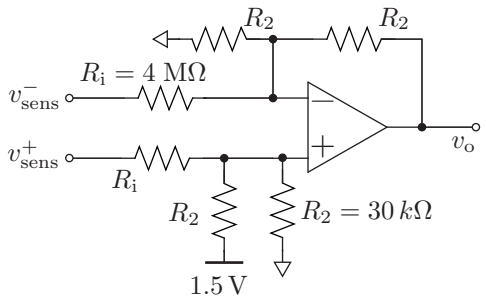

Figure 9: AC voltage sensing circuitry.

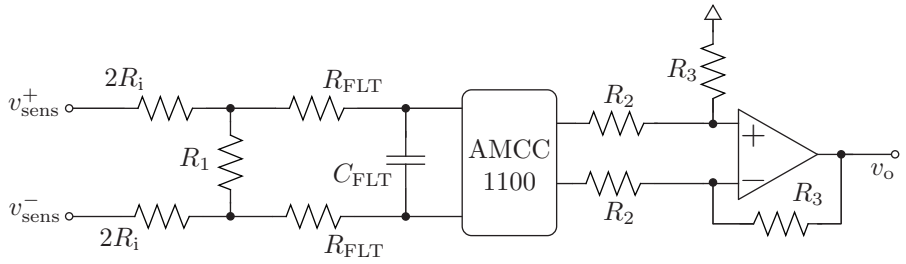

Figure 10: DC voltage sensing circuitry.

6.3 DC Voltage Sensing Circuit

The DC input voltage sensing circuitry is shown in Fig. 10. The input-to-output relation is derived as

$$v_\mathrm{o} = \frac{R_1}{4R_\mathrm{i} + R_1}\frac{R_3}{R_2}G_\mathrm{amcc}v_\mathrm{sens}\ [\mathrm{V}], \tag{3}$$

where $v_\mathrm{sens} = v^+_\mathrm{sens} - v^-_\mathrm{sens}$ is the voltage to be sensed. $G_\mathrm{amcc} = 8$ is the gain of the differential isolation amplifier AMCC1100 in the circuit. Lastly, this circuit employs $R_i = 100\,k\Omega$, $R_2 = 2\,k\Omega$, and $R_3 = 4.3\,k\Omega$.

7 Additional components

This section walks through other accessories needed to build the hardware in addition to the Bill of Materials (BOM). Users need to order the following components available with vendors like Mouser/ DigiKey/ TI.

7.0.1 MCU

This board is designed to support Texas Instrument's F28379 MCU. User must order this MCU and install Code Composer Studio™ integrated development environment (IDE).

7.0.2 MOSFET assembly

For proper thermal management of the switching devices, the user must place a thermally conductive tape (3M™ Thermally Conductive Adhesive Transfer Tape 8810) between the heatsink and the MOSFET. They must then use clips (Wakefield Solutions OmniKlip TO-247/TO-264 Heat Sinks) to hold it firmly as shown in Fig. 11.

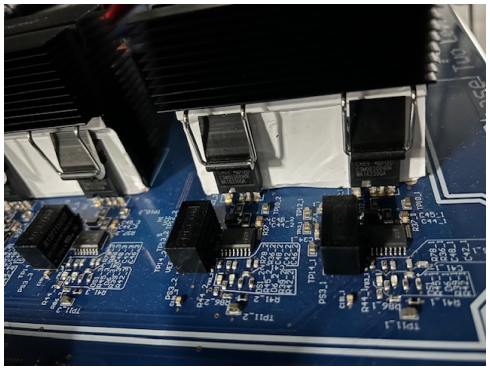

Figure 11: MOSFET and heatsink assembly reference

7.0.3 Inductor assembly

The user needs to custom build the inverter side inductance. In the schematic and PCB layout, only the bobbin footprint is created. This bobbin needs to be mechanically connected to the PCB. In order to assemble the complete inductor, components like the magnetic wires, cores, shim stock, and Kapton tape are wrapped around the bobbin.

The inductor on the inverter side on each leg is chosen to be 120 μF. The components used in the final design are listed in Tab. 5. A Kapton tape is used to hold everything in place firmly. The number of turns needed should be around 48 and can be adjusted to match the required inductance. Measure inductance and R_s using a precision LCR meter. The R_s should be around 1.3 - 1.5 Ohms at 100kHz. Minor modifications based on measurements of the LCR meter are acceptable. Custom inductors when soldered to the appropriate designators on the PCB should look like Fig. 12.

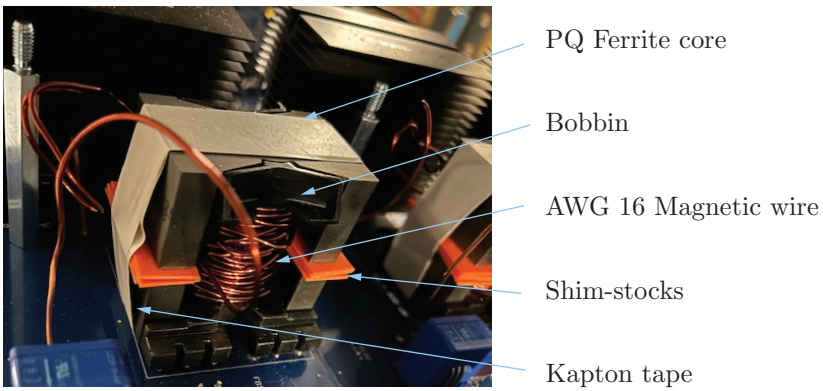

Figure 12: Custom Inductor construction.

Ferrite core set	PQ50/50-N95-DG100, Mouser part no: 871-B65981Q0100K095
Wire	AWG16 magnetic wire
Shim-stock	Coral (Qty - 4)

Table 5: Key specifications in inverter-side inductor manufacturing.

7.0.4 Standoffs

The user needs to order and assemble Hex Nuts (M5x0.8mm) and M5 Standoffs in the 9 holes provided on the PCB. To protect the components assembled on the PCB, they must make sure to stack sufficient number of standoffs above and below the PCB.

7.0.5 RF Cables

The user needs to order around 30 RF Cable Assemblies (RG174/U SMA Male/Male, 2ft). They must connect the cables at the bottom of the PCB according to the designators (Jxx) printed.

8 Software

To download the Software related files see files and documentation at GitHub - UNIFI Consortium.

9 Design Files

9.1 Schematics

To download the schematics, see the design files at GitHub - UNIFI Consortium.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at GitHub - UNIFI Consortium.

9.3 Altium Project

To download the Altium Designer® project files, see the design files at GitHub - UNIFI Consortium.

9.4 Gerber Files

To download the Gerber files, see the design files at GitHub - UNIFI Consortium.

9.5 Assembly Drawings

To download the assembly drawings, see the design files at GitHub - UNIFI Consortium.

9.6 CCS Project

To download the Code Composer Studio® files, see the design files at GitHub - UNIFI Consortium.

References

[1] Ieee standard for harmonic control in electric power systems. *IEEE Std 519-2022 (Revision of IEEE Std 519-2014)*, pages 1–31, 2022.

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[4] BC Parikshith. Integrated approach to filter design for grid connected power converters. *MSc (Engg.) thesis, Indian Institute of Science, Bangalore, India*, 2009.