UNIFI's Grid-Forming (GFM) Inverter Reference Design: A Tutorial on Modeling, Control, and Experimental Implementation of GFM Inverters

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DISCLAIMER

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List of Acronyms

UNIFI	UNiversal Interoperability for grid-Forming Inverters
dVOC	Dispatchable Virtual Oscillator Control
GFL	Grid-Following
GFM	Grid-Forming
IBR	Inverter Based Resources
PI	Proportional-Integral
PWM	Pulse-Width Modulation
SG	Synchronous Generator
VI	Virtual Impedance
VSM	Virtual Synchronous Machine

Executive Summary

The UNIFI Consortium's tutorial on grid-forming (GFM) inverters provides a comprehensive guide to the modeling, control, and experimental implementation of GFM inverters. As the integration of renewable energy accelerates, the transition from traditional grid following (GFL) to GFM inverters is crucial to ensure stable and sustainable power systems. This document outlines a reference design for three-phase and single-phase GFM inverters developed at the University of Texas at Austin. Key features of this tutorial include:

- **GFM Control Strategies**: Detailed explanations of primary grid-forming control methods such as droop control, virtual synchronous machine (VSM) control, and dispatchable virtual oscillator control (dVOC), each suited for various operational dynamics.
- **Cascaded Controller Design**: Guidance on selecting control gains for outer voltage and inner current loops based on time-scale separation to ensure efficient operation under varying grid conditions.
- **LCL Filter Design**: Methodologies for designing filters to optimize performance, reduce ripple, and ensure compatibility with inverter hardware.
- **Current Limiting Techniques**: Analysis of current-reference saturation and virtual impedance-based current limiting methods to protect inverters during faults without compromising stability.
- **Single-Phase GFM Inverter Control**: An overview of single-phase GFM inverter control, emphasizing its relevance for applications like rooftop photovoltaic systems and solid-state transformers.
- **Experimental Validation**: Demonstration of GFM inverters' robustness and interoperability under steady-state and fault conditions, supported by experimental data.

The tutorial also provides step-by-step guidance for accessing and using UNIFI's GitHub repository, enabling users to design, build, and test GFM inverters efficiently. By fostering collaboration and equipping users with accessible resources, this initiative aims to drive widespread adoption of GFM technology across academia, utilities, and industries.

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1 Introduction

Electrical power generation is shifting from centralized to decentralized systems due to growing renewable energy integration. A key challenge in this transition is replacing synchronous generators (SGs) with inverter-based generation. In systems with SGs, grid-connected inverters rely on the voltage and frequency set by the SG, acting as controlled current sources to supply active and reactive power. This operating mode, dependent on a strong voltage source, is called 'Grid-following' (GFL). However, if all synchronous machines are removed, GFL inverters cannot operate due to the lack of a voltage reference. This limitation prevents grids from being fully operated by inverter-based resources (IBR). In the absence of synchronous generation, some inverters must maintain grid voltage and frequency. These inverters, known as 'Grid-forming' (GFM) inverters, ensure stable voltage and frequency, even during load changes, generator disconnections, unbalanced grid conditions, or system faults [2, 3]. GFM inverters will be critical as renewable energy penetration increases [4, 5, 6]. The transition of our power grid from present to future is shown in Fig. 1.

To this end, the UNiversal Interoperability for grid-Forming Inverters (UNIFI) Consortium is tackling key challenges in integrating GFM inverters into the electric grid. To advance research in GFM control, this document details the control design used in UNIFI's GFM inverter reference design, available on their GitHub page.

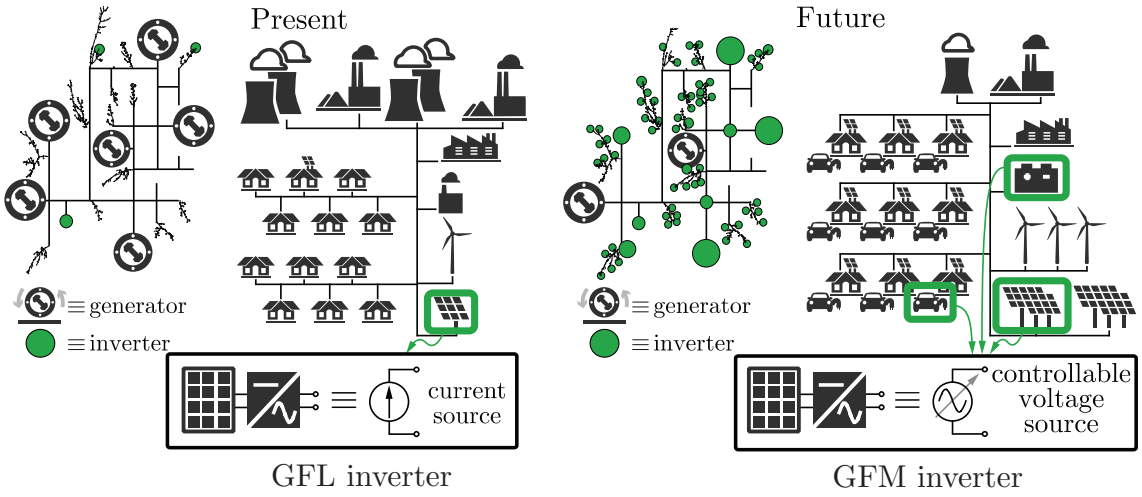

Figure 1. Transition from grid-following (GFL) to grid-forming (GFM) inverter.

Definition of GFM inverters: The North American Electric Reliability Corporation (NERC) [7] defined GFM controls as follows:

> *"GFM IBR controls maintain an internal voltage phasor that is constant or nearly constant in the sub-transient to transient time frame. This allows the IBR to immediately respond to changes in the external system and maintain IBR control stability during challenging network conditions. The voltage phasor must be controlled to maintain synchronism with other devices in the grid and must also regulate active and reactive power appropriately to support the grid."*.

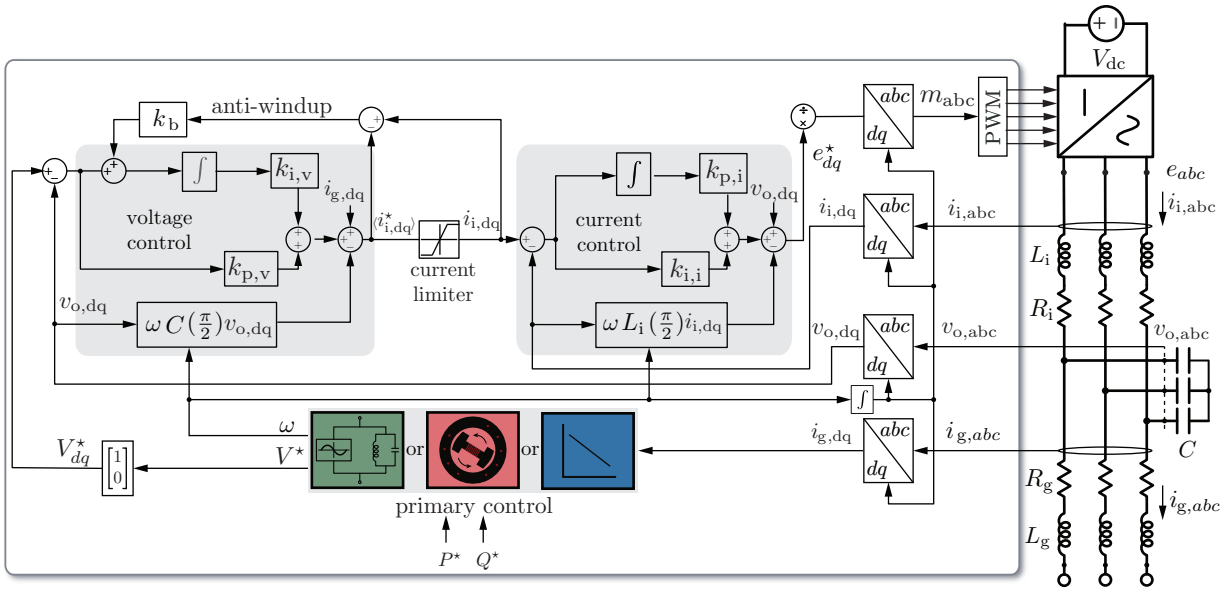

Figure 2. Cascaded grid-forming controller with primary control, outer voltage control, and inner current control.

The UNIFI consortium defines GFM IBR controls as follows in accordance with the NERC definition [2]:

> *"GFM IBR controls maintain an internal voltage phasor that is constant or nearly constant in the sub-transient to transient time frame."*

2 Grid-forming Inverter Control

The GFM inverter regulates its real and reactive power exchange with the grid by controlling the voltage and frequency at its point of connection. This can be achieved via a cascade control structure, where a primary loop determines the references (angle and magnitude of the voltage) for voltage and current control loops. These cascaded loops dictate the references for the PWM block.

The cascaded control structure of the GFM inverter with a LCL filter is shown in Fig. 2. The output LCL-filter currents and voltages are sensed and fed as inputs to these various control loops. Depending on the reference frame that is leveraged in the controls, the input measurements are first transformed using Clarke and Park transformations. We denote the reference active and reactive power set points by $P^\star$ and $Q^\star$, respectively; i_i and i_g denote the inverter- and grid-side LCL-filter currents, respectively, with the superscript indicating which reference frame is leveraged; v_o and v_g denote the LCL-filter capacitor voltage and the terminal voltage, respectively, with the superscript indicating the reference frame; L_i, R_i, L_g, and R_g denote the inductive and resistive components of the inverter- and grid-side inductive parts of the LCL filter, and C denotes the LCL-filter capacitor.

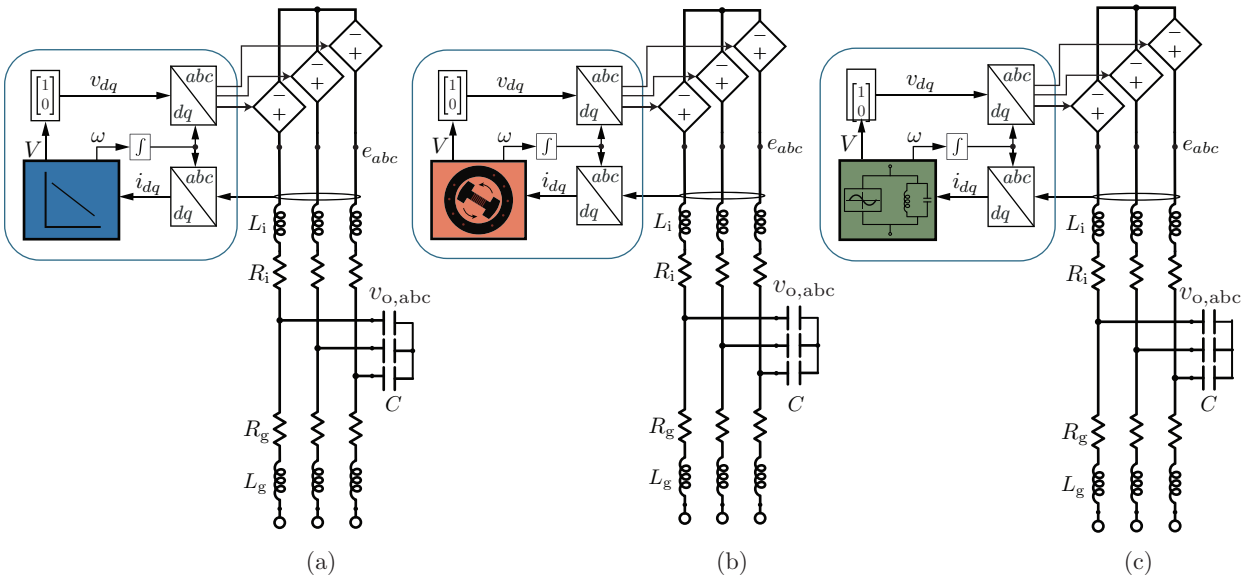

Figure 3. Primary controllers of GFM inverters: (a) droop control, (b) virtual synchronous machine (VSM) control, and dispatchable virtual oscillator control (dVOC).

2.1 Primary Control

The role of the primary control is to determine the frequency and voltage references ((ω and $V^\star$) of the GFM inverters as functions of active and reactive power, assuming that these components are decoupled. Three of these primary controllers have emerged as candidates for future large-scale adoption: droop control, virtual synchronous machine (VSM) control, and dispatchable virtual oscillator control (dVOC)[8].

2.1.1 Droop Control

In a similar manner to the operation of synchronous generators on the grid, droop control uses deviations in power output to determine the frequency and voltage set points of a GFM inverter[9]. As the power supplied by the inverter deviates from the set points, P^* and Q^*, the frequency and voltage will deviate from nominal values, ω_0 and V_0 as per the following droop laws,

$$\omega = \omega_0 - m_\mathrm{p}(P - P^*) \tag{1a}$$
$$V^\star = V_0 - n_\mathrm{q}(Q - Q^*) \tag{1b}$$

where m_p and n_q are droop gains which can be calculated as,

$$m_\mathrm{p} = \frac{\omega_\mathrm{max} - \omega_\mathrm{min}}{S_\mathrm{nom}} \quad \text{and} \quad n_\mathrm{q} = \frac{V_\mathrm{max} - V_\mathrm{min}}{S_\mathrm{nom}}, \tag{2}$$

where $(\cdot)_{\mathrm{max(or\ min)}}$ denotes the highest (or lowest) allowed value of the quantity and S_nom is the rated apparent power of the inverter [10]. If there are multiple GFM inverters with different droop gains connected in parallel, then droop characteristics ensure proportional power sharing [9]. Active power contribution of each GFM inverter can be estimated as

$$m_{\mathrm{p},1}P_1 = m_{\mathrm{p},2}P_2 = m_{\mathrm{p},3}P_3 = \ldots\ldots = m_{\mathrm{p},n}P_n, \tag{3}$$

where $m_{\mathrm{p},i}$ and P_i are droop constant and active power contribution of the i-th inverter, respectively.

2.1.2 Virtual Synchronous Machine (VSM) Control

VSM control uses the dynamics of synchronous generators to set the voltage and frequency of the GFM inverter [11]. To determine frequency, a VSM primary controller emulates the synchronous generator dynamics described by

$$M\dot{\omega} = \omega_0 - \omega + D\left(\omega_0 - \omega\right) - m_{\mathrm{p}}\left(P - P^*\right) \tag{4a}$$

$$V^* = V_0 - n_{\mathrm{q}}\left(Q - Q^*\right), \tag{4b}$$

where M and D are inertia constant and damping constant, respectively. If H is normalized inertia constant, then $M = 2HS_{\mathrm{nom}}/\omega_0$ [12].

2.1.3 Dispatchable Virtual Oscillator Control (dVOC)

Inspired by the self-synchronizing behavior of non-linear oscillators, dVOC is a control strategy where where inverters are programmed to emulate the dynamics of weakly nonlinear limit-cycle oscillators such as dead-zone and Van der Pol oscillators[13]. The dynamical equations of the dVOC are given as

$$\dot{V}^* = \mu V^*\left(V_0^2 - (V^*)^2\right) - \frac{2\eta}{3V^*}\left(Q - Q^\star\right) \tag{5a}$$

$$\dot{\theta} = \omega = \omega_0 - \frac{2\eta}{3(V^*)^2}\left(P - P^\star\right), \tag{5b}$$

where μ and η are control gains. The detailed parameters design can be referred to [14]. dVOC has received recent attention as analysis shows that it subsumes the functionality of conventional droop control in steady state while providing enhanced dynamic speed [15] due to its time-domain implementation[16].

Although these three primary controllers may exhibit different transient behaviors due to inherent dynamic differences, their steady-state performance can be aligned by adjusting the control gains. As a result, all primary controllers can be represented in a generic form during steady-state operation, as shown in [8]. Interoperability of different primary controllers is demonstrated in Section 5.

2.2 Inner Current and Outer Voltage Control

The internal control loops of the GFM inverter generate converter-switching signals that shape the IBR voltage based on the outputs of the primary control loop. Two proportional-integral (PI) controllers with proportional and integral gains $k_{\mathrm{p,i}}$, $k_{\mathrm{i,i}}$, respectively, and $k_{\mathrm{p,v}}$, $k_{\mathrm{i,v}}$, respectively, are correspondingly used to regulate i_{dq} and $v_{\mathrm{o,dq}}$, respectively. Feedforward and decoupling controls are included in the control structure. In order to prevent overcurrents, current-controller commands are limited by a saturation block and a companion anti-windup function. The integral states are

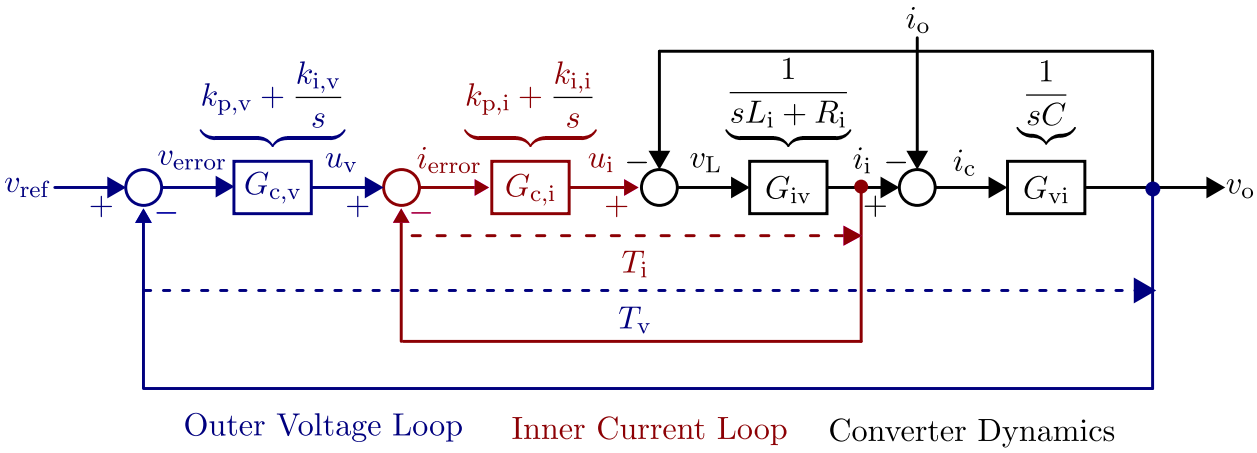

Figure 4. Control block diagram of voltage and current control loops

$\dot{\gamma}_{dq} := [\dot{\gamma}_d, \dot{\gamma}_q]^\top = [i^\star_{i,dq} - i_{i,dq}]$ and $\dot{\phi}_{dq} := \left[\dot{\phi}_d, \dot{\phi}_q\right]^\top = [v^\star_{o,dq} - v_{o,dq}]$. The equations which defines the outer voltage and inner current control loop dynamics are as follows,

$$i^\star_{i,d} = k_{p,v}\dot{\phi}_d + k_{i,v}\phi_d + i_{o,d} - \omega C v_{o,q} \tag{6a}$$

$$i^\star_{i,q} = k_{p,v}\dot{\phi}_q + k_{i,v}\phi_q + i_{o,q} + \omega C v_{o,d} \tag{6b}$$

and,

$$e^\star_d = k_{p,i}\dot{\gamma}_d + k_{i,i}\gamma_d + v_{o,d} - \omega L_f i_{i,q} \tag{7a}$$

$$e^\star_q = k_{p,i}\dot{\gamma}_q + k_{i,i}\gamma_q + v_{o,q} + \omega L_f i_{i,d} \tag{7b}$$

2.2.1 Selection of Current Control Loop Gains

Fig. 4 shows the inner current and outer voltage control loops that shape the inverter current and capacitor voltage of the GFM inverter. $G_{c,i}$ and $G_{c,v}$ are the PI compensators for the current and voltage loop, respectively. G_{iv} and G_{vi} are transfer functions that describe the plant dynamics of the current control loop and the voltage control loop, respectively. The system can be modeled as an RL circuit (inverter-side filter inductor and its resistance) in the synchronous dq reference frame. Therefore, $G_{iv} = \frac{1}{sL_i + R_i}$, where L_i and R_i are filter parameters.

The open-loop gain of the current controller, T_i, is the product of the GFM inverter's voltage to current transfer function, G_{iv}, and the current loop controller compensator, $G_{c,i}$. Hence, T_i is defined as follows:

$$T_i = G_{iv}G_{c,i} = \frac{1}{sL_i + R_i}\left(k_{p,i} + \frac{k_{i,i}}{s}\right) \tag{8}$$

From (8), rearranging $G_{c,i}$ yields

$$T_i = \frac{1}{sL_i + R_i}\frac{s\frac{k_{p,i}}{k_{i,i}} + 1}{\frac{s}{k_{i,i}}} \tag{9}$$

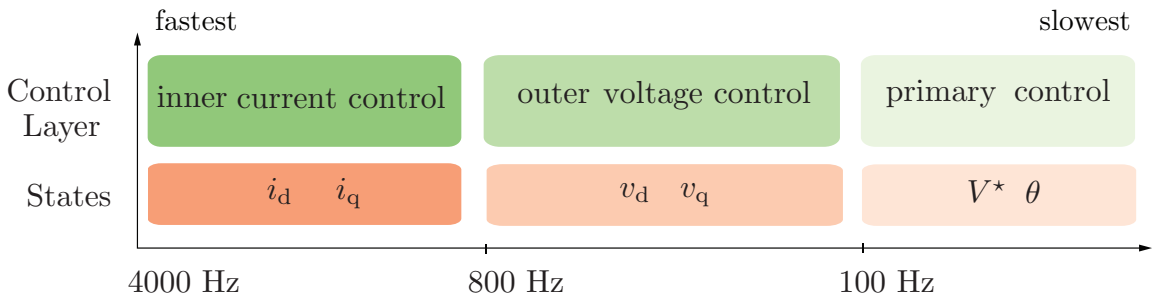

Figure 5. Timescale separation of different GFM control layers.

The closed loop gain, $\frac{T_i}{1+T_i}$, is a second order transfer function. From (9), we can write,

$$\frac{T_i}{1+T_i} = \frac{s\frac{k_{p,i}}{k_{i,i}} + 1}{s^2\frac{L_i}{k_{i,i}} + s(\frac{R_i}{k_{i,i}} + \frac{k_{p,i}}{k_{i,i}}) + 1} \tag{10}$$

Proper selection of the controller gains, k_p and k_i can lead to a pole-zero cancellation. This will reduce the order of the closed-loop transfer function and convert it to a simplified first-order transfer function as follows:

$$\frac{s\frac{k_{p,i}}{k_{i,i}} + 1}{s^2\frac{L_i}{k_{i,i}} + s(\frac{R_i}{k_{i,i}} + \frac{k_{p,i}}{k_{i,i}}) + 1} = \frac{1}{\frac{s}{\omega_i} + 1} \tag{11}$$

where ω_i is the current controller bandwidth. Cross-multiplying (11) yields the expressions of the current compensator gains which facilitate pole-zero cancelation. Therefore,

$$k_{p,i} = L_i\omega_i \quad \text{and} \quad k_{i,i} = R_i\omega_i. \tag{12}$$

where ω_i is taken to be at most a tenth of the inverter's switching frequency. Though unmodeled controller delays necessitate further reductions in ω_i. Timescale separation among different control layers is shown in Fig. 5.

2.2.2 Selection of Voltage Control Loop Gains

From Fig. 4, the open-loop gain of the voltage controller, T_v, is given as the product of the GFM inverter's current-to-voltage transfer function, G_{vi}, the voltage loop compensator, $G_{c,v}$, and the closed-loop current gain, $\frac{T_i}{1+T_i}$. Therefore, T_v can be expressed as:

$$T_v = G_{c,v}\frac{T_i}{1+T_i}G_{vi} = \left(k_{p,v} + \frac{k_{i,v}}{s}\right)\left(\frac{1}{\frac{s}{\omega_i}+1}\right)\left(\frac{1}{sC}\right), \tag{13}$$

where we define the time constants:

$$\tau_i = \frac{1}{\omega_i}, \quad \tau_{PI} = \frac{1}{\omega_{PI}} = \frac{k_{p,v}}{k_{i,v}}. \tag{14}$$

Substituting these definitions into (13), T_{v} can be rearranged as:

$$T_{\mathrm{v}} = \frac{k_{\mathrm{p,v}}}{\tau_{\mathrm{PI}} C} \frac{\tau_{\mathrm{PI}} s + 1}{\tau_{\mathrm{i}} s + 1} \frac{1}{s^2}. \tag{15}$$

Using (15), the goal of the voltage compensator, $G_{\mathrm{c,v}}$, is to maximize the phase angle of T_{v} at the crossover frequency ω_{c}, where $|T_{\mathrm{v}}(j\omega_{\mathrm{c}})| = 1$. The crossover frequency ω_{c} is selected to be sufficiently distinct from ω_{i}.
The three poles (two at dc) and the single zero in (15) suggest that the phase response has a concave shape, which implies that the phase response is maximized when:

$$\frac{d\angle T_{\mathrm{v}}}{d\omega} = 0. \tag{16}$$

Applying this condition to (15) gives the frequency at which the phase is maximized:

$$\omega = \frac{1}{\sqrt{\tau_{\mathrm{i}} \tau_{\mathrm{PI}}}}. \tag{17}$$

To ensure this maximum phase point aligns with the crossover frequency, we substitute (17) into the definition of the crossover frequency $|T_{\mathrm{v}}(j\omega_{\mathrm{c}})| = 1$, yielding:

$$\frac{k_{\mathrm{p,v}}}{C} \sqrt{\tau_{\mathrm{i}} \tau_{\mathrm{PI}}} = 1. \tag{18}$$

Solving (18) for $k_{\mathrm{p,v}}$ gives:

$$k_{\mathrm{p,v}} = C\omega_{\mathrm{c}}. \tag{19}$$

Using the definition of τ_{PI} from (14), $k_{\mathrm{i,v}}$ can then be determined as:

$$k_{\mathrm{i,v}} = \frac{C\omega_{\mathrm{c}}^3}{\omega_{\mathrm{i}}}. \tag{20}$$

The 3-Φ inverter we use in UNIFI reference design is switched at a frequency of 100 kHz. To ensure the voltage control effort signals can be realized at the switch terminals, the current control bandwidth, ω_{i} is picked as being sufficiently lower at 4 kHz. Therefore, the outer voltage control loop is even slower with an bandwidth, ω_{c} of 800 Hz. The primary controller is the slowest and the cut-off frequency of the low-pass filter in the primary controller is 100 Hz. Once the bandwidths are decided, controller gains can be calculated using the expressions shown in Table 1 [17].

Table 1. PI Controller Parameters

Symbol	Parameter	Expression
$k_{\mathrm{p,i}}$	proportional gain of current controller	$L_{\mathrm{i}}\omega_{\mathrm{i}}$
$k_{\mathrm{i,i}}$	integral gain of current controller	$R_{\mathrm{i}}\omega_{\mathrm{i}}$
$k_{\mathrm{p,v}}$	proportional gain of voltage controller	$C\omega_{\mathrm{c}}$
$k_{\mathrm{i,v}}$	integral gain of voltage controller	$C\omega_{\mathrm{c}}^3/\omega_{\mathrm{i}}$

Even though a cascade voltage-current control structure is well established in the literature, some studies aimed at increasing the bandwidth of the GFM inverter's inner control loops have examined the idea of eliminating the current/voltage control loops. In these studies, the voltage references obtained by the primary control loop are fed directly into the converter PWM generator module without incorporating current/voltage control loops, as shown in Fig. 6. The advantages and limitations of such a single loop GFM controller compared to multi-loop control are elaborated in [18].

3 LCL Filter Design

The GFM inverter is connected to the grid via LCL filter, as shown in Fig. 2. The design constraints taken into consideration in UNIFI reference design are listed as follows:

1. The resonant frequency of LCL filter is chosen to satisfy, $f_{\text{res}} = 10\% f_{\text{sw}}$
2. The maximum current ripple (defined as peak to peak) on inverter-side filter inductor is obtained from nominal value of current as $\Delta I_{\text{pp}} = 20\% \cdot I_0$.
3. The maximum voltage ripple, ΔV_{pp} is limited to 1% of the nominal voltage V_0
4. Inverter-side inductance L_{i} is chosen based on the maximum allowable ripple in the inductor current, as follows:

$$L_{\text{i}} = \frac{V_{\text{dc}}}{4 f_{\text{sw}} \Delta I_{\text{pp}}}.$$

5. Grid-side inductance L_{g} can be selected as 10% of the inverter side inductance, L_{i}
6. The maximum and minimum values of filter capacitance C_{max} and C_{min} respectively are obtained as follows:

$$C_{\text{max}} = \frac{0.05(S_{\text{nom}}/3)}{V_0^2 \omega_0} \quad \text{and} \quad C_{\text{min}} = \frac{\Delta I_{\text{pp}}}{8 f_{\text{sw}} \Delta V_{\text{pp}}},$$

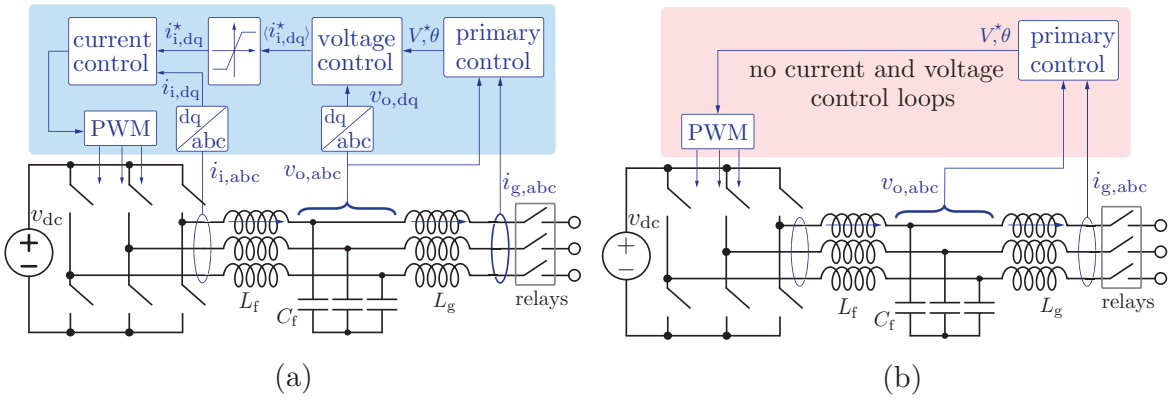

Figure 6. (a) cascaded multi-loop and (b) single-loop grid-forming controller.

Table 2. Dynamic and algebraic system equations of a GFM inverter with LCL filter

	System dynamics
Droop	$\omega = \omega_0 - m_\mathrm{p}\left(P - P^*\right)$ $V^* = V_0 - n_\mathrm{q}\left(Q - Q^*\right)$
VSM	$M\dot{\omega} = \omega_0 - \omega + D\left(\omega_0 - \omega\right) - m_\mathrm{p}\left(P - P^*\right)$ $V^* = V_0 - n_\mathrm{q}\left(Q - Q^*\right)$
dVOC	$\dot{V}^* = \mu V^*\left(V_0^2 - (V^*)^2\right) - \frac{2\eta}{3V^*}\left(Q - Q^\star\right)$ $\dot{\theta} = \omega = \omega_0 - \frac{2\eta}{3(V^*)^2}\left(P - P^\star\right)$
Voltage controller	$i^\star_\mathrm{i,d} = k_\mathrm{p,v}\dot{\phi}_\mathrm{d} + k_\mathrm{i,v}\phi_\mathrm{d} + i_\mathrm{o,d} - \omega C v_\mathrm{o,q}$ $i^\star_\mathrm{i,q} = k_\mathrm{p,v}\dot{\phi}_\mathrm{q} + k_\mathrm{i,v}\phi_\mathrm{q} + i_\mathrm{o,q} + \omega C v_\mathrm{o,d}$
Current controller	$e^\star_\mathrm{d} = k_\mathrm{p,i}\dot{\gamma}_\mathrm{d} + k_\mathrm{i,i}\gamma_\mathrm{d} + v_\mathrm{o,d} - \omega L_\mathrm{f} i_\mathrm{i,q}$ $e^\star_\mathrm{q} = k_\mathrm{p,i}\dot{\gamma}_\mathrm{q} + k_\mathrm{i,i}\gamma_\mathrm{q} + v_\mathrm{o,q} + \omega L_\mathrm{f} i_\mathrm{i,d}$
Line dynamics (LCL filter)	$\begin{bmatrix}\dot{i}_\mathrm{d}\\ \dot{i}_\mathrm{q}\end{bmatrix} = \begin{bmatrix}-\frac{R_\mathrm{i}}{L_\mathrm{i}} & \omega\\ -\omega & -\frac{R_\mathrm{i}}{L_\mathrm{i}}\end{bmatrix}\begin{bmatrix}i_\mathrm{d}\\ i_\mathrm{q}\end{bmatrix} + \frac{1}{L_\mathrm{i}}\begin{bmatrix}v_\mathrm{d} - v_\mathrm{o,d}\\ v_\mathrm{q} - v_\mathrm{o,q}\end{bmatrix}$ $\begin{bmatrix}\dot{i}_\mathrm{o,d}\\ \dot{i}_\mathrm{o,q}\end{bmatrix} = \begin{bmatrix}-\frac{R_\mathrm{g}}{L_\mathrm{g}} & \omega\\ -\omega & -\frac{R_\mathrm{g}}{L_\mathrm{g}}\end{bmatrix}\begin{bmatrix}i_\mathrm{o,d}\\ i_\mathrm{o,q}\end{bmatrix} + \frac{1}{L_\mathrm{g}}\begin{bmatrix}v_\mathrm{o,d} - e_\mathrm{d}\\ v_\mathrm{o,q} - e_\mathrm{q}\end{bmatrix}$ $\begin{bmatrix}\dot{v}_\mathrm{o,d}\\ \dot{v}_\mathrm{o,q}\end{bmatrix} = \begin{bmatrix}0 & \omega\\ -\omega & 0\end{bmatrix}\begin{bmatrix}\dot{v}_\mathrm{o,d}\\ \dot{v}_\mathrm{o,q}\end{bmatrix} + \frac{1}{C}\begin{bmatrix}i_\mathrm{d} - i_\mathrm{o,d}\\ i_\mathrm{q} - i_\mathrm{o,q}\end{bmatrix}$

where C_max is decided based on maximum allowable reactive power injection by the filter capacitor and C_min is limited by the maximum permissible ripple in capacitor voltage.

7. The value of filter capacitance C is found using the value of f_res, L_i, and L_g as follows,

$$C = \frac{1}{\omega_\mathrm{res}^2 L_\mathrm{eqv}},$$

where $L_\mathrm{eqv} = \frac{L_i L_g}{L_i + L_g}$.

8. Damping resistance, R_d is taken equal to the characteristic impedance of the LCL circuit.

Considering all the above constraints, the LCL filter parameters are listed in Table 3.

4 Single-phase GFM Inverter Control

This document primarily addresses the control design of three-phase grid-forming (GFM) inverters. While three-phase inverters are more prevalent, single-phase GFM inverters are increasingly

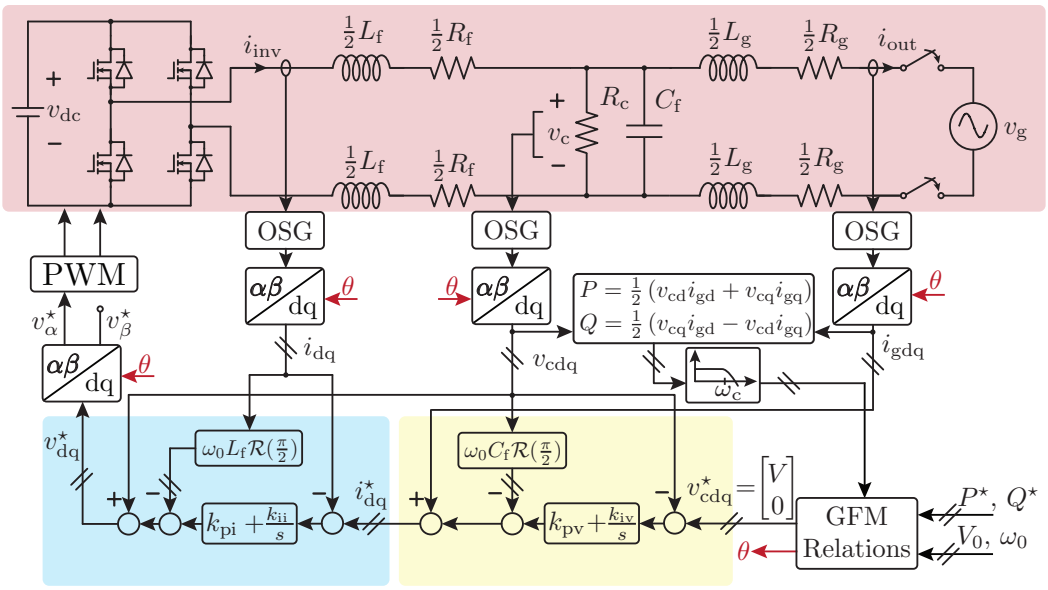

Figure 7. Architecture of a standard grid-forming controller for a single-phase inverter, featuring cascaded voltage and current control loops.

significant in modern power systems, particularly in applications such as rooftop photovoltaic systems and single-phase solid-state transformers. This section briefly explains the control design of single-phase GFM inverters.

Figure 7 depicts the architecture of a generic GFM controller for a single-phase inverter equipped with an LCL filter. Similar to the three-phase controller, the single-phase GFM controller comprises three control loops: an innermost current control loop, a capacitor voltage control loop, and an outermost primary GFM control loop, which provides the reference for the voltage controller. However, as conveyed in Fig. 8, the control of a single-phase inverter in the dq-frame requires the synthesis of orthogonal components, , followed by the $\alpha\beta$ to dq transformation. Common methods for generating orthogonal signals include second-order generalized integrators (SOGI) [19, 20], and Hilbert transformations [21, 22], among others. Once all signals are transformed to dq-frame, cascaded controllers as explained in Section 2.2 can be applied for single-phase inverters.

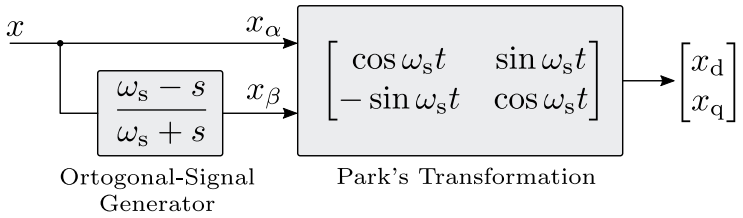

Figure 8. Conversion of a single-phase signal in natural reference frame to synchronous reference frame using an orthogonal signal generator and Park transformation, where ω_s denotes the system frequency.

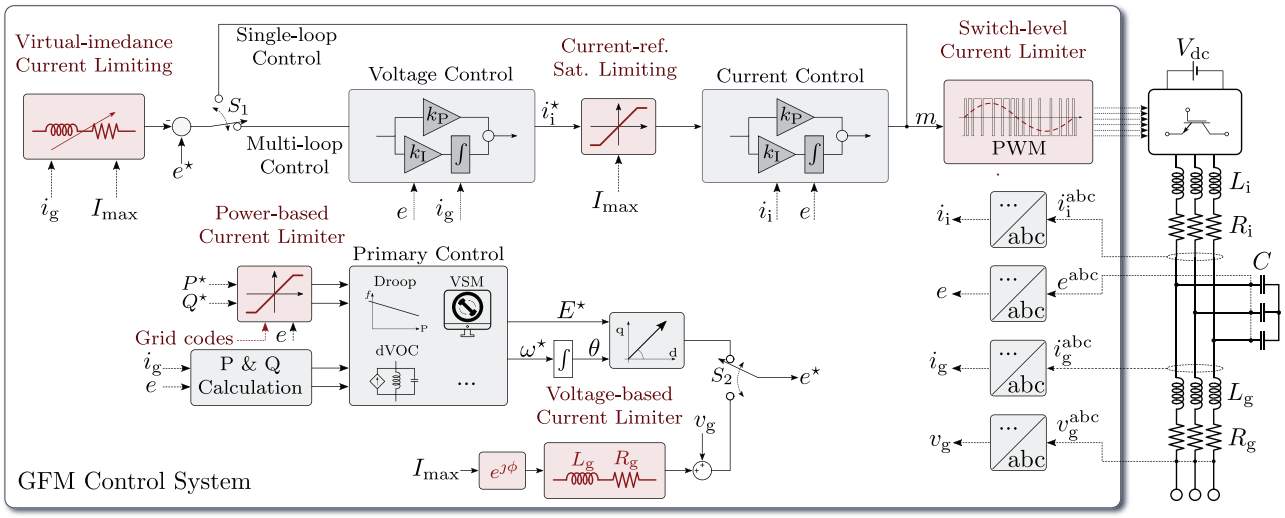

Figure 9. Overview of direct and indirect current-limiting methods for GFM inverters [1].

5 Current Limiters of GFM Inverters

Despite significant interest in GFM inverters, GFM control dynamics during off-nominal and contingency conditions pose several challenges. Synchronous generators can deliver 5–10× their rated current for a certain period of time without damage. However, power electronics switches in an inverter can only tolerate overcurrents marginally exceeding the nominal value. Therefore, different direct and indirect current limiters are used to protect the inverter hardware from thermal breakdown during excessive overcurrents, as shown in Fig. 9. Detailed descriptions of different current limiters and their system-level impact can be found in [1].

In UNIFI reference design, the two most common current limiters: current reference saturator and virtual impedance-based limiters are implemented to curtail inverter currents during faults.

5.1 Current-Reference Saturation Limiting

Current-reference signal, $i_i^\star$—which is generated by an outer control loop, such as the voltage controller—is being saturated to limit the output current during disturbances. The saturation gain, ρ, dynamically scales the current-reference signal, $i_i^\star$, according to:

$$\rho = \begin{cases} 1 & \text{if } |i_i^\star| < I_{max} \\ \dfrac{I_{max}}{|i_i^\star|} & \text{if } |i_i^\star| > I_{max}, \end{cases} \tag{21}$$

where $|i_i^\star|$ denotes the magnitude of the reference current.

5.2 Virtual-Impedance (VI) Current Limiting

A VI current limiter curtails the current by increasing the inverter output impedance. By redirecting the sensed output current through a VI and subtracting the VI voltage drop from the voltage-

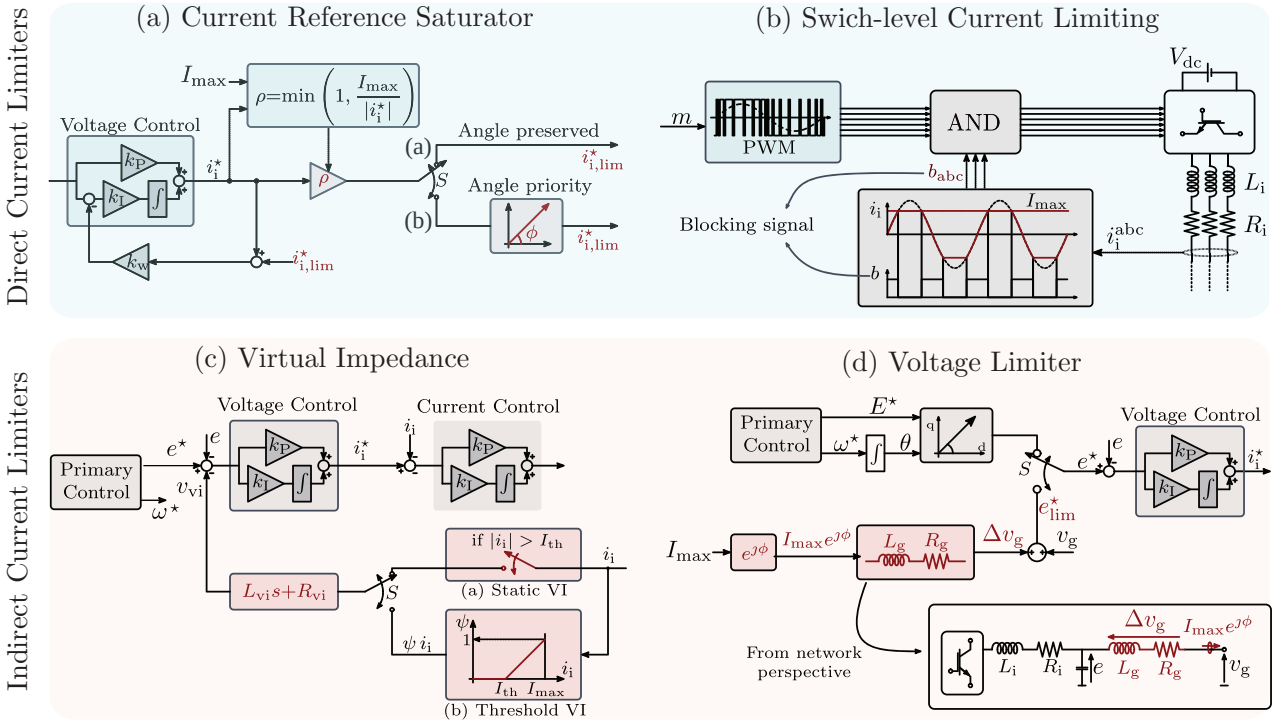

Figure 10. Detailed representation of common direct ((a) and (b)) and indirect ((c) and (d)) current limiters [1].

reference signal, current limiting can be achieved [23].

This current limiter can be implemented as a static VI or threshold VI. Static VI can lead to latch-up and under-utilization of inverter currents. For the threshold VI limiter, the VI voltage drop, v_{vi}, can be described by:

$$v_{\text{vi}} = (sL_{\text{vi}} + R_{\text{vi}})\, i_{\text{i}} \psi, \tag{22}$$

where L_{vi} and R_{vi} denote the inductive and resistive parts of the VI, respectively. As illustrated in Fig. 10(b), the threshold function, ψ, can be defined by:

$$\psi = \begin{cases} 0 & \text{if } |i_{\text{i}}| \leq I_{\text{th}} \\ \dfrac{|i_{\text{i}}| - I_{\text{th}}}{I_{\text{max}} - I_{\text{th}}} & \text{if } |i_{\text{i}}| > I_{\text{th}}. \end{cases} \tag{23}$$

Note that, compared to direct current-limiting methods that modulate the current reference, VI current-limiting methods modulate the voltage reference, thereby preventing the voltage controller from commanding an excessive inverter output current. The most common direct and indirect current limiters are shown in Fig. 10.

The design of current limiters is a delicate exercise in balancing multiple objectives. On the one hand, limiters must act quickly to protect inverter hardware from thermal damage. On the other hand, they need to maintain grid stability and facilitate post-fault recovery. This dual purpose often results in trade-offs that require careful consideration. Recent advances point toward hybrid current

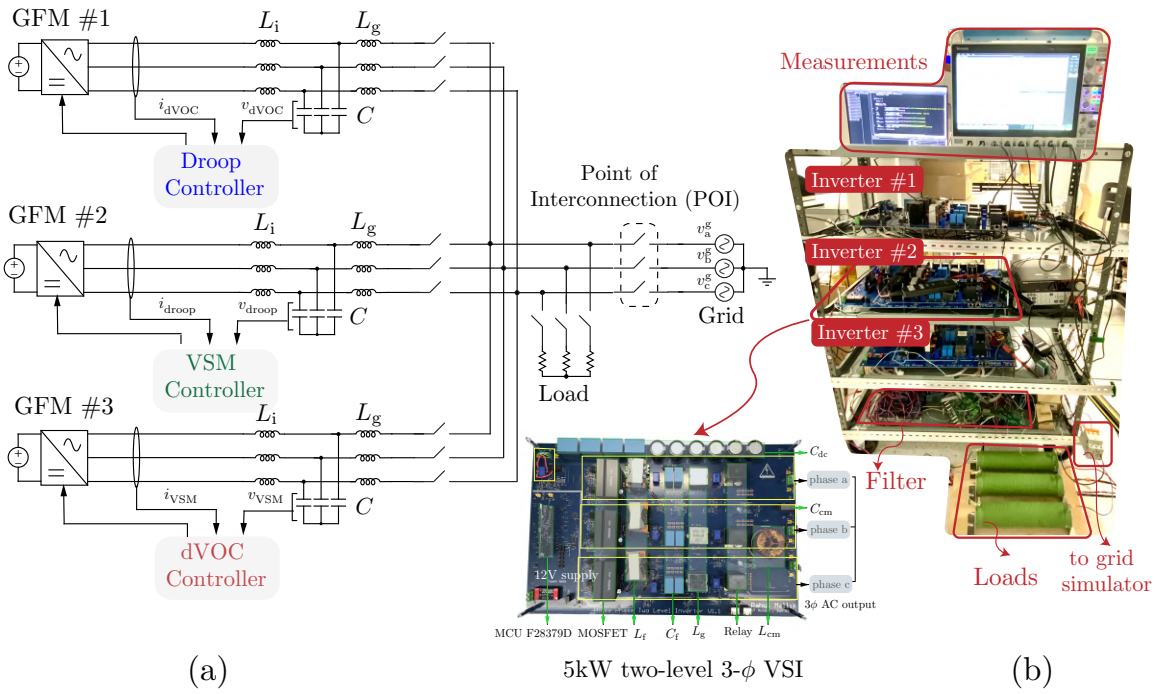

Figure 11. Three GFM inverters with different primary controllers are connected in parallel, as shown in (a). Hardware test setup is shown in (b).

limiters as a promising solution. By combining the strengths of direct and indirect approaches, hybrid limiters can offer fast fault response alongside improved stability and synchronization. For example, integrating a fast-acting direct limiter for immediate protection with a virtual impedance mechanism for transient stability ensures a balanced approach to current limiting.

6 Results and Discussions

In this section, we evaluate the performance of GFM inverters when subjected to diverse scenarios, including grid-connected and islanded operations, as well as fault conditions. The insights gained from these results highlight the effectiveness of control strategies, current-limiting mechanisms, and hardware design principles discussed in earlier sections.

6.1 Operation of GFM Inverters Under Steady-State

As discussed in Section 2, the control gains of different primary GFM controllers can be tuned to achieve identical steady-state performance. To demonstrate this, an experimental test setup is constructed, as shown in Fig. 11, where three identical GFM inverters are digitally programmed with droop, VSM, and dVOC controllers, and connected in parallel.

Table 3 lists some of the critical design specifications of the 5000 W/208 V three-phase grid-forming (GFM) inverter. The inverter output terminal is connected (via an LCL filter) to a resistive load bank and a grid simulator such that both islanded and grid-connected experiments can be performed.

Table 3. Key System Specifications

Symbol	Parameter	Value	Unit
S_{nom}	Power rating	5000	VA
V_{dc}	Input DC voltage	400	V
V_0	Nominal AC voltage (RMS)	208	V
I_0	Nominal AC current (RMS)	13.87	A
ω_0	Nominal angular frequency	$2\pi 60$	rad/s
f_{sw}	Switching frequency	100	kHz
f_{ctrl}	Control frequency	20	kHz
L_{i}	Filter inductance	300	μH
L_{g}	Output inductance	30	μH
R_{i}	Filter resistance	0.1	Ω
R_{g}	Output resistance	0.1	Ω
C	Equivalent filter capacitance	7	μF
R_{d}	Damping resistance	5	Ω

In grid-connected mode, the three inverters are energized sequentially, following a presynchronization procedure before being connected to the grid. Figure 12 shows that the steady-state terminal voltages of the three parallel inverters synchronize with each other and, in grid-connected mode, align with the grid voltage. During this mode, both the grid and inverters supply power to the load, with each inverter injecting current to track its respective power reference. The system remains stable with a mix of GFM inverters in grid-connected mode, successfully demonstrating their interoperability.

When the grid is disconnected by opening the circuit breaker at the point of interconnection, the system transitions to islanded mode. Figure 12 shows that in islanded mode, the inverter terminal voltages remain synchronized. However, the inverter currents adjust to meet the load demand, being equally shared among the three inverters, as evident by the nearly identical current levels. Thus successful demonstration of interoperability extends to islanded mode, where even without a stiff grid, the GFM inverters with different primary controllers maintain stable operation.

6.2 Operation of GFM Inverters Under Faults

As explained in Section 4, inverters are typically unable to sustain more than 1.5 times their nominal current. To protect inverters under overcurrent conditions, various current limiters are employed. However, these current limiters can negatively affect transient stability, post-fault recovery, and grid re-synchronization [1]. In the test system shown in Fig. 13, a droop-controlled GFM inverter with virtual impedance-based current limiters is used to successfully demonstrate fault ride-through capability. A similar procedure shown in [4] is used to decide virtual impedance parameters.

Figure 14(a) illustrates the voltage and current waveforms during a 65% undervoltage fault. When the current limiter activates, the inverter current is limited to the maximum allowable value, I_{max}, during the fault. After the fault is cleared, the GFM inverter successfully re-synchronizes with the

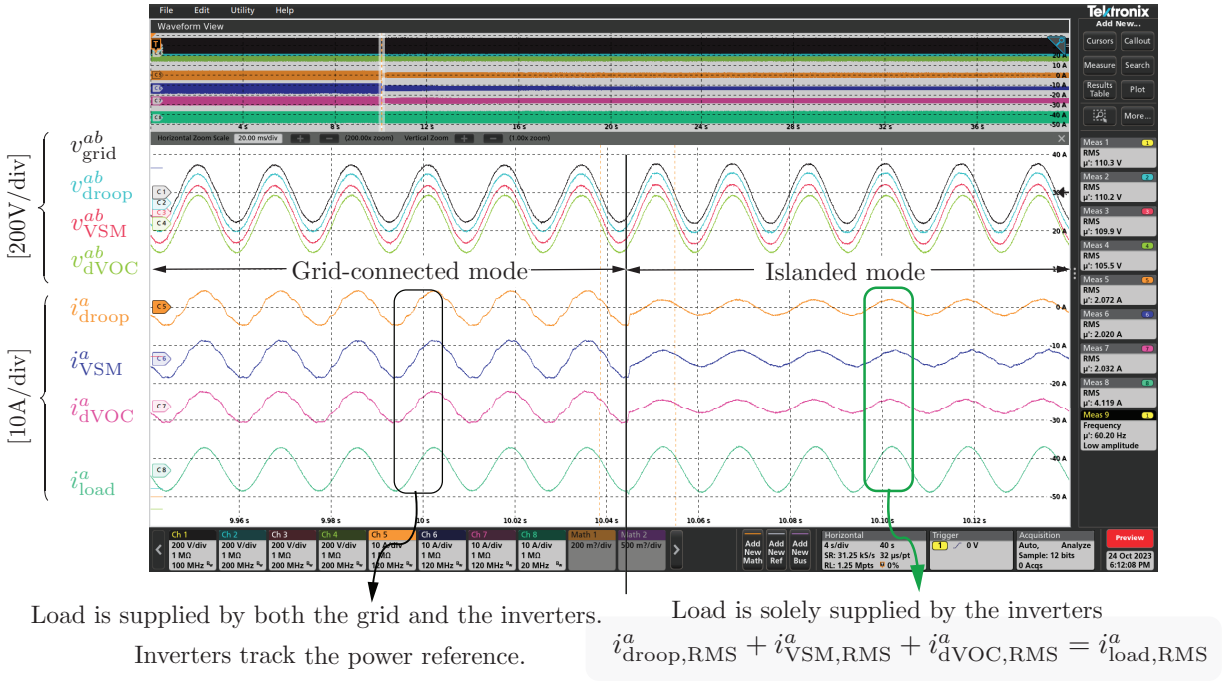

Figure 12. Interoperability of parallel-connected GFM inverters in islanded and grid-connected mode.

grid and returns to its pre-fault nominal state. The phases of fault onset and recovery during the undervoltage fault are captured in Fig. 14(c) and (e).

Similarly, Fig. 14(b), (d), and (f) depict the system response to a phase jump fault, where phase-A of the grid simulator experiences a 60° phase jump. These results underscore the effectiveness of virtual impedance-based current limiters under balanced undervoltage and phase-jump faults.

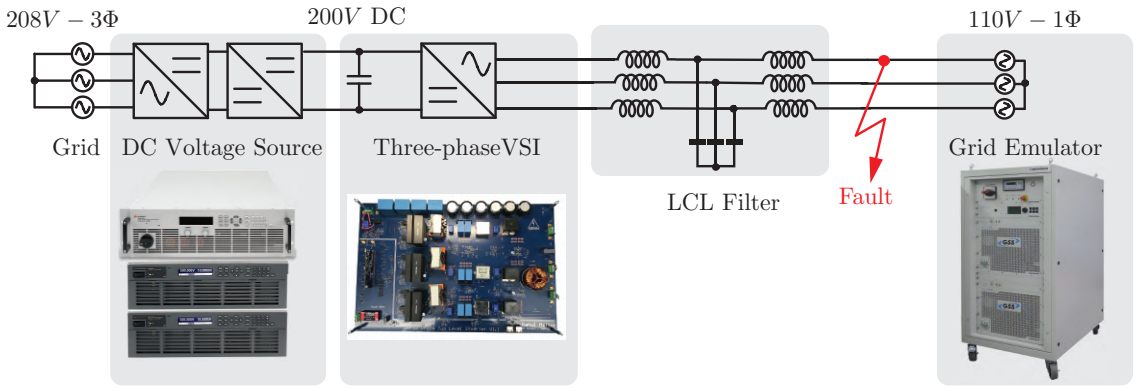

Figure 13. Experimental setup to perform fault ride-through experiments of GFM inverters.

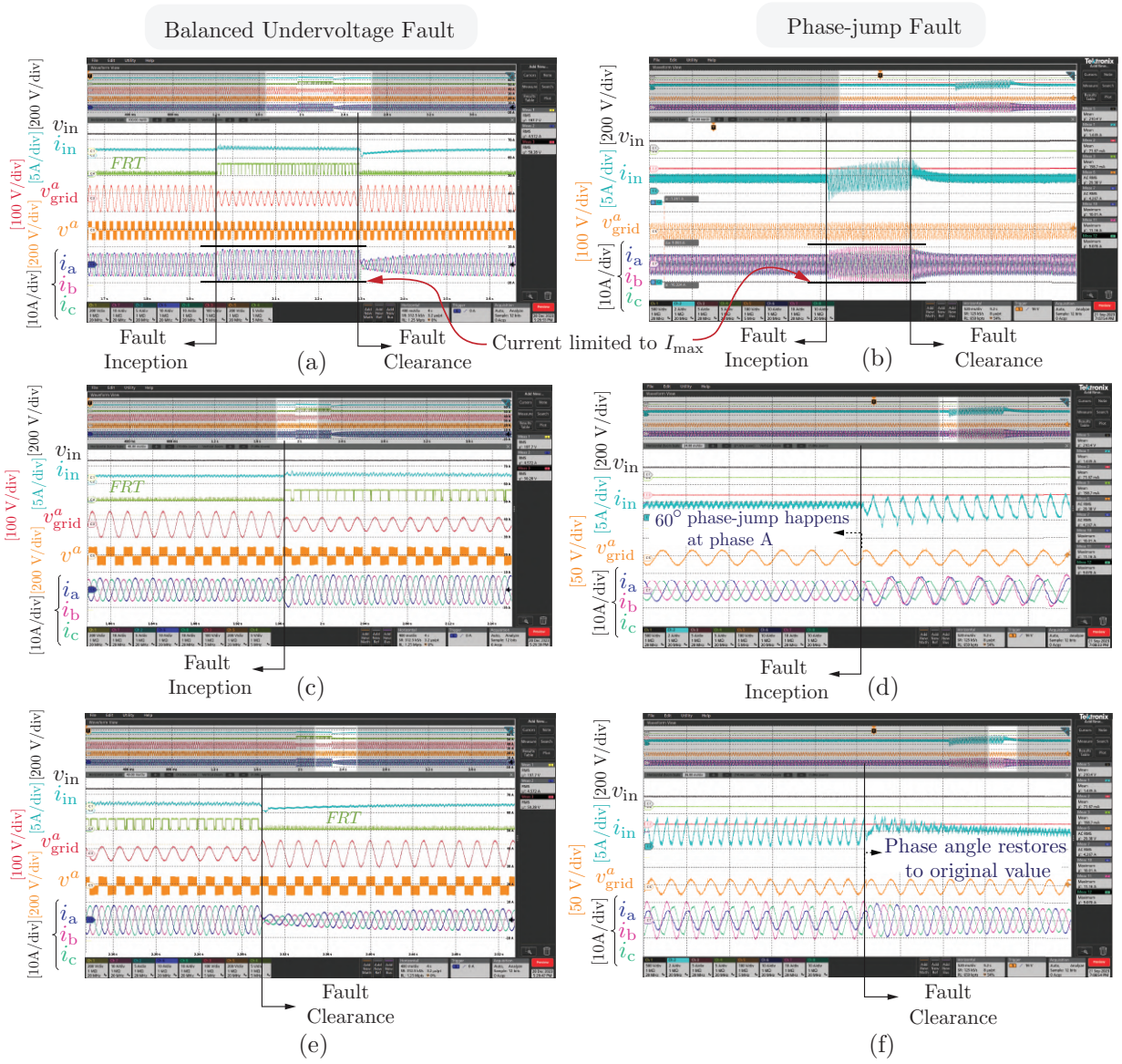

Figure 14. The successful demonstration of (a) balanced undervoltage and (b) phase jump fault ride-through of the GFM inverter with a virtual impedance-based current limiter is shown. Fault inception phases are zoomed in on Figures (c) and (d), while fault clearance phases are zoomed in on Figures (e) and (f) to clearly capture the transitions from pre-fault to fault and from fault to post-fault conditions.

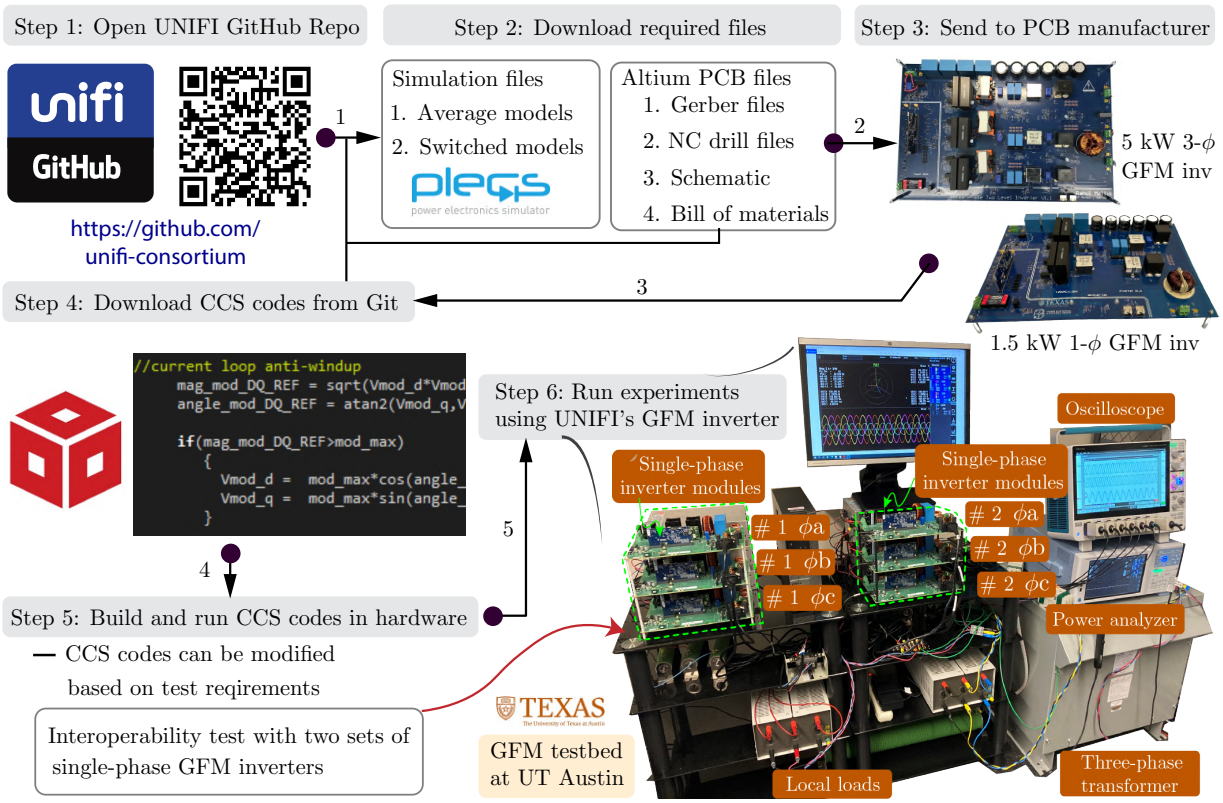

Figure 15. Workflow from accessing the UNIFI GitHub page to successfully conducting experiments with UNIFI's reference GFM hardware.

7 Guidance for External Users: How to Use the UNIFI GitHub Repository?

The various materials comprising the reference designs for both single-phase and three-phase GFM inverters have been uploaded to two GitHub repositories on the UNIFI GitHub page. In addition to this control design document, each repository contains a hardware design document, PLECS simulation files, Altium PCB files, and Code Composer Studio code files.

Figure 15 illustrates the step-by-step workflow for accessing, building, and testing UNIFI's reference GFM inverter hardware. The process begins by navigating to the UNIFI GitHub repository, accessible via the provided link or QR code (Step 1). Users then download the necessary design files, such as Gerber files, NC drill files, schematics, and the bill of materials (BOM) (Step 2). These files are sent to a PCB manufacturer to fabricate the hardware (Step 3). Subsequently, users download the control codes from the GitHub repository (Step 4), which can be modified based on specific testing requirements. Control codes are written on Texas Instruments' Code Composer Studio (CCS) platform and finally executed on a TI-TMS320F28379D microcontroller for experimentation (Step 5).

The goal of these reference designs is to equip users with limited experience in GFM inverters with

the tools and resources needed to design, build, operate, and test their own GFM inverters. This initiative fosters collaboration within the GFM community, promoting widespread adoption across industries, utilities, and academia, supported by the resources and guidance available through the UNIFI GitHub repository.

8 Conclusion

In conclusion, this document provides a detailed tutorial on grid-forming (GFM) inverter reference designs developed by the UNIFI consortium. It covers essential aspects such as GFM control strategies, LCL filter design, current-limiting methods, and step-by-step guidance for users to access, build, and test these designs via the UNIFI GitHub repository. The document demonstrates the robustness and interoperability of GFM inverters under various conditions, including steady-state operation, fault scenarios, and grid transitions, supported by experimental results. By equipping users with comprehensive resources and fostering collaboration within the GFM community, this initiative aims to advance the integration of renewable energy resources, promoting reliable and sustainable power systems for the future.

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