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## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

### General Description

The MAX96792A converts dual GMSL™ 3/2 serial inputs to MIPI CSI-2. It receives forward-channel video data, and simultaneously receives and transmits bidirectional control channel data over Coaxial or Shielded-Twisted Pair (STP) cables. The PAM-4 based GMSL3 serial link operates at 12Gbps in the forward direction and 187.5Mbps in reverse direction. The MAX96792A is backward compatible with GMSL2 and can be paired with 6Gbps or 3Gbps GMSL2 serializers. The GMSL inputs operate independently, allowing video with different timing and resolution to be received on each input. The two GMSL links can also have different data rates. Video data from both inputs can be aggregated for output on a single CSI-2 port and can be replicated on a second output port for redundant processing. The device is configured using an I<sup>2</sup>C or UART interface. GPIO, I<sup>2</sup>C, UART, and SPI tunnels are available.

The device is AEC-Q100 qualified.

Data can be transmitted over low-cost 50Ω Coax or 100Ω STP cables that meet the GMSL3 or GMSL2 channel specification. See **Table 1** for typical maximum cable lengths. Contact the factory for the GMSL3 or GMSL2 channel specifications.

**Table 1. Typical Maximum Cable Length vs. Attenuation**

	3.2mm Ø 50Ω Coax, Foam Dielectric	2.7mm Ø 50Ω Coax, Solid Dielectric	100Ω Shielded Twisted Pair, AWG26
<b>Attenuation at 3GHz (Typ, Room Temp)</b>	0.9dB/m	1.6dB/m	1.8dB/m
<b>Attenuation at 3GHz (Max, Aged, +105°C)</b>	1.1dB/m	2.0dB/m	2.2dB/m
<b>GMSL Fwd/Rev Data Rate</b>	<b>Typical Maximum Cable Length at +105°C</b>		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m
12Gbps/187.5Mbps	14m	8m	7m

### Applications

- Advanced Driver Assistance Systems (ADAS)
- 8MP ~ 15MP Forward-Vision Camera (FVC) Systems
- Aggregated Camera Data Forwarding
- eMirror Camera Systems

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[Ordering Information](#) appears at end of data sheet.

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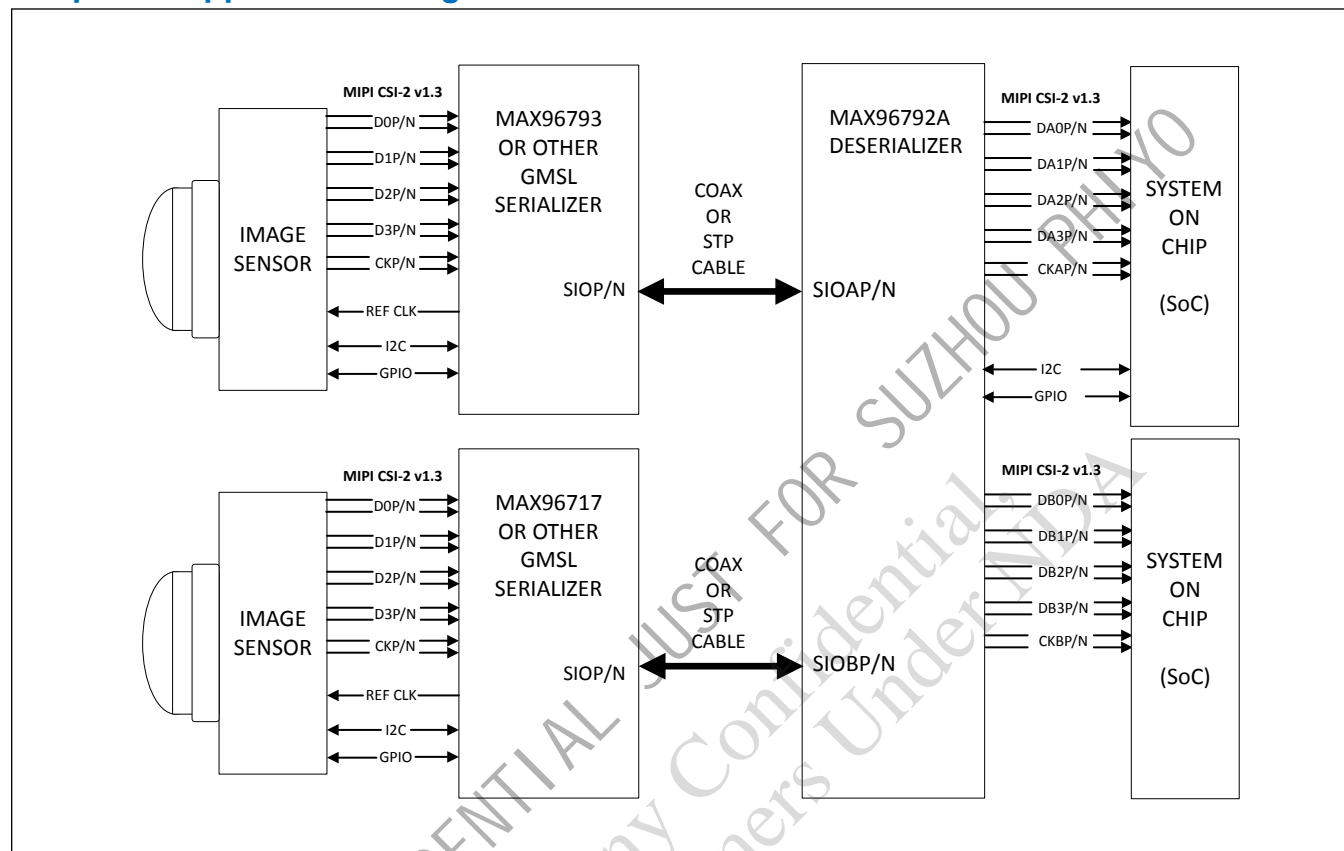
### Benefits and Features

- Automotive Grade High-Speed Link
  - -18db at 3GHz (12Gbps) Maximum Insertion Loss
  - Auto Adapt for Changes in Channel Conditions
  - Operates -40°C to +105°C Ambient
- Two MIPI CSI-2 v1.3 Output Ports
  - 2 x 4-Lane D-PHY v1.2 Rated at 2.5Gbps/Lane
  - 2 x 2-Lane C-PHY v1.0 Rated at 4.57Gbps/Lane
  - Supports 16 Virtual Channels
- Dual GMSL3 Inputs
  - 12Gbps GMSL3 Forward-Link Rate
  - GMSL2 Backward-Compatible 6Gbps/3Gbps Link Rates
  - 187.5Mbps Reverse-Link Rate
- Supports Tunneling and Pixel-Mode Video Transport
- Bidirectional Control-Channel Supports
  - 11 Configurable GPIO
  - 1 x I<sup>2</sup>C/UART Port up to 1MHz
  - 2x Pass-Through Ports
    - Up to 2M Baud as UART
    - Up to 1Mbps as I<sup>2</sup>C
  - 1x SPI Port, up to 25MHz
- Reduces BOM and Space Savings
  - 48-Pin 7mm x 7mm Side-Wettable TQFN
  - Reference-over-Reverse (RoR) Channel Clocking for Crystal-Free Operation on Serializers
  - Industry's Smallest Power-over-Coax (PoC)
- Safety-Ready
  - ASIL-B Compliant

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

### Simplified Applications Diagram



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

## TABLE OF CONTENTS

General Description . . . . .	1
Applications . . . . .	1
Benefits and Features . . . . .	1
Simplified Applications Diagram . . . . .	2
Absolute Maximum Ratings . . . . .	10
Package Information . . . . .	10
48-Pin TQFN-SW . . . . .	10
Electrical Characteristics . . . . .	11
Typical Operating Characteristics . . . . .	21
Pin Configuration . . . . .	22
MAX96792A . . . . .	22
Pin Descriptions . . . . .	22
Functional Block Diagram . . . . .	27
Configuration Pin Connections . . . . .	27
Block Diagram . . . . .	27
Detailed Description . . . . .	28
Additional Documentation . . . . .	28
Recommended Operating Conditions . . . . .	28
ESD Protection . . . . .	28
External Component Requirements . . . . .	29
Figures . . . . .	31
Introduction . . . . .	39
Product Overview . . . . .	40
GMSL3 Overview . . . . .	41
Link Error Generator . . . . .	42
Video Pipeline in Pixel Mode . . . . .	42
Watermarking . . . . .	42
Video (Data) Line CRC . . . . .	42
Vertical and Data Enable or Data Valid Sync Outputs . . . . .	43
Control-Channel and Side Channels . . . . .	43
Main I <sup>2</sup> C/UART . . . . .	43
I <sup>2</sup> C/UART CRC and Message Counter . . . . .	43
Pass-Through I <sup>2</sup> C/UART . . . . .	43
Serial Peripheral Interface (SPI) . . . . .	44
General Purpose Input and Output (GPIO) . . . . .	44
Delay in Non-Delay-Compensated Mode . . . . .	45
Delay-Compensated Mode . . . . .	45
Frame-Sync . . . . .	45
Control-Channel Retransmission on Error . . . . .	45

## TABLE OF CONTENTS (CONTINUED)

Automatic Repeat Request/Automatic Retransmission (ARQ) . . . . .	45
Other Functions . . . . .	45
Tunneling and Pixel Modes . . . . .	46
Forward-Error Correction (FEC) . . . . .	47
Functional Safety Features . . . . .	47
GMSL3 Physical Layer . . . . .	48
Cabling Options . . . . .	48
GMSL3 Bandwidth Sharing . . . . .	48
GMSL3 Bandwidth Calculations . . . . .	48
Eye-Opening Monitor . . . . .	49
Line-Fault . . . . .	50
Coax Mode . . . . .	50
STP Mode . . . . .	51
Adaptive Equalization (AEQ) . . . . .	52
Video Pipes . . . . .	52
Video-Timing Generator . . . . .	54
RGB888 Video-Pattern Generator . . . . .	54
Pseudorandom Binary Sequence (PRBS) . . . . .	54
Video PRBS . . . . .	54
Link PRBS . . . . .	54
Video-Memory ECC Protection . . . . .	55
Scheduler/Arbiter . . . . .	55
Control-Channel CRC Generation and Checking . . . . .	55
Serial Peripheral Interface (SPI) . . . . .	55
CSI-2 Output Interface . . . . .	56
Lane Configurations and Data Rates . . . . .	56
CSI-2 Virtual Channel and Data Type Interleaving . . . . .	56
Video PRBS Generator/Checker . . . . .	56
MIPI CSI-2 Output Raw PRBS Generator . . . . .	57
Lane Deskew . . . . .	57
Minimum Blanking . . . . .	57
MIPI End-to-End Packet Spacing . . . . .	57
CFG Latch at Power-Up Pins . . . . .	58
MFP Function Map and Slew Settings . . . . .	59
MFP Pin Equivalent Circuits . . . . .	60
Power-Up and Link Start-Up . . . . .	61
Device Reset . . . . .	62
Link and Video Lock . . . . .	62
Link Lock . . . . .	62

## TABLE OF CONTENTS (CONTINUED)

Video Lock . . . . .	63
Error and Fault-Condition Monitoring . . . . .	63
Clocking . . . . .	63
Spread-Spectrum Clocking . . . . .	63
Power Supplies . . . . .	63
Power Standby and Sleep Mode . . . . .	64
PCB Layout Guidelines for GMSL . . . . .	64
Ground Plane . . . . .	64
High-Speed GMSL Traces . . . . .	64
Power-Over-Coax Layout . . . . .	65
Shielded Twisted-Pair Layout . . . . .	65
Thermal Management . . . . .	66
Applications Information . . . . .	67
Programming Notes . . . . .	67
Software Programming Model . . . . .	67
Main I <sup>2</sup> C/UART Tunnel . . . . .	67
Control-Channel Programming . . . . .	67
Conventional I <sup>2</sup> C/UART Control-Channel Programming . . . . .	67
Host-to-Peripheral Main I <sup>2</sup> C and Pass-Through I <sup>2</sup> C Communication . . . . .	67
I <sup>2</sup> C Write Packet Format . . . . .	68
I <sup>2</sup> C Read Packet Format . . . . .	68
Main I <sup>2</sup> C Host-to-GMSL2 Device Communication . . . . .	68
Main UART . . . . .	68
UART Base Mode . . . . .	68
UART Bypass Mode . . . . .	69
Switching Between UART Base and Bypass Modes . . . . .	69
UART Frame Format . . . . .	69
Synchronization Frame . . . . .	70
Acknowledge Frame . . . . .	70
Write Packet . . . . .	70
Read Packet . . . . .	71
I <sup>2</sup> C/UART Control-Channel Programming with Optional CRC and Message Counter . . . . .	71
I <sup>2</sup> C/UART CRC and Message Counter Options . . . . .	71
I <sup>2</sup> C Writes with CRC . . . . .	71
I <sup>2</sup> C Reads with CRC . . . . .	72
Message Counter Writes . . . . .	72
Message Counter Reads . . . . .	72
UART Writes with CRC . . . . .	72
UART Reads with CRC . . . . .	73

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

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**TABLE OF CONTENTS (CONTINUED)**

---

Typical Application Circuits .....	75
Ordering Information .....	75
Register Map .....	76
Register Details .....	109
Revision History .....	346

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## LIST OF FIGURES

Figure 1. GMSL3 Reverse-Channel Serial Outputs	31
Figure 2. Ideal Single-Ended and Resulting Differential HS Signals	31
Figure 3. Possible Delta $V_{CMTX}$ and Delta $V_{OD}$ Distortions of Single-Ended HS Signals	32
Figure 4. D-PHY Signaling Levels	32
Figure 5. C-PHY DC Characteristics	33
Figure 6. C-PHY Possible $\Delta V_{CPTX}$ and $\Delta V_{OD}$ Distortions of Single-Ended HS Signals	33
Figure 7. C-PHY Ideal Single-Ended and Resulting Differential High-Speed Signals	34
Figure 8. Lock Time	34
Figure 9. GMSL3 Video Latency	35
Figure 10. GPI-to-GPO Delay and Skew	35
Figure 11. D-PHY High-Speed Data Transmission in Bursts. Reference: MIPI Specification for D-PHY v. 1.2, 01-Aug 2014	35
Figure 12. D-PHY Data Clock Timing	36
Figure 13. Switching the Clock Lane between Clock Transmission and Low-Power Mode	36
Figure 14. D-PHY High-Speed Skew Calibration. Reference: MIPI Specification for D-PHY v. 1.2, 01-Aug 2014	37
Figure 15. C-PHY HS Burst Data Transmission. Reference: MIPI Specification for C-PHY v. 1.0, 05-Aug 2014	37
Figure 16. I <sup>2</sup> C Timing Parameters	38
Figure 17. SPI Master-Mode Timing Parameters	38
Figure 18. SPI Slave-Mode Timing Parameters	39
Figure 19. Ideal Single-Ended and Resulting Differential HS Signals	39
Figure 20. Single Link	40
Figure 21. Dual Link, Separate Data	40
Figure 22. Dual Link, Data Aggregation	41
Figure 23. Dual Link, Data Aggregation and Replication	41
Figure 24. Pixel Mode	46
Figure 25. Tunneling Mode	47
Figure 26. Video Frame Format for Bandwidth Calculation	49
Figure 27. Line Fault Detection Location Options	50
Figure 28. Typical GMSL Link Application Circuit for Coax Cable	51
Figure 29. Typical GMSL Link Application Circuit for Twisted Pair (Line Fault Pair #1: LMN0 and LMN1, Option #2)	52
Figure 30. GMSL3 Video Output of Separate Ports	53
Figure 31. GMSL3 Video Aggregated and Replicated	54
Figure 32. SPI Bridge	56
Figure 33. Video Timing	57
Figure 34. End-to-End Packet Spacing	58
Figure 35. Standard High-Speed GPIO	61
Figure 36. Standard I <sup>2</sup> C GPIO	61
Figure 37. Coax PoC Layout Example	65
Figure 38. STP Layout Example	66

# LIST OF FIGURES (CONTINUED)

Figure 39. I <sup>2</sup> C Write Packet Format .....	68
Figure 40. I <sup>2</sup> C Read Packet Format .....	68
Figure 41. UART Protocol for Base Mode .....	69
Figure 42. UART Data Format for Base Mode .....	70
Figure 43. UART Synchronization Frame .....	70
Figure 44. UART Acknowledge Frame .....	70
Figure 45. UART Write Packet Format .....	71
Figure 46. UART Read Packet Format .....	71
Figure 47. I <sup>2</sup> C CRC Engine .....	71
Figure 48. I <sup>2</sup> C Multiple-Byte Write with CRC .....	72
Figure 49. I <sup>2</sup> C Single-Byte Write with CRC .....	72
Figure 50. I <sup>2</sup> C Multiple-Byte Read with CRC .....	72
Figure 51. I <sup>2</sup> C Single-Byte Read with CRC .....	72
Figure 52. UART CRC Engine .....	73
Figure 53. UART Multiple-Byte Write Transactions with CRC .....	73
Figure 54. UART Single-Byte Write Transaction with CRC .....	73
Figure 55. UART Multiple-Byte Read Transaction with CRC .....	73
Figure 56. UART Single-Byte Read Transaction with CRC .....	74



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

---

**LIST OF TABLES**


---

Table 1. Typical Maximum Cable Length vs. Attenuation . . . . .	1
Table 2. Recommended Operating Conditions . . . . .	28
Table 3. ESD Protection . . . . .	28
Table 4. External Component Requirements . . . . .	29
Table 5. SPI Latching Edge and Speed . . . . .	44
Table 6. Typical GPIO Delays for Forward-Link and Reverse-Link Transmission . . . . .	44
Table 7. Forward- and Reverse-Link Bandwidth Utilization . . . . .	49
Table 8. Coax Mode Line-Fault Configuration Options . . . . .	51
Table 9. STP Mode Line Fault Configuration Options for LMN0/LMN1 . . . . .	51
Table 10. STP Mode Line-Fault Configuration Options for LMN2/LMN3 . . . . .	51
Table 11. Video-Pattern Generator Pixel Clock Selection. . . . .	54
Table 12. CFG0 Input Map . . . . .	58
Table 13. CFG1 Input Map . . . . .	58
Table 14. MFP Pin Function Map . . . . .	59
Table 15. Control- and Side-Channel Typical Rise and Fall Times. . . . .	60

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

### Absolute Maximum Ratings

(All voltages with respect to ground)		D-PHY, C-PHY Pins ( <a href="#">Note b</a> )	-0.3V to ( $V_{TERM} + 0.1V$ )
$V_{DDIO}$	-0.3V to +3.9V	XRES, X2	-0.3V to ( $V_{DD18} + 0.3V$ )
$V_{DD18}$	-0.3V to +2.0V	All Other Pins ( <a href="#">Note c</a> )	-0.3V to ( $V_{DDIO} + 0.3V$ )
$V_{DD}$	-0.3V to +2.0V	Continuous Power Dissipation (Multilayer Board) ( $T_A = +70^{\circ}C$ , derate 40mW/ $^{\circ}C$ above $+70^{\circ}C$ .)	mW to 2200mW
$V_{TERM}$	-0.3V to +1.32V	Storage Temperature Range	-40 $^{\circ}C$ to +150 $^{\circ}C$
CAP_VDD	-0.3V to +1.2V	Soldering Temperature (Reflow)	+260 $^{\circ}C$
SIO_ (Active State) ( <a href="#">Note a</a> )	+0.5V to +2.0V		
SIO_ (Inactive State) ( <a href="#">Note a</a> )	-0.3V to +1.1V		

**Note a:** Active state means device is powered-up, and not in sleep or power-down mode. Inactive means device is not powered-up, or powered-up in sleep or power-down mode.

**Note b:**  $V_{TERM} \leq +1.26V$ .

**Note c:**  $V_{DDIO}$  = specified maximum voltage or 3.9V, whichever is lower.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Package Information

#### 48-Pin TQFN-SW

Package Code	T4877Y+11
Outline Number	<a href="#">21-100045</a>
Land Pattern Number	<a href="#">90-100016</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	25 $^{\circ}C/W$
Junction to Case ( $\theta_{JC}$ )	1 $^{\circ}C/W$

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

# MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

### Electrical Characteristics

( $V_{DD18} = 1.7V$  to  $1.9V$ ,  $V_{DD} = 0.95V$  to  $1.05V$  or  $V_{DD} = 1.14V$  to  $1.26V$ ,  $V_{DDIO} = 1.7V$  to  $3.6V$ ,  $V_{TERM} = 1.14$  to  $1.26V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ , EP connected to PCB ground, typical values are at  $V_{DD18} = V_{DDIO} = 1.8V$ ,  $V_{DD} = 1.0V$ ,  $V_{TERM} = 1.2V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted. ([Note 1](#)))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL3 REVERSE-CHANNEL SERIAL I/O (SIOAP, SIOAN, SIOBP, SIOBN)—SEE <a href="#">Figure 1</a>							
Output-Voltage Swing (Single-Ended)	V <sub>O</sub>	GMSL2 mode	R <sub>L</sub> = 100Ω±1%, (V <sub>OH</sub> - V <sub>OL</sub> ) for all outputs	190	250	310	mV
Output-Voltage Swing (Differential)	V <sub>ODT</sub>	GMSL2 Mode	R <sub>L</sub> = 100Ω±1%, peak-to-peak differential voltage	380	500	620	mV
Output-Voltage Swing (Single-Ended)	V <sub>O</sub>	12Gbps forward data rate (GMSL3-mode)	R <sub>L</sub> = 100Ω±1%, (V <sub>OH</sub> -V <sub>OL</sub> ) for all outputs	110	150	190	mV
Output-Voltage Swing (Differential)	V <sub>ODT</sub>	12Gbps forward data rate (GMSL3-mode)	R <sub>L</sub> = 100Ω±1%, peak-to-peak differential voltage	220	300	380	mV
Change in V <sub>OD</sub> Between Complementary Output States	ΔV <sub>OD</sub>	R <sub>L</sub> = 100Ω ±1%,  V <sub>OD(H)</sub> - V <sub>OD(L)</sub>				25	mV
Differential Output Offset Voltage	V <sub>OS</sub>	R <sub>L</sub> = 100Ω±1%, offset voltage in each output state	GMSL2-mode	V <sub>DD18</sub> - 0.45	V <sub>DD18</sub> - 0.3	V <sub>DD18</sub> - 0.15	V
			GMSL3-mode	V <sub>DD18</sub> - 0.4	V <sub>DD18</sub> - 0.25	V <sub>DD18</sub> - 0.1	
Change in V <sub>OS</sub> Between Complimentary Output States	ΔV <sub>OS</sub>	R <sub>L</sub> = 100Ω ±1%,  V <sub>OD(H)</sub> - V <sub>OD(L)</sub>				25	mV
Output Termination Resistance (Internal)	R <sub>T</sub>	Any pin to V <sub>DD18</sub>		50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / C-PHY AND D-PHY LP TRANSMITTER							
High-Level Output Voltage	V <sub>OH</sub>	See <a href="#">Figure 4</a> , <a href="#">Figure 5</a>		0.95	1.2	1.3	V
Low-Level Output Voltage	V <sub>OL</sub>	See <a href="#">Figure 4</a> , <a href="#">Figure 5</a>		-50		50	mV
Output Impedance	Z <sub>OLP</sub>	<a href="#">(Note 9)</a>		110			Ω
DC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER							
HS Transmit Static Common-Mode Voltage	V <sub>CMTX</sub>	See <a href="#">Figure 4</a>		150	200	250	mV
V <sub>CMTX</sub> Mismatch when Output is Differential-1 or Differential-0	ΔV <sub>CMTX(1,0)</sub>	ΔV <sub>CMTX(1,0)</sub> = (V <sub>CMTX(1)</sub> - V <sub>CMTX(0)</sub> )/2, See <a href="#">Figure 3</a>				5	mV
HS Transmit Differential Voltage	V <sub>OD</sub>	See <a href="#">Figure 2</a>		140	200	270	mV
V <sub>OD</sub> Mismatch when Output is Differential-1 or Differential-0	ΔV <sub>OD</sub>	See <a href="#">Figure 3</a>				14	mV
HS Output High Voltage	V <sub>OHHS</sub>	See <a href="#">Figure 4</a>				360	mV

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

## Electrical Characteristics (continued)

( $V_{DD18} = 1.7V$  to  $1.9V$ ,  $V_{DD} = 0.95V$  to  $1.05V$  or  $V_{DD} = 1.14V$  to  $1.26V$ ,  $V_{DDIO} = 1.7V$  to  $3.6V$ ,  $V_{TERM} = 1.14$  to  $1.26V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ , EP connected to PCB ground, typical values are at  $V_{DD18} = V_{DDIO} = 1.8V$ ,  $V_{DD} = 1.0V$ ,  $V_{TERM} = 1.2V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Output Impedance	$Z_{OS}$		40	50	62.5	$\Omega$
Single-Ended Output Impedance Mismatch	$\Delta Z_{OS}$				15	%
<b>DC ELECTRICAL CHARACTERISTICS / C-PHY HS TRANSMITTER</b>						
HS Transmit Static Common-Point Voltage	$V_{CPTX}$	See Figure 5, (Note 4, Note 6)	175	225 to 250	310	mV
$V_{CPTX}$ Mismatch when Output is in any of the Six High-Speed States	$ \Delta V_{CPTX(HS)} $	See Figure 6			9	mV
HS Transmit Differential Voltage of the Differential Strong 1 and Strong 0	$ \Delta V_{OD} _{strong}$	See Figure 7, (Note 4)			300	mV
HS Transmit Differential Voltage of the Differential Weak 1 and Weak 0	$ \Delta V_{OD} _{weak}$	See Figure 7, (Note 4)	97			mV
$V_{OD}$ Mismatch Between the Absolute Values of the Differential Strong 1 and Strong 0 Output Voltage is any of the Six Possible High-Speed States	$ \Delta V_{OD} $	See Figure 6			17	mV
HS Output High Voltage	$V_{OHHS}$	See Figure 5, (Note 4)			425	mV
Single-Ended Output Impedance	$Z_{OS}$		40	50	60	$\Omega$
Single-Ended Output Impedance Mismatch	$\Delta Z_{OS}$				10	%
<b>DC ELECTRICAL CHARACTERISTICS / I/O PINS (GPIO)</b>						
High-Level Input Voltage	$V_{IH}$		$0.7 \times V_{DDIO}$			V
Low-Level Input Voltage	$V_{IL}$			$0.3 \times V_{DDIO}$		V
High-Level Output Voltage	$V_{OH}$	$I_{OH} = -4mA$	$V_{DDIO} - 0.4$			V
Low-Level Output Voltage	$V_{OL}$	$I_{OL} = 4mA$		0.4		V
Input Current	$I_{IN}$	$V_{IN} = 0$ to $V_{DDIO}$ . All pullup/pulldown devices disabled.			1	$\mu A$
Input Capacitance	$C_{IN}$			5		pF
Input Pullup/Pulldown Resistance	$R_{IN}$	40k $\Omega$ enabled		40		k $\Omega$
		1M $\Omega$ enabled		1		M $\Omega$

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

Electrical Characteristics (continued)

( $V_{DD18} = 1.7V$  to  $1.9V$ ,  $V_{DD} = 0.95V$  to  $1.05V$  or  $V_{DD} = 1.14V$  to  $1.26V$ ,  $V_{DDIO} = 1.7V$  to  $3.6V$ ,  $V_{TERM} = 1.14$  to  $1.26V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ , EP connected to PCB ground, typical values are at  $V_{DD18} = V_{DDIO} = 1.8V$ ,  $V_{DD} = 1.0V$ ,  $V_{TERM} = 1.2V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS (SDA_, SCL_, SDA_RX, TX_SCL, LOCK, ERRB/LFLT, ODO)						
High-Level Input Voltage	V <sub>IH</sub>		0.7 x V <sub>DDIO</sub>			V
Low-Level Input Voltage	V <sub>IL</sub>				0.3 x V <sub>DDIO</sub>	V
Low-Level Open-Drain Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4mA			0.4	V
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 to V <sub>DDIO</sub> . All pullup/pulldown devices disabled.			1	μA
Input Capacitance	C <sub>IN</sub>			3		pF
Internal Pullup Resistor	R <sub>PU</sub>	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V <sub>IH</sub>		0.7 x V <sub>DDIO</sub>			V
Low-Level Input Voltage	V <sub>IL</sub>				0.3 x V <sub>DDIO</sub>	V
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 to V <sub>DDIO</sub>			6	μA
Internal Pulldown Resistance	R <sub>PD</sub>			1		MΩ
Input Capacitance	C <sub>IN</sub>			3		pF
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4mA	V <sub>DDIO</sub> - 0.4			V
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / LINE FAULT DETECTION INPUT, (See <a href="#">Figure 28</a> , <a href="#">Figure 29</a> )						
Open Pin Voltage	V <sub>O0</sub>	LMN0, LMN2		1.25		V
	V <sub>O1</sub>	LMN1, LMN3		0.75		
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL), (X1/OSC, X2)						
X1 Input Capacitance	C <sub>IN_X1</sub>			3		pF
X2 Input Capacitance	C <sub>IN_X2</sub>			1		pF
X2 Limit Resistor	R <sub>LIM</sub>			1.2		kΩ
Feedback Resistor	R <sub>FB</sub>			10		kΩ
Transconductance	g <sub>m</sub>			28		mA/V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (X1/OSC DRIVEN BY EXTERNAL CLOCK, X2 FLOATING)						
High-Level Input Voltage	V <sub>IH</sub>		0.9			V
Low-Level Input Voltage	V <sub>IL</sub>				0.4	V
X1 Input Capacitance	C <sub>IN_X1</sub>			3		pF
Input Resistance	R <sub>IN</sub>			10		kΩ

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

Electrical Characteristics (continued)

( $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $V_{TERM}$  = 1.14 to 1.26V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $V_{TERM}$  = 1.2V,  $T_A$  = 25°C, unless otherwise noted. ([Note 1](#)))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS							
Supply Current	I <sub>DD</sub>	2x 12Gbps input, 2x 4-lane output, 2.5Gbps/lane	V <sub>DD</sub> = 1.05V		365	850	mA
			V <sub>DD</sub> = 1.26V		365	850	mA
			V <sub>DD18</sub> = 1.9V		210	250	mA
			V <sub>TERM</sub> = 1.26V		31	40	
Maximum V <sub>DDIO</sub> Supply Current ( <a href="#">Note 5</a> )	I <sub>DDIO</sub>	Per toggling GPIO, C <sub>L</sub> = 20pF	V <sub>DDIO</sub> = 1.9V		44		μA/MHz
			V <sub>DDIO</sub> = 3.6V		81		
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Maximum Power-Down Current	I <sub>DD</sub>	V <sub>DDIO</sub> at 3.6V	T <sub>A</sub> = +25°C		6		μA
			T <sub>A</sub> = +105°C		7		
		V <sub>TERM</sub> at 1.26V	T <sub>A</sub> = +25°C		< 1		
			T <sub>A</sub> = +105°C		< 1		
		V <sub>DD18</sub> at 1.9V	T <sub>A</sub> = +25°C		< 1		
			T <sub>A</sub> = +105°C		28		
		V <sub>DD</sub> at 1.26V	T <sub>A</sub> = +25°C		6		
			T <sub>A</sub> = +105°C		6		
DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENT							
Maximum Sleep Current	I <sub>DD</sub>	V <sub>DDIO</sub> at 3.6V	T <sub>A</sub> = +25°C		9		μA
			T <sub>A</sub> = +105°C		9		
		V <sub>TERM</sub> at 1.26V	T <sub>A</sub> = +25°C		< 1		
			T <sub>A</sub> = +105°C		< 1		
		V <sub>DD18</sub> at 1.9V	T <sub>A</sub> = +25°C		17		
			T <sub>A</sub> = +105°C		47		
		V <sub>DD</sub> at 1.26V	T <sub>A</sub> = +25°C		7		
			T <sub>A</sub> = +105°C		6		
AC ELECTRICAL CHARACTERISTICS / GMSL3 FORWARD-CHANNEL SWITCHING CHARACTERISTICS							
Lock Time	t <sub>LOCK</sub>	From power-up, one-shot reset, or rising edge of PWDNB to rising edge of LOCK. See <a href="#">Figure 8</a>			68		ms
Maximum Video Initialization Time	t <sub>VIDEOSTART</sub>	Time from GMSL3 video packets at SIO <sub>-</sub> to valid packets at the CSI-2 output (assumes link locked and registers configured).			0.1 + (6600 x T <sub>PCLK</sub> )		ms
Maximum Video Latency	t <sub>VL</sub>	Time from the first pixel in a GMSL3 packet at SIO <sub>-</sub> to the first pixel in the CSI-2 output packet. See <a href="#">Figure 9</a>			1 video line + (128 x T <sub>PCLK</sub> )		s
PWDNB Hold Time	t <sub>HOLD_PWDNB</sub>	The minimum duration PWDNB must be held LOW to reset the chip.			1		ms

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

## Electrical Characteristics (continued)

( $V_{DD18} = 1.7V$  to  $1.9V$ ,  $V_{DD} = 0.95V$  to  $1.05V$  or  $V_{DD} = 1.14V$  to  $1.26V$ ,  $V_{DDIO} = 1.7V$  to  $3.6V$ ,  $V_{TERM} = 1.14$  to  $1.26V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ , EP connected to PCB ground, typical values are at  $V_{DD18} = V_{DDIO} = 1.8V$ ,  $V_{DD} = 1.0V$ ,  $V_{TERM} = 1.2V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AC ELECTRICAL CHARACTERISTICS / GMSL3 REVERSE CHANNEL SERIAL OUTPUTS (SIO_P, SIO_N) (Note 2)</b>						
Serial Output Rise Time	$t_R$	20% to 80%, $V_O = 250mV$ , $R_L = 100\Omega$		2300		ps
Serial Output Fall Time	$t_F$	80% to 20%, $V_O = 250mV$ , $R_L = 100\Omega$		2300		ps
Total Serial Output Jitter	$t_{TSOJ}$	PRBS7, single-ended or differential output		0.15		UI (p-p)
Deterministic Serial Output Jitter	$t_{DSOJ}$	PRBS7, single-ended or differential output		0.1		UI (p-p)
GPI-GPO Delay Reverse Path	$t_{GPDR}$	Delay-compensated mode See Figure 10		15		$\mu s$
		Non-delay-compensated mode See Figure 10		6		
GPI-GPO Skew Reverse Path	$t_{SKEW}$	Delay-compensated mode See Figure 10		7		ns
<b>AC ELECTRICAL CHARACTERISTICS / CSI-2 HS TRANSMITTER, CONFIGURED AS D-PHY</b>						
Common-Level Variations, HF	$\Delta V_{CMTX(HF)}$	> 450MHz, See Figure 3 (Note 2)			15	mV <sub>RMS</sub>
Common-Level Variations, LF	$\Delta V_{CMTX(LF)}$	50MHz to 450MHz, See Figure 3 (Note 2)			25	mV <sub>PEAK</sub>
20% to 80% Rise Time and Fall Time	$t_R$ and $t_F$	(Note 2)			0.4	UI
		(Note 5)	50			ps
Tx Differential Return Loss	$S_{ddTX}$	$f_{HMAX} = 1.0GHz$		-10		dB
		$f_{MAX} = 1.5GHz$		-8		
Tx Common Mode Return Loss	$S_{ccTX}$	$f_{MAX} = 1.5GHz$		-7		dB
Data-Lane Bit Rate	$DLBR$		80		2500	Mbps
Clock-Lane Frequency	$CLFREQ$		40		1250	MHz
CSI-2 Output Inter-Packet Spacing	$t_{SPACE}$			300 + 370UI		ns
<b>AC ELECTRICAL CHARACTERISTICS / D-PHY AND C-PHY LP TRANSMITTER (Note 2)</b>						
15% to 85% Rise Time and Fall Time	$T_{RLP}/T_{FLP}$	(Note 3)			25	ns
30% to 85% Rise Time	$T_{REOT}$	See Figure 11, Figure 15, (Note 8)			35	ns
Load Capacitance	$C_{LOAD}$	(Note 3)	0		70	pF
<b>AC ELECTRICAL CHARACTERISTICS / D-PHY DATA-CLOCK TIMING (Note 2)</b>						
UI Instantaneous	$UI_{INST}$		0.4		12.5	ns
UI Variation	$\Delta UI$	$UI \geq 1ns$ , within a single burst	-10%		10%	UI
		$0.667ns < UI < 1ns$ , within a single burst	-5%		5%	
Data to Clock Skew	$T_{SKEW}$	0.08Gbps to 1.0Gbps, See Figure 12	-0.15		0.15	$UI_{INST}$
		> 1.0Gbps to 1.5Gbps, See Figure 12	-0.20		0.20	
Static Data to Clock Skew (Tx)	$T_{SKEW(TX) Static}$	> 1.5Gbps, See Figure 12	-0.20		0.20	$UI_{INST}$



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

### Electrical Characteristics (continued)

( $V_{DD18} = 1.7V$  to  $1.9V$ ,  $V_{DD} = 0.95V$  to  $1.05V$  or  $V_{DD} = 1.14V$  to  $1.26V$ ,  $V_{DDIO} = 1.7V$  to  $3.6V$ ,  $V_{TERM} = 1.14$  to  $1.26V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ , EP connected to PCB ground, typical values are at  $V_{DD18} = V_{DDIO} = 1.8V$ ,  $V_{DD} = 1.0V$ ,  $V_{TERM} = 1.2V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted. ([Note 1](#)))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Data to Clock Skew (Tx)	$T_{SKEW(TX)}$ Dynamic	> 1.5Gbps, See <a href="#">Figure 12</a>	-0.15		0.15	UI <sub>INST</sub>
<b>AC ELECTRICAL CHARACTERISTICS / CSI-2 D-PHY GLOBAL OPERATION TIMING (<a href="#">Note 2</a>)</b>						
Time that the HS clock must be Driven by the Transmitter Prior to any Associated Data Lane Beginning the Transition from LP to HS Mode	$T_{CLK-PRE}$	See <a href="#">Figure 13</a>	8			UI <sub>INST</sub>
Time that the Transmitter Drives the Clock Lane LP-00 Line State Immediately Before the HS-0 Line State Starting the HS Transmission	$T_{CLK-PREPARE}$	See <a href="#">Figure 13</a>	38		95	ns
$T_{CLK-PREPARE}$ + Time that the Transmitter Drives the HS-0 State Prior to Starting the Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	See <a href="#">Figure 13</a>	300			ns
Transmitted Time Interval from the Start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ to the Start of the LP-11 State Following a HS Burst	$T_{EOT}$	See <a href="#">Figure 11</a> , <a href="#">Figure 13</a> , and <a href="#">Figure 14</a>			$105 + 12 \times UI$	ns
Time that the Transmitter Drives LP-11 Following a HS Burst	$T_{HS-EXIT}$	See <a href="#">Figure 11</a> , <a href="#">Figure 13</a> , and <a href="#">Figure 14</a>	100			ns
Time that the Transmitter Drives the Data Lane LP-00 Line State Immediately Before the HS-0 Line State Starting the HS Transmission	$T_{HS-PREPARE}$	See <a href="#">Figure 11</a> , <a href="#">Figure 13</a> , and <a href="#">Figure 14</a>	$40 + 4 \times UI$		$85 + 6 \times UI$	ns
$T_{HS-PREPARE}$ + Time that the Transmitter Drives the HS-0 State Prior to Transmitting the Sync Sequence	$T_{HS-PREPARE} + T_{HS-ZERO}$	See <a href="#">Figure 11</a>	$145 + 10 \times UI$			ns
Time that the Transmitter Drives the Flipped Differential State After Last Payload Data Bit of a HS Transmission Burst	$T_{HS-TRAIL}$	See <a href="#">Figure 11</a> , <a href="#">Figure 14</a>	$60 + 4 \times UI$			ns



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

Electrical Characteristics (continued)

( $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $V_{TERM}$  = 1.14 to 1.26V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $V_{TERM}$  = 1.2V,  $T_A$  = 25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Initialization	T <sub>INIT</sub>		100			μs
Transmitted Length of Any Low-Power State Period.	T <sub>LPX</sub>	See <a href="#">Figure 11</a> , <a href="#">Figure 13</a> , and <a href="#">Figure 14</a>	50			ns
Time that the Transmitter Drives the Skew-Calibration Sync Pattern, 0xFFFF	T <sub>SKEWCAL_SYNC</sub>	See <a href="#">Figure 14</a>		16		UI
Time that the Transmitter Drives the Skew-Calibration Pattern in the Initial Skew-Calibration Mode	T <sub>SKEWCAL</sub>	See <a href="#">Figure 14</a>			100	μs
		See <a href="#">Figure 14</a>	2 <sup>15</sup>		UI	
Time that the Transmitter Drives the Skew-Calibration Pattern in the Periodic Skew-Calibration Mode	T <sub>SKEWCAL</sub>	See <a href="#">Figure 14</a>			10	μs
		See <a href="#">Figure 14</a>	2 <sup>10</sup>		UI	
AC ELECTRICAL CHARACTERISTICS / CSI-2 HS TRANSMITTER, CONFIGURED AS C-PHY						
Common-Level Variations ( <a href="#">Note 2</a> )	ΔV <sub>CPTX(HF)</sub>	> 450MHz			15	mV <sub>RMS</sub>
	ΔV <sub>CPTX(LF)</sub>	50MHz to 450MHz			25	mV <sub>PEAK</sub>
Rise Time	t <sub>R</sub>	Strong 0 to weak 1 transition, -58mV to +58mV, Z <sub>ID</sub> = 100Ω ( <a href="#">Note 2</a> )			0.285	UI
Fall time	t <sub>F</sub>	Strong 1 to weak 0 transition, +58mV to -58mV, Z <sub>ID</sub> = 100Ω ( <a href="#">Note 2</a> )			0.285	UI
Rise Time and Fall Time Limit	t <sub>RISE-FALL-MAX</sub>	-58mV to +58mV, Z <sub>ID</sub> = 100Ω. ( <a href="#">Note 2</a> , <a href="#">Note 7</a> )			360	ps
Differential-Mode Reflection Coefficient ( <a href="#">Note 10</a> )	S <sub>ddTX</sub>	f <sub>H</sub> = 1.25GHz		-12		dB
		f <sub>MAX</sub> = 1.875GHz		-9		
Common-Mode Reflection Coefficient ( <a href="#">Note 10</a> )	S <sub>ccTX</sub>	f <sub>MAX</sub> = 1.875GHz		-10		dB
C-PHY Lane Bit Rate	C <sub>BR</sub>		182		4571	Mbps
CSI-2 Output Inter-Packet Spacing	t <sub>SPACE</sub>			300 + 370 x UI		ns
UI Instantaneous	UI <sub>INST</sub>		0.4		12.5	ns
AC ELECTRICAL CHARACTERISTICS / CSI-2 C-PHY GLOBAL OPERATION TIMING—SEE <a href="#">Figure 15</a> ( <a href="#">Note 2</a> )						
Time that the Transmitter Drives the 3-Wire LP-000 Line State Immediately Before the HS_+x Line State Starting the HS Transmission	t <sub>3-PREPARE</sub>	( <a href="#">Note 2</a> )	38		95	ns

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

## Electrical Characteristics (continued)

( $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $V_{TERM}$  = 1.14 to 1.26V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $V_{TERM}$  = 1.2V,  $T_A$  = 25°C, unless otherwise noted. ([Note 1](#)))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time that the Transmitter Drives LP-111 Following a HS Burst	$t_{3\text{-HS-EXIT}}$	( <a href="#">Note 2</a> )	100			ns
Transmitted Length of Any Low-Power State Period	$t_{LPX}$	( <a href="#">Note 1</a> , <a href="#">Note 2</a> )	50			ns
Initialization Time	$t_{INIT}$	( <a href="#">Note 2</a> )	100			μs
<b>AC ELECTRICAL CHARACTERISTICS / I<sup>2</sup>C/UART PORT TIMING—SEE <a href="#">Figure 16</a></b>						
I <sup>2</sup> C/UART Bit Rate			9.6		1000	kbps
Output Fall Time	$t_F$	70% to 30%, $C_L$ = 20pF to 100pF, 1kΩ pullup to $V_{DDIO}$	20 x $V_{DDIO}/5$ . 5V		150	ns
I <sup>2</sup> C/UART Wake Time	$t_{WAKEUP}$	From power-up, or rising edge of PWDNB to local register access. For remote register access, I <sup>2</sup> C/UART wake time is the same as lock time ( $t_{LOCK}$ ).		2.25		ms
<b>AC ELECTRICAL CHARACTERISTICS / I<sup>2</sup>C TIMING—SEE <a href="#">Figure 16</a></b>						
SCL Clock Frequency	$f_{SCL}$	Low $f_{SCL}$ range: (I2CMSTBT = 010, I2CSLVSH = 10)	9.6		100	kHz
		Mid $f_{SCL}$ range: (I2CMSTBT 101, I2CSLVSH = 01)	> 100		400	
		High $f_{SCL}$ range: (I2CMSTBT = 111, I2CSLVSH = 00)	> 400		1000	
Start Condition Hold Time	$t_{HD:STA}$	$f_{SCL}$ range, Low	4			μs
		$f_{SCL}$ range, Mid	0.6			
		$f_{SCL}$ range, High	0.26			
Low Period of SCL Clock	$t_{LOW}$	$f_{SCL}$ range, Low	4.7			μs
		$f_{SCL}$ range, Mid	1.3			
		$f_{SCL}$ range, High	0.5			
High Period of SCL Clock	$t_{HIGH}$	$f_{SCL}$ range, Low	4			μs
		$f_{SCL}$ range, Mid	0.6			
		$f_{SCL}$ range, High	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	$f_{SCL}$ range, Low	4.7			μs
		$f_{SCL}$ range, Mid	0.6			
		$f_{SCL}$ range, High	0.26			
Data Hold Time	$t_{HD:DAT}$	$f_{SCL}$ range, Low	0			ns
		$f_{SCL}$ range, Mid	0			
		$f_{SCL}$ range, High	0			
Data Setup Time	$t_{SU:DAT}$	$f_{SCL}$ range, Low	250			ns
		$f_{SCL}$ range, Mid	100			
		$f_{SCL}$ range, High	50			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

Electrical Characteristics (continued)

( $V_{DD18} = 1.7V$  to  $1.9V$ ,  $V_{DD} = 0.95V$  to  $1.05V$  or  $V_{DD} = 1.14V$  to  $1.26V$ ,  $V_{DDIO} = 1.7V$  to  $3.6V$ ,  $V_{TERM} = 1.14$  to  $1.26V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ , EP connected to PCB ground, typical values are at  $V_{DD18} = V_{DDIO} = 1.8V$ ,  $V_{DD} = 1.0V$ ,  $V_{TERM} = 1.2V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for Stop Condition	$t_{SU:STO}$	$f_{SCL}$ range, Low	4			$\mu s$
		$f_{SCL}$ range, Mid	0.6			
		$f_{SCL}$ range, High	0.26			
Bus Free Time	$t_{BUF}$	$f_{SCL}$ range, Low	4.7			$\mu s$
		$f_{SCL}$ range, Mid	1.3			
		$f_{SCL}$ range, High	0.5			
Data Valid Time	$t_{VD:DAT}$	$f_{SCL}$ range, Low			3.45	$\mu s$
		$f_{SCL}$ range, Mid			0.9	
		$f_{SCL}$ range, High			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	$f_{SCL}$ range, Low			3.45	$\mu s$
		$f_{SCL}$ range, Mid			0.9	
		$f_{SCL}$ range, High			0.45	
Pulse Width of Spikes Suppressed	$t_{SP}$	$f_{SCL}$ range, Low			50	ns
		$f_{SCL}$ range, Mid			50	
		$f_{SCL}$ range, High			50	
Capacitive Load on Each Bus Line	$C_B$	(Note 2)			100	pF
<b>AC ELECTRICAL CHARACTERISTICS / SPI MASTER—SEE Figure 17 (Note 11)</b>						
Programmable Operating Frequency Range	$f_{MCK}$	(Note 2)	0.588		25	MHz
SCLK Period	$t_{MCK}$			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	$t_{MCH}, t_{MCL}$	$C_L = 5pF$ (Note 2)	$t_{MCK}/2 - 3$	$t_{MCK}/2$		ns
MOSI Data Output Delay	$t_{MOD}$	After SCLK falling edge (Note 2)	-6		3	ns
MISO Input Setup Time	$t_{MIS}$	Before programmed sampling edge (Note 2)	13.5			ns
MISO Input Hold Time	$t_{MIH}$	After programmed sampling edge (Note 2)	-2			ns
<b>AC ELECTRICAL CHARACTERISTICS / SPI SLAVE—SEE Figure 18 (Note 11)</b>						
Operating Frequency	$f_{SCK}$	(Note 2)			25	MHz
SCLK Period	$t_{SCK}$			$1/f_{SCK}$		ns
MISO Data Output Delay	$t_{SOD}$	After SCLK falling edge, (Note 2)	3		12.5	ns
MOSI Input Setup Time	$t_{SIS}$	Before SCLK rising edge	5			ns
MOSI Input Hold Time	$t_{SIH}$	After SCLK rising edge	3			ns
<b>AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1/OSC, X2)</b>						
Frequency	$f_{REF}$			25		MHz

# MAX96792A

# Dual GMSL3/2 to CSI-2 Deserializer

## Electrical Characteristics (continued)

( $V_{DD18} = 1.7V$  to  $1.9V$ ,  $V_{DD} = 0.95V$  to  $1.05V$  or  $V_{DD} = 1.14V$  to  $1.26V$ ,  $V_{DDIO} = 1.7V$  to  $3.6V$ ,  $V_{TERM} = 1.14$  to  $1.26V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ , EP connected to PCB ground, typical values are at  $V_{DD18} = V_{DDIO} = 1.8V$ ,  $V_{DD} = 1.0V$ ,  $V_{TERM} = 1.2V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted. ([Note 1](#)))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Stability + Frequency Tolerance	$f_{TN}$		-200		+200	ppm
<b>AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (EXTERNAL INPUT ON X1/OSC, X2 FLOATING)</b>						
Frequency	$F_{REF}$			25		MHz
Frequency Stability + Frequency Tolerance	$f_{TN}$		-200		+200	ppm
Duty Cycle	DC		40	50	60	%
Input Jitter	$t_{JIN}$	Forward data rate = 12Gbps bit rate, Reverse data rate = 187.5Mbps, RoR not used by serializer, Sinusoidal jitter < 1MHz (rising edge)			150	ps (p-p)
		Forward data rate = 12Gbps bit rate, Reverse data rate = 187.5Mbps, RoR used by serializer, Sinusoidal jitter < 1MHz (rising edge)			75	
Input Rise Time	$t_R$	10% to 90%		5		ns
Input Fall Time	$t_F$	90% to 10%		5		ns

**Note 1:** Limits are 100% tested at  $T_A = +105^{\circ}C$ , unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Maximum supply currents are specified for  $T_J = +105^{\circ}C$ .

**Note 2:** Not production tested. Guaranteed by design and characterization.

**Note 3:**  $C_{LOAD}$  includes the low-frequency equivalent transmission line capacitance. The capacitance of Tx and Rx are assumed to always be < 10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

**Note 4:** Value when driving into load impedance  $Z_{ID} = 100\Omega$ .

**Note 5:** MFP pin speed programmed to fastest setting (TTS = 00). See the [MFP Function Map and Slew Settings](#) section for details on MFP speed programming.

**Note 6:** Typical value of  $V_{CPTX}$  should be in the specified range depending upon the supply voltage used for each implementation.

**Note 7:** Measured as average across any 50mV segment of the output signal transition.

**Note 8:** The rise-time of  $t_{REOT}$  starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

**Note 9:** Though no maximum value for  $Z_{OLP}$  is specified, the LP transmitter output impedance ensures the  $t_{RLP}/t_{FLP}$  specification is met.

**Note 10:** Differential-Mode and Common-Mode reflection coefficients are compliant with MIPI C-PHY V1.0 requirements over all specified operating frequencies.

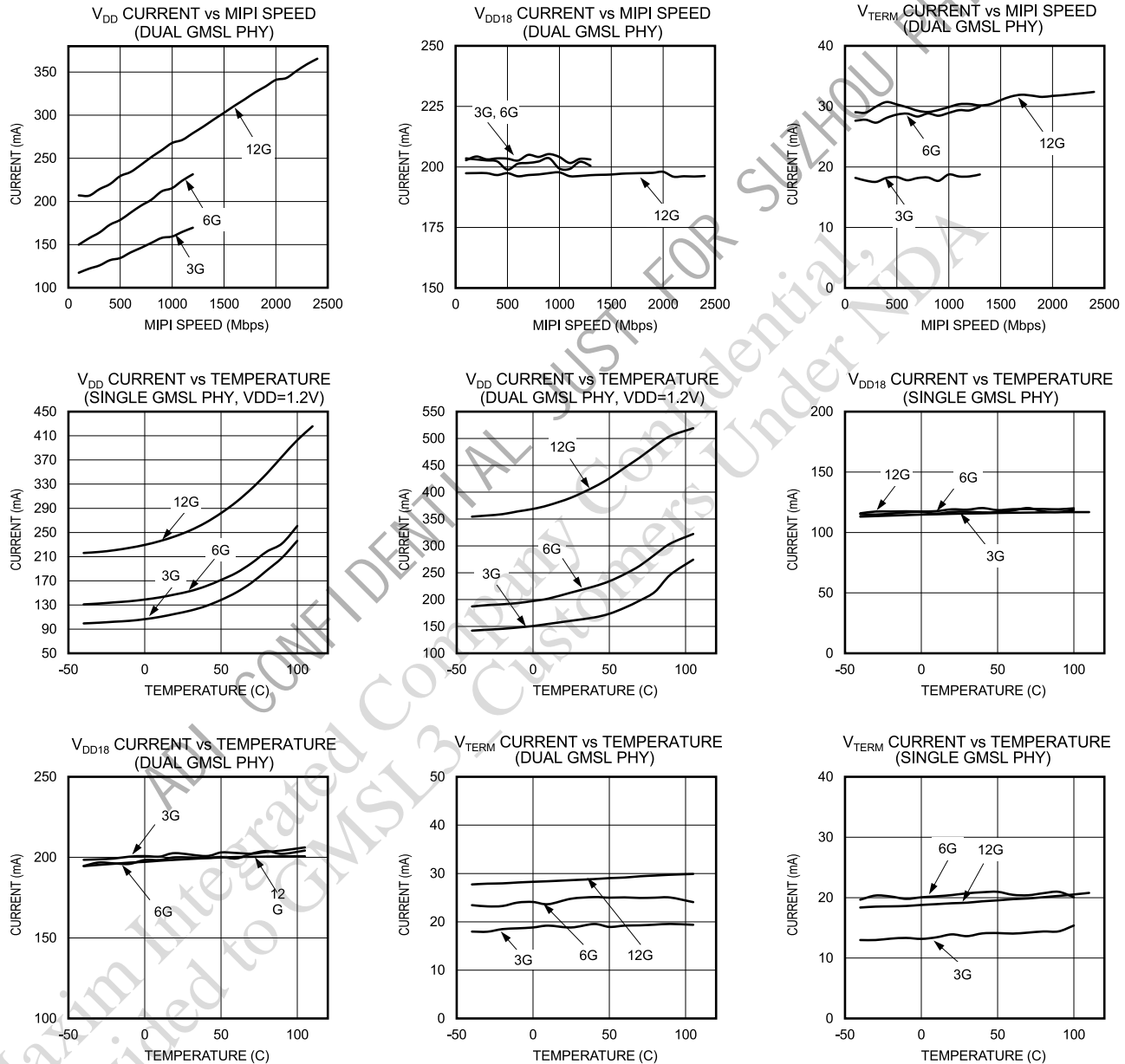
**Note 11:** Measured at 25MHz.

# MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

### Typical Operating Characteristics

( $V_{\text{TERM}} = 1.2\text{V}$ ,  $V_{\text{DD18}} = 1.8\text{V}$ ,  $V_{\text{DDIO}} = 1.8\text{V}$ ,  $V_{\text{DD}} = 1.0\text{V}$ ,  $T_A = +25^\circ\text{C}$  unless otherwise noted. PRBS24 data. Single GMSL PHY configuration at 6Gbps or 12Gbps: SIOA or SIOB GMSL input enabled, data output on 4-lane Port A or Port B. Single GMSL PHY configuration at 3Gbps: SIOA or SIOB GMSL input enabled, data output on 2-lane Port A or Port B. Dual GMSL PHY configuration: SIOA (6Gbps or 12Gbps) data output on 4-lane CSI-2 Port A, SIOB (6Gbps or 12Gbps) data output on 4-lane CSI-2 Port B. SIOA (3Gbps) data output on 2-lane CSI-2 Port A, SIOB (3Gbps) data output on 2-lane CSI-2 Port B)

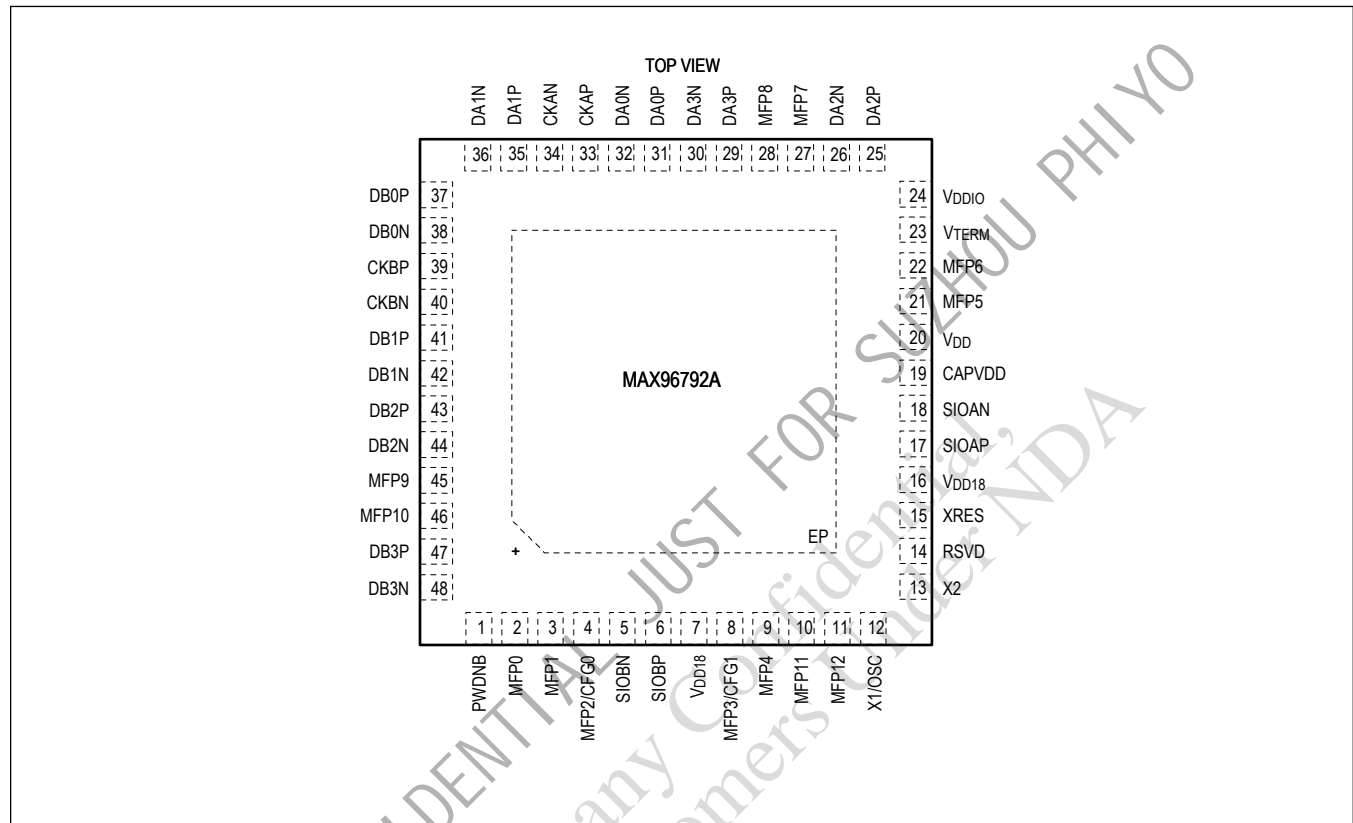


MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

## Pin Configuration

MAX96792A



## Pin Descriptions

PIN	NAME	FUNCTION MODE	FUNCTION
		GMSL3/2	
GMSL3/2 Serial Link			
5	SIOBN	SIOBN	Inverted Twisted-Pair Serial-Data Input/Output B
6	SIOBP	SIOBP	Noninverted Coax/Twisted Pair Serial Data Input/Output B
17	SIOAP	SIOAP	Noninverted Coax/Twisted-Pair Serial-Data Input/Output A
18	SIOAN	SIOAN	Inverted Twisted-Pair Serial-Data Input/Output A
CSI-2 INTERFACE (*) INDICATES DEFAULT STATE AFTER POWER-UP (NOTE: LEAVE PINS OPEN IF UNUSED)			
25	DA2P	DA2P	CSI-2 Port A Data Lane 2 Noninverted Output (D-PHY 4-Lane Mode).
26	DA2N	DA2N	CSI-2 Port A Data Lane 2 Inverted Output (D-PHY 4-Lane Mode).
29	DA3P	DA3P	CSI-2 Port A Data Lane 3 Noninverted Output (D-PHY 4-Lane Mode).
30	DA3N	DA3N	CSI-2 Port A Data Lane 3 Inverted Output (D-PHY 4-Lane Mode).
31	DA0P	DA0P* DD0A	DA0P: CSI-2 Port A Data Lane 0 Noninverted Output (D-PHY 4-Lane Mode). DD0A: CSI-2 Port D Data Lane 0 A-Output (C-PHY 2-Lane Mode).

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MAX96792A**

PIN	NAME	FUNCTION MODE	FUNCTION
		GMSL3/2	
32	DA0N	DA0N* DD0B	DA0N: CSI-2 Port A Data Lane 0 Inverted Output (D-PHY 4-Lane Mode). DD0B: CSI-2 Port D Data Lane 0 B-Output (C-PHY 2-Lane Mode).
33	CKAP	CKAP* DD0C	CKAP: CSI-2 Port A Clock Lane Noninverted Output (D-PHY 4-Lane Mode). DD0C: CSI-2 Port D Data Lane 0 C-Output (C-PHY 2-Lane Mode).
34	CKAN	CKAN* DD1A	CKAN: CSI-2 Port A Clock Lane Inverted Output (D-PHY 4-Lane Mode). DD1A: CSI-2 Port D Data Lane 1 A-Output (C-PHY 2-Lane Mode).
35	DA1P	DA1P* DD1B	DA1P: CSI-2 Port A Data Lane 1 Noninverted Output (D-PHY 4-Lane Mode). DD1B: CSI-2 Port D Data Lane 1 B-Output (C-PHY 2-Lane Mode).
36	DA1N	DA1N* DD1C	DA1N: CSI-2 Port A Data Lane 1 Inverted Output (D-PHY 4-Lane Mode). DD1C: CSI-2 Port D Data Lane 1 C-Output (C-PHY 2-Lane Mode).
37	DB0P	DB0P* DE0A	DB0P: CSI-2 Port B Data Lane 0 Noninverted Output (D-PHY 4-Lane Mode). DE0A: CSI-2 Port E Data Lane 0 A-Output (C-PHY 2-Lane Mode).
38	DB0N	DB0N* DE0B	DB0N: CSI-2 Port B Data Lane 0 Inverted Output (D-PHY 4-Lane Mode). DE0B: CSI-2 Port E Data Lane 0 B-Output (C-PHY 2-Lane Mode).
39	CKBP	CKBP* DE0C	CKBP: CSI-2 Port B Clock Lane Noninverted Output (D-PHY 4-Lane Mode). DE0C: CSI-2 Port E Data Lane 0 C-Output (C-PHY 2-Lane Mode).
40	CKBN	CKBN* DE1A	CKBN: CSI-2 Port B Clock Lane Inverted Output (D-PHY 4-Lane Mode). DE1A: CSI-2 Port E Data Lane 1 A-Output (C-PHY 2-Lane Mode).
41	DB1P	DB1P* DE1B	DB1P: CSI-2 Port B Data Lane 1 Noninverted Output (D-PHY 4-Lane Mode). DE1B: CSI-2 Port E Data Lane 1 B-Output (C-PHY 2-Lane Mode).
42	DB1N	DB1N* DE1C	DB1N: CSI-2 Port B Data Lane 1 Inverted Output (D-PHY 4-Lane Mode). DE1C: CSI-2 Port E Data Lane 1 C-Output (C-PHY 2-Lane Mode).
43	DB2P	DB2P	CSI-2 Port B Data Lane 2 Noninverted Output (D-PHY 4-Lane Mode).
44	DB2N	DB2N	CSI-2 Port B Data Lane 2 Inverted Output (D-PHY 4-Lane Mode).
47	DB3P	DB3P	CSI-2 Port B Data Lane 3 Noninverted Output (D-PHY 4-Lane Mode).
48	DB3N	DB3N	CSI-2 Port B Data Lane 3 Inverted Output (D-PHY 4-Lane Mode).



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MAX96792A**

PIN	NAME	FUNCTION MODE	FUNCTION
		GMSL3/2	
MULTIFUNCTION PINS (NOTE: LEAVE PINS OPEN IF UNUSED)			
2	MFP0	GPIO0* SDA1 RX1 SDA2 RX2 SCLK FRSYNC_OUT VS2 DE1/DV1 MS	GPIO0: Configurable General-Purpose Input or Output. Power-up default is GPIO general-purpose input with a 1MΩ pulldown to ground. SDA1: Pass-Through I <sup>2</sup> C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . RX1: Pass-Through UART Input with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . SDA2: Pass-Through I <sup>2</sup> C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . RX2: Pass-Through UART Input with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . SCLK: SPI Clock. When configured as a master, push-pull clock output. When configured as a slave, clock input with internal 1MΩ pulldown to ground. FRSYNC_OUT: Frame Sync Push-Pull Output. VS2: Video Stream Vertical Sync Monitor Push-Pull Output. DE1/DV1: Video Stream Data Enable or Data Valid Monitor Push-Pull Output. MS: UART Mode Select with Internal 1MΩ Pulldown to Ground. MS state can also be temporarily overwritten by a register write.
3	MFP1	LOCK* SCL1 TX1 SCL2 TX2 GPIO1	LOCK: Open-Drain Lock Indication Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . SCL1: Pass-Through I <sup>2</sup> C Clock Input/Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . TX1: Pass-Through UART Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . SCL2: Pass-Through I <sup>2</sup> C Clock Input/Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . TX2: Pass-Through UART Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . GPIO1: General-Purpose Input or Output.
4	MFP2/CFG0	GPO2* SS1 BNE CFG0	CFG0: Configuration Pin. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor-divider between V <sub>DDIO</sub> and EP. See <a href="#">Table 12</a> . GPO2*: General-purpose output. Power-up default is high impedance. SS1: SPI Slave Select. When configured as the master, Slave 1 Select push-pull output. BNE: When Configured as SPI Slave, SPI Buffer Not Empty Push-Pull Output. When BNE is high, SPI data is available.
8	MFP3/CFG1	GPO3* CFG1 VS1 DE0/DV0 SS2	GPO3: General-Purpose Push-Pull Output. Power-up default is high impedance. CFG1: Configuration Pin. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor-divider between V <sub>DDIO</sub> and EP. See <a href="#">Table 13</a> . VS1: Video Stream Vertical Sync Monitor Push-Pull Output. DE0/DV0: Video Stream Data Enable or Data Valid Monitor Push-Pull Output. SS2: SPI Slave Select. When configured as the master, Slave 2 Select push-pull output.



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MAX96792A

PIN	NAME	FUNCTION MODE	FUNCTION
		GMSL3/2	
9	MFP4	ERRB* GPIO4 RO(Alt)	ERRB: Open-Drain Error Indication Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . When ERRB is low, a data error, line fault, or interrupt is detected. ERRB is high when PWDNB is low. GPIO4: General-Purpose Input or Output. RO(Alt): When Configured as a Slave, SPI Mode-Select Input with an Internal 1MΩ Pulldown to Ground. When RO is high, enables a master read from MISO. When RO is low, enables a master write to MOSI.
21	MFP5	RX1* RX2 SDA1 GPIO5 SDA2 MOSI LOCK(Alt)	RX1: Pass-Through UART Input with an Internal 40kΩ Pullup to V <sub>DDIO</sub> (Default 1Mbps Rate). RX2: Pass-Through UART Input with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . SDA1: Pass-Through I <sup>2</sup> C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . GPIO5: Configurable General-Purpose Input or Output. Power-up default with a receiver enabled and open-drain driver high with an internal 40kΩ pullup to V <sub>DDIO</sub> . SDA2: Pass-Through I <sup>2</sup> C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . MOSI: SPI Master Out Slave In. When configured as master, the push-pull output drives data to the external slave. When configured as a slave, input with an internal 1MΩ pulldown to ground that receives data from external master. LOCK(Alt): Alternate Lock Indicator. Open-drain lock indication output with an internal 40kΩ pullup to V <sub>DDIO</sub> .
22	MFP6	TX1* TX2 SCL2 SCL1 GPIO6 MISO	TX1: Pass-Through UART Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> (Default 1Mbps Rate). TX2: Pass-Through UART Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> . SCL2: Pass-Through I <sup>2</sup> C Clock Input/Open-Drain Output with an Internal Pullup to V <sub>DDIO</sub> . SCL1: Pass-Through I <sup>2</sup> C Clock Input/Open-Drain Output with an Internal Pullup to V <sub>DDIO</sub> . GPIO6: Configurable General-Purpose Input or Output. Power-up default with a receiver enabled and open-drain driver high with an internal 40kΩ pullup to V <sub>DDIO</sub> . MISO: SPI Master In Slave Out. When configured as a master, input with an internal 1MΩ pulldown to ground that receives data from the external slave. When configured as a slave, push-pull output that drives data to an external master.
27	MFP7	GPI7* LMN0 RO	GPI7: General-Purpose Input with a 1MΩ Pulldown to Ground. LMN0: Line-Fault Monitor Input. RO: When Configured as a Slave, SPI Mode-Select Input with an Internal 1MΩ Pulldown to Ground. When RO is high, enables a master read from MISO. When RO is low, enables a master write to MOSI.
28	MFP8	GPI8* LMN1	GPI8: General-Purpose Input with a 1MΩ Pulldown to Ground. LMN1: Line-Fault Monitor Input.
45	MFP9	GPI9* LMN2	GPI9: General-Purpose Input with a 1MΩ Pulldown to Ground. LMN2: Line-Fault Monitor Input.
46	MFP10	GPI10* LMN3	GPI10: General-Purpose Input with a 1MΩ Pulldown to Ground. LMN3: Line-Fault Monitor Input.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MAX96792A**

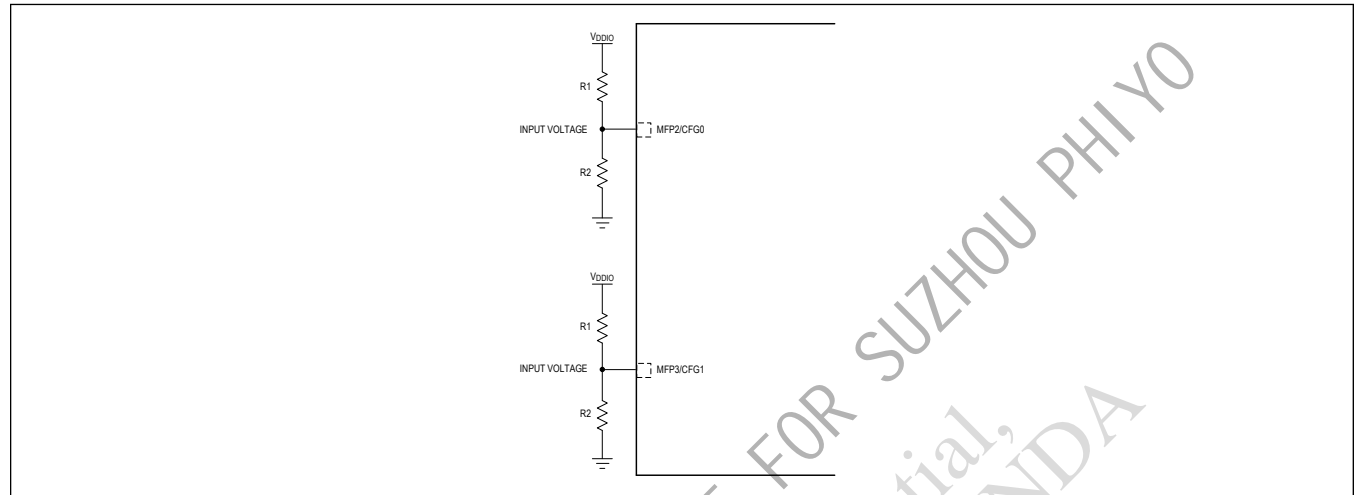
PIN	NAME	FUNCTION MODE	FUNCTION
		GMSL3/2	
10	MFP11	SDA RX* GPI11_ODO11	RX: UART Input with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SDA or RX Selected by CFG0 at Power-Up). SDA: I <sup>2</sup> C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> (SDA or RX Selected by CFG0 at Power-Up). GPI11_ODO11: General-Purpose Input and/or Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> .
11	MFP12	SCL TX* GPI12_ODO12	TX: UART Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> (SCL or TX Selected by CFG0 at Power-Up). SCL: I <sup>2</sup> C Clock Input/Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> (SCL or TX Selected by CFG0 at Power-Up). GPI12_ODO12: General-Purpose Input and/or Open-Drain Output with an Internal 40kΩ Pullup to V <sub>DDIO</sub> .
<b>MISCELLANEOUS -SEE EXTERNAL COMPONENTS REQUIREMENTS TABLE</b>			
1	PWDNB	PWDNB	PWDNB: Active-Low, Power-Down Input with an Internal 1MΩ Pulldown to Ground. Set PWDNB Low to Enter Power-Down Mode.
12	X1/OSC	X1/OSC	Crystal/Oscillator Input. If a crystal is used, connect to one terminal of a 25MHz ±200ppm crystal and connect a load capacitor from X1/OSC to EP (load capacitor value depends on crystal used). If an oscillator is used, supply a 25MHz ±200ppm signal.
13	X2	X2	Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal and connect a load capacitor from X1/OSC to EP (load capacitor value depends on crystal used). Leave open if an oscillator is used.
15	XRES	XRES	Used to Calibrate SIO Output Driver Swings. Connect a 402Ω ±1% resistor between XRES and EP.
19	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1V Core Supply.
14	RSVD	RSVD	Reserved. Do not connect.
<b>POWER SUPPLIES - SEE EXTERNAL COMPONENT REQUIREMENTS TABLE</b>			
16	V <sub>DD18</sub>	V <sub>DD18</sub>	1.8V Analog Supply.
7	V <sub>DD18</sub>	V <sub>DD18</sub>	1.8V Analog Supply.
20	V <sub>DD</sub>	V <sub>DD</sub>	1.0V Core Supply. This pin includes an optional on-chip LDO. Connect a 0.95V to 1.05V supply to bypass LDO. Connect a 1.14V to 1.26V supply to use the internal 1.0V regulator. To use the internal 1V regulator, first write REG_ENABLE=1, and then write REG_MNL=1. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
24	V <sub>DDIO</sub>	V <sub>DDIO</sub>	1.8V to 3.3V I/O supply.
23	V <sub>TERM</sub>	V <sub>TERM</sub>	1.14V to 1.26V MIPI supply. Bypass V <sub>TERM</sub> to EP with a 0.1μF capacitor placed as close as possible to the device.
EP	EP	EP	Exposed Pad. EP is internally connected to device ground. EP MUST be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

MAX96792A

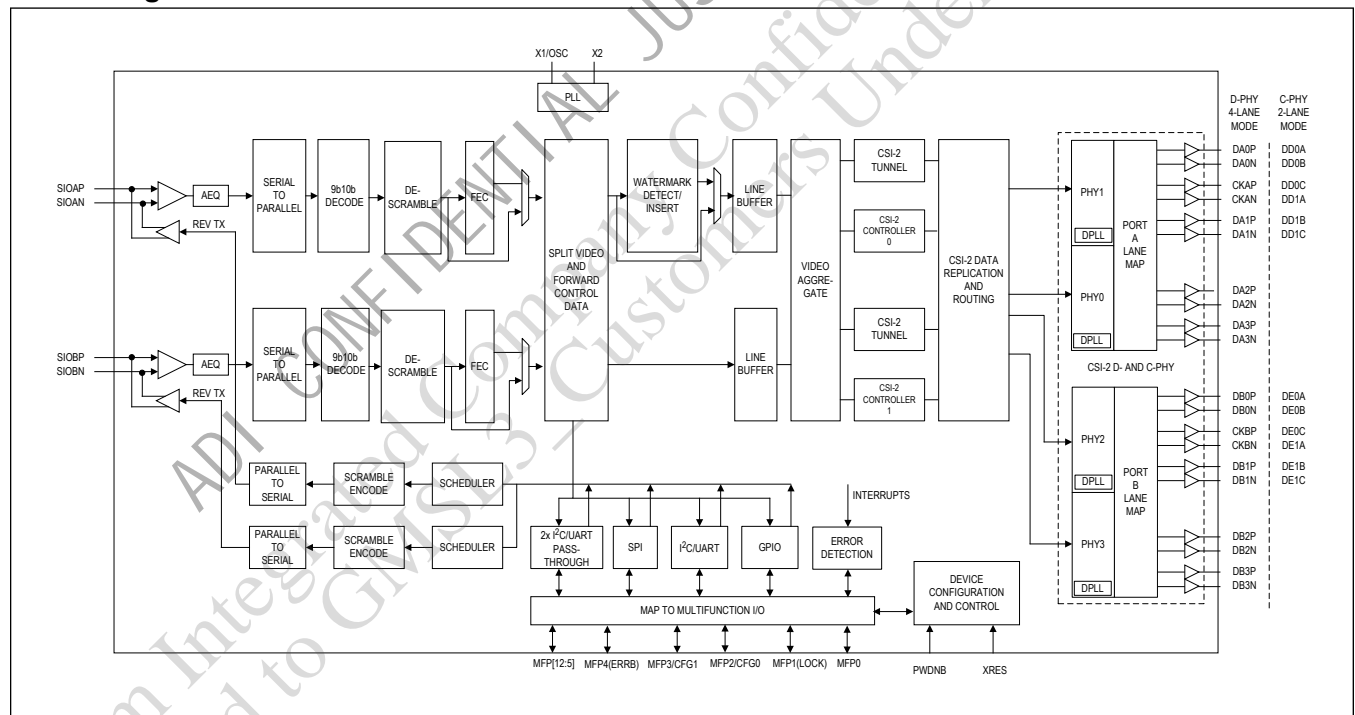
Dual GMSL3/2 to CSI-2 Deserializer

## Functional Block Diagram

### Configuration Pin Connections



### Block Diagram



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

## Detailed Description

## Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews, and register definitions. The following information is needed to correctly design with this device:

- The **GMSL3 Channel Specification** and **GMSL2 Channel Specification** contain physical layer requirements for the PCB traces, cables, and connectors for GMSL3 12Gbps PAM4 links and GMSL2 3Gbps or 6Gbps NRZ links, respectively.
- The **GMSL2 Hardware Design Guide** contains recommendations for PCB design, applications circuits, selection of external components, and guidelines for use of GMSL2 signal integrity tools.
- The **GMSL2 User Guide** and **GMSL3 User Guide** contain detailed programming guidelines for device features.
- **Errata sheets** contain deviations from published device specifications, and are specific to part number and revision ID.

Contact the factory for these documents and additional guidance on MAX96792A features.

## Recommended Operating Conditions

Table 2. Recommended Operating Conditions

PARAMETER	PIN NAME	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Voltage Range	V <sub>TERM</sub>		1.14	1.2	1.26	V
	V <sub>DD18</sub>		1.7	1.8	1.9	
	V <sub>DD</sub>	1.0V	0.95	1.0	1.05	
		1.2V	1.14	1.2	1.26	
	V <sub>DDIO</sub>	1.8V	1.7	1.8	1.9	
		3.3V	3.0	3.3	3.6	
Maximum Supply Noise (Note a)	V <sub>TERM</sub>			50		mV <sub>P-P</sub>
	V <sub>DD18</sub>			25		
	V <sub>DD</sub>	1.0V		50		
		1.2V		50		
	V <sub>DDIO</sub>	1.8V		50		
		3.3V		100		
Operating Junction Temperature, T <sub>J</sub>			-40		+125	°C

Note a: Supply noise < 1MHz. Supply voltage ripple is assumed to be symmetric around the measured DC supply voltage. For example, 25mV<sub>P-P</sub> means ±12.5mV peak voltage.

## ESD Protection

Table 3. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIO <sub>__</sub>	V <sub>ESD</sub>	Human Body Model (HBM), R <sub>D</sub> = 1.5kΩ, C <sub>S</sub> = 100pF		±8		kV
		ISO10605, R <sub>D</sub> = 330Ω, C <sub>S</sub> = 150pF, Contact Discharge		±6		
		ISO10605, R <sub>D</sub> = 330Ω, C <sub>S</sub> = 150pF, Air Discharge		±6		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V <sub>ESD</sub>	Human Body Model (HBM), R <sub>D</sub> = 1.5kΩ, C <sub>S</sub> = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

## External Component Requirements

**Table 4. External Component Requirements**

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
XRES	R <sub>XRES</sub>	Connect R <sub>XRES</sub> resistor between XRES pin and ground.	402 ±1%. Use a single resistor	Ω
Line-Fault Pulldown Resistor	R <sub>PD</sub>	Connect to ground at far end of Coax/STP cable; only required if line-fault detection is used.	49.9 ±1%	kΩ
Line-Fault Series Resistor - Coax Mode	R <sub>EXT1</sub>	LMN0, LMN1, LMN2, or LMN3	48.7 ±1%	kΩ
	R <sub>EXT2</sub>		DNI	
Line-Fault Series Resistor - STP Mode	R <sub>EXT1</sub>	See Line-Fault Section in <a href="#">Detailed Descriptions</a> for STP Mode.	48.7 ±1%	kΩ
	R <sub>EXT2</sub>	See Line-Fault Section in <a href="#">Detailed Descriptions</a> for STP Mode.	42.2 ±1%	
Link Isolation Capacitors	C <sub>LINK</sub>	Place close to the SIO_ pins (5, 6, 17, 18) used in the application.	0.1	μF
Coax Mode Termination Resistor	R <sub>TERM</sub>	In Coax mode, connect R <sub>TERM</sub> between unused SIO pin and ground on each Coax link.	49.9 ±1%	Ω
Crystal		Place as close as possible to pins 12 and 13.	25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values that compensate for the X1 and X2 input, and PCB node capacitances. Place the capacitors as close as possible to pin 12 (X1/OSC) and pin 13 (X2).		
V <sub>DDIO</sub> Decoupling Capacitor*		Place a 0.01μF capacitor as close as possible to pin 24. Include a minimum of 10μF bulk decoupling on the PCB.	0.01 + 10	μF
V <sub>DD18</sub> Decoupling Capacitors*		Place a 0.01μF capacitor as close as possible to pins 7 and 16. Connect both V <sub>DD18</sub> pins together and include a minimum of 10μF bulk decoupling on the PCB.	(2x) 0.01 + 10	μF
V <sub>TERM</sub> Decoupling Capacitor*		Place a 0.01μF capacitor as close as possible to pin 23. Include a minimum of 10μF bulk decoupling on the PCB.	0.01 + 10	μF
V <sub>DD</sub> Decoupling Capacitor*		Place a 0.1μF capacitor as close as possible to pin 20. Include a minimum of 10μF bulk decoupling on the PCB.	0.1 + 10	μF
CAP_VDD Decoupling Capacitor		Place a 0.1μF capacitor as close as possible to pin 19. Include a minimum of 10μF bulk decoupling near the pin.	0.1 + 10	μF
Open-Drain Pullup Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations.		
Resistors for Configuration Pin Resistor-Divider	R1, R2	Place resistor-divider close to pin 4 (MFP2/CFG0).	See <a href="#">Table 12</a> .	Ω
	R1, R2	Place resistor-divider close to pin 8 (MFP3/CFG1).	See <a href="#">Table 13</a> .	Ω

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

\* With exception of CAP\_VDD, power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

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## Figures

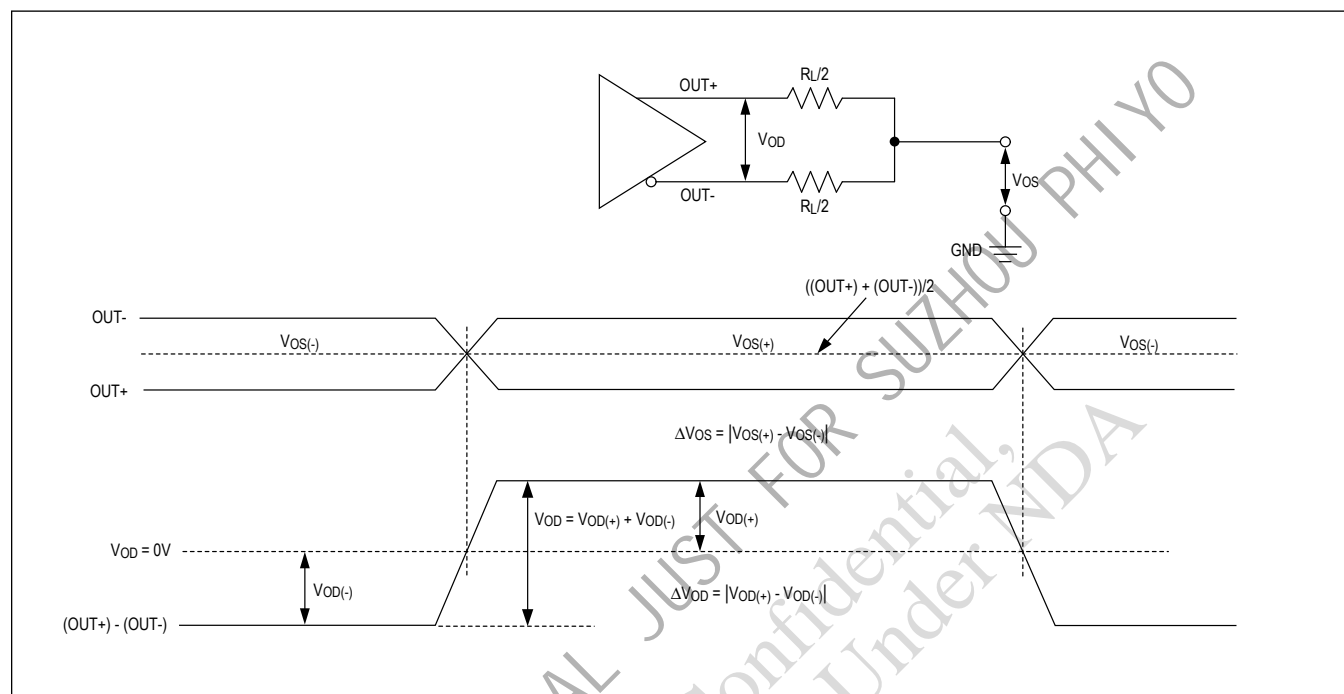


Figure 1. GMSL3 Reverse-Channel Serial Outputs

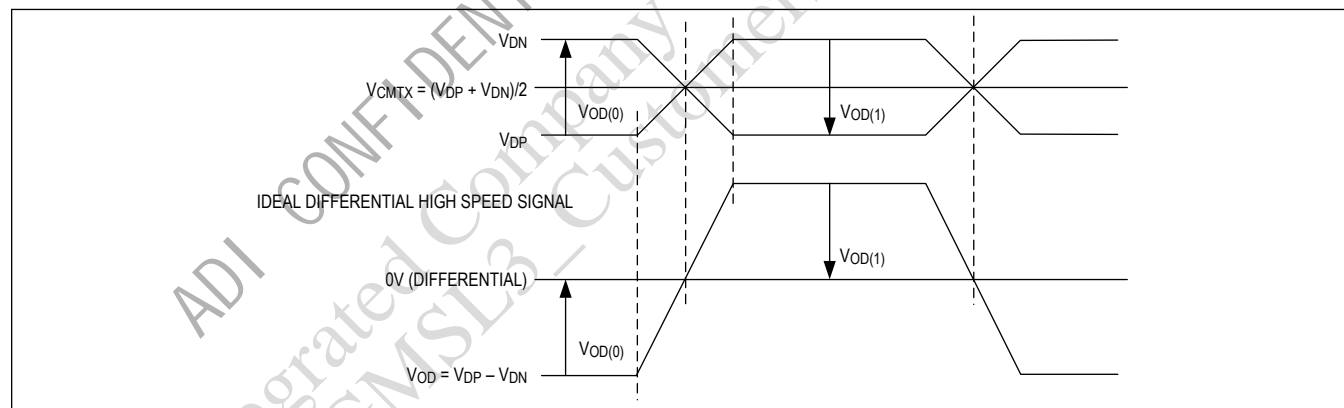


Figure 2. Ideal Single-Ended and Resulting Differential HS Signals

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MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

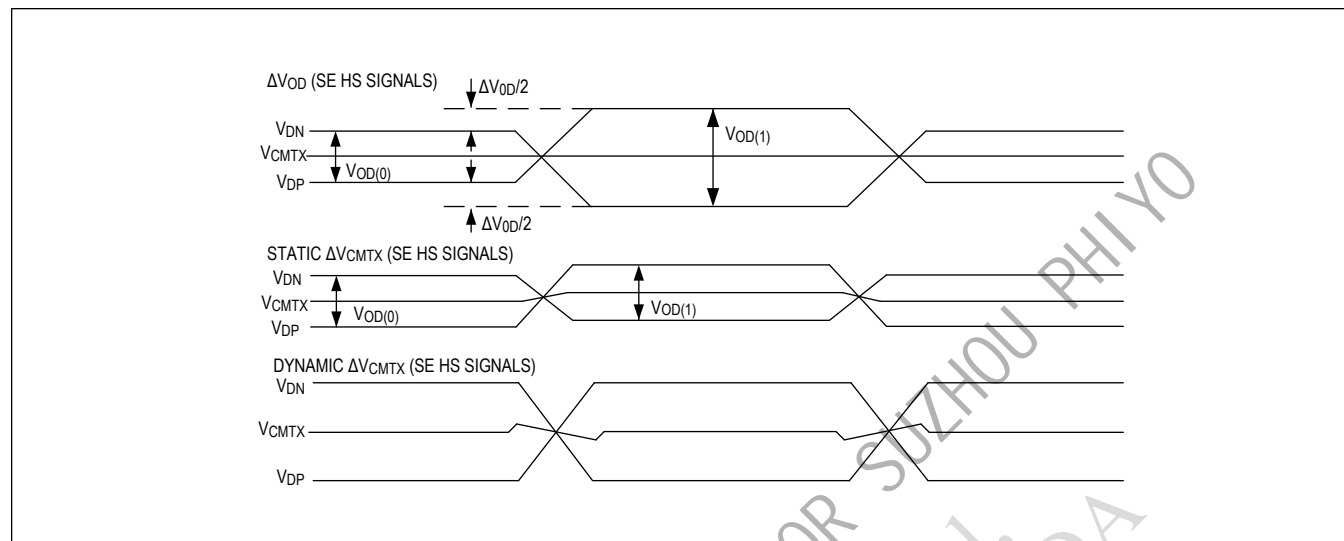


Figure 3. Possible Delta  $V_{CMTX}$  and Delta  $V_{OD}$  Distortions of Single-Ended HS Signals

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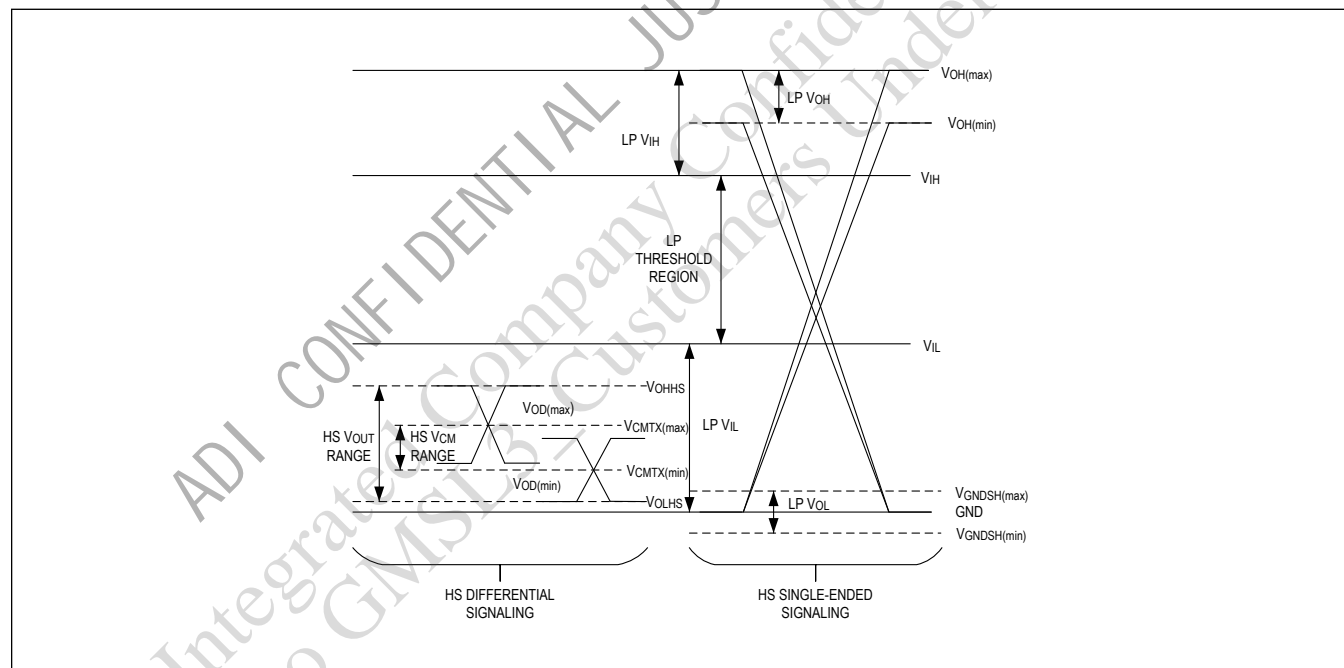


Figure 4. D-PHY Signaling Levels

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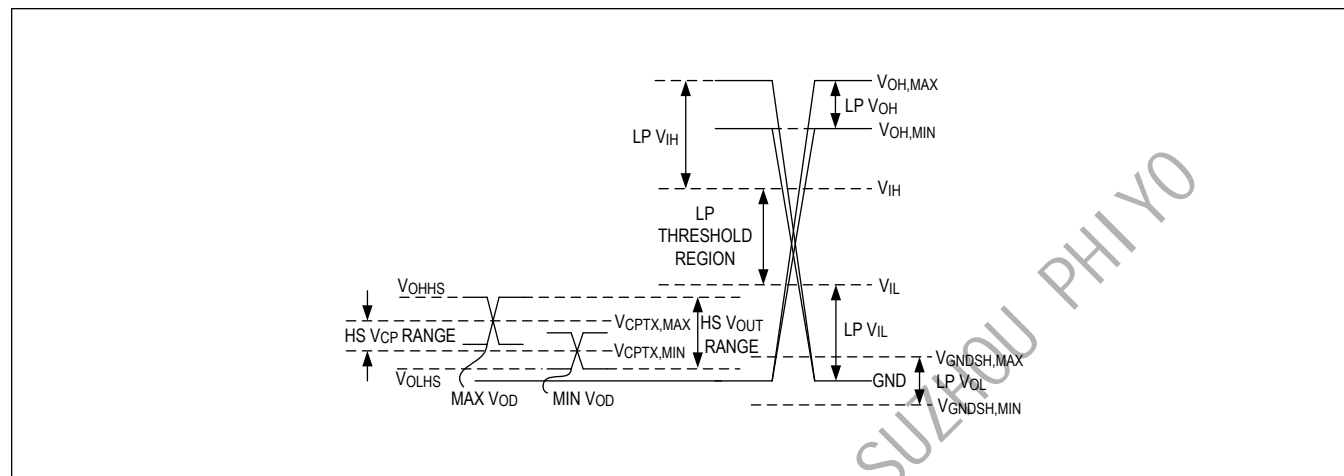


Figure 5. C-PHY DC Characteristics

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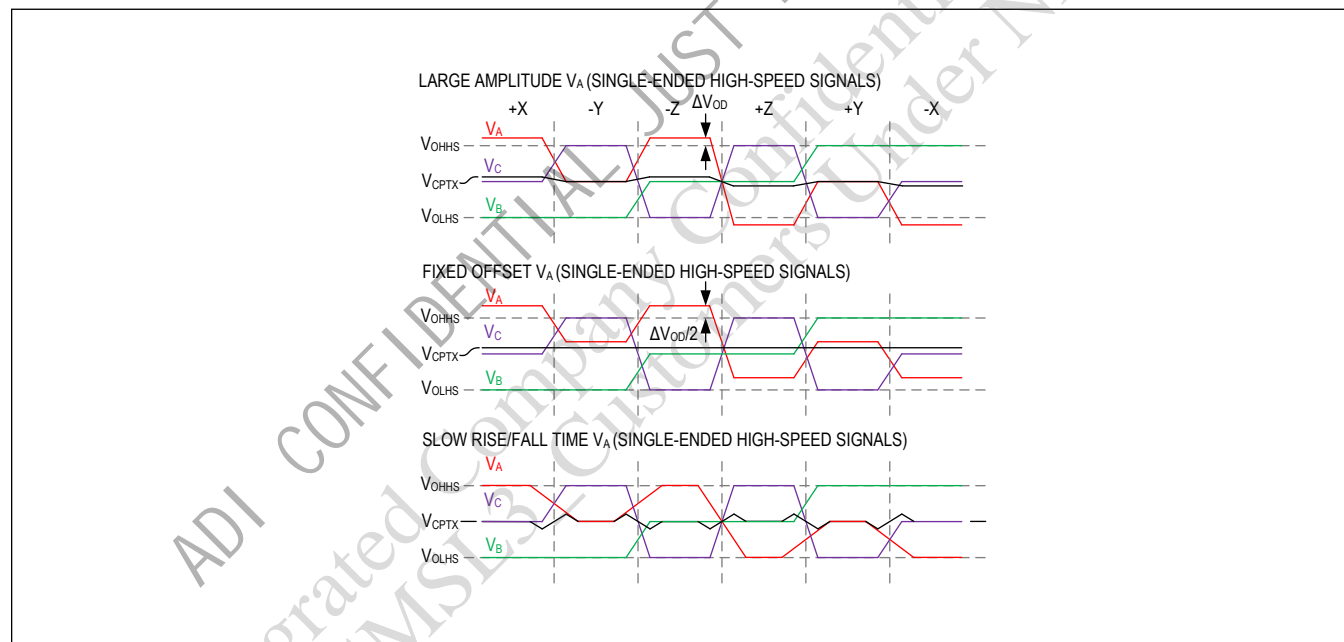


Figure 6. C-PHY Possible  $\Delta V_{CPTX}$  and  $\Delta V_{OD}$  Distortions of Single-Ended HS Signals

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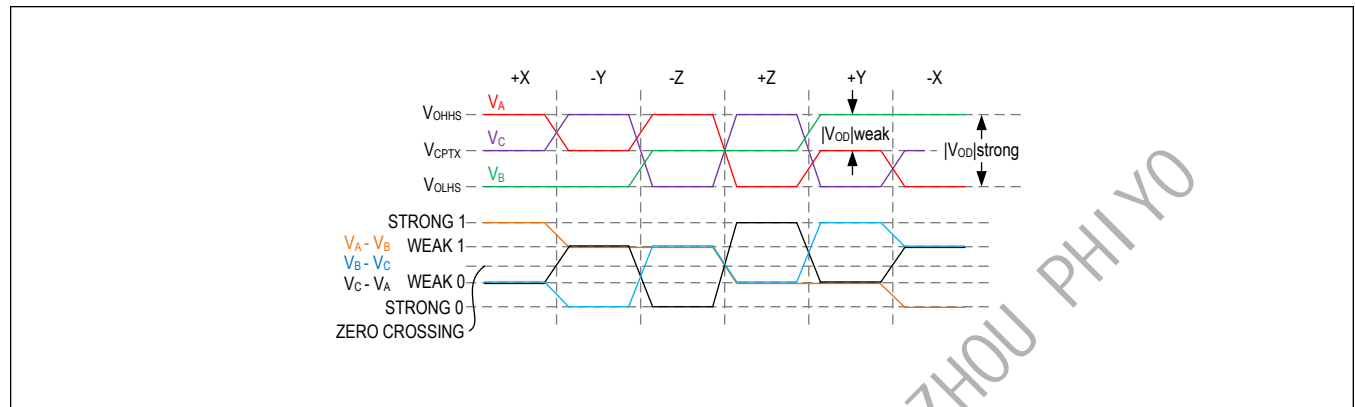


Figure 7. C-PHY Ideal Single-Ended and Resulting Differential High-Speed Signals

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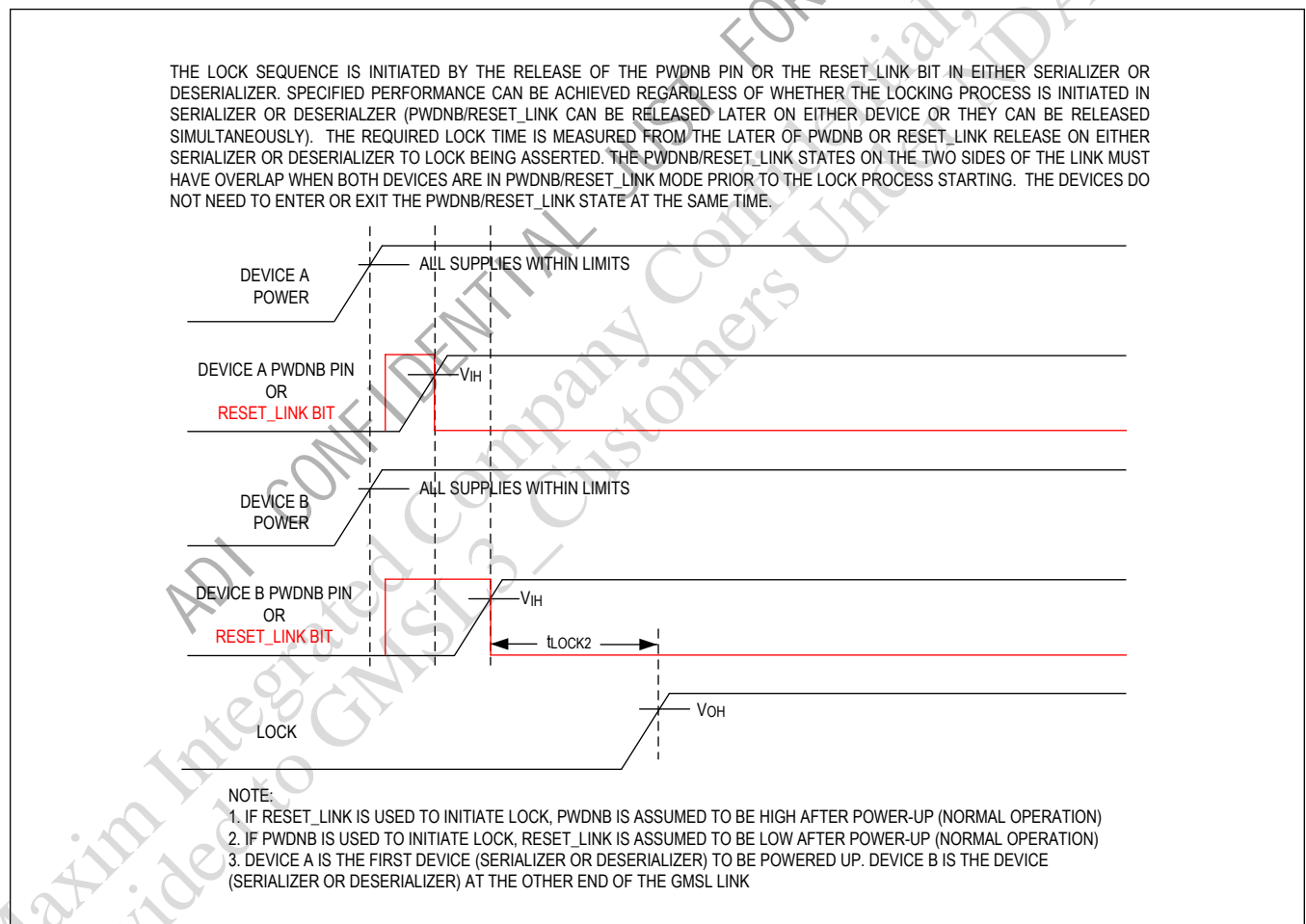


Figure 8. Lock Time

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Dual GMSL3/2 to CSI-2 Deserializer

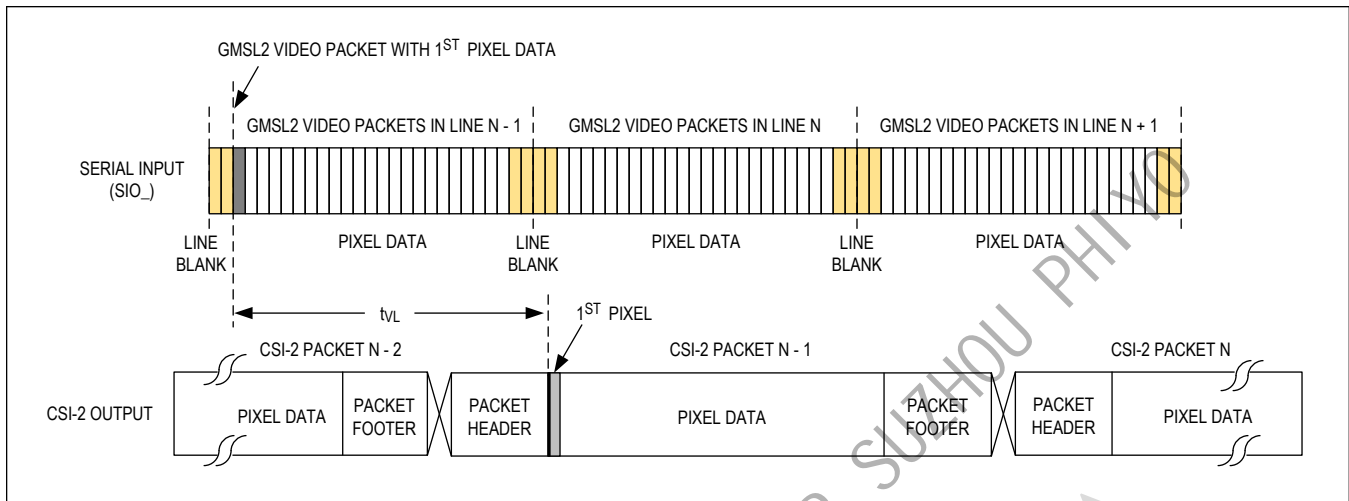


Figure 9. GMSL3 Video Latency

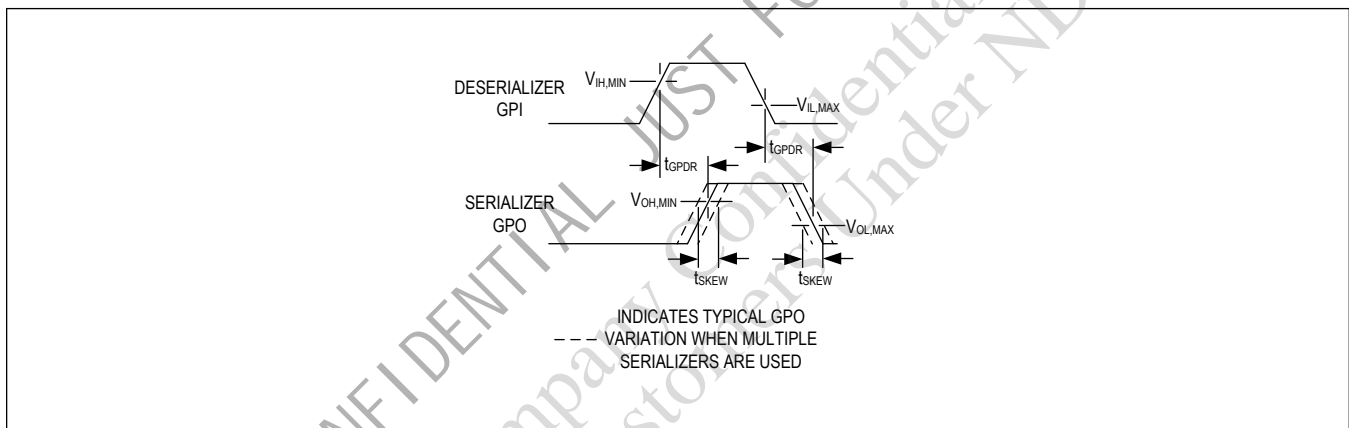


Figure 10. GPI-to-GPO Delay and Skew

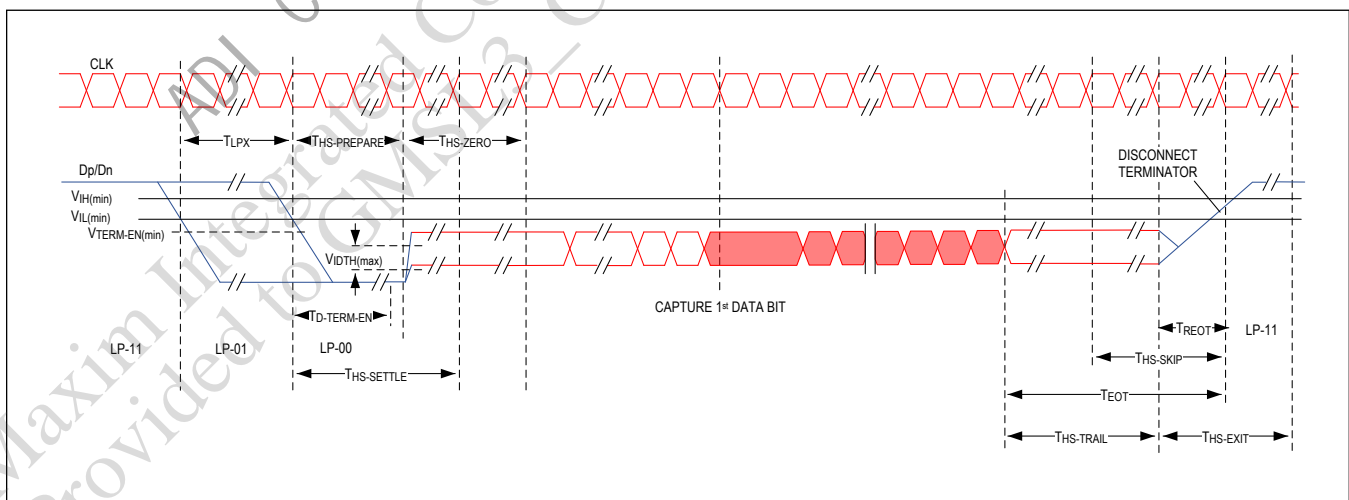
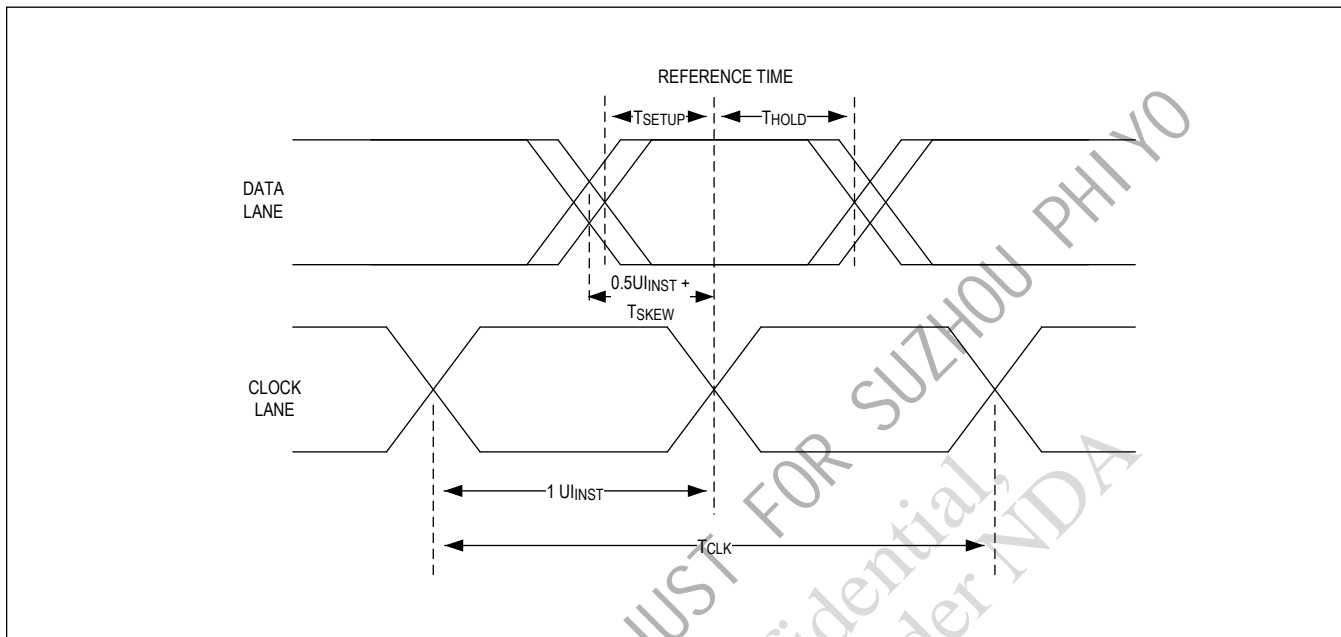


Figure 11. D-PHY High-Speed Data Transmission in Bursts. Reference: MIPI Specification for D-PHY v. 1.2, 01-Aug 2014

## MAX96792A

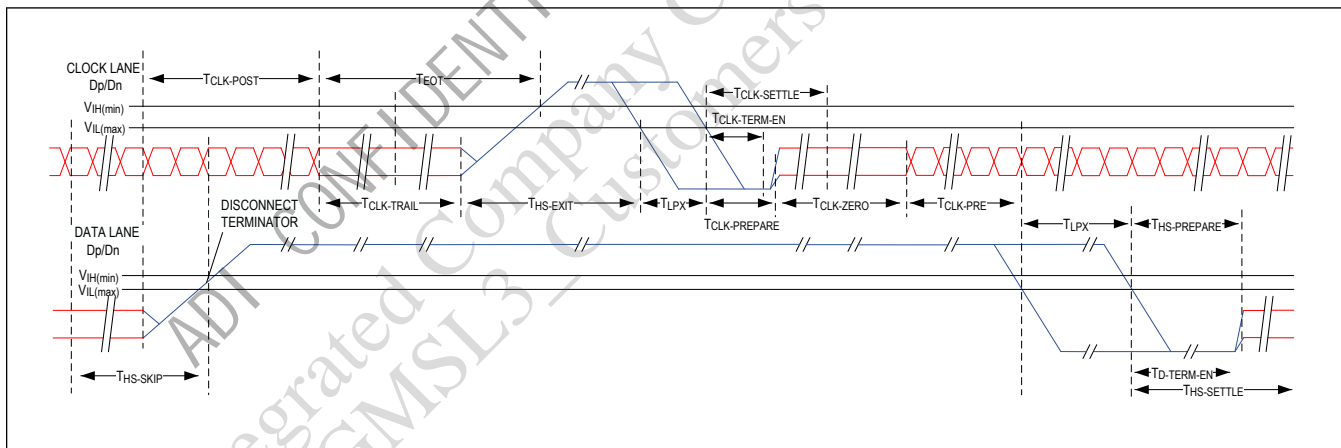
## Dual GMSL3/2 to CSI-2 Deserializer

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**Figure 12. D-PHY Data Clock Timing**

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**Figure 13. Switching the Clock Lane between Clock Transmission and Low-Power Mode**

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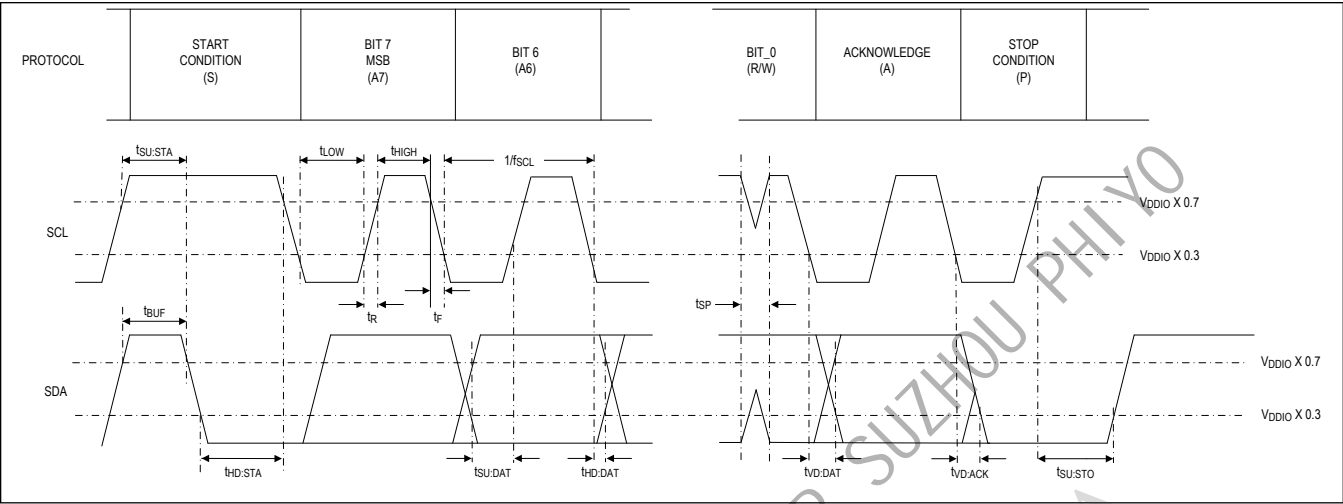


Figure 16. I<sup>2</sup>C Timing Parameters

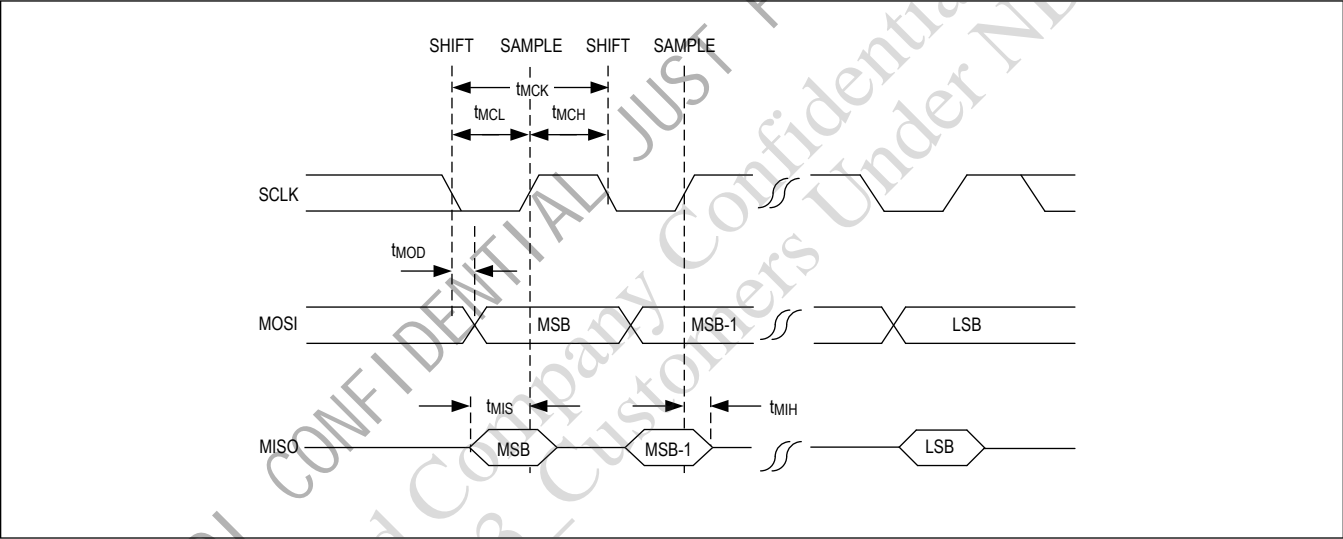


Figure 17. SPI Master-Mode Timing Parameters

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

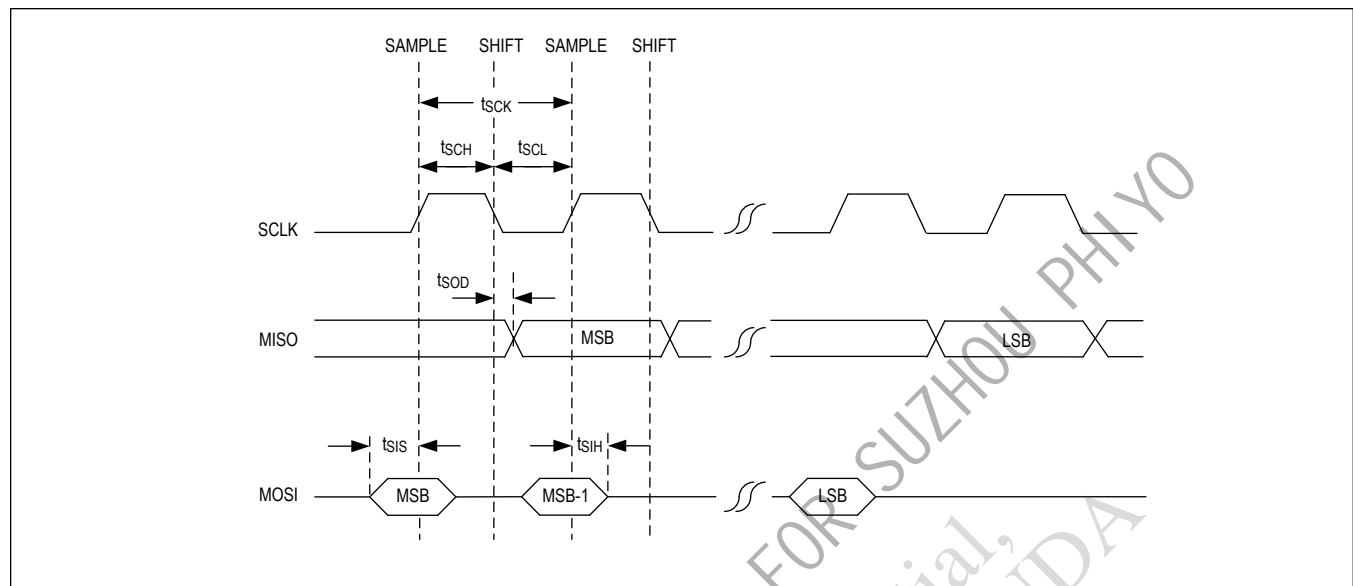


Figure 18. SPI Slave-Mode Timing Parameters

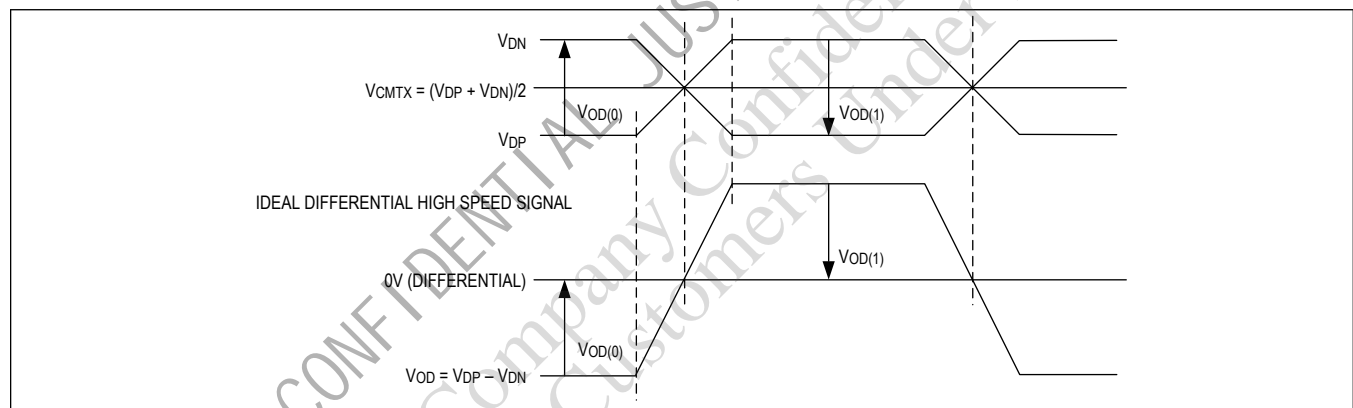


Figure 19. Ideal Single-Ended and Resulting Differential HS Signals

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### Introduction

Analog Devices' GMSL3 serializers and deserializers provide high-speed, low bit-error-rate, bidirectional serial data transport. They support a comprehensive suite of sensor and communication interfaces over a single wire. The MAX96792A deserializer supports two modes of operation to transmit MIPI CSI-2 data over the line. The pixel-mode offers flexible video data transfer, while the tunneling-mode provides bandwidth-efficient CSI-2 video data transfer with inherent end-to-end data integrity.

GMSL3 deserializers support up to 12Gbps forward and 187.5Mbps reverse packetized-data transmission over each fixed-speed link. The MAX96792A's inputs can be aggregated such that incoming data from two remotely located sensors is combined and routed to any available combination of CSI-2 outputs. Once aggregated, the data can also be replicated to drive two SoCs.

The following sections provide a brief overview of the device functions and features. Contact the factory for additional information, and details on configuration of each function and feature.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

### Product Overview

The MAX96792A GMSL3/2 dual-channel deserializer converts data on single or dual GMSL serial inputs to CSI-2 packets on one or two CSI-2 output ports. It also sends and receives side-channel data, enabling full-duplex transmission of forward-path sensor data and bidirectional data over low-cost 50Ω Coax or 100Ω STP cables meeting the GMSL3 channel specification.

The MAX96792A's CSI-2 output interfaces are configurable as C-PHY or D-PHY. The interfaces can be configured as dual four-lane D-PHY v1.2 or a dual two-lane C-PHY v1.0 output ports. The number of active D-PHY v1.2 data lanes is programmable as one, two, three, or four lanes. The C-PHY interface is programmable as one or two lanes. Supported data types include RAW8/10/12/14/16/20, RGB555/666/888/YUV422 8/10-bit, user-defined and generic long-packet data types. Up to 16 virtual channels are also supported.

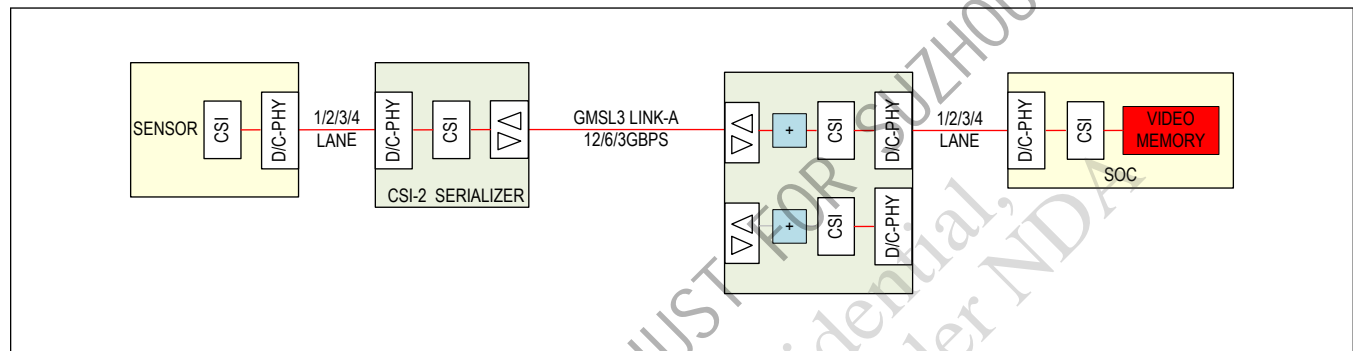


Figure 20. Single Link

A basic use-case is a single sensor having a MIPI D-PHY output, as shown in [Figure 20](#) with the sensor's output sent to an SoC at a data rate of 3Gbps, 6Gbps, or 12Gbps. Two GMSL2 or GMSL3 serializers can be used with one MAX96792A deserializer to connect two sensors to one or two SoCs. The cable types, sensor timing, and data rates do not have to be the same, the links can be set to either forward rate (both 6Gbps or 12Gbps). See [Figure 21](#). Data from Link A and Link B are output on separate, dedicated CSI-2 ports for capture by the SoC. Dedicated ports allow an SoC with slower D-PHY lanes to capture data from two sources.

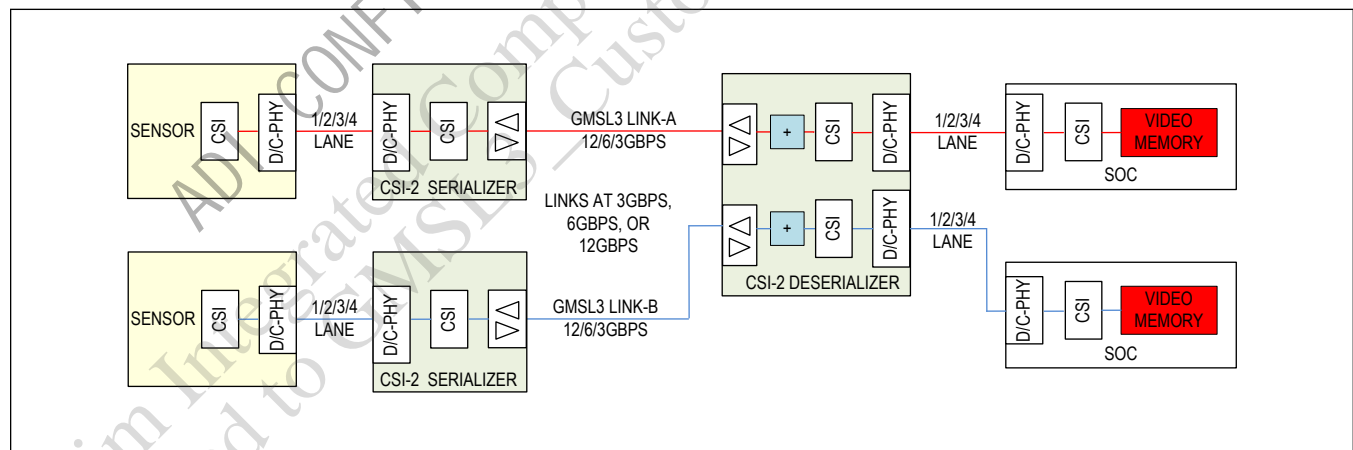


Figure 21. Dual Link, Separate Data

The MAX96792A supports data aggregation, as detailed in [Figure 22](#). The sources can have different video timing and resolution, the serial links can be set to either forward rate (3Gbps, 6Gbps, or 12Gbps). The SoC identifies the video source by reading the packet's virtual channel or data type. If both sources use the same virtual channel or data type, the MAX96792A can assign a different virtual channel and/or data type (16 are available) if the part is operated in the



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

pixel mode. The aggregated data can be replicated and output on both MIPI ports, allowing multiple SoCs to process the same data, as shown in [Figure 23](#).

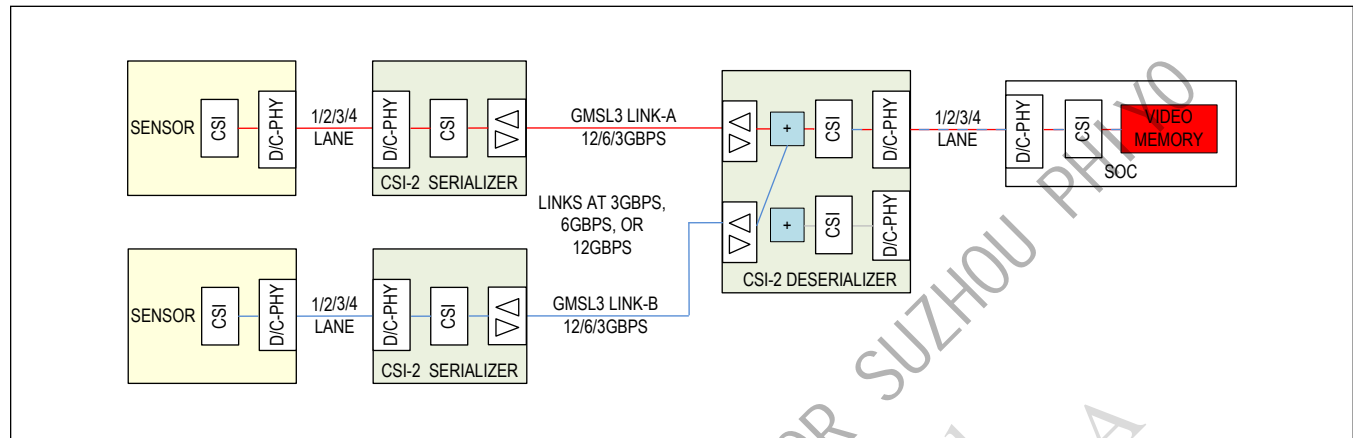


Figure 22. Dual Link, Data Aggregation

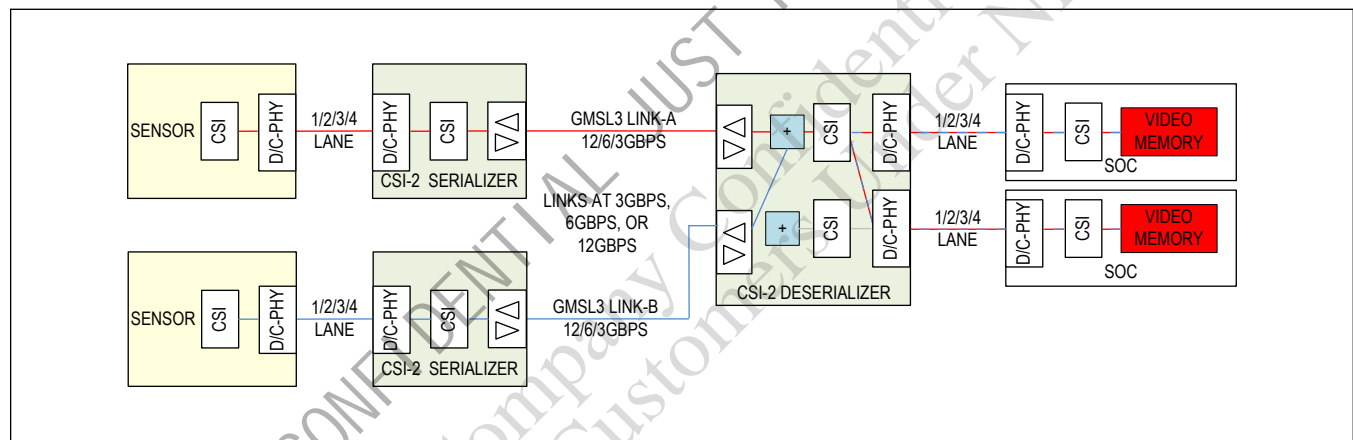


Figure 23. Dual Link, Data Aggregation and Replication

The MAX96792A is an ideal sensor deserializer when cameras are connected to an SoC with CSI-2 input. RADAR and LiDAR sensors can also be supported where a high-speed SPI is generally required.

### GMSL3 Overview

GMSL3 is a fixed-rate protocol designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or from an external reference frequency. The link clock is not related to the video pixel clock beyond the natural constraint that the video bandwidth cannot exceed the available link bandwidth.

GMSL3 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth. The same data protocol is used on forward and reverse channels, and for both video and control-channel data.

GMSL3 supports a comprehensive suite of common embedded communication protocols. All devices utilize a primary I<sup>2</sup>C/UART control-channel interface that an Electronic Control Unit (ECU) uses to access serializer and deserializer

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

registers, as well as peripheral devices. This access can be initiated from either end of the link. Devices include two additional I<sup>2</sup>C/UART ports to access lower priority local registers or communicate with remote peripherals. These pass-through ports do not have access to the device registers.

An SPI master/slave is also included. The Serial Peripheral Interface (SPI) enables a host SPI master on one side of the GMSL3 link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL3 devices. A GMSL3 device can be configured as either an SPI master or a slave. The SPI port functions exclusively as a pass-through port without access to serializer or deserializer registers.

All GMSL3 devices include a versatile suite of General Purpose Input/Output (GPIO) pins that work with the GMSL3 peripheral communication protocols. In general, the GPIOs function as user-defined inputs or outputs whose states can be either automatically forwarded across the link or controlled by register settings. GPIOs are typically used to tunnel low-speed (< 100Kbps) signals over the GMSL3 link, although rates in excess of 1MHz are also supported. A GPIO tunnel can be set up in the forward or reverse direction.

GMSL3 provides extensive data integrity and safety features, including watermark generation/detection, Cyclic Redundancy Check (CRC) error detection for control and video data, and Error Correction Code (ECC) protection of video memory. Watermark generation and detection verify the video image is not frozen. CRC error detection identifies errors in the video or control-data streams. For control-channel CRC errors, automatic retransmission of the flagged packet maximizes control-channel speed and reliability. The internal video memory includes ECC protection to detect and correct internally-corrupted pixel data.

GMSL3 devices incorporate numerous link-margin optimization and monitoring functions that ensure high link margin and robust functionality. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor function provides continuous link-margin diagnosis and includes various threshold alarm levels that trigger runtime alerts whenever link degradation is detected. Pseudorandom Binary Sequencing (PRBS) checking verifies correct link and video channel operation.

### Link Error Generator

Each GMSL link includes a configurable error generator that injects errors into the outgoing data stream immediately prior to transmission. The deserializer injects errors into the reverse channel and the serializer injects errors into the forward channel. The receiving device detects, counts, and flags the errors, enabling a thorough validation of the system's response to error conditions of varying severity.

### Video Pipeline in Pixel Mode

The video channel is designed to receive and decode video data received from the GMSL3 serializer, and transport it to the CSI-2 output ports. Data types supported are RGB888, RGB666, RGB565, YUV422-8, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20, user-defined, embedded, and null. Video input data consists of color, Horizontal Sync (HS), and Vertical Sync (VS) synchronous to the PCLK. Video flows through the design as described in the following sections.

### Watermarking

The watermarking block detects a frozen frame failure in a frame-based processing system between the generator and detector. This feature specifically detects frozen frames caused by SoCs in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector. Most GMSL2 and GMSL3 devices contain both a watermark generator and detector. This allows both serializers and deserializers to insert or detect a watermark in a safety-relevant video stream. The watermark generator inserts a time-varying watermark that is highly redundant and robust to image processing and display stream compression. The watermark detector looks for this time-varying watermark, and failure to detect all the generated watermarks indicates a frozen-frame failure between the generator and detector in a frame-based processing system. Upon detection of this error condition, the watermark detector can generate an interrupt and/or blank the output video, returning the display to a safe state in less than 500ms.

### Video (Data) Line CRC

The MAX96792A includes a 32-bit video-line CRC error checker to guarantee the integrity of each video line transported across the GMSL3 link. A video-line CRC is generated on the serializer side of the link, and is transferred over the link to the MAX96792A along with the corresponding video data. The MAX96792A compares the CRC received from the serializer with the CRC it generated for a given video line. Any discrepancy between the CRC codes indicates an error in the video data.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

**Vertical and Data Enable or Data Valid Sync Outputs**

The MAX96792A can output the Vertical Sync (VS) and Data Enable/Valid (DE/DV) of a video stream to monitor video timing by a processor. This feature provides access to VS and DE/DV signals unavailable directly at the CSI-2 output. VS and/or DE/DV outputs are alternate functions of MFP0 and MFP3.

**Control-Channel and Side Channels**

A  $\mu$ C or other controller can send and receive control and side-channel data over the GMSL3 serial link simultaneously with high-speed video data. The MAX96792A supports the following interfaces:

- Main I<sup>2</sup>C/UART (internal access)
- Pass-through I<sup>2</sup>C/UART
- SPI
- GPIO

All the above interfaces can pass data through the GMSL3 link, but the GMSL3 device registers can be accessed and configured only through the main I<sup>2</sup>C/UART interface.

The side channel, with its various interfaces, is accessed using multifunction pins. Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit in the number of pins available on a given device, not all interfaces can be simultaneously supported. See [Pin Descriptions](#) and [Table 14](#) for default and alternate multifunction pin functions, as well as available combinations of interfaces.

**Main I<sup>2</sup>C/UART**

The main I<sup>2</sup>C/UART is located on the SDA\_RX and SCL\_TX pins of each GMSL3 device. The I<sup>2</sup>C (SDA, SCL) or UART (Tx, Rx) interface is selected by the CFG0 pin voltage at power-up (see [Table 12](#)). The selected interface provides master access to both GMSL3 registers and device registers from either end of the link.

The master microcontroller ( $\mu$ C) can reside on either end of the link (usually the serializer side for display applications and deserializer side for camera applications). The MAX96792A supports dual master microcontrollers, provided that software arbitration (such as token passing) is used to prevent packet collisions. The control channel allows only one master  $\mu$ C to communicate at a time.

To configure peripheral devices over the link, the GMSL3 serializer and deserializer must use the same control-channel interface (both I<sup>2</sup>C or both UART). Unlike legacy GMSL1 devices, there is no I<sup>2</sup>C-to-UART conversion capability. I<sup>2</sup>C/UART outputs are open-drain and require appropriately sized external pullup resistors for proper operation.

For detailed main channel programming information, see the [Control-Channel Programming](#) section under [Applications Information](#).

**I<sup>2</sup>C/UART CRC and Message Counter**

The MAX96792A provides additional functional safety by adding an optional CRC to I<sup>2</sup>C/UART read/write transactions and a separate message counter for read and write packets. These features are disabled by default and can be enabled by register programming. The CRC and message counter can be used together or individually. The CRC and message counter features only apply to device register read/write transactions and are not supported for pass-through traffic. The CRC and/or message counter can be enabled in the serializer, deserializer, or both.

The first CRC byte covers the data for the first 6 bytes: Device Address, Register Address MSB, Register Address LSB, Message Counter MSB, Message Counter LSB, and the first data byte. If there are multiple data bytes after the first byte, then a CRC byte is appended after each subsequent data byte. The CRC engine is reset to 0 after each CRC calculation is completed, meaning a fresh CRC calculation is done for each additional byte. The CRC polynomial for I<sup>2</sup>C/UART is  $P(x) = x^8 + x^6 + x^3 + x^2 + 1$ .

**Pass-Through I<sup>2</sup>C/UART**

The MAX96792A has two pass-through I<sup>2</sup>C/UART channels. These channels do not have access to registers in either the GMSL3 serializer or deserializer; they simply tunnel the I<sup>2</sup>C or UART signal across the GMSL3 link. This allows I<sup>2</sup>C channels to be separated so that no multimaster conflicts occur. I<sup>2</sup>C/UART outputs are open-drain and require appropriately-sized external pullup resistors for proper operation.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

**Serial Peripheral Interface (SPI)**

The MAX96792A enables a host SPI master on one side of the GMSL3 link to control a peripheral SPI slave on the opposite side. Communication may be in either direction across the GMSL3 link.

The SPI clock range is 600kHz to 25MHz. Care must be taken to meet set-up and hold-time requirements when using at speeds higher than 20MHz. The speed rating for each MFP must be set correctly for reliable operation. [Table 5](#) specifies the recommended drive strength and latching edge for the SPI as a function of SCLK speed.

**Table 5. SPI Latching Edge and Speed**

FREQUENCY	V <sub>DDIO</sub>	LATCHING EDGE	PIOX_SLEW[1:0]
<12.5MHz	1.7V to 2.24V	Opposite from Shift	01
	2.25V to 3.6V		10
12.5MHz to 25MHz	1.7V to 2.24V	Opposite from Shift	00
	2.25V to 3.6V		01

**General Purpose Input and Output (GPIO)**

The MAX96792A provides up to 13 GPIO/GPO/GPI, dependent on device feature utilization. GPIOs are typically used to tunnel low-speed (< 100Kbps) signals over the GMSL3 link, although rates in excess of 1MHz can also be supported. A GPIO tunnel can be set up in the forward or reverse direction. MFP pins can be programmed as GPI, GPO (push-pull output), or ODO (open-drain output).

Each GPIO pin can be configured as an input, output, or input/output by programming the GPIO\_TX\_EN and GPIO\_RX\_EN register bits of each GPIO pin. Note that unwanted loop behavior is avoided for pins configured as input/output; when the pin is driven by a transition received from the remote side, the driven GPIO transition is not transmitted back. GPIO pins may alternately be controlled and read solely from registers.

Most GPIO pins can be programmed for 1MΩ or 40kΩ pullup or pulldown (or none).

When a GPIO is programmed as GPO, the GPO can generally be programmed for open-drain or push-pull output.

A GPIO packet has 32 possible GPIO channel IDs. Each GPI is mapped to a channel ID according to the GPIO\_TX\_ID register. On the receiving end, each GPO outputs the received data with a programmed GPIO channel ID corresponding to the GPIO\_RX\_ID register for that pin. This provides flexibility in determining which GPIO input drives which GPIO output.

GPIO transmissions are transition-based; a GPIO packet is created and transmitted on the GMSL3 link when a rising-edge or falling-edge transition is detected at a GPIO pin. Several GPIO transitions at different GPIO pins can be grouped into a single packet. These pin transitions can be transmitted in two different modes: regular and delay-compensated.

The GPIO channel is not bandwidth efficient and should be used for low-speed signals only. Each GPIO transition uses 40 bits to 80 bits on the GMSL3 link for transmit and 40 bits to 60 bits on the reverse (due to received ACK packets). Bandwidth usage values vary based on channel configuration: (Automatic Repeat Request (ARQ) enable, CRC enable, and double-header enable, all impact channel bandwidth usage.

The state of each GPIO can be read or written by register, either locally or remotely, over the GMSL3 link by a μC using the control-channel I<sup>2</sup>C/UART interface. In non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible, based on priority and available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Use non-delay-compensated mode with signals tolerant to delay variation (i.e. μC interrupts). Priority can be set for GPI pins using registers. If no priority is set, GPI transitions are transmitted in the order they occur. However, when priority is set, transitions on GPI with higher priority are transmitter earlier.

Typical GMSL3 device delays for forward-link and reverse-link rates are shown in [Table 6](#).

**Table 6. Typical GPIO Delays for Forward-Link and Reverse-Link Transmission**

DIRECTION	DELAY COMPENSATION (TX_COMP_EN)	DELAY
GPIO forwarding from serializer to deserializer (6/3Gbps forward channel)	0	1μs

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**Table 6. Typical GPIO Delays for Forward-Link and Reverse-Link Transmission (continued)**

DIRECTION	DELAY COMPENSATION (TX_COMP_EN)	DELAY
GPIO forwarding from deserializer to serializer (187.5Mbps reverse channel)	1	3.5μs
	0	6μs
	1	15μs

**Delay in Non-Delay-Compensated Mode**

In the non-delay-compensated mode, the value of the transition is transmitted along with the GPIO channel ID. Note that GPIO channel latency is not fixed; the GMSL3 link has variable delay as a result of multiple communication channels sharing the link. A maximum latency limit is established by the GMSL3 bandwidth-sharing scheme, but significant fluctuation remains. Use the non-delay-compensated GPIO mode with signals invariant to the delay variations (e.g., μC interrupts).

**Delay-Compensated Mode**

In the delay-compensated mode (also called jitter compensation or jitter minimization compensation), a timestamp value is transmitted in addition to the value of the transition and GPIO channel ID. This timestamp is a high-resolution value sampled by an internal 600MHz clock that records when the GPIO transition is detected at the input. The remote-side chip uses the timestamp value to wait and output the GPIO transition after a total fixed delay from the GPIO input transition. This method mitigates possible variable latency issues by making the total GPIO input-to-output delay a precise, fixed value. Use the delay-compensated GPIO mode for signals for which the relative timing of rising and falling edges are important (e.g., Pulse-Width Modulation (PWM), camera frame-sync, radar ramp trigger, and low-speed Universal Asynchronous Receiver-Transmitter (UART) signals). The delay-compensated mode is enabled using TX\_COMP\_EN register fields for each GPIO.

**Frame-Sync**

In surround-view camera applications, the sensors usually require a frame-sync signal to synchronize the output of a frame with the other cameras in the system. Most GPIOs can be configured as GPI and linked to a frame-sync signal generated by a surround-view camera Electronic Control Unit (ECU).

**Control-Channel Retransmission on Error****Automatic Repeat Request/Automatic Retransmission (ARQ)**

Communications channels with control data (I<sup>2</sup>C/UART, GPIO, SPI) are relatively low bandwidth, but require the highest data-integrity protection. An optional automatic packet retransmission method, ARQ (Automatic Repeat Request), is employed here. ARQ works in conjunction with 16-bit packet CRC to detect if packets are received without error.

Packets are appended with a 2-bit sequence number at the transmit side and an acknowledge packet is sent from the receiver side upon successful receipt of each data packet. These packets are stored on the transmit side until acknowledged. If the acknowledge packet does not arrive in a predetermined interval, or the sequence number of the acknowledge packet does not match the expected value, the packet waiting at the top of the queue is automatically retransmitted.

The acknowledge packet uses the same header field as low-bandwidth packets, but begins with a different special symbol to distinguish it from regular data packets. This simplified format keeps retransmission exchanges independent from the communication channel. Note that this smaller packet format contains no data, obviating the need for full 16-bit CRC. Instead, the header symbol is sent twice in the packet, and the instances are checked against each other to ensure a match. The acknowledge packets also include a 2-bit sequence number that is the same sequence number of the correctly received data packet. The data packet transmitter tracks the acknowledged packets.

**Other Functions**

The devices include a video crossbar. The crossbar can be used to reorder the color and sync signals.



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

GMSL3 devices incorporate numerous link-margin optimization and monitoring functions to ensure high link margin. Continuous (1Hz) Adaptive Equalization (AEQ) optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor function for continuous link-margin diagnosis with various threshold alarm levels is available for runtime alerts of link degradation. Pseudorandom Binary Sequence (PRBS) checking verifies correct link and video-channel operation.

### Tunneling and Pixel Modes

The MAX96792A is specifically designed for Advanced Driver Assistance Systems (ADAS), where data integrity is a key safety requirement. Prior GMSL2 solutions supported only the pixel mode to transport MIPI CSI-2 data over the GMSL link. In the pixel mode, the CSI-2 headers and footers are removed in the serializer, and the video data is sent to one or more video pipes. The CSI-2 header includes the Data Type (DT) and Virtual Channel (VC), which is sent separately as an info-frame. The header also includes an ECC (Error Correction Code), which is also removed. The packet footer contains the CSI-2 CRC (Cyclic Redundancy Check). The serializer combines video-line data from the video pipe (or pipes) with control-channel data and adds CRC to the GMSL3 packet. Removing the headers and footers optimizes the bandwidth of the GMSL link when in the pixel mode, and provides flexibility in how different data types are packetized and number of video pipes used. The deserializer receives the data and verifies the GMSL3 packet-CRC. The sensor data is then used to recreate the header and footer, ECC, and CRC, respectively, in the deserializer to duplicate the CSI-2 data received by the serializer. See [Figure 24](#).

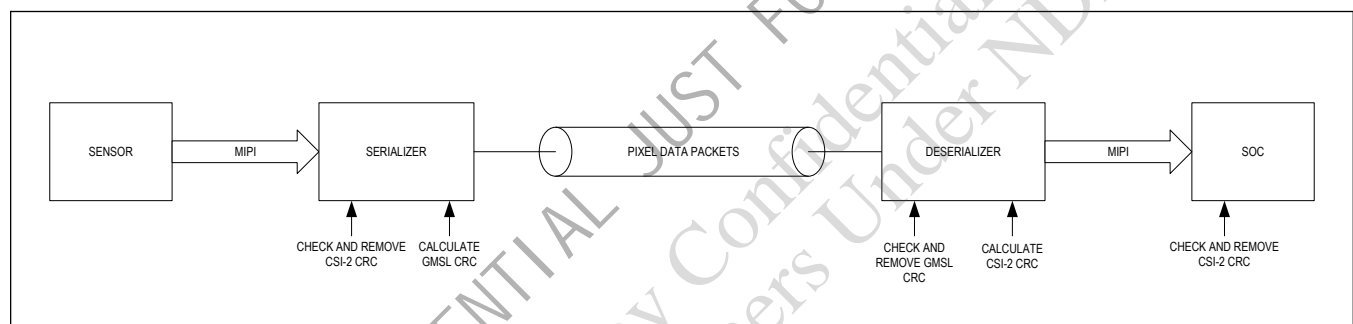


Figure 24. Pixel Mode

In the tunneling mode, the CSI-2 ECC and CRC bytes are checked at the CSI-2 interface of the serializer input, ensuring error free operation across the CSI-2 interface. The received byte stream, including CRC and ECC, as routing and pixel data, is packetized and forwarded over the GMSL3 link as GMSL packets. Data integrity across the GMSL3 link is guaranteed with a separately calculated line-CRC that covers the entire CSI-2 packet content (including original CRC and ECC). The deserializer reconstructs the CSI-2 packet from decapsulated GMSL data. The original CRC and ECCs from the video source are used in the packet to be transmitted across the CSI-2 interface to the SoC. Because the SoC is checking the received content using the original ECC and CRC from the video source, it is the recommended transmission mode for safety-critical applications, where end-to-end data integrity is important. A deserializer in the tunneling mode can interface only to CSI-2 to GMSL serializers that support the tunneling mode. The serializer combines sensor and control data, and adds CRC to the GMSL3 packets. See [Figure 25](#). The deserializer receives the transmitted GMSL3 packets, checks the CRC, separates video data from control data, and reconstructs each CSI-2 packet from multiple GMSL3 packets, outputting them on the standard Mobile Industry Processor Interface (MIPI) exactly as received at the serializer. The tunneling mode ensures end-to-end data integrity and is more bandwidth-efficient if multiple data types are being sent, but does not allow processing the video data such as watermarking or lossy data compression.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

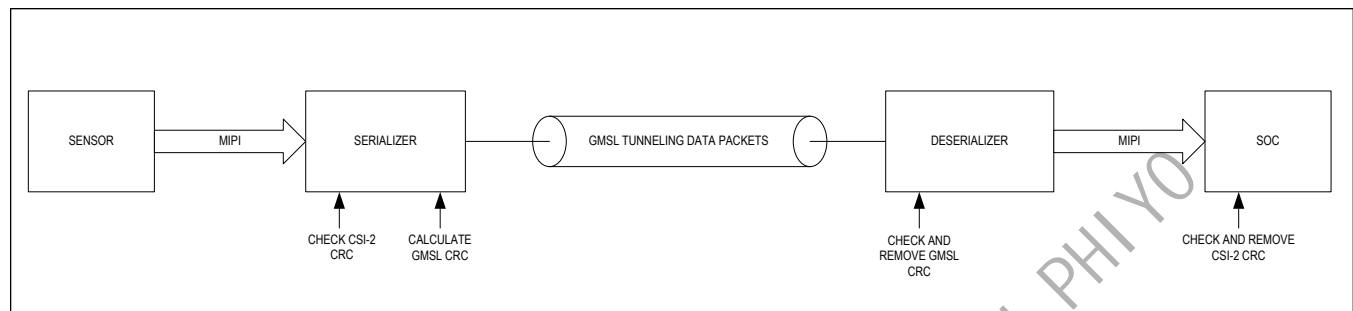


Figure 25. Tunneling Mode

### Forward-Error Correction (FEC)

The MAX96792A supports a Reed-Solomon Forward-Error Correction (FEC) for added link robustness. The Reed-Solomon encoding adds a 6-bit correction word to every 121 bits of data for an effective throughput of 93.3% in return for a bit error rate (BER) reduction from  $10^{-15}$  to  $10^{-55}$ . The maximum payload of the 12Gbps GMSL3 link with FEC is 9.7Gbps. The primary need for FEC in GMSL3 products arises from higher bit-rates and higher-loss links (longer cables, more connectors). FEC is required for GMSL3 mode using PAM4 signaling (12Gbps), but is an option for GMSL2 mode (6Gbps or 3Gbps) using Non-Return to Zero (NRZ) signaling.

The FEC block processes data in blocks of 128 symbols. Each symbol is 18 bits wide. Up to 3 symbol errors (up to 54 bit errors if the errors are a continuous burst) detected in a block of 2,560 bits can be corrected. If the number of errors in a block are higher, there are uncorrected errors. These errors are flagged by the CRC part of the FEC block. The FEC block contains error counters, both for corrected and uncorrected errors, and the FEC input bit-error rate is a good indication of link quality. Keep the FEC input BER  $< 10^{-7}$  for error-free operation.

#### Features:

- Burst error correction capability equivalent to 2 to 3 link symbols.
- Debug capability to enable analyzing quality of received data.
  - Number of errors corrected, number of uncorrectable errors.
  - Interrupt output when uncorrectable errors exceed threshold.

#### Notes:

- Correction is available for all data traffic in the GMSL lanes supporting FEC.
- Enabling FEC reduces the available bandwidth by 6.7%.
- FEC adds approximately 4300 UI latency to the link.
- When FEC is used, it must be on in both the serializer and deserializer.

### Functional Safety Features

The MAX96792A integrates a number of safety features, including Power-on Self Test (POST), which includes Logic Built-in Self Test (LBIST), Memory Built-In Self Test (MBIST), and a power manager that reports undervoltage/overvoltage conditions. The host interface (I<sup>2</sup>C/UART) has an optional CRC capability and optional message counter for I<sup>2</sup>C/UART traffic.

At power-up, LBIST verifies that key logic blocks are correctly functioning and free of latent faults. MBIST checks the line-buffer memories to ensure data is stored correctly prior to being sent to the MIPI output ports. The POST produces a pass/fail result that can be read through a register for each test. A POST failure on start-up does not prevent the device from operation, but is reflected in registers POST\_LBIST\_PASSED and POST\_MBIST\_PASSED.

A register CRC (REGCRC) detects unintended changes in the configuration registers. A CRC value for the configuration registers is computed and stored on demand at start-up. During operation, the REGCRC block periodically calculates the CRC of the configuration registers and compares the calculated value to the stored value. A mismatch can be reported through ERRB.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

**GMSL3 Physical Layer**

Analog Devices' GMSL3 serial link family has transmitter and receiver capabilities enabled simultaneously, allowing full-duplex operation on a single wire. A single cable between the serializer and deserializer delivers data transmitted from each end of the link. Forward transmission refers to data sent from the serializer to the deserializer. Reverse transmission refers to data sent from the deserializer to the serializer.

Fixed forward rate options of 3Gbps, 6Gbps, or 12Gbps are available for both Coax and STP. The reverse rate is fixed at 187.5Mbps.

**Cabling Options**

MAX96792A devices support either 50Ω Coax or 100Ω Shielded-Twisted Pair (STP) cabling. Cable attenuation and return loss characteristics must stay within the requirements of the GMSL3 channel specification to achieve robust full-duplex link performance. These requirements vary with selected link rate. The available link rates and adaptive equalization support a wide range of cabling options.

Coax or STP mode and data rates are configured upon start-up, and determine which cabling option applies. In the Coax mode, use only the noninverted SIO pins. AC-couple and terminate the unused SIO pins using the series connection of a 100nF capacitor and a 49.9Ω resistor. In the STP configuration, both the noninverted and inverted pins are enabled by default.

Maximum cable length is limited by the frequency-dependent attenuation of the cable. Additionally, PCB and inline connectors degrade the return loss characteristic of the cable assembly. The GMSL3 channel specification allows two inline connectors, and provides detailed requirements for cable attenuation and return loss, as well as insertion loss and return loss requirements for PCB traces. In general, any physical channel implementation compliant with the GMSL3 channel specification can be used with reliable results. Contact the factory for the GMSL3 channel specification document.

Coax or STP operation of the GMSL inputs is determined by the level of CFG1 pin at power-up. The GMSL links are configured the same by default, but can be changed after power-up by register programming. See [Table 13](#).

**GMSL3 Bandwidth Sharing**

The GMSL forward link bandwidth is shared flexibly between different communication channels requesting the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation: if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol fulfills this sharing requirement. The maximum non-video packet size is limited to 64 words to prevent one channel from monopolizing the link bandwidth and ensure other channels are served. Other bandwidth-sharing mechanisms are discussed in the following section.

A bandwidth sharing scheme is employed for multiple pending requests of the same priority setting to avoid creating buffer overflows. Without bandwidth sharing, a burst data request from a channel can cause buffer overflow in other communications channels on the link. Bandwidth sharing, however, considers predefined bandwidth share ratios and recent bandwidth usage averages of each type of communication channel to avoid buffer overflows and ensure all channels are served.

The arbiter continuously measures the bandwidth usage of each channel and filters the data according to analysis of the moving averages. This data is then compared to assigned bandwidth share ratios. To ensure link bandwidth parity, the arbiter takes this recent bandwidth usage information to decide which channel is allocated to use the link for each new packet transmission request. Consider a link allocated for either video or SPI communications, where video is assigned 90% link share and SPI is given 5% share. A burst SPI transmission request on this link can cause video overflow buffering if the SPI bandwidth share exceeds 10% of the total. To avoid video buffering, SPI is allotted no more than 10% of the link to preserve the remaining 90% for video communications.

**GMSL3 Bandwidth Calculations**

The GMSL3 forward link has a fixed link rate of 3Gbps, 6Gbps, or 12Gbps. The reverse link rate is also fixed at 187.5Mbps. The GMSL3 protocol and line coding overhead is roughly 14%. Forward-Error Correction, used for 12Gbps forward rate, adds 6.7%. This leaves approximately 2.6Gbps, 5.2Gbps, or 9.7Gbps of data throughput in the forward direction, and 162Mbps in the reverse direction.



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

Ensure the worst use cases do not exceed the available throughput of the forward and reverse links. Analog Devices' Evaluation Kit (EVK) GUI includes a bandwidth (BW) calculator for initial bandwidth requirements estimates. Analog Devices also has other tools to calculate link bandwidth utilization. Consult the factory for high-bandwidth use cases for error-free performance. See [Figure 26](#) for definitions of terms.

[Table 7](#) provides estimates of the bandwidth utilization for each communication channel.

**Table 7. Forward- and Reverse-Link Bandwidth Utilization**

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video (Forward Path Only)	$H \times V \times \text{fps} \times \text{bpp} \times (1 + (\% \text{ horizontal blanking})/100 + (\% \text{ vertical blanking})/100) \times 1.16$ Maximum bandwidth is limited by pixel clock rate PCLK. Pixel mode: $\text{PCLK} = \text{MIPI data rate}/\text{bpp}$ Pixel mode (double pixel mode): $\text{PCLK} = \text{MIPI data rate}/(2 \times \text{bpp})$ Tunneling mode: $\text{PCLK} = \text{MIPI data rate}/24$ Maximum PCLK = 600MHz for 6Gbps or 12Gbps link rate Maximum PCLK = 300MHz for 3Gbps link rate
I <sup>2</sup> C	18 to 60 x I <sup>2</sup> C clock rate, depending on available link bandwidth
UART	6 x UART bit rate, 5.5 x when parity bit enabled
SPI	2.5 x SPI rate
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation

Note: Bandwidth utilization for all control-channel and side-channel communication increases by 6.7% when FEC is enabled. FEC is required for 12Gbps operation.

Definitions:

H = Horizontal resolution

V = Vertical resolution

fps = Frames per second

bpp = Bits per pixel

MIPI data rate = Aggregate data rate of all lanes in the MIPI

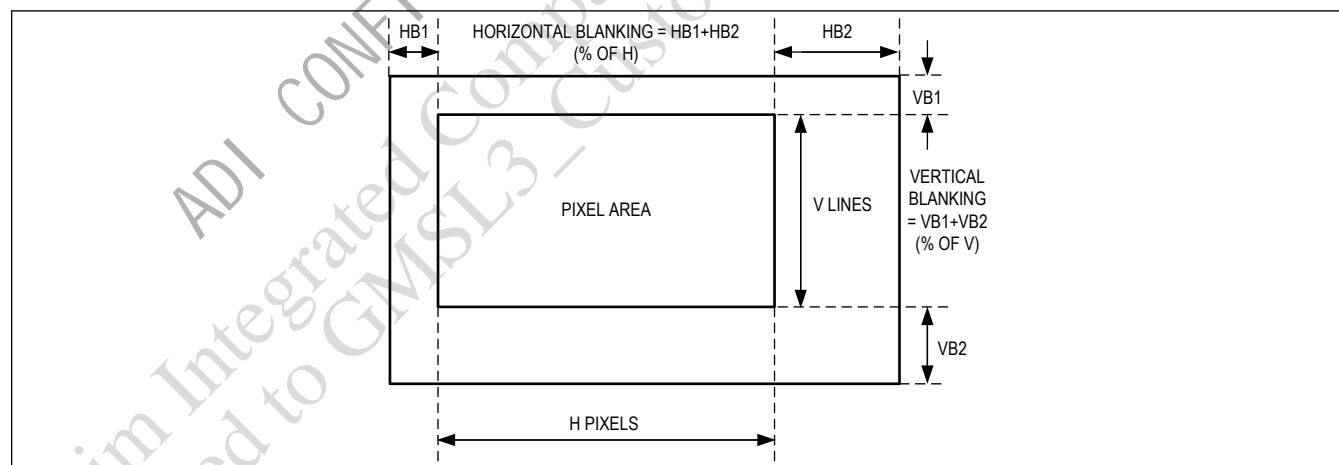


Figure 26. Video Frame Format for Bandwidth Calculation

### Eye-Opening Monitor

The Eye-Opening Monitor (EOM) enables GMSL2 parts to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error free, but have less link margin than desired. This allows proactive reaction to deteriorating cable performance before any link errors

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

occur. GMSL2 devices can measure the horizontal or vertical eye opening of the equalizer's output. The measurement is activated automatically at a ~1Hz rate once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye-opening is then reported, and the EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds. Note that the EOM is a recommended diagnostic for GMSL2 mode (3Gbps or 6Gbps), not for GMSL3-mode (12Gbps).

### Line-Fault

GMSL deserializers include a novel line-fault detection circuit. It detects and reports open-circuit, short-to-battery, short-to-ground, and line-to-line short. The line-fault monitor requires external resistors  $R_{EXT1}$  and  $R_{PD}$  in Coax mode, and  $R_{EXT1}$ ,  $R_{EXT2}$ , and  $R_{PD}$  in STP mode connected to the LMN\_ pins as detailed in the following sections.

The line-fault monitor is disabled by default, configuration options are available through registers, and status can be read by the register. If unmasked, a line-fault condition asserts  $ERRB$ . Line-fault detection cannot be used in conjunction with Power-over-Coax (POC) or AC-coupled ground applications.

The line-fault monitor pins offer flexible connection and programming in either Coax or STP applications.

[Figure 27](#) illustrates the two configuration options for the location of line-fault detection. The Local-Side Serializer Configuration is typically used for display links and Local-Side Deserializer Configuration for camera links; however, either configuration can be used on any device serial link system. Additionally, either applies to Coax or STP mode.

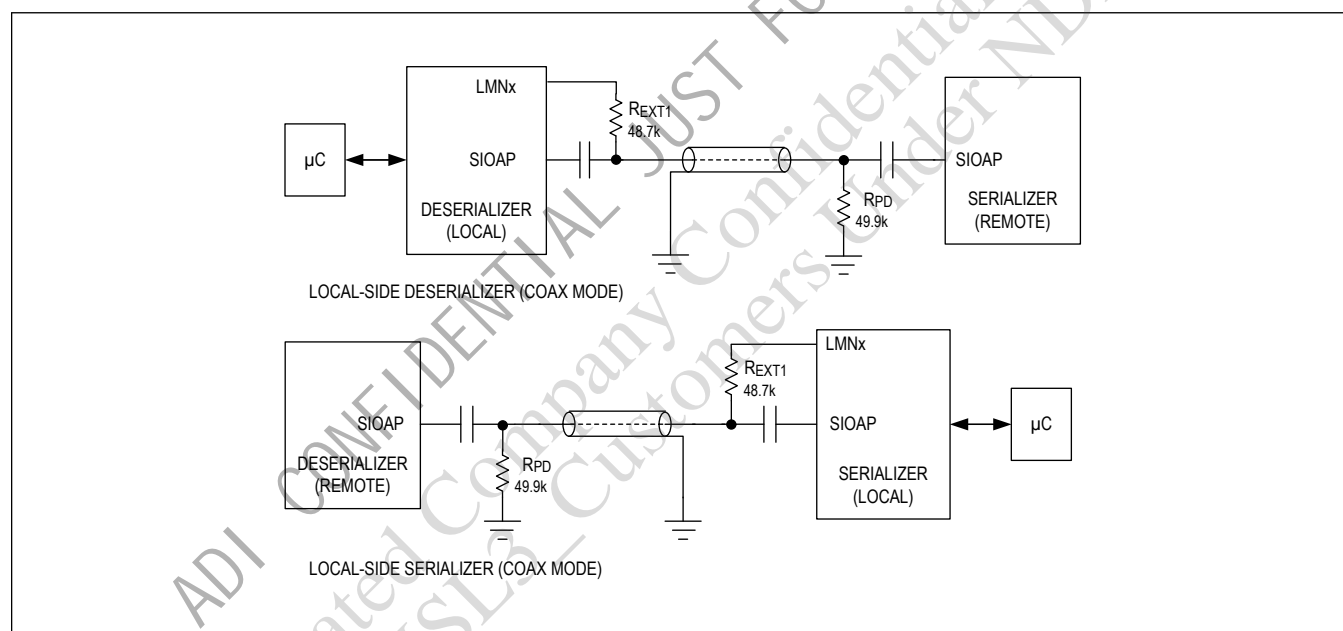


Figure 27. Line Fault Detection Location Options

The LMNx pins (LMN0 to LMN3) are typically mapped to different multifunctional pins on each unique part and package options. Some parts may have up to four line-fault detectors, depending on the package options and pin availability.

### Coax Mode

In Coax applications, any LMNx pin can be used. The local side sources the line-fault. The local-side device requires a single 48.7kΩ resistor ( $R_{EXT1}$ ) connected directly from any of the LMNx pins to the serial link.  $R_{EXT2}$  is not used in Coax applications. The remote side of the serial link requires a 49.9kΩ resistor ( $R_{PD}$ ) connected from the serial link to GND. Any of the line-monitor pins can be used in Coax applications.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**Table 8. Coax Mode Line-Fault Configuration Options**

SIGNAL	SIOAP	SIOBP
Line-Fault Pin	LMNx (any LMN pin)	LMNx (any LMN pin)
$R_{EXT1}$	48.7k $\Omega$	48.7k $\Omega$

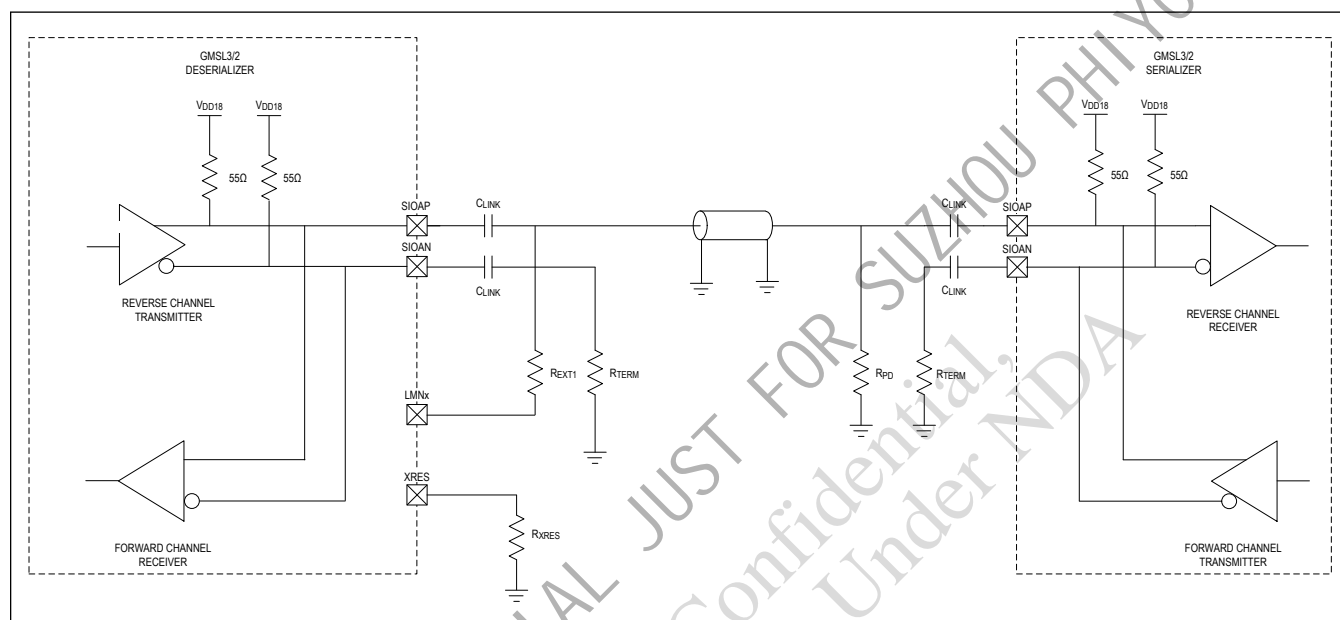


Figure 28. Typical GMSL Link Application Circuit for Coax Cable

### STP Mode

If the serial link is operating in twisted-pair mode, connect one line to an even-numbered pin (LMN0/2) and other line to an odd-numbered pin (LMN1/3) on the local side. For reliable line-fault detection, the even-numbered pins (i.e., LMN0 and LMN2) must be connected to the line using a 42.2k $\Omega$  resistor ( $R_{EXT2}$ ); the odd-numbered pins (i.e., LMN1 and LMN3) must use a 48.7k $\Omega$  resistor ( $R_{EXT1}$ ) to connect to the line (as with single-ended mode)). On the remote side, both lines require a 49.9k $\Omega$  resistor ( $R_{PD}$ ) connected to GND.

For full operation of line-fault detection in twisted-pair applications, use either LMN0/1 or LMN2/3 pairs. This pairing is required for proper operation of the line-to-line short detection; however, this pairing is not necessary for the detection of other fault conditions.

Line Fault Pair #1 (LMN0/LMN1) Resistor Values and Connection Choices in STP Mode

**Table 9. STP Mode Line Fault Configuration Options for LMN0/LMN1**

LINE FAULT PAIR #1: LMN0 AND LMN1	SIOAP	SIOAN
Option #1	LMN0: $R_{EXT2}$ = 42.2k $\Omega$ to serial link	LMN1: $R_{EXT1}$ = 48.7k $\Omega$ to serial link
Option #2	LMN1: $R_{EXT1}$ = 48.7k $\Omega$ to serial link	LMN0: $R_{EXT2}$ = 42.2k $\Omega$ to serial link

Line-Fault Pair #2 (LMN2/LMN3) Resistor Values and Connection Choices in STP Mode

**Table 10. STP Mode Line-Fault Configuration Options for LMN2/LMN3**

LINE FAULT PAIR #2: LMN2 AND LMN3	SIOAP	SIOBN
Option #1	LMN2: $R_{EXT2}$ = 42.2k $\Omega$ to serial link	LMN3: $R_{EXT1}$ = 48.7k $\Omega$ to serial link
Option #2	LMN3: $R_{EXT1}$ = 48.7k $\Omega$ to serial link	LMN2: $R_{EXT2}$ = 42.2k $\Omega$ to serial link

Identical options apply to the GMSL B-port (SIOBP and SIOBN pins).

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

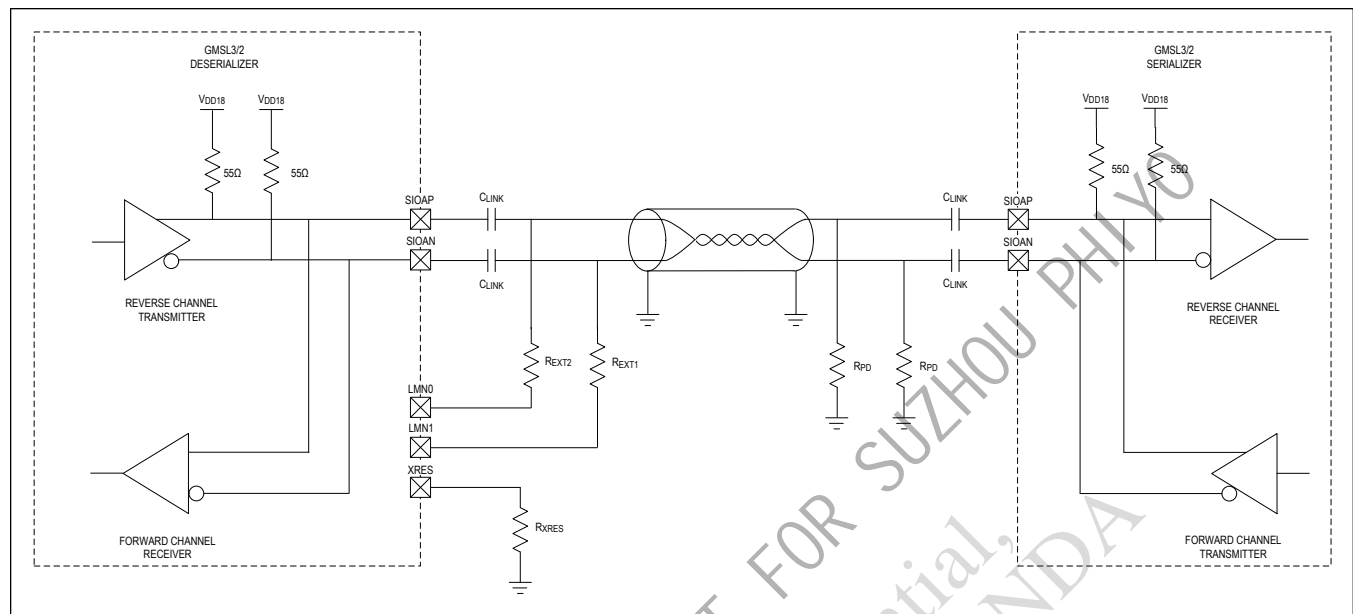


Figure 29. Typical GMSL Link Application Circuit for Twisted Pair (Line Fault Pair #1: LMN0 and LMN1, Option #2)

### Adaptive Equalization (AEQ)

The GMSL3 devices automatically adapt the forward path receiver characteristics to compensate for insertion loss and return loss characteristics of the channel, which consist of the cables, connectors, and PCBs. This approach optimizes performance on any channel that meets the GMSL3 channel specification.

The equalizer architecture makes GMSL3 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock and then invoked at a rate of approximately 1Hz to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye-opening by using the built-in eye-opening monitor.

### Video Pipes

In the GMSL3 pixel mode, the transportation of video data is based on the concept of video pipes. Carrying data in pipes allows GMSL3 to bridge different digital video interfaces (i.e., parallel YUV422 source to CSI-2 sink), and perform watermark generation and detection. A pipe carries a video stream (or streams) and video synchronization data, and operates in one of three modes. In all modes, a pipe can carry multiple concurrent video streams, with each stream having different virtual channels and data types as follows:

- Mode 1: Streams with constant bits per pixel (bpp) of up to 24bpp. The bpp of the streams must be the same.
- Mode 2: Streams with 16, 14, 12, 10, or 8bpp. Streams less than 16bpp are padded with zeros.
- Mode 3: Streams with two different bpp rates. The bpp of one stream must be twice the bpp of the other stream. The highest bpp stream is 24bpp.

Modes 1 and 3 carry data at full bandwidth, but put more restrictions on bpp than Mode 2. Mode 2 allows streams with different bpp rates, but streams of less than 16bpp are carried using more bandwidth than necessary on the GMSL3 link (because of zero-padding). Mode 1 or 3 is sufficient for most applications. Mode 2 requires less programming and is more convenient if the application does not require maximum link bandwidth.

The MAX96792A has two video pipes, one for each GMSL3 port. Each of the two pipes has a dedicated video-line buffer. Each 32k byte (256kb) video-line buffer has the capacity for a line length of up to 8,191 24-bit pixels (8,191 pixels include line-blanking pixels). The number of pipes used by all serializers connected to the MAX96792A cannot exceed two pipes.

Before data enters a line buffer, it goes through a crosspoint switch, and a Data Type (DT) and Virtual Channel (VC) reassignment stage. If the video source has a CSI-2 output, packet DT and VC can be left as-is or reassigned through register programming. Up to 16 DT/VC incoming pairs can be mapped to 16 DT/VC outgoing pairs.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

If the video source does not have a CSI-2 output, a DT and VC can be programmed in the MAX96792A for insertion into the CSI-2 output packet. The crosspoint switch can change the order of the bits in the incoming video pixel data to any order, if desired.

A line buffer stores a complete line of video data before the data is available for readout by an aggregator. Each buffer connects to two aggregators, but only one aggregator (as programmed by the user) can read a line of data out of the buffer at a time. Once data is read out, it cannot be read out a second time by the same aggregator or by the other aggregator. However, in a time-domain multiplexed fashion, both aggregators can be programmed to read from the same buffer.

Data is read out from line memory on a first-come, first-served basis. When a complete line of data has filled a line memory, it is read out. The order in which the line memories reach filled status is the order in which they are read out.

In the pixel mode, video data can be routed according to DT or VC, based on the source CSI-2 packet's DT/VC, or by a DT/VC assigned or reassigned by the MAX96792A. For example, data in Pipe Y with VC0 can be programmed to be read out by Aggregator A, while data in Pipe Y with VC1 can be programmed to be read out by Aggregator B. In the tunneling mode, data cannot be routed by VC or DT, but is simply sent to the programmed aggregator.

The aggregator forwards the line of video or data from the line buffer, and video-synchronization data to its associated CSI-2 controller for packet generation. Packets can be output on the controller's port or replicated by routing them to the other port. For example, CSI-2 Controller 0 can output packets on D-PHY Port A or also route them for output of D-PHY Port B.

A D-PHY or C-PHY port can only accept packets from one controller; it cannot aggregate packets from the two controllers.

To prevent buffer overflow, the CSI-2 port data rate must be programmed to a rate equal to or greater than the incoming data rate. Programming the output rate to be faster than the bandwidth of the incoming video or data increases packet spacing (LP time between packets).

No reformatting of the data occurs in the tunneling mode. It is a requirement for functional safety that the video data is unchanged, such that it can be compared against the tunneled CSI-2 CRC by the host.

After data exits a retiming buffer, it goes through a crosspoint switch, and a Data Type (DT) and Virtual Channel (VC) reassignment stage. If the video source has a CSI-2 output, packet DT and VC can each be left as-is, or reassigned by register programming.

[Figure 30](#) shows the MAX96792A operating with the input data from each input port kept separate, while [Figure 31](#) shows the ability to combine the data from each input port onto both output ports.

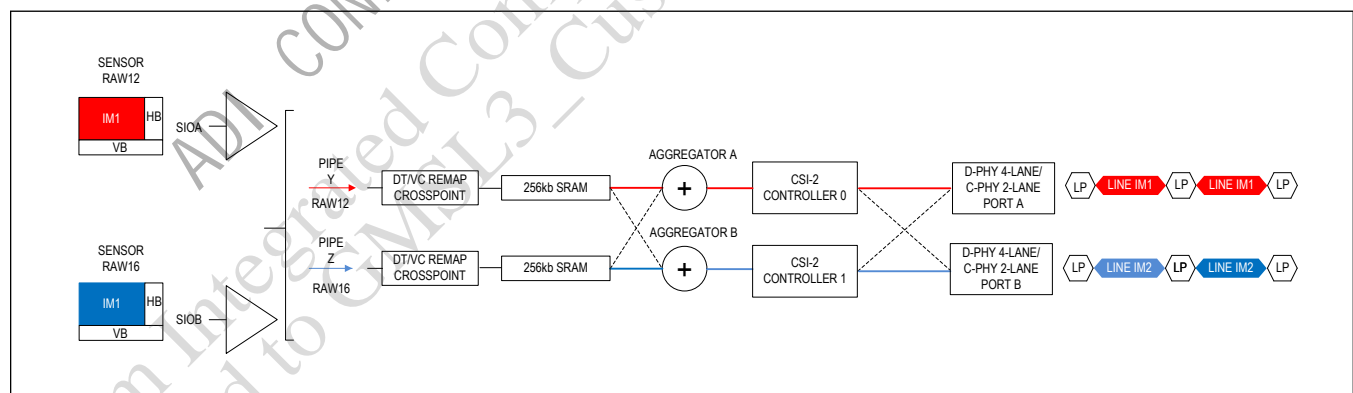


Figure 30. GMSL3 Video Output of Separate Ports

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

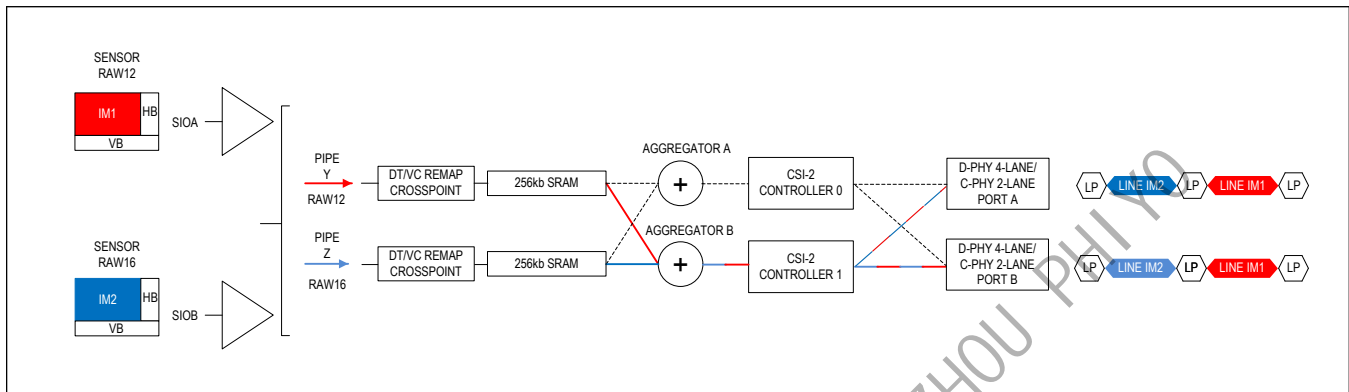


Figure 31. GMSL3 Video Aggregated and Replicated

### Video-Timing Generator

The Video-Timing Generator (VTG) can substitute HS, VS, and DE signals with the signals it generates as defined by the configuration registers. The VTG can generate almost any type of SYNC-signal set pattern in various modes to start the generated patterns. With proper register programming, it is possible to generate any desired PCLK output frequency without an attached serializer. The VTG can generate a test pattern at any resolution with internally-generated clocks.

### RGB888 Video-Pattern Generator

The built-in RGB888 VPG can be used for debug purposes. Video of any resolution can be generated by the VPG without a GMSL connection, or video from the peripheral can be replaced by the video-pattern generated by the VPG as programmed from the configuration registers (see PATGEN\_1 register block). The VPG can generate checkerboard and gradient patterns using RGB888 data. The pixel clock for the VPG is sourced internally, and is configured using the following registers:

Table 11. Video-Pattern Generator Pixel Clock Selection

0x38[1]	0x38[0]	0x1FC[7] PATGEN_CLK_SRC	PIXEL CLOCK (MHz)
0	0	x	25
0	1	x	75
1	x	0	150
1	x	1	600

### Pseudorandom Binary Sequence (PRBS)

#### Video PRBS

The video channel of the serializer implements a PRBS pattern generator that operates with bit-error verification in the deserializer to test channel operation. The PRBS generator works with the clock received from the source.

#### Link PRBS

The link PRBS test is an evaluation tool to validate error-free operation across the GMSL channel using a PRBS-7 data pattern. It can be useful for the prototyping and verification phases of evaluating the GMSL SerDes devices.

The link PRBS floods the entire link bandwidth with PRBS-7 data. Regularly packetized data such as video and control channel commands cannot be sent during the test. Once the test is enabled, the control channel is lost, and remote communication is unavailable. To properly operate the link PRBS test, access to both local and remote device registers is required without the serial link as the control-channel transmission medium. This can be achieved only by accessing the control interfaces on both the serializer and deserializer to configure the link PRBS generator/checker on each end of the link.



### Video-Memory ECC Protection

The integrity of data propagating through the video pipeline's memory is guaranteed by Error-Correction Code (ECC), which corrects 1-bit errors, and detects 1-bit or 2-bit errors per 32 bits of video data. This functionality provides protection of data unprotected by the CRCs of the incoming Gigabit Multimedia Serial Link (GMSL) stream or outgoing Camera Serial Interface (CSI) stream, eliminating the possibility that internally-generated bit errors might corrupt the outgoing CSI-2 stream. The state of the ERRB pin can be used to detect the presence of errors. Intentional memory-error injection is available for diagnosis.

### Scheduler/Arbiter

A scheduler transmits packets with high priority values before lower priority values. Each communication transmit adapter sets a priority for the packet request before transmitting data to the remote side. The priority value is 2 bits, which allows for the following settings: 0 = Low, 1 = Normal, 2 = High, and 3 = Urgent. The scheduler, provided sufficient link bandwidth, chooses to transmit the packet with the highest priority among the pending active requests. Priority levels become more important as link bandwidth becomes scarce, and prioritization should be assigned accordingly.

In most cases, each transmitter adapter should use the normal priority setting (priority = 1) to allow the scheduler to choose the transmission schedule based on recent bandwidth usage. Packet priority can be increased if packets require low latency or have waited for a specified period of time. For example, packets with requirements on maximum latency can have increased priority if the packet request is not serviced until half of the maximum latency requirement has elapsed. This can also be used for communications channels with continuous data flow (e.g., video). Priority can be increased when the transmit adapter data buffer approaches overflow. Conversely, register configuration allows the priority settings of each channel to be overridden. This option is useful if the host  $\mu$ C wants to prioritize one channel over the others.

Communications channels with very relaxed latency requirements can use the low-priority setting (priority = 0). These low-priority packets are not serviced by the scheduler if there are any pending requests of a higher priority setting. In this arrangement, link-bandwidth assignment can reach the theoretical maximum for video. Low-priority packets can then be transmitted during video horizontal-blanking time, during which the video-channel bandwidth usage drops considerably.

### Control-Channel CRC Generation and Checking

Every packet (excluding Idle and Acknowledge packets) can be protected by a 16-bit packet Cyclic Redundancy Check (CRC). Each packet type can be individually configured to enable or disable packet CRC. By default, all control-channel packets transporting I<sup>2</sup>C, UART, SPI, or GPIO data have packet CRC. For the forward control-channel, the CRC is generated for each control-channel packet transported across the link to the deserializer. In the deserializer, a CRC is calculated based on the packet content and is compared to the received CRC. A mismatch results in automatic retransmission of the packet. Similarly, for the reverse channel, the CRC is generated in the deserializer and is checked in the serializer. Also, here, a mismatch results in automatic retransmission of the control channel packet.

For a GPIO, each packet transmitted across the link represents a GPIO transition and its routing information. Thus, each transition results in a 16-bit CRC being transported across the link, adding to bandwidth consumption.

Note that as acknowledge packets contain no data and the header is repeated, CRC is unnecessary.

The 16-bit packet CRC generator polynomial is:  $x^{16} + x^{15} + x^2 + 1$ .

### Serial Peripheral Interface (SPI)

The MAX96792A includes one SPI bridge, enabling a host SPI master on one side of the GMSL3 link to control a peripheral SPI slave on the opposite side. Communication can be in either direction across the GMSL link.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

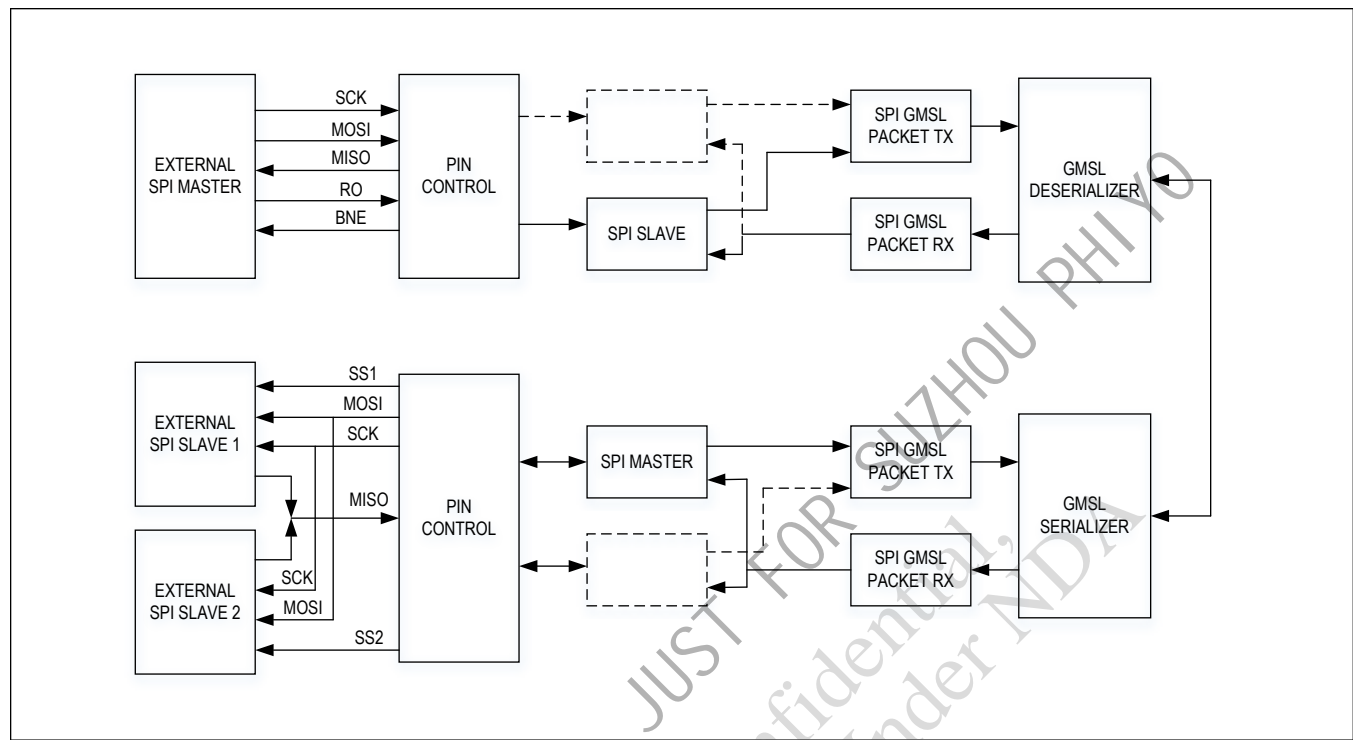


Figure 32. SPI Bridge

### CSI-2 Output Interface

#### Lane Configurations and Data Rates

Video data is output to unidirectional MIPI CSI-2 v1.3 output ports. Each port can be configured to use either D-PHY v1.2 or C-PHY v1.0. The interface offers a high degree of flexibility. When configured as D-PHY, each interface supports either 1, 2, 3, or 4 differential lanes. Up to four lanes on each port are supported if the part is configured to use one or two ports. When configured as C-PHY, each port supports either one or two lanes/trios. To ease PCB layout, lane swapping is supported independently of the number of lanes used. For example, when the device is configured to enable a single lane, that lane can be any one of the four lanes available within that port. If two lanes are enabled, those two lanes can be any two lanes within the port. Lane polarity swapping within a lane is also supported.

#### CSI-2 Virtual Channel and Data Type Interleaving

The device supports virtual channels, including Virtual-Channel Extension (VCX) introduced in CSI-2 v2.0, enabling up to 16 virtual channels.

#### Video PRBS Generator/Checker

GMSL3 devices include built-in video PRBS generators/checkers for video link testing. For example, a serializer's PRBS generator can be used in conjunction with a deserializer's PRBS checker to test the GMSL2 video channel that connects the two devices. Here, the MAX96792A's PRBS checker functionality compares the received PRBS stream with the predicted PRBS data to establish any errors.

The MAX96792A also includes the video PRBS generator functionality to test downstream video devices that receive video through the MAX96792A's CSI-2 output. This includes GMSL serializers connected in a loopback configuration with CSI and GMSL video paths being tested at the same time.

Note that all link bandwidth is not used by the video channel alone. So, it is possible to have a bit error on the link that does not cause a video PRBS error.

To run the video PRBS test, first enable the PRBS generator on the transmitter side, then enable the checker on the



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

receiver side. The PRBS checker automatically syncs itself to the incoming PRBS pattern. If it is unable to sync within a few cycles, it then asserts the PRBS\_FAIL register. To stop the PRBS test, first turn the checker off on the receiver side, then turn the generator off on the transmitter side.

PRBS errors can be read from the VPRBS\_ERR register on the deserializer side. Any PRBS error causes the ERRB pin to go low in the deserializer by default (see VPRBS\_ERR\_OEN and VPRBS\_ERR\_FLAG register bits).

Note that the video channel shares link bandwidth. So, it is possible to have a bit error on the link that does not cause a video PRBS error.

### MIPI CSI-2 Output Raw PRBS Generator

The MAX96792A facilitates MIPI PHY characterization by generating PRBS output streams in the HS transmit mode directly from each C/D-PHY output lane. The available patterns are PRBS9, PRBS11, and PRBS18, and the resulting output data is a continuous stream not packetized by the CSI-2 controllers.

### Lane Deskew

The device's CSI-2 interface, configured to use D-PHY, supports interlane deskew by transmitting deskew patterns from the transmitter when the bit transmission rate is 1.5Gbps/lane and above. Deskew is optional for data rates lower than 1.5Gbps/lane. Deskew must be turned on using DESKEW\_INIT and DESKEW\_PER registers for each MIPI PHY. Refer to the GMSL2 User Guide for details on configuring the lane deskew function.

### Minimum Blanking

The minimum horizontal blanking period needed by the CSI-2 serializers and deserializers is the maximum of either 40 pixels or  $300\text{ns} + 370\text{UI}$  (where UI is defined as the period of CSI-2 lane rate). For most cases, 40 pixels is the larger number. The minimum vertical blanking period is one video line. The minimum vertical front porch is one video line. The recommended vertical back porch is one video line.

The minimum vertical back porch in pixel mode is the maximum of:

- 40 pixels
- $300\text{ns} + 370\text{UI}$

The minimum vertical back porch in tunneling mode is the maximum of:

- 40 pixels
- $200 \text{ PCLK periods} + 233\text{ns}$ , where  $\text{PCLK} = \text{total MIPI data rate}/24$
- $300\text{ns} + 370\text{UI}$

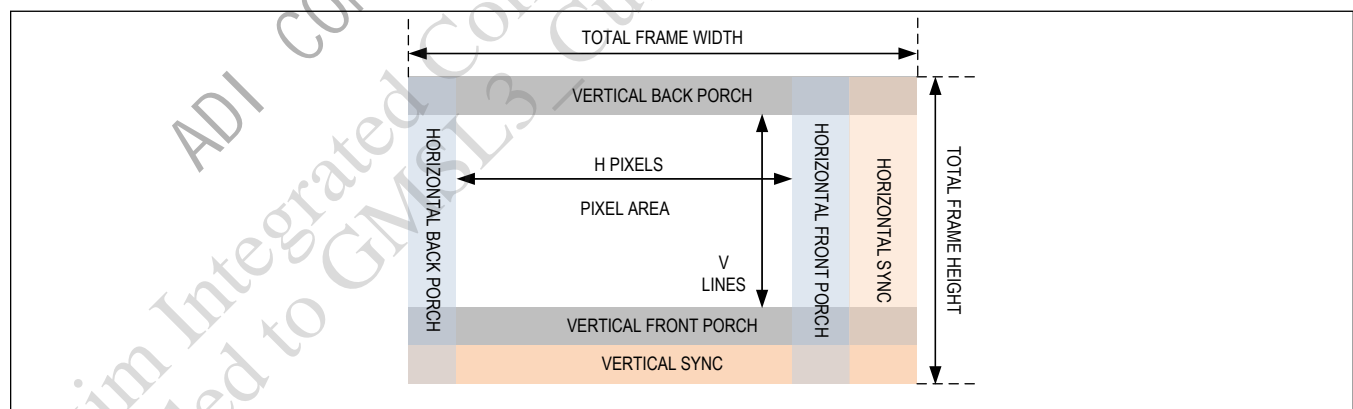


Figure 33. Video Timing

### MIPI End-to-End Packet Spacing

When in the tunneling mode, timing requirements must be met to avoid a false line-CRC error flag. Figure 34 shows the end-to-end packet spacing (L1, L2, ... LN, LE, LS) must be a minimum of  $200 \times \text{PCLK} + 233\text{ns}$ , where PCLK is the total

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

MIPI data rate/24. This limit is typically a concern for the line-end short packets, which follow the last long data packet of a frame. An alternate solution is to disable the line-CRC check and rely on the MIPI CSI-2 packet CRC, which is a valid verification of error-free data reception.

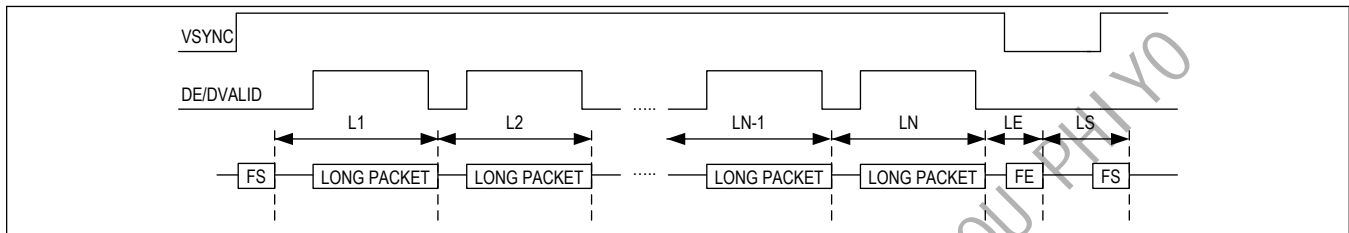


Figure 34. End-to-End Packet Spacing

### CFG Latch at Power-Up Pins

At power-up or after reset, the voltages at the CFG pins (set by the voltage divider) are sampled. The sampled level is used to set the initial value of certain registers.

Table 12. CFG0 Input Map

CFG0 INPUT VOLTAGE SPECIFICATION (Notes a, b) (% of V <sub>DDIO</sub> )			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note c)		MAPPED CONFIGURATION (Note d, e)	
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	I2CSEL	DEVICE ADDRESS
0.0%	0.0%	11.7%	OPEN	10k	I <sup>2</sup> C	0x50
16.9%	20.2%	23.6%	80.6k	20.5k		0x54
28.8%	31.2%	35.5%	68.1k	32.4k		0x98
40.7%	44.0%	47.4%	56.2k	44.2k		0xD4
52.6%	56.0%	59.3%	44.2k	56.2k	UART	0xD4
64.5%	67.9%	71.2%	32.4k	68.1k		0x98
76.4%	79.8%	83.1%	20.5k	80.6k		0x54
88.3%	100%	100%	10k	OPEN		0x50

#### Notes:

- Resistor divider tolerance, V<sub>DDIO</sub> supply ripple, and external loading must not cause the CFG0 input voltage to exceed the maximum or minimum limits.
- Other than the CFG0 input resistor divider, any load on CFG0 must be  $\geq 25 \times (R1 + R2)$ .
- Each resistor in the voltage divider must be  $\leq 100k\Omega$ .
- I2CSEL: I<sup>2</sup>C or UART interface for SDA\_RX and SCL\_TX.
- When this address is selected, both serial inputs are automatically enabled. A single serial input can be programmed after power-up, if desired.

Table 13. CFG1 Input Map

SPECIFICATION (Notes a, b) (% of V <sub>DDIO</sub> )			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note c)		MAPPED CONFIGURATION		
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	COAX OR TWISTED PAIR	DATA RATE [Gbps]	TUNNEL/ PIXEL MODE
0.0%	0.0%	11.7%	OPEN	10k	STP	6	Tunnel
16.9%	20.2%	23.6%	80.6k	20.5k		12	
28.8%	32.1%	35.5%	68.1k	32.4k		3	Pixel
40.7%	44.0%	47.4%	56.2k	44.2k		6	

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**Table 13. CFG1 Input Map (continued)**

SPECIFICATION (Notes a, b) (% of V <sub>DDIO</sub> )			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note c)		MAPPED CONFIGURATION		
52.6%	56.0%	59.3%	44.2k	56.2k	COAX	6	Tunnel
64.5%	67.95%	71.2%	32.4k	68.1k		12	
76.4%	79.8%	83.1%	20.5k	80.6k		3	Pixel
88.3%	100%	100%	10k	OPEN		6	
						PAM4	
						NRZ	

**Notes:**

- Resistor divider tolerance, V<sub>DDIO</sub> supply ripple, and external loading must not cause the CFG1 input voltage to exceed the maximum or minimum limit.
- Other than the CFG1 input resistor divider, any load on CFG1 must be  $\geq 25 \times (R1 + R2)$ .
- Each resistor in the voltage divider must be  $\leq 100k\Omega$ .

**MFP Function Map and Slew Settings**

Side-channel functions, such as SPI and pass-through I<sup>2</sup>C/UART, are enabled by programming multifunction pins. Each MFP has several possible functions, but only one can be used at a time.

Some functions require only a single MFP, but most are implemented across a group of MFPs. For example, LOCK is a single MFP, but SPI takes several MFPs. MFP functions are selected to suit each use-case by programming the appropriate registers.

The [Pin Description](#) table shows default and alternate functions for each MFP. [Table 14](#) also shows priority, left to right, with highest priority on the left. A higher-priority function must be disabled when a lower-priority function is enabled, both by register writes.

Each MFP has a programmable slew setting that sets the transition time, as shown in [Table 15](#). Slew settings listed as I<sup>2</sup>C apply to pass-through I<sup>2</sup>C pins when pass-through I<sup>2</sup>C is enabled. The pin slew default in [Table 14](#) suits the MFP's normal application requirements. Except for I<sup>2</sup>C/UART and GPI\_ODO functions, where transition times are fixed, the transition time of each speed group can be changed from the default value through register programming.

Transition times depend on the transition-time setting and V<sub>DDIO</sub> supply voltage. See [Table 15](#) for typical transition times.

**Table 14. MFP Pin Function Map**

PIN	LATCH ON POWER- UP	I <sup>2</sup> C/UART	SPI	OTHER FUNCTIONS	GPIO	POWER-UP DEFAULT	PIN SLEW DEFAULT (BINARY)
MFP0		SDA1_RX1, SDA2_RX2	SCLK	FSYNC_OUT, VS2, DE2/ DV2, MS	GPIO0	GPI (1M $\Omega$ to GND)	10
MFP1		SCL1_TX1, SCL2_TX2		LOCK	GPIO1	LOCK (ODO, 40k $\Omega$ to V <sub>DDIO</sub> )	11
MFP2	CFG0		BNE, SS1		GPO2	DISABLED (Hi-Z)	11
MFP3	CFG1		SS2	VS1, DE1/DV1	GPO3	DISABLED (Hi-Z)	11
MFP4			RO(Alt)	ERRB	GPIO4	ERRB (ODO, 40k $\Omega$ to V <sub>DDIO</sub> )	11
MFP5		SDA1_RX1, SDA2_RX2	MOSI	LOCK(Alt)	GPIO5	RX1 (40k $\Omega$ to V <sub>DDIO</sub> )	10

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**Table 14. MFP Pin Function Map (continued)**

PIN	LATCH ON POWER-UP	I <sup>2</sup> C/UART	SPI	OTHER FUNCTIONS	GPIO	POWER-UP DEFAULT	PIN SLEW DEFAULT (BINARY)
MFP6		SCL1_TX1, SCL2_TX2	MISO		GPIO6	TX1 (40kΩ to V <sub>DDIO</sub> )	10
MFP7			RO	LMN0	GPI7	GPI7 (1MΩ to GND)	NA
MFP8				LMN1	GPI8	GPI8 (1MΩ to GND)	NA
MFP9				LMN2	GPI9	GPI9 (1MΩ to GND)	NA
MFP10				LMN3	GPI10	GPI10 (1MΩ to GND)	NA
MFP11		SDA_RX			GPI11_ODO11	SDA or RX (ODO, 40kΩ to V <sub>DDIO</sub> )	NA
MFP12		SCL_TX			GPI12_ODO12	SCL or TX (ODO, 40kΩ to V <sub>DDIO</sub> )	NA

All MFP pins are Hi-Z in power-down state.

All MFP IOs are latched in sleep mode.

Hi-Z - 1MΩ pullup/pulldown is disabled and input/output is disabled.

Latched – Value of input before sleep mode entered remains latched in sleep mode and after return to power-up mode.

ODO = Open-Drain Output

**Table 15. Control- and Side-Channel Typical Rise and Fall Times**

PIN SLEW	RISE TIME (ns) (20% to 80%), C <sub>L</sub> = 10pF		FALL TIME (ns) (80% to 20%), C <sub>L</sub> = 10pF	
	V <sub>DDIO</sub> = 1.8V	V <sub>DDIO</sub> = 3.3V	V <sub>DDIO</sub> = 1.8V	V <sub>DDIO</sub> = 3.3V
00	1.0	0.6	0.8	0.5
01	2.1	1.1	2.0	1.1
10	4.0	2.3	4.3	2.3
11	9.0	5.0	10.0	5.0
I <sup>2</sup> C	NA	NA	40	30

#### MFP Pin Equivalent Circuits

In general, MFP pins can all be classified as either programmable high-speed GPIO or programmable I<sup>2</sup>C/ODO (Open-Drain Output) GPIOs. Equivalent circuit representations are shown in [Figure 35](#) and [Figure 36](#).

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

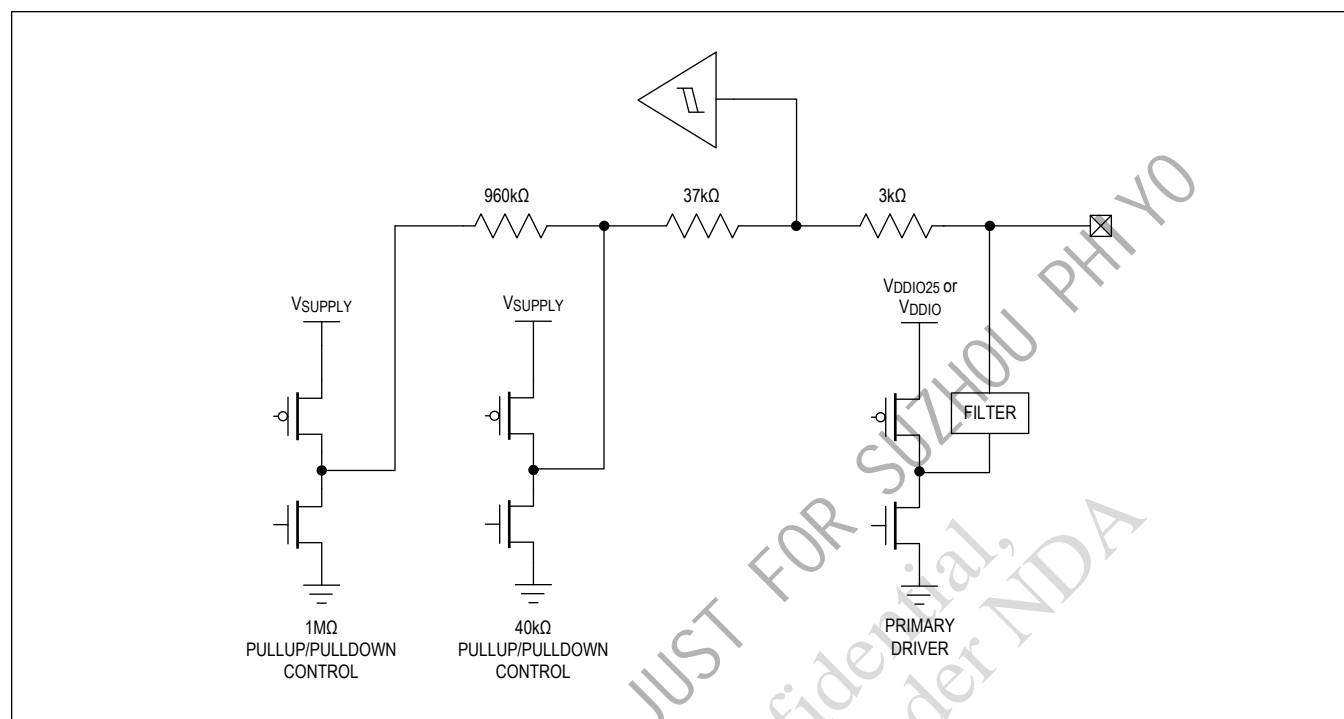


Figure 35. Standard High-Speed GPIO

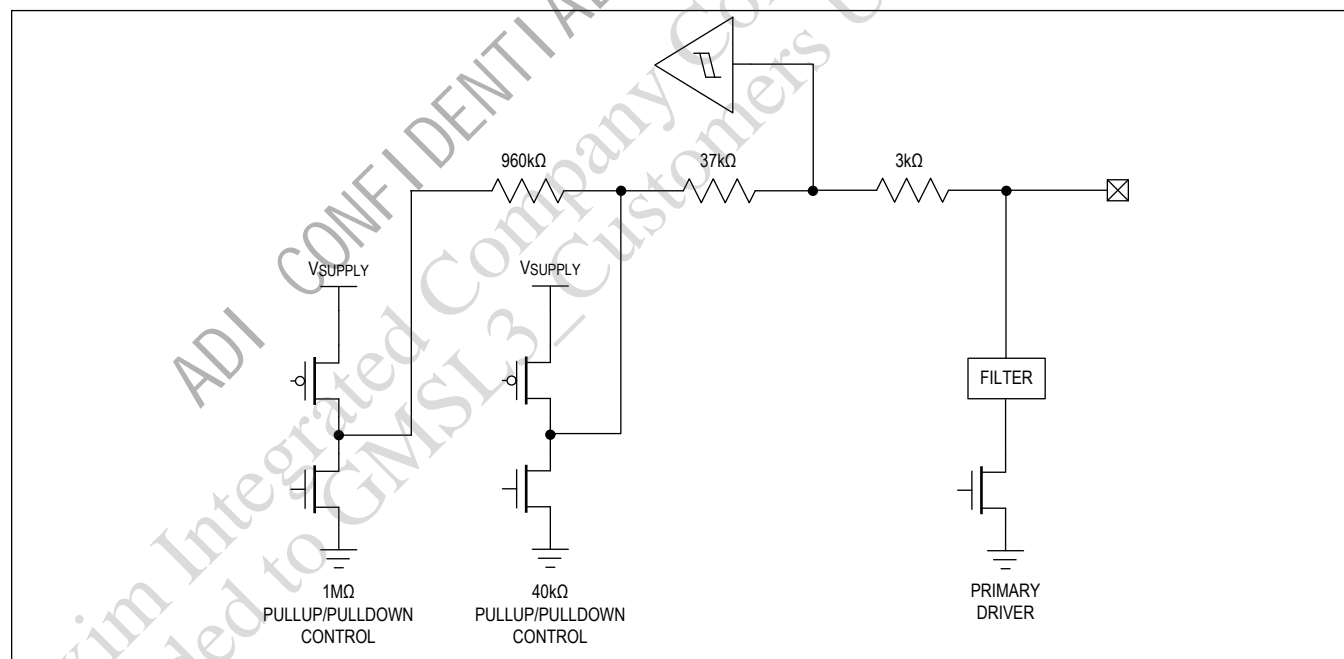


Figure 36. Standard I<sup>2</sup>C GPIO

### Power-Up and Link Start-Up

GMSL3 ICs are in power-down mode when the PWDNB pin is low or when any of the power supplies are down. Registers and configurations are set to default reset conditions.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

The serializer and deserializer may power up in any order. After all power supplies are up and PWDNB is released, each device starts its power-up sequence and performs these actions in sequence:

1. Latch at power-up CFG pin levels. Set the internal registers according to the selected configuration (selected by CFG0, CFG1).
2. The control channel (I<sup>2</sup>C or UART) is functional on local side. The device registers are writable and readable.
3. The link is established based on the following settings:
  - a. Single-link auto-selection mode (AUTO\_LINK = 1 and LINK\_CFG = 1 or 2): Automatically select the PHY to establish a GMSL3 link by periodically trying to handshake using PHY A and PHY B.
  - b. Single-link manual-selection mode (AUTO\_LINK = 1 and LINK\_CFG = 1 or 2): Set LINK\_EN\_B to 0 and keep LINK\_EN\_A at 1 to establish a link using PHY A. Set LINK\_EN\_A to 0 and keep LINK\_EN\_B at 1 to establish a link using PHY B.
  - c. Reverse-splitter mode. Link A and Link B (AUTO\_LINK = 1 and LINK\_CFG = 3) are selected: Mode aggregates data from both links within the deserializer to output on one or two MIPI output ports.
4. Each enabled PHY performs link calibration, equalizer adaptation, and data-channel locking. Both devices set their LOCK pins high.
5. The control channel is available from the remote side.

The entire link-up process, from the time that the last part's PWDNB input is brought high, takes typically 65ms for any channels that meet the GMSL3 channel specification.

After the devices are linked, they can be configured. This can be done locally or over the control-channel, by a microcontroller on either the serializer or deserializer side.

### Device Reset

There are three general reset options available through register writes:

1. RESET\_ALL resets all blocks including all registers, digital blocks, and analog blocks. This process is similar to driving the PWDNB pin low and then high. Note: If the sleep mode is used, do not use RESET\_ALL, as it returns the device to the sleep mode.
2. Setting RESET\_LINK resets all GMSL PHY-related digital logic and data pipelines. After this bit is set, all control registers are still accessible through the local control-channel and their values are preserved. The link and data pipelines are held in RESET until RESET\_LINK is cleared.
3. RESET\_ONESHOT resets all GMSL PHY-related digital logic and data pipelines, and then automatically clears itself. This is similar to setting and clearing RESET\_LINK.

Program the registers that affect GMSL link operation (i.e., TX\_RATE, RX\_RATE, CXTA/A/B, AUTO\_LINK, LINK\_CFG, GMSL2) first, followed by RESET\_ONESHOT, or set these registers when RESET\_LINK = 1 and then set RESET\_LINK = 0. Setting LINK\_CFG = 3 is a special case that requires writing LINK\_CFG = 3 and RESET\_ONESHOT = 1 in the same register byte write.

### Link and Video Lock

#### Link Lock

Link lock happens automatically on power-up, and is an indication the cable is plugged in and the system is up and running. Lock is obtained with no interaction or commands from the  $\mu$ C to the GMSL parts. Both serializers and deserializers have an open-drain LOCK output pin, and a related status register. If two GMSL links are used, lock status is not asserted until both links are locked.

Link lock indicates the PLLs for the GMSL3 link are locked to each other and the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I<sup>2</sup>C/UART, SPI, GPIO) can be used immediately after link lock is asserted.

The GMSL3 link uses the crystal or external reference input as the reference clock for the GMSL3 link. So, a valid video input (pixel clock) is not needed for the GMSL3 link to lock. For parts that are GMSL1 backward compatible, a valid input pixel clock is needed for link lock in GMSL1 mode.



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

**Video Lock**

Video lock bit indicates the deserializer is receiving valid video data. After the GMSL3 link is locked, the deserializer video output PLL starts its locking sequence. The deserializer normally starts outputting video data several milliseconds after it asserts line lock, provided it is receiving video packets from the serializer. The video lock status is typically read from a register. However, the deserializer LOCK pin behavior can be changed by a register setting so that the LOCK pin is asserted only when the deserializer is outputting video.

**Error and Fault-Condition Monitoring**

The MAX96792A deserializer has an open-drain, multipurpose error-reporting and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers. So, the reason for assertion of ERRB can be determined by reading the register status. Errors can be automatically forwarded across the link from a serializer so that certain serializer errors, such as CSI-2 input-CRC, can be automatically flagged by the MAX96792A's ERRB output.

The following are key points for reference:

1. ERRB is enabled by default.
2. ERRB has a 40k pullup to  $V_{DDIO}$  by default.
3. If the device powers down ( $PWDNB = 0$  or undervoltage), ERRB transitions to an HiZ state.
4. For ERRB to go low in the power-down state, an external pulldown to ground is needed.

**Clocking**

The MAX96792A requires an external reference clock source to generate internal device clocks. The external reference can be a 25MHz crystal or oscillator with  $\pm 200$ ppm accuracy.

**Spread-Spectrum Clocking**

Spread-spectrum clocking is used to mitigate electromagnetic interference emitted from the devices. Narrow frequency peaks of the clock signal are reduced by modulating the internal 6GHz clock at a rate of 25kHz with a saw-tooth profile that extends the frequency by  $\pm 1250$ ppm.

**Power Supplies**

There is no required sequence to bring up the device power supplies. An on-chip power management block manages the power domains during power-up.

The MAX96792A provides flexible power supply configurations.

The 1V core supply can be provided directly or through an internal Low Dropout (LDO) regulator. To minimize power dissipation, connect  $1.0V \pm 5\%$  to  $V_{DD}$ . If  $V_{DD} < 1.1V$  and  $CAP\_VDD < 1.05V$ , the regulator is automatically disabled at power-up and low-resistance switches connect  $V_{DD}$  to the internal supply rails. When using the internal LDO, connect  $1.2V \pm 5\%$  to  $V_{DD}$ , and following power-up, write  $REG\_ENABLE = 1$ , then write  $REG\_MNL = 1$  as part of the device initialization to enable the internal LDO.

The  $V_{DDIO}$  supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the part. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

$V_{DD18}$  is the analog supply. Connect  $1.8V \pm 5\%$ .

$V_{TERM}$  is the D-PHY/C-PHY driver and termination supply. Connect  $1.2V \pm 5\%$ .

Power supply ramp-time recommendation:  $20\mu s < \text{ramp time} < 2ms$ . Power supply ramps must be monotonic. Once the supply voltage reaches the minimum supply voltage limit, it should not be allowed to drop below the specification.

Proper power supply bypassing of all supplies is essential for high-frequency circuit stability. See [Table 4](#). See [Table 2](#) for power supply tolerances and noise requirements. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

The MAX96792A provides extensive power supply diagnostics capabilities. Undervoltage detection is included for all power supplies. Moderate undervoltage conditions on the  $V_{DD18}$  and  $V_{DDIO}$  supply voltages can be indicated using either the ERRB pin or by reading the register field associated with the power supply undervoltage flag. An undervoltage

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

condition on the  $V_{DD}$  supply, which can corrupt the register configuration, is detected by the power manager and results in a reset. Similarly, a severe undervoltage condition on  $V_{DD18}$  or  $V_{DDIO}$  also results in a reset. When a reset occurs, device configuration reverts to the power-up default state when the supplies have recovered, and the host device must initiate the power-on initialization procedure to return the device to full operation.

Overvoltage detection is also provided for all supply voltages. As in the case of undervoltage events, an overvoltage situation can be reported by the ERRB pin in addition to a dedicated internal interrupt flag. No further action is taken by the power manager during an overvoltage situation, and the device continues to operate, although it may sustain damage depending on the duration and magnitude of the overvoltage event.

When relying on the ERRB pin to convey the occurrence of an undervoltage event, connect an external  $1M\Omega$  resistor between the ERRB pin and ground, because ERRB is not a power-up default MFP function. As a result, following a reset triggered by an undervoltage event, the ERRB MFP pin reverts to high impedance as opposed to ERRB. During an error state, the host device expects ERRB to drive logic low, and the presence of the aforementioned resistor enables the appropriate logic level to be maintained following the reset, alerting the host device that attention is required.

### Power Standby and Sleep Mode

A power manager block is present in all GMSL3 products. Its primary function is to monitor supply voltages, and control power-down (standby) and sleep modes.

There are two ways to enter low-power mode while all power supplies are active: asserting the PWDNB pin or invoking the sleep state. Both states offer very-low-power supply currents.

Asserting the PWDNB pin (active-low) places the device in standby power mode, and resets the digital registers and configurations to their default power-up conditions. Any supply dropping below its internal threshold settings also places the device in power-down mode.

The sleep state preserves critical register settings and configurations. Retained registers are detailed in the Register Table. The device can be put into the sleep state through an I<sup>2</sup>C/UART command. The resume state restores the device to the presleep condition without the need for additional register writes. Resume is invoked by an I<sup>2</sup>C command or a low-frequency clock beacon transmitted from the master device over the GMSL3 link. Note that GPIO levels set by received values from the other side of the link are not retained when entering the sleep mode. Disable GPIO receive and set GPIO values to known levels before entering the sleep mode.

### PCB Layout Guidelines for GMSL

Proper circuit board design techniques are required for optimal GMSL link performance. This includes having at least a four-layer board to provide a proper ground plane reference, adequate thermal impedance, DC supply pin bypassing, power-over-coax or line-fault design, and high-speed GMSL trace impedance matching.

#### Ground Plane

A consistent ground plane, generally the second layer, is recommended to provide isolation from the high-speed GMSL traces, and other traces and components that can couple noise onto the GMSL signals. This also simplifies the design of impedance-matched transmission lines. The ground plane is also key to providing a low thermal impedance to the device's exposed paddle.

#### High-Speed GMSL Traces

Proper transmission-line design techniques are needed to achieve optimal GMSL link performance. The characteristic impedance must be closely matched to the desired impedance ( $50\Omega$  single-ended or  $100\Omega$  differential). Any mismatch increases insertion-loss and causes reflections (degrade return-loss). The suggested layout practices are:

- Use only  $100\Omega$  differential or  $50\Omega$  single-ended traces.
- Minimize length of high-speed traces.
- Minimize pad stubs by placing component pads directly on the signal trace.
- Use ground cutouts under pads as required, (1.3x area of pad).
- Follow vendor layout recommendations for components, including connectors.
- Avoid sharp bends on high-speed traces.
- Place AC-coupling capacitors within 500mils of the SIOx pins.
- Place the GMSL device as close to the serial-link connector as possible to minimize insertion loss.



- Stitch ground layers together with vias near high-speed traces.

### Power-Over-Coax Layout

When used, the Power-over-Coax (PoC) circuit must provide a low DC-series resistance to the power supply while minimizing the loading of the GMSL forward and reverse signals. The PoC circuit wants to behave as a Bias-Tee, and this requires proper layout techniques for optimal GMSL link performance, including:

- Place the smallest valued inductor (highest SRF) on the GMSL signal trace.
- Place the next smallest valued inductor after the smallest.
- Use ground cutouts as needed under first two inductors and resistors. See [Figure 37](#).
- Place the PoC as close to the device as possible, within 1/2 UI (most important for the deserializer).

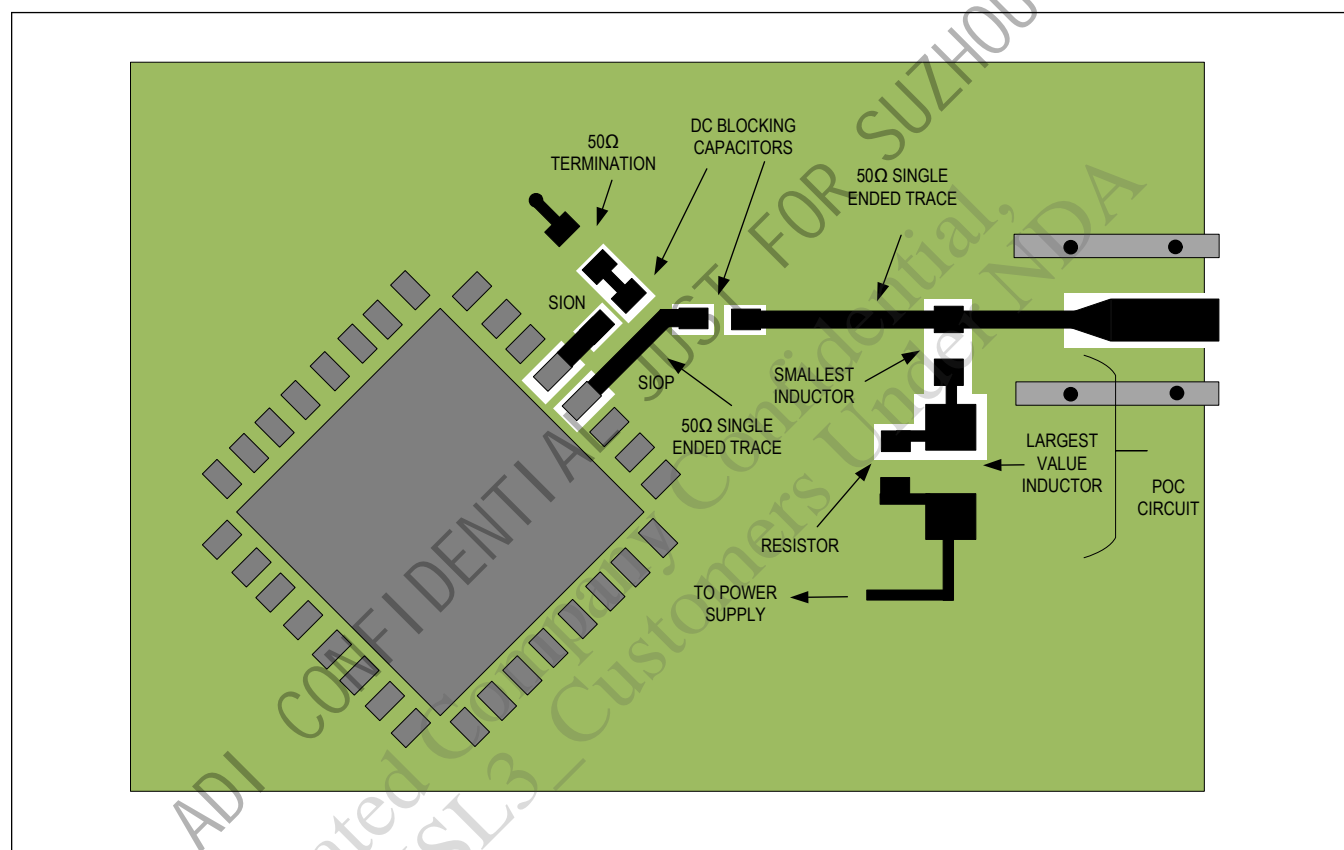


Figure 37. Coax PoC Layout Example

### Shielded Twisted-Pair Layout

Shielded Twisted-Pair (STP) designs require the differential traces to closely maintain a differential impedance of 100Ω. Use ground cutouts under AC-coupling capacitors and line-fault resistors. See [Figure 38](#).

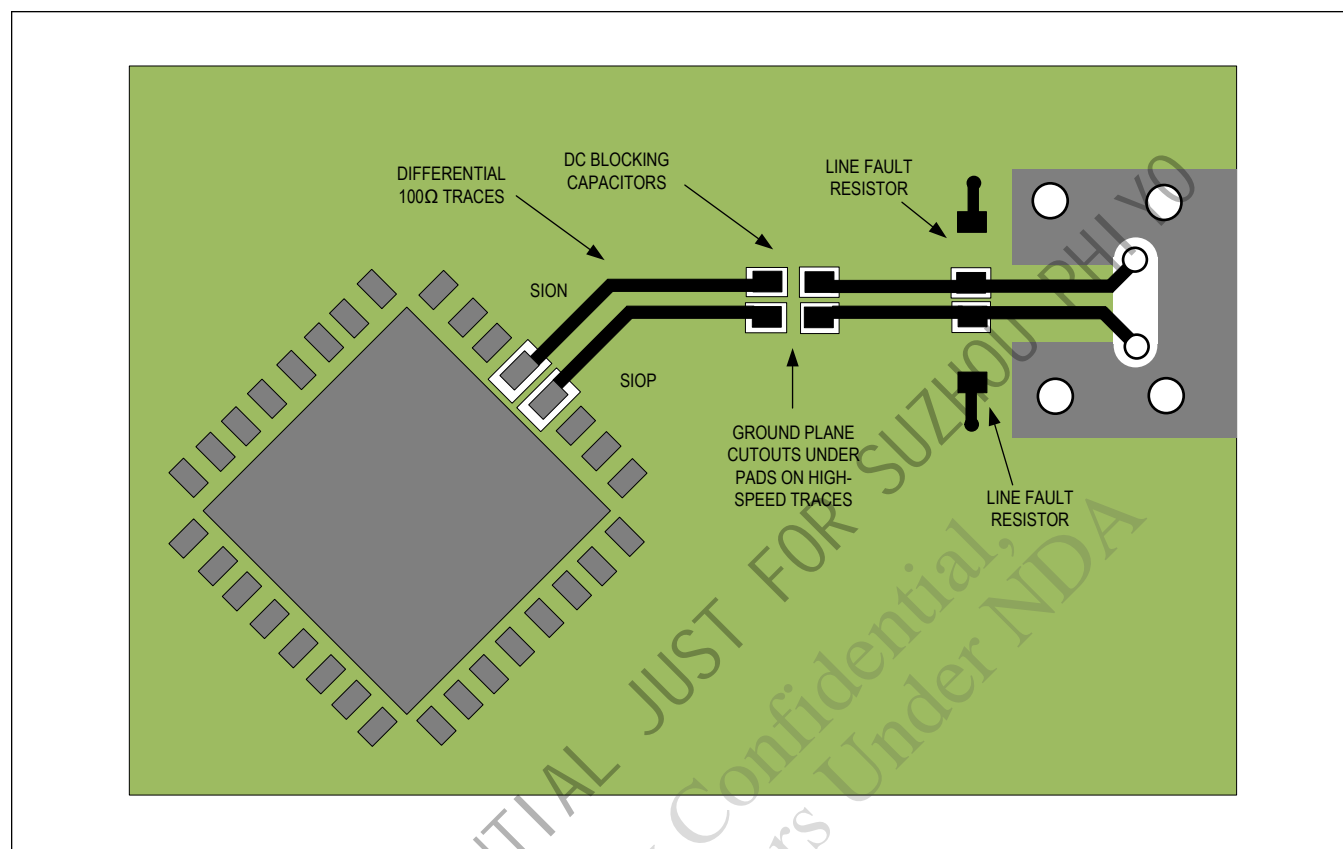


Figure 38. STP Layout Example

### Thermal Management

Power consumption of GMSL3 devices varies based on use case. Take care to provide sufficient heat dissipation with proper board and cooling design techniques. The package exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below +125°C to avoid impacting device reliability.

Refer to Tutorial 4083 ([www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial)) for further guidance.

## Applications Information

### Programming Notes

#### MANDATORY REGISTER PROGRAMMING

**Make the following register writes to ensure proper operation. Without these writes, the operation of the device as specified in the data sheet cannot be guaranteed.**

If the part is used with  $V_{DD} = 1.2V$ , execute the following register writes during initialization:

Set bit [2] = '1' in register 0x10

Set bit [4] = '1' in register 0x12

### Software Programming Model

Analog Devices' automotive serializers and deserializers follow a general software programming model. Except for features that require in-operation control-channel accesses such as ASIL safety measures and interrupt handling, use the following programming model:

1. Set the impacted functional blocks to disabled or reset mode. Place the part in IDLE state to stop all side-channel and video traffic, followed by a register write (RESET\_LINK = 1) to stop the GMSL link.
2. Fully configure the settings for each feature before it is enabled.
3. Establish the link by setting RESET\_LINK = 0 and wait for the link to lock.
4. Start video and side-channel traffic.

If changing the configuration of a feature during the operation of other features, disable the reconfigured feature, change its settings, and re-enable it.

### Main I<sup>2</sup>C/UART Tunnel

By default, the main I<sup>2</sup>C/UART control channel is also sent to the remote-side device and any peripheral connections. This allows control of the GMSL devices from either end of the link. For multimaster configurations, with microcontrollers connected to both the serializer and deserializer, disable the remote control-channel through register settings to prevent bus contention.

### Control-Channel Programming

At power-up, GMSL3 device registers are accessed and configured only through the main I<sup>2</sup>C/UART interface. The pass-through I<sup>2</sup>C/UART interfaces can be enabled for access to the device registers through register control.

### Conventional I<sup>2</sup>C/UART Control-Channel Programming

#### Host-to-Peripheral Main I<sup>2</sup>C and Pass-Through I<sup>2</sup>C Communication

When communicating between a host and peripheral, main and pass-through I<sup>2</sup>C operations are the same. A pass-through I<sup>2</sup>C across the GMSL3 link connects the host's I<sup>2</sup>C master to the peripheral's I<sup>2</sup>C slave. This logically connects separated I<sup>2</sup>C buses, enabling I<sup>2</sup>C transactions across the serial link to occur (with some delay) as if performed on the same physical I<sup>2</sup>C bus. The GMSL3 serializer and deserializer are intermediary devices; the host I<sup>2</sup>C master connects to a GMSL2 device I<sup>2</sup>C slave, and the peripheral I<sup>2</sup>C slave connects to a GMSL3 device I<sup>2</sup>C master. For example, when the host I<sup>2</sup>C master transacts on one side of the link (local-side), data is forwarded to the other side (remote-side) by the I<sup>2</sup>C slave of the local-side GMSL2 device. Data is then received by the I<sup>2</sup>C master of the remote-side GMSL2 device, which in turn generates the same I<sup>2</sup>C transaction with the peripheral slave I<sup>2</sup>C. The remote-side GMSL3 device sends back any I<sup>2</sup>C data expected by the local-side. Note, this device does not support pass-through I<sup>2</sup>C/UART channels to access the main I<sup>2</sup>C/UART control-channel on the remote side.

The I<sup>2</sup>C interface uses clock stretching (holding SCL low) to account for timing differences between the master and slave, and to allow time for data to be forwarded and received across the serial link. All local-side I<sup>2</sup>C devices must support clock stretching by the GMSL3 device. Remote-side I<sup>2</sup>C devices are not required to support clock stretching.

SDA and SCL lines operate as both an input and open-drain output. Pullup resistors are required on SDA and SCL.

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

Register addresses are 16 bits wide. Single or multiple data bytes can be written or read (by address auto-increments).

### I<sup>2</sup>C Write Packet Format

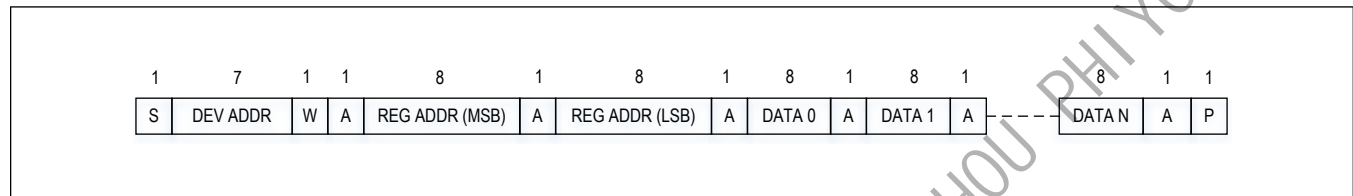


Figure 39. I<sup>2</sup>C Write Packet Format

### I<sup>2</sup>C Read Packet Format

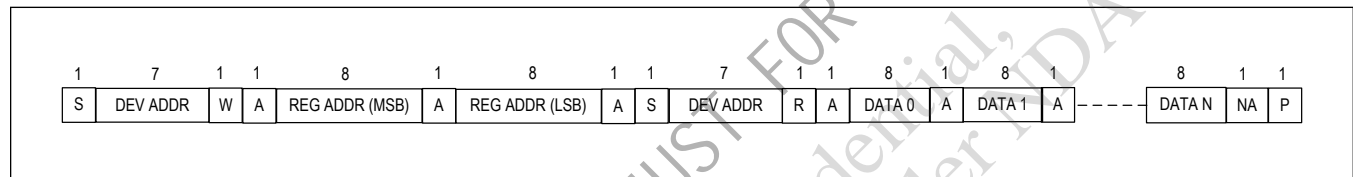


Figure 40. I<sup>2</sup>C Read Packet Format

### Main I<sup>2</sup>C Host-to-GMSL2 Device Communication

The host I<sup>2</sup>C master has access to GMSL3 serializer and deserializer registers. The host can program GMSL3 device registers to change the pass-through I<sup>2</sup>C/UART interface as I<sup>2</sup>C or UART.

### Main UART

When the main I<sup>2</sup>C/UART is configured as a UART, there are two operating modes: Base and Bypass.

### UART Base Mode

In the base mode, the microcontroller communicates with the serializer and deserializer, where registers in these and peripheral devices can be accessed. The base mode is typically enabled by default at power-up. In the base mode, the  $\mu$ C is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL3 UART-packet protocol. The  $\mu$ C can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer. The  $\mu$ C communicates with a UART peripheral in the base mode (through INTTYPE register settings). The device addresses of the serializer and deserializer in this mode are programmable. In the base mode, the serializer, deserializer, and peripheral registers can be written and read using the half-duplex GMSL3 UART protocol. The base mode is enabled by default at power-up.

[Figure 41](#) shows the UART protocol for writing and reading in the base mode.

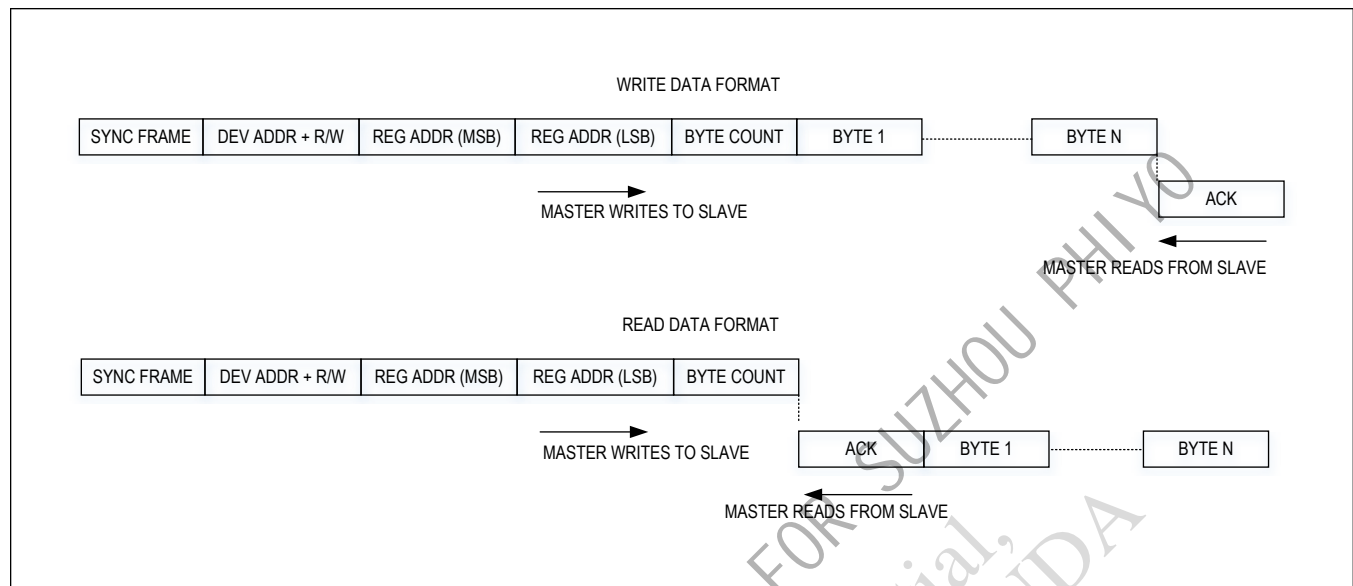


Figure 41. UART Protocol for Base Mode

### UART Bypass Mode

In the bypass mode, the serializer/deserializer ignore UART commands from the  $\mu$ C, and the  $\mu$ C communicates only with the peripherals using its own defined UART protocol. The  $\mu$ C cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL3 link. Ignoring UART transactions prevents inadvertent misprogramming of serializer and deserializer registers. The device addresses of the serializer and deserializer in this mode are not programmable.

### Switching Between UART Base and Bypass Modes

There are two ways to switch between the base and bypass modes: programming the BYPASS\_TO register and using the device MS pin.

When setting the bypass mode through register, BYPASS\_TO is programmed to have a timeout (2ms, 8ms, or 32ms). The bypass mode is active only as long as there is UART activity. When there is no UART activity for the selected timeout, both devices exit the bypass mode and the bit is automatically cleared.

When in the UART bypass mode, random data may be output if link lock is lost. This issue can be avoided by not enabling the UART bypass mode until all initial device programming is completed.

When set by the MS pin, a high-level puts the device into the bypass mode, and a low-level puts the device in the base mode. MS is set on the fly and is not latched on power-up.

### UART Frame Format

Regular UART frames with an even-parity bit are used to carry 1 byte of data each. A frame consists of a low-start bit followed by 8 data bits, a parity bit, and a high-stop bit. The parity bit is high if the number of 1s in the 8-bit data is odd; otherwise, it is low. There must be at least 1 high-stop bit. If the next frame is in the same packet, there can be at most 4 high bits from the end of the stop bit to the beginning of the next start bit. Note that for a parity-bit error, the packet, starting from the frame with the error, is discarded. The start of each frame is always a high-to-low transition (i.e., the stop-bit is high and the start-bit is low). The phase of the internal UART bit clock is adjusted using the start-bit of each frame. The framer calibrates the length of 1 UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In the bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions; the recipient of the data must perform error checking. The parity bit can optionally be disabled before entering the bypass mode. Note that the bit rate in the bypass mode must be the same bit rate last used in the base mode. See [Figure 42](#).

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

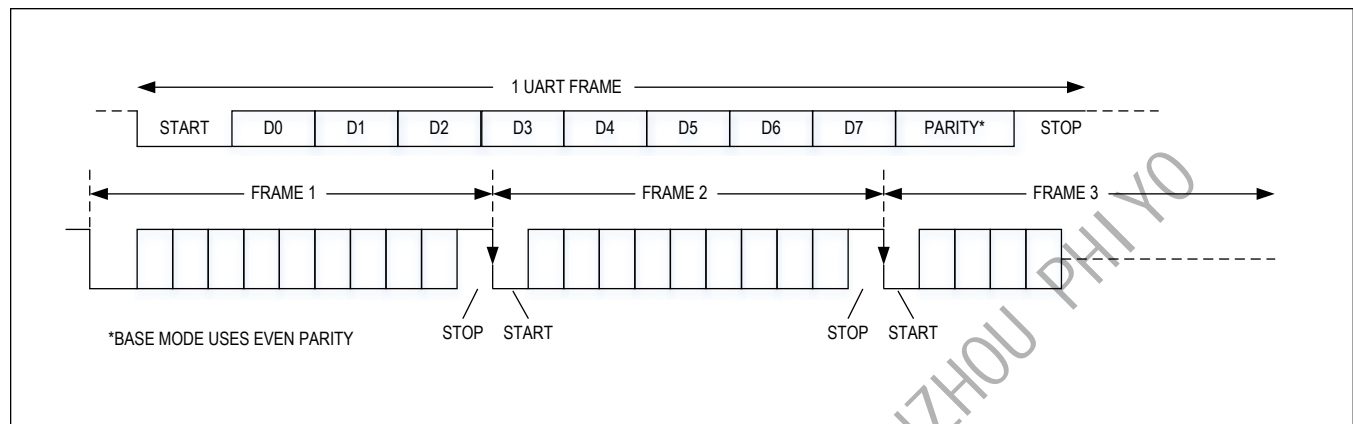


Figure 42. UART Data Format for Base Mode

### Synchronization Frame

The serializer/deserializer must calibrate internal bit-length counters with the UART bit rate for proper recovery of UART frames. The  $\mu$ C sends a synchronization frame (a regular UART frame with the value 0x79) as the first frame of each data packet. The synchronization frame allows the addressed device to calibrate the bit length in terms of the device's internal 150 MHz clock. A synchronization frame must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next synchronization frame. See [Figure 43](#).

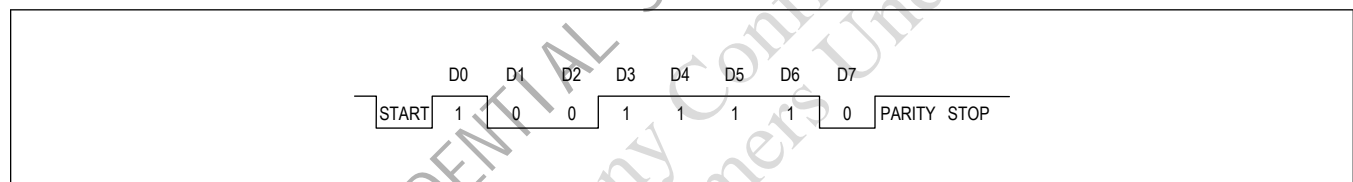


Figure 43. UART Synchronization Frame

### Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the  $\mu$ C that no errors are detected in the transmitted packet. The acknowledge frame is sent after the last bit of a valid packet is received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent. See [Figure 44](#).

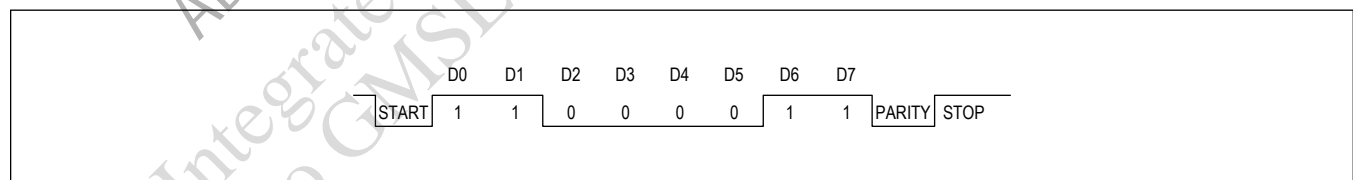


Figure 44. UART Acknowledge Frame

### Write Packet

Write packets consist of a 5-byte packet header followed by 1 or more data bytes. A packet is recognized as a write packet when the LSB of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors are detected while receiving a valid write packet. Byte Count indicates the number of data bytes to be written, and this number cannot be zero. See [Figure 45](#).

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

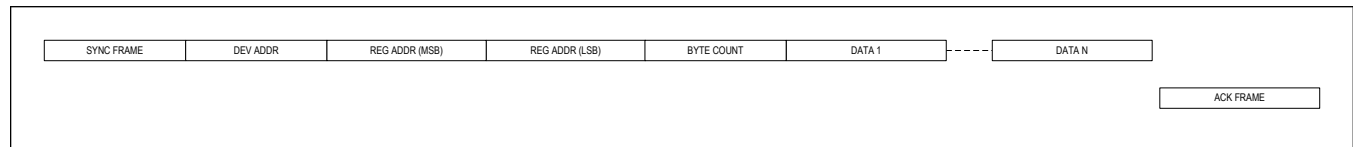


Figure 45. UART Write Packet Format

### Read Packet

Read packets consist of 5 bytes. The LSB of the device address frame is 1 for read packets. If no errors are detected while receiving a valid read packet, the addressed device responds with an acknowledge frame followed by 1 or more data bytes. Byte Count indicates the number of data bytes to be read and this number cannot be zero. See [Figure 46](#).

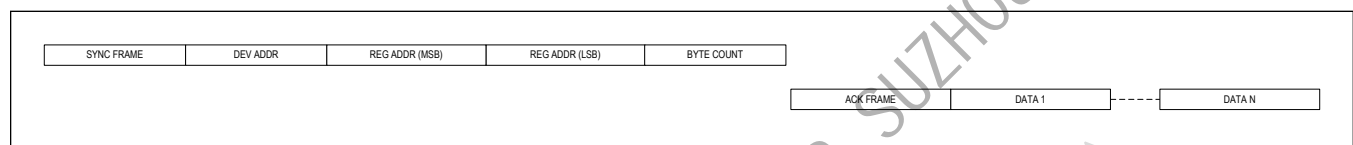


Figure 46. UART Read Packet Format

### I<sup>2</sup>C/UART Control-Channel Programming with Optional CRC and Message Counter

The MAX96792A provides additional functional safety by adding an optional CRC to I<sup>2</sup>C/UART read/write transactions, and a separate message counter for read and write packets. These features are disabled by default at power-up, but can be enabled by register settings. The CRC and message counter can be used together or individually. The CRC and message counter features only apply to device register read/write transactions, and are not supported for pass-through traffic. The CRC and/or message counter can be enabled in the serializer, deserializer, or both.

### I<sup>2</sup>C/UART CRC and Message Counter Options

At power-up, the I<sup>2</sup>C/UART CRC and Message Counter features are disabled by default in the MAX96792A. Both features can be enabled or disabled through register control.

### I<sup>2</sup>C Writes with CRC

To provide additional functional safety for Advanced Driver Assistance Systems (ADAS) applications, the MAX96792A supports the addition of a Cyclic Redundancy Check (CRC) to I<sup>2</sup>C transactions. When enabled, the master  $\mu$ C must compute and send a CRC byte after each data byte. See [Figure 47](#). For each single-byte or multibyte write, the serializer first clears the CRC engine. The first CRC includes the device address byte, register address bytes, message counter bytes, and first data byte. For all following data bytes, the CRC engine is reset and the CRC byte covers the additional data byte. See [Figure 48](#) and [Figure 49](#). The serializer receives the data byte, calculates the CRC using an identical CRC engine, and verifies a match before accepting the data byte. If the CRCs do not match, a write is not accepted, a NACK is transmitted, and the error counter is triggered.

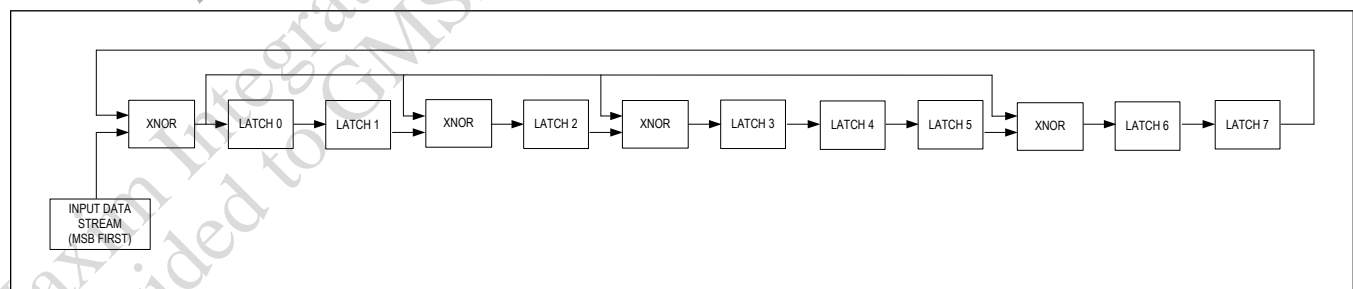


Figure 47. I<sup>2</sup>C CRC Engine



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

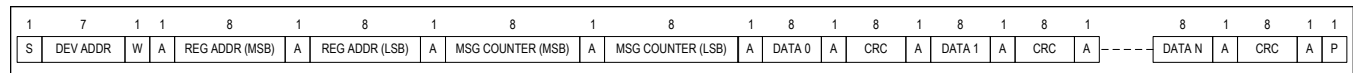


Figure 48. I<sup>2</sup>C Multiple-Byte Write with CRC

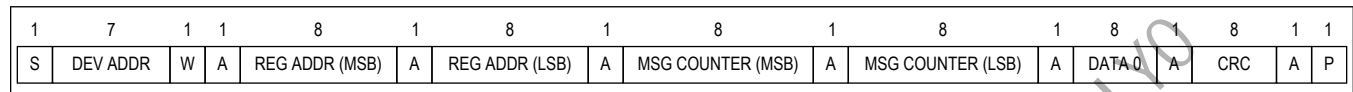


Figure 49. I<sup>2</sup>C Single-Byte Write with CRC

### I<sup>2</sup>C Reads with CRC

For I<sup>2</sup>C reads of the MAX96792A's registers, the device's CRC engine clears and then uses the outgoing device address byte, register address bytes, message counter bytes, and first data byte to calculate the CRC byte. This is added to the data stream directly after the corresponding data byte. The CRC engine is subsequently cleared again for all other data bytes. See [Figure 50](#) and [Figure 51](#). When the  $\mu$ C receives the I<sup>2</sup>C read data, either through the MAX96792A or directly from the device on the other side of the link, the  $\mu$ C's CRC engine should calculate a CRC byte for each data byte and compare with the transmitted CRC byte.

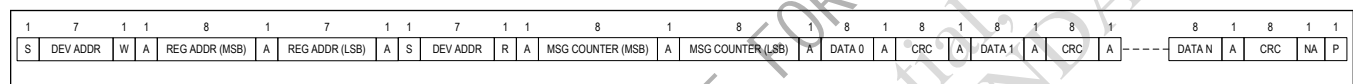


Figure 50. I<sup>2</sup>C Multiple-Byte Read with CRC

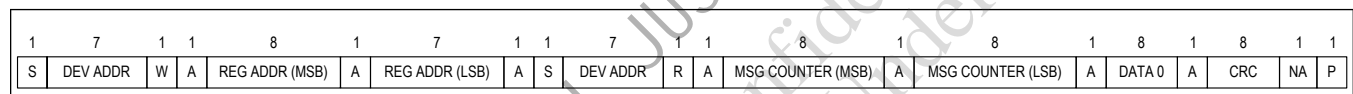


Figure 51. I<sup>2</sup>C Single-Byte Read with CRC

### Message Counter Writes

An additional functional safety feature of the MAX96792A is a message counter, which can be used with the I<sup>2</sup>C/UART CRC feature. If enabled, the device expects a 2-byte message count from the  $\mu$ C, indicating the number of writes being sent. The MAX96792A counts the number of write transactions and compares it with the count sent by the  $\mu$ C. If the two counts match, the write is accepted. If the two counts do not match, the write is rejected, a NACK is sent in return, and the error counter is incremented. A programmable threshold for the error counter asserts ERRB, when reached.

### Message Counter Reads

For read transactions, the MAX96792A sends the message counter value to the  $\mu$ C along with the requested data. The  $\mu$ C should compare the sent message count against its stored value and accept the data if the counts match. Note that a read transaction has a repeated start condition, with the device address byte sent twice. This results in each read transaction incrementing the message counter twice, once for each device address byte. If the two message counter values do not agree, the data should be rejected.

If a read is requested from the last used registers address, resulting in only one device address byte, the message counter is incremented once.

If the message counter values for the MAX96792A and  $\mu$ C do not agree, the device's message counter can be reset using a register write and the  $\mu$ C's counter should also be reset. If the  $\mu$ C is reset, or if its message counter is reset for any reason, the devices' counter must be reset using a register write as well.

### UART Writes with CRC

To provide additional functional safety for Advanced Driver Assistance Systems (ADAS) applications, the MAX96792A supports the addition of a Cyclic Redundancy Check (CRC) to UART transactions. When enabled, the master  $\mu$ C must compute and send a CRC byte after each data byte. See [Figure 52](#). For each single-byte or multibyte write, first clear the CRC engine. The first CRC includes the sync frame, device address byte, register address bytes, message counter bytes, and the first data byte. All bytes are sent LSB first. For all following data bytes, the CRC engine is reset and



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

the CRC byte covers the additional data byte. See [Figure 53](#) and [Figure 54](#). The MAX96792A receives the data byte, calculates the CRC using an identical CRC engine, and verifies a match before accepting the data byte. If the CRCs do not match, a write is not accepted, a NACK is transmitted, and the error counter is triggered.

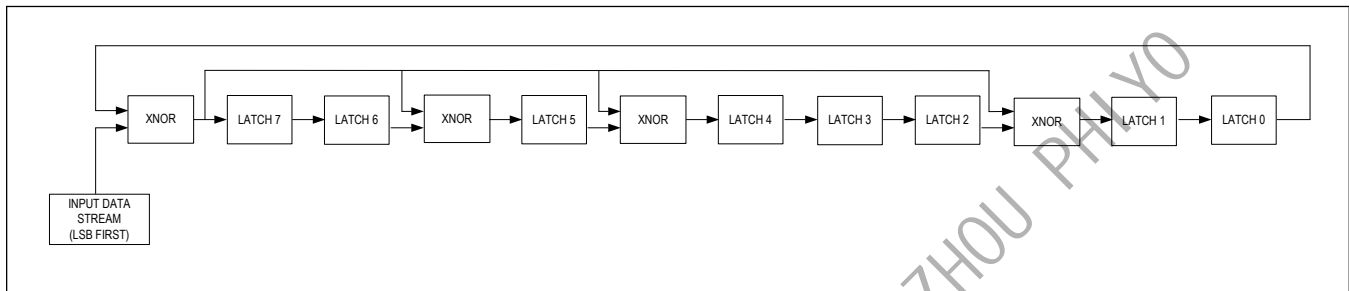


Figure 52. UART CRC Engine

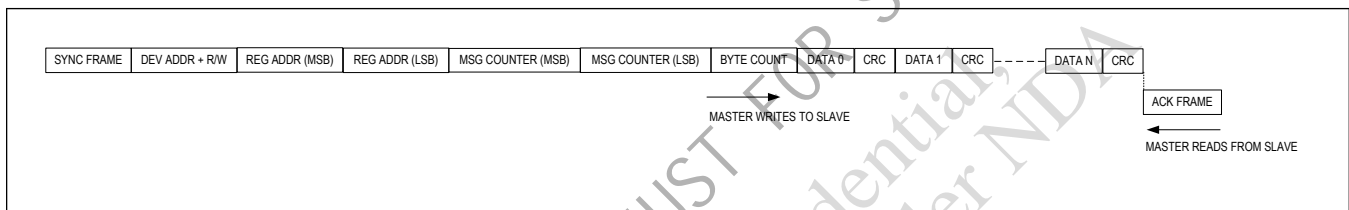


Figure 53. UART Multiple-Byte Write Transactions with CRC

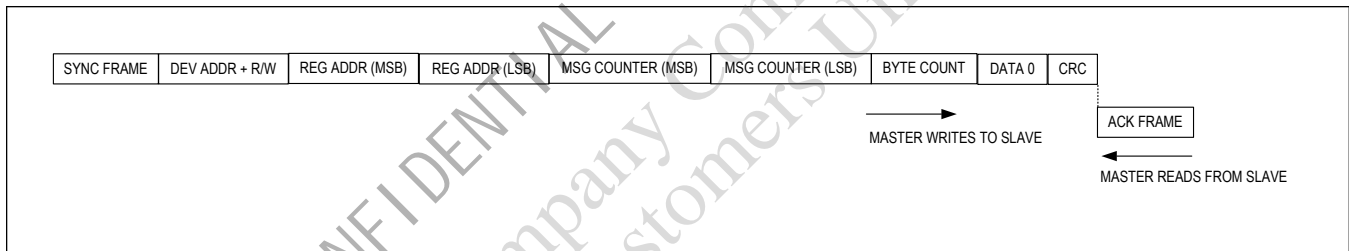


Figure 54. UART Single-Byte Write Transaction with CRC

### UART Reads with CRC

For UART reads of MAX96792A's registers, the device's CRC engine clears and then uses the outgoing sync frame, device address byte, register address bytes, message counter bytes, and the first data byte to calculate the CRC byte. This is added to the data stream directly after the corresponding data byte. All bytes are sent LSB first. The CRC engine is subsequently cleared again for all other data bytes. See [Figure 55](#) and [Figure 56](#). When the  $\mu$ C receives the UART read data, either through the serializer on the other side of the link or directly from the MAX96792A, the  $\mu$ C's CRC engine can calculate a CRC byte for each data byte and compare with the transmitted CRC byte. The ACK frame is not included in the CRC calculation because the  $\mu$ C is looking for the ACK value of 0xC3. If there is an error, the  $\mu$ C treats the frame as a NACK and rejects the data. Note that the read command from the  $\mu$ C does not include CRC.

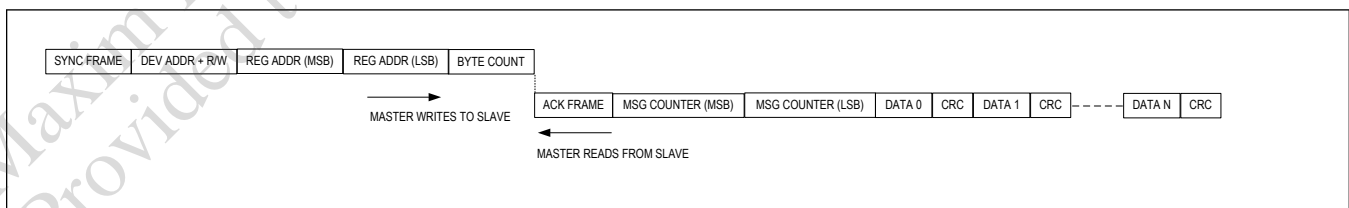


Figure 55. UART Multiple-Byte Read Transaction with CRC

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

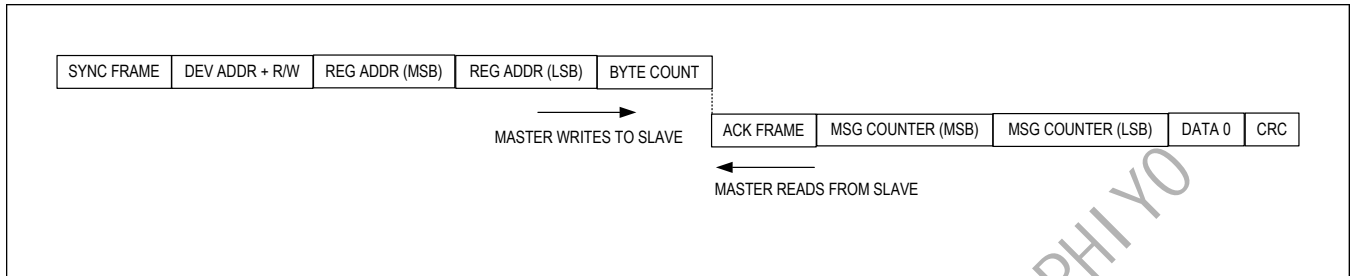


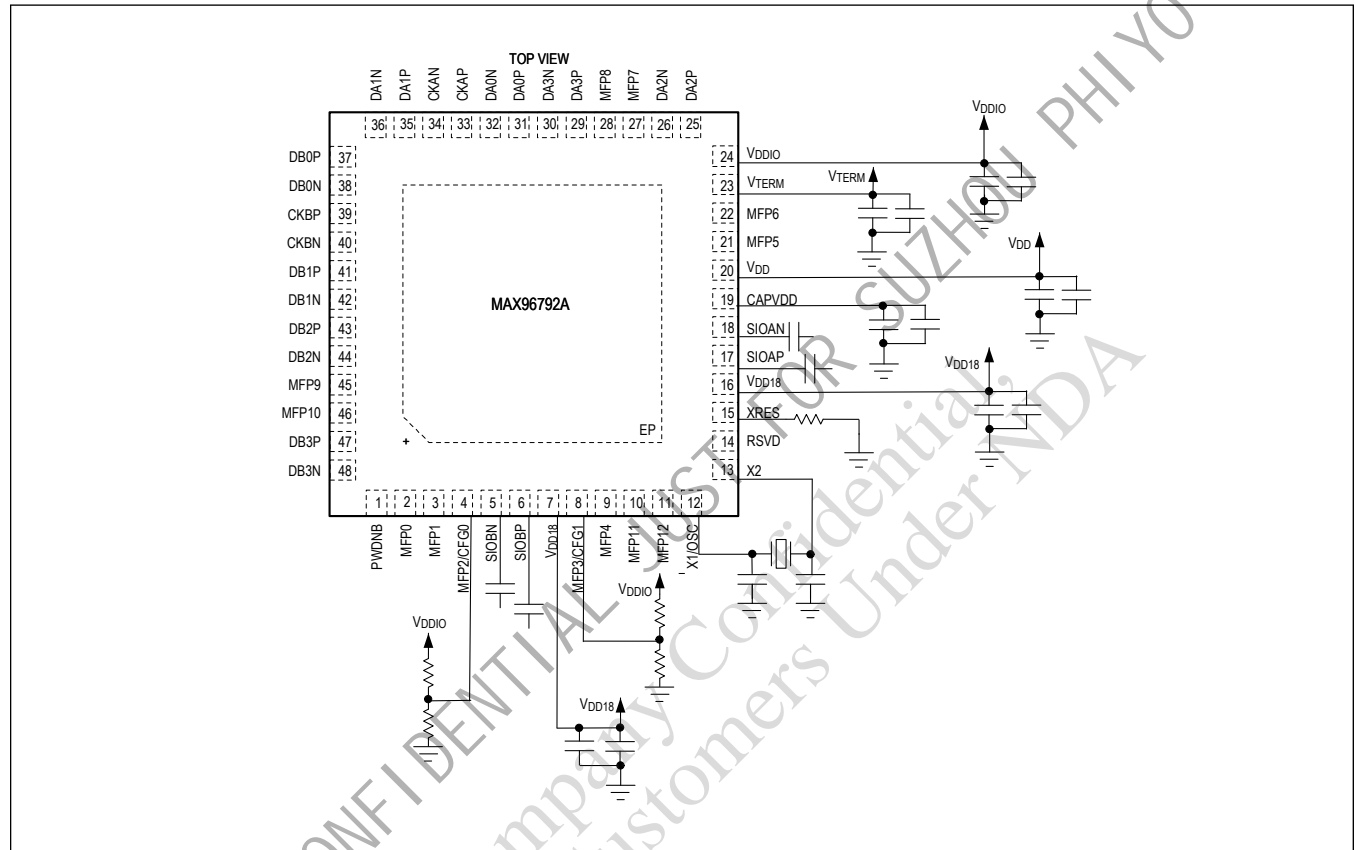
Figure 56. UART Single-Byte Read Transaction with CRC

## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

### Typical Application Circuits

See [Table 4](#).



### Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX96792AGTM/VY+	-40°C to +105°C	48 TQFN wettable flank
MAX96792AGTM/VY+T	-40°C to +105°C	48 TQFN wettable flank

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V Denotes automotive qualified.

Y Denotes wettable flank.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

## Register Map

### Reserved, Unused, and Read-Only Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write).

In this document, default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

See Programming Notes section for important mandatory register writes on start-up.

Note: \*Indicates the register is stored when entering sleep mode and is restored upon exit.

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x90	REG0[7:0]*	DEV_ADDR[6:0]							CFG_BLK_OCK
0x01	0x02	REG1[7:0]*	IIC_2_EN_N	IIC_1_EN_N	DIS_LO_CAL_CC	DIS_REM_CC	TX_RATE[1:0]		RX_RATE[1:0]	
0x02	0x63	REG2[7:0]*	–	VID_EN_Z	VID_EN_Y	–	–	–	RSVD	RSVD
0x03	0x53	REG3[7:0]*	LOCK_CFG	PT_SWAP	UART_2_EN	UART_1_EN	–	DIS_REM_CC_B	RSVD	RSVD
0x04	0xC2	REG4[7:0]*	GMSL3_B	GMSL3_A	RSVD	RSVD	TX_RATE_B[1:0]		RX_RATE_B[1:0]	
0x05	0xC0	REG5[7:0]*	LOCK_EN_N	ERRB_EN_N	LOCK_ALT_EN	RSVD	PU_LF3	PU_LF2	PU_LF1	PU_LF0
0x06	0xC0	REG6[7:0]*	RSVD	RSVD	RSVD	I2CSEL	RSVD[3:0]			
0x07	0x27	REG7[7:0]*	CMP_VTERM_STATUS	–	RSVD[5:0]					
0x0D	0xB6	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x03	REG14[7:0]	RSVD[3:0]				DEV_REV[3:0]			
0x26	0x22	REG26[7:0]	–	LF_1[2:0]			–	LF_0[2:0]		
0x27	0x22	REG27[7:0]	–	LF_3[2:0]			–	LF_2[2:0]		
0x38	0x00	IO_CHK0[7:0]	PIN_DRV_EN_0[7:0]							
OVERLAP										
TCTRL										
0x08	0x00	PWR0[7:0]	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x09	0x00	PWR1[7:0]	RSVD	RSVD	PORZ_STATUS[5:0]					
0x0C	0x15	PWR4[7:0]*	RSVD	DIS_LO_CAL_WAKE	WAKE_EN_N_B	WAKE_EN_N_A	RSVD[3:0]			
0x10	0x11	CTRL0[7:0]*	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	REG_ENABLED	LINK_CFG[1:0]	

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x11	0x0A	<a href="#">CTRL1[7:0]*</a>	RSVD	RSVD	RSVD	–	RSVD	CXTP_B	RSVD	CXTP_A
0x12	0x04	<a href="#">CTRL2[7:0]</a>	RSVD	RSVD	RESET_ONESHOT_B	REG_MNL	RSVD[1:0]		RSVD[1:0]	
0x13	0x10	<a href="#">CTRL3[7:0]</a>	RSVD	RSVD	LINK_MODE[1:0]		LOCKED	ERROR	CMU_LOCKED	RESET_LINK_B
0x18	0xA0	<a href="#">INTR0[7:0]*</a>	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x19	0x00	<a href="#">INTR1[7:0]*</a>	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x1A	0x0B	<a href="#">INTR2[7:0]*</a>	RSVD	RSVD	REM_ERR_OEN	RSVD	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
0x1B	0x00	<a href="#">INTR3[7:0]</a>	RSVD	RSVD	REM_ERR_FLAG	RSVD	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x1C	0x09	<a href="#">INTR4[7:0]*</a>	EOM_ERR_OEN_B	EOM_ERR_OEN_A	FEC_RX_ERR_OEN	–	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
0x1D	0x00	<a href="#">INTR5[7:0]</a>	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	FEC_RX_ERR_FLAG	–	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
0x1E	0x1C	<a href="#">INTR6[7:0]*</a>	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	FSYNC_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	–	VID_PXL_CRC_ERR_OEN
0x1F	0x00	<a href="#">INTR7[7:0]</a>	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	FSYNC_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	–	VID_PXL_CRC_ERR
0x20	0xFF	<a href="#">INTR8[7:0]*</a>	ERR_TX_EN	RSVD	ERR_TX_EN_B	ERR_TX_ID[4:0]				
0x21	0xFF	<a href="#">INTR9[7:0]*</a>	ERR_RX_EN	RSVD	ERR_RX_EN_B	ERR_RX_ID[4:0]				
0x22	0x00	<a href="#">CNT0[7:0]</a>	DEC_ERR_A[7:0]							
0x23	0x00	<a href="#">CNT1[7:0]</a>	DEC_ERR_B[7:0]							
0x24	0x00	<a href="#">CNT2[7:0]</a>	IDLE_ERR[7:0]							
0x25	0x00	<a href="#">CNT3[7:0]</a>	PKT_CNT[7:0]							
GMSL										
0x28	0x60	<a href="#">TX0[7:0]*</a>	RSVD[1:0]		RSVD	RSVD	–	–	RX_FEC_EN	RSVD
0x29	0x08	<a href="#">TX1[7:0]*</a>	LINK_PBS_GEN	RSVD	–	ERRG_EN_A	RSVD	RSVD	RSVD	RSVD
0x2A	0x20	<a href="#">TX2[7:0]*</a>	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x2B	0x44	<a href="#">TX3[7:0]*</a>	RSVD[1:0]		RX_FEC_ACTIVE	RSVD	–	RSVD[2:0]		
0x2C	0x00	<a href="#">RX0[7:0]*</a>	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
0x2D	0x28	<a href="#">RX1[7:0]*</a>	LINK_PBS_CHK	RSVD	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x2F	0x00	<a href="#">RX3[7:0]</a>	–	–	–	RSVD	RSVD	RSVD	RSVD	RSVD
0x30	0x41	<a href="#">GPIOA[7:0]*</a>	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
0x31	0x88	<a href="#">GPIOB[7:0]*</a>	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
CC										
0x40	0x26	<a href="#">I2C_0[7:0]*</a>	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x41	0x56	<a href="#">I2C_1[7:0]*</a>	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x42	0x00	<a href="#">I2C_2[7:0]*</a>	SRC_A[6:0]						–	
0x43	0x00	<a href="#">I2C_3[7:0]*</a>	DST_A[6:0]						–	
0x44	0x00	<a href="#">I2C_4[7:0]*</a>	SRC_B[6:0]						–	
0x45	0x00	<a href="#">I2C_5[7:0]*</a>	DST_B[6:0]						–	
0x47	0x00	<a href="#">I2C_7[7:0]</a>	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REMAK_ACKED	REMAK_RECVED
0x48	0x42	<a href="#">UART_0[7:0]*</a>	RSVD[1:0]		REMS_EN	LOC_MS_EN	BYPASS_DIS_PARR	BYPASS_TO[1:0]		BYPASS_EN
0x49	0x96	<a href="#">UART_1[7:0]</a>	BITLEN_LSB[7:0]							
0x4A	0x80	<a href="#">UART_2[7:0]</a>	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
0x4C	0x26	<a href="#">I2C_PT_0[7:0]</a>	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
0x4D	0x56	<a href="#">I2C_PT_1[7:0]</a>	RSVD	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
0x4E	0x00	<a href="#">I2C_PT_2[7:0]</a>	RSVD	I2C_TIMED_OUT_2	RSVD	RSVD	RSVD	I2C_TIMED_OUT_1	RSVD	RSVD
0x4F	0x88	<a href="#">UART_PT_0[7:0]</a>	BITLEN_MAN_CFG_2	DIS_PARR_2	RSVD	RSVD	BITLEN_MAN_CFG_1	DIS_PARR_1	RSVD	RSVD
CFGH_VIDEO_X										
0x50	0x00	<a href="#">RX0[7:0]*</a>	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGH_VIDEO_Y										
0x51	0x01	<a href="#">RX0[7:0]*</a>	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGH_VIDEO_Z										
0x52	0x02	<a href="#">RX0[7:0]*</a>	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGH_VIDEO_U										
0x53	0x03	<a href="#">RX0[7:0]*</a>	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGH_INFOFR										
0x60	0xF0	<a href="#">TR0[7:0]*</a>	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x61	0xB0	<a href="#">TR1[7:0]*</a>	BW_MULT[1:0]			BW_VAL[5:0]				
0x63	0x00	<a href="#">TR3[7:0]*</a>	–	–	–	–	–	TX_SRC_ID[2:0]		
0x64	0xFF	<a href="#">TR4[7:0]*</a>	RX_SRC_SEL[7:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
CFGL SPI										
0x68	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x69	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x6B	0x00	TR3[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0x6C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x6D	0x98	ARQ0[7:0]*	RSVD	RSVD	MATCH_SRC_ID	ACK_SR_C_ID	EN	DIS_DBL_ACK_R_ETX	–	–
0x6E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x6F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGCC CC										
0x70	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x71	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x73	0x00	TR3[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0x74	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x75	0x98	ARQ0[7:0]*	RSVD	RSVD	MATCH_SRC_ID	ACK_SR_C_ID	EN	DIS_DBL_ACK_R_ETX	–	–
0x76	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x77	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL GPIO										
0x78	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x79	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x7B	0x00	TR3[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0x7C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x7D	0x98	ARQ0[7:0]*	RSVD	RSVD	MATCH_SRC_ID	ACK_SR_C_ID	EN	DIS_DBL_ACK_R_ETX	–	–
0x7E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x7F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGCC IIC_X										
0x80	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x81	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x83	0x00	TR3[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0x84	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x85	0x98	<a href="#">ARQ0[7:0]*</a>	RSVD	RSVD	MATCH_SRC_ID	ACK_SR_C_ID	EN	DIS_DBL_ACK_R_ETX	-	-
0x86	0x72	<a href="#">ARQ1[7:0]*</a>	-	MAX_RT[2:0]			-	-	MAX_RT_ERR_OEN	RT_CNT_OEN
0x87	0x00	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR	RT_CNT[6:0]						
CFG_C IIC_Y										
0x88	0xF0	<a href="#">TR0[7:0]*</a>	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x89	0xB0	<a href="#">TR1[7:0]*</a>	BW_MULT[1:0]		BW_VAL[5:0]					
0x8B	0x00	<a href="#">TR3[7:0]*</a>	-	-	-	-	-	TX_SRC_ID[2:0]		
0x8C	0xFF	<a href="#">TR4[7:0]*</a>	RX_SRC_SEL[7:0]							
0x8D	0x98	<a href="#">ARQ0[7:0]*</a>	RSVD	RSVD	MATCH_SRC_ID	ACK_SR_C_ID	EN	DIS_DBL_ACK_R_ETX	-	-
0x8E	0x72	<a href="#">ARQ1[7:0]*</a>	-	MAX_RT[2:0]			-	-	MAX_RT_ERR_OEN	RT_CNT_OEN
0x8F	0x00	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR	RT_CNT[6:0]						
VID_RX Y										
0x112	0x32	<a href="#">VIDEO_RX0[7:0]*</a>	LCRC_E RR	RSVD	RSVD	RSVD	RSVD	LINE_C RC_SEL	LINE_C RC_EN	DIS_PKT_DET
0x115	0x40	<a href="#">VIDEO_RX3[7:0]*</a>	RSVD	HD_TR_MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN
0x118	0x02	<a href="#">VIDEO_RX6[7:0]</a>	RSVD[2:0]			RSVD	LIM_HE ART	-	RSVD	RSVD
0x11A	0x02	<a href="#">VIDEO_RX8[7:0]</a>	VID_BLK_LEN_E RR	VID_LO CK	VID_PKT_DET	VID_SE Q_ERR	RSVD[3:0]			
0x11C	0x00	<a href="#">VIDEO_RX10[7:0]</a>	VID_OV ERFLOW	MASK_V IDEO_D E	RSVD[5:0]					
VID_RX Z										
0x124	0x32	<a href="#">VIDEO_RX0[7:0]*</a>	LCRC_E RR	RSVD	RSVD	RSVD	RSVD	LINE_C RC_SEL	LINE_C RC_EN	DIS_PKT_DET
0x127	0x40	<a href="#">VIDEO_RX3[7:0]*</a>	RSVD	HD_TR_MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN
0x12A	0x02	<a href="#">VIDEO_RX6[7:0]</a>	RSVD[2:0]			RSVD	LIM_HE ART	-	RSVD	RSVD
0x12C	0x02	<a href="#">VIDEO_RX8[7:0]</a>	VID_BLK_LEN_E RR	VID_LO CK	VID_PKT_DET	VID_SE Q_ERR	RSVD[3:0]			
0x12E	0x00	<a href="#">VIDEO_RX10[7:0]</a>	VID_OV ERFLOW	MASK_V IDEO_D E	RSVD[5:0]					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB	
VIDEO_PIPE_SEL											
0x160	0x03	VIDEO_PIPE_EN[7:0]*	–	–	–	–	–	–	VIDEO_PIPE_EN[1:0]		
0x161	0x32	VIDEO_PIPE_SEL[7:0]*	–	–	VIDEO_PIPE_SEL_Z[2:0]			VIDEO_PIPE_SEL_Y[2:0]			
0x162	0x00	LINK_SEL[7:0]*	–	–	–	–	SPI_LINK_SELECT	UART_2_LINK_SELECT	UART_1_LINK_SELECT	UART_0_LINK_SELECT	
SPI											
0x170	0x08	SPI_0[7:0]*	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNORE_ID	SPI_CC_EN	MST_SLVN	SPI_EN	
0x171	0x1D	SPI_1[7:0]*	SPI_LOC_N[5:0]							SPI_BASE_PRIO[1:0]	
0x172	0x03	SPI_2[7:0]*	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_M0D3_F	SPI_M0D3	SPIM_S2_ACT_H	SPIM_S1_ACT_H	
0x173	0x00	SPI_3[7:0]*	SPIM_SS_DLY_CLKS[7:0]								
0x174	0x00	SPI_4[7:0]*	SPIM_SCK_LO_CLKS[7:0]								
0x175	0x00	SPI_5[7:0]*	SPIM_SCK_HI_CLKS[7:0]								
0x176	0x00	SPI_6[7:0]*	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN	
0x177	0x00	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	RO_ALT	SPIS_BYTE_CNT[4:0]					
0x178	0x00	SPI_8[7:0]*	REQ_HOLD_OFF_TO[7:0]								
WM											
0x190	0x00	WM_0[7:0]*	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN	
0x192	0x50	WM_2[7:0]*	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]		
0x194	0x10	WM_4[7:0]	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]		
0x195	0x00	WM_5[7:0]	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR	
0x196	0x00	WM_6[7:0]	WM_TIMER[7:0]								
0x1AE	0x00	WM_WREN_0[7:0]	WM_WREN_L[7:0]								
0x1AF	0x00	WM_WREN_1[7:0]	WM_WREN_H[7:0]								
VRX Y											
0x1E0	0x00	CROSS_0[7:0]*	–	CROSS0_I	CROSS0_F	CROSS0[4:0]					
0x1E1	0x01	CROSS_1[7:0]*	–	CROSS1_I	CROSS1_F	CROSS1[4:0]					
0x1E2	0x02	CROSS_2[7:0]*	–	CROSS2_I	CROSS2_F	CROSS2[4:0]					
0x1E3	0x03	CROSS_3[7:0]*	–	CROSS3_I	CROSS3_F	CROSS3[4:0]					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB						LSB
0x1E4	0x04	<a href="#">CROSS_4[7:0]</a> I*	–	CROSS4_I	CROSS4_F	CROSS4[4:0]			
0x1E5	0x05	<a href="#">CROSS_5[7:0]</a> I*	–	CROSS5_I	CROSS5_F	CROSS5[4:0]			
0x1E6	0x06	<a href="#">CROSS_6[7:0]</a> I*	–	CROSS6_I	CROSS6_F	CROSS6[4:0]			
0x1E7	0x07	<a href="#">CROSS_7[7:0]</a> I*	–	CROSS7_I	CROSS7_F	CROSS7[4:0]			
0x1E8	0x08	<a href="#">CROSS_8[7:0]</a> I*	–	CROSS8_I	CROSS8_F	CROSS8[4:0]			
0x1E9	0x09	<a href="#">CROSS_9[7:0]</a> I*	–	CROSS9_I	CROSS9_F	CROSS9[4:0]			
0x1EA	0x0A	<a href="#">CROSS_10[7:0]</a> I*	–	CROSS10_I	CROSS10_F	CROSS10[4:0]			
0x1EB	0x0B	<a href="#">CROSS_11[7:0]</a> I*	–	CROSS11_I	CROSS11_F	CROSS11[4:0]			
0x1EC	0x0C	<a href="#">CROSS_12[7:0]</a> I*	–	CROSS12_I	CROSS12_F	CROSS12[4:0]			
0x1ED	0x0D	<a href="#">CROSS_13[7:0]</a> I*	–	CROSS13_I	CROSS13_F	CROSS13[4:0]			
0x1EE	0x0E	<a href="#">CROSS_14[7:0]</a> I*	–	CROSS14_I	CROSS14_F	CROSS14[4:0]			
0x1EF	0x0F	<a href="#">CROSS_15[7:0]</a> I*	–	CROSS15_I	CROSS15_F	CROSS15[4:0]			
0x1F0	0x10	<a href="#">CROSS_16[7:0]</a> I*	–	CROSS16_I	CROSS16_F	CROSS16[4:0]			
0x1F1	0x11	<a href="#">CROSS_17[7:0]</a> I*	–	CROSS17_I	CROSS17_F	CROSS17[4:0]			
0x1F2	0x12	<a href="#">CROSS_18[7:0]</a> I*	–	CROSS18_I	CROSS18_F	CROSS18[4:0]			
0x1F3	0x13	<a href="#">CROSS_19[7:0]</a> I*	–	CROSS19_I	CROSS19_F	CROSS19[4:0]			
0x1F4	0x14	<a href="#">CROSS_20[7:0]</a> I*	–	CROSS20_I	CROSS20_F	CROSS20[4:0]			
0x1F5	0x15	<a href="#">CROSS_21[7:0]</a> I*	–	CROSS21_I	CROSS21_F	CROSS21[4:0]			
0x1F6	0x16	<a href="#">CROSS_22[7:0]</a> I*	–	CROSS22_I	CROSS22_F	CROSS22[4:0]			
0x1F7	0x17	<a href="#">CROSS_23[7:0]</a> I*	–	CROSS23_I	CROSS23_F	CROSS23[4:0]			
0x1F8	0x18	<a href="#">CROSS_HS[7:0]</a> I*	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]			
0x1F9	0x19	<a href="#">CROSS_VS[7:0]</a> I*	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]			
0x1FA	0x1A	<a href="#">CROSS_DE[7:0]</a> I*	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]			
0x1FB	0x00	<a href="#">PRBS_ERR[7:0]</a> I	VPRBS_ERR[7:0]						

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x1FC	0x80	<a href="#">VPRBS[7:0]*</a>	PATGEN _CLK_S RC	–	VPRBS_ FAIL	VPRBS_ CHK_EN	–	–	RSVD	VIDEO_ LOCK
0x1FD	0x1B	<a href="#">CROSS_27[7:0]</a>	RSVD	CROSS2 7_I	CROSS2 7_F	CROSS27[4:0]				
0x1FE	0x1C	<a href="#">CROSS_28[7:0]</a>	–	CROSS2 8_I	CROSS2 8_F	CROSS28[4:0]				
0x1FF	0x1D	<a href="#">CROSS_29[7:0]</a>	–	CROSS2 9_I	CROSS2 9_F	CROSS29[4:0]				
VRX Z										
0x200	0x00	<a href="#">CROSS_0[7:0]</a> <a href="#">I*</a>	–	CROSS0 _I	CROSS0 _F	CROSS0[4:0]				
0x201	0x01	<a href="#">CROSS_1[7:0]</a> <a href="#">I*</a>	–	CROSS1 _I	CROSS1 _F	CROSS1[4:0]				
0x202	0x02	<a href="#">CROSS_2[7:0]</a> <a href="#">I*</a>	–	CROSS2 _I	CROSS2 _F	CROSS2[4:0]				
0x203	0x03	<a href="#">CROSS_3[7:0]</a> <a href="#">I*</a>	–	CROSS3 _I	CROSS3 _F	CROSS3[4:0]				
0x204	0x04	<a href="#">CROSS_4[7:0]</a> <a href="#">I*</a>	–	CROSS4 _I	CROSS4 _F	CROSS4[4:0]				
0x205	0x05	<a href="#">CROSS_5[7:0]</a> <a href="#">I*</a>	–	CROSS5 _I	CROSS5 _F	CROSS5[4:0]				
0x206	0x06	<a href="#">CROSS_6[7:0]</a> <a href="#">I*</a>	–	CROSS6 _I	CROSS6 _F	CROSS6[4:0]				
0x207	0x07	<a href="#">CROSS_7[7:0]</a> <a href="#">I*</a>	–	CROSS7 _I	CROSS7 _F	CROSS7[4:0]				
0x208	0x08	<a href="#">CROSS_8[7:0]</a> <a href="#">I*</a>	–	CROSS8 _I	CROSS8 _F	CROSS8[4:0]				
0x209	0x09	<a href="#">CROSS_9[7:0]</a> <a href="#">I*</a>	–	CROSS9 _I	CROSS9 _F	CROSS9[4:0]				
0x20A	0x0A	<a href="#">CROSS_10[7:0]</a> <a href="#">I*</a>	–	CROSS1 0_I	CROSS1 0_F	CROSS10[4:0]				
0x20B	0x0B	<a href="#">CROSS_11[7:0]</a> <a href="#">I*</a>	–	CROSS1 1_I	CROSS1 1_F	CROSS11[4:0]				
0x20C	0x0C	<a href="#">CROSS_12[7:0]</a> <a href="#">I*</a>	–	CROSS1 2_I	CROSS1 2_F	CROSS12[4:0]				
0x20D	0x0D	<a href="#">CROSS_13[7:0]</a> <a href="#">I*</a>	–	CROSS1 3_I	CROSS1 3_F	CROSS13[4:0]				
0x20E	0x0E	<a href="#">CROSS_14[7:0]</a> <a href="#">I*</a>	–	CROSS1 4_I	CROSS1 4_F	CROSS14[4:0]				
0x20F	0x0F	<a href="#">CROSS_15[7:0]</a> <a href="#">I*</a>	–	CROSS1 5_I	CROSS1 5_F	CROSS15[4:0]				
0x210	0x10	<a href="#">CROSS_16[7:0]</a> <a href="#">I*</a>	–	CROSS1 6_I	CROSS1 6_F	CROSS16[4:0]				
0x211	0x11	<a href="#">CROSS_17[7:0]</a> <a href="#">I*</a>	–	CROSS1 7_I	CROSS1 7_F	CROSS17[4:0]				
0x212	0x12	<a href="#">CROSS_18[7:0]</a> <a href="#">I*</a>	–	CROSS1 8_I	CROSS1 8_F	CROSS18[4:0]				
0x213	0x13	<a href="#">CROSS_19[7:0]</a> <a href="#">I*</a>	–	CROSS1 9_I	CROSS1 9_F	CROSS19[4:0]				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x214	0x14	<a href="#">CROSS_20[7:0]*</a>	–	CROSS2_0_I	CROSS2_0_F	CROSS20[4:0]				
0x215	0x15	<a href="#">CROSS_21[7:0]*</a>	–	CROSS2_1_I	CROSS2_1_F	CROSS21[4:0]				
0x216	0x16	<a href="#">CROSS_22[7:0]*</a>	–	CROSS2_2_I	CROSS2_2_F	CROSS22[4:0]				
0x217	0x17	<a href="#">CROSS_23[7:0]*</a>	–	CROSS2_3_I	CROSS2_3_F	CROSS23[4:0]				
0x218	0x18	<a href="#">CROSS_HS[7:0]*</a>	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x219	0x19	<a href="#">CROSS_VS[7:0]*</a>	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x21A	0x1A	<a href="#">CROSS_DE[7:0]*</a>	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x21B	0x00	<a href="#">PRBS_ERR[7:0]</a>	VPRBS_ERR[7:0]							
0x21C	0x80	<a href="#">VPRBS[7:0]*</a>	PATGEN_CLK_SRC	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	RSVD	VIDEO_LOCK
0x21D	0x1B	<a href="#">CROSS_27[7:0]</a>	RSVD	CROSS2_7_I	CROSS2_7_F	CROSS27[4:0]				
0x21E	0x1C	<a href="#">CROSS_28[7:0]</a>	–	CROSS2_8_I	CROSS2_8_F	CROSS28[4:0]				
0x21F	0x1D	<a href="#">CROSS_29[7:0]</a>	–	CROSS2_9_I	CROSS2_9_F	CROSS29[4:0]				
VRX_PATGEN_0										
0x240	0x03	<a href="#">PATGEN_0[7:0]</a>	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
0x241	0x00	<a href="#">PATGEN_1[7:0]</a>	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIGGER
0x242	0x00	<a href="#">VS_DLY_2[7:0]</a>	VS_DLY_2[7:0]							
0x243	0x00	<a href="#">VS_DLY_1[7:0]</a>	VS_DLY_1[7:0]							
0x244	0x00	<a href="#">VS_DLY_0[7:0]</a>	VS_DLY_0[7:0]							
0x245	0x00	<a href="#">VS_HIGH_2[7:0]</a>	VS_HIGH_2[7:0]							
0x246	0x00	<a href="#">VS_HIGH_1[7:0]</a>	VS_HIGH_1[7:0]							
0x247	0x00	<a href="#">VS_HIGH_0[7:0]</a>	VS_HIGH_0[7:0]							
0x248	0x00	<a href="#">VS_LOW_2[7:0]</a>	VS_LOW_2[7:0]							
0x249	0x00	<a href="#">VS_LOW_1[7:0]</a>	VS_LOW_1[7:0]							
0x24A	0x00	<a href="#">VS_LOW_0[7:0]</a>	VS_LOW_0[7:0]							
0x24B	0x00	<a href="#">V2H_2[7:0]</a>	V2H_2[7:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB						LSB
0x24C	0x00	<a href="#">V2H_1[7:0]</a>							V2H_1[7:0]
0x24D	0x00	<a href="#">V2H_0[7:0]</a>							V2H_0[7:0]
0x24E	0x00	<a href="#">HS_HIGH_1[7:0]</a>							HS_HIGH_1[7:0]
0x24F	0x00	<a href="#">HS_HIGH_0[7:0]</a>							HS_HIGH_0[7:0]
0x250	0x00	<a href="#">HS_LOW_1[7:0]</a>							HS_LOW_1[7:0]
0x251	0x00	<a href="#">HS_LOW_0[7:0]</a>							HS_LOW_0[7:0]
0x252	0x00	<a href="#">HS_CNT_1[7:0]</a>							HS_CNT_1[7:0]
0x253	0x00	<a href="#">HS_CNT_0[7:0]</a>							HS_CNT_0[7:0]
0x254	0x00	<a href="#">V2D_2[7:0]</a>							V2D_2[7:0]
0x255	0x00	<a href="#">V2D_1[7:0]</a>							V2D_1[7:0]
0x256	0x00	<a href="#">V2D_0[7:0]</a>							V2D_0[7:0]
0x257	0x00	<a href="#">DE_HIGH_1[7:0]</a>							DE_HIGH_1[7:0]
0x258	0x00	<a href="#">DE_HIGH_0[7:0]</a>							DE_HIGH_0[7:0]
0x259	0x00	<a href="#">DE_LOW_1[7:0]</a>							DE_LOW_1[7:0]
0x25A	0x00	<a href="#">DE_LOW_0[7:0]</a>							DE_LOW_0[7:0]
0x25B	0x00	<a href="#">DE_CNT_1[7:0]</a>							DE_CNT_1[7:0]
0x25C	0x00	<a href="#">DE_CNT_0[7:0]</a>							DE_CNT_0[7:0]
0x25D	0x00	<a href="#">GRAD_INCR[7:0]</a>							GRAD_INCR[7:0]
0x25E	0x00	<a href="#">CHKR_COLOR_A_L[7:0]</a>							CHKR_COLOR_A_L[7:0]
0x25F	0x00	<a href="#">CHKR_COLOR_A_M[7:0]</a>							CHKR_COLOR_A_M[7:0]
0x260	0x00	<a href="#">CHKR_COLOR_A_H[7:0]</a>							CHKR_COLOR_A_H[7:0]
0x261	0x00	<a href="#">CHKR_COLOR_B_L[7:0]</a>							CHKR_COLOR_B_L[7:0]
0x262	0x00	<a href="#">CHKR_COLOR_B_M[7:0]</a>							CHKR_COLOR_B_M[7:0]
0x263	0x00	<a href="#">CHKR_COLOR_B_H[7:0]</a>							CHKR_COLOR_B_H[7:0]
0x264	0x00	<a href="#">CHKR_RPT_A[7:0]</a>							CHKR_RPT_A[7:0]
0x265	0x00	<a href="#">CHKR_RPT_B[7:0]</a>							CHKR_RPT_B[7:0]
0x266	0x00	<a href="#">CHKR_ALT[7:0]</a>							CHKR_ALT[7:0]

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
GPIO0 0										
0x2B0	0x83	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2B1	0xA0	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2B2	0x40	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	GPIO_R ECVED	–	GPIO_RX_ID[4:0]				
GPIO1 1										
0x2B3	0x84	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2B4	0xA1	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2B5	0x41	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO2 2										
0x2B6	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2B7	0x22	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2B8	0x42	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO3 3										
0x2B9	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2BA	0x23	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2BB	0x43	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO4 4										
0x2BC	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2BD	0xA4	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2BE	0x44	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO5 5										
0x2BF	0x84	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2C0	0xA5	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2C1	0x45	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO6 6										
0x2C2	0x83	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2C3	0xA6	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				



## MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x2C4	0x46	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO7 7										
0x2C5	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2C6	0xA7	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2C7	0x47	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO8 8										
0x2C8	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2C9	0xA8	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2CA	0x48	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO9 9										
0x2CB	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2CC	0xA9	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2CD	0x49	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO10 10										
0x2CE	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2CF	0xAA	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2D0	0x4A	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO11 11										
0x2D1	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2D2	0xAB	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2D3	0x4B	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO12 12										
0x2D4	0x81	<a href="#">GPIO_A[7:0]*</a>	RES_CF G	RSVD	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x2D5	0xAC	<a href="#">GPIO_B[7:0]*</a>	PULL_UPDN_SEL[1 :0]		OUT_TY PE	GPIO_TX_ID[4:0]				
0x2D6	0x4C	<a href="#">GPIO_C[7:0]*</a>	OVR_RE S_CFG	RSVD	–	GPIO_RX_ID[4:0]				
CMU										
0x302	0x00	<a href="#">CMU2[7:0]</a>	RSVD	PFDDIV_RSHORT[2:0]			RSVD	RSVD[1:0]		RSVD

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
BACKTOP										
0x308	0x01	BACKTOP1[7:0]*	CSIPLLU_LOCK	CSIPLLZ_LOCK	CSIPLLY_LOCK	CSIPLLX_LOCK	LINE_SP_L2	-	RSVD	BACKTOP_EN
0x30B	0x00	BACKTOP4[7:0]*	VS_VC2_L[7:0]							
0x30C	0x00	BACKTOP5[7:0]*	VS_VC2_H[7:0]							
0x30D	0x00	BACKTOP6[7:0]*	VS_VC3_L[7:0]							
0x30E	0x00	BACKTOP7[7:0]*	VS_VC3_H[7:0]							
0x312	0x00	BACKTOP11[7:0]	-	cmd_ove_rflow3	cmd_ove_rflow2	-	-	LMO_Z	LMO_Y	-
0x313	0x02	BACKTOP12[7:0]*	-	-	-	-	-	RSVD	CSI_OUT_EN	RSVD
0x314	0x00	BACKTOP13[7:0]	soft_vc_y[3:0]				-	-	-	-
0x315	0x00	BACKTOP14[7:0]	-	-	-	-	soft_vc_z[3:0]			
0x316	0x00	BACKTOP15[7:0]	soft_dt_y_h[1:0]		-	-	-	-	-	-
0x317	0x00	BACKTOP16[7:0]	soft_dt_z_h[3:0]				soft_dt_y_l[3:0]			
0x318	0x00	BACKTOP17[7:0]	-	-	-	-	-	-	soft_dt_z_l[1:0]	
0x319	0x00	BACKTOP18[7:0]	soft_bpp_z_h[2:0]				soft_bpp_y[4:0]			
0x31A	0x00	BACKTOP19[7:0]	-	-	-	-	-	-	soft_bpp_z_l[1:0]	
0x31B	0x00	BACKTOP20[7:0]	phy0_csi_tx_dppll_fb_fraction_in_l[7:0]							
0x31C	0x00	BACKTOP21[7:0]	-	bpp8dblz	bpp8dbly	-	phy0_csi_tx_dppll_fb_fraction_in_h[3:0]			
0x31D	0x2F	BACKTOP22[7:0]	override_bpp_vc_dty	-	phy0_csi_tx_dppll_fb_fraction_predef_en	phy0_csi_tx_dppll_predef_freq[4:0]				
0x31E	0x00	BACKTOP23[7:0]	phy1_csi_tx_dppll_fb_fraction_in_l[7:0]							
0x31F	0x00	BACKTOP24[7:0]	-	bpp8dblz_mode	bpp8dbly_mode	-	phy1_csi_tx_dppll_fb_fraction_in_h[3:0]			
0x320	0x2F	BACKTOP25[7:0]	-	override_bpp_vc_dtz	phy1_csi_tx_dppll_fb_fraction_predef_en	phy1_csi_tx_dppll_predef_freq[4:0]				
0x321	0x00	BACKTOP26[7:0]	phy2_csi_tx_dppll_fb_fraction_in_l[7:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x322	0x00	<a href="#">BACKTOP27[7:0]</a>	yuv_8_10_mux_mode4	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x323	0x2F	<a href="#">BACKTOP28[7:0]</a>	–	–	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]				
0x324	0x00	<a href="#">BACKTOP29[7:0]</a>	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x325	0x00	<a href="#">BACKTOP30[7:0]</a>	BACKTOP_W_FRAME	–	–	–	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x326	0x2F	<a href="#">BACKTOP31[7:0]</a>	–	–	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]				
0x327	0x00	<a href="#">BACKTOP32[7:0]</a>	–	bpp10dbl_z_mode	bpp10dbl_y_mode	–	–	bpp10dbl_z	bpp10dbl_y	–
0x328	0x00	<a href="#">BACKTOP33[7:0]</a>	–	–	–	–	–	bpp12dbl_z	bpp12dbl_y	–
MIPI_PHY										
0x330	0x04	<a href="#">MIPI_PHY0[7:0]*</a>	force_csi_out_en	RSVD	RSVD	phy_1x4_b_22	phy_1x4_a_22	phy_2x4	RSVD	phy_4x2
0x331	0x00	<a href="#">MIPI_PHY1[7:0]*</a>	t_hs_przero[1:0]		t_hs_prep[1:0]		RSVD[1:0]		t_clk_przero[1:0]	
0x332	0xF4	<a href="#">MIPI_PHY2[7:0]*</a>	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
0x333	0x4E	<a href="#">MIPI_PHY3[7:0]*</a>	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
0x334	0xE4	<a href="#">MIPI_PHY4[7:0]*</a>	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
0x335	0x00	<a href="#">MIPI_PHY5[7:0]*</a>	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
0x336	0x00	<a href="#">MIPI_PHY6[7:0]*</a>	phy_cp1	phy_cp0	phy3_pol_map[2:0]			phy2_pol_map[2:0]		
0x339	0x00	<a href="#">MIPI_PHY9[7:0]</a>	phy_cp0_dst[1:0]		–	RSVD	RSVD	–	RSVD	phy_cp0_overflow
0x33A	0x02	<a href="#">MIPI_PHY10[7:0]</a>	phy_cp0_src[1:0]		RSVD[2:0]			–	RSVD	phy_cp0_underflow
0x33B	0x00	<a href="#">MIPI_PHY11[7:0]</a>	phy_cp1_dst[1:0]		RSVD[2:0]			–	RSVD	phy_cp1_overflow
0x33C	0x02	<a href="#">MIPI_PHY12[7:0]</a>	phy_cp1_src[1:0]		RSVD[2:0]			–	RSVD	phy_cp1_underflow
0x33D	0x00	<a href="#">MIPI_PHY13[7:0]</a>	–	–	t_t3_prebegin[5:0]					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x33E	0x11	<a href="#">MIPI_PHY14[7:0]</a>	–	t_t3_post[4:0]					t_t3_prep[1:0]	
0x33F	0x00	<a href="#">MIPI_PHY15[7:0]</a> *	–	–	–	–	RST_MIPITX_LOC[3:0]			
0x340	0x00	<a href="#">MIPI_PHY16[7:0]</a> *	–	–	TUN_DATA_CRC_ERR_OEN	TUN_EC_C_UNCORR_ERR_OEN	TUN_EC_C_CORR_ERR_OEN	–	–	VID_OVERFLOW_OEN
0x341	0x00	<a href="#">MIPI_PHY17[7:0]</a>	–	–	TUN_DATA_CRC_ERR	TUN_EC_C_UNCORR_ERR	TUN_EC_C_CORR_ERR	–	–	VID_OVERFLOW_FLAG
0x342	0x00	<a href="#">MIPI_PHY18[7:0]</a>	csi2_tx2_pkt_cnt[3:0]				csi2_tx1_pkt_cnt[3:0]			
0x343	0x00	<a href="#">MIPI_PHY19[7:0]</a>	csi2_dup2_pkt_cnt[3:0]				csi2_dup1_pkt_cnt[3:0]			
0x344	0x00	<a href="#">MIPI_PHY20[7:0]</a>	phy1_pkt_cnt[3:0]				phy0_pkt_cnt[3:0]			
0x345	0x00	<a href="#">MIPI_PHY21[7:0]</a>	phy3_pkt_cnt[3:0]				phy2_pkt_cnt[3:0]			
FSYNC										
0x3E0	0x0E	<a href="#">FSYNC_0[7:0]</a> *	EN_OFLOW_RST_FS	RSVD	FSYNC_OUT_PIN	EN_VSGEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
0x3E1	0x00	<a href="#">FSYNC_1[7:0]</a> *	RSVD[1:0]		RSVD[1:0]		FSYNC_PER_DIV[3:0]			
0x3E2	0x81	<a href="#">FSYNC_2[7:0]</a> *	MST_LINK_SEL[2:0]			K_VAL_SIGN	K_VAL[3:0]			
0x3E3	0x00	<a href="#">FSYNC_3[7:0]</a> *	P_VAL_L[7:0]							
0x3E4	0x00	<a href="#">FSYNC_4[7:0]</a> *	–	–	P_VAL_SIGN	P_VAL_H[4:0]				
0x3E5	0x00	<a href="#">FSYNC_5[7:0]</a> *	FSYNC_PERIOD_L[7:0]							
0x3E6	0x00	<a href="#">FSYNC_6[7:0]</a> *	FSYNC_PERIOD_M[7:0]							
0x3E7	0x00	<a href="#">FSYNC_7[7:0]</a> *	FSYNC_PERIOD_H[7:0]							
0x3E8	0x00	<a href="#">FSYNC_8[7:0]</a> 1	FRM_DIFF_ERR_THR_L[7:0]							
0x3E9	0x0F	<a href="#">FSYNC_9[7:0]</a> 1	–	–	–	FRM_DIFF_ERR_THR_H[4:0]				
0x3EA	0x00	<a href="#">FSYNC_10[7:0]</a> 1	OVLP_WINDOW_L[7:0]							
0x3EB	0x00	<a href="#">FSYNC_11[7:0]</a> 1	EN_FSIN_LAST	–	–	OVLP_WINDOW_H[4:0]				
0x3EF	0x96	<a href="#">FSYNC_15[7:0]</a> 1	FS_GPIO_TYPE	FS_USE_XTAL	–	AUTO_FSLINKS	–	FS_EN_Z	FS_EN_Y	–
0x3F0	0x00	<a href="#">FSYNC_16[7:0]</a> 1	FSYNC_ERR_CNT[7:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x3F1	0xF0	<a href="#">FSYNC_17[7:0]</a>	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
0x3F2	0x00	<a href="#">FSYNC_18[7:0]</a>	CALC_FRM_LEN_L[7:0]							
0x3F3	0x00	<a href="#">FSYNC_19[7:0]</a>	CALC_FRM_LEN_M[7:0]							
0x3F4	0x00	<a href="#">FSYNC_20[7:0]</a>	CALC_FRM_LEN_H[7:0]							
0x3F5	0x00	<a href="#">FSYNC_21[7:0]</a>	FRM_DIFF_L[7:0]							
0x3F6	0x00	<a href="#">FSYNC_22[7:0]</a>	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]					
0x3F7	0x00	<a href="#">FSYNC_23[7:0]</a> *	EN_SYNC_COM_P	EN_LINK_RESET	-	-	-	FSYNC_OVR_Z	FSYNC_OVR_Y	-
MIPI_TX 0										
0x40A	0xD0	<a href="#">MIPI_TX10[7:0]</a> *	CSI2_LANE_CNT[1:0]	CSI2_CPHY_EN	RSVD	-	-	-	-	-
MIPI_TX 1										
0x441	0x00	<a href="#">MIPI_TX1[7:0]</a> *	MODE[7:0]							
0x442	0x00	<a href="#">MIPI_TX2[7:0]</a>	STATUS[7:0]							
0x443	0x01	<a href="#">MIPI_TX3[7:0]</a>	DESKEW_INIT[7:0]							
0x444	0x01	<a href="#">MIPI_TX4[7:0]</a>	DESKEW_PER[7:0]							
0x44A	0xD0	<a href="#">MIPI_TX10[7:0]</a> *	CSI2_LANE_CNT[1:0]	CSI2_CPHY_EN	RSVD	CSI_VC_X_EN	RSVD[2:0]			
0x44B	0x00	<a href="#">MIPI_TX11[7:0]</a> *	MAP_EN_L[7:0]							
0x44C	0x00	<a href="#">MIPI_TX12[7:0]</a> *	MAP_EN_H[7:0]							
0x44D	0x00	<a href="#">MIPI_TX13[7:0]</a> *	MAP_SRC_0[7:0]							
0x44E	0x00	<a href="#">MIPI_TX14[7:0]</a> *	MAP_DST_0[7:0]							
0x44F	0x00	<a href="#">MIPI_TX15[7:0]</a> *	MAP_SRC_1[7:0]							
0x450	0x00	<a href="#">MIPI_TX16[7:0]</a> *	MAP_DST_1[7:0]							
0x451	0x00	<a href="#">MIPI_TX17[7:0]</a> *	MAP_SRC_2[7:0]							
0x452	0x00	<a href="#">MIPI_TX18[7:0]</a> *	MAP_DST_2[7:0]							
0x453	0x00	<a href="#">MIPI_TX19[7:0]</a> *	MAP_SRC_3[7:0]							
0x454	0x00	<a href="#">MIPI_TX20[7:0]</a> *	MAP_DST_3[7:0]							
0x455	0x00	<a href="#">MIPI_TX21[7:0]</a>	MAP_SRC_4[7:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB						LSB
0x456	0x00	<a href="#">MIPI_TX22[7:0]</a>	MAP_DST_4[7:0]						
0x457	0x00	<a href="#">MIPI_TX23[7:0]</a>	MAP_SRC_5[7:0]						
0x458	0x00	<a href="#">MIPI_TX24[7:0]</a>	MAP_DST_5[7:0]						
0x459	0x00	<a href="#">MIPI_TX25[7:0]</a>	MAP_SRC_6[7:0]						
0x45A	0x00	<a href="#">MIPI_TX26[7:0]</a>	MAP_DST_6[7:0]						
0x45B	0x00	<a href="#">MIPI_TX27[7:0]</a>	MAP_SRC_7[7:0]						
0x45C	0x00	<a href="#">MIPI_TX28[7:0]</a>	MAP_DST_7[7:0]						
0x45D	0x00	<a href="#">MIPI_TX29[7:0]</a>	MAP_SRC_8[7:0]						
0x45E	0x00	<a href="#">MIPI_TX30[7:0]</a>	MAP_DST_8[7:0]						
0x45F	0x00	<a href="#">MIPI_TX31[7:0]</a>	MAP_SRC_9[7:0]						
0x460	0x00	<a href="#">MIPI_TX32[7:0]</a>	MAP_DST_9[7:0]						
0x461	0x00	<a href="#">MIPI_TX33[7:0]</a>	MAP_SRC_10[7:0]						
0x462	0x00	<a href="#">MIPI_TX34[7:0]</a>	MAP_DST_10[7:0]						
0x463	0x00	<a href="#">MIPI_TX35[7:0]</a>	MAP_SRC_11[7:0]						
0x464	0x00	<a href="#">MIPI_TX36[7:0]</a>	MAP_DST_11[7:0]						
0x465	0x00	<a href="#">MIPI_TX37[7:0]</a>	MAP_SRC_12[7:0]						
0x466	0x00	<a href="#">MIPI_TX38[7:0]</a>	MAP_DST_12[7:0]						
0x467	0x00	<a href="#">MIPI_TX39[7:0]</a>	MAP_SRC_13[7:0]						
0x468	0x00	<a href="#">MIPI_TX40[7:0]</a>	MAP_DST_13[7:0]						
0x469	0x00	<a href="#">MIPI_TX41[7:0]</a>	MAP_SRC_14[7:0]						
0x46A	0x00	<a href="#">MIPI_TX42[7:0]</a>	MAP_DST_14[7:0]						
0x46B	0x00	<a href="#">MIPI_TX43[7:0]</a>	MAP_SRC_15[7:0]						
0x46C	0x00	<a href="#">MIPI_TX44[7:0]</a>	MAP_DST_15[7:0]						
0x46D	0x00	<a href="#">MIPI_TX45[7:0]</a> <sup>*</sup>	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]			
0x46E	0x00	<a href="#">MIPI_TX46[7:0]</a> <sup>*</sup>	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB						LSB
0x46F	0x00	<a href="#">MIPI_TX47[7:0]*</a>	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]
0x470	0x00	<a href="#">MIPI_TX48[7:0]*</a>	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]
0x472	0x00	<a href="#">MIPI_TX50[7:0]</a>	SKEW_PER_SEL[7:0]						
0x473	0x00	<a href="#">MIPI_TX51[7:0]*</a>	TUN_WAIT_VS_START[2:0]			ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8 ALT_MEM_MAP12
0x474	0x08	<a href="#">MIPI_TX52[7:0]*</a>	TUN_NO_CORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1:0]		DESKEW_TUN_SRC	TUN_DEST TUN_EN
0x475	0x00	<a href="#">MIPI_TX53[7:0]*</a>	DESKEW_TUN_OFFSET[7:0]						
0x476	0x00	<a href="#">MIPI_TX54[7:0]*</a>	TUN_PKT_START_ADDR[7:0]						
0x477	0x00	<a href="#">MIPI_TX55[7:0]</a>	-	-	-	-	-	-	TUN_NO_CORR_LENGTH
MIPI_TX 2									
0x481	0x00	<a href="#">MIPI_TX1[7:0]*</a>	MODE[7:0]						
0x482	0x00	<a href="#">MIPI_TX2[7:0]</a>	STATUS[7:0]						
0x483	0x01	<a href="#">MIPI_TX3[7:0]</a>	DESKEW_INIT[7:0]						
0x484	0x01	<a href="#">MIPI_TX4[7:0]</a>	DESKEW_PER[7:0]						
0x48A	0xD0	<a href="#">MIPI_TX10[7:0]*</a>	CSI2_LANE_CNT[1:0]	CSI2_CPHY_EN	RSVD	CSI_VC_X_EN	RSVD[2:0]		
0x48B	0x00	<a href="#">MIPI_TX11[7:0]*</a>	MAP_EN_L[7:0]						
0x48C	0x00	<a href="#">MIPI_TX12[7:0]*</a>	MAP_EN_H[7:0]						
0x48D	0x00	<a href="#">MIPI_TX13[7:0]*</a>	MAP_SRC_0[7:0]						
0x48E	0x00	<a href="#">MIPI_TX14[7:0]*</a>	MAP_DST_0[7:0]						
0x48F	0x00	<a href="#">MIPI_TX15[7:0]*</a>	MAP_SRC_1[7:0]						
0x490	0x00	<a href="#">MIPI_TX16[7:0]*</a>	MAP_DST_1[7:0]						
0x491	0x00	<a href="#">MIPI_TX17[7:0]*</a>	MAP_SRC_2[7:0]						
0x492	0x00	<a href="#">MIPI_TX18[7:0]*</a>	MAP_DST_2[7:0]						
0x493	0x00	<a href="#">MIPI_TX19[7:0]*</a>	MAP_SRC_3[7:0]						
0x494	0x00	<a href="#">MIPI_TX20[7:0]*</a>	MAP_DST_3[7:0]						
0x495	0x00	<a href="#">MIPI_TX21[7:0]</a>	MAP_SRC_4[7:0]						



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB						LSB
0x496	0x00	<a href="#">MIPI_TX22[7:0]</a>	MAP_DST_4[7:0]						
0x497	0x00	<a href="#">MIPI_TX23[7:0]</a>	MAP_SRC_5[7:0]						
0x498	0x00	<a href="#">MIPI_TX24[7:0]</a>	MAP_DST_5[7:0]						
0x499	0x00	<a href="#">MIPI_TX25[7:0]</a>	MAP_SRC_6[7:0]						
0x49A	0x00	<a href="#">MIPI_TX26[7:0]</a>	MAP_DST_6[7:0]						
0x49B	0x00	<a href="#">MIPI_TX27[7:0]</a>	MAP_SRC_7[7:0]						
0x49C	0x00	<a href="#">MIPI_TX28[7:0]</a>	MAP_DST_7[7:0]						
0x49D	0x00	<a href="#">MIPI_TX29[7:0]</a>	MAP_SRC_8[7:0]						
0x49E	0x00	<a href="#">MIPI_TX30[7:0]</a>	MAP_DST_8[7:0]						
0x49F	0x00	<a href="#">MIPI_TX31[7:0]</a>	MAP_SRC_9[7:0]						
0x4A0	0x00	<a href="#">MIPI_TX32[7:0]</a>	MAP_DST_9[7:0]						
0x4A1	0x00	<a href="#">MIPI_TX33[7:0]</a>	MAP_SRC_10[7:0]						
0x4A2	0x00	<a href="#">MIPI_TX34[7:0]</a>	MAP_DST_10[7:0]						
0x4A3	0x00	<a href="#">MIPI_TX35[7:0]</a>	MAP_SRC_11[7:0]						
0x4A4	0x00	<a href="#">MIPI_TX36[7:0]</a>	MAP_DST_11[7:0]						
0x4A5	0x00	<a href="#">MIPI_TX37[7:0]</a>	MAP_SRC_12[7:0]						
0x4A6	0x00	<a href="#">MIPI_TX38[7:0]</a>	MAP_DST_12[7:0]						
0x4A7	0x00	<a href="#">MIPI_TX39[7:0]</a>	MAP_SRC_13[7:0]						
0x4A8	0x00	<a href="#">MIPI_TX40[7:0]</a>	MAP_DST_13[7:0]						
0x4A9	0x00	<a href="#">MIPI_TX41[7:0]</a>	MAP_SRC_14[7:0]						
0x4AA	0x00	<a href="#">MIPI_TX42[7:0]</a>	MAP_DST_14[7:0]						
0x4AB	0x00	<a href="#">MIPI_TX43[7:0]</a>	MAP_SRC_15[7:0]						
0x4AC	0x00	<a href="#">MIPI_TX44[7:0]</a>	MAP_DST_15[7:0]						
0x4AD	0x00	<a href="#">MIPI_TX45[7:0]</a>	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]			
0x4AE	0x00	<a href="#">MIPI_TX46[7:0]</a>	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB						LSB
0x4AF	0x00	<a href="#">MIPI_TX47[7:0]</a> *	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]
0x4B0	0x00	<a href="#">MIPI_TX48[7:0]</a> *	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]
0x4B2	0x00	<a href="#">MIPI_TX50[7:0]</a>	SKEW_PER_SEL[7:0]						
0x4B3	0x00	<a href="#">MIPI_TX51[7:0]</a>	TUN_WAIT_VS_START[2:0]		ALT2_M EM_MA P8	MODE_ DT	ALT_ME M_MAP1 0	ALT_ME M_MAP8	ALT_ME M_MAP1 2
0x4B4	0x0E	<a href="#">MIPI_TX52[7:0]</a> *	TUN_NO _CORR	DESKEW_TUN[1:0]	TUN_SER_LANE_N UM[1:0]	DESKE W_TUN_ SRC	TUN_DE ST		TUN_EN
0x4B5	0x00	<a href="#">MIPI_TX53[7:0]</a> *	DESKEW_TUN_OFFSET[7:0]						
0x4B6	0x00	<a href="#">MIPI_TX54[7:0]</a> *	TUN_PKT_START_ADDR[7:0]						
0x4B7	0x00	<a href="#">MIPI_TX55[7:0]</a>	-	-	-	-	-	-	TUN_NO _CORR LENGTH
<b>MIPI_TX 3</b>									
0x4CA	0xD0	<a href="#">MIPI_TX10[7:0]</a> *	CSI2_LANE_CNT[1:0]	CSI2_CP HY_EN	RSVD	-	-	-	-
<b>MIPI_TX_EXT 1</b>									
0x510	0x00	<a href="#">MIPI_TX_EXT 0[7:0]</a>	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-	-
0x511	0x00	<a href="#">MIPI_TX_EXT 1[7:0]</a>	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-	-
0x512	0x00	<a href="#">MIPI_TX_EXT 2[7:0]</a>	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-	-
0x513	0x00	<a href="#">MIPI_TX_EXT 3[7:0]</a>	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-	-
0x514	0x00	<a href="#">MIPI_TX_EXT 4[7:0]</a>	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-	-
0x515	0x00	<a href="#">MIPI_TX_EXT 5[7:0]</a>	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		-	-	-
0x516	0x00	<a href="#">MIPI_TX_EXT 6[7:0]</a>	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		-	-	-
0x517	0x00	<a href="#">MIPI_TX_EXT 7[7:0]</a>	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		-	-	-
0x518	0x00	<a href="#">MIPI_TX_EXT 8[7:0]</a>	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		-	-	-
0x519	0x00	<a href="#">MIPI_TX_EXT 9[7:0]</a>	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		-	-	-
0x51A	0x00	<a href="#">MIPI_TX_EXT 10[7:0]</a>	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		-	-	-
0x51B	0x00	<a href="#">MIPI_TX_EXT 11[7:0]</a>	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		-	-	-
0x51C	0x00	<a href="#">MIPI_TX_EXT 12[7:0]</a>	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		-	-	-

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB					LSB
0x51D	0x00	<a href="#">MIPI_TX_EXT 13[7:0]</a>	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		–	–
0x51E	0x00	<a href="#">MIPI_TX_EXT 14[7:0]</a>	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		–	–
0x51F	0x00	<a href="#">MIPI_TX_EXT 15[7:0]</a>	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		–	–
MIPI_TX_EXT 2								
0x520	0x00	<a href="#">MIPI_TX_EXT 0[7:0]</a>	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		–	–
0x521	0x00	<a href="#">MIPI_TX_EXT 1[7:0]</a>	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		–	–
0x522	0x00	<a href="#">MIPI_TX_EXT 2[7:0]</a>	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		–	–
0x523	0x00	<a href="#">MIPI_TX_EXT 3[7:0]</a>	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		–	–
0x524	0x00	<a href="#">MIPI_TX_EXT 4[7:0]</a>	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		–	–
0x525	0x00	<a href="#">MIPI_TX_EXT 5[7:0]</a>	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		–	–
0x526	0x00	<a href="#">MIPI_TX_EXT 6[7:0]</a>	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		–	–
0x527	0x00	<a href="#">MIPI_TX_EXT 7[7:0]</a>	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		–	–
0x528	0x00	<a href="#">MIPI_TX_EXT 8[7:0]</a>	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		–	–
0x529	0x00	<a href="#">MIPI_TX_EXT 9[7:0]</a>	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		–	–
0x52A	0x00	<a href="#">MIPI_TX_EXT 10[7:0]</a>	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		–	–
0x52B	0x00	<a href="#">MIPI_TX_EXT 11[7:0]</a>	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		–	–
0x52C	0x00	<a href="#">MIPI_TX_EXT 12[7:0]</a>	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		–	–
0x52D	0x00	<a href="#">MIPI_TX_EXT 13[7:0]</a>	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		–	–
0x52E	0x00	<a href="#">MIPI_TX_EXT 14[7:0]</a>	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		–	–
0x52F	0x00	<a href="#">MIPI_TX_EXT 15[7:0]</a>	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		–	–
MISC								
0x540	0x00	<a href="#">CFG_0[7:0]</a>	VS_OUT1[2:0]		RSVD[4:0]			
0x541	0x00	<a href="#">CFG_1[7:0]</a>	VS_OUT2[2:0]		RSVD[4:0]			
0x542	0x00	<a href="#">CFG_2[7:0]</a>	HS_OUT1[2:0]		RSVD[4:0]			
0x548	0x96	<a href="#">UART_PT_0[7:0]*</a>	BITLEN_PT_1_L[7:0]					
0x549	0x00	<a href="#">UART_PT_1[7:0]*</a>	–	–	BITLEN_PT_1_H[5:0]			
0x54A	0x96	<a href="#">UART_PT_2[7:0]*</a>	BITLEN_PT_2_L[7:0]					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x54B	0x00	<a href="#">UART_PT_3[7:0]*</a>	–	–	BITLEN_PT_2_H[5:0]					
0x550	0x00	<a href="#">I2C_PT_4[7:0]</a>	SRC_A_1[6:0]							–
0x551	0x00	<a href="#">I2C_PT_5[7:0]</a>	DST_A_1[6:0]							–
0x552	0x00	<a href="#">I2C_PT_6[7:0]</a>	SRC_B_1[6:0]							–
0x553	0x00	<a href="#">I2C_PT_7[7:0]</a>	DST_B_1[6:0]							–
0x554	0x00	<a href="#">I2C_PT_8[7:0]</a>	SRC_A_2[6:0]							–
0x555	0x00	<a href="#">I2C_PT_9[7:0]</a>	DST_A_2[6:0]							–
0x556	0x00	<a href="#">I2C_PT_10[7:0]</a>	SRC_B_2[6:0]							–
0x557	0x00	<a href="#">I2C_PT_11[7:0]</a>	DST_B_2[6:0]							–
0x55C	0x00	<a href="#">CNT4[7:0]</a>	VID_PXL_CRC_ERR0[7:0]							
0x55D	0x00	<a href="#">CNT5[7:0]</a>	VID_PXL_CRC_ERR1[7:0]							
0x55E	0x00	<a href="#">CNT6[7:0]</a>	VID_PXL_CRC_ERR2[7:0]							
0x55F	0x00	<a href="#">CNT7[7:0]</a>	VID_PXL_CRC_ERR3[7:0]							
0x568	0x06	<a href="#">PORT_TUN_ONLY[7:0]*</a>	–	–	–	–	TUN_ON LY_2	TUN_ON LY_1	TUN_ON LY_CC	
0x569	0xAA	<a href="#">UNLOCK_KEY[7:0]*</a>	UNLOCK_KEY[7:0]							
0x570	0xFE	<a href="#">PIO_SLEW_0[7:0]*</a>	PIO03_SLEW[1:0]		PIO02_SLEW[1:0]		PIO01_SLEW[1:0]		PIO00_SLEW[1:0]	
0x571	0x83	<a href="#">PIO_SLEW_1[7:0]*</a>	PIO07_SLEW[1:0]		–	–	–	–	PIO04_SLEW[1:0]	
0x572	0x02	<a href="#">PIO_SLEW_2[7:0]*</a>	–	–	–	–	–	–	PIO08_SLEW[1:0]	
0x575	0x00	<a href="#">HS_VS_ACT_Y[7:0]</a>	–	DE_DET_Y	VS_DET_Y	HS_DET_Y	–	–	VS_POL_Y	HS_POL_Y
0x576	0x00	<a href="#">HS_VS_ACT_Z[7:0]</a>	–	DE_DET_Z	VS_DET_Z	HS_DET_Z	–	–	VS_POL_Z	HS_POL_Z
0x577	0x60	<a href="#">DP_ORSTB_CTL[7:0]*</a>	–	DP_RST_MIPI3_CHK	DP_RST_STABL_E_CHK	DP_RST_MIPI2_CHK	DP_RST_MIPI_C_HK	DP_RST_VP_CH_KB	RSVD	RSVD
0x578	0x15	<a href="#">PM_OV_STA_T2[7:0]*</a>	VTERM_OV_OEN	VREG_OV_OEN	VTERM_OV_LEVEL[1:0]		RSVD[1:0]		VREG_OV_LEVEL[1:0]	
0x579	0x00	<a href="#">PM_OV_STA_T3[7:0]</a>	VTERM_OV_FLAG	VREG_OV_FLAG	RSVD	–	RSVD	RSVD	RSVD	RSVD
<b>CC_EXT</b>										
0x808	0x02	<a href="#">UART_0[7:0]*</a>	–	–	REM_MS_EN_1	LOC_MS_EN_1	–	BYPASS_TO_1[1:0]		BYPASS_EN_1
0x809	0x02	<a href="#">UART_1[7:0]*</a>	–	–	REM_MS_EN_2	LOC_MS_EN_2	–	BYPASS_TO_2[1:0]		BYPASS_EN_2

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB	
0x80E	0x06	<a href="#">I2C_PT_0[7:0]</a>	RSVD	I2C_RE GSLV_0 _TIMED _OUT	-	-	RSVD	I2C_INTREG_SLV_TO[2:0]			
0x80F	0x36	<a href="#">I2C_PT_1[7:0]</a>	I2C_RE GSLV_2 _TIMED _OUT	I2C_RE GSLV_1 _TIMED _OUT	I2C_INTREG_SLV_2_TO[2:0]			I2C_INTREG_SLV_1_TO[2:0]			
GMSL1_COMMON											
0xF00	0x03	<a href="#">GMSL1_EN[7:0]*</a>	-	-	-	-	-	-	LINK_EN _B	LINK_EN _A	
SPI_CC_WR											
0x1300	0x00	<a href="#">SPI_CC_WR[7:0]</a>	-	-	-	-	-	-	-	-	
SPI_CC_RD											
0x1380	0x00	<a href="#">SPI_CC_RD[7:0]</a>	-	-	-	-	-	-	-	-	
RLMS A											
0x1403	0x0A	<a href="#">RLMS3[7:0]</a>	AdaptEn	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]		
0x1404	0x4B	<a href="#">RLMS4[7:0]</a>	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]	EOM_P E R_MOD	EOM_E N		
0x1405	0x10	<a href="#">RLMS5[7:0]</a>	EOM_M AN_TRG _REQ	EOM_MIN_THR[6:0]							
0x1406	0x80	<a href="#">RLMS6[7:0]</a>	EOM_PV MODE	EOM_RST_THR[6:0]							
0x1407	0x00	<a href="#">RLMS7[7:0]</a>	EOM_D ONE	EOM[6:0]							
0x140A	0x08	<a href="#">RLMSA[7:0]</a>	RSVD	RSVD	RSVD[1:0]		DFEAdpDly[3:0]				
0x1418	0x0F	<a href="#">RLMS18[7:0]</a>	RSVD	RSVD[2:0]			RSVD	VgaHiGa in	RSVD[1:0]		
0x1421	0x04	<a href="#">RLMS21[7:0]</a>	RSVD	-	BSTMuH[5:0]						
0x1423	0x45	<a href="#">RLMS23[7:0]</a>	-	RSVD	BSTInit[5:0]						
0x1431	0x18	<a href="#">RLMS31[7:0]</a>	RSVD	-	OSNMuH[5:0]						
0x1445	0xC8	<a href="#">RLMS45[7:0]</a>	RSVD	CRUSS CSeISR En	RSVD[1:0]		RSVD	RSVD[2:0]			
0x1446	0xB3	<a href="#">RLMS46[7:0]</a>	RSVD[3:0]				RSVD	CRULpCtrl[2:0]			
0x1447	0x03	<a href="#">RLMS47[7:0]</a>	RSVD	RSVD	RSVD	RSVD	RSVD	CRUSSCSeI[1:0]	RSVD		
0x1464	0x90	<a href="#">RLMS64[7:0]*</a>	RSVD[3:0]				RSVD	RSVD	TxSSCMode[1:0]		
0x1470	0x01	<a href="#">RLMS70[7:0]*</a>	RSVD	TxSSCFrqCtrl[6:0]							
0x1471	0x02	<a href="#">RLMS71[7:0]*</a>	RSVD	TxSSCCenSprSt[5:0]						TxSSCE n	
0x1472	0xCF	<a href="#">RLMS72[7:0]*</a>	TxSSCPreScIL[7:0]								
0x1473	0x00	<a href="#">RLMS73[7:0]*</a>	RSVD[4:0]					TxSSCPreScIH[2:0]			
0x1474	0x00	<a href="#">RLMS74[7:0]*</a>	TxSSCPhL[7:0]								
0x1475	0x00	<a href="#">RLMS75[7:0]*</a>	RSVD	TxSSCPhH[6:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB	
0x148C	0x00	<a href="#">RLMS8C[7:0]</a>	RSVD	cap_pre_out_rlms[6:0]							
0x1495	0x69	<a href="#">RLMS95[7:0]</a>	TxAmpL ManEn	RSVD	TxAmplMan[5:0]						
0x1498	0x40	<a href="#">RLMS98[7:0]</a>	Cal_cap _pre_out _en	RSVD	RSVD[2:0]			RSVD[2:0]			
0x14A4	0xBD	<a href="#">RLMSA4[7:0]</a>	AEQ_PER_MULT[1: 0]	AEQ_PER[5:0]							
0x14A5	0x50	<a href="#">RLMSA5[7:0]</a>	RSVD[1:0]		PHYC_WBLOCK_D LY[1:0]		RSVD[1:0]		RSVD[1:0]		
0x14A7	0x01	<a href="#">RLMSA7[7:0]</a>	MAN_CT RL_EN	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	
0x14A8	0x00	<a href="#">RLMSA8[7:0]</a>	FW_PHY _CTRL	FW_PHY _PU_TX	FW_PHY _RSTB	RSVD	RSVD	RSVD	RSVD	RSVD	
0x14A9	0x00	<a href="#">RLMSA9[7:0]</a>	FW_REP CAL_RS TB	RSVD	FW_TXD _SQUEL CH	FW_TXD _EN	FW_RX D_EN	RSVD	RSVD	RSVD	
0x14AC	0xA0	<a href="#">RLMSAC[7:0]</a>	RSVD	ErrChPhSecFR3G[6:0]							
0x14AD	0x60	<a href="#">RLMSAD[7:0]</a>	RSVD	ErrChPhPriFR3G[6:0]							
RLMS B											
0x1503	0x0A	<a href="#">RLMS3[7:0]</a>	AdaptEn	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]		
0x1504	0x4B	<a href="#">RLMS4[7:0]</a>	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0 ]		EOM_PE R_MOD E	EOM_E N	
0x1505	0x10	<a href="#">RLMS5[7:0]</a>	EOM_M AN_TRG _REQ	EOM_MIN_THR[6:0]							
0x1506	0x80	<a href="#">RLMS6[7:0]</a>	EOM_PV _MODE	EOM_RST_THR[6:0]							
0x1507	0x00	<a href="#">RLMS7[7:0]</a>	EOM_D ONE	EOM[6:0]							
0x150A	0x08	<a href="#">RLMSA[7:0]</a>	RSVD	RSVD	RSVD[1:0]		DFEAdpDly[3:0]				
0x1518	0x0F	<a href="#">RLMS18[7:0]</a>	RSVD	RSVD[2:0]			RSVD	VgaHiGa in	RSVD[1:0]		
0x1521	0x04	<a href="#">RLMS21[7:0]</a>	RSVD	–	BSTMuH[5:0]						
0x1523	0x45	<a href="#">RLMS23[7:0]</a>	–	RSVD	BSTInit[5:0]						
0x1531	0x18	<a href="#">RLMS31[7:0]</a>	RSVD	–	OSNMuH[5:0]						
0x1545	0xC8	<a href="#">RLMS45[7:0]</a>	RSVD	CRUSS CSeISR En	RSVD[1:0]		RSVD	RSVD[2:0]			
0x1546	0xB3	<a href="#">RLMS46[7:0]</a>	RSVD[3:0]				RSVD	CRULpCtrl[2:0]			
0x1547	0x03	<a href="#">RLMS47[7:0]</a>	RSVD	RSVD	RSVD	RSVD	RSVD	CRUSSCSeI[1:0]		RSVD	
0x1564	0x90	<a href="#">RLMS64[7:0]*</a>	RSVD[3:0]				RSVD	RSVD	TxSSCMode[1:0]		
0x1570	0x01	<a href="#">RLMS70[7:0]*</a>	RSVD	TxSSCFrqCtrl[6:0]							
0x1571	0x02	<a href="#">RLMS71[7:0]*</a>	RSVD	TxSSCCenSprSt[5:0]							TxSSCE n
0x1572	0xCF	<a href="#">RLMS72[7:0]*</a>	TxSSCPreScL[7:0]								
0x1573	0x00	<a href="#">RLMS73[7:0]*</a>	RSVD[4:0]					TxSSCPreScH[2:0]			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x1574	0x00	<a href="#">RLMS74[7:0]*</a>	TxSSCPHL[7:0]							
0x1575	0x00	<a href="#">RLMS75[7:0]*</a>	RSVD	TxSSCPHH[6:0]						
0x158C	0x00	<a href="#">RLMS8C[7:0]</a>	RSVD	cap_pre_out_rlms[6:0]						
0x1595	0x69	<a href="#">RLMS95[7:0]</a>	TxAmpI ManEn	RSVD	TxAmpIMan[5:0]					
0x1598	0x40	<a href="#">RLMS98[7:0]</a>	Cal_cap _pre_out _en	RSVD	RSVD[2:0]			RSVD[2:0]		
0x15A4	0xBD	<a href="#">RLMSA4[7:0]</a>	AEQ_PER_MULT[1: 0]	AEQ_PER[5:0]						
0x15A5	0x50	<a href="#">RLMSA5[7:0]</a>	RSVD[1:0]		PHYC_WBLOCK_D LY[1:0]		RSVD[1:0]		RSVD[1:0]	
0x15A7	0x01	<a href="#">RLMSA7[7:0]</a>	MAN_CT RL_EN	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0x15A8	0x00	<a href="#">RLMSA8[7:0]</a>	FW_PHY _CTRL	FW_PHY _PU_TX	FW_PHY _RSTB	RSVD	RSVD	RSVD	RSVD	RSVD
0x15A9	0x00	<a href="#">RLMSA9[7:0]</a>	FW_REP CAL_RS TB	RSVD	FW_TXD _SQUEL CH	FW_TXD _EN	FW_RX D_EN	RSVD	RSVD	RSVD
0x15AC	0xA0	<a href="#">RLMSAC[7:0]</a>	RSVD	ErrChPhSecFR3G[6:0]						
0x15AD	0x60	<a href="#">RLMSAD[7:0]</a>	RSVD	ErrChPhPriFR3G[6:0]						
DPLL CSI1										
0x1C00	0xF5	<a href="#">DPLL_0[7:0]*</a>	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_s oft_rst_n
0x1C03	0x82	<a href="#">DPLL_3[7:0]*</a>	config_s el_clock_ out_use_ external	config_di sable_di v_out_ex p	config_u se_intern al_pll_m ode_valu es	config_u se_intern al_divide r_values	RSVD	RSVD[2:0]		
0x1C07	0x04	<a href="#">DPLL_7[7:0]</a>	config_di v_fb_L	config_div_in[4:0]					RSVD[1:0]	
0x1C08	0x14	<a href="#">DPLL_8[7:0]</a>	config_div_fb_H[7:0]							
0x1C0A	0x81	<a href="#">DPLL_10[7:0]</a>	RSVD	config_div_out_exp[2:0]			RSVD[3:0]			
DPLL CSI2										
0x1D00	0xF5	<a href="#">DPLL_0[7:0]*</a>	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_s oft_rst_n
0x1D03	0x82	<a href="#">DPLL_3[7:0]*</a>	config_s el_clock_ out_use_ external	config_di sable_di v_out_ex p	config_u se_intern al_pll_m ode_valu es	config_u se_intern al_divide r_values	RSVD	RSVD[2:0]		
0x1D07	0x04	<a href="#">DPLL_7[7:0]</a>	config_di v_fb_L	config_div_in[4:0]					RSVD[1:0]	
0x1D08	0x14	<a href="#">DPLL_8[7:0]</a>	config_div_fb_H[7:0]							
0x1D0A	0x81	<a href="#">DPLL_10[7:0]</a>	RSVD	config_div_out_exp[2:0]			RSVD[3:0]			
DPLL CSI3										
0x1E00	0xF5	<a href="#">DPLL_0[7:0]*</a>	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_s oft_rst_n



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x1E03	0x82	<a href="#">DPLL_3[7:0]*</a>	config_sel_clock_out_use_external	config_divisible_div_out_exp	config_use_internal_pll_mode_values	config_use_internal_divider_values	RSVD	RSVD[2:0]		
0x1E07	0x04	<a href="#">DPLL_7[7:0]</a>	config_div_fb_L	config_div_in[4:0]				RSVD[1:0]		
0x1E08	0x14	<a href="#">DPLL_8[7:0]</a>	config_div_fb_H[7:0]							
0x1E0A	0x81	<a href="#">DPLL_10[7:0]</a>	RSVD	config_div_out_exp[2:0]			RSVD[3:0]			
DPLL CSI4										
0x1F00	0xF5	<a href="#">DPLL_0[7:0]*</a>	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
0x1F03	0x82	<a href="#">DPLL_3[7:0]*</a>	config_sel_clock_out_use_external	config_divisible_div_out_exp	config_use_internal_pll_mode_values	config_use_internal_divider_values	RSVD	RSVD[2:0]		
0x1F07	0x04	<a href="#">DPLL_7[7:0]</a>	config_div_fb_L	config_div_in[4:0]				RSVD[1:0]		
0x1F08	0x14	<a href="#">DPLL_8[7:0]</a>	config_div_fb_H[7:0]							
0x1F0A	0x81	<a href="#">DPLL_10[7:0]</a>	RSVD	config_div_out_exp[2:0]			RSVD[3:0]			
FEC										
0x2000	0x00	<a href="#">CLEAR_STATS[7:0]</a>	-	-	-	-	CLEAR_BITS_CORRECTED	CLEAR_BLOCKS_UNCORRECTABLE	CLEAR_BLOCKS_PROCESSED	CLEAR_ALL_STATS
0x2001	0x00	<a href="#">STATS_CONTROL[7:0]</a>	-	-	-	-	-	-	-	STATS_ENABLE
0x2008	0x00	<a href="#">CORRECTED_THRESHOLD_0[7:0]</a>	BIT_ERRS_CORRECTED_THRESHOLD_0[7:0]							
0x2009	0x00	<a href="#">CORRECTED_THRESHOLD_1[7:0]</a>	BIT_ERRS_CORRECTED_THRESHOLD_1[7:0]							
0x200A	0x00	<a href="#">CORRECTED_THRESHOLD_2[7:0]</a>	BIT_ERRS_CORRECTED_THRESHOLD_2[7:0]							
0x200B	0x00	<a href="#">CORRECTED_THRESHOLD_3[7:0]</a>	BIT_ERRS_CORRECTED_THRESHOLD_3[7:0]							
0x200C	0x00	<a href="#">ERROR_THRESHOLD_0[7:0]</a>	UNCORRECTED_ERROR_THRESHOLD_0[7:0]							
0x200D	0x00	<a href="#">ERROR_THRESHOLD_1[7:0]</a>	UNCORRECTED_ERROR_THRESHOLD_1[7:0]							
0x200E	0x00	<a href="#">ERROR_THRESHOLD_2[7:0]</a>	UNCORRECTED_ERROR_THRESHOLD_2[7:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x200F	0x00	<a href="#">ERROR_THR ESHOLD_3[7: 0]</a>	UNCORRECTED_ERROR_THRESHOLD_3[7:0]							
0x2020	0x00	<a href="#">BLOCKS_UN CORRECTAB LE_0[7:0]</a>	UNCORRECTABLE_BLOCKS_0[7:0]							
0x2021	0x00	<a href="#">BLOCKS_UN CORRECTAB LE_1[7:0]</a>	UNCORRECTABLE_BLOCKS_1[7:0]							
0x2022	0x00	<a href="#">BLOCKS_UN CORRECTAB LE_2[7:0]</a>	UNCORRECTABLE_BLOCKS_2[7:0]							
0x2023	0x00	<a href="#">BLOCKS_UN CORRECTAB LE_3[7:0]</a>	UNCORRECTABLE_BLOCKS_3[7:0]							
0x2024	0x00	<a href="#">BITS_CORRE CTED_0[7:0]</a>	BIT_ERRS_CORRECTED_0[7:0]							
0x2025	0x00	<a href="#">BITS_CORRE CTED_1[7:0]</a>	BIT_ERRS_CORRECTED_1[7:0]							
0x2026	0x00	<a href="#">BITS_CORRE CTED_2[7:0]</a>	BIT_ERRS_CORRECTED_2[7:0]							
0x2027	0x00	<a href="#">BITS_CORRE CTED_3[7:0]</a>	BIT_ERRS_CORRECTED_3[7:0]							
0x2028	0x00	<a href="#">BLOCKS_PR OCESSSED_0[ 7:0]</a>	BLOCKS_PROCESSED_0[7:0]							
0x2029	0x00	<a href="#">BLOCKS_PR OCESSSED_1[ 7:0]</a>	BLOCKS_PROCESSED_1[7:0]							
0x202A	0x00	<a href="#">BLOCKS_PR OCESSSED_2[ 7:0]</a>	BLOCKS_PROCESSED_2[7:0]							
0x202B	0x00	<a href="#">BLOCKS_PR OCESSSED_3[ 7:0]</a>	BLOCKS_PROCESSED_3[7:0]							
FEC_B										
0x2100	0x00	<a href="#">CLEAR_STA TS[7:0]</a>	-	-	-	-	CLEAR_BITS_C ORREC TED_B	CLEAR_BLOCKS UNCO RRECTA BLE_B	CLEAR_BLOCKS PROCE SSED_B	CLEAR_ALL_ST ATS_B
0x2101	0x00	<a href="#">STATS_CON TROL[7:0]</a>	-	-	-	-	-	-	-	STATS_ENABLE _B
0x2108	0x00	<a href="#">CORRECTED _THRESHOL D_0[7:0]</a>	BIT_ERRS_CORRECTED_THRESHOLD_0_B[7:0]							
0x2109	0x00	<a href="#">CORRECTED _THRESHOL D_1[7:0]</a>	BIT_ERRS_CORRECTED_THRESHOLD_1_B[7:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB						LSB
0x210A	0x00	<a href="#">CORRECTED_THRESHOLD_2[7:0]</a>	BIT_ERRS_CORRECTED_THRESHOLD_2_B[7:0]						
0x210B	0x00	<a href="#">CORRECTED_THRESHOLD_3[7:0]</a>	BIT_ERRS_CORRECTED_THRESHOLD_3_B[7:0]						
0x210C	0x00	<a href="#">ERROR_THRESHOLD_0[7:0]</a>	UNCORRECTED_ERROR_THRESHOLD_0_B[7:0]						
0x210D	0x00	<a href="#">ERROR_THRESHOLD_1[7:0]</a>	UNCORRECTED_ERROR_THRESHOLD_1_B[7:0]						
0x210E	0x00	<a href="#">ERROR_THRESHOLD_2[7:0]</a>	UNCORRECTED_ERROR_THRESHOLD_2_B[7:0]						
0x210F	0x00	<a href="#">ERROR_THRESHOLD_3[7:0]</a>	UNCORRECTED_ERROR_THRESHOLD_3_B[7:0]						
0x2120	0x00	<a href="#">BLOCKS_UNCORRECTABLE_0[7:0]</a>	UNCORRECTABLE_BLOCKS_0_B[7:0]						
0x2121	0x00	<a href="#">BLOCKS_UNCORRECTABLE_1[7:0]</a>	UNCORRECTABLE_BLOCKS_1_B[7:0]						
0x2122	0x00	<a href="#">BLOCKS_UNCORRECTABLE_2[7:0]</a>	UNCORRECTABLE_BLOCKS_2_B[7:0]						
0x2123	0x00	<a href="#">BLOCKS_UNCORRECTABLE_3[7:0]</a>	UNCORRECTABLE_BLOCKS_3_B[7:0]						
0x2124	0x00	<a href="#">BITS_CORRECTED_0[7:0]</a>	BIT_ERRS_CORRECTED_0_B[7:0]						
0x2125	0x00	<a href="#">BITS_CORRECTED_1[7:0]</a>	BIT_ERRS_CORRECTED_1_B[7:0]						
0x2126	0x00	<a href="#">BITS_CORRECTED_2[7:0]</a>	BIT_ERRS_CORRECTED_2_B[7:0]						
0x2127	0x00	<a href="#">BITS_CORRECTED_3[7:0]</a>	BIT_ERRS_CORRECTED_3_B[7:0]						
0x2128	0x00	<a href="#">BLOCKS_PROCESSED_0[7:0]</a>	BLOCKS_PROCESSED_0_B[7:0]						
0x2129	0x00	<a href="#">BLOCKS_PROCESSED_1[7:0]</a>	BLOCKS_PROCESSED_1_B[7:0]						
0x212A	0x00	<a href="#">BLOCKS_PROCESSED_2[7:0]</a>	BLOCKS_PROCESSED_2_B[7:0]						
0x212B	0x00	<a href="#">BLOCKS_PROCESSED_3[7:0]</a>	BLOCKS_PROCESSED_3_B[7:0]						

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
FUNC_SAFE										
0x3000	0x00	REGCRC0[7:0]*	-	-	RSVD	GEN_ROLLING_CRC	I2C_WRCOMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
0x3001	0x00	REGCRC1[7:0]*	CRC_PERIOD[7:0]							
0x3002	0x00	REGCRC2[7:0]	REGCRC_LSB[7:0]							
0x3003	0x00	REGCRC3[7:0]	REGCRC_MSB[7:0]							
0x3008	0x00	I2C_UART_CRC0[7:0]	-	-	-	-	-	-	-	RESET_MSGCNTR
0x3009	0x00	I2C_UART_CRC1[7:0]*	MSGCNTR_ERR_THR[2:0]			CRC_ERR_THR[2:0]			RESET_MSGCNTR_ERR_CNT	RESET_CRC_ERR_CNT
0x300A	0x00	I2C_UART_CRC2[7:0]	CRC_VAL[7:0]							
0x300B	0x00	I2C_UART_CRC3[7:0]	MSGCNTR_LSB[7:0]							
0x300C	0x00	I2C_UART_CRC4[7:0]	MSGCNTR_MSB[7:0]							
0x300D	0x00	I2C_UART_CRC5[7:0]	CRC_ERR_CNT[7:0]							
0x300E	0x00	I2C_UART_CRC6[7:0]	MSGCNTR_ERR_CNT[7:0]							
0x300F	0x06	I2C_UART_CRC7[7:0]*	-	-	-	MSGCNTR_PORT_SEL[1:0]		CC_MSGCNTR_EN	CC_CRC_EN	CC_CRC_MSGCNTR_OVR
0x3010	0xE2	FS_INTR0[7:0]*	I2C_UART_MSGCNTR_ERR_OEN	I2C_UART_CRC_ERR_OEN	MEM_ECC_ERR2_OEN	MEM_ECC_ERR1_OEN	-	-	EFUSE_CRC_ERR_OEN	REG_CRC_ERR_OEN
0x3011	0x00	FS_INTR1[7:0]	I2C_UART_MSGCNTR_ERR_INT	I2C_UART_CRC_ERR_INT	MEM_ECC_ERR2_INT	MEM_ECC_ERR1_INT	-	-	EFUSE_CRC_ERR_FLAG	REG_CRC_ERR_FLAG
0x3016	0x00	MEM_ECC0[7:0]*	MEM_ECC_ERR2_THR[2:0]			MEM_ECC_ERR1_THR[2:0]			RESET_MEM_ECC_ERR2_CNT	RESET_MEM_ECC_ERR1_CNT
0x3017	0x00	MEM_ECC1[7:0]	MEM_ECC_ERR1_CNT[7:0]							
0x3018	0x00	MEM_ECC2[7:0]	MEM_ECC_ERR2_CNT[7:0]							
0x3020	0x00	REG_POST0[7:0]*	POST_DONE	POST_MBISSSED	POST_LBISSSED	-	-	RSVD	POST_RUN_MBISSSED	POST_RUN_LBISSSED
0x3030	0xFF	REGCRC8[7:0]	SKIP0_LSB[7:0]							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x3031	0xFF	<a href="#">REGCRC9[7:0]</a>	SKIP0_MSB[7:0]							
0x3032	0xFF	<a href="#">REGCRC10[7:0]</a>	SKIP1_LSB[7:0]							
0x3033	0xFF	<a href="#">REGCRC11[7:0]</a>	SKIP1_MSB[7:0]							
0x3034	0xFF	<a href="#">REGCRC12[7:0]</a>	SKIP2_LSB[7:0]							
0x3035	0xFF	<a href="#">REGCRC13[7:0]</a>	SKIP2_MSB[7:0]							
0x3036	0xFF	<a href="#">REGCRC14[7:0]</a>	SKIP3_LSB[7:0]							
0x3037	0xFF	<a href="#">REGCRC15[7:0]</a>	SKIP3_MSB[7:0]							
0x3038	0xFF	<a href="#">REGCRC16[7:0]</a>	SKIP4_LSB[7:0]							
0x3039	0xFF	<a href="#">REGCRC17[7:0]</a>	SKIP4_MSB[7:0]							
0x303A	0xFF	<a href="#">REGCRC18[7:0]</a>	SKIP5_LSB[7:0]							
0x303B	0xFF	<a href="#">REGCRC19[7:0]</a>	SKIP5_MSB[7:0]							
0x303C	0xFF	<a href="#">REGCRC20[7:0]</a>	SKIP6_LSB[7:0]							
0x303D	0xFF	<a href="#">REGCRC21[7:0]</a>	SKIP6_MSB[7:0]							
0x303E	0xFF	<a href="#">REGCRC22[7:0]</a>	SKIP7_LSB[7:0]							
0x303F	0xFF	<a href="#">REGCRC23[7:0]</a>	SKIP7_MSB[7:0]							
0x304F	0x00	<a href="#">CC_RTTN_ERR[7:0]</a>	-	-	-	-	RSVD	RESET_EFUSE_CRC_ERR	INJECT_EFUSE_CRC_ERR	INJECT_RTTN_CRC_ERR
<b>TCTRL_EXT</b>										
0x5009	0x00	<a href="#">CTRL9[7:0]</a>	RSVD	RSVD	-	-	LOCKED_B	-	-	-
0x5010	0x88	<a href="#">INTR10[7:0]*</a>	RTTN_CRC_ERR_OEN	IDLE_ERR_OEN_B	FEC_RX_ERR_OEN_B	VDD18_OV_OEN	MAX_RT_OEN_B	RT_CNT_OEN_B	PKT_CNT_OEN_B	VDD_OV_OEN
0x5011	0x00	<a href="#">INTR11[7:0]</a>	RTTN_CRC_INT	IDLE_ERR_FLAG_B	FEC_RX_ERR_FLAG_B	VDD18_OV_FLAG	MAX_RT_FLAG_B	RT_CNT_FLAG_B	PKT_CNT_FLAG_B	VDD_OV_FLAG
0x5012	0x00	<a href="#">INTR13[7:0]</a>	FEC_B_I_NACTIVE_OEN	FEC_A_I_NACTIVE_OEN	-	-	-	-	video_m em_overf low_oen	LOSS_OF_LOCK_OEN
0x5013	0x00	<a href="#">INTR14[7:0]</a>	FEC_B_I_NACTIVE	FEC_A_I_NACTIVE	-	-	-	-	video_m em_overf low	LOSS_OF_LOCK_FLAG
0x5018	0x1F	<a href="#">INTR12[7:0]*</a>	-	-	-	ERR_RX_ID_B[4:0]				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x5024	0x00	CNT2[7:0]	IDLE_ERR_B[7:0]							
0x5025	0x00	CNT3[7:0]	PKT_CNT_B[7:0]							
OVERLAP										
VID_RX_EXT Y										
0x501A	0x00	VIDEO_RX13[7:0]	-	-	-	-	-	-	-	LOSS_OF_VIDEO_LOCK_OEN
0x501B	0x00	VIDEO_RX14[7:0]	-	-	-	-	-	-	-	LOSS_OF_VIDEO_LOCK_OEN
VID_RX_EXT Z										
0x5020	0x00	VIDEO_RX13[7:0]	-	-	-	-	-	-	-	LOSS_OF_VIDEO_LOCK_OEN
0x5021	0x00	VIDEO_RX14[7:0]	-	-	-	-	-	-	-	LOSS_OF_VIDEO_LOCK_OEN
GMSL B										
0x5028	0x60	TX0[7:0]*	RSVD[1:0]		RSVD	RSVD	-	-	RX_FEC_EN	RSVD
0x5029	0x08	TX1[7:0]*	LINK_PRBS_GEN	RSVD	-	ERRG_EN_B	RSVD	RSVD	RSVD	RSVD
0x502A	0x20	TX2[7:0]*	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]		ERRG_PER	
0x502B	0x44	TX3[7:0]*	RSVD[1:0]		RX_FEC_ACTIVE	RSVD	-	RSVD[2:0]		
0x502C	0x00	RX0[7:0]*	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
0x5030	0x41	GPIOA[7:0]*	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
0x5031	0x88	GPIOB[7:0]*	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
CFGH_B VIDEO_X										
0x5050	0x00	RX0[7:0]*	RX_CRC_EN_B	-	-	-	-	-	STR_SEL_B[1:0]	
CFGH_B VIDEO_Y										
0x5051	0x01	RX0[7:0]*	RX_CRC_EN_B	-	-	-	-	-	STR_SEL_B[1:0]	
CFGH_B VIDEO_Z										
0x5052	0x02	RX0[7:0]*	RX_CRC_EN_B	-	-	-	-	-	STR_SEL_B[1:0]	
CFGH_B VIDEO_U										
0x5053	0x03	RX0[7:0]*	RX_CRC_EN_B	-	-	-	-	-	STR_SEL_B[1:0]	
CFGH_B INFOFR										
0x5060	0xF0	TR0[7:0]*	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
0x5061	0xB0	TR1[7:0]*	BW_MULT_B[1:0]		BW_VAL_B[5:0]					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB						LSB
0x5063	0x00	<a href="#">TR3[7:0]*</a>	–	–	–	–	–	TX_SRC_ID_B[2:0]	
0x5064	0xFF	<a href="#">TR4[7:0]*</a>	RX_SRC_SEL_B[7:0]						
CFG_C_B CC									
0x5070	0xF0	<a href="#">TR0[7:0]*</a>	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]
0x5071	0xB0	<a href="#">TR1[7:0]*</a>	BW_MULT_B[1:0]		BW_VAL_B[5:0]				
0x5073	0x00	<a href="#">TR3[7:0]*</a>	–	–	–	–	–	TX_SRC_ID_B[2:0]	
0x5074	0xFF	<a href="#">TR4[7:0]*</a>	RX_SRC_SEL_B[7:0]						
0x5075	0x98	<a href="#">ARQ0[7:0]*</a>	RSVD	RSVD	RSVD	RSVD	EN_B	DIS_DBL_ACK_R_ETX_B	–
0x5076	0x72	<a href="#">ARQ1[7:0]*</a>	–	RSVD[2:0]			–	–	MAX_RT_ERR_O_EN_B
0x5077	0x00	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR_B	RT_CNT_B[6:0]					
CFG_L_B GPIO									
0x5078	0xF0	<a href="#">TR0[7:0]*</a>	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]
0x5079	0xB0	<a href="#">TR1[7:0]*</a>	BW_MULT_B[1:0]		BW_VAL_B[5:0]				
0x507B	0x00	<a href="#">TR3[7:0]*</a>	–	–	–	–	–	TX_SRC_ID_B[2:0]	
0x507C	0xFF	<a href="#">TR4[7:0]*</a>	RX_SRC_SEL_B[7:0]						
0x507D	0x98	<a href="#">ARQ0[7:0]*</a>	RSVD	RSVD	RSVD	RSVD	EN_B	DIS_DBL_ACK_R_ETX_B	–
0x507E	0x72	<a href="#">ARQ1[7:0]*</a>	–	RSVD[2:0]			–	–	MAX_RT_ERR_O_EN_B
0x507F	0x00	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR_B	RT_CNT_B[6:0]					
CFG_C_B IIC_X									
0x5080	0xF0	<a href="#">TR0[7:0]*</a>	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]
0x5081	0xB0	<a href="#">TR1[7:0]*</a>	BW_MULT_B[1:0]		BW_VAL_B[5:0]				
0x5083	0x00	<a href="#">TR3[7:0]*</a>	–	–	–	–	–	TX_SRC_ID_B[2:0]	
0x5084	0xFF	<a href="#">TR4[7:0]*</a>	RX_SRC_SEL_B[7:0]						
0x5085	0x98	<a href="#">ARQ0[7:0]*</a>	RSVD	RSVD	RSVD	RSVD	EN_B	DIS_DBL_ACK_R_ETX_B	–
0x5086	0x72	<a href="#">ARQ1[7:0]*</a>	–	RSVD[2:0]			–	–	MAX_RT_ERR_O_EN_B
0x5087	0x00	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR_B	RT_CNT_B[6:0]					
CFG_C_B IIC_Y									
0x5088	0xF0	<a href="#">TR0[7:0]*</a>	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]
0x5089	0xB0	<a href="#">TR1[7:0]*</a>	BW_MULT_B[1:0]		BW_VAL_B[5:0]				



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x508B	0x00	<a href="#">TR3[7:0]*</a>	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0x508C	0xFF	<a href="#">TR4[7:0]*</a>	RX_SRC_SEL_B[7:0]							
0x508D	0x98	<a href="#">ARQ0[7:0]*</a>	RSVD	RSVD	RSVD	RSVD	EN_B	DIS_DBL _ACK_R ETX_B	–	–
0x508E	0x72	<a href="#">ARQ1[7:0]*</a>	–	RSVD[2:0]			–	–	MAX_RT _ERR_O _EN_B	RT_CNT _OEN_B
0x508F	0x00	<a href="#">ARQ2[7:0]</a>	MAX_RT _ERR_B	RT_CNT_B[6:0]						
GPIO0_B 0										
0x52B0	0x02	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52B1	0x00	<a href="#">GPIO_B[7:0]*</a>	–	–	–	GPIO_TX_ID_B[4:0]				
0x52B2	0x40	<a href="#">GPIO_C[7:0]*</a>	–	GPIO_R ECVED_ B	–	GPIO_RX_ID_B[4:0]				
GPIO0_B 1										
0x52B3	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52B4	0x01	<a href="#">GPIO_B[7:0]*</a>	–	–	–	GPIO_TX_ID_B[4:0]				
0x52B5	0x41	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–	GPIO_RX_ID_B[4:0]				
GPIO0_B 2										
0x52B6	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52B7	0x02	<a href="#">GPIO_B[7:0]*</a>	–	–	–	GPIO_TX_ID_B[4:0]				
0x52B8	0x42	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–	GPIO_RX_ID_B[4:0]				
GPIO0_B 3										
0x52B9	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52BA	0x03	<a href="#">GPIO_B[7:0]*</a>	–	–	–	GPIO_TX_ID_B[4:0]				
0x52BB	0x43	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–	GPIO_RX_ID_B[4:0]				
GPIO0_B 4										
0x52BC	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52BD	0x04	<a href="#">GPIO_B[7:0]*</a>	–	–	–	GPIO_TX_ID_B[4:0]				
0x52BE	0x44	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–	GPIO_RX_ID_B[4:0]				
GPIO0_B 5										
0x52BF	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52C0	0x05	<a href="#">GPIO_B[7:0]*</a>	–	–	–	GPIO_TX_ID_B[4:0]				
0x52C1	0x45	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–	GPIO_RX_ID_B[4:0]				
GPIO0_B 6										
0x52C2	0x02	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52C3	0x06	<a href="#">GPIO_B[7:0]*</a>	–	–	–	GPIO_TX_ID_B[4:0]				

# MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

ADDRESS	RESET	NAME	MSB							LSB
0x52C4	0x46	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–					GPIO_RX_ID_B[4:0]
<b>GPIO0_B 7</b>										
0x52C5	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52C6	0x07	<a href="#">GPIO_B[7:0]*</a>	–	–	–					GPIO_TX_ID_B[4:0]
0x52C7	0x47	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–					GPIO_RX_ID_B[4:0]
<b>GPIO0_B 8</b>										
0x52C8	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52C9	0x08	<a href="#">GPIO_B[7:0]*</a>	–	–	–					GPIO_TX_ID_B[4:0]
0x52CA	0x48	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–					GPIO_RX_ID_B[4:0]
<b>GPIO0_B 9</b>										
0x52CB	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52CC	0x09	<a href="#">GPIO_B[7:0]*</a>	–	–	–					GPIO_TX_ID_B[4:0]
0x52CD	0x49	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–					GPIO_RX_ID_B[4:0]
<b>GPIO0_B 10</b>										
0x52CE	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52CF	0x0A	<a href="#">GPIO_B[7:0]*</a>	–	–	–					GPIO_TX_ID_B[4:0]
0x52D0	0x4A	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–					GPIO_RX_ID_B[4:0]
<b>GPIO0_B 11</b>										
0x52D1	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52D2	0x0B	<a href="#">GPIO_B[7:0]*</a>	–	–	–					GPIO_TX_ID_B[4:0]
0x52D3	0x4B	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–					GPIO_RX_ID_B[4:0]
<b>GPIO0_B 12</b>										
0x52D4	0x00	<a href="#">GPIO_A[7:0]*</a>	–	RSVD	TX_COM P_EN_B	–	–	GPIO_R X_EN_B	GPIO_T X_EN_B	–
0x52D5	0x0C	<a href="#">GPIO_B[7:0]*</a>	–	–	–					GPIO_TX_ID_B[4:0]
0x52D6	0x4C	<a href="#">GPIO_C[7:0]*</a>	–	RSVD	–					GPIO_RX_ID_B[4:0]

### Register Details

#### [REG0 \(0x0\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1001000							0b0
Access Type	Write, Read							Write, Read

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE																		
DEV_ADDR	7:1	<p>Device I<sup>2</sup>C Address</p> <p>Default value is set by the CFG0 pin as follows:</p> <table><tr><td>CFG0</td><td>Device Address</td></tr><tr><td>000</td><td>0b0101000</td></tr><tr><td>001</td><td>0b0101010</td></tr><tr><td>010</td><td>0b1001100</td></tr><tr><td>011</td><td>0b1101010</td></tr><tr><td>100</td><td>0b1101010</td></tr><tr><td>101</td><td>0b1001100</td></tr><tr><td>110</td><td>0b0101010</td></tr><tr><td>111</td><td>0b0101000</td></tr></table>	CFG0	Device Address	000	0b0101000	001	0b0101010	010	0b1001100	011	0b1101010	100	0b1101010	101	0b1001100	110	0b0101010	111	0b0101000	<p>0b0000000: I<sup>2</sup>C write/read address is 0x00/0x01</p> <p>0b0000001: I<sup>2</sup>C write/read address is 0x02/0x03</p> <p>...</p> <p>0b1001000: I<sup>2</sup>C write/read address is 0x90/0x91</p> <p>0b1001010: I<sup>2</sup>C write/read address is 0x94/0x95</p> <p>0b1001100: I<sup>2</sup>C write/read address is 0x98/0x99</p> <p>0b1101000: I<sup>2</sup>C write/read address is 0xD0/0xD1</p> <p>0b1101010: I<sup>2</sup>C write/read address is 0xD4/0xD5</p> <p>0b1101100: I<sup>2</sup>C write/read address is 0xD8/0xD9</p> <p>0b0101000: I<sup>2</sup>C write/read address is 0x50/0x51</p> <p>0b0101010: I<sup>2</sup>C write/read address is 0x54/0x55</p> <p>...</p> <p>...</p> <p>0b1111111: I<sup>2</sup>C write/read address is 0xFE/0xFF</p>
CFG0	Device Address																				
000	0b0101000																				
001	0b0101010																				
010	0b1001100																				
011	0b1101010																				
100	0b1101010																				
101	0b1001100																				
110	0b0101010																				
111	0b0101000																				
CFG_BLOCK	0	<p>Configuration Block</p> <p>When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration. The only way to clear this register and regain write access is with a power cycle or toggling the PWDNB pin.</p>	<p>0b0: Not blocked</p> <p>0b1: Blocked</p>																		

**REG1 (0x1)\***

BIT	7	6	5	4	3	2	1	0
Field	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RX_RATE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b00		0b10	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
IIC_2_EN	7	Enable pass-through I <sup>2</sup> C Channel 2 (SDA2/ RX2, SCL2/TX2)	0b0: I <sup>2</sup> C pass-through Channel 2 disabled 0b1: I <sup>2</sup> C pass-through Channel 2 enabled
IIC_1_EN	6	Enable pass-through I <sup>2</sup> C Channel 1 (SDA1/ RX1, SCL1/TX1)	0b0: I <sup>2</sup> C pass-through Channel 1 disabled 0b1: I <sup>2</sup> C pass-through Channel 1 enabled
DIS_LOCAL_CC	5	Disable control channel connection to RX/ SDA and TX/SCL pins	0b0: RX/SDA and TX/XCL connected to control channel 0b1: RX/SDA and TX/SCL disconnected from control channel
DIS_REM_C C	4	Disable access to Link A serializer control channel over GMSL2 connection from RX/ SDA and TX/SCL pins.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
TX_RATE	3:2	Link A Transmitter Rate When changing this value, restart the link with a write to the RESET_ONESHOT or RESET_LINK register for the new value to take effect.	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
RX_RATE	1:0	Link A Receiver Rate When changing this value, restart the link with a write to the RESET_ONESHOT or RESET_LINK register for the new value to take effect. Default value is set by configuration pins at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: 12Gbps (applies to GMSL3 capable parts)

**REG2 (0x2)\***

BIT	7	6	5	4	3	2	1	0
Field	–	VID_EN_Z	VID_EN_Y	–	–	–	RSVD	RSVD
Reset	–	0b1	0b1	–	–	–	0b1	0b1
Access Type	–	Write, Read	Write, Read	–	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_Z	6	Enable data transmission through video pipe Z	0b0: Video pipe Z disabled 0b1: Video pipe Z enabled
VID_EN_Y	5	Enable data transmission through video pipe Y	0b0: Video pipe Y disabled 0b1: Video pipe Y enabled

**REG3 (0x3)\***

BIT	7	6	5	4	3	2	1	0
Field	LOCK_CFG	PT_SWAP	UART_2_EN	UART_1_EN	–	DIS_REM_CC_B	RSVD	RSVD
Reset	0b0	0b1	0b0	0b1	–	0b0	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_CFG	7	Configure LOCK pin behavior	0b0: GMSL2 link locked 0b1: GMSL2 link locked and MIPI output started
PT_SWAP	6	Swap I <sup>2</sup> C/UART pass-through 1 pin assignments with pass-through 2 pin assignments. Swaps SDA1_RX1 (MFP0) with SDA2_RX2 (MFP5), and SCL1_TX1 (MFP1) with SCL2_TX2 (MFP6).	0b0: Do not swap pin assignments 0b1: Swap pin assignments
UART_2_EN	5	Enable pass-through UART Channel 2 (SDA2/RX2, SCL2/TX2) (MFP5/6)	0b0: Pass-through UART Channel 2 disabled 0b1: Pass-through UART Channel 2 enabled
UART_1_EN	4	Enable pass-through UART Channel 1 (SDA1/RX1, SCL1/TX1) (MFP0/1)	0b0: Pass-through UART Channel 1 disabled 0b1: Pass-through UART Channel 1 enabled
DIS_REM_CC_B	2	Disable access to Link B serializer control channel over GMSL2 connection from RX/SDA and TX/SCL pins	0b0: Remote control channel enabled 0b1: Remote control channel disabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**REG4 (0x4)\***

BIT	7	6	5	4	3	2	1	0
Field	GMSL3_B	GMSL3_A	RSVD	RSVD	TX_RATE_B[1:0]		RX_RATE_B[1:0]	
Reset	0b1	0b1	0b0	0b0	0b00		0b10	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL3_B	7	GMSL3 or 2 selection for Link B. Bit is set according to the latched CFG pin value at power-up. When changing this value, restart the link with a write to the RESET_ONESHOT or RESET_LINK register for the new value to take effect.	0x0: GMSL2 0x1: GMSL3
GMSL3_A	6	GMSL3 or 2 selection for Link A. Bit is set according to the latched CFG pin value at power-up. When changing this value, restart the link with a write to the RESET_ONESHOT or RESET_LINK register for the new value to take effect.	0x0: GMSL2 0x1: GMSL3
TX_RATE_B	3:2	Link B Transmitter Rate When changing this value, restart the link with a write to the RESET_ONESHOT or RESET_LINK register for the new value to take effect.	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE_B	1:0	Link B Receiver Rate When changing this value, restart the link with a write to the RESET_ONESHOT or RESET_LINK register for the new value to take effect. Default value is set by configuration pins at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: 12Gbps (applies to GMSL3 capable parts)

**REG5 (0x5)\***

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	LOCK_ALT_EN	RSVD	PU_LF3	PU_LF2	PU_LF1	PU_LF0
Reset	0b1	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enable LOCK output	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enable ERRB output	0b0: ERRB output disabled 0b1: ERRB output enabled
LOCK_ALT_EN	5	Enable LOCK alternate output	0b0: LOCK output disabled 0b1: LOCK output enabled
PU_LF3	3	Power up line-fault monitor 3	0b0: Line-fault monitor 3 disabled 0b1: Line-fault monitor 3 enabled
PU_LF2	2	Power up line-fault monitor 2	0b0: Line-fault monitor 2 disabled 0b1: Line-fault monitor 2 enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
PU_LF1	1	Power up line-fault monitor 1	0b0: Line-fault monitor 1 disabled 0b1: Line-fault monitor 1 enabled
PU_LF0	0	Power up line-fault monitor 0	0b0: Line-fault monitor 0 disabled 0b1: Line-fault monitor 0 enabled

**REG6 (0x6)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	I2CSEL	RSVD[3:0]			
Reset	0b1	0b1	0b0	0b0	0x0			
Access Type				Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
I2CSEL	4	I <sup>2</sup> C/UART selection Bit is set according to the CFG0 pin value at power-up. Changing this value through a register write is not recommended. Instead, change the CFG0 pin voltage and power up the device again.	0: UART 1: I <sup>2</sup> C

**REG7 (0x7)\***

BIT	7	6	5	4	3	2	1	0
Field	CMP_VTER M_STATUS	—	RSVD[5:0]					
Reset	0b0	—	0x27					
Access Type	Read Only	—						

BITFIELD	BITS	DESCRIPTION	DECODE
CMP_VTER M_STATUS	7	V <sub>TERM</sub> supply undervoltage comparator status  Latched low when switched V <sub>TERM</sub> supply < 1V. Cleared when the CMP_STATUS word is read and the switched V <sub>TERM</sub> supply is > 1V.	0b0: Latched low when V <sub>TERM</sub> < 1V 0b1: 0b1: Latched high when V <sub>TERM</sub> > 1V

**REG13 (0xD)**

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0xB6							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device Identifier	0xB6: MAX96792A

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**REG14 (0xE)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				DEV_REV[3:0]			
Reset	0x0				0x3			
Access Type					Read Only			
BITFIELD	BITS	DESCRIPTION			DECODE			
DEV_REV	3:0	Device Revision. Refer device Errata Sheet for correct RESET value.			0xX: Revision ID number. Refer to errata for specific revision ID.			

**REG26 (0x26)**

BIT	7	6	5	4	3	2	1	0
Field	–	LF_1[2:0]			–	LF_0[2:0]		
Reset	–	0b010			–	0b010		
Access Type	–	Read Only			–	Read Only		
BITFIELD	BITS	DESCRIPTION			DECODE			
LF_1	6:4	Line-fault status of wire connected to LMN1 pin			0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short			
LF_0	2:0	Line-fault status of wire connected to LMN0 pin			0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short			

**REG27 (0x27)**

BIT	7	6	5	4	3	2	1	0
Field	–	LF_3[2:0]			–	LF_2[2:0]		
Reset	–	0b010			–	0b010		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_3	6:4	Line-fault status of wire connected to LMN3 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short
LF_2	2:0	Line-fault status of wire connected to LMN2 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**IO\_CHK0 (0x38)**

BIT	7	6	5	4	3	2	1	0
Field	PIN_DRV_EN_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITLEVEL	BITS	DESCRIPTION	DECODE
PIN_DRV_EN_0	7:0	<p>Bits 1:0: Set source clock frequency for RGB888 test pattern generator.</p> <p>Used together with register PATGEN_CLK_SRC register bit. When bit 1 of this register is set to 1, PATGEN_CLK_SRC controls the clock selection. When bit 1 is 0, then bit 0 controls the clock selection. See PATGEN_CLK_SRC for more details.</p> <p>Bits 7:2: Reserved</p>	<p>0x00: See RGB888 Video-Pattern Generator Section</p> <p>0x01: See RGB888 Video-Pattern Generator Section</p> <p>0x02: See RGB888 Video-Pattern Generator Section</p> <p>0x03: See RGB888 Video-Pattern Generator Section</p> <p>Others: Reserved</p>

**PWR0 (0x8)**

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[2:0]				CMP_STATUS[4:0]			
Reset	0b000				0b00000			
Access Type	Read Only				Read Only			

BITLEVEL	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:5	Switched 1V supply comparator status bits	<p>0bXX1: Latched high when CAP_VDD &lt; 0.82V</p> <p>0bX1X: Latched high when CAP_VDD &lt; 0.82V</p> <p>0bX00: CAP_VDD &gt; 0.82V</p> <p>0b1XX: Reserved</p>
CMP_STATUS	4:0	VDD18, VDDIO, and CAP_VDD supply voltage comparator status bits	<p>0bXXXX0: Latched low when VDD18 &lt; 1.617V</p> <p>0bXXX0X: Latched low when switched VDDIO supply &lt; 1.617V</p> <p>0bXX0XX: Latched low when CAP_VDD &lt; 0.82V</p> <p>0bX0XXX: Reserved</p> <p>0b0XXXX: Reserved</p> <p>0bXX111: All supplies are at expected levels</p>

**PWR1 (0x9)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	PORZ_STATUS[5:0]					
Reset	0b0	0b0	0b000000					
Access Type			Read Only					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
PORZ_STAT US	5:0	Power-on-reset status bits Bit 0: Latched low when either $V_{DD18} < 1.516V$ or $V_{DDIO} < 1.055V$	Bit 1: Reserved Bit 2: Latched low when $V_{DDIO} < 1.055V$ Bit 3: Reserved Bit 4: Latched low when $V_{DD18} < 1.516V$ (resets 1V domain, need to raise $V_{DD18}$ above 1.516V to read registers) Bit 5: Reserved

**PWR4 (0xC)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b1	0x5			
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable wake-up by local $\mu C$ from SDA_RX pin	0b0: Local wake-up enabled 0b1: Local wake-up disabled
WAKE_EN_B	5	Enable wake-up by remote chip connected to Link B	0b0: Link B remote wake-up disabled 0b1: Link B remote wake-up enabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to Link A	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled

**CTRL0 (0x10)\***

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	REG_ENABLE	LINK_CFG[1:0]	
Reset	0b0	0b0	0b0	0b1	0b0	0b0	0b01	
Access Type	Write, Read	Write, Read	Write Clears All, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Device Reset Writing a 1 to this bit resets the device (including all blocks) and resets registers to defaults. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset
RESET_LINK	6	Link Reset Resets entire data path on Link A (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link A reset 0b1: Activate link A reset
RESET_ONESHOT	5	One-Shot Link Reset Reset entire data path on Link A (keep register settings). Write 1 to activate reset, bit self clears and automatically releases reset.	0b0: No action 0b1: Reset data path

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_LINK	4	Automatically selects link configuration (single A or single B) Reverse splitter mode (two GMSL links enabled) is not automatic. For reverse splitter mode, set LINK_CFG = 11.	0b0: Disable auto link configuration 0b1: Enable auto link configuration
SLEEP	3	Activates sleep mode	0b0: Sleep mode disabled 0b1: Sleep mode enabled
REG_ENABLER	2	Enables V <sub>DD</sub> LDO regulator. See Programming Notes.	0b0: V <sub>DD</sub> LDO regulator bypassed 0b1: V <sub>DD</sub> LDO regulator enabled. LDO should always be used unless V <sub>DD</sub> is 1.05V or lower.
LINK_CFG	1:0	AUTO_LINK and this bitfield selects the link configuration per the decode table.	0b00: Reserved 0b01: Reserved. To select link A only, use LINK_EN_A and LINK_EN_B registers. This is the method to manually select link A only. 0b10: Reserved. To select link A only, use LINK_EN_A and LINK_EN_B registers. This is the method to manually select link B only. 0b11: Reverse Splitter mode. Both Link A and Link B selected.

#### CTRL1 (0x11)\*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	RSVD	CXTP_B	RSVD	CXTP_A
Reset	0b0	0b0	0b0	–	0b1	0b0	0b1	0b0
Access Type				–		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_B	2	Coax/twisted-pair cable select for Link B Bit is set according to the latched CFG pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/twisted-pair cable select for Link A Bit is set according to the latched CFG pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

#### CTRL2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RESET_ONESHOT_B	REG_MNL	RSVD[1:0]		RSVD[1:0]	
Reset	0b0	0b0	0b0	0b0	0b01		0b00	
Access Type			Write Clears All, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ONESHOT_B	5	Reset entire data path on Link B (keep register settings). Write 1 to activate reset, bit self clears and automatically releases reset.	0b0: No action 0b1: Reset data path

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
REG_MNL	4	Enable regulator manual mode to allow regulator to be forced on or off through REG_ENABLE (0x10).	0b0: Normal mode 0b1: Regulator manual mode

**CTRL3 (0x13)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	LINK_MODE[1:0]		LOCKED	ERROR	CMU_LOCKED	RESET_LINK_B
Reset	0b0	0b0	0b01		0b0	0b0	0b0	0b0
Access Type			Read Only		Read Only	Read Only	Read Only	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_MODE	5:4	Active link mode status	0b00: Reserved 0b01: Single Link A 0b10: Single Link B 0b11: Reverse Splitter mode (Both link A and B)
LOCKED	3	GMSL link locked (bidirectional). For Link A only.	0b0: GMSL2 link A not locked 0b1: GMSL2 link A locked
ERROR	2	Reflects global error status	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock multiplier unit (CMU) locked	0b0: CMU not locked 0b1: CMU locked
RESET_LINK_B	0	Reset entire data path on Link B (keep register settings).  Write 1 to activate reset, write 0 to release reset.	0b0: Release link B reset 0b1: Activate link B reset

**INTR0 (0x18)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	0b1	0b0	0b1	–	0b0	0b000		
Access Type				–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A (0x22), DEC_ERR_B (0x23), and IDLE_ERR (0x24) bitfields after ERRB pin is asserted for 1μs.	0b0: Autoreset disabled 0b1: Autoreset enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_THR	2:0	<p>Decoding and Idle-Error Reporting Threshold</p> <p>DEC_ERR_FLAG_A (0x1B) is asserted when DEC_ERR_A (0x22) <math>\geq</math> DEC_ERR_THR.</p> <p>DEC_ERR_FLAG_B (0x1B) is asserted when DEC_ERR_B (0x23) <math>\geq</math> DEC_ERR_THR.</p> <p>IDLE_ERR_FLAG (0x1B) is asserted when IDLE_ERR (0x24) <math>\geq</math> DEC_ERR_THR.</p> <p>IDLE_ERR_FLAG_B (0x5011) is asserted when IDLE_ERR_B (0x5024) <math>\geq</math> DEC_ERR_THR.</p>	<p>0b000: 1 error</p> <p>0b001: 2 errors</p> <p>0b010: 4 errors</p> <p>0b011: 8 errors</p> <p>0b100: 16 errors</p> <p>0b101: 32 errors</p> <p>0b110: 64 errors</p> <p>0b111: 128 errors</p>

#### INTR1 (0x19)\*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0x0				0b0	0b000		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	<p>Packet-Count Multiplier Exponent</p> <p>See the description of PKT_CNT (register CNT3) bitfield.</p>	0bXXX: PKT_CNT exponent
AUTO_CNT_RST_EN	3	Automatically resets PKT_CNT bitfield (register CNT3) after ERRB pin is asserted for 1 $\mu$ s.	<p>0b0: Autoreset disabled</p> <p>0b1: Autoreset enabled</p>
PKT_CNT_THR	2:0	<p>Packet-count reporting threshold</p> <p>See the description of PKT_CNT (register CNT3).</p> <p>PKT_CNT_FLAG is asserted when PKT_CNT <math>\geq</math> PKT_CNT_THR.</p>	<p>0b000: 1 packet</p> <p>0b001: 2 packets</p> <p>0b010: 4 packets</p> <p>0b011: 8 packets</p> <p>0b100: 16 packets</p> <p>0b101: 32 packets</p> <p>0b110: 64 packets</p> <p>0b111: 128 packets</p>

#### INTR2 (0x1A)\*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_OEN	RSVD	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b1	0b1
Access Type			Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_OEN	5	Enables reporting of remote-error status (REM_ERR_FLAG - 0x1B) at ERRB pin	<p>0b0: Reporting disabled</p> <p>0b1: Reporting enabled</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_OEN	3	Enables reporting of line-fault interrupt (LFLT_INT - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
IDLE_ERR_OEN	2	Enables reporting of idle-word errors (IDLE_ERR_FLAG - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_B	1	Enables reporting of decoding errors (DEC_ERR_FLAG_B - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enable reporting of decoding errors (DEC_ERR_FLAG_A - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

#### INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_FLAG	RSVD	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type			Read Only		Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_FLAG	5	Received remote-side error status (inverse of remote side ERRB pin level)	0b0: No remote-side error 0b1: Remote-side error
LFLT_INT	3	Line-Fault Interrupt Asserted when any one of line-fault monitors indicates a fault status. See LF_0 (0x26) and LF_1 (0x26) bitfields for more information.	0b0: No line fault 0b1: Line fault
IDLE_ERR_FLAG	2	Idle-Word-Error Flag for Link A Asserted when IDLE_ERR (0x23) ≥ DEC_ERR_THR (0x18). For Link A only.	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_B	1	Decoding Error Flag for Link B Asserted when DEC_ERR_B (0x23) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_A	0	Decoding Error Flag for Link A Asserted when DEC_ERR_A (0x22) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted

#### INTR4 (0x1C)\*

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_OEN_B	EOM_ERR_OEN_A	FEC_RX_ERR_OEN	–	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
Reset	0b0	0b0	0b0	–	0b1	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_B	7	Enable reporting of eye-opening monitor (EOM) error (EOM_ERR_FLAG_B - 0x1D) for Link B at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_A	6	Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_A - 0x1D) for Link A at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
FEC_RX_ERR_OEN	5	Enable reporting of Link A FEC receive errors exceeding thresholds (FEC_ERR_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enable reporting of Link A combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enable reporting of Link A combined ARQ retransmission event flag (RT_CNT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enable reporting of Link A packet count flag (PKT_CNT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
WM_ERR_OEN	0	Enable reporting of watermark errors (WM_ERR_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

**INTR5 (0x1D)**

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	FEC_RX_ERR_FLAG	—	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
Reset	0b0	0b0	0b0	—	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	—	Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_B	7	Eye-opening is below configured threshold for Link B	0b0: No EOM error on Link B 0b1: EOM error on Link B
EOM_ERR_FLAG_A	6	Eye-opening is below configured threshold for Link A	0b0: No EOM error on Link A 0b1: EOM error on Link A
FEC_RX_ERR_FLAG	5	FEC Receive Errors Flag for Link A  Asserted when the FEC receiver correctable OR uncorrectable error counters exceed their thresholds for the first time. When reading this flag, the status gets cleared. The FEC statistics counters must also be reset for this flag to be asserted again. See the CLEAR_STATS register to reset the counters.	0b0: Flag not asserted 0b1: Flag asserted
MAX_RT_FLAG	3	Combined ARQ maximum retransmission limit error flag. For Link A only.  Asserted when any of the selected channel's ARQ retransmission limit is reached.  Selection is done by each channel's MAX_RT_ERR_OEN (0x1C) register bit.	0b0: Flag not asserted 0b1: Flag asserted



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_FLAG	2	Combined ARQ Retransmission Event Flag. For Link A only.  Asserted when any of the selected channels have done at least one ARQ retransmission.  Selection is done by each channel's RT_CNT_OEN register bit.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet Count Flag. For Link A only.  Asserted when PKT_CNT (0x25) ≥ PKT_CNT_THR (0x19)	0b0: Flag not asserted 0b1: Flag asserted
WM_ERR_FLAG	0	Watermark Error Flag  Asserted when a watermark error is detected	0b0: Flag not asserted 0b1: Flag asserted

#### INTR6 (0x1E)\*

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	FSYNC_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	–	VID_PXL_CRC_ERR_OEN
Reset	0b0	0b0	0b0	0b1	0b1	0b1	–	0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	7	Enable reporting of VDDCMP interrupt (VDDCMP_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VDDBAD_INT_OEN	5	Enable reporting of VDDBAD interrupt (VDDBAD_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
FSYNC_ERR_OEN	4	Enable reporting of frame-sync errors (FSYNC_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LCRC_ERR_OEN	3	Enable reporting of video-line CRC errors (LCRC_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VPRBS_ERR_OEN	2	Enable reporting of video PRBS errors (VPRBS_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VID_PXL_CRC_ERR_OEN	0	Enable reporting of GMSL link packet CRC errors for video pixel data at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

#### INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	FSYNC_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	–	VID_PXL_CRC_ERR
Reset	0b0	0b0	0b0	0b0	0b0	0b0	–	0b0
Access Type	Read Only		Read Only	Read Only	Read Only	Read Only	–	Read Only

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	7	VDDCMP interrupt flag. This is a combined flag for undervoltage conditions for V <sub>DD18</sub> , V <sub>DDIO</sub> , CAP_VDD, and V <sub>TERM</sub> .	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	5	V <sub>DD</sub> status interrupt. This is a flag for CAP_VDD undervoltage condition.	0b0: Flag not asserted 0b1: Flag asserted
FSYNC_ERR_FLAG	4	Frame-sync error flag Asserted when FSYNC_ERR_CNT (0x3F0) ≥ FSYNC_ERR_THR (0x3F1).	0b0: Flag not asserted 0b1: Flag asserted
LCRC_ERR_FLAG	3	Video-line CRC error flag Asserted when a video-line CRC error is detected.	0b0: Flag not asserted 0b1: Flag asserted
VPRBS_ERR_FLAG	2	Video PRBS error flag Asserted when VPRBS_ERR (register PRBS_ERR) > 0	0b0: Flag not asserted 0b1: Flag asserted
VID_PXL_CRC_ERR	0	GMSL link packet CRC error flag for video pixel data	0b0: Error counter interrupt output not enabled 0b1: Error counter interrupt output enabled

#### INTR8 (0x20)\*

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	RSVD	ERR_TX_EN_B	ERR_TX_ID[4:0]				
Reset	0b1	0b1	0b1	0b11111				
Access Type	Write, Read		Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
ERR_TX_EN	7	Transmit local error status (inverse of ERRB pin level) to Link A remote side through GPIO channel		0b0: Transmit error status disabled 0b1: Transmit error status enabled				
ERR_TX_EN_B	5	Transmit local-error status (inverse of ERRB pin level) to Link B remote side through GPIO channel		0b0: Transmit error status disabled 0b1: Transmit error status enabled				
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX		0bXXXXX: Value of GPIO ID for transmitting ERR_TX				

#### INTR9 (0x21)\*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	RSVD	ERR_RX_EN_B	ERR_RX_ID[4:0]				
Reset	0b1	0b1	0b1	0b11111				
Access Type	Write, Read		Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
ERR_RX_EN	7	Receive Link A remote-error status (inverse of ERRB pin level) through GPIO channel		0b0: Receive error status disabled 0b1: Receive error status enabled				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_B	5	Receive Link B remote-error status (inverse of ERRB pin level) through GPIO channel	0b0: Receive error status disabled 0b1: Receive error status enabled
ERR_RX_ID	4:0	GPIO ID used for receiving ERR_RX	0bXXXXX: Value of GPIO ID for receiving ERR_RX

#### CNT0 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	Number of decoding (disparity) errors detected at Link A Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

#### CNT1 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_B	7:0	Number of decoding (disparity) errors detected at Link B Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link B decoding errors detected

#### CNT2 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of idle-word errors detected for Link A. Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle-word errors detected

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**CNT3 (0x25)**

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	<p>Number of received packets of a selected type for Link A</p> <p>Packet type is selected with PKT_CNT_SEL (0x2C) register.</p> <p>Reported packet count is a scaled value, such that actual packet count is <math>\geq \text{PKT\_CNT} \times (2^{\text{PKT\_CNT\_EXP}})</math> and <math>&lt; (\text{PKT\_CNT} + 1) \times (2^{\text{PKT\_CNT\_EXP}})</math>.</p> <p>When maximum value is reported, packet count is greater or equal to the reported value.</p>	0xXX: Scaled number of received packets

**TX0 (0x28)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD	RSVD	–	–	RX_FEC_EN	RSVD
Reset	0b01		0b1	0b0	–	–	0b0	0b0
Access Type					–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
RX_FEC_EN	1	Enable Forward-Error Correction (FEC) on Link A in forward direction. For GMSL3 parts, bit is set according to the latched CFG1 pin value at power-up.

**TX1 (0x29)\***

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_GEN	RSVD	–	ERRG_EN_A	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	–	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_GEN	7	Enable link PRBS-7 generator	0x0: Disabled 0x1: Enabled
ERRG_EN_A	4	Error generator enable for Link A (reverse channel). Error injection applies to all data going across the link.	0b0: Link A error generator disabled 0b1: Link A error generator enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**TX2 (0x2A)\***

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0b00		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error generator average bit-error rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits
ERRG_BURST	3:1	Error generator burst-error length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error generator error-distribution selection	0b0: Pseudorandom 0b1: Periodic

**TX3 (0x2B)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RX_FEC_ACTIVE	RSVD	–	RSVD[2:0]		
Reset	0b01		0b0	0b0	–	0b100		
Access Type			Read Only		–			

BITFIELD	BITS	DESCRIPTION
RX_FEC_ACTIVE	5	FEC is active

**RX0 (0x2C)\***

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
Reset	0b00		0x0	0b0	0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Select the subtype of Low-Bandwidth (LBW) packets to count at PKT_CNT (0x25) bitfield register	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_SEL	3:0	<p>Select the type of received packets to count at PKT_CNT (0x25) bitfield</p> <p>The selected packet type must be supported by the device.</p>	<p>0x0: None            0x1: VIDEO            0x2: Reserved            0x3: INFO Frame            0x4: SPI            0x5: I<sup>2</sup>C            0x6: UART            0x7: GPIO            0x8: Reserved            0x9: Reserved            0xA: Reserved            0xB: Reserved            0xC: Reserved            0xD: Reserved            0xE: All            0xF: Unknown and packets with error</p>

#### RX1 (0x2D)\*

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_CHK	RSVD	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD
Reset	0b0	0x0	0b10		0b10		0b0	0b0
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_CHK	7	Enable link PRBS-7 checker	<p>0x0: Disabled            0x1: Enabled</p>

#### RX3 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RSVD	RSVD	RSVD	RSVD	RSVD
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–					

#### GPIOA (0x30)\*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0b1	0b000001					
Access Type			Write, Read					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITLEFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	<p>Compensation delay multiplier for the forward direction. For Link A.</p> <p>This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link.</p> <p>Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.</p>	0bXXXXXX: Forward compensation delay multiplier value

#### GPIOB (0x31)\*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0b10		0b001000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	<p>Wait time after a GPIO transition to create a packet. For Link A.</p> <p>This allows grouping transitions of different GPIO inputs in a single packet and so increases GPIO bandwidth usage efficiency.</p>	<p>0b00: Disabled</p> <p>0b01: 200ns</p> <p>0b10: 500ns</p> <p>0b11: 1000ns</p>
GPIO_REV_CDLY	5:0	<p>Compensation delay multiplier for the reverse direction. For Link A.</p> <p>This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link.</p> <p>Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.</p>	<p>0bXXXXXX: Reverse compensation delay multiplier value</p>

#### I2C\_0 (0x40)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	<p>I<sup>2</sup>C-to-I<sup>2</sup>C slave-setup and hold-time setting.</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p>	<p>0b00: Set for I<sup>2</sup>C Fast-mode Plus speed (1Mbps)</p> <p>0b01: Set for I<sup>2</sup>C Fast-mode speed (400Kbps)</p> <p>0b10: Set for I<sup>2</sup>C standard-mode speed (100Kbps)</p> <p>0b11: Reserved</p>



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO	2:0	<p>I<sup>2</sup>C-to-I<sup>2</sup>C slave timeout setting.</p> <p>Internal GMSL2 I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p>	<p>0b000: 16μs</p> <p>0b001: 1ms</p> <p>0b010: 2ms</p> <p>0b011: 4ms</p> <p>0b100: 8ms</p> <p>0b101: 16ms</p> <p>0b110: 32ms</p> <p>0b111: Disabled</p>

**I2C\_1 (0x41)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	0b0	0b101			–	0b110		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	<p>I<sup>2</sup>C-to-I<sup>2</sup>C master bit rate setting.</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device on the remote side from the external I<sup>2</sup>C master).</p> <p>Set this according to the I<sup>2</sup>C speed mode.</p>	<p>0b000: 9.92Kbps - Set for I<sup>2</sup>C Standard mode speed</p> <p>0b001: 33.2Kbps - Set for I<sup>2</sup>C Standard mode speed</p> <p>0b010: 99.2Kbps - Set for I<sup>2</sup>C Standard or Fast-mode speed</p> <p>0b011: 123Kbps - Set for I<sup>2</sup>C Fast-mode speed</p> <p>0b100: 203Kbps - Set for I<sup>2</sup>C Fast-mode speed</p> <p>0b101: 397Kbps - Set for I<sup>2</sup>C Fast or Fast-mode Plus speed</p> <p>0b110: 625Kbps - Set for I<sup>2</sup>C Fast-mode Plus speed</p> <p>0b111: 980Kbps - Set for I<sup>2</sup>C Fast-mode Plus speed</p>
MST_TO	2:0	<p>I<sup>2</sup>C-to-I<sup>2</sup>C master timeout setting.</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p>	<p>0b000: 16μs</p> <p>0b001: 1ms</p> <p>0b010: 2ms</p> <p>0b011: 4ms</p> <p>0b100: 8ms</p> <p>0b101: 16ms</p> <p>0b110: 32ms</p> <p>0b111: Disabled</p>

**I2C\_2 (0x42)\***

BIT	7	6	5	4	3	2	1	0
Field				SRC_A[6:0]				–
Reset				0b0000000				–
Access Type				Write, Read				–

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITLEFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I <sup>2</sup> C address translator source A for main control channel.  When an I <sup>2</sup> C transaction across the GMSL link has a device address matching I <sup>2</sup> C SRC_A, the device address as seen on the remote side is replaced by the device address in I <sup>2</sup> C DST_A.	0bXXXXXXX: Value of I <sup>2</sup> C SRC_A

I2C\_3 (0x43)\*

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITLEFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I <sup>2</sup> C address translator destination A for main control channel.  See the description of I <sup>2</sup> C SRC_A.	0bXXXXXXX: Value of I <sup>2</sup> C DST_A

I2C\_4 (0x44)\*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITLEFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I <sup>2</sup> C address translator source B for main control channel.  When an I <sup>2</sup> C transaction across the GMSL link has a device address matching I <sup>2</sup> C SRC_B, the device address as seen on the remote side is replaced by the device address in I <sup>2</sup> C DST_B.	0bXXXXXXX: Value of I <sup>2</sup> C SRC_B

I2C\_5 (0x45)\*

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I <sup>2</sup> C address translator destination B for main control channel.  See the description of I <sup>2</sup> C SRC_B.	0bXXXXXXX: Value of I <sup>2</sup> C DST_B

#### I2C 7 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVD
Reset	0b0	0b0	–	–	–	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	–	–	–	Read Clears All	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
UART_RX_OVERFLOW	7	Flag to indicate overflow of the UART FIFO that holds data to receive from the GMSL link
UART_TX_OVERFLOW	6	Flag to indicate overflow of the UART FIFO that holds data to transmit across the GMSL link
I2C_TIMED_OUT	2	Internal I <sup>2</sup> C-to-I <sup>2</sup> C slave or master has timed out while receiving packet from remote device
REM_ACK_ACKED	1	Inverse of the I <sup>2</sup> C Ack Bit received from remote side. Set to 1 when the Ack is received.
REM_ACK_RECVD	0	I <sup>2</sup> C Ack Bit for any I <sup>2</sup> C byte is received from remote side for the previous I <sup>2</sup> C packet.

#### UART\_0 (0x48)\*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	0b01		0b0	0b0	0b0	0b01		0b0
Access Type			Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN	5	Enables UART Bypass Mode Control by Remote GPIO Pin  When set, remote chip's GPIO is used as MS pin (UART mode select).  When MS is high, chip is in bypass mode, otherwise, chip is in base mode.  In bypass mode, the UART interface can only access an external UART interface through the MFP pins, and cannot access the control channel. In base mode, the control channel access is enabled.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
LOC_MS_EN	4	<p>Enables UART bypass mode control by local GPIO pin</p> <p>Set to use GPIO2 pin as MS pin (UART mode select).</p> <p>When MS is high, chip is in bypass mode, otherwise, chip is in base mode.</p> <p>In bypass mode, the UART interface can only access an external UART interface through the MFP pins, and cannot access the control channel. In base mode, the control channel access is enabled.</p>	<p>0b0: UART bypass mode not controlled by local MS pin</p> <p>0b1: UART bypass mode controlled by local MS pin</p>
BYPASS_DIS_PAR	3	Selects whether or not to receive and send parity bit in bypass mode	<p>0b0: Receive and send parity bit in bypass mode</p> <p>0b1: Do not receive and send parity bit in bypass mode</p>
BYPASS_TO	2:1	<p>UART Soft-Bypass Timeout Duration</p> <p>When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power down.</p>	<p>0b00: 2ms</p> <p>0b01: 8ms</p> <p>0b10: 32ms</p> <p>0b11: Disabled (bypass mode active until next power cycle/PWDNB)</p>
BYPASS_EN	0	<p>Enable UART Soft-Bypass Mode</p> <p>Bypass mode remains active as long as there is UART activity.</p> <p>When there is no UART activity for the selected duration (configured by BYPASS_TO bitfield), device exits bypass mode and the bit is automatically cleared.</p>	<p>0b0: UART soft-bypass mode disabled</p> <p>0b1: UART soft-bypass mode enabled</p>

#### UART 1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB[7:0]							
Reset	0x96							
Access Type	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
BITLEN_LSB	7:0	UART detected bit length, low 8 bits. Detected UART pin BAUD rate in terms of 150MHz clock cycles.			0xXX: UART detected bit length, low 8 bits			

#### UART 2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
Reset	0b10		0b000000					
Access Type	Write, Read		Read Only					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
OUT_DELAY	7:6	UART initial output delay In base mode, first received UART byte of a packet (Sync or Ack frame) is delayed by the configured number of bit times to output the UART frames of the same packet back to back on remote side. This delay avoids a gap between the first byte and remaining bytes.
BITLEN_MSB	5:0	UART detected bit length, high 6 bits. Detected UART pin BAUD rate in terms of 150MHz clock cycles.

#### I2C\_PT\_0 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_PT	5:4	Pass-Through 1 and 2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Setup and Hold-Time Setting (Setup, Hold)  Configures the interval between SDA and SCL transitions when driven by the internal I <sup>2</sup> C slave.	0b00: Set for I <sup>2</sup> C Fast-mode Plus speed (1Mbps) 0b01: Set for I <sup>2</sup> C Fast-mode speed (400Kbps) 0b10: Set for I <sup>2</sup> C Standard-mode speed (100Kbps) 0b11: Reserved
SLV_TO_PT	2:0	Pass-Through 1 and 2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Timeout Setting  Internal GMSL2 I <sup>2</sup> C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16μs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

#### I2C\_PT\_1 (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
Reset	0b0	0b101			–	0b110		
Access Type		Write, Read			–	Write, Read		

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT	6:4	<p>Pass-Through 1 and 2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit-Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate (SCL clock frequency) used by the internal I<sup>2</sup>C master (in the device on the remote side from the external I<sup>2</sup>C master).</p> <p>Set according to the I<sup>2</sup>C speed mode.</p>	<p>0b000: 9.92Kbps - Set for I<sup>2</sup>C Standard mode speed</p> <p>0b001: 33.2Kbps - Set for I<sup>2</sup>C Standard mode speed</p> <p>0b010: 99.2Kbps - Set for I<sup>2</sup>C Standard or Fast-mode speed</p> <p>0b011: 123Kbps - Set for I<sup>2</sup>C Fast-mode speed</p> <p>0b100: 203Kbps - Set for I<sup>2</sup>C Fast-mode speed</p> <p>0b101: 397Kbps - Set for I<sup>2</sup>C Fast or Fast-mode Plus speed</p> <p>0b110: 625Kbps - Set for I<sup>2</sup>C Fast-mode Plus speed</p> <p>0b111: 980Kbps - Set for I<sup>2</sup>C Fast-mode Plus speed</p>
MST_TO_PT	2:0	<p>Pass-Through 1 and 2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p>	<p>0b000: 16μs</p> <p>0b001: 1ms</p> <p>0b010: 2ms</p> <p>0b011: 4ms</p> <p>0b100: 8ms</p> <p>0b101: 16ms</p> <p>0b110: 32ms</p> <p>0b111: Disabled</p>

#### I2C\_PT\_2 (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	I2C_TIMED_OUT_2	RSVD	RSVD	RSVD	I2C_TIMED_OUT_1	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type		Read Clears All				Read Clears All		

BITFIELD	BITS	DESCRIPTION
I2C_TIMED_OUT_2	6	In pass-through I <sup>2</sup> C channel 2, internal I <sup>2</sup> C-to-I <sup>2</sup> C slave or master has timed out while receiving packet from remote device
I2C_TIMED_OUT_1	2	In pass-through I <sup>2</sup> C channel 1, internal I <sup>2</sup> C-to-I <sup>2</sup> C slave or master has timed out while receiving packet from remote device

#### UART\_PT\_0 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	RSVD	RSVD	BITLEN_MAN_CFG_1	DIS_PAR_1	RSVD	RSVD
Reset	0b1	0b0	0b0	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Use the custom UART bit rate (selected by the BITLEN_PT_2_L - 0x548 and BITLEN_PT_2_H - 0x549 bitfields) in pass-through UART Channel 1.	<p>0b0: Use standard bit rate</p> <p>0b1: Use custom bit rate</p>
DIS_PAR_2	6	Disable parity bit in pass-through UART Channel 2	<p>0b0: Parity bit enabled</p> <p>0b1: Parity bit disabled</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MA N_CFG_1	3	Use the custom UART bit rate (selected by the BITLEN_PT_1_L - 0x54A and BITLEN_PT_1_H - 0x54B bitfields) in pass-through UART Channel 1.	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_1	2	Disable parity bit in pass-through UART Channel 1	0b0: Parity bit enabled 0b1: Parity bit disabled

**RX0 (0x50)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0b00	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Reserved. Do not use (legacy). Use register 0x161 VIDEO_PIPE_SEL instead.	

**RX0 (0x51)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0b01	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Reserved. Do not use (legacy). Use register 0x161 VIDEO_PIPE_SEL instead.	

**RX0 (0x52)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0b10	
Access Type	Write, Read	–	–	–	–	–	Write, Read	



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Reserved. Do not use (legacy). Use register 0x161 VIDEO_PIPE_SEL instead.	

**RX0 (0x53)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0b11	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Reserved. Do not use (legacy). Use register 0x161 VIDEO_PIPE_SEL instead.	

**TR0 (0x60, 0x68, 0x78)\***

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**TR1 (0x61, 0x69, 0x71, 0x79, 0x81, 0x89)\***

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					
BITLEN	START	END	DESCRIPTION		DECODE			
BW_MULT	7:6		Channel bandwidth-allocation multiplication factor		0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16			
BW_VAL	5:0		Channel bandwidth-allocation base. Used to calculate percentage of total link bandwidth used for this port.  Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.		0bXXXXXX: Channel base-bandwidth value			

**TR3 (0x63, 0x6B, 0x73, 0x7B, 0x83, 0x8B)\***

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID[2:0]		
Reset	—	—	—	—	—	0b000		
Access Type	—	—	—	—	—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel.  Default value is based on the device address set by the CFG0 pin.	0bXXX: Source ID for packets from this channel

**TR4 (0x64, 0x6C, 0x74, 0x7C, 0x84, 0x8C)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITLEN	START	END	DESCRIPTION		DECODE			
RX_SRC_SEL	7:0		Receive packets from selected sources. Each bit indicates if packets with that source ID should be received or not. This is a one-hot encoding.  For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.		0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

ARQ0 (0x6D, 0x75, 0x7D, 0x85, 0x8D)\*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	MATCH_SRC_ID	ACK_SRC_ID	EN	DIS_DBL_ACK_RET_X	–	–
Reset	0b1	0b0	0b0	0b1	0b1	0b0	–	–
Access Type			Write, Read	Write, Read	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MATCH_SRC_ID	5	Ack packet source ID checking method	0: All received Ack packets are accepted 1: Ack packet is accepted if SRC_ID of the received Ack packet matches TX_SRC_ID register
ACK_SRC_ID	4	Select what to use as SRC_ID in transmitted Ack packets	0: Use SRC_ID of the received data packet 1: Use TX_SRC_ID register
EN	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled
DIS_DBL_ACK_RET_X	2	Disable retransmission due to receiving same acknowledge twice.	0b0: Enabled 0b1: Disabled

ARQ1 (0x6E, 0x76, 0x7E, 0x86, 0x8E)\*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ stops retransmitting after trying retransmission after this many times for a single packet.	0bXXX: Binary value for number of times to retransmit
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR - 0x616) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin.  When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x6F, 0x77, 0x7F, 0x87, 0x8F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER R	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

TR0 (0x70, 0x80, 0x88)\*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

VIDEO\_RX0 (0x112, 0x124)\*

BIT	7	6	5	4	3	2	1	0
Field	LCRC_ERR	RSVD	RSVD	RSVD	RSVD	LINE_CRC_SEL	LINE_CRC_EN	DIS_PKT_DET
Reset	0b0	0b0	0b1	0b1	0b0	0b0	0b1	0b0
Access Type	Read Clears All					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR	7	Video-Line CRC Error Flag	0b0: No video line CRC error detected 0b1: Video line CRC error detected
LINE_CRC_SEL	2	Line-CRC Trigger Selection	0: Use DE 1: Use HS
LINE_CRC_EN	1	Video-Line CRC Enable	0b0: Video line CRC disabled 0b1: Video line CRC enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_PKT_DET	0	<p>Disable Packet Detector.</p> <p>Can be used when LIM_HEART is set to 1, to prevent the video pipe from timing out and resetting when no video packets are sent during long blanking intervals.</p> <p>If the video is restarted with a different bpp when the packet detector is disabled, toggle this register or the video receive enable register to make sure the video link restarts.</p>	<p>0b0: Packet detector enabled 0b1: Packet detector disabled</p>

**VIDEO\_RX3 (0x115, 0x127)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	HD_TR_MO DE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
Reset	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type		Write, Read	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HD_TR_MO DE	6	Selects whether HS, DE tracking is fully periodic or if it stops during vertical blanking during HV tracking	<p>0b0: Allow only partial periodic HS,DE tracking (stops during vertical blanking) 0b1: Allow partial periodic and full periodic HS, DE tracking</p>
DLOCKED	5	DE tracking locked	<p>0b0: DE tracking not locked 0b1: DE tracking locked</p>
VLOCKED	4	VS tracking locked	<p>0b0: VS tracking not locked 0b1: VS tracking locked</p>
HLOCKED	3	HS tracking locked	<p>0b0: HS tracking not locked 0b1: HS tracking locked</p>
DTRACKEN	2	<p>DE tracking enable (disable if FSYNC = 1)</p> <p>The system observes DE pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.</p>	<p>0b0: DE tracking disabled 0b1: DE tracking enabled</p>
VTRACKEN	1	<p>VS tracking enable (disable if FSYNC = 1)</p> <p>The system observes VS pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.</p>	<p>0b0: VS tracking disabled 0b1: VS tracking enabled</p>
HTRACKEN	0	<p>HS tracking enable (disable if FSYNC = 1)</p> <p>The system observes HS pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.</p>	<p>0b0: HSYNC tracking disabled 0b1: HSYNC tracking enabled</p>

MAX96792A

## Dual GMSL3/2 to CSI-2 Deserializer

## VIDEO\_RX6 (0x118, 0x12A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			RSVD	LIM_HEART	–	RSVD	RSVD
Reset	0b000			0b0	0b0	–	0b1	0b0
Access Type					Write, Read	–		

BITFIELD	BITS	DESCRIPTION	DECODE
LIM_HEART	3	Disable heartbeat during blanking. Heartbeat is periodic video sync packets sent from the serializer so that the deserializer video output can replicate the video timing as seen in the serializer input. It is not necessary for MIPI.	0b0: Heartbeat enabled during blanking 0b1: Heartbeat disabled during blanking

### VIDEO\_RX8 (0x11A, 0x12C)

BIT	7	6	5	4	3	2	1	0
Field	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x2			
Access Type	Read Clears All	Read Only	Read Only	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
VID_BLK_LEN_ERR	7	Video Rx video pixel data block-length error detected. A length mismatch happens when the received data length does not match what is expected for the video data bits per pixel.	0b0: No error detected 0b1: Video Rx block-length error detected
VID_LOCK	6	Video pipeline locked.  Can also read the following registers to check if MIPI TX is outputting data: csi2_tx1/2_pkt_cnt, csi2_dup1/2_pkt_cnt, phy0/1/2/3_pkt_cnt.	0b0: Video pipeline not locked 0b1: Video pipeline locked
VID_PKT_DET	5	Sufficient video Rx packet throughput detected. When LIM_HEART=0, this is at least one video packet every 100us. When LIM_HEART=1, this is at least one video packet every 10ms.	0b0: Not enough throughput 0b1: Sufficient throughput detected
VID_SEQ_ERR	4	Video Rx sequence error occurred. A sequence is an alternating 0 and 1 sent in the video packet headers. When a packet is dropped, there are two successive 0s or 1s.	0b0: No error detected 0b1: Error detected

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

VIDEO\_RX10 (0x11C, 0x12E)

BIT	7	6	5	4	3	2	1	0
Field	VID_OVER FLOW	MASK_VID EO_DE	RSVD[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Read Clears All	Write, Read						
BITLEN	BITS	DESCRIPTION			DECODE			
VID_OVERFLOW	7	Sticky bit for overflow detected in video Rx buffers, read to clear.			0: No error detected 1: Error detected			
MASK_VIDEO_DE	6	Masks video when DE is low			0x0: Do not mask when DE is low 0x1: Mask when DE is low			

VIDEO\_PIPE\_EN (0x160)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VIDEO_PIPE_EN[1:0]	
Reset	–	–	–	–	–	–	0b11	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_EN	1:0	Enables for video pipes	Bit 0 is enabled for Pipe Y, bit 1 is enabled for Pipe Z

VIDEO\_PIPE\_SEL (0x161)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	VIDEO_PIPE_SEL_Z[2:0]			VIDEO_PIPE_SEL_Y[2:0]		
Reset	–	–	0b110			0b010		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_Z	5:3	Selects the incoming stream ID to receive in Video Pipe Z	0x0: Link A stream ID 00 0x1: Link A stream ID 01 0x2: Link A stream ID 10 0x3: Link A stream ID 11 0x4: Link B stream ID 00 0x5: Link B stream ID 01 0x6: Link B stream ID 10 0x7: Link B stream ID 11
VIDEO_PIPE_SEL_Y	2:0	Selects the incoming stream ID to receive in Video Pipe Y	0x0: Link A stream ID 00 0x1: Link A stream ID 01 0x2: Link A stream ID 10 0x3: Link A stream ID 11 0x4: Link B stream ID 00 0x5: Link B stream ID 01 0x6: Link B stream ID 10 0x7: Link B stream ID 11



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

LINK\_SEL (0x162)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPI_LINK_SELECT	UART_2_LINK_SELECT	UART_1_LINK_SELECT	UART_0_LINK_SELECT
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LINK_SELECT	3	Selects link connection for SPI Port	0x0: Link A 0x1: Link B
UART_2_LINK_SELECT	2	UART Pass-Through 2 Link Connection Select	0x0: Link A 0x1: Link B
UART_1_LINK_SELECT	1	UART Pass-Through 1 Link Connection Select	0x0: Link A 0x1: Link B
UART_0_LINK_SELECT	0	Control Channel UART Link Connection Select	0x0: Link A 0x1: Link B

SPI\_0 (0x170)\*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNORE_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0b00		0b00		0b1	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Program to local ID if filtering packets based on header ID.	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_CC_TRG_ID	5:4	ID for GMSL2 header in SPI control-channel bridge mode	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_IGNORE_ID	3	Selects if SPI should use or ignore header ID to decide on packet acceptance	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_CC_EN	2	Enable control-channel SPI bridge function	0b0: SPI bridge disabled 0b1: SPI bridge enabled
MST_SLVN	1	Selects if SPI is master or slave	0b0: SPI slave 0b1: SPI master
SPI_EN	0	Enable SPI channel	0b0: SPI channel disabled 0b1: SPI channel enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

SPI\_1 (0x171)\*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
Reset	0b000111						0b01	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Sets the packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value more than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes ... 0b111111: Packet size is 127 bytes
SPI_BASE_PRIO	1:0	Starting GMSL2 request priority, advances by 1 (if room) if Tx buffer is over half-full.	

SPI\_2 (0x172)\*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0b000			0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Hold off transmitting data across GMSL link until this number of extra bytes are received on SPI port.	0b00: No extra bytes 0b01: 1 extra byte 0b10: 2 extra bytes 0b11: 3 extra bytes
FULL_SCK_SETUP	4	Sample MISO after half- or full-SCK period.	0b0: MISO sampled after half-SCK period 0b1: MISO sampled after full-SCK period
SPI_MOD3_F	3	Allows the suppression of an extra SCK prior to SS deassertion when SPI mode 3 is selected.	0b0: Extra SCK present prior to SS deassertion when in SPI mode 3 0b1: Extra SCK suppressed prior to SS deassertion when in SPI mode 3
SPI_MOD3	2	Selects SPI mode 0 or 3. In both modes, data is sampled on the rising clock edge and shifted out on the falling edge.	0b0: SPI mode 0. Clock polarity and phase are 0. Slave select asserts when clock is low. 0b1: SPI mode 3. Clock polarity and phase are 1. Slave select asserts when clock is high.
SPIM_SS2_ACT_H	1	Sets the polarity for SS2 when the SPI is a master.	0b0: Slave select 2 is active low 0b1: Slave select 2 is active high
SPIM_SS1_ACT_H	0	Sets the polarity for SS1 when the SPI is a master.	0b0: Slave select 1 is active low 0b1: Slave select 1 is active high

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**SPI\_3 (0x173)\***

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between: <ul style="list-style-type: none"> <li>• Assertion of SS and start of SCK pulses</li> <li>• End of SCK pulses and deassertion of SS</li> <li>• Deassertion of SS and reassertion of SS (if necessary)</li> </ul>			0xXX: Number of clock delays			

**SPI\_4 (0x174)\***

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time.			0xXX: Number of clocks for SCK low time			

**SPI\_5 (0x175)\***

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time.			0xXX: Number of clocks for SCK high time			

**SPI\_6 (0x176)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION			DECODE			
BNE	5	Alternate GPU status register to use for BNE status if GPIO is not available			0b0: Buffer empty 0b1: Buffer not empty			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
SPIS_RWN	4	Alternate GPU control register to use for read and write control if GPIO is not available.	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enable GPIO for use as Slave Select 2 output.	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
SS_IO_EN_1	2	Enable GPIO for use as Slave Select 1 output.	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
BNE_IO_EN	1	Enable GPIO for use as BNE output for SPI data available status.	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function
RWN_IO_EN	0	Enable GPIO for use as RO input for control of SPI data movement.	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function

SPI 7 (0x177)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	RO_ALT	SPIS_BYTE_CNT[4:0]				
Reset	0b0	0b0	0b0	0b00000				
Access Type	Read Clears All	Read Clears All	Write, Read	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	SPI Rx buffer overflow flag	0b0: No SPI Rx buffer overflow 0b1: SPI Rx buffer overflow
SPI_TX_OVRFLW	6	SPI Tx buffer overflow flag	0b0: No SPI Tx buffer overflow 0b1: SPI Tx buffer overflow
RO_ALT	5	When set to 1, use the alternative pin for RO	
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer	0bXXXXX: Number of bytes available

SPI 8 (0x178)\*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100nS increments) for GMSL2 request hold off (0 is disable).	0xXX: Number of 100nS delay increments for GMSL2 request hold off

WM 0 (0x190)\*

BIT	7	6	5	4	3	2	1	0
Field	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
Reset	0b0	0b000			0b00		–	0b0
Access Type	Write, Read	Write, Read			Write, Read		–	Write, Read

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
WM_LEN	7	Watermark Length	0b0: 32-bit 0b1: 64-bit
WM_MODE	6:4	Watermark Mode	0b000: Default generator mode - cycle through all 4 watermarks in video stream 0b001: Error generator mode - cycle through only 2 watermarks to replicate a frozen frame error condition 0b010: Reserved 0b011: Reserved 0b100: Reserved 0b101: Reserved 0b110: Reserved 0b111: Reserved
WM_DET	3:2	Watermark Detection/Generation	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WM_EN	0	Watermark Enable	0b0: Watermarking disabled 0b1: Watermarking enabled

**WM\_2 (0x192)\***

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
Reset	–	0b101			0b0	0b0	0b00	
Access Type	–				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HsyncPol	3	HS Polarity	0b0: Noninverting 0x1: Invert
VsyncPol	2	VS Polarity	0b0: Noninverting 0x1: Invert
WM_NPFILT	1:0	Phase accumulator terminal count	0xXX: Counter value

**WM\_4 (0x194)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
Reset	–	–	0b01		0b0	–	0b00	
Access Type	–	–				–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WM_MASKMODE	1:0	Sets watermark video mask behavior for the device	0b00: Mask video if WM is detected 0b01: Mask video if WM is detected, blank if error is detected 0b10: Reserved b011: Reserved

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

WM\_5 (0x195)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	WM_DETO UT	WM_ERRO R
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–		Read Only	Read Only

BITLED	BITS	DESCRIPTION	DECODE
WM_DETOU T	1	Live value of frame-based detection output	0b0: Watermark not detected 0b1: Watermark detected
WM_ERROR	0	Live value of active-high watermark error	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.

WM\_6 (0x196)

BIT	7	6	5	4	3	2	1	0
Field	WM_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITLED	BITS	DESCRIPTION	DECODE
WM_TIMER	7:0	Time (in 2ms steps) the frozen-frame condition must be observed before an error is generated.  0 = No filter	0xXX: Number of milliseconds

WM\_WREN\_0 (0x1AE)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITLED	BITS	DESCRIPTION	DECODE
WM_WREN_ L	7:0	Works in conjunction with WM_WREN_H to enable writing to watermark registers.  Writing is enabled to watermark registers when 0xBA is written to WM_WREN_L and 0xDC is written to WM_WREN_H registers. Otherwise, watermark registers are read-only.	0xBA: Enables writing to WM registers Others: WM registers remain read-only

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

WM\_WREN\_1 (0x1AF)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEVEL	BITS	DESCRIPTION			DECODE			
WM_WREN_H	7:0	<p>Works in conjunction with WM_WREN_L to enable writing to watermark registers.</p> <p>Writing is enabled to watermark registers when 0xBA is written to WM_WREN_L and 0xDC is written to WM_WREN_H registers. Otherwise, watermark registers are read-only.</p>			<p>0xDC: Enables writing to WM registers Others: WM registers remain read-only</p>			

CROSS\_0 (0x1E0, 0x200)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0b0	0b0	0b00000				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITLEVEL	BITS	DESCRIPTION			DECODE			
CROSS0_I	6	Invert outgoing bit 0			<p>0b0: Do not invert bit 0b1: Invert bit</p>			
CROSS0_F	5	Force outgoing bit 0 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			<p>0b0: Do not force bit to zero 0b1: Force bit to zero</p>			
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0			0bXXXXX: Incoming bit position			

CROSS\_1 (0x1E1, 0x201)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0b0	0b0	0b00001				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITLEVEL	BITS	DESCRIPTION			DECODE			
CROSS1_I	6	Invert outgoing bit 1			<p>0b0: Do not invert bit 0b1: Invert bit</p>			
CROSS1_F	5	Force outgoing bit 1 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			<p>0b0: Do not force bit to zero 0b1: Force bit to zero</p>			
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1			0bXXXXX: Incoming bit position			



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

CROSS\_2 (0x1E2, 0x202)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0b0	0b0	0b00010				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS2_I	6	Invert outgoing bit 2			0b0: Do not invert bit 0b1: Invert bit			
CROSS2_F	5	Force outgoing bit 2 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2			0bXXXXX: Incoming bit position			

CROSS\_3 (0x1E3, 0x203)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0b0	0b0	0b00011				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS3_I	6	Invert outgoing bit 3			0b0: Do not invert bit 0b1: Invert bit			
CROSS3_F	5	Force outgoing bit 3 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3			0bXXXXX: Incoming bit position			

CROSS\_4 (0x1E4, 0x204)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0b0	0b0	0b00100				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS4_I	6	Invert outgoing bit 4			0b0: Do not invert bit 0b1: Invert bit			
CROSS4_F	5	Force outgoing bit 4 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4			0bXXXXX: Incoming bit position			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

CROSS\_5 (0x1E5, 0x205)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0b0	0b0	0b00101				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS5_I	6	Invert outgoing bit 5			0b0: Do not invert bit 0b1: Invert bit			
CROSS5_F	5	Force outgoing bit 5 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5			0bXXXXX: Incoming bit position			

CROSS\_6 (0x1E6, 0x206)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0b0	0b0	0b00110				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS6_I	6	Invert outgoing bit 6			0b0: Do not invert bit 0b1: Invert bit			
CROSS6_F	5	Force outgoing bit 6 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6			0bXXXXX: Incoming bit position			

CROSS\_7 (0x1E7, 0x207)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0b0	0b0	0b00111				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS7_I	6	Invert outgoing bit 7			0b0: Do not invert bit 0b1: Invert bit			
CROSS7_F	5	Force outgoing bit 7 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7			0bXXXXX: Incoming bit position			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

CROSS\_8 (0x1E8, 0x208)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0b0	0b0	0b01000				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS8_I	6	Invert outgoing bit 8			0b0: Do not invert bit 0b1: Invert bit			
CROSS8_F	5	Force outgoing bit 8 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8			0bXXXXX: Incoming bit position			

CROSS\_9 (0x1E9, 0x209)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0b0	0b0	0b01001				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS9_I	6	Invert outgoing bit 9			0b0: Do not invert bit 0b1: Invert bit			
CROSS9_F	5	Force outgoing bit 9 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9			0bXXXXX: Incoming bit position			

CROSS\_10 (0x1EA, 0x20A)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0b0	0b0	0b01010				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS10_I	6	Invert outgoing bit 10			0b0: Do not invert bit 0b1: Invert bit			
CROSS10_F	5	Force outgoing bit 10 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10			0bXXXXX: Incoming bit position			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

CROSS\_11 (0x1EB, 0x20B)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0b0	0b0	0b01011				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS11_I	6	Invert outgoing bit 11			0b0: Do not invert bit 0b1: Invert bit			
CROSS11_F	5	Force outgoing bit 11 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11			0bXXXXX: Incoming bit position			

CROSS\_12 (0x1EC, 0x20C)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0b0	0b0	0b01100				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS12_I	6	Invert outgoing bit 12			0b0: Do not invert bit 0b1: Invert bit			
CROSS12_F	5	Force outgoing bit 12 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12			0bXXXXX: Incoming bit position			

CROSS\_13 (0x1ED, 0x20D)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0b0	0b0	0b01101				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS13_I	6	Invert outgoing bit 13			0b0: Do not invert bit 0b1: Invert bit			
CROSS13_F	5	Force outgoing bit 13 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13	0bXXXXX: Incoming bit position

**CROSS\_14 (0x1EE, 0x20E)\***

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0b0	0b0	0b01110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Invert outgoing bit 14	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Force outgoing bit 14 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14	0bXXXXX: Incoming bit position

**CROSS\_15 (0x1EF, 0x20F)\***

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0b0	0b0	0b01111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Invert outgoing bit 15	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Force outgoing bit 15 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15	0bXXXXX: Incoming bit position

**CROSS\_16 (0x1F0, 0x210)\***

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0b0	0b0	0b10000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Invert outgoing bit 16	0b0: Do not invert bit 0b1: Invert bit

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_F	5	Force outgoing bit 16 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16	0bXXXXX: Incoming bit position

**CROSS 17 (0x1F1, 0x211)\***

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0b0	0b0	0b10001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Invert outgoing bit 17	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Force outgoing bit 17 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17	0bXXXXX: Incoming bit position

**CROSS 18 (0x1F2, 0x212)\***

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0b0	0b0	0b10010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Invert outgoing bit 18	0b0: Do not invert bit 0b1: Invert bit
CROSS18_F	5	Force outgoing bit 18 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18	0bXXXXX: Incoming bit position

**CROSS 19 (0x1F3, 0x213)\***

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0b0	0b0	0b10011				
Access Type	–	Write, Read	Write, Read	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Invert outgoing bit 19	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Force outgoing bit 19 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19	0bXXXXX: Incoming bit position

**CROSS 20 (0x1F4, 0x214)\***

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0b0	0b0	0b10100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Invert outgoing bit 20	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Force outgoing bit 20 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20	0bXXXXX: Incoming bit position

**CROSS 21 (0x1F5, 0x215)\***

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0b0	0b0	0b10101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Invert outgoing bit 21	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Force outgoing bit 21 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21	0bXXXXX: Incoming bit position



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

CROSS\_22 (0x1F6, 0x216)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0b0	0b0	0b10110				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS22_I	6	Invert outgoing bit 22			0b0: Do not invert bit 0b1: Invert bit			
CROSS22_F	5	Force outgoing bit 22 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22			0bXXXXX: Incoming bit position			

CROSS\_23 (0x1F7, 0x217)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0b0	0b0	0b10111				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS23_I	6	Invert outgoing bit 23			0b0: Do not invert bit 0b1: Invert bit			
CROSS23_F	5	Force outgoing bit 23 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23			0bXXXXX: Incoming bit position			

CROSS\_HS (0x1F8, 0x218)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
Reset	–	0b0	0b0	0b11000				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS_HS_I	6	Invert CROSS_HS			0b0: Do not invert bit 0b1: Invert bit			
CROSS_HS_F	5	Force CROSS_HS to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS_HS	4:0	Map selected internal signal to HS			0bXXXXX: Incoming bit position			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

CROSS\_VS (0x1F9, 0x219)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
Reset	–	0b0	0b0	0b11001				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS_VS_I	6	Invert CROSS_VS			0b0: Do not invert bit 0b1: Invert bit			
CROSS_VS_F	5	Force CROSS_VS to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS_VS	4:0	Map selected internal signal to VS			0bXXXXX: Incoming bit position			

CROSS\_DE (0x1FA, 0x21A)\*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
Reset	–	0b0	0b0	0b11010				
Access Type	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
CROSS_DE_I	6	Invert CROSS_DE			0b0: Do not invert bit 0b1: Invert bit			
CROSS_DE_F	5	Force CROSS_DE to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.			0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS_DE	4:0	Map selected internal signal to DE			0bXXXXX: Incoming bit position			

PRBS\_ERR (0x1FB, 0x21B)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BITFIELD	BITS	DESCRIPTION			DECODE			
VPRBS_ERR	7:0	Video PRBS error counter, clears on read			0xXX: Number of video PRBS errors since last read			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**VPRBS (0x1FC, 0x21C)\***

BIT	7	6	5	4	3	2	1	0
Field	PATGEN_CLK_SRC	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	RSVD	VIDEO_LOCK
Reset	0b1	–	0b0	0b0	–	–	0b0	0b0
Access Type	Write, Read	–	Read Only	Write, Read	–	–		Read Only

BITLEN	BIT	DESCRIPTION	DECODE
PATGEN_CLK_SRC	7	Pattern-generator clock source for video PRBS 7, 9, 24, checkerboard, and gradient patterns. Bit 1 of the PIN_DRV_EN_0 register must be set to 1 for this register to take effect. If it is set to 0, then PIN_DRV_EN_0 bit 0 is used to select between a 75MHz clock (when 1) and 25MHz clk (when 0).	0x0: 150MHz 0x1: 600MHz (default)
VPRBS_FAIL	5	Video PRBS check pass/fail	0b0: Video PRBS check passed 0b1: Video check failed
VPRBS_CHK_EN	4	Enable video PRBS checker	0b0: Video PRBS checker disabled 0b1: Video PRBS checker enabled
VIDEO_LOCK	0	Video channel is locked and outputting valid video data	0b0: Video channel not locked 0b1: Video channel locked

**CROSS\_27 (0x1FD, 0x21D)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD	CROSS27_I	CROSS27_F	CROSS27[4:0]				
Reset	0b0	0b0	0b0	0b11011				
Access Type		Write, Read	Write, Read	Write, Read				

BITLEN	BIT	DESCRIPTION	DECODE
CROSS27_I	6	Invert outgoing bit 27	0b0: Do not invert bit 0b1: Invert bit
CROSS27_F	5	Force outgoing bit 27 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS27	4:0	Maps incoming bit position set by this field to the outgoing bit position 27	0bXXXXX: Incoming bit position

**CROSS\_28 (0x1FE, 0x21E)**

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
Reset	–	0b0	0b0	0b11100				
Access Type	–	Write, Read	Write, Read	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS28_I	6	Invert outgoing bit 28	0b0: Do not invert bit 0b1: Invert bit
CROSS28_F	5	Force outgoing bit 28 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS28	4:0	Maps incoming bit position set by this field to the outgoing bit position 28	0bXXXXX: Incoming bit position

#### CROSS 29 (0x1FF, 0x21F)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
Reset	–	0b0	0b0	0b11101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS29_I	6	Invert outgoing bit 29	0b0: Do not invert bit 0b1: Invert bit
CROSS29_F	5	Force outgoing bit 29 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS29	4:0	Maps incoming bit position set by this field to the outgoing bit position 29	0bXXXXX: Incoming bit position

#### PATGEN 0 (0x240)

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b11	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_VS	7	Enable to generate VS output according to the timing definition programmed in the registers in the VRX_PATGEN block	0b0: Do not generate VS 0b1: Generate VS
GEN_HS	6	Enable to generate HS output according to the timing definition programmed in the registers in the VRX_PATGEN block	0b0: Do not generate HS 0b1: Generate HS
GEN_DE	5	Enable to generate DE output according to the timing definition programmed in the registers in the VRX_PATGEN block	0b0: Do not generate DE 0b1: Generate DE
VS_INV	4	Invert VSYNC output of video-timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INV	3	Invert HSYNC output of video-timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INV	2	Invert DE output of video-timing generator	0b0: Do not invert DE 0b1: Invert DE

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
VTG_MODE	1:0	<p>Video-Timing Generation Mode</p> <p>VS input edge triggers the generation of continuous frames of VSO/HSO/DEO even if no more VS input edges.</p> <p>If the next VS input edge comes earlier or later than expected by VS period, the newly-generated frame is correct.</p> <p>The current VSO/HSO/DEO is cut or extended at the time of the rising edge of the newly-generated VSO/HSO/DEO.</p>	<p>0b00: VS-tracking mode VS input's period (VS_HIGH + VS_LOW) is tracked. After VS tracking is locked, any VS input edge (glitches) not in the expected PCLK cycle is ignored. VS tracking is locked with three consecutive matches and unlocked by three consecutive mismatches. When unlocked or at power-up, the next VS input edge is assumed to be the right VS edge.</p> <p>0b01: VS on trigger mode One VS input edge triggers the generation of one frame of VSO/HSO/DEO. If the next VS input edge comes earlier or later than expected by VS period, the newly-generated frame is correct. The current VSO/HSO/DEO is cut or extended at the time of the rising edge of the newly-generated VSO/HSO/DEO.</p> <p>0b10: Auto-repeat mode VS input edge triggers the generation of continuous frames of VSO/HSO/DEO even if no more VS input edges. If the next VS input edge comes earlier or later than expected by VS period, the newly-generated frame is correct. The current VSO/HSO/DEO is cut or extended at the time of the rising edge of the newly-generated VSO/HSO/DEO.</p> <p>0b11: Free-running mode Automatically starts generating the pattern relying on VS input.</p>

#### PATGEN\_1 (0x241)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIG
Reset	0b0	–	0b00		–	–	–	0b0
Access Type	Write, Read	–	Write, Read		–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_MODE	7	Gradient Pattern-Generator Mode	<p>0b0: Gradient mode increasing. Each gradient color starts from a value of 0x00 and increases to 0xFF.</p> <p>0b1: Gradient mode decreasing. Each gradient color starts from a value of 0xFF and decreases to 0x00.</p>
PATGEN_MODE	5:4	Pattern-Generator Mode	<p>0b00: Pattern generator disabled (use video from the serializer input (default)).</p> <p>0b01: Generate checkerboard pattern</p> <p>0b10: Generate gradient pattern</p> <p>0b11: Reserved</p>
VS_TRIG	0	Select VS trigger edge	<p>0b0: Falling edge</p> <p>0b1: Rising edge</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

VS\_DLY\_2 (0x242)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_2	7:0	VS delay in terms of PCLK cycles The generated output VS is delayed by VS_DELAY cycles from the input VS. ([23:16])	0xXX: Most significant byte of VS delay

VS\_DLY\_1 (0x243)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_1	7:0	VS delay in terms of PCLK cycles The generated output VS is delayed by VS_DELAY cycles from the input VS. ([15:8])	0xXX: Middle significant byte of VS delay

VS\_DLY\_0 (0x244)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_0	7:0	VS delay in terms of PCLK cycles The generated output VS is delayed by VS_DELAY cycles from the input VS. ([7:0])	0xXX: Least significant byte of VS delay

VS\_HIGH\_2 (0x245)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_2	7:0	VS high period in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS high period

#### VS\_HIGH\_1 (0x246)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_1	7:0	VS high period in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS high period

#### VS\_HIGH\_0 (0x247)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_0	7:0	VS high period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of VS high period

#### VS\_LOW\_2 (0x248)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_2	7:0	VS low period in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS low period

#### VS\_LOW\_1 (0x249)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_1	7:0	VS low period in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS low period



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

VS\_LOW\_0 (0x24A)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_0	7:0	VS low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of VS low period

V2H\_2 (0x24B)

BIT	7	6	5	4	3	2	1	0
Field	V2H_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_2	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS edge to first HS rising edge

V2H\_1 (0x24C)

BIT	7	6	5	4	3	2	1	0
Field	V2H_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_1	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS edge to first HS rising edge

V2H\_0 (0x24D)

BIT	7	6	5	4	3	2	1	0
Field	V2H_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_0	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of VS edge to first HS rising edge

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

HS\_HIGH\_1 (0x24E)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
HS_HIGH_1	7:0	HS high period in terms of PCLK cycles ([15:8])			0xXX: Most significant byte of HS high period			

HS\_HIGH\_0 (0x24F)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
HS_HIGH_0	7:0	HS high period in terms of PCLK cycles ([7:0])			0xXX: Least significant byte of HS high period			

HS\_LOW\_1 (0x250)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
HS_LOW_1	7:0	HS low period in terms of PCLK cycles ([15:8])			0xXX: Most significant byte of HS low period			

HS\_LOW\_0 (0x251)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
HS_LOW_0	7:0	HS low period in terms of PCLK cycles ([7:0])			0xXX: Least significant byte of HS low period			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[HS\\_CNT\\_1 \(0x252\)](#)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_1	7:0	HS pulses per frame ([15:8])	0xXX: Most significant byte of HS pulses per frame

[HS\\_CNT\\_0 \(0x253\)](#)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_0	7:0	HS pulses per frame [7:0]	0xXX: Least significant byte of HS pulses per frame

[V2D\\_2 \(0x254\)](#)

BIT	7	6	5	4	3	2	1	0
Field	V2D_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_2	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS edge to first DE

[V2D\\_1 \(0x255\)](#)

BIT	7	6	5	4	3	2	1	0
Field	V2D_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_1	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS edge to first DE

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

V2D\_0 (0x256)

BIT	7	6	5	4	3	2	1	0
Field	V2D_0[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
V2D_0	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles ([23:16])			0xXX: Least significant byte of VS edge to first DE			

DE\_HIGH\_1 (0x257)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
DE_HIGH_1	7:0	DE high period in terms of PCLK cycles ([15:8])			0xXX: Most significant byte of DE high period			

DE\_HIGH\_0 (0x258)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
DE_HIGH_0	7:0	DE high period in terms of PCLK cycles ([7:0])			0xXX: Least significant byte of DE high period			

DE\_LOW\_1 (0x259)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
DE_LOW_1	7:0	DE low period in terms of PCLK cycles ([15:8])			0xXX: Most significant byte of DE low period			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

DE\_LOW\_0 (0x25A)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_0	7:0	DE low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of DE low period

DE\_CNT\_1 (0x25B)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_1	7:0	Active lines per frame ([15:8])	0xXX: Most significant byte of DE pulses per frame

DE\_CNT\_0 (0x25C)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_0	7:0	Active lines per frame ([7:0])	0xXX: Least significant byte of DE pulses per frame

GRAD\_INCR (0x25D)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_INCR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_INCR	7:0	Gradient mode increment amount (increment amount is the register value divided by 4). Each successive pixel's value in a line increments by this amount divided by 4.	0xXX: Gradient increment base

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

CHKR\_COLOR\_A\_L (0x25E)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_L[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_COLOR_A_L	7:0	Checkerboard mode Color A low byte			0xXX: Least significant byte of checkerboard mode Color A			

CHKR\_COLOR\_A\_M (0x25F)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_M[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_COLOR_A_M	7:0	Checkerboard mode Color A middle byte			0xXX: Middle significant byte of checkerboard mode Color A			

CHKR\_COLOR\_A\_H (0x260)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_H[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_COLOR_A_H	7:0	Checkerboard mode Color A high byte			0xXX: Most significant byte of checkerboard mode Color A			

CHKR\_COLOR\_B\_L (0x261)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_L[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_COLOR_B_L	7:0	Checkerboard mode Color B low byte			0xXX: Least significant byte of checkerboard mode Color B			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[CHKR\\_COLOR\\_B\\_M \(0x262\)](#)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_M[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_COLOR_B_M	7:0	Checkerboard mode Color B middle byte			0xXX: Middle significant byte of checkerboard mode Color B			

[CHKR\\_COLOR\\_B\\_H \(0x263\)](#)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_H[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_COLOR_B_H	7:0	Checkerboard mode Color B high byte			0xXX: Most significant byte of checkerboard mode Color B			

[CHKR\\_RPT\\_A \(0x264\)](#)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_A[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_RPT_A	7:0	Checkerboard mode Color A repeat count			0xXX: Repeat count of checkerboard mode Color A			

[CHKR\\_RPT\\_B \(0x265\)](#)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_B[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_RPT_B	7:0	Checkerboard mode Color B repeat count			0xXX: Repeat count of checkerboard mode Color B			



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**CHKR\_ALT (0x266)**

BIT	7	6	5	4	3	2	1	0
Field	CHKR_ALT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITLEN	BIT	DESCRIPTION	DECODE
CHKR_ALT	7:0	Checkerboard mode alternate line count. Number of successive video lines that have the color A before switching to color B, and vice versa.	0xXX: Checkerboard mode alternate line count

**GPIO\_A (0x2B0)\***

GPIO 0

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITLEN	BIT	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x2B1)\***

GPIO 0

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00000				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x2B2)\*

GPIO 0

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00000				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value from across the GMSL link	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x2B3)\*

GPIO 1

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

#### GPIO B (0x2B4)\*

GPIO 1

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00001				
Access Type	Write, Read		Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration			0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved			
OUT_TYPE	5	Driver type selection			0b0: Open-drain 0b1: Push-pull			
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

#### GPIO C (0x2B5)\*

GPIO 1

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00001				
Access Type	Write, Read		–	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITLEFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO A (0x2B6)\*

GPIO 2

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITLEFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

#### GPIO B (0x2B7)\*

GPIO 2

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b00		0b1	0b00010				
Access Type	Write, Read		Write, Read	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO C (0x2B8)\*

GPIO 2

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00010				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO A (0x2B9)\*

GPIO 3

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

#### GPIO\_B (0x2BA)\*

GPIO 3

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b00		0b1	0b00011				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x2BB)\*

GPIO 3

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00011				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**GPIO\_A (0x2BC)\***

GPIO 4

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x2BD)\***

GPIO 4

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00100				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x2BE)\***

GPIO 4



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00100				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO A (0x2BF)\*

GPIO 5

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

#### GPIO B (0x2C0)\*

GPIO 5

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00101				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x2C1)\*

GPIO 5

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00101				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x2C2)\*

GPIO 6

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO B (0x2C3)\***

GPIO 6

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00110				
Access Type	Write, Read		Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration		0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved				
OUT_TYPE	5	Driver type selection		0b0: Open-drain 0b1: Push-pull				
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting		0bXXXXX: This GPIO transmit ID				

**GPIO C (0x2C4)\***

GPIO 6

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	—	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	—	0b00110				
Access Type	Write, Read		—	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO A (0x2C5)\*

GPIO 7

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

#### GPIO B (0x2C6)\*

GPIO 7

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00111				
Access Type	Write, Read		Write, Read	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO C (0x2C7)\*

GPIO 7

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00111				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO A (0x2C8)\*

GPIO 8

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

#### GPIO\_B (0x2C9)\*

GPIO 8

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01000				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x2CA)\*

GPIO 8

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01000				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**GPIO\_A (0x2CB)\***

GPIO 9

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x2CC)\***

GPIO 9

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01001				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x2CD)\***

GPIO 9



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01001				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO A (0x2CE)\*

GPIO 10

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

#### GPIO B (0x2CF)\*

GPIO 10

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01010				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x2D0)\*

GPIO 10

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01010				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x2D1)\*

GPIO 11

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO B (0x2D2)\***

GPIO 11

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01011				
Access Type	Write, Read		Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration		0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved				
OUT_TYPE	5	Driver type selection		0b0: Open-drain 0b1: Open-drain				
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting		0bXXXXX: This GPIO transmit ID				

**GPIO C (0x2D3)\***

GPIO 11

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	—	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	—	0b01011				
Access Type	Write, Read		—	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO A (0x2D4)\*

GPIO 12

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

#### GPIO B (0x2D5)\*

GPIO 12

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01100				
Access Type	Write, Read		Write, Read	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer Pullup/Pulldown Configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Open-drain
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x2D6)\*

GPIO 12

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01100				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting.  When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO.  When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### CMU2 (0x302)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	PFDDIV_RSHORT[2:0]			RSVD	RSVD[1:0]		RSVD
Reset	0b0	0b000			0b0	0b00		0b0
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PFDDIV_RSHORT	6:4	PFDDIV regulator voltage control. Controls the supply voltage to the 6GHz clock generation PLL phase detector and dividers.	0: VREG_PFDDIV = 1.0V 1: VREG_PFDDIV = 1.1V 2: VREG_PFDDIV = 0.875V 3: VREG_PFDDIV = 0.94V 4: VREG_PFDDIV = 1.0V 5: VREG_PFDDIV = 1.1V 6: VREG_PFDDIV = 0.875V 7: VREG_PFDDIV = 0.94V

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BACKTOP1 (0x308)\***

BIT	7	6	5	4	3	2	1	0
Field	CSIPLLU_LOCK	CSIPLLZ_LOCK	CSIPLLY_LOCK	CSIPLLX_LOCK	LINE_SPL2	–	RSVD	BACKTOP_EN
Reset	0b0	0b0	0b0	0b0	0b0	–	0b0	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Write, Read	–		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLLU_LOCK	7	CSI MIPI TX PLL 3 locked (PLL for MIPI Port F in 4x2 mode)	0b0: CSI2 PLL 3 not locked 0b1: CSI2 PLL 3 locked
CSIPLLZ_LOCK	6	CSI MIPI TX PLL 2 locked (PLL for MIPI Port B in 2x4 mode, Port E in 4x2 mode)	0b0: CSI2 PLL 2 not locked 0b1: CSI2 PLL 2 locked
CSIPLLY_LOCK	5	CSI MIPI TX PLL 1 locked (PLL for MIPI Port A in 2x4 mode, Port D in 4x2 mode)	0b0: CSI2 PLL 1 not locked 0b1: CSI2 PLL 1 locked
CSIPLLX_LOCK	4	CSI MIPI TX PLL 0 locked (PLL for MIPI Port C in 4x2 mode)	0b0: CSI2 PLL 0 not locked 0b1: CSI2 PLL 0 locked
LINE_SPL2	3	Line based distribution to line memories for Video Pipeline Z. When set, even-numbered video lines are stored in one-line buffer memory array, odd lines are stored in another.	0b0: Disable line-based distribution to line memories for Video Pipeline Z 0b1: Enable line-based distribution to line memories for Video Pipeline Z
BACKTOP_EN	0	Backtop (line-buffer memory) write logic enable. Setting to 0 stops data output from the MIPI transmitter.	0b0: Disable writes to BACKTOP (line buffer) memories 0b1: Enable writes to BACKTOP (line buffer) memories

**BACKTOP4 (0x30B)\***

BIT	7	6	5	4	3	2	1	0
Field	VS_VC2_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC2_L	7:0	For each video frame, override whether Frame Start-End short packets are sent out for each VC. Pipe Y/MIPI output A.  When register is set to 0, there is no override. When not set to 0, each of the 16 bits enables Frame Start-End short packets for virtual channels 0-15. For example bit 0 set to 1 enables packets for VC0, bit 1 enables packets for VC1, etc.	0bXXXXXXXX1: Override to enable packets for VC0 0bXXXXXXXX1X: Override to enable packets for VC1 0bXXXXXX1XX: Override to enable packets for VC2 etc...

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BACKTOP5 (0x30C)\***

BIT	7	6	5	4	3	2	1	0
Field	VS_VC2_H[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEN	BITS	DESCRIPTION			DECODE			
VS_VC2_H	7:0	<p>For each video frame, override whether Frame Start-End short packets are sent out for each VC. Pipe Y/MIPI output A.</p> <p>When register is set to 0, there is no override. When not set to 0, each of the 16 bits enables Frame Start-End short packets for virtual channels 0-15. For example bit 0 set to 1 enables packets for VC0, bit 1 enables packets for VC1, etc.</p>			<p>0bXXXXXXXX1: Override to enable packets for VC8  0bXXXXXXXX1X: Override to enable packets for VC9  0bXXXXXXXX1XX: Override to enable packets for VC10  etc...</p>			

**BACKTOP6 (0x30D)\***

BIT	7	6	5	4	3	2	1	0
Field	VS_VC3_L[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEN	BITS	DESCRIPTION			DECODE			
VS_VC3_L	7:0	<p>For each video frame, override whether Frame Start-End short packets are sent out for each VC. Pipe Z/MIPI output B.</p> <p>When register is set to 0, there is no override. When not set to 0, each of the 16 bits enables Frame Start-End short packets for virtual channels 0-15. For example bit 0 set to 1 enables packets for VC0, bit 1 enables packets for VC1, etc.</p>			<p>0bXXXXXXXX1: Override to enable packets for VC0  0bXXXXXXXX1X: Override to enable packets for VC1  0bXXXXXXXX1XX: Override to enable packets for VC2  etc...</p>			

**BACKTOP7 (0x30E)\***

BIT	7	6	5	4	3	2	1	0
Field	VS_VC3_H[7:0]							
Reset	0x00							
Access Type	Write, Read							



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC3_H	7:0	<p>For each video frame, override whether Frame Start-End short packets are sent out for each VC. Pipe Z/MIPI output B.</p> <p>When register is set to 0, there is no override. When not set to 0, each of the 16 bits enables Frame Start-End short packets for virtual channels 0-15. For example bit 0 set to 1 enables packets for VC0, bit 1 enables packets for VC1, etc.</p>	<p>0bXXXXXXX1: Override to enable packets for VC8</p> <p>0bXXXXXXX1X: Override to enable packets for VC9</p> <p>0bXXXXXX1XX: Override to enable packets for VC10</p> <p>etc...</p>

#### BACKTOP11 (0x312)

BIT	7	6	5	4	3	2	1	0
Field	–	cmd_overflow w3	cmd_overflow w2	–	–	LMO_Z	LMO_Y	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–	Read Only	Read Only	–	–	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_overflow w3	6	Pipeline Z line memory command FIFO overflow detected. FIFO is for commands sent to MIPI TX to output frame start/end and lines of pixel data.	<p>0b0: Pipeline Z no line memory command FIFO overflow</p> <p>0b1: Pipeline Z line memory command FIFO overflow</p>
cmd_overflow w2	5	Pipeline Y line memory command FIFO overflow detected. FIFO is for commands sent to MIPI TX to output frame start/end and lines of pixel data.	<p>0b0: Pipeline Y no line memory command FIFO overflow</p> <p>0b1: Pipeline Y line memory command FIFO overflow</p>
LMO_Z	2	Pipeline Z line memory overflow sticky register	<p>0b0: Pipeline Z no line memory overflow</p> <p>0b1: Pipeline Z line memory overflow</p>
LMO_Y	1	Pipeline Y line memory overflow sticky register	<p>0b0: Pipeline Y no line memory overflow</p> <p>0b1: Pipeline Y line memory overflow</p>

#### BACKTOP12 (0x313)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	CSI_OUT_EN	RSVD
Reset	–	–	–	–	–	0b0	0b1	0b0
Access Type	–	–	–	–	–		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CSI_OUT_EN	1	Enable CSI output	<p>0b0: CSI output disabled</p> <p>0x1: CSI output enabled</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BACKTOP13 (0x314)**

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_y[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–
BITFIELD	BITS	DESCRIPTION			DECODE			
soft_vc_y	7:4	Software-defined virtual channel number for Pipeline Y			0xX: Software-defined virtual channel number for Pipeline Y			

**BACKTOP14 (0x315)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	soft_vc_z[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE			
soft_vc_z	3:0	Software-defined virtual channel number for Pipeline Z			0xX: Software-defined virtual channel number for Pipeline Z			

**BACKTOP15 (0x316)**

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_y_h[1:0]		–	–	–	–	–	–
Reset	0b00		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–
BITFIELD	BITS	DESCRIPTION			DECODE			
soft_dt_y_h	7:6	High bits of software-defined data type for Pipeline Y			0bXX: High bits of software-defined data type for Pipeline Y			

**BACKTOP16 (0x317)**

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_z_h[3:0]				soft_dt_y_l[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE			
soft_dt_z_h	7:4	High bits of software-defined data type for Pipeline Z			0xX: High bits of software-defined data type for Pipeline Z			
soft_dt_y_l	3:0	Low bits of software-defined data type for Pipeline Y			0bXX: Low bits of software-defined data type for Pipeline Y			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BACKTOP17 (0x318)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	soft_dt_z_l[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
soft_dt_z_l	1:0	Low bits of software-defined data type for Pipeline Z

**BACKTOP18 (0x319)**

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_z_h[2:0]			soft_bpp_y[4:0]				
Reset	0b000			0b00000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_z_h	7:5	High bits of software-defined bpp for Pipeline Z	0bXX: High bits of software-defined bpp for Pipeline Z
soft_bpp_y	4:0	Software-defined bpp for Pipeline Y	0x8: Datatypes = x2A, x10-12, x31-37 0xA: Datatypes = x2B 0xC: Datatypes = x2C 0xE: Datatypes = x2D 0x10: Datatypes = x22, x1E, x2E, 0x12: Datatypes = x23 0x14: Datatypes = x1F, x2F 0x18: Datatypes = x24, x30

**BACKTOP19 (0x31A)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	soft_bpp_z_l[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_z_l	1:0	Low bits of software-defined bpp for Pipeline Z	0bXX: Low bits of software-defined bpp for Pipeline Z

**BACKTOP20 (0x31B)**

BIT	7	6	5	4	3	2	1	0
Field	phy0_csi_tx_dppll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY0 frequency fine-tuning. See app note.	0xXX: PHY0 frequency fine-tuning override low byte

#### BACKTOP21 (0x31C)

BIT	7	6	5	4	3	2	1	0
Field	–	bpp8dblz	bpp8dbly	–	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	–	0b0	0b0	–	0x0			
Access Type	–	Write, Read	Write, Read	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dblz	6	bpp = 8 processed as 16-bit color enable for Pipeline Z. Used to give all video data flowing through a single pipe the same bpp, to maximize capacity of video pipeline.	0b0: Do not process bpp = 8 as 16-bit color 0b1: Process bpp = 8 as 16-bit color
bpp8dbly	5	bpp = 8 processed as 16-bit color enable for Pipeline Y. Used to give all video data flowing through a single pipe the same bpp, to maximize capacity of video pipeline.	0b0: Do not process bpp = 8 as 16-bit color 0b1: Process bpp = 8 as 16-bit color
phy0_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for PHY0 frequency fine-tuning	0xX: PHY0 frequency fine-tuning override high nibble

#### BACKTOP22 (0x31D)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dty	–	phy0_csi_tx_dpll_fb_fraction_predef_en	phy0_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	–	0b1	0b01111				
Access Type	Write, Read	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dty	7	Software-override enable for BPP, VC, and DT	0b0: Software-override for BPP, VC, and DT disabled 0x1: Software-override for BPP, VC, and DT enabled
phy0_csi_tx_dpll_fb_fraction_predef_en	5	CSI PHY0 software-override disable for frequency fine-tuning. When set to 1, PLL uses predefined frequency from phy0_csi_tx_dpll_predef_freq bit field.	0b0: Software-override for frequency fine-tuning enabled 0x1: Software-override for frequency fine-tuning disabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_csi_tx_dpll_predef_freq	4:0	Determines CSI PHY0 output frequency in multiples of 100Mbps (DPHY) or 100Msps (CPHY) (PLL for MIPI Port C in 4x2 mode). PLLs should be put in reset before changing this register (config_soft_rst_n bit).	0x0: 80Mbps/Msps 0x1: 100Mbps/Msps 0x2: 200Mbps/Msps 0x3: 300Mbps/Msps 0x4: 400Mbps/Msps 0x5: 500Mbps/Msps 0x6: 600Mbps/Msps 0x7: 700Mbps/Msps 0x8: 800Mbps/Msps 0x9: 900Mbps/Msps 0xA: 1000Mbps/Msps 0xB: 1100Mbps/Msps 0xC: 1200Mbps/Msps 0xD: 1300Mbps/Msps 0xE: 1400Mbps/Msps 0xF: 1500Mbps/Msps 0x10: 1600Mbps/Msps 0x11: 1700Mbps/Msps 0x12: 1800Mbps/Msps 0x13: 1900Mbps/Msps 0x14: 2000Mbps/Msps 0x15: 2100Mbps/Msps 0x16: 2200Mbps/Msps 0x17: 2300Mbps/Msps 0x18: 2400Mbps/Msps 0x19: 2500Mbps/Msps Others: 1500Mbps/Msps

#### BACKTOP23 (0x31E)

BIT	7	6	5	4	3	2	1	0
Field	phy1_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
phy1_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY1 frequency fine-tuning. Refer app note.			0xXX: PHY1 frequency fine-tuning override low byte			

#### BACKTOP24 (0x31F)

BIT	7	6	5	4	3	2	1	0
Field	—	bpp8dblz_m ode	bpp8dbly_m ode	—	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	—	0b0	0b0	—	0x0			
Access Type	—	Write, Read	Write, Read	—	Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE			
bpp8dblz_mo de	6	Enable 8-bit write alternate map to RAMs for Pipeline Z			0b0: Write alternative map disabled 0x1: Write alternative map enabled			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbly_mode	5	Enable 8-bit write alternate map to RAMs for Pipeline Y	0b0: Write alternative map disabled 0x1: Write alternative map enabled
phy1_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for PHY1 frequency fine-tuning	0xX: PHY1 frequency fine-tuning override high nibble

**BACKTOP25 (0x320)**

BIT	7	6	5	4	3	2	1	0
Field	—	override_bpp_vc_dtz	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
Reset	—	0b0	0b1	0b01111				
Access Type	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dtz	6	Software-override enable for BPP, VC, and DT	0b0: Software-override for BPP, VC, and DT disabled 0x1: Software-override for BPP, VC, and DT enabled
phy1_csi_tx_dpll_fb_fraction_predef_en	5	CSI PHY1 software-override disable for frequency fine-tuning. When set to 1, PLL uses predefined frequency from phy1_csi_tx_dpll_predef_freq bit field.	fine-tuning 0b0: Software-override for frequency fine tuning enabled 0x1: Software-override for frequency fine-tuning disabled
phy1_csi_tx_dpll_predef_freq	4:0	Determines CSI PHY1 output frequency in multiples of 100Mbps (DPHY) or 100Msps (CPHY) (PLL for MIPI Port A in 2x4 mode, Port D in 4x2 mode). PLLs should be put in reset before changing this register (config_soft_rst_n bit).	0x0: 80Mbps/Msps 0x1: 100Mbps/Msps 0x2: 200Mbps/Msps 0x3: 300Mbps/Msps 0x4: 400Mbps/Msps 0x5: 500Mbps/Msps 0x6: 600Mbps/Msps 0x7: 700Mbps/Msps 0x8: 800Mbps/Msps 0x9: 900Mbps/Msps 0xA: 1000Mbps/Msps 0xB: 1100Mbps/Msps 0xC: 1200Mbps/Msps 0xD: 1300Mbps/Msps 0xE: 1400Mbps/Msps 0xF: 1500Mbps/Msps 0x10: 1600Mbps/Msps 0x11: 1700Mbps/Msps 0x12: 1800Mbps/Msps 0x13: 1900Mbps/Msps 0x14: 2000Mbps/Msps 0x15: 2100Mbps/Msps 0x16: 2200Mbps/Msps 0x17: 2300Mbps/Msps 0x18: 2400Mbps/Msps 0x19: 2500Mbps/Msps Others: 1500Mbps/Msps

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BACKTOP26 (0x321)**

BIT	7	6	5	4	3	2	1	0
Field	phy2_csi_tx_dppll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dppll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY2 frequency fine-tuning. Refer app note.	0xXX: PHY2 frequency fine-tuning override low byte

**BACKTOP27 (0x322)**

BIT	7	6	5	4	3	2	1	0
Field	yuv_8_10_mux_mode4	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	phy2_csi_tx_dppll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
yuv_8_10_mux_mode4	7	Enable YUV422 8-/10-bit muxed mode support	0b0: Disabled 0b1: Enabled
yuv_8_10_mux_mode3	6	Enable YUV422 8-/10-bit muxed mode support	0b0: Disabled 0b1: Enabled
yuv_8_10_mux_mode2	5	Enable YUV422 8-/10-bit muxed mode support	0b0: Disabled 0b1: Enabled
yuv_8_10_mux_mode1	4	Enable YUV422 8-/10-bit muxed mode support	0b0: Disabled 0b1: Enabled
phy2_csi_tx_dppll_fb_fraction_in_h	3:0	High nibble of software-override value for PHY2 frequency fine tuning	0xX: PHY2 frequency fine-tuning override high nibble

**BACKTOP28 (0x323)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	phy2_csi_tx_dppll_fb_fraction_predef_en	phy2_csi_tx_dppll_predef_freq[4:0]				
Reset	–	–	0b1	0b01111				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dppll_fb_fraction_predef_en	5	CSI PHY2 software-override disable for frequency fine-tuning. When set to 1, PLL uses predefined frequency from phy2_csi_tx_dppll_predef_freq bit field.	0b0: Software-override for frequency fine-tuning enabled 0x1: Software-override for frequency fine-tuning disabled



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITLED	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dpll_predef_freq	4:0	Determines CSI PHY2 output frequency in multiples of 100Mbps (DPHY) or 100Msps (CPHY) (PLL for MIPI Port B in 2x4 mode, Port E in 4x2 mode). PLLs should be put in reset before changing this register (config_soft_rst_n bit).	0x0: 80Mbps/Msps 0x1: 100Mbps/Msps 0x2: 200Mbps/Msps 0x3: 300Mbps/Msps 0x4: 400Mbps/Msps 0x5: 500Mbps/Msps 0x6: 600Mbps/Msps 0x7: 700Mbps/Msps 0x8: 800Mbps/Msps 0x9: 900Mbps/Msps 0xA: 1000Mbps/Msps 0xB: 1100Mbps/Msps 0xC: 1200Mbps/Msps 0xD: 1300Mbps/Msps 0xE: 1400Mbps/Msps 0xF: 1500Mbps/Msps 0x10: 1600Mbps/Msps 0x11: 1700Mbps/Msps 0x12: 1800Mbps/Msps 0x13: 1900Mbps/Msps 0x14: 2000Mbps/Msps 0x15: 2100Mbps/Msps 0x16: 2200Mbps/Msps 0x17: 2300Mbps/Msps 0x18: 2400Mbps/Msps 0x19: 2500Mbps/Msps Others: 1500Mbps/Msps

#### BACKTOP29 (0x324)

BIT	7	6	5	4	3	2	1	0
Field	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY3 frequency fine-tuning. Refer app note.	0xXX: PHY3 frequency fine-tuning override low byte

#### BACKTOP30 (0x325)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP_W_FRAME	—	—	—	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	—	—	—	0x0			
Access Type	Write, Read	—	—	—	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP_W_FRAME	7	When this register is set, BACKTOP (line buffer memory) waits for a new frame before generating MIPI packet requests to the MIPI TX.	0b0: Does not wait for a new frame start 0b1: Waits for a frame start

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for PHY3 frequency fine-tuning	0xX: PHY3 frequency fine-tuning override high nibble

**BACKTOP31 (0x326)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]				
Reset	–	–	0b1	0b01111				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_csi_tx_dpll_fb_fraction_predef_en	5	CSI PHY3 software-override disable for frequency fine-tuning. When set to 1, PLL uses predefined frequency from phy3_csi_tx_dpll_predef_freq bit field.	0b0: Software-override for frequency fine-tuning enabled 0x1: Software-override for frequency fine-tuning disabled
phy3_csi_tx_dpll_predef_freq	4:0	Determines CSI PHY3 output frequency in multiples of 100Mbps (DPHY) or 100Msps (CPHY) (PLL for MIPI Port F in 4x2 mode). PLLs should be put in reset before changing this register (config_soft_rst_n bit).	0x0: 80Mbps/Msps 0x1: 100Mbps/Msps 0x2: 200Mbps/Msps 0x3: 300Mbps/Msps 0x4: 400Mbps/Msps 0x5: 500Mbps/Msps 0x6: 600Mbps/Msps 0x7: 700Mbps/Msps 0x8: 800Mbps/Msps 0x9: 900Mbps/Msps 0xA: 1000Mbps/Msps 0xB: 1100Mbps/Msps 0xC: 1200Mbps/Msps 0xD: 1300Mbps/Msps 0xE: 1400Mbps/Msps 0xF: 1500Mbps/Msps 0x10: 1600Mbps/Msps 0x11: 1700Mbps/Msps 0x12: 1800Mbps/Msps 0x13: 1900Mbps/Msps 0x14: 2000Mbps/Msps 0x15: 2100Mbps/Msps 0x16: 2200Mbps/Msps 0x17: 2300Mbps/Msps 0x18: 2400Mbps/Msps 0x19: 2500Mbps/Msps Others: 1500Mbps/Msps

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BACKTOP32 (0x327)**

BIT	7	6	5	4	3	2	1	0
Field	–	bpp10dblz_mode	bpp10dbly_mode	–	–	bpp10dblz	bpp10dbly	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–	Write, Read	Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dblz_mode	6	Enable 8-bit write alternate map to RAMs for Pipeline Z	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp10dbly_mode	5	Enable 8-bit write alternate map to RAMs for Pipeline Y	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp10dblz	2	bpp = 8 processed as 16-bit color enable for Pipeline Z. Used to give all video data flowing through a single pipe the same bpp, to maximize capacity of video pipeline.	0b0: Do not process bpp = 8 as 16-bit color 0b1: Process bpp = 8 as 16-bit color
bpp10dbly	1	bpp = 8 processed as 16-bit color enable for Pipeline Y. Used to give all video data flowing through a single pipe the same bpp, to maximize capacity of video pipeline.	0b0: Do not process bpp = 8 as 16-bit color 0b1: Process bpp = 8 as 16-bit color

**BACKTOP33 (0x328)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	bpp12dblz	bpp12dbly	–
Reset	–	–	–	–	–	0b0	0b0	–
Access Type	–	–	–	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp12dblz	2	bpp = 8 processed as 16-bit color enable for Pipeline Z. Used to give all video data flowing through a single pipe the same bpp, to maximize capacity of video pipeline.	0b0: Do not process bpp = 8 as 16-bit color 0b1: Process bpp = 8 as 16-bit color
bpp12dbly	1	bpp = 8 processed as 16-bit color enable for Pipeline Y. Used to give all video data flowing through a single pipe the same bpp, to maximize capacity of video pipeline.	0b0: Do not process bpp = 8 as 16-bit color 0b1: Process bpp = 8 as 16-bit color

**MIPI\_PHY0 (0x330)\***

BIT	7	6	5	4	3	2	1	0
Field	force_csi_out_en	RSVD	RSVD	phy_1x4b_2	phy_1x4a_2	phy_2x4	RSVD	phy_4x2
Reset	0b0	0b0	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read			Write, Read	Write, Read	Write, Read		Write, Read

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
force_csi_out_en	7	Force CSI output clock for use in MIPI loopback test	0b0: CSI output clock not enabled for MIPI loopback test 0b1: CSI output clock enabled for MIPI loopback test
phy_1x4b_22	4	MIPI output configured as 2x2 and 1x4. PLLs should be put in reset before changing this register (config_soft_rst_n bit).	0b0: 1x4 and 2x2 configuration not selected 0b1: MIPI output configured as three ports. Port A is two two-ports, each with two data lanes using PHY0 and PH1. Port C is one four-lane port using PHY2 and PHY3
phy_1x4a_22	3	MIPI output configured as 1x4 and 2x2. PLLs should be put in reset before changing this register (config_soft_rst_n bit).	0b0: 1x4 and 2x2 configuration not selected 0b1: MIPI output configured as three ports. Port A is one port with four data lanes using PHY0 and PH1. Port C is two ports, each with two data lanes using PHY2 and PHY3
phy_2x4	2	MIPI output configured as 2x4. PLLs should be put in reset before changing this register (config_soft_rst_n bit).	0b0: 2x4 not selected 0b1: MIPI output configured as two ports with four data lanes each. Port A uses PHY0 and PHY1, Port B uses PHY2 and PHY3.
phy_4x2	0	MIPI output configured as 4x2. PLLs should be put in reset before changing this register (config_soft_rst_n bit).	0b0: 4x2 configuration not selected 0b1: MIPI output configured as four two-lane MIPI ports

**MIPI\_PHY1 (0x331)\***

BIT	7	6	5	4	3	2	1	0
Field	t_hs_przero[1:0]		t_hs_prep[1:0]		RSVD[1:0]		t_clk_przero[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read				Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_przero	7:6	Typical DPHY data lane HS_prep + HS_zero timing	0b00: 146ns + 24UI 0b01: 160ns + 24UI 0b10: 173ns + 24UI 0b11: 200ns + 24UI
t_hs_prep	5:4	Typical DPHY data lane HS_prepare timing	0b00: 46.7ns + 4UI 0b01: 53.4ns + 4UI 0b10: 60.0ns + 4UI 0b11: 66.7ns + 4UI
t_clk_przero	1:0	Typical DPHY clock lane HS_prepare + HS_zero timing	0b00: 306ns 0b01: 600ns 0b10: 900ns 0b11: 1200ns

**MIPI\_PHY2 (0x332)\***

BIT	7	6	5	4	3	2	1	0
Field	phy_Stdbby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
Reset	0xF				0b01		0b00	
Access Type	Write, Read				Write, Read		Write, Read	

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
phy_Stdbby_n	7:4	Put MIPI PHY into standby mode if not used to save power. One bit per PHY.	0bXXX0: Put PHY0 in standby mode 0bXX0X: Put PHY1 in standby mode 0bX0XX: Put PHY2 in standby mode 0b0XXX: Put PHY3 in standby mode 0b0000: All PHYs in standby mode ... 0b1111: All PHYs not in standby mode
t_lpx	3:2	Typical DPHY T <sub>Lpx</sub> timing	0b00: 53.4ns 0b01: 106.7ns 0b10: 160ns 0b11: 213.4ns
t_hs_trail	1:0	Typical DPHY data lane HS_trail timing	0b00: 66.7ns + 8UI 0b01: 80ns + 8UI 0b10: 93.4ns + 8UI 0b11: 106.7ns + 8UI

**MIPI\_PHY3 (0x333)\***

BIT	7	6	5	4	3	2	1	0
Field	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
Reset	0x4				0xE			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lane_map	7:4	MIPI PHY1 to Port A lane mapping in 2 x 4 configurations  Bits[1:0] map PHY1 data lane 0 Bits[3:2] map PHY1 data lane 1	0bXX00: Map PHY1 D0 to Port A D0 0bXX01: Map PHY1 D0 to Port A D1 0bXX10: Map PHY1 D0 to Port A D2 0bXX11: Map PHY1 D0 to Port A D3 0b00XX: Map PHY1 D1 to Port A D0 0b01XX: Map PHY1 D1 to Port A D1 0b10XX: Map PHY1 D1 to Port A D2 0b11XX: Map PHY1 D1 to Port A D3
phy0_lane_map	3:0	MIPI PHY0 to Port A lane mapping in 2 x 4 configurations  Bits[1:0] map PHY0 data lane 0 Bits[3:2] map PHY0 data lane 1	0bXX00: Map PHY0 D0 to Port A D0 0bXX01: Map PHY0 D0 to Port A D1 0bXX10: Map PHY0 D0 to Port A D2 0bXX11: Map PHY0 D0 to Port A D3 0b00XX: Map PHY0 D1 to Port A D0 0b01XX: Map PHY0 D1 to Port A D1 0b10XX: Map PHY0 D1 to Port A D2 0b11XX: Map PHY0 D1 to Port A D3

**MIPI\_PHY4 (0x334)\***

BIT	7	6	5	4	3	2	1	0
Field	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
Reset	0xE				0x4			
Access Type	Write, Read				Write, Read			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_lane_map	7:4	MIPI PHY3 to Port B lane mapping in 2 x 4 configurations  Bits[1:0] map PHY3 data lane 0 Bits[3:2] map PHY3 data lane 1	0bXX00: Map PHY3 D0 to Port B D0 0bXX01: Map PHY3 D0 to Port B D1 0bXX10: Map PHY3 D0 to Port B D2 0bXX11: Map PHY3 D0 to Port B D3 0b00XX: Map PHY3 D1 to Port B D0 0b01XX: Map PHY3 D1 to Port B D1 0b10XX: Map PHY3 D1 to Port B D2 0b11XX: Map PHY3 D1 to Port B D3
phy2_lane_map	3:0	MIPI PHY2 to Port B lane mapping in 2 x 4 configurations  Bits[1:0] map PHY2 data lane 0 Bits[3:2] map PHY2 data lane 1	0bXX00: Map PHY2 D0 to Port B D0 0bXX01: Map PHY2 D0 to Port B D1 0bXX10: Map PHY2 D0 to Port B D2 0bXX11: Map PHY2 D0 to Port B D3 0b00XX: Map PHY2 D1 to Port B D0 0b01XX: Map PHY2 D1 to Port B D1 0b10XX: Map PHY2 D1 to Port B D2 0b11XX: Map PHY2 D1 to Port B D3

**MIPI\_PHY5 (0x335)\***

BIT	7	6	5	4	3	2	1	0
Field	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
Reset	0b00		0b000			0b000		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
t_clk_prep	7:6	Typical DPHY clock lane HS_prepare timing	0b00: 40ns 0b01: 46.7ns 0b10: 53.4ns 0b11: 60ns
phy1_pol_map	5:3	MIPI PHY1 lane polarity.  In DPHY mode, this controls the polarity for clock, D1, and D0. In normal polarity, P is positive, N is negative. In inverse polarity, P is negative, N is positive.  In CPHY mode, this controls the A and C pin routing in the ABC three-pin trio. In normal polarity, no pins in the ABC trio are swapped. In inverse polarity, the A and C pins are swapped.	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane (DPHY only) 0b1XX: Inverse polarity for clock lane (DPHY only)
phy0_pol_map	2:0	MIPI PHY0 lane polarity.  In DPHY mode, this controls the polarity for clock, D1, and D0. In normal polarity, P is positive, N is negative. In inverse polarity, P is negative, N is positive.  In CPHY mode, this controls the A and C pin routing in the ABC three-pin trio. In normal polarity, no pins in the ABC trio are swapped. In inverse polarity, the A and C pins are swapped.	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane (DPHY only) 0b1XX: Inverse polarity for clock lane (DPHY only)

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_PHY6 (0x336)\***

BIT	7	6	5	4	3	2	1	0
Field	phy_cp1	phy_cp0	phy3_pol_map[2:0]			phy2_pol_map[2:0]		
Reset	0b0	0b0	0b000			0b000		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp1	7	MIPI PHY port copy enable 1. Used for video replication/duplication to have all video data outputting on one MIPI PHY to also output on another PHY. When enabled, the data from the PHY set in phy_cp1_src is copied to the PHY set in the phy_cp1_dst.	0b0: Do not copy MIPI PHY data 0b1: Copy MIPI data from source PHY to destination PHY
phy_cp0	6	MIPI PHY port copy enable 0. Used for video replication/duplication to have all video data outputting on one MIPI PHY to also output on another PHY. When enabled, the data from the PHY set in phy_cp0_src is copied to the PHY set in the phy_cp0_dst.	0b0: Do not copy MIPI PHY data 0b1: Copy MIPI data from source PHY to destination PHY
phy3_pol_map	5:3	MIPI PHY3 lane polarity.  In DPHY mode, this controls the polarity for clock, D1, and D0. In normal polarity, P is positive, N is negative. In inverse polarity, P is negative, N is positive.  In CPHY mode, this controls the A and C pin routing in the ABC three-pin trio. In normal polarity, no pins in the ABC trio are swapped. In inverse polarity, the A and C pins are swapped.	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane (DPHY only) 0b1XX: Inverse polarity for clock lane (DPHY only)
phy2_pol_map	2:0	MIPI PHY2 lane polarity.  In DPHY mode, this controls the polarity for clock, D1, and D0. In normal polarity, P is positive, N is negative. In inverse polarity, P is negative, N is positive.  In CPHY mode, this controls the A and C pin routing in the ABC three-pin trio. In normal polarity, no pins in the ABC trio are swapped. In inverse polarity, the A and C pins are swapped.	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane (DPHY only) 0b1XX: Inverse polarity for clock lane (DPHY only)

**MIPI\_PHY9 (0x339)**

BIT	7	6	5	4	3	2	1	0
Field	phy_cp0_dst[1:0]		–	RSVD	RSVD	–	RSVD	phy_cp0_overflow
Reset	0b00		–	0b0	0b0	–	0b0	0b0
Access Type	Write, Read		–			–		Read Clears All



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp0_dst	7:6	MIPI PHY copy 0 destination. See phy_cp0 for details.	0x0: MIPI PHY 0 0x1: MIPI PHY 1 0x2: MIPI PHY 2 0x3: MIPI PHY 3
phy_cp0_overflow	0	PHY copy 0 FIFO overflow flag (sticky)	0b0: No overflow error has occurred 0b1: Overflow error has occurred

#### MIPI\_PHY10 (0x33A)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp0_src[1:0]		RSVD[2:0]			–	RSVD	phy_cp0_underflow
Reset	0b00		0b000			–	0b1	0b0
Access Type	Write, Read					–		Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp0_src	7:6	MIPI PHY copy 0 source. See phy_cp0 for details.	0x0: Reserved 0x1: MIPI PHY 1 0x2: MIPI PHY 2 0x3: Reserved
phy_cp0_underflow	0	PHY copy 0 FIFO underflow flag (sticky)	0b0: No underflow error has occurred 0b1: Underflow error has occurred

#### MIPI\_PHY11 (0x33B)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp1_dst[1:0]		RSVD[2:0]			–	RSVD	phy_cp1_overflow
Reset	0b00		0b000			–	0b0	0b0
Access Type	Write, Read					–		Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp1_dst	7:6	MIPI PHY copy 1 destination. See phy_cp1 for details.	0x0: MIPI PHY 0 0x1: MIPI PHY 1 0x2: MIPI PHY 2 0x3: MIPI PHY 3
phy_cp1_overflow	0	PHY copy 1 FIFO overflow flag (sticky)	0b0: No overflow error has occurred 0b1: Overflow error has occurred

#### MIPI\_PHY12 (0x33C)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp1_src[1:0]		RSVD[2:0]			–	RSVD	phy_cp1_underflow
Reset	0b00		0b000			–	0b1	0b0
Access Type	Write, Read					–		Read Clears All

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp1_src	7:6	MIPI PHY copy 1 source. See phy_cp1 for details.	0x0: Reserved 0x1: MIPI PHY 1 0x2: MIPI PHY 2 0x3: Reserved
phy_cp1_und erflow	0	PHY copy 1 FIFO underflow flag (sticky)	0b0: No underflow error has occurred 0b1: Underflow error has occurred

#### MIPI\_PHY13 (0x33D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	t_t3_prebegin[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
t_t3_prebegin	5:0	CPHY prebegin phase of the preamble (t3_prebegin + 1) x 7UI

#### MIPI\_PHY14 (0x33E)

BIT	7	6	5	4	3	2	1	0
Field	–	t_t3_post[4:0]					t_t3_prep[1:0]	
Reset	–	0x04					0x1	
Access Type	–	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_t3_post	6:2	CPHY post length after HS data = (t3_post + 1) x 7UI	
t_t3_prep	1:0	CPHY Tbs_prepare timing	0x0: 40ns 0x1: 55ns 0x2: 66.7ns 0x3: 86.7ns

#### MIPI\_PHY15 (0x33F)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RST_MIPITX_LOC[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RST_MIPITX _LOC	3:0	Active high reset to MIPI controller  DP_RST_MIPI_CHKB must be enabled to use this reset.	0b0000: Normal operation enabled 0bXX1X: Active high reset to CSI2/MIPI controller 1 0bX1XX: Active high reset to CSI2/MIPI controller 2 Others: Reserved

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_PHY16 (0x340)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	TUN_DATA_CRC_ERR_OEN	TUN_ECC_UNCORR_ERR_OEN	TUN_ECC_CORR_ERR_OEN	–	–	VID_OVERFLOW_OEN
Reset	–	–	0b0	0b0	0b0	–	–	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
TUN_DATA_CRC_ERR_OEN	5	For tunneling mode, enable reporting at ERRB pin of DPHY/CPHY data CRC errors
TUN_ECC_UNCORR_ERR_OEN	4	For tunneling mode, enable reporting at ERRB pin of uncorrectable errors on DPHY ECC or CPHY header CRC
TUN_ECC_CORR_ERR_OEN	3	For tunneling mode, enable reporting at ERRB pin of correctable errors on DPHY ECC or CPHY header CRC
VID_OVERFLOW_OEN	0	Enable reporting of video pipe overflow (VID_OVERFLOW) at ERRB pin

**MIPI\_PHY17 (0x341)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	TUN_DATA_CRC_ERR	TUN_ECC_UNCORR_ERR	TUN_ECC_CORR_ERR	–	–	VID_OVERFLOW_FLAG
Reset	–	–	0b0	0b0	0b0	–	–	0b0
Access Type	–	–	Read Only	Read Only	Read Only	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
TUN_DATA_CRC_ERR	5	For tunneling mode, DPHY/CPHY data CRC errors Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear.
TUN_ECC_UNCORR_ERR	4	For tunneling mode, uncorrectable errors on DPHY ECC or CPHY header CRC Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear.
TUN_ECC_CORR_ERR	3	For tunneling mode, correctable errors on DPHY ECC or CPHY header CRC. Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear.
VID_OVERFLOW_FLAG	0	Combined error status of all video pipe overflow (VID_OVERFLOW) bits. Read individual VID_OVERFLOW bits to clear.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MIPI\_PHY18 (0x342)

BIT	7	6	5	4	3	2	1	0
Field	csi2_tx2_pkt_cnt[3:0]				csi2_tx1_pkt_cnt[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
csi2_tx2_pkt_cnt	7:4	Packet Count of CSI2 Controller 2. Used for debug to determine if video data is outputting from CSI2 Controller.	0bXXXX: Number of packets out since video started
csi2_tx1_pkt_cnt	3:0	Packet Count of CSI2 Controller 1. Used for debug to determine if video data is outputting from CSI2 Controller.	0bXXXX: Number of packets out since video started

MIPI\_PHY19 (0x343)

BIT	7	6	5	4	3	2	1	0
Field	csi2_dup2_pkt_cnt[3:0]				csi2_dup1_pkt_cnt[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
csi2_dup2_pkt_cnt	7:4	Packet Count of CSI2 Duplication 2. Used for debug to determine if video data is outputting from CSI2 Duplication.	0bXXXX: Number of packets out since video started
csi2_dup1_pkt_cnt	3:0	Packet Count of CSI2 Duplication 1. Used for debug to determine if video data is outputting from CSI2 Duplication.	0bXXXX: Number of packets out since video started

MIPI\_PHY20 (0x344)

BIT	7	6	5	4	3	2	1	0
Field	phy1_pkt_cnt[3:0]				phy0_pkt_cnt[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_pkt_cnt	7:4	Packet Count of MIPI PHY1. Used for debug to determine if video data is outputting from MIPI PHY.	0bXXXX: Number of packets out since video started
phy0_pkt_cnt	3:0	Packet Count of MIPI PHY0. Used for debug to determine if video data is outputting from MIPI PHY.	0bXXXX: Number of packets out since video started

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_PHY21 (0x345)**

BIT	7	6	5	4	3	2	1	0
Field	phy3_pkt_cnt[3:0]				phy2_pkt_cnt[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_pkt_cnt	7:4	Packet Count of MIPI PHY3. Used for debug to determine if video data is outputting from MIPI PHY.	0bXXXX: Number of packets out since video started
phy2_pkt_cnt	3:0	Packet Count of MIPI PHY2. Used for debug to determine if video data is outputting from MIPI PHY.	0bXXXX: Number of packets out since video started

**FSYNC\_0 (0x3E0)\***

BIT	7	6	5	4	3	2	1	0
Field	EN_OFLOW_RST_FS	RSVD	FSYNC_OUT_PIN	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
Reset	0b0	0b0	0b0	0b0	0b11		0b10	
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
EN_OFLOW_RST_FS	7	When enabled, memory overflow resets frame sync generation	0b0: Do not reset frame sync generation when memory overflow occurs 0b1: Reset frame sync generation when memory overflow occurs
FSYNC_OUT_PIN	5	Select pin to output frame sync signal (effective only when FSYNC_METH = 01)	0b0: Reserved 0b1: MFP0
EN_VS_GEN	4	When enabled, VS is generated internally by the frame sync generator (not effective when FSYNC_MODE = 11)	0x0: Internal frame sync does not generate VS 0x1: Internal frame sync generates VS
FSYNC_MODE	3:2	Frame Synchronization Mode	GMSL2/3: 0b00: Frame sync generation is on. FSYNC_OUT pin is not used as FSYNC output, but a GPIO on the remote side can be used 0b01: Frame sync generation is on. FSYNC_OUT pin is used as FSYNC output and drives a slave device, and a GPIO on the remote side can be used 0b10: Frame sync generation is off. FSYNC_OUT pin is not used as FSYNC output. 0b11: Frame sync generation is off. FSYNC_OUT pin is not used as FSYNC output
FSYNC_METHOD	1:0	Frame Synchronization Method	0b00: Manual 0b01: Semi-auto 0b10: Auto 0b11: Reserved

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**FSYNC\_1 (0x3E1)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		FSYNC_PER_DIV[3:0]			
Reset	0b00		0b00		0x0			
Access Type					Write, Read			

BITLEN	BITS	DESCRIPTION	DECODE
FSYNC_PER_DIV	3:0	Frame sync transmission period in terms of VSYNC periods	0x0: 1 0x1: 2 0x2: 4 0x3: 6 0x4: 8 0x5: 10 0x6: 12 0x7: 16 0x8: 20 0x9: 24 0xA: 32 0xB: 48 0xC: 64 0xD: 80 0xE: 96 0xF: 128

**FSYNC\_2 (0x3E2)\***

BIT	7	6	5	4	3	2	1	0
Field	MST_LINK_SEL[2:0]			K_VAL_SIG_N	K_VAL[3:0]			
Reset	0b100			0b0	0x1			
Access Type	Write, Read			Write, Read	Write, Read			

BITLEN	BITS	DESCRIPTION	DECODE
MST_LINK_SEL	7:5	Master link select for frame sync generation	0b000: Reserved 0b001: Video Y 0b010: Video Z 0b011: Reserved 0b100: Auto select 0b101: Auto select 0b110: Auto select 0b111: Auto select
K_VAL_SIG_N	4	Sign bit of K_VAL	0b0: K_VAL is positive 0b1: K_VAL is negative

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
K_VAL	3:0	Desired frame sync margin (microseconds, typical) with respect to the V <sub>SYNC</sub> of the slowest link in auto mode or with respect to the V <sub>SYNC</sub> of the master link in semi-auto mode.	0x0: 1 0x1: 2 0x2: 3 0x3: 4 0x4: 5 0x5: 6 0x6: 7 0x7: 8 0x8: 10 0x9: 12 0xA: 14 0xB: 16 0xC: 20 0xD: 24 0xE: 28 0xF: 32

**FSYNC\_3 (0x3E3)\***

BIT	7	6	5	4	3	2	1	0
Field	P_VAL_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_L	7:0	Low byte of desired frame sync margin in terms of PCLK cycles with respect to the V <sub>SYNC</sub> of the slowest link in auto mode or with respect to the V <sub>SYNC</sub> of the master link in semi-auto mode	0xXX: Low byte of PCLK cycles frame sync margin

**FSYNC\_4 (0x3E4)\***

BIT	7	6	5	4	3	2	1	0
Field	—	—	P_VAL_SIG N	P_VAL_H[4:0]				
Reset	—	—	0b0	0b00000				
Access Type	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_SIG N	5	Sign bit of P_VAL	0b0: P_VAL is positive 0b1: P_VAL is negative
P_VAL_H	4:0	High bits of desired frame sync margin in terms of PCLK cycles with respect to the V <sub>SYNC</sub> of the slowest link in auto mode or with respect to the V <sub>SYNC</sub> of the master link in semi-auto mode	0b00000: High bits of PCLK cycles frame sync margin



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**FSYNC\_5 (0x3E5)\***

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_L[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FSYNC_PERIOD_L	7:0	Low byte of frame sync period in terms of pixel clock effective when FSYNC_METH (0x3E0) = 00 and FSYNC_MODE (0x3E0) = 0x)			0xXX: Low byte of PCLK cycles in frame period			

**FSYNC\_6 (0x3E6)\***

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_M[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FSYNC_PERIOD_M	7:0	Middle byte of frame sync period in terms of pixel clock (effective when FSYNC_METH (0x3E0) = 00 and FSYNC_MODE (0x3E0) = 0x)			0xXX: Middle byte of PCLK cycles in frame period			

**FSYNC\_7 (0x3E7)\***

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_H[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FSYNC_PERIOD_H	7:0	High byte of frame sync period in terms of pixel clock (effective when FSYNC_METH (0x3E0) = 00 and FSYNC_MODE (0x3E0) = 0x)			0xXX: High byte of PCLK cycles in frame period			

**FSYNC\_8 (0x3E8)**

BIT	7	6	5	4	3	2	1	0
Field	FRM_DIFF_ERR_THR_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_ERR_THR_L	7:0	Low byte of the error threshold for difference between the earliest and latest VSYNCs in terms of PCLK cycles.  The default is 40μs for 96MHz PCLK. The function is disabled when all 13 bits are zeros.	0xXX: Low byte of PCLK cycles in the VSYNC error threshold

#### FSYNC\_9 (0x3E9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FRM_DIFF_ERR_THR_H[4:0]				
Reset	–	–	–	0b01111				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_ERR_THR_H	4:0	High bits of the error threshold for difference between the earliest and latest VSYNCs in terms of PCLK cycles.  The default is 40μs for 96MHz PCLK. The function is disabled when all 13 bits are zeros.	0bXXXXX: High bits of PCLK cycles in the VSYNC error threshold

#### FSYNC\_10 (0x3EA)

BIT	7	6	5	4	3	2	1	0
Field	OVLP_WINDOW_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OVLP_WIND_OW_L	7:0	Low byte of the overlap window value in terms of PCLK cycles. The window starts from the VS rising edge from the fastest image sensor and ends when a frame sync signal is seen.  The default is 60μs for 96MHz PCLK. The function is disabled when all 13 bits are zeros.	0xXX: Low byte of PCLK cycles in the VSYNC overlap window.

#### FSYNC\_11 (0x3EB)

BIT	7	6	5	4	3	2	1	0
Field	EN_FSIN_L AST	–	–	OVLP_WINDOW_H[4:0]				
Reset	0b0	–	–	0b00000				
Access Type	Write, Read	–	–	Write, Read				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
EN_FSIN_LAST	7	FSIN position	0b0: FSIN can occur anywhere with respect to VS rising edges 0b1: FSIN occurs after all rising edges
OVLP_WINDOW_H	4:0	Low byte of the overlap window value in terms of PCLK cycles. The window starts from the VS rising edge from the fastest image sensor and ends when a frame sync signal is seen.  The default is 60µs for 96MHz PCLK. The function is disabled when all 13 bits are zeros.	0bXXXXX: High bits of PCLK cycles in the VSYNC overlap window.

#### FSYNC\_15 (0x3EF)

BIT	7	6	5	4	3	2	1	0
Field	FS_GPIO_TYPE	FS_USE_XTAL	–	AUTO_FS_LINKS	–	FS_EN_Z	FS_EN_Y	–
Reset	0b1	0b0	–	0b1	–	0b1	0b1	–
Access Type	Write, Read	Write, Read	–	Write, Read	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
FS_GPIO_TYPE	7	Select the type of FSYNC signal to output from GPIO	0x0: GSML1 type 0x1: GSML2 type
FS_USE_XTAL	6	Use crystal oscillator clock for generating frame sync signal	0x0: Disabled 0x1: Enabled
AUTO_FS_LINKS	4	Select how links are selected for frame sync generation	0x0: Include links selected by FS_LINK_x register bits in frame sync generation 0x1: Include all enabled links in frame sync generation
FS_EN_Z	2	Include Video Pipe Z in frame-sync generation  This is used only if AUTO_FS_LINKS = 0.	0x0: Do not include Video Pipe Z in frame-sync generation 0x1: Include Video Pipe Z in frame-sync generation
FS_EN_Y	1	Include Video Pipe Y in frame-sync generation  This is used only if AUTO_FS_LINKS = 0	0x0: Do not include Video Pipe Y in frame-sync generation 0x1: Include Video Pipe Y in frame-sync generation

#### FSYNC\_16 (0x3F0)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_ERR_CNT	7:0	Frame Sync Error Counter  Resets to 0 when read or when FSYNC_LOCKED goes high.	0xXX: Frame sync error counter

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

### FSYNC\_17 (0x3F1)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
Reset	0b11110					0b000		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_TX_ID	7:3	GPIO ID used for transmitting FSYNC signal. The remote side should set the corresponding GPIO_RX_ID to the same value.	0bXXXXX: GPIO ID
FSYNC_ERR_THR	2:0	Frame Sync Error Threshold Reporting FSYNC_ERR_FLAG is asserted when FSYNC_ERR_CNT (0x3F0) ≥ FSYNC_ERR_THR.	0bXXX: Frame sync error reporting threshold

### FSYNC\_18 (0x3F2)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_L	7:0	Low byte of calculated VS period (number of PCLKs) of master link in auto or semi-auto synchronization mode. Use when FSYNC_METH (0x03E) = 10 and FSYNC_MODE (0x3E) = 0x.	0xXX: Low byte of PCLKs in VS period in master link auto or semi-auto synchronization mode.

### FSYNC\_19 (0x3F3)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_M[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_M	7:0	Middle byte of calculated VS period (number of PCLKs) of master link in auto or semi-auto synchronization mode. Use when FSYNC_METH (0x03E) = 10 and FSYNC_MODE (0x3E) = 0x.	0xXX: Middle byte of PCLKs in VS period in master link auto or semi-auto synchronization mode.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**FSYNC\_20 (0x3F4)**

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_H[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_H	7:0	High byte of calculated VS period (number of PCLKs) of master link in auto or semi-auto synchronization mode.  Use when FSYNC_METH (0x03E) = 10 and FSYNC_MODE (0x3E) = 0x.	0xXX: High byte of PCLKs in VS period in master link auto or semi-auto synchronization mode.

**FSYNC\_21 (0x3F5)**

BIT	7	6	5	4	3	2	1	0
Field	FRM_DIFF_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_L	7:0	Low byte of the difference between the fastest and the slowest frame in terms of master PCLK cycles	0xXX: Low byte of number of PCLKs in the difference between the fastest and slowest frame.

**FSYNC\_22 (0x3F6)**

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Read Clears All	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_LOSS_OF_LOCK	7	Frame Synchronization Lost Lock Flag  Cleared when read.	0b0: Frame sync lock not lost 0b1: Frame sync lock lost
FSYNC_LOCKED	6	Frame Synchronization Lock Flag	0b0: Frame sync not locked 0b1: Frame sync locked
FRM_DIFF_H	5:0	High bits of the difference between the fastest and the slowest frame in terms of master PCLK cycles	0bXXXXXX: High bits of number of PCLKs in the difference between the fastest and slowest frame.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**FSYNC\_23 (0x3F7)\***

BIT	7	6	5	4	3	2	1	0
Field	EN_SYNC_COMP	EN_LINK_R_ESET	–	–	–	FSYNC_OV_R_Z	FSYNC_OV_R_Y	–
Reset	0b0	0b0	–	–	–	0b0	0b0	–
Access Type	Write, Read	Write, Read	–	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN_SYNC_COMP	7	Bypass FSYNC sync complete term in CSI_OUT_EN (0x313).  Enabling sync complete may cause video out to stop if a GMSL link drop occurs during internal frame sync configurations.	0x0: Bypass FSYNC sync complete 0x1: Enable bypass FSYNC sync complete
EN_LINK_R_ESET	6	Internal Frame Sync Reset Link Enable  If enabled, may not operate correctly if GMSL link drop occurs.	0x0: Disable link reset capability 0x1: Enable link reset capability
FSYNC_OV_R_Z	2	Override of video_lock_1 during internal frame sync configuration using FS_LINK_X.  If logic 1, Link 1 continues to be seen by frame sync state machines even if GMSL link drop occurs. Not used in AUTO_FS_LINKS mode.	0b0: Do not include Video Pipe Z in frame sync generation 0b1: Include Video Pipe Z in frame sync generation
FSYNC_OV_R_Y	1	Override of video_lock_1 during internal frame sync configuration using FS_LINK_X.  If logic 1, Link 1 continues to be seen by frame sync state machines even if GMSL link drop occurs. Not used in AUTO_FS_LINKS mode.	0b0: Do not include Video Pipe Y in frame sync generation 0b1: Include Video Pipe Y in frame sync generation

**MIPI\_TX10 (0x40A)\***

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	RSVD	–	–	–	–
Reset	0b11		0b0	0b1	–	–	–	–
Access Type	Write, Read		Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	Set number of MIPI data lanes	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes 0b11: Four data lanes
CSI2_CPHY_EN	5	Enable CPHY	0b0: CPHY disabled 0b1: CPHY enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MIPI\_TX1 (0x441)\*

BIT	7	6	5	4	3	2	1	0
Field	MODE[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MODE	7:0	MIPI Tx Mode			0bXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXX1: Enable MIPI VS short packet counter			

MIPI\_TX2 (0x442)

BIT	7	6	5	4	3	2	1	0
Field	STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
STATUS	7:0	MIPI Tx Status  The register is split into decode segments: bit[0] SYNC mode enable. bit[1] Video sync flag bit[2] Loss of video sync flag bit[3] Tunneling mode: DPHY ECC or CPHY header CRC error (correctable) bit[4] Tunneling mode: DPHY ECC or CPHY header CRC error (uncorrectable) bit[5] Tunneling mode: DPHY/CPHY data CRC error			0bXXXXXXX0: SYNC mode disabled 0bXXXXXXX1: SYNC mode enabled 0bXXXXXXX0X: Video channels not in-sync 0bXXXXXXX1X: Video channels in-sync 0bXXXXXX0XX: No loss of video sync 0bXXXXXX1XX: Video sync lost after last read of this register or RESET. 0bXXXX0XXX: No tunneling ECC correctable error 0bXXXX1XXX: Tunneling ECC correctable error after last read of this register or RESET. 0bXXX0XXXX: No tunneling ECC uncorrectable error 0bXXX1XXXX: Tunneling ECC uncorrectable error after last read of this register or RESET. 0bXX0XXXXX: No tunneling data CRC error 0bXX1XXXXX: Tunneling data CRC error after last read of this register or RESET.			

MIPI\_TX3 (0x443)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x01							
Access Type	Write, Read							



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_INIT	7:0	<p>DPHY Deskew Initial Calibration Control</p> <p>The register is split into six decode segments:</p> <p>bit[7] Selects auto-initial deskew calibration on or off</p> <p>bit[6] Reserved</p> <p>bit[5] Any bit change initiates an initial calibration if bit 4 = 1</p> <p>bit[4] Selects manual initial on or off</p> <p>bit[3] Reserved</p> <p>bits[2:0] Selects initial deskew width</p>	<p>0bXXXXX000: Reserved</p> <p>0bXXXXX001: Initial deskew width = 2 x 32k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX010: Initial deskew width = 3 x 32k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX011: Initial deskew width = 4 x 32k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX100: Initial deskew width = 5 x 32k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX101: Initial deskew width = 6 x 32k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX110: Initial deskew width = 7 x 32k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX111: Initial deskew width = 8 x 32k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXX0XXX: Reserved</p> <p>0bXXXX1XXX: Reserved</p> <p>0bXXX0XXXX: Manual initial off</p> <p>0bXXX1XXXX: Manual initial on</p> <p>0bXX0XXXXX: If bit 4 = 1, triggers one-time immediate initial skew calibration</p> <p>0bX1XXXXXX: If bit 4 = 1, triggers one-time immediate initial skew calibration</p> <p>0bX0XXXXXX: Reserved</p> <p>0bX1XXXXXX: Reserved</p> <p>0b0XXXXXXX: Auto initial deskew off</p> <p>0b1XXXXXXX: Auto initial deskew on</p>

#### MIPI\_TX4 (0x444)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x01							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_P ER	7:0	<p>DPHY Periodic Deskew Calibration Control</p> <p>The register is split into four decode segments:</p> <p>bit[7] Selects periodic deskew calibration on or off</p> <p>bit[6] Selects generation on rising or falling edge of VS</p> <p>bits[5:3] Selects periodic interval</p> <p>bits[2:0] Selects periodic deskew width</p>	<p>0bXXXXX000: Reserved</p> <p>0bXXXXX001: Periodic deskew width = 2k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX010: Periodic deskew width = 3k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX011: Periodic deskew width = 4k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX100: Periodic deskew width = 5k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX101: Periodic deskew width = 6k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX110: Periodic deskew width = 7k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX111: Periodic deskew width = 8k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXX000XXX: Periodic deskew calibration generated every frame</p> <p>0bXX001XXX: Periodic deskew calibration generated every 2 frames</p> <p>0bXX010XXX: Periodic deskew calibration generated every 4 frames</p> <p>0bXX011XXX: Periodic deskew calibration generated every 8 frames</p> <p>0bXX100XXX: Periodic deskew calibration generated every 16 frames</p> <p>0bXX101XXX: Periodic deskew calibration generated every 32 frames</p> <p>0bXX110XXX: Periodic deskew calibration generated every 64 frames</p> <p>0bXX111XXX: Periodic deskew calibration generated every 128 frames</p> <p>0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS</p> <p>0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS</p> <p>0b0XXXXXXX: Periodic deskew calibration off</p> <p>0b1XXXXXXX: Periodic deskew calibration on</p>

**MIPI\_TX10 (0x44A)\***

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	RSVD	CSI_VCX_EN	RSVD[2:0]		
Reset	0b11		0b0	0b1	0b0	0b000		
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	Set number of MIPI data lanes	<p>0b00: One data lane</p> <p>0b01: Two data lanes</p> <p>0b10: Three data lanes</p> <p>0b11: Four data lanes</p>
CSI2_CPHY_EN	5	Enable CPHY	<p>0b0: CPHY disabled</p> <p>0b1: CPHY enabled</p>
CSI_VCX_EN	3	Enable VC Extension	<p>0b0: Disabled</p> <p>0b1: Enabled</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX11 (0x44B)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	<p>Mapping Enable Low Byte [7:0]</p> <p>Each bit enables one of eight mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream.</p> <p>Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.</p> <p>In video pixel mode, this is used to change any VC, DT, CSI2 controller destination.</p>	<p>0xX1: Enable MAP_SRC_0 (0x44D) and MAP_DST_0 (0x44E) bitfields</p> <p>0xX2: Enable MAP_SRC_1 (0x44F) and MAP_DST_1 (0x450) bitfields</p> <p>0xX4: Enable MAP_SRC_2 (0x451) and MAP_DST_2 (0x452) bitfields</p> <p>0xX8: Enable MAP_SRC_3 (0x453) and MAP_DST_3 (0x454) bitfields</p> <p>0x1X: Enable MAP_SRC_4 (0x455) and MAP_DST_4 (0x456) bitfields</p> <p>0x2X: Enable MAP_SRC_5 (0x457) and MAP_DST_5 (0x458) bitfields</p> <p>0x4X: Enable MAP_SRC_6 (0x459) and MAP_DST_6 (0x45A) bitfields</p> <p>0x8X: Enable MAP_SRC_7 (0x45B) and MAP_DST_7 (0x45C) bitfields</p>

**MIPI\_TX12 (0x44C)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	<p>Mapping Enable High Byte [15:8]</p> <p>Each bit enables one of eight mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream.</p> <p>Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.</p> <p>In video pixel mode, this is used to change any VC, DT, CSI2 controller destination.</p>	<p>ValueEnumerationDecode</p> <p>0xX1: Enable MAP_SRC_8 (0x45D) and MAP_DST_8 (0x45E) bitfields</p> <p>0xX2: Enable MAP_SRC_9 (0x45F) and MAP_DST_9 (0x460) bitfields</p> <p>0xX4: Enable MAP_SRC_10 (0x461) and MAP_DST_10 (0x462) bitfields</p> <p>0xX8: Enable MAP_SRC_11 (0x463) and MAP_DST_11 (0x464) bitfields</p> <p>0x1X: Enable MAP_SRC_12 (0x465) and MAP_DST_12 (0x466) bitfields</p> <p>0x2X: Enable MAP_SRC_13 (0x467) and MAP_DST_13 (0x468) bitfields</p> <p>0x4X: Enable MAP_SRC_14 (0x469) and MAP_DST_14 (0x46A) bitfields</p> <p>0x8X: Enable MAP_SRC_15 (0x46B) and MAP_DST_15 (0x46C) bitfields</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX13 (0x44D)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Mapping Source Register 0  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 0

**MIPI\_TX14 (0x44E)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Mapping Destination Register 0  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 0

**MIPI\_TX15 (0x44F)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Mapping Source Register 1  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 1

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[MIPI\\_TX16 \(0x450\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Mapping Destination Register 1  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 1

[MIPI\\_TX17 \(0x451\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Mapping Source Register 2  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 2

[MIPI\\_TX18 \(0x452\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Mapping Destination Register 2  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 2

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[MIPI\\_TX19 \(0x453\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Mapping Source Register 3  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 3

[MIPI\\_TX20 \(0x454\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Mapping Destination Register 3  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 3

[MIPI\\_TX21 \(0x455\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Mapping Source Register 4  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 4

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[MIPI\\_TX22 \(0x456\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Mapping Destination Register 4  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 4

[MIPI\\_TX23 \(0x457\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Mapping Source Register 5  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 5

[MIPI\\_TX24 \(0x458\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Mapping Destination Register 5  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 5



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MIPI\_TX25 (0x459)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Mapping Source Register 6  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 6

MIPI\_TX26 (0x45A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Mapping Destination Register 6  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 6

MIPI\_TX27 (0x45B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Mapping Source Register 7  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 7

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX28 (0x45C)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Mapping Destination Register 7  The register is split into two decode segments: bits [7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 7

**MIPI\_TX29 (0x45D)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Mapping Source Register 8  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 8

**MIPI\_TX30 (0x45E)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Mapping Destination Register 8  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 8

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX31 (0x45F)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Mapping Source Register 9  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 9

**MIPI\_TX32 (0x460)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Mapping Destination Register 9  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 9

**MIPI\_TX33 (0x461)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Mapping Source Register 10  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 10

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MIPI\_TX34 (0x462)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Mapping Destination Register 10  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 10

MIPI\_TX35 (0x463)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Mapping Source Register 11  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 11

MIPI\_TX36 (0x464)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Mapping Destination Register 11  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 11

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[MIPI\\_TX37 \(0x465\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Mapping Source Register 12  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 12

[MIPI\\_TX38 \(0x466\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Mapping Destination Register 12  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 12

[MIPI\\_TX39 \(0x467\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Mapping Source Register 13  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 13

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MIPI\_TX40 (0x468)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Mapping Destination Register 13  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 13

MIPI\_TX41 (0x469)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Mapping Source Register 14  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 14

MIPI\_TX42 (0x46A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Mapping Destination Register 14  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 14

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX43 (0x46B)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEN	BITS	DESCRIPTION			DECODE			
MAP_SRC_15	7:0	Mapping Source Register 15  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type			0xXX: VC and DT source for map 15			

**MIPI\_TX44 (0x46C)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEN	BITS	DESCRIPTION			DECODE			
MAP_DST_15	7:0	Mapping Destination Register 15  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type			0xXX: VC and DT destination for map 15			

**MIPI\_TX45 (0x46D)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	CSI2 controller destination for MAP_SRC_3 (0x453) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_2	5:4	CSI2 controller destination for MAP_SRC_2 (0x451) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_1	3:2	CSI2 controller destination for MAP_SRC_1 (0x44F) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_0	1:0	CSI2 controller destination for MAP_SRC_0 (0x44D) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

**MIPI\_TX46 (0x46E)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	CSI2 controller destination for MAP_SRC_7 (0x45B) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_6	5:4	CSI2 controller destination for MAP_SRC_6 (0x459) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_5	3:2	CSI2 controller destination for MAP_SRC_5 (0x457) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_4	1:0	CSI2 controller destination for MAP_SRC_4 (0x455) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

**MIPI\_TX47 (0x46F)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	CSI2 controller destination for MAP_SRC_11 (0x463) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_10	5:4	CSI2 controller destination for MAP_SRC_10 (0x461) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_9	3:2	CSI2 controller destination for MAP_SRC_9 (0x45F) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITLEFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_8	1:0	CSI2 controller destination for MAP_SRC_8 (0x45D) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

**MIPI\_TX48 (0x470)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITLEFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	CSI2 controller destination for MAP_SRC_15 (0x46B) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_14	5:4	CSI2 controller destination for MAP_SRC_14 (0x469) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_13	3:2	CSI2 controller destination for MAP_SRC_13 (0x467) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_12	1:0	CSI2 controller destination for MAP_SRC_12 (0x465) and MAP_DST_0 (0x44E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

**MIPI\_TX50 (0x472)**

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	<p>Periodic Deskew Select Register</p> <p>The register is split into three decode segments:</p> <p>bit[7] Select periodic deskew calibration for one or all virtual channels</p> <p>bits[6:5] Reserved</p> <p>bits[4:0] Virtual channel to generate periodic deskew calibration when only one channel is selected by bit 7</p>	<p>0b0XXXXXXX: Generate periodic calibration deskew calibration on all Virtual Channels</p> <p>0b1XXX0000: Periodic deskew calibration generated by Virtual Channel 0</p> <p>0b1XXX0001: Periodic deskew calibration generated by Virtual Channel 1</p> <p>0b1XXX0010: Periodic deskew calibration generated by Virtual Channel 2</p> <p>0b1XXX0011: Periodic deskew calibration generated by Virtual Channel 3</p> <p>0b1XXX0100: Periodic deskew calibration generated by Virtual Channel 4</p> <p>0b1XXX0101: Periodic deskew calibration generated by Virtual Channel 5</p> <p>0b1XXX0110: Periodic deskew calibration generated by Virtual Channel 6</p> <p>0b1XXX0111: Periodic deskew calibration generated by Virtual Channel 7</p> <p>0b1XXX1000: Periodic deskew calibration generated by Virtual Channel 8</p> <p>0b1XXX1001: Periodic deskew calibration generated by Virtual Channel 9</p> <p>0b1XXX1010: Periodic deskew calibration generated by Virtual Channel 10</p> <p>0b1XXX1011: Periodic deskew calibration generated by Virtual Channel 11</p> <p>0b1XXX1100: Periodic deskew calibration generated by Virtual Channel 12</p> <p>0b1XXX1101: Periodic deskew calibration generated by Virtual Channel 13</p> <p>0b1XXX1110: Periodic deskew calibration generated by Virtual Channel 14</p> <p>0b1XXX1111: Periodic deskew calibration generated by Virtual Channel 15</p>

**MIPI\_TX51 (0x473)\***

BIT	7	6	5	4	3	2	1	0
Field	TUN_WAIT_VS_START[2:0]			ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	0x0			0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_WAIT_VS_START	7:5	<p>Number of VS frames to wait before sending MIPI packet</p> <p>Tunneling mode only.</p>	<p>0x0: No wait</p> <p>Others: Number of frames to wait</p>
ALT2_MEM_MAP8	4	Alternative memory map enable for 8-bit DT. When set to 1, expects received video data to be packed into 24-bit in an alternative way by the serializer.	<p>0b0: Alternate memory map disabled</p> <p>0b1: Alternate memory map enabled</p>
MODE_DT	3	MIPI Tx enable 24-bit packing of 8-bit MIPI UDP	<p>0b0: Disabled</p> <p>0b1: Enabled</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_MEM_MAP10	2	Alternative memory map enable for 10-bit DT (expect alternative bit packing by serializer)	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP8	1	Alternative memory map enable for 8-bit DT (expect alternative bit packing by serializer)	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP12	0	Alternative memory map enable for 12-bit DT (expect alternative bit packing by serializer)	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled

**MIPI\_TX52 (0x474)\***

BIT	7	6	5	4	3	2	1	0
Field	TUN_NO_C ORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1: 0]		DESKEW_T UN_SRC	TUN_DEST	TUN_EN
Reset	0b0	0x0		0x1		0b0	0b0	0b0
Access Type	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_NO_C ORR	7	Do not enable header error correction in tunneling mode	0b0: Tunneling error correction enabled 0b1: Tunneling error correction disabled
DESKEW_T UN	6:5	Deskew Mode for CSI2 Tunneling	0b00: Periodic deskew using deserializer DESKEW_PER register 0b01: Periodic deskew follows what Serializer receives with small offset adjustment by DESKEW_TUN_OFFSET. 0b10: Periodic deskew occurrence follows Serializer but width determined by register DESKEW_PER 0b11: Reserved
TUN_SER_L ANE_NUM	4:3	Number of lanes in the serializer. Applies to CSI2 tunneling mode only, and CPHY mode only.	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes 0b11: Four data lanes
DESKEW_T UN_SRC	2	Tunneling Deskew Source Select	0b0: Pipe Y 0b1: Pipe Z
TUN_DEST	1	Tunneling Pipe Destination	0b0: MIPI PHY 1 0b1: MIPI PHY 2
TUN_EN	0	Tunneling Enable  The CFG pin sets this value initially, and further register writes to this register changes the value.	0b0: Tunneling disabled 0b1: Tunneling enabled

**MIPI\_TX53 (0x475)\***

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_TUN_OFFSET[7:0]							
Reset	0x0							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_TUN_OFFSET	7:0	Tunneling Deskew Width Offset	Used for DESKEW_TUN=1 case: increase this number of BCLK (8UI) to the detected deskew pulse width.

**MIPI\_TX54 (0x476)\***

BIT	7	6	5	4	3	2	1	0
Field	TUN_PKT_START_ADDR[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TUN_PKT_START_ADDR	7:0	Specifies the start address of the long packet in tunneling mode.  When 0, the long packet is sent out when the whole line is filled in the line memory. When not 0, the long packet begins when TUN_PKT_START_ADDR x 32 bytes are filled in the line memory.

**MIPI\_TX55 (0x477)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	TUN_NO_CORR_LENGTH
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_NO_CORR_LENGTH	0	Do not enable header error packet length correction in tunneling mode	0b0: Tunneling error correction enabled 0b1: Tunneling error correction disabled

**MIPI\_TX1 (0x481)\***

BIT	7	6	5	4	3	2	1	0
Field	MODE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	7:0	MIPI Tx Mode	0bXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXX1: Enable MIPI VS short packet counter

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MIPI\_TX2 (0x482)

BIT	7	6	5	4	3	2	1	0
Field	STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
STATUS	7:0	<p>MIPI Tx Status</p> <p>The register is split into decode segments:</p> <p>bit[0] SYNC mode enable.</p> <p>bit[1] Video sync flag</p> <p>bit[2] Loss of video sync flag</p> <p>bit[3] Tunneling mode: DPHY ECC or CPHY header CRC error (correctable)</p> <p>bit[4] Tunneling mode: DPHY ECC or CPHY header CRC error (uncorrectable)</p> <p>bit[5] Tunneling mode: DPHY/CPHY data CRC error</p>	<p>0bXXXXXXXX0: SYNC mode disabled</p> <p>0bXXXXXXXX1: SYNC mode enabled</p> <p>0bXXXXXXXX0X: Video channels not in-sync</p> <p>0bXXXXXXXX1X: Video channels in-sync</p> <p>0bXXXXX0XX: No loss of video sync</p> <p>0bXXXXX1XX: Video sync lost after last read of this register or RESET.</p> <p>0bXXXXX0XXX: No tunneling ECC correctable error</p> <p>0bXXXXX1XXX: Tunneling ECC correctable error after last read of this register or RESET.</p> <p>0bXXX0XXXX: No tunneling ECC uncorrectable error</p> <p>0bXXX1XXXX: Tunneling ECC uncorrectable error after last read of this register or RESET.</p> <p>0bXX0XXXXX: No tunneling data CRC error</p> <p>0bXX1XXXXX: Tunneling data CRC error after last read of this register or RESET.</p>

MIPI\_TX3 (0x483)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x01							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_IN IT	7:0	<p>DPHY DeskeW Initial Calibration Control</p> <p>The register is split into six decode segments:</p> <p>bit[7] Selects auto-initial deskeW calibration on or off</p> <p>bit[6] Reserved</p> <p>bit[5] Any bit change initiates an initial calibration if bit 4 =1</p> <p>bit[4] Selects manual initial on or off</p> <p>bit[3] Reserved</p> <p>bits[2:0] Selects initial deskeW width</p>	<p>0bXXXXXX000: Reserved</p> <p>0bXXXXXX001: Initial deskeW width = 2 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI</p> <p>0bXXXXXX010: Initial deskeW width = 3 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI</p> <p>0bXXXXXX011: Initial deskeW width = 4 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI</p> <p>0bXXXXXX100: Initial deskeW width = 5 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI</p> <p>0bXXXXXX101: Initial deskeW width = 6 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI</p> <p>0bXXXXXX110: Initial deskeW width = 7 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI</p> <p>0bXXXXXX111: Initial deskeW width = 8 x 32k UI - (t_lpx+t_hs_przero)[UI] - 16 UI</p> <p>0bXXXXX0XXX: Reserved</p> <p>0bXXXXX1XXX: Reserved</p> <p>0bXXX0XXXX: Manual initial off</p> <p>0bXXX1XXXX: Manual initial on</p> <p>0bXX0XXXXX: If bit 4 = 1, triggers one-time immediate initial skew calibration</p> <p>0bXX1XXXXX: If bit 4 = 1, triggers one-time immediate initial skew calibration</p> <p>0bX0XXXXXX: Reserved</p> <p>0bX1XXXXXX: Reserved</p> <p>0b0XXXXXXX: Auto initial deskeW off</p> <p>0b1XXXXXXX: Auto initial deskeW on</p>

#### MIPI\_TX4 (0x484)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x01							
Access Type	Write, Read							



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_P ER	7:0	<p>DPHY Periodic Deskew Calibration Control</p> <p>The register is split into four decode segments:</p> <p>bit[7] Selects periodic deskew calibration on or off</p> <p>bit[6] Selects generation on rising or falling edge of VS</p> <p>bits[5:3] Selects periodic interval</p> <p>bits[2:0] Selects periodic deskew width</p>	<p>0bXXXXX000: Reserved</p> <p>0bXXXXX001: Periodic deskew width = 2k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX010: Periodic deskew width = 3k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX011: Periodic deskew width = 4k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX100: Periodic deskew width = 5k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX101: Periodic deskew width = 6k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX110: Periodic deskew width = 7k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXXXXX111: Periodic deskew width = 8k UI - (t<sub>lpx</sub>+t<sub>hs_przero</sub>)[UI] - 16 UI</p> <p>0bXX000XXX: Periodic deskew calibration generated every frame</p> <p>0bXX001XXX: Periodic deskew calibration generated every 2 frames</p> <p>0bXX010XXX: Periodic deskew calibration generated every 4 frames</p> <p>0bXX011XXX: Periodic deskew calibration generated every 8 frames</p> <p>0bXX100XXX: Periodic deskew calibration generated every 16 frames</p> <p>0bXX101XXX: Periodic deskew calibration generated every 32 frames</p> <p>0bXX110XXX: Periodic deskew calibration generated every 64 frames</p> <p>0bXX111XXX: Periodic deskew calibration generated every 128 frames</p> <p>0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS</p> <p>0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS</p> <p>0b0XXXXXXX: Periodic deskew calibration off</p> <p>0b1XXXXXXX: Periodic deskew calibration on</p>

**MIPI\_TX10 (0x48A)\***

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	RSVD	CSI_VCX_EN	RSVD[2:0]		
Reset	0b11		0b0	0b1	0b0	0b000		
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	Set number of MIPI data lanes	<p>0b00: One data lane</p> <p>0b01: Two data lanes</p> <p>0b10: Three data lanes</p> <p>0b11: Four data lanes</p>
CSI2_CPHY_EN	5	Enable CPHY	<p>0b0: CPHY disabled</p> <p>0b1: CPHY enabled</p>
CSI_VCX_EN	3	Enable VC Extension	<p>0b0: Disable VC extension</p> <p>0x1: Enable VC extension</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX11 (0x48B)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	<p>Mapping Enable Low Byte [7:0]</p> <p>Each bit enables one of eight mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream.</p> <p>Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.</p> <p>In video pixel mode, this is use to change any VC, DT, CSI2 controller destination.</p>	<p>0xX1: Enable MAP_SRC_0 (0x48D) and MAP_DST_0 (0x48E) bitfields</p> <p>0xX2: Enable MAP_SRC_1 (0x48F) and MAP_DST_1 (0x490) bitfields</p> <p>0xX4: Enable MAP_SRC_2 (0x491) and MAP_DST_2 (0x492) bitfields</p> <p>0xX8: Enable MAP_SRC_3 (0x493) and MAP_DST_3 (0x494) bitfields</p> <p>0x1X: Enable MAP_SRC_4 (0x495) and MAP_DST_4 (0x496) bitfields</p> <p>0x2X: Enable MAP_SRC_5 (0x497) and MAP_DST_5 (0x498) bitfields</p> <p>0x4X: Enable MAP_SRC_6 and (0x499) and MAX_DST_6 (0x49A) bitfields</p> <p>0x8X: Enable MAP_SRC_7 (0x49B) and MAP_DST_7 (0x49C) bitfields</p>

**MIPI\_TX12 (0x48C)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	<p>Mapping Enable High Byte [15:8]</p> <p>Each bit enables one of eight mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream.</p> <p>Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.</p> <p>In video pixel mode, this is use to change any VC, DT, CSI2 controller destination.</p>	<p>0xX1: Enable MAP_SRC_8 (0x49D) and MAP_DST_8 (0x49E) bitfields</p> <p>0xX2: Enable MAP_SRC_9 (0x49F) and MAP_DST_9 (0x4A0) bitfields</p> <p>0xX4: Enable MAP_SRC_10 (0x4A1) and MAP_DST_10 (0x4A2) bitfields</p> <p>0xX8: Enable MAP_SRC_11 (0x4A3) and MAP_DST_11 (0x4A4) bitfields</p> <p>0x1X: Enable MAP_SRC_12 (0x4A5) and MAP_DST_12 (0x4A6) bitfields</p> <p>0x2X: Enable MAP_SRC_13 (0x4A7) and MAP_DST_13 (0x4A8) bitfields</p> <p>0x4X: Enable MAP_SRC_14 (0x4A9) and MAP_DST_14 (0x4AA) bitfields</p> <p>0x8X: Enable MAP_SRC_15 (0x4AB) and MAP_DST_15 (x4AC) bitfields</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX13 (0x48D)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Mapping Source Register 0  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 0

**MIPI\_TX14 (0x48E)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Mapping Destination Register 0  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 0

**MIPI\_TX15 (0x48F)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Mapping Source Register 1  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 1

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX16 (0x490)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Mapping Destination Register 1  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 1

**MIPI\_TX17 (0x491)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Mapping Source Register 2  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 2

**MIPI\_TX18 (0x492)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Mapping Destination Register 2  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 2

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MIPI\_TX19 (0x493)\*

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Mapping Source Register 3  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 3

MIPI\_TX20 (0x494)\*

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Mapping Destination Register 3  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 3

MIPI\_TX21 (0x495)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Mapping Source Register 4  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 4

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[MIPI\\_TX22 \(0x496\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Mapping Destination Register 4  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 4

[MIPI\\_TX23 \(0x497\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Mapping Source Register 5  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 5

[MIPI\\_TX24 \(0x498\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Mapping Destination Register 5  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 5

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[MIPI\\_TX25 \(0x499\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Mapping Source Register 6  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 6

[MIPI\\_TX26 \(0x49A\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Mapping Destination Register 6  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 6

[MIPI\\_TX27 \(0x49B\)](#)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Mapping Source Register 7  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 7



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX28 (0x49C)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Mapping Destination Register 7  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 7

**MIPI\_TX29 (0x49D)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Mapping Source Register 8  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 8

**MIPI\_TX30 (0x49E)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Mapping Destination Register 8  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 8

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX31 (0x49F)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Mapping Source Register 9  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 9

**MIPI\_TX32 (0x4A0)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Mapping Destination Register 9  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 9

**MIPI\_TX33 (0x4A1)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Mapping Source Register 10  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 10

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX34 (0x4A2)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Mapping Destination Register 10  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 10

**MIPI\_TX35 (0x4A3)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Mapping Source Register 11  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 11

**MIPI\_TX36 (0x4A4)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Mapping Destination Register 11  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 11

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX37 (0x4A5)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Mapping Source Register 12  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 12

**MIPI\_TX38 (0x4A6)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Mapping Destination Register 12  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT destination for map 12

**MIPI\_TX39 (0x4A7)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Mapping Source Register 13  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type	0xXX: VC and DT source for map 13

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX40 (0x4A8)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEVEL	BITS	DESCRIPTION			DECODE			
MAP_DST_13	7:0	Mapping Destination Register 13  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type			0xXX: VC and DT destination for map 13			

**MIPI\_TX41 (0x4A9)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEVEL	BITS	DESCRIPTION			DECODE			
MAP_SRC_14	7:0	Mapping Source Register 14  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type			0xXX: VC and DT source for map 14			

**MIPI\_TX42 (0x4AA)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEVEL	BITS	DESCRIPTION			DECODE			
MAP_DST_14	7:0	Mapping Destination Register 14  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type			0xXX: VC and DT destination for map 14			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX43 (0x4AB)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEN	BITS	DESCRIPTION			DECODE			
MAP_SRC_15	7:0	Mapping Source Register 15  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type			0xXX: VC and DT source for map 15			

**MIPI\_TX44 (0x4AC)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITLEN	BITS	DESCRIPTION			DECODE			
MAP_DST_15	7:0	Mapping Destination Register 15  The register is split into two decode segments: bits[7:6] VC - Virtual channel bits[5:0] DT - Data type			0xXX: VC and DT destination for map 15			

**MIPI\_TX45 (0x4AD)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	CSI2 controller destination for MAP_SRC_3 (0x493) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_2	5:4	CSI2 controller destination for MAP_SRC_2 (0x491) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_1	3:2	CSI2 controller destination for MAP_SRC_1 (0x48F) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_0	1:0	CSI2 controller destination for MAP_SRC_0 (0x48D) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

**MIPI\_TX46 (0x4AE)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	CSI2 controller destination for MAP_SRC_7 (0x49B) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_6	5:4	CSI2 controller destination for MAP_SRC_6 (0x499) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_5	3:2	CSI2 controller destination for MAP_SRC_5 (0x497) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_4	1:0	CSI2 controller destination for MAP_SRC_4 (0x495) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

**MIPI\_TX47 (0x4AF)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	CSI2 controller destination for MAP_SRC_11 (0x4A3) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_10	5:4	CSI2 controller destination for MAP_SRC_10 (0x4A1) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_9	3:2	CSI2 controller destination for MAP_SRC_9 (0x49F) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_8	1:0	CSI2 controller destination for MAP_SRC_8 (0x49D) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

**MIPI\_TX48 (0x4B0)\***

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	CSI2 controller destination for MAP_SRC_15 (0x4AB) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_14	5:4	CSI2 controller destination for MAP_SRC_14 (0x4A9) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_13	3:2	CSI2 controller destination for MAP_SRC_13 (0x4A8) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)
MAP_DPHY_DEST_12	1:0	CSI2 controller destination for MAP_SRC_12 (0x4A6) and MAP_DST_0 (0x48E) mapping bitfields	0b00: Map to DPHY0 (4x2 mode only) 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3 (4x2 mode only)

**MIPI\_TX50 (0x4B2)**

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	<p>Periodic Deskew Select Register</p> <p>The register is split into three decode segments:</p> <p>bit[7] Select periodic deskew calibration for one or all virtual channels</p> <p>bits[6:5] Reserved</p> <p>bits[4:0] Virtual channel to generate periodic deskew calibration when only one channel is selected by bit 7</p>	<p>0b0XXXXXXX: Generate periodic calibration deskew calibration on all virtual channels</p> <p>0b1XXX0000: Periodic deskew calibration generated by virtual channel 0</p> <p>0b1XXX0001: Periodic deskew calibration generated by virtual channel 1</p> <p>0b1XXX0010: Periodic deskew calibration generated by virtual channel 2</p> <p>0b1XXX0011: Periodic deskew calibration generated by virtual channel 3</p> <p>0b1XXX0100: Periodic deskew calibration generated by virtual channel 4</p> <p>0b1XXX0101: Periodic deskew calibration generated by virtual channel 5</p> <p>0b1XXX0110: Periodic deskew calibration generated by virtual channel 6</p> <p>0b1XXX0111: Periodic deskew calibration generated by virtual channel 7</p> <p>0b1XXX1000: Periodic deskew calibration generated by virtual channel 8</p> <p>0b1XXX1001: Periodic deskew calibration generated by virtual channel 9</p> <p>0b1XXX1010: Periodic deskew calibration generated by virtual channel 10</p> <p>0b1XXX1011: Periodic deskew calibration generated by virtual channel 11</p> <p>0b1XXX1100: Periodic deskew calibration generated by virtual channel 12</p> <p>0b1XXX1101: Periodic deskew calibration generated by virtual channel 13</p> <p>0b1XXX1110: Periodic deskew calibration generated by virtual channel 14</p> <p>0b1XXX1111: Periodic deskew calibration generated by virtual channel 15</p>

#### MIPI\_TX51 (0x4B3)

BIT	7	6	5	4	3	2	1	0
Field	TUN_WAIT_VS_START[2:0]			ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	0x0			0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_WAIT_VS_START	7:5	<p>Number of VS frames to wait before sending MIPI packet</p> <p>Tunneling mode only.</p>	<p>0x0: No wait</p> <p>Others: Number of frames to wait</p>
ALT2_MEM_MAP8	4	Alternative memory map enable for 8-bit DT. When set to 1, expects received video data to be packed into 24-bit in an alternative way by the serializer.	<p>0b0: Alternate memory map disabled</p> <p>0b1: Alternate memory map enabled</p>
MODE_DT	3	MIPI Tx enable 24-bit packing of 8-bit MIPI UDP	<p>0b0: Disabled</p> <p>0b1: Enabled</p>

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_MEM_MAP10	2	Alternative memory map enable for 10-bit DT (expect alternative bit packing by serializer)	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP8	1	Alternative memory map enable for 8-bit DT (expect alternative bit packing by serializer)	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP12	0	Alternative memory map enable for 12-bit DT (expect alternative bit packing by serializer)	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled

**MIPI\_TX52 (0x4B4)\***

BIT	7	6	5	4	3	2	1	0
Field	TUN_NO_C ORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1: 0]		DESKEW_T UN_SRC	TUN_DEST	TUN_EN
Reset	0b0	0x0		0x1		0b1	0b1	0b0
Access Type	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_NO_C ORR	7	Do not enable header error correction in tunneling mode	0b0: Tunneling error correction enabled 0b1: Tunneling error correction disabled
DESKEW_T UN	6:5	Deskew Mode for CSI2 Tunneling	0b00: Periodic deskew using deserializer DESKEW_PER register 0b01: Periodic deskew follows what Serializer receives with small offset adjustment by DESKEW_TUN_OFFSET. 0b10: Periodic deskew occurrence follows Serializer but width determined by register DESKEW_PER 0b11: Reserved
TUN_SER_L ANE_NUM	4:3	Number of lanes in the serializer. Applies to CSI2 tunneling mode only, and CPHY mode only.	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes 0b11: Four data lanes
DESKEW_T UN_SRC	2	Tunneling Deskew Source Select	0b0: Pipe Y 0b1: Pipe Z
TUN_DEST	1	Tunneling Pipe Destination	0b0: MIPI PHY 1 0b1: MIPI PHY 2
TUN_EN	0	Tunneling Enabled  The CFG pin sets this value initially, and further register writes to this register changes the value.	0b0: Tunneling disabled 0b1: Tunneling enabled

**MIPI\_TX53 (0x4B5)\***

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_TUN_OFFSET[7:0]							
Reset	0x0							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_TUN_OFFSET	7:0	Tunneling Deskew Width Offset	Used for DESKEW_TUN=1 case: increase this number of BCLK (8UI) to the detected deskew pulse width.

**MIPI\_TX54 (0x4B6)\***

BIT	7	6	5	4	3	2	1	0
Field	TUN_PKT_START_ADDR[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TUN_PKT_START_ADDR	7:0	Specifies the start address of the long packet in tunneling mode.  When 0, the long packet is sent out when the whole line is filled in line memory. When not 0, the long packet begins when TUN_PKT_START_ADDR x 32 bytes are filled in the line memory.

**MIPI\_TX55 (0x4B7)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	TUN_NO_CORR_LENGTH
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_NO_CORR_LENGTH	0	Do not enable header error packet length correction in tunneling mode	0b0: Tunneling error correction enabled 0b1: Tunneling error correction disabled

**MIPI\_TX10 (0x4CA)\***

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	RSVD	–	–	–	–
Reset	0b11		0b0	0b1	–	–	–	–
Access Type	Write, Read		Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	Set number of MIPI data lanes	0b00: One data lane for port 0b01: Two data lanes for port 0b10: Three data lanes for port 0b11: Four data lanes for port
CSI2_CPHY_EN	5	Enable CPHY	0b0: CPHY disabled 0b1: CPHY enabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX\_EXT0 (0x510)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_0_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_0_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT1 (0x511)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_1_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_1_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT2 (0x512)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_2_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_2_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT3 (0x513)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_3_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_3_H	4:2	Mapping register destination VC high 3 bits for extended mode

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

MIPI\_TX\_EXT4 (0x514)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_4_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_4_H	4:2	Mapping register destination VC high 3 bits for extended mode

MIPI\_TX\_EXT5 (0x515)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_5_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_5_H	4:2	Mapping register destination VC high 3 bits for extended mode

MIPI\_TX\_EXT6 (0x516)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_6_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_6_H	4:2	Mapping register destination VC high 3 bits for extended mode

MIPI\_TX\_EXT7 (0x517)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_7_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_7_H	4:2	Mapping register destination VC high 3 bits for extended mode

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX\_EXT8 (0x518)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_8_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_8_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT9 (0x519)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_9_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_9_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT10 (0x51A)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_10_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_10_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT11 (0x51B)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_11_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_11_H	4:2	Mapping register destination VC high 3 bits for extended mode



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX\_EXT12 (0x51C)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_12_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_12_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT13 (0x51D)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_13_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_13_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT14 (0x51E)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_14_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_14_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT15 (0x51F)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_15_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_15_H	4:2	Mapping register destination VC high 3 bits for extended mode

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX\_EXT0 (0x520)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_0_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_0_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT1 (0x521)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_1_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_1_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT2 (0x522)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_2_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_2_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT3 (0x523)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_3_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_3_H	4:2	Mapping register destination VC high 3 bits for extended mode

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX\_EXT4 (0x524)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_4_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_4_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT5 (0x525)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_5_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_5_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT6 (0x526)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_6_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_6_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT7 (0x527)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_7_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_7_H	4:2	Mapping register destination VC high 3 bits for extended mode

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX\_EXT8 (0x528)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_8_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_8_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT9 (0x529)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_9_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_9_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT10 (0x52A)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_10_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_10_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT11 (0x52B)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_11_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_11_H	4:2	Mapping register destination VC high 3 bits for extended mode

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**MIPI\_TX\_EXT12 (0x52C)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_12_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_12_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT13 (0x52D)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_13_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_13_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT14 (0x52E)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_14_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_14_H	4:2	Mapping register destination VC high 3 bits for extended mode

**MIPI\_TX\_EXT15 (0x52F)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION
MAP_SRC_15_H	7:5	Mapping register source VC high 3 bits for extended mode
MAP_DST_15_H	4:2	Mapping register destination VC high 3 bits for extended mode

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

CFG\_0 (0x540)

BIT	7	6	5	4	3	2	1	0
Field	VS_OUT1[2:0]			RSVD[4:0]				
Reset	0b000			0b00000				
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_OUT1	7:5	Output VSYNC from VS1 pin  MSB is enabled. LSB 2 bits select which video pipeline to output.	0x0: Reserved 0x1: From Video Pipeline Y 0x2: From Video Pipeline Z 0x3: Reserved

CFG\_1 (0x541)

BIT	7	6	5	4	3	2	1	0
Field	VS_OUT2[2:0]			RSVD[4:0]				
Reset	0b000			0b00000				
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_OUT2	7:5	Output VSYNC from VS2 pin  MSB is enabled. LSB 2 bits select which video pipeline to output.	0x0: Reserved 0x1: From Video Pipeline Y 0x2: From Video Pipeline Z 0x3: Reserved

CFG\_2 (0x542)

BIT	7	6	5	4	3	2	1	0
Field	HS_OUT1[2:0]			RSVD[4:0]				
Reset	0b000			0b00000				
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_OUT1	7:5	Output DE/DV from HS1 pin  MSB is enabled. LSB 2 bits select which video pipeline to output.	0x0: Reserved 0x1: From Video Pipeline Y 0x2: From Video Pipeline Z 0x3: Reserved

UART\_PT\_0 (0x548)\*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_1_L[7:0]							
Reset	0x96							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_L	7:0	<p>Custom UART bit length for pass-through UART Channel 1</p> <p>Set BITLEN_MAN_CFG_1 (0x4F) to 1 to use this value.</p> <p>Set this register to the UART bit length divided by 6.666ns (LSB 8 bits)</p>	0xXX: Low byte of custom UART bit length for pass-through UART Channel 1

UART\_PT\_1 (0x549)\*

BIT	7	6	5	4	3	2	1	0
Field	—	—	BITLEN_PT_1_H[5:0]					
Reset	—	—	0b000000					
Access Type	—	—	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_H	5:0	<p>High byte of custom UART bit length for pass-through UART Channel 1.</p> <p>Set BITLEN_MAN_CFG_1 (0x4F) to 1 to use this value.</p> <p>Set this register to the UART bit length divided by 6.666ns (LSB 8 bits).</p>	0xXX: High byte of custom UART bit length for pass-through UART Channel 1

UART\_PT\_2 (0x54A)\*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_2_L[7:0]							
Reset	0x96							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_L	7:0	<p>Low byte of custom UART bit length for pass-through UART Channel 2.</p> <p>Set BITLEN_MAN_CFG_2 (0x4F) to 1 to use this value.</p> <p>Set this register to the UART bit length divided by 6.666ns (LSB 8 bits).</p>	0xXX: Low byte of custom UART bit length for pass-through UART Channel 2

UART\_PT\_3 (0x54B)\*

BIT	7	6	5	4	3	2	1	0
Field	—	—	BITLEN_PT_2_H[5:0]					
Reset	—	—	0b000000					
Access Type	—	—	Write, Read					



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_H	5:0	High byte of custom UART bit length for pass-through UART Channel 2.  Set BITLEN_MAN_CFG_1 (0x4F) to 2 to use this value.  Set this register to the UART bit length divided by 6.666ns (LSB 8 bits).	0xXX: High byte of custom UART bit length for pass-through UART Channel 2

I2C\_PT\_4 (0x550)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_1[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
SRC_A_1	7:1	I <sup>2</sup> C address translator source A for pass-through 1 port  When an I <sup>2</sup> C transaction across the GMSL link has a device address matching I <sup>2</sup> C SRC_A_1, the device address as seen on the remote side is replaced by the device address in I <sup>2</sup> C DST_A_1.

I2C\_PT\_5 (0x551)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_1[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
DST_A_1	7:1	I <sup>2</sup> C address translator destination A for pass-through 1 port  See the description of SRC_A_1.

I2C\_PT\_6 (0x552)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_1[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
SRC_B_1	7:1	I <sup>2</sup> C address translator source B for pass-through 1 port  When an I <sup>2</sup> C transaction across the GMSL link has a device address matching I <sup>2</sup> C SRC_B_1, the device address as seen on the remote side is replaced by the device address in I <sup>2</sup> C DST_B_1.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

I2C\_PT\_7 (0x553)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_1[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
DST_B_1	7:1	I <sup>2</sup> C address translator destination B for pass-through port 1 See the description of SRC_B_1.

I2C\_PT\_8 (0x554)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_2[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
SRC_A_2	7:1	I <sup>2</sup> C address translator source A for pass-through 2 port When an I <sup>2</sup> C transaction across the GMSL link has a device address matching I <sup>2</sup> C SRC_A_2, the device address as seen on the remote side is replaced by the device address in I <sup>2</sup> C DST_A_2.

I2C\_PT\_9 (0x555)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_2[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
DST_A_2	7:1	I <sup>2</sup> C address translator destination A for pass-through 2 port See the description of SRC_A_2.

I2C\_PT\_10 (0x556)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_2[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
SRC_B_2	7:1	I <sup>2</sup> C address translator source B for pass-through 2 port  When an I <sup>2</sup> C transaction across the GMSL link has a device address matching I <sup>2</sup> C SRC_B_2, the device address as seen on the remote side is replaced by the device address in I <sup>2</sup> C DST_B_2.

#### I2C\_PT\_11 (0x557)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_2[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
DST_B_2	7:1	I <sup>2</sup> C address translator destination B for pass-through 2 port  See the description of SRC_B_2.

#### CNT4 (0x55C)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR0[7:0]							–
Reset	0x00							–
Access Type	Read Clears All							–

BITFIELD	BITS	DESCRIPTION
VID_PXL_CRC_ERR0	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK.

#### CNT5 (0x55D)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR1[7:0]							–
Reset	0x00							–
Access Type	Read Clears All							–

BITFIELD	BITS	DESCRIPTION
VID_PXL_CRC_ERR1	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK.

#### CNT6 (0x55E)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR2[7:0]							–
Reset	0x00							–
Access Type	Read Clears All							–

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
VID_PXL_CRC_ERR2	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK.

#### CNT7 (0x55F)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR3[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
VID_PXL_CRC_ERR3	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK.

#### PORT\_TUN\_ONLY (0x568)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TUN_ONLY_2	TUN_ONLY_1	TUN_ONLY_CC
Reset	–	–	–	–	–	0b1	0b1	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_ONLY_2	2	Disable control channel access from RX2/SDA2 and TX2/SCL2	0x0: CC and Tunnel 0x1: Tunnel only
TUN_ONLY_1	1	Disable control channel access from RX1/SDA1 and TX1/SCL1	0x0: CC and Tunnel 0x1: Tunnel only
TUN_ONLY_CC	0	Disable control channel access from RX/SDA and TX/SCL	0x0: CC and Tunnel 0x1: Tunnel only

#### UNLOCK\_KEY (0x569)\*

BIT	7	6	5	4	3	2	1	0
Field	UNLOCK_KEY[7:0]							
Reset	0xAA							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
UNLOCK_KEY	7:0	Register must be at unlock value to enable write access to port control pins DIS_LOCAL_CC, IIC_1_EN, IIC_2_EN, UART_1_EN, UART_2_EN, TUN_ONLY_CC, TUN_ONLY_1, and TUN_ONLY_2.  Defaults to unlocked.	0xAA: Unlock write access Others: Lock write access

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

PIO\_SLEW\_0 (0x570)\*

BIT	7	6	5	4	3	2	1	0
Field	PIO03_SLEW[1:0]		PIO02_SLEW[1:0]		PIO01_SLEW[1:0]		PIO00_SLEW[1:0]	
Reset	0b11		0b11		0b11		0b10	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
PIO03_SLEW	7:6	Rise and fall time speed setting on pad ring for this PIO. 00 value is the fastest rise and fall time, and 11 value is the slowest. This PIO corresponds to MFP3.
PIO02_SLEW	5:4	Rise and fall time speed setting on pad ring for this PIO. 00 value is the fastest rise and fall time, and 11 value is the slowest. This PIO corresponds to MFP2.
PIO01_SLEW	3:2	Rise and fall time speed setting on pad ring for this PIO. 00 value is the fastest rise and fall time, and 11 value is the slowest. This PIO corresponds to MFP1.
PIO00_SLEW	1:0	Rise and fall time speed setting on pad ring for this PIO. 00 value is the fastest rise and fall time, and 11 value is the slowest. This PIO corresponds to MFP0.

PIO\_SLEW\_1 (0x571)\*

BIT	7	6	5	4	3	2	1	0
Field	PIO07_SLEW[1:0]		–	–	–	–	PIO04_SLEW[1:0]	
Reset	0b10		–	–	–	–	0b11	
Access Type	Write, Read		–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
PIO07_SLEW	7:6	Rise and fall time speed setting on pad ring for this PIO. 00 value is the fastest rise and fall time, and 11 value is the slowest. This PIO corresponds to MFP5.
PIO04_SLEW	1:0	Rise and fall time speed setting on pad ring for this PIO. 00 value is the fastest rise and fall time, and 11 value is the slowest. This PIO corresponds to MFP4.

PIO\_SLEW\_2 (0x572)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PIO08_SLEW[1:0]	
Reset	–	–	–	–	–	–	0b10	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
PIO08_SLEW	1:0	Rise and fall time speed setting on pad ring for this PIO. 00 value is the fastest rise and fall time, and 11 value is the slowest. This PIO corresponds to MFP6.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

HS\_VS\_ACT\_Y (0x575)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET_Y	VS_DET_Y	HS_DET_Y	–	–	VS_POL_Y	HS_POL_Y
Reset	–	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITLED	BITS	DESCRIPTION	DECODE
DE_DET_Y	6	DE activity is detected	0x0: DE is not detected 0x1: DE is detected
VS_DET_Y	5	VS activity is detected	0x0: VS is not detected 0x1: VS is detected
HS_DET_Y	4	HS activity is detected	0x0: HS is not detected 0x1: HS is detected
VS_POL_Y	1	Detected VS polarity	0x0: Active low 0x1: Active high
HS_POL_Y	0	Detected HS polarity	0x0: Active low 0x1: Active high

HS\_VS\_ACT\_Z (0x576)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET_Z	VS_DET_Z	HS_DET_Z	–	–	VS_POL_Z	HS_POL_Z
Reset	–	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITLED	BITS	DESCRIPTION	DECODE
DE_DET_Z	6	DE activity is detected	0x0: DE is not detected 0x1: DE is detected
VS_DET_Z	5	VS activity is detected	0x0: VS is not detected 0x1: VS is detected
HS_DET_Z	4	HS activity is detected	0x0: HS is not detected 0x1: HS is detected
VS_POL_Z	1	Detected VS polarity	0x0: Active low 0x1: Active high
HS_POL_Z	0	Detected HS polarity	0x0: Active low 0x1: Active high

DP\_ORSTB\_CTL (0x577)\*

BIT	7	6	5	4	3	2	1	0
Field	–	DP_RST_M IPI3_CHKKB	DP_RST_S TABLE_CH KB	DP_RST_M IPI2_CHKKB	DP_RST_M IPI_CHKKB	DP_RST_V P_CHKKB	RSVD	RSVD
Reset	–	0b1	0b1	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
DP_RST_MIPI3_CHKBB	6	Select reset mode to MIPI controllers. This bit should be set to 1, if required, to have completely independent resets, and linkup of Link A and B.	0x0: Legacy 0x1: Enable auto reset of command FIFO read pointer (controls line memory output to MIPI TX) in MIPI TX
DP_RST_STABLE_CHKBB	5	Select reset mode when changing register values.	0x0: Legacy 0x1: Prevent resets while control register values are changing
DP_RST_MIPI2_CHKBB	4	Select reset mode to MIPI controllers. This bit should be set to 1, if required, to have completely independent resets, and linkup of Link A and B.	0x0: Legacy 0x1: Independent reset functionality. Enable auto reset of MIPI controllers.
DP_RST_MIPI_CHKBB	3	Select reset mode to MIPI controllers.	0x0: Legacy 0x1: Independent reset functionality. This enables RST_MIPITX_LOC[3:0] (0x33F) to reset controllers individually.
DP_RST_VP_CHKBB	2	Select reset mode to VIDEO_RX, VRX blocks. This bit should be set to 1, if required, to have completely independent resets, and linkup of Link A and B.	0x0: Legacy 0x1: Independent reset functionality

**PM\_OV\_STAT2 (0x578)\***

BIT	7	6	5	4	3	2	1	0
Field	VTERM_OV_OEN	VREG_OV_OEN	VTERM_OV_LEVEL[1:0]		RSVD[1:0]		VREG_OV_LEVEL[1:0]	
Reset	0b0	0b0	0x1		0x1		0x1	
Access Type	Write, Read	Write, Read	Write, Read				Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VTERM_OV_OEN	7	Enable VTERM overvoltage status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled
VREG_OV_OEN	6	Enable VREG (LDO regulated V <sub>DD</sub> ) overvoltage status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled
VTERM_OV_LEVEL	5:4	VTERM overvoltage comparator trip level	0x0: 1.32V 0x1: 1.35V 0x2: 1.38V 0x3: 1.41V
VREG_OV_LEVEL	1:0	VREG (LDO regulated V <sub>DD</sub> ) overvoltage comparator trip level	0x0: 1.32 V 0x1: 1.35 V 0x2: 1.38 V 0x3: 1.41 V

**PM\_OV\_STAT3 (0x579)**

BIT	7	6	5	4	3	2	1	0
Field	VTERM_OV_FLAG	VREG_OV_FLAG	RSVD	–	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	–	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All		–				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
VTERM_OV_FLAG	7	Sticky status value for V <sub>TERM</sub> overvoltage	0b0: Overvoltage condition not detected 0b1: Overvoltage condition detected
VREG_OV_FLAG	6	Sticky status value for V <sub>REG</sub> (LDO regulated V <sub>DD</sub> ) overvoltage	0b0: Overvoltage condition not detected 0b1: Overvoltage condition detected

**UART\_0 (0x808)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	REM_MS_EN_1	LOC_MS_EN_1	–	BYPASS_TO_1[1:0]		BYPASS_EN_1
Reset	–	–	0b0	0b0	–	0b01		0b0
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN_1	5	Enable UART bypass mode control by remote GPIO pin.  When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_1	4	Enable UART bypass mode control by local GPIO pin.  Set to use GPIO2 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_TO_1	2:1	UART soft-bypass timeout duration.  When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled
BYPASS_EN_1	0	Enable UART soft-bypass mode.  Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

**UART\_1 (0x809)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	REM_MS_EN_2	LOC_MS_EN_2	–	BYPASS_TO_2[1:0]		BYPASS_EN_2
Reset	–	–	0b0	0b0	–	0b01		0b0
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		Write, Read



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN_2	5	Enable UART bypass mode control by remote GPIO pin.  When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_2	4	Enable UART bypass mode control by local GPIO pin.  Set to use GPIO2 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_TO_2	2:1	UART soft-bypass timeout duration.  When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power-down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled
BYPASS_EN_2	0	Enable UART soft-bypass mode.  Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

#### I2C\_PT\_0 (0x80E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	I2C_REGSLV_0_TIMED_OUT	–	–	RSVD	I2C_INTREG_SLV_TO[2:0]		
Reset	0b0	0x0	–	–	0b0	0x6		
Access Type		Read Only	–	–		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSLV_0_TIMED_OUT	6	Internal I2C-to-Register slave for Main Control Channel timed out while waiting for the master or the internal register access FSM.	0x0: Internal I2C-to-Register slave for Main Control Channel 0 has not timed out 0x1: Internal I2C-to-Register slave for Main Control Channel 0 has timed out
I2C_INTREG_SLV_TO	2:0	I2C-to-Internal Register Slave 0 Timeout Setting  Internal register I2C slave 0 times out after the configured duration if it does not receive any response from the external master or internal register FSM. This slave serves the I2C Main Control Channel.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

I2C\_PT\_1 (0x80F)\*

BIT	7	6	5	4	3	2	1	0
Field	I2C_REGSL V_2_TIMED_OUT	I2C_REGSL V_1_TIMED_OUT	I2C_INTREG_SLV_2_TO[2:0]			I2C_INTREG_SLV_1_TO[2:0]		
Reset	0x0	0x0	0x6			0x6		
Access Type	Read Only	Read Only	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSL V_2_TIMED_OUT	7	Internal I <sup>2</sup> C-to-Register slave for Pass-Through Port 2 timed out while waiting for the master or the internal register access FSM.	0x0: Internal I <sup>2</sup> C-to-Register slave for Pass-Through Port 2 has not timed out 0x1: Internal I <sup>2</sup> C-to-Register slave for Pass-Through Port 2 has timed out
I2C_REGSL V_1_TIMED_OUT	6	Internal I <sup>2</sup> C-to-Register slave for Pass-Through Port 1 timed out while waiting for the master or the internal register access FSM.	- 0x0: Internal I <sup>2</sup> C-to-Register slave for Pass-Through Port 1 has not timed out 0x1: Internal I <sup>2</sup> C-to-Register slave for Pass-Through Port 1 has timed out
I2C_INTREG_SLV_2_TO	5:3	I <sup>2</sup> C-to-Internal Register Slave 2 timeout setting  Internal register I <sup>2</sup> C slave 2 times out after the configured duration if it does not receive any response from the external master or internal register FSM. This slave serves the I <sup>2</sup> C Pass-Through Port 2.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled
I2C_INTREG_SLV_1_TO	2:0	I <sup>2</sup> C-to-Internal Register Slave 1 Timeout Setting  Internal register I <sup>2</sup> C slave 1 times out after the configured duration if it does not receive any response from the external master or internal register FSM. This slave serves the I <sup>2</sup> C Pass-Through Port 1.	0b000: 1ms 0b001: 2ms 0b010: 4ms 0b011: 8ms 0b100: 16ms 0b101: 32ms 0b110: 35ms 0b111: Disabled

GMSL1\_EN (0xF00)\*

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	LINK_EN_B	LINK_EN_A
Reset	-	-	-	-	-	-	0b1	0b1
Access Type	-	-	-	-	-	-	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_EN_B	1	Enable link B	0x0: Disable Link B 0x1: Enable Link B
LINK_EN_A	0	Enable link A	0x0: Disable Link A 0x1: Enable Link A

SPI\_CC\_WR (0x1300)

SPI data to write over the GMSL link. Use this address space to send write data across the GMSL link.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

### [SPI\\_CC\\_RD\\_ \(0x1380\)](#)

SPI data read over the GMSL link. Use this address space to read data sent across the GMSL link.

### [RLMS3 \(0x1403, 0x1503\)](#)

BIT	7	6	5	4	3	2	1	0
Field	AdaptEn	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD[1:0]	
Reset	0b0	0b0	0b0	0b0	0b1	0x0	0b10	
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
AdaptEn	7	Adapt process enable

### [RLMS4 \(0x1404, 0x1504\)](#)

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x4				0b10		0b1	0b1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	A factor (N) used to select the order of number of observations in each eye-monitor window.  N is used in the equation: Observations = $6.29 \times 10^{(N + 2)}$	0xX: N factor
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits allowed in a measurement window	0b00: Allow no errors 0b01: Allow one error 0b10: Allow two errors 0b11: Allow three errors
EOM_PER_MODE	1	Eye-Opening Monitor Periodic Mode Enable	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Eye-Opening Monitor Enable	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

### [RLMS5 \(0x1405, 0x1505\)](#)

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0b0	0b0010000						
Access Type	Write Only	Write, Read						

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye-Opening Monitor Manual Trigger For use when periodic mode is disabled.	0b0: No action 0b1: EOM manual trigger request
EOM_MIN_THR	6:0	The eye-opening monitor minimum threshold as defined by the equation: $\% \text{ eye opening} = \text{EOM\_MIN\_THR}/64$ . If the value is zero, the EOM is disabled.	0bXXXXXXX: Eye-opening monitor minimum threshold factor

**RLMS6 (0x1406, 0x1506)**

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	EOM_RST_THR[6:0]						
Reset	0b1	0b0000000						
Access Type	Write, Read	Write, Read						
BITFIELD	BITS	DESCRIPTION		DECODE				
EOM_PV_MODE	7	Eye-opening is measured vertically or horizontally.		0b0: Vertical opening mode 0b1: Horizontal opening mode				
EOM_RST_THR	6:0	The eye-opening monitor refresh threshold as defined by the equation: $\% \text{ eye opening} = \text{EOM\_MIN\_THR}/64$ . If the value is zero, the EOM is disabled.		0bXXXXXXX: EOM refresh threshold factor				

**RLMS7 (0x1407, 0x1507)**

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						
BITFIELD	BITS	DESCRIPTION		DECODE				
EOM_DONE	7	Eye-Opening Monitor Measurement Done		0b0: EOM not complete 0b1: EOM complete				
EOM	6:0	Last completed EOM observation		0bXXXXXXX: EOM measurement result				

**RLMSA (0x140A, 0x150A)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[1:0]		DFEAdpDly[3:0]			
Reset	0x0	0x0	0b00		0x8			
Access Type					Write, Read			

BITFIELD	BITS	DESCRIPTION
DFEAdpDly	3:0	DFE adapt enable delay (milliseconds) (default is 4 for slow receiver)

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[RLMS18 \(0x1418, 0x1518\)](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD[2:0]			RSVD	VgaHiGain	RSVD[1:0]	
Reset	0x0	0x0			0b1	0b1	0b11	
Access Type						Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VgaHiGain	2	55nm FR VGA has an addition gain stage instead of the FFE stage. This control bit (VgaHiGain) configures this gain stage to track the other stages or operate in a high-gain mode.	0: High Gain Stage Tracks VGA 1: VGA High Gain Stage Mode

[RLMS21 \(0x1421, 0x1521\)](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	BSTMuH[5:0]					
Reset	0x0	–	0x04					
Access Type		–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BSTMuH	5:0	BST adapt gain MSB

[RLMS23 \(0x1423, 0x1523\)](#)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	BSTInit[5:0]					
Reset	–	0b1	0b000101					
Access Type	–		Write, Read					

BITFIELD	BITS	DESCRIPTION
BSTInit	5:0	BST initial value (Default is 0 for slow receiver)

[RLMS31 \(0x1431, 0x1531\)](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	OSNMuH[5:0]					
Reset	0b0	–	0b011000					
Access Type		–	Write, Read					

BITFIELD	BITS	DESCRIPTION
OSNMuH	5:0	OSN adapt gain MSB

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[RLMS45 \(0x1445, 0x1545\)](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	CRUSSCSe ISREn	RSVD[1:0]		RSVD	RSVD[2:0]		
Reset	0b1	0b1	0b00		0b1	0b000		
Access Type		Write, Read						
BITFIELD		BITS		DESCRIPTION				
CRUSSCSeISREn		6		Override enable for CRU SSC SEL for Slow Receiver only				

[RLMS46 \(0x1446, 0x1546\)](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				RSVD	CRULpCtrl[2:0]		
Reset	0xB				0b0	0b011		
Access Type						Write, Read		
BITFIELD	BITS		DESCRIPTION			DECODE		
CRULpCtrl	2:0		CRU loop control for Fast Receiver and Slow Receiver For Slow Receiver Rate, if override is disabled, following values are used: Rate 11=101 Rate 10=011 Rate 01=001 Rate 00=000			0b000: 1 CRU edge (highest bandwidth) 0b001: 2 CRU edges 0b010: 1 CRU edge 0b011: 4 CRU edges (default setting) 0b100: 4 CRU edges 0b101: 8 CRU edges 0b110: 4 CRU edges 0b111: 16 CRU edges (lowest bandwidth)		

[RLMS47 \(0x1447, 0x1547\)](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	CRUSSCSe[1:0]		RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b01		0b1
Access Type						Write, Read		
BITFIELD		BITS		DESCRIPTION				
CRUSSCSe		2:1		CRU spread spectrum adjust select For Slow Receiver while override is disabled Rate 11=10 Rate 10=10 Rate 01=01 Rate 00=01				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[RLMS64 \(0x1464, 0x1564\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				RSVD	RSVD	TxSSCMode[1:0]	
Reset	0x9				0x0	0b0	0b00	
Access Type							Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx Spread Spectrum Mode	00: Spread spectrum disabled 01: Reserved 10: Reserved 11: Spread spectrum enabled (center spread)

[RLMS70 \(0x1470, 0x1570\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TxSSCFrqCtrl[6:0]						
Reset	0b0	0b0000001						
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx SSC modulation amplitude (frequency deviation) control	0x07: SSC 268 PPM 0x06: SSC 580 PPM 0x03: SSC 970 PPM 0x01: SSC 1750 PPM 0x01: SSC 2530 PPM Others: Reserved

[RLMS71 \(0x1471, 0x1571\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	0x0	0b000001						0b0
Access Type		Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx SSC center spread starting phase	0x02: Set this value if SSC Generation is enabled (RLMS64) 0x00: Otherwise
TxSSCEn	0	Tx spread spectrum enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

[RLMS72 \(0x1472, 0x1572\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreScIL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreScIL	7:0	Tx SSC frequency prescaler bits 7:0. Decode values are for bits 7:0, concatenate with TXSSCPreScIH for final value.	0xC9: SSC 268 PPM 0xAB: SSC 580 PPM 0xAB: SSC 970 PPM 0xF9: SSC 1750 PPM 0xAB: SSC 2530 PPM Others: Reserved

**RLMS73 (0x1473, 0x1573)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD[4:0]					TxSSCPreScIH[2:0]		
Reset	0x00					0b000		
Access Type						Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreScIH	2:0	Tx SSC frequency prescaler bits 10:8. Decode values are for bits 10:8, concatenate with TXSSCPreScIL for final value.	0x02: SSC 268 PPM 0x00: SSC 580 PPM 0x00: SSC 970 PPM 0x00: SSC 1750 PPM 0x00: SSC 2530 PPM Others: Reserved

**RLMS74 (0x1474, 0x1574)\***

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx SSC phase accumulator increment bits 7:0. Decode values are for bits 7:0, concatenate with TXSSCPhH for final value.	0xF9: SSC 268 PPM 0x63: SSC 580 PPM 0x63: SSC 970 PPM 0x2C: SSC 1750 PPM 0x63: SSC 2530 PPM Others: Reserved

**RLMS75 (0x1475, 0x1575)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TxSSCPhH[6:0]						
Reset	0b0	0b00000000						
Access Type		Write, Read						



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx SSC phase accumulator increment bits 14:8. Decode values are for bits 14:8, concatenate with TXSSCPhL for final value.	0x01: If SSC Generation enabled (RLMS64) and desired spread is 268 PPM 0x07: If SSC Generation enabled (RLMS64) and desired spread is 580 PPM 0x07: If SSC Generation enabled (RLMS64) and desired spread is 970 PPM 0x05: If SSC Generation enabled (RLMS64) and desired spread is 1750 PPM 0x07: If SSC Generation enabled (RLMS64) and desired spread is 2530 PPM Others: Reserved

#### RLMS8C (0x148C, 0x158C)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	cap_pre_out_rlms[6:0]						
Reset	0b0	0b0000000						
Access Type		Write, Read						
BITFIELD	BITS	DESCRIPTION						
cap_pre_out_rlms	6:0	cap_preout value during RLMS if overridden						

#### RLMS95 (0x1495, 0x1595)

BIT	7	6	5	4	3	2	1	0
Field	TxAmpIManEn	RSVD	TxAmplMan[5:0]					
Reset	0b0	0b1	0b101001					
Access Type	Write, Read		Write, Read					
BITFIELD	BITS	DESCRIPTION				DECODE		
TxAmpIManEn	7	TX amplitude manual override				0: Do not manually override Tx amplitude 1: Manually override Tx amplitude		
TxAmpIMan	5:0	Tx amplitude				0bXXXXXX: Binary amplitude 10mV per count		

#### RLMS98 (0x1498, 0x1598)

BIT	7	6	5	4	3	2	1	0
Field	Cal_cap_pre_out_en	RSVD	RSVD[2:0]			RSVD[2:0]		
Reset	0b0	0b1	0b000			0b000		
Access Type	Write, Read							
BITFIELD		BITS		DESCRIPTION				
Cal_cap_pre_out_en		7		Enable manual override for cap_pre_out during RLMS				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**RLMSA4 (0x14A4, 0x15A4)**

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0b10		0b111101					
Access Type	Write, Read		Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE			
AEQ_PER_MULT	7:6	Adaptive EQ period multiplier			00: 1ms 01: 4ms 10: 16ms 11: 64ms			
AEQ_PER	5:0	Adaptive EQ period Periodic adaptation is disabled when value is 0. Adaptive EQ period is (AEQ_PER value times AEQ_PER_MULT).						

**RLMSA5 (0x14A5, 0x15A5)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		PHYC_WBLOCK_DLY[1:0]		RSVD[1:0]		RSVD[1:0]	
Reset	0b01		0b01		0b00		0b00	
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PHYC_WBLOCK_DLY	5:4	PHY controller word boundary lock start delay	00: 1ms 01: 2ms 10: 4ms 11: 8ms

**RLMSA7 (0x14A7, 0x15A7)**

BIT	7	6	5	4	3	2	1	0
Field	MAN_CTRL_EN	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAN_CTRL_EN	7	PHY controller manual mode enable			0b0: PHY controller manual mode disabled 0b1: PHY controller manual mode enabled			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[RLMSA8 \(0x14A8, 0x15A8\)](#)

BIT	7	6	5	4	3	2	1	0
Field	FW_PHY_CTRL	FW_PHY_PU_TX	FW_PHY_RSTB	RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
FW_PHY_CTRL	7	PHY controller firmware mode enable
FW_PHY_PU_TX	6	Override PHY controller output
FW_PHY_RSTB	5	Override PHY controller output

[RLMSA9 \(0x14A9, 0x15A9\)](#)

BIT	7	6	5	4	3	2	1	0
Field	FW_REPCAL_RSTB	RSVD	FW_TXD_SQUELCH	FW_TXD_EN	FW_RXD_EN	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
FW_REPCAL_RSTB	7	Override PHY controller output
FW_TXD_SQUELCH	5	Override PHY controller output
FW_TXD_EN	4	Override PHY controller output
FW_RXD_EN	3	Override PHY controller output

[RLMSAC \(0x14AC, 0x15AC\)](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	ErrChPhSecFR3G[6:0]						
Reset	0b1	0x20						
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION
ErrChPhSecFR3G	6:0	Error channel phase secondary (odd)

[RLMSAD \(0x14AD, 0x15AD\)](#)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	ErrChPhPriFR3G[6:0]						
Reset	0b0	0x60						
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION
ErrChPhPriFR3G	6:0	Error channel phase primary (even)

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**DPLL\_0 (0x1C00)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0b1	0b1	0b1	0b1	0b0	0b1	0b0	0b1
Access Type								Write, Read
BITFIELD		BITS		DESCRIPTION				
config_soft_rst_n		0		Setting this to 1 resets the PLL functional registers, config_regs are not reset.				

**DPLL\_3 (0x1C03)\***

BIT	7	6	5	4	3	2	1	0
Field	config_sel_clock_out_use_external	config_disable_div_out_exp	config_use_internal_pll_mode_values	config_use_internal_divider_values	RSVD	RSVD[2:0]		
Reset	0b1	0b0	0b0	0b0	0b0	0b010		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION
config_sel_clock_out_use_external	7	When 1, i_sel_clock_out is used to select output clock. Otherwise, internal registers are used.
config_disable_div_out_exp	6	Forces div_out_exp to 7, which disables the divider
config_use_internal_pll_mode_values	5	Bypasses internal pll_mode controls and uses config_reg values
config_use_internal_divider_values	4	Forces all divider values to come from internal controls

**DPLL\_7 (0x1C07)**

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_L	config_div_in[4:0]					RSVD[1:0]	
Reset	0b0	0b00001					0b00	
Access Type	Write, Read	Write, Read						

BITLEN	BITFIELD	BITS	DESCRIPTION
1	config_div_fb_L	7	Sets the feedback divider value when i_div_use_external = 0
5	config_div_in	6:2	Sets the divide value of the input divider connected to i_clk_in, the main PLL clock input

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**DPLL\_8 (0x1C08)**

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_H[7:0]							
Reset	0x14							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
config_div_fb_H	7:0	Sets the feedback divider value when i_div_use_external = 0

**DPLL\_10 (0x1C0A)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD	config_div_out_exp[2:0]			RSVD[3:0]			
Reset	0b1	0b000			0x1			
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION
config_div_out_exp	6:4	Sets the output exponential divider value when i_div_use_external = 0

**DPLL\_0 (0x1D00)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0b1	0b1	0b1	0b1	0b0	0b1	0b0	0b1
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
config_soft_rst_n	0	Setting this to 1 resets the PLL functional registers, config_regs are not reset.

**DPLL\_3 (0x1D03)\***

BIT	7	6	5	4	3	2	1	0
Field	config_sel_clock_out_use_external	config_disable_div_out_exp	config_use_internal_pll_mode_values	config_use_internal_divider_values	RSVD	RSVD[2:0]		
Reset	0b1	0b0	0b0	0b0	0b0	0b010		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION
config_sel_clock_out_use_external	7	When 1, i_sel_clock_out is used to select output clock. Otherwise, internal registers are used.
config_disable_div_out_exp	6	Forces div_out_exp to 7, which disables the divider

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
config_use_internal_pll_mode_values	5	Bypasses internal pll_mode controls and uses config_reg values
config_use_internal_divider_values	4	Forces all divider values to come from internal controls

#### DPLL\_7 (0x1D07)

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_L	config_div_in[4:0]					RSVD[1:0]	
Reset	0b0	0b00001					0b00	
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
config_div_fb_L	7	Sets the feedback divider value when i_div_use_external = 0
config_div_in	6:2	Sets the divide value of the input divider connected to i_clk_in, the main PLL clock input

#### DPLL\_8 (0x1D08)

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_H[7:0]							
Reset	0x14							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
config_div_fb_H	7:0	Sets the feedback divider value when i_div_use_external = 0

#### DPLL\_10 (0x1D0A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	config_div_out_exp[2:0]			RSVD[3:0]			
Reset	0b1	0b000			0x1			
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION
config_div_out_exp	6:4	Sets the output exponential divider value when i_div_use_external = 0

#### DPLL\_0 (0x1E00)\*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0b1	0b1	0b1	0b1	0b0	0b1	0b0	0b1
Access Type								Write, Read

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
config_soft_rst_n	0	Setting this to 1 resets the PLL functional registers, config_regs are not reset.

#### DPLL\_3 (0x1E03)\*

BIT	7	6	5	4	3	2	1	0
Field	config_sel_clock_out_use_external	config_disable_div_out_exp	config_use_internal_pll_mode_values	config_use_internal_divider_values	RSVD	RSVD[2:0]		
Reset	0b1	0b0	0b0	0b0	0b0	0b010		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION
config_sel_clock_out_use_external	7	When 1, i_sel_clock_out is used to select output clock. Otherwise, internal registers are used.
config_disable_div_out_exp	6	Forces div_out_exp to 7, which disables the divider
config_use_internal_pll_mode_values	5	Bypasses internal pll_mode controls and uses config_reg values
config_use_internal_divider_values	4	Forces all divider values to come from internal controls

#### DPLL\_7 (0x1E07)

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_L	config_div_in[4:0]					RSVD[1:0]	
Reset	0b0	0b00001					0b00	
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
config_div_fb_L	7	Sets the feedback divider value when i_div_use_external = 0
config_div_in	6:2	Sets the divide value of the input divider connected to i_clk_in, the main PLL clock input

#### DPLL\_8 (0x1E08)

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_H[7:0]							
Reset	0x14							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
config_div_fb_H	7:0	Sets the feedback divider value when i_div_use_external = 0

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**DPLL\_10 (0x1E0A)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD	config_div_out_exp[2:0]			RSVD[3:0]			
Reset	0b1	0b000			0x1			
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION
config_div_out_exp	6:4	Sets the output exponential divider value when i_div_use_external = 0

**DPLL\_0 (0x1F00)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0b1	0b1	0b1	0b1	0b0	0b1	0b0	0b1
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
config_soft_rst_n	0	Setting this to 1 resets the PLL functional registers, config_regs are not reset.

**DPLL\_3 (0x1F03)\***

BIT	7	6	5	4	3	2	1	0
Field	config_sel_clock_out_use_external	config_disable_div_out_exp	config_use_internal_pll_mode_values	config_use_internal_divider_values	RSVD	RSVD[2:0]		
Reset	0b1	0b0	0b0	0b0	0b0	0b010		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION
config_sel_clock_out_use_external	7	When 1, i_sel_clock_out is used to select output clock. Otherwise, internal registers are used.
config_disable_div_out_exp	6	Forces div_out_exp to 7, which disables the divider
config_use_internal_pll_mode_values	5	Bypasses internal pll_mode controls and uses config_reg values
config_use_internal_divider_values	4	Forces all divider values to come from internal controls



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**DPLL\_7 (0x1F07)**

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_L	config_div_in[4:0]					RSVD[1:0]	
Reset	0b0	0b00001					0b00	
Access Type	Write, Read	Write, Read						
BITFIELD		BITS		DESCRIPTION				
config_div_fb_L		7		Sets the feedback divider value when i_div_use_external = 0				
config_div_in		6:2		Sets the divide value of the input divider connected to i_clk_in, the main PLL clock input				

**DPLL\_8 (0x1F08)**

BIT	7	6	5	4	3	2	1	0
Field	config_div_fb_H[7:0]							
Reset	0x14							
Access Type	Write, Read							
BITFIELD		BITS		DESCRIPTION				
config_div_fb_H		7:0		Sets the feedback divider value when i_div_use_external = 0				

**DPLL\_10 (0x1F0A)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD	config_div_out_exp[2:0]			RSVD[3:0]			
Reset	0b1	0b000			0x1			
Access Type		Write, Read						
BITFIELD		BITS		DESCRIPTION				
config_div_out_exp		6:4		Sets the output exponential divider value when i_div_use_external = 0				

**CLEAR\_STATS (0x2000)**

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	CLEAR_BITS_CORRECTED	CLEAR_BLOCKS_UNCORRECTABLE	CLEAR_BLOCKS_PROCESSED	CLEAR_ALL_STATS
Reset	—	—	—	—	0b0	0b0	0b0	0b0
Access Type	—	—	—	—	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read
BITFIELD		BITS		DESCRIPTION				
CLEAR_BITS_CORRECTED		3		Clear counter for number of bits corrected by FEC				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
CLEAR_BLOCKS_UNCORRECTABLE	2	Clear counter for number of uncorrectable FEC blocks
CLEAR_BLOCKS_PROCESSED	1	Clear counter for number of FEC blocks processed
CLEAR_ALL_STATS	0	Clear all FEC stats and counters

#### STATS\_CONTROL (0x2001)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	STATS_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
STATS_ENABLE	0	Enable FEC stats collection for Link A

#### CORRECTED\_THRESHOLD\_0 (0x2008)

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_THRESHOLD_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BIT_ERRS_CORRECTED_THRESHOLD_0	7:0	Threshold (decimal value) for number of bit errors seen before FEC error is asserted. Bits 7:0. Set this to the maximum value so that the FEC error flag is not asserted and any correctable errors that occurred are successfully corrected.

#### CORRECTED\_THRESHOLD\_1 (0x2009)

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_THRESHOLD_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BIT_ERRS_CORRECTED_THRESHOLD_1	7:0	Threshold (decimal value) for number of bit errors seen before FEC error is asserted. Bits 15:8. Set this to the maximum value so that the FEC error flag is not asserted and any correctable errors that occurred are successfully corrected.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**CORRECTED\_THRESHOLD\_2 (0x200A)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_THRESHOLD_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BIT_ERRS_CORRECTED_THRESHOLD_2	7:0	Threshold (decimal value) for number of bit errors seen before FEC error is asserted. Bits 23:16. Set this to the maximum value so that the FEC error flag is not asserted and any correctable errors that occurred are successfully corrected.

**CORRECTED\_THRESHOLD\_3 (0x200B)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_THRESHOLD_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BIT_ERRS_CORRECTED_THRESHOLD_3	7:0	Threshold (decimal value) for number of bit errors seen before FEC error is asserted. Bits 31:24. Set this to the maximum value so that the FEC error flag is not asserted and any correctable errors that occurred are successfully corrected.

**ERROR\_THRESHOLD\_0 (0x200C)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTED_ERROR_THRESHOLD_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UNCORRECTED_ERROR_THRESHOLD_0	7:0	Threshold (decimal value) for number of uncorrected blocks seen before FEC error is asserted. Bits 7:0.

**ERROR\_THRESHOLD\_1 (0x200D)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTED_ERROR_THRESHOLD_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UNCORRECTED_ERROR_THRESHOLD_1	7:0	Threshold (decimal value) for number of uncorrected blocks seen before FEC error is asserted. Bits 15:8.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**ERROR\_THRESHOLD\_2 (0x200E)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTED_ERROR_THRESHOLD_2[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD		BITS		DESCRIPTION				
UNCORRECTED_ERROR_THRESHOLD_2		7:0		Threshold (decimal value) for number of uncorrected blocks seen before FEC error is asserted. Bits 23:16.				

**ERROR\_THRESHOLD\_3 (0x200F)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTED_ERROR_THRESHOLD_3[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD		BITS		DESCRIPTION				
UNCORRECTED_ERROR_THRESHOLD_3		7:0		Threshold (decimal value) for number of uncorrected blocks seen before FEC error is asserted. Bits 31:24.				

**BLOCKS\_UNCORRECTABLE\_0 (0x2020)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTABLE_BLOCKS_0[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
UNCORRECTABLE_BLOCKS_0		7:0		Number of uncorrectable blocks. Bits 7:0.				

**BLOCKS\_UNCORRECTABLE\_1 (0x2021)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTABLE_BLOCKS_1[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
UNCORRECTABLE_BLOCKS_1		7:0		Number of uncorrectable blocks. Bits 15:8.				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BLOCKS\_UNCORRECTABLE\_2 (0x2022)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTABLE_BLOCKS_2[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
UNCORRECTABLE_BLOCKS_2		7:0		Number of uncorrectable blocks. Bits 23:16.				

**BLOCKS\_UNCORRECTABLE\_3 (0x2023)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTABLE_BLOCKS_3[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
UNCORRECTABLE_BLOCKS_3		7:0		Number of uncorrectable blocks. Bits 31:24.				

**BITS\_CORRECTED\_0 (0x2024)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_0[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_0		7:0		Number of bit errors corrected. Bits 7:0.				

**BITS\_CORRECTED\_1 (0x2025)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_1[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_1		7:0		Number of bit errors corrected. Bits 15:8.				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BITS\_CORRECTED\_2 (0x2026)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_2[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_2		7:0		Number of bit errors corrected. Bits 23:16.				

**BITS\_CORRECTED\_3 (0x2027)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_3[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_3		7:0		Number of bit errors corrected. Bits 31:24.				

**BLOCKS\_PROCESSED\_0 (0x2028)**

BIT	7	6	5	4	3	2	1	0
Field	BLOCKS_PROCESSED_0[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BLOCKS_PROCESSED_0		7:0		Number of 120-bit blocks processed. Bits 7:0.				

**BLOCKS\_PROCESSED\_1 (0x2029)**

BIT	7	6	5	4	3	2	1	0
Field	BLOCKS_PROCESSED_1[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BLOCKS_PROCESSED_1		7:0		Number of 120-bit blocks processed. Bits 15:8.				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BLOCKS\_PROCESSED\_2 (0x202A)**

BIT	7	6	5	4	3	2	1	0
Field	BLOCKS_PROCESSED_2[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS		DESCRIPTION					
BLOCKS_PROCESSED_2	7:0		Number of 120-bit blocks processed. Bits 23:16.					

**BLOCKS\_PROCESSED\_3 (0x202B)**

BIT	7	6	5	4	3	2	1	0
Field	BLOCKS_PROCESSED_3[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS		DESCRIPTION					
BLOCKS_PROCESSED_3	7:0		Number of 120-bit blocks processed. Bits 31:24.					

**CLEAR\_STATS (0x2100)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CLEAR_BITS_CORRECTED_B	CLEAR_BLOCKS_UNCORRECTABLE_B	CLEAR_BLOCKS_PROCESSED_B	CLEAR_ALL_STATS_B
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read
BITFIELD	BITS		DESCRIPTION					
CLEAR_BITS_CORRECTED_B	3		Clear counter for number of bits corrected by FEC					
CLEAR_BLOCKS_UNCORRECTABLE_B	2		Clear counter for number of uncorrectable FEC blocks					
CLEAR_BLOCKS_PROCESSED_B	1		Clear counter for number of FEC blocks processed					
CLEAR_ALL_STATS_B	0		Clear all FEC stats and counters					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

### STATS\_CONTROL (0x2101)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	STATS_ENABLE_B
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
BITFIELD		BITS		DESCRIPTION				
STATS_ENABLE_B		0		Enable FEC stats collection for Link B				

### CORRECTED\_THRESHOLD\_0 (0x2108)

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_THRESHOLD_0_B[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_THRESHOLD_0_B		7:0		Threshold (decimal value) for number of bit errors seen before FEC error is asserted. Bits 7:0. Set this to the maximum value so that the FEC error flag is not asserted and any correctable errors that occurred are successfully corrected.				

### CORRECTED\_THRESHOLD\_1 (0x2109)

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_THRESHOLD_1_B[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_THRESHOLD_1_B		7:0		Threshold (decimal value) for number of bit errors seen before FEC error is asserted. Bits 15:8. Set this to the maximum value so that the FEC error flag is not asserted and any correctable errors that occurred are successfully corrected..				

### CORRECTED\_THRESHOLD\_2 (0x210A)

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_THRESHOLD_2_B[7:0]							
Reset	0x00							
Access Type	Write, Read							



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
BIT_ERRS_CORRECTED_THRESHOLD_2_B	7:0	Threshold (decimal value) for number of bit errors seen before FEC error is asserted. Bits 23:16. Set this to the maximum value so that the FEC error flag is not asserted and any correctable errors that occurred are successfully corrected.

#### CORRECTED\_THRESHOLD\_3 (0x210B)

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_THRESHOLD_3_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BIT_ERRS_CORRECTED_THRESHOLD_3_B	7:0	Threshold (decimal value) for number of bit errors seen before FEC error is asserted. Bits 31:24. Set this to the maximum value so that the FEC error flag is not asserted and any correctable errors that occurred are successfully corrected.

#### ERROR\_THRESHOLD\_0 (0x210C)

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTED_ERROR_THRESHOLD_0_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UNCORRECTED_ERROR_THRESHOLD_0_B	7:0	Threshold (decimal value) for number of uncorrected blocks seen before FEC error is asserted. Bits 7:0.

#### ERROR\_THRESHOLD\_1 (0x210D)

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTED_ERROR_THRESHOLD_1_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UNCORRECTED_ERROR_THRESHOLD_1_B	7:0	Threshold (decimal value) for number of uncorrected blocks seen before FEC error is asserted. Bits 15:8.

#### ERROR\_THRESHOLD\_2 (0x210E)

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTED_ERROR_THRESHOLD_2_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
UNCORRECTED_ERR OR_THRESHOLD_2_B	7:0	Threshold (decimal value) for number of uncorrected blocks seen before FEC error is asserted. Bits 23:16.

#### ERROR\_THRESHOLD\_3 (0x210F)

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTED_ERROR_THRESHOLD_3_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
UNCORRECTED_ERR OR_THRESHOLD_3_B	7:0	Threshold (decimal value) for number of uncorrected blocks seen before FEC error is asserted. Bits 31:24.

#### BLOCKS\_UNCORRECTABLE\_0 (0x2120)

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTABLE_BLOCKS_0_B[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNCORRECTABLE_BLK S_0_B	7:0	Number of uncorrectable blocks. Bits 7:0.

#### BLOCKS\_UNCORRECTABLE\_1 (0x2121)

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTABLE_BLOCKS_1_B[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNCORRECTABLE_BLK S_1_B	7:0	Number of uncorrectable blocks. Bits 15:8.

#### BLOCKS\_UNCORRECTABLE\_2 (0x2122)

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTABLE_BLOCKS_2_B[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
UNCORRECTABLE_BLK S_2_B	7:0	Number of uncorrectable blocks. Bits 23:16.

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BLOCKS\_UNCORRECTABLE\_3 (0x2123)**

BIT	7	6	5	4	3	2	1	0
Field	UNCORRECTABLE_BLOCKS_3_B[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
UNCORRECTABLE_BLOCKS_3_B		7:0		Number of uncorrectable blocks. Bits 31:24.				

**BITS\_CORRECTED\_0 (0x2124)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_0_B[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_0_B		7:0		Number of bit errors corrected. Bits 7:0.				

**BITS\_CORRECTED\_1 (0x2125)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_1_B[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_1_B		7:0		Number of bit errors corrected. Bits 15:8.				

**BITS\_CORRECTED\_2 (0x2126)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_2_B[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_2_B		7:0		Number of bit errors corrected. Bits 23:16.				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BITS\_CORRECTED\_3 (0x2127)**

BIT	7	6	5	4	3	2	1	0
Field	BIT_ERRS_CORRECTED_3_B[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BIT_ERRS_CORRECTED_3_B		7:0		Number of bit errors corrected. Bits 31:24.				

**BLOCKS\_PROCESSED\_0 (0x2128)**

BIT	7	6	5	4	3	2	1	0
Field	BLOCKS_PROCESSED_0_B[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BLOCKS_PROCESSED_0_B		7:0		Number of 120-bit blocks processed. Bits 7:0.				

**BLOCKS\_PROCESSED\_1 (0x2129)**

BIT	7	6	5	4	3	2	1	0
Field	BLOCKS_PROCESSED_1_B[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BLOCKS_PROCESSED_1_B		7:0		Number of 120-bit blocks processed. Bits 15:8.				

**BLOCKS\_PROCESSED\_2 (0x212A)**

BIT	7	6	5	4	3	2	1	0
Field	BLOCKS_PROCESSED_2_B[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
BLOCKS_PROCESSED_2_B		7:0		Number of 120-bit blocks processed. Bits 23:16.				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**BLOCKS\_PROCESSED\_3 (0x212B)**

BIT	7	6	5	4	3	2	1	0
Field	BLOCKS_PROCESSED_3_B[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLOCKS_PROCESSED_3_B	7:0	Number of 120-bit blocks processed. Bits 31:24.

**REGCRC0 (0x3000)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	GEN_ROLLING_CRC	I2C_WR_COMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–		Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION
GEN_ROLLING_CRC	4	Calculate CRC using additional 2-bit counter, so CRC value cycles every 4 invocations.
I2C_WR_COMPUTE	3	Execute CRC computation after every I2C register write.
PERIODIC_COMPUTE	2	Perform CRC check on a periodic basis, based on CRC_PERIOD value.
CHECK_CRC	1	Upon calculation of CRC, compare with previous calculation, except on first time through. On miscompare, issue ERRB.
RESET_CRC	0	Reset CRC value to 16'FFFF.

**REGCRC1 (0x3001)\***

BIT	7	6	5	4	3	2	1	0
Field	CRC_PERIOD[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CRC_PERIOD	7:0	Period for CRC recomputation. This allows to vary the CRC computation time. Period = (value + 1) x 2ms  0000_0000 - 2ms 0000_0001 - 4ms ...

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[REGCRC2 \(0x3002\)](#)

BIT	7	6	5	4	3	2	1	0
Field	REGCRC_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
REGCRC_LSB		7:0		CRC result LSB				

[REGCRC3 \(0x3003\)](#)

BIT	7	6	5	4	3	2	1	0
Field	REGCRC_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD		BITS		DESCRIPTION				
REGCRC_MSB		7:0		CRC result MSB				

[I2C\\_UART\\_CRC0 \(0x3008\)](#)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RESET_MS GCNTR
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write Clears All, Read
BITFIELD		BITS		DESCRIPTION				
RESET_MSGCNTR		0		Reset Message Counter Value to 0				

[I2C\\_UART\\_CRC1 \(0x3009\)\\*](#)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_ERR_THR[2:0]			CRC_ERR_THR[2:0]			RESET_MS GCNTR_ER R_CNT	RESET_CR C_ERR_CN T
Reset	0b0			0b0			0b0	0b0
Access Type	Write, Read			Write, Read			Write Clears All, Read	Write Clears All, Read
BITFIELD		BITS		DESCRIPTION				
MSGCNTR_ERR_THR		7:5		I2C/UART Message counter error reporting threshold. <ul style="list-style-type: none"> <li>I2C_UART_MSGCNTR_ERR_INT is asserted when MSGCNTR_ERR_CNT ≥ MSGCNTR_ERR_THR</li> </ul>				

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
CRC_ERR_THR	4:2	I <sup>2</sup> C/UART CRC error reporting threshold <ul style="list-style-type: none"> <li>I<sup>2</sup>C_UART_CRC_ERR_INT is asserted when CRC_ERR_CNT ≥ CRC_ERR_THR</li> </ul>
RESET_MSGCNTR_ERR_CNT	1	Reset Message Counter Error Count to 0
RESET_CRC_ERR_CNT	0	Reset CRC Error Count to 0

#### I<sup>2</sup>C\_UART\_CRC2 (0x300A)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VAL[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS	DESCRIPTION						
CRC_VAL	7:0	Calculated CRC value for the last write transaction						

#### I<sup>2</sup>C\_UART\_CRC3 (0x300B)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS	DESCRIPTION						
MSGCNTR_LSB	7:0	Bits 7:0 of current message counter value						

#### I<sup>2</sup>C\_UART\_CRC4 (0x300C)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							
BITFIELD	BITS	DESCRIPTION						
MSGCNTR_MSB	7:0	Bits 7:0 of current message counter value						

#### I<sup>2</sup>C\_UART\_CRC5 (0x300D)

BIT	7	6	5	4	3	2	1	0
Field	CRC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
CRC_ERR_CNT	7:0	Number of CRC errors observed

#### I2C UART CRC6 (0x300E)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_ERR_CNT	7:0	Number of message counter errors observed

#### I2C UART CRC7 (0x300F)\*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MSGCNTR_PORT_SEL[1:0]		CC_MSGCNTR_EN	CC_CRC_EN	CC_CRC_MSGCNTR_OVR
Reset	–	–	–	0x0		0b1	0b1	0b0
Access Type	–	–	–	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MSGCNTR_PORT_SEL	4:3	Selects the current message/CRC counter  Selects between the ports for values read from MSGCNTR_LSB/MSB, MSGCNTR_ERR_CNT, CRC_VAL, and CRC_ERR_CNT.	0x0: Main I2C/UART interface 0x1: I2C/UART pass-through 1 0x2: I2C/UART pass-through 2 0x3: Reserved
CC_MSGCNTR_EN	2	Enable I2C/UART message counter override when set to 1  Only active when CC_CRC_MSGCNTR_OVR = 1.	0b0: Reporting disabled 0b1: Reporting enabled
CC_CRC_EN	1	Enable I2C/UART CRC override when set to 1  Only active when CC_CRC_MSGCNTR_OVR = 1.	0b0: Reporting disabled 0b1: Reporting enabled
CC_CRC_MSGCNTR_OVR	0	Enable I2C/UART CRC or message counter override when set to 1  When 0, eFuse controls CRC and message counter options.	0b0: Reporting disabled 0b1: Reporting enabled



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**FS\_INTR0 (0x3010)\***

BIT	7	6	5	4	3	2	1	0
Field	I2C_UART_MSGCNTR_ERR_OEN	I2C_UART_CRC_ERR_OEN	MEM_ECC_ERR2_OEN	MEM_ECC_ERR1_OEN	–	–	EFUSE_CRC_ERR_OEN	REG_CRC_ERR_OEN
Reset	0b1	0b1	0b1	0b0	–	–	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_UART_MSGCNTR_ERR_OEN	7	Enable reporting of I <sup>2</sup> C/UART message counter errors (I2C_UART_MSGCNTR_ERR_INT) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
I2C_UART_CRC_ERR_OEN	6	Enable reporting of I <sup>2</sup> C/UART CRC errors (I2C_UART_CRC_ERR_INT) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MEM_ECC_ERR2_OEN	5	Enable reporting of memory ECC 2-bit uncorrectable errors at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MEM_ECC_ERR1_OEN	4	Enable reporting of memory ECC 1-bit correctable errors at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
EFUSE_CRC_ERR_OEN	1	Enable reporting eFuse CRC at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
REG_CRC_ERR_OEN	0	Enable reporting register CRC at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

**FS\_INTR1 (0x3011)**

BIT	7	6	5	4	3	2	1	0
Field	I2C_UART_MSGCNTR_ERR_INT	I2C_UART_CRC_ERR_INT	MEM_ECC_ERR2_INT	MEM_ECC_ERR1_INT	–	–	EFUSE_CRC_ERR_FLAG	REG_CRC_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_UART_MSGCNTR_ERR_INT	7	I <sup>2</sup> C/UART message counter error, asserted when MSGCNTR_ERR_CNT ≥ MSGCNTR_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted
I2C_UART_CRC_ERR_INT	6	I <sup>2</sup> C/UART CRC error, asserted when CRC_ERR_CNT ≥ CRC_ERR_THR	0b0: Flag not asserted 0b1: Flag asserted
MEM_ECC_ERR2_INT	5	Decoding error flag for 2-bit uncorrectable memory ECC errors, asserted when MEM_ECC_ERR2_CNT ≥ MEM_ECC_ERR2_THR.	0b0: Flag not asserted 0b1: Flag asserted
MEM_ECC_ERR1_INT	4	Decoding error flag for 1-bit correctable memory ECC errors, asserted when MEM_ECC_ERR1_CNT ≥ MEM_ECC_ERR1_THR.	0b0: Flag not asserted 0b1: Flag asserted

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
EFUSE_CRC_ERR_FLAG	1	An error occurred on the eFuse CRC calculation	0b0: Flag not asserted 0b1: Flag asserted
REG_CRC_ERR_FLAG	0	An error occurred on the register CRC calculation	0b0: Flag not asserted 0b1: Flag asserted

#### MEM\_ECC0 (0x3016)\*

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR2_THR[2:0]			MEM_ECC_ERR1_THR[2:0]			RESET_MEM_ECC_ERR2_CNT	RESET_MEM_ECC_ERR1_CNT
Reset	0b0			0b0			0b0	0b0
Access Type	Write, Read			Write, Read			Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION
MEM_ECC_ERR2_THR	7:5	Decoding and error reporting threshold. MEM_ECC_ERR2 is asserted when MEM_ECC_ERR2_CNT ≥ MEM_ECC_ERR2_THR.
MEM_ECC_ERR1_THR	4:2	Decoding and error reporting threshold. MEM_ECC_ERR1 is asserted when MEM_ECC_ERR1_CNT ≥ MEM_ECC_ERR1_THR.
RESET_MEM_ECC_ERR2_CNT	1	Reset memory ECC 2-bit error count to 0
RESET_MEM_ECC_ERR1_CNT	0	Reset memory ECC 1-bit error count to 0

#### MEM\_ECC1 (0x3017)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR1_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MEM_ECC_ERR1_CNT	7:0	Number of 1-bit correctable memory ECC errors observed

#### MEM\_ECC2 (0x3018)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ECC_ERR2_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MEM_ECC_ERR2_CNT	7:0	Number of 2-bit uncorrectable memory ECC errors observed

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**REG\_POST0 (0x3020)\***

BIT	7	6	5	4	3	2	1	0
Field	POST_DON E	POST_MBI ST_PASSE D	POST_LBIS T_PASSED	–	–	RSVD	POST_RUN _MBIST	POST_RUN _LBIST
Reset	0b0	0b0	0b0	–	–	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	–	–		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
POST_DON E	7	POST (Power-on Self-Test LBIST and/or MBIST) is run	0b0: POST is not run 0b1: POST is run
POST_MBIS T_PASSED	6	MBIST passed during POST (Power-on Self Test). Valid when POST_DONE is asserted.	0b0: MBIST failed during POST run (or is not enabled) 0b1: MBIST passed during POST run
POST_LBIST _PASSED	5	LBIST passed during POST (Power-on Self Test). Valid when POST_DONE is asserted.	0b0: LBIST failed during POST run (or is not enabled) 0b1: LBIST passed during POST run
POST_RUN_ MBIST	1	Indicates if this device is enabled to run MBIST during POST. Read-only.	0b0: MBIST disabled 0b1: MBIST enabled
POST_RUN_ LBIST	0	Indicates if this device is enabled to run LBIST during POST. Read-only.	0b0: LBIST disabled 0b1: LBIST enabled

**REGCRC8 (0x3030)**

BIT	7	6	5	4	3	2	1	0
Field	SKIP0_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP0_LSB	7:0	Address 0 to skip (LSB). This can be used to exclude whole registers from the CRC calculation.	0xXX: LSB of address

**REGCRC9 (0x3031)**

BIT	7	6	5	4	3	2	1	0
Field	SKIP0_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKIP0_MSB	7:0	Address 0 to skip (MSB). This can be used to exclude whole registers from the CRC calculation.	0xXX: MSB of address

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[REGCRC10 \(0x3032\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP1_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP1_LSB	7:0	Address 1 to skip (LSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: LSB of address			

[REGCRC11 \(0x3033\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP1_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP1_MSB	7:0	Address 1 to skip (MSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: MSB of address			

[REGCRC12 \(0x3034\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP2_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP2_LSB	7:0	Address 2 to skip (LSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: LSB of address			

[REGCRC13 \(0x3035\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP2_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP2_MSB	7:0	Address 2 to skip (MSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: MSB of address			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[REGCRC14 \(0x3036\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP3_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP3_LSB	7:0	Address 3 to skip (LSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: LSB of address			

[REGCRC15 \(0x3037\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP3_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP3_MSB	7:0	Address 3 to skip (MSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: MSB of address			

[REGCRC16 \(0x3038\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP4_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP4_LSB	7:0	Address 4 to skip (LSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: LSB of address			

[REGCRC17 \(0x3039\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP4_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP4_MSB	7:0	Address 4 to skip (MSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: MSB of address			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

[REGCRC18 \(0x303A\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP5_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP5_LSB	7:0	Address 5 to skip (LSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: LSB of address			

[REGCRC19 \(0x303B\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP5_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP5_MSB	7:0	Address 5 to skip (MSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: MSB of address			

[REGCRC20 \(0x303C\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP6_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP6_LSB	7:0	Address 6 to skip (LSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: LSB of address			

[REGCRC21 \(0x303D\)](#)

BIT	7	6	5	4	3	2	1	0
Field	SKIP6_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP6_MSB	7:0	Address 6 to skip (MSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: MSB of address			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**REGCRC22 (0x303E)**

BIT	7	6	5	4	3	2	1	0
Field	SKIP7_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP7_LSB	7:0	Address 7 to skip (LSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: LSB of address			

**REGCRC23 (0x303F)**

BIT	7	6	5	4	3	2	1	0
Field	SKIP7_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SKIP7_MSB	7:0	Address 7 to skip (MSB). This can be used to exclude whole registers from the CRC calculation.			0xXX: MSB of address			

**CC\_RTTN\_ERR (0x304F)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	RESET_EF USE_CRC_ ERR	INJECT_EF USE_CRC_ ERR	INJECT_RT TN_CRC_ ERR
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–		Write Clears All, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION			DECODE			
RESET_EFUSE_CRC_ERR	2	Reset eFuse CRC error status to 0						
INJECT_EFUSE_CRC_ERR	1	Set this bit before reading eFuse values to inject error to eFuse CRC value. Use for ASIL evaluation purposes.			0b0: Do not inject eFuse CRC errors 0b1: Inject eFuse CRC errors			
INJECT_RTTN_CRC_ERR	0	Set this bit before going into sleep mode to inject error to RTTN CRC value. Use for ASIL evaluation purposes.			0b0: Do not inject retention memory CRC errors 0b1: Inject retention memory CRC errors			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**CTRL9 (0x5009)**

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	LOCKED_B	–	–	–
Reset	0b0	0b0	–	–	0b0	–	–	–
Access Type			–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_B	3	GMSL link locked (bidirectional). For Link B only.	0b0: GMSL link B not locked 0b1: GMSL link B locked

**INTR10 (0x5010)\***

BIT	7	6	5	4	3	2	1	0
Field	RTTN_CRC_ERR_OEN	IDLE_ERR_OEN_B	FEC_RX_ERR_OEN_B	VDD18_OV_OEN	MAX_RT_OEN_B	RT_CNT_OEN_B	PKT_CNT_OEN_B	VDD_OV_OEN
Reset	0b1	0b0	0b0	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RTTN_CRC_ERR_OEN	7	Retention Memory Restore CRC Error Output Enable  If this bit is set, RTTN_CRC_ERR is passed on to the ERRB logic and affects the ERRB output.	0b0: Disabled 0b1: Enabled
IDLE_ERR_OEN_B	6	Enable reporting of Link B idle-word errors (IDLE_ERR_FLAG_B) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
FEC_RX_ERR_OEN_B	5	Enable reporting of Link B FEC receive errors exceeding thresholds (FEC_ERR_FLAG) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VDD18_OV_OEN	4	Enable VDD18 overvoltage status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN_B	3	Enable reporting of Link B combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN_B	2	Enable reporting of Link B combined ARQ retransmission event flag (RT_CNT_FLAG) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN_B	1	Enable reporting of Link B packet count flag (PKT_CNT_FLAG_B) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VDD_OV_OEN	0	Enable VDD overvoltage status on ERRB	0b0: Reporting disabled 0b1: Reporting enabled



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**INTR11 (0x5011)**

BIT	7	6	5	4	3	2	1	0
Field	RTTN_CRC_INT	IDLE_ERR_FLAG_B	FEC_RX_ERR_FLAG_B	VDD18_OV_FLAG	MAX_RT_FLAG_B	RT_CNT_FLAG_B	PKT_CNT_FLAG_B	VDD_OV_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Clears All	Read Only	Read Only	Read Only	Read Clears All

BITLEN	BITS	DESCRIPTION	DECODE
RTTN_CRC_INT	7	Retention Memory Restore CRC Error Interrupt.  When the device wakes up, contents of retention memory is loaded back to main registers. The restored data is covered by CRC. If CRC fails, this bit is set.	0b0: Flag not asserted 0b1: Flag asserted
IDLE_ERR_FLAG_B	6	Idle-Word Error Flag for Link B  Asserted when IDLE_ERR_B ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted
FEC_RX_ERR_FLAG_B	5	FEC Receive Errors Flag for Link B  Asserted when the FEC receiver correctable OR uncorrectable error counters exceeded their thresholds for the first time. When reading this flag, the status gets cleared. The FEC statistics counters must also be reset for this flag to be asserted again. See the CLEAR_STATS register to reset the counters.	0b0: Flag not asserted 0b1: Flag asserted
VDD18_OV_FLAG	4	Sticky status value for V <sub>DD</sub> overvoltage	0b0: Overvoltage condition not detected 0b1: Overvoltage condition detected
MAX_RT_FLAG_B	3	Combined ARQ maximum retransmission limit error flag for Link B.  Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN register bit.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG_B	2	Combined ARQ retransmission event flag for Link B  Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN register bit.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG_B	1	Packet Count Flag for Link B  Asserted when PKT_CNT_B ≥ PKT_CNT_THR.	0b0: Flag not asserted 0b1: Flag asserted
VDD_OV_FLAG	0	Sticky status value for V <sub>DD</sub> overvoltage flag	0b0: Overvoltage condition not detected 0b1: Overvoltage condition detected

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**INTR13 (0x5012)**

BIT	7	6	5	4	3	2	1	0
Field	FEC_B_INACTIVE_OEN	FEC_A_INACTIVE_OEN	–	–	–	–	video_mem_overflow_oen	LOSS_OF_LOCK_OEN
Reset	0b0	0b0	–	–	–	–	0b0	0b0
Access Type	Write, Read	Write, Read	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_B_INACTIVE_OEN	7	Enable reporting of link B FEC handshake error (FEC_B_INACTIVE) at the ERRB pin.	0x0: Reporting is disabled 0x1: Reporting is enabled
FEC_A_INACTIVE_OEN	6	Enable reporting of link A FEC handshake error (FEC_A_INACTIVE) at the ERRB pin.	0x0: Reporting is disabled 0x1: Reporting is enabled
video_mem_overflow_oen	1	Enable reporting of BACKTOP video memory overflow error (video_mem_overflow) at the ERRB pin.	0x0: Reporting is disabled 0x1: Reporting is enabled
LOSS_OF_LOCK_OEN	0	Enable reporting loss-of-lock detection (LOSS_OF_LOCK_FLAG) at the ERRB pin.	0x0: Reporting is disabled 0x1: Reporting is enabled

**INTR14 (0x5013)**

BIT	7	6	5	4	3	2	1	0
Field	FEC_B_INACTIVE	FEC_A_INACTIVE	–	–	–	–	video_mem_overflow	LOSS_OF_LOCK_FLAG
Reset	0b0	0b0	–	–	–	–	0b0	0b0
Access Type	Read Clears All	Read Clears All	–	–	–	–	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_B_INACTIVE	7	Error flag indicating that when the FEC Decoder on link B is enabled through the config pin, the expected FEC Encoder handshake Info-Frame from the Serializer is not received 1ms past link B lock. The handshake is required before the FEC Decoder is officially turned ON. This is a clear-on-read sticky error flag.	0x0: No error is detected 0x1: Error is detected
FEC_A_INACTIVE	6	Error flag indicating that when the FEC Decoder on link A is enabled through the config pin, the expected FEC Encoder handshake Info-Frame from the Serializer is not received 1ms past link A lock. The handshake is required before the FEC Decoder is officially turned ON. This is a clear-on-read sticky error flag.	0x0: No error is detected 0x1: Error is detected

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
video_mem_overflow	1	Flag indicating that 1 or more of the following BACKTOP memory overflow errors are detected: 1) Video pipe Y Line Memory Overflow (LMO_Y) 2) Video pipe Z Line Memory Overflow (LMO_Z) 3) Video pipe Y Command FIFO overflow (cmd_overflow2) 4) Video pipe Z Command FIFO overflow (cmd_overflow3)  User can poll the individual error flags, LMO_Y, LMO_Z, cmd_overflow2, and cmd_overflow3 in the BACKTOP11 register to determine which specific error(s) are detected.	0x0: No BACKTOP memory overflow errors are detected 0x1: One of more BACKTOP memory overflow errors are detected
LOSS_OF_LOCK_FLAG	0	Loss of lock detection flag (sticky)	0x0: No loss of GMSL lock or MIPI video output is detected 0x1: Loss of GMSL lock (lock_cfg=0) or loss of MIPI video output (lock_cfg=1) detection flag

#### INTR12 (0x5018)\*

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	—	—
Reset	—	—	—	—	—	—	—	—
Access Type	—	—	—	—	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_ID_B	4:0	GPIO ID used for receiving ERR_RX for Link B	0bXXXXX: Value of GPIO ID for receiving ERR_RX

#### CNT2 (0x5024)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	—	—
Reset	—	—	—	—	—	—	—	—
Access Type	—	—	—	—	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_B	7:0	Number of idle-word errors detected for Link B  Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle-word errors detected

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**CNT3 (0x5025)**

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_B	7:0	<p>Number of received packets of a selected type for Link B.</p> <p>Packet type is selected with PKT_CNT_SEL register.</p> <p>Reported packet count is a scaled value, such that actual packet count is <math>\geq \text{PKT\_CNT} \times (2^{\text{PKT\_CNT\_EXP}})</math> and <math>&lt; (\text{PKT\_CNT} + 1) \times (2^{\text{PKT\_CNT\_EXP}})</math>.</p> <p>When maximum value is reported, packet count is greater or equal to the reported value.</p>	0xXX: Scaled number of received packets

**VIDEO\_RX13 (0x501A)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOSS_OF_VIDEO_LOCK_OEN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOSS_OF_VIDEO_LOCK_OEN	0	Enable reporting loss of pipe Y video lock (VIDEO_RX13::LOSS_OF_VIDEO_LOCK) at the ERRB pin	0x0: Reporting is disabled 0x1: Reporting is enabled

**VIDEO\_RX14 (0x501B)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOSS_OF_VIDEO_LOCK
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
LOSS_OF_VIDEO_LOCK	0	Loss of pipe Y video lock detection flag (sticky)	0x0: Loss of pipe Y video lock is NOT detected 0x1: Loss of pipe Y video lock is detected

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

VIDEO\_RX13 (0x5020)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOSS_OF_VIDEO_LOCK_OEN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOSS_OF_VIDEO_LOCK_OEN	0	Enable reporting loss of pipe Z video lock (VIDEO_RX14::LOSS_OF_VIDEO_LOCK) at the ERRB pin	0x0: Reporting is disabled 0x1: Reporting is enabled

VIDEO\_RX14 (0x5021)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOSS_OF_VIDEO_LOCK
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
LOSS_OF_VIDEO_LOCK	0	Loss of pipe Z video lock detection flag (sticky)	0x0: Loss of pipe Z video lock is NOT detected 0x1: Loss of pipe Z video lock is detected

TX0 (0x5028)\*

For GMSL Link B

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD	RSVD	–	–	RX_FEC_EN	RSVD
Reset	0b01		0b1	0b0	–	–	0b0	0b0
Access Type					–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
RX_FEC_EN	1	Enable forward error correction (FEC) on Link B in forward direction. For GMSL3 parts, bit is set according to the latched CFG1 pin value at power-up.

TX1 (0x5029)\*

For GMSL Link B

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_GEN	RSVD	–	ERRG_EN_B	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	–	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_GEN	7	Enable link PRBS-7 generator	0x0: Disabled 0x1: Enabled
ERRG_EN_B	4	Error generator enable for Link B (reverse channel). Error injection applies to all data going across the link.	0b0: Link B error generator disabled 0b1: Link B error generator enabled

### TX2 (0x502A)\*

For GMSL Link B

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0b00		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error-generator average-bit error rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits
ERRG_BURST	3:1	Error-generator burst-error length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error-generator error-distribution selection	0b0: Pseudorandom 0b1: Periodic

### TX3 (0x502B)\*

For GMSL Link B

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RX_FEC_ACTIVE	RSVD	–	RSVD[2:0]		
Reset	0b01		0b0	0b0	–	0b100		
Access Type			Read Only		–			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION
RX_FEC_ACTIVE	5	FEC is active

#### RX0 (0x502C)\*

For GMSL Link B

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
Reset	0b00		0x0	0b0	0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Select the subtype of low-bandwidth packets to count at PKT_CNT register	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Select the type of received packets to count at PKT_CNT register	0x0: None 0x1: VIDEO 0x2: Reserved 0x3: INFO Frame 0x4: SPI 0x5: I2C 0x6: UART 0x7: GPIO 0x8: Reserved 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All 0xF: Unknown and packets with error

#### GPIOA (0x5030)\*

For GMSL Link B

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0b1	0b000001					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. For Link B.  This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link.  Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**GPIOB (0x5031)\***

For GMSL Link B

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0b10		0b001000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet. For Link B.  This allows grouping transitions of different GPIO inputs in a single packet and so increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. For Link B.  This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link.  Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

**RX0 (0x5050)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN_B	–	–	–	–	–	STR_SEL_B[1:0]	
Reset	0b0	–	–	–	–	–	0b00	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_B	7	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL_B	1:0	Reserved. Do not use (legacy). Use register 0x161 VIDEO_PIPE_SEL instead.	

**RX0 (0x5051)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN_B	–	–	–	–	–	STR_SEL_B[1:0]	
Reset	0b0	–	–	–	–	–	0b01	
Access Type	Write, Read	–	–	–	–	–	Write, Read	



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_B	7	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL_B	1:0	Reserved. Do not use (legacy). Use register 0x161 VIDEO_PIPE_SEL instead.	

**RX0 (0x5052)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN_B	–	–	–	–	–	STR_SEL_B[1:0]	
Reset	0b0	–	–	–	–	–	0b10	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_B	7	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL_B	1:0	Reserved. Do not use (legacy). Use register 0x161 VIDEO_PIPE_SEL instead.	

**RX0 (0x5053)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN_B	–	–	–	–	–	STR_SEL_B[1:0]	
Reset	0b0	–	–	–	–	–	0b11	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_B	7	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL_B	1:0	Reserved. Do not use (legacy). Use register 0x161 VIDEO_PIPE_SEL instead.	

**TR0 (0x5060)\***

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculate and append CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

**TR1 (0x5061)\***

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Used to calculate percentage of total link bandwidth used for this port.  Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base BW value

**TR3 (0x5063)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	<p>Source identifier used in packets transmitted from this channel.</p> <p>Default value is based on the device address set by the CFG0 pin.</p>	0bXXX: Source ID for packets from this channel

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**TR4 (0x5064)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receive packets from selected sources. Each bit indicates if packets with that source ID should be received or not. This is a one-hot encoding.  For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

**TR0 (0x5070, 0x5080, 0x5088)\***

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculate and append CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

**TR1 (0x5071, 0x5081, 0x5089)\***

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Used to calculate percentage of total link bandwidth used for this port.  Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base BW value

**TR3 (0x5073, 0x5083, 0x508B)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this channel.  Default value is based on the device address set by the CFG0 pin.	0bXXX: Source ID for packets from this channel

**TR4 (0x5074, 0x5084, 0x508C)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receive packets from selected sources. Each bit indicates if packets with that source ID should be received or not. This is a one-hot encoding.  For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**ARQ0 (0x5075, 0x5085, 0x508D)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	EN_B	DIS_DBL_A CK_RETX_ B	–	–
Reset	0b1	0b0	0b0	0b1	0b1	0b0	–	–
Access Type					Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN_B	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled
DIS_DBL_A CK_RETX_B	2	Disable retransmission due to receiving same acknowledge twice	0b0: Enabled 0b1: Disabled

**ARQ1 (0x5076, 0x5086, 0x508E)\***

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_E RR_OEN_B	RT_CNT_O EN_B
Reset	–	0b111			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER R_OEN_B	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmission limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmission limit errors reporting at ERRB pin enabled
RT_CNT_OE N_B	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin.  When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

**ARQ2 (0x5077, 0x5087, 0x508F)**

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_E RR_B	RT_CNT_B[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER R_B	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

**TR0 (0x5078)\***

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

**TR1 (0x5079)\***

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]				BW_VAL_B[5:0]			
Reset	0b10				0b110000			
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE			
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor			0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16			
BW_VAL_B	5:0	Channel bandwidth-allocation base. Used to calculate percentage of total link bandwidth used for this port.  Fair bandwidth use ratio = $BW\_VAL \times BW\_MULT / 10$ as a percentage of total link bandwidth.			0bXXXXXX: Channel base BW value			

**TR3 (0x507B)\***

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this channel.  Default value is based on the device address set by the CFG0 pin.	0bXXX: Source ID for packets from this channel

**TR4 (0x507C)\***

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receive packets from selected sources. Each bit indicates if packets with that source ID should be received or not. This is a one-hot encoding.  For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... 0xFF: Packets from all source IDs received

**ARQ0 (0x507D)\***

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	EN_B	DIS_DBL_A CK_RETX_B	–	–
Reset	0b1	0b0	0b0	0b1	0b1	0b0	–	–
Access Type					Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN_B	3	Enable ARQ	0b0: ARQ disabled 0b1: ARQ enabled
DIS_DBL_A CK_RETX_B	2	Disable retransmission due to receiving same acknowledge twice	0b0: Enabled 0b1: Disabled

**ARQ1 (0x507E)\***

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_E RR_OEN_B	RT_CNT_O EN_B
Reset	–	0b111			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER R_OEN_B	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OE N_B	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin.  When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

#### ARQ2 (0x507F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ER RR_B	RT_CNT_B[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER R_B	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

#### GPIO\_A (0x52B0)\*

GPIO 0

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_ EN_B	–	–	GPIO_RX_ EN_B	GPIO_TX_ EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b1	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E N_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_E N_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E N_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52B1)\*

GPIO 0



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52B2)\*

GPIO 0

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b00000				
Access Type	–	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value from across the GMSL link	
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52B3)\*

GPIO 1

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52B4)\*

GPIO 1

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b00001				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52B5)\*

GPIO 1

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b00001				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52B6)\*

GPIO 2

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52B7)\*

GPIO 2

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b00010				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52B8)\*

GPIO 2

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b00010				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52B9)\*

GPIO 3

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52BA)\*

GPIO 3

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b00011				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52BB)\*

GPIO 3

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b00011				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52BC)\*

GPIO 4

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52BD)\*

GPIO 4

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b00100				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52BE)\*

GPIO 4

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b00100				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52BF)\*

GPIO 5

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52C0)\*

GPIO 5

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b00101				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52C1)\*

GPIO 5

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b00101				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52C2)\*

GPIO 6

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b1	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52C3)\*

GPIO 6

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b00110				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52C4)\*

GPIO 6

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b00110				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52C5)\*

GPIO 7

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52C6)\*

GPIO 7

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b00111				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52C7)\*

GPIO 7

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b00111				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52C8)\*

GPIO 8

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52C9)\*

GPIO 8



MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b01000				
Access Type	–	–	–	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

#### GPIO\_C (0x52CA)\*

GPIO 8

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b01000				
Access Type	–		–	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

#### GPIO\_A (0x52CB)\*

GPIO 9

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_EN_B	5	Enables jitter minimization compensation			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			

#### GPIO\_B (0x52CC)\*

GPIO 9

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b01001				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52CD)\*

GPIO 9

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b01001				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52CE)\*

GPIO 10

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52CF)\*

GPIO 10

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b01010				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52D0)\*

GPIO 10

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b01010				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52D1)\*

GPIO 11

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52D2)\*

GPIO 11

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b01011				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

#### GPIO\_C (0x52D3)\*

GPIO 11

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b01011				
Access Type	–		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

#### GPIO\_A (0x52D4)\*

GPIO 12

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	TX_COMP_EN_B	–	–	GPIO_RX_EN_B	GPIO_TX_EN_B	–
Reset	–	0b0	0b0	–	–	0b0	0b0	–
Access Type	–		Write, Read	–	–	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	5	Enables jitter minimization compensation	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_RX_EN_B	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN_B	1	GPIO Tx source control. Set to 1 to transmit the local MFP input value across the GMSL link.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

#### GPIO\_B (0x52D5)\*

GPIO 12

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GPIO_TX_ID_B[4:0]				
Reset	–	–	–	0b01100				
Access Type	–	–	–	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

#### GPIO\_C (0x52D6)\*

GPIO 12

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	–	0b01100				
Access Type	–		–	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

MAX96792A

Dual GMSL3/2 to CSI-2 Deserializer

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/22	Initial Release for Market Intro	-

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