*Click **here** to ask an associate for production status of specific part numbers.*

MAX96752

GMSL2 Deserializer with Dual LVDS (OLDI) Output

General Description

The MAX96752 deserializers convert a single- or dual-link GMSL™ serial input to single or dual OLDI. They also send and receive side-channel and peripheral control data, enabling full-duplex, single-wire transmission of video and bidirectional data.

The OLDI output can be configured as single-port (4 or 8 lanes) or dual-port (2 x 4 lanes) for flexibility in driving displays with a variety of resolutions. Each port accommodates pixel clock rates of up to 150MHz, and in dual-port mode, the MAX96752 support a combined pixel clock of up to 300MHz.

The GMSL2 concurrent control channel operates in I^2C or UART mode. Two additional pass-through I^2C or UART channels and a pass-through SPI channel are provided for peripheral control. The bidirectional audio channel supports I^2S stereo and up to 8 channels in TDM mode.

Operation is specified over the -40°C to +105°C automotive temperature range. The devices are AEC-Q100 qualified.

Data can be transmitted over low-cost 50Ω Coax or 100Ω STP cables that meet the GMSL2 channel specification.

Table 1. Typical Maximum Cable Length vs. Attenuation

	3.2mm Ø 50Ω Coax, Foam Dielectric	2.7mm Ø 50Ω Coax, Solid Dielectric	100Ω Shielded Twisted Pair, AWG26
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, +105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at +105°C**		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m

Applications

- Cluster and Heads-Up Displays
- Central Information Displays
- Rear-Seat Infotainment Displays

Benefits and Features

- 1 x 4, 2 x 4, or 1 x 8 OLDI Output Lane Configurations
- 3Gbps or 6Gbps Forward Link Rates for System and Power Flexibility
- Full-Duplex Capability Over a Single Wire
- Supports Up to 300MHz PCLK
- Supports Video Replication and Dual-View Splitting for Driving Two Displays
- Uses Low-Cost 50Ω Coax or 100Ω STP Cables
- Forward and Reverse I^2S or 7.1 TDM Audio
- Optional Internal VDD Regulator
- ASIL-Relevant Functional Safety Features
  - ASIL-B Compliant
  - 16-Bit CRC Protection of Control Channel Data (I^2C, UART, SPI, GPIO, Audio)

    Retransmission of All Control Channel Data (I^2C, UART, SPI, GPIO, Audio) Upon Error Detection
  - Optional 32-Bit Video Line Cyclic Redundancy Check (CRC)
  - Selectable Interrupts for Fault Detection
  - Video Watermark Detection
- Performance Tools Ensure High Link Margin
  - Continuous Adaptive Equalization on GMSL links
  - Forward and Reverse Channel Pseudorandom Binary Sequence (PRBS) Generator and Checker for BER Testing of Serial I/O Links
  - Eye-Opening Monitor for Continuous Link Margin Diagnosis
- Concurrent Control Channel for Device Configuration and Communicating with Remote Peripherals
  - I^2C, UART, Pass-Through I^2C/UART, SPI, and Tunneled or Register-Programmable GPIO
  - Settable Priority Levels
  - Eight Hardware Programmable Device Addresses
  - Up to 14 Programmable General Purpose Input/Output (GPIO)
  - Sleep Mode with Register State Retention
- Compact 8mm x 8mm TQFN Package with Exposed Pad

***Ordering Information** appears at end of data sheet.*

19-101779; Rev 0; 1/24

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Simplified Block Diagram

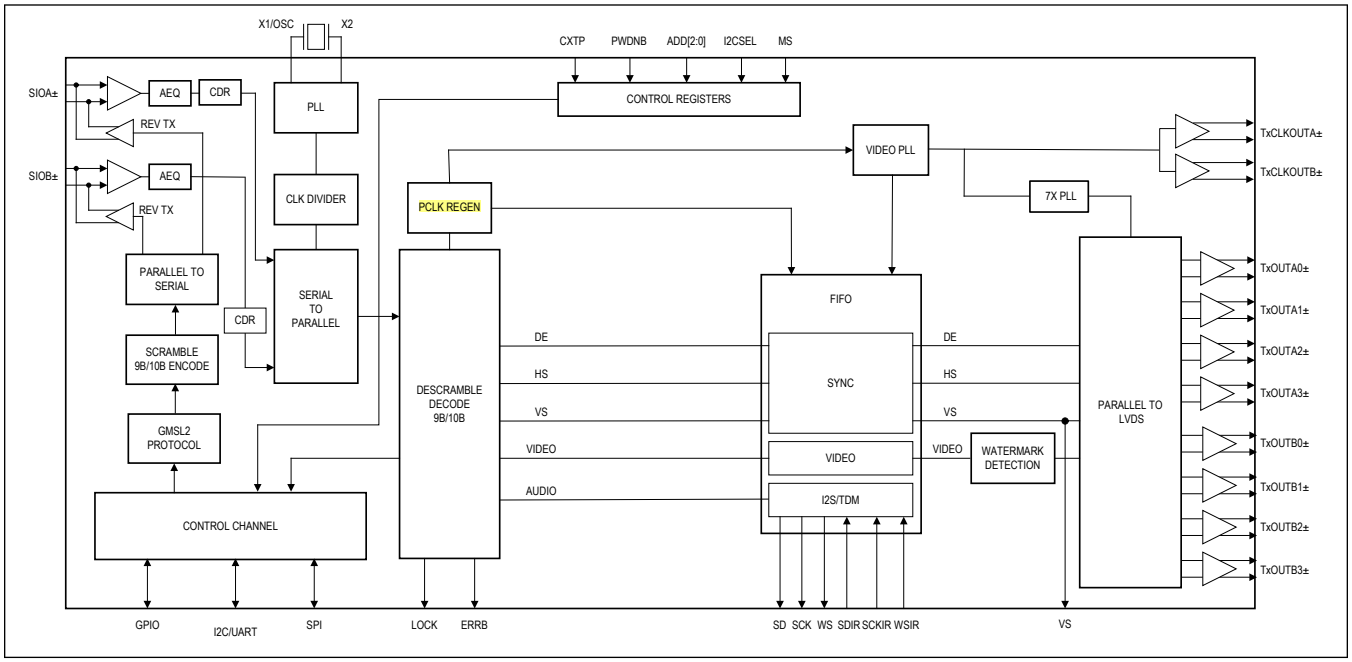


TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Simplified Block Diagram . . . 2
Absolute Maximum Ratings . . . 8
Package Information . . . 8
56-Pin TQFN . . . 8
56-Pin TQFN-SW (Side-Wettable) . . . 8
Electrical Characteristics . . . 9
Typical Operating Characteristics . . . 16
Pin Configuration . . . 17
Pin Description . . . 17
Recommended Operating Conditions, External Component Requirements, and ESD Protection . . . 23
Functional Diagrams . . . 25
Detailed Description . . . 29
Additional Documentation . . . 29
Introduction . . . 29
Product Overview . . . 29
OLDI Pixel Clock and Pixel Interleaving . . . 29
Deserializer Modes . . . 29
Single Video Stream, Single GMSL2 Link . . . 30
Single Video Stream, Dual GMSL2 Links . . . 30
Single Video Stream with Serializer Replication . . . 30
Single Video Stream with OLDI Deserializer Replication . . . 31
Serializer Dual-View Mode with OLDI Deserializer Splitter Mode . . . 31
Other Functions . . . 31
GMSL2 Protocol . . . 31
GMSL2 Physical Layer . . . 32
Cabling Options . . . 32
Line Fault . . . 32
Line Fault in AC-Coupled Ground Applications . . . 33
GMSL2 Bandwidth Sharing . . . 33
GMSL2 Bandwidth Calculations . . . 34
Power Supplies . . . 34
Thermal Management . . . 35
Control Channel and Side Channels . . . 35
Primary I^2C/UART . . . 35
Pass-Through I^2C/UART . . . 36
Serial Peripheral Interface (SPI) . . . 36

TABLE OF CONTENTS (CONTINUED)

- I^2S/TDM Audio . . . 36
- Control Channel Latencies . . . 36
- General-Purpose Inputs and Outputs (GPIO) . . . 36
- Multifunction Pin Assignments . . . 37
- SPI and I^2S Speed Programming . . . 38
- Latch-On Power-Up Pins . . . 38
- Clocking . . . 39
  - GMSL Reference Clock . . . 39
  - Spread-Spectrum Clocking (SSC) . . . 39
- Power-Up and Link Start-Up . . . 39
  - Device Reset . . . 40
- Link and Video Lock . . . 40
  - GMSL2 Link Lock . . . 41
  - Video Lock . . . 42
- Power Standby and Sleep Mode . . . 42
- Error and Fault Condition Monitoring . . . 42
- Adaptive Equalization (AEQ) . . . 42
- Video Pipeline . . . 43
  - Video Line Cyclic Redundancy Check (CRC) . . . 43
  - Rx Crossbar, Video PRBS Checker, and Watermark Checker . . . 43
  - Video-Timing Constraints . . . 43
- Eye-Opening Monitor (EOM) . . . 43
- Watermarking . . . 43
- Vertical Sync Output for Backlight Pulse-Width Modulation (PWM) Synchronization . . . 43
- Pseudorandom Binary Sequence (PRBS) . . . 44
  - Video PRBS . . . 44
  - Audio PRBS . . . 44
- OpenLDI (OLDI) Deserializer Video Output . . . 44
  - Overview . . . 44
  - Odd/Even Pixel Interleaving in Dual OLDI Mode . . . 44
  - Maximum OLDI Pixel Clock . . . 44
  - Flexible Output Programming . . . 44
  - Color Lookup Table (LUT) . . . 44
  - Spread-Spectrum . . . 44

Applications Information . . . 45
- Software Programming Model . . . 45
- Programming Notes . . . 45
  - Mandatory Register Programing . . . 45
- Control-Channel Programming . . . 45

TABLE OF CONTENTS (CONTINUED)

Device Address . . . 46
I2C Programming . . . 46
I2C Write-Packet Format . . . 46
I2C Read-Packet Format . . . 46
Host-to-Peripheral Primary I2C and Pass-Through I2C Communication . . . 46
UART Programming . . . 46
UART Base Mode . . . 46
UART Bypass Mode . . . 47
Switching Between UART Base and Bypass Modes . . . 47
UART Frame Format . . . 47
Synchronization Frame . . . 48
Acknowledge Frame . . . 48
Write Packet . . . 48
Read Packet . . . 48
Ordering Information . . . 49
Register Map . . . 50
MAX96752 . . . 50
Register Details . . . 64
Revision History . . . 159

LIST OF FIGURES

Figure 1. Serial Output Parameters . . . 25
Figure 2. Video Initialization Time . . . 26
Figure 3. Video Latency . . . 26
Figure 4. LVDS Output Pulse Positions . . . 26
Figure 5. I^2C Timing Parameters. . . . 27
Figure 6. SPI Main Mode Timing Parameters . . . 27
Figure 7. SPI Subordinate Mode Timing Parameters . . . 28
Figure 8. I^2S Main Timing Diagram . . . 28
Figure 9. I^2S Subordinate Timing Diagram . . . 28
Figure 10. Single Video Stream, Single GMSL2 Link at Either 3Gbps or 6Gbps, MAX96752 Deserializer with Single or Dual OLDI Outputs . . . 30
Figure 11. Single Video Stream, Dual GMSL2 Links with Both at Either 3Gbps or 6Gbps, MAX96752 Deserializer with Single or Dual OLDI Outputs . . . 30
Figure 12. Serializer Replication, Dual GMSL2 Links, OLDI Deserializers with Single or Dual OLDI Outputs . . . 30
Figure 13. Single Stream OLDI Deserializer, Identical Video on Both Displays . . . 31
Figure 14. Serializer Dual-View Splitter Mode, Convert Dual-View to Pixel Interleave, Send Dual-Views Down Single GMSL2 Link, Dual OLDI Deserializer Splits Pixel Interleaved Dual-View, Each Video Stream (View) Must Have Identical Timing, Can Also Be Done in Dual GMSL2 Link Mode . . . 31
Figure 15. Typical GMSL2 Link Application Circuit for Coax Cable . . . 33
Figure 16. Typical GMSL2 Link Application Circuit for Twisted Pair . . . 33
Figure 17. GMSL2 Lock Time . . . 41
Figure 18. I^2C Write-Packet Format . . . 46
Figure 19. I^2C Read-Packet Format . . . 46
Figure 20. GMSL2 UART Protocol for Base Mode . . . 47
Figure 21. UART Data Format for Base Mode . . . 48
Figure 22. UART Synchronization Frame . . . 48
Figure 23. UART Acknowledge Frame . . . 48
Figure 24. UART Write-Packet Format . . . 48
Figure 25. UART Read-Packet Format . . . 49

LIST OF TABLES

Table 1. Typical Maximum Cable Length vs. Attenuation . . . 1
Table 2. Recommended Operating Conditions . . . 23
Table 3. External Component Requirements . . . 23
Table 4. ESD Protection . . . 24
Table 5. Forward and Reverse Link Bandwidth Utilization . . . 34
Table 6. Typical Control Channel Latencies . . . 36
Table 7. Typical GPIO Delays for Forward and Reverse Link Transmission . . . 37
Table 8. GPIO Pin Function Map . . . 37
Table 9. Control- and Side-Channel Typical Rise and Fall Times . . . 38
Table 10. Recommended I^2S Pin Programming . . . 38
Table 11. Recommended SPI Pin Programming . . . 38
Table 12. Device Address . . . 39
Table 13. GMSL Link Conditions . . . 45
Table 14. Mandatory Register Writes . . . 45

Absolute Maximum Ratings

(All voltages with respect to ground.) .....
V_{DDIO} ..... -0.3V to +3.9V
V_{DD18} ..... -0.3V to +2.0V
V_{DDD}, V_{DDA} ..... -0.3V to +1.1V
V_{REG}, V_{REGA} ..... -0.3V to +2.0V
SIO__ (Active State) (*Note a*)..... (V_{DD18} - 1.1V) to V_{DD18}
SIO__ (Inactive State) (*Note a*) ..... -0.3V to +1.1V
XRES, X2 ..... -0.3V to (V_{DD18} + 0.3V)
All Other Pins (*Note b*) ..... -0.3V to (V_{DDIO} + 0.3V)
Continuous Power Dissipation (T_A = +70°C TQFN) (Multilayer board, derate 40mW/°C above +70°C) 2200mW
Storage Temperature Range .....-40°C to +150°C
Soldering Temperature (Reflow)..... +260°C

Note a: Active State means the device is powered up and not in Sleep or Power-down modes. Inactive means the device is not powered up or powered up in Sleep or Power-down mode.

Note b: Specified maximum voltage or 3.9V, whichever is lower.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56-Pin TQFN

Package Code	T5688+6
Outline Number	21-0135
Land Pattern Number	90-100041
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	25°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1°C/W

56-Pin TQFN-SW (Side-Wettable)

Package Code	T5688Y+6
Outline Number	21-100046
Land Pattern Number	90-100048
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	25°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board in still air. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V or V_{REG} = V_{REGA} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL2 DESERIALIZER REVERSE CHANNEL SERIAL OUTPUTS (SIO_P, SIO_N) —See Figure 1						
Output Voltage Swing (Single-Ended)	V_O	R_L = 100Ω ±1%	190	250	310	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, peak-to-peak differential voltage	380	500	620	mV
Change in V_{OD} between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)} - V_{OD(L)} \rvert$			25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state	V_{DD18} - 0.45	V_{DD18} - 0.3	V_{DD18} - 0.15	V
Change in V_{OS} between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert (V_{OS(H)} - V_{OS(L)}) \rvert$			25	mV
Termination Resistance (Internal)	R_T	Any Pin to V_{DD18}	50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / LVDS OUTPUTS						
Differential Output Voltage	V_{OD}	Full swing enabled	250		450	mV
		Half swing enabled	125		225	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}				25	mV
Common-Mode Voltage	V_{OS}		1.125		1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}				25	mV
Output Short Circuit Current	I_{OS}	Tx_ pin shorted to 0V or V_{DD18}	-15		+15	mA
Magnitude of Differential Output Short Circuit Current	I_{OSD}	Differential output pair shorted together			15	mA
Output High Impedance Current	I_{OZ}	Output powered down, Tx_ pin shorted to 0V or V_{DD18}	-0.5		+0.5	µA
DC ELECTRICAL CHARACTERISTICS / I/O PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V or V_{REG} = V_{REGA} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup/Pulldown Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup Resistance	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Internal Pulldown Resistance	R_{PD}			1		MΩ
Input Capacitance	C_{IN}			3		pF
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2)						
X1 Input Capacitance	C_{IN_X1}			5.5		pF
X2 Input Capacitance	C_{IN_X2}			4		pF
Internal X2 Limit Resistor	R_{LIM}			1.2		kΩ
Internal Feedback Resistor	R_{FB}			10		kΩ
Transconductance	g_m			28		mA/V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1, X2 UNCONNECTED)						
High-Level Input Voltage	V_{IH}		0.9			V

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V or V_{REG} = V_{REGA} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}					0.4	V
Input Impedance	R_{IN}				10		kΩ
X1 Input Capacitance	C_{IN_X1}				5.5		pF
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS							
Supply Current	I_{DD}	148.5MHz PCLK, dual OLDI output at 74.25MHz, color bar pattern. (Note 2)	V_{DD18}		125	180	mA
			V_{DDD}		83	250	
			V_{DDA}		7	15	
			V_{REG} (Note 3)		75	250	
			V_{REGA} (Note 3)		8	20	
Maximum V_{DDIO} Supply Current	I_{DDIO}	Per GPIO toggling at 50 MHz, CL = 10pF	V_{DDIO} at 1.9V		44		µA/MHz
			V_{DDIO} at 3.6V		81		
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Maximum Power-Down Current (Note 3)	I_{DD}	V_{DDIO} at 3.6V	T_A = 25ºC		4		µA
			T_A = 105ºC		5		
		V_{DD18} at 1.9V	T_A = 25ºC		18		
			T_A = 105ºC		37		
		V_{DDD} at 1.05V	T_A = 25ºC		7		
			T_A = 105ºC		15		
		V_{DDA} at 1.05V	T_A = 25ºC		4		
			T_A = 105ºC		10		
		V_{REG} at 1.9V	T_A = 25ºC		0		
			T_A = 105ºC		1		
		V_{REGA} at 1.9V	T_A = 25ºC		0.2		
			T_A = 105ºC		1		
DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENT							
Maximum Sleep Current (Note 3)	I_{DD}	V_{DDIO} at 1.9V	T_A = 25ºC		7		µA
			T_A = 105ºC		7		
		V_{DD18} at 1.9V	T_A = 25ºC		30		
			T_A = 105ºC		50		
		V_{DDD} at 1.05V	T_A = 25ºC		5		
			T_A = 105ºC		15		
		V_{DDA} at 1.05V	T_A = 25ºC		4		
			T_A = 105ºC		10		
		V_{REG} at 1.9V	T_A = 25ºC		4		
			T_A = 105ºC		4		
		V_{REGA} at 1.9V	T_A = 25ºC		0.2		
			T_A = 105ºC		1		

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V or V_{REG} = V_{REGA} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / FORWARD CHANNEL SWITCHING CHARACTERISTICS						
Lock Time	t_{LOCK}	(Note 4) (Note 6)		50		ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from GMSL2 video packet input at SIO± input to when pixels appear at OLDI outputs, assuming link and configuration are already established		0.2 + 45,000 x t_{PCLK}		ms
Maximum Video Latency	t_{VL}	Time from pixel within GMSL2 packet at SIO± to output at OLDI interface		400 x t_{PCLK}		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip		1		ms
AC ELECTRICAL CHARACTERISTICS / DESERIALIZER REVERSE CHANNEL SERIAL OUTPUTS						
GMSL Reverse Channel Transmitter Rise/Fall Time	t_R, t_F	20% to 80%, V_O = 250mV, R_L = 100Ω		2300		ps
Total Serial Output p-p Jitter	t_{TSOJ2}	PRBS7, single-ended or differential output		0.25		UI
Deterministic Serial Output p-p Jitter	t_{DSOJ2}	PRBS7, single-ended or differential output		0.15		UI
AC ELECTRICAL CHARACTERISTICS / LVDS OUTPUTS						
LVDS Clock Frequency	$f_{TXCLKOUT}$	Single OLDI output (Note 2)	6.45		150	MHz
LVDS Output Rise Time	t_R	From 20% to 80%, C_L = 5pF, R_L = 100Ω (Note 2)		170	350	ps
LVDS Output Fall Time	t_F	From 20% to 80%, C_L = 5pF, R_L = 100Ω (Note 2)		170	350	ps
LVDS Output Pulse Position	t_{PPosN}	$f_{TXCLKOUT}$ = 150MHz (Note 2) (Figure 4)	N/ 7xT_{CLK} - 100	N/ 7xT_{CLK}	N/ 7xT_{CLK} + 100	ps
LVDS Output Jitter		$f_{TXCLKOUT}$ = 150MHz, BER = 10^{-12}		110		ps_{P-P}
LVDS Output Enable Time	t_{LVEN}	Measured from the last bit of UART packet that enables the LVDS to the point that LVDS output amplitude crosses 250mV (Note 2)			50	µs
LVDS Output Disable Time	t_{LVDS}	Measured from the last bit of UART packet that enables the LVDS to the point that LVDS output amplitude crosses 0V (Note 2)			50	µs
AC ELECTRICAL CHARACTERISTICS / I^2C/UART PORT TIMING						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO} (Note 2)	20 x V_{DDIO}/5.5V		150	ns
I^2C/UART Wake Time		From power-up or rising edge of PWDNB to local register access; for remote register access, I^2C/UART wake time is the same as lock time (t_{LOCK}).		1.1	4	ms

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V or V_{REG} = V_{REGA} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / I²C TIMING (*Note 2*)						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I²C MST_BT = 010, I²C SLV_SH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I²C MST_BT = 101, I²C SLV_SH = 01)	100		400	
		High f_{SCL} range: (I²C MST_BT = 111, I²C SLV_SH = 00)	400		1000	
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V or V_{REG} = V_{REGA} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load on Each Bus Line	C_B				100	pF
AC ELECTRICAL CHARACTERISTICS / SPI MAIN (See Figure 6)						
Operating Frequency	f_{MCK}		0.588		25	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	(*Note 2*)	$t_{MCK}/2$ - 3	$t_{MCK}/2$		ns
MOSI Data Output Delay	t_{MOD}	After SCLK falling edge (*Note 2*)	-2.3		2.3	ns
MISO Input Setup Time	t_{MIS}	Before programmed sampling edge (*Note 2*)	13.5			ns
MISO Input Hold Time	t_{MIH}	After programmed sampling edge (*Note 2*)	-2			ns
AC ELECTRICAL CHARACTERISTICS / SPI Subordinate (See Figure 7)						
Operating Frequency	f_{SCK}	(*Note 2*)			25	MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns
MISO Data Output Delay	t_{SOD}	After SCLK falling edge (*Note 2*)	0		11.6	ns
MOSI Input Setup Time	t_{SIS}	Before SCLK rising edge (*Note 2*)	5			ns
MOSI Input Hold Time	t_{SIH}	After SCLK rising edge (*Note 2*)	3			ns
AC ELECTRICAL CHARACTERISTICS / I^2S/TDM MAIN TIMING (*Note 2*) (*Note 5*)						
WS Frequency	f_{WS}		8		192	kHz
Sample Word Length	n_{WS}		8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$	0.512		49.152	MHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$	0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$	0.35 x t_{SCK}			ns
SD, WS Valid Time Before SCK	t_{MAVS}	$t_{SCK} = 1/f_{SCK}$	0.2 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{MAVH}	$t_{SCK} = 1/f_{SCK}$	0.2 x t_{SCK}	0.5 x t_{SCK}		ns
AC ELECTRICAL CHARACTERISTICS / I^2S/TDM SUBORDINATE TIMING (*Note 2*) (*Note 5*)						
WS Frequency	f_{WS}	(*Note 2*)	8		192	kHz
Sample Word Length	n_{WS}	(*Note 2*)	8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$ (*Note 2*)	0.512		49.152	MHz
SD, WS Setup Time	t_{SAS}		4			ns
SD, WS Hold Time	t_{SAH}		4			ns

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDD} = V_{DDA} = 0.95V to 1.05V or V_{REG} = V_{REGA} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DDD} = V_{DDA} = 1.0V, T_A = 25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2) (*Note 2*)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1, X2 FLOATING) (*Note 2*)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
Input Jitter		Forward data rate = 6Gbps, Reverse data rate = 187Mbps, sinusoidal jitter < 1MHz (rising edge)			600	ps p-p
Input Duty Cycle	t_{DUTY}		40		60	%
Input Fall Time	T_F	80% to 20%			4	ns

Note 1: Limits are 100% tested at T_A = +105°C unless otherwise noted. Limits within the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: If the V_{DD} regulators are used, use the V_{REG} and V_{REGA} currents instead of the V_{DDD} and V_{DDA} currents. If the regulators are not used, ignore the V_{REG} and V_{REGA} currents and use the V_{DDD} and V_{DDA} currents.

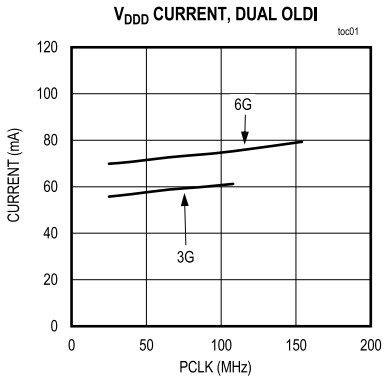
Note 4: From power-up, release of RESET_LINK or rising edge of PWDNB pin to rising edge of LOCK pin. t_{RD} must be <90ms. For more information, see *GMSL2 Link Lock* section.

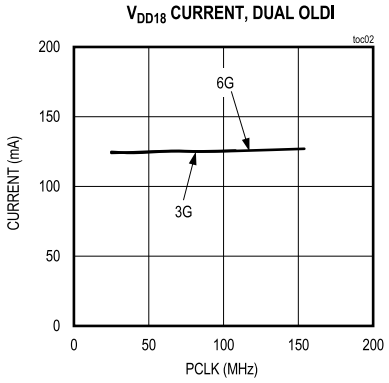
Note 5: Measured at 50MHz. See the *SPI and I²S Speed Programming* section for pin programming recommendations.

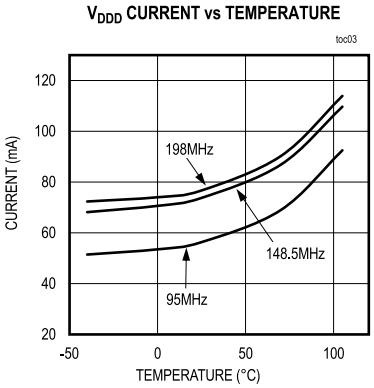
Note 6: Production tested using ECS-250-18-33Q-DS crystal.

Typical Operating Characteristics

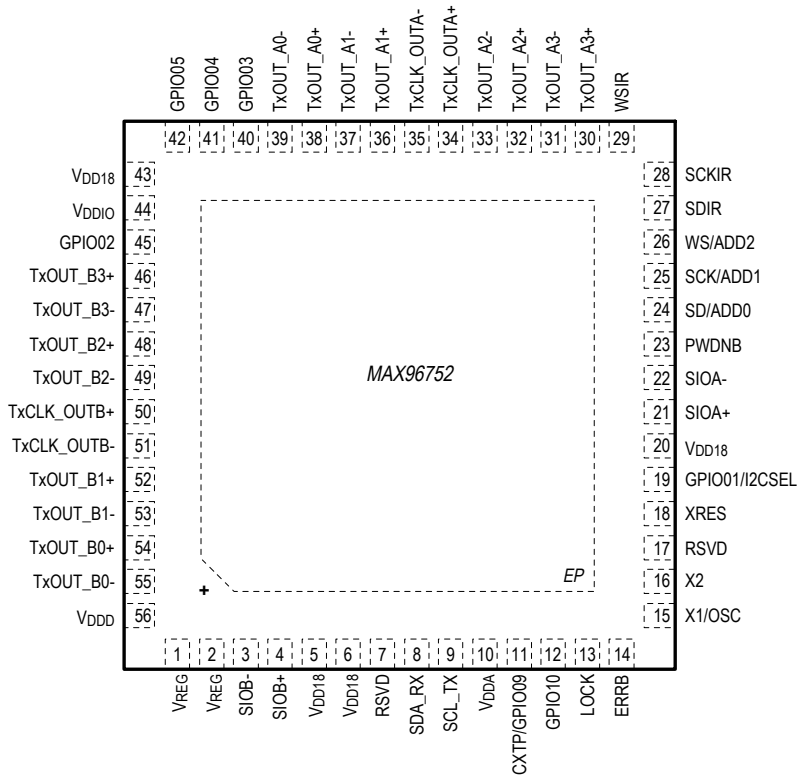
((TA = +25°C unless otherwise noted, 6G = Single GMSL 2 PHY, 6Gbps FWD; 3G = Single GMSL 2 PHY, 3Gbps FWD; 198MHz = Single GMSL 2 PHY, PCLK = 198MHz, 6Gbps FWD; 148MHz = Single GMSL 2 PHY, PCLK = 148.5MHz, 6Gbps FWD; 95MHz = Single GMSL2 PHY, PCLK = 95MHz, 3Gbps FWD))







Pin Configuration



Pin Description

PIN	NAME	FUNCTION MODE SIGNAL NAME	FUNCTION
GMSL2 SERIAL LINK			
21	SIOA+	SIOA+	Noninverted Coax/Twisted-Pair Serial-Data Input 1
22	SIOA-	SIOA-	Inverted Twisted-Pair Serial-Data Input 1
4	SIOB+	SIOB+	Noninverted Coax/Twisted-Pair Serial-Data Input 2
3	SIOB-	SIOB-	Inverted Twisted-Pair Serial-Data Input 2
OLDI INTERFACE (Unused OLDI ports should be powered down using Register: *OLDI2*)			
30	TxOUT_A3+	TxOUT_A3+	LVDS Data Output Port A
31	TxOUT_A3-	TxOUT_A3-	LVDS Data Output Port A
32	TxOUT_A2+	TxOUT_A2+	LVDS Data Output Port A
33	TxOUT_A2-	TxOUT_A2-	LVDS Data Output Port A
36	TxOUT_A1+	TxOUT_A1+	LVDS Data Output Port A
37	TxOUT_A1-	TxOUT_A1-	LVDS Data Output Port A
38	TxOUT_A0+	TxOUT_A0+	LVDS Data Output Port A
39	TxOUT_A0-	TxOUT_A0-	LVDS Data Output Port A

PIN	NAME	FUNCTION MODE SIGNAL NAME	FUNCTION
34	TxCLK_OUTA+	TxCLK_OUTA+	LVDS Clock Output Port A
35	TxCLK_OUTA-	TxCLK_OUTA-	LVDS Clock Output Port A
46	TxOUT_B3+	TxOUT_B3+	LVDS Data Output Port B
47	TxOUT_B3-	TxOUT_B3-	LVDS Data Output Port B
48	TxOUT_B2+	TxOUT_B2+	LVDS Data Output Port B
49	TxOUT_B2-	TxOUT_B2-	LVDS Data Output Port B
52	TxOUT_B1+	TxOUT_B1+	LVDS Data Output Port B
53	TxOUT_B1-	TxOUT_B1-	LVDS Data Output Port B
54	TxOUT_B0+	TxOUT_B0+	LVDS Data Output Port B
55	TxOUT_B0-	TxOUT_B0-	LVDS Data Output Port B
50	TxCLK_OUTB+	TxCLK_OUTB+	LVDS Clock Output Port B
51	TxCLK_OUTB-	TxCLK_OUTB-	LVDS Clock Output Port B
CONTROL AND GPIO (* denotes default state after power-up)			
19	GPIO01/I2CSEL	I2CSEL GPO01* VS	I2CSEL: Control-Channel Interface Select for Primary I^2C/UART with an Internal 1MΩ Pulldown to Ground. State is latched at power-up. Set I2CSEL high to select I^2C interface. Set I2CSEL low to select UART interface. GPO01: Configurable General-Purpose Output. By default, configured to output the GPI01 value received from the serializer. VS: Vertical Sync Push-Pull Output
45	GPIO02	GPIO02* WMD MS	GPIO02: Configurable General-Purpose Input or Output. GMSL2 power-up default is high impedance with an unconnected input receiver. User must drive pin to ground or V_{DDIO} or enable internal pull-up or pull-down resistor. WMD: Watermark Detect Push-Pull Output. High when watermark is detected. MS: UART Mode Select with an Internal 1MΩ Pulldown to Ground. Set MS low to select Base mode. Set MS high to select Bypass mode. MS state can also be temporarily overwritten by a register write. Note: Leave pin unconnected when not used.

PIN	NAME	FUNCTION MODE SIGNAL NAME	FUNCTION
40	GPIO03	GPIO03* MOSI SDA1_RX1	GPIO03: Configurable General-Purpose Input or Output. GMSL2 power-up default is high impedance with an unconnected input receiver. User must drive pin to ground or V_{DDIO} or enable internal pull-up or pull-down resistor. MOSI: SPI Main Out Subordinate In. When configured as the main, push-pull output that drives data to external subordinate. When configured as a subordinate, input with an internal 1MΩ pulldown to ground that receives data from an external main. SDA1_RX1: Pass-Through I^2C1 Serial-Data Input/Output or UART1 Receive. Internal 40kΩ pullup to V_{DDIO}. SDA1: I^2C serial data input/ open-drain output. RX1: UART input. Note: Leave pin unconnected when not used.
41	GPIO04	GPIO04* MISO	GPIO04: Configurable General-Purpose Input or Output. GMSL2 power-up default is high impedance with an unconnected input receiver. User must drive pin to ground or V_{DDIO} or enable internal pull-up or pull-down resistor. MISO: SPI Main In Subordinate Out. When configured as the main, input with an internal 1MΩ pulldown to ground that receives data from an external subordinate. When configured as a subordinate, push-pull output that drives data to an external main. Note: Leave pin unconnected when not used.
42	GPIO05	GPIO05* SCLK SCL1_TX1	GPIO05: Configurable General-Purpose Input or Output. GMSL2 power-up default is high impedance with an unconnected input receiver. User must drive pin to ground or V_{DDIO} or enable internal pull-up or pull-down resistor. SCLK: SPI Clock. When configured as the main, push-pull clock output. When configured as a subordinate, clock input with an internal 1MΩ pulldown to ground. SCL1_TX1: Pass-Through I^2C1 Serial-Clock Input/Output or UART1 Transmit. Internal 40kΩ pullup to V_{DDIO}. SCL1: I^2C clock input/ open-drain output. TX1: UART open-drain output. Note: Leave pin unconnected when not used.
27	SDIR	SDIR* GPIO06 SDA2_RX2	SDIR: I^2S/TDM Serial-Data Input with an Internal 1MΩ Pulldown to Ground. Supports reverse audio from deserializer to serializer . GPIO06: Configurable General-Purpose Input or Output. GMSL2 power-up default is high impedance with an unconnected input receiver. User must drive pin to ground or V_{DDIO} or enable internal pull-up or pull-down resistor. SDA2_RX2: Pass-Through I^2C2 Serial-Data Input/Output or UART2 Receive. Internal 40kΩ Pullup to V_{DDIO}. SDA2: I^2C serial data input/open-drain output. RX2: UART input. Note: Leave pin unconnected when not used.

PIN	NAME	FUNCTION MODE SIGNAL NAME	FUNCTION
28	SCKIR	SCKIR* GPIO07	SCKIR: I^2S/TDM Serial-Clock Input with an Internal 1MΩ Pulldown to Ground. Supports reverse audio from the deserializer to the serializer. GPIO07: Configurable General-Purpose Input or Output. GMSL2 power-up default is high impedance with an unconnected input receiver. User must drive pin to ground or V_{DDIO} or enable internal pull-up or pull-down resistor. Note: Leave pin unconnected when not used.
29	WSIR	WSIR* GPIO08 SCL2_TX2	WSIR: I^2S/TDM Serial-Word Select Input with an Internal 1MΩ Pulldown to Ground. Supports reverse audio from the deserializer to the serializer. GPIO08: Configurable General-Purpose Input or Output. GMSL2 power-up default is high impedance with an unconnected input receiver. User must drive pin to ground or V_{DDIO} or enable internal pull-up or pull-down resistor. SCL2_TX2: Pass-Through I^2C2 Serial-Clock Input/Output or UART2 Transmit. Internal 40kΩ pullup to V_{DDIO}. SCL2: I^2C clock input/ open-drain output. TX2: UART open-drain output. Note: Leave pin unconnected when not used.
11	GPIO09/CXTP	CXTP GPO09* BNE SS1	CXTP: Coax/Twisted-Pair Select Input with an Internal 1MΩ Pulldown to Ground. State is latched on power-up. Set CXTP high for Coax cable drive. Set CXTP low for a Twisted-Pair cable. GPO09: Configurable General-Purpose Output BNE: Buffer Not Empty. When configured as subordinate, SPI BNE push-pull output. When BNE is high, indicates SPI data is available. SS1: SPI Subordinate Select 1. When configured as the main, subordinate 1 selects push-pull output.
12	GPIO10	GPIO10* RO SS2	GPIO10: Configurable General-Purpose Input or Output. GMSL2 power-up default is high impedance with an unconnected input receiver. User must drive pin to ground or V_{DDIO} or enable internal pullup or pulldown resistor. RO: When configured as a subordinate, SPI mode-select input with an internal 1MΩ pulldown to ground. When RO is high, enables main read from MISO. When RO is low, enables the main write to MOSI. SS2: SPI Subordinate Select 2. When configured as the main, subordinate 2 selects push-pull output. Note: Leave pin unconnected when not used.

PIN	NAME	FUNCTION MODE SIGNAL NAME	FUNCTION
24	SD/ADD0	ADD0 SD* GPO11	ADD0: Address Selection Input with an Internal 1MΩ Pulldown to Ground. Latched on power-up. SD: I^2S/TDM Serial Data Push-Pull Output. Supports forward-channel audio from the serializer to the deserializer. GPO11: Configurable General-Purpose Output
25	SCK/ADD1	ADD1 SCK* GPO12	ADD1: Address Selection Input with an Internal 1MΩ Pulldown to Ground. Latched on power-up. SCK: I^2S/TDM Serial Clock Push-Pull Output. Supports forward-channel audio from the serializer to the deserializer. GPO12: Configurable General-Purpose Output
26	WS/ADD2	ADD2 WS* GPO13	ADD2: Address Selection Input with an Internal 1MΩ Pulldown to Ground. Latched on power-up. WS: I^2S/TDM Word Select Push-Pull Output. Supports forward-channel audio from the serializer to the deserializer. GPO13: Configurable General-Purpose Output
8	SDA_RX	SDA_RX* GPIO14	SDA_RX: I^2C Serial-Data Input/Output or UART Receive. Internal 40kΩ pullup to V_{DDIO}. SDA: I^2C serial data input/open-drain output. RX: UART input. GPIO14: Configurable General-Purpose Input or Open-Drain Output. Function available only if the MAX96752 is programmed over the GMSL2 link and not locally. Internal 40kΩ pullup to V_{DDIO}.
9	SCL_TX	SCL_TX* GPIO15	SCL_TX: I^2C Serial-Clock Input/Output or UART Transmit. Internal 40kΩ pullup to V_{DDIO}. SCL: I^2C clock input/open-drain output. TX: UART open-drain output. GPIO15: Configurable General-Purpose Input or Open-Drain Output. Function available only if the MAX96752 is programmed over the GMSL2 link and not locally. Internal 40kΩ pullup to V_{DDIO}.
13	LOCK	LOCK	Open-Drain Lock Indication Output with an Internal 40kΩ Pullup to V_{DDIO}.
14	ERRB	ERRB	Open-Drain Error Indication Output with an Internal 40kΩ Pullup to V_{DDIO}. When ERRB is low, this indicates a data error or interrupt is detected. ERRB is high when PWDNB is low.
23	PWDNB	PWDNB	Active-Low, Power-Down Input with an Internal 1MΩ Pulldown to Ground. Set PWDNB low to enter Power-down mode.
MISCELLANEOUS—SEE Table 3			
15	X1/OSC	X1/OSC	Crystal/Oscillator Input. Connect to either a 25MHz crystal or 25MHz external clock source.
16	X2	X2	Crystal Input. Connect to one terminal of a 25MHz crystal and connect a load capacitor from X1/OSC to ground (load capacitor value depends on crystal used).
18	XRES	XRES	Used to calibrate SIO output driver swings. Connect an external 402Ω ±1% resistor between XRES and ground.
7, 17	RSVD	RSVD	Reserved. Make no electrical connection to this pin.

PIN	NAME	FUNCTION MODE SIGNAL NAME	FUNCTION
POWER SUPPLIES—SEE Table 3			
1	V_{REG}	V_{REG}	Internal 1.0V Digital Regulator Supply. If using the regulator, connect a 1.8V ±5% supply. If not using the regulator, make no connection.
56	V_{DDD}	V_{DDD}	Core Digital 1V Supply. If using the V_{REG} regulator, do not apply any voltage to this pin. If not using the regulator, connect a 1.0V ±5% supply.
2	V_{REGA}	V_{REGA}	Internal 1.0V Analog Regulator Supply. If using the regulator, connect a 1.8V ±5% supply. If not using the regulator, make no connection.
10	V_{DDA}	V_{DDA}	Core Analog 1V Supply. If using the V_{REGA} regulator, do not apply any voltage to this pin. If not using the regulator, connect a 1.0V ±5% supply.
44	V_{DDIO}	V_{DDIO}	1.8V to 3.3V I/O Supply
5, 6, 20, 43	V_{DD18}	V_{DD18}	1.8V ±5% I/O Supply
—	EP	EP	Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Recommended Operating Conditions, External Component Requirements, and ESD Protection

Table 2. Recommended Operating Conditions

PARAMETER	PIN NAME	NOMINAL VOLTAGE (V)	MIN	TYP	MAX	UNIT
Supply Range	V_{DD18}		1.7	1.8	1.9	V
	V_{DDIO}	1.8	1.7	1.8	1.9	V
		3.3	3.0	3.3	3.6	V
	V_{DDD}, V_{DDA} (if driven externally)		0.95	1.0	1.05	V
	V_{REG}, V_{REGA} (if regulators used)		1.7	1.8	1.9	V
Maximum Supply Noise	V_{DD18}			25		mV_{P-P}
	V_{DDIO}	1.8		50		mV_{P-P}
		3.3		100		mV_{P-P}
	V_{DDD}, V_{DDA}			25		mV_{P-P}
	V_{REG}, V_{REGA} (if regulators used)			25		mV_{P-P}
Operating Junction Temperature, T_J			-40		+125	°C

Note: *Supply noise < 1MHz.*

See Figure 15 and Figure 16.

Table 3. External Component Requirements

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
XRES	R_{XRES}		402 ±1%. Use a single resistor.	Ω
Line-Fault Pulldown Resistor	R_{PD}	If line fault is used by the serializer. See Figure 15 and Figure 16	49.9 ±1%	kΩ
Link Isolation Capacitors	C_{LINK}	Place close to the SIO pins (21, 22, 4, 3) used in the application.	0.1	µF
Termination Resistors for Unused GMSL2 Inputs in Coax Mode	R_{TERM}	Place close to the Link Isolation Capacitor(s) for the unused SIO input(s) in Coax mode. See Figure 15	49.9 ±1%	Ω
Crystal		Place as close as possible to X1/OSC (pin 15) and X2 (pin 16).	25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values which compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible X1/OSC (pin 15) and X2 (pin 16).	Application specific	
V_{DDIO} Decoupling Capacitors*		Place a 0.01µF capacitor as close as possible to V_{DDIO} (pin 44). Include a minimum of 10µF bulk decoupling on the PCB.	0.01 + 10	µF
V_{DD18} Decoupling Capacitors*		Place a 0.01µF capacitor as close as possible to V_{DD18}. Place another 0.01µF capacitor as close as possible to V_{DD18} (pins 5 and 6) and run separate traces from each pin to the capacitor. Include a minimum of 10µF bulk decoupling on the PCB.	(3x) 0.01 + 10	µF

Table 3. External Component Requirements (continued)

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
V_{DDD}, V_{DDA} Decoupling Capacitors*		Place 0.1µF capacitors as close as possible to V_{DDA} (pin 10) and V_{DDD} (pin 56). If driving with a 1V supply, include a minimum of 10µF bulk decoupling on the PCB. If using the internal 1V regulators, also include 10µF bulk decoupling capacitors for V_{DDD} and V_{DDA}. See the configuration information in the *Power Supplies* section.	(2x) 0.1 + 10 or (2x) 0.1 + (2x) 10	µF
V_{REG}, V_{REGA} Decoupling Capacitors*		If using the internal regulators for V_{DDD} and V_{DDA}, place a 0.1uF capacitor as close as possible to V_{REG} (pin 1) and V_{REGA} (pin 2). If sharing the V_{DD18} supply for V_{REG} and V_{REGA}, no bulk decoupling capacitance is required. If not using the internal 1V regulators, make no connection to these pins. See the configuration information in the *Power Supplies* section.	(2x) 0.1 if using internal regulator	µF
Open-Drain Pullup Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations.	Application specific	

* Power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

Table 4. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIO_	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±8		kV
		ISO 10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, Coax Configuration		±6		
		ISO 10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, STP Configuration		±4		
		ISO 10605, R_D = 330Ω, C_S = 150pF, Air Discharge		±8		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Functional Diagrams

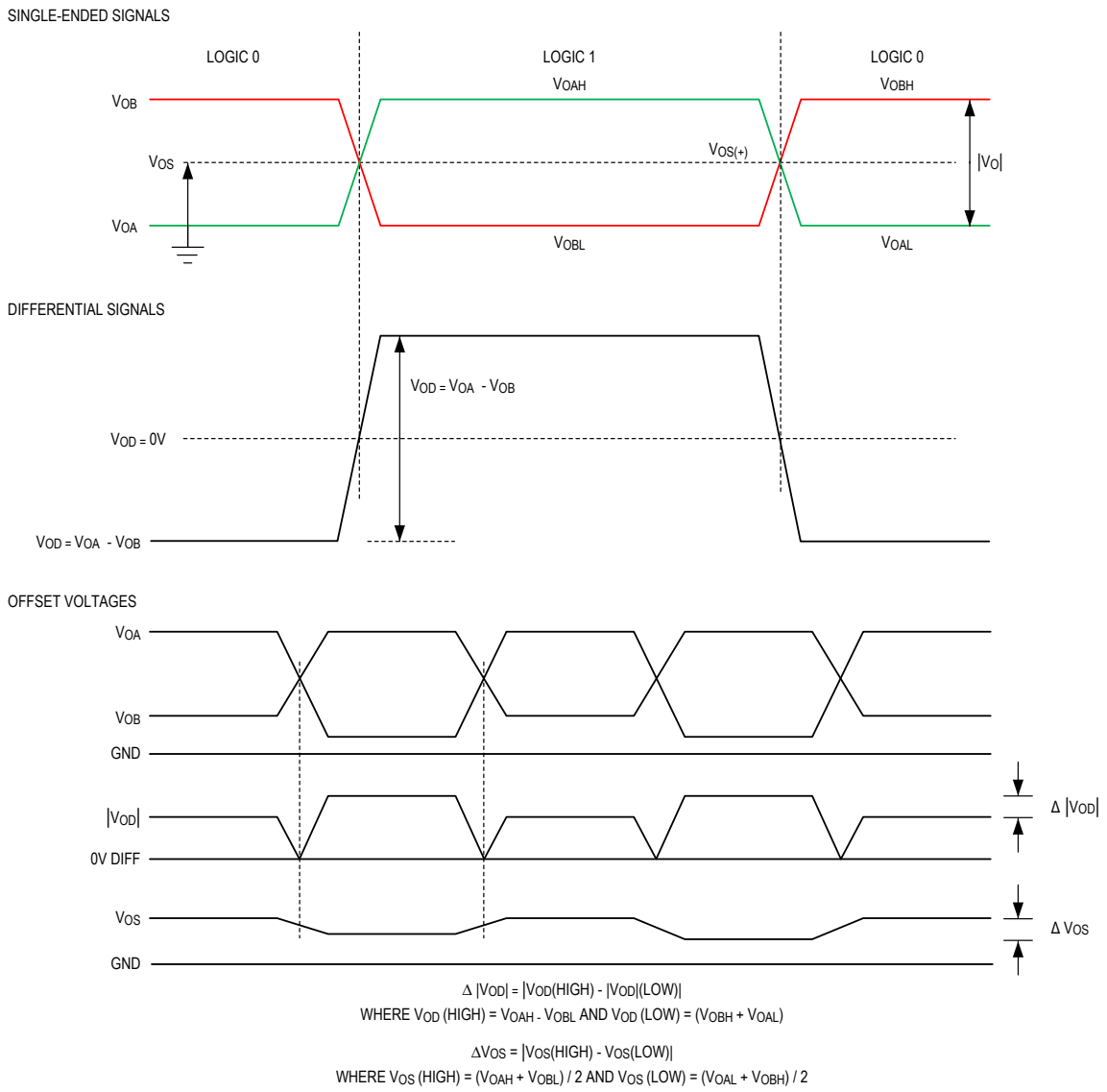


Figure 1. Serial Output Parameters

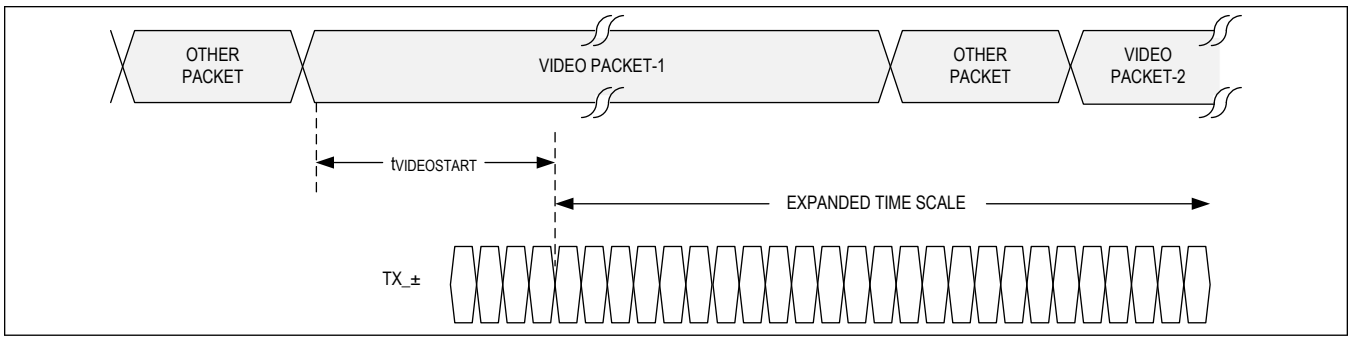


Figure 2. Video Initialization Time

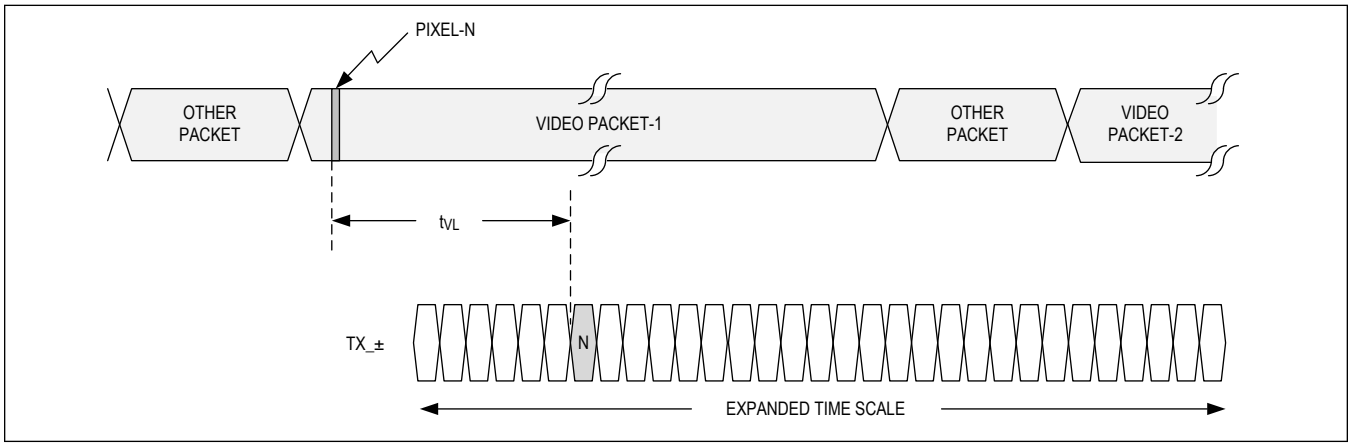


Figure 3. Video Latency

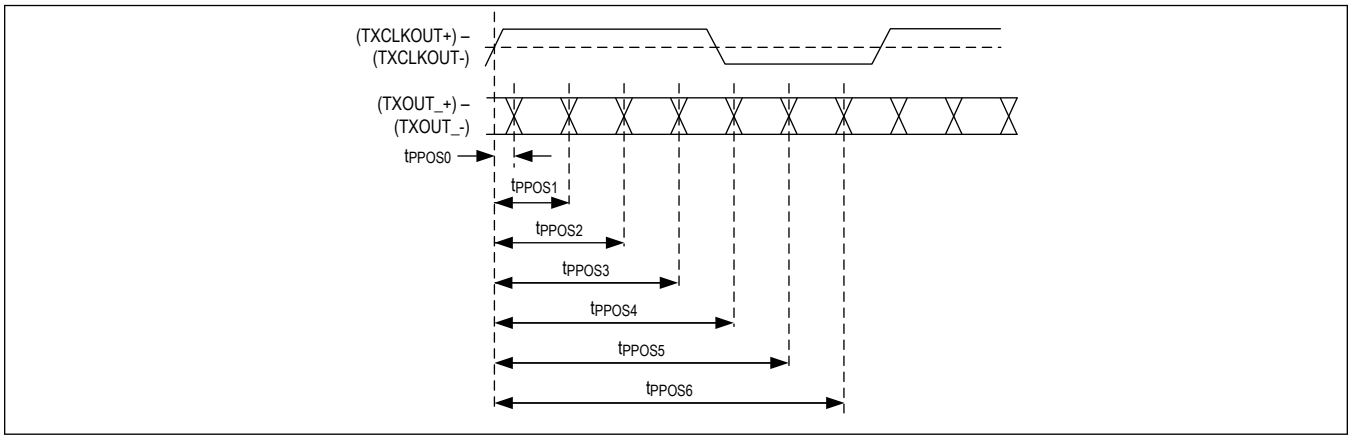


Figure 4. LVDS Output Pulse Positions

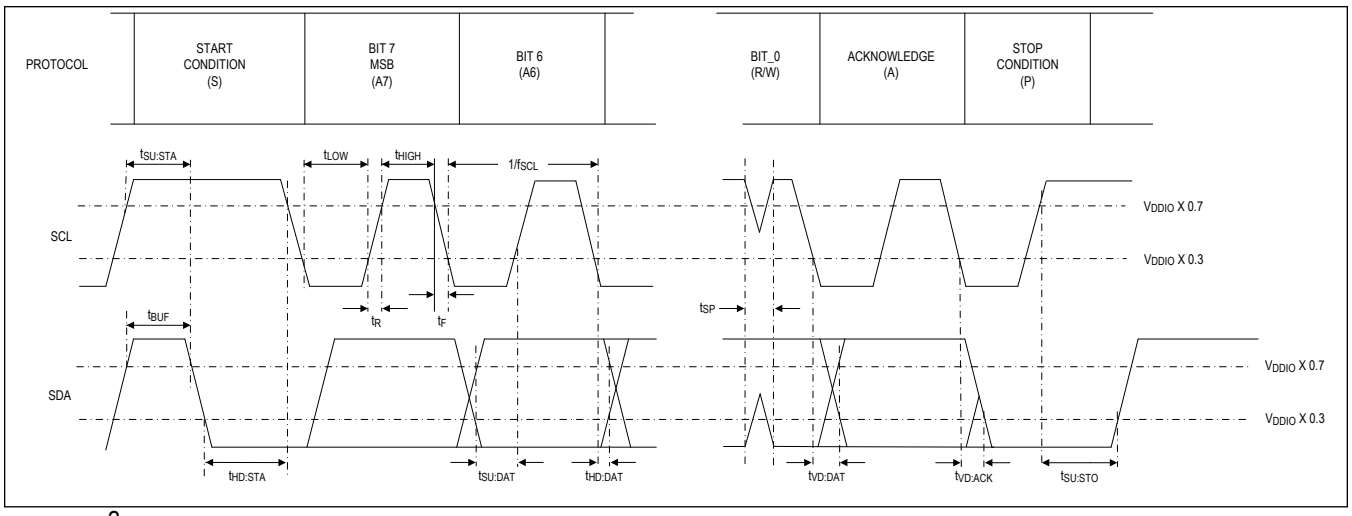


Figure 5. I²C Timing Parameters

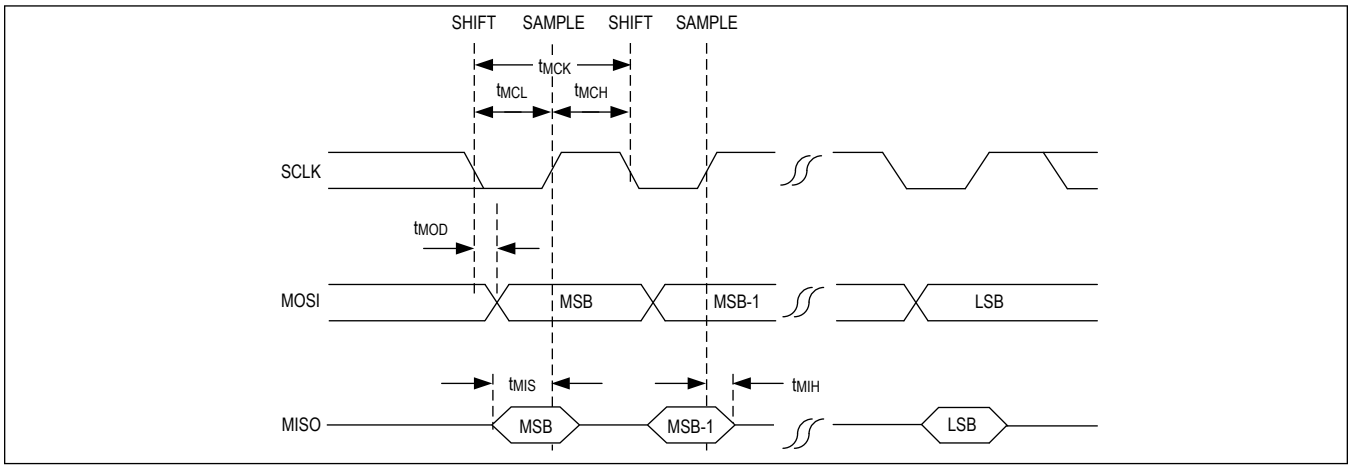


Figure 6. SPI Main Mode Timing Parameters

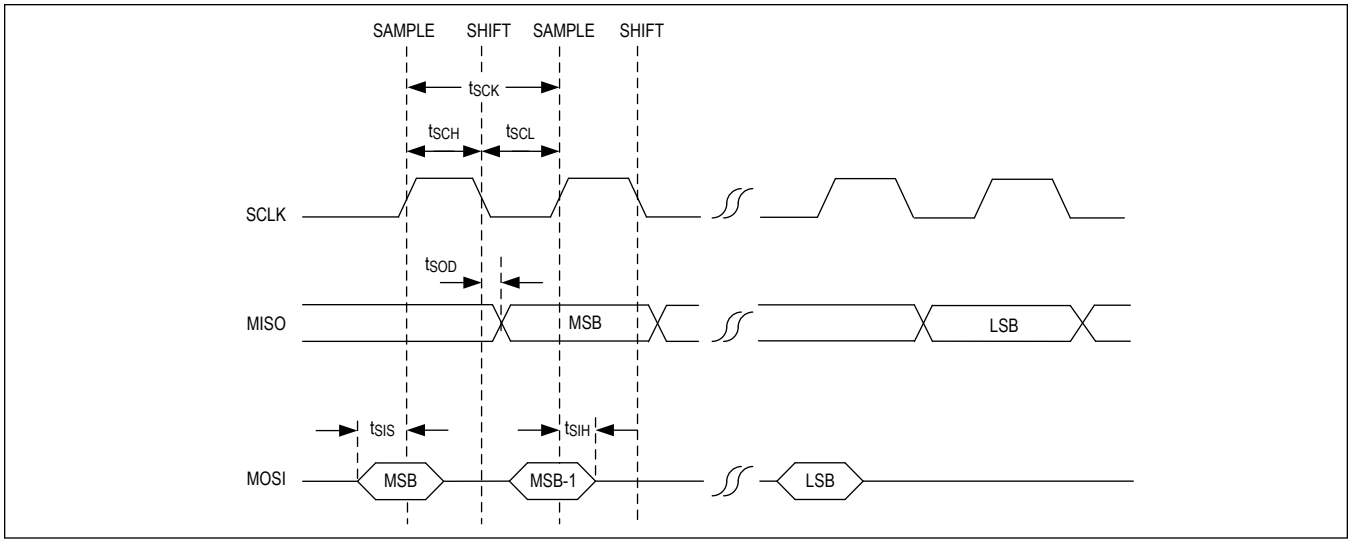


Figure 7. SPI Subordinate Mode Timing Parameters

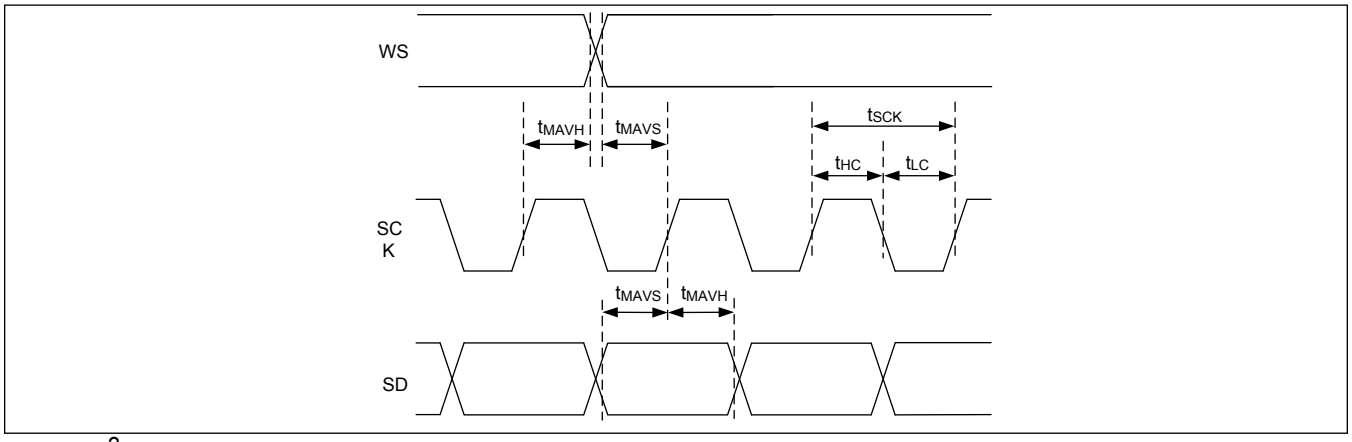


Figure 8. I²S Main Timing Diagram

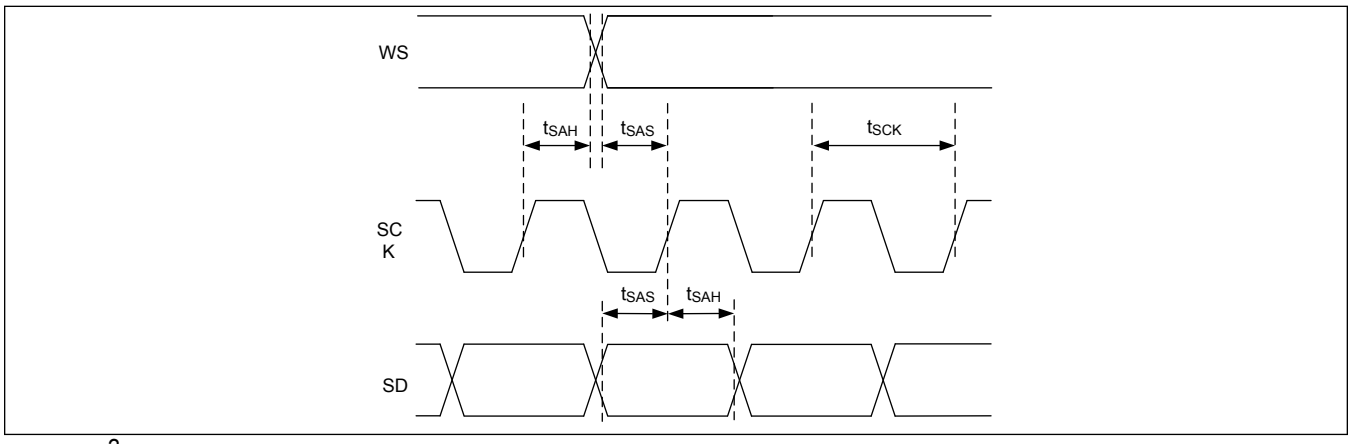


Figure 9. I²S Subordinate Timing Diagram

Detailed Description

Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews and register definitions. Designers must also have the following information to correctly design using this device:

- The **GMSL2 Channel Specification** contains physical layer requirements for the PCB traces, cables, and connectors that constitute the GMSL2 link.
- The **GMSL2 Hardware Design Guide** contains recommendations for PCB design, applications circuits, selection of external components, and guidelines for use of GMSL2 signal integrity tools.
- The **GMSL2 User Guide** contains detailed programming guidelines for GMSL2 device features.
- The **MAX96752 User Guide** contains detailed programming guidelines for MAX96752 device features.
- **Errata sheets** contain deviations from published device specifications and are specific to part number and revision ID.

Contact the factory for these documents and for additional guidance on the MAX96752 features.

Introduction

Analog Devices' GMSL2 serializers and deserializers provide sophisticated link management for high-speed, low bit-error-rate, serial data transport. They support a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL2 provides up to 6Gbps forward and 187.5Mbps reverse packetized data transmission over each fixed-speed link. Devices with two GMSL2 links provide a total capacity of 12Gbps and 375Mbps reverse in specific configurations.

The following sections provide a brief overview of the device functions and features. Contact the factory for additional information and details on the configuration of each function and feature.

Product Overview

The MAX96752 converts a single video stream received on a single- or dual-link GMSL2 input to an LVDS (OLDI) output for driving display panels. Video data is mapped to OLDI output ports A, B, or both. The output can drive with OLDI or VESA® formats.

For more information about the OLDI standard, refer to the Open LVDS Display Interface (OLDI) Specification.

OLDI Pixel Clock and Pixel Interleaving

The OLDI clock output is generated by the deserializer based on the tracked and measured clock frequency of its video input. When using a single output port, the maximum OLDI PCLK of 150MHz supports up to full high-definition (FHD) (1920x1080, 24-bit/60Hz) or equivalent.

In dual OLDI mode, the interleaved even and odd pixels of the video stream are each routed to the A and B output ports, which are connected to a single display. This divides the video PCLK by a factor of 2 at the OLDI ports. FHD can thus be displayed with approximately 75MHz clocking on each port, keeping the PCLK below the FM radio band.

In dual OLDI mode, the MAX96752 support up to a 300MHz PCLK if both GMSL2 link inputs are used. This enables display of interleaved WQXGA (2560x1600, 24-bit/60Hz) or equivalent video. If only one GMSL link is used, the maximum PCLK is limited to approximately 217MHz by the 6Gbps link bandwidth. This enables display of 2560x1080, 24-bit/60Hz, or equivalent video.

Deserializer replication supports identical FHD, or equivalent, video to be sent to 2 displays.

Dual-view splitter mode supports 2 side-by-side FHD displays with different content split from a single video stream.

The MAX96752 provides flexible output configuration, a color lookup table for gamma correction, and programmable spread-spectrum clocking. Pixel mapping to the A and B ports can be swapped.

Deserializer Modes

The MAX96752 has a single video pipeline. Each device can support single video streams, video replication, and dual-view splitting to enable a single deserializer to support multiple system configurations as illustrated in Figure 10–Figure 14. All use cases are shown with a high-definition multimedia interface (HDMI) serializer, but these configurations are

supported with other video interfaces as well.

Single Video Stream, Single GMSL2 Link

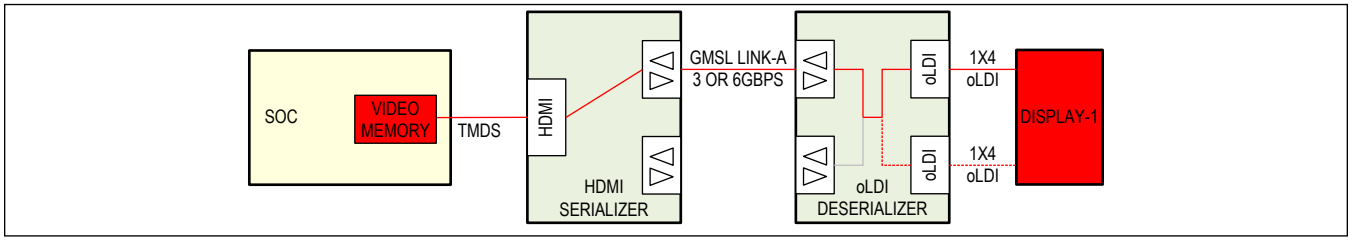


Figure 10. Single Video Stream, Single GMSL2 Link at Either 3Gbps or 6Gbps, MAX96752 Deserializer with Single or Dual OLDI Outputs

Single Video Stream, Dual GMSL2 Links

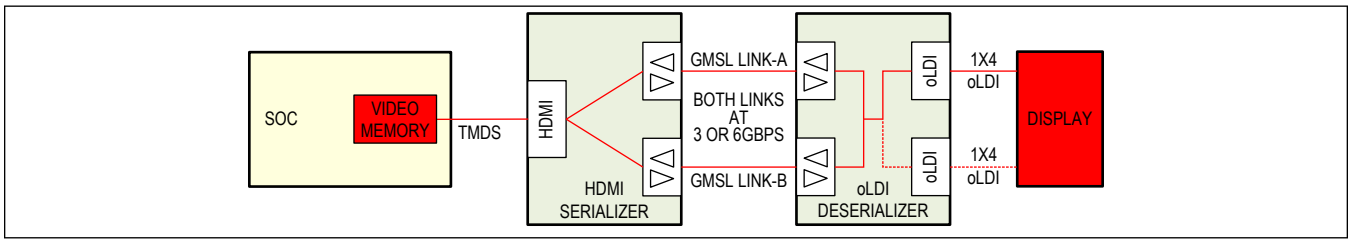


Figure 11. Single Video Stream, Dual GMSL2 Links with Both at Either 3Gbps or 6Gbps, MAX96752 Deserializer with Single or Dual OLDI Outputs

Single Video Stream with Serializer Replication

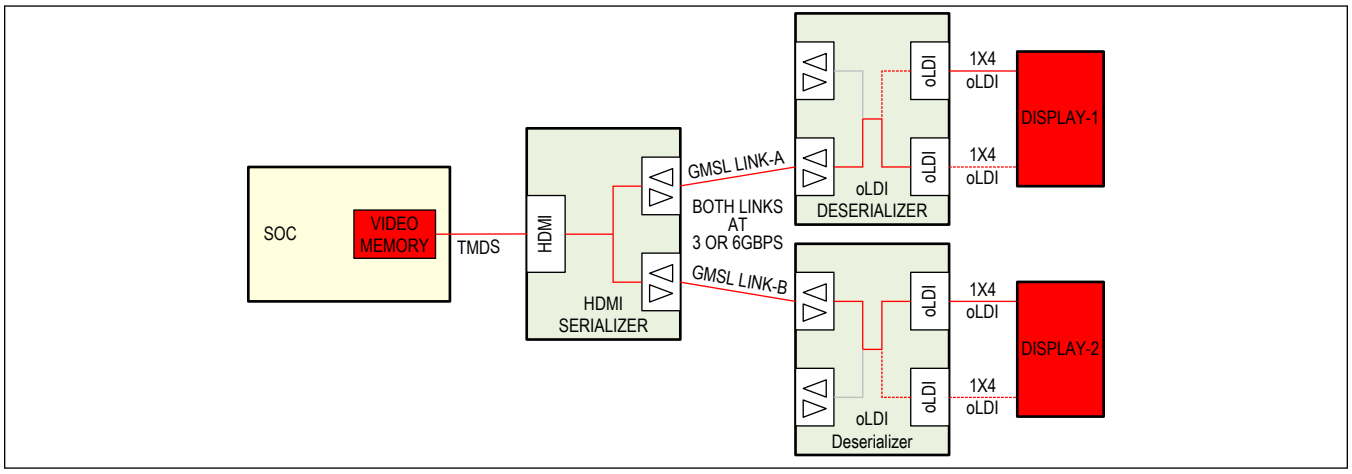


Figure 12. Serializer Replication, Dual GMSL2 Links, OLDI Deserializers with Single or Dual OLDI Outputs

Single Video Stream with OLDI Deserializer Replication

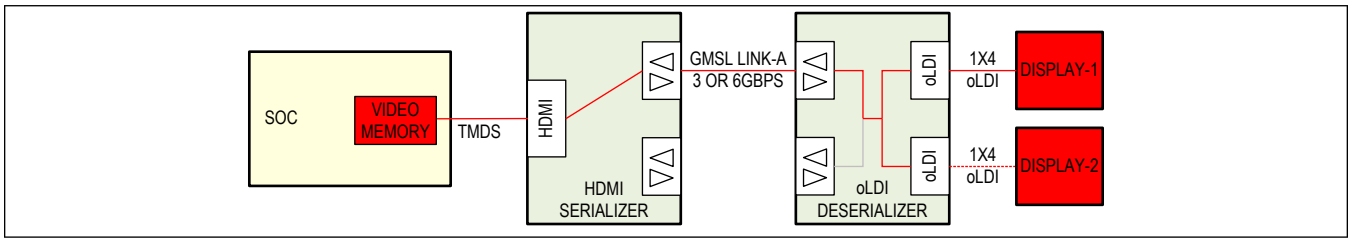


Figure 13. Single Stream OLDI Deserializer, Identical Video on Both Displays

Serializer Dual-View Mode with OLDI Deserializer Splitter Mode

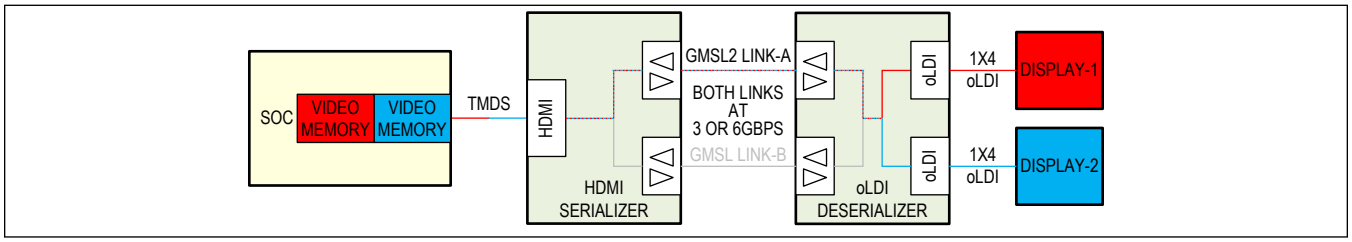


Figure 14. Serializer Dual-View Splitter Mode, Convert Dual-View to Pixel Interleave, Send Dual-Views Down Single GMSL2 Link, Dual OLDI Deserializer Splits Pixel Interleaved Dual-View, Each Video Stream (View) Must Have Identical Timing, Can Also Be Done in Dual GMSL2 Link Mode

Other Functions

GMSL2 serializers and deserializers have a primary I^2C/UART control channel interface that an ECU uses to access serializer and deserializer registers, as well as peripheral devices, from either end of the link. Each device also has two pass-through I^2C/UART channels available for local or remote peripheral control. The pass-through I^2C/UART channels do not have access to serializer and deserializer registers.

The MAX96752 supports both forward (serializer to deserializer) and reverse (deserializer to serializer) audio channels. The audio channels support I^2S stereo and up to 8 channels in Time-Division Multiplexing (TDM) mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 bits to 32 bits.

The MAX96752 additionally include an SPI main/subordinate, including two subordinate select pins, for peripheral control. The SPI enables a host SPI main on one side of the GMSL2 link to control a peripheral SPI subordinate on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL2 devices (a GMSL2 device can be configured as an SPI main or subordinate).

The MAX96752 provide up to 15 GPIOs, dependent on device feature utilization. GPIOs are typically used to tunnel low speed (< 100kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward or reverse direction.

The devices include a video crossbar and watermark generation or detection. The crossbar can be used to reorder the color and sync signals. The watermark generation and detection is used to verify the video image is not frozen.

GMSL2 devices incorporate numerous link margin optimization and monitoring functions to ensure high link margin. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor (EOM) function for continuous link margin diagnosis with various threshold alarm levels is available for runtime alerts of link degradation. PRBS checking verifies correct link and video channel operation.

GMSL2 Protocol

GMSL2 is a fixed-rate transmission medium designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or external reference frequency. The link clock does not have any relation to the video pixel clock.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a

flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth.

The same data protocol is used on forward and reverse channels and for both video and control-channel data.

GMSL2 Physical Layer

Analog Devices' GMSL2 family of serial links have transmitter and receiver capability enabled simultaneously, allowing full-duplex operation on a single wire. A single cable between the serializer and deserializer delivers data being transmitted from each end of the link. Forward transmission is data being sent from the serializer to the deserializer. Reverse transmission is data being sent from the deserializer to the serializer.

Forward rate options are fixed at 3Gbps or 6Gbps, with defaults of 6Gbps in Coax mode and 3Gbps in STP mode. The reverse rate is fixed at 187.5Mbps.

Both forward and reverse rates are doubled in dual-link configuration, in which a serializer and paired deserializer are connected using two links. Dual-link mode is not available in all GMSL2 device configurations.

Cabling Options

GMSL2 supports operation with either 50Ω Coaxial or 100Ω Shielded-Twisted Pair (STP) cabling.

Coax or STP operation is determined by the state of CXTP at power-up. Set CXTP high for Coax cable drive (single-ended with default 6Gbps link rate). Set CXTP low for STP mode (differential with default 3Gbps link rate). See the *Latch-On-Power-Up Pins* section.

In Coax mode, use only the noninverted SIO pin. AC-couple and terminate the inverting SIO pin using the series connection of a 100nF capacitor and a 49.9Ω resistor. In STP configurations, both the noninverted and inverted SIO pins are enabled by default.

Cable attenuation and return loss characteristics must stay within the requirements of the GMSL2 channel specification to achieve robust full-duplex link performance. These requirements vary with selected link rate. The available link rates and GMSL2 adaptive equalization enable support of a wide range of cabling options.

Maximum cable length is limited by the frequency-dependent attenuation of the cable. Additionally, PCB and in-line connectors degrade the return loss characteristic of the cable assembly. The GMSL2 channel specification allows two inline connectors and provides detailed requirements for cable attenuation and return loss, as well as insertion loss and return loss requirements for PCB traces. In general, any physical channel implementation compliant with the GMSL2 channel specification can be used with reliable results. Contact the factory for the GMSL2 channel specification document.

A 100nF AC-coupling capacitor is normally used for GMSL2 links.

See Figure 15 and Figure 16 for typical GMSL2 serial link configurations.

Line Fault

GMSL2 serializers include a novel line-fault detection circuit. It detects and reports open-circuit, short-to-battery, short-to-ground, and line-to-line short. The line-fault monitor requires external resistors R_{EXT} and R_{PD} connected to the LMN pins as shown in Figure 15 and Figure 16.

The line-fault monitor is enabled by default, and configuration options are available through registers. Its status can be read by register. If unmasked, a line fault condition asserts ERRB. Line fault detection cannot be used in conjunction with power over coax (POC).

The line-fault monitor pins offer flexible connection and programming. On parts with multiple GMSL2 links, either pair (i.e., LMN1A/LMN0A) can be used with either link (i.e., SIOA+/SIOA-). In addition, the pins within each pair can be assigned to either polarity of the link.

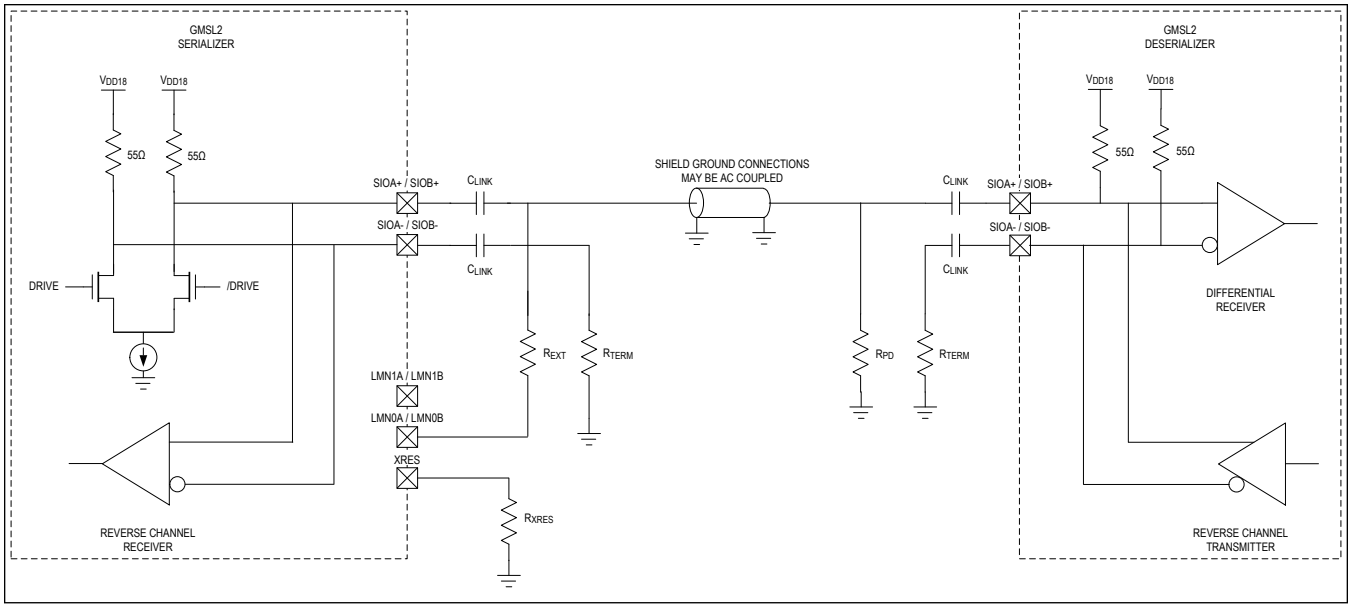


Figure 15. Typical GMSL2 Link Application Circuit for Coax Cable

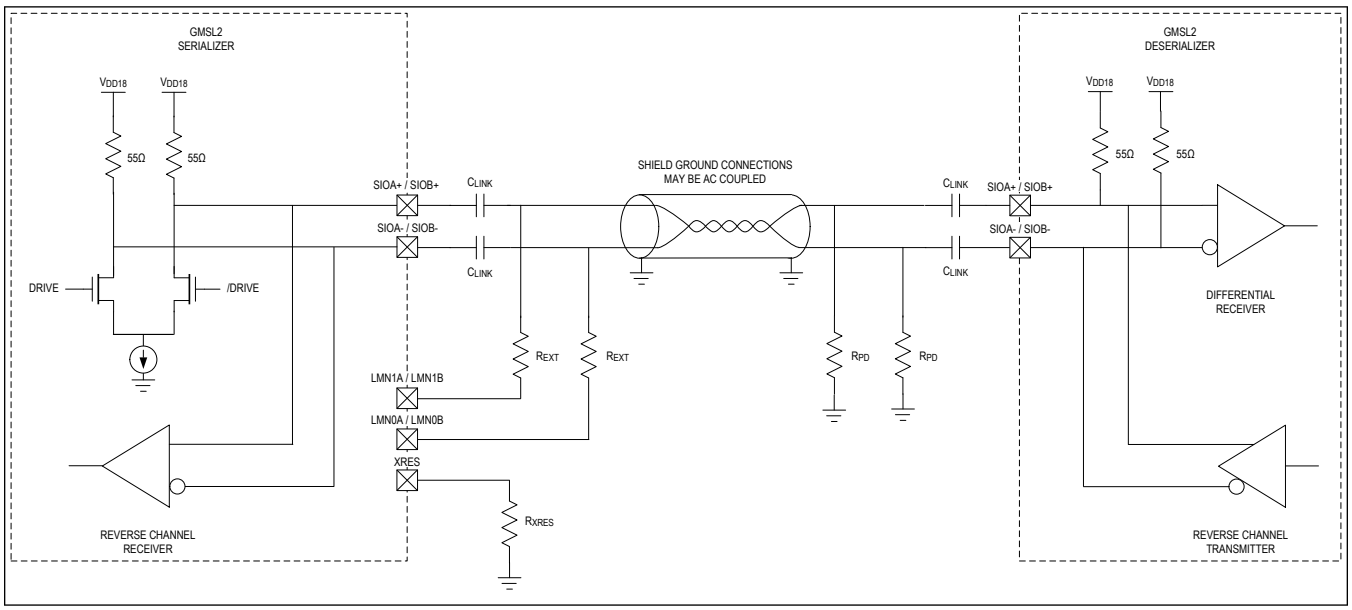


Figure 16. Typical GMSL2 Link Application Circuit for Twisted Pair

Line Fault in AC-Coupled Ground Applications

Use of the line fault function is NOT recommended in applications with a floating cable shield. Contact the factory for details.

GMSL2 Bandwidth Sharing

The GMSL forward bandwidth is shared between video, the I^2C/UART control channel, pass-through I^2C/UARTs, I^2S/TDM audio, SPI, and GPIOs, plus various protocol-specific data exchanges (i.e., info frames, sync, and acknowledgments). The reverse channel bandwidth is also shared with all the above, with the exception of video packets.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

Link bandwidth is shared flexibly between the various communication channels requesting the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation; if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol fulfills this sharing requirement. The maximum packet size is limited to prevent one single channel from monopolizing the link bandwidth and to ensure other channels are served.

The video and control channel packets can be assigned a priority level. There are four priority levels: low, normal, high, and urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with maximum latency requirements can be assigned an increased priority.

GMSL2 Bandwidth Calculations

The GMSL2 forward link has a fixed link rate of 3Gbps or 6Gbps. The reverse link rate is fixed at 187.5Mbps. The GMSL2 protocol overhead is roughly 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

Ensure the worst-use cases do not exceed the available throughput of the forward and reverse links. Analog Devices' evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator for initial bandwidth requirements estimates. Analog Devices also has other tools to calculate link bandwidth utilization. Consult the factory for high bandwidth use cases to ensure error-free performance.

Table 5 provides estimates of the bandwidth utilization for each communication channel.

Table 5. Forward and Reverse Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Display Video (Forward Path Only)	PCLK x (bpp + 0.5 + packet_CRC) x 10/9 x 2048/2047
I^2C	13 to 40 x I^2C clock rate
UART	6 x UART bit rate
SPI	1.7 to 3.1 x SPI rate, depending on SPI byte length
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation
I^2S/TDM	BW = sample_rate x 20 x (roundup (channelcnt x sample_depth/18 + 0.5) + 2)

Definitions:

PCLK = Total horizontal pixels x total vertical lines x frame rate. Total horizontal includes blanking pixels, and total vertical includes blanking lines.

bpp = Bits per pixel (typically 24)

packet_CRC = 0.5 when packet CRC is enabled, = 0 when packet CRC is disabled. Packet CRC is disabled by default.

sample_rate = Audio sample rate (samples per second)

sample_depth = Bits per sample per audio channel (must be the same for all channels)

channelcnt = Number of audio channels

Power Supplies

The MAX96752 provides flexible power supply configurations.

The V_{DDIO} supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing with the part. V_{DD18} is the primary analog supply and is fixed at 1.8V.

For best power efficiency, provide a 1.0V supply to both analog V_{DDA} and digital V_{DDD} pins. Make no connection to the V_{REGA} or V_{REG} pins.

Alternatively, the MAX96752 provides the capability of internally regulating 1.8V down to 1V for the V_{DDD} and V_{DDA} supplies. This eliminates the need to provide a separate 1.0V supply. Connect the 1.8V V_{DD18} supply to V_{REG} and V_{REGA}. Do not connect an external voltage to the V_{DDA} or V_{DDD} pins.

Internal logic senses the voltage at V_{REG} and appropriately enables or disables the two regulators. If 1.7V < V_{REG} < 1.9V, the regulators are enabled; otherwise, they are disabled. The V_{REG} and V_{REGA} regulators cannot be used independently.

Power supply ramp-time recommendation: 20µs < ramp time < 2ms. Power supply ramps should be monotonic. Once the supply voltage reaches the minimum supply voltage limit, it should not be allowed to drop below the specification.

Proper power supply bypassing of all supplies is essential for high-frequency circuit stability. See Table 3. See Table 2 for power supply tolerances and noise requirements. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

Analog Devices provides power management ICs (PMICs) optimized for supporting serial link devices. Contact the factory for information.

Thermal Management

Power consumption of GMSL2 devices varies based on their use case. Use care to provide sufficient heat dissipation with proper board and cooling design techniques. The package's exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below +125°C to meet electrical specifications and avoid impacting device reliability.

For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Control Channel and Side Channels

A microcontroller (µC) or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. All GMSL2 devices support the following interfaces:

- Primary I^2C/UART (internal access)
- Pass-through I^2C/UART
- SPI
- GPIO

Some GMSL2 devices also support I^2S/TDM audio. Data from all of these interfaces tunnel through the GMSL2 link, but the GMSL2 device registers can be accessed and configured only through the primary I^2C/UART interface.

The side channel, with its various interfaces, is accessed through multifunction GPIO pins (MFPs on some devices). Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit in the number of pins available on a given device, not all interfaces can be simultaneously supported. See Table 8 and the *Pin Descriptions* section for default and alternate multifunction pin functions, as well as available combinations of interfaces.

Primary I^2C/UART

The primary I^2C/UART is located on the SDA_RX and SCL_TX pins of each GMSL2 device. The I^2C (SDA, SCL) or UART (Tx, Rx) interface is selected by the I2CSEL configuration pin state at power-up (See the *Latch-On Power-Up Pins* section). The selected interface provides main access to GMSL2 registers, as well as peripheral device registers, from either end of the link.

The main µC can be located on either end of the link (usually the serializer side for display applications and the deserializer side for camera applications). Dual main microcontrollers are supported, wherein DIS_REM_CC settings in register REG2 for each link can disable the remote control channel communications on that link. Optionally, software arbitration, such as token passing, can be used to prevent packet collisions.

To configure peripheral devices over the link, the GMSL2 serializer and deserializer must use the same control channel interface (both I^2C or both UART). Unlike GMSL1 devices, there is no I^2C-to-UART conversion capability. I^2C/UART outputs are open-drain and require appropriately-sized external pull-up resistors for proper operation.

For detailed primary channel programming information, see the Control-Channel Programming section under *Applications Information*.

Pass-Through I²C/UART

GMSL2 devices have two pass-through I²C/UART channels. These channels do not have access to registers in either the GMSL2 serializer or deserializer; they simply tunnel the I²C or UART signal across the GMSL2 link. This can be useful for separating I²C channels so that multi-main conflicts do not occur. I²C/UART outputs are open-drain and require appropriately-sized external pull-up resistors for proper operation.

Serial Peripheral Interface (SPI)

GMSL2 enables a host SPI main on one side of the GMSL2 link to control a peripheral SPI subordinate on the opposite side. Communication can be in either direction across the GMSL2 link. Although multiple SPI peripherals may be connected, only one must be communicated with at a time. Contact the factory for guidance on configuring SPI connections.

The SPI clock range is 600kHz to 25MHz. Exercise care to meet setup and hold time requirements when using at speeds higher than 20MHz.

I²S/TDM Audio

GMSL2 devices for display applications support I²S stereo and up to 8 channels of audio in TDM mode. In GMSL2 mode, most devices have two audio channels, one each in the forward and reverse directions. Sample rates of 8kHz to 192kHz and sample depths of 8-bits to 32-bits are supported. In GMSL2 mode, the maximum SCK frequency is 49.152MHz. For system flexibility, GMSL2 devices can act as either the subordinate or main at either end of the link.

Control Channel Latencies

Table 6. Typical Control Channel Latencies

FUNCTION	FORWARD	REVERSE	NOTES
I²C	< 10µs	< 10µs	
UART	< 10µs	< 10µs	
Audio	< 100µs	< 100µs	For typical use cases
SPI	< 10µs	< 10µs	Round trip

General-Purpose Inputs and Outputs (GPIO)

GPIOs are typically used to tunnel low speed (< 100kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based; a GPIO packet is created and transmitted on the GMSL2 link when a rising or falling edge transition is detected at a GPI pin. The transition is regenerated at a GPO on the other end of the link.

The multifunction pins GPIO can be programmed as GPI (input), GPO (push-pull output or open-drain output), or GPIO (bidirectional input/output). Each GPIO can also be programmed for 1MΩ or 40kΩ pull-up or pull-down (or none). Although an internal pull-up is provided, high-speed open-drain outputs require an appropriate value external pull-up resistor to V_{DDIO}. Inputs cannot be left unconnected. Always ensure that every pin configured as an input has a pull-up or pull-down programmed or is driven by another IC.

A GPI on one side of the serial link can be mapped to a single GPO or multiple GPOs on the other side of the link. Each GPI is assigned a pin ID with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0–GPIO0, GPIO1–GPIO1, GPIO2–GPIO2, etc. However, GPIO mapping can be arbitrarily changed through register settings. GPI transitions can be transmitted in two modes: Delay-compensated and Non-delay-compensated. When delay compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases, but jitter and skew decrease.

The state of each GPIO can be read or written by register either locally or remotely over the GMSL2 link by a µC using the control channel I²C/UART interface.

In Non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible based on available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Non-delay-compensated mode should be used with signals tolerant to delay variation (i.e., µC interrupts).

GPI transitions are transmitted in the order they occur.

Typical GMSL2-only device delays for 6Gbps forward and 187Mbps reverse link rates are shown in Table 7.

Table 7. Typical GPIO Delays for Forward and Reverse Link Transmission

	DELAY COMPENSATION	DELAY
GPIO forwarding from serializer to deserializer (6Gbps forward channel)	0	720ns
	1	3.5µs
GPIO forwarding from deserializer to serializer (187Mbps reverse channel)	0	6µs
	1	15µs

Multifunction Pin Assignments

Multiple functions are assigned to each multifunction pin. They cannot be used simultaneously. Some functions require only a single MFP, but most are implemented across a group of MFPs. For example, WMD is a single MFP, but SPI takes several MFPs. A user selects MFP functions to suit the use case by programming the appropriate registers.

The pin description indicates the function modes for each multifunction pin, listed in order of priority. Higher priority modes must be turned off when lower-priority modes are enabled, both through register writes. Table 8 indicates how latch-on power-up, I^2C/UART, audio, SPI, and other functions are mapped to the multifunction pins.

Pins are grouped by speed settings with different output rise and fall times to facilitate optimizing for different speed requirements of the different functions. Pins labeled A and B are pin speed groups. They can have their speeds changed as a group by register settings (i.e., the speed of the entire group B (GPIO[2:13]) is changed in unison for all grouped pins and for all functions on these pins, with the exception of I^2C/UART). Each group can be programmed to one of four speeds. See Table 9 for typical rise and fall times for the speed settings.

The primary channel I^2C always uses I^2C speed setting. Enabling the pass-through I^2C1 or pass-through I^2C2 in group B sets these pins (two each) to the I^2C speed independent of the B pin speed group setting.

Table 8. GPIO Pin Function Map

PIN	LATCH ON POWER-UP	I^2C/UART	AUDIO	SPI	OTHER FUNCTIONS	GPIO	SPEED GROUP	DEFAULT SPEED
GPIO01	I2CSEL				VS	GPIO01	A	11
GPIO02		MS			WMD	GPIO02	B	10
GPIO03		Pass-through 1 SDA/RX		MOSI		GPIO03	B/I^2C	10
GPIO04				MISO		GPIO04	B	10
GPIO05		Pass-through 1 SCL/TX		SCLK		GPIO05	B/I^2C	10
GPIO06		Pass-through 2 SDA/RX	Rev Path SD			GPIO06	B/I^2C	10
GPIO07			Rev Path SCK			GPIO07	B	10
GPIO08		Pass-through 2 SCL/TX	Rev Path WS			GPIO08	B/I^2C	10
GPIO09	CXTP			BNE, SS1		GPO09	B	10
GPIO10				RO, SS2		GPIO10	B	10
GPIO11	ADD0		Fwd Path SD			GPO11	B	10
GPIO12	ADD1		Fwd Path SCK			GPO12	B	10
GPIO13	ADD2		Fwd Path WS			GPO13	B	10

Table 8. GPIO Pin Function Map (continued)

PIN	LATCH ON POWER-UP	I²C/UART	AUDIO	SPI	OTHER FUNCTIONS	GPIO	SPEED GROUP	DEFAULT SPEED
GPIO14		Primary channel SDA/Rx				GPIO14	I²C	I²C
GPIO15		Primary channel SCL/Tx				GPIO15	I²C	I²C

Table 9. Control- and Side-Channel Typical Rise and Fall Times

PIN OR GPIO SPEED SETTING	RISE TIME*		FALL TIME**	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
ERRB, LOCK	1.0ns	0.6ns	0.8ns	0.5ns
01	2.1ns	1.1ns	2.0ns	1.1ns
10	4.0ns	2.3ns	4.3ns	2.3ns
11	9ns	5ns	10ns	30n
I²C	***	***	40ns	30ns

*20 to 80%, 20pF load. Rise time is for push-pull output configuration.

**80 to 20%, 20pF load.

***Rise time for open-drain outputs depends on external pull-up resistor value.

SPI and I²S Speed Programming

The SPI and I²S interfaces may be used over a wide range of frequencies. The MAX96752 provides flexible GPIO speed programming to maintain timing margins while minimizing radiated electromagnetic interference (EMI).

Table 10 and Table 11 provide guidance on recommended speed settings for various I²S and SPI operating frequencies and V_{DDIO} supply voltages. See Table 9 for GPIO pin speed programming information.

At lower frequencies, SPI data is typically latched on the opposite clock edge on which it is shifted. See Figure 6 and Figure 7. However, at higher frequencies, the data must be latched on the same edge as the shift to meet setup and hold time requirements. Table 11 provides guidance on programming the latching clock edge.

Table 10. Recommended I²S Pin Programming

FREQUENCY	V_{DDIO}	RECOMMENDED SPEED SETTING
< 25MHZ	1.7V to 2.24V	10
	2.25V to 3.6V	11
25MHZ to 50MHZ	1.7V to 2.24V	01
	2.25V to 3.6V	10

Table 11. Recommended SPI Pin Programming

FREQUENCY	V_{DDIO}	LATCHING EDGE	RECOMMENDED SPEED SETTING
< 12.5MHZ	1.7V to 2.24V	Opposite from shift	10
	2.25V to 3.6V		11
12.5MHZ to 25MHZ	1.7V to 2.24V	Opposite from shift	01
	2.25V to 3.6V		10

Latch-On Power-Up Pins

The logic state at specific configuration input pins are latched on power-up. These states set initial register values and

functional modes that cannot be easily programmed through I2C or UART after the device powers up.

Bias the pins to V_{DDIO} for a logic 1 or GND for a logic 0 using sufficiently high-value resistors (up to 10kΩ). Make sure the voltage seen at the pin is at a valid logic level to ensure proper latching.

All latch-on power-up pins also double as general-purpose output-only pins after power-up. Before the pin states are latched, the device does not drive the pin. Use the GPIO pins that function doubly as latch-on-power-up pins only as outputs, unless it is guaranteed that the proper pin logic state is present at the pin at power-up.

When the pin is used as an output, the pin should not be driven externally, and the power-up state is solely determined by the external resistor.

Here is the list and description of latch-on power-up bits:

ADD2, ADD1, ADD0: These bits set the device address (DEV_ADDR) used as the subordinate address by I2C and UART. They also set the default value of the TX_SRC_ID registers of each low bandwidth channel (audio, info-frame, I2C, UART, SPI, GPIO). Device addresses can be changed after power-up by writing to the DEV_ADDR register.

Table 12. Device Address

ADDRESS BITS ADD[2:0]	DEVICE ADDRESS
000	0x90
001	0x94
010	0x98
011	0xD0
100	0xD4
101	0xD8
110	0x50
111	0x54

CXTP: This bit sets the device into Coaxial or Twisted-Pair mode, with the value reflected in both register bits CXTP_A and CXTP_B. This bit can be changed after power-up, as one link can be set as Coax and the other as Twisted-Pair. CXTP = 0 sets differential mode operation at 3Gbps GMSL2 forward link rate, while CXTP = 1 sets single-ended Coax operation at 6Gbps GMSL2 forward link rate. The default reverse channel rate is set to 187.5Mbps independent of the CXTP setting.

I2CSEL: This bit selects either I2C or UART mode for internal register access and remote (over GMSL2 link) control channel communication. Set I2CSEL = 0 for UART or I2CSEL = 1 for I2C.

Clocking

GMSL Reference Clock

The GMSL2 devices require a reference clock source to generate the 6GHz line rate clock and associated internal clocks. Both the serializer and deserializer can be clocked with an external 25MHz crystal or an external clock source with a frequency accuracy of ±200ppm.

Spread-Spectrum Clocking (SSC)

Analog Devices' GMSL2 links provide exceptional EMI performance. Optional SSC is available to mitigate EMI emitted from devices and interconnections, and provide additional margin.

SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to ±2500ppm from the center frequency.

Power-Up and Link Start-Up

GMSL2 devices are in power-down mode when PWDNB pin is low or when any of the power supplies are down. Register and configurations are set to default reset conditions.

The serializer and deserializer can power up in any order. After PWDNB is released and all power supplies are up, each

device starts its power-up sequence and performs the following actions in sequence:

1. Latch-on-power-up pins register set. Set internal registers according to the selected configuration: I2CSEL, CXTP, ADD0, ADD1, ADD2, RCLKEN (if available).
2. Control channel (I^2C or UART) is functional on local side. Device registers are writable and readable.
3. Link is established based on settings as described. Not all GMSL2 parts support the full suite of configuration options.
   a. Single Link Auto Selection mode (AUTO_LINK = 1 and LINK_CFG = 1 or 2): Automatically select which PHY to use to establish GMSL2 link by periodically trying to handshake using PHY A and PHY B. Note: AUTO_LINK = 1 is the default and recommended setting to optimize lock time.
   b. Single Link Manual Selection mode (AUTO_LINK = 0 and LINK_CFG = 1 or 2): If LINK_CFG = 1, establish link using PHY A. If LINK_CFG = 2, establish link using PHY B.
   c. Dual Link mode (LINK_CFG = 0): Establish link using both PHYs.
   d. Splitter (serializer)/Aggregator (deserializer) mode (LINK_CFG = 3): Establish link using both PHYs (for specific applications only).
4. Each enabled PHY performs link calibration, equalizer adaptation, and data channel locking. Both devices set their LOCK pin high.
5. Control channel is available from the remote side.

The link-up process, from the time that the last part's PWDNB input is brought high, typically takes approximately 50ms nominally for any channels that meet the GMSL2 channel specification.

After the devices are linked, they can be configured. This can be done locally or over the control channel by a microcontroller on either the serializer or deserializer side.

Device Reset

There are three general reset options available through register writes:

1. RESET_ALL resets all blocks, including all registers, digital blocks, and analog blocks. This process is similar to driving the PWDNB pin low and then high. Note: If Sleep mode is being used, do not use RESET_ALL as it returns the device to Sleep mode.
2. Setting RESET_LINK resets all GMSL PHY-related digital logic and data pipelines. After this bit is set, all control registers are still accessible through the local control channel. The link remains in RESET until RESET_LINK is cleared.
3. RESET_ONESHOT resets all GMSL PHY-related digital logic and data pipelines, then automatically clears itself. RESET_ONESHOT should only be set when GMSL link LOCK is present. This is similar to setting and clearing RESET_LINK.

Program the registers that affect the GMSL2 link operation first (e.g., TX_RATE, RX_RATE, CXTP_A/B, AUTO_LINK, LINK_CFG, GMSL2), followed by RESET_LINK or RESET_ONESHOT, or set these registers when RESET_LINK = 1, then set RESET_LINK = 0.

Link and Video Lock

GMSL2 Link Lock

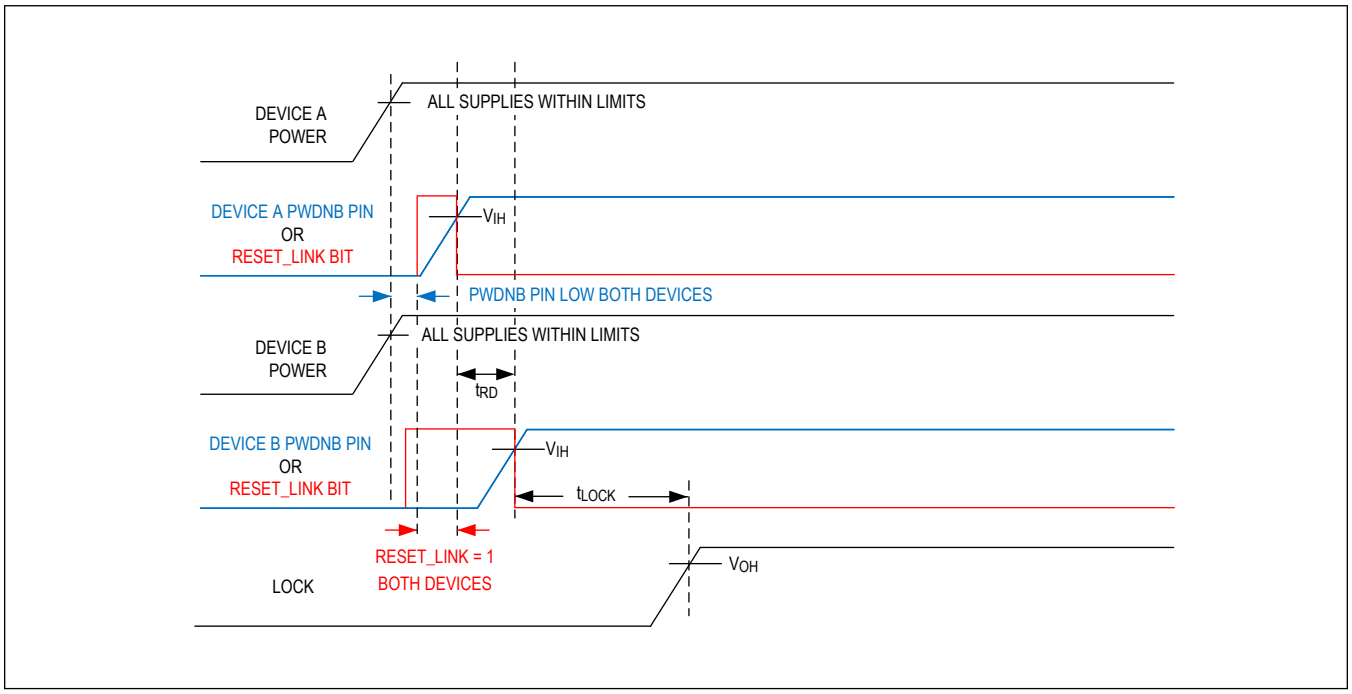


Figure 17. GMSL2 Lock Time

Figure 17 illustrates the sequence that is used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power-up or resume operation from a RESET_LINK state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I^2C/UART, SPI, GPIO, audio) can be used immediately after link lock is asserted.

The device will establish single link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in, and the system is up and running. Lock is obtained with no interaction between the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

Dual-link and splitter configurations require additional user programming. For guidance on enabling these configurations and optimizing the lock time, contact the factory.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links, so a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. Lock time is measured from the later of PWDNB or RESET_LINK release in either the serializer or deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate lock, PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, RESET_LINK is assumed to be low after power-up (normal operation).
6. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices) must be less than the threshold specified in *Note 4*. Contact the factory for guidance if this timing cannot be

guaranteed.

7. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and the deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permissible t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.
8. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This will minimize any disruptions caused by a transient loss in connectivity.

Video Lock

Video lock bit indicates the deserializer is receiving valid video data. After the GMSL2 link is locked, the deserializer video output PLL starts its locking sequence. The deserializer normally starts outputting video data several milliseconds after it asserts line lock, provided it is receiving video packets from the serializer. The video lock status is typically read from a register. However, the deserializer LOCK pin behavior can be changed by a register setting so that the LOCK pin is asserted only when the deserializer is outputting video.

Power Standby and Sleep Mode

A power manager block is present in all GSML2 products. Its primary function is to monitor supply voltages and control Power-down (standby) and Sleep modes.

There are two ways to go into Low Power mode while all power supplies are active: asserting the PWDNB pin or invoking the sleep state. Both states offer very low power supply currents.

Asserting the PWDNB pin (active-low) places the device in Standby Power mode and resets the digital registers and configurations to their default power-up condition. Any supply dropping below its internal threshold settings also places the device in Power-down mode.

The sleep state preserves all critical register settings and configurations. The register table indicates which registers are retained. The device can be put into the sleep state through an I^2C/UART command.

The resume state restores the device to the presleep condition without the need for additional register writes. There are two ways to resume normal operations from Sleep mode:

Local Wakeup:

- Local wakeup entails the local host processor initiating a dummy control channel transaction, which briefly wakes up the device. In I^2C mode, the initial temporary wakeup requires four falling edges on SDA. Depending on the device address used, there may need to be multiple consecutive dummy transactions issued by the host to achieve the required four SDA falling edges. The dummy transaction(s) must immediately be followed by the host processor setting SLEEP=0 to permanently exit Sleep mode. The device automatically returns to Sleep mode if SLEEP remains set to 0.

Remote Wakeup:

- All GMSL devices include wakeup detectors to observe GMSL link activity and briefly turn on the device when activity is detected. The link can then lock, providing an opportunity for a remote host to disable Sleep mode (setting SLEEP=0). The device automatically reverts to Sleep mode if SLEEP remains set to 1.

GPIOs are placed in Hi-Z during Power-down and Sleep modes.

Error and Fault Condition Monitoring

Both the serializer and deserializer have an open-drain, multipurpose error reporting and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers. The reason for assertion of ERRB can be determined by reading the register status.

Adaptive Equalization (AEQ)

GMSL2 devices automatically adapt receiver characteristics to compensate for the insertion and return loss

characteristics of the channel, which consists of the cables, connectors, and PCBs. This optimizes performance on any channel that meets the GMSL2 channel specification. The equalizer architecture makes GMSL2 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock and then is invoked at a ~1Hz rate to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye opening by using the built in eye-opening monitor.

Video Pipeline

Video Line Cyclic Redundancy Check (CRC)

A CRC32 polynomial is used to generate a 32-bit code at the end of each DE or HS pulse. This code is transferred to the receiver (deserializer) side using info frames. The CRC checker generates the same code on the receiver side and checks if the generated and received CRC codes are the same. If not, it asserts an error. The CRC check is done at every falling edge of DE on the receiver side even if the infoframe is not received.

Rx Crossbar, Video PRBS Checker, and Watermark Checker

The device's VRX block contains functions including crossbar, watermark, and video PRBS checker.

Data received from the video FIFO is fed to a crossbar switch before it is passed on to the balance of the video pipeline. The crossbar is configured from the configuration registers and can be used to reorder the color and sync signal. It can also be used to invert the signals individually and force them to a constant value, if desired.

The watermark block is used to check if the video image is not frozen.

The video PRBS checker needs to be enabled after the video is locked.

Video-Timing Constraints

Review the data sheet of the paired serializer to the MAX96752 to determine timing constraints on the active video and blanking timing parameters.

Eye-Opening Monitor (EOM)

The EOM enables GMSL2 parts to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error free, but has less link margin than desired. This allows proactive reaction to deteriorating cable performance before any link errors occur. GMSL2 devices can measure the horizontal or vertical eye opening of the equalizer's output. The measurement is activated automatically at a ~1Hz rate once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye-opening is then reported, and the EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds.

Watermarking

The watermarking block detects a frozen frame failure in a frame-based processing system between the generator and detector. This feature specifically detects frozen frames caused by system-on-chip (SOCs) in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector. GMSL2 devices contain both a watermark generator and detector. This allows both serializers and deserializers to insert or detect a watermark in a safety-relevant video stream. The watermark generator inserts a time-varying watermark that is highly redundant and robust to image processing and display stream compression. The watermark detector looks for this time-varying watermark, and if it fails to see all the generated watermarks, this indicates a frozen frame failure in a frame-based processing system between the generator and detector. Upon detection of this error condition, the watermark detector can generate an interrupt and/or blank the output video returning the display to a safe state in less than 500ms.

Vertical Sync Output for Backlight Pulse-Width Modulation (PWM) Synchronization

The deserializer can optionally synchronize the backlight PWM output with the vertical sync (VS) signal to ensure that video output is accurately dimmed and video data is properly aligned with the start of the video frame. Highly predictable video performance is achieved by aligning the PWM output with the start of the video frame. Write 1 to the VS_OUT_EN register field to enable this function; write 0 to the same field to disable it. Note that enabling VS output is a secondary function of a GPIO pin.

Pseudorandom Binary Sequence (PRBS)

Video PRBS

The video channel has a PRBS generator in the serializer and a PRBS checker in the deserializer to test the video channel operation. The video PRBS generator can work with the PCLK recovered by the serializer from an HDMI, parallel, or mobile industry processor interface (MIPI) input. An external PCLK can also be provided to a designated GPIO pin to run the video PRBS generator.

Note that all link bandwidth is not used by the video channel alone in the GMSL2 mode; it is possible to have a bit error on the link that does not cause a video PRBS error.

Audio PRBS

The audio channel includes a PRBS generator on the transmitter side and a checker at the receiver side to test the audio channel operation. The audio PRBS generator can operate using the incoming I^2S SCK and WS signals or using an internally-generated reference clock. The detected audio channel bit errors are reported through a status register.

OpenLDI (OLDI) Deserializer Video Output

Overview

OLDI interface drives display panels from the deserializer. It receives video data from the video pipeline and maps it to OLDI output ports A, B, or both. The output can drive with OLDI or VESA formats. The OLDI clock output is generated by the deserializer based on the tracked and measured clock frequency of video input at the serializer. For more information about the OLDI standard, refer to OpenLDI specification.

Odd/Even Pixel Interleaving in Dual OLDI Mode

The OLDI output processor can split the output to the two OLDI ports at half the PCLK frequency by using the active-high or active-low versions of the DE or HS signals for even/odd pixel alignment or without any alignment at all.

Maximum OLDI Pixel Clock

The MAX96752 supports a maximum pixel clock of 300MHz. The OLDI output ports each support 150MHz. Therefore, in Single-output mode, a maximum of 150MHz is supported. In Even/Odd Pixel Interleaved Dual-port mode, video streams up to 300MHz PCLK frequency can be output from the device.

Flexible Output Programming

- Configurable as 1 x 4, 1 x 8, or 2 x 4 lanes.
- Four lanes (for RGB888) or optionally three lanes (for RGB666) of the OLDI ports can be enabled.
- The OLDI output lanes can be inverted and/or swapped.
- VS can be viewed on GPIO01. It includes an optional single-cycle glitch filter.

Color Lookup Table (LUT)

The LUT is intended mainly for gamma correction. It has 3 x 256, 8-bit registers that allow any color in the RGB domain to be mapped to any RGB color. This can be used to generate color filters or gamma correction maps.

Spread-Spectrum

The OLDI output port can be programmed to have 0.5% center SSC with 20kHz to 40kHz triangular modulation frequency. It is possible to program the spread-spectrum percentage up to 4%. OLDI SSC mode programming is independent of the GMSL high-speed clock SSC mode.

Applications Information

Software Programming Model

Analog Devices' automotive serializers and deserializers are designed to follow a general software programming model. Except for features that require in-operation control channel accesses such as the ASIL safety measures and interrupt handling, the following programming model should be used:

1. Set the impacted functional blocks to disabled or reset mode. A general method to place the part in IDLE state is to stop all side channel and video traffic, followed by a register write (RESET_LINK = 1) to stop the GMSL link.
2. Fully configure the settings for each feature before it is enabled.
3. Establish the link by setting RESET_LINK = 0 and wait for the link to lock.
4. Start video and side channel traffic.

If the configuration of a feature is to be changed during the operation of other features, disable the feature that is reconfigured, change its settings, and re-enable it.

Programming Notes

Make the following register writes to ensure proper operation of the MAX96752. Without these writes, the operation of the device specified in the data sheet cannot be guaranteed

Mandatory Register Programing

Depending on system application, two register writes may be needed to ensure the quality of the GMSL link. There are internal circuits (Error Channel) that are, by default, periodically power cycled to perform receiver optimization functions. This power cycling can degrade performance (e.g., link performance, video integrity, etc.) under certain conditions (higher V_{DD} voltages; low temperatures). This problem is prevented by disabling the power cycling function, so the Error Channel is powered on continuously. See the table below for the conditions that require the register writes.

Table 13. GMSL Link Conditions

GMSL Link Speed	Mode of Operation	Workaround Requirements
6 Gbps	Single Link	Required
6 Gbps	Multiple Link	Required
3 Gbps	Single/Multiple Link	Not needed

Workaround

The Error Channel must be forced to remain on (not power cycled) via register writes below.

These register writes must be performed immediately after every power-up and device reset. Receiver optimization and all other functions are not impacted by this workaround. Total current increase is insignificant and does not impact the EC table values.

Table 14. Mandatory Register Writes

Register	Default Value	Write Value	Description
0x449	0x71	0x75	Force Channel A Error Channel always on
0x549	0x71	0x75	Force Channel B Error Channel always on

Control-Channel Programming

GMSL device registers can only be accessed and configured through the I^2C/UART interface in either the I^2C or UART mode. By default, the primary I^2C/UART channel is also sent to the remote-side device and any peripheral connections. This allows control of the GMSL devices from either end of the link. For multi-main configurations, with microcontrollers connected to both the serializer and deserializer, disable the remote control channel through register settings to prevent bus contention.

SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a main, followed by the device's 7-bit subordinate address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

Device Address

Each device on the I²C/UART control channel must have a unique address. The GMSL2 device address is set to one of several 7-bit addresses according to the state of the ADD[2:0] pins at power-up. See the *Latch-On-Power-Up Pins* section. Note that device address can be changed after power-up by writing to the DEV_ADDR register.

I²C Programming

Each device has an internal I²C subordinate for register access. The internal registers can be written and read according to the I²C protocol using the packet formats in Figure 18 and Figure 19.

I²C Write-Packet Format

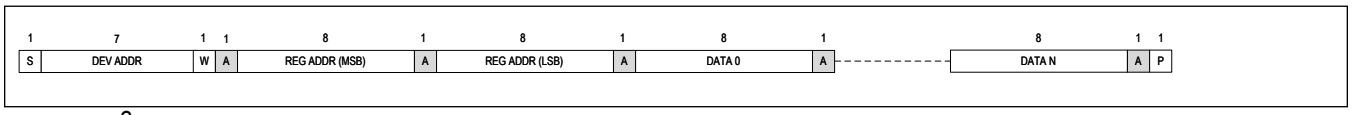


Figure 18. I²C Write-Packet Format

I²C Read-Packet Format

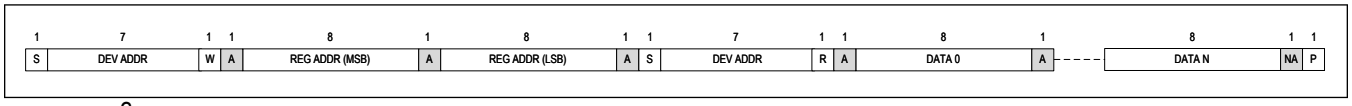


Figure 19. I²C Read-Packet Format

Host-to-Peripheral Primary I²C and Pass-Through I²C Communication

When communicating between a host and peripheral, primary and pass-through I²C operation are the same. An I²C tunnel across the GMSL2 link connects the host's I²C main to the remote I²C subordinate. This logically connects separated I²C buses, enabling I²C transactions across the serial link to occur (with some delay) as if performed on the same physical I²C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I²C main connects to a GMSL2 device I²C subordinate, and the peripheral I²C subordinate connects to a GMSL2 device I²C main. For example, when the host I²C main transacts on one side of the link (local-side), data is forwarded to the other side (remote-side) by the I²C subordinate of the local-side GMSL2 device. Data is then received by the I²C main of the remote-side GMSL2 device, which in turn generates the same I²C transaction with the peripheral subordinate I²C. The remote-side GMSL2 device sends back any I²C data expected by the local-side.

The I²C interface uses clock stretching (holding SCL low) to account for timing differences between main and subordinate and to allow time for data to be forwarded and received across the serial link. All local-side I²C devices must support clock stretching by the GMSL2 device; remote-side I²C devices are not required to support clock stretching.

The host can program the GMSL2 device registers to independently configure the pass-through I²C/UART interfaces as either I²C or UART.

UART Programming

When the primary I²C/UART interface is configured as UART, there are two operating modes: base and bypass.

UART Base Mode

Base mode is the means of µC communication with the serializer and deserializer in which registers in these devices, as well as registers in peripheral devices, can be accessed. Base mode is enabled by default at power-up. In Base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL2 UART packet protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer. The µC communicates with a UART peripheral in Base mode (through INTTYPE

register settings). The device addresses of the serializer and deserializer in this mode are programmable.

In Base mode, serializer, deserializer, and peripheral registers can be written and read using the half-duplex GMSL2 UART protocol.

Figure 20 shows the UART protocol for writing and reading in Base mode.

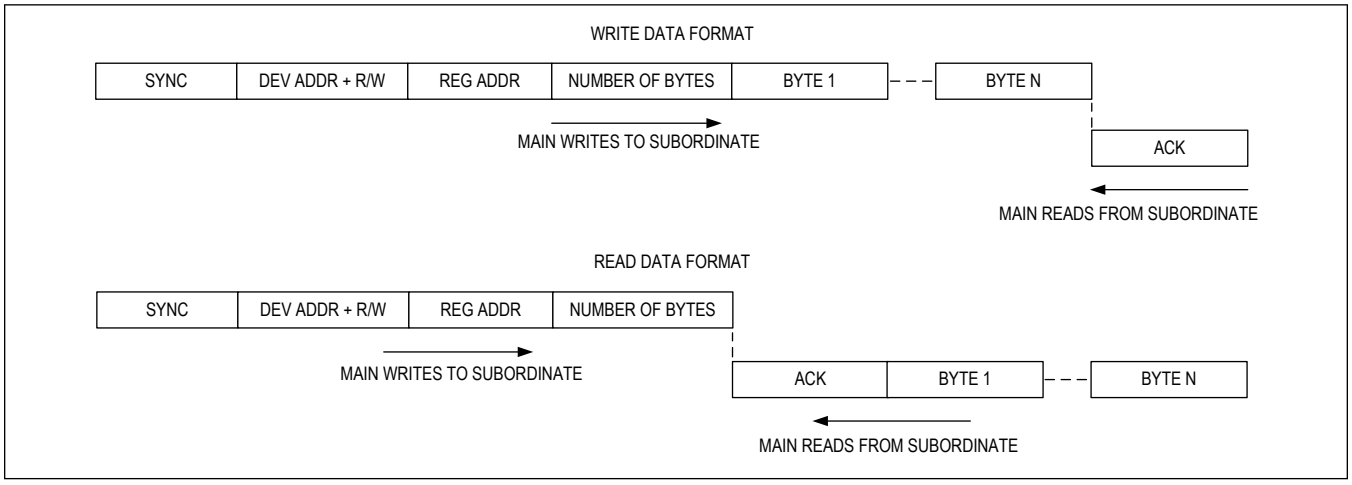


Figure 20. GMSL2 UART Protocol for Base Mode

UART Bypass Mode

In Bypass mode, the serializer/deserializer ignore UART commands from the µC, allowing the µC to communicate only with peripheral devices. The µC cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL link. Ignoring UART transactions prevents inadvertent misprogramming of serializer and deserializer registers. The device addresses of the serializer and deserializer in this mode are not programmable.

Switching Between UART Base and Bypass Modes

There are two ways to switch between Base and Bypass modes: programming the register and using the MS pin.

When register programmed, Bypass mode is active only as long as there is UART activity. When there is no UART activity for a selected timeout, both devices exit Bypass mode, and the bit is automatically cleared.

When set by the MS pin, a high pin level puts the device into Bypass mode, and a low level puts the device in Base mode. MS is set on the fly and is not latched on power-up.

UART Frame Format

Regular UART frames with an even parity bit are used to carry 1 byte of data each. A frame consists of a low start bit followed by 8 data bits, a parity bit, and is finished with a high stop bit. The parity bit is high if the number of ones in the 8 bits of data is odd. Otherwise, the parity bit is low. There must be at least 1 high stop bit. If the next frame is in the same packet, there can be at most 4 high bits from the end of the stop bit to the beginning of the next start bit. Note that in the case of a parity bit error, the packet is discarded, starting from the frame with the error. The start of each frame is always a high-to-low transition (i.e., the stop bit is high and the start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer calibrates the length of one UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions, and the recipient of the data must perform error checking. The parity bit (which is enabled by default in bypass mode) can be disabled before entering Bypass mode. Note that the bit rate in Bypass mode must be the same bit rate last used in Base mode.

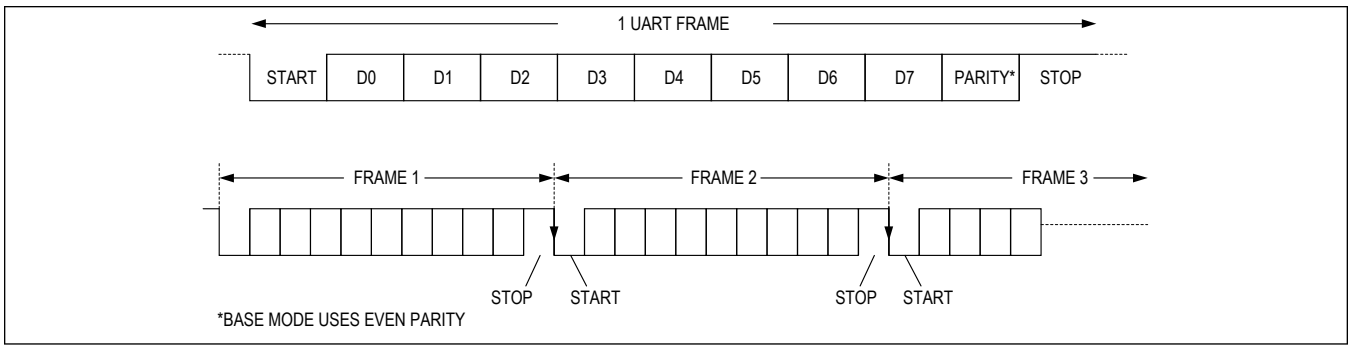


Figure 21. UART Data Format for Base Mode

Synchronization Frame

The serializer/deserializer must calibrate internal bit-length counters with the UART bit rate for proper recovery of UART frames. A synchronization frame (a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal 150MHz clock. Synchronization frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next synchronization frame.

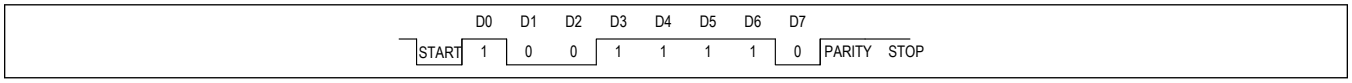


Figure 22. UART Synchronization Frame

Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors are detected in the transmitted packet, and it is recognized as valid. This is sent after the last bit of a successfully recognized packet is received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

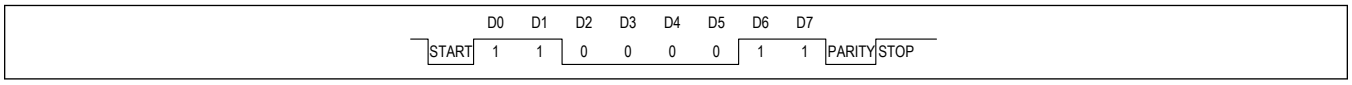


Figure 23. UART Acknowledge Frame

Write Packet

Write packets consist of a 5-byte packet header followed by one or more data bytes. A packet is recognized as a write packet when the LSb of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors were detected while receiving the write packet and the write packet is valid. Byte count indicates the number of data bytes to be written, and it cannot be 0.

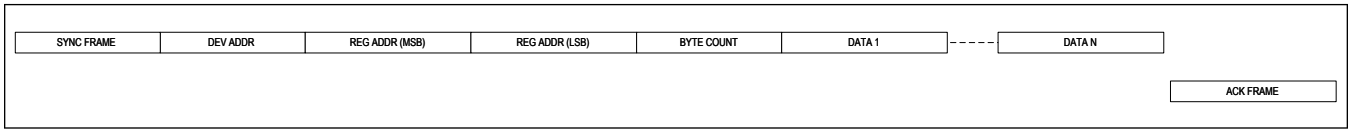


Figure 24. UART Write-Packet Format

Read Packet

Read packet consists of 5 bytes. The LSb of the device address frame is 1 for read packets. If no errors were detected while receiving the read packet and the packet is valid, the addressed device responds with an acknowledge frame followed by one or more data bytes. Byte count indicates the number of data bytes to be read, and it cannot be 0.

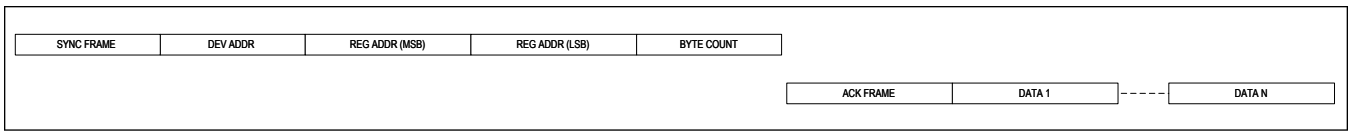


Figure 25. UART Read-Packet Format

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX96752GTN/V+	-40°C to +105°C	56-Lead TQFN-EP
MAX96752GTN/V+T	-40°C to +105°C	56-Lead TQFN-EP
MAX96752GTN/VY+	-40°C to +105°C	56-Lead TQFN-SW-EP
MAX96752GTN/VY+T	-40°C to +105°C	56-Lead TQFN-SW-EP

/V Denotes an automotive-qualified part.

+ Denotes a lead(Pb)-free/RoHS/compliant package.

T Denotes tape and reel

EP = Exposed Pad

Register Map

MAX96752

Reserved, Unused, and Read-Only Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (read/replace/write).

In this document, default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

Note: *Indicates the register is stored when entering sleep mode and is restored upon exit.

To ensure proper device operation, see both:

1) Mandatory Register Programming section based on existing Errata documentation

2) Device-specific User Guide

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x90	REG0[7:0]*	DEV_ADDR[6:0]							CFG_BLOCK
0x01	0x02	REG1[7:0]*	LVDS_HALFSW	–	IIC_2_EN	IIC_1_EN	TX_RATE[1:0]		RX_RATE[1:0]	
0x02	0x47	REG2[7:0]*	LOCK_CFG	VID_EN	DIS_LOCAL_CC	DIS_REM_CC	–	AUD_TX_EN	RSVD	RSVD
0x03	0x20	REG3[7:0]*	RSVD	–	RSVD	I2CSEL	UART_2_EN	UART_1_EN	–	VIDEO_LOCK
0x0D	0x82	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x01	REG14[7:0]	RSVD[3:0]				DEV_REV[3:0]			
0x0F	0x00	REG15[7:0]	RSVD	RSVD	SPEED_CPBL[1:0]		RSVD	DUAL_CPBL	SPLTR_CPBL	RSVD
0x38	0x00	IO_CHK0[7:0]	RSVD[7:0]							
0x39	0x00	IO_CHK1[7:0]	PIN_DRV_EN_1[7:0]							
0x3A	0x30	IO_CHK2[7:0]	PIN_DRV_SEL	–	RSVD[1:0]		RSVD	RSVD	PIN_DRV_EN_2[1:0]	
0x3B	0x00	IO_CHK3[7:0]	RSVD[7:0]							
0x3C	0x00	IO_CHK4[7:0]	PIN_IN_1[7:0]							
OVERLAP										
TCTRL										
0x08	0x00	PWR0[7:0]	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x09	0x00	PWR1[7:0]	OVERTEMP	RSVD	RSVD[5:0]					
0x0C	0x1A	PWR4[7:0]*	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x10	0x11	CTRL0[7:0]*	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	–	LINK_CFG[1:0]	
0x11	0x22	CTRL1[7:0]*	–	–	RSVD	CXTP_B	BACK_COMP_SPLTR	RSVD	RSVD	CXTP_A
0x13	0x10	CTRL3[7:0]	RSVD	RSVD	LINK_MODE[1:0]		LOCKED	ERROR	CMU_LOCKED	–
0x18	0xA0	INTR0[7:0]*	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x19	0x00	INTR1[7:0]*	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x1A	0x03	INTR2[7:0]*	RSVD	RSVD	REM_ERR_OEN	RSVD	RSVD	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
0x1B	0x00	INTR3[7:0]	RSVD	RSVD	REM_ERR_FLAG	RSVD	RSVD	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x1C	0x09	INTR4[7:0]*	RSVD	EOM_ERR_OEN_A	–	RSVD	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
0x1D	0x00	INTR5[7:0]	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	–	RSVD	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
0x1E	0x0E	INTR6[7:0]*	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	VDD_OV_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	APRBS_ERR_OEN	VID_PXL_CRC_ERR_OEN
0x1F	0x00	INTR7[7:0]	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	VDD_OV_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	APRBS_ERR_FLAG	VID_PXL_CRC_ERR_FLAG
0x20	0x1F	INTR8[7:0]*	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x21	0x5F	INTR9[7:0]*	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
0x22	0x00	CNT0[7:0]	DEC_ERR_A[7:0]							
0x24	0x00	CNT2[7:0]	IDLE_ERR[7:0]							
0x25	0x00	CNT3[7:0]	PKT_CNT[7:0]							
0x26	0x00	CNT4[7:0]	VID_PXL_CRC_ERR[7:0]							
GMSL										
0x29	0x00	TX1[7:0]*	LINK_PRBS_GEN	–	ERRG_EN_B	ERRG_EN_A	–	–	RSVD	RSVD
0x2A	0x20	TX2[7:0]*	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x2B	0x44	TX3[7:0]*	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x2C	0x00	RX0[7:0]*	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x30	0x41	GPIOA[7:0]*	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
0x31	0x88	GPIOB[7:0]*	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
CC										
0x40	0x26	I2C_0[7:0]*	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x41	0x56	I2C_1[7:0]*	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x42	0x00	I2C_2[7:0]*	SRC_A[6:0]							–
0x43	0x00	I2C_3[7:0]*	DST_A[6:0]							–
0x44	0x00	I2C_4[7:0]*	SRC_B[6:0]							–
0x45	0x00	I2C_5[7:0]*	DST_B[6:0]							–
0x46	0x08	I2C_6[7:0]*	–	–	–	–	I2C_AUTO_CFG	I2C_SRC_CNT[2:0]		
0x47	0x00	I2C_7[7:0]	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
0x48	0x42	UART_0[7:0]*	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
0x49	0x96	UART_1[7:0]	BITLEN_LSB[7:0]							
0x4A	0x80	UART_2[7:0]	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
0x4C	0x26	I2C_PT_0[7:0]	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
0x4D	0x56	I2C_PT_1[7:0]	MST_DBL_PT	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
0x4E	0x00	I2C_PT_2[7:0]	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
0x4F	0x00	UART_PT_0[7:0]	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
CFGH VIDEO										
0x50	0x00	RX0[7:0]*	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGL AUDIO										
0x58	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x59	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x5B	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x5C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x5D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	RSVD	–	–	–
0x5E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN

ADDRESS	RESET	NAME	MSB							LSB
0x5F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGI INFOFR										
0x60	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x61	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x63	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x64	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
CFGL SPI										
0x68	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x69	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x6B	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x6C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x6D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	RSVD	–	–	–
0x6E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x6F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC CC										
0x70	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x71	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x73	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x74	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x75	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	RSVD	–	–	–
0x76	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x77	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL GPIO										
0x78	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x79	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x7B	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x7C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x7D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	RSVD	–	–	–
0x7E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x7F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL IIC_X										
0xA0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xA3	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xA4	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xA5	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	RSVD	–	–	–
0xA6	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0xA7	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL IIC_Y										
0xA8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xAB	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xAC	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xAD	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	RSVD	–	–	–
0xAE	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0xAF	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
VID_RX										
0x100	0x32	VIDEO_RX0[7:0]*	LCRC_ERR	RSVD	RSVD	RSVD	RSVD	RSVD	LINE_CRC_EN	RSVD
0x103	0x40	VIDEO_RX3[7:0]*	RSVD	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x104	0x0C	VIDEO_RX4[7:0]	VID_OVERFLW_LIM_L[7:0]							
0x105	0xD0	VIDEO_RX5[7:0]	VID_UNDERFLW_LIM_L[7:0]							
0x106	0x02	VIDEO_RX6[7:0]	VID_SAR_INC_H[2:0]			–	–	–	VID_UNDERFLW_LIM_H	VID_OVERFLW_LIM_H

ADDRESS	RESET	NAME	MSB							LSB
0x107	0x40	VIDEO_RX7[7:0]	VID_SAR_INC_L[7:0]							
0x108	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
0x10A	0x00	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	RSVD[5:0]					
0x111	0x00	CLOCKGEN[7:0]*	–	–	–	–	CLK_FREEZE_RNG[1:0]		CLK_FREEZE_CONS	CLK_FREEZE
AUD_TX AX										
0x120	0xB0	AUDIO_TX0[7:0]*	I2S_TDM_CFG[1:0]		I2S_CFG[1:0]		INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
0x121	0x4E	AUDIO_TX1[7:0]*	AUD_PRIO[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	RSVD[1:0]	
0x125	0x00	AUDIO_TX5[7:0]	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
0x127	0x00	AUDIO_TX7[7:0]	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
0x128	0x40	AUDIO_TX8[7:0]	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
AUD_RX										
0x140	0x21	AUDIO_RX1[7:0]*	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
0x143	0x00	AUDIO_RX4[7:0]	APRBS_ERR[7:0]							
0x146	0x02	AUDIO_RX7[7:0]*	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
0x148	0x00	AUDIO_RX9[7:0]	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			
0x14D	0x00	INFO_RX4[7:0]	–	INFO_AUD_DEPTH[6:0]						
SPI										
0x160	0x08	SPI_0[7:0]*	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
0x161	0x1D	SPI_1[7:0]*	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
0x162	0x03	SPI_2[7:0]*	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
0x163	0x00	SPI_3[7:0]*	SPIM_SS_DLY_CLKS[7:0]							
0x164	0x00	SPI_4[7:0]*	SPIM_SCK_LO_CLKS[7:0]							
0x165	0x00	SPI_5[7:0]*	SPIM_SCK_HI_CLKS[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x166	0x00	SPI_6[7:0]*	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
0x167	0x00	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
0x168	0x00	SPI_8[7:0]*	REQ_HOLD_OFF_TO[7:0]							
WM										
0x188	0x00	WM_0[7:0]*	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		WME_EN	WM_EN
0x18A	0x50	WM_2[7:0]*	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
0x18B	0x14	WM_3[7:0]*	–	WM_TH[6:0]						
0x18C	0x10	WM_4[7:0]*	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
0x18D	0x00	WM_5[7:0]	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR
0x18E	0x00	WM_6[7:0]	WM_TIMER[7:0]							
0x1AE	0x00	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x1AF	0x00	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
VRX										
0x1B0	0x00	CROSS_0[7:0]*	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x1B1	0x01	CROSS_1[7:0]*	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x1B2	0x02	CROSS_2[7:0]*	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x1B3	0x03	CROSS_3[7:0]*	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x1B4	0x04	CROSS_4[7:0]*	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x1B5	0x05	CROSS_5[7:0]*	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x1B6	0x06	CROSS_6[7:0]*	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x1B7	0x07	CROSS_7[7:0]*	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x1B8	0x08	CROSS_8[7:0]*	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x1B9	0x09	CROSS_9[7:0]*	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x1BA	0x0A	CROSS_10[7:0]*	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x1BB	0x0B	CROSS_11[7:0]*	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x1BC	0x0C	CROSS_12[7:0]*	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x1BD	0x0D	CROSS_13[7:0]*	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x1BE	0x0E	CROSS_14[7:0]*	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x1BF	0x0F	CROSS_15[7:0]*	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x1C0	0x10	CROSS_16[7:0]*	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x1C1	0x11	CROSS_17[7:0]*	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x1C2	0x12	CROSS_18[7:0]*	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x1C3	0x13	CROSS_19[7:0]*	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x1C4	0x14	CROSS_20[7:0]*	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x1C5	0x15	CROSS_21[7:0]*	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x1C6	0x16	CROSS_22[7:0]*	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x1C7	0x17	CROSS_23[7:0]*	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x1C8	0x18	CROSS_24[7:0]*	–	CROSS24_I	CROSS24_F	CROSS24[4:0]				
0x1C9	0x19	CROSS_25[7:0]*	–	CROSS25_I	CROSS25_F	CROSS25[4:0]				
0x1CA	0x1A	CROSS_26[7:0]*	–	CROSS26_I	CROSS26_F	CROSS26[4:0]				
0x1CB	0x1B	CROSS_27[7:0]*	–	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x1CC	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1CD	0x00	OLDI0[7:0]*	RSVD	–	VPRBS_FAIL	VPRBS_CHK_EN	RSVD	LUT_C_EN	LUT_B_EN	LUT_A_EN
0x1CE	0x06	OLDI1[7:0]*	OLDI_OUTSEL	OLDI_FORMAT	OLDI_4TH_LANE	OLDI_SWAP_AB	OLDI_SPL_EN	OLDI_SPL_MODE[1:0]		OLDI_SPL_POL
0x1CF	0x08	OLDI2[7:0]*	PD_LVDS_B	PD_LVDS_A	RSVD	VS_OUT_EN	RSVD	RSVD	OLDI_DUP	SSEN
0x1D0	0x00	OLDI3[7:0]*	LANE_INV_B0	LANE_SEL_B0[2:0]			LANE_INV_A0	LANE_SEL_A0[2:0]		
0x1D1	0x11	OLDI4[7:0]*	LANE_INV_B1	LANE_SEL_B1[2:0]			LANE_INV_A1	LANE_SEL_A1[2:0]		
0x1D2	0x22	OLDI5[7:0]*	LANE_INV_B2	LANE_SEL_B2[2:0]			LANE_INV_A2	LANE_SEL_A2[2:0]		
0x1D3	0x33	OLDI6[7:0]*	LANE_INV_B3	LANE_SEL_B3[2:0]			LANE_INV_A3	LANE_SEL_A3[2:0]		
0x1D4	0x44	OLDI7[7:0]*	LANE_INV_BCLK	LANE_SEL_BCLK[2:0]			LANE_INV_ACLK	LANE_SEL_ACLK[2:0]		

ADDRESS	RESET	NAME	MSB							LSB
0x1EA	0x04	VRX46[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	DUAL_OLDI_AUTO_RST_ALIGNED	DUAL_OLDI_AUTO_RST_ALIGN
GPIO1 1										
0x203	0x84	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x204	0xA1	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x205	0x41	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO2 2										
0x206	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x207	0xA2	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x208	0x42	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO3 3										
0x209	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x20A	0xA3	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x20B	0x43	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO4 4										
0x20C	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x20D	0xA4	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x20E	0x44	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO5 5										
0x20F	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x210	0xA5	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x211	0x45	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO6 6										
0x212	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x213	0xA6	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x214	0x46	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
GPIO7 7										
0x215	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x216	0xA7	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x217	0x47	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO8 8										
0x218	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x219	0xA8	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x21A	0x48	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO9 9										
0x21B	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x21C	0xA9	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x21D	0x49	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO10 10										
0x21E	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x21F	0xAA	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x220	0x4A	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO11 11										
0x221	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x222	0x2B	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x223	0x4B	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO12 12										
0x224	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x225	0x2C	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x226	0x4C	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO13 13										
0x227	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x228	0x2D	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x229	0x4D	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO14 14										
0x22A	0x18	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x22B	0x4E	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x22C	0x4E	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO15 15										
0x22D	0x18	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x22E	0x4F	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x22F	0x4F	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
CMU										
0x244	0x0B	CMU4[7:0]	RSVD[1:0]		RSVD[1:0]		GPIO_SPEED_B[1:0]		GPIO_SPEED_A[1:0]	
MISC										
0x24A	0xDC	UART_PT_0[7:0]	BITLEN_PT_1_L[7:0]							
0x24B	0x05	UART_PT_1[7:0]	–	–	BITLEN_PT_1_H[5:0]					
0x24C	0xDC	UART_PT_2[7:0]	BITLEN_PT_2_L[7:0]							
0x24D	0x05	UART_PT_3[7:0]	–	–	BITLEN_PT_2_H[5:0]					
0x252	0x00	I2C_PT_4[7:0]*	SRC_A_1[6:0]							–
0x253	0x00	I2C_PT_5[7:0]*	DST_A_1[6:0]							–
0x254	0x00	I2C_PT_6[7:0]*	SRC_B_1[6:0]							–
0x255	0x00	I2C_PT_7[7:0]*	DST_B_1[6:0]							–
0x256	0x00	I2C_PT_8[7:0]*	SRC_A_2[6:0]							–
0x257	0x00	I2C_PT_9[7:0]*	DST_A_2[6:0]							–
0x258	0x00	I2C_PT_10[7:0]*	SRC_B_2[6:0]							–
0x259	0x00	I2C_PT_11[7:0]*	DST_B_2[6:0]							–
0x25D	0x05	PM_OV_START[7:0]	–	–	–	–	RSVD[1:0]		OV_LEVEL[1:0]	

ADDRESS	RESET	NAME	MSB							LSB
0x2D2	0x00	LOSS_INT_OEN[7:0]*	–	–	–	–	–	–	LOSS_OF_LOCK_OEN	LOSS_OF_VIDEO_LOCK_OEN
0x2D3	0x00	LOSS_INT_FLAG[7:0]	–	–	–	–	–	–	LOSS_OF_LOCK_FLAG	LOSS_OF_VIDEO_LOCK_FLAG
RLMS A										
0x403	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x404	0x4B	RLMS4[7:0]*	RSVD_EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		RSVD_EOM_PER_MODE	EOM_EN
0x405	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x406	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x407	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x434	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x435	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x437	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x438	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x439	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x43A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x43B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x43D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x43E	0xB3	RLMS3E[7:0]	ErrChPhSecTA	ErrChPhSec[6:0]						
0x43F	0x72	RLMS3F[7:0]	ErrChPhPriTA	ErrChPhPri[6:0]						
0x449	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x458	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x459	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x464	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x470	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x471	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x472	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x473	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x474	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x475	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x476	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	

ADDRESS	RESET	NAME	MSB							LSB
0x495	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x4A4	0xBD	RLMSA4[7:0]*	RSVD_AEQ_PER_MULT[1:0]		RSVD_AEQ_PER[5:0]					
0x4AC	0xCD	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
0x4AD	0x0D	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
0x4AE	0xCE	RLMSAE[7:0]	ErrChPhSecTAFR1G5	ErrChPhSecFR1G5[6:0]						
0x4AF	0x0F	RLMSAF[7:0]	ErrChPhPriTAFR1G5	ErrChPhPriFR1G5[6:0]						
0x4B0	0xB4	RLMSB0[7:0]	ErrChPhSecTASR1G5	ErrChPhSecSR1G5[6:0]						
0x4B1	0x73	RLMSB1[7:0]	ErrChPhPriTASR1G5	ErrChPhPriSR1G5[6:0]						
0x4B2	0xBE	RLMSB2[7:0]	ErrChPhSecTASRG75	ErrChPhSecSRG75[6:0]						
0x4B3	0x7D	RLMSB3[7:0]	ErrChPhPriTASRG75	ErrChPhPriSRG75[6:0]						
0x4B4	0xBC	RLMSB4[7:0]	ErrChPhSecTASRG375	ErrChPhSecSRG375[6:0]						
0x4B5	0x7B	RLMSB5[7:0]	ErrChPhPriTASRG375	ErrChPhPriSRG375[6:0]						
0x4B6	0xBB	RLMSB6[7:0]	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
0x4B7	0x7A	RLMSB7[7:0]	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
RLMS B										
0x503	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x504	0x4B	RLMS4[7:0]*	RSVD_EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		RSVD_EOM_PER_MODE	EOM_EN
0x505	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x506	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						

ADDRESS	RESET	NAME	MSB							LSB
0x507	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x534	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x535	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x537	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMon Done	EyeMon CntClr	EyeMon Start	EyeMon Ph	EyeMon DPol
0x538	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x539	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x53A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x53B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x53D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPh TogEn
0x53E	0xB3	RLMS3E[7:0]	ErrChPh SecTA	ErrChPhSec[6:0]						
0x53F	0x72	RLMS3F[7:0]	ErrChPh PriTA	ErrChPhPri[6:0]						
0x549	0x71	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x558	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x559	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x564	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x570	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x571	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x572	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x573	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x574	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x575	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x576	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x595	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x5A4	0xBD	RLMSA4[7:0]*	RSVD_AEQ_PER_MULT[1:0]		RSVD_AEQ_PER[5:0]					
0x5AC	0xCD	RLMSAC[7:0]	ErrChPh SecTAFR3G	ErrChPhSecFR3G[6:0]						
0x5AD	0x0D	RLMSAD[7:0]	ErrChPh PriTAFR3G	ErrChPhPriFR3G[6:0]						
0x5AE	0xCE	RLMSAE[7:0]	ErrChPh SecTAFR1G5	ErrChPhSecFR1G5[6:0]						
0x5AF	0x0F	RLMSAF[7:0]	ErrChPh PriTAFR1G5	ErrChPhPriFR1G5[6:0]						
0x5B0	0xB4	RLMSB0[7:0]	ErrChPh SecTASR1G5	ErrChPhSecSR1G5[6:0]						

ADDRESS	RESET	NAME	MSB							LSB
0x5B1	0x73	RLMSB1[7:0]	ErrChPhPriTASR1G5	ErrChPhPriSR1G5[6:0]						
0x5B2	0xBE	RLMSB2[7:0]	ErrChPhSecTASRG75	ErrChPhSecSRG75[6:0]						
0x5B3	0x7D	RLMSB3[7:0]	ErrChPhPriTASRG75	ErrChPhPriSRG75[6:0]						
0x5B4	0xBC	RLMSB4[7:0]	ErrChPhSecTASRG375	ErrChPhSecSRG375[6:0]						
0x5B5	0x7B	RLMSB5[7:0]	ErrChPhPriTASRG375	ErrChPhPriSRG375[6:0]						
0x5B6	0xBB	RLMSB6[7:0]	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
0x5B7	0x7A	RLMSB7[7:0]	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
DPLL AUD										
0xB00	0xF5	DPLL_0[7:0]*	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
0xB03	0x82	DPLL_3[7:0]*	RSVD	RSVD	RSVD	RSVD	RSVD	config_spread_bit_ratio[2:0]		
DPLL OLDI										
0xD00	0xF5	DPLL_0[7:0]*	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
0xD03	0x82	DPLL_3[7:0]*	RSVD	RSVD	RSVD	RSVD	RSVD	config_spread_bit_ratio[2:0]		
COLOR_A_LUT										
0x1000	0x00	LUT_A_[7:0]	LUT_A_[7:0]							
COLOR_B_LUT										
0x1100	0x00	LUT_B_[7:0]	LUT_B_[7:0]							
COLOR_C_LUT										
0x1200	0x00	LUT_C_[7:0]	LUT_C_[7:0]							

Register Details

REG0 (0x0)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1001000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device Address Default value is set by the ADD[2:0] pins as follows: ADD[2:0] Device Address 000 0b1001000 001 0b1001010 010 0b1001100 011 0b1101000 100 0b1101010 101 0b1101100 110 0b0101000 111 0b0101010	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 ... ... 0b1001000: I²C write/read address is 0x90/0x91 0b1001010: I²C write/read address is 0x94/0x95 0b1001100: I²C write/read address is 0x98/0x99 0b1101000: I²C write/read address is 0xD0/0xD1 0b1101010: I²C write/read address is 0xD4/0xD5 0b1101100: I²C write/read address is 0xD8/0xD9 0b0101000: I²C write/read address is 0x50/0x51 0b0101010: I²C write/read address is 0x54/0x55 ... ... 0b1111111: I²C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.	0b0: Not Blocked 0b1: Blocked

REG1 (0x1)*

BIT	7	6	5	4	3	2	1	0
Field	LVDS_HALFSW	–	IIC_2_EN	IIC_1_EN	TX_RATE[1:0]		RX_RATE[1:0]	
Reset	0x0	–	0x0	0x0	0x0		0x2	
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LVDS_HALFSW	7	LVDS Driver Amplitude Setting	0x0: Full-swing amplitude (350mV typ.) 0x1: Half-swing amplitude (175mV typ.)
IIC_2_EN	5	Enables pass-through I²C Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: Disable pass-through 0b1: Enable pass-through
IIC_1_EN	4	Enables pass-through I²C Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: Disable pass-through 0b1: Enable pass-through
TX_RATE	3:2	Transmitter Rate When changed, becomes active after next link reset.	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE	1:0	Receiver Rate When changed, becomes active after next link reset. Default value is set by CXTP pin at power-up: 6Gbps when CXTP = 1 (coaxial cable) and 3Gbps when CXTP = 0 (twisted-pair cable).	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

REG2 (0x2)*

BIT	7	6	5	4	3	2	1	0
Field	LOCK_CFG	VID_EN	DIS_LOCAL_CC	DIS_REM_CC	–	AUD_TX_EN	RSVD	RSVD
Reset	0b0	0b1	0b0	0b0	–	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_CFG	7	Configures LOCK pin behavior	0b0: GMSL link locked 0b1: GMSL link locked and Video output started
VID_EN	6	Video receive pipeline enable	0b0: Video disabled 0b1: Video enabled
DIS_LOCAL_CC	5	Disables control-channel connection to RX/SDA and TX/SCL pins	0b0: RX/SDA and TX/XCL connected to control channel 0b1: RX/SDA and TX/SCL disconnected from control channel
DIS_REM_CC	4	Disables remote control channel link over GMSL2 connection	0b0: Remote control channel enabled 0b1: Remote control channel disabled
AUD_TX_EN	2	Audio transmit enable over reverse channel	0b0: Audio transmit channel X disabled 0b1: Audio transmit channel X enabled

REG3 (0x3)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RSVD	I2CSEL	UART_2_EN	UART_1_EN	–	VIDEO_LOCK
Reset	0b0	–	0x1	0b0	0x0	0x0	–	0b0
Access Type		–		Write, Read	Write, Read	Write, Read	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
I2CSEL	4	I^2C/UART Selection This bit is set according to the latched I2CSEL pin value at power-up.	0b0: UART 0b1: I^2C
UART_2_EN	3	Enables pass-through UART Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: Disable pass-through 0b1: Enable pass-through
UART_1_EN	2	Enables pass-through UART Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: Disable pass-through 0b1: Enable pass-through
VIDEO_LOCK	0	Indicates whether video channel is locked and outputting valid video data	0b0: Video channel not locked 0b1: Video channel locked

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0x82							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device Identifier	0x82: MAX96752

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				DEV_REV[3:0]			
Reset	0x0				0x01			
Access Type					Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision	0xX: Device revision number

REG15 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	SPEED_CPBL[1:0]		RSVD	DUAL_CPBL	SPLTR_CPBL	RSVD
Reset	0x0	0x0	0x0		0b0	0b0	0b0	0b0
Access Type			Read Only			Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
SPEED_CPBL	5:4	Video Resolution Capability	0b00: No PCLK frequency limit 0b01: Reserved 0b10: Reserved 0b11: Reserved
DUAL_CPBL	2	Dual-Link Capability	0b0: Dual-link mode is available 0b1: Dual-link mode is not available
SPLTR_CPBL	1	Splitter-Mode Capability	0b0: Splitter mode is available 0b1: Splitter mode is not available

IO_CHK0 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x00							
Access Type								

IO_CHK1 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	PIN_DRV_EN_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_DRV_EN_1	7:0	Enables individual pin output buffers and drives the value selected by PIN_DRV_SEL (0x3A) to that pin so that the driven value can be read from the PIN_IN_1 (0x3C) bitfield. This allows testing of IO buffer input and output paths. When the pin is driven using this register, it must not be externally driven by any other strong driver.	[6:0]: Reserved [7]: 0 = Disable GMSL2 output buffer [7]: 1 = Enable GMSL2 output buffer

IO_CHK2 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	PIN_DRV_SEL	–	RSVD[1:0]		RSVD	RSVD	PIN_DRV_EN_2[1:0]	
Reset	0x0	–	0x3		0x0	0x0	0x0	
Access Type	Write, Read	–					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_DRV_SEL	7	Selects polarity for driving dedicated IOs When PIN_DRV_EN = 0, this register is used to enable IO buffer receivers for DEDIO pins.	0b0: Drive low level 0b1: Drive high level
PIN_DRV_EN_2	1:0	Enables individual pin output buffers and drives the value selected by PIN_DRV_SEL (0x3A) to that pin so that the driven value can be read from the PIN_IN_2 (0x3D) bitfield. This allows testing of IO buffer input and output paths. When the pin is driven using this register, it must not be externally driven by any other strong driver.	0bX0: Disable LOCK output buffer 0bX1: Enable LOCK output buffer 0b0X: Disable ERRB output buffer 0b1X: Enable ERRB output buffer

IO_CHK3 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x00							
Access Type								

IO_CHK4 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	PIN_IN_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_IN_1	7:0	Pin Level Readback Each bit contains the level at the pin, either driven externally or by the PIN_DRV_SEL (0x3A) value if the equivalent bit is enabled in the PIN_DRV_EN_1 (0x39) bitfield.	[6:0]: Reserved [7]: GMSL2

PWR0 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:5	Power manager switched 1V supply comparator status bits	0bXX1: Latched high when V_{DD_sw} < 0.82V 0bX1X: Latched high when V_{DD_sw} < 0.82V 0b1XX: Reserved
CMP_STATUS	4:0	Power manager comparator status bits	0bXXXX0: Latched low when V_{DD18} < 1.617V 0bXXX0X: Latched low when switched V_{DDIO} supply < 1.617V 0bXX0XX: Latched low when V_{DD_sw} < 0.802V 0bX0XXX: Reserved 0b0XXXX: Reserved

PWR1 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	OVERTEMP	RSVD	RSVD[5:0]					
Reset	0x0	0x0	0x0					
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
OVERTEMP	7	Temperature Monitor Overtemp Indicator Trip temperature T_{TRIP} set by SET_TEMP1P0[1:0] in CMU6	0x0: T < T_{TRIP} 0x1: T > T_{TRIP}

PWR4 (0xC)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			
Reset	0	0	0x0	0x1	0xA			
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable wake-up by local µC from SDA_RX pin	0b0: Local wake-up enabled 0b1: Local wake-up disabled
WAKE_EN_B	5	Enables wake-up by remote chip connected to Link B	0b0: Link B remote wake-up disabled 0b1: Link B remote wake-up enabled
WAKE_EN_A	4	Enables wake-up by remote chip connected to Link A	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled

CTRL0 (0x10)*

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	–	LINK_CFG[1:0]	
Reset	0b0	0b0	0b0	0b1	0b0	–	0b01	
Access Type	Write, Read	Write, Read	Write Clears All, Read	Write, Read	Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Device Reset Writing 1 to this bit resets the device, returning all blocks and registers to their default values. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset
RESET_LINK	6	Resets the whole data path (keeping register settings) Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT	5	Resets the whole data path (keeps register settings) one shot Write 1 to activate reset. The bit self clears and automatically releases reset.	0b0: No action 0b1: Reset data path
AUTO_LINK	4	Automatically selects which link to enable (A or B) Dual-link and splitter modes are not automatic. For Dual-link mode, set LINK_CFG = 00. For Splitter mode, set LINK_CFG = 11.	0b0: Disable auto link configuration 0b1: Enable auto link configuration
SLEEP	3	Activates Sleep Mode	0b0: Sleep mode disabled 0b1: Sleep mode enabled
LINK_CFG	1:0	AUTO_LINK and this bitfield select the link configuration per the decode table.	0b00: If AUTO_LINK = 0, dual-link is selected. If AUTO_LINK = 1, Link mode is automatically selected. 0b01: If AUTO_LINK = 0, Link A is selected. If AUTO_LINK = 1, Link mode is automatically selected. 0b10: If AUTO_LINK = 0, Link B is selected. If AUTO_LINK = 1, Link mode is automatically selected. 0b11: Splitter mode

CTRL1 (0x11)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	CXTP_B	BACK_COMP_SPLTR	RSVD	RSVD	CXTP_A
Reset	–	–	0b1	0b0	0x0	0x0	0b1	0b0
Access Type	–	–		Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_B	4	Coax/Twisted-Pair Cable Select for Link B Bit is set according to the latched CXTP pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
BACK_COMP_SPLTR	3	Enables Splitter mode compatibility	0b0: Compatibility disabled 0b1: Compatibility enabled
CXTP_A	0	Coax/Twisted-Pair Cable Select for Link A Bit is set according to the latched CXTP pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

CTRL3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	LINK_MODE[1:0]		LOCKED	ERROR	CMU_LOCKED	–
Reset	0	0	0x1		0	0	0	–
Access Type			Read Only		Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_MODE	5:4	Active Link Mode	0b00: Dual-link 0b01: Link A 0b10: Link B 0b11: Splitter mode
LOCKED	3	GMSL2 Link Locked (bidirectional)	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects Error Status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock Multiplier Unit (CMU) Lock Status	0b0: CMU not locked 0b1: CMU locked

INTR0 (0x18)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	0x1	0x0	0x1	–	0	0x0		
Access Type				–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A (0x22), DEC_ERR_B (0x23), and IDLE_ERR (0x24) registers after ERRB pin is asserted for 1µs	0b0: Auto-reset disabled 0b1: Auto-reset enabled
DEC_ERR_THR	2:0	Decoding and Idle-Error Reporting Threshold DEC_ERR_FLAG_A (0x1B) is asserted when DEC_ERR_A (0x22) ≥ DEC_ERR_THR DEC_ERR_FLAG_B (0x1B) is asserted when DEC_ERR_B (0x23) ≥ DEC_ERR_THR IDLE_ERR_FLAG is asserted when IDLE_ERR (0x24) ≥ DEC_ERR_THR	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

INTR1 (0x19)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0x0				0	0x0		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet Count Multiplier Exponent See the description of PKT_CNT register.	0bXXX: PKT_CNT exponent
AUTO_CNT_RST_EN	3	Automatically resets PKT_CNT (register 0x25) after ERRB pin is asserted for 1µs	0b0: Auto-reset disabled 0b1: Auto-reset enabled
PKT_CNT_THR	2:0	Packet Count Reporting Threshold (see PKT_CNT (0x25) description) PKT_CNT_FLAG (0x1D) is asserted when PKT_CNT ≥ PKT_CNT_THR.	0b000: 1 0b001: 2 0b010: 4 0b011: 8 0b100: 16 0b101: 32 0b110: 64 0b111: 128

INTR2 (0x1A)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_OEN	RSVD	RSVD	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0	0	0	0x0	0x0	0	1	1
Access Type			Write, Read			Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_OEN	5	Enables reporting of remote-error status (REM_ERR) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
IDLE_ERR_OEN	2	Enables reporting of idle word errors (IDLE_ERR_FLAG - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_OEN_B	1	Enables reporting of decoding errors (DEC_ERR_FLAG_B - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enables reporting of decoding errors (DEC_ERR_FLAG_A - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_FLAG	RSVD	RSVD	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0	0	0	0	0	0	0	0
Access Type			Read Only			Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_FLAG	5	Received remote side error status (inverse of remote side ERRB pin level)	0b0: No remote side error 0b1: Remote side error
IDLE_ERR_FLAG	2	Idle-Word Error Flag Asserted when IDLE_ERR (0x1C) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_B	1	Decoding Error Flag for Link B Asserted when DEC_ERR_B (0x1B) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_A	0	Decoding Error Flag for Link A Asserted when DEC_ERR_A (0x1A) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted

INTR4 (0x1C)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	EOM_ERR_OEN_A	–	RSVD	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
Reset	0	0	–	0	1	0	0	1
Access Type		Write, Read	–		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_A	6	Enable reporting of Eye-Opening Monitor error (EOM_ERR_FLAG_A) for Link A at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enables reporting of combined ARQ re-transmission event flag (RT_CNT_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enables reporting of packet count flag (PKT_CNT_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
WM_ERR_OEN	0	Enables reporting of watermark errors (WM_ERR_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	–	RSVD	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
Reset	0	0	–	0	0	0	0	0
Access Type	Read Only	Read Only	–		Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_B	7	Eye-Opening is below configured threshold for Link B.	0b0: No EOM error on Link B 0b1: EOM error on Link B
EOM_ERR_FLAG_A	6	Eye-Opening is below configured threshold for Link A.	0b0: No EOM error on Link A 0b1: EOM error on Link A
MAX_RT_FLAG	3	Combined ARQ Maximum Retransmission Limit Error Flag Asserted when any of the selected channels' ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN (0x1C) register bit.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG	2	Combined ARQ Retransmission Event Flag Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN register bit.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet Count Flag Asserted when PKT_CNT (0x1D) ≥ PKT_CNT_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted
WM_ERR_FLAG	0	Watermark Error Flag Asserted when a watermark error is detected.	0b0: Flag not asserted 0b1: Flag asserted

INTR6 (0x1E)*

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	VDD_OV_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	APRBS_ERR_OEN	VID_PXL_CRC_ERR_OEN
Reset	0b0	0b0	0b0	0x0	1	1	1	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	7	Enables reporting of V_{DDCMP} interrupt (VDDCMP_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_INT_OEN	5	Enables reporting of V_{DDBAD} interrupt (VDDBAD_INT_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VDD_OV_OEN	4	Enables V_{DD} overvoltage status on ERRB	0b0: Do not enable V_{DD} overvoltage status 0b1: Enable V_{DD} overvoltage status
LCRC_ERR_OEN	3	Enables reporting of video line CRC errors (LCRC_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VPRBS_ERR_OEN	2	Enables reporting of video PRBS errors (VPRBS_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
APRBS_ERR_OEN	1	Enables reporting of audio PRBS errors (APRBS_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VID_PXL_CRC_ERR_OEN	0	Enables reporting of video pixel CRC errors (VID_PXL_CRC_ERR_FLAG - 0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	VDD_OV_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	APRBS_ERR_FLAG	VID_PXL_CRC_ERR_FLAG
Reset	0	0	0	0x0	0	0	0	0x0
Access Type	Read Clears All		Read Clears All	Read Clears All	Read Clears All	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	7	V_{DDCMP} Interrupt Flag	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	5	V_{DDBAD} Status Interrupt Flag	0b0: Flag not asserted 0b1: Flag asserted
VDD_OV_FLAG	4	V_{DD} Overvoltage Indication Flag This bit stays high when asserted and must be cleared by the user. It is set when V_{DD} exceeds the overvoltage threshold. It is cleared when read. See OV_LEVEL (0x25D) bitfield for overvoltage threshold value.	0x0: V_{DD} overvoltage not detected 0x1: V_{DD} overvoltage detected
LCRC_ERR_FLAG	3	Video Line CRC Error Flag. Read this bit to clear. Asserted when a video line CRC error is detected.	0b0: Flag not asserted 0b1: Flag asserted
VPRBS_ERR_FLAG	2	Video PRBS Error Flag Asserted when VPRBS_ERR > 0.	0b0: Flag not asserted 0b1: Flag asserted
APRBS_ERR_FLAG	1	Audio PRBS Error Flag Asserted when APRBS_ERR > 0.	0b0: Flag not asserted 0b1: Flag asserted
VID_PXL_CRC_ERR_FLAG	0	Video Pixel CRC Error Flag. Read VID_PXL_CRC_ERR to clear. Asserted when video pixel CRC error count > 0.	0b0: Flag not asserted 0b1: Flag asserted

INTR8 (0x20)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0	–	–	0x1F				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmit local error status (inverse of ERRB pin level) to remote side through GPIO channel	0b0: Transmit error status disabled 0b1: Transmit error status enabled
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX	0bXXXXX: Value of GPIO ID for transmitting ERR_TX

INTR9 (0x21)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
Reset	0	1	–	0x1F				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Receive remote error status (inverse of ERRB pin level) through GPIO channel	0b0: Receive error status disabled 0b1: Receive error status enabled
ERR_RX_ID	4:0	GPIO ID used for receiving ERR_RX	0bXXXXX: Value of GPIO ID for receiving ERR_RX

CNT0 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	Number of decoding (disparity) errors detected at Link A. Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

CNT2 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of idle-word errors detected. Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT3 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of received packets of a selected type. Packet type is selected with PKT_CNT_SEL (0x2C) register. Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT x ($2^{PKT_CNT_EXP}$) and < (PKT_CNT + 1) x ($2^{PKT_CNT_EXP}$). When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

CNT4 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR	7:0	Number of video pixel CRC errors detected at video stream Reset after each Read operation or with the rising edge of LOCK.	0bXXXXXXXX: Number of video pixel CRC errors detected

TX1 (0x29)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_GEN	–	ERRG_EN_B	ERRG_EN_A	–	–	RSVD	RSVD
Reset	0	–	0	0	–	–	0	0
Access Type	Write, Read	–	Write, Read	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_GEN	7	Enables Link PRBS-7 generator	0b0: Link PRBS generator disabled 0b1: Link PRBS generator enabled
ERRG_EN_B	5	Error Generator Enable for Link B	0b0: Link B error generator disabled 0b1: Link B error generator enabled
ERRG_EN_A	4	Error Generator Enable for Link A	0b0: Link A error generator disabled 0b1: Link A error generator enabled

TX2 (0x2A)*

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0x0		0x2		0x0			0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error Generator Average Bit-Error Rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits
ERRG_BURST	3:1	Selects the error generator burst-error length in bits. For example, if the bitfield value is 0b100, the burst-error length is 8 bits. Thus, each time an 8-bit error burst is generated, there is an error in the first and the last bit of the 8-bit window and the probability of an error in each of the remaining 6 bits is 50%.	0b000: 1 bit 0b001: 2 bits 0b010: 3 bits 0b011: 4 bits 0b100: 8 bits 0b101: 12 bits 0b110: 16 bits 0b111: 20 bits
ERRG_PER	0	Error Generator Error Distribution Selection	0b0: Pseudo random 0b1: Periodic

TX3 (0x2B)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
Reset	0x1		–	–	–	0b100		
Access Type			–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	ARQ Timeout Duration Multiplier Multiplies a timeout base constant to set the ARQ timeout. The timeout base is set by the reverse channel link rate (RX_RATE) as follows: RX_RATE Timeout base 187.5Mbps 8µs	0b000: 0.5 x timeout base 0b001: 1.0 x timeout base 0b010: 1.5 x timeout base 0b011: 2.0 x timeout base 0b100: 2.5 x timeout base 0b101: 3.0 x timeout base 0b110: 3.5 x timeout base 0b111: 4.0 x timeout base

RX0 (0x2C)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
Reset	0x0		–	0	0x0			
Access Type	Write, Read		–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Select the subtype of low bandwidth (LBW) packets to count at PKT_CNT(0x1D) bitfield	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Select the type of received packets to count at PKT_CNT (0x1D) bitfield	0x0: None 0x1: VIDEO 0x2: AUDIO 0x3: INFO Frame 0x4: SPI 0x5: I^2C 0x6: UART 0x7: GPIO 0x8: Reserved 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All 0xF: Unknown and packets with error

GPIOA (0x30)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0x0	0b1	0x01					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_FAST_BIDIR_EN	7	GPIO fast-direction switch for bidirectional IO	0b0: Fast-direction switch disabled 0b1: Fast-direction switch enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction This must be same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x31)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0x2		0x08					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet This allows grouping transitions of different GPIO inputs in a single packet, increasing GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

I2C_0 (0x40)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I^2C-to-I^2C subordinate-setup and hold-time setting Configures the interval between SDA and SCL transitions when driven by the internal I^2C subordinate.	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C Standard-mode speed 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO	2:0	I²C-to-I²C subordinate Timeout Setting Internal GMSL2 I²C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x41)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	0b0	0x5			–	0b110		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	I²C-to-I²C Main Bit Rate Setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). Set this according to the I²C Speed mode.	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO	2:0	I²C-to-I²C Main Timeout Setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x42)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I^2C address translator source A When I^2C device address matches I^2C SRC_A, internal I^2C main (on remote side) replaces the device address by I^2C DST_A.	0bXXXXXXX: Value of I^2C SRC_A

I2C_3 (0x43)*

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I^2C address translator destination A See the description of I^2C SRC_A.	0bXXXXXXX: Value of I^2C DST_A

I2C_4 (0x44)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I^2C address translator source B When I^2C device address matches I^2C SRC_B, internal I^2C Main (on remote side) replaces the device address by I^2C DST_B.	0bXXXXXXX: Value of I^2C SRC_B

I2C_5 (0x45)*

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I^2C address translator destination B See the description of I^2C SRC_B.	0bXXXXXXX: Value of I^2C DST_B

I2C_6 (0x46)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	I2C_AUTO_CFG	I2C_SRC_CNT[2:0]		
Reset	–	–	–	–	0x1	0b0		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_AUTO_CFG	3	When this bit = 1, I^2C-to-I^2C number of links is determined based on Splitter mode automatically. In Splitter mode, a response from two I^2C channels is expected; otherwise, a response from one I^2C channel is expected.	0b0: Number of I^2C-to-I^2C links set by I2C_SRC_CNT[2:0] bits 0b1: Splitter mode automatically determines the number of I^2C-to-I^2C links
I2C_SRC_CNT	2:0	I^2C-to-I^2C number of links (valid when I2C_AUTO_SRC = 0). Set this to N - 1 when expecting I^2C response from N remote I^2C transmitters (usually the same as the number of remote devices connected to this device).	0b000: One deserializer connected 0b001: Two deserializers connected 0b010: Reserved 0b011: Reserved 0b100: Reserved 0b101: Reserved 0b110: Reserved 0b111: Reserved

I2C_7 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
Reset	0x0	0x0	–	–	–	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	–	–	–	Read Clears All	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
UART_RX_OVERFLOW	7	UART Rx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred
UART_TX_OVERFLOW	6	UART Tx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred
I2C_TIMED_OUT	2	Indicates whether internal I^2C-to-I^2C subordinate or main has timed out while receiving packet from remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED	1	Inverse of the I^2C acknowledge bit received from remote side	0x0: I^2C acknowledge bit received as 1 0x1: I^2C acknowledge bit received as 0
REM_ACK_RECVED	0	I^2C acknowledge bit for any I^2C byte is received from remote side for the previous I^2C packet	0b0: I^2C acknowledge bit not received 0b1: I^2C acknowledge bit received

UART_0 (0x48)*

BIT	7	6	5	4	3	2	1	0
Field	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	0x1		0b0	0b0	0b0	0x1		0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ARB_TO_LEN	7:6	UART Rx source arbitration timeout duration UART Rx processes packets from a single UART source at any time. When UART Rx does not receive any UART packets for this duration, it selects the next UART source according to the source ID of the next following received packet.	0b00: 1ms 0b01: 2ms 0b10: 8ms 0b11: 32ms
REM_MS_EN	5	Enables UART Bypass mode control by remote GPIO pin When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in Bypass mode; otherwise, chip is in Base mode.	0b0: UART Bypass mode not controlled by remote MS pin 0b1: UART Bypass mode controlled by remote MS pin
LOC_MS_EN	4	Enables UART Bypass mode control by local GPIO pin Set to use GPIO2 pin as MS pin (UART mode select). When MS is high, chip is in Bypass mode; otherwise, chip is in Base mode.	0b0: UART Bypass mode not controlled by local MS pin 0b1: UART Bypass mode controlled by local MS pin
BYPASS_DIS_PAR	3	Selects whether to receive and send parity bit in Bypass mode	0b0: Receive and send parity bit in Bypass mode 0b1: Do not receive and send parity bit in Bypass mode
BYPASS_TO	2:1	UART soft-bypass timeout duration	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Reserved
BYPASS_EN	0	Enables UART Soft-bypass mode Bypass mode remains active as long as there is UART activity. When there is no UART activity for the selected duration (configured by BYPASS_TO bitfield), the device exits Bypass mode, and the bit is automatically cleared.	0b0: UART Soft-bypass mode disabled 0b1: UART Soft-bypass mode enabled

UART_1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB[7:0]							
Reset	0x96							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB	7:0	UART detected bit length in terms of internal 150MHz clock (LSB)	0xXX: UART detected bit length (LSB)

UART_2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
Reset	0x2		0x00					
Access Type	Write, Read		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_DELAY	7:6	UART Initial Output Delay In Base mode, the first received UART byte of a packet (sync or acknowledge frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back-to-back on the remote side.	0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit
BITLEN_MSB	5:0	UART detected bit length in terms of internal 150MHz clock (6 MSbs)	0bXXXXXX: UART detected bit length (6 MSbs)

I2C_PT_0 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_PT	5:4	Pass-through I^2C-to-I^2C subordinate setup and hold time setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I^2C subordinate. Set according to the I^2C Speed mode shown in the decode table.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: NA
SLV_TO_PT	2:0	Pass-through I^2C-to-I^2C subordinate timeout setting Internal GMSL2 I^2C subordinate times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0bXXX: Subordinate timeout duration

I2C_PT_1 (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	MST_DBL_PT	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type	Write, Read	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_DBL_PT	7	Doubles the pass-through I²C-to-I²C main bit rate (MST_BT)	0x0: Do not double the pass-through I²C-to-I²C main bit rate 0x1: Double the pass-through I²C-to-I²C main bit rate
MST_BT_PT	6:4	Pass-through I²C-to-I²C main bit rate setting Configures the I²C bit rate used by the internal I²C main (in the device on the remote side from the external I²C main). Set according to the I²C Speed mode shown in the decode table. Fast-mode Plus = 101 to 111 Fast-mode = 010 to 100 Standard mode = 000 to 001	0b00x: Standard mode 0b01x: Fast-mode 0b100: Fast-mode 0b101: Fast-mode Plus 0b11x: Fast-mode Plus
MST_TO_PT	2:0	Pass-through I²C-to-I²C main timeout setting Internal GMSL2 I²C main times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	

I2C_PT_2 (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Read Clears All	Read Only	Read Only	Write, Read	Read Clears All	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
XOVER_EN_2	7	Connect pass-through I²C/UART Channel 2 to primary control channel on the remote side	0x0: Do not connect pass-through I²C/UART Channel 2 to primary control channel 0x1: Connect pass-through I²C/UART Channel 2 to primary control channel
I2C_TIMED_OUT_2	6	Indicates that, in pass-through I²C Channel 2, internal I²C-to-I²C subordinate or main has timed out while receiving packet from the remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED_2	5	Indicates that, in pass-through I²C Channel 2, inverse of the I²C acknowledge bit was received from the remote side	0x0: I²C acknowledge bit received as 1 0x1: Inverse I²C acknowledge bit received as 0

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ACK_RECVED_2	4	Indicates that, in pass-through I²C Channel 2, I²C acknowledge bit for any I²C byte was received from the remote side for the previous I²C packet	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received
XOVER_EN_1	3	Connects pass-through I²C/UART Channel 1 to primary control channel on the remote side	0x0: Do not connect pass-through I²C/UART Channel 1 to primary control channel 0x1: Connect pass-through I²C/UART Channel 1 to primary control channel
I2C_TIMED_OUT_1	2	Indicates that, in pass-through I²C Channel 1, internal I²C-to-I²C subordinate or main has timed out while receiving packet from the remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED_1	1	Indicates that, in pass-through I²C Channel 1, inverse of the I²C acknowledge bit was received from the remote side	0x0: I²C acknowledge bit received as 1 0x1: I²C acknowledge bit received as 0
REM_ACK_RECVED_1	0	Indicates that, in pass-through I²C Channel 1, I²C acknowledge bit for any I²C byte was received from the remote side for the previous I²C packet	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received

UART_PT_0 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Read Clears All	Read Clears All	Write, Read	Write, Read	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Enables the use of custom UART bit rate (BITLEN_PT_1 register) in pass-through UART Channel 2	0x0: Do not use custom UART bit rate in pass-through UART Channel 2 0x1: Use custom UART bit rate in pass-through UART Channel 2
DIS_PAR_2	6	Disables parity bit in pass-through UART Channel 2	0x0: Enable parity bit in pass-through UART Channel 2 0x1: Do not enable parity bit in pass-through UART Channel 2
UART_RX_OVERFLOW_2	5	Pass-Through UART Rx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred
UART_TX_OVERFLOW_2	4	Pass-Through UART Tx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred
BITLEN_MAN_CFG_1	3	Selects whether or not to use custom UART bit rate (BITLEN_PT_1 register) in pass-through UART Channel 1	0x0: Do not use custom UART bit rate in pass-through UART Channel 1 0x1: Use custom UART bit rate in pass-through UART Channel 1
DIS_PAR_1	2	Disables parity bit in pass-through UART Channel 1	0x0: Enable parity bit in pass-through UART Channel 1 0x1: Do not enable parity bit in pass-through UART Channel 1
UART_RX_OVERFLOW_1	1	Pass-Through UART Rx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred

BITFIELD	BITS	DESCRIPTION	DECODE
UART_TX_OVERFLOW_1	0	Pass-Through UART Tx FIFO Overflow	0x0: No overflow occurred 0x1: Overflow occurred

RX0 (0x50)*

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0x0	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	Receive Packet CRC Enable	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Receive Packets with Selected stream ID	0bXX: Receive packets with this stream ID

TR0 (0x58, 0x60, 0x68, 0x78, 0xA0, 0xA8)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x59, 0x61, 0x69, 0x71, 0x79, 0xA1, 0xA9)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x5B, 0x63, 0x6B, 0x73, 0x7B, 0xA3, 0xAB)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x1	–	0x0		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	Selects whether or not packets are transmitted over GMSLB in Splitter mode When 0, packets from this port are not transmitted from Port B; otherwise, packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in splitter mode 0b1: Packets are transmitted over GMSLB in splitter mode
TX_SPLT_MASK_A	4	Selects whether or not packets are transmited over GMSLB in Splitter mode. When 0, packets from this port are not transmitted from Port A; otherwise, packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in splitter mode 0b1: Packets are transmitted over GMSLA in splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value is set by ADD2, ADD1 and ADD0.	0bXXX: Source ID for packets from this channel

TR4 (0x5C, 0x64, 0x6C, 0x74, 0x7C, 0xA4, 0xAC)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x5D, 0x6D, 0x75, 0x7D, 0xA5, 0xAD)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	RSVD	–	–	–
Reset	0x1	0x0	0x0	0x1	0x1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	Selects what values ARQ settings are based on When this bit = 1, ARQ settings are automatically selected based on Splitter mode	0b0: ARQ settings are based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID bitfield
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register

ARQ1 (0x5E, 0x6E, 0x76, 0x7E, 0xA6, 0xAE)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum Retransmission Limit ARQ stops retransmitting after "X" number of retransmission attempts for a single packet. Where "X" represents the decimal value assigned to these 3 bits (up to 7).	0bXXX: Maximum retransmission limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR - ARQ2 register) for this channel at ERRB pin.	0b0: ARQ maximum retransmission limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmission limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x5F, 0x6F, 0x77, 0x7F, 0xA7, 0xAF)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0x0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT - ARQ1 register) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

TR0 (0x70)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC, and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

VIDEO_RX0 (0x100)*

BIT	7	6	5	4	3	2	1	0
Field	LCRC_ERR	RSVD	RSVD	RSVD	RSVD	RSVD	LINE_CRC_EN	RSVD
Reset	0x0	0b0	0b1	0b1	0b0	0b0	0b1	0x0
Access Type	Read Clears All						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR	7	Video Line CRC Error Flag. Read LCRC_ERR_FLAG register at 0x1F to clear.	0b0: No video line CRC detected 0b1: Video line CRC detected
LINE_CRC_EN	1	Video Line CRC enable	0b0: Video line CRC disabled 0b1: Video line CRC enabled

VIDEO_RX3 (0x103)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
Reset	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type		Write, Read	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HD_TR_MODE	6	HS, DE Tracking enable full periodic pattern	0b0: Allow only partial periodic HS, DE 0b1: Allow partial periodic and full periodic HS, DE
DLOCKED	5	DE Tracking Locked	0b0: DE tracking not locked 0b1: DE tracking locked
VLOCKED	4	VS Tracking Locked	0b0: VS tracking not locked 0b1: VS tracking locked
HLOCKED	3	HS Tracking Locked	0b0: HS tracking not locked 0b1: HS tracking locked
DTRACKEN	2	DE Tracking Enable (disabled if FSYNC = 1) The system observes DE pulses and can compensate for a limited number of missing pulses or suppress glitches when it locks on the pattern.	0b0: DE tracking disabled 0b1: DE tracking enabled
VTRACKEN	1	VS Tracking Enable (disabled if FSYNC = 1) The system observes VS pulses and can compensate for a limited number of missing pulses or suppress glitches when it locks on the pattern.	0b0: VS tracking disabled 0b1: VS tracking enabled

BITFIELD	BITS	DESCRIPTION	DECODE
HTRACKEN	0	HS Tracking Enable (disabled if FSYNC = 1) The system observes HS pulses and can compensate for a limited number of missing pulses or suppress glitches when it locks on the pattern.	0b0: HS tracking disabled 0b1: HSYNC tracking enabled

VIDEO_RX4 (0x104)

BIT	7	6	5	4	3	2	1	0
Field	VID_OVERFLW_LIM_L[7:0]							
Reset	0x0C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_OVERFLW_LIM_L	7:0	Lower byte of 9-bit video FIFO overflow threshold during lock	0xXX: Video FIFO overflow threshold during lock (LSB)

VIDEO_RX5 (0x105)

BIT	7	6	5	4	3	2	1	0
Field	VID_UNDERFLW_LIM_L[7:0]							
Reset	0xD0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_UNDERFLW_LIM_L	7:0	Lower byte of 9-bit video FIFO underflow threshold during lock	0xXX: Video FIFO underflow threshold during lock (LSB)

VIDEO_RX6 (0x106)

BIT	7	6	5	4	3	2	1	0
Field	VID_SAR_INC_H[2:0]			–	–	–	VID_UNDERFLW_LIM_H	VID_OVERFLW_LIM_H
Reset	0x0			–	–	–	0b1	0b0
Access Type	Write, Read			–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VID_SAR_INC_H	7:5	Upper bits of 10-bit video clock regeneration SAR start point	0bXXX: Video clock regeneration SAR start point (3 MSbs)
VID_UNDERFLW_LIM_H	1	Upper bit of 9-bit video FIFO underflow threshold during lock	0bX: Video FIFO underflow threshold during lock (MSb)
VID_OVERFLW_LIM_H	0	Upper bit of 9-bit video FIFO overflow threshold during lock	0bX: Video FIFO overflow threshold during lock (MSb)

VIDEO_RX7 (0x107)

BIT	7	6	5	4	3	2	1	0
Field	VID_SAR_INC_L[7:0]							
Reset	0x40							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_SAR_INC_L	7:0	Lower byte of 10-bit video clock regeneration SAR start point	0xXX: Video clock regeneration SAR start point (LSB)

VIDEO_RX8 (0x108)

BIT	7	6	5	4	3	2	1	0
Field	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x2			
Access Type	Read Clears All	Read Only	Read Only	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
VID_BLK_LEN_ERR	7	Video Rx Block Length Error Detection	0b0: No error detected 0b1: Video Rx block length error detected
VID_LOCK	6	Video Pipeline Locked	0b0: Video pipeline not locked 0b1: Video pipeline locked
VID_PKT_DET	5	Sufficient Video Rx Packet Throughput Detected	0b0: Not enough throughput 0b1: Sufficient throughput detected
VID_SEQ_ERR	4	Video Rx Sequence Error Detection	0b0: No error detected 0b1: Error detected

VIDEO_RX10 (0x10A)

BIT	7	6	5	4	3	2	1	0
Field	–	MASK_VIDEO_DE	RSVD[5:0]					
Reset	–	0x0	0x00					
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
MASK_VIDEO_DE	6	Mask Video with DE	0x0: Do not mask video with DE 0x1: Mask video with DE

CLOCKGEN (0x111)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CLK_FREEZE_RNG[1:0]		CLK_FREEZE_CONS	CLK_FREEZE
Reset	–	–	–	–	0x0		0b0	0b0
Access Type	–	–	–	–	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CLK_FREEZE_RNG	3:2	Selects the frequency when outputting a preset clock frequency on Tx clock outputs	0b00: 50MHz 0b01: 100MHz 0b10: 200MHz 0b11: 300MHz
CLK_FREEZE_CONS	1	Selects Tx clock output when video not locked and enabled by CLK_FREEZE	0b0: Output last clock frequency 0b1: Output frequency selected by CLK_FREEZE_RNG
CLK_FREEZE	0	Selects whether or not to always output video clock on Tx clock outputs even when receiver is not locked	0b0: Tx clock outputs disabled when video not locked 0b1: Always output video clock

AUDIO_TX0 (0x120)*

BIT	7	6	5	4	3	2	1	0
Field	I2S_TDM_CFG[1:0]		I2S_CFG[1:0]		INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
Reset	0x2		0x3		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2S_TDM_CFG	7:6	Audio Format Configuration	0b00: Force stereo 0b01: Force TDM 0b10: Auto select stereo or TDM 0b11: Reserved
I2S_CFG	5:4	Audio Channel Configuration Must be set the same on both I^2S Tx adapters.	0b00: Reserved 0b01: Reserved 0b10: Reserved 0b11: Use local I^2S input pins as audio source
INV_SCK	3	Inverts SCK (when using local I^2S interface)	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS	2	Inverts WS (when using local I^2S interface)	0b0: Do not invert WS 0b1: Invert WS
FORCE_AUD	1	Forces Audio Data to Zero	0b0: Normal audio data 0b1: Audio data forced to zero
AUD_SINK_SRC	0	Sink-Sourced Mode Enable for Audio TX For use on the deserializer side when forward audio channel clock is used as the main audio clock.	0b0: Transmit audio in Normal mode 0b1: Transmit audio in Sink-sourced mode

AUDIO_TX1 (0x121)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_PRIO[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	RSVD[1:0]	
Reset	0x1		0x0		0b1	0b1	0x2	
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_PRIO	7:6	Scheduler Audio Priority	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 3
AUD_STR_TX	5:4	Audio Stream ID	0b00: Use stream ID 0 0b01: Use stream ID 1 0b10: Use stream ID 2 0b11: Use stream ID 3
AUD_DRIFT_DET_EN	3	Audio Clock Drift Detection Enable Resets subsystem on SCK frequency drift and reports it.	0b0: Audio clock drift detection disabled 0b1: Audio clock drift detection enabled
AUD_INF_PER	2	Audio Periodic Information Frame Transmission Enable	0b0: Audio periodic information frame transmission disabled 0b1: Audio periodic information frame transmission enabled

AUDIO_TX5 (0x125)

BIT	7	6	5	4	3	2	1	0
Field	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_DRIFT_ERR	7	Indicates whether audio clock frequency drift is detected	0b0: Audio clock frequency drift not detected 0b1: Audio clock frequency drift detected
AUD_FIFO_WARN	6	Indicates whether audio FIFO is more than half full	0b0: Audio FIFO is less than or equal to half full 0b1: Audio FIFO is more than half full
AUD_OVERFLOW	5	Indicates whether audio buffer overflow is detected	0b0: Audio buffer overflow not detected 0b1: Audio buffer overflow detected
ACLKDET	4	Audio Clock Detect	0b0: Audio clock not detected 0b1: Audio clock detected

AUDIO_TX7 (0x127)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
Reset	0b0	0b0	0x0					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_SEL	7	Audio PRBS clock selection (program to 0 in Sink-sourced mode)	0b0: SCK selected 0b1: Internal oscillator clock selected (150MHz)
PRBSEN_AUD	6	Audio PRBS Enable	0b0: Audio PRBS disabled 0b1: Audio PRBS enabled

AUDIO_TX8 (0x128)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
Reset	0b0	0b1	0x0					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_WS_LEN	7	Selects the length of the generated WS pulse	0b0: 256 data bits per WS cycle 0b1: 32 data bits per WS cycle
PRBS_WS_GEN	6	Audio PRBS WS generation enable	0b0: Audio PRBS WS generation disabled 0b1: Audio PRBS WS generation enabled

AUDIO_RX1 (0x140)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
Reset	0b0	0b0	0b1	0b0	0b0	0b0	–	0b1
Access Type	Write, Read				Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_RX_SINK_SRC	7	Sink-sourced mode enable for audio Rx (for use on the serializer side)	0b0: Received audio in Normal mode 0b1: Received audio in Sink-sourced mode
INV_SCK_RX	3	Inverts SCK at I^2S output	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS_RX	2	Inverts WS at I^2S output	0b0: Do not invert WS 0b1: Invert WS
AUD_EN_RX	0	Audio Receiver Adapter Enable	0b0: Audio receiver disabled 0b1: Audio receiver enabled

AUDIO_RX4 (0x143)

BIT	7	6	5	4	3	2	1	0
Field	APRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_ERR	7:0	Audio PRBS Error Counter Clears on read.	0xXX: Number of audio PRBS errors

AUDIO_RX7 (0x146)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
Reset	0x0			0b0	0x0		0b1	0b0
Access Type				Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_CHK_EN	4	Enable Audio PRBS Checker	0b0: Audio PRBS checker disabled 0b1: Audio PRBS checker enabled
AUD_STRM	3:2	Selects audio stream for reception	0b00: Receive stream ID 0 0b01: Receive stream ID 1 0b10: Receive stream ID 2 0b11: Receive stream ID 3

AUDIO_RX9 (0x148)

BIT	7	6	5	4	3	2	1	0
Field	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Read Clears All	Read Only	Read Only	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_BLK_LEN_ERR	7	Indicates whether or not audio Rx block length error is detected	0b0: Received audio block length error not detected 0b1: Received audio block length error detected
AUD_LOCK	6	Indicates whether or not audio pipeline frequency is locked	0b0: Audio pipeline frequency is not locked 0b1: Audio pipeline frequency is locked
AUD_PKT_DET	5	Indicates whether or not sufficient audio Rx packet throughput is detected	0b0: Valid audio stream not detected 0b1: Valid audio stream detected
APRBS_VALID	4	Indicates whether or not audio PRBS is running	0b0: Audio PRBS is not running 0b1: Audio PRBS is running

INFO_RX4 (0x14D)

BIT	7	6	5	4	3	2	1	0
Field	–	INFO_AUD_DEPTH[6:0]						
Reset	–	0x00						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
INFO_AUD_DEPTH	6:0	Received audio depth value from info frames

SPI_0 (0x160)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0x0		0x0		0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Programs to local ID if filtering packets based on header ID	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_CC_TRG_ID	5:4	ID for GMSL2 header in SPI control-channel bridge mode	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_IGNR_ID	3	Selects if SPI should use or ignore header ID to determine packet acceptance	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_CC_EN	2	Enables control channel SPI bridge function	0b0: SPI bridge disabled 0b1: SPI bridge enabled
MST_SLVN	1	Selects if SPI is main or subordinate.	0b0: SPI subordinate 0b1: SPI main
SPI_EN	0	Enables SPI channel	0b0: SPI channel disabled 0b1: SPI channel enabled

SPI_1 (0x161)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
Reset	0x07						0x1	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Sets the packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value greater than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes ... ... 0b111111: Packet size is 127 bytes

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_BASE_PRIO	1:0	Starting GMSL2 request priority Advances by 1 (space permitting) if Tx buffer is over half full.	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 3

SPI_2 (0x162)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0x0			0x0	0x0	0x0	0x1	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Hold off GMSL2 request until this number of extra bytes is received on SPI port	0b000: Request after every byte received 0b001: Request after 2 bytes received 0b010: Request after 3 bytes received ... ... 0b111: Request after 8 bytes received
FULL_SCK_SETUP	4	Sample MISO after half- or full-SCK period	0b0: MISO sampled after half SCK period 0b1: MISO sampled after full SCK period
SPI_MOD3_F	3	Allows the suppression of an extra SCK prior to SS deassertion when SPI mode 3 is selected	0b0: Extra SCK present prior to SS deassertion when in SPI mode 3 0b1: Extra SCK suppressed prior to SS deassertion when in SPI mode 3
SPI_MOD3	2	Selects SPI mode 0 or 3	0b0: SPI mode 0 0b1: SPI mode 3
SPIM_SS2_ACT_H	1	Sets the polarity for SS2 when the SPI is a main.	0b0: Subordinate select 2 is active low 0b1: Subordinate select 2 is active high
SPIM_SS1_ACT_H	0	Sets the polarity for SS1 when the SPI is a main.	0b0: Subordinate select 1 is active low 0b1: Subordinate select 1 is active high

SPI_3 (0x163)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between each of the following: – Assertion of SS and start of SCK pulses – End of SCK pulses and deassertion of SS – Deassertion of SS and reassertion of SS, if necessary	0xXX: Number of clock delays

SPI_4 (0x164)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time	0xXX: Number of clocks for SCK low time

SPI_5 (0x165)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time	0xXX: Number of clocks for SCK high time

SPI_6 (0x166)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	Alternate GPU status register to use for BNE status if GPIO is not available	0b0: Buffer empty 0b1: Buffer not empty
SPIS_RWN	4	Alternate GPU Control register to use for Read/Write control if GPIO is not available.	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enables GPIO for use as Subordinate Select 2 output.	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
SS_IO_EN_1	2	Enables GPIO for use as Subordinate Select 1 output	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
BNE_IO_EN	1	Enables GPIO for use as BNE output for SPI data available status	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function
RWN_IO_EN	0	Enables GPIO for use as RO input for control of SPI data movement	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function

SPI_7 (0x167)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
Reset	0b0	0b0	–	0x0				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	SPI Rx Buffer Overflow Flag	0b0: No SPI Rx buffer overflow 0b1: SPI Rx buffer overflow
SPI_TX_OVRFLW	6	SPI Tx Buffer Overflow Flag	0b0: No SPI Tx buffer overflow 0b1: SPI Tx buffer overflow
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer	0bXXXXX: Number of bytes available

SPI_8 (0x168)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100nS increments) for GMSL2 request hold-off (0 is disable).	0xXX: Number of 100nS delay increments for GMSL2 request hold-off

WM_0 (0x188)*

BIT	7	6	5	4	3	2	1	0
Field	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		WME_EN	WM_EN
Reset	0b0	0x0			0x0		0x0	0b0
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_LEN	7	Watermark Length	0b0: 32-bit 0b1: 64-bit
WM_MODE	6:4	Watermark Mode	0b000: Default generator mode - cycle through all 4 watermarks in video stream 0b001: Error generator mode - cycle through only 2 watermarks to replicate a frozen frame error condition 0b010: Reserved 0b011: Reserved 0b100: Reserved 0b101: Reserved 0b110: Reserved 0b111: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
WM_DET	3:2	Watermark Detection/Generation	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WME_EN	1	Enables WM error to be driven to GPIO pin	0x0: Disabled 0x1: Enabled
WM_EN	0	Watermark Enable	0b0: Watermarking disabled 0b1: Watermarking enabled

WM_2 (0x18A)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
Reset	–	0x5			0x0	0x0	0x0	
Access Type	–				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HsyncPol	3	HS Polarity (only effective for watermark block)	0b0: Noninverting 0x1: Inverting
VsyncPol	2	VS Polarity (only effective for watermark block)	0b0: Noninverting 0x1: Inverting
WM_NPFILT	1:0	Phase accumulator terminal count	0bXX: Phase accumulator terminal count

WM_3 (0x18B)*

BIT	7	6	5	4	3	2	1	0
Field	–	WM_TH[6:0]						
Reset	–	0x14						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TH	6:0	Matched filter threshold	0bXXXXXXX: Matched filter threshold

WM_4 (0x18C)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
Reset	–	–	0x1		0b0	–	0x0	
Access Type	–	–				–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WM_MASKMODE	1:0	Sets watermark mask for the device	0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved b011: Reserved

WM_5 (0x18D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
WM_DETOUT	1	Live frame-based detection output	0b0: Watermark not detected 0b1: Watermark detected
WM_ERROR	0	Live active-high watermark error	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears

WM_6 (0x18E)

BIT	7	6	5	4	3	2	1	0
Field	WM_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TIMER	7:0	Time in 2ms steps that the frozen-frame condition must be observed before an error is generated. 0 = no filter.	0xXX: Number of milliseconds

WM_WREN_0 (0x1AE)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_L	7:0	Works in conjunction with WM_WREN_H (0x1AF) to enable writing to watermark registers. When 0xBA is written to WM_WREN_L and 0xDC is written to WM_WREN_H, watermark registers are write-enabled; otherwise, watermark registers are read-only.	0xBA: Enables writing to watermark registers (only if WM_WREN_H contains the value 0xDC) All other values: Watermark registers are read-only

WM_WREN_1 (0x1AF)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_H	7:0	Works in conjunction with WM_WREN_L (0x1AE) to enable writing to watermark registers. When 0xBA is written to WM_WREN_L and 0xDC is written to WM_WREN_H, watermark registers are write-enabled; otherwise, watermark registers are read-only.	0xDC: Enables writing to watermark registers (only if WM_WREN_L contains the value 0xBA) All other values: Watermark registers are read-only

CROSS_0 (0x1B0)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0x0	0x0	0x00				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS0_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

CROSS_1 (0x1B1)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0x0	0x0	0x01				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS1_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1	0bXXXXX: Incoming bit position

CROSS_2 (0x1B2)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0x0	0x0	0x02				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS2_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS2_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2	0bXXXXX: Incoming bit position

CROSS_3 (0x1B3)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0x0	0x0	0x03				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS3_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3	0bXXXXX: Incoming bit position

CROSS_4 (0x1B4)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0x0	0x0	0x04				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS4_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4	0bXXXXX: Incoming bit position

CROSS_5 (0x1B5)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0x0	0x0	0x05				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS5_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS5_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5	0bXXXXX: Incoming bit position

CROSS_6 (0x1B6)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0x0	0x0	0x06				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS6_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS6_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6	0bXXXXX: Incoming bit position

CROSS_7 (0x1B7)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0x0	0x0	0x07				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS7_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7	0bXXXXX: Incoming bit position

CROSS_8 (0x1B8)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0x0	0x0	0x08				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS8_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS8_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8	0bXXXXX: Incoming bit position

CROSS_9 (0x1B9)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0x0	0x0	0x09				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS9_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS9_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9	0bXXXXX: Incoming bit position

CROSS_10 (0x1BA)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0x0	0x0	0x0A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS10_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10	0bXXXXX: Incoming bit position

CROSS_11 (0x1BB)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0x0	0x0	0x0B				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS11_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS11_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11	0bXXXXX: Incoming bit position

CROSS_12 (0x1BC)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0x0	0x0	0x0C				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS12_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS12_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12	0bXXXXX: Incoming bit position

CROSS_13 (0x1BD)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0x0	0x0	0x0D				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS13_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13	0bXXXXX: Incoming bit position

CROSS_14 (0x1BE)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0x0	0x0	0x0E				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14	0bXXXXX: Incoming bit position

CROSS_15 (0x1BF)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0x0	0x0	0x0F				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15	0bXXXXX: Incoming bit position

CROSS_16 (0x1C0)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0x0	0x0	0x10				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS16_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16	0bXXXXX: Incoming bit position

CROSS_17 (0x1C1)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0x0	0x0	0x11				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17	0bXXXXX: Incoming bit position

CROSS_18 (0x1C2)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0x0	0x0	0x12				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS18_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18	0bXXXXX: Incoming bit position

CROSS_19 (0x1C3)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0x0	0x0	0x13				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19	0bXXXXX: Incoming bit position

CROSS_20 (0x1C4)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0x0	0x0	0x14				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20	0bXXXXX: Incoming bit position

CROSS_21 (0x1C5)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0x0	0x0	0x15				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21	0bXXXXX: Incoming bit position

CROSS_22 (0x1C6)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0x0	0x0	0x16				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS22_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22	0bXXXXX: Incoming bit position

CROSS_23 (0x1C7)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0x0	0x0	0x17				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS23_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS23_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23	0bXXXXX: Incoming bit position

CROSS_24 (0x1C8)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS24_I	CROSS24_F	CROSS24[4:0]				
Reset	–	0x0	0x0	0x18				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS24_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS24_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS24	4:0	Maps incoming bit position set by this field to the outgoing bit position 24	0bXXXXX: Incoming bit position

CROSS_25 (0x1C9)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS25_I	CROSS25_F	CROSS25[4:0]				
Reset	–	0x0	0x0	0x19				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS25_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS25_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS25	4:0	Maps incoming bit position set by this field to the outgoing bit position 25	0bXXXXX: Incoming bit position

CROSS_26 (0x1CA)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS26_I	CROSS26_F	CROSS26[4:0]				
Reset	–	0x0	0x0	0x1A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS26_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS26_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS26	4:0	Maps incoming bit position set by this field to the outgoing bit position 26	0bXXXXX: Incoming bit position

CROSS_27 (0x1CB)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS27_I	CROSS27_F	CROSS27[4:0]				
Reset	–	0x0	0x0	0x1B				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS27_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS27_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS27	4:0	Maps incoming bit position set by this field to the outgoing bit position 27	0bXXXXX: Incoming bit position

PRBS_ERR (0x1CC)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_ERR	7:0	Video PRBS Error Counter Clears on read.	0xXX: Number of video PRBS errors since last read

OLDI0 (0x1CD)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	VPRBS_FAIL	VPRBS_CHK_EN	RSVD	LUT_C_EN	LUT_B_EN	LUT_A_EN
Reset	0b0	–	0b0	0b0	0b0	0x0	0x0	0x0
Access Type		–	Read Only	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_FAIL	5	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: Video PRBS check passed 0b1: Video PRBS check failed
VPRBS_CHK_EN	4	Enables video PRBS checker	0b0: Video PRBS checker disabled 0b1: Video PRBS checker enabled
LUT_C_EN	2	Enables Color C lookup table (LUT) [23:16]	0b0: Color C LUT disabled 0b1: Color C LUT enabled
LUT_B_EN	1	Enables Color B lookup table (LUT) [15:8]	0b0: Color B LUT disabled 0b1: Color B LUT enabled
LUT_A_EN	0	Enables Color A lookup table (LUT) [7:0]	0b0: Color A LUT disabled 0b1: Color A LUT enabled

OLDI1 (0x1CE)*

BIT	7	6	5	4	3	2	1	0
Field	OLDI_OUTSEL	OLDI_FORMAT	OLDI_4TH_LANE	OLDI_SWAP_AB	OLDI_SPL_EN	OLDI_SPL_MODE[1:0]		OLDI_SPL_POL
Reset	0x0	0x0	0x0	0x0	0x0	0x3		0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OLDI_OUTSEL	7	Selects which OLDI port to use for data output. Set this register when VID_LOCK = 0.	0b0: Port A 0b1: Port B
OLDI_FORMAT	6	Output format of LVDS port. Set this register when VID_LOCK = 0.	0b0: OLDI 0b1: VESA
OLDI_4TH_LANE	5	OLDI lane count. Set this register when VID_LOCK = 0.	0b0: Four lanes 0b1: Three lanes
OLDI_SWAP_AB	4	Swaps OLDI ports A and B. Set this register when VID_LOCK = 0.	0b0: Ports A and B not swapped 0b1: Ports A and B swapped
OLDI_SPL_EN	3	OLDI Splitter Enable. Set this register when VID_LOCK = 0.	0b0: Splitter disabled 0b1: Splitter enabled
OLDI_SPL_MODE	2:1	OLDI Splitter Mode. Set this register when VID_LOCK = 0.	0b00: Random 0b01: Split with HS 0b10: Split with VS 0b11: Split with DE
OLDI_SPL_POL	0	Set to 0 for dual OLDI applications. Set this register when VID_LOCK = 0.	0b0: Falling Edge 0b1: Rising Edge

OLDI2 (0x1CF)*

BIT	7	6	5	4	3	2	1	0
Field	PD_LVDS_B	PD_LVDS_A	RSVD	VS_OUT_EN	RSVD	RSVD	OLDI_DUP	SSEN
Reset	0b0	0b0	0x0	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read	Write, Read		Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PD_LVDS_B	7	Selects power-up/power-down status for LVDS output driver B	0b0: LVDS ouptut driver B powered up 0b1: LVDS output driver B powered down
PD_LVDS_A	6	Selects power-up/power-down status for LVDS output driver A	0b0: LVDS output driver A powered up 0b1: LVDS output driver A powered down
VS_OUT_EN	4	Selects whether or not to output VSYNC from GPIO	0b0: VSYNC not output 0b1: Output VSYNC from GPIO
OLDI_DUP	1	Selects whether or not to duplicate OLDI at both ports	0b0: OLDI not duplicated 0b1: OLDI duplicated at both ports
SSEN	0	Enables spread spectrum OLDI output clock Spread percentage is adjusted from OLDIPLL registers. Default percentage is 0.5%.	0b0: Spread spectrum disabled 0b1: Spread spectrum enabled

OLDI3 (0x1D0)*

BIT	7	6	5	4	3	2	1	0
Field	LANE_INV_B0	LANE_SEL_B0[2:0]			LANE_INV_A0	LANE_SEL_A0[2:0]		
Reset	0b0	0x0			0b0	0x0		
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LANE_INV_B0	7	Lane B0 polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted
LANE_SEL_B0	6:4	Selects OLDI Port B Lane 0 output pins	0b000: Output from B0 0b001: Output from B1 0b010: Output from B2 0b011: Output from B3 0b100: Output from BCLK 0b101: Reserved 0b110: Reserved 0b111: Reserved
LANE_INV_A0	3	Lane A0 polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted
LANE_SEL_A0	2:0	Selects OLDI Port A Lane 0 output pins	0b000: Output from A0 0b001: Output from A1 0b010: Output from A2 0b011: Output from A3 0b100: Output from ACLK 0b101: Reserved 0b110: Reserved 0b111: Reserved

OLDI4 (0x1D1)*

BIT	7	6	5	4	3	2	1	0
Field	LANE_INV_B1	LANE_SEL_B1[2:0]			LANE_INV_A1	LANE_SEL_A1[2:0]		
Reset	0b0	0x1			0b0	0x1		
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LANE_INV_B1	7	Lane B1 polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted
LANE_SEL_B1	6:4	Selects OLDI Port B Lane 1 output pins	0b000: Output from B0 0b001: Output from B1 0b010: Output from B2 0b011: Output from B3 0b100: Output from BCLK 0b101: Reserved 0b110: Reserved 0b111: Reserved
LANE_INV_A1	3	Lane A1 polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted
LANE_SEL_A1	2:0	Selects OLDI Port A Lane 1 output pins	0b000: Output from A0 0b001: Output from A1 0b010: Output from A2 0b011: Output from A3 0b100: Output from ACLK 0b101: Reserved 0b110: Reserved 0b111: Reserved

OLDI5 (0x1D2)*

BIT	7	6	5	4	3	2	1	0
Field	LANE_INV_B2	LANE_SEL_B2[2:0]			LANE_INV_A2	LANE_SEL_A2[2:0]		
Reset	0b0	0x2			0b0	0x2		
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LANE_INV_B2	7	Lane B2 polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted
LANE_SEL_B2	6:4	Selects OLDI Port B Lane 2 output pins	0b000: Output from B0 0b001: Output from B1 0b010: Output from B2 0b011: Output from B3 0b100: Output from BCLK 0b101: Reserved 0b110: Reserved 0b111: Reserved
LANE_INV_A2	3	Lane A2 polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted

BITFIELD	BITS	DESCRIPTION	DECODE
LANE_SEL_A2	2:0	Selects OLDI Port A Lane 2 output pins	0b000: Output from A0 0b001: Output from A1 0b010: Output from A2 0b011: Output from A3 0b100: Output from ACLK 0b101: Reserved 0b110: Reserved 0b111: Reserved

OLDI6 (0x1D3)*

BIT	7	6	5	4	3	2	1	0
Field	LANE_INV_B3	LANE_SEL_B3[2:0]			LANE_INV_A3	LANE_SEL_A3[2:0]		
Reset	0b0	0x3			0b0	0x3		
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LANE_INV_B3	7	Lane B3 polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted
LANE_SEL_B3	6:4	Selects OLDI Port B Lane 3 output pins	0b000: Output from B0 0b001: Output from B1 0b010: Output from B2 0b011: Output from B3 0b100: Output from BCLK 0b101: Reserved 0b110: Reserved 0b111: Reserved
LANE_INV_A3	3	Lane A3 polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted
LANE_SEL_A3	2:0	Selects OLDI Port A Lane 3 output pins	0b000: Output from A0 0b001: Output from A1 0b010: Output from A2 0b011: Output from A3 0b100: Output from ACLK 0b101: Reserved 0b110: Reserved 0b111: Reserved

OLDI7 (0x1D4)*

BIT	7	6	5	4	3	2	1	0
Field	LANE_INV_BCLK	LANE_SEL_BCLK[2:0]			LANE_INV_ACLK	LANE_SEL_ACLK[2:0]		
Reset	0b0	0x4			0b0	0x4		
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LANE_INV_BCLK	7	Lane BCLK polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted

BITFIELD	BITS	DESCRIPTION	DECODE
LANE_SEL_BCLK	6:4	Selects OLDI Port B Clock Lane output pins	0b000: Output from B0 0b001: Output from B1 0b010: Output from B2 0b011: Output from B3 0b100: Output from BCLK 0b101: Reserved 0b110: Reserved 0b111: Reserved
LANE_INV_ACLK	3	Lane ACLK polarity inversion	0b0: Lane polarity not inverted 0b1: Lane polarity inverted
LANE_SEL_ACLK	2:0	Selects OLDI Port A Clock Lane output pins	0b000: Output from A0 0b001: Output from A1 0b010: Output from A2 0b011: Output from A3 0b100: Output from ACLK 0b101: Reserved 0b110: Reserved 0b111: Reserved

VRX46 (0x1EA)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	–	RSVD	DUAL_OLDI_AUTO_RST_ALIGNED	DUAL_OLDI_AUTO_RST_ALIGN
Reset	0b0	0b0	0b0	0b0	–	0x1	0b0	0b0
Access Type					–		Read Clears All	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DUAL_OLDI_AUTO_RST_ALIGNED	1	Reports if the OLDI output reset itself after it detected a non-alignment on the OLDI outputs. Available in rev 7 and newer parts.	0x0: No reset observed 0x1: Reset observed
DUAL_OLDI_AUTO_RST_ALIGN	0	Selects if the dual OLDI output should be reset upon a detection of misalignment of DE signals on the output ports. Reset is applied if 4 consecutive lines have an alignment issue. Available in rev 7 and newer parts.	0x0: Auto reset on non-alignment disabled 0x1: Auto reset on non-alignment enabled

GPIO_A (0x203)*

GPIO 1

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x204)*

1

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x01				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x205)*

1

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x01				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x206)* 2

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x207)* 2

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x02				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x208)* 2

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x02				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x209)* 3

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x20A)* 3

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x03				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x20B)* 3

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x03				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x20C)* 4

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x20D)*

4

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x04				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x20E)*

4

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x04				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x20F)*

5

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x210)*

5

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x05				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x211)* 5

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x05				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x212)* 6

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x213)*

6

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x06				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x214)*

6

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x06				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x215)*

7

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x216)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x07				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x217)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x07				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x218)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x219)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x08				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull up/down configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x21A)*

8

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x08				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x21B)*

9

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x21C)*

9

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x09				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull up/down configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x21D)*

9

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x09				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x21E)*

10

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x21F)* 10

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x0A				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x220)* 10

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x0A				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x221)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x222)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x0B				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup/Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x223)* 11

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x0B				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x224)* 12

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x225)* 12

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x0C				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x226)* 12

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x0C				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x227)* 13

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x228)* 13

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x0D				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x229)* 13

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x0D				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x22A)* 14

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b0	0x0	0x0	0b1	0b1	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x22B)* 14

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x1		0b0	0x0E				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	I^2C IO is only open-drain	0bX: NA
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x22C)* 14

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x0E				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

GPIO_A (0x22D)* 15

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b0	0x0	0x0	0b1	0b1	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Pullup/Pulldown Resistor Strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x22E)* 15

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x1		0b0	0x0F				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	I^2C IO is only open-drain	0bX: NA
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: GPIO transmit ID

GPIO_C (0x22F)* 15

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x0F				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: GPIO receive ID

CMU4 (0x244)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		GPIO_SPEED_B[1:0]		GPIO_SPEED_A[1:0]	
Reset	0b00		0b00		0b10		0b11	
Access Type					Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_SPEED_B	3:2	Controls GPIO Speed Group B (GPIO2 to GPIO13) transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V	0: 2ns, 1ns 1: 4ns, 2ns 2: 8ns, 4ns 3: 16ns, 8ns
GPIO_SPEED_A	1:0	Controls GPIO Speed Group A (GPIO0 and GPIO1) transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V	0: 2ns, 1ns 1: 4ns, 2ns 2: 8ns, 4ns 3: 16ns, 8ns

UART_PT_0 (0x24A)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_1_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_L	7:0	Custom UART bit length for pass-through UART Channel 1 Set BITLEN_MAN_CFG_1 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (LSB).	0xXX: Lower byte of custom UART bit length for pass-through UART Channel 1

UART_PT_1 (0x24B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_1_H[5:0]					
Reset	–	–	0x05					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_H	5:0	Custom UART bit length for pass-through UART Channel 1 Set BITLEN_MAN_CFG_1 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (6 MSbs).	0xXX: Upper bits of custom UART bit length for pass-through UART Channel 1

UART_PT_2 (0x24C)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_2_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_L	7:0	Custom UART bit length for pass-through UART Channel 2 Set BITLEN_MAN_CFG_2 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (LSB).	0xXX: Lower byte of custom UART bit length for pass-through UART Channel 2

UART_PT_3 (0x24D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_2_H[5:0]					
Reset	–	–	0x05					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_H	5:0	Custom UART bit length for pass-through UART Channel 2 Set BITLEN_MAN_CFG_2 to 1 to use this value. Set this register to the UART bit length divided by 6.666ns (6 MSbs).	0xXX: Upper bits of custom UART bit length for pass-through UART Channel 2

I2C_PT_4 (0x252)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_1[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_1	7:1	I^2C address translator source A Works in conjunction with DST_A_1. When I^2C device address matches SRC_A_1, internal I^2C main (on remote side) replaces the device address by DST_A_1.	0bXXXXXXX: Address of I^2C device that is to be replaced by the address in DST_A_1

I2C_PT_5 (0x253)*

BIT	7	6	5	4	3	2	1	0
Field	DST_A_1[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_1	7:1	I^2C address translator destination A Works in conjunction with SRC_A_1. See the description of SRC_A_1.	0bXXXXXXX: Address that is to replace the address of the device pointed to in SRC_A_1

I2C_PT_6 (0x254)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_1[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_1	7:1	I^2C address translator source B Works in conjunction with DST_B_1. When I^2C device address matches SRC_B_1, internal I^2C main (on remote side) replaces the device address by DST_B_1.	0bXXXXXXX: Address of I^2C device that is to be replaced by the address in DST_B_1

I2C_PT_7 (0x255)*

BIT	7	6	5	4	3	2	1	0
Field	DST_B_1[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_1	7:1	I^2C address translator destination B Works in conjunction with SRC_B_1. See the description of SRC_B_1.	0bXXXXXXX: Address that is to replace the address of the device pointed to in SRC_B_1

I2C_PT_8 (0x256)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_2[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_2	7:1	I^2C address translator source A Works in conjunction with DST_A_2. When I^2C device address matches SRC_A_2, internal I^2C main (on remote side) replaces the device address by DST_A_2.	0bXXXXXXX: Address of I^2C device that is to be replaced by the address in DST_A_2

I2C_PT_9 (0x257)*

BIT	7	6	5	4	3	2	1	0
Field	DST_A_2[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_2	7:1	I^2C address translator destination A Works in conjunction with SRC_A_2. See the description of SRC_A_2.	0bXXXXXXX: Address that is to replace the address of the device pointed to in SRC_A_2

I2C_PT_10 (0x258)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_2[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_2	7:1	I^2C address translator source B Works in conjunction with DST_B_2. When I^2C device address matches SRC_B_2, internal I^2C main (on remote side) replaces the device address by DST_B_2.	0bXXXXXXX: Address of I^2C device that is to be replaced by the address in DST_B_2

I2C_PT_11 (0x259)*

BIT	7	6	5	4	3	2	1	0
Field	DST_B_2[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_2	7:1	I^2C address translator destination A Works in conjunction with SRC_B_2. See the description of SRC_B_2.	0bXXXXXXX: Address that is to replace the address of the device pointed to in SRC_B_2

PM_OV_STAT (0x25D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD[1:0]		OV_LEVEL[1:0]	
Reset	–	–	–	–	0x1		0x1	
Access Type	–	–	–	–			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
OV_LEVEL	1:0	V_{DDSW} Overvoltage Comparator Trip Level V_{TRIP_OV}	0x0: 1.105V + V_{HYST_OV} 0x1: 1.124V + V_{HYST_OV} 0x2: 1.157V + V_{HYST_OV} 0x3: 1.184V + V_{HYST_OV}

LOSS_INT_OEN (0x2D2)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LOSS_OF_LOCK_OEN	LOSS_OF_VIDEO_LOCK_OEN
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOSS_OF_LOCK_OEN	1	Enables reporting loss of lock on ERRB pin. Available in rev 7 and newer parts.	0x0: Disabled 0x1: Enabled
LOSS_OF_VIDEO_LOCK_OEN	0	Enables reporting loss of video lock on ERRB pin. Available in rev 7 and newer parts.	0x0: Disabled 0x1: Enabled

LOSS_INT_FLAG (0x2D3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LOSS_OF_LOCK_FLAG	LOSS_OF_VIDEO_LOCK_FLAG
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
LOSS_OF_LOCK_FLAG	1	Loss of lock on GMSL link is detected (sticky). Read this bitfield to clear. Available in rev 7 and newer parts.	0x0: Not detected 0x1: Detected
LOSS_OF_VIDEO_LOCK_FLAG	0	Loss of video lock on GMSL link is detected (sticky). Read this bitfield to clear. Available in rev 7 and newer parts.	0x0: Not detected 0x1: Detected

RLMS3 (0x403, 0x503)

BIT	7	6	5	4	3	2	1	0
Field	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
Reset	0b0	0b0	0b0	0b0	0b1	–	0b10	
Access Type	Write, Read					–		

BITFIELD	BITS	DESCRIPTION	DECODE
AdaptEn	7	Adapt process enable	0b0: Manual adaptation process disabled 0b1: Manual adaptation process enabled

RLMS4 (0x404, 0x504)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD_EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		RSVD_EOM_PER_MODE	EOM_EN
Reset	0x4				0b10		0b1	0b1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD_EOM_CHK_AMOUNT	7:4	This factor (N) is used to select the order of number of observations in each eye-monitor window, as follows: Observations = 6.29 x $10^{(N + 2)}$.	0xX: N factor
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits to allow in a measurement window	0b00: Allow no errors 0b01: Allow one error 0b10: Allow two errors 0b11: Allow three errors
RSVD_EOM_PER_MODE	1	Eye-opening monitor periodic mode enable	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Eye-opening monitor enable	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

RLMS5 (0x405, 0x505)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0b0	0b0010000						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye-opening monitor manual trigger For use when periodic mode is disabled.	0b0: No action 0b1: EOM manual trigger request
EOM_MIN_THR	6:0	The eye-opening monitor minimum threshold as defined by the following equation: Eye-opening percentage = EOM_MIN_THR/64. If the value is zero, the EOM is disabled.	0bXXXXXXX: EOM minimum threshold factor

RLMS6 (0x406, 0x506)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	EOM_RST_THR[6:0]						
Reset	0b1	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_MODE	7	Eye-opening is measured vertically or horizontally	0b0: Vertical opening mode 0b1: Horizontal opening mode
EOM_RST_THR	6:0	The eye-opening monitor refresh threshold as defined by the following equation: Eye-opening percentage = EOM_MIN_THR/64. If the value is zero, the EOM is disabled.	0bXXXXXXX: EOM refresh threshold factor

RLMS7 (0x407, 0x507)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-opening monitor measurement done	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Last completed eye-opening monitor observation	0bXXXXXXX: EOM measurement result

RLMS34 (0x434, 0x534)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntL	7:0	Eye-monitor period count (RxClk20) LSB	0xXX: Eye-monitor period count (least significant byte)

RLMS35 (0x435, 0x535)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntH	7:0	Eye-monitor period count (RxClk20) MSB	0xXX: Eye-monitor period count (most significant byte)

RLMS37 (0x437, 0x537)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–			Read Only	Write Only	Write Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonDone	4	Eye-monitor period complete (read-only, reset on start)	0b0: Eye-monitor data collection not complete 0b1: Eye-monitor data collection complete
EyeMonCntClr	3	Eye-monitor error/valid count clear (one-shot) Readback is EyeMonClrPL from long pulse generation.	0b0: NA 0b1: Clear eye-monitor data collection counters
EyeMonStart	2	Eye-monitor start (one-shot) Readback is EyeMonStClrPL from long pulse generation for both start and clear.	0b0: NA 0b1: Start eye-monitor data collection
EyeMonPh	1	Eye-monitor phase	0b0: Eye-monitor search early phase 0b1: Eye-monitor search late phase
EyeMonDPol	0	Eye-monitor data polarity	0b0: Eye-monitor search for ones 0b1: Eye-monitor search for zeros

RLMS38 (0x438, 0x538)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntL	7:0	Eye-monitor error count (read-only)	0xXX: Eye-monitor error count (LSB)

RLMS39 (0x439, 0x539)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntH	7:0	Eye-monitor error count (read-only)	0xXX: Eye-monitor error count (MSB)

RLMS3A (0x43A, 0x53A)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntL	7:0	Eye-monitor valid (hit) count (read-only)	0xXX: Eye-monitor valid count (LSB)

RLMS3B (0x43B, 0x53B)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntH	7:0	Eye-monitor valid (hit) count (read-only)	0xXX: Eye-monitor valid count (MSB)

RLMS3D (0x43D, 0x53D)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPh[6:0]							ErrChPhTogEn
Reset	0b0000000							0b1
Access Type	Read Only							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPh	7:1	Error channel phase (read-only)	0bXXXXXXX: 5.6 degrees per step
ErrChPhTogEn	0	Error channel phase toggle enable	0b0: Use primary phase only 0b1: Auto toggle phase between primary and secondary

RLMS3E (0x43E, 0x53E)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTA	ErrChPhSec[6:0]						
Reset	0b1	0b0110011						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTA	7	Error-channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSec	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel (fast receive, secondary phase).	0bxxxxxxx: Error channel phase secondary (odd)

RLMS3F (0x43F, 0x53F)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTA	ErrChPhPri[6:0]						
Reset	0b0	0b1110010						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTA	7	Error-channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPri	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel (fast receive, primary phase).	0bxxxxxxx: Error channel phase primary (even)

RLMS49 (0x449, 0x549)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
Reset	–	0b1	0b1	0b1	0b0	0b0	–	0b1
Access Type	–					Write, Read	–	

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPwrUp	2	Error channel power-down	0b0: Error channel power disabled 0b1: Error channel power enabled

RLMS58 (0x458, 0x558)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh1[6:0]						
Reset	–	0b0101000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh1	6:0	Error channel target amplitude for ones.	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS59 (0x459, 0x559)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh0[6:0]						
Reset	–	0b1101000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh0	6:0	Error channel target amplitude for zeros.	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS64 (0x464, 0x564)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
Reset	–	–	–	–	–	0b0	0b00	
Access Type	–	–	–	–	–		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx Spread Spectrum mode	0b00: Spread spectrum disabled 0b01: Reserved 0b10: Reserved 0b11: Spread spectrum enabled (center spread)

RLMS70 (0x470, 0x570)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0b0000001						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx spread spectrum frequency control	0bXXXXXXX: Tx spread spectrum center frequency control

RLMS71 (0x471, 0x571)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0b000001						0b0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx spread spectrum center spread startup control	0bXXXXXX: Tx spread spectrum center spread startup control

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCEn	0	Tx spread spectrum enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x472, 0x572)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx Spread Spectrum Frequency Prescaler Low Byte	0xXX: Tx spread spectrum frequency prescaler low byte

RLMS73 (0x473, 0x573)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclH	2:0	Tx Spread Spectrum Frequency Prescaler High Bits	0bXXX: Tx spread spectrum frequency pre-scaler high bits

RLMS74 (0x474, 0x574)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx Spread Spectrum Interpolator Phase Low Byte	0xXX: Tx spread spectrum frequency interpolator phase low byte

RLMS75 (0x475, 0x575)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx Spread Spectrum Interpolator Phase	0bXXXXXXX: Tx spread spectrum frequency interpolator phase high bits

RLMS76 (0x476, 0x576)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx spread spectrum interpolator phase quadrant	0xbXX: Tx spread spectrum interpolator phase quadrant

RLMS95 (0x495, 0x595)

BIT	7	6	5	4	3	2	1	0
Field	TxAmplManEn	RSVD	TxAmplMan[5:0]					
Reset	0b0	0b1	0b101001					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplManEn	7	Tx Amplitude Manual Override	0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude
TxAmplMan	5:0	Tx Amplitude	0bXXXXXX: Binary amplitude 10mV per count

RLMSA4 (0x4A4, 0x5A4)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD_AEQ_PER_MULT[1:0]		RSVD_AEQ_PER[5:0]					
Reset	0b10		0b111101					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD_AEQ_PER_MULT	7:6	This bit field is reserved. Adaptive EQ period multiplier	0b00: 1ms 0b01: 4ms 0b10: 16ms 0b11: 64ms
RSVD_AEQ_PER	5:0	This bit field is reserved. Adaptive EQ Period Periodic adaptation is disabled when value is 0. Adaptive EQ period is (AEQ_PER value x AEQ_PER_MULT).	0bXXXXXX: Only zeros have a special meaning. See Description

RLMSAC (0x4AC, 0x5AC)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
Reset	0b1	0b1001101						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTAFR3G	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecFR3G	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Fast Receive, Secondary Phase, 3Gbps)	0bXXXXXXX: Chosen phase value

RLMSAD (0x4AD, 0x5AD)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
Reset	0b0	0b0001101						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTAFR3G	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriFR3G	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Fast Receive, Primary Phase, 3Gbps)	0bXXXXXXX: Chosen phase value

RLMSAE (0x4AE, 0x5AE)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTAFR1G5	ErrChPhSecFR1G5[6:0]						
Reset	0b1	0b1001110						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTAFR1G5	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecFR1G5	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Fast Receive, Secondary Phase, 1.5Gbps)	0bXXXXXXX: Chosen phase value

RLMSAF (0x4AF, 0x5AF)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTAFR1G5	ErrChPhPriFR1G5[6:0]						
Reset	0b0	0b0001111						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTAFR1G5	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriFR1G5	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Fast Receive, Primary Phase, 1.5Gbps)	0bXXXXXXX: Chosen phase value

RLMSB0 (0x4B0, 0x5B0)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASR1G5	ErrChPhSecSR1G5[6:0]						
Reset	0b1	0b0110100						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASR1G5	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSR1G5	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Slow Receive, Secondary Phase, 1.5Gbps)	0bXXXXXXX: Chosen phase value

RLMSB1 (0x4B1, 0x5B1)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASR1G5	ErrChPhPriSR1G5[6:0]						
Reset	0b0	0b1110011						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASR1G5	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSR1G5	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Slow Receive, Primary Phase, 1.5Gbps)	0bXXXXXXX: Chosen phase value

RLMSB2 (0x4B2, 0x5B2)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG75	ErrChPhSecSRG75[6:0]						
Reset	0b1	0b0111110						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG75	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSRG75	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Secondary Phase, 750Mbps)	0bXXXXXXX: Chosen phase value

RLMSB3 (0x4B3, 0x5B3)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG75	ErrChPhPriSRG75[6:0]						
Reset	0b0	0b1111101						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG75	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSRG75	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Slow Receive, Primary Phase, 750Mbps)	0bXXXXXXX: Chosen phase value

RLMSB4 (0x4B4, 0x5B4)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG375	ErrChPhSecSRG375[6:0]						
Reset	0b1	0b0111100						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG375	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSRG375	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Slow Receive, Secondary Phase, 375Mbps)	0bXXXXXXX: Chosen phase value

RLMSB5 (0x4B5, 0x5B5)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG375	ErrChPhPriSRG375[6:0]						
Reset	0b0	0b1111011						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG375	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSRG375	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Slow Receive, Primary Phase, 375Mbps)	0bXXXXXXX: Chosen phase value

RLMSB6 (0x4B6, 0x5B6)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
Reset	0b1	0b0111011						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG1875	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSRG1875	6:0	A 7-bit phase command used for eye monitoring and during adaptation by the error channel. (Slow Receive, Secondary Phase, 187.5Mbps)	0bXXXXXXX: Chosen phase value

RLMSB7 (0x4B7, 0x5B7)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
Reset	0b0	0b1111010						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG1875	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSRG1875	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Primary Phase, 187.5Mbps)	0bXXXXXXX: Chosen phase value

DPLL_0 (0xB00, 0xD00)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	config_soft_rst_n
Reset	0x1	0x1	0x1	0x1	0x0	0x1	0x0	0x1
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
config_soft_rst_n	0	DPLL Soft Reset Pin. Read out the value of this bitfield before writing to other bits in this register.

DPLL_3 (0xB03, 0xD03)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	config_spread_bit_ratio[2:0]		
Reset	0x1	0x0	0x0	0x0	0x0	0x2		
Access Type						Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
config_spread_bit_ratio	2:0	Controls the magnitude of the triangle wave input to the divider dsm as a percentage of the nominal divider value. If config registers are reset, the config_spread_bit_ratio value will not propagate to the triangle wave without rewriting to it. Likewise, if the triangle wave module is reset, the user will need to rewrite to spread_bit_ratio to set it back to desired value.	001: 0.25% 010: 0.5% 011: 1% 100: 2% 101: 4% 110: 4% 111: 4%

LUT_A_ (0x1000)

Color Look Up Table page for Red, the 256 bytes under this register block correspond to the LUT memory rows when written or read.

BIT	7	6	5	4	3	2	1	0
Field	LUT_A_[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LUT_A_	7:0	Color Look-Up Table page for Red, the 256 bytes under this register block correspond to the LUT memory rows when written or read.

LUT_B_ (0x1100)

Color Look Up Table page for Green, the 256 bytes under this register block correspond to the LUT memory rows when written or read.

BIT	7	6	5	4	3	2	1	0
Field	LUT_B_[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LUT_B_	7:0	Color Look-Up Table page for Green, the 256 bytes under this register block correspond to the LUT memory rows when written or read.

LUT_C_ (0x1200)

Color Look Up Table page for Blue, the 256 bytes under this register block correspond to the LUT memory rows when written or read.

BIT	7	6	5	4	3	2	1	0
Field	LUT_C_[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
LUT_C_	7:0	Color Look-Up Table page for Blue, the 256 bytes under this register block correspond to the LUT memory rows when written or read.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/24	Initial Release	—

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