

## MAX96722

# Quad GMSL2 to CSI-2 Deserializer with GMSL1 Compatibility

PRELIMINARY

### General Description

The MAX96722 deserializer converts GMSL2 or GMSL1 serial inputs into MIPI CSI-2 D-PHY or C-PHY formatted outputs. The device allows each link to simultaneously transmit bidirectional control-channel data while forward video transmissions are in progress. The MAX96722 can accommodate as many as four remotely located sensors using industry-standard coax or STP interconnects. Each GMSL2 serial link operates at a fixed rate of 3Gbps in the forward direction and 187.5Mbps in the reverse direction. In GMSL1 mode, the MAX96722 can be paired with first-generation 3.12Gbps or 1.5Gbps GMSL1 serializers or operate up to 3.12Gbps with GMSL2 serializers in GMSL1 mode.

The MAX96722 supports both aggregation and replication of video data, enabling streams from multiple remotely located sensors to be combined and routed to one or more of the available CSI-2 outputs. Data can also be routed based on virtual channel ID, enabling multiple streams from a single GMSL input to be routed independently to different CSI-2 outputs. Alternatively, data from multiple sensors can be synchronized and combined in a single CSI-2 stream within a composite superframe using frame concatenation. The CSI-2 interface supports both 2x4 lane and 4x2 lane configurations using either C-PHY or D-PHY.

A variety of peripheral communication options are provided for flexible local register access and remote device programming. Three I<sup>2</sup>C/UART ports support redundant local and remote internal register access with concurrent or tunneled remote peripheral communication. An additional two SPI ports are provided as tunneling interfaces to remote peripherals (GMSL2).

Contact the factory to receive the GMSL2 Channel Specification document to confirm compliance.

### Applications

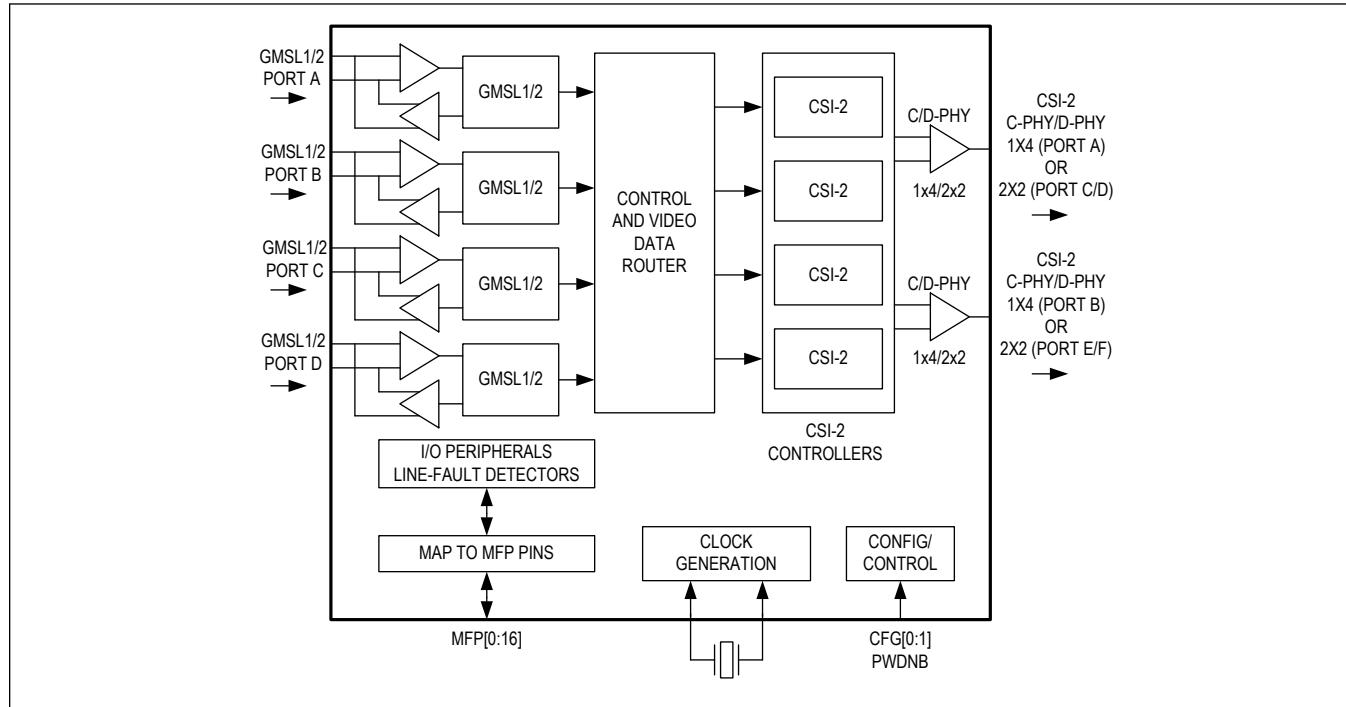
- High-Resolution Camera Systems
  - Rear-View Cameras
  - Driver Monitoring Systems
  - Gesture Cameras
- Safety Critical ADAS/Autonomous Driving Sensors
  - RADAR
  - LIDAR
  - Surround-View Cameras
  - High-Resolution Cameras
- Synchronized Multisensor Systems

### Benefits and Features

- MIPI CSI-2 v1.3 Output Configurable as 2x4-Lane, 1x4-Lane + 2x2-Lane, or 4x2-Lane
  - Selectable D-PHY v1.2 at 80Mbps-to-2.5Gbps/Lane or C-PHY v1.0 at 182Mbps-to-5.7Gbps/Lane
  - 16/32-Channel Virtual Channel Support (D/C-PHY)
  - Flexible Aggregation and Routing of Incoming Data via CSI-2 VC or Frame Concatenation
  - Data can be Replicated and Routed to any CSI Port
  - Supports RAW8/10/12/14/16/20, RGB565/666/888,YUV422 8-/10-Bit Formats
  - Double Pixel Mode for Transmission Efficiency
  - CSI-2 Lane Reassignment and Polarity Flip
  - MIPI/GMSL Video PRBS Generator and Checker
  - Checkerboard/Color Gradient Pattern Generator
  - Raw CSI-2 PRBS Generator
  - Independent Configuration of all Video Paths and GMSL/CSI-2 Ports
- Quad GMSL Inputs with Independently Configurable GMSL1/2 Operation, Link Speed, and Video Format
  - Mixed GMSL1/GMSL2 Support
  - Backward compatible with GMSL1 Serializers
  - GMSL1 Forward Link Speed up to 3.12Gbps
  - GMSL2 Link Speed of 3Gbps (Forward) and 187.5Mbps (Reverse)
  - Simultaneous Support of Both Synchronized and Non-Synchronized Cameras
  - Enables Precise Synchronization of Multiple Serializers for Large Camera Systems
  - GMSL PRBS Generator/Checker for Link Testing
  - Eye-Opening Monitor for Continuous Diagnostics
  - Adaptive Equalization Enables up to 15m Coax Cable with Multiple Inline Connectors
  - Compatible with 50Ω Coax or 100Ω STP
- ASIL-B Compliant (GMSL2)
  - Video Watermark Insertion and Detection
  - 16-bit CRC Protection of Control-Channel Data with Retransmission Upon Error Detection
  - Optional 32-bit CRC Protection of Video Line Data
  - ECC Protection of Video Data Memory
  - CRC Protection of CSI-2 Data Streams
- Concurrent Control Channel for Device Configuration and Communicating with Remote Peripherals
  - 3x I<sup>2</sup>C/UART, 2x SPI, 17x GPIO
  - Eight Hardware-Selectable Device Addresses
- Programmable Spread Spectrum for EMI Reduction
- Line-Fault Monitoring for GMSL Link
- 64-Lead 9 x 9mm TQFN with Exposed Pad

[Ordering Information](#) appears at end of datasheet.

## Simplified Block Diagram



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## Absolute Maximum Ratings

(All voltages with respect to ground.) .....	-0.3V to +1.1V
V <sub>DDIO</sub> .....	-0.3V to +3.9V
V <sub>DD18</sub> .....	-0.3V to +2.0V
V <sub>DD</sub> .....	-0.3V to +2.0V
V <sub>TERM</sub> .....	-0.3V to +1.32V
CAP_VDD .....	-0.3V to +1.2V
SIO_ (Active State) <sup>a</sup> .....	(V <sub>DD18</sub> - 1.1V) to V <sub>DD18</sub>
SIO_ (Inactive State) <sup>a</sup> .....	-0.3V to +1.1V
DA/B_P/N, CKA/B/C/FP/N <sup>b</sup> .....	-0.3V to (V <sub>TERM</sub> + 0.1V)
XRES, X2 .....	-0.3V to (V <sub>DD18</sub> + 0.3V)
All Other Pins <sup>c</sup> .....	-0.3V to (V <sub>DDIO</sub> + 0.3V)
Continuous Power Dissipation - Multilayer Board <sup>d</sup> .....	2412mW
Storage Temperature Range .....	-40°C to +150°C
Soldering Temperature (reflow) .....	+260°C

**Note 1:** Active state means device powered-up and not in sleep or power-down modes. Inactive state means device not powered-up, or powered-up in sleep or power-down mode.

**Note 2:** Specified maximum voltage or 1.36V, whichever is lower.

**Note 3:** Specified maximum voltage or 3.9V, whichever is lower.

**Note 4:** Derate 44mW/°C above T<sub>A</sub> = +70°C. Maximum dissipation is determined using specified θ<sub>JA</sub> and assuming maximum acceptable die temperature of 125°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 64-pin TQFN

Package Code	T6499+2
Outline Number	<a href="#">21-100060</a>
Land Pattern Number	<a href="#">90-100053</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	22.8°C/W
Junction to Case (θ <sub>JC</sub> )	5.4°C/W

### 64-pin TQFN-SW (Side-Wettable)

Package Code	T6499Y+2
Outline Number	<a href="#">21-100326</a>
Land Pattern Number	<a href="#">90-100053</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	22.8°C/W
Junction to Case (θ <sub>JC</sub> )	5.4°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](#). Note that a "+", "#", or ":" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](#).

**Electrical Characteristics**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ELECTRICAL CHARACTERISTICS / GMSL2 REVERSE CHANNEL SERIAL OUTPUTS - <a href="#">Figure 1</a></b>						
Output Voltage Swing (Single-ended)	$V_O$	$R_L = 100\Omega \pm 1\%$	190	250	310	mV
Output Voltage Swing (Differential)	$V_{ODT}$	$R_L = 100\Omega \pm 1\%$ peak-to-peak differential voltage	380	500	620	mV
Change in $V_{OD}$ Between Complementary Output States	$\Delta V_{OD}$	$R_L = 100\Omega \pm 1\%$ $ V_{OD(H)} - V_{OD(L)} $			25	mV
Differential Output Offset Voltage	$V_{OS}$	$R_L = 100\Omega \pm 1\%$ offset voltage in each output state	$V_{DD18} - 0.45$	$V_{DD18} - 0.3$	$V_{DD18} - 0.15$	V
Change in $V_{OS}$ Between Complementary Output States	$\Delta V_{OS}$	$R_L = 100\Omega \pm 1\%$ $ V_{OS(H)} - V_{OS(L)} $			25	mV
Termination Resistance (Internal)	$R_T$	Any pin to $V_{DD18}$	50	55	60	$\Omega$
<b>DC ELECTRICAL CHARACTERISTICS / GMSL1 REVERSE CHANNEL SERIAL OUTPUTS - <a href="#">Figure 2</a></b>						
Differential High Output Peak Voltage $V_{(SIO_P)} - V_{(SIO_N)}$	$V_{RODH}$	Forward channel disabled STP mode $R_L = 100\Omega$	HIM disabled	30	70	mV
			HIM enabled	50	110	
Differential Low Output Peak Voltage $V_{(SIO_P)} - V_{(SIO_N)}$	$V_{RODL}$	Forward channel disabled STP mode $R_L = 100\Omega$	HIM disabled	-70	-30	mV
			HIM enabled	-110	-50	
Single-Ended High Output Peak Voltage	$V_{ROSH}$	Forward channel disabled coax mode $R_L = 100\Omega$	HIM disabled	30	70	mV
			HIM enabled	50	110	
Single-Ended Low Output Peak Voltage	$V_{ROSL}$	Forward channel disabled coax mode $R_L = 100\Omega$	HIM disabled	-70	-30	mV
			HIM enabled	-110	-50	
Differential Output Offset Voltage ( $V_{(SIO_P)} + V_{(SIO_N)}/2$ )	$V_{OS}$	STP mode	$V_{DD18} - 0.3$	$V_{DD18}$		V
Termination Resistance (Internal)	$R_T$	Any pin to $V_{DD18}$	50	55	60	$\Omega$
<b>DC ELECTRICAL CHARACTERISTICS / C-PHY and D-PHY LP TRANSMITTER</b>						
Thevenin High-Level Output Voltage	$V_{OH}$	<a href="#">Figure 3</a> <a href="#">Figure 6</a>	0.95	1.2	1.3	V
Thevenin Low-Level Output Voltage	$V_{OL}$	<a href="#">Figure 3</a> <a href="#">Figure 6</a>	-50		50	mV
Output Impedance	$Z_{OLP}$		110			$\Omega$

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER</b>						
HS Transmit Static Common-Mode Voltage	$V_{CMTX}$	<a href="#">Figure 3</a>	150	200	250	mV
$V_{CMTX}$ Mismatch when Output is Differential-1 or Differential-0	$ \Delta V_{CMTX(1,0)} $	$\Delta V_{CMTX(1,0)} = (V_{CMTX(1)} - V_{CMTX(0)}) / 2$ <a href="#">Figure 4</a>		5		mV
HS Transmit Differential Voltage	$ V_{OD} $	<a href="#">Figure 5</a>	140	200	270	mV
$V_{OD}$ Mismatch when Output is Differential-1 or Differential-0	$ \Delta V_{OD} $	<a href="#">Figure 4</a>		14		mV
HS Output High Voltage	$V_{OHHS}$	<a href="#">Figure 3</a>		360		mV
Single-Ended Output Impedance	$Z_{OS}$		40	50	62.5	$\Omega$
Single-Ended Output Impedance Mismatch	$\Delta Z_{OS}$			10		%
<b>DC ELECTRICAL CHARACTERISTICS / C-PHY HS TRANSMITTER</b>						
HS Transmit Static Common-Point Voltage	$V_{CPTX}$	$Z_{ID} = 100\Omega$ <a href="#">Figure 6</a>	175	310		mV
$V_{CPTX}$ Mismatch when Output is in any of the Six High-Speed States	$ \Delta V_{CPTX(HS)} $	<a href="#">Figure 7</a>		9		mV
HS Transmit Differential Voltage of the Differential Strong 1 and Strong 0	$ V_{OD} $ strong	$Z_{ID} = 100\Omega$ <a href="#">Figure 8</a>		300		mV
HS Transmit Differential Voltage of the Differential Weak 1 and Weak 0	$ V_{OD} $ weak	$Z_{ID} = 100\Omega$ <a href="#">Figure 8</a>	97			mV
$V_{OD}$ Mismatch Between the Absolute Values of the Differential Strong 1 and Strong 0 Output Voltages in any of the Six Possible High-Speed States	$ \Delta V_{OD} $	<a href="#">Figure 7</a>		17		mV
HS Output High Voltage	$V_{OHHS}$	$Z_{ID} = 100\Omega$ <a href="#">Figure 6</a>		425		mV
Single-Ended Output Impedance	$Z_{OS}$		40	50	60	$\Omega$
Single-Ended Output Impedance Mismatch	$\Delta Z_{OS}$			10		%

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ELECTRICAL CHARACTERISTICS / I/O PINS</b>						
High-Level Input Voltage	$V_{IH}$		$0.7 \times V_{DDIO}$			V
Low-Level Input Voltage	$V_{IL}$			$0.3 \times V_{DDIO}$		V
High-Level Output Voltage	$V_{OH}$	$I_{OH} = -4\text{mA}$		$V_{DDIO} - 0.4$		V
Low-Level Output Voltage	$V_{OL}$	$I_{OL} = 4\text{mA}$		0.4		V
Input Current	$I_{IN}$	All pullup/pulldown devices disabled. $V_{IN} = 0\text{V}$ to $V_{DDIO}$		1		$\mu\text{A}$
Input Capacitance	$C_{IN}$			3		pF
Internal Pullup/Pulldown Resistance	$R_{IN}$	40k $\Omega$ enabled		40		k $\Omega$
		1M $\Omega$ enabled		1		M $\Omega$
<b>DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS</b>						
High-Level Input Voltage	$V_{IH}$		$0.7 \times V_{DDIO}$			V
Low-Level Input Voltage	$V_{IL}$			$0.3 \times V_{DDIO}$		V
Low-Level Open-Drain Output Voltage	$V_{OL}$	$I_{OL} = 4\text{mA}$		0.4		V
Input Current	$I_{IN}$	All pullup/pulldown devices disabled. $V_{IN} = 0\text{V}$ to $V_{DDIO}$		1		$\mu\text{A}$
Input Capacitance	$C_{IN}$			3		pF
Internal Pullup Resistance	$R_{PU}$	40k $\Omega$ enabled		40		k $\Omega$
		1M $\Omega$ enabled		1		M $\Omega$
<b>DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT</b>						
High-Level Input Voltage	$V_{IH}$		$0.7 \times V_{DDIO}$			V
Low-Level Input Voltage	$V_{IL}$			$0.3 \times V_{DDIO}$		V
Input Current	$I_{IN}$	$V_{IN} = 0\text{V}$ to $V_{DDIO}$		6		$\mu\text{A}$
Internal Pulldown Resistance	$R_{PD}$			1		M $\Omega$
Input Capacitance	$C_{IN}$			3		pF
<b>DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS</b>						
High-Level Output Voltage	$V_{OH}$	$I_{OH} = -4\text{mA}$		$V_{DDIO} - 0.4$		V
Low-Level Output Voltage	$V_{OL}$	$I_{OL} = 4\text{mA}$		0.4		V

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ELECTRICAL CHARACTERISTICS / LINE-FAULT DETECTION INPUTS</b>						
Open Pin Voltage	$V_{O0}$	LMN0, LMN2, LMN4, LMN6		1.25		V
	$V_{O1}$	LMN1, LMN3, LMN5, LMN7		0.75		
<b>DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (CRYSTAL) (X1/OSC, X2)</b>						
X1 Input Capacitance	$C_{IN\_X1}$			3		pF
X2 Input Capacitance	$C_{IN\_X2}$			1		pF
Internal X2 Limit Resistor	$R_{LIM}$			1.2		kΩ
Internal Feedback Resistor	$R_{FB}$			10		kΩ
Transconductance	$g_m$			28		mA/V
<b>DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED)</b>						
High-Level Input Voltage	$V_{IH}$		0.9			V
Low-Level Input Voltage	$V_{IL}$			0.4		V
Input Impedance	$R_{IN}$			10		kΩ
X1 Input Capacitance	$C_{IN\_X1}$			3		pF

PRELIMINARY

PRELIMINARY

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENT - GMSL2 MODE (Note 3)</b>						
Supply Current	I <sub>DD1</sub>	4x 3Gbps input 1x 4-lane output 2500Mbps/lane 4 video pipes enabled RGB888 D-PHY	V <sub>TERM</sub>	19	25	mA
			V <sub>DD18</sub>	268	325	
			V <sub>DD</sub> , LDO Disabled	251	750	
			V <sub>DD</sub> , LDO Enabled	240	725	
		4x 3Gbps input 1x 2-lane output 5700Mbps/lane 4 video pipes enabled RGB888 C-PHY	V <sub>TERM</sub>	13	20	
	I <sub>DD2</sub>		V <sub>DD18</sub>	268	325	
			V <sub>DD</sub> , LDO Disabled	315	800	
			V <sub>DD</sub> , LDO Enabled	305	775	
		Replicate mode 4x 3Gbps input 2x 4-lane output 2500Mbps/lane 4 video pipes enabled RGB888 D-PHY	V <sub>TERM</sub>	35	50	
			V <sub>DD18</sub>	268	325	
Maximum V <sub>DDIO</sub> Supply Current (Note 4)	I <sub>DDIO</sub>	Per toggling GPIO, $C_L$ = 20pF	V <sub>DDIO</sub> = 1.8V Range	44	μA/MHz	
			V <sub>DDIO</sub> = 3.3V Range	81		
<b>DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENT - GMSL1 MODE (Note 3)</b>						
Supply Current	I <sub>DD1</sub>	4x 3Gbps input 1x 4-lane output 2500Mbps/lane RGB888 D-PHY	V <sub>TERM</sub>	15.6	25	mA
			V <sub>DD18</sub>	135	190	
			V <sub>DD</sub> , LDO Disabled	93	575	
			V <sub>DD</sub> , LDO Enabled	83	550	
	I <sub>DD2</sub>	Replicate Mode 4x 3Gbps input 2x 4-lane output 2500Mbps/lane RGB888 D-PHY	V <sub>TERM</sub>	29	50	
			V <sub>DD18</sub>	135	190	
			V <sub>DD</sub> , LDO Disabled	100	625	
			V <sub>DD</sub> , LDO Enabled	91	600	

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum $V_{DDIO}$ Supply Current (Note 4)	$I_{DDIO}$	Per toggling GPIO, $C_L$ = 20pF	$V_{DDIO}$ = 1.8V Range		44		$\mu A/MHz$
			$V_{DDIO}$ = 3.3V Range		81		
<b>DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT</b>							
Maximum Power-Down Current	$I_{DD}$	$V_{TERM}$ = 1.26V	$T_A$ = 25°C	< 1			$\mu A$
			$T_A$ = 105°C	< 1			
		$V_{DD18}$ = 1.9V	$T_A$ = 25°C	< 1			
			$T_A$ = 105°C	14			
		$V_{DD}$ = 1.26V	$T_A$ = 25°C	< 1			
			$T_A$ = 105°C	< 1			
		$V_{DDIO}$ = 3.6V	$T_A$ = 25°C	7			
			$T_A$ = 105°C	7			
<b>DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENT</b>							
Maximum Sleep Current	$I_{DD}$	$V_{TERM}$ = 1.26V	$T_A$ = 25°C	< 1			$\mu A$
			$T_A$ = 105°C	< 1			
		$V_{DD18}$ = 1.9V	$T_A$ = 25°C	5			
			$T_A$ = 105°C	19			
		$V_{DD}$ = 1.26V	$T_A$ = 25°C	< 1			
			$T_A$ = 105°C	< 1			
		$V_{DDIO}$ = 3.6V	$T_A$ = 25°C	9			
			$T_A$ = 105°C	9			
<b>AC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD CHANNEL</b>							
Lock Time	$t_{LOCK2}$	(Note 11) <a href="#">Figure 9</a>		45	60	ms	
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from GMSL2 video packets at SIO_ to valid packets at the CSI-2 output (assumes link locked and registers configured)		0.1ms + (6600 x $t_{PCLK}$ )		ms	
Maximum Video Latency	$t_{VL}$	Time from the first pixel in a GMSL2 packet at SIO_ to the first pixel in the CSI-2 output packet. <a href="#">Figure 10</a>		1 video line + (128 x $t_{PCLK}$ )		s	
PWDNB Hold Time	$t_{HOLD\_PWDNB}$	The minimum duration PWDNB must be held LOW to reset the device.		1		ms	
<b>AC ELECTRICAL CHARACTERISTICS / GMSL2 REVERSE CHANNEL</b>							
GMSL Reverse Channel Transmitter Rise/Fall Time	$t_R, t_F$	20% to 80%, $V_O$ = 250mV, $R_L$ = 100Ω		2300		ps	

PRELIMINARY

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Serial Output p-p Jitter	$t_{TSOJ}$	PRBS7, single-ended or differential output		0.15		UI
Deterministic Serial Output p-p Jitter	$t_{DSOJ}$	PRBS7, single-ended or differential output		0.1		UI
GPI-GPO Delay Reverse Path	$t_{GPDR}$	Delay-Compensated Mode <a href="#">Table 4</a> <a href="#">Figure 11</a>		15		$\mu s$
		Non-Delay-Compensated Mode <a href="#">Table 4</a> <a href="#">Figure 11</a>		6		
GPI-GPO Skew Reverse Path	$t_{SKEW}$	Delay-Compensated Mode <a href="#">Figure 11</a>		7		ns
<b>AC ELECTRICAL CHARACTERISTICS / GMSL1</b>						
Maximum Lock Time	$t_{LOCK1}$	<a href="#">Figure 12</a>		4		ms
Maximum Power-up Time	$t_{PU}$	<a href="#">Figure 13</a>		8.5		ms
Maximum Video Latency	$t_{VL}$	Time from the first pixel in a video line at SIO_ to the first pixel in the CSI-2 output packet <a href="#">Figure 14</a>		1 video line + (128 x $t_{PCLK}$ )		s
PWDNB Hold Time	$t_{HOLD\_PWDNB}$	The minimum duration PWDNB must be held LOW to reset the device		1		ms
Reverse Control-Channel Output Rise Time	$t_R$	No forward channel data transmission <a href="#">Figure 2</a> (Note 2)	100	400		ns
Reverse Control-Channel Output Fall Time	$t_F$	No forward channel data transmission <a href="#">Figure 2</a> (Note 2)	100	400		ns
GPI-to-GPO Delay	$t_{GPIO}$	Deserializer GPI to serializer GPO (cable delay not included) <a href="#">Figure 15</a> (Note 2)		350		$\mu s$
<b>AC ELECTRICAL CHARACTERISTICS / C-PHY and D-PHY LP TRANSMITTER (Note 2)</b>						
15% to 85% Rise Time and Fall Time	$t_{RLP}/t_{FLP}$	(Note 5)		25		ns
30% to 85% Rise Time	$t_{REOT}$	<a href="#">Figure 16</a> , <a href="#">Figure 20</a> (Note 6)		35		ns
Load Capacitance	$C_{LOAD}$	(Note 5)	0	70		pF
<b>AC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER (Note 2)</b>						
Common-Level Variations, HF	$\Delta V_{CMTX(HF)}$	> 450MHz <a href="#">Figure 4</a>		15		$mV_{RMS}$
Common-Level Variations, LF	$\Delta V_{CMTX(LF)}$	50MHz to 450MHz <a href="#">Figure 4</a>		25		$mV_{PEAK}$

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
20%-80% Rise Time and Fall Time	$t_R$ and $t_F$			0.4		UI
			50			ps
Differential-Mode Reflection Coefficient (Note 7)	$S_{dd,TX}$	$f_h\text{MAX} = 1.25\text{GHz}$		-4.5		dB
		$f\text{MAX} = 1.875\text{GHz}$		-2.5		
Common-Mode Reflection Coefficient (Note 7)	$S_{cc,TX}$	$f\text{MAX} = 1.875\text{GHz}$		-2.5		dB
Data Lane Bit Rate	$D_{L,BR}$		80	2500		Mbps
Clock Lane Frequency	$CL_{FREQ}$		40	1250		MHz
CSI-2 Output Inter-packet Spacing	$t_{SPACE}$		300ns + 370UI			ns

**AC ELECTRICAL CHARACTERISTICS / D-PHY DATA-CLOCK TIMING (Note 2)**

UI Instantaneous	$UI_{INST}$		0.4	12.5	ns
UI Variation	$\Delta UI$	$UI \geq 1\text{ns}$ within a single burst	-10%	10%	UI
		$0.667\text{ns} \leq UI \leq 1\text{ns}$ within a single burst	-5%	5%	
Data to Clock Skew	$t_{SKEW}$	0.08 to 1.0Gbps ( <a href="#">Figure 17</a> )	-0.15	0.15	$UI_{INST}$
		> 1.0Gbps to 1.5Gbps ( <a href="#">Figure 17</a> )	-0.2	0.2	
Static Data to Clock Skew	$t_{SKEW}$ Static	> 1.5Gbps ( <a href="#">Figure 17</a> )	-0.2	0.2	$UI_{INST}$
Dynamic Data to Clock Skew	$t_{SKEW}$ Dynamic	> 1.5Gbps ( <a href="#">Figure 17</a> )	-0.15	0.15	$UI_{INST}$

**AC ELECTRICAL CHARACTERISTICS / D-PHY GLOBAL OPERATION TIMING (Note 2)**

Time that the HS Clock must be Driven by the Transmitter Prior to any Associated Data Lane Beginning the Transition from LP to HS Mode	$t_{CLK-PRE}$	<a href="#">Figure 19</a>	8		UI
Time that the Transmitter Drives the Clock Lane LP-00 Line State Immediately Before the HS-0 Line State Starting the HS Transmission	$t_{CLK-PREPARE}$	<a href="#">Figure 19</a>	38	95	ns
$t_{CLK-PREPARE} +$ Time that the Transmitter Drives the HS-0 State Prior to Starting the Clock	$t_{CLK-PREPARE} + t_{CLK-ZERO}$	<a href="#">Figure 19</a>	300		ns

**Electrical Characteristics (continued)**

( $V_{TERM} = 1.14V$  to  $1.26V$ ,  $V_{DD18} = 1.7V$  to  $1.9V$ ,  $V_{DD} = 0.95V$  to  $1.05V$  or  $V_{DD} = 1.14V$  to  $1.26V$ ,  $V_{DDIO} = 1.7V$  to  $3.6V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ , EP connected to PCB ground, typical values are at  $V_{TERM} = 1.2V$ ,  $V_{DD18} = V_{DDIO} = 1.8V$ ,  $V_{DD} = 1.0V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitted Time Interval from the Start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ , to the Start of the LP-11 State Following a HS Burst	$t_{EOT}$	<a href="#">Figure 16</a> , <a href="#">Figure 18</a> , <a href="#">Figure 19</a>			$105 + 12xUI$	ns
Time that the Transmitter Drives LP-11 Following a HS Burst	$t_{HS-EXIT}$	<a href="#">Figure 16</a> , <a href="#">Figure 18</a> , <a href="#">Figure 19</a>	100			ns
Time that the Transmitter Drives the Data Lane LP-00 Line State Immediately Before the HS-0 Line State Starting the HS Transmission	$t_{HS-PREPARE}$	<a href="#">Figure 16</a> , <a href="#">Figure 18</a> , <a href="#">Figure 19</a>	$40 + 4xUI$		$85 + 6xUI$	ns
$T_{HS-PREPARE} +$ Time that the Transmitter Drives the HS-0 State Prior to Transmitting the Sync Sequence	$t_{HS-PREPARE} + t_{HS-ZERO}$	<a href="#">Figure 16</a>	$145 + 10xUI$			ns
Time that the Transmitter Drives the Flipped Differential State After Last Payload Data Bit of a HS Transmission Burst	$t_{HS-TRAIL}$	<a href="#">Figure 16</a> , <a href="#">Figure 18</a>	$60 + 4xUI$			ns
Initialization Time	$t_{INIT}$		100			$\mu s$
Transmitted Length of any Low-Power State Period	$t_{LPX}$	<a href="#">Figure 16</a> , <a href="#">Figure 18</a> , <a href="#">Figure 19</a>	50			ns
Time that the Transmitter Drives the Skew-Calibration Sync Pattern, 0xFFFF	$t_{SKEWCAL\_SYNC}$	<a href="#">Figure 18</a>		16		UI
Time that the Transmitter Drives the Skew-Calibration Pattern in the Initial Skew-Calibration Mode	$t_{SKEWCAL}$	<a href="#">Figure 18</a>		100		$\mu s$
		<a href="#">Figure 18</a>	$2^{15}$			UI
Time that the Transmitter Drives the Skew-Calibration Pattern in the Periodic Skew-Calibration Mode	$t_{SKEWCAL}$	<a href="#">Figure 18</a>		10		$\mu s$
		<a href="#">Figure 18</a>	$2^{10}$			UI

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AC ELECTRICAL CHARACTERISTICS / C-PHY HS TRANSMITTER (Note 2)</b>						
Common-Level Variations	$\Delta V_{CPTX(HF)}$	> 450MHz		15		mVRMS
	$\Delta V_{CPTX(LF)}$	50MHz to 450MHz		25		mVPEAK
Rise Time	$t_R$	Strong 0 to Weak 1 transition, -58mV to +58mV, $Z_{ID}$ = 100Ω		0.285		UI
Fall Time	$t_F$	Strong 1 to Weak 0 transition, +58mV to -58mV, $Z_{ID}$ = 100Ω		0.285		UI
Rise Time and Fall Time Limit	$t_{RISE-FALL-MAX}$	-58mV to +58mV, $Z_{ID}$ = 100Ω (Note 9)		360		ps
Differential-Mode Reflection Coefficient (Note 8)	$S_{dd,TX}$	$f_{hMAX} = 1.25\text{GHz}$		-5		dB
Common-Mode Reflection Coefficient (Note 8)		$f_{MAX} = 1.875\text{GHz}$		-3		
C-PHY Lane Bit Rate	$C_{BR}$		182	5700		Mbps
CSI-2 Output Inter-Packet Spacing	$t_{SPACE}$			300ns + 370UI		ns
UI Instantaneous	$UI_{INST}$		0.4	12.5		ns
<b>AC ELECTRICAL CHARACTERISTICS / C-PHY GLOBAL OPERATION TIMING - <a href="#">Figure 20</a> (Note 2)</b>						
Time that the Transmitter Drives the 3-Wire LP-000 Line State Immediately Before the HS_+x Line State Starting the HS Transmission	$t_{3-PREPARE}$		38	95		ns
Time that the Transmitter Drives LP-111 Following a HS Burst	$t_{3-HS-EXIT}$		100			ns
Transmitted Length of any Low-Power State Period	$t_{LPX}$		50			ns
Initialization Time	$t_{INIT}$		100			μs
<b>AC ELECTRICAL CHARACTERISTICS / I<sup>2</sup>C/UART PORT TIMING</b>						
Output Fall Time	$t_F$	70% to 30%, $C_L$ = 20pF to 100pF, 1kΩ pullup to $V_{DDIO}$ (Note 2)	$20 \times V_{DDIO}/5.$ 5V	150		ns
I <sup>2</sup> C/UART Wake Time	$t_{WAKEUP}$	From power-up, or rising edge of PWDNB to local register access. For remote register access, I <sup>2</sup> C/UART wake time is the same as lock time ( $t_{LOCK\_}$ ).		2.25		ms

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AC ELECTRICAL CHARACTERISTICS / I<sup>2</sup>C TIMING - <a href="#">Figure 21</a></b>						
SCL Clock Frequency	f <sub>SCL</sub>	Low f <sub>SCL</sub> range: (I2C_MST_BT = 010, I2C_SLV_SH = 10)	9.6	100		kHz
		Mid f <sub>SCL</sub> range: (I2C_MST_BT = 101, I2C_SLV_SH = 01)	100	400		
		High f <sub>SCL</sub> range: (I2C_MST_BT = 111, I2C_SLV_SH = 00)	400	1000		
Start Condition Hold Time	t <sub>HD:STA</sub>	f <sub>SCL</sub> range, low	4			μs
		f <sub>SCL</sub> range, mid	0.6			
		f <sub>SCL</sub> range, high	0.26			
Low Period of SCL Clock	t <sub>LOW</sub>	f <sub>SCL</sub> range, low	4.7			μs
		f <sub>SCL</sub> range, mid	1.3			
		f <sub>SCL</sub> range, high	0.5			
High Period of SCL Clock	t <sub>HIGH</sub>	f <sub>SCL</sub> range, low	4			μs
		f <sub>SCL</sub> range, mid	0.6			
		f <sub>SCL</sub> range, high	0.26			
Repeated Start Condition Setup Time	t <sub>SU:STA</sub>	f <sub>SCL</sub> range, low	4.7			μs
		f <sub>SCL</sub> range, mid	0.6			
		f <sub>SCL</sub> range, high	0.26			
Data Hold Time	t <sub>HD:DAT</sub>	f <sub>SCL</sub> range, low	0			ns
		f <sub>SCL</sub> range, mid	0			
		f <sub>SCL</sub> range, high	0			
Data Setup Time	t <sub>SU:DAT</sub>	f <sub>SCL</sub> range, low	250			ns
		f <sub>SCL</sub> range, mid	100			
		f <sub>SCL</sub> range, high	50			
Setup Time for Stop Condition	t <sub>SU:STO</sub>	f <sub>SCL</sub> range, low	4			μs
		f <sub>SCL</sub> range, mid	0.6			
		f <sub>SCL</sub> range, high	0.26			
Bus Free Time	t <sub>BUF</sub>	f <sub>SCL</sub> range, low	4.7			μs
		f <sub>SCL</sub> range, mid	1.3			
		f <sub>SCL</sub> range, high	0.5			
Data Valid Time	t <sub>VD:DAT</sub>	f <sub>SCL</sub> range, low		3.45		μs
		f <sub>SCL</sub> range, mid		0.9		
		f <sub>SCL</sub> range, high		0.45		
Data Valid Acknowledge Time	t <sub>VD:ACK</sub>	f <sub>SCL</sub> range, low		3.45		μs
		f <sub>SCL</sub> range, mid		0.9		
		f <sub>SCL</sub> range, high		0.45		

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Width of Spikes Suppressed	$t_{SP}$	$f_{SCL}$ range, low		50		ns
		$f_{SCL}$ range, mid		50		
		$f_{SCL}$ range, high		50		
Capacitive Load On Each Bus Line	$C_B$	(Note 2)		100		pF
<b>AC ELECTRICAL CHARACTERISTICS / SPI MASTER - <a href="#">Figure 22</a> (Note 10)</b>						
Operating Frequency	$f_{MCK}$	(Note 2)	0.588	25		MHz
SCLK Period	$t_{MCK}$			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	$t_{MCH}, t_{MCL}$	(Note 2)	$t_{MCK}/2 - 3$	$t_{MCK}/2$		ns
MOSI Data Output Delay	$t_{MOD}$	After SCLK Falling Edge (Note 2)	-2.3	2.3		ns
MISO Input Setup Time	$t_{MIS}$	Before Programmed Sampling Edge (Note 2)	13.5			ns
MISO Input Hold Time	$t_{MIH}$	After Programmed Sampling Edge (Note 2)	-2			ns
<b>AC ELECTRICAL CHARACTERISTICS / SPI SLAVE <a href="#">Figure 23</a> (Note 10)</b>						
Operating Frequency	$f_{SCK}$	(Note 2)		50		MHz
SCLK Period	$t_{SCK}$			$1/f_{SCK}$		ns
MISO Data Output Delay	$t_{SOD}$	After SCLK Falling Edge (Note 2)	2.0	11.3		ns
MOSI Input Setup Time	$t_{SIS}$	Before SCLK Rising Edge (Note 2)	5			ns
MOSI Input Hold Time	$t_{SIH}$	After SCLK Rising Edge (Note 2)	3			ns
<b>AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (CRYSTAL)(X1/OSC, X2) (Note 2)</b>						
Frequency	$f_{XTAL}$		25			MHz
Frequency Stability + Frequency Tolerance	$f_{TN}$			$\pm 200$		ppm
<b>AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1/OSC, X2 UNCONNECTED) (Note 2)</b>						
Frequency	$f_{REF}$		25			MHz
Frequency Stability + Frequency Tolerance	$f_{TN}$			$\pm 200$		ppm
Input Jitter		Link Speed = 3Gbps/187.5Mbps sinusoidal jitter < 1MHz (falling edge) upstream serializer using crystal reference		600		ps p-p
Input Duty Cycle	$t_{DUTY}$		40	60		%
Input Fall Time	$t_F$	80% to 20%		4		ns

**Electrical Characteristics (continued)**

( $V_{TERM}$  = 1.14V to 1.26V,  $V_{DD18}$  = 1.7V to 1.9V,  $V_{DD}$  = 0.95V to 1.05V or  $V_{DD}$  = 1.14V to 1.26V,  $V_{DDIO}$  = 1.7V to 3.6V,  $T_A$  = -40°C to +105°C, EP connected to PCB ground, typical values are at  $V_{TERM}$  = 1.2V,  $V_{DD18}$  =  $V_{DDIO}$  = 1.8V,  $V_{DD}$  = 1.0V,  $T_A$  = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ESD PROTECTION</b>						
SIO__	$V_{ESD}$	Human Body Model (HBM), $R_D$ = 1.5kΩ, $C_S$ = 100pF	±8			kV
		ISO10605, $R_D$ = 330Ω, $C_S$ = 150pF, Contact Discharge, Coax Configuration	±6			
		ISO10605, $R_D$ = 330Ω, $C_S$ = 150pF, Contact Discharge, STP Configuration	±4			
		ISO10605, $R_D$ = 330Ω, $C_S$ = 150pF, Air Discharge	±8			
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)	750			V
All Other Pins	$V_{ESD}$	Human Body Model (HBM), $R_D$ = 1.5kΩ, $C_S$ = 100pF	±4			kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)	750			V

**Note 5:** Limits are 100% tested at  $T_A$  = +105°C unless otherwise noted. Limits within the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

**Note 6:** Not production tested. Guaranteed by design and characterization.

**Note 7:** Color bar pattern. For  $V_{TERM}/V_{DD}/V_{DD18}$  supply current specifications,  $V_{DDIO}$  = 1.8V/3.3V typ/max. For  $V_{TERM}/V_{DD18}/V_{DDIO}$  supply current specifications,  $V_{DD}$  = 1V.

**Note 8:** MFP pin speed programmed to fastest setting (TTS = 00). See Multifunction Pin Configuration for details regarding MFP speed programming.

**Note 9:**  $C_{LOAD}$  includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

**Note 10:** Additional capacitance up to 60pF (D-PHY) or 90pF (C-PHY) at RX termination center tap.

**Note 11:** Differential-mode and common-mode reflection coefficient are compliant with MIPI D-PHY V1.2 requirements over all specified operating frequencies.

**Note 12:** Differential-mode and common-mode reflection coefficient are compliant with MIPI C-PHY V1.0 requirements over all specified operating frequencies.

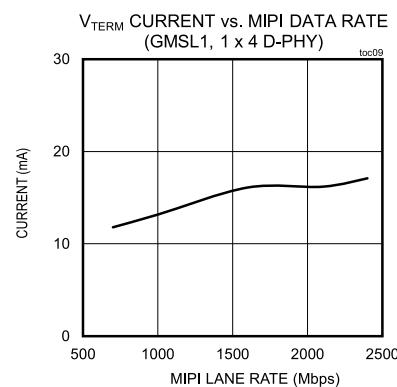
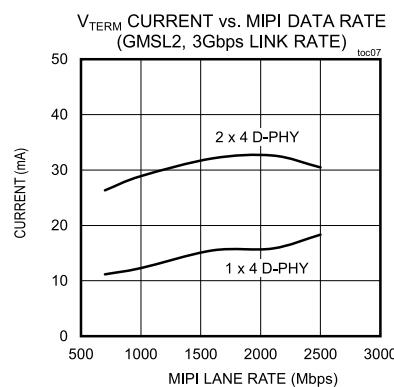
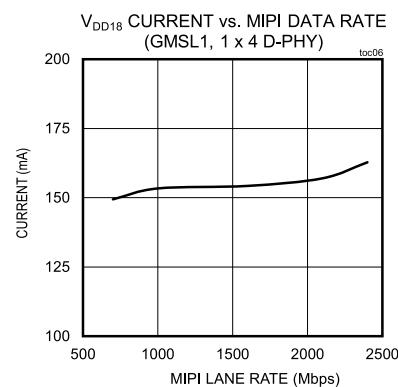
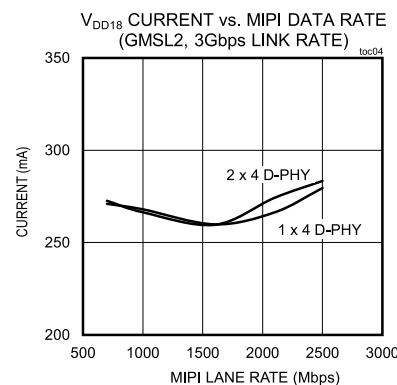
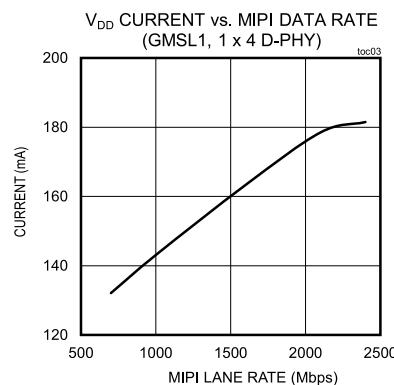
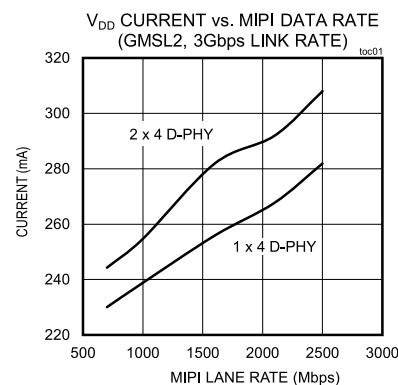
**Note 13:** For rates ≤ 1.5Gbps,  $t_R$  and  $t_F$  shall be ≤ min (0.4UI, t<sub>RISE-FALL-MAX</sub>)

**Note 14:** Measured at 50MHz. For  $V_{DDIO} < 2.25V$ , speed group A and C TTS = 00 and for  $V_{DDIO} \geq 2.25V$ , speed group A and C TTS = 01. See Multifunction Pin Configuration for details regarding MFP speed programming.

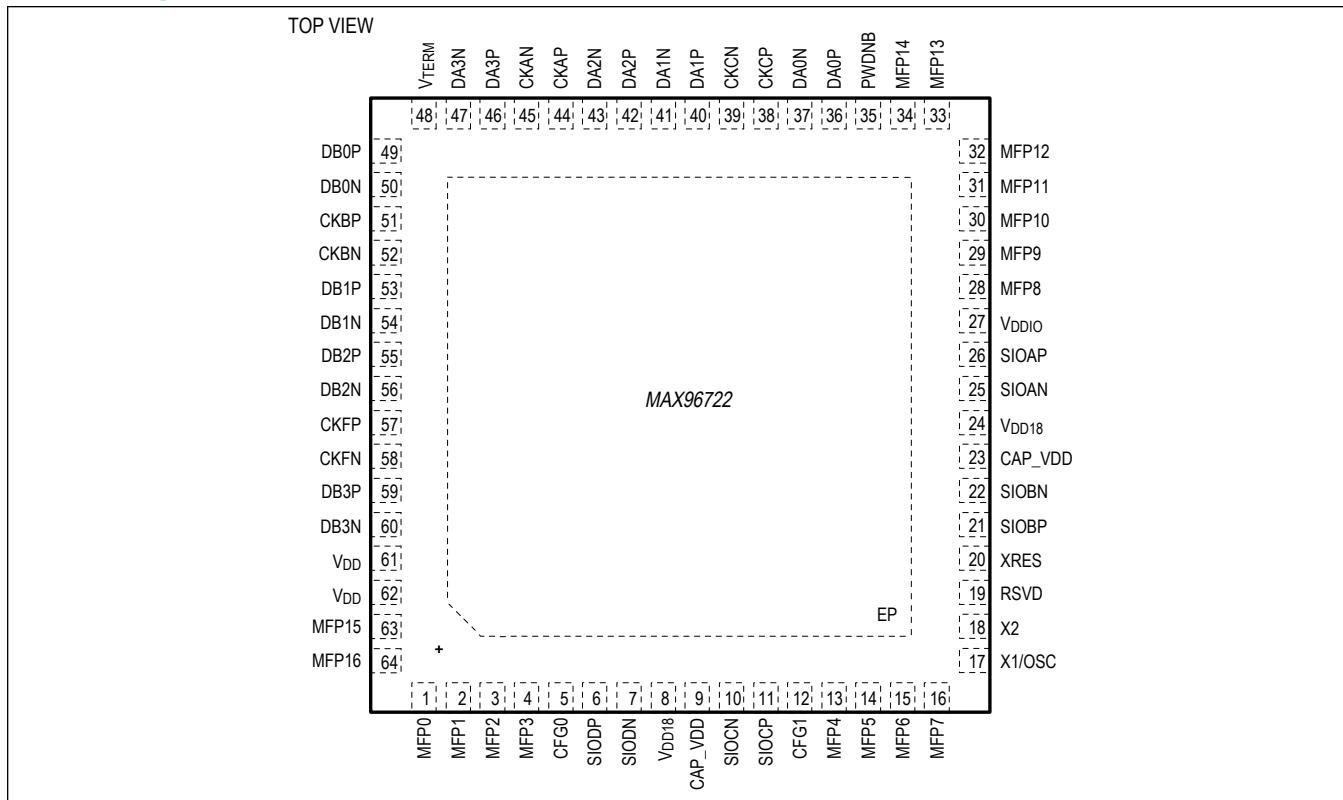
**Note 15:** Production tested using ECS ECS-250-18-33Q-DS crystal.

## Typical Operating Characteristics

( $V_{TERM} = 1.2V$ ,  $V_{DD18} = 1.8V$ ,  $V_{DDIO} = 3.3V$ ,  $V_{DD} = 1.0V$ , Coax Mode, RGB888 video format, all GMSL links active with identical configuration, dual port MIPI configurations utilize replication,  $T_A = +25^\circ C$ , unless otherwise noted.)



**PRELIMINARY**

**Pin Configuration****Pin Description**

PIN	NAME	FUNCTION MODE	FUNCTION
<b>GMSL2/GMSL1 SERIAL LINK</b>			
26	SIOAP	SIOAP	Noninverted Coax/Twisted-Pair Serial-Data I/O A.
25	SIOAN	SIOAN	Inverted Twisted-Pair Serial-Data I/O A.
21	SIOBP	SIOBP	Noninverted Coax/Twisted-Pair Serial-Data I/O B.
22	SIOBN	SIOBN	Inverted Twisted-Pair Serial-Data I/O B.
11	SIOCP	SIOCP	Noninverted Coax/Twisted-Pair Serial-Data I/O C.
10	SIOCN	SIOCN	Inverted Twisted-Pair Serial-Data I/O C.
6	SIODP	SIODP	Noninverted Coax/Twisted-Pair Serial-Data I/O D.
7	SIODN	SIODN	Inverted Twisted-Pair Serial-Data I/O D.

**PRELIMINARY**

PIN	NAME	FUNCTION MODE	FUNCTION	
<b>CSI-2 INTERFACE - PORT A/C/D (* denotes default state after power-up)</b>				
36	DA0P	DA0P* DC0P A0A C0A	DA0P* DC0P A0A C0A	DA0P: D-PHY Port A Data Lane 0 Noninverted Output (4-lane mode).  DC0P: D-PHY Port C Data Lane 0 Noninverted Output (2-lane mode).  A0A: C-PHY Port A Lane 0 Output A (4-lane mode).  C0A: C-PHY Port C Lane 0 Output A (2-lane mode).
37	DA0N	DA0N* DC0N A0B C0B	DA0N* DC0N A0B C0B	DA0N: D-PHY Port A Data Lane 0 Inverted Data Output (4-lane mode).  DC0N: D-PHY Port C Data Lane 0 Inverted Output (2-lane mode).  A0B: C-PHY Port A Lane 0 Output B (4-lane mode).  C0B: C-PHY Port C Lane 0 Output B (2-lane mode).
40	DA1P	DA1P* DC1P A1B C1B	DA1P* DC1P A1B C1B	DA1P: D-PHY Port A Data Lane 1 Noninverted Output (4-lane mode).  DC1P: D-PHY Port C Data Lane 1 Noninverted Output (2-lane mode).  A1B: C-PHY Port A Lane 1 Output B (4-lane mode).  C1B: C-PHY Port C Lane 1 Output B (2-lane mode).
41	DA1N	DA1N* DC1N A1C C1C	DA1N* DC1N A1C C1C	DA1N: D-PHY Port A Data Lane 1 Inverted Output (4-lane mode).  DC1N: D-PHY Port C Data Lane 1 Inverted Output (2-lane mode).  A1C: C-PHY Port A Lane 1 Output C (4-lane mode).  C1C: C-PHY Port C Lane 1 Output C (2-lane mode).
42	DA2P	DA2P* DD0P A2A D0A	DA2P* DD0P A2A D0A	DA2P: D-PHY Port A Data Lane 2 Noninverted Output (4-lane mode).  DD0P: D-PHY Port D Data Lane 0 Noninverted Output (2-lane mode).  A2A: C-PHY Port A Lane 2 Output A (4-lane mode).  D0A: C-PHY Port D Lane 0 Output A (2-lane mode).

**PRELIMINARY**

PIN	NAME	FUNCTION MODE		FUNCTION
43	DA2N	DA2N* DD0N A2B D0B	DA2N* DD0N A2B D0B	DA2N: D-PHY Port A Data Lane 2 Inverted Output (4-lane mode). DD0N: D-PHY Port D Data Lane 0 Inverted Output (2-lane mode). A2B: C-PHY Port A Lane 2 Output B (4-lane mode). D0B: C-PHY Port D Lane 0 Output B (2-lane mode).
46	DA3P	DA3P* DD1P A3B D1B	DA3P* DD1P A3B D1B	DA3P: D-PHY Port A Data Lane 3 Noninverted Output (4-lane mode). DD1P: D-PHY Port D Data Lane 1 Noninverted output (2-lane mode). A3B: C-PHY Port A Lane 3 Output B (4-lane mode). D1B: C-PHY Port D Lane 1 Output B (2-lane mode).
47	DA3N	DA3N* DD1N A3C D1C	DA3N* DD1N A3C D1C	DA3N: D-PHY Port A Data Lane 3 Inverted Output (4-lane mode). DD1N: D-PHY Port D Data Lane 1 Inverted Output (2-lane mode). A3C: C-PHY Port A Lane 3 Output C (4-lane mode). D1C: C-PHY Port D Lane 1 Output C (2-lane mode).
44	CKAP	CKAP* CKDP DISABLED A2C D0C	CKAP* CKDP DISABLED A2C D0C	CKAP: D-PHY Port A Clock Lane Noninverted Output (4-lane mode). CKDP: D-PHY Port D Clock Lane Noninverted Output (2-lane mode). DISABLED: D-PHY Clock Output Function is Disabled in 4-Lane Mode When CKAP/N(alt) Function is Enabled, and CKAP/N Pins Drive D-PHY LP00 State. Port A clock output is driven from CKCP/N pins. A2C: C-PHY Port A Lane 2 Output C (4-lane mode). D0C: C-PHY Port D Lane 0 Output C (2-lane mode).

**PRELIMINARY**

PIN	NAME	FUNCTION MODE	FUNCTION
45	CKAN	CKAN* CKDN DISABLED A3A D1A	CKAN: D-PHY Port A Clock Lane Inverted Output (4-lane mode). CKDN: D-PHY Port D Clock Lane Inverted Output (2-lane mode). DISABLED: D-PHY Clock Output Function is Disabled in 4-Lane Mode When CKAP/N(alt) Function is Enabled, and CKAP/N Pins Drive D-PHY LP00 State. Port A clock output is driven from CKCP/N pins. A3A: C-PHY Port A Lane 3 Output A (4-lane mode). D1A: C-PHY Port D Lane 1 Output A (2-lane mode).
38	CKCP	DISABLED* CKCP CKAP(alt) A0C C0C	DISABLED: D-PHY Clock Output Function is Disabled by Default in 4-Lane Mode, and CKCP/N Pins Drive D-PHY LP00 State. Port A clock output is driven from CKAP/N pins. CKCP: D-PHY Port C Clock Lane Noninverted Output (2-lane mode). CKAP(alt): D-PHY Port A Clock Lane Noninverted Output Alternate (4-lane mode). When CKAP/N(alt) function is enabled, CKAP/N pins drive D-PHY LP00 state. A0C: C-PHY Port A Lane 0 Output C (4-lane mode). C0C: C-PHY Port C Lane 0 Output C (2-lane mode).
39	CKCN	DISABLED* CKCN CKAN(alt) A1A C1A	DISABLED: D-PHY Clock Output Function is Disabled by Default in 4-Lane Mode, and CKCP/N Pins Drive D-PHY LP00 State. Port A clock output is driven from CKAP/N pins. CKCN: D-PHY Port C Clock Lane Inverted Output (2-lane mode). CKAN(alt): D-PHY Port A Clock Lane Inverted Output Alternate (4-lane mode). When CKAP/N(alt) function is enabled, CKAP/N pins drive D-PHY LP00 state. A1A: C-PHY Port A Lane 1 Output A (4-lane mode). C1A: C-PHY Port C Lane 1 Output A (2-lane mode).

**PRELIMINARY**

PIN	NAME	FUNCTION MODE	FUNCTION	
<b>CSI-2 INTERFACE - PORT B/E/F (* denotes default state after power-up)</b>				
49	DB0P	DB0P* DE0P B0A E0A	DB0P* DE0P B0A E0A	DB0P: D-PHY Port B Data Lane 0 Noninverted Output (4-lane mode).  DE0P: D-PHY Port E Data Lane 0 Noninverted Output (2-lane mode).  B0A: C-PHY Port B Lane 0 Output A (4-lane mode).  E0A: C-PHY Port E Lane 0 Output A (2-lane mode).
50	DB0N	DB0N* DE0N B0B E0B	DB0N* DE0N B0B E0B	DB0N: D-PHY Port B Data Lane 0 Inverted Output (4-lane mode).  DE0N: D-PHY Port E Data Lane 0 Inverted Output (2-lane mode).  B0B: C-PHY Port B Lane 0 Output B (4-lane mode).  E0B: C-PHY Port E Lane 0 Output B (2-lane mode).
53	DB1P	DB1P* DE1P B1B E1B	DB1P* DE1P B1B E1B	DB1P: D-PHY Port B Data Lane 1 Noninverted Output (4-lane mode).  DE1P: D-PHY Port E Data Lane 1 Noninverted Output (2-lane mode).  B1B: C-PHY Port B Lane 1 Output B (4-lane mode).  E1B: C-PHY Port E Lane 1 Output B (2-lane mode).
54	DB1N	DB1N* DE1N B1C E1C	DB1N* DE1N B1C E1C	DB1N: D-PHY Port B Data Lane 1 Inverted Output (4-lane mode).  DE1N: D-PHY Port E Data Lane 1 Inverted Output (2-lane mode).  B1C: C-PHY Port B Lane 1 Output C (4-lane mode).  E1C: C-PHY Port E Lane 1 Output C (2-lane mode).
55	DB2P	DB2P* DF0P B2A F0A	DB2P* DF0P B2A F0A	DB2P: D-PHY Port B Data Lane 2 Noninverted Output (4-lane mode).  DF0P: D-PHY Port F Data Lane 0 Noninverted Output (2-lane mode).  B2A: C-PHY Port B Lane 2 Output A (4-lane mode).  F0A: C-PHY Port F Lane 0 Output A (2-lane mode).

**PRELIMINARY**

PIN	NAME	FUNCTION MODE		FUNCTION
56	DB2N	DB2N* DF0N B2B F0B	DB2N* DF0N B2B F0B	DB2N: D-PHY Port B Data Lane 2 Inverted Output (4-lane mode). DF0N: D-PHY Port F Data Lane 0 Inverted Output (2-lane mode). B2B: C-PHY Port B Lane 2 Output B (4-lane mode). F0B: C-PHY Port F Lane 0 Output B (2-lane mode).
59	DB3P	DB3P* DF1P B3B F1B	DB3P* DF1P B3B F1B	DB3P: D-PHY Port B Data Lane 3 Noninverted Output (4-lane mode). DF1P: D-PHY Port F Data Lane 1 Noninverted Output (2-lane mode). B3B: C-PHY Port B Lane 3 Output B (4-lane mode). F1B: C-PHY Port F Lane 1 Output B (2-lane mode).
60	DB3N	DB3N* DF1N B3C F1C	DB3N* DF1N B3C F1C	DB3N: D-PHY Port B Data Lane 3 Inverted Output (4-lane mode). DF1N: D-PHY Port F Data Lane 1 Inverted Output (2-lane mode). B3C: C-PHY Port B Lane 3 Output C (4-lane mode). F1C: C-PHY Port F Lane 1 Output C (2-lane mode).
51	CKBP	CKBP* CKEP DISABLED B0C E0C	CKBP* CKEP DISABLED B0C E0C	CKBP: D-PHY Port B Clock Lane Noninverted Output (4-lane mode). CKEP: D-PHY Port E Clock Lane Noninverted Output (2-lane mode). DISABLED: D-PHY Clock Output Function is Disabled in 4-Lane Mode When CKBP/N(alt) Function is Enabled, and CKBP/N Pins Drive D-PHY LP00 State. Port B clock output is driven from CKFP/N pins. B0C: C-PHY Port B Lane 0 Output C (4-lane mode). E0C: C-PHY Port E Lane 0 Output C (2-lane mode).

**PRELIMINARY**

PIN	NAME	FUNCTION MODE	FUNCTION
52	CKBN	CKBN* CKEN DISABLED B1A E1A	CKBN: D-PHY Port B Clock Lane Inverted Output (4-lane mode).  CKEN: D-PHY Port E Clock Lane Inverted Output (2-lane mode).  DISABLED: D-PHY Clock Output Function is Disabled in 4-Lane Mode When CKBP/N(alt) Function is Enabled, and CKBP/N Pins Drive D-PHY LP00 State. Port B clock output is driven from CKFP/N pins.  B1A: C-PHY Port B Lane 1 Output A (4-lane mode).  E1A: C-PHY Port E Lane 1 Output A (2-lane mode).
57	CKFP	DISABLED* CKFP CKBP(alt) B2C F0C	DISABLED: D-PHY Clock Output Function is Disabled by Default in 4-Lane Mode, and CKFP/N Pins Drive D-PHY LP00 State. Port B clock output is driven from CKBP/N pins  CKFP: D-PHY Port F Clock Lane Noninverted Output (2-lane mode).  CKBP(alt): D-PHY Port B Clock Lane Noninverted Output Alternate (4-lane mode). When CKBP/N(alt) function is enabled, CKBP/N pins drive D-PHY LP00 state.  B2C: C-PHY Port B Lane 2 Output C (4-lane mode).  F0C: C-PHY Port F Lane 0 Output C (2-lane mode).
58	CKFN	DISABLED* CKFN CKBN(alt) B3A F1A	DISABLED: D-PHY Clock Output Function is Disabled by Default in 4-Lane Mode, and CKFP/N Pins Drive D-PHY LP00 State. Port B clock output is driven from CKBP/N pins  CKFN: D-PHY Port F Clock Lane Inverted Output (2-lane mode).  CKBN(alt): D-PHY Port B Clock Lane Inverted Output Alternate (4-lane mode). When CKBP/N(alt) function is enabled, CKBP/N pins drive D-PHY LP00 state.  B3A: C-PHY Port B Lane 3 Output A (4-lane mode).  F1A: C-PHY Port F Lane 1 Output A (2-lane mode).

PIN	NAME	FUNCTION MODE		FUNCTION
<b>MULTIFUNCTION PINS</b> (* denotes default state after power-up) (** GMSL1 has limited GPIO tunneling capability; generic GPIO functions are accessible by register read/write only)				
1	MFP0	MS LMN6 GPIO0*	MS LMN6 GPIO0(**)**	MS: UART Mode Select with Internal 1MΩ Pulldown to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be temporarily overwritten by a register write.  LMN6: Line-Fault Monitor Input 6. Use in conjunction with L MN7 for STP applications.  GPIO0: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
2	MFP1	LOCK* GPIO1	LOCK* GPIO1**	LOCK: Open-Drain Lock Indication Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> .  GPIO1: Configurable General Purpose Input or Output.
3	MFP2	FSYNC GPIO2*	FSYNC GPIO1 GPIO2(**)**	FSYNC: Frame Sync Output (master) or Input (slave).  GPIO1: CMOS Input for Dedicated GPI-GPO Sync Signal GPIO1 in GMSL1 Mode.  GPIO2: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
4	MFP3	ERRB* GPIO3	ERRB* GPIO3**	ERRB: Open-Drain Error Indication Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> . ERRB = low indicates that a data error or interrupt has been detected.  GPIO3: Configurable General Purpose Input or Output.
13	MFP4	SDA2* RX2* VS GPIO4	SDA2* RX2* GPIO VS GPIO4**	SDA2: Port 2 I <sup>2</sup> C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SDA or RX specified by I2CSEL/MFP13 at power-up).  RX2: Port 2 UART Input (SDA or RX specified by I2CSEL/MFP13 at power-up).  GPIO0: CMOS Input for Dedicated GPI-GPO Sync Signal GPIO0 in GMSL1 Mode.  VS: Vertical Sync Monitor Push-Pull Output.  GPIO4: Configurable General Purpose Input or Output.

PIN	NAME	FUNCTION MODE		FUNCTION
14	MFP5	SCLK_0 LMN7 GPIO5*	LMN7 GPIO5(**)	SCLK_0: SPI Interface 0 Clock. When configured as master, push-pull clock output. When configured as slave, clock input with internal 1MΩ pulldown to ground.  LMN7: Line-Fault Monitor Input 7. Use in conjunction with LMN6 for STP applications.  GPIO5: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
15	MFP6	MOSI_0 LMN0 GPIO6*	CNTL1 LMN0 GPIO6(**)	MOSI_0: SPI Interface 0 Master Out Slave In. When configured as master, push-pull output that drives data to external slave. When configured as slave, input with internal 1MΩ pulldown to ground that receives data from external master.  CNTL1: GMSL1 Control Output 1 with Push-Pull Driver. Tunnels from corresponding input pin on serializer.  LMN0: Line-Fault Monitor Input 0. Use in conjunction with LMN1 for STP applications.  GPIO6: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
16	MFP7	MISO_0 LMN1 GPIO7*	CNTL2 LMN1 GPIO7(**)	MISO_0: SPI Interface 0 Master In Slave Out. When configured as master, input with internal 1MΩ pulldown to ground that receives data from external slave. When configured as slave, push-pull output that drives data to an external master.  CNTL2: GMSL1 Control Output 2 with Push-Pull Driver. Tunnels from corresponding input pin on serializer.  LMN1: Line-Fault Monitor Input 1. Use in conjunction with LMN0 for STP applications.  GPIO7: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.

PIN	NAME	FUNCTION MODE	FUNCTION
28	MFP8	SDA1(ALT) RX1(ALT) BNE_0 SS1_0 LMN2 GPIO8*	SDA1(ALT): Alternate Port 1 I <sup>2</sup> C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SDA or RX specified by I2CSEL/MFP13 at power-up, user must specify alternate function mapping via register configuration).  RX1(ALT): Alternate Port 1 UART Input (SDA or RX specified by I2CSEL/MFP13 at power-up, user must specify alternate function mapping via register configuration).  BNE_0: SPI interface 0. When Configured as Slave, SPI Buffer Not Empty Push-pull Output. BNE = high indicates SPI data is available.  SS1_0: SPI interface 0. When Configured as Master, SPI Slave 1 Select Push-Pull Output.  CNTL3: GMSL1 Control Output 3 with Push-Pull Driver. Tunnels from corresponding input pin on serializer.  LMN2: Line-Fault Monitor Input 2. Use in conjunction with LMN3 for STP applications.  GPIO8: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
29	MFP9	SCL1(ALT) TX1(ALT) RO_0 SS2_0 LMN3 GPIO9*	SCL1(ALT): Alternate Port 1 I <sup>2</sup> C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SCL or TX specified by I2CSEL/MFP13 at power-up, user must specify alternate function mapping via register configuration).  TX1(ALT): Alternate Port 1 UART Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SCL or TX specified by I2CSEL/MFP13 at power-up, user must specify alternate function mapping via register configuration).  RO_0: SPI Interface 0. When configured as slave, SPI mode-select input with internal 1MΩ pulldown to ground. RO = high enables master read from MISO. RO = low enables master write to MOSI.  SS2_0: SPI Interface 0. When configured as master, SPI slave 2 select push-pull output.  CNTL0: GMSL1 Control Output 0 with Push-Pull Driver. Tunnels from corresponding input pin on serializer.  LMN3: Line-Fault Monitor Input 3. Use in conjunction with LMN2 for STP applications.  GPIO9: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.

PIN	NAME	FUNCTION MODE	FUNCTION
30	MFP10	FSYNC(ALT) SCLK_1 LMN4 GPIO10*	FSYNC(ALT) SCLK_1: SPI Interface 1 Clock. When configured as master, push-pull clock output. When configured as slave, clock input with internal 1MΩ pulldown to ground. GPI2: CMOS Input for Dedicated GPI-GPO Sync Signal GPI2 in GMSL1 Mode. LMN4: Line-Fault Monitor Input 4. Use in conjunction with LMN5 for STP applications. GPIO10: Configurable General Purpose Input or Output. Power-up default is I/O disabled with 1MΩ pulldown to ground.
31	MFP11	SDA1* RX1* MOSI_1 GPIO11	SDA1: Port 1 I <sup>2</sup> C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SDA or RX specified by I2CSEL/MFP13 at power-up). RX1: Port 1 UART Input with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SDA or RX specified by I2CSEL/MFP13 at power-up). MOSI_1: SPI Interface 1 Master Out Slave In. When configured as master, push-pull output that drives data to external slave. When configured as slave, input with internal 1MΩ pulldown to ground that receives data from external master. GPIO11: Configurable General Purpose Input or Output.
32	MFP12	SCL1* TX1* MISO_1 GPIO12	SCL1: Port 1 I <sup>2</sup> C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SCL or TX specified by I2CSEL/MFP13 at power-up). TX1: Port 1 UART Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SCL or TX specified by I2CSEL/MFP13 at power-up). MISO_1: SPI Interface 1 Master In Slave Out. When configured as master, input with internal 1MΩ pulldown to ground that receives data from external slave. When configured as slave, push-pull output that drives data to an external master. GPIO12: Configurable General Purpose Input or Output.

PIN	NAME	FUNCTION MODE	FUNCTION
33	MFP13	I2CSEL BNE_1 SS1_1 HS GPO13*	<p>I2CSEL: Control-Channel Interface Select Input for all I<sup>2</sup>C/UART Interfaces. State is latched at power-up. Function changes to GPO13 after I2CSEL is latched. Connect pullup resistor to V<sub>DDIO</sub> to select I<sup>2</sup>C interface. Connect pulldown resistor to ground to select UART interface.</p> <p>BNE_1: SPI Interface 1. When configured as slave, SPI buffer not empty push-pull output. BNE = high indicates SPI data is available.</p> <p>SS1_1: SPI Interface 1. When configured as master, SPI slave 1 select push-pull output.</p> <p>HS: Horizontal Sync Monitor Push-Pull Output.</p> <p>CNTL4: GMSL1 Control Output 4 with Push-Pull Driver. Tunnels from corresponding input pin on serializer.</p> <p>GPO13 (GPIO13): Configurable General Purpose Output. Power-up default following I2CSEL state latching is logic low output. GPIO functionality with input receiver can be enabled following power-up by writing ASIL_GPIO_EN = 1.</p>
34	MFP14	SCL2* TX2* RO_1 SS2_1 LMN5 DE GPIO14	<p>SCL2: Port 2 I<sup>2</sup>C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V<sub>DDIO</sub> (SCL or TX specified by I2CSEL/MFP13 at power-up).</p> <p>TX2: Port 2 UART Output With Internal 40kΩ Pullup to V<sub>DDIO</sub> (SCL or TX specified by I2CSEL/MFP13 at power-up).</p> <p>RO_1: SPI Interface 1. When configured as slave, SPI mode-select input with internal 1MΩ pulldown to ground. RO = high enables master read from MISO. RO = low enables master write to MOSI.</p> <p>SS2_1: SPI Interface 1. When configured as master, SPI slave 2 select push-pull output.</p> <p>GPIO3: CMOS Input for Dedicated GPI-GPO Sync Signal GPIO3 in GMSL1 Mode.</p> <p>LMN5: Line-Fault Monitor Input 5. Use in conjunction with LMN4 for STP applications.</p> <p>DE: Data Enable Monitor Push-Pull Output.</p> <p>GPIO14: Configurable General Purpose Input or Output.</p>

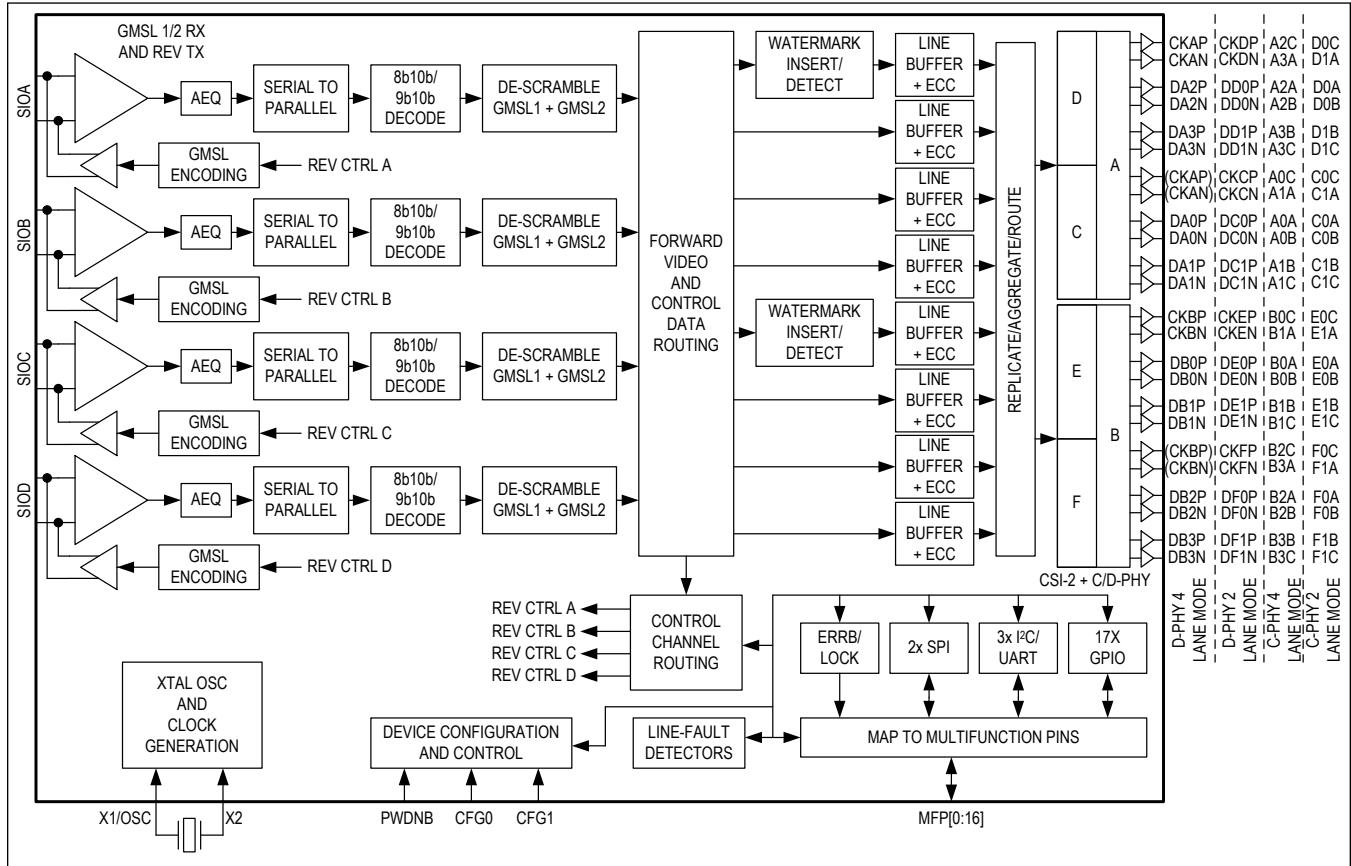
PIN	NAME	FUNCTION MODE		FUNCTION
		SDA*	RX*	
63	MFP15	SDA* RX* ODO15/GPI15	SDA* RX* ODO15/GPI15**	SDA: Port 0 I <sup>2</sup> C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SDA or RX specified by I2CSEL/MFP13 at power-up).  RX: Port 0 UART Input with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SDA or RX specified by I2CSEL/MFP13 at power-up).  ODO15/GPI15: Configurable General Purpose Input and/or Open-Drain Output with Selectable Internal Pullup.
64	MFP16	SCL* TX* ODO16/GPI16	SCL* TX* ODO16/GPI16**	SCL: Port 0 I <sup>2</sup> C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SCL or TX specified by I2CSEL/MFP13 at power-up).  TX: Port 0 UART Output with Internal 40kΩ Pullup to V <sub>DDIO</sub> (SCL or TX specified by I2CSEL/MFP13 at power-up).  ODO16/GPI16: Configurable General Purpose Input and/or Open-Drain Output with Selectable Internal Pullup.
<b>MISCELLANEOUS</b> See <a href="#">Table 2</a>				
5	CFG0	CFG0	CFG0	Configuration Pin 0. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between V <sub>DDIO</sub> and ground. See <a href="#">Table 7</a> for configuration details.
12	CFG1	CFG1	CFG1	Configuration Pin 1. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between V <sub>DDIO</sub> and ground. See <a href="#">Table 8</a> for configuration details.
35	PWDNB	PWDNB	PWDNB	Active Low Power-Down Input with 1MΩ Pulldown to Ground. Apply logic low to place device in power-down mode. Connect to V <sub>DDIO</sub> /logic high for normal operation.
17	X1/OSC	X1/OSC	X1/OSC	X1/OSC: Crystal/Oscillator Input. Connect to either one terminal of a ±200ppm 25MHz crystal or a 25MHz external clock source. If crystal is used, connect a load capacitor from X1/OSC to ground (Load capacitor value depends on crystal used).
18	X2	X2	X2	X2: Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal. If crystal is used, connect a load capacitor from X2 to ground (Load capacitor value depends on crystal used). If external oscillator is connected to X1/OSC, leave X2 floating.
19	RSVD	RSVD	RSVD	Reserved: Make No Electrical Connection to this Pin.
20	XRES	XRES	XRES	Connect 402Ω 1% Resistor Between XRES and Ground.

PIN	NAME	FUNCTION MODE		FUNCTION
<b>POWER SUPPLIES</b> See <a href="#">Table 2</a>				
8,24	VDD18	VDD18	VDD18	1.8V Analog Power Supply. Place decoupling capacitor connected to PCB ground plane as close as possible to each pin.
27	VDDIO	VDDIO	VDDIO	1.8V to 3.3V I/O Power Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
48	VTERM	VTERM	VTERM	1.2V CSI C-PHY/D-PHY Power Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
61,62	VDD	VDD	VDD	1.0V Core Power Supply. This pin includes an optional on-chip LDO. Connect a 1V (0.95V to 1.05V) supply to bypass LDO. Connect a 1.2V (1.14V to 1.26V) supply to use the internal 1.0V regulator. In order to use the internal 1V regulator, first write REG_ENABLE = 1, and then write REG_MNL = 1. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
9,23	CAP_VDD	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1.0V Core Power Supply. Place decoupling capacitor connected to PCB ground plane as close as possible to each pin. Connect CAP_VDD pins together on board with low impedance copper pour.
EP	EP	EP	EP	Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

**PRELIMINARY**

## Functional Diagrams

### Functional Block Diagram



## Recommended Operating Conditions

### Recommended Operating Conditions

**Table 1. Recommended Operating Conditions**

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	VTERM		1.14	1.2	1.26	V
	VDD18		1.7	1.8	1.9	
	VDD	1.0V	0.95	1.0	1.05	
		1.2V	1.14	1.2	1.26	
	VDDIO		1.7		3.6	
Operating Junction Temperature (T <sub>J</sub> )			-40		125	°C

### External Component Requirements

[Table 2](#) details critical components that must be connected to the specified pins for correct functionality. This table is not an exhaustive listing of all components that may be needed in a typical application. Please refer to the MAX96722 EV Kit schematic for a detailed example of a typical application circuit.

**Table 2. External Component Requirements**

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT	
XRES	R <sub>XRES</sub>	Connect R <sub>XRES</sub> resistor between XRES pin and ground.	402 ±1%. Use a single resistor.	Ω	
Link Isolation Capacitors	C <sub>LINK</sub>	Place in series with and in close proximity to the SIO pins (pins 6, 7, 10, 11, 21, 22, 25, 26)	GMSL2 Mode, GMSL1 Mode (HIM enabled)	0.1	μF
			GMSL1 Mode (HIM disabled) (also compliant with GMSL2 and GMSL1/HIM operation)	0.22	
Termination Resistors for SIO_N pins in Coax mode	R <sub>TERM</sub>	Connect in series with C <sub>LINK</sub> capacitor between SIO_N and ground when GMSL link is configured in Coax mode. Place near associated SIO_N pin.	49.9 ±1%	Ω	
Crystal		Place as close as possible to pins X1/OSC (pin 17) and X2 (pin 18) and connect between these two pins.	25MHz ±200ppm		
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values which compensate for X1/OSC (pin 17) and X2 (pin 18) and PCB node capacitances. Place the capacitors as close as possible to pins X1/OSC (pin 17) and X2 (pin 18).			
V <sub>DDIO</sub> Decoupling Capacitors		Place 0.01μF capacitor as close as possible to pin VDDIO (pin 27). Include a minimum of 10μF bulk decoupling on the PCB.	0.01μF + 10μF		
V <sub>DD18</sub> Decoupling Capacitors		Place a 0.01μF capacitor as close as possible to each VDD18 pin (pin 8 and pin 24). Include a minimum of 10μF bulk decoupling on the PCB.	2 x 0.01μF + 10μF		
V <sub>DD</sub> Decoupling Capacitors		Place a 0.1μF capacitor as close as possible to each VDD pin (pin 61 and pin 62). Include a minimum of 10μF bulk decoupling on the PCB.	2 x 0.1μF + 10μF		

**Table 2. External Component Requirements (continued)**

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
VTERM Decoupling Capacitors		Place 0.01µF capacitor as close as possible to pin VTERM (pin 48). Include a minimum of 10µF bulk decoupling on the PCB.	0.01µF + 10µF	
CAP_VDD Decoupling Capacitors		Place a 0.1µF capacitor as close as possible to each CAP_VDD pin (pin 9 and pin 23). Include a minimum of 10µF bulk decoupling on the PCB.	2 x 0.1µF + 10µF	
Miscellaneous External Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations. Series termination resistors and pullup/pulldown resistors may be required depending on application.		
Resistors for Configuration Pin Resistor Dividers (CFG0, CFG1)	R1, R2	Place resistor divider close to pin CFG0 (pin 5). Resistor values depend on desired configuration.	Use ±1% Tolerance Resistors. See <a href="#">Table 7</a> .	Ω
	R1, R2	Place resistor divider close to pin CFG1 (pin 12). Resistor values depend on desired configuration.	Use ±1% Tolerance Resistors. See <a href="#">Table 8</a> .	Ω
Line-Fault Pulldown Resistor	RPD	Connect to ground at far end of cable opposite active line-fault detector. Line-fault detection cannot be used in conjunction with PoC.	49.9 ± 1%	kΩ
Line-Fault Resistor	R <sub>EXT</sub>	Connect between GMSL interconnect and LMN line-fault detector input. Line-fault detection cannot be used in conjunction with PoC.	LMN0/2/4/6 STP Mode	42.2 ± 1%
			LMN0/2/4/6 Coax Mode	48.7 ± 1%
			LMN1/3/5/7 STP/Coax Mode	48.7 ± 1%
Power-over-Coax (PoC) Network		If PoC is used to power remote camera modules, connect PoC components to active GMSL links to provide remote power feed. Contact the factory for recommended PoC network designs and suggested component placement. The far-end of the link (camera side) should include a corresponding PoC network to receive power if this feature is used. PoC cannot be used in conjunction with line-fault detection.		

**PRELIMINARY**

## Functional Diagrams

### GMSL2 Serial Output Parameters

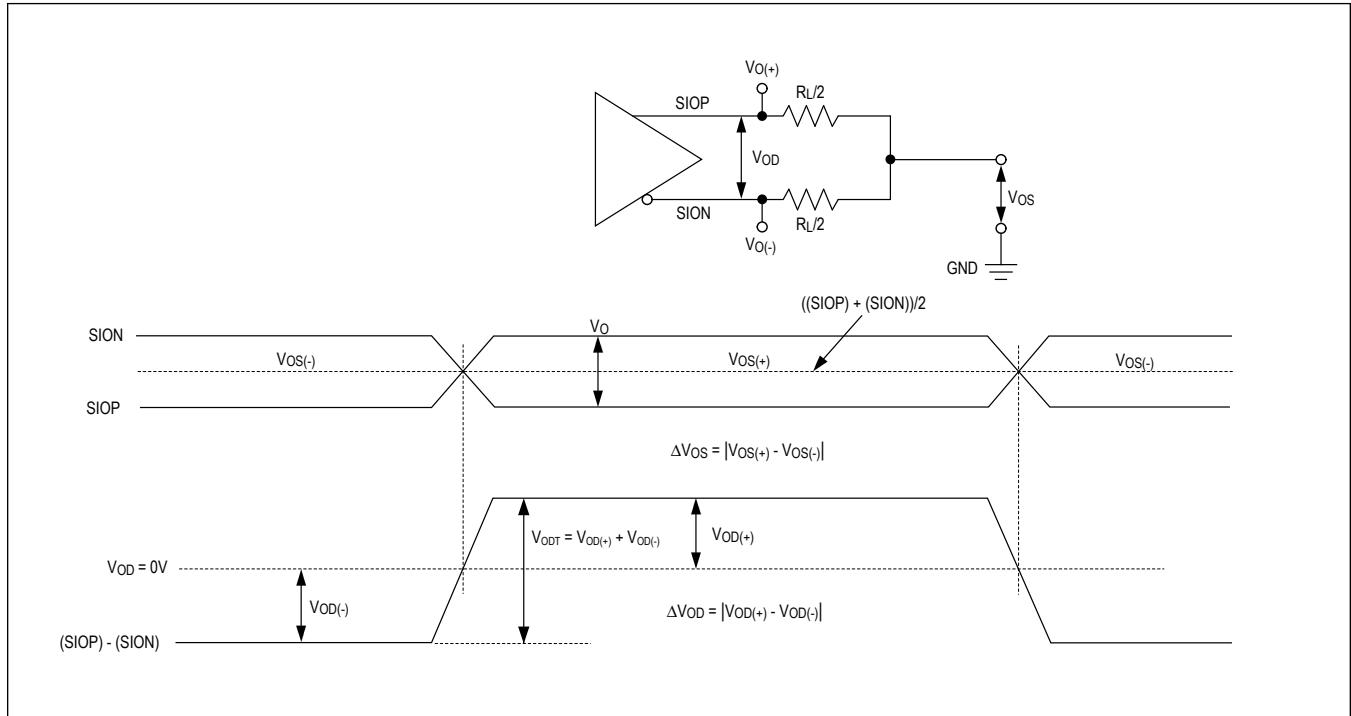


Figure 1. GMSL2 Serial Output Parameters

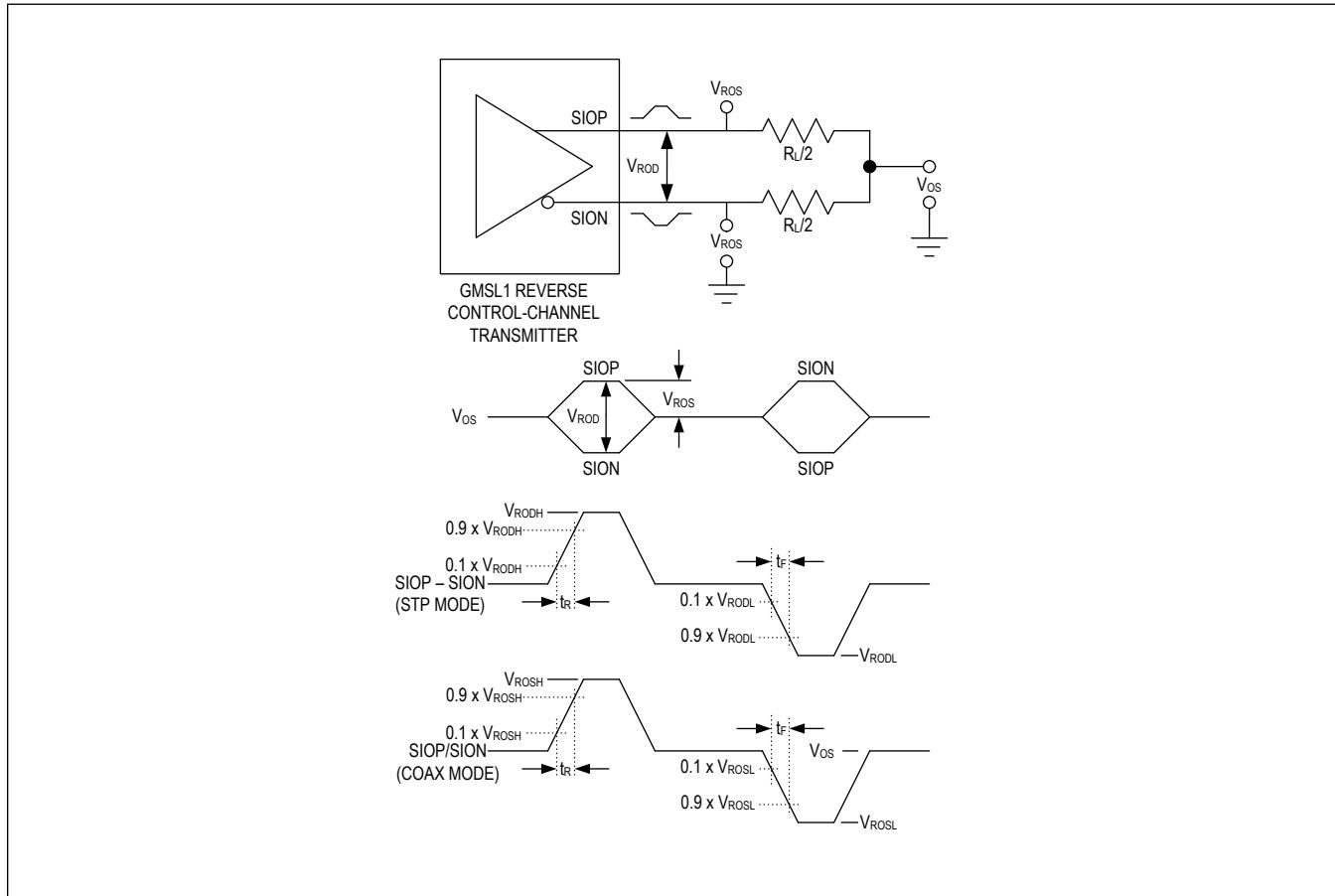
**GMSL1 Serial Output Parameters**

Figure 2. GMSL1 Serial Output Parameters

**PRELIMINARY**

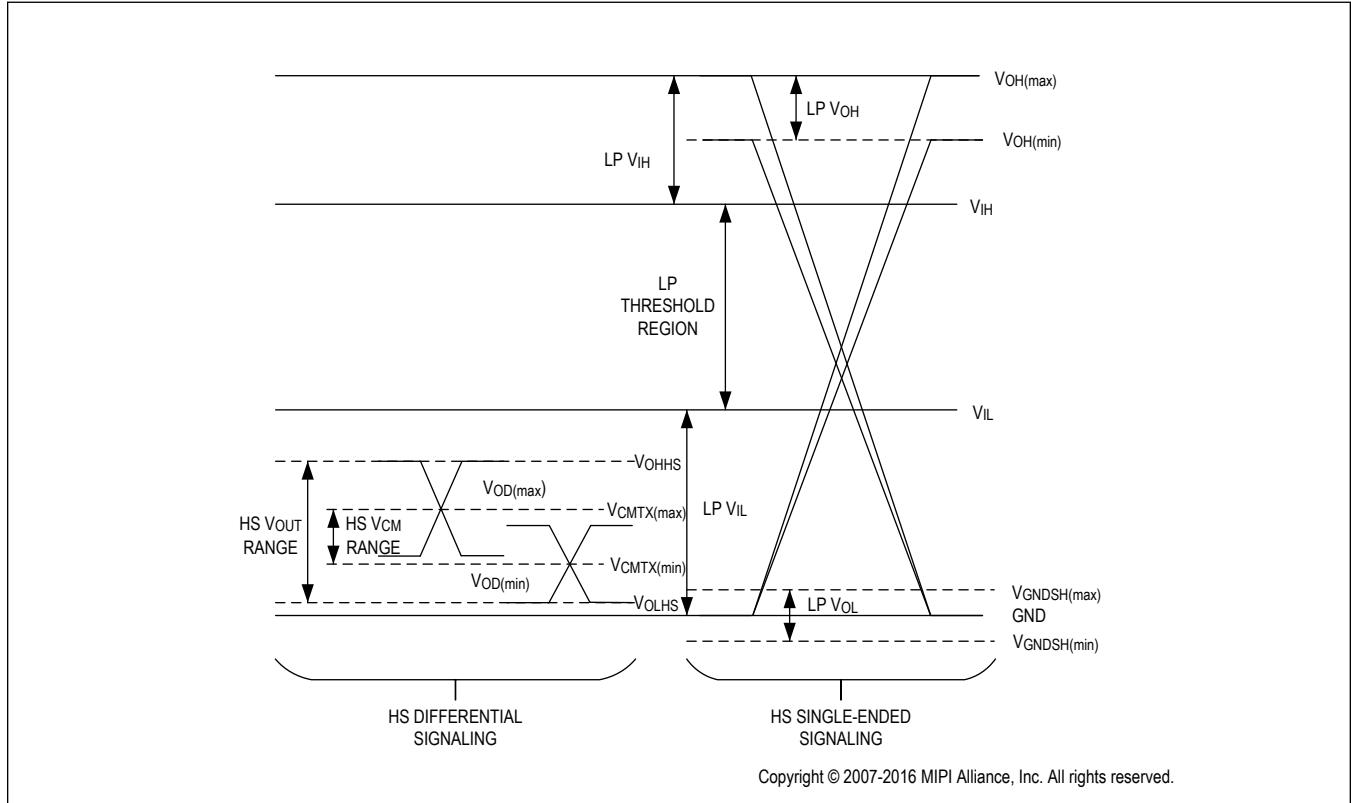
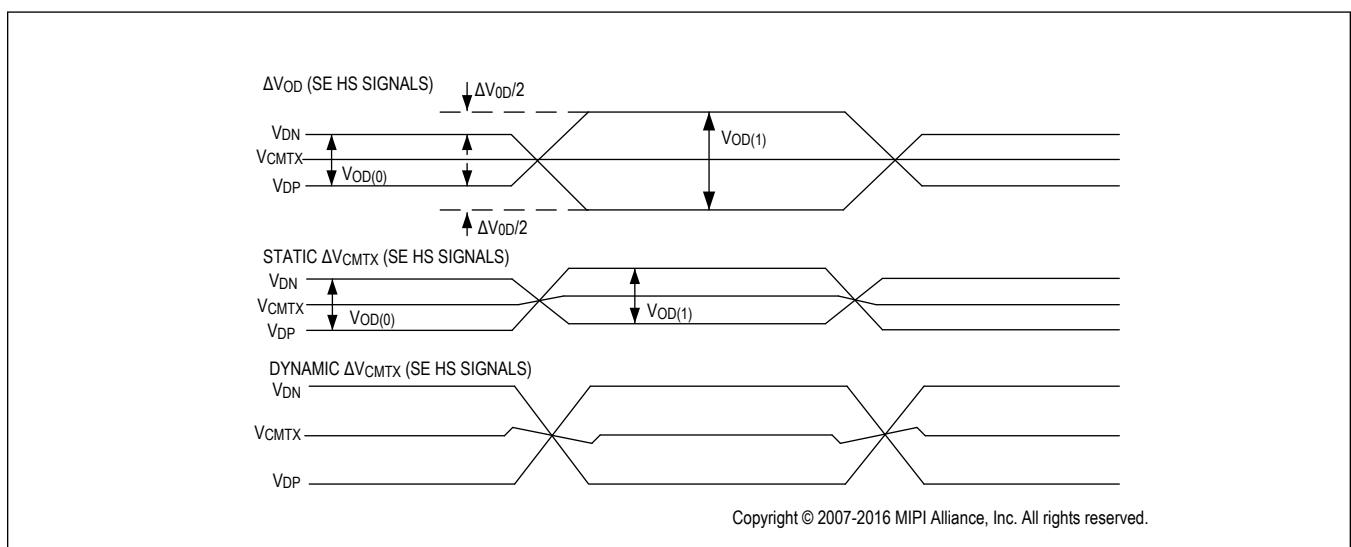
**D-PHY DC Characteristics**

Figure 3. D-PHY DC Characteristics

**D-PHY Possible  $\Delta V_{CMTX}$  and  $\Delta V_{OD}$  Distortions of Single-ended HS Signals**Figure 4. D-PHY Possible  $\Delta V_{CMTX}$  and  $\Delta V_{OD}$  Distortions of Single-ended HS Signals

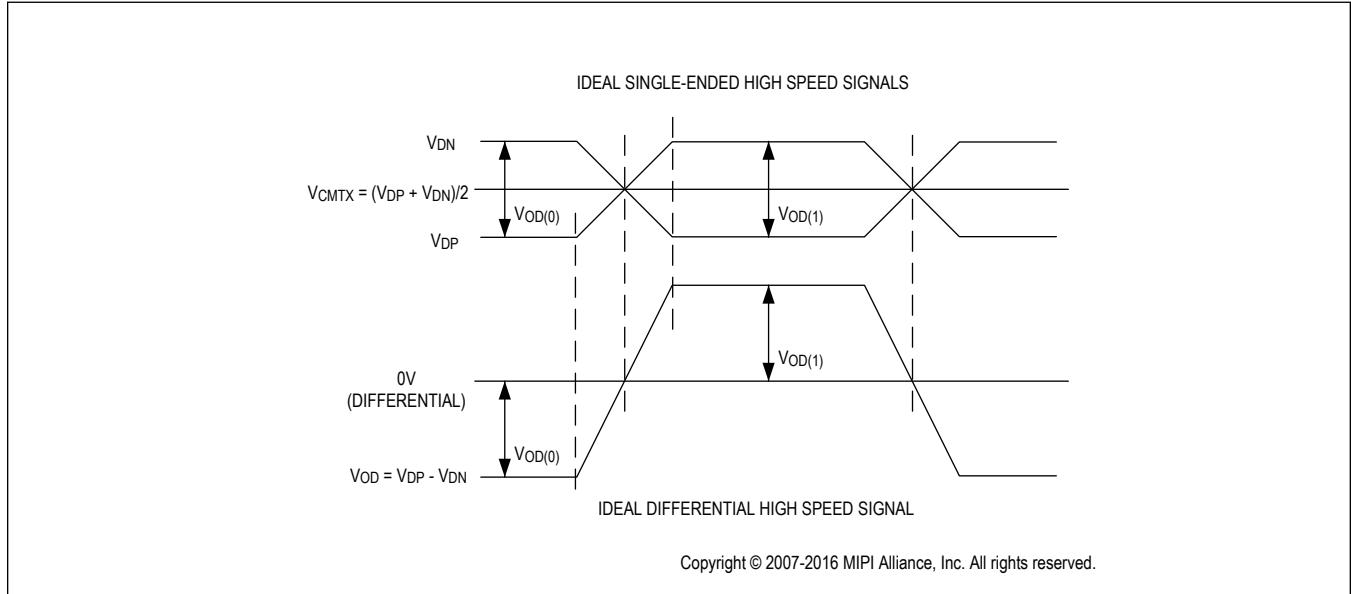
**D-PHY Ideal Single-ended and Resulting Differential HS Signals**

Figure 5. D-PHY Ideal Single-ended and Resulting Differential HS Signals

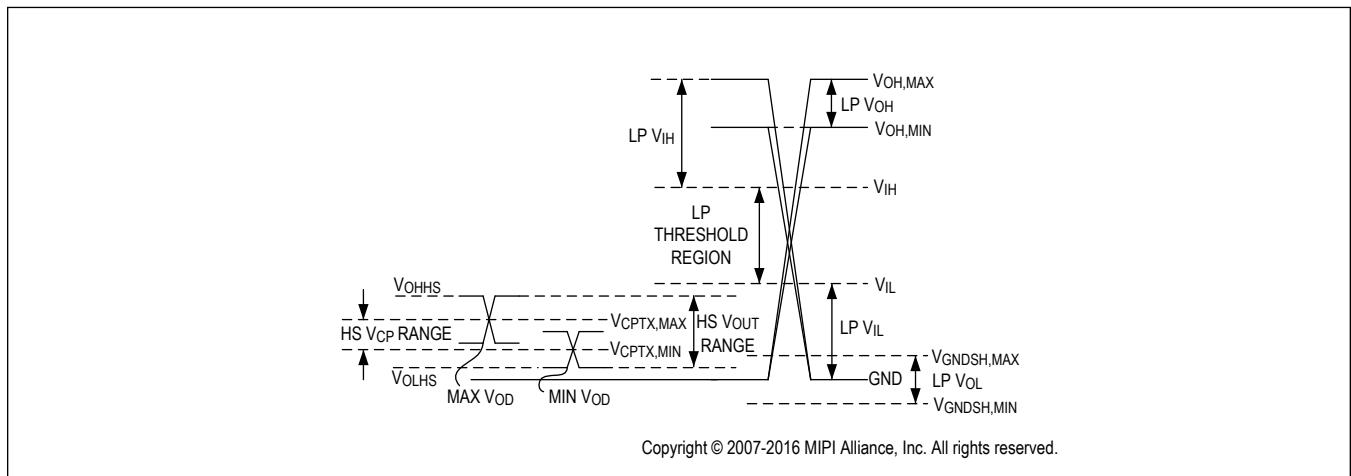
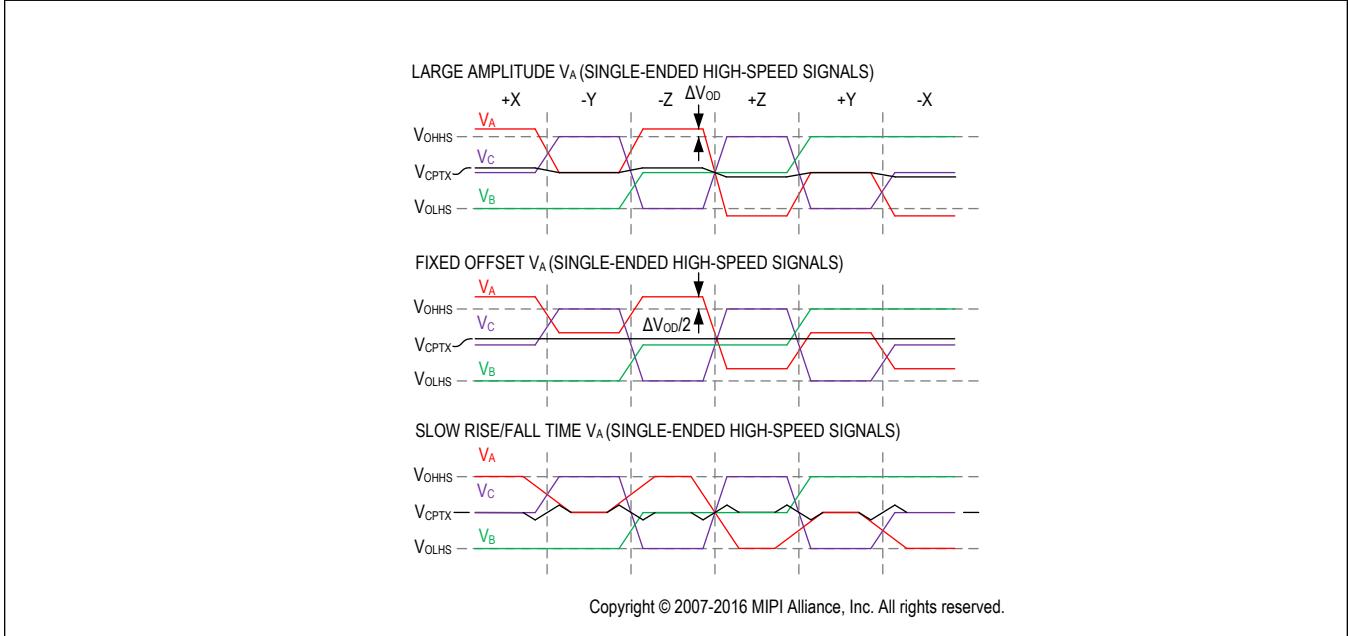
**C-PHY DC Characteristics**

Figure 6. C-PHY DC Characteristics

**C-PHY Possible  $\Delta V_{CPTX}$  and  $\Delta V_{OD}$  Distortions of Single-Ended HS Signals**Figure 7. C-PHY Possible  $\Delta V_{CPTX}$  and  $\Delta V_{OD}$  Distortions of Single-Ended HS Signals

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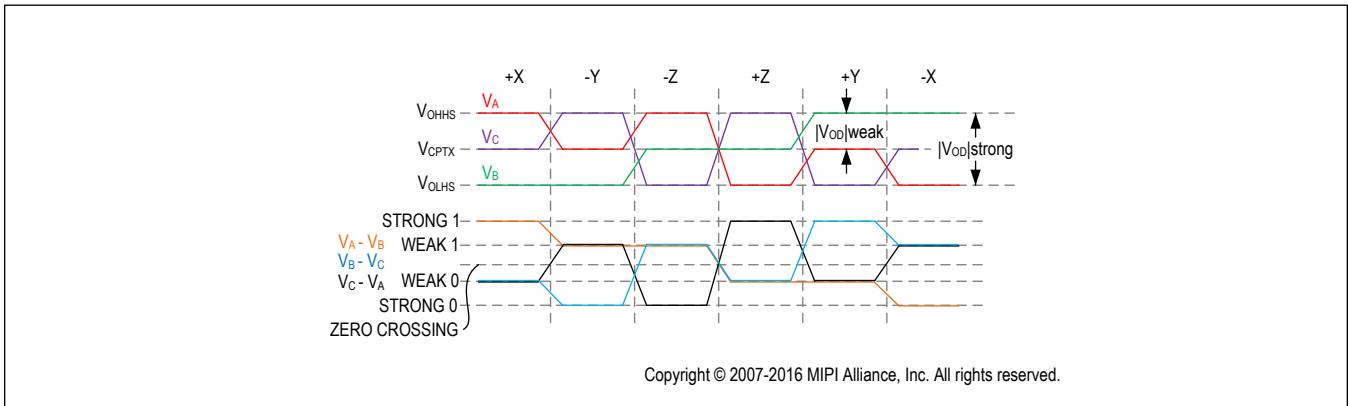
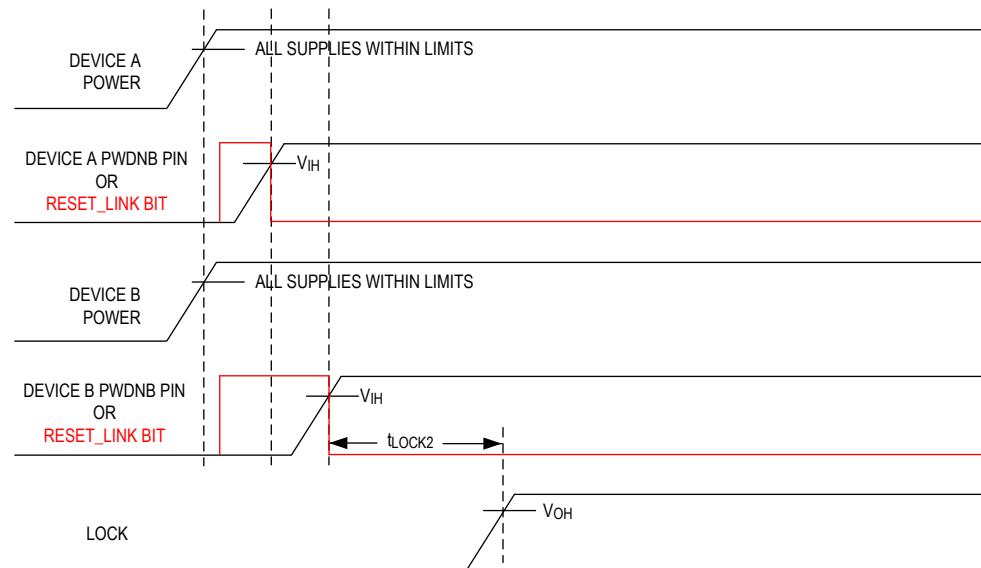
**C-PHY Ideal Single-Ended and Resulting Differential High-Speed Signals**

Figure 8. C-PHY Ideal Single-Ended and Resulting Differential High-Speed Signals

**GMSL2 Lock Time**

THE LOCK SEQUENCE IS INITIATED BY THE RELEASE OF THE PWDNB PIN OR THE RESET\_LINK BIT IN EITHER SERIALIZER OR DESERIALIZER. SPECIFIED PERFORMANCE CAN BE ACHIEVED REGARDLESS OF WHETHER THE LOCKING PROCESS IS INITIATED IN SERIALIZER OR DESERIALIZER (PWDNB/RESET\_LINK CAN BE RELEASED LATER ON EITHER DEVICE OR THEY CAN BE RELEASED SIMULTANEOUSLY). THE REQUIRED LOCK TIME IS MEASURED FROM THE LATER OF PWDNB OR RESET\_LINK RELEASE ON EITHER SERIALIZER OR DESERIALIZER TO LOCK BEING ASSERTED. THE PWDNB/RESET\_LINK STATES ON THE TWO SIDES OF THE LINK MUST HAVE OVERLAP WHEN BOTH DEVICES ARE IN PWDNB/RESET\_LINK MODE PRIOR TO THE LOCK PROCESS STARTING. THE DEVICES DO NOT NEED TO ENTER OR EXIT THE PWDNB/RESET\_LINK STATE AT THE SAME TIME.



## NOTE:

1. IF RESET\_LINK IS USED TO INITIATE LOCK, PWDNB IS ASSUMED TO BE HIGH AFTER POWER-UP (NORMAL OPERATION)
2. IF PWDNB IS USED TO INITIATE LOCK, RESET\_LINK IS ASSUMED TO BE LOW AFTER POWER-UP (NORMAL OPERATION)

Figure 9. GMSL2 Lock Time

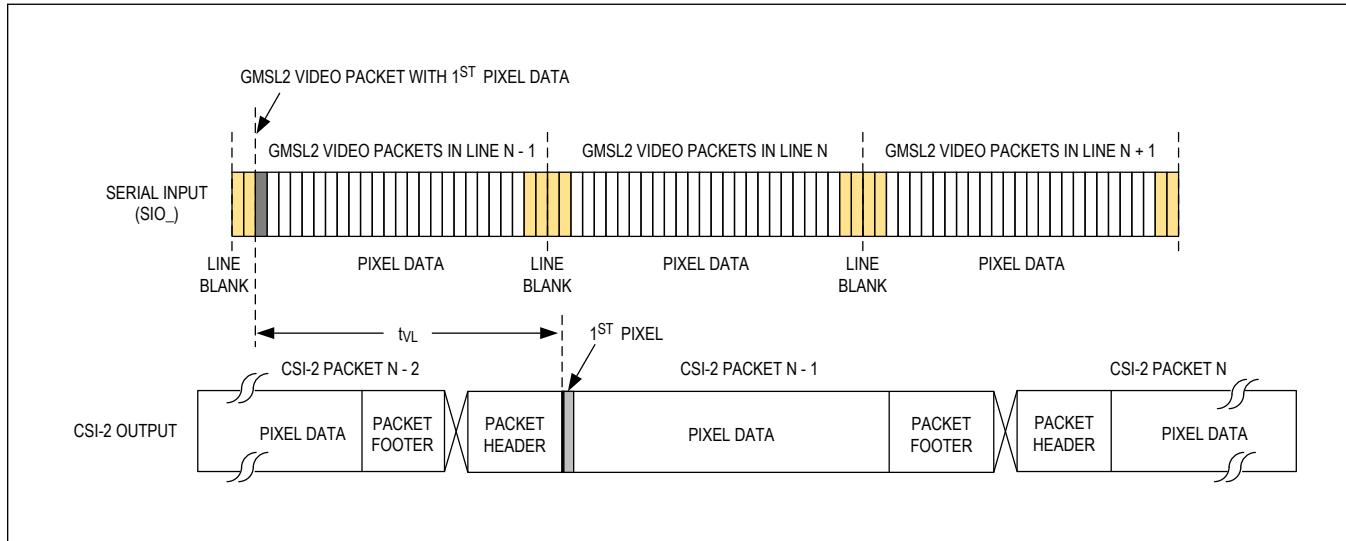
**GMSL2 Video Latency**

Figure 10. GMSL2 Video Latency

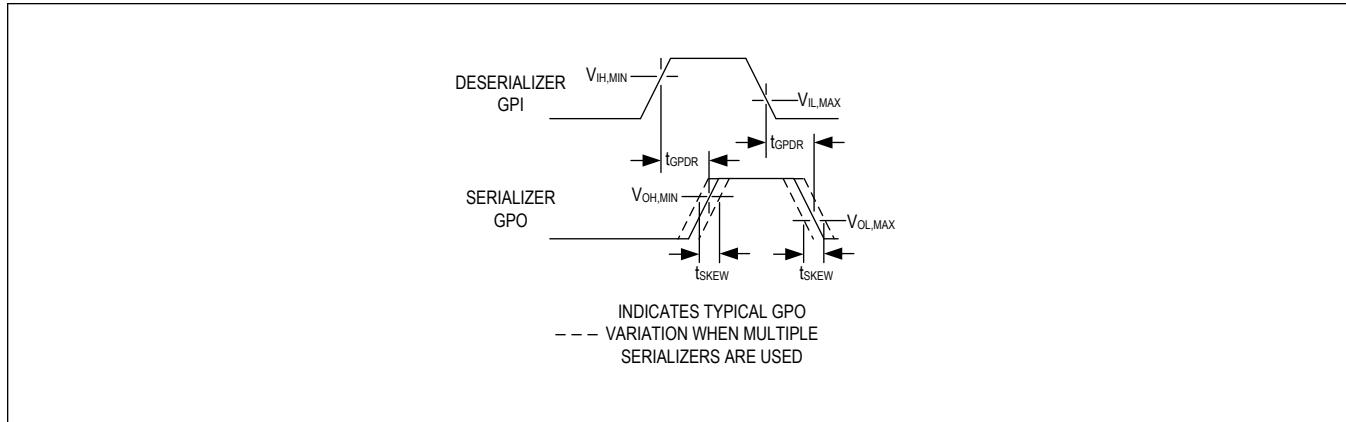
**GMSL2 GPIO-to-GPO Delay and Skew**

Figure 11. GMSL2 GPIO-to-GPO Delay and Skew

PRELIMINARY

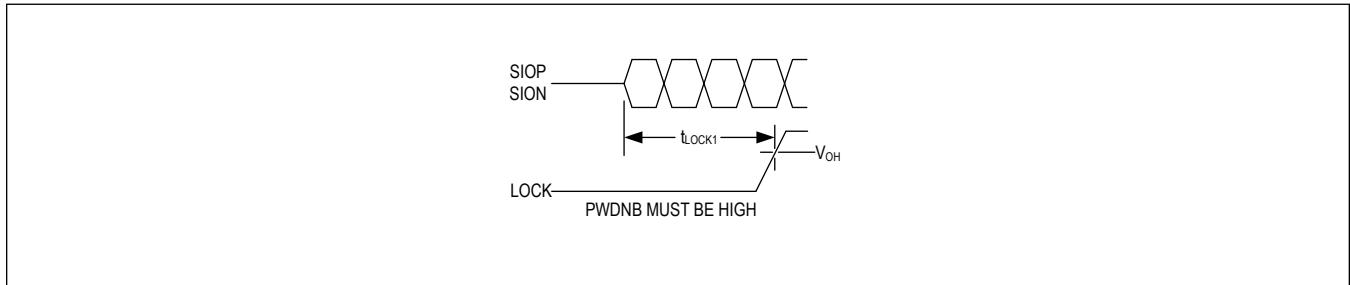
**GMSL1 Lock Time**

Figure 12. GMSL1 Lock Time

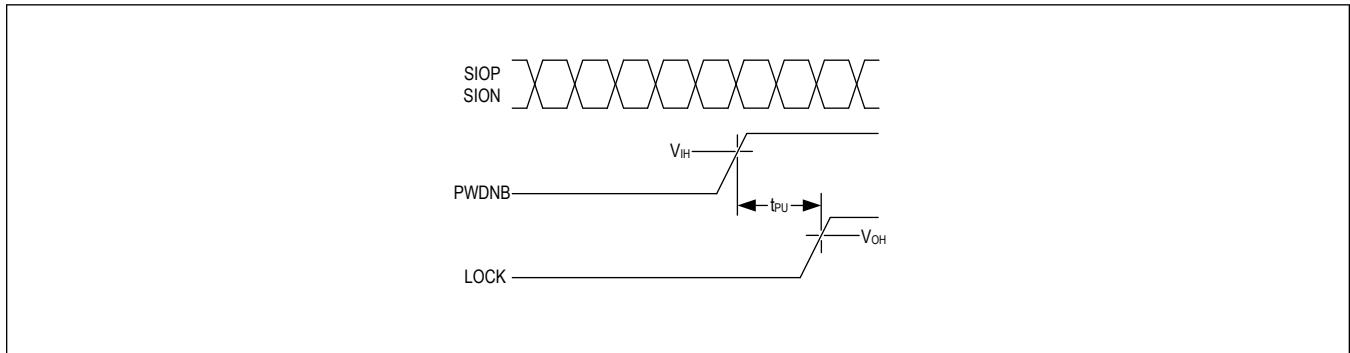
**GMSL1 Power-up Delay**

Figure 13. GMSL1 Power-up Delay

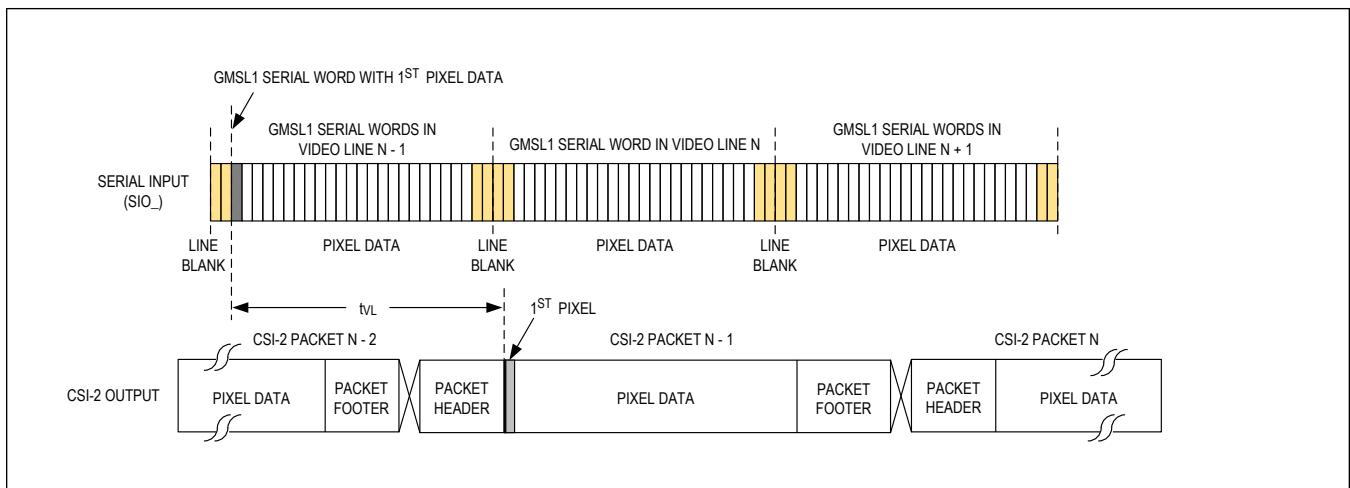
**GMSL1 Video Latency**

Figure 14. GMSL1 Video Latency

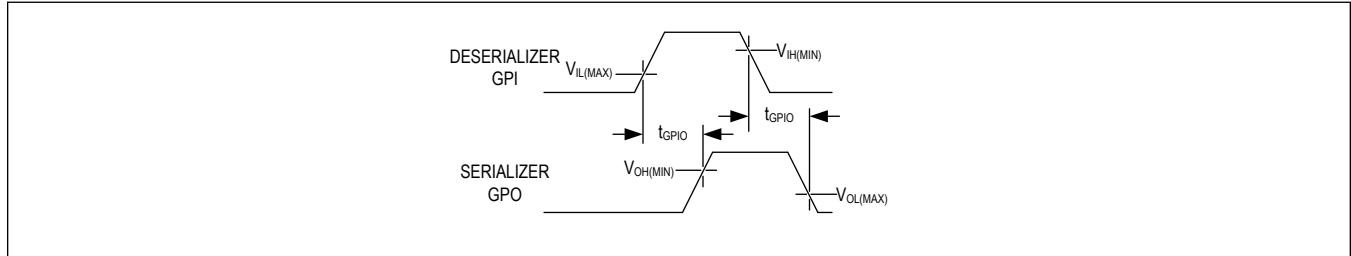
**GMSL1 GPI-to-GPO Delay**

Figure 15. GMSL1 GPI-to-GPO Delay

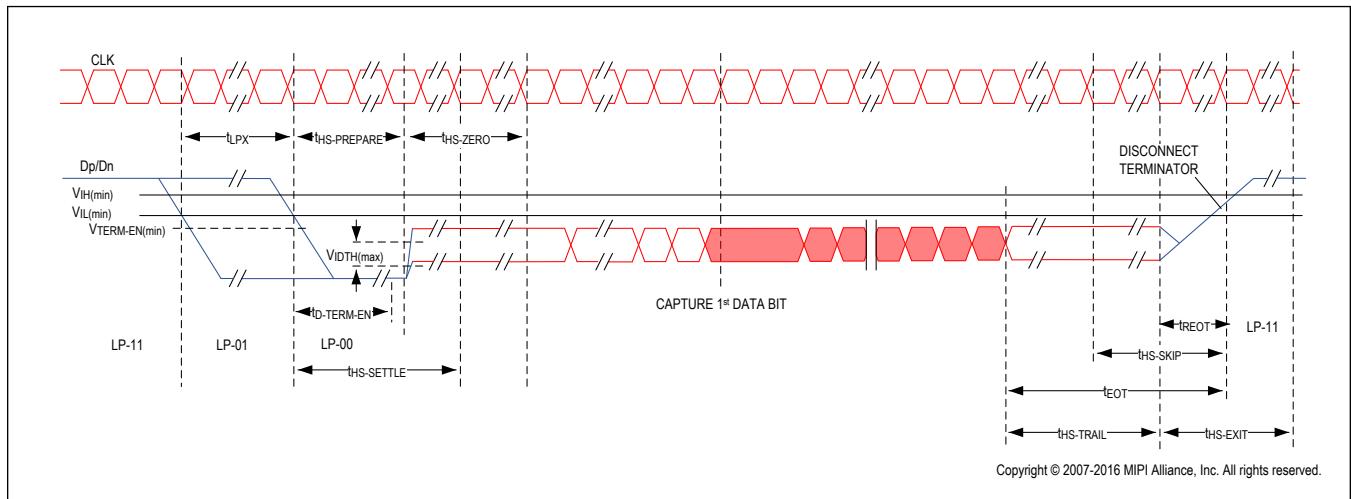
**D-PHY HS Burst Data Transmission**

Figure 16. D-PHY HS Burst Data Transmission

**PRELIMINARY**

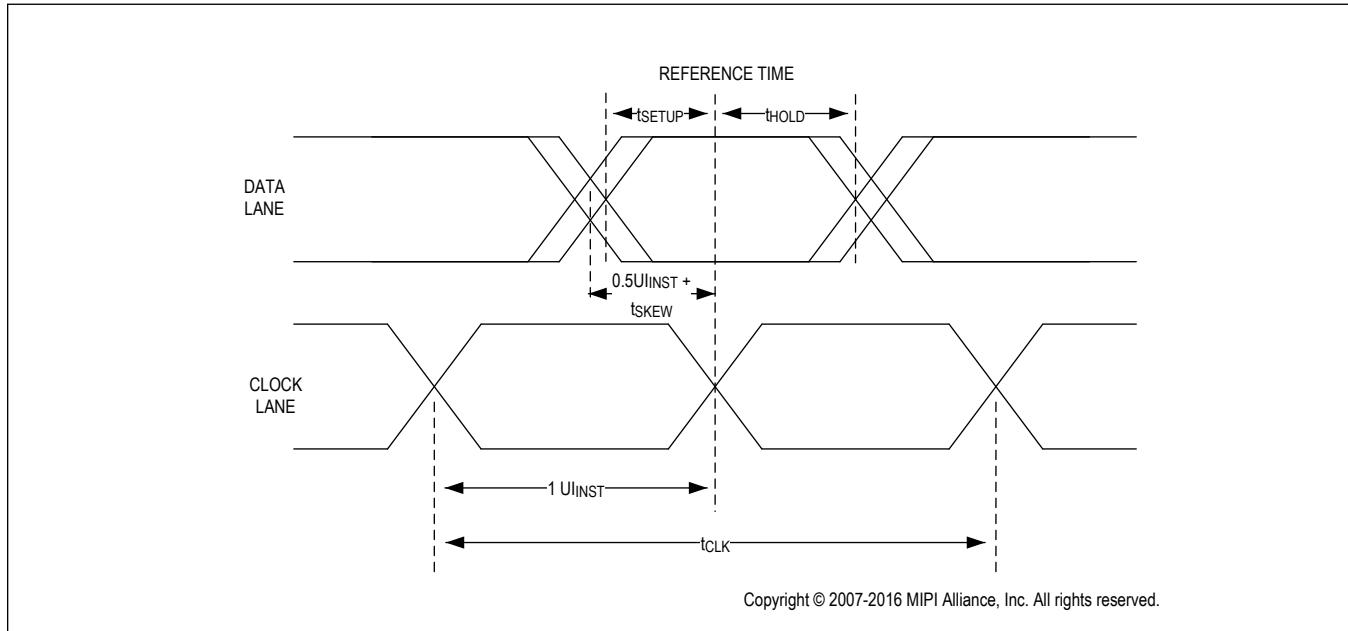
**D-PHY Data Clock Timing**

Figure 17. D-PHY Data Clock Timing

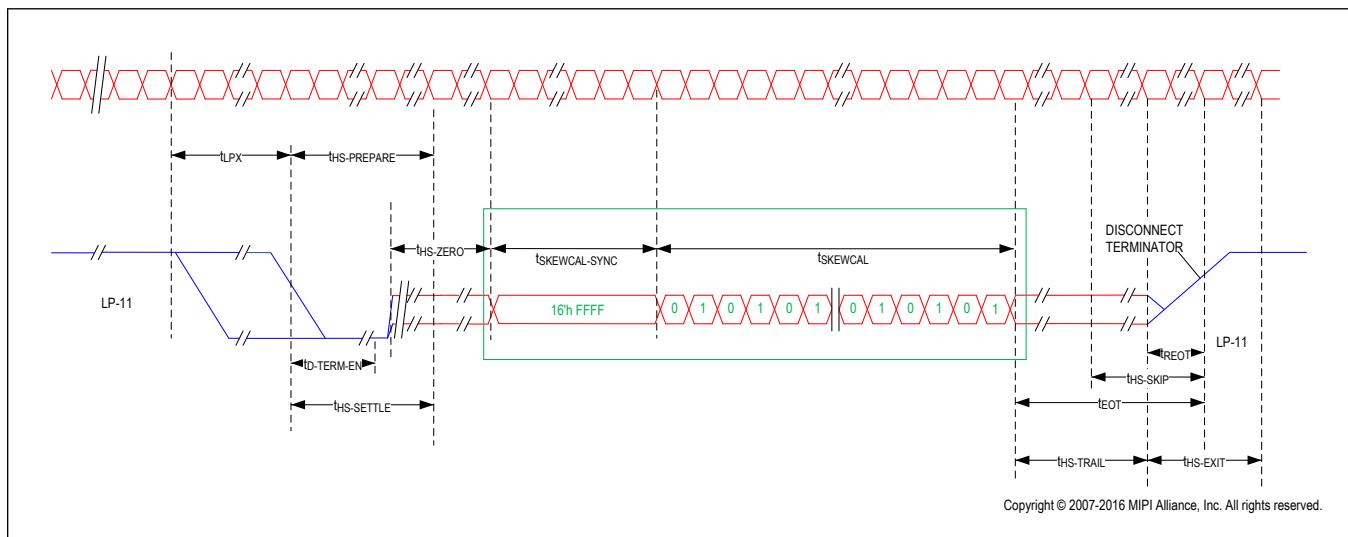
**D-PHY High-Speed Skew Calibration**

Figure 18. D-PHY High-Speed Skew Calibration

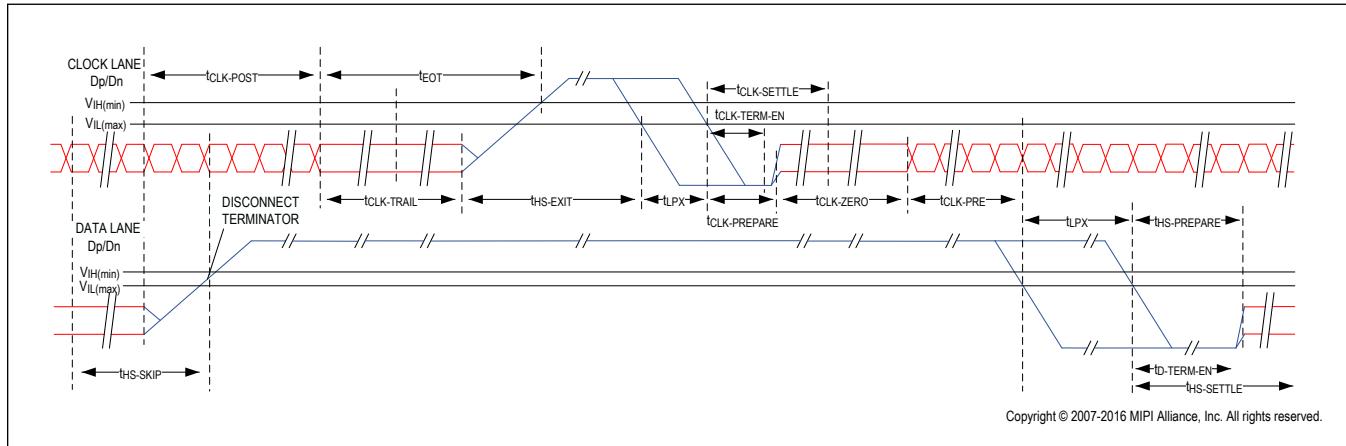
**D-PHY Switching Clock Lane From Active Transmission to Low-Power Mode**

Figure 19. D-PHY Switching Clock Lane From Active Transmission to Low-Power Mode

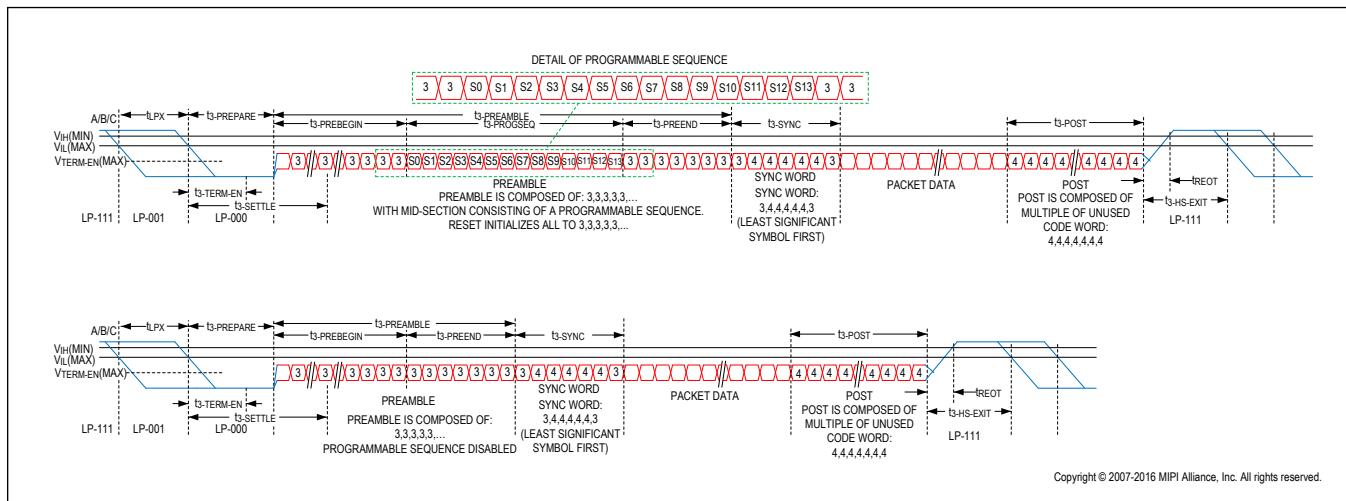
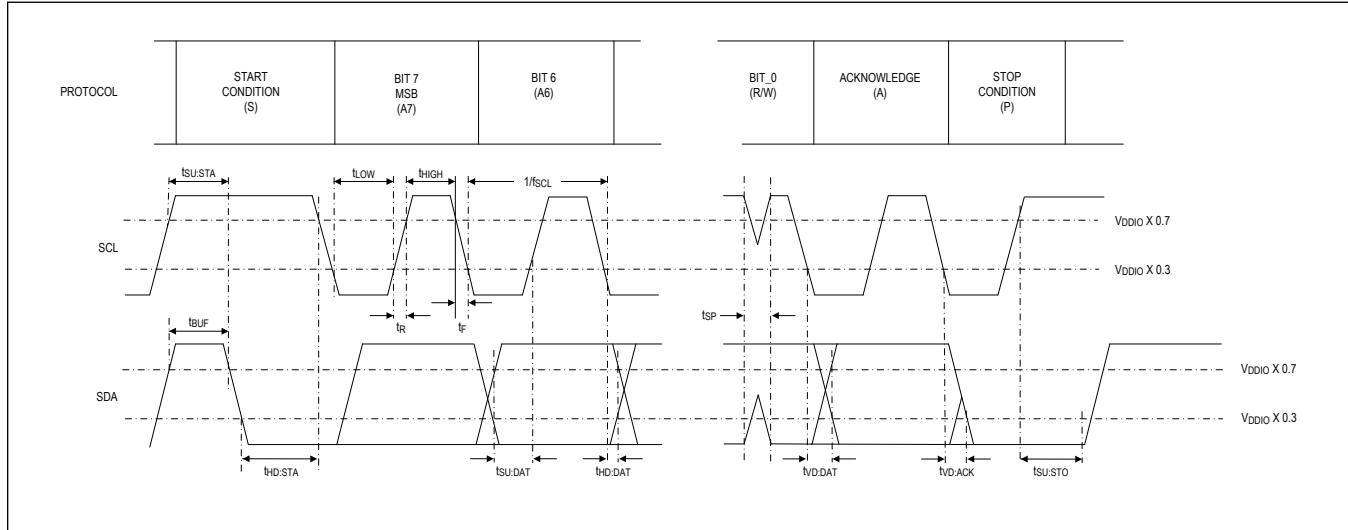
**C-PHY HS Burst Data Transmission**

Figure 20. C-PHY HS Burst Data Transmission

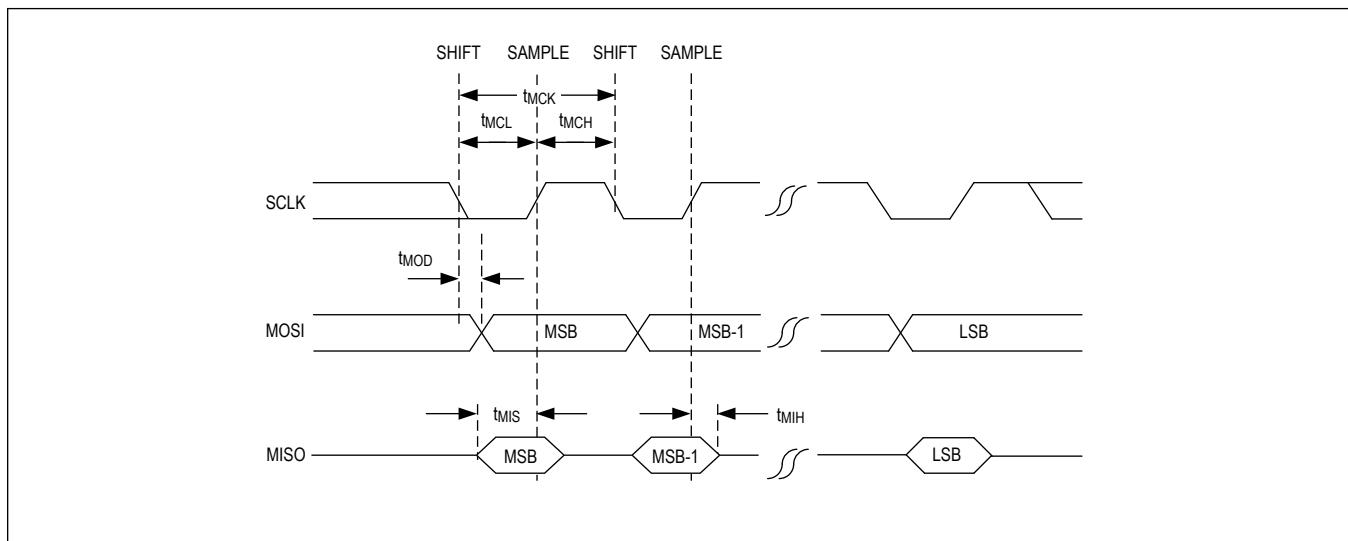
**PRELIMINARY**

## I<sup>2</sup>C Timing Parameters



*Figure 21. I<sup>2</sup>C Timing Parameters*

## SPI Master Mode Timing Parameters



*Figure 22. SPI Master Mode Timing Parameters*

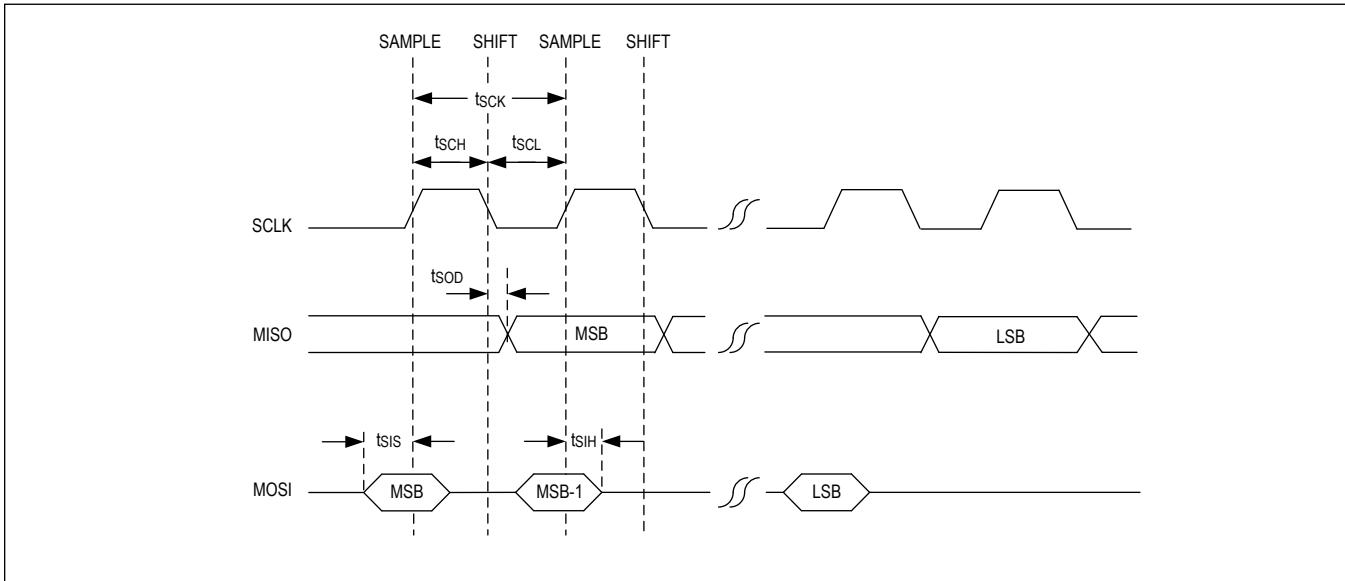
**SPI Slave Mode Timing Parameters**

Figure 23. SPI Slave Mode Timing Parameters

**Detailed Description****Introduction**

Maxim's GMSL2 serializers and deserializers provide sophisticated link management for high-speed, low bit-error-rate, bidirectional serial data transport. They support a comprehensive suite of display, camera, and communication interfaces over a single wire.

The MAX96722 provides up to 3Gbps forward and 187.5Mbps reverse packetized data transmission over each fixed-speed link. The MAX96722's inputs can be aggregated such that incoming data from four remotely located sensors is combined and routed to any available combination of CSI outputs. With this capability, it is possible to transport data from four remote sensors to an SoC using a single CSI-2 port.

The following sections provide a brief overview of the device functions and features. Contact the factory for additional information and details on the configuration of each function and feature.

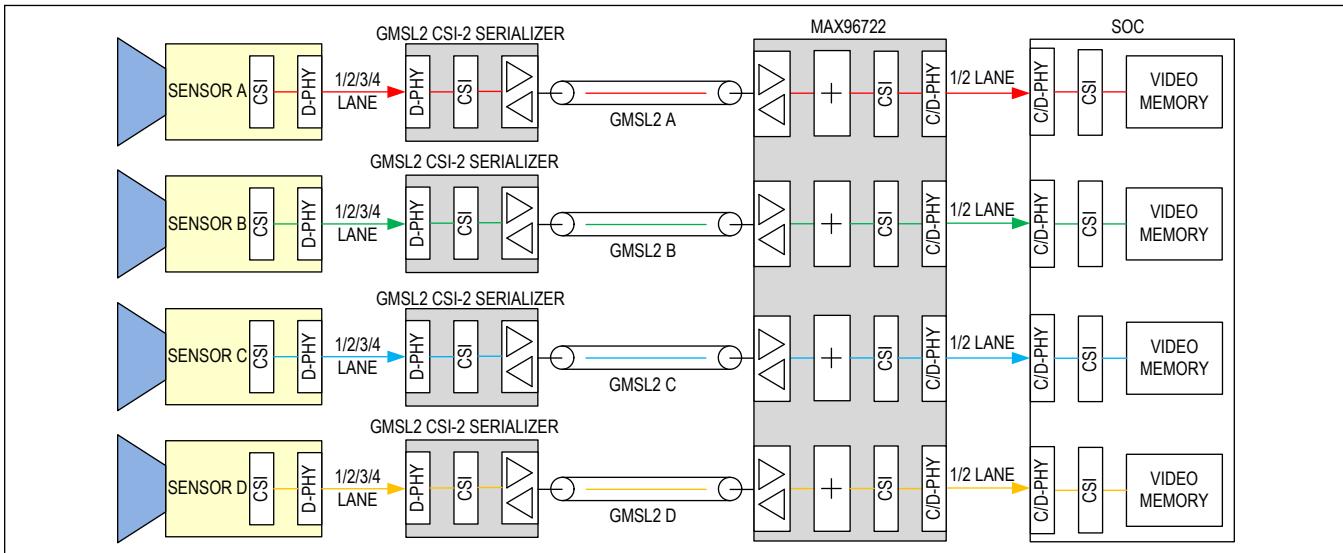
**Product Overview**

The MAX96722 deserializer converts four GMSL2 or GMSL1 inputs to up to four independent MIPI CSI-2 C/D-PHY outputs containing a combined total of up to eight lanes. It also sends and receives control channel data, enabling full-duplex transmission of forward path video and bidirectional control data over low-cost 50Ω coax or 100Ω STP cables that meet the GMSL2 channel specification. In backward compatible GMSL1 mode, the MAX96722 can be paired with 3.12Gbps or 1.5Gbps GMSL1 serializers or operate up to 3.12Gbps with GMSL2 serializers operated in GMSL1 mode.

The MAX96722 has dual 4-lane or quad 2-lane CSI-2 v1.3 output ports which support data-rates of 80Mbps to 2.5Gbps per lane in D-PHY mode or 182Mbps to 5.7Gbps per lane in C-PHY mode. The number of active data lanes in each CSI-2 port is programmable with 4-lane ports providing one, two, three, or four lanes and 2-lane ports providing one or two lanes. Supported data types include RAW8/10/12/14/16/20, RGB565/666/888, YUV422 8/10-bit, user defined, and generic long packet data types. Up to 16 virtual channels are supported in D-PHY mode while C-PHY mode provides up to 32 virtual channels, enabling flexible routing of separate data streams.

The MAX96722 is intended to be paired with Maxim GMSL2 serializers or previous generation GMSL1 serializers.

Several common multisensor use cases are supported with the MAX96722 being particularly well suited to surround-view sensor systems that include four physically separate cameras or other sensors. The simplest conceptual system following this topology includes four independent sensors, each with a serializer, routed to the MAX96722's four GMSL inputs. The resulting CSI-2 streams from each sensor are then routed separately to the four independent CSI-2 C/D-PHY outputs, providing a system with four independent inputs and outputs where each input's data is uniquely routed to a dedicated output. This scenario is detailed in [Figure 24](#).



*Figure 24. Four Independent Sensors with Dedicated CSI-2 Interfaces*

A similar example is the case where each GMSL link streams data from more than one sensor. The MAX9295D serializer, for example, includes a pair of independent CSI-2 input ports. As a result, each remote sensor location using this device could interface to two independent sensors with multiple data types. In this case, the data from each pair of remotely located sensors is separated within a given link by appropriately mapping the virtual channel of each source. The total combined video throughput shared by each pair of remotely located sensors is 3Gbps (minus GMSL2 overhead), and each sensor can utilize a unique output format (GMSL2 only, may be limited by the number of available video pipes). An example of this system is shown in [Figure 25](#). Each of the MAX96722's four GMSL inputs can be independently configured to create a system consisting of a hybrid of those shown in [Figure 24](#) and [Figure 25](#). In this case, some links support a single sensor while other links support multiple sensors, each of which has a unique output format. (This applies in GMSL2 mode only when multiple sensors utilize a common link).

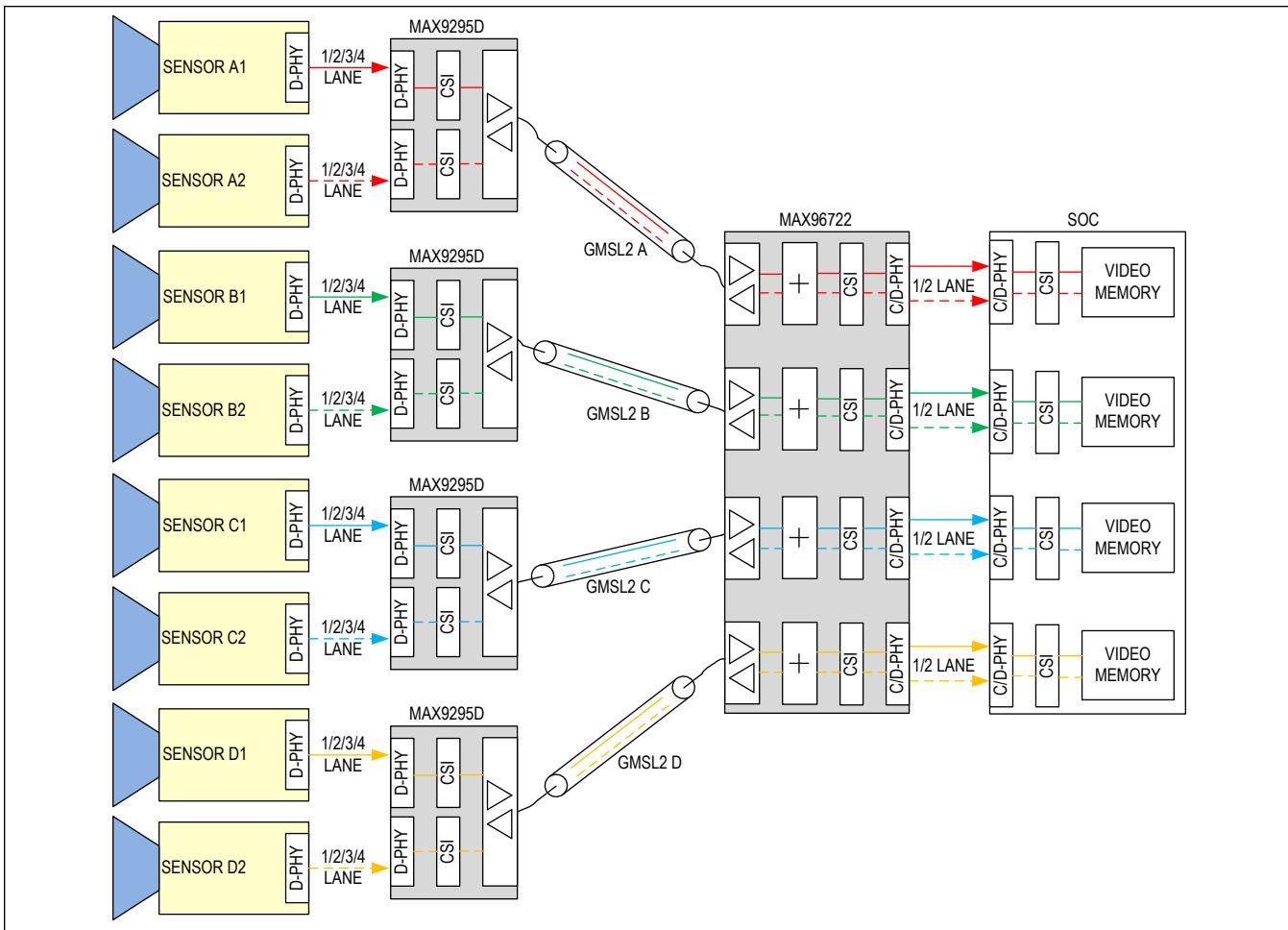


Figure 25. Four Independent Dual Sensors with Dedicated CSI-2 Interfaces

The MAX96722 also supports data aggregation and replication. These features allow simultaneous streams from different sensors to be combined within a single CSI-2 output stream (aggregation) and then routed to multiple CSI-2 output ports (replication). Thus, data from several sensors can be combined into a single stream that connects to more than one SoC. The result is a more efficient utilization of SoC input resources, because the combined stream is transferred to a single CSI-2 port on each SoC.

The sensors can have different video timing and resolution. The SoC identifies the video source by reading each packet's virtual channel ID. If both sources initially use the same virtual channel, the MAX96722 reassigns virtual channels so that separate streams can be identified by the SoC.

[Figure 26](#) illustrates an example of four sensor streams combined by the MAX96722 into a single CSI port that streams data from all sensors to the SoC.

Alternatively, partial aggregation is also possible. In this case, data from some sensors is combined within a common CSI stream while data from other sensors is concurrently routed to separate, independent CSI ports. (See [Figure 27](#).) In general, any incoming stream with a unique virtual channel ID can be independently routed to any CSI output regardless of which GMSL input sources the data. Each CSI output can simultaneously stream many virtual channels, enabling a single CSI port to transfer data from a wide range of remote sensors in physically separate locations.

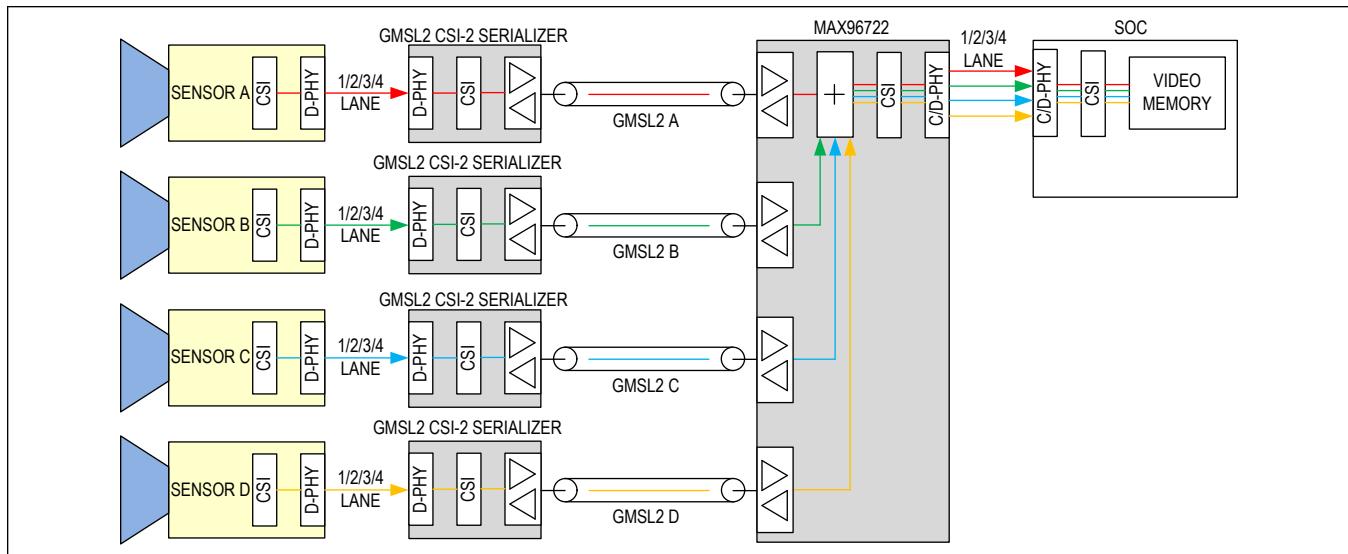


Figure 26. Four Independent Sensors Aggregated to a Single CSI-2 Output

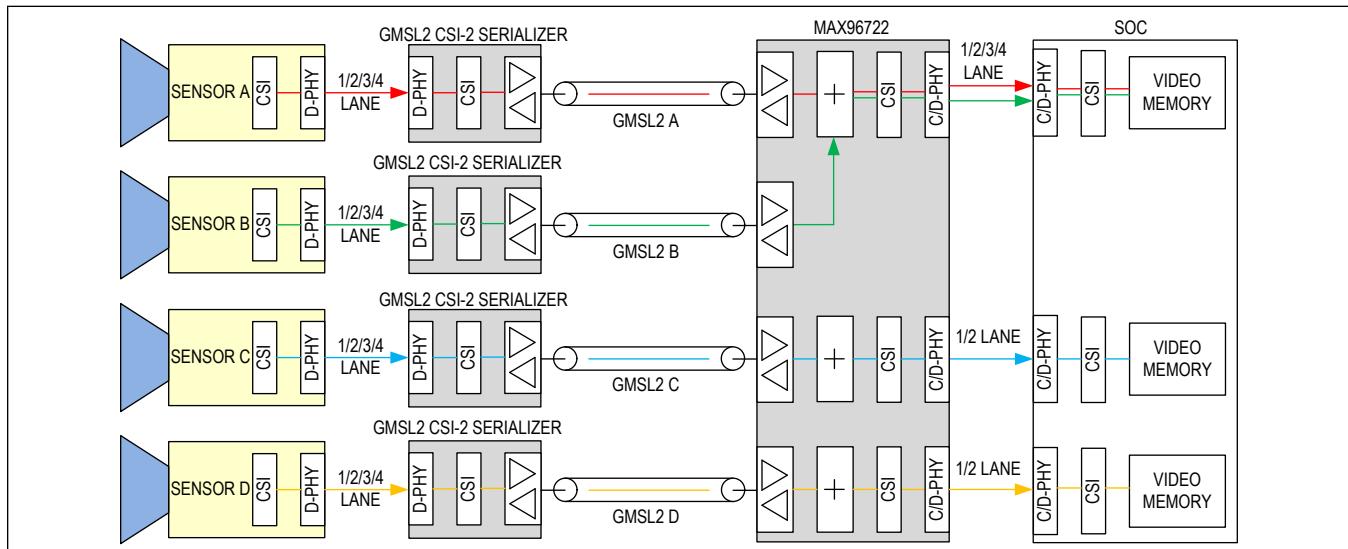


Figure 27. Four Independent Sensors Utilizing Partial Aggregation

Some applications require the video stream to be processed in parallel by multiple devices. In these cases, a single CSI-2 stream must be routed to multiple physical CSI-2 interfaces. The MAX96722 accommodates this requirement with the ability to replicate the output of any of the CSI-2 controllers to multiple C/D-PHY outputs as shown in [Figure 28](#).

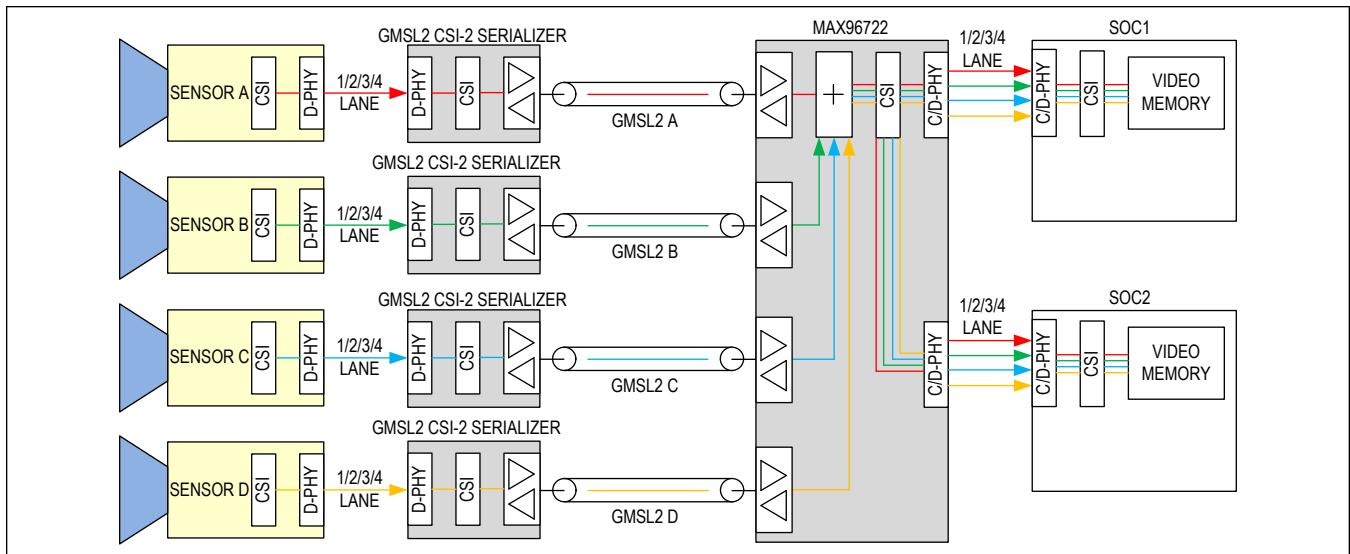
**MAX96722****Quad GMSL2 to CSI-2 Deserializer  
with GMSL1 Compatibility**

Figure 28. Four Independent Sensors Aggregated to a Single CSI-2 Stream and Replicated to Two PHY Outputs

The MAX96722's ability to simultaneously accommodate a variety of sensors with varied output formats extends to the GMSL link portion of the system. Each of the four links can independently accommodate a GMSL1 or GMSL2 serializer operating at any supported link rate. Each serializer can utilize any supported video input interface and format (within the constraints of the number of available video pipes). This enables a single MAX96722 to simultaneously interface with up to four unique types of sensors, each utilizing a different serializer with its own link configuration and video interface. The incoming data streams can be aggregated, enabling a single CSI-2 port to transfer all video data regardless of the serializer and link configuration used by each of the sensors. [Figure 29](#) illustrates an example of a mixed parallel GMSL1/CSI GMSL2 system with four sensors.

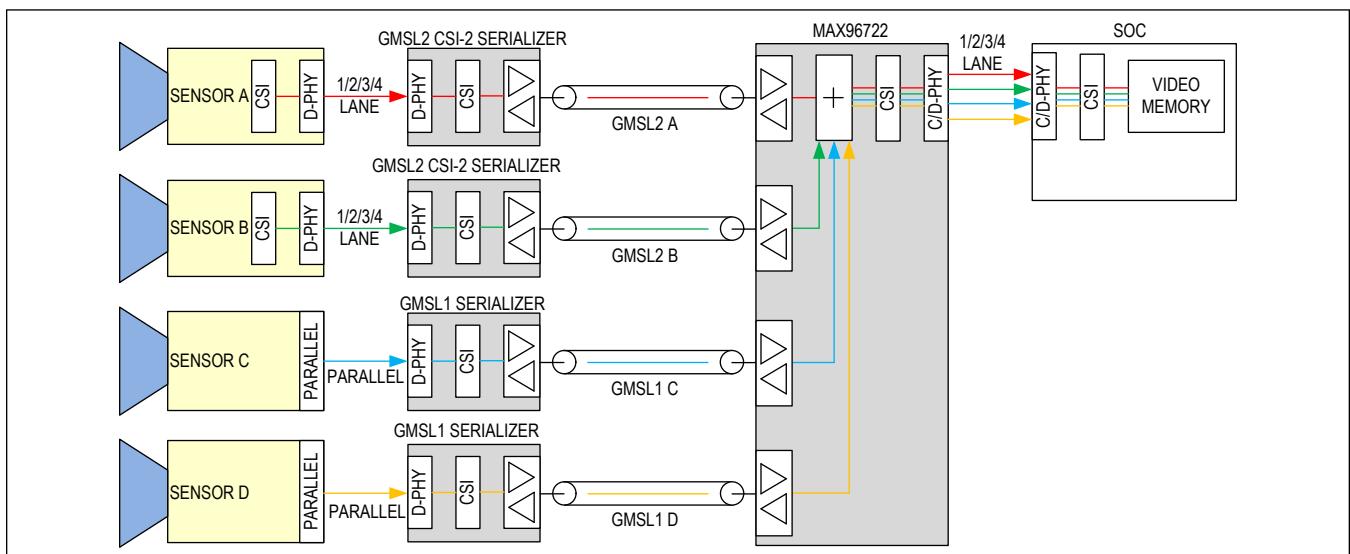


Figure 29. Four Independent Sensors with Mixed GMSL1/GMSL2 Links and Parallel/CSI-2 Video Ports

**GMSL2 Overview**

GMSL2 is a fixed-rate transmission medium designed to carry multiple types of communication channels concurrently.

The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or from an external reference frequency. The link clock is not related to the video pixel clock beyond the natural constraint that the video bandwidth cannot exceed the available link bandwidth.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth. The same data protocol is used on forward and reverse channels, and for both video and control-channel data.

GMSL2 provides a flexible broadband data link that can transport high bandwidth bidirectional data between remotely located devices. The MAX96722 is specifically designed to be an interface between multiple remotely located high resolution cameras or similar sensors and a centrally located processor with a particular focus on surround-view sensors. In addition to the core video/broadband streaming portion of the link, GMSL2 devices provide a variety of peripheral/auxiliary functions to enable flexible, robust system implementations.

Received video data is transferred to the SoC using an industry standard CSI-2 interface. Extensive signal routing options enable data from multiple remote sensors to be routed to a single video output port. A flexible video pattern generator providing common video test patterns and PRBS can be used to test downstream video devices to validate functionality of the CSI-2 interface.

GMSL2 supports a comprehensive suite of common embedded communication protocols. All devices utilize a primary I<sup>2</sup>C/UART control-channel interface that an ECU uses to access serializer and deserializer registers, as well as peripheral devices. This access can be initiated from either end of the link. The MAX96722 includes two additional I<sup>2</sup>C/UART ports that can be used to access lower priority local register or to communicate with remote serializers and peripherals. Each GMSL link provides a dedicated control channel through which any one of the three I<sup>2</sup>C/UART ports can communicate with the serializer or the peripherals connected to that link. Each link supports two additional tunneled pass-through I<sup>2</sup>C/UART channels that are available for remote peripheral communication. The connectivity of the I<sup>2</sup>C/UART ports can be configured independently for each of the GMSL links, enabling different I<sup>2</sup>C/UART ports to access the control channel and the tunneled channels of each link.

Two SPI master/slave interfaces, each including two slave select pins, are included in the MAX96722. The SPI interfaces enable a host SPI master on one side of the GMSL2 link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL2 devices. (A GMSL2 device can be configured as either a SPI master or a slave.) The two SPI ports are fully independent, and they function exclusively as pass-through ports without access to serializer or deserializer registers.

All GMSL2 devices include a versatile suite of GPIO pins that work with the GMSL2 peripheral communication protocols. In general the GPIOs function as user-defined inputs or outputs whose states can be either automatically forwarded across the link or controlled by register settings. GPIOs are typically used to tunnel low speed (<100Kbps) signals over the GMSL2 link, although rates in excess of 1MHz are also supported. A GPIO tunnel can be set up in the forward or reverse direction.

GMSL2 provides extensive data integrity and safety features, including watermark generation/detection, CRC error detection for control and video data, and ECC protection of video memory. Watermark generation and detection verifies that the video image is not frozen. CRC error detection enables identification of errors in the video or control data streams. In the case of control channel CRC errors, automatic re-transmission of the flagged packet maximizes control channel speed and reliability. The internal video memory includes ECC protection to enable detection and correction of internally corrupted pixel data.

GMSL2 devices incorporate numerous link margin optimization and monitoring functions that ensure high link margin and robust functionality. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor function provides continuous link margin diagnosis and includes various threshold alarm levels that trigger run-time alerts whenever link degradation is detected. PRBS checking verifies correct link and video channel operation.

### Video Pipeline

The video channel transmits high bandwidth video data from a serializer to a deserializer. (Video data only flows in the forward direction.) The MAX96722 supports a variety of common data types, including RAW8/10/12/14/16/20, RGB565/666/888, and YUV8/10-bit. The video channel offers extensive signal routing flexibility, enabling multiple cameras or other sensors to interface seamlessly with different C/D-PHY CSI output port configurations. It also includes several key safety features required in ASIL compliant systems (available only with GMSL2), and the internal memory associated with the video pipeline is ECC protected to ensure data integrity.

### Video Pipes, Aggregation, and Replication

In GMSL2 mode, the transmission of video data is based on the concept of video pipes. Carrying data in pipes allows GMSL2 to bridge different digital video interfaces and perform watermark generation and detection.

A pipe carries a video stream (or streams) and video synchronization data. Each pipe operates in one of three modes. In all modes a pipe can carry multiple concurrent video streams, with each stream having different virtual channels and data types.

Mode 1: Streams with constant bits per pixel (bpp) of up to 24bpp. The bpp of the streams must be the same.

Mode 2: Streams with 16, 14, 12, 10 or 8bpp. Streams less than 16bpp are padded with zeros.

Mode 3: Streams with two different bpp. The bpp of one stream must be twice the bpp of the other stream. The higher bpp stream maximum is 24bpp.

Mode 1 and Mode 3 carry data at full bandwidth but put more restrictions on bpp than Mode 2. Mode 2 allows streams with different bpp, but streams of less than 16bpp are carried using more bandwidth than necessary on the GMSL2 link because of zero padding. Mode 1 or Mode 3 are sufficient for most applications. Mode 2 requires less programming and is more convenient if the application does not require maximum link bandwidth.

The MAX96722 has four GMSL input ports, each accommodating up to four independent pipes in GMSL2 mode. In GMSL1 mode, only a single, dedicated video pipe is available per link. These capabilities are consistent with those of other GMSL2 devices. To accommodate the greater number of GMSL inputs and incoming video streams, the MAX96722 provides a total of eight internal video pipes that are shared by the four GMSL inputs as shown in [Figure 30](#). Each internal pipe can be mapped to any one of the incoming GMSL video streams, and as a result up to eight internal pipes can be mapped to a single GMSL2 input port. The combined total number of video pipes utilized by all connected serializers cannot exceed the eight internal pipes provided by the MAX96722. In GMSL1 mode, a total of four internal video pipes is available with fixed mapping between each GMSL1 input and a single internal pipe as shown in [Figure 30](#). In mixed GMSL1/GMSL2 systems, the GMSL1 input streams are routed to the dedicated GMSL1 pipe associated with each active GMSL1 input. Incoming GMSL2 streams can be routed to any of the available pipes not dedicated to an active GMSL1 input. In general, the content of any video pipe can be routed to any of the CSI output ports. The exception is that only pipes 0 to 3 are available sources for synchronous aggregation.

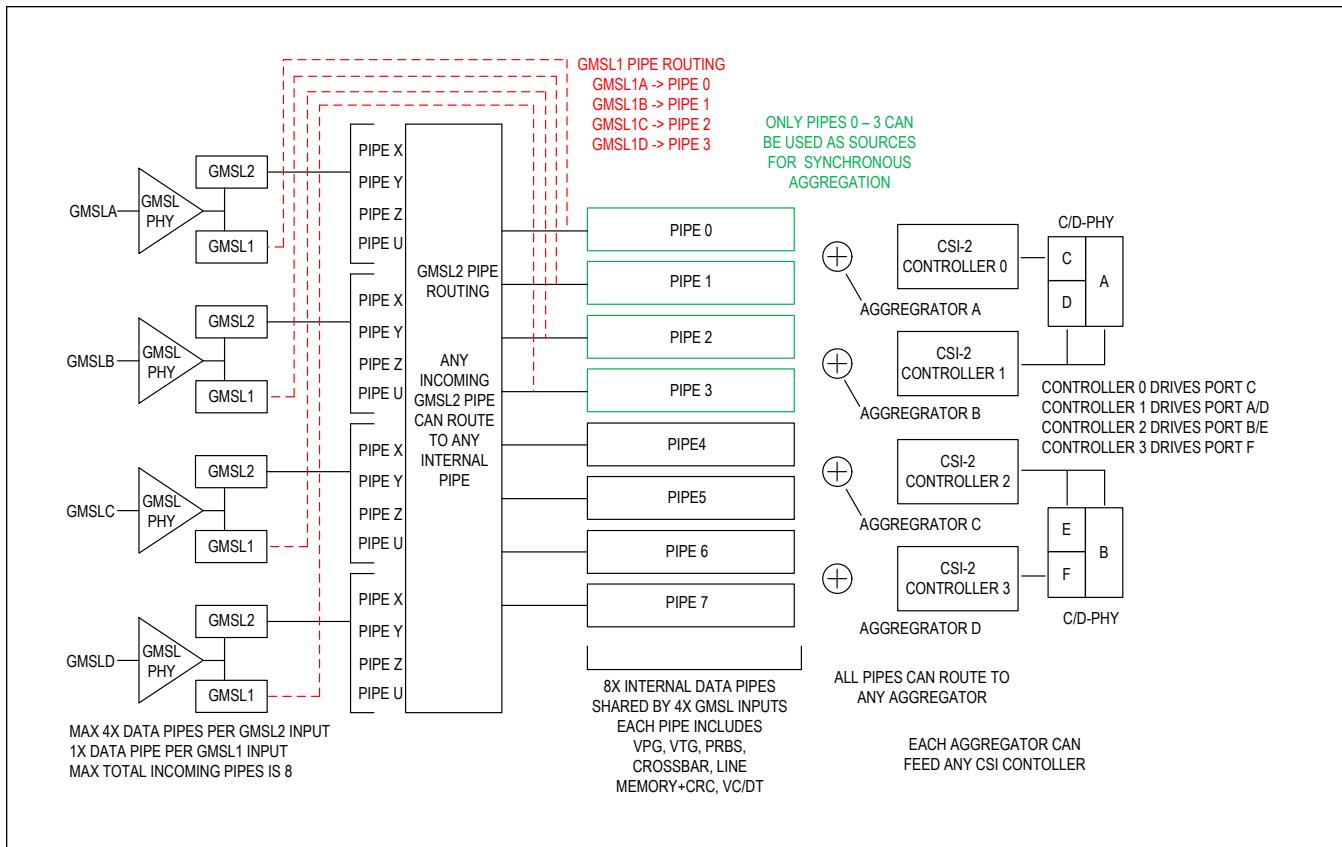


Figure 30. Video Pipes and Routing

In typical applications, a single camera requires either one or two pipes depending on whether it supports High Dynamic Range (HDR) imaging. For standard cameras using YUV422 formatted video, a single pipe is sufficient to transport all data. For HDR cameras using more complicated data formats, such as RAW16/8-bit Embedded Data and RAW12, a pair of pipes must be dedicated to carry the resulting video stream. The eight available internal pipes enable the MAX96722 to dedicate two internal pipes to each of the four cameras in a high definition surroundview system that uses quad HDR cameras. The example shown in [Figure 31](#) illustrates an application in which two links interface to HDR cameras (two dedicated pipes) while the other two links stream video from standard cameras (one dedicated pipe). GMSL1 operation limits each link to a single pipe, which reduces flexibility in handling certain types of sensor streams.

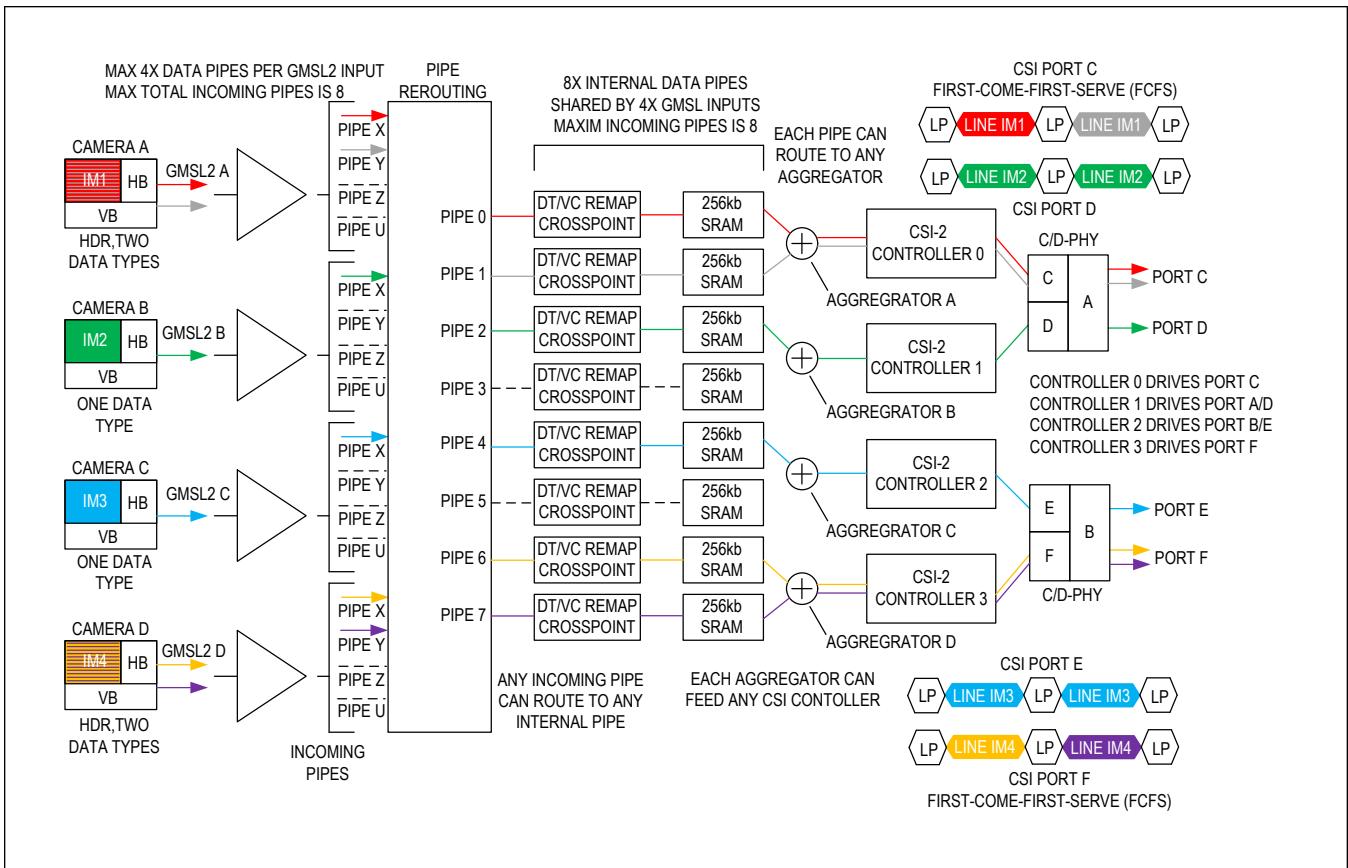


Figure 31. MAX96722 Video Pipe Example with Partial FCFS Aggregation

When video data is received by one of the MAX96722's GMSL inputs, it is immediately forwarded to one of the internal video pipes. Note that a single pipe can carry many separate streams, provided that they comply with certain mode dependent format limitations. The channel ID of each incoming CSI stream can be reassigned if desired, and the order of the bits can optionally be remapped using the RX crosspoint switch. Video data then fills the dedicated line buffer associated with each pipe as controlled by the sync data.

Each line buffer can be routed to any one of the four aggregators, which can be used to combine data from multiple video pipes and/or virtual channels within a single CSI-2 stream. Only one aggregator can read data out of a given buffer. Once data is read, it cannot be read a second time by another aggregator. Up to eight pipes can be aggregated by one aggregator. Video data can be routed according to DT or VC based on the source CSI-2 packet's DT/VC, or it can be routed by a DT/VC assigned in the MAX96722. For example, data in pipe 0 with VC0 can be programmed to be read out by Aggregator A while data in pipe 0 with VC1 can be programmed to be read out by Aggregator B. This maximizes data routing flexibility and enables multiple streams within a single pipe to be routed to separate CSI output ports.

Aggregated data is typically read out from line memory on a "First Come First Served" (FCFS) basis as shown in [Figure 31](#) and [Figure 34](#). In this case, data from all eight video pipes is visible to the aggregators. The order in which the line memories reach filled status is the order in which they are read out. When a complete line of video data has filled the line memory, it is routed as specified by the aggregator to one of the CSI controllers for packet generation. In this case, the outgoing CSI data streams can be viewed as independent parallel streams that may have independent timing, although they may be effectively synchronized depending on the nature of the video sources used.

Alternatively, data can be aggregated in specific sequences corresponding to side-by-side (4WxH) or line-interleaved (Wx4H) output formats (see [Figure 32](#)). All data sources must use the same resolution and virtual channel assignment, and they must be precisely synchronized. The resulting output is a single stream consisting of a superframe that holds

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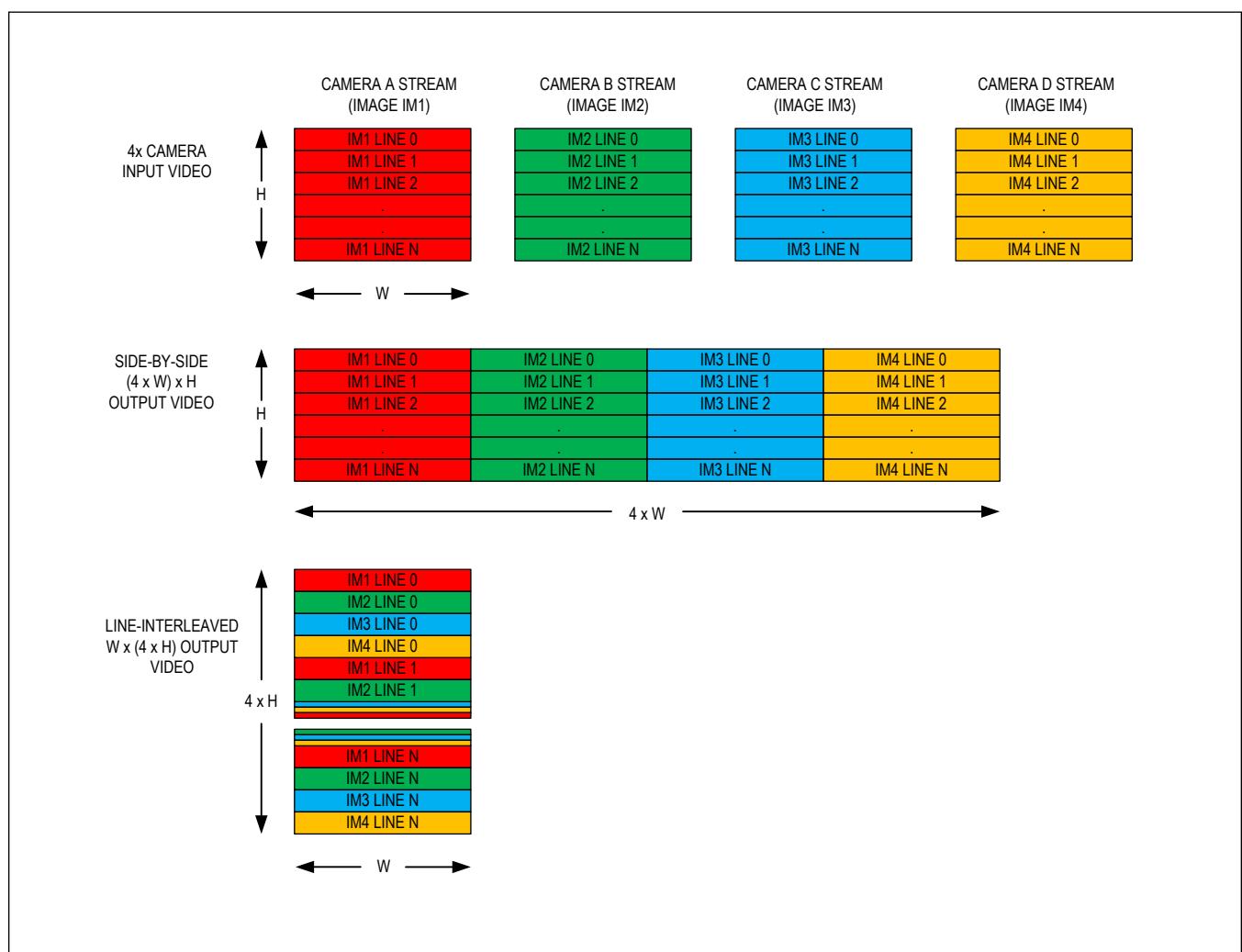


Figure 32. Side-by-Side and Line-Interleaved Synchronous Aggregation Frame Formats

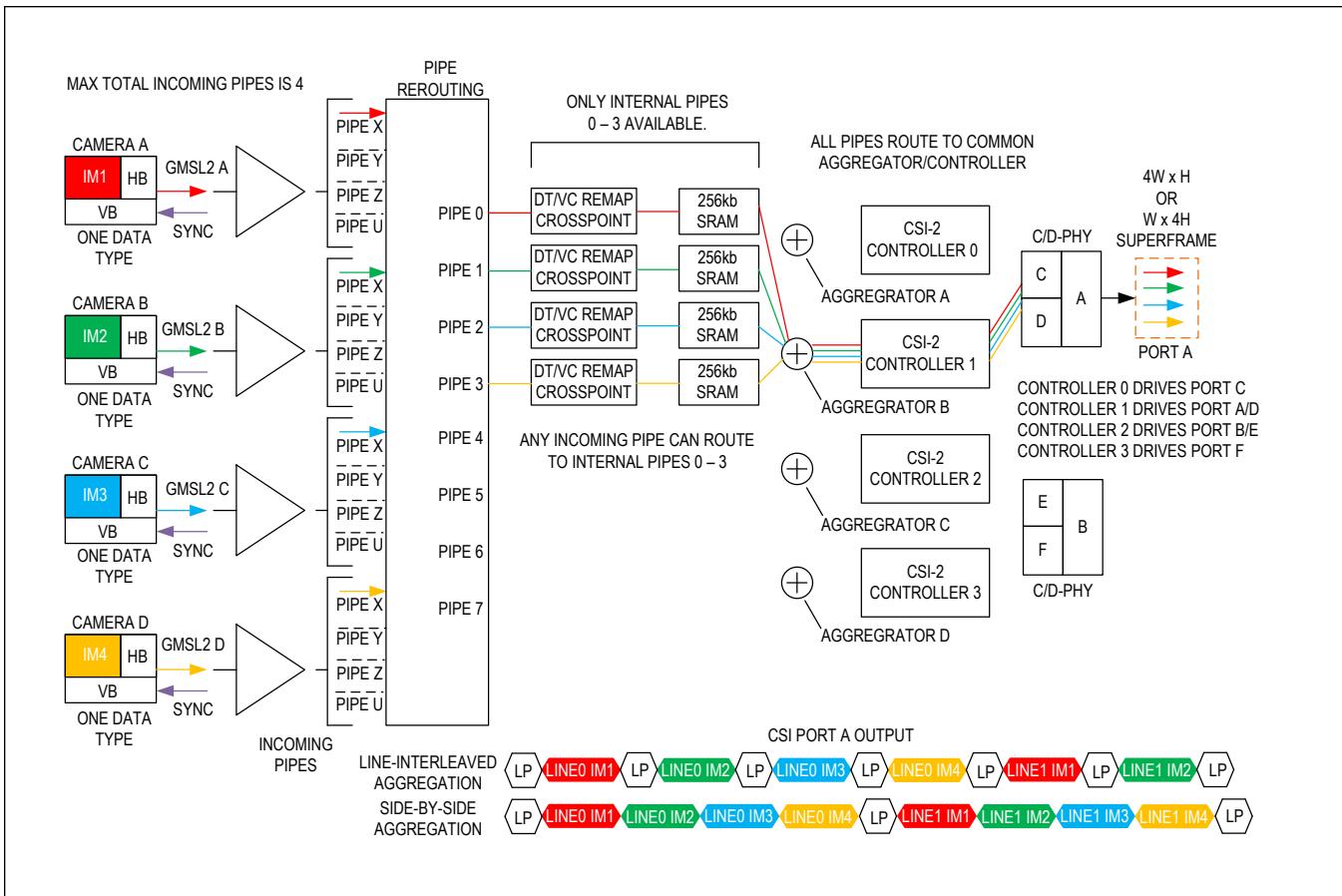


Figure 33. MAX96722 Video Pipe Example with Synchronous Aggregation

Regardless of the type of aggregation used, the output of each CSI controller can drive one or more CSI ports depending on whether replication is used and how the CSI ports are configured. For example, CSI controller 1 can output packets on C-PHY/D-PHY Port A and/or C-PHY/D-PHY Port B (and/or C-PHY/D-PHY Ports C/D/E/F depending on the configuration).

The MAX96722 includes features that minimize the disruption resulting from one of the links failing in multilink systems that use aggregation. With systems using synchronous aggregation, the MAX96722 masks the failed link's video data with 0's. This allows overall timing to continue as expected, enabling the remaining video streams to proceed uninterrupted. Similarly, with systems using FCFS aggregation, the video stream associated with a link that has failed will be terminated at the end of a line to avoid a sudden disruption that may impact other streams using the same physical interface.

[Figure 34](#) illustrates an example in which CSI controller 1 combines data from all four GMSL inputs with FCFS aggregation and then replicates the resulting output to CSI ports A and B. Note that a given PHY port can only accept packets from one controller. Data cannot be aggregated at the input of a PHY. All aggregation must be realized in the prior aggregation blocks. The CSI-2 port data rate needs to be programmed equal to or greater than the incoming data rate to prevent buffer overflow. Programming the output rate to be faster than the bandwidth of the incoming video increases packet spacing (LP time between packets).

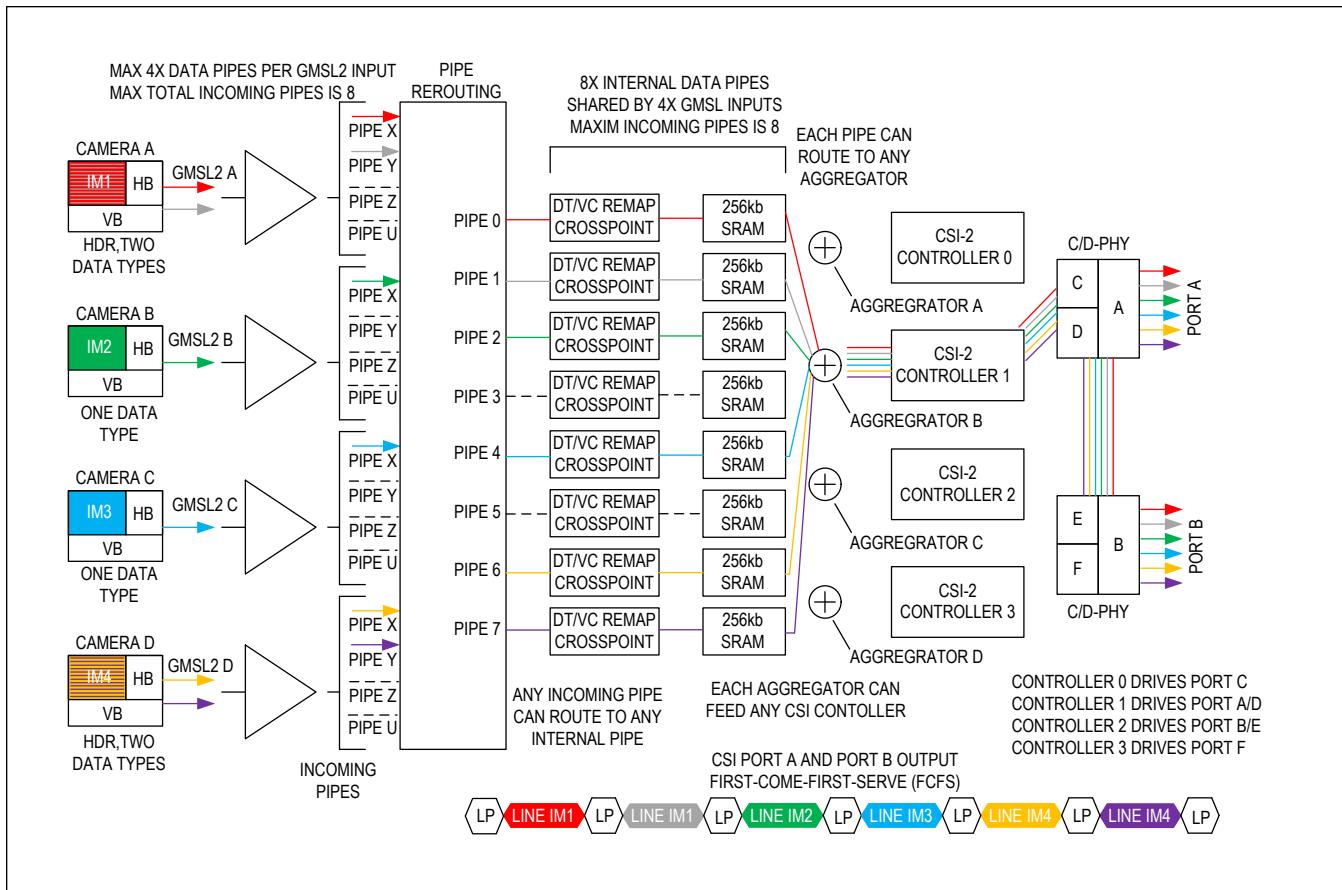


Figure 34. MAX96722 Video Pipe Example with FCFS Aggregation and Replication

### Video Crossbar

The incoming video stream or VPG output passes through a crossbar switch that enables arbitrary remapping of all bits in the video stream. A single bit can be remapped to multiple locations in the serial stream if desired. The default routing of the crossbar is such that no remapping occurs (crossbar function is completely transparent by default).

### Watermarking

The watermarking block allows users to detect a frozen frame failure between the generator and the detector in a frame-based processing system. This feature specifically targets frozen frames caused by errors in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector. The MAX96722 contains two watermark generators/detectors. This enables it to insert or detect a watermark concurrently on two safety critical video streams. The watermark generator inserts a time-varying watermark that is highly redundant and robust with respect to image processing and display stream compression. The watermark detector looks for this time-varying watermark. A failure to detect any of the generated watermarks indicates that a frozen frame failure has occurred between the generator and detector. In this error condition the watermark detector can generate an interrupt and/or blank the output video, returning the display to a safe-state in less than 500ms.

### Video Line CRC

The MAX96722 includes a GMSL video CRC error checker, which can be used in safety critical applications to guarantee the integrity of the video stream. The error checker utilizes a CRC32 polynomial function to generate a 32-bit CRC code for each received line of video data. This same CRC code is also generated on the serializer side of the link, and this code is transferred over the link to the MAX96722 along with the corresponding video data. The MAX96722 then compares

the CRC received from the serializer with the CRC it has generated for a given line of video data. Any discrepancy in the CRC codes indicates an error in the video data.

### Video Timing Monitor

The MAX96722 provides optional monitoring of the video sync signals HS, VS, and DE, which are not readily available via the CSI-2 outputs. The sync signals can be derived from the content of any of the eight video pipes. In both GMSL2 and GMSL1 modes, the sync signals can be driven to MFP pins (VS=MFP4, HS=MFP13, DE=MFP14) for monitoring. In addition, the sync monitor HS, VS, and DE signals can be observed using the VID\_HVD\_DET registers.

### Video Memory ECC Protection

The integrity of data propagating through the video pipeline's memory is guaranteed by ECC, which enables correction of 1-bit errors and detection of 1- or 2-bit errors per 32 bits of video data. This functionality provides protection of data that is not protected by the CRCs of the incoming GMSL stream or the outgoing CSI stream, eliminating the possibility that internally generated silent bit errors might corrupt the outgoing CSI-2 stream. The state of the ERRB pin can be used to detect the presence of errors. Intentional memory error injection is available for diagnostic purposes.

### Control Channel and Side Channels

A μC or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. The MAX96722 supports the following interfaces:

1. 3x I<sup>2</sup>C/UART
2. 2x SPI
3. 17x GPIO

Data from all interfaces tunnels through the GMSL2 link, but only one of the I<sup>2</sup>C/UART interfaces can access remote serializer registers at a given time over any one of the links. All I<sup>2</sup>C/UART ports offer concurrent access to local registers via arbitration. The default state of all I<sup>2</sup>C/UART ports is specified by the power-up state of the I2CSEL/MFP13 pin. See I<sup>2</sup>C/UART for further information.

Control and side-channel peripheral interfaces are accessed via multifunction GPIO pins (MFP pins). Multifunction pins have a default function and can be programmed to a variety of alternate functions after power-up. Due to a practical limit on the number of pins available on a given device, not all interfaces can be simultaneously supported. See the Multifunction Pin Configuration section and the [Pin Descriptions](#) for default and alternate multifunction pin functions as well as available combinations of interfaces.

### I<sup>2</sup>C/UART

The MAX96722 includes three independent I<sup>2</sup>C/UART interfaces. These interfaces are the only means by which local or remote (serializer) registers can be accessed. The operating mode of all three ports is set at power-up via the I2CSEL/MFP13 pin. Following power-up, the mode of each port can be independently changed by register programming. The master μC is typically located on the MAX96722 side of the link, although this is not strictly required, and communication can be initiated by a device on either side of the link. For correct operation, the control channel of each of the MAX96722's links must be configured in the same mode as the serializer connected to that link (both I<sup>2</sup>C or both UART; each link's control channel can use a different control channel port/mode with the constraint that each MAX96722 UART port can only be routed to one link). Unlike GMSL1 devices, there is no I<sup>2</sup>C-to-UART conversion capability. I<sup>2</sup>C/UART outputs are open drain and require appropriately-sized external pullup resistors for proper operation.

In general, each of the three I<sup>2</sup>C/UART ports can be used to access internal MAX96722 registers, remote serializer registers, and remote peripheral registers. All three ports provide concurrent local register access. Each GMSL2 link provides a dedicated control channel through which any one of the ports can communicate with either a remote serializer connected to that link or with any remote peripherals connected to the serializer's control channel port. Each link's control channel can be independently assigned to any one of the three I<sup>2</sup>C/UART ports. Each link includes an additional pair of tunneled pass-through channels for remote peripheral communication. For any given link, the tunneled pass-through channels can be assigned to the two I<sup>2</sup>C/UART ports that are not routed to the control channel. Routing of the I<sup>2</sup>C/UART ports to each link's control channel and tunneled channels is independent, enabling different combinations of local ports to access the control channel and the tunneled channels of each GMSL link.

Regarding local (deserializer) register access, all three ports provide simultaneous local access with lower indexed ports having the highest priority. In I<sup>2</sup>C mode, a local port's local register access cannot be disconnected unless the port is disabled. Therefore, all active I<sup>2</sup>C ports have local register access at all times. For a port operating in UART mode, local register access can be disabled by forcing the port into bypass mode.

Remote serializer registers are visible only by means of the dedicated GMSL2 link control channel, which supports only a single port. Therefore, only one port at a time can access remote registers over a given link. By default, port 0 is routed to the control channel of each link. With appropriate configuration, port 1 or port 2 can also be routed to the control channel to support remote serializer register access. The two ports not routed to the control channel can be tunneled to the remote side of the link and used for peripheral communication by using the GMSL2 serializer's pass-through functions. Links operated in GMSL1 mode do not support the GMSL2 serializer pass-through tunnels. As a result, any links operated in GMSL1 mode provide only a single control channel with both serializer and peripheral register access. Note that a remote pass-through interface still provides local register access unless the port is configured as a UART in bypass mode. Therefore, the MAX96722's I<sup>2</sup>C device address is always present on every active I<sup>2</sup>C port. [Figure 35](#) details the routing of the three I<sup>2</sup>C/UART ports.

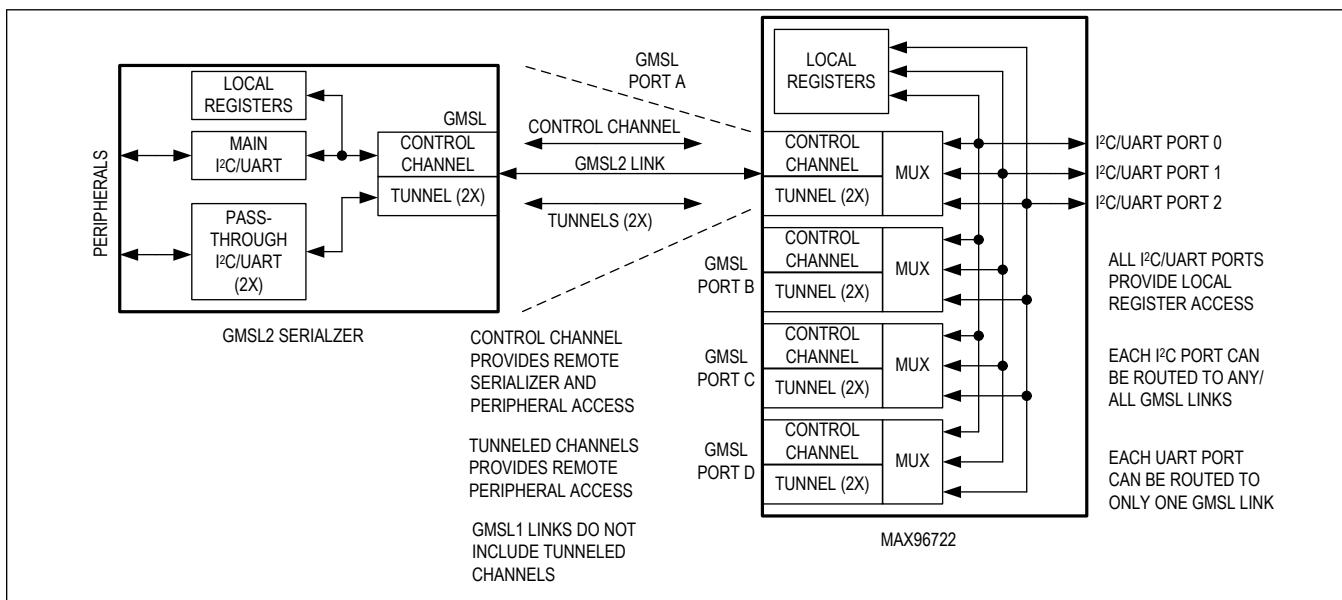


Figure 35. I<sup>2</sup>C/UART Control Routing

Each port's connectivity can be independently programmed for each of the four GMSL links. This enables different ports to access each link's control channel and tunneled channels. In addition, the tunneled channels can be enabled or disabled separately in each of the links, providing extensive flexibility in routing data from specific MAX96722 ports to particular remote devices. This is especially useful in UART applications, which lack I<sup>2</sup>C's intrinsic multidevice support and which are frequently limited to point-to-point communication between two devices. Ports operated in I<sup>2</sup>C mode can simultaneously communicate over any number of available GMSL links while ports operated in UART mode can only communicate over one link at a time.

In UART mode, the MAX96722 can either be configured to operate in base mode or bypass mode. In base mode, the host uses a special protocol that identifies the target device and register. Using this protocol, all UART ports provide concurrent local register access, and the UART port connected to a link's control channel can access remote serializer registers and protocol compliant remote peripheral registers associated with the link. In bypass mode, the serializer and deserializer ignore all control channel traffic, and the UART ports simply forward traffic across the link, effectively operating as pass-throughs. GMSL device register access is not possible in this case.

Each UART's mode is controlled by either the programmable shared local MS MFP function, a dedicated remote MS MFP function, or dedicated local control bits. When internal local registers are used to control the UART mode, each UART

can be independently placed in either temporary or permanent bypass mode. In temporary bypass mode, the UART port maintains bypass mode as long as traffic is present on the port. After a user-defined period of idle activity, the bypass mode times out and the port returns to base mode. In permanent bypass mode, the timeout is disabled and the port remains in bypass mode until a reset returns it to base mode. When a port is in permanent bypass mode, subsequent GMSL device register access through the port is blocked until after a reset.

If either local or remote MS MFP functions control an external UART's mode, the UART mode responds immediately to the specified MS MFP state. When a remote MS MFP function sets the UART mode, the MS pin controls only the mode of the UART connected to the remote device through the dedicated GMSL control channel. Thus, it is possible that MS MFP functions in different remote devices can be used to control the modes of different MAX96722 UART ports. A UART routed to a remote device as a remote pass-through does not change mode in response to the remote MS MFP function.

Any of the three UART ports can provide local access in addition to being connected to one of the GMSL link control channels. Thus, more than one port can operate as a control channel port that requires mode control. Depending on how UART mode control is realized, this could result in multiple ports relying on local MS MFP mode control. To meet this requirement, the shared local MS MFP function can be routed to all UART ports simultaneously.

When the user wishes to control only one UART's mode at a given time, great care must be taken in managing the routing of the local MS MFP. Otherwise, the modes of other UART ports could be inadvertently changed when not intended.

For details regarding operation of the I<sup>2</sup>C/UART interfaces, see [Control Channel Programming](#).

## SPI

The MAX96722 includes 2 independent SPI ports. SPI functionality is available only in links that use GMSL2 mode. These ports enable a host SPI master on one side of the GMSL2 link to control a peripheral SPI slave on the opposite side. Communication can be in either direction across the GMSL2 link. Each SPI port can communicate across one GMSL2 link at a time. The SPI clock range is 600kHz to 50MHz. Care must be taken to meet setup and hold time requirements when operating the interface at speeds higher than 20MHz. [Table 12](#) includes recommended settings for the SPI interfaces for optimal performance at different clock speeds.

## Control Channel Latency

All control channels exhibit finite latency. Typical latency for each function is given in [Table 3](#). For I<sup>2</sup>C, which requires an immediate ACK from the receiver following each byte, clock stretching is used to temporarily pause communication as the ACK propagates through the control channel. All I<sup>2</sup>C devices that communicate over the link must support clock stretching.

**Table 3. Control Channel Latency**

FUNCTION	FORWARD	REVERSE	NOTES
I <sup>2</sup> C	< 10µs	< 10µs	
UART	< 10µs	< 10µs	
SPI	< 10µs	< 10µs	Round Trip

## General Purpose Inputs and Outputs (GPIO)

GPIO are typically used to tunnel low speed (<100Kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward (serializer to deserializer ) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based. A GPIO packet is created and transmitted on the GMSL2 link when a rising or falling edge transition occurs at a GPI pin. The transition is regenerated at the corresponding GPO on the other end of the link.

Multifunction pins can be programmed as GPI (input), GPO (push-pull output or open-drain output, although some MFP pins only support open drain output) or GPIO (bi-directional input/output). Most GPIOs can also be programmed for 1MΩ or 40kΩ pullup or pulldown (or none). Although an internal pullup is provided, high-speed open-drain outputs require an appropriate value external pullup resistor to V<sub>DDIO</sub>. Inputs cannot be left floating. Always ensure that every pin configured as an input has a pullup or pulldown programmed or is driven by another IC or external pullup/pulldown.

A GPI on one side of the serial link can be mapped to either a single GPO or to multiple GPOs on the other side of the

link. Each GPI is assigned a pin ID, with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0-GPIO0, GPIO1-GPIO1, GPIO2-GPIO2, etc. However, the GPIO mapping can be arbitrarily changed by register settings.

GPI transitions can be transmitted in two modes: delay-compensated and non-delay-compensated. When delay compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases but jitter and skew decrease. The delay compensated mode's low skew is especially valuable when remotely located sensors must be precisely synchronized.

The state of each GPIO can be read or written by register either locally, using any of the three I<sup>2</sup>C/UART ports, or remotely via the I<sup>2</sup>C/UART interface that is routed to the GMSL2 control channel.

In non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible, based on priority and available link bandwidth. This variable delay is the result of multiple communication channels sharing the link. Non-delay-compensated mode can be used with signals tolerant to delay variation to minimize latency (i.e., μC interrupts).

Priority can be set for GPI pins via register control. If no priority is set, GPI transitions are transmitted in the order they occur. However, when priority is set, transitions on GPI with higher priority are transmitted earlier.

Typical GMSL2-only device delays for the 187.5Mbps reverse link is shown in [Table 4](#).

**Table 4. Typical GPIO Delays for Reverse Link Transmission**

GPIO CHANNEL	DELAY COMPENSATION	DELAY
GPIO forwarding from deserializer to serializer (187.5Mbps reverse channel)	0	6μs
	1	15μs

### GMSL2 Physical Layer

Maxim's GMSL2 family of serial links have transmitter and receiver capability enabled simultaneously, enabling full duplex operation on a single wire. A single cable between the serializer and deserializer delivers data being transmitted from each end of the link. Forward transmission is data being sent from the serializer to the deserializer. Reverse transmission is data being sent from the deserializer to the serializer.

The forward rate is fixed at 3Gbps. The reverse rate is fixed at 187.5Mbps.

Each of the MAX96722's four GMSL inputs can be independently configured for different link rates or GMSL2/GMSL1 operation.

### Cabling Options

GMSL1/2 supports either 50Ω coaxial or 100Ω shielded-twisted pair (STP) cabling. Cable attenuation and return loss characteristics must stay within the requirements of the GMSL Channel Specification to achieve robust full-duplex link performance. These requirements vary depending on GMSL1/GMSL2 mode and GMSL1 PCLK frequency. A wide range of cabling options are supported in both GMSL1 and GMSL2 modes.

Coax or STP mode and GMSL1/2 mode are configured upon startup and determine which cabling option applies. In coax mode, use only the noninverted SIO pin of a given link. AC-couple and terminate the inverting SIO pin using the series connection of a 100nF capacitor and a 49.9Ω resistor. In STP configuration, both the noninverted and inverted SIO pins of a given link are enabled by default.

Maximum cable length is limited by the frequency-dependent attenuation of the cable. Additionally, PCB and in-line connectors degrade the return loss characteristic of the cable assembly. The GMSL channel specification allows two inline connectors and provides detailed requirements for cable attenuation and return loss, as well as insertion loss and return loss requirements for PCB traces. In general, any physical channel implementation that is compliant with the GMSL channel specification can be used, with reliable results. Contact the factory to receive the GMSL Channel Specification document.

A 100nF AC-coupling capacitor is typically used for both GMSL1 (with high immunity) and GMSL2 links.

**GMSL2 Bandwidth Sharing**

The GMSL forward bandwidth is shared between video, the I<sup>2</sup>C/UART control channel, pass-through I<sup>2</sup>C/UARTs, SPI, GPIOs, and various protocol specific data exchanges (i.e. info frames, sync, and acknowledgements). The reverse channel bandwidth is also shared with all the above, with the exception of video packets, which cannot be transmitted over the reverse link.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

GMSL2 offers considerable flexibility in how link bandwidth is shared between the various communication channels requesting the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation: if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol fulfills this sharing requirement. The maximum packet size is limited to prevent one single channel from monopolizing the link bandwidth and to ensure other channels are served.

The video and control channel packets can be assigned a priority level. There are four priority levels: low, normal, high, and urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with stringent latency requirements can be assigned an increased priority.

**GMSL2 Bandwidth Calculations**

The GMSL2 forward link has a fixed link rate of 3Gbps. The reverse link rate is fixed at 187.5Mbps. The GMSL2 protocol overhead is roughly 14%. This leaves approximately 2.6Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

Worst-case applications must not exceed the available throughput of the forward and reverse links. Maxim's evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that estimates initial bandwidth requirements. Maxim offers other tools that are also useful for calculating link bandwidth utilization. Consult the factory for high-bandwidth use cases to ensure error-free performance.

[Table 5](#) provides rough estimates of the bandwidth utilization for each of the communication channels. Note that the video channel is available only in the forward link direction, and therefore bandwidth cannot be allocated to video in the reverse link. Bandwidth can be allocated to all other functions in both the forward and reverse directions.

**Table 5. Forward and Reverse Link Bandwidth Utilization**

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video	H x V x fps x bpp x (1% blanking/100) x 1.14
I <sup>2</sup> C	18 to 60 x I <sup>2</sup> C clock rate, depending on available link bandwidth
UART	6 x UART bit rate, 5.5 x when parity bit enabled
SPI	2.5 x SPI rate
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled

Definitions:

H = horizontal resolution

V = vertical resolution

fps = frames per second

bpp = bits per pixel

**Eye Opening Monitor**

The eye-opening monitor (EOM) enables GMSL2 parts to monitor the link-margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error free but have less link-margin than desired. The EOM allows the user to proactively react to deteriorating cable performance before any link errors occur. GMSL2 parts measure either the horizontal or the vertical eye opening of the equalizer's output. The

measurement is activated automatically at a ~1Hz rate once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye opening is then reported, and the EOM triggers an interrupt or a reset if the opening falls below user-defined thresholds.

### **Video PRBS Generator/Checker**

GMSL2 devices include built-in video PRBS generators/checkers for video link testing. For example, a serializer's PRBS generator can be used in conjunction with a deserializer's PRBS checker for testing the GMSL2 video channel that connects the two devices. In this case, the MAX96722's PRBS checker functionality compares the received PRBS stream with the predicted PRBS data to establish whether any errors are present.

The MAX96722 also includes video PRBS generator functionality that enables the testing of downstream video devices that receive video via the MAX96722's CSI-2 output. This includes GMSL2 serializers that are connected in a loopback configuration with CSI and GMSL video paths being tested at the same time.

Note that all link bandwidth is not used by the video channel alone in GMSL2 mode, so it is possible to have a bit error on the link which does not cause a video PRBS error. Additional discussion of this functionality can be found in the CSI Video Output Ports section.

### **Link Error Generator**

Each of the GMSL links includes a configurable error generator that injects errors into the outgoing data stream immediately prior to transmission. The deserializer injects errors into the reverse channel; the serializer injects errors into the forward channel. The receiving device detects, counts, and flags the errors, enabling a thorough validation of the system's response to error conditions of varying severity.

### **AEQ (Adaptive Equalization)**

The GMSL2 devices automatically adapt receiver characteristics to compensate for the insertion and return loss characteristics of the channel, which consists of the cables, connectors, and PCBs. This approach optimizes performance on any channel that meets the GMSL2 channel specification. The equalizer architecture helps guard GMSL2 links against the affects of noise, crosstalk, and reflections. Initial adaptation is performed during link lock. After the link is established, the AEQ continues running in the background, updating settings at a rate of ~1Hz to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye opening by using the built in eye-opening monitor.

### **GMSL1 Backwards Compatibility**

The MAX96722 is designed to pair with any GMSL1 serializer. However, the device does not support the entire range of features available across all GMSL1 serializers. GMSL1 backwards compatibility is only supported with forward link rates from 500Mbps to 3.12Gbps and a reverse link rate of 1Mbps. When paired with a GMSL2 serializer for GMSL1 operation, both devices must be configured to use GMSL1 compatibility mode. When the MAX96722 is paired with a legacy GMSL1 only serializer, the MAX96722 must be configured for GMSL1 compatibility mode, and the available forward link rate is reduced to the rate limitations of the specified GMSL1 serializer.

[Table 6](#) specifies the availability of common GMSL1/GMSL2 features in GMSL2 devices that are operated in GMSL1 mode. Note that some GMSL2 features, such as SPI, are only available in GMSL2 mode, and as a result they are never available in GMSL1 mode, regardless of the devices used. If a feature is not supported by both devices in a link, then it should be disabled. To utilize a feature, it must be enabled and configured consistently so that appropriate settings are applied to both ends of the link.

Most features specified in [Table 6](#) can be enabled or disabled by appropriate register configurations and by the state of the CFG0 and CFG1 input pins at power-up. Hardware design of both serializer and deserializer subsystems must account for correct connection of configuration pins to achieve the desired settings. Interfacing coax interconnects to non-coax capable GMSL1 devices requires special hardware considerations to ensure reliable functionality. Contact the factory for additional information regarding general GMSL1 operation or GMSL1/GMSL2 device interoperability.

**Table 6. Feature Availability in GMSL1 Mode**

FEATURE NAME	GMSL2 SERIALIZER IN GMSL1 MODE	GMSL2 DESERIALIZER IN GMSL1 MODE
Coax	Yes	Yes
Bus Width Select (BWS)	Yes	Yes
High-Bandwidth Mode (HIBW)	Yes	Yes
Data Rate Select (DRS) (Low-Speed Mode)	Yes	Yes
DBL (Double Mode)	Yes	Yes
HSYNC/VSYNC Encoding	Yes	Yes
Pixel CRC (6 bits per pixel)	Yes	Yes
Video Line CRC (32 bits per line)	Yes	Yes
Hamming Error Correction	No	No
I <sup>2</sup> C to I <sup>2</sup> C	Yes	Yes
UART to UART	Yes	Yes
UART to I <sup>2</sup> C	No	No
Pass-Through I <sup>2</sup> C Channels	No	No
I <sup>2</sup> C Address Translation	Yes	Yes
SPI Control Channel	No	No
High-Immunity Mode	Yes	Yes
REV_FAST with HIBW Mode	Yes	Yes
Packet Control Channel with CRC	Yes	Yes
Packet CC Retransmission	Yes	Yes
Configuration Link	Yes	Yes
GPI to GPO on Reverse Channel	Yes	Yes
Frame Sync	Yes	Yes
Delay Compensated GPI/GPO	No	No
UART Base Mode	Yes	Yes
UART Bypass Mode	Yes	Yes
Spread Spectrum	Yes	Yes
Pre/De-emphasis	No	N/A
Legacy Programmable Equalization	N/A	No
GMSL1 Adaptive Equalization	N/A	Yes
Twisted-Pair Splitter Mode	No	N/A
Watermark	Yes	Yes
Video Timing Generator	Yes	No
Video Crossbar	Yes	Yes
PRBS	Yes	Yes
CNTL0,1,2,3 on Forward Channel	Yes	Yes
A/V Status Register Interrupt	No	No
HS/VS/DE Inversion	Yes	Yes
WS/SCK Inversion	Yes	N/A

**Table 6. Feature Availability in GMSL1 Mode (continued)**

Jitter-Filtering PLL	No	No
Sleep Mode	Yes	Yes
Line-Fault	Yes	Yes

### CSI Video Output Ports

The MAX96722 includes a flexible CSI-2 compliant video output supporting both the D-PHY v1.2 and C-PHY v1.0 standards. The output includes a total of eight data lanes and four independent CSI-2 controllers. These can be configured as four 2-lane ports, which can be combined to alternatively provide two 4-lane ports or a combination of one 4-lane and two 2-lane ports. Each 4-lane port can consist of one, two, three, or four data lanes while each 2-lane port includes either one or two active data lanes. Each D-PHY lane supports HS data rates from 80Mbps to 2.5Gbps while each C-PHY lane supports HS data rates of 182Mbps to 5.7Gbps. To simplify signal routing, lanes within a given port can be arbitrarily assigned via lane swapping, and their polarity can be inverted if desired. Each CSI port is fully independent, and the user can separately configure or reset each port to suite the requirements of a given application.

### Video Pattern Generator

The MAX96722 includes a pair of flexible video pattern generators (VPG) that serve as a valuable tool for debugging video path functionality. Link lock is not required for VPG operation. Therefore, the VPG feature can be used even when the GMSL link is not functional. For optimal convenience, the VPGs are clocked based on the integrated 25MHz oscillator that provides global clock generation, eliminating the need for the user to provide a dedicated external clock for use with the VPG feature. Available PCLK frequencies are 25MHz, 75MHz, 150MHz, and 375MHz.

Each VPG supports a wide range of video resolutions and frame rates. Two video pattern options are available. The first option is a color gradient; the second option is a checkerboard pattern. All patterns are typically generated using 24b RGB color space. The outputs of the two generators can be synchronized if desired, and the resulting streams can be routed to any of the available C/D-PHY outputs. Aggregation and replication features can be used in conjunction with the VPG produced data streams.

### Video PRBS Generator/Checker

In addition to the checkerboard and gradient video pattern generators discussed above, each of the internal video pipes includes a video PRBS generator/checker. The available sequences are PRBS7, PRBS9, and PRBS24 at PCLK frequencies of 25MHz, 75MHz, 150MHz, and 375MHz. As is the case for the gradient and checkerboard patterns, the PRBS sequences can be routed by the aggregation and replication capabilities of the MAX96722, and they are packetized into CSI-2 compliant streams at the CSI output. The video PRBS stream can be checked by a device located at the opposite end of the CSI-2 link or routed back to the MAX96722 in a loopback configuration using a CSI-2 input serializer that drives one of the MAX96722's GMSL inputs. For more information on the video PRBS functionality, see GMSL2 Overview.

### CSI Output Raw PRBS Generator

The MAX96722 facilitates MIPI PHY characterization by enabling the generation of PRBS output streams in HS transmit mode directly from each C-PHY/D-PHY output lane. The available patterns are PRBS9, PRBS11, and PRBS18, and the resulting output data is a continuous stream that is not packetized by the CSI-2 controllers.

### CFG Latch at Power-up Pins

Voltage levels at the CFG0 and CFG1 pins are latched at power-up, or upon a low-to-high transition of PWDNB. These levels set initial register values and functional modes that may not be easily programmed through I<sup>2</sup>C or UART after the IC powers up. The CFG pins select device address, GMSL2 or GMSL1, serial rate, coax or STP, and high immunity mode. The user must identify the desired power-up state of the MAX96722 and correspondingly select the values of the resistors connected to CFG0 and CFG1 according to [Table 7](#) and [Table 8](#).

The voltage level for each pin is set by an external precision resistor divider connected between V<sub>DDIO</sub> and ground, or for some configurations, by a single resistor connected to V<sub>DDIO</sub> or ground. [Table 7](#) and [Table 8](#) show the recommended

resistor values to select each configuration. The voltage level at the CFG pins is latched about 1ms after all MAX96722 supplies reach minimum levels required by the power-on reset (PoR) circuit.

**Table 7. CFG0 Input Map**

CFG0 INPUT VOLTAGE (PERCENTAGE OF $V_{DDIO}$ ) (NOTES A, B)			SUGGESTED RESISTOR VALUES ( $\pm 1\%$ TOLERANCE) (NOTE C)		MAPPED CONFIGURATION (NOTE D)
MIN	TYP	MAX	R1 ( $\Omega$ )	R2 ( $\Omega$ )	DEVICE ADDRESS
0.0%	0.0%	11.7%	OPEN	10000	0x52
16.9%	20.2%	23.6%	80600	20500	0x54
28.8%	32.1%	35.5%	68100	32400	0x5A
40.7%	44.0%	47.4%	56200	44200	0x92
52.6%	56.0%	59.3%	44200	56200	0x96
64.5%	67.9%	71.2%	32400	68100	0x9A
76.4%	79.8%	83.1%	20500	80600	0xD2
88.3%	100%	100%	10000	OPEN	0xD6

**Table 8. CFG1 Input Map**

CFG1 INPUT VOLTAGE (PERCENTAGE of $V_{DDIO}$ ) (NOTES A, B)			SUGGESTED RESISTOR VALUES ( $\pm 1\%$ TOLERANCE) (NOTE C)		MAPPED CONFIGURATION (NOTES D, E)		
MIN	TYP	MAX	R1 ( $\Omega$ )	R2 ( $\Omega$ )	CXTP	GMSL1/GMSL2	HIM/ GMSL2 Rate
16.9%	20.2%	23.6%	80600	20500	COAX	GMSL1	HIM Enabled
28.8%	32.1%	35.5%	68100	32400			HIM Disabled
52.6%	56.0%	59.3%	44200	56200	STP	GMSL2	3Gbps
64.5%	67.9%	71.2%	32400	68100		GMSL1	HIM Enabled
76.4%	79.8%	83.1%	20500	80600			HIM Disabled
88.3%	100%	100%	10000	OPEN	COAX	GMSL2	3Gbps

#### Notes:

A) Voltage divider resistor tolerance,  $V_{DDIO}$  supply ripple, and external loading must not cause the CFG0 or CFG1 input voltage to exceed the maximum or minimum limits.

B) Until the input voltage is latched, any load on CFG0 or CFG1 (other than R1 and R2) must be  $\geq 25 \times (R1 + R2)$ . Load capacitance (including R1 and R2) must be lumped-load  $\leq 10\text{pF}$ .

C) Each resistor in the voltage divider must be  $\leq 100\text{k}\Omega$ .

R1 connects to  $V_{DDIO}$ , R2 connects to GND.

D) DEVICE ADDRESS: Device Address

CXTP: Shielded twisted-pair (SIO\_P, SIO\_N) or coax (SIO\_P) serial link.

GMSL1/GMSL2: GMSL1 or GMSL2 operating mode.

HIM applies when GMSL1 operating mode is selected. High Immunity Mode for reverse control channel.

GMSL2 rate applies when GMSL2 operating mode is selected. Rate fixed at 3Gbps forward and 187.5Mbps reverse.

E) GMSL1 default BWS = 0 (24-bit).

#### Multifunction Pin Configuration

The MAX96722 provides a wide range of peripheral I/O functions. These functions are mapped via register control to an

array of multifunction pins (MFP). Each MFP has several possible functions, but only one can be used at a time.

In most cases, MFP pins can be used as a generic I/O pins. However, a limited number of pins support only CMOS GPO functionality or open drain output functions. MFP13 is a special case. It defaults to GPO only, which is a useful debug feature that enables a toggling GPI on the opposite side of the link to be tunneled across the link with minimal programming. To enable input functionality of this pin, register bit ASIL\_GPIO\_EN must be written to a value of 1.

The various peripheral interfaces and other special functions are distributed between different pins, enabling the user to utilize a variety of interfaces and special functions simultaneously. Some functions require only a single MFP pin, but many are implemented across a group of MFPs. For example, ERRB is a single MFP while an SPI interface requires several pins. A user selects MFP functions to suit their use-case by programming the appropriate registers.

The [Pin Descriptions](#) shows default and alternate functions for each MFP, listed in order of priority (highest priority listed first). [Table 9](#) also shows priority, with highest priority on the left. A higher priority function must be disabled when a lower-priority function is enabled, both by register writes.

**Table 9. MFP Pin Function Map**

PIN	LATCH ON POWER-UP	I <sup>2</sup> C/UART FSYNC	SPI	GMSL1 GPI MS LOCK ERRB	LINE-FAULT	MONITOR	GMSL1 CNTL	GPIO	SPEED GROUP
MFP0				MS	LMN6			GPIO0	D
MFP1				LOCK				GPIO1	D
MFP2		FSYNC		GPI1				GPIO2	D
MFP3				ERRB				GPIO3	D
MFP4		SDA2/RX2		GPI0		VS		GPIO4	D
MFP5			SCLK_0		LMN7			GPIO5	C
MFP6			MOSI_0		LMN0		CNTL1	GPIO6	C
MFP7			MISO_0		LMN1		CNTL2	GPIO7	C
MFP8		SDA1/ RX1(alt)	BNE_0/ SS1_0		LMN2		CNTL3	GPIO8	B
MFP9		SCL1/ TX1(alt)	RO_0/ SS2_0		LMN3		CNTL0	GPIO9	B
MFP10		FSYNC(alt)	SCLK_1	GPI2	LMN4			GPIO10	A
MFP11		SDA1/RX1	MOSI_1					GPIO11	A
MFP12		SCL1/TX1	MISO_1					GPIO12	A
MFP13	I2CSEL		BNE_1/ SS1_1			HS	CNTL4	GPO13 (GPIO13)	B
MFP14		SCL2/TX2	RO_1/ SS2_1	GPI3	LMN5	DE		GPIO14	B
MFP15		SDA/RX						ODO15/ GPI15	I <sup>2</sup> C
MFP16		SCL/TX						ODO16/ GPI16	I <sup>2</sup> C

The drive strength of most MFP outputs is adjustable. These MFPs are placed in one of four speed groups, each having an adjustable output transition time setting (TTS). Pins are grouped together according to the most frequently used functions available across multiple pins. Except for I<sup>2</sup>C/UART and GPI/ODO functions, whose transition times are fixed and specified as I<sup>2</sup>C speed group, the transition time of each speed group can be changed from the default value by register programming. When the speed group's transition time is changed, the transition time of all MFP's in the speed group is changed. Certain MFP functions override the TTS setting. For example, I<sup>2</sup>C/UART MFP functions automatically

switch the MFP output driver to an open drain output whose speed corresponds to the I<sup>2</sup>C speed group.

Transition times depend on the transition time setting and V<sub>DDIO</sub> supply voltage. Refer to [Table 10](#) for typical rise and fall times for each TTS setting. The suggested TTS setting for each speed group at both common V<sub>DDIO</sub> supply voltages is shown in [Table 11](#). To change drive strength of a group of pins, simply find the desired I/O function in [Table 9](#) and check the speed group with which it is associated. This is specified in the Speed Group column. The relevant register field for each speed group is called x\_SPEED, where x is A, B, C, or D depending on the speed group. The register field can be programmed with one of the four possible TTS settings given in [Table 10](#) to specify the transition time of a given group of pins. MFP pins associated exclusively with speed group I<sup>2</sup>C have fixed output drive strength, and as a result no register adjustment of TTS is available for these pins. MFP functions with dedicated open drain outputs, such as I<sup>2</sup>C/UART, ERRB, and LOCK, automatically override the output driver configuration so that register control of drive strength is bypassed.

**Table 10. MFP Pin Typical Output Rise and Fall Times**

TRANSITION TIME SETTING (TTS)	RISE TIME (ns) (20% to 80%), C <sub>L</sub> = 10pF		FALL TIME (ns) (80% to 20%), C <sub>L</sub> = 10pF	
	V <sub>DDIO</sub> = 1.8V	V <sub>DDIO</sub> = 3.3V	V <sub>DDIO</sub> = 1.8V	V <sub>DDIO</sub> = 3.3V
00	1.0	0.6	0.8	0.5
01	2.1	1.1	2.0	1.1
10	4.0	2.3	4.3	2.9
11	8.8	5.0	10.1	5.1
I <sup>2</sup> C	N/A	N/A	40	30

**Table 11. Suggested MFP Pin Speed Settings**

SPEED GROUP	SUGGESTED TTS	
	V <sub>DDIO</sub> = 1.8V	V <sub>DDIO</sub> = 3.3V
A	01	10
B	11	11
C	01	10
D	11	11

### Speed Programming for SPI

The SPI interface can be used over a wide range of frequencies. The MAX96722 provides flexible GPIO speed programming (see Multifunction Pin Configuration) to maintain timing margins while minimizing radiated EMI. [Table 12](#) provides guidance on recommended speed settings for various SPI operating frequencies and V<sub>DDIO</sub> supply voltages while [Table 10](#) details the typical transition time associated with each available drive strength setting.

At lower frequencies, SPI data is typically latched on the opposite clock edge from which it is shifted as shown in [Figure 22](#) and [Figure 23](#). However, to meet timing requirements at higher frequencies, the data must be latched on the same edge as the shift. [Table 12](#) provides guidance for programming the latching clock edge.

**Table 12. Recommended SPI Pin Programming**

FREQUENCY (MHz)	V <sub>DDIO</sub> (V)	LATCHING EDGE	RECOMMENDED TTS
< 12.5	1.7 to 2.24	Opposite From Shift	01
	2.25 to 3.6		10
12.5 to 25	1.7 to 2.24	Opposite From Shift	00
	2.25 to 3.6		01
25 to 50	1.7 to 2.24	Same As Shift	00

**Table 12. Recommended SPI Pin Programming (continued)**

	2.25 to 3.6		01
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### Power-up and Link Start-up

GMSL2 ICs are in power-down mode when the PWDNB pin is low or when any of the power supplies are disabled. When in power-down mode, device configuration is reset to the default power-up state.

The serializer and deserializer can power up in any order. After PWDNB is released and all power supplies have settled, each device starts its power-up sequence and performs the following operations:

1. Latch CFG and I2CSEL pin states and set internal registers accordingly. See [Table 7](#) and [Table 8](#).
2. Main control channel (I<sup>2</sup>C or UART) is functional on local side. Local device registers are writable and readable. Perform local configuration as needed to establish links.
3. Links are established based on default configuration specified by CFG1 pin power-up state, which specifies global configuration for all links.
4. Perform link calibration, equalizer adaptation, and data channel locking. LOCK pin is driven high when all enabled links are locked and ready. The status of individual links can be monitored by reading individual link lock status bits.
5. Control channel is available from/to remote side.
6. If using the internal VDD regulator ( $V_{DD} = 1.2V$ ), enable the regulator function as described in the Power Supplies section.

After each link is established, all devices associated with that link can be configured. This can be done locally or remotely over the control channel by a microcontroller on either side of the link.

### Device Reset

There are three general reset options available through register writes:

1. RESET\_ALL resets all blocks including all registers and digital and analog blocks. This is similar to driving the PWDNB pin low and then high. This bit is automatically cleared when written.
2. Setting RESET\_LINK\_x resets all GMSL PHY related logic as well as the data pipeline for the specified link (where x is A, B, C, or D). After this bit is set, all local control registers are still accessible. The link remains in RESET until the bit is cleared.
3. Setting RESET\_ONESHOT\_x resets all GMSL PHY related logic and the data pipeline for the associated link (where x is A, B, C, or D). The bit then automatically clears itself. This is similar to setting and then clearing one of the RESET\_LINK\_x bits.

When configuring a GMSL link, program registers which control operation of the desired GMSL link first, then issue a link reset using the associated RESET\_LINK\_x or RESET\_ONESHOT\_x bits.

### Link and Video Lock

#### Link Lock

Link lock occurs automatically following power-up as part of the power-up process. Successful lock is an indication that all cables are plugged in and the system is up and running. Lock is obtained with no interaction between the microcontroller and GMSL devices. An open-drain LOCK output pin and a related status register bits indicate the lock status. In the case of the MAX96722, all four available links are enabled by default, and the LOCK indication pin is driven high only when all links are locked. The lock status of individual links is available via the lock status bit associated with each link.

Link lock indicates that the PLLs for the GMSL2 link are locked to each other and the data receive paths are locked (forward channel in serializer, reverse channel in deserializer). Video and control channel functions (I<sup>2</sup>C/UART, SPI, and GPIO) can be used immediately after link lock is asserted.

GMSL2 devices utilize the crystal or external reference input as the reference clock for the GMSL2 link, so a valid video input is not needed for the GMSL2 link to lock.

## Video Lock

Video lock indicates that the deserializer is receiving valid video data. After the GMSL2 link has locked, the deserializer video output PLL will initiate its locking sequence. The deserializer normally starts outputting video data several milliseconds after it asserts link lock, provided that it is receiving video packets from the serializer. Video lock status is typically read from a register. However, the deserializer LOCK pin behavior can be changed by a register setting so that the LOCK pin is asserted only when the deserializer is outputting video.

## Clocking

### Reference Clock

GMSL2 devices require a reference clock source to generate the 6GHz line rate clock and associated internal clocks. Both serializers and deserializers are clocked via 25MHz crystals or external low jitter 25MHz clock sources with a frequency accuracy of  $\pm 200\text{ppm}$ .

### Spread-Spectrum Clocking

Maxim's GMSL2 links provide exceptional EMI performance. Optional spread-spectrum clocking (SSC) is available to mitigate electromagnetic interference emitted from devices and inter-connections and provide additional margin. SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to  $\pm 2500\text{ppm}$  from the center frequency.

## Error and Fault Condition Monitoring

The MAX96722 includes an open-drain, multipurpose error reporting and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. Errors can be automatically forwarded across the link from the serializer, so certain serializer side errors, such as CSI-2 input CRC errors, can automatically be flagged by the MAX96722's LOCK output. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers, so the reason for assertion of ERRB can be determined by reading the register status.

## Line-Fault

GMSL2 devices include a novel line-fault detection circuit. It detects and reports open-circuit, short to battery, short to ground, and line-to-line short conditions on the GMSL interconnect. The line-fault monitor requires external resistors  $R_{EXT}$  and  $R_{PD}$  connected to the LMN pins as shown in [Figure 36](#) and [Figure 37](#). Note that these figures illustrate the connection scheme that is employed when the deserializer's line-fault detectors are used, which is typically the case in camera applications. The serializer's line fault detectors can alternatively be used, and in this case the LMN connections and placement of  $R_{EXT}$  and  $R_{PD}$  are reversed between the serializer and deserializer sides of the link. Whether serializer or deserializer line-fault detectors should be used depends on the architecture of a given system. In general, the device that is used to detect line-fault should have a clear communication channel to the primary system controller module that does not depend on the integrity of the GMSL link. In both cases, a  $49.9\text{k}\Omega$ , 1% tolerance resistor ( $R_{PD}$ ) is connected from each GMSL signal line to ground at the end of the link opposite the location of the line-fault detectors, while a  $42.2\text{k}\Omega$  (LMN0 with STP) or  $48.7\text{k}\Omega$  (LMN0 with coax, LMN1), 1% tolerance resistor ( $R_{EXT}$ ) is connected from each GMSL signal line to the relevant LMN\_ pin of the device whose line-fault detectors are utilized. Only the specified resistor values/tolerances should be used to ensure correct functionality. Note that  $R_{PD}$  and  $R_{EXT}$  are located on opposite sides of the link, so the line-fault detection must be considered in the design of both the serializer and deserializer portions of a system. Line-fault detection cannot be used in conjunction with power-over-cable (PoC), and it should not be used in applications in which there is a potential difference between the grounds at opposite ends of the link.

The MAX96722 provides four pairs of line-fault detection inputs. The LMN functions are available as part of the MFP pin array. The presence of a fault condition can be flagged using the ERRB output. The line-fault monitor pins offer flexible connection and programming. Each line-fault input can be assigned to either polarity of the link when in STP mode. In coax mode, a single line fault input is required, and in this case either of the available line-fault input functions within a given pair can be used. The unneeded line-fault function within each pair can be disabled, and the corresponding MFPs can be used for other functions in coax mode. In applications that do not require line-fault detection, line-fault inputs can

be disabled and the corresponding MFPs can be used for alternate functions as needed. When using line-fault detection with STP interconnects, it is important to correctly associate each pair of pins to enable full functionality (LMN0 + LMN1, LMN2 + LMN3, LMN4 + LMN5, and LMN6 + LMN7).

The presence of a fault can be reported by the ERRB MFP function as mentioned previously. A fault condition generates an interrupt that is forwarded across the link such that the ERRB output of the serializer will flag a line-fault detected by the deserializer and vice-versa. In addition, the LFLT\_INT bits flag the presence of a fault condition, enabling convenient register access. In the event of a fault, ERRB will be driven low while LFLT\_INT is written to a value of 1. Further details of a fault event are available in register fields LF\_0 to LF\_7 (depending on which line-fault inputs are being used in a given application).

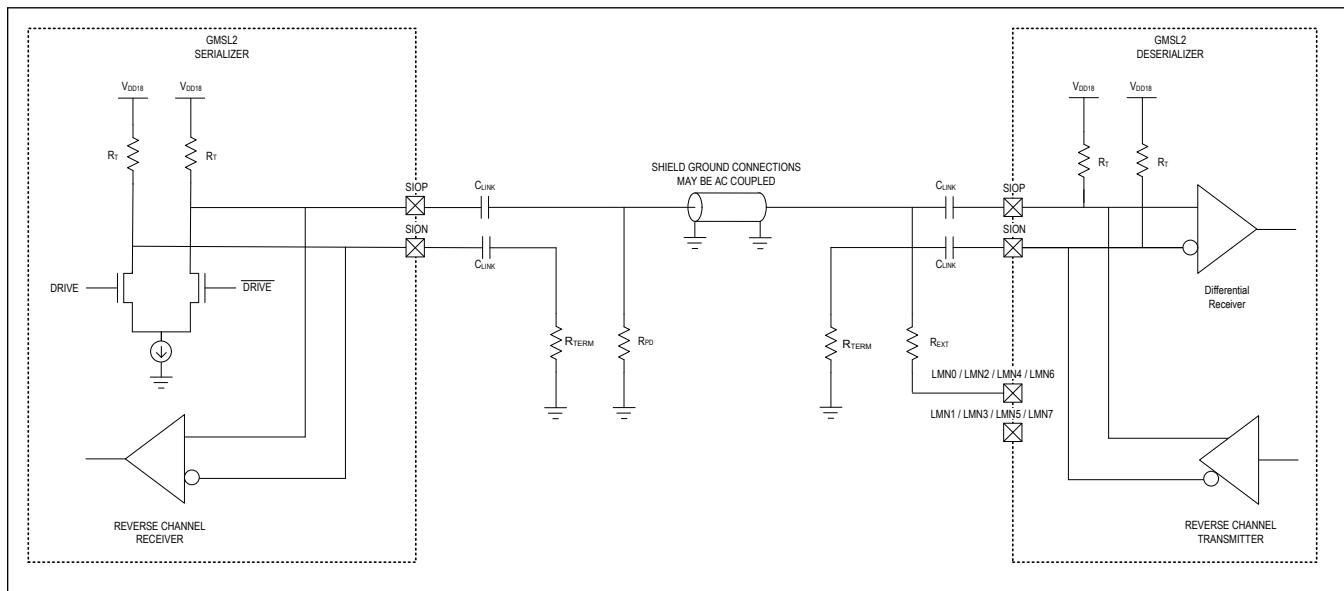


Figure 36. Typical GMSL1/2 Link Application Circuit for Coax Cable

**PRELIMINARY**

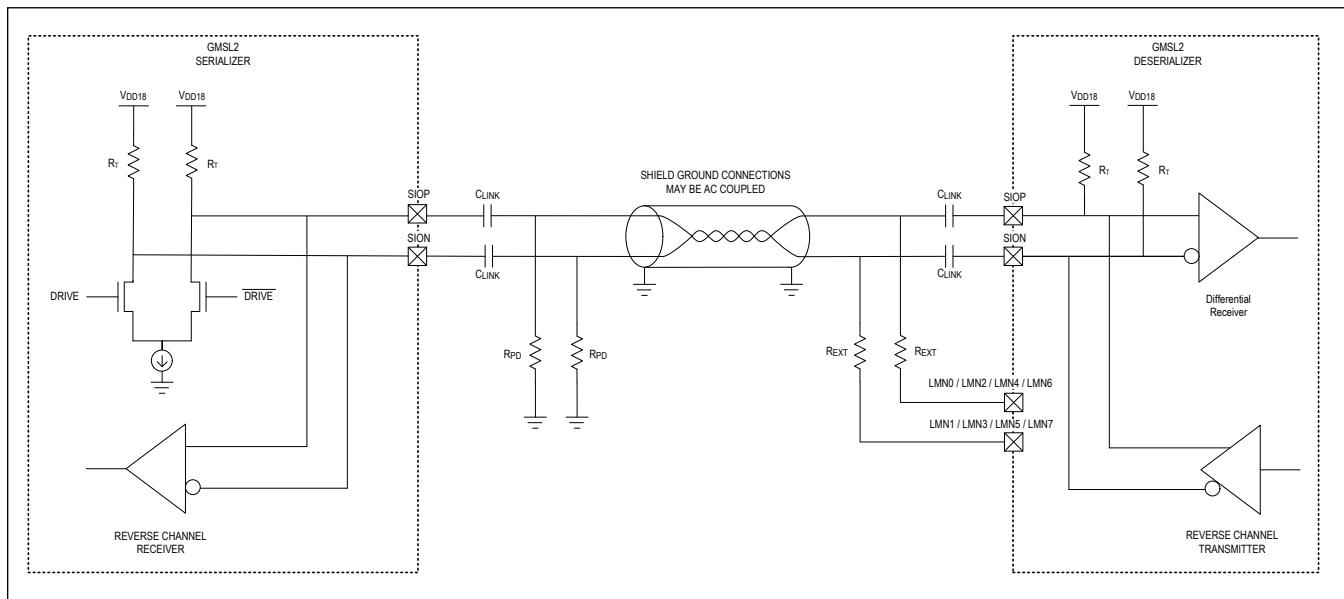


Figure 37. Typical GMSL1/2 Link Application Circuit for Twisted Pair

## Power Supplies

The MAX96722 provides flexible power supply configurations.

The 1V core supply can be provided directly or supplied by an internal regulator. To minimize power dissipation, connect  $1.0V \pm 5\%$  to  $V_{DD}$ . If  $V_{DD} < 1.1V$  and  $CAP\_VDD < 1.05V$ , the regulator is automatically disabled at power-up and low-resistance switches connect  $V_{DD}$  to the internal supply rails. If using the internal regulator, connect  $1.2V \pm 5\%$  to  $V_{DD}$  and write  $REG\_ENABLE = 1$  and  $REG\_MNL = 1$  in order following power-up as part of the device initialization to enable the internal LDO.

The  $V_{DDIO}$  supply for the I/O pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the MAX96722. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

$V_{DD18}$  is the primary analog supply. Connect  $1.8V \pm 5\%$ .

$V_{TERM}$  is the supply for the MIPI CSI C-PHY/D-PHY interface. Connect  $1.2V \pm 5\%$ .

Proper bypassing of all supplies is essential for optimal performance. In all cases, a decoupling capacitor should be placed as close as possible to each supply pin. See [Table 2](#) for guidance regarding appropriate decoupling for each supply pin. See [Table 1](#) for power supply tolerances and noise requirements. Contact factory for guidance on sharing supplies and optimizing supply decoupling.

## Power Supply Monitoring

Extensive power supply diagnostics capabilities are provided by the device. Undervoltage detection is included for all power supplies. Under voltage conditions on the  $V_{DD18}$ ,  $V_{DDIO}$ , and  $V_{TERM}$  supply voltages can be indicated via either the  $ERRB$  pin or by reading the register field associated with the power supply undervoltage flag. An undervoltage condition on the  $V_{DD}$  supply, which could corrupt the register configuration, is detected by the power manager and results in a reset. Similarly, severe undervoltage conditions on  $V_{DDIO}$  or  $V_{DD18}$  also result in a reset. In the case of a reset, device configuration reverts to the power-up default state when the supplies have recovered, and the host device must initiate the power-on initialization procedure to return the device to full operation.

Oversupply detection is also provided, although only for the internal  $V_{DD}$  supply voltage ( $CAP\_VDD$ ). As in the case of undervoltage events, an oversupply situation can be reported by the  $ERRB$  pin in addition to a dedicated internal interrupt flag. No further action is taken by the power manager during an oversupply situation, and the device will continue to operate normally, although it may sustain damage depending on the duration and magnitude of the oversupply event.

## Standby and Sleep Mode

The MAX96722 includes a power manager block. Its primary function is to monitor supply voltages and control low power standby and sleep modes.

There are two ways to enter low power mode while all power supplies are active. The first is to assert the  $PWDNB$  pin (active low). This places the device in standby mode and resets the registers and device configurations to their default power up state. If any supply drops below its internal threshold, the device will automatically enter standby mode regardless of the state of  $PWDNB$ .

The second way to enter low power mode is to invoke an I<sup>2</sup>C/UART command that puts the device into sleep mode. Putting the device in sleep mode preserves all critical register settings and configurations. The resume state restores the device back to the pre-sleep condition without the need for additional register writes. Resume is invoked by an I<sup>2</sup>C command or a low frequency clock beacon transmitted from the master device over the GMSL2 link.

## Thermal Management

Power consumption of the MAX96722 varies based on the use case. Care must be taken by the user to provide sufficient heat dissipation with proper board design and cooling techniques. The package's exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below 125°C to meet electrical specifications

and avoid impacting device reliability.

Refer to Tutorial 4083 ([www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial)) for further guidance.

**PRELIMINARY**

## Register Map

### Reserved and Unused Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write). In this document default values are provided for read-only register bits. Read-only bit states are changed at powerup according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

### Programming Notes

For specified performance, execute the following register writes during initialization:

- Set bits [2:0] = 3'b000 in registers 0x1445, 0x1545, 0x1645, 0x1745
- Set bits [7:0] = 0x03 in registers 0x14D1, 0x15D1, 0x16D1, 0x17D1
- Set bits [7:0] = 0x10 in register 0x6C2

ADDRESS	NAME	MSB							LSB
<b>DEV</b>									
0x00	<u>REG0[7:0]</u>								CFG_BL_OCK
0x01	<u>REG1[7:0]</u>		IIC_SEL[1:0]		DIS_LOC_CC[1:0]	IIC_SEL_P2	DIS_LO_C_CC_P2	ALT_IIC_SEL	FAILOVER
0x03	<u>REG3[7:0]</u>		DIS_Rem_CC_D[1:0]		DIS_Rem_CC_C[1:0]		DIS_Rem_CC_B[1:0]		DIS_Rem_CC_A[1:0]
0x04	<u>REG4[7:0]</u>	VID_EN_7	VID_EN_6	VID_EN_5	VID_EN_4	VID_EN_3	VID_EN_2	VID_EN_1	VID_EN_0
0x05	<u>REG5[7:0]</u>	LOCK_E_N	ERRB_E_N	LOCK_C_FG	-	-	-	-	-
0x06	<u>REG6[7:0]</u>	GMSL2_D	GMSL2_C	GMSL2_B	GMSL2_A	LINK_EN_D	LINK_EN_C	LINK_EN_B	LINK_EN_A
0x07	<u>REG7[7:0]</u>					CC_CROSSOVER_SEL[7:0]			
0x08	<u>DEBUG_EXTRA_1[7:0]</u>	PATGEN_SYNC	-	-	-	-	-	-	-
0x09	<u>DEBUG_EXTRA[7:0]</u>						DEBUG_EXTRA[7:0]		
0x0A	<u>CTRL12[7:0]</u>	-	-	-	-	LOCKED_B	-	-	-
0x0B	<u>CTRL13[7:0]</u>	-	-	-	-	LOCKED_C	-	-	-
0x0C	<u>CTRL14[7:0]</u>	-	-	-	-	LOCKED_D	-	-	-
0x0D	<u>REG13[7:0]</u>					DEV_ID[7:0]			
0x0E	<u>REG14[7:0]</u>	DIS_LO_CAL_WA KE_P2	-	AUTO_SLEEP_DIS	-		DIS_Rem_CC_P2[3:0]		
0x10	<u>REG26[7:0]</u>	TX_RATE_PHYB[1:0]	-	-	TX_RATE_PHYA[1:0]	-	-		

ADDRESS	NAME	MSB							LSB
0x11	<a href="#">REG27[7:0]</a>	TX_RATE_PHYD[1:0]	-	-	TX_RATE_PHYC[1:0]	-	-	-	
<b>TOP_CTRL</b>									
0x12	<a href="#">PWR0[7:0]</a>	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x13	<a href="#">PWR1[7:0]</a>	-	RESET_ALL	-	-	-	-	-	-
0x17	<a href="#">CTRL0[7:0]</a>	WAKE_E_N_D	WAKE_E_N_C	WAKE_E_N_B	WAKE_E_N_A	SLEEP	REG_EN_ABLE	DIS_LOCAL_WAKE[1:0]	
0x18	<a href="#">CTRL1[7:0]</a>	RESET_LINK_D	RESET_LINK_C	RESET_LINK_B	RESET_LINK_A	RESET_ONESHOT_D	RESET_ONESHOT_C	RESET_ONESHOT_B	RESET_ONESHOT_A
0x19	<a href="#">CTRL2[7:0]</a>	-	-	-	REG_MNL	-	-	-	-
0x1A	<a href="#">CTRL3[7:0]</a>	-	-	-	-	LOCKED	ERROR	CMU_LOCKED	-
0x22	<a href="#">CTRL11[7:0]</a>	-	CXTP_D	-	CXTP_C	-	CXTP_B	-	CXTP_A
0x23	<a href="#">INTR0[7:0]</a>	-	-	-	-	AUTO_E_RR_RST_EN	DEC_ERR_THR[2:0]		
0x24	<a href="#">INTR1[7:0]</a>	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x25	<a href="#">INTR2[7:0]</a>	-	-	-	-	DEC_ER_R_OEN_D	DEC_ER_R_OEN_C	DEC_ER_R_OEN_B	DEC_ER_R_OEN_A
0x26	<a href="#">INTR3[7:0]</a>	-	-	-	-	DEC_ER_R_FLAG_D	DEC_ER_R_FLAG_C	DEC_ER_R_FLAG_B	DEC_ER_R_FLAG_A
0x27	<a href="#">INTR4[7:0]</a>	EOM_E_RR_OEN_D	EOM_E_RR_OEN_C	EOM_E_RR_OEN_B	EOM_E_RR_OEN_A	RTTN_CRC_ERR_OEN	LFLT_IN_T_OEN	WM1_E_RR_OEN	WM_ER_R_OEN
0x28	<a href="#">INTR5[7:0]</a>	EOM_E_RR_FLA_G_D	EOM_E_RR_FLA_G_C	EOM_E_RR_FLA_G_B	EOM_E_RR_FLA_G_A	RTTN_CRC_INT	LFLT_IN_T	WM1_E_RR_FLA_G	WM_ER_R_FLAG
0x29	<a href="#">INTR6[7:0]</a>	G1_D_E_RR_OEN	G1_C_E_RR_OEN	G1_B_E_RR_OEN	G1_A_E_RR_OEN	LCRC_E_RR_OEN	VPRBS_ERR_OE_N	REM_ER_R_OEN	FSYNC_ERR_OE_N
0x2A	<a href="#">INTR7[7:0]</a>	G1_D_E_RR_FLA_G	G1_C_E_RR_FLA_G	G1_B_E_RR_FLA_G	G1_A_E_RR_FLA_G	LCRC_E_RR_FLA_G	VPRBS_ERR_FLAG	REM_ER_R_FLAG	FSYNC_ERR_FLAG
0x2B	<a href="#">INTR8[7:0]</a>	-	-	-	-	IDLE_ER_R_OEN_D	IDLE_ER_R_OEN_C	IDLE_ER_R_OEN_B	IDLE_ER_R_OEN_A
0x2C	<a href="#">INTR9[7:0]</a>	-	-	-	-	IDLE_ER_R_FLAG_D	IDLE_ER_R_FLAG_C	IDLE_ER_R_FLAG_B	IDLE_ER_R_FLAG_A
0x2D	<a href="#">INTR10[7:0]</a>	RT_CNT_OEN_D	RT_CNT_OEN_C	RT_CNT_OEN_B	RT_CNT_OEN_A	MAX_RT_OEN_D	MAX_RT_OEN_C	MAX_RT_OEN_B	MAX_RT_OEN_A

ADDRESS	NAME	MSB							LSB
0x2E	<u>INTR11[7:0]</u>	RT_CNT_FLAG_D	RT_CNT_FLAG_C	RT_CNT_FLAG_B	RT_CNT_FLAG_A	MAX_RT_FLAG_D	MAX_RT_FLAG_C	MAX_RT_FLAG_B	MAX_RT_FLAG_A
0x2F	<u>INTR12[7:0]</u>	ERR_TX_EN	MEM_E_RR_OEN	-		ERR_TX_ID[4:0]			
0x30	<u>INTR13[7:0]</u>	ERR_RX_EN_A	-	-		ERR_RX_ID_A[4:0]			
0x31	<u>INTR14[7:0]</u>	ERR_RX_EN_B	-	-		ERR_RX_ID_B[4:0]			
0x32	<u>INTR15[7:0]</u>	ERR_RX_EN_C	-	-		ERR_RX_ID_C[4:0]			
0x33	<u>INTR16[7:0]</u>	ERR_RX_EN_D	-	-		ERR_RX_ID_D[4:0]			
0x35	<u>CNT0[7:0]</u>				DEC_ERR_A[7:0]				
0x36	<u>CNT1[7:0]</u>				DEC_ERR_B[7:0]				
0x37	<u>CNT2[7:0]</u>				DEC_ERR_C[7:0]				
0x38	<u>CNT3[7:0]</u>				DEC_ERR_D[7:0]				
0x39	<u>CNT4[7:0]</u>				IDLE_ERR_A[7:0]				
0x3A	<u>CNT5[7:0]</u>				IDLE_ERR_B[7:0]				
0x3B	<u>CNT6[7:0]</u>				IDLE_ERR_C[7:0]				
0x3C	<u>CNT7[7:0]</u>				IDLE_ERR_D[7:0]				
0x40	<u>CNT8[7:0]</u>				PKT_CNT_A[7:0]				
0x41	<u>CNT9[7:0]</u>				PKT_CNT_B[7:0]				
0x42	<u>CNT10[7:0]</u>				PKT_CNT_C[7:0]				
0x43	<u>CNT11[7:0]</u>				PKT_CNT_D[7:0]				
0x44	<u>VID_PXL_CRC_ERR_OEN[7:0]</u>	MEM_E_CC_ERR_2_OEN	MEM_E_CC_ERR_1_OEN	-	-	VID_PXL_CRC_E_RR_OEN_D	VID_PXL_CRC_E_RR_OEN_C	VID_PXL_CRC_E_RR_OEN_B	VID_PXL_CRC_E_RR_OEN_A
0x45	<u>VID_PXL_CRC_ERR_INT[7:0]</u>	MEM_E_CC_ERR_2_INT	MEM_E_CC_ERR_1_INT	-	-	VID_PXL_CRC_E_RR_D	VID_PXL_CRC_E_RR_C	VID_PXL_CRC_E_RR_B	VID_PXL_CRC_E_RR_A
0x46	<u>PWR_STATUS_OEN[7:0]</u>	VDDCM_P_INT_OEN	-	VDDBAD_INT_OE_N	-	-	-	-	-
0x47	<u>PWR_STATUS_FLAG[7:0]</u>	VDDCM_P_INT_FLAG	-	VDDBAD_INT_FLAG	-	-	-	-	-
0x48	<u>PM_OV_STAT[7:0]</u>	-	-	-	-	-	-	OV_LEVEL[1:0]	
0x49	<u>VIDEO_MASKED_OEN[7:0]</u>	-	-	CMP_VT_ERM_MASK	VDD_OV_OEN	VIDEO_MASKED_3_OE_N	VIDEO_MASKED_2_OE_N	VIDEO_MASKED_1_OE_N	VIDEO_MASKED_0_OE_N
0x4A	<u>VIDEO_MASKED_FLAG[7:0]</u>	-	-	CMP_VT_ERM_STATUS	VDD_OV_FLAG	VIDEO_MASKED_3_FLAG	VIDEO_MASKED_2_FLAG	VIDEO_MASKED_1_FLAG	VIDEO_MASKED_0_FLAG

ADDRESS	NAME	MSB							LSB
0x4C	DEV_REV[7:0]	-	-	-	-	DEV_REV[3:0]			
<b>CFGH_A VIDEO_X</b>									
0x50	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL[1:0]
<b>CFGH_A VIDEO_Y</b>									
0x51	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL[1:0]
<b>CFGH_A VIDEO_Z</b>									
0x52	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL[1:0]
<b>CFGH_A VIDEO_U</b>									
0x53	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL[1:0]
<b>CFGH_B VIDEO_X</b>									
0x54	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_B[1:0]
<b>CFGH_B VIDEO_Y</b>									
0x55	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_B[1:0]
<b>CFGH_B VIDEO_Z</b>									
0x56	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_B[1:0]
<b>CFGH_B VIDEO_U</b>									
0x57	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_B[1:0]
<b>CFGH_C VIDEO_X</b>									
0x58	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_C[1:0]
<b>CFGH_C VIDEO_Y</b>									
0x59	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_C[1:0]
<b>CFGH_C VIDEO_Z</b>									
0x5A	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_C[1:0]
<b>CFGH_C VIDEO_U</b>									
0x5B	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_C[1:0]
<b>CFGH_D VIDEO_X</b>									
0x5C	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_D[1:0]
<b>CFGH_D VIDEO_Y</b>									
0x5D	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_D[1:0]
<b>CFGH_D VIDEO_Z</b>									
0x5E	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_D[1:0]
<b>CFGH_D VIDEO_U</b>									
0x5F	RX0[7:0]	-	-	-	-	-	-	-	STR_SEL_D[1:0]
<b>CFGH_VIDEO_CRC</b>									
0x60	CFGH_VIDEO_CRC0[7:0]	RX_CRC_EN_A_B[7:0]							
0x61	CFGH_VIDEO_CRC1[7:0]	RX_CRC_EN_C_D[7:0]							
<b>CFGI_A INFOFR</b>									
0x70	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	-	-	PRI0_VAL[1:0]	-	-	
0x71	TR1[7:0]	BW_MULT[1:0]				BW_VAL[5:0]			

ADDRESS	NAME	MSB							LSB		
0x72	TR2[7:0]	-	-	-	-	-	TX_SRC_ID[2:0]				
0x73	TR3[7:0]			RX_SRC_SEL[7:0]							
<b>CFG1_B INFOFR</b>											
0x74	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	-	-	PRI_O_VAL_B[1:0]	-	-			
0x75	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]							
0x76	TR2[7:0]	-	-	-	-	-	TX_SRC_ID_B[2:0]				
0x77	TR3[7:0]			RX_SRC_SEL_B[7:0]							
<b>CFG1_C INFOFR</b>											
0x78	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	-	-	PRI_O_VAL_C[1:0]	-	-			
0x79	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]							
0x7A	TR2[7:0]	-	-	-	-	-	TX_SRC_ID_C[2:0]				
0x7B	TR3[7:0]			RX_SRC_SEL_C[7:0]							
<b>CFG1_D INFOFR</b>											
0x7C	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	-	-	PRI_O_VAL_D[1:0]	-	-			
0x7D	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]							
0x7E	TR2[7:0]	-	-	-	-	-	TX_SRC_ID_D[2:0]				
0x7F	TR3[7:0]			RX_SRC_SEL_D[7:0]							
<b>CFG_S SPI_0</b>											
0x80	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	-	-	PRI_O_VAL[1:0]	PRI_O_CFG[1:0]				
0x81	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]							
0x83	TR3[7:0]	-	-	-	-	-	TX_SRC_ID[2:0]				
0x84	TR4[7:0]			RX_SRC_SEL[7:0]							
0x85	ARQ0[7:0]	-	-	-	ACK_SR_C_ID	ARQ_EN	ARQ_EN	-	-		
0x86	ARQ1[7:0]	-	MAX_RT[2:0]		-	-	MAX_RT_ERR_O_EN	RT_CNT_OEN			
0x87	ARQ2[7:0]	MAX_RT_ERR			RT_CNT[6:0]						
<b>CFG_S SPI_1</b>											
0x90	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	-	-	PRI_O_VAL[1:0]	-	-			
0x91	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]							
0x93	TR3[7:0]	-	-	-	-	-	TX_SRC_ID[2:0]				
0x94	TR4[7:0]			RX_SRC_SEL[7:0]							
0x95	ARQ0[7:0]	-	-	-	-	ARQ_EN	ARQ_EN	-	-		
0x96	ARQ1[7:0]	-	MAX_RT[2:0]		-	-	MAX_RT_ERR_O_EN	RT_CNT_OEN			

## MAX96722

Quad GMSL2 to CSI-2 Deserializer  
with GMSL1 Compatibility**PRELIMINARY**

ADDRESS	NAME	MSB							LSB
0x97	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR	RT_CNT[6:0]						
<b>CFG_L_A GPIO</b>									
0xA0	<a href="#">TR0[7:0]</a>	TX_CRC_EN	RX_CRC_EN	-	-	PRIO_VAL[1:0]	-	-	
0xA1	<a href="#">TR1[7:0]</a>	BW_MULT[1:0]						BW_VAL[5:0]	
0xA3	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID[2:0]		
0xA4	<a href="#">TR4[7:0]</a>	RX_SRC_SEL[7:0]							
0xA5	<a href="#">ARQ0[7:0]</a>	-	-	-	-	ARQ_EN	ARQ_EN	-	-
0xA6	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT_ERR_OEN	RT_CNT_OEN
0xA7	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR	RT_CNT[6:0]						
<b>CFG_L_B GPIO</b>									
0xA8	<a href="#">TR0[7:0]</a>	TX_CRC_EN_B	RX_CRC_EN_B	-	-	PRIO_VAL_B[1:0]	-	-	
0xA9	<a href="#">TR1[7:0]</a>	BW_MULT_B[1:0]						BW_VAL_B[5:0]	
0xAB	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID_B[2:0]		
0xAC	<a href="#">TR4[7:0]</a>	RX_SRC_SEL_B[7:0]							
0xAD	<a href="#">ARQ0[7:0]</a>	-	-	-	-	ARQ_EN_B	ARQ_EN	-	-
0xAE	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
0xAF	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR_B	RT_CNT_B[6:0]						
<b>CFG_L_C GPIO</b>									
0xB0	<a href="#">TR0[7:0]</a>	TX_CRC_EN_C	RX_CRC_EN_C	-	-	PRIO_VAL_C[1:0]	-	-	
0xB1	<a href="#">TR1[7:0]</a>	BW_MULT_C[1:0]						BW_VAL_C[5:0]	
0xB3	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID_C[2:0]		
0xB4	<a href="#">TR4[7:0]</a>	RX_SRC_SEL_C[7:0]							
0xB5	<a href="#">ARQ0[7:0]</a>	-	-	-	-	ARQ_EN_C	ARQ_EN	-	-
0xB6	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
0xB7	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR_C	RT_CNT_C[6:0]						
<b>CFG_L_D GPIO</b>									
0xB8	<a href="#">TR0[7:0]</a>	TX_CRC_EN_D	RX_CRC_EN_D	-	-	PRIO_VAL_D[1:0]	-	-	
0xB9	<a href="#">TR1[7:0]</a>	BW_MULT_D[1:0]						BW_VAL_D[5:0]	
0xBB	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID_D[2:0]		
0xBC	<a href="#">TR4[7:0]</a>	RX_SRC_SEL_D[7:0]							

ADDRESS	NAME	MSB							LSB				
0xBD	<u>ARQ0[7:0]</u>	-	-	-	-	ARQ_EN_D	ARQ_EN	-	-				
0xBE	<u>ARQ1[7:0]</u>	-	-	-	-	-	-	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D				
0xBF	<u>ARQ2[7:0]</u>	MAX_RT_ERR_D	RT_CNT_D[6:0]										
<b>CC</b>													
0xC7	<u>I2C_7[7:0]</u>	I2C_RE GSLV_1_TIMED_OUT	I2C_INTREG_SLV_1_TO[2:0]			I2C_RE GSLV_0_TIMED_OUT	I2C_INTREG_SLV_0_TO[2:0]						
0xC8	<u>UART_0[7:0]</u>	-	-	REM_MS_EN_0	LOC_MS_EN_0	BYPASS_DIS_PAR_0	BYPASS_TO_0[1:0]	BYPASS_EN_0					
0xC9	<u>UART_1[7:0]</u>	BITLEN_LSB_0[7:0]											
0xCA	<u>UART_2[7:0]</u>	OUT_DELAY_0[1:0]		BITLEN_MSB_0[5:0]									
0xCB	<u>UART_3[7:0]</u>	ARB_TO_LEN_1[1:0]	REM_MS_EN_1	LOC_MS_EN_1	BYPASS_DIS_PAR_1	BYPASS_TO_1[1:0]		BYPASS_EN_1					
0xCC	<u>UART_4[7:0]</u>	BITLEN_LSB_1[7:0]											
0xCD	<u>UART_5[7:0]</u>	OUT_DELAY_1[1:0]		BITLEN_MSB_1[5:0]									
0xCE	<u>UART_6[7:0]</u>	UART_2_LINK_SEL_ECT[1:0]	GMSL1_UART_A_RB_TO	GMSL1_UART_A_RB_EN	UART_1_LINK_SEL_ECT[1:0]	UART_0_LINK_SEL_ECT[1:0]							
0xD0	<u>UART_7[7:0]</u>	-	-	UART_2_RX_OV_ERFLOW_W	UART_2_RX_OV_ERFLOW_W	UART_1_RX_OV_ERFLOW_W	UART_1_RX_OV_ERFLOW_W	UART_0_RX_OV_ERFLOW_W	UART_0_RX_OV_ERFLOW_W				
0xD1	<u>UART_8[7:0]</u>	-	-	REM_MS_EN_2	LOC_MS_EN_2	BYPASS_DIS_PAR_2	BYPASS_TO_2[1:0]		BYPASS_EN_2				
0xD2	<u>UART_9[7:0]</u>	BITLEN_LSB_2[7:0]											
0xD3	<u>UART_10[7:0]</u>	OUT_DELAY_2[1:0]		BITLEN_MSB_2[5:0]									
0xD4	<u>I2C_8[7:0]</u>	-	-	-	-	I2C_RE GSLV_2_TIMED_OUT	I2C_INTREG_SLV_2_TO[2:0]						
<b>LINE_FAULT</b>													
0xE0	<u>REG0[7:0]</u>	PU_LF7	PU_LF6	PU_LF5	PU_LF4	PU_LF3	PU_LF2	PU_LF1	PU_LF0				
0xE1	<u>REG1[7:0]</u>	-	LF_1[2:0]		-	LF_0[2:0]							
0xE2	<u>REG2[7:0]</u>	-	LF_3[2:0]		-	LF_2[2:0]							
0xE3	<u>REG3[7:0]</u>	-	LF_5[2:0]		-	LF_4[2:0]							
0xE4	<u>REG4[7:0]</u>	-	LF_7[2:0]		-	LF_6[2:0]							
0xE5	<u>REG5[7:0]</u>	LFLT_INT_FLAG[7:0]											
0xE6	<u>REG6[7:0]</u>	MASK_L_F7	MASK_L_F6	MASK_L_F5	MASK_L_F4	MASK_L_F3	MASK_L_F2	MASK_L_F1	MASK_L_F0				

ADDRESS	NAME	MSB							LSB			
<b>VIDEO_PIPE_SEL</b>												
0xF0	<u>VIDEO_PIPE_SEL_0[7:0]</u>	VIDEO_PIPE_SEL_1[3:0]					VIDEO_PIPE_SEL_0[3:0]					
0xF1	<u>VIDEO_PIPE_SEL_1[7:0]</u>	VIDEO_PIPE_SEL_3[3:0]					VIDEO_PIPE_SEL_2[3:0]					
0xF2	<u>VIDEO_PIPE_SEL_2[7:0]</u>	VIDEO_PIPE_SEL_5[3:0]					VIDEO_PIPE_SEL_4[3:0]					
0xF3	<u>VIDEO_PIPE_SEL_3[7:0]</u>	VIDEO_PIPE_SEL_7[3:0]					VIDEO_PIPE_SEL_6[3:0]					
0xF4	<u>VIDEO_PIPE_EN[7:0]</u>	VIDEO_PIPE_EN[7:0]										
<b>HVD_GPIO_CTRL</b>												
0xFA	<u>HVD_GPIO_CTRL_0[7:0]</u>	-	DE_EN	HS_EN	VS_EN	-	HVD_SEL[2:0]					
<b>VID_RX 0</b>												
0x100	<u>VIDEO_RX0[7:0]</u>	LCRC_E RR	-	-	SEQ_MI SS_EN	-	-	LINE_C RC_EN	DIS_PKT _DET			
0x103	<u>VIDEO_RX3[7:0]</u>	-	HD_TR_ MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN			
0x106	<u>VIDEO_RX6[7:0]</u>	-	-	-	-	LIM_HE ART	-	-	-			
0x108	<u>VIDEO_RX8[7:0]</u>	VID_BLK _LEN_E RR	VID_LO CK	VID_PKT _DET	VID_SE Q_ERR	-	-	-	-			
0x10A	<u>VIDEO_RX10[7:0]</u>	-	MASK_V IDEO_D E	-	-	-	-	-	-			
<b>VID_RX 1</b>												
0x112	<u>VIDEO_RX0[7:0]</u>	LCRC_E RR	-	-	SEQ_MI SS_EN	-	-	LINE_C RC_EN	DIS_PKT _DET			
0x115	<u>VIDEO_RX3[7:0]</u>	-	HD_TR_ MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN			
0x118	<u>VIDEO_RX6[7:0]</u>	-	-	-	-	LIM_HE ART	-	-	-			
0x11A	<u>VIDEO_RX8[7:0]</u>	VID_BLK _LEN_E RR	VID_LO CK	VID_PKT _DET	VID_SE Q_ERR	-	-	-	-			
0x11C	<u>VIDEO_RX10[7:0]</u>	-	MASK_V IDEO_D E	-	-	-	-	-	-			
<b>VID_RX 2</b>												
0x124	<u>VIDEO_RX0[7:0]</u>	LCRC_E RR	-	-	SEQ_MI SS_EN	-	-	LINE_C RC_EN	DIS_PKT _DET			
0x127	<u>VIDEO_RX3[7:0]</u>	-	HD_TR_ MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN			
0x12A	<u>VIDEO_RX6[7:0]</u>	-	-	-	-	LIM_HE ART	-	-	-			

ADDRESS	NAME	MSB							LSB
0x12C	<u>VIDEO_RX8[7:0]</u>	VID_BLK_LEN_E RR	VID_LO CK	VID_PKT _DET	VID_SE Q_ERR	-	-	-	-
0x12E	<u>VIDEO_RX10[7:0]</u>	-	MASK_V IDEO_D E	-	-	-	-	-	-
<b>VID_RX 3</b>									
0x136	<u>VIDEO_RX0[7:0]</u>	LCRC_E RR	-	-	SEQ_MI SS_EN	-	-	LINE_C RC_EN	DIS_PKT _DET
0x139	<u>VIDEO_RX3[7:0]</u>	-	HD_TR_ MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN
0x13C	<u>VIDEO_RX6[7:0]</u>	-	-	-	-	LIM_HE ART	-	-	-
0x13E	<u>VIDEO_RX8[7:0]</u>	VID_BLK LEN_E RR	VID_LO CK	VID_PKT _DET	VID_SE Q_ERR	-	-	-	-
0x140	<u>VIDEO_RX10[7:0]</u>	-	MASK_V IDEO_D E	-	-	-	-	-	-
<b>VID_RX 4</b>									
0x148	<u>VIDEO_RX0[7:0]</u>	LCRC_E RR	-	-	SEQ_MI SS_EN	-	-	LINE_C RC_EN	DIS_PKT _DET
0x14B	<u>VIDEO_RX3[7:0]</u>	-	HD_TR_ MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN
0x14E	<u>VIDEO_RX6[7:0]</u>	-	-	-	-	LIM_HE ART	-	-	-
0x150	<u>VIDEO_RX8[7:0]</u>	VID_BLK LEN_E RR	VID_LO CK	VID_PKT _DET	VID_SE Q_ERR	-	-	-	-
0x152	<u>VIDEO_RX10[7:0]</u>	-	MASK_V IDEO_D E	-	-	-	-	-	-
<b>VID_RX 5</b>									
0x160	<u>VIDEO_RX0[7:0]</u>	LCRC_E RR	-	-	SEQ_MI SS_EN	-	-	LINE_C RC_EN	DIS_PKT _DET
0x163	<u>VIDEO_RX3[7:0]</u>	-	HD_TR_ MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN
0x166	<u>VIDEO_RX6[7:0]</u>	-	-	-	-	LIM_HE ART	-	-	-
0x168	<u>VIDEO_RX8[7:0]</u>	VID_BLK LEN_E RR	VID_LO CK	VID_PKT _DET	VID_SE Q_ERR	-	-	-	-
0x16A	<u>VIDEO_RX10[7:0]</u>	-	MASK_V IDEO_D E	-	-	-	-	-	-
<b>VID_RX 6</b>									
0x172	<u>VIDEO_RX0[7:0]</u>	LCRC_E RR	-	-	SEQ_MI SS_EN	-	-	LINE_C RC_EN	DIS_PKT _DET

ADDRESS	NAME	MSB							LSB
0x175	<u>VIDEO_RX3[7:0]</u>	-	HD_TR_MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN
0x178	<u>VIDEO_RX6[7:0]</u>	-	-	-	-	LIM_HE ART	-	-	-
0x17A	<u>VIDEO_RX8[7:0]</u>	VID_BLK_LEN_E RR	VID_LO CK	VID_PKT_DET	VID_SE Q_ERR	-	-	-	-
0x17C	<u>VIDEO_RX10[7:0]</u>	-	MASK_V IDEO_D E	-	-	-	-	-	-
<b>VID_RX 7</b>									
0x184	<u>VIDEO_RX0[7:0]</u>	LCRC_E RR	-	-	SEQ_MISSEN	-	-	LINE_CRC_EN	DIS_PKT_DET
0x187	<u>VIDEO_RX3[7:0]</u>	-	HD_TR_MODE	DLOCKE D	VLOCKE D	HLOCKE D	DTRACK EN	VTRACK EN	HTRACK EN
0x18A	<u>VIDEO_RX6[7:0]</u>	-	-	-	-	LIM_HE ART	-	-	-
0x18C	<u>VIDEO_RX8[7:0]</u>	VID_BLK_LEN_E RR	VID_LO CK	VID_PKT_DET	VID_SE Q_ERR	-	-	-	-
0x18E	<u>VIDEO_RX10[7:0]</u>	-	MASK_V IDEO_D E	-	-	-	-	-	-
<b>VRX_0 0</b>									
0x1C0	<u>CROSS_0[7:0]</u>	-	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x1C1	<u>CROSS_1[7:0]</u>	-	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x1C2	<u>CROSS_2[7:0]</u>	-	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x1C3	<u>CROSS_3[7:0]</u>	-	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x1C4	<u>CROSS_4[7:0]</u>	-	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x1C5	<u>CROSS_5[7:0]</u>	-	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x1C6	<u>CROSS_6[7:0]</u>	-	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x1C7	<u>CROSS_7[7:0]</u>	-	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x1C8	<u>CROSS_8[7:0]</u>	-	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x1C9	<u>CROSS_9[7:0]</u>	-	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x1CA	<u>CROSS_10[7:0]</u>	-	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x1CB	<u>CROSS_11[7:0]</u>	-	CROSS11_I	CROSS11_F	CROSS11[4:0]				

ADDRESS	NAME	MSB							LSB
0x1CC	CROSS_12[7:0]	-	CROSS1 2_I	CROSS1 2_F					CROSS12[4:0]
0x1CD	CROSS_13[7:0]	-	CROSS1 3_I	CROSS1 3_F					CROSS13[4:0]
0x1CE	CROSS_14[7:0]	-	CROSS1 4_I	CROSS1 4_F					CROSS14[4:0]
0x1CF	CROSS_15[7:0]	-	CROSS1 5_I	CROSS1 5_F					CROSS15[4:0]
0x1D0	CROSS_16[7:0]	-	CROSS1 6_I	CROSS1 6_F					CROSS16[4:0]
0x1D1	CROSS_17[7:0]	-	CROSS1 7_I	CROSS1 7_F					CROSS17[4:0]
0x1D2	CROSS_18[7:0]	-	CROSS1 8_I	CROSS1 8_F					CROSS18[4:0]
0x1D3	CROSS_19[7:0]	-	CROSS1 9_I	CROSS1 9_F					CROSS19[4:0]
0x1D4	CROSS_20[7:0]	-	CROSS2 0_I	CROSS2 0_F					CROSS20[4:0]
0x1D5	CROSS_21[7:0]	-	CROSS2 1_I	CROSS2 1_F					CROSS21[4:0]
0x1D6	CROSS_22[7:0]	-	CROSS2 2_I	CROSS2 2_F					CROSS22[4:0]
0x1D7	CROSS_23[7:0]	-	CROSS2 3_I	CROSS2 3_F					CROSS23[4:0]
0x1D8	CROSS_HS[7:0]	-	CROSS_HS_I	CROSS_HS_F					CROSS_HS[4:0]
0x1D9	CROSS_VS[7:0]	-	CROSS_VS_I	CROSS_VS_F					CROSS_VS[4:0]
0x1DA	CROSS_DE[7:0]	-	CROSS_DE_I	CROSS_DE_F					CROSS_DE[4:0]
0x1DB	PRBS_ERR[7:0]				VPRBS_ERR[7:0]				
0x1DC	VPRBS[7:0]	PATGEN _CLK_S RC	-	-	VPRBS2 4_GENC HK_EN	VPRBS7 _GENCH K_EN	VPRBS9 _GENCH K_EN	DIS_GLI TCH_FIL T	VIDEO_LOCK
0x1DD	CROSS_27[7:0]	ALT_CR OSSBAR	CROSS2 7_I	CROSS2 7_F					CROSS27[4:0]
0x1DE	CROSS_28[7:0]	-	CROSS2 8_I	CROSS2 8_F					CROSS28[4:0]
0x1DF	CROSS_29[7:0]	-	CROSS2 9_I	CROSS2 9_F					CROSS29[4:0]
<b>VRX_0 1</b>									
0x1E0	CROSS_0[7:0]	-	CROSS0 _I	CROSS0 _F					CROSS0[4:0]
0x1E1	CROSS_1[7:0]	-	CROSS1 _I	CROSS1 _F					CROSS1[4:0]
0x1E2	CROSS_2[7:0]	-	CROSS2 _I	CROSS2 _F					CROSS2[4:0]

ADDRESS	NAME	MSB						LSB
0x1E3	CROSS_3[7:0]	-	CROSS3_I	CROSS3_F				CROSS3[4:0]
0x1E4	CROSS_4[7:0]	-	CROSS4_I	CROSS4_F				CROSS4[4:0]
0x1E5	CROSS_5[7:0]	-	CROSS5_I	CROSS5_F				CROSS5[4:0]
0x1E6	CROSS_6[7:0]	-	CROSS6_I	CROSS6_F				CROSS6[4:0]
0x1E7	CROSS_7[7:0]	-	CROSS7_I	CROSS7_F				CROSS7[4:0]
0x1E8	CROSS_8[7:0]	-	CROSS8_I	CROSS8_F				CROSS8[4:0]
0x1E9	CROSS_9[7:0]	-	CROSS9_I	CROSS9_F				CROSS9[4:0]
0x1EA	CROSS_10[7:0]	-	CROSS10_I	CROSS10_F				CROSS10[4:0]
0x1EB	CROSS_11[7:0]	-	CROSS11_I	CROSS11_F				CROSS11[4:0]
0x1EC	CROSS_12[7:0]	-	CROSS12_I	CROSS12_F				CROSS12[4:0]
0x1ED	CROSS_13[7:0]	-	CROSS13_I	CROSS13_F				CROSS13[4:0]
0x1EE	CROSS_14[7:0]	-	CROSS14_I	CROSS14_F				CROSS14[4:0]
0x1EF	CROSS_15[7:0]	-	CROSS15_I	CROSS15_F				CROSS15[4:0]
0x1F0	CROSS_16[7:0]	-	CROSS16_I	CROSS16_F				CROSS16[4:0]
0x1F1	CROSS_17[7:0]	-	CROSS17_I	CROSS17_F				CROSS17[4:0]
0x1F2	CROSS_18[7:0]	-	CROSS18_I	CROSS18_F				CROSS18[4:0]
0x1F3	CROSS_19[7:0]	-	CROSS19_I	CROSS19_F				CROSS19[4:0]
0x1F4	CROSS_20[7:0]	-	CROSS20_I	CROSS20_F				CROSS20[4:0]
0x1F5	CROSS_21[7:0]	-	CROSS21_I	CROSS21_F				CROSS21[4:0]
0x1F6	CROSS_22[7:0]	-	CROSS22_I	CROSS22_F				CROSS22[4:0]
0x1F7	CROSS_23[7:0]	-	CROSS23_I	CROSS23_F				CROSS23[4:0]
0x1F8	CROSS_HS[7:0]	-	CROSS_HS_I	CROSS_HS_F				CROSS_HS[4:0]
0x1F9	CROSS_VS[7:0]	-	CROSS_VS_I	CROSS_VS_F				CROSS_VS[4:0]
0x1FA	CROSS_DE[7:0]	-	CROSS_DE_I	CROSS_DE_F				CROSS_DE[4:0]

ADDRESS	NAME	MSB							LSB
0x1FB	<u>PRBS_ERR[7:0]</u>								VPRBS_ERR[7:0]
0x1FC	<u>VPRBS[7:0]</u>	PATGEN_CLK_SRC	-	-	VPRBS24_GENC_HK_EN	VPRBS7_GENCH_K_EN	VPRBS9_GENCH_K_EN	DIS_GLI_TCH_FILT	VIDEO_LOCK
0x1FD	<u>CROSS_27[7:0]</u>	ALT_CR_OSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x1FE	<u>CROSS_28[7:0]</u>	-	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x1FF	<u>CROSS_29[7:0]</u>	-	CROSS29_I	CROSS29_F	CROSS29[4:0]				
<b>VRX_0 2</b>									
0x200	<u>CROSS_0[7:0]</u>	-	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x201	<u>CROSS_1[7:0]</u>	-	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x202	<u>CROSS_2[7:0]</u>	-	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x203	<u>CROSS_3[7:0]</u>	-	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x204	<u>CROSS_4[7:0]</u>	-	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x205	<u>CROSS_5[7:0]</u>	-	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x206	<u>CROSS_6[7:0]</u>	-	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x207	<u>CROSS_7[7:0]</u>	-	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x208	<u>CROSS_8[7:0]</u>	-	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x209	<u>CROSS_9[7:0]</u>	-	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x20A	<u>CROSS_10[7:0]</u>	-	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x20B	<u>CROSS_11[7:0]</u>	-	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x20C	<u>CROSS_12[7:0]</u>	-	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x20D	<u>CROSS_13[7:0]</u>	-	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x20E	<u>CROSS_14[7:0]</u>	-	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x20F	<u>CROSS_15[7:0]</u>	-	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x210	<u>CROSS_16[7:0]</u>	-	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x211	<u>CROSS_17[7:0]</u>	-	CROSS17_I	CROSS17_F	CROSS17[4:0]				

ADDRESS	NAME	MSB							LSB
0x212	CROSS_18[7:0]	-	CROSS1 8_I	CROSS1 8_F	CROSS18[4:0]				
0x213	CROSS_19[7:0]	-	CROSS1 9_I	CROSS1 9_F	CROSS19[4:0]				
0x214	CROSS_20[7:0]	-	CROSS2 0_I	CROSS2 0_F	CROSS20[4:0]				
0x215	CROSS_21[7:0]	-	CROSS2 1_I	CROSS2 1_F	CROSS21[4:0]				
0x216	CROSS_22[7:0]	-	CROSS2 2_I	CROSS2 2_F	CROSS22[4:0]				
0x217	CROSS_23[7:0]	-	CROSS2 3_I	CROSS2 3_F	CROSS23[4:0]				
0x218	CROSS_HS[7:0]	-	CROSS_ HS_I	CROSS_ HS_F	CROSS_HS[4:0]				
0x219	CROSS_VS[7:0]	-	CROSS_ VS_I	CROSS_ VS_F	CROSS_VS[4:0]				
0x21A	CROSS_DE[7:0]	-	CROSS_ DE_I	CROSS_ DE_F	CROSS_DE[4:0]				
0x21B	PRBS_ERR[7:0]				VPRBS_ERR[7:0]				
0x21C	VPRBS[7:0]	PATGEN _CLK_S RC	-	-	VPRBS2 4_GENC HK_EN	VPRBS7 _GENCH K_EN	VPRBS9 _GENCH K_EN	DIS_GLI TCH_FIL T	VIDEO_LOCK
0x21D	CROSS_27[7:0]	ALT_CR OSSBAR	CROSS2 7_I	CROSS2 7_F	CROSS27[4:0]				
0x21E	CROSS_28[7:0]	-	CROSS2 8_I	CROSS2 8_F	CROSS28[4:0]				
0x21F	CROSS_29[7:0]	-	CROSS2 9_I	CROSS2 9_F	CROSS29[4:0]				
<b>VRX_0 3</b>									
0x220	CROSS_0[7:0]	-	CROSS0 _I	CROSS0 _F	CROSS0[4:0]				
0x221	CROSS_1[7:0]	-	CROSS1 _I	CROSS1 _F	CROSS1[4:0]				
0x222	CROSS_2[7:0]	-	CROSS2 _I	CROSS2 _F	CROSS2[4:0]				
0x223	CROSS_3[7:0]	-	CROSS3 _I	CROSS3 _F	CROSS3[4:0]				
0x224	CROSS_4[7:0]	-	CROSS4 _I	CROSS4 _F	CROSS4[4:0]				
0x225	CROSS_5[7:0]	-	CROSS5 _I	CROSS5 _F	CROSS5[4:0]				
0x226	CROSS_6[7:0]	-	CROSS6 _I	CROSS6 _F	CROSS6[4:0]				
0x227	CROSS_7[7:0]	-	CROSS7 _I	CROSS7 _F	CROSS7[4:0]				
0x228	CROSS_8[7:0]	-	CROSS8 _I	CROSS8 _F	CROSS8[4:0]				

ADDRESS	NAME	MSB							LSB
0x229	CROSS_9[7:0]	-	CROSS9_I	CROSS9_F					CROSS9[4:0]
0x22A	CROSS_10[7:0]	-	CROSS10_I	CROSS10_F					CROSS10[4:0]
0x22B	CROSS_11[7:0]	-	CROSS11_I	CROSS11_F					CROSS11[4:0]
0x22C	CROSS_12[7:0]	-	CROSS12_I	CROSS12_F					CROSS12[4:0]
0x22D	CROSS_13[7:0]	-	CROSS13_I	CROSS13_F					CROSS13[4:0]
0x22E	CROSS_14[7:0]	-	CROSS14_I	CROSS14_F					CROSS14[4:0]
0x22F	CROSS_15[7:0]	-	CROSS15_I	CROSS15_F					CROSS15[4:0]
0x230	CROSS_16[7:0]	-	CROSS16_I	CROSS16_F					CROSS16[4:0]
0x231	CROSS_17[7:0]	-	CROSS17_I	CROSS17_F					CROSS17[4:0]
0x232	CROSS_18[7:0]	-	CROSS18_I	CROSS18_F					CROSS18[4:0]
0x233	CROSS_19[7:0]	-	CROSS19_I	CROSS19_F					CROSS19[4:0]
0x234	CROSS_20[7:0]	-	CROSS20_I	CROSS20_F					CROSS20[4:0]
0x235	CROSS_21[7:0]	-	CROSS21_I	CROSS21_F					CROSS21[4:0]
0x236	CROSS_22[7:0]	-	CROSS22_I	CROSS22_F					CROSS22[4:0]
0x237	CROSS_23[7:0]	-	CROSS23_I	CROSS23_F					CROSS23[4:0]
0x238	CROSS_HS[7:0]	-	CROSS_HS_I	CROSS_HS_F					CROSS_HS[4:0]
0x239	CROSS_VS[7:0]	-	CROSS_VS_I	CROSS_VS_F					CROSS_VS[4:0]
0x23A	CROSS_DE[7:0]	-	CROSS_DE_I	CROSS_DE_F					CROSS_DE[4:0]
0x23B	PRBS_ERR[7:0]				VPRBS_ERR[7:0]				
0x23C	VPRBS[7:0]	PATGEN_CLK_SRC	-	-	VPRBS24_GENC_HK_EN	VPRBS7_GENCH_K_EN	VPRBS9_GENCH_K_EN	DIS_GLI_TCH_FILT	VIDEO_LOCK
0x23D	CROSS_27[7:0]	ALT_CR_OSSBAR	CROSS27_I	CROSS27_F					CROSS27[4:0]
0x23E	CROSS_28[7:0]	-	CROSS28_I	CROSS28_F					CROSS28[4:0]
0x23F	CROSS_29[7:0]	-	CROSS29_I	CROSS29_F					CROSS29[4:0]

ADDRESS	NAME	MSB						LSB
<b>VRX_0 4</b>								
0x240	CROSS_0[7:0]	-	CROSS0 _I	CROSS0 _F				CROSS0[4:0]
0x241	CROSS_1[7:0]	-	CROSS1 _I	CROSS1 _F				CROSS1[4:0]
0x242	CROSS_2[7:0]	-	CROSS2 _I	CROSS2 _F				CROSS2[4:0]
0x243	CROSS_3[7:0]	-	CROSS3 _I	CROSS3 _F				CROSS3[4:0]
0x244	CROSS_4[7:0]	-	CROSS4 _I	CROSS4 _F				CROSS4[4:0]
0x245	CROSS_5[7:0]	-	CROSS5 _I	CROSS5 _F				CROSS5[4:0]
0x246	CROSS_6[7:0]	-	CROSS6 _I	CROSS6 _F				CROSS6[4:0]
0x247	CROSS_7[7:0]	-	CROSS7 _I	CROSS7 _F				CROSS7[4:0]
0x248	CROSS_8[7:0]	-	CROSS8 _I	CROSS8 _F				CROSS8[4:0]
0x249	CROSS_9[7:0]	-	CROSS9 _I	CROSS9 _F				CROSS9[4:0]
0x24A	CROSS_10[7:0]	-	CROSS10 _I	CROSS10 _F				CROSS10[4:0]
0x24B	CROSS_11[7:0]	-	CROSS11 _I	CROSS11 _F				CROSS11[4:0]
0x24C	CROSS_12[7:0]	-	CROSS12 _I	CROSS12 _F				CROSS12[4:0]
0x24D	CROSS_13[7:0]	-	CROSS13 _I	CROSS13 _F				CROSS13[4:0]
0x24E	CROSS_14[7:0]	-	CROSS14 _I	CROSS14 _F				CROSS14[4:0]
0x24F	CROSS_15[7:0]	-	CROSS15 _I	CROSS15 _F				CROSS15[4:0]
0x250	CROSS_16[7:0]	-	CROSS16 _I	CROSS16 _F				CROSS16[4:0]
0x251	CROSS_17[7:0]	-	CROSS17 _I	CROSS17 _F				CROSS17[4:0]
0x252	CROSS_18[7:0]	-	CROSS18 _I	CROSS18 _F				CROSS18[4:0]
0x253	CROSS_19[7:0]	-	CROSS19 _I	CROSS19 _F				CROSS19[4:0]
0x254	CROSS_20[7:0]	-	CROSS20 _I	CROSS20 _F				CROSS20[4:0]
0x255	CROSS_21[7:0]	-	CROSS21 _I	CROSS21 _F				CROSS21[4:0]
0x256	CROSS_22[7:0]	-	CROSS22 _I	CROSS22 _F				CROSS22[4:0]

ADDRESS	NAME	MSB							LSB
0x257	CROSS_23[7:0]	-	CROSS2 3_I	CROSS2 3_F	CROSS23[4:0]				
0x258	CROSS_HS[7:0]	-	CROSS_ HS_I	CROSS_ HS_F	CROSS_HS[4:0]				
0x259	CROSS_VS[7:0]	-	CROSS_ VS_I	CROSS_ VS_F	CROSS_VS[4:0]				
0x25A	CROSS_DE[7:0]	-	CROSS_ DE_I	CROSS_ DE_F	CROSS_DE[4:0]				
0x25B	PRBS_ERR[7:0]				VPRBS_ERR[7:0]				
0x25C	VPRBS[7:0]	PATGEN _CLK_S RC	-	-	VPRBS2 4_GENC HK_EN	VPRBS7 _GENCH K_EN	VPRBS9 _GENCH K_EN	DIS_GLI TCH_FIL T	VIDEO_LOCK
0x25D	CROSS_27[7:0]	ALT_CR OSSBAR	CROSS2 7_I	CROSS2 7_F	CROSS27[4:0]				
0x25E	CROSS_28[7:0]	-	CROSS2 8_I	CROSS2 8_F	CROSS28[4:0]				
0x25F	CROSS_29[7:0]	-	CROSS2 9_I	CROSS2 9_F	CROSS29[4:0]				
<b>VRX_0 5</b>									
0x260	CROSS_0[7:0]	-	CROSS0 _I	CROSS0 _F	CROSS0[4:0]				
0x261	CROSS_1[7:0]	-	CROSS1 _I	CROSS1 _F	CROSS1[4:0]				
0x262	CROSS_2[7:0]	-	CROSS2 _I	CROSS2 _F	CROSS2[4:0]				
0x263	CROSS_3[7:0]	-	CROSS3 _I	CROSS3 _F	CROSS3[4:0]				
0x264	CROSS_4[7:0]	-	CROSS4 _I	CROSS4 _F	CROSS4[4:0]				
0x265	CROSS_5[7:0]	-	CROSS5 _I	CROSS5 _F	CROSS5[4:0]				
0x266	CROSS_6[7:0]	-	CROSS6 _I	CROSS6 _F	CROSS6[4:0]				
0x267	CROSS_7[7:0]	-	CROSS7 _I	CROSS7 _F	CROSS7[4:0]				
0x268	CROSS_8[7:0]	-	CROSS8 _I	CROSS8 _F	CROSS8[4:0]				
0x269	CROSS_9[7:0]	-	CROSS9 _I	CROSS9 _F	CROSS9[4:0]				
0x26A	CROSS_10[7:0]	-	CROSS1 0_I	CROSS1 0_F	CROSS10[4:0]				
0x26B	CROSS_11[7:0]	-	CROSS1 1_I	CROSS1 1_F	CROSS11[4:0]				
0x26C	CROSS_12[7:0]	-	CROSS1 2_I	CROSS1 2_F	CROSS12[4:0]				
0x26D	CROSS_13[7:0]	-	CROSS1 3_I	CROSS1 3_F	CROSS13[4:0]				

ADDRESS	NAME	MSB							LSB
0x26E	CROSS_14[7:0]	-	CROSS1_4_I	CROSS1_4_F	CROSS14[4:0]				
0x26F	CROSS_15[7:0]	-	CROSS1_5_I	CROSS1_5_F	CROSS15[4:0]				
0x270	CROSS_16[7:0]	-	CROSS1_6_I	CROSS1_6_F	CROSS16[4:0]				
0x271	CROSS_17[7:0]	-	CROSS1_7_I	CROSS1_7_F	CROSS17[4:0]				
0x272	CROSS_18[7:0]	-	CROSS1_8_I	CROSS1_8_F	CROSS18[4:0]				
0x273	CROSS_19[7:0]	-	CROSS1_9_I	CROSS1_9_F	CROSS19[4:0]				
0x274	CROSS_20[7:0]	-	CROSS2_0_I	CROSS2_0_F	CROSS20[4:0]				
0x275	CROSS_21[7:0]	-	CROSS2_1_I	CROSS2_1_F	CROSS21[4:0]				
0x276	CROSS_22[7:0]	-	CROSS2_2_I	CROSS2_2_F	CROSS22[4:0]				
0x277	CROSS_23[7:0]	-	CROSS2_3_I	CROSS2_3_F	CROSS23[4:0]				
0x278	CROSS_HS[7:0]	-	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x279	CROSS_VS[7:0]	-	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x27A	CROSS_DE[7:0]	-	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x27B	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x27C	VPRBS[7:0]	PATGEN_CLK_SRC	-	-	VPRBS2_4_GENC_HK_EN	VPRBS7_GENCH_K_EN	VPRBS9_GENCH_K_EN	DIS_GLITCH_TCH_FILT	VIDEO_LOCK
0x27D	CROSS_27[7:0]	ALT_CR_OSSBAR	CROSS2_7_I	CROSS2_7_F	CROSS27[4:0]				
0x27E	CROSS_28[7:0]	-	CROSS2_8_I	CROSS2_8_F	CROSS28[4:0]				
0x27F	CROSS_29[7:0]	-	CROSS2_9_I	CROSS2_9_F	CROSS29[4:0]				
<b>VRX_0 6</b>									
0x280	CROSS_0[7:0]	-	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x281	CROSS_1[7:0]	-	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x282	CROSS_2[7:0]	-	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x283	CROSS_3[7:0]	-	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x284	CROSS_4[7:0]	-	CROSS4_I	CROSS4_F	CROSS4[4:0]				

ADDRESS	NAME	MSB							LSB
0x285	CROSS_5[7:0]	-	CROSS5_I	CROSS5_F					CROSS5[4:0]
0x286	CROSS_6[7:0]	-	CROSS6_I	CROSS6_F					CROSS6[4:0]
0x287	CROSS_7[7:0]	-	CROSS7_I	CROSS7_F					CROSS7[4:0]
0x288	CROSS_8[7:0]	-	CROSS8_I	CROSS8_F					CROSS8[4:0]
0x289	CROSS_9[7:0]	-	CROSS9_I	CROSS9_F					CROSS9[4:0]
0x28A	CROSS_10[7:0]	-	CROSS10_I	CROSS10_F					CROSS10[4:0]
0x28B	CROSS_11[7:0]	-	CROSS11_I	CROSS11_F					CROSS11[4:0]
0x28C	CROSS_12[7:0]	-	CROSS12_I	CROSS12_F					CROSS12[4:0]
0x28D	CROSS_13[7:0]	-	CROSS13_I	CROSS13_F					CROSS13[4:0]
0x28E	CROSS_14[7:0]	-	CROSS14_I	CROSS14_F					CROSS14[4:0]
0x28F	CROSS_15[7:0]	-	CROSS15_I	CROSS15_F					CROSS15[4:0]
0x290	CROSS_16[7:0]	-	CROSS16_I	CROSS16_F					CROSS16[4:0]
0x291	CROSS_17[7:0]	-	CROSS17_I	CROSS17_F					CROSS17[4:0]
0x292	CROSS_18[7:0]	-	CROSS18_I	CROSS18_F					CROSS18[4:0]
0x293	CROSS_19[7:0]	-	CROSS19_I	CROSS19_F					CROSS19[4:0]
0x294	CROSS_20[7:0]	-	CROSS20_I	CROSS20_F					CROSS20[4:0]
0x295	CROSS_21[7:0]	-	CROSS21_I	CROSS21_F					CROSS21[4:0]
0x296	CROSS_22[7:0]	-	CROSS22_I	CROSS22_F					CROSS22[4:0]
0x297	CROSS_23[7:0]	-	CROSS23_I	CROSS23_F					CROSS23[4:0]
0x298	CROSS_HS[7:0]	-	CROSS_HS_I	CROSS_HS_F					CROSS_HS[4:0]
0x299	CROSS_VS[7:0]	-	CROSS_VS_I	CROSS_VS_F					CROSS_VS[4:0]
0x29A	CROSS_DE[7:0]	-	CROSS_DE_I	CROSS_DE_F					CROSS_DE[4:0]
0x29B	PRBS_ERR[7:0]				VPRBS_ERR[7:0]				
0x29C	VPRBS[7:0]	PATGEN_CLK_SRC	-	-	VPRBS24_GENC_HK_EN	VPRBS7_GENCH_K_EN	VPRBS9_GENCH_K_EN	DIS_GLI_TCH_FIL_T	VIDEO_LOCK

ADDRESS	NAME	MSB						LSB
0x29D	<u>CROSS_27[7:0]</u>	ALT_CR OSSBAR	CROSS2 7_I	CROSS2 7_F				CROSS27[4:0]
0x29E	<u>CROSS_28[7:0]</u>	-	CROSS2 8_I	CROSS2 8_F				CROSS28[4:0]
0x29F	<u>CROSS_29[7:0]</u>	-	CROSS2 9_I	CROSS2 9_F				CROSS29[4:0]
<b>VRX_0 7</b>								
0x2A0	<u>CROSS_0[7:0]</u>	-	CROSS0 _I	CROSS0 _F				CROSS0[4:0]
0x2A1	<u>CROSS_1[7:0]</u>	-	CROSS1 _I	CROSS1 _F				CROSS1[4:0]
0x2A2	<u>CROSS_2[7:0]</u>	-	CROSS2 _I	CROSS2 _F				CROSS2[4:0]
0x2A3	<u>CROSS_3[7:0]</u>	-	CROSS3 _I	CROSS3 _F				CROSS3[4:0]
0x2A4	<u>CROSS_4[7:0]</u>	-	CROSS4 _I	CROSS4 _F				CROSS4[4:0]
0x2A5	<u>CROSS_5[7:0]</u>	-	CROSS5 _I	CROSS5 _F				CROSS5[4:0]
0x2A6	<u>CROSS_6[7:0]</u>	-	CROSS6 _I	CROSS6 _F				CROSS6[4:0]
0x2A7	<u>CROSS_7[7:0]</u>	-	CROSS7 _I	CROSS7 _F				CROSS7[4:0]
0x2A8	<u>CROSS_8[7:0]</u>	-	CROSS8 _I	CROSS8 _F				CROSS8[4:0]
0x2A9	<u>CROSS_9[7:0]</u>	-	CROSS9 _I	CROSS9 _F				CROSS9[4:0]
0x2AA	<u>CROSS_10[7:0]</u>	-	CROSS1 0_I	CROSS1 0_F				CROSS10[4:0]
0x2AB	<u>CROSS_11[7:0]</u>	-	CROSS1 1_I	CROSS1 1_F				CROSS11[4:0]
0x2AC	<u>CROSS_12[7:0]</u>	-	CROSS1 2_I	CROSS1 2_F				CROSS12[4:0]
0x2AD	<u>CROSS_13[7:0]</u>	-	CROSS1 3_I	CROSS1 3_F				CROSS13[4:0]
0x2AE	<u>CROSS_14[7:0]</u>	-	CROSS1 4_I	CROSS1 4_F				CROSS14[4:0]
0x2AF	<u>CROSS_15[7:0]</u>	-	CROSS1 5_I	CROSS1 5_F				CROSS15[4:0]
0x2B0	<u>CROSS_16[7:0]</u>	-	CROSS1 6_I	CROSS1 6_F				CROSS16[4:0]
0x2B1	<u>CROSS_17[7:0]</u>	-	CROSS1 7_I	CROSS1 7_F				CROSS17[4:0]
0x2B2	<u>CROSS_18[7:0]</u>	-	CROSS1 8_I	CROSS1 8_F				CROSS18[4:0]
0x2B3	<u>CROSS_19[7:0]</u>	-	CROSS1 9_I	CROSS1 9_F				CROSS19[4:0]

ADDRESS	NAME	MSB							LSB
0x2B4	CROSS_20[7:0]	-	CROSS2_0_I	CROSS2_0_F	CROSS20[4:0]				
0x2B5	CROSS_21[7:0]	-	CROSS2_1_I	CROSS2_1_F	CROSS21[4:0]				
0x2B6	CROSS_22[7:0]	-	CROSS2_2_I	CROSS2_2_F	CROSS22[4:0]				
0x2B7	CROSS_23[7:0]	-	CROSS2_3_I	CROSS2_3_F	CROSS23[4:0]				
0x2B8	CROSS_HS[7:0]	-	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x2B9	CROSS_VS[7:0]	-	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x2BA	CROSS_DE[7:0]	-	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x2BB	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x2BC	VPRBS[7:0]	PATGEN_CLK_SRC	-	-	VPRBS2_4_GENC_HK_EN	VPRBS7_GENCH_K_EN	VPRBS9_GENCH_K_EN	DIS_GLI_TCH_FILT	VIDEO_LOCK
0x2BD	CROSS_27[7:0]	ALT_CR_OSSBAR	CROSS2_7_I	CROSS2_7_F	CROSS27[4:0]				
0x2BE	CROSS_28[7:0]	-	CROSS2_8_I	CROSS2_8_F	CROSS28[4:0]				
0x2BF	CROSS_29[7:0]	-	CROSS2_9_I	CROSS2_9_F	CROSS29[4:0]				
<b>GPIO0 0</b>									
0x300	GPIO_A[7:0]	RES_CFG	-	TX_COMM_P_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x301	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
0x302	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO1 1</b>									
0x303	GPIO_A[7:0]	RES_CFG	-	TX_COMM_P_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x304	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
0x305	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO2 2</b>									
0x306	GPIO_A[7:0]	RES_CFG	-	TX_COMM_P_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x307	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
0x308	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				

ADDRESS	NAME	MSB							LSB
<b>GPIO3 3</b>									
0x309	<a href="#">GPIO_A[7:0]</a>	RES_CF G	-	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x30A	<a href="#">GPIO_B[7:0]</a>	PULL_UPDN_SEL[1: 0]	OUT_TY PE						GPIO_TX_ID[4:0]
0x30B	<a href="#">GPIO_C[7:0]</a>	OVR_RE S_CFG	-	-					GPIO_RX_ID[4:0]
<b>GPIO4 4</b>									
0x30C	<a href="#">GPIO_A[7:0]</a>	RES_CF G	-	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x30D	<a href="#">GPIO_B[7:0]</a>	PULL_UPDN_SEL[1: 0]	OUT_TY PE						GPIO_TX_ID[4:0]
0x30E	<a href="#">GPIO_C[7:0]</a>	OVR_RE S_CFG	-	-					GPIO_RX_ID[4:0]
<b>GPIO5 5</b>									
0x310	<a href="#">GPIO_A[7:0]</a>	RES_CF G	-	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x311	<a href="#">GPIO_B[7:0]</a>	PULL_UPDN_SEL[1: 0]	OUT_TY PE						GPIO_TX_ID[4:0]
0x312	<a href="#">GPIO_C[7:0]</a>	OVR_RE S_CFG	-	-					GPIO_RX_ID[4:0]
<b>GPIO6 6</b>									
0x313	<a href="#">GPIO_A[7:0]</a>	RES_CF G	-	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x314	<a href="#">GPIO_B[7:0]</a>	PULL_UPDN_SEL[1: 0]	OUT_TY PE						GPIO_TX_ID[4:0]
0x315	<a href="#">GPIO_C[7:0]</a>	OVR_RE S_CFG	-	-					GPIO_RX_ID[4:0]
<b>GPIO7 7</b>									
0x316	<a href="#">GPIO_A[7:0]</a>	RES_CF G	-	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x317	<a href="#">GPIO_B[7:0]</a>	PULL_UPDN_SEL[1: 0]	OUT_TY PE						GPIO_TX_ID[4:0]
0x318	<a href="#">GPIO_C[7:0]</a>	OVR_RE S_CFG	-	-					GPIO_RX_ID[4:0]
<b>GPIO8 8</b>									
0x319	<a href="#">GPIO_A[7:0]</a>	RES_CF G	-	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x31A	<a href="#">GPIO_B[7:0]</a>	PULL_UPDN_SEL[1: 0]	OUT_TY PE						GPIO_TX_ID[4:0]
0x31B	<a href="#">GPIO_C[7:0]</a>	OVR_RE S_CFG	-	-					GPIO_RX_ID[4:0]
<b>GPIO9 9</b>									
0x31C	<a href="#">GPIO_A[7:0]</a>	RES_CF G	-	TX_COM P_EN	GPIO_O UT	GPIO_IN	GPIO_R X_EN	GPIO_T X_EN	GPIO_O UT_DIS
0x31D	<a href="#">GPIO_B[7:0]</a>	PULL_UPDN_SEL[1: 0]	OUT_TY PE						GPIO_TX_ID[4:0]

ADDRESS	NAME	MSB							LSB
0x31E	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO10 10</b>									
0x320	GPIO_A[7:0]	RES_CFG	-	TX_COM_P_EN	GPIO_UT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x321	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	OUT_TY_P_E	GPIO_TX_ID[4:0]					
0x322	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO11 11</b>									
0x323	GPIO_A[7:0]	RES_CFG	-	TX_COM_P_EN	GPIO_UT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x324	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	OUT_TY_P_E	GPIO_TX_ID[4:0]					
0x325	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO12 12</b>									
0x326	GPIO_A[7:0]	RES_CFG	-	TX_COM_P_EN	GPIO_UT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x327	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	OUT_TY_P_E	GPIO_TX_ID[4:0]					
0x328	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO13 13</b>									
0x329	GPIO_A[7:0]	RES_CFG	-	TX_COM_P_EN	GPIO_UT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x32A	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	OUT_TY_P_E	GPIO_TX_ID[4:0]					
0x32B	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO14 14</b>									
0x32C	GPIO_A[7:0]	RES_CFG	-	TX_COM_P_EN	GPIO_UT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x32D	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	OUT_TY_P_E	GPIO_TX_ID[4:0]					
0x32E	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO15 15</b>									
0x330	GPIO_A[7:0]	RES_CFG	-	TX_COM_P_EN	GPIO_UT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS
0x331	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]	-	GPIO_TX_ID[4:0]					
0x332	GPIO_C[7:0]	OVR_RS_CFG	-	-	GPIO_RX_ID[4:0]				
<b>GPIO16 16</b>									
0x333	GPIO_A[7:0]	RES_CFG	-	TX_COM_P_EN	GPIO_UT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_UT_DIS

ADDRESS	NAME	MSB							LSB	
0x334	<a href="#">GPIO_B[7:0]</a>	PULL_UPDN_SEL[1 :0]	–	GPIO_TX_ID[4:0]						
0x335	<a href="#">GPIO_C[7:0]</a>	OVR_RE_S_CFG	–	–	GPIO_RX_ID[4:0]					
<b>GPIO0_B 0</b>										
0x337	<a href="#">GPIO_B[7:0]</a>	–	TX_COMM_P_EN_B	GPIO_T_X_EN_B	GPIO_TX_ID_B[4:0]					
0x338	<a href="#">GPIO_C[7:0]</a>	–	–	GPIO_RX_X_EN_B	GPIO_RX_ID_B[4:0]					
<b>GPIO0_B 1</b>										
0x33A	<a href="#">GPIO_B[7:0]</a>	–	TX_COMM_P_EN_B	GPIO_T_X_EN_B	GPIO_TX_ID_B[4:0]					
0x33B	<a href="#">GPIO_C[7:0]</a>	–	–	GPIO_RX_X_EN_B	GPIO_RX_ID_B[4:0]					
<b>GPIO0_B 2</b>										
0x33D	<a href="#">GPIO_B[7:0]</a>	–	TX_COMM_P_EN_B	GPIO_T_X_EN_B	GPIO_TX_ID_B[4:0]					
0x33E	<a href="#">GPIO_C[7:0]</a>	–	–	GPIO_RX_X_EN_B	GPIO_RX_ID_B[4:0]					
<b>GPIO0_B 3</b>										
0x341	<a href="#">GPIO_B[7:0]</a>	–	TX_COMM_P_EN_B	GPIO_T_X_EN_B	GPIO_TX_ID_B[4:0]					
0x342	<a href="#">GPIO_C[7:0]</a>	–	–	GPIO_RX_X_EN_B	GPIO_RX_ID_B[4:0]					
<b>GPIO0_B 4</b>										
0x344	<a href="#">GPIO_B[7:0]</a>	–	TX_COMM_P_EN_B	GPIO_T_X_EN_B	GPIO_TX_ID_B[4:0]					
0x345	<a href="#">GPIO_C[7:0]</a>	–	–	GPIO_RX_X_EN_B	GPIO_RX_ID_B[4:0]					
<b>GPIO0_B 5</b>										
0x347	<a href="#">GPIO_B[7:0]</a>	–	TX_COMM_P_EN_B	GPIO_T_X_EN_B	GPIO_TX_ID_B[4:0]					
0x348	<a href="#">GPIO_C[7:0]</a>	–	–	GPIO_RX_X_EN_B	GPIO_RX_ID_B[4:0]					
<b>GPIO0_B 6</b>										
0x34A	<a href="#">GPIO_B[7:0]</a>	–	TX_COMM_P_EN_B	GPIO_T_X_EN_B	GPIO_TX_ID_B[4:0]					
0x34B	<a href="#">GPIO_C[7:0]</a>	–	–	GPIO_RX_X_EN_B	GPIO_RX_ID_B[4:0]					
<b>GPIO0_B 7</b>										
0x34D	<a href="#">GPIO_B[7:0]</a>	–	TX_COMM_P_EN_B	GPIO_T_X_EN_B	GPIO_TX_ID_B[4:0]					
0x34E	<a href="#">GPIO_C[7:0]</a>	–	–	GPIO_RX_X_EN_B	GPIO_RX_ID_B[4:0]					

ADDRESS	NAME	MSB						LSB
<b>GPIO0_B 8</b>								
0x351	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x352	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]
<b>GPIO0_B 9</b>								
0x354	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x355	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]
<b>GPIO0_B 10</b>								
0x357	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x358	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]
<b>GPIO0_B 11</b>								
0x35A	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x35B	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]
<b>GPIO0_B 12</b>								
0x35D	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x35E	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]
<b>GPIO0_B 13</b>								
0x361	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x362	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]
<b>GPIO0_B 14</b>								
0x364	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x365	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]
<b>GPIO0_B 15</b>								
0x367	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x368	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]
<b>GPIO0_B 16</b>								
0x36A	<a href="#">GPIO_B[7:0]</a>	-	TX_COM_P_EN_B	GPIO_T_X_EN_B				GPIO_RX_ID_B[4:0]
0x36B	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R_X_EN_B				GPIO_RX_ID_B[4:0]

ADDRESS	NAME	MSB						LSB
<b>GPIO0_C 0</b>								
0x36D	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x36E	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 1</b>								
0x371	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x372	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 2</b>								
0x374	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x375	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 3</b>								
0x377	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x378	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 4</b>								
0x37A	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x37B	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 5</b>								
0x37D	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x37E	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 6</b>								
0x381	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x382	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 7</b>								
0x384	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x385	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 8</b>								
0x387	<a href="#">GPIO_B[7:0]</a>	-	TX_COM P_EN_C	GPIO_T X_EN_C				GPIO_TX_ID_C[4:0]
0x388	<a href="#">GPIO_C[7:0]</a>	-	-	GPIO_R X_EN_C				GPIO_RX_ID_C[4:0]

ADDRESS	NAME	MSB						LSB
<b>GPIO0_C 9</b>								
0x38A	GPIO_B[7:0]	-	TX_COM_P_EN_C	GPIO_T_X_EN_C				GPIO_RX_ID_C[4:0]
0x38B	GPIO_C[7:0]	-	-	GPIO_R_X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 10</b>								
0x38D	GPIO_B[7:0]	-	TX_COM_P_EN_C	GPIO_T_X_EN_C				GPIO_RX_ID_C[4:0]
0x38E	GPIO_C[7:0]	-	-	GPIO_R_X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 11</b>								
0x391	GPIO_B[7:0]	-	TX_COM_P_EN_C	GPIO_T_X_EN_C				GPIO_RX_ID_C[4:0]
0x392	GPIO_C[7:0]	-	-	GPIO_R_X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 12</b>								
0x394	GPIO_B[7:0]	-	TX_COM_P_EN_C	GPIO_T_X_EN_C				GPIO_RX_ID_C[4:0]
0x395	GPIO_C[7:0]	-	-	GPIO_R_X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 13</b>								
0x397	GPIO_B[7:0]	-	TX_COM_P_EN_C	GPIO_T_X_EN_C				GPIO_RX_ID_C[4:0]
0x398	GPIO_C[7:0]	-	-	GPIO_R_X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 14</b>								
0x39A	GPIO_B[7:0]	-	TX_COM_P_EN_C	GPIO_T_X_EN_C				GPIO_RX_ID_C[4:0]
0x39B	GPIO_C[7:0]	-	-	GPIO_R_X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 15</b>								
0x39D	GPIO_B[7:0]	-	TX_COM_P_EN_C	GPIO_T_X_EN_C				GPIO_RX_ID_C[4:0]
0x39E	GPIO_C[7:0]	-	-	GPIO_R_X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_C 16</b>								
0x3A1	GPIO_B[7:0]	-	TX_COM_P_EN_C	GPIO_T_X_EN_C				GPIO_RX_ID_C[4:0]
0x3A2	GPIO_C[7:0]	-	-	GPIO_R_X_EN_C				GPIO_RX_ID_C[4:0]
<b>GPIO0_D 0</b>								
0x3A4	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3A5	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]

ADDRESS	NAME	MSB						LSB
<b>GPIO0_D 1</b>								
0x3A7	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3A8	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]
<b>GPIO0_D 2</b>								
0x3AA	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3AB	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]
<b>GPIO0_D 3</b>								
0x3AD	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3AE	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]
<b>GPIO0_D 4</b>								
0x3B1	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3B2	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]
<b>GPIO0_D 5</b>								
0x3B4	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3B5	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]
<b>GPIO0_D 6</b>								
0x3B7	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3B8	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]
<b>GPIO0_D 7</b>								
0x3BA	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3BB	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]
<b>GPIO0_D 8</b>								
0x3BD	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3BE	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]
<b>GPIO0_D 9</b>								
0x3C1	GPIO_B[7:0]	-	TX_COM_P_EN_D	GPIO_T_X_EN_D				GPIO_RX_ID_D[4:0]
0x3C2	GPIO_C[7:0]	-	-	GPIO_R_X_EN_D				GPIO_RX_ID_D[4:0]

ADDRESS	NAME	MSB							LSB
<b>GPIO0_D 10</b>									
0x3C4	<u>GPIO_B[7:0]</u>	-	TX_COM_P_EN_D	GPIO_T_X_EN_D					GPIO_RX_ID_D[4:0]
0x3C5	<u>GPIO_C[7:0]</u>	-	-	GPIO_R_X_EN_D					GPIO_RX_ID_D[4:0]
<b>GPIO0_D 11</b>									
0x3C7	<u>GPIO_B[7:0]</u>	-	TX_COM_P_EN_D	GPIO_T_X_EN_D					GPIO_RX_ID_D[4:0]
0x3C8	<u>GPIO_C[7:0]</u>	-	-	GPIO_R_X_EN_D					GPIO_RX_ID_D[4:0]
<b>GPIO0_D 12</b>									
0x3CA	<u>GPIO_B[7:0]</u>	-	TX_COM_P_EN_D	GPIO_T_X_EN_D					GPIO_RX_ID_D[4:0]
0x3CB	<u>GPIO_C[7:0]</u>	-	-	GPIO_R_X_EN_D					GPIO_RX_ID_D[4:0]
<b>GPIO0_D 13</b>									
0x3CD	<u>GPIO_B[7:0]</u>	-	TX_COM_P_EN_D	GPIO_T_X_EN_D					GPIO_RX_ID_D[4:0]
0x3CE	<u>GPIO_C[7:0]</u>	-	-	GPIO_R_X_EN_D					GPIO_RX_ID_D[4:0]
<b>GPIO0_D 14</b>									
0x3D1	<u>GPIO_B[7:0]</u>	-	TX_COM_P_EN_D	GPIO_T_X_EN_D					GPIO_RX_ID_D[4:0]
0x3D2	<u>GPIO_C[7:0]</u>	-	-	GPIO_R_X_EN_D					GPIO_RX_ID_D[4:0]
<b>GPIO0_D 15</b>									
0x3D4	<u>GPIO_B[7:0]</u>	-	TX_COM_P_EN_D	GPIO_T_X_EN_D					GPIO_RX_ID_D[4:0]
0x3D5	<u>GPIO_C[7:0]</u>	-	-	GPIO_R_X_EN_D					GPIO_RX_ID_D[4:0]
<b>GPIO0_D 16</b>									
0x3D7	<u>GPIO_B[7:0]</u>	-	TX_COM_P_EN_D	GPIO_T_X_EN_D					GPIO_RX_ID_D[4:0]
0x3D8	<u>GPIO_C[7:0]</u>	-	-	GPIO_R_X_EN_D					GPIO_RX_ID_D[4:0]
<b>GPIO_MS_ID</b>									
0x3F0	<u>MS_ID_A[7:0]</u>	-	-	-					RX_MS_ID_A[4:0]
0x3F1	<u>MS_ID_B[7:0]</u>	-	-	-					RX_MS_ID_B[4:0]
0x3F2	<u>MS_ID_C[7:0]</u>	-	-	-					RX_MS_ID_C[4:0]
0x3F3	<u>MS_ID_D[7:0]</u>	-	-	-					RX_MS_ID_D[4:0]
<b>BACKTOP</b>									
0x400	<u>BACKTOP1[7:0]</u>	CSIPLL3_LOCK	CSIPLL2_LOCK	CSIPLL1_LOCK	CSIPLL0_LOCK	LINE_SP_L2	LINE_SP_L0	-	BACKTOP_EN
0x40A	<u>BACKTOP11[7:0]</u>	cmd_ove_rflow3	cmd_ove_rflow2	cmd_ove_rflow1	cmd_ove_rflow0	LMO_3	LMO_2	LMO_1	LMO_0

ADDRESS	NAME	MSB							LSB							
0x40B	<a href="#">BACKTOP12[7:0]</a>	soft_bpp_0[4:0]				-	CSI_OUT_EN	-								
0x40C	<a href="#">BACKTOP13[7:0]</a>	soft_vc_1[3:0]			soft_vc_0[3:0]											
0x40D	<a href="#">BACKTOP14[7:0]</a>	soft_vc_3[3:0]			soft_vc_2[3:0]											
0x40E	<a href="#">BACKTOP15[7:0]</a>	soft_dt_1_h[1:0]		soft_dt_0[5:0]												
0x40F	<a href="#">BACKTOP16[7:0]</a>	soft_dt_2_h[3:0]			soft_dt_1_l[3:0]											
0x410	<a href="#">BACKTOP17[7:0]</a>	soft_dt_3[5:0]				soft_dt_2_l[1:0]										
0x411	<a href="#">BACKTOP18[7:0]</a>	soft_bpp_2_h[2:0]			soft_bpp_1[4:0]											
0x412	<a href="#">BACKTOP19[7:0]</a>	-	soft_bpp_3[4:0]				soft_bpp_2_l[1:0]									
0x413	<a href="#">BACKTOP20[7:0]</a>	phy0_csi_tx_dpll_fb_fraction_in_l[7:0]														
0x414	<a href="#">BACKTOP21[7:0]</a>	bpp8dbl3	bpp8dbl2	bpp8dbl1	bpp8dbl0	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]										
0x415	<a href="#">BACKTOP22[7:0]</a>	override_bpp_vc_dt_1	override_bpp_vc_dt_0	phy0_csi_tx_dpll_fb_fraction_predef_en	phy0_csi_tx_dpll_predef_freq[4:0]											
0x416	<a href="#">BACKTOP23[7:0]</a>	phy1_csi_tx_dpll_fb_fraction_in_l[7:0]														
0x417	<a href="#">BACKTOP24[7:0]</a>	bpp8dbl3_mode	bpp8dbl2_mode	bpp8dbl1_mode	bpp8dbl0_mode	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]										
0x418	<a href="#">BACKTOP25[7:0]</a>	override_bpp_vc_dt_3	override_bpp_vc_dt_2	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]											
0x419	<a href="#">BACKTOP26[7:0]</a>	phy2_csi_tx_dpll_fb_fraction_in_l[7:0]														
0x41A	<a href="#">BACKTOP27[7:0]</a>	yuv_8_1_0_mux_mode3	yuv_8_1_0_mux_mode2	yuv_8_1_0_mux_mode1	yuv_8_1_0_mux_mode0	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]										
0x41B	<a href="#">BACKTOP28[7:0]</a>	override_bpp_vc_dt_5	override_bpp_vc_dt_4	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]											
0x41C	<a href="#">BACKTOP29[7:0]</a>	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]														
0x41D	<a href="#">BACKTOP30[7:0]</a>	override_bpp_vc_dt_7	override_bpp_vc_dt_6	bpp10dbl3_mode	bpp10dbl3	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]										
0x41E	<a href="#">BACKTOP31[7:0]</a>	bpp10dbl2_mode	bpp10dbl2	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]											
0x41F	<a href="#">BACKTOP32[7:0]</a>	bpp10dbl1_mode	bpp10dbl1	bpp10dbl0_mode	bpp10dbl0	bpp12dbl3	bpp12dbl2	bpp12dbl1	bpp12dbl0							
<b>BACKTOP_1</b>																
0x420	<a href="#">BACKTOP1[7:0]</a>	-	-	-	-	LINE_SP_L6	LINE_SP_L4	-	-							

ADDRESS	NAME	MSB							LSB		
0x429	<a href="#">BACKTOP10[7:0]</a>	DE_SEL_7	DE_SEL_6	DE_SEL_5	DE_SEL_4	LS_LE_EN7	LS_LE_EN6	LS_LE_EN5	LS_LE_EN4		
0x42A	<a href="#">BACKTOP11[7:0]</a>	cmd_ove_rflow7	cmd_ove_rflow6	cmd_ove_rflow5	cmd_ove_rflow4	LMO_7	LMO_6	LMO_5	LMO_4		
0x42B	<a href="#">BACKTOP12[7:0]</a>	soft_bpp_4[4:0]					-	-	-		
0x42C	<a href="#">BACKTOP13[7:0]</a>	soft_vc_5[3:0]				soft_vc_4[3:0]					
0x42D	<a href="#">BACKTOP14[7:0]</a>	soft_vc_7[3:0]				soft_vc_6[3:0]					
0x42E	<a href="#">BACKTOP15[7:0]</a>	soft_dt_5_h[1:0]				soft_dt_4[5:0]					
0x42F	<a href="#">BACKTOP16[7:0]</a>	soft_dt_6_h[3:0]				soft_dt_5_l[3:0]					
0x430	<a href="#">BACKTOP17[7:0]</a>	soft_dt_7[5:0]					soft_dt_6_l[1:0]				
0x431	<a href="#">BACKTOP18[7:0]</a>	soft_bpp_6_h[2:0]				soft_bpp_5[4:0]					
0x432	<a href="#">BACKTOP19[7:0]</a>	-	soft_bpp_7[4:0]					soft_bpp_6_l[1:0]			
0x434	<a href="#">BACKTOP21[7:0]</a>	bpp8dbl7	bpp8dbl6	bpp8dbl5	bpp8dbl4	-	-	-	-		
0x435	<a href="#">BACKTOP22[7:0]</a>	-	-	-	-	n_vs_block[3:0]					
0x436	<a href="#">BACKTOP23[7:0]</a>	dis_vs7	dis_vs6	dis_vs5	dis_vs4	dis_vs3	dis_vs2	dis_vs1	dis_vs0		
0x437	<a href="#">BACKTOP24[7:0]</a>	bpp8dbl7_mode	bpp8dbl6_mode	bpp8dbl5_mode	bpp8dbl4_mode	-	-	-	-		
0x438	<a href="#">BACKTOP25[7:0]</a>	mem_err_7	mem_err_6	mem_err_5	mem_err_4	mem_err_3	mem_err_2	mem_err_1	mem_err_0		
0x43A	<a href="#">BACKTOP27[7:0]</a>	yuv_8_1_0_mux_mode7	yuv_8_1_0_mux_mode6	yuv_8_1_0_mux_mode5	yuv_8_1_0_mux_mode4	-	-	-	-		
0x43D	<a href="#">BACKTOP30[7:0]</a>	-	-	bpp10dbl7_mode	bpp10dbl7	-	-	-	-		
0x43E	<a href="#">BACKTOP31[7:0]</a>	bpp10dbl6_mode	bpp10dbl6	-	-	-	-	-	-		
0x43F	<a href="#">BACKTOP32[7:0]</a>	bpp10dbl5_mode	bpp10dbl5	bpp10dbl4_mode	bpp10dbl4	bpp12dbl7	bpp12dbl6	bpp12dbl5	bpp12dbl4		
<b>FSYNC</b>											
0x4A0	<a href="#">FSYNC_0[7:0]</a>	-	-	FSYNC_OUT_PI_N	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC METH[1:0]			
0x4A1	<a href="#">FSYNC_1[7:0]</a>	-	-	-	-	FSYNC_PER_DIV[3:0]					
0x4A2	<a href="#">FSYNC_2[7:0]</a>	MST_LINK_SEL[2:0]			K_VAL_SIGN	K_VAL[3:0]					
0x4A3	<a href="#">FSYNC_3[7:0]</a>	P_VAL_L[7:0]									
0x4A4	<a href="#">FSYNC_4[7:0]</a>	-	-	P_VAL_SIGN	P_VAL_H[4:0]						
0x4A5	<a href="#">FSYNC_5[7:0]</a>	FSYNC_PERIOD_L[7:0]									
0x4A6	<a href="#">FSYNC_6[7:0]</a>	FSYNC_PERIOD_M[7:0]									
0x4A7	<a href="#">FSYNC_7[7:0]</a>	FSYNC_PERIOD_H[7:0]									
0x4A8	<a href="#">FSYNC_8[7:0]</a>	FRM_DIFF_ERR_THR_L[7:0]									
0x4A9	<a href="#">FSYNC_9[7:0]</a>	-	-	-	FRM_DIFF_ERR_THR_H[4:0]						
0x4AA	<a href="#">FSYNC_10[7:0]</a>	OVLP_WINDOW_L[7:0]									

ADDRESS	NAME	MSB							LSB			
0x4AB	<u>FSYNC_11[7:0]</u>	EN_FSI_N_LAST	-	-	OVLP_WINDOW_H[4:0]							
0x4AF	<u>FSYNC_15[7:0]</u>	FS_GPO_TYPE	FS_USE_XTAL	-	AUTO_FS_LINKS	FS_LINK_3	FS_LINK_2	FS_LINK_1	FS_LINK_0			
0x4B0	<u>FSYNC_16[7:0]</u>	FSYNC_ERR_CNT[7:0]										
0x4B1	<u>FSYNC_17[7:0]</u>	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]					
0x4B2	<u>FSYNC_18[7:0]</u>	CALC_FRM_LEN_L[7:0]										
0x4B3	<u>FSYNC_19[7:0]</u>	CALC_FRM_LEN_M[7:0]										
0x4B4	<u>FSYNC_20[7:0]</u>	CALC_FRM_LEN_H[7:0]										
0x4B5	<u>FSYNC_21[7:0]</u>	FRM_DIFF_L[7:0]										
0x4B6	<u>FSYNC_22[7:0]</u>	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]								
0x4B7	FSYNC_23[7:0]	-	-	-	-	-	-	-	-			
<b>SPI_0</b>												
0x4E0	<u>SPI_0[7:0]</u>	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]	SPI IGN R_ID	SPI_CC_EN	MST_SL_VN	SPI_EN				
0x4E1	<u>SPI_1[7:0]</u>	SPI_LOC_N[5:0]					-	-				
0x4E2	<u>SPI_2[7:0]</u>	REQ_HOLD_OFF[2:0]			FULL_SCK_SET_UP	SPI_MO_D3_F	SPI_MO_D3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H			
0x4E3	<u>SPI_3[7:0]</u>	SPIM_SS_DLY_CLKS[7:0]										
0x4E4	<u>SPI_4[7:0]</u>	SPIM_SCK_LO_CLKS[7:0]										
0x4E5	<u>SPI_5[7:0]</u>	SPIM_SCK_HI_CLKS[7:0]										
0x4E6	<u>SPI_6[7:0]</u>	-	-	BNE	SPIS_R_WN	SS_IO_E_N_2	SS_IO_E_N_1	BNE_IO_EN	RWN_IO_EN			
0x4E7	<u>SPI_7[7:0]</u>	SPI_RX_OVRFLW	SPI_TX_OVRFLW	-	SPIS_BYTE_CNT[4:0]							
0x4E8	<u>SPI_8[7:0]</u>	REQ_HOLD_OFF_TO[7:0]										
0x4E9	<u>SPI_9[7:0]</u>						SPI_0_LINK_SELECT[1:0]					
<b>SPI_1</b>												
0x4F0	<u>SPI_0[7:0]</u>	SPI_LOC_ID_1[1:0]		SPI_CC_TRG_ID_1[1:0]	SPI IGN R_ID_1	SPI_CC_EN_1	MST_SL_VN_1	SPI_EN_1				
0x4F1	<u>SPI_1[7:0]</u>	SPI_LOC_N_1[5:0]					-	-				
0x4F2	<u>SPI_2[7:0]</u>	REQ_HOLD_OFF_1[2:0]			FULL_SCK_SET_UP_1	SPI_MO_D3_F_1	SPI_MO_D3_1	SPIM_SS2_ACT_H_1	SPIM_SS1_ACT_H_1			
0x4F3	<u>SPI_3[7:0]</u>	SPIM_SS_DLY_CLKS_1[7:0]										
0x4F4	<u>SPI_4[7:0]</u>	SPIM_SCK_LO_CLKS_1[7:0]										
0x4F5	<u>SPI_5[7:0]</u>	SPIM_SCK_HI_CLKS_1[7:0]										
0x4F6	<u>SPI_6[7:0]</u>	-	-	BNE_1	SPIS_R_WN_1	SS_IO_E_N_2_1	SS_IO_E_N_1_1	BNE_IO_EN_1	RWN_IO_EN_1			

ADDRESS	NAME	MSB							LSB
0x4F7	SPI_7[7:0]	SPI_RX_OVRFL_W_1	SPI_TX_OVRFL_W_1	-	SPIS_BYTE_CNT_1[4:0]				
0x4F8	SPI_8[7:0]	REQ_HOLD_OFF_TO_1[7:0]							
0x4F9	SPI_9[7:0]						SPI_1_LINK_SELEC_T[1:0]		
<b>CFGC_A CC_0</b>									
0x500	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	-	-	PRI_O_VAL[1:0]	PRI_O_CFG[1:0]		
0x501	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x503	TR3[7:0]	-	-	-	-	-	TX_SRC_ID[2:0]		
0x504	TR4[7:0]	RX_SRC_SEL[7:0]							
0x505	ARQ0[7:0]	-	-	-	-	EN	DIS_DBL_ACK_R_ETX	-	-
0x506	ARQ1[7:0]	-	-	-	-	-	-	MAX_RT_ERR_O_EN	RT_CNT_OEN
0x507	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
<b>CFGC_B CC_0</b>									
0x510	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	-	-	PRI_O_VAL_B[1:0]	PRI_O_CFG_B[1:0]		
0x511	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x513	TR3[7:0]	-	-	-	-	-	TX_SRC_ID_B[2:0]		
0x514	TR4[7:0]	RX_SRC_SEL_B[7:0]							
0x515	ARQ0[7:0]	-	-	-	-	EN_B	DIS_DBL_ACK_R_ETX_B	-	-
0x516	ARQ1[7:0]	-	-	-	-	-	-	MAX_RT_ERR_O_EN_B	RT_CNT_OEN_B
0x517	ARQ2[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
<b>CFGC_C CC_0</b>									
0x520	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	-	-	PRI_O_VAL_C[1:0]	PRI_O_CFG_C[1:0]		
0x521	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0x523	TR3[7:0]	-	-	-	-	-	TX_SRC_ID_C[2:0]		
0x524	TR4[7:0]	RX_SRC_SEL_C[7:0]							
0x525	ARQ0[7:0]	-	-	-	-	EN_C	DIS_DBL_ACK_R_ETX_C	-	-
0x526	ARQ1[7:0]	-	-	-	-	-	-	MAX_RT_ERR_O_EN_C	RT_CNT_OEN_C

ADDRESS	NAME	MSB							LSB
0x527	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR_C	RT_CNT_C[6:0]						
<b>CFGC_D CC_0</b>									
0x530	<a href="#">TR0[7:0]</a>	TX_CRC_EN_D	RX_CRC_EN_D	-	-	PRIO_VAL_D[1:0]	PRIO_CFG_D[1:0]		
0x531	<a href="#">TR1[7:0]</a>	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0x533	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID_D[2:0]		
0x534	<a href="#">TR4[7:0]</a>	RX_SRC_SEL_D[7:0]							
0x535	<a href="#">ARQ0[7:0]</a>	-	-	-	-	EN_D	DIS_DBL_ACK_R_ETX_D	-	-
0x536	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT_ERR_O_EN_D	RT_CNT_OEN_D
0x537	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR_D	RT_CNT_D[6:0]						
<b>CFGC_A CC_1</b>									
0x560	<a href="#">TR0[7:0]</a>	TX_CRC_EN	RX_CRC_EN	-	-	PRIO_VAL[1:0]	PRIO_CFG[1:0]		
0x561	<a href="#">TR1[7:0]</a>	BW_MULT[1:0]		BW_VAL[5:0]					
0x563	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID[2:0]		
0x564	<a href="#">TR4[7:0]</a>	RX_SRC_SEL[7:0]							
0x565	<a href="#">ARQ0[7:0]</a>	-	-	-	-	EN	DIS_DBL_ACK_R_ETX	-	-
0x566	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT_ERR_O_EN	RT_CNT_OEN
0x567	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR	RT_CNT[6:0]						
<b>CFGC_B CC_1</b>									
0x570	<a href="#">TR0[7:0]</a>	TX_CRC_EN_B	RX_CRC_EN_B	-	-	PRIO_VAL_B[1:0]	PRIO_CFG_B[1:0]		
0x571	<a href="#">TR1[7:0]</a>	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x573	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID_B[2:0]		
0x574	<a href="#">TR4[7:0]</a>	RX_SRC_SEL_B[7:0]							
0x575	<a href="#">ARQ0[7:0]</a>	-	-	-	-	EN_B	DIS_DBL_ACK_R_ETX_B	-	-
0x576	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT_ERR_O_EN_B	RT_CNT_OEN_B
0x577	<a href="#">ARQ2[7:0]</a>	MAX_RT_ERR_B	RT_CNT_B[6:0]						
<b>CFGC_C CC_1</b>									
0x580	<a href="#">TR0[7:0]</a>	TX_CRC_EN_C	RX_CRC_EN_C	-	-	PRIO_VAL_C[1:0]	PRIO_CFG_C[1:0]		

ADDRESS	NAME	MSB							LSB		
0x581	<a href="#">TR1[7:0]</a>	BW_MULT_C[1:0]	BW_VAL_C[5:0]								
0x583	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID_C[2:0]				
0x584	<a href="#">TR4[7:0]</a>	RX_SRC_SEL_C[7:0]									
0x585	<a href="#">ARQ0[7:0]</a>	-	-	-	-	EN_C	DIS_DBL _ACK_R ETX_C	-	-		
0x586	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT _ERR_O EN_C	RT_CNT _OEN_C		
0x587	<a href="#">ARQ2[7:0]</a>	MAX_RT _ERR_C	RT_CNT_C[6:0]								
<b>CFGC_D CC_1</b>											
0x590	<a href="#">TR0[7:0]</a>	TX_CRC _EN_D	RX_CRC _EN_D	-	-	PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]			
0x591	<a href="#">TR1[7:0]</a>	BW_MULT_D[1:0]		BW_VAL_D[5:0]							
0x593	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID_D[2:0]				
0x594	<a href="#">TR4[7:0]</a>	RX_SRC_SEL_D[7:0]									
0x595	<a href="#">ARQ0[7:0]</a>	-	-	-	-	EN_D	DIS_DBL _ACK_R ETX_D	-	-		
0x596	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT _ERR_O EN_D	RT_CNT _OEN_D		
0x597	<a href="#">ARQ2[7:0]</a>	MAX_RT _ERR_D	RT_CNT_D[6:0]								
<b>CFGC_A CC_2</b>											
0x5A0	<a href="#">TR0[7:0]</a>	TX_CRC _EN	RX_CRC _EN	-	-	PRIO_VAL[1:0]		PRIO_CFG[1:0]			
0x5A1	<a href="#">TR1[7:0]</a>	BW_MULT[1:0]		BW_VAL[5:0]							
0x5A3	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID[2:0]				
0x5A4	<a href="#">TR4[7:0]</a>	RX_SRC_SEL[7:0]									
0x5A5	<a href="#">ARQ0[7:0]</a>	-	-	-	-	EN	DIS_DBL _ACK_R ETX	-	-		
0x5A6	<a href="#">ARQ1[7:0]</a>	-	-	-	-	-	-	MAX_RT _ERR_O EN	RT_CNT _OEN		
0x5A7	<a href="#">ARQ2[7:0]</a>	MAX_RT _ERR	RT_CNT[6:0]								
<b>CFGC_B CC_2</b>											
0x5B0	<a href="#">TR0[7:0]</a>	TX_CRC _EN_B	RX_CRC _EN_B	-	-	PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]			
0x5B1	<a href="#">TR1[7:0]</a>	BW_MULT_B[1:0]		BW_VAL_B[5:0]							
0x5B3	<a href="#">TR3[7:0]</a>	-	-	-	-	-	TX_SRC_ID_B[2:0]				
0x5B4	<a href="#">TR4[7:0]</a>	RX_SRC_SEL_B[7:0]									

## MAX96722

Quad GMSL2 to CSI-2 Deserializer  
with GMSL1 Compatibility**PRELIMINARY**

ADDRESS	NAME	MSB							LSB			
0x5B5	<u>ARQ0[7:0]</u>	-	-	-	-	EN_B	DIS_DBL _ACK_R ETX_B	-	-			
0x5B6	<u>ARQ1[7:0]</u>	-	-	-	-	-	-	MAX_RT _ERR_O EN_B	RT_CNT _OEN_B			
0x5B7	<u>ARQ2[7:0]</u>	MAX_RT _ERR_B	RT_CNT_B[6:0]									
<b>CFG_C CC_2</b>												
0x5C0	<u>TR0[7:0]</u>	TX_CRC _EN_C	RX_CRC _EN_C	-	-	PRIO_VAL_C[1:0]	PRIO_CFG_C[1:0]					
0x5C1	<u>TR1[7:0]</u>	BW_MULT_C[1:0]		BW_VAL_C[5:0]								
0x5C3	<u>TR3[7:0]</u>	-	-	-	-	-	TX_SRC_ID_C[2:0]					
0x5C4	<u>TR4[7:0]</u>	RX_SRC_SEL_C[7:0]										
0x5C5	<u>ARQ0[7:0]</u>	-	-	-	-	EN_C	DIS_DBL _ACK_R ETX_C	-	-			
0x5C6	<u>ARQ1[7:0]</u>	-	-	-	-	-	-	MAX_RT _ERR_O EN_C	RT_CNT _OEN_C			
0x5C7	<u>ARQ2[7:0]</u>	MAX_RT _ERR_C	RT_CNT_C[6:0]									
<b>CFG_D CC_2</b>												
0x5D0	<u>TR0[7:0]</u>	TX_CRC _EN_D	RX_CRC _EN_D	-	-	PRIO_VAL_D[1:0]	PRIO_CFG_D[1:0]					
0x5D1	<u>TR1[7:0]</u>	BW_MULT_D[1:0]		BW_VAL_D[5:0]								
0x5D3	<u>TR3[7:0]</u>	-	-	-	-	-	TX_SRC_ID_D[2:0]					
0x5D4	<u>TR4[7:0]</u>	RX_SRC_SEL_D[7:0]										
0x5D5	<u>ARQ0[7:0]</u>	-	-	-	-	EN_D	DIS_DBL _ACK_R ETX_D	-	-			
0x5D6	<u>ARQ1[7:0]</u>	-	-	-	-	-	-	MAX_RT _ERR_O EN_D	RT_CNT _OEN_D			
0x5D7	<u>ARQ2[7:0]</u>	MAX_RT _ERR_D	RT_CNT_D[6:0]									
<b>CC_G2P0_A</b>												
0x640	<u>I2C_0[7:0]</u>	-	-	SLV_SH_P0_A[1:0]	-	SLV_TO_P0_A[2:0]						
0x641	<u>I2C_1[7:0]</u>	-	MST_BT_P0_A[2:0]			-	MST_TO_P0_A[2:0]					
0x642	<u>I2C_2[7:0]</u>	SRC_A_P0_A[6:0]							-			
0x643	<u>I2C_3[7:0]</u>	DST_A_P0_A[6:0]							-			
0x644	<u>I2C_4[7:0]</u>	SRC_B_P0_A[6:0]							-			
0x645	<u>I2C_5[7:0]</u>	DST_B_P0_A[6:0]							-			
<b>CC_G2P0_B</b>												
0x650	<u>I2C_0[7:0]</u>	-	-	SLV_SH_P0_B[1:0]	-	SLV_TO_P0_B[2:0]						
0x651	<u>I2C_1[7:0]</u>	-	MST_BT_P0_B[2:0]			-	MST_TO_P0_B[2:0]					

ADDRESS	NAME	MSB						LSB
0x652	I2C_2[7:0]				SRC_A_P0_B[6:0]			-
0x653	I2C_3[7:0]				DST_A_P0_B[6:0]			-
0x654	I2C_4[7:0]				SRC_B_P0_B[6:0]			-
0x655	I2C_5[7:0]				DST_B_P0_B[6:0]			-
<b>CC_G2P0_C</b>								
0x660	I2C_0[7:0]	-	-	SLV_SH_P0_C[1:0]	-		SLV_TO_P0_C[2:0]	
0x661	I2C_1[7:0]	-		MST_BT_P0_C[2:0]	-		MST_TO_P0_C[2:0]	
0x662	I2C_2[7:0]			SRC_A_P0_C[6:0]			-	
0x663	I2C_3[7:0]			DST_A_P0_C[6:0]			-	
0x664	I2C_4[7:0]			SRC_B_P0_C[6:0]			-	
0x665	I2C_5[7:0]			DST_B_P0_C[6:0]			-	
<b>CC_G2P0_D</b>								
0x670	I2C_0[7:0]	-	-	SLV_SH_P0_D[1:0]	-		SLV_TO_P0_D[2:0]	
0x671	I2C_1[7:0]	-		MST_BT_P0_D[2:0]	-		MST_TO_P0_D[2:0]	
0x672	I2C_2[7:0]			SRC_A_P0_D[6:0]			-	
0x673	I2C_3[7:0]			DST_A_P0_D[6:0]			-	
0x674	I2C_4[7:0]			SRC_B_P0_D[6:0]			-	
0x675	I2C_5[7:0]			DST_B_P0_D[6:0]			-	
<b>CC_G2P1_A</b>								
0x680	I2C_0[7:0]	-	-	SLV_SH_P1_A[1:0]	-		SLV_TO_P1_A[2:0]	
0x681	I2C_1[7:0]	-		MST_BT_P1_A[2:0]	-		MST_TO_P1_A[2:0]	
0x682	I2C_2[7:0]			SRC_A_P1_A[6:0]			-	
0x683	I2C_3[7:0]			DST_A_P1_A[6:0]			-	
0x684	I2C_4[7:0]			SRC_B_P1_A[6:0]			-	
0x685	I2C_5[7:0]			DST_B_P1_A[6:0]			-	
<b>CC_G2P2_A</b>								
0x688	I2C_0[7:0]	-	-	SLV_SH_P2_A[1:0]	-		SLV_TO_P2_A[2:0]	
0x689	I2C_1[7:0]	-		MST_BT_P2_A[2:0]	-		MST_TO_P2_A[2:0]	
0x68A	I2C_2[7:0]			SRC_A_P2_A[6:0]			-	
0x68B	I2C_3[7:0]			DST_A_P2_A[6:0]			-	
0x68C	I2C_4[7:0]			SRC_B_P2_A[6:0]			-	
0x68D	I2C_5[7:0]			DST_B_P2_A[6:0]			-	
<b>CC_G2P1_B</b>								
0x690	I2C_0[7:0]	-	-	SLV_SH_P1_B[1:0]	-		SLV_TO_P1_B[2:0]	
0x691	I2C_1[7:0]	-		MST_BT_P1_B[2:0]	-		MST_TO_P1_B[2:0]	
0x692	I2C_2[7:0]			SRC_A_P1_B[6:0]			-	
0x693	I2C_3[7:0]			DST_A_P1_B[6:0]			-	
0x694	I2C_4[7:0]			SRC_B_P1_B[6:0]			-	
0x695	I2C_5[7:0]			DST_B_P1_B[6:0]			-	
<b>CC_G2P2_B</b>								
0x698	I2C_0[7:0]	-	-	SLV_SH_P2_B[1:0]	-		SLV_TO_P2_B[2:0]	

ADDRESS	NAME	MSB						LSB	
0x699	I2C_1[7:0]	-	MST_BT_P2_B[2:0]		-	MST_TO_P2_B[2:0]			
0x69A	I2C_2[7:0]		SRC_A_P2_B[6:0]					-	
0x69B	I2C_3[7:0]		DST_A_P2_B[6:0]					-	
0x69C	I2C_4[7:0]		SRC_B_P2_B[6:0]					-	
0x69D	I2C_5[7:0]		DST_B_P2_B[6:0]					-	
<b>CC_G2P1_C</b>									
0x6A0	I2C_0[7:0]	-	-	SLV_SH_P1_C[1:0]	-	SLV_TO_P1_C[2:0]			
0x6A1	I2C_1[7:0]	-	MST_BT_P1_C[2:0]		-	MST_TO_P1_C[2:0]			
0x6A2	I2C_2[7:0]		SRC_A_P1_C[6:0]					-	
0x6A3	I2C_3[7:0]		DST_A_P1_C[6:0]					-	
0x6A4	I2C_4[7:0]		SRC_B_P1_C[6:0]					-	
0x6A5	I2C_5[7:0]		DST_B_P1_C[6:0]					-	
<b>CC_G2P2_C</b>									
0x6A8	I2C_0[7:0]	-	-	SLV_SH_P2_C[1:0]	-	SLV_TO_P2_C[2:0]			
0x6A9	I2C_1[7:0]	-	MST_BT_P2_C[2:0]		-	MST_TO_P2_C[2:0]			
0x6AA	I2C_2[7:0]		SRC_A_P2_C[6:0]					-	
0x6AB	I2C_3[7:0]		DST_A_P2_C[6:0]					-	
0x6AC	I2C_4[7:0]		SRC_B_P2_C[6:0]					-	
0x6AD	I2C_5[7:0]		DST_B_P2_C[6:0]					-	
<b>CC_G2P1_D</b>									
0x6B0	I2C_0[7:0]	-	-	SLV_SH_P1_D[1:0]	-	SLV_TO_P1_D[2:0]			
0x6B1	I2C_1[7:0]	-	MST_BT_P1_D[2:0]		-	MST_TO_P1_D[2:0]			
0x6B2	I2C_2[7:0]		SRC_A_P1_D[6:0]					-	
0x6B3	I2C_3[7:0]		DST_A_P1_D[6:0]					-	
0x6B4	I2C_4[7:0]		SRC_B_P1_D[6:0]					-	
0x6B5	I2C_5[7:0]		DST_B_P1_D[6:0]					-	
<b>CC_G2P2_D</b>									
0x6B8	I2C_0[7:0]	-	-	SLV_SH_P2_D[1:0]	-	SLV_TO_P2_D[2:0]			
0x6B9	I2C_1[7:0]	-	MST_BT_P2_D[2:0]		-	MST_TO_P2_D[2:0]			
0x6BA	I2C_2[7:0]		SRC_A_P2_D[6:0]					-	
0x6BB	I2C_3[7:0]		DST_A_P2_D[6:0]					-	
0x6BC	I2C_4[7:0]		SRC_B_P2_D[6:0]					-	
0x6BD	I2C_5[7:0]		DST_B_P2_D[6:0]					-	
<b>CMU</b>									
0x6C2	CMU2[7:0]	RSVD	RSVD[2:0]		RSVD	RSVD[1:0]	RSVD		
0x6C4	CMU4[7:0]	A_SPEED[1:0]	B_SPEED[1:0]		C_SPEED[1:0]	D_SPEED[1:0]			
<b>MISC</b>									
0x6DF	DP_ORSTB_CTL[7:0]	-	DP_RST_MIPI3	DP_RST_STABLE	DP_RST_MIPI2	DP_RST_MIPI	DP_RST_VP	DP_RST_FS	DP_RST_CC
<b>MIPI_TX_EXT 0</b>									
0x800	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-		

**PRELIMINARY**

ADDRESS	NAME	MSB					LSB
0x801	<a href="#">MIPI_TX_EXT1[7:0]</a>	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-
0x802	<a href="#">MIPI_TX_EXT2[7:0]</a>	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-
0x803	<a href="#">MIPI_TX_EXT3[7:0]</a>	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-
0x804	<a href="#">MIPI_TX_EXT4[7:0]</a>	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-
0x805	<a href="#">MIPI_TX_EXT5[7:0]</a>	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		-	-
0x806	<a href="#">MIPI_TX_EXT6[7:0]</a>	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		-	-
0x807	<a href="#">MIPI_TX_EXT7[7:0]</a>	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		-	-
0x808	<a href="#">MIPI_TX_EXT8[7:0]</a>	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		-	-
0x809	<a href="#">MIPI_TX_EXT9[7:0]</a>	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		-	-
0x80A	<a href="#">MIPI_TX_EXT10[7:0]</a>	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		-	-
0x80B	<a href="#">MIPI_TX_EXT11[7:0]</a>	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		-	-
0x80C	<a href="#">MIPI_TX_EXT12[7:0]</a>	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		-	-
0x80D	<a href="#">MIPI_TX_EXT13[7:0]</a>	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		-	-
0x80E	<a href="#">MIPI_TX_EXT14[7:0]</a>	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		-	-
0x80F	<a href="#">MIPI_TX_EXT15[7:0]</a>	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		-	-
<b>MIPI_TX_EXT 1</b>							
0x810	<a href="#">MIPI_TX_EXT0[7:0]</a>	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-
0x811	<a href="#">MIPI_TX_EXT1[7:0]</a>	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-
0x812	<a href="#">MIPI_TX_EXT2[7:0]</a>	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-
0x813	<a href="#">MIPI_TX_EXT3[7:0]</a>	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-
0x814	<a href="#">MIPI_TX_EXT4[7:0]</a>	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-
0x815	<a href="#">MIPI_TX_EXT5[7:0]</a>	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		-	-
0x816	<a href="#">MIPI_TX_EXT6[7:0]</a>	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		-	-
0x817	<a href="#">MIPI_TX_EXT7[7:0]</a>	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		-	-
0x818	<a href="#">MIPI_TX_EXT8[7:0]</a>	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		-	-
0x819	<a href="#">MIPI_TX_EXT9[7:0]</a>	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		-	-
0x81A	<a href="#">MIPI_TX_EXT10[7:0]</a>	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		-	-
0x81B	<a href="#">MIPI_TX_EXT11[7:0]</a>	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		-	-
0x81C	<a href="#">MIPI_TX_EXT12[7:0]</a>	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		-	-
0x81D	<a href="#">MIPI_TX_EXT13[7:0]</a>	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		-	-
0x81E	<a href="#">MIPI_TX_EXT14[7:0]</a>	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		-	-
0x81F	<a href="#">MIPI_TX_EXT15[7:0]</a>	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		-	-
<b>MIPI_TX_EXT 2</b>							
0x820	<a href="#">MIPI_TX_EXT0[7:0]</a>	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-
0x821	<a href="#">MIPI_TX_EXT1[7:0]</a>	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-
0x822	<a href="#">MIPI_TX_EXT2[7:0]</a>	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-
0x823	<a href="#">MIPI_TX_EXT3[7:0]</a>	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-
0x824	<a href="#">MIPI_TX_EXT4[7:0]</a>	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-
0x825	<a href="#">MIPI_TX_EXT5[7:0]</a>	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		-	-
0x826	<a href="#">MIPI_TX_EXT6[7:0]</a>	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		-	-
0x827	<a href="#">MIPI_TX_EXT7[7:0]</a>	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		-	-

ADDRESS	NAME	MSB					LSB
0x828	<a href="#">MIPI_TX_EXT8[7:0]</a>	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		-	-
0x829	<a href="#">MIPI_TX_EXT9[7:0]</a>	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		-	-
0x82A	<a href="#">MIPI_TX_EXT10[7:0]</a>	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		-	-
0x82B	<a href="#">MIPI_TX_EXT11[7:0]</a>	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		-	-
0x82C	<a href="#">MIPI_TX_EXT12[7:0]</a>	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		-	-
0x82D	<a href="#">MIPI_TX_EXT13[7:0]</a>	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		-	-
0x82E	<a href="#">MIPI_TX_EXT14[7:0]</a>	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		-	-
0x82F	<a href="#">MIPI_TX_EXT15[7:0]</a>	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		-	-
<b>MIPI_TX_EXT 3</b>							
0x830	<a href="#">MIPI_TX_EXT0[7:0]</a>	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-
0x831	<a href="#">MIPI_TX_EXT1[7:0]</a>	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-
0x832	<a href="#">MIPI_TX_EXT2[7:0]</a>	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-
0x833	<a href="#">MIPI_TX_EXT3[7:0]</a>	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-
0x834	<a href="#">MIPI_TX_EXT4[7:0]</a>	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-
0x835	<a href="#">MIPI_TX_EXT5[7:0]</a>	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		-	-
0x836	<a href="#">MIPI_TX_EXT6[7:0]</a>	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		-	-
0x837	<a href="#">MIPI_TX_EXT7[7:0]</a>	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		-	-
0x838	<a href="#">MIPI_TX_EXT8[7:0]</a>	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		-	-
0x839	<a href="#">MIPI_TX_EXT9[7:0]</a>	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		-	-
0x83A	<a href="#">MIPI_TX_EXT10[7:0]</a>	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		-	-
0x83B	<a href="#">MIPI_TX_EXT11[7:0]</a>	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		-	-
0x83C	<a href="#">MIPI_TX_EXT12[7:0]</a>	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		-	-
0x83D	<a href="#">MIPI_TX_EXT13[7:0]</a>	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		-	-
0x83E	<a href="#">MIPI_TX_EXT14[7:0]</a>	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		-	-
0x83F	<a href="#">MIPI_TX_EXT15[7:0]</a>	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		-	-
<b>MIPI_TX_EXT 4</b>							
0x840	<a href="#">MIPI_TX_EXT0[7:0]</a>	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-
0x841	<a href="#">MIPI_TX_EXT1[7:0]</a>	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-
0x842	<a href="#">MIPI_TX_EXT2[7:0]</a>	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-
0x843	<a href="#">MIPI_TX_EXT3[7:0]</a>	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-
0x844	<a href="#">MIPI_TX_EXT4[7:0]</a>	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-
0x845	<a href="#">MIPI_TX_EXT5[7:0]</a>	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		-	-
0x846	<a href="#">MIPI_TX_EXT6[7:0]</a>	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		-	-
0x847	<a href="#">MIPI_TX_EXT7[7:0]</a>	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		-	-
0x848	<a href="#">MIPI_TX_EXT8[7:0]</a>	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		-	-
0x849	<a href="#">MIPI_TX_EXT9[7:0]</a>	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		-	-
0x84A	<a href="#">MIPI_TX_EXT10[7:0]</a>	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		-	-
0x84B	<a href="#">MIPI_TX_EXT11[7:0]</a>	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		-	-
0x84C	<a href="#">MIPI_TX_EXT12[7:0]</a>	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		-	-
0x84D	<a href="#">MIPI_TX_EXT13[7:0]</a>	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		-	-
0x84E	<a href="#">MIPI_TX_EXT14[7:0]</a>	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		-	-

ADDRESS	NAME	MSB					LSB
0x84F	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		-	-
<b>MIPI_TX_EXT 5</b>							
0x850	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-
0x851	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-
0x852	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-
0x853	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-
0x854	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-
0x855	MIPI_TX_EXT5[7:0]	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		-	-
0x856	MIPI_TX_EXT6[7:0]	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		-	-
0x857	MIPI_TX_EXT7[7:0]	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		-	-
0x858	MIPI_TX_EXT8[7:0]	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		-	-
0x859	MIPI_TX_EXT9[7:0]	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		-	-
0x85A	MIPI_TX_EXT10[7:0]	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		-	-
0x85B	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		-	-
0x85C	MIPI_TX_EXT12[7:0]	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		-	-
0x85D	MIPI_TX_EXT13[7:0]	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		-	-
0x85E	MIPI_TX_EXT14[7:0]	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		-	-
0x85F	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		-	-
<b>MIPI_TX_EXT 6</b>							
0x860	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-
0x861	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-
0x862	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-
0x863	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-
0x864	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-
0x865	MIPI_TX_EXT5[7:0]	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]		-	-
0x866	MIPI_TX_EXT6[7:0]	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]		-	-
0x867	MIPI_TX_EXT7[7:0]	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]		-	-
0x868	MIPI_TX_EXT8[7:0]	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]		-	-
0x869	MIPI_TX_EXT9[7:0]	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]		-	-
0x86A	MIPI_TX_EXT10[7:0]	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]		-	-
0x86B	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]		-	-
0x86C	MIPI_TX_EXT12[7:0]	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]		-	-
0x86D	MIPI_TX_EXT13[7:0]	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]		-	-
0x86E	MIPI_TX_EXT14[7:0]	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]		-	-
0x86F	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]		-	-
<b>MIPI_TX_EXT 7</b>							
0x870	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]		MAP_DST_0_H[2:0]		-	-
0x871	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]		MAP_DST_1_H[2:0]		-	-
0x872	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]		MAP_DST_2_H[2:0]		-	-
0x873	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]		MAP_DST_3_H[2:0]		-	-
0x874	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]		MAP_DST_4_H[2:0]		-	-

ADDRESS	NAME	MSB						LSB
0x875	<a href="#">MIPI_TX_EXT5[7:0]</a>	MAP_SRC_5_H[2:0]		MAP_DST_5_H[2:0]			-	-
0x876	<a href="#">MIPI_TX_EXT6[7:0]</a>	MAP_SRC_6_H[2:0]		MAP_DST_6_H[2:0]			-	-
0x877	<a href="#">MIPI_TX_EXT7[7:0]</a>	MAP_SRC_7_H[2:0]		MAP_DST_7_H[2:0]			-	-
0x878	<a href="#">MIPI_TX_EXT8[7:0]</a>	MAP_SRC_8_H[2:0]		MAP_DST_8_H[2:0]			-	-
0x879	<a href="#">MIPI_TX_EXT9[7:0]</a>	MAP_SRC_9_H[2:0]		MAP_DST_9_H[2:0]			-	-
0x87A	<a href="#">MIPI_TX_EXT10[7:0]</a>	MAP_SRC_10_H[2:0]		MAP_DST_10_H[2:0]			-	-
0x87B	<a href="#">MIPI_TX_EXT11[7:0]</a>	MAP_SRC_11_H[2:0]		MAP_DST_11_H[2:0]			-	-
0x87C	<a href="#">MIPI_TX_EXT12[7:0]</a>	MAP_SRC_12_H[2:0]		MAP_DST_12_H[2:0]			-	-
0x87D	<a href="#">MIPI_TX_EXT13[7:0]</a>	MAP_SRC_13_H[2:0]		MAP_DST_13_H[2:0]			-	-
0x87E	<a href="#">MIPI_TX_EXT14[7:0]</a>	MAP_SRC_14_H[2:0]		MAP_DST_14_H[2:0]			-	-
0x87F	<a href="#">MIPI_TX_EXT15[7:0]</a>	MAP_SRC_15_H[2:0]		MAP_DST_15_H[2:0]			-	-
<b>MIPI_PHY</b>								
0x8A0	<a href="#">MIPI_PHY0[7:0]</a>	force_csi_out_en	force_clk3_en	force_clk0_en	phy_1x4b_22	phy_1x4a_22	phy_2x4	- phy_4x2
0x8A1	<a href="#">MIPI_PHY1[7:0]</a>	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]
0x8A2	<a href="#">MIPI_PHY2[7:0]</a>		phy_Stby_n[3:0]			t_lpx[1:0]		t_hs_trail[1:0]
0x8A3	<a href="#">MIPI_PHY3[7:0]</a>		phy1_lane_map[3:0]			phy0_lane_map[3:0]		
0x8A4	<a href="#">MIPI_PHY4[7:0]</a>		phy3_lane_map[3:0]			phy2_lane_map[3:0]		
0x8A5	<a href="#">MIPI_PHY5[7:0]</a>	t_clk_prep[1:0]		phy1_pol_map[2:0]		phy0_pol_map[2:0]		
0x8A6	<a href="#">MIPI_PHY6[7:0]</a>	-	-	phy3_pol_map[2:0]		phy2_pol_map[2:0]		
0x8A8	<a href="#">MIPI_PHY8[7:0]</a>	t_lpxesc[2:0]		-	-	-	-	-
0x8A9	<a href="#">MIPI_PHY9[7:0]</a>		phy_cp0[4:0]			-	-	-
0x8AA	<a href="#">MIPI_PHY10[7:0]</a>		phy_cp1[4:0]			-	-	-
0x8AB	<a href="#">MIPI_PHY11[7:0]</a>		phy_cp_err[3:0]		-	-	-	-
0x8AD	<a href="#">MIPI_PHY13[7:0]</a>	-	-		t_t3_prebegin[5:0]			
0x8AE	<a href="#">MIPI_PHY14[7:0]</a>	-		t_t3_post[4:0]			t_t3_prep[1:0]	
0x8C0	<a href="#">MIPI_PRBS_0[7:0]</a>	MIPI_PRBS_EN_P1_LN1[1:0]	MIPI_PRBS_EN_P1_LN0[1:0]	MIPI_PRBS_EN_P0_LN1[1:0]	MIPI_PRBS_EN_P0_LN0[1:0]			
0x8C1	<a href="#">MIPI_PRBS_1[7:0]</a>	MIPI_PRBS_EN_P3_LN1[1:0]	MIPI_PRBS_EN_P3_LN0[1:0]	MIPI_PRBS_EN_P2_LN1[1:0]	MIPI_PRBS_EN_P2_LN0[1:0]			
0x8C3	<a href="#">MIPI_PRBS_3[7:0]</a>	-	-	-	-	-	MIPI_CUSTOM_SEED_2[1:0]	
0x8C4	<a href="#">MIPI_PRBS_4[7:0]</a>			MIPI_CUSTOM_SEED_1[7:0]				
0x8C5	<a href="#">MIPI_PRBS_5[7:0]</a>			MIPI_CUSTOM_SEED_0[7:0]				
0x8C6	<a href="#">MIPI_PHY_15[7:0]</a>		Force_Video_Mask[3:0]			Auto_Mask_En[3:0]		
0x8C7	<a href="#">MIPI_PHY_16[7:0]</a>	-	-	-	-	Video_Mask_Restart_En[3:0]		
0x8C9	<a href="#">MIPI_PHY_18[7:0]</a>	-	-	-	-	RST_MIPI_TX_LOC[3:0]		
0x8D0	<a href="#">MIPI_PHY_19[7:0]</a>		csi2_tx1_pkt_cnt[3:0]			csi2_tx0_pkt_cnt[3:0]		
0x8D1	<a href="#">MIPI_PHY_20[7:0]</a>		csi2_tx3_pkt_cnt[3:0]			csi2_tx2_pkt_cnt[3:0]		
0x8D2	<a href="#">MIPI_PHY_21[7:0]</a>		phy1_pkt_cnt[3:0]			phy0_pkt_cnt[3:0]		
0x8D3	<a href="#">MIPI_PHY_22[7:0]</a>		phy3_pkt_cnt[3:0]			phy2_pkt_cnt[3:0]		

ADDRESS	NAME	MSB							LSB
<b>MIPI_TX 0</b>									
0x901	MIPI_TX1[7:0]								MODE[7:0]
0x902	MIPI_TX2[7:0]								STATUS[7:0]
0x903	MIPI_TX3[7:0]								DESKEW_INIT[7:0]
0x904	MIPI_TX4[7:0]								DESKEW_PER[7:0]
0x905	MIPI_TX5[7:0]								CSI2_T_PRE[7:0]
0x906	MIPI_TX6[7:0]								CSI2_T_POST[7:0]
0x907	MIPI_TX7[7:0]								CSI2_TX_GAP[7:0]
0x908	MIPI_TX8[7:0]								CSI2_TWAKEUP_L[7:0]
0x909	MIPI_TX9[7:0]								CSI2_TWAKEUP_M[7:0]
0x90A	MIPI_TX10[7:0]	CSI2_LANE_CNT[1: 0]	CSI2_CP HY_EN	csi2_vcx _en	-				CSI2_TWAKEUP_H[2:0]
0x90B	MIPI_TX11[7:0]								MAP_EN_L[7:0]
0x90C	MIPI_TX12[7:0]								MAP_EN_H[7:0]
0x90D	MIPI_TX13[7:0]								MAP_SRC_0[7:0]
0x90E	MIPI_TX14[7:0]								MAP_DST_0[7:0]
0x90F	MIPI_TX15[7:0]								MAP_SRC_1[7:0]
0x910	MIPI_TX16[7:0]								MAP_DST_1[7:0]
0x911	MIPI_TX17[7:0]								MAP_SRC_2[7:0]
0x912	MIPI_TX18[7:0]								MAP_DST_2[7:0]
0x913	MIPI_TX19[7:0]								MAP_SRC_3[7:0]
0x914	MIPI_TX20[7:0]								MAP_DST_3[7:0]
0x915	MIPI_TX21[7:0]								MAP_SRC_4[7:0]
0x916	MIPI_TX22[7:0]								MAP_DST_4[7:0]
0x917	MIPI_TX23[7:0]								MAP_SRC_5[7:0]
0x918	MIPI_TX24[7:0]								MAP_DST_5[7:0]
0x919	MIPI_TX25[7:0]								MAP_SRC_6[7:0]
0x91A	MIPI_TX26[7:0]								MAP_DST_6[7:0]
0x91B	MIPI_TX27[7:0]								MAP_SRC_7[7:0]
0x91C	MIPI_TX28[7:0]								MAP_DST_7[7:0]
0x91D	MIPI_TX29[7:0]								MAP_SRC_8[7:0]
0x91E	MIPI_TX30[7:0]								MAP_DST_8[7:0]
0x91F	MIPI_TX31[7:0]								MAP_SRC_9[7:0]
0x920	MIPI_TX32[7:0]								MAP_DST_9[7:0]
0x921	MIPI_TX33[7:0]								MAP_SRC_10[7:0]
0x922	MIPI_TX34[7:0]								MAP_DST_10[7:0]
0x923	MIPI_TX35[7:0]								MAP_SRC_11[7:0]
0x924	MIPI_TX36[7:0]								MAP_DST_11[7:0]
0x925	MIPI_TX37[7:0]								MAP_SRC_12[7:0]
0x926	MIPI_TX38[7:0]								MAP_DST_12[7:0]
0x927	MIPI_TX39[7:0]								MAP_SRC_13[7:0]

ADDRESS	NAME	MSB							LSB
0x928	<a href="#">MIPI_TX40[7:0]</a>							MAP_DST_13[7:0]	
0x929	<a href="#">MIPI_TX41[7:0]</a>							MAP_SRC_14[7:0]	
0x92A	<a href="#">MIPI_TX42[7:0]</a>							MAP_DST_14[7:0]	
0x92B	<a href="#">MIPI_TX43[7:0]</a>							MAP_SRC_15[7:0]	
0x92C	<a href="#">MIPI_TX44[7:0]</a>							MAP_DST_15[7:0]	
0x92D	<a href="#">MIPI_TX45[7:0]</a>	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]				
0x92E	<a href="#">MIPI_TX46[7:0]</a>	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]				
0x92F	<a href="#">MIPI_TX47[7:0]</a>	MAP_DPHY_DEST_11[1:0]	MAP_DPHY_DEST_10[1:0]	MAP_DPHY_DEST_9[1:0]	MAP_DPHY_DEST_8[1:0]				
0x930	<a href="#">MIPI_TX48[7:0]</a>	MAP_DPHY_DEST_15[1:0]	MAP_DPHY_DEST_14[1:0]	MAP_DPHY_DEST_13[1:0]	MAP_DPHY_DEST_12[1:0]				
0x931	<a href="#">MIPI_TX49[7:0]</a>			MAP_CON[7:0]					
0x932	<a href="#">MIPI_TX50[7:0]</a>			SKEW_PER_SEL[7:0]					
0x933	<a href="#">MIPI_TX51[7:0]</a>	-	-	-	ALT2_M EM_MA P8	MODE_DT	ALT_ME M_MAP10	ALT_ME M_MAP8	ALT_ME M_MAP12
0x934	<a href="#">MIPI_TX52[7:0]</a>	video_masked_latched[3:0]					video_masked[3:0]		
<b>MIPI_TX 1</b>									
0x941	<a href="#">MIPI_TX1[7:0]</a>				MODE[7:0]				
0x942	<a href="#">MIPI_TX2[7:0]</a>				STATUS[7:0]				
0x943	<a href="#">MIPI_TX3[7:0]</a>				DESKEW_INIT[7:0]				
0x944	<a href="#">MIPI_TX4[7:0]</a>				DESKEW_PER[7:0]				
0x945	<a href="#">MIPI_TX5[7:0]</a>				CSI2_T_PRE[7:0]				
0x946	<a href="#">MIPI_TX6[7:0]</a>				CSI2_T_POST[7:0]				
0x947	<a href="#">MIPI_TX7[7:0]</a>				CSI2_TX_GAP[7:0]				
0x948	<a href="#">MIPI_TX8[7:0]</a>				CSI2_TWAKEUP_L[7:0]				
0x949	<a href="#">MIPI_TX9[7:0]</a>				CSI2_TWAKEUP_M[7:0]				
0x94A	<a href="#">MIPI_TX10[7:0]</a>	CSI2_LANE_CNT[1:0]	CSI2_CPHY_EN	csi2_vcx_en	-	CSI2_TWAKEUP_H[2:0]			
0x94B	<a href="#">MIPI_TX11[7:0]</a>				MAP_EN_L[7:0]				
0x94C	<a href="#">MIPI_TX12[7:0]</a>				MAP_EN_H[7:0]				
0x94D	<a href="#">MIPI_TX13[7:0]</a>				MAP_SRC_0[7:0]				
0x94E	<a href="#">MIPI_TX14[7:0]</a>				MAP_DST_0[7:0]				
0x94F	<a href="#">MIPI_TX15[7:0]</a>				MAP_SRC_1[7:0]				
0x950	<a href="#">MIPI_TX16[7:0]</a>				MAP_DST_1[7:0]				
0x951	<a href="#">MIPI_TX17[7:0]</a>				MAP_SRC_2[7:0]				
0x952	<a href="#">MIPI_TX18[7:0]</a>				MAP_DST_2[7:0]				
0x953	<a href="#">MIPI_TX19[7:0]</a>				MAP_SRC_3[7:0]				
0x954	<a href="#">MIPI_TX20[7:0]</a>				MAP_DST_3[7:0]				
0x955	<a href="#">MIPI_TX21[7:0]</a>				MAP_SRC_4[7:0]				
0x956	<a href="#">MIPI_TX22[7:0]</a>				MAP_DST_4[7:0]				

ADDRESS	NAME	MSB							LSB
0x957	<a href="#">MIPI_TX23[7:0]</a>							MAP_SRC_5[7:0]	
0x958	<a href="#">MIPI_TX24[7:0]</a>							MAP_DST_5[7:0]	
0x959	<a href="#">MIPI_TX25[7:0]</a>							MAP_SRC_6[7:0]	
0x95A	<a href="#">MIPI_TX26[7:0]</a>							MAP_DST_6[7:0]	
0x95B	<a href="#">MIPI_TX27[7:0]</a>							MAP_SRC_7[7:0]	
0x95C	<a href="#">MIPI_TX28[7:0]</a>							MAP_DST_7[7:0]	
0x95D	<a href="#">MIPI_TX29[7:0]</a>							MAP_SRC_8[7:0]	
0x95E	<a href="#">MIPI_TX30[7:0]</a>							MAP_DST_8[7:0]	
0x95F	<a href="#">MIPI_TX31[7:0]</a>							MAP_SRC_9[7:0]	
0x960	<a href="#">MIPI_TX32[7:0]</a>							MAP_DST_9[7:0]	
0x961	<a href="#">MIPI_TX33[7:0]</a>							MAP_SRC_10[7:0]	
0x962	<a href="#">MIPI_TX34[7:0]</a>							MAP_DST_10[7:0]	
0x963	<a href="#">MIPI_TX35[7:0]</a>							MAP_SRC_11[7:0]	
0x964	<a href="#">MIPI_TX36[7:0]</a>							MAP_DST_11[7:0]	
0x965	<a href="#">MIPI_TX37[7:0]</a>							MAP_SRC_12[7:0]	
0x966	<a href="#">MIPI_TX38[7:0]</a>							MAP_DST_12[7:0]	
0x967	<a href="#">MIPI_TX39[7:0]</a>							MAP_SRC_13[7:0]	
0x968	<a href="#">MIPI_TX40[7:0]</a>							MAP_DST_13[7:0]	
0x969	<a href="#">MIPI_TX41[7:0]</a>							MAP_SRC_14[7:0]	
0x96A	<a href="#">MIPI_TX42[7:0]</a>							MAP_DST_14[7:0]	
0x96B	<a href="#">MIPI_TX43[7:0]</a>							MAP_SRC_15[7:0]	
0x96C	<a href="#">MIPI_TX44[7:0]</a>							MAP_DST_15[7:0]	
0x96D	<a href="#">MIPI_TX45[7:0]</a>	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]				
0x96E	<a href="#">MIPI_TX46[7:0]</a>	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]				
0x96F	<a href="#">MIPI_TX47[7:0]</a>	MAP_DPHY_DEST_11[1:0]	MAP_DPHY_DEST_10[1:0]	MAP_DPHY_DEST_9[1:0]	MAP_DPHY_DEST_8[1:0]				
0x970	<a href="#">MIPI_TX48[7:0]</a>	MAP_DPHY_DEST_15[1:0]	MAP_DPHY_DEST_14[1:0]	MAP_DPHY_DEST_13[1:0]	MAP_DPHY_DEST_12[1:0]				
0x971	<a href="#">MIPI_TX49[7:0]</a>				MAP_CON[7:0]				
0x972	<a href="#">MIPI_TX50[7:0]</a>				SKEW_PER_SEL[7:0]				
0x973	<a href="#">MIPI_TX51[7:0]</a>	-	-	-	ALT2_M_EM_MA_P8	MODE_DT	ALT_ME_M_MAP10	ALT_ME_M_MAP8	ALT_ME_M_MAP12
0x974	<a href="#">MIPI_TX52[7:0]</a>		video_masked_latched[3:0]				video_masked[3:0]		
<b>MIPI_TX 2</b>									
0x981	<a href="#">MIPI_TX1[7:0]</a>						MODE[7:0]		
0x982	<a href="#">MIPI_TX2[7:0]</a>						STATUS[7:0]		
0x983	<a href="#">MIPI_TX3[7:0]</a>						DESKEW_INIT[7:0]		
0x984	<a href="#">MIPI_TX4[7:0]</a>						DESKEW_PER[7:0]		
0x985	<a href="#">MIPI_TX5[7:0]</a>						CSI2_T_PRE[7:0]		
0x986	<a href="#">MIPI_TX6[7:0]</a>						CSI2_T_POST[7:0]		

**PRELIMINARY**

ADDRESS	NAME	MSB							LSB
0x987	<a href="#">MIPI_TX7[7:0]</a>	CSI2_TX_GAP[7:0]							
0x988	<a href="#">MIPI_TX8[7:0]</a>	CSI2_TWAKEUP_L[7:0]							
0x989	<a href="#">MIPI_TX9[7:0]</a>	CSI2_TWAKEUP_M[7:0]							
0x98A	<a href="#">MIPI_TX10[7:0]</a>	CSI2_LANE_CNT[1:0]	CSI2_CPHY_EN	csi2_vcxe_en	-	CSI2_TWAKEUP_H[2:0]			
0x98B	<a href="#">MIPI_TX11[7:0]</a>	MAP_EN_L[7:0]							
0x98C	<a href="#">MIPI_TX12[7:0]</a>	MAP_EN_H[7:0]							
0x98D	<a href="#">MIPI_TX13[7:0]</a>	MAP_SRC_0[7:0]							
0x98E	<a href="#">MIPI_TX14[7:0]</a>	MAP_DST_0[7:0]							
0x98F	<a href="#">MIPI_TX15[7:0]</a>	MAP_SRC_1[7:0]							
0x990	<a href="#">MIPI_TX16[7:0]</a>	MAP_DST_1[7:0]							
0x991	<a href="#">MIPI_TX17[7:0]</a>	MAP_SRC_2[7:0]							
0x992	<a href="#">MIPI_TX18[7:0]</a>	MAP_DST_2[7:0]							
0x993	<a href="#">MIPI_TX19[7:0]</a>	MAP_SRC_3[7:0]							
0x994	<a href="#">MIPI_TX20[7:0]</a>	MAP_DST_3[7:0]							
0x995	<a href="#">MIPI_TX21[7:0]</a>	MAP_SRC_4[7:0]							
0x996	<a href="#">MIPI_TX22[7:0]</a>	MAP_DST_4[7:0]							
0x997	<a href="#">MIPI_TX23[7:0]</a>	MAP_SRC_5[7:0]							
0x998	<a href="#">MIPI_TX24[7:0]</a>	MAP_DST_5[7:0]							
0x999	<a href="#">MIPI_TX25[7:0]</a>	MAP_SRC_6[7:0]							
0x99A	<a href="#">MIPI_TX26[7:0]</a>	MAP_DST_6[7:0]							
0x99B	<a href="#">MIPI_TX27[7:0]</a>	MAP_SRC_7[7:0]							
0x99C	<a href="#">MIPI_TX28[7:0]</a>	MAP_DST_7[7:0]							
0x99D	<a href="#">MIPI_TX29[7:0]</a>	MAP_SRC_8[7:0]							
0x99E	<a href="#">MIPI_TX30[7:0]</a>	MAP_DST_8[7:0]							
0x99F	<a href="#">MIPI_TX31[7:0]</a>	MAP_SRC_9[7:0]							
0x9A0	<a href="#">MIPI_TX32[7:0]</a>	MAP_DST_9[7:0]							
0x9A1	<a href="#">MIPI_TX33[7:0]</a>	MAP_SRC_10[7:0]							
0x9A2	<a href="#">MIPI_TX34[7:0]</a>	MAP_DST_10[7:0]							
0x9A3	<a href="#">MIPI_TX35[7:0]</a>	MAP_SRC_11[7:0]							
0x9A4	<a href="#">MIPI_TX36[7:0]</a>	MAP_DST_11[7:0]							
0x9A5	<a href="#">MIPI_TX37[7:0]</a>	MAP_SRC_12[7:0]							
0x9A6	<a href="#">MIPI_TX38[7:0]</a>	MAP_DST_12[7:0]							
0x9A7	<a href="#">MIPI_TX39[7:0]</a>	MAP_SRC_13[7:0]							
0x9A8	<a href="#">MIPI_TX40[7:0]</a>	MAP_DST_13[7:0]							
0x9A9	<a href="#">MIPI_TX41[7:0]</a>	MAP_SRC_14[7:0]							
0x9AA	<a href="#">MIPI_TX42[7:0]</a>	MAP_DST_14[7:0]							
0x9AB	<a href="#">MIPI_TX43[7:0]</a>	MAP_SRC_15[7:0]							
0x9AC	<a href="#">MIPI_TX44[7:0]</a>	MAP_DST_15[7:0]							
0x9AD	<a href="#">MIPI_TX45[7:0]</a>	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]				

ADDRESS	NAME	MSB						LSB
0x9AE	<a href="#">MIPI_TX46[7:0]</a>	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]			
0x9AF	<a href="#">MIPI_TX47[7:0]</a>	MAP_DPHY_DEST_11[1:0]	MAP_DPHY_DEST_10[1:0]	MAP_DPHY_DEST_9[1:0]	MAP_DPHY_DEST_8[1:0]			
0x9B0	<a href="#">MIPI_TX48[7:0]</a>	MAP_DPHY_DEST_15[1:0]	MAP_DPHY_DEST_14[1:0]	MAP_DPHY_DEST_13[1:0]	MAP_DPHY_DEST_12[1:0]			
0x9B1	<a href="#">MIPI_TX49[7:0]</a>			MAP_CON[7:0]				
0x9B2	<a href="#">MIPI_TX50[7:0]</a>			SKEW_PER_SEL[7:0]				
0x9B3	<a href="#">MIPI_TX51[7:0]</a>	-	-	-	ALT2_ME_M_MAP8	MODE_DT	ALT_ME_M_MAP10	ALT_ME_M_MAP12
0x9B4	<a href="#">MIPI_TX52[7:0]</a>	video_masked_latched[3:0]			video_masked[3:0]			
<b>MIPI_TX 3</b>								
0x9C1	<a href="#">MIPI_TX1[7:0]</a>			MODE[7:0]				
0x9C2	<a href="#">MIPI_TX2[7:0]</a>			STATUS[7:0]				
0x9C3	<a href="#">MIPI_TX3[7:0]</a>			DESKEW_INIT[7:0]				
0x9C4	<a href="#">MIPI_TX4[7:0]</a>			DESKEW_PER[7:0]				
0x9C5	<a href="#">MIPI_TX5[7:0]</a>			CSI2_T_PRE[7:0]				
0x9C6	<a href="#">MIPI_TX6[7:0]</a>			CSI2_T_POST[7:0]				
0x9C7	<a href="#">MIPI_TX7[7:0]</a>			CSI2_TX_GAP[7:0]				
0x9C8	<a href="#">MIPI_TX8[7:0]</a>			CSI2_TWAKEUP_L[7:0]				
0x9C9	<a href="#">MIPI_TX9[7:0]</a>			CSI2_TWAKEUP_M[7:0]				
0x9CA	<a href="#">MIPI_TX10[7:0]</a>	CSI2_LANE_CNT[1:0]	CSI2_CPHY_EN	csi2_vcx_en	-	CSI2_TWAKEUP_H[2:0]		
0x9CB	<a href="#">MIPI_TX11[7:0]</a>			MAP_EN_L[7:0]				
0x9CC	<a href="#">MIPI_TX12[7:0]</a>			MAP_EN_H[7:0]				
0x9CD	<a href="#">MIPI_TX13[7:0]</a>			MAP_SRC_0[7:0]				
0x9CE	<a href="#">MIPI_TX14[7:0]</a>			MAP_DST_0[7:0]				
0x9CF	<a href="#">MIPI_TX15[7:0]</a>			MAP_SRC_1[7:0]				
0x9D0	<a href="#">MIPI_TX16[7:0]</a>			MAP_DST_1[7:0]				
0x9D1	<a href="#">MIPI_TX17[7:0]</a>			MAP_SRC_2[7:0]				
0x9D2	<a href="#">MIPI_TX18[7:0]</a>			MAP_DST_2[7:0]				
0x9D3	<a href="#">MIPI_TX19[7:0]</a>			MAP_SRC_3[7:0]				
0x9D4	<a href="#">MIPI_TX20[7:0]</a>			MAP_DST_3[7:0]				
0x9D5	<a href="#">MIPI_TX21[7:0]</a>			MAP_SRC_4[7:0]				
0x9D6	<a href="#">MIPI_TX22[7:0]</a>			MAP_DST_4[7:0]				
0x9D7	<a href="#">MIPI_TX23[7:0]</a>			MAP_SRC_5[7:0]				
0x9D8	<a href="#">MIPI_TX24[7:0]</a>			MAP_DST_5[7:0]				
0x9D9	<a href="#">MIPI_TX25[7:0]</a>			MAP_SRC_6[7:0]				
0x9DA	<a href="#">MIPI_TX26[7:0]</a>			MAP_DST_6[7:0]				
0x9DB	<a href="#">MIPI_TX27[7:0]</a>			MAP_SRC_7[7:0]				
0x9DC	<a href="#">MIPI_TX28[7:0]</a>			MAP_DST_7[7:0]				
0x9DD	<a href="#">MIPI_TX29[7:0]</a>			MAP_SRC_8[7:0]				

ADDRESS	NAME	MSB							LSB
0x9DE	<a href="#">MIPI_TX30[7:0]</a>								MAP_DST_8[7:0]
0x9DF	<a href="#">MIPI_TX31[7:0]</a>								MAP_SRC_9[7:0]
0x9E0	<a href="#">MIPI_TX32[7:0]</a>								MAP_DST_9[7:0]
0x9E1	<a href="#">MIPI_TX33[7:0]</a>								MAP_SRC_10[7:0]
0x9E2	<a href="#">MIPI_TX34[7:0]</a>								MAP_DST_10[7:0]
0x9E3	<a href="#">MIPI_TX35[7:0]</a>								MAP_SRC_11[7:0]
0x9E4	<a href="#">MIPI_TX36[7:0]</a>								MAP_DST_11[7:0]
0x9E5	<a href="#">MIPI_TX37[7:0]</a>								MAP_SRC_12[7:0]
0x9E6	<a href="#">MIPI_TX38[7:0]</a>								MAP_DST_12[7:0]
0x9E7	<a href="#">MIPI_TX39[7:0]</a>								MAP_SRC_13[7:0]
0x9E8	<a href="#">MIPI_TX40[7:0]</a>								MAP_DST_13[7:0]
0x9E9	<a href="#">MIPI_TX41[7:0]</a>								MAP_SRC_14[7:0]
0x9EA	<a href="#">MIPI_TX42[7:0]</a>								MAP_DST_14[7:0]
0x9EB	<a href="#">MIPI_TX43[7:0]</a>								MAP_SRC_15[7:0]
0x9EC	<a href="#">MIPI_TX44[7:0]</a>								MAP_DST_15[7:0]
0x9ED	<a href="#">MIPI_TX45[7:0]</a>	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]				
0x9EE	<a href="#">MIPI_TX46[7:0]</a>	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]				
0x9EF	<a href="#">MIPI_TX47[7:0]</a>	MAP_DPHY_DEST_11[1:0]	MAP_DPHY_DEST_10[1:0]	MAP_DPHY_DEST_9[1:0]	MAP_DPHY_DEST_8[1:0]				
0x9F0	<a href="#">MIPI_TX48[7:0]</a>	MAP_DPHY_DEST_15[1:0]	MAP_DPHY_DEST_14[1:0]	MAP_DPHY_DEST_13[1:0]	MAP_DPHY_DEST_12[1:0]				
0x9F1	<a href="#">MIPI_TX49[7:0]</a>					MAP_CON[7:0]			
0x9F2	<a href="#">MIPI_TX50[7:0]</a>					SKEW_PER_SEL[7:0]			
0x9F3	<a href="#">MIPI_TX51[7:0]</a>	-	-	-	ALT2_M_EM_MA_P8	MODE_DT	ALT_ME_M_MAP10	ALT_ME_M_MAP8	ALT_ME_M_MAP12
0x9F4	<a href="#">MIPI_TX52[7:0]</a>			video_masked_latched[3:0]			video_masked[3:0]		
<b>MIPI_TX 4</b>									
0xA0B	<a href="#">MIPI_TX11[7:0]</a>						MAP_EN_L[7:0]		
0xA0C	<a href="#">MIPI_TX12[7:0]</a>						MAP_EN_H[7:0]		
0xA0D	<a href="#">MIPI_TX13[7:0]</a>						MAP_SRC_0[7:0]		
0xA0E	<a href="#">MIPI_TX14[7:0]</a>						MAP_DST_0[7:0]		
0xA0F	<a href="#">MIPI_TX15[7:0]</a>						MAP_SRC_1[7:0]		
0xA10	<a href="#">MIPI_TX16[7:0]</a>						MAP_DST_1[7:0]		
0xA11	<a href="#">MIPI_TX17[7:0]</a>						MAP_SRC_2[7:0]		
0xA12	<a href="#">MIPI_TX18[7:0]</a>						MAP_DST_2[7:0]		
0xA13	<a href="#">MIPI_TX19[7:0]</a>						MAP_SRC_3[7:0]		
0xA14	<a href="#">MIPI_TX20[7:0]</a>						MAP_DST_3[7:0]		
0xA15	<a href="#">MIPI_TX21[7:0]</a>						MAP_SRC_4[7:0]		
0xA16	<a href="#">MIPI_TX22[7:0]</a>						MAP_DST_4[7:0]		
0xA17	<a href="#">MIPI_TX23[7:0]</a>						MAP_SRC_5[7:0]		

ADDRESS	NAME	MSB							LSB
0xA18	<a href="#">MIPI_TX24[7:0]</a>							MAP_DST_5[7:0]	
0xA19	<a href="#">MIPI_TX25[7:0]</a>							MAP_SRC_6[7:0]	
0xA1A	<a href="#">MIPI_TX26[7:0]</a>							MAP_DST_6[7:0]	
0xA1B	<a href="#">MIPI_TX27[7:0]</a>							MAP_SRC_7[7:0]	
0xA1C	<a href="#">MIPI_TX28[7:0]</a>							MAP_DST_7[7:0]	
0xA1D	<a href="#">MIPI_TX29[7:0]</a>							MAP_SRC_8[7:0]	
0xA1E	<a href="#">MIPI_TX30[7:0]</a>							MAP_DST_8[7:0]	
0xA1F	<a href="#">MIPI_TX31[7:0]</a>							MAP_SRC_9[7:0]	
0xA20	<a href="#">MIPI_TX32[7:0]</a>							MAP_DST_9[7:0]	
0xA21	<a href="#">MIPI_TX33[7:0]</a>							MAP_SRC_10[7:0]	
0xA22	<a href="#">MIPI_TX34[7:0]</a>							MAP_DST_10[7:0]	
0xA23	<a href="#">MIPI_TX35[7:0]</a>							MAP_SRC_11[7:0]	
0xA24	<a href="#">MIPI_TX36[7:0]</a>							MAP_DST_11[7:0]	
0xA25	<a href="#">MIPI_TX37[7:0]</a>							MAP_SRC_12[7:0]	
0xA26	<a href="#">MIPI_TX38[7:0]</a>							MAP_DST_12[7:0]	
0xA27	<a href="#">MIPI_TX39[7:0]</a>							MAP_SRC_13[7:0]	
0xA28	<a href="#">MIPI_TX40[7:0]</a>							MAP_DST_13[7:0]	
0xA29	<a href="#">MIPI_TX41[7:0]</a>							MAP_SRC_14[7:0]	
0xA2A	<a href="#">MIPI_TX42[7:0]</a>							MAP_DST_14[7:0]	
0xA2B	<a href="#">MIPI_TX43[7:0]</a>							MAP_SRC_15[7:0]	
0xA2C	<a href="#">MIPI_TX44[7:0]</a>							MAP_DST_15[7:0]	
0xA2D	<a href="#">MIPI_TX45[7:0]</a>	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0xA2E	<a href="#">MIPI_TX46[7:0]</a>	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0xA2F	<a href="#">MIPI_TX47[7:0]</a>	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0xA30	<a href="#">MIPI_TX48[7:0]</a>	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0xA31	<a href="#">MIPI_TX49[7:0]</a>	-	-	-	-	MODE_DT	ALT_ME_M_MAP10	ALT_ME_M_MAP8	ALT_ME_M_MAP12
<b>MIPI_TX 5</b>									
0xA4B	<a href="#">MIPI_TX11[7:0]</a>						MAP_EN_L[7:0]		
0xA4C	<a href="#">MIPI_TX12[7:0]</a>						MAP_EN_H[7:0]		
0xA4D	<a href="#">MIPI_TX13[7:0]</a>						MAP_SRC_0[7:0]		
0xA4E	<a href="#">MIPI_TX14[7:0]</a>						MAP_DST_0[7:0]		
0xA4F	<a href="#">MIPI_TX15[7:0]</a>						MAP_SRC_1[7:0]		
0xA50	<a href="#">MIPI_TX16[7:0]</a>						MAP_DST_1[7:0]		
0xA51	<a href="#">MIPI_TX17[7:0]</a>						MAP_SRC_2[7:0]		
0xA52	<a href="#">MIPI_TX18[7:0]</a>						MAP_DST_2[7:0]		
0xA53	<a href="#">MIPI_TX19[7:0]</a>						MAP_SRC_3[7:0]		
0xA54	<a href="#">MIPI_TX20[7:0]</a>						MAP_DST_3[7:0]		

ADDRESS	NAME	MSB							LSB
0xA55	MIPI_TX21[7:0]								MAP_SRC_4[7:0]
0xA56	MIPI_TX22[7:0]								MAP_DST_4[7:0]
0xA57	MIPI_TX23[7:0]								MAP_SRC_5[7:0]
0xA58	MIPI_TX24[7:0]								MAP_DST_5[7:0]
0xA59	MIPI_TX25[7:0]								MAP_SRC_6[7:0]
0xA5A	MIPI_TX26[7:0]								MAP_DST_6[7:0]
0xA5B	MIPI_TX27[7:0]								MAP_SRC_7[7:0]
0xA5C	MIPI_TX28[7:0]								MAP_DST_7[7:0]
0xA5D	MIPI_TX29[7:0]								MAP_SRC_8[7:0]
0xA5E	MIPI_TX30[7:0]								MAP_DST_8[7:0]
0xA5F	MIPI_TX31[7:0]								MAP_SRC_9[7:0]
0xA60	MIPI_TX32[7:0]								MAP_DST_9[7:0]
0xA61	MIPI_TX33[7:0]								MAP_SRC_10[7:0]
0xA62	MIPI_TX34[7:0]								MAP_DST_10[7:0]
0xA63	MIPI_TX35[7:0]								MAP_SRC_11[7:0]
0xA64	MIPI_TX36[7:0]								MAP_DST_11[7:0]
0xA65	MIPI_TX37[7:0]								MAP_SRC_12[7:0]
0xA66	MIPI_TX38[7:0]								MAP_DST_12[7:0]
0xA67	MIPI_TX39[7:0]								MAP_SRC_13[7:0]
0xA68	MIPI_TX40[7:0]								MAP_DST_13[7:0]
0xA69	MIPI_TX41[7:0]								MAP_SRC_14[7:0]
0xA6A	MIPI_TX42[7:0]								MAP_DST_14[7:0]
0xA6B	MIPI_TX43[7:0]								MAP_SRC_15[7:0]
0xA6C	MIPI_TX44[7:0]								MAP_DST_15[7:0]
0xA6D	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]				
0xA6E	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]				
0xA6F	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]	MAP_DPHY_DEST_10[1:0]	MAP_DPHY_DEST_9[1:0]	MAP_DPHY_DEST_8[1:0]				
0xA70	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]	MAP_DPHY_DEST_14[1:0]	MAP_DPHY_DEST_13[1:0]	MAP_DPHY_DEST_12[1:0]				
0xA71	MIPI_TX49[7:0]	-	-	-	-	MODE_DT	ALT_ME_M_MAP10	ALT_ME_M_MAP12	
<b>MIPI_TX 6</b>									
0xA8B	MIPI_TX11[7:0]						MAP_EN_L[7:0]		
0xA8C	MIPI_TX12[7:0]						MAP_EN_H[7:0]		
0xA8D	MIPI_TX13[7:0]						MAP_SRC_0[7:0]		
0xA8E	MIPI_TX14[7:0]						MAP_DST_0[7:0]		
0xA8F	MIPI_TX15[7:0]						MAP_SRC_1[7:0]		
0xA90	MIPI_TX16[7:0]						MAP_DST_1[7:0]		
0xA91	MIPI_TX17[7:0]						MAP_SRC_2[7:0]		

ADDRESS	NAME	MSB							LSB
0xA92	MIPI_TX18[7:0]								MAP_DST_2[7:0]
0xA93	MIPI_TX19[7:0]								MAP_SRC_3[7:0]
0xA94	MIPI_TX20[7:0]								MAP_DST_3[7:0]
0xA95	MIPI_TX21[7:0]								MAP_SRC_4[7:0]
0xA96	MIPI_TX22[7:0]								MAP_DST_4[7:0]
0xA97	MIPI_TX23[7:0]								MAP_SRC_5[7:0]
0xA98	MIPI_TX24[7:0]								MAP_DST_5[7:0]
0xA99	MIPI_TX25[7:0]								MAP_SRC_6[7:0]
0xA9A	MIPI_TX26[7:0]								MAP_DST_6[7:0]
0xA9B	MIPI_TX27[7:0]								MAP_SRC_7[7:0]
0xA9C	MIPI_TX28[7:0]								MAP_DST_7[7:0]
0xA9D	MIPI_TX29[7:0]								MAP_SRC_8[7:0]
0xA9E	MIPI_TX30[7:0]								MAP_DST_8[7:0]
0xA9F	MIPI_TX31[7:0]								MAP_SRC_9[7:0]
0xAA0	MIPI_TX32[7:0]								MAP_DST_9[7:0]
0xAA1	MIPI_TX33[7:0]								MAP_SRC_10[7:0]
0xAA2	MIPI_TX34[7:0]								MAP_DST_10[7:0]
0xAA3	MIPI_TX35[7:0]								MAP_SRC_11[7:0]
0xAA4	MIPI_TX36[7:0]								MAP_DST_11[7:0]
0xAA5	MIPI_TX37[7:0]								MAP_SRC_12[7:0]
0xAA6	MIPI_TX38[7:0]								MAP_DST_12[7:0]
0xAA7	MIPI_TX39[7:0]								MAP_SRC_13[7:0]
0xAA8	MIPI_TX40[7:0]								MAP_DST_13[7:0]
0xAA9	MIPI_TX41[7:0]								MAP_SRC_14[7:0]
0xAAA	MIPI_TX42[7:0]								MAP_DST_14[7:0]
0xAAB	MIPI_TX43[7:0]								MAP_SRC_15[7:0]
0xAAC	MIPI_TX44[7:0]								MAP_DST_15[7:0]
0xAAD	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]				
0AAE	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]				
0AAF	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]	MAP_DPHY_DEST_10[1:0]	MAP_DPHY_DEST_9[1:0]	MAP_DPHY_DEST_8[1:0]				
0xAB0	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]	MAP_DPHY_DEST_14[1:0]	MAP_DPHY_DEST_13[1:0]	MAP_DPHY_DEST_12[1:0]				
0xAB1	MIPI_TX49[7:0]	-	-	-	-	MODE_DT	ALT_ME_M_MAP10	ALT_ME_M_MAP12	
<b>MIPI_TX 7</b>									
0xACB	MIPI_TX11[7:0]						MAP_EN_L[7:0]		
0xACC	MIPI_TX12[7:0]						MAP_EN_H[7:0]		
0ACD	MIPI_TX13[7:0]						MAP_SRC_0[7:0]		
0ACE	MIPI_TX14[7:0]						MAP_DST_0[7:0]		

ADDRESS	NAME	MSB							LSB
0xACF	<a href="#">MIPI_TX15[7:0]</a>								MAP_SRC_1[7:0]
0xAD0	<a href="#">MIPI_TX16[7:0]</a>								MAP_DST_1[7:0]
0xAD1	<a href="#">MIPI_TX17[7:0]</a>								MAP_SRC_2[7:0]
0xAD2	<a href="#">MIPI_TX18[7:0]</a>								MAP_DST_2[7:0]
0xAD3	<a href="#">MIPI_TX19[7:0]</a>								MAP_SRC_3[7:0]
0xAD4	<a href="#">MIPI_TX20[7:0]</a>								MAP_DST_3[7:0]
0xAD5	<a href="#">MIPI_TX21[7:0]</a>								MAP_SRC_4[7:0]
0xAD6	<a href="#">MIPI_TX22[7:0]</a>								MAP_DST_4[7:0]
0xAD7	<a href="#">MIPI_TX23[7:0]</a>								MAP_SRC_5[7:0]
0xAD8	<a href="#">MIPI_TX24[7:0]</a>								MAP_DST_5[7:0]
0xAD9	<a href="#">MIPI_TX25[7:0]</a>								MAP_SRC_6[7:0]
0xADA	<a href="#">MIPI_TX26[7:0]</a>								MAP_DST_6[7:0]
0xADB	<a href="#">MIPI_TX27[7:0]</a>								MAP_SRC_7[7:0]
0xADC	<a href="#">MIPI_TX28[7:0]</a>								MAP_DST_7[7:0]
0xADD	<a href="#">MIPI_TX29[7:0]</a>								MAP_SRC_8[7:0]
0xAE0	<a href="#">MIPI_TX30[7:0]</a>								MAP_DST_8[7:0]
0xAFD	<a href="#">MIPI_TX31[7:0]</a>								MAP_SRC_9[7:0]
0xAE0	<a href="#">MIPI_TX32[7:0]</a>								MAP_DST_9[7:0]
0xAE1	<a href="#">MIPI_TX33[7:0]</a>								MAP_SRC_10[7:0]
0xAE2	<a href="#">MIPI_TX34[7:0]</a>								MAP_DST_10[7:0]
0xAE3	<a href="#">MIPI_TX35[7:0]</a>								MAP_SRC_11[7:0]
0xAE4	<a href="#">MIPI_TX36[7:0]</a>								MAP_DST_11[7:0]
0xAE5	<a href="#">MIPI_TX37[7:0]</a>								MAP_SRC_12[7:0]
0xAE6	<a href="#">MIPI_TX38[7:0]</a>								MAP_DST_12[7:0]
0xAE7	<a href="#">MIPI_TX39[7:0]</a>								MAP_SRC_13[7:0]
0xAE8	<a href="#">MIPI_TX40[7:0]</a>								MAP_DST_13[7:0]
0xAE9	<a href="#">MIPI_TX41[7:0]</a>								MAP_SRC_14[7:0]
0xAEA	<a href="#">MIPI_TX42[7:0]</a>								MAP_DST_14[7:0]
0xAEB	<a href="#">MIPI_TX43[7:0]</a>								MAP_SRC_15[7:0]
0xAEC	<a href="#">MIPI_TX44[7:0]</a>								MAP_DST_15[7:0]
0xAED	<a href="#">MIPI_TX45[7:0]</a>	MAP_DPHY_DEST_3[1:0]	MAP_DPHY_DEST_2[1:0]	MAP_DPHY_DEST_1[1:0]	MAP_DPHY_DEST_0[1:0]				
0xAEE	<a href="#">MIPI_TX46[7:0]</a>	MAP_DPHY_DEST_7[1:0]	MAP_DPHY_DEST_6[1:0]	MAP_DPHY_DEST_5[1:0]	MAP_DPHY_DEST_4[1:0]				
0xAF0	<a href="#">MIPI_TX47[7:0]</a>	MAP_DPHY_DEST_11[1:0]	MAP_DPHY_DEST_10[1:0]	MAP_DPHY_DEST_9[1:0]	MAP_DPHY_DEST_8[1:0]				
0xAF0	<a href="#">MIPI_TX48[7:0]</a>	MAP_DPHY_DEST_15[1:0]	MAP_DPHY_DEST_14[1:0]	MAP_DPHY_DEST_13[1:0]	MAP_DPHY_DEST_12[1:0]				
0xAF1	<a href="#">MIPI_TX49[7:0]</a>	-	-	-	-	MODE_DT	ALT_ME_M_MAP10	ALT_ME_M_MAP12	
<b>GMSL1 A</b>									
0xB02	GMSL1_2[7:0]	-	-	-	-	-	-	-	-

ADDRESS	NAME	MSB							LSB					
0xB04	GMSL1_4[7:0]	-	-	PRBSEN	CC_PORT_SEL[1:0]	-	-	FWDCC_EN						
0xB05	GMSL1_5[7:0]	I2CMET_HOD	NO_RE_M_MST	HVTR_M_ODE	EN_EQ	EQTUNE[3:0]								
0xB06	GMSL1_6[7:0]	HIGHIM_M	MAX_RT_EN	I2C_RT_EN	GPI_CO_MP_EN	GPI_RT_EN	HV_SRC[2:0]							
0xB07	GMSL1_7[7:0]	DBL	DRS	BWS	-	HIBW	HVEN	-	PXL_CRC					
0xB08	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSY_NC_TX	-	PKTCC_EN	CC_CRC_LENGTH[1:0]						
0xB0D	GMSL1_D[7:0]	I2C_LOC_ACK	-	-	-	-	HS_TRACK_FSY_NC	-	-					
0xB0E	GMSL1_E[7:0]	DET_THR[7:0]												
0xB0F	GMSL1_F[7:0]	-	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	-	-	PRBS_TYPE					
0xB10	GMSL1_10[7:0]	RCEG_TYPE[1:0]	RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN						
0xB11	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PR_B[1:0]	RCEG_LO_BST_LEN[1:0]							
0xB12	GMSL1_12[7:0]	UNDER_BST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]	LINE_CRC_EN_GMSL1	-	MAX_RT_ERR_EN	RCEG_ERR_PER_EN						
0xB13	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MOD_E_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN THR_G1[4:0]									
0xB14	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MOD_E	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]									
0xB15	GMSL1_15[7:0]	DET_ERR[7:0]												
0xB16	GMSL1_16[7:0]	PRBS_ERR[7:0]												
0xB17	GMSL1_17[7:0]	-	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	-	-	-					
0xB18	GMSL1_18[7:0]	CC_RETR_CNT[7:0]												
0xB19	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]												
0xB1A	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]												
0xB1B	GMSL1_1B[7:0]	-	-	-	-	LINE_CRC_ERR	-	-						
0xB1C	GMSL1_1C[7:0]	-	-	EOM_EYE_WIDTH[5:0]										
0xB1D	GMSL1_1D[7:0]	-	-	-	UNDER_BOOST_DET	AEQ_BST[3:0]								
0xB20	GMSL1_20[7:0]	CRC_VALUE_0[7:0]												
0xB21	GMSL1_21[7:0]	CRC_VALUE_1[7:0]												
0xB22	GMSL1_22[7:0]	CRC_VALUE_2[7:0]												

ADDRESS	NAME	MSB							LSB					
0xB23	GMSL1_23[7:0]	CRC_VALUE_3[7:0]												
0xB96	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]				-	-	-						
0xBCB	GMSL1_CB[7:0]	-	-	-	-	-	-	-	LOCKED_G1					
<b>GMSL1 B</b>														
0xC02	GMSL1_2[7:0]	-	-	-	-	-	-	-	-					
0xC04	GMSL1_4[7:0]	-	-	PRBSEN	CC_PORT_SEL[1:0]		-	-	FWDCC_EN					
0xC05	GMSL1_5[7:0]	I2CMET_HOD	NO_RE_M_MST	HVTR_M_ODE	EN_EQ	EQTUNE[3:0]								
0xC06	GMSL1_6[7:0]	HIGHIM_M	MAX_RT_EN	I2C_RT_EN	GPI_CO_MP_EN	GPI_RT_EN	HV_SRC[2:0]							
0xC07	GMSL1_7[7:0]	DBL	DRS	BWS	-	HIBW	HVEN	-	PXL_CR_C					
0xC08	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSY_NC_TX	-	PKTCC_EN	CC_CRC_LENGTH[1:0]						
0xC0D	GMSL1_D[7:0]	I2C_LOC_ACK	-	-	-	-	HS_TRA_CK_FSY_NC	-	-					
0xC0E	GMSL1_E[7:0]	DET_THR[7:0]												
0xC0F	GMSL1_F[7:0]	-	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	-	-	PRBS_TYPE					
0xC10	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]			RCEG_EN						
0xC11	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PR_B[1:0]		RCEG_LO_BST_LEN[1:0]						
0xC12	GMSL1_12[7:0]	UNDER_BST_DET_EN	CC_CRC_ERR_E_N	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	-	MAX_RT_ERR_E_N	RCEG_E_RR_PER_EN					
0xC13	GMSL1_13[7:0]	EOM_EN_G1	EOM_PEMOD_E_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN THR_G1[4:0]									
0xC14	GMSL1_14[7:0]	AEQ_EN	AEQ_PEMOD_E	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]									
0xC15	GMSL1_15[7:0]	DET_ERR[7:0]												
0xC16	GMSL1_16[7:0]	PRBS_ERR[7:0]												
0xC17	GMSL1_17[7:0]	-	MAX_RT_ERR_I2C	PRBS_O_K	GPI_IN	MAX_RT_ERR_GPI	-	-	-					
0xC18	GMSL1_18[7:0]	CC_RETRO_CNT[7:0]												
0xC19	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]												
0xC1A	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]												
0xC1B	GMSL1_1B[7:0]	-	-	-	-	-	LINE_CRC_ERR	-	-					
0xC1C	GMSL1_1C[7:0]	-	-	EOM_EYE_WIDTH[5:0]										

ADDRESS	NAME	MSB							LSB					
0xC1D	GMSL1_1D[7:0]	-	-	-	UNDER BOOST_DET	AEQ_BST[3:0]								
0xC20	GMSL1_20[7:0]	CRC_VALUE_0[7:0]				CRC_VALUE_1[7:0]								
0xC21	GMSL1_21[7:0]	CRC_VALUE_2[7:0]				CRC_VALUE_3[7:0]								
0xC22	GMSL1_22[7:0]	CONV_GMSL1_DATATYPE[4:0]				-	-	-						
0xC23	GMSL1_23[7:0]	PRBSEN				CC_PORT_SEL[1:0]								
0xC96	GMSL1_96[7:0]	EN_EQ				EQTUNE[3:0]								
0xCCB	GMSL1_CB[7:0]	-	-	-	-	-	-	-	LOCKED_G1					
<b>GMSL1 C</b>														
0xD02	GMSL1_2[7:0]	-	-	-	-	-	-	-	-					
0xD04	GMSL1_4[7:0]	-	-	PRBSEN	CC_PORT_SEL[1:0]		-	-	FWDCC_EN					
0xD05	GMSL1_5[7:0]	I2CMET_HOD	NO_RE_M_MST	HVTR_M_ODE	EN_EQ	EQTUNE[3:0]								
0xD06	GMSL1_6[7:0]	HIGHIM_M	MAX_RT_EN	I2C_RT_EN	GPI_CO_MP_EN	GPI_RT_EN	HV_SRC[2:0]							
0xD07	GMSL1_7[7:0]	DBL	DRS	BWS	-	HIBW	HVEN	-	PXL_CRC					
0xD08	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSY_NC_TX	-	PKTCC_EN	CC_CRC_LENGTH[1:0]						
0xD0D	GMSL1_D[7:0]	I2C_LOC_ACK	-	-	-	-	HS_TRACK_FSY_NC	-	-					
0xD0E	GMSL1_E[7:0]	DET_THR[7:0]												
0xD0F	GMSL1_F[7:0]	-	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	-	-	PRBS_TYPE					
0xD10	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]			RCEG_EN						
0xD11	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PR_B[1:0]	RCEG_LO_BST_LEN[1:0]							
0xD12	GMSL1_12[7:0]	UNDER_BST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	-	MAX_RT_ERR_EN	RCEG_ERR_PER_EN					
0xD13	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MOD_E_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN THR_G1[4:0]									
0xD14	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MOD_E	AEQ_MAN_TRG_REQ	EOM_PER THR[4:0]									
0xD15	GMSL1_15[7:0]	DET_ERR[7:0]												
0xD16	GMSL1_16[7:0]	PRBS_ERR[7:0]												
0xD17	GMSL1_17[7:0]	-	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	-	-	-					

ADDRESS	NAME	MSB							LSB				
0xD18	GMSL1_18[7:0]	CC_RETR_CNT[7:0]											
0xD19	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]											
0xD1A	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]											
0xD1B	GMSL1_1B[7:0]	-	-	-	-	-	LINE_C RC_ERR	-	-				
0xD1C	GMSL1_1C[7:0]	-	-	EOM_EYE_WIDTH[5:0]									
0xD1D	GMSL1_1D[7:0]	-	-	-	UNDER BOOST DET	AEQ_BST[3:0]							
0xD20	GMSL1_20[7:0]	CRC_VALUE_0[7:0]											
0xD21	GMSL1_21[7:0]	CRC_VALUE_1[7:0]											
0xD22	GMSL1_22[7:0]	CRC_VALUE_2[7:0]											
0xD23	GMSL1_23[7:0]	CRC_VALUE_3[7:0]											
0xD96	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					-	-	-				
0xDCB	GMSL1_CB[7:0]	-	-	-	-	-	-	-	LOCKED _G1				
<b>GMSL1 D</b>													
0xE02	GMSL1_2[7:0]	-	-	-	-	-	-	-	-				
0xE04	GMSL1_4[7:0]	-	-	PRBSEN	CC_PORT_SEL[1:0]		-	-	FWDCC EN				
0xE05	GMSL1_5[7:0]	I2CMET HOD	NO_RE M_MST	HVTR_M ODE	EN_EQ	EQTUNE[3:0]							
0xE06	GMSL1_6[7:0]	HIGHIM M	MAX_RT _EN	I2C_RT_ EN	GPI_CO MP_EN	GPI_RT_ EN	HV_SRC[2:0]						
0xE07	GMSL1_7[7:0]	DBL	DRS	BWS	-	HIBW	HVEN	-	PXL_CR C				
0xE08	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSY NC_TX	-	PKTCC EN	CC_CRC_LENGTH[ 1:0]					
0xE0D	GMSL1_D[7:0]	I2C_LOC _ACK	-	-	-	-	HS_TRA CK_FSY NC	-	-				
0xE0E	GMSL1_E[7:0]	DET_THR[7:0]											
0xE0F	GMSL1_F[7:0]	-	EN_DE_ FILT	EN_HS_ FILT	EN_VS_ FILT	DE_EN	-	-	PRBS_T YPE				
0xE10	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_B OUND	RCEG_ERR_NUM[3:0]			RCEG_E N					
0xE11	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PR B[1:0]	RCEG_LO_BST_LE N[1:0]						
0xE12	GMSL1_12[7:0]	UNDER BST_DE T_EN	CC_CRC _ERR_E N	LINE_CRC_LOC[1:0]		LINE_C RC_EN GMSL1	-	MAX_RT _ERR_E N	RCEG_E RR_PER _EN				
0xE13	GMSL1_13[7:0]	EOM_E N_G1	EOM_PE R_MOD E_G1	EOM_M AN_TRG _REQ_G 1	EOM_MIN THR_G1[4:0]								

ADDRESS	NAME	MSB							LSB			
0xE14	GMSL1_14[7:0]	AEQ_EN	AEQ_PE R_MOD E	AEQ_MA N_TRG_ REQ	EOM_PER_THR[4:0]							
0xE15	GMSL1_15[7:0]				DET_ERR[7:0]							
0xE16	GMSL1_16[7:0]				PRBS_ERR[7:0]							
0xE17	GMSL1_17[7:0]	-	MAX_RT _ERR_I2 C	PRBS_O K	GPI_IN	MAX_RT _ERR_G PI	-	-	-			
0xE18	GMSL1_18[7:0]				CC_RETR_CNT[7:0]							
0xE19	GMSL1_19[7:0]				CC_CRC_ERRCNT[7:0]							
0xE1A	GMSL1_1A[7:0]				RCEG_ERR_CNT[7:0]							
0xE1B	GMSL1_1B[7:0]	-	-	-	-	-	LINE_C RC_ERR	-	-			
0xE1C	GMSL1_1C[7:0]	-	-		EOM_EYE_WIDTH[5:0]							
0xE1D	GMSL1_1D[7:0]	-	-	-	UNDER BOOST_ DET		AEQ_BST[3:0]					
0xE20	GMSL1_20[7:0]				CRC_VALUE_0[7:0]							
0xE21	GMSL1_21[7:0]				CRC_VALUE_1[7:0]							
0xE22	GMSL1_22[7:0]				CRC_VALUE_2[7:0]							
0xE23	GMSL1_23[7:0]				CRC_VALUE_3[7:0]							
0xE96	GMSL1_96[7:0]				CONV_GMSL1_DATATYPE[4:0]			-	-			
0xECB	GMSL1_CB[7:0]	-	-	-	-	-	-	-	LOCKED _G1			
<b>GMSL A</b>												
0x1001	TX1[7:0]	-	-	-	ERRG_E N	-	-	-	-			
0x1002	TX2[7:0]		ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]		ERRG_P ER			
0x1003	TX3[7:0]	-	-	-	-	-	TIMEOUT[2:0]					
0x1004	RX0[7:0]		PKT_CNT_LBW[1:0]		-	-	PKT_CNT_SEL[3:0]					
0x1008	GPIOA[7:0]	-	-		GPIO_FWD_CDLY[5:0]							
0x1009	GPIOB[7:0]		GPIO_TX_WNDW[1: 0]		GPIO_REV_CDLY[5:0]							
<b>GMSL B</b>												
0x1011	TX1[7:0]	-	-	-	ERRG_E N	-	-	-	-			
0x1012	TX2[7:0]		ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]		ERRG_P ER			
0x1013	TX3[7:0]	-	-	-	-	-	TIMEOUT[2:0]					
0x1014	RX0[7:0]		PKT_CNT_LBW[1:0]		-	-	PKT_CNT_SEL[3:0]					
0x1018	GPIOA[7:0]	-	-		GPIO_FWD_CDLY[5:0]							
0x1019	GPIOB[7:0]		GPIO_TX_WNDW[1: 0]		GPIO_REV_CDLY[5:0]							

ADDRESS	NAME	MSB							LSB
<b>GMSL C</b>									
0x1021	<u>TX1[7:0]</u>	-	-	-	ERRG_EN	-	-	-	-
0x1022	<u>TX2[7:0]</u>		ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]		ERRG_P_E_R
0x1023	<u>TX3[7:0]</u>	-	-	-	-	-		TIMEOUT[2:0]	
0x1024	<u>RX0[7:0]</u>		PKT_CNT_LBW[1:0]		-	-		PKT_CNT_SEL[3:0]	
0x1028	<u>GPIOA[7:0]</u>	-	-				GPIO_FWD_CDLY[5:0]		
0x1029	<u>GPIOB[7:0]</u>		GPIO_TX_WNDW[1:0]				GPIO_REV_CDLY[5:0]		
<b>GMSL D</b>									
0x1031	<u>TX1[7:0]</u>	-	-	-	ERRG_EN	-	-	-	-
0x1032	<u>TX2[7:0]</u>		ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]		ERRG_P_E_R
0x1033	<u>TX3[7:0]</u>	-	-	-	-	-		TIMEOUT[2:0]	
0x1034	<u>RX0[7:0]</u>		PKT_CNT_LBW[1:0]		-	-		PKT_CNT_SEL[3:0]	
0x1038	<u>GPIOA[7:0]</u>	-	-				GPIO_FWD_CDLY[5:0]		
0x1039	<u>GPIOB[7:0]</u>		GPIO_TX_WNDW[1:0]				GPIO_REV_CDLY[5:0]		
<b>VRX_PATGEN_0 0</b>									
0x1050	<u>PATGEN_0[7:0]</u>	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
0x1051	<u>PATGEN_1[7:0]</u>	GRAD_MODE	-	PATGEN_MODE[1:0]	-	-	-	VS_TRI_G	
0x1052	<u>VS_DLY_2[7:0]</u>				VS_DLY_2[7:0]				
0x1053	<u>VS_DLY_1[7:0]</u>				VS_DLY_1[7:0]				
0x1054	<u>VS_DLY_0[7:0]</u>				VS_DLY_0[7:0]				
0x1055	<u>VS_HIGH_2[7:0]</u>				VS_HIGH_2[7:0]				
0x1056	<u>VS_HIGH_1[7:0]</u>				VS_HIGH_1[7:0]				
0x1057	<u>VS_HIGH_0[7:0]</u>				VS_HIGH_0[7:0]				
0x1058	<u>VS_LOW_2[7:0]</u>				VS_LOW_2[7:0]				
0x1059	<u>VS_LOW_1[7:0]</u>				VS_LOW_1[7:0]				
0x105A	<u>VS_LOW_0[7:0]</u>				VS_LOW_0[7:0]				
0x105B	<u>V2H_2[7:0]</u>				V2H_2[7:0]				
0x105C	<u>V2H_1[7:0]</u>				V2H_1[7:0]				
0x105D	<u>V2H_0[7:0]</u>				V2H_0[7:0]				
0x105E	<u>HS_HIGH_1[7:0]</u>				HS_HIGH_1[7:0]				
0x105F	<u>HS_HIGH_0[7:0]</u>				HS_HIGH_0[7:0]				
0x1060	<u>HS_LOW_1[7:0]</u>				HS_LOW_1[7:0]				
0x1061	<u>HS_LOW_0[7:0]</u>				HS_LOW_0[7:0]				
0x1062	<u>HS_CNT_1[7:0]</u>				HS_CNT_1[7:0]				
0x1063	<u>HS_CNT_0[7:0]</u>				HS_CNT_0[7:0]				
0x1064	<u>V2D_2[7:0]</u>				V2D_2[7:0]				

ADDRESS	NAME	MSB							LSB
0x1065	V2D_1[7:0]								V2D_1[7:0]
0x1066	V2D_0[7:0]								V2D_0[7:0]
0x1067	DE_HIGH_1[7:0]								DE_HIGH_1[7:0]
0x1068	DE_HIGH_0[7:0]								DE_HIGH_0[7:0]
0x1069	DE_LOW_1[7:0]								DE_LOW_1[7:0]
0x106A	DE_LOW_0[7:0]								DE_LOW_0[7:0]
0x106B	DE_CNT_1[7:0]								DE_CNT_1[7:0]
0x106C	DE_CNT_0[7:0]								DE_CNT_0[7:0]
0x106D	GRAD_INCR[7:0]								GRAD_INCR[7:0]
0x106E	CHKR_COLOR_A_L[7:0]								CHKR_COLOR_A_L[7:0]
0x106F	CHKR_COLOR_A_M[7:0]								CHKR_COLOR_A_M[7:0]
0x1070	CHKR_COLOR_A_H[7:0]								CHKR_COLOR_A_H[7:0]
0x1071	CHKR_COLOR_B_L[7:0]								CHKR_COLOR_B_L[7:0]
0x1072	CHKR_COLOR_B_M[7:0]								CHKR_COLOR_B_M[7:0]
0x1073	CHKR_COLOR_B_H[7:0]								CHKR_COLOR_B_H[7:0]
0x1074	CHKR_RPT_A[7:0]								CHKR_RPT_A[7:0]
0x1075	CHKR_RPT_B[7:0]								CHKR_RPT_B[7:0]
0x1076	CHKR_ALT[7:0]								CHKR_ALT[7:0]
<b>VRX_PATGEN_0 1</b>									
0x1080	PATGEN_0[7:0]	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
0x1081	PATGEN_1[7:0]	GRAD_MODE	-	PATGEN_MODE[1:0]	-	-	-	-	VS_TRI_G
0x1082	VS_DLY_2[7:0]				VS_DLY_2[7:0]				
0x1083	VS_DLY_1[7:0]				VS_DLY_1[7:0]				
0x1084	VS_DLY_0[7:0]				VS_DLY_0[7:0]				
0x1085	VS_HIGH_2[7:0]				VS_HIGH_2[7:0]				
0x1086	VS_HIGH_1[7:0]				VS_HIGH_1[7:0]				
0x1087	VS_HIGH_0[7:0]				VS_HIGH_0[7:0]				
0x1088	VS_LOW_2[7:0]				VS_LOW_2[7:0]				
0x1089	VS_LOW_1[7:0]				VS_LOW_1[7:0]				
0x108A	VS_LOW_0[7:0]				VS_LOW_0[7:0]				
0x108B	V2H_2[7:0]				V2H_2[7:0]				
0x108C	V2H_1[7:0]				V2H_1[7:0]				
0x108D	V2H_0[7:0]				V2H_0[7:0]				
0x108E	HS_HIGH_1[7:0]				HS_HIGH_1[7:0]				
0x108F	HS_HIGH_0[7:0]				HS_HIGH_0[7:0]				
0x1090	HS_LOW_1[7:0]				HS_LOW_1[7:0]				

ADDRESS	NAME	MSB							LSB
0x1091	HS_LOW_0[7:0]								HS_LOW_0[7:0]
0x1092	HS_CNT_1[7:0]								HS_CNT_1[7:0]
0x1093	HS_CNT_0[7:0]								HS_CNT_0[7:0]
0x1094	V2D_2[7:0]								V2D_2[7:0]
0x1095	V2D_1[7:0]								V2D_1[7:0]
0x1096	V2D_0[7:0]								V2D_0[7:0]
0x1097	DE_HIGH_1[7:0]								DE_HIGH_1[7:0]
0x1098	DE_HIGH_0[7:0]								DE_HIGH_0[7:0]
0x1099	DE_LOW_1[7:0]								DE_LOW_1[7:0]
0x109A	DE_LOW_0[7:0]								DE_LOW_0[7:0]
0x109B	DE_CNT_1[7:0]								DE_CNT_1[7:0]
0x109C	DE_CNT_0[7:0]								DE_CNT_0[7:0]
0x109D	GRAD_INCR[7:0]								GRAD_INCR[7:0]
0x109E	CHKR_COLOR_A_L[7:0]								CHKR_COLOR_A_L[7:0]
0x109F	CHKR_COLOR_A_M[7:0]								CHKR_COLOR_A_M[7:0]
0x10A0	CHKR_COLOR_A_H[7:0]								CHKR_COLOR_A_H[7:0]
0x10A1	CHKR_COLOR_B_L[7:0]								CHKR_COLOR_B_L[7:0]
0x10A2	CHKR_COLOR_B_M[7:0]								CHKR_COLOR_B_M[7:0]
0x10A3	CHKR_COLOR_B_H[7:0]								CHKR_COLOR_B_H[7:0]
0x10A4	CHKR_RPT_A[7:0]								CHKR_RPT_A[7:0]
0x10A5	CHKR_RPT_B[7:0]								CHKR_RPT_B[7:0]
0x10A6	CHKR_ALT[7:0]								CHKR_ALT[7:0]
<b>VID_PXL_CRC_ERR</b>									
0x11D0	CNT_AX[7:0]								VID_PXL_CRC_ERR_AX[7:0]
0x11D1	CNT_AY[7:0]								VID_PXL_CRC_ERR_AY[7:0]
0x11D2	CNT_AZ[7:0]								VID_PXL_CRC_ERR_AZ[7:0]
0x11E0	CNT_AU[7:0]								VID_PXL_CRC_ERR_AU[7:0]
0x11E1	CNT_BX[7:0]								VID_PXL_CRC_ERR_BX[7:0]
0x11E2	CNT_BY[7:0]								VID_PXL_CRC_ERR_BY[7:0]
0x11E3	CNT_BZ[7:0]								VID_PXL_CRC_ERR_BZ[7:0]
0x11E4	CNT_BU[7:0]								VID_PXL_CRC_ERR_BU[7:0]
0x11E5	CNT_CX[7:0]								VID_PXL_CRC_ERR_CX[7:0]
0x11E6	CNT_CY[7:0]								VID_PXL_CRC_ERR_CY[7:0]
0x11E7	CNT_CZ[7:0]								VID_PXL_CRC_ERR_CZ[7:0]
0x11E8	CNT_CU[7:0]								VID_PXL_CRC_ERR_CU[7:0]
0x11E9	CNT_DX[7:0]								VID_PXL_CRC_ERR_DX[7:0]
0x11EA	CNT_DY[7:0]								VID_PXL_CRC_ERR_DY[7:0]

ADDRESS	NAME	MSB							LSB
0x11EB	CNT_DZ[7:0]	VID_PXL_CRC_ERR_DZ[7:0]							
0x11EC	CNT_DU[7:0]	VID_PXL_CRC_ERR_DU[7:0]							
<b>VID_HVD_DET</b>									
0x11F0	DE_DET[7:0]	DE_DET_7	DE_DET_6	DE_DET_5	DE_DET_4	DE_DET_3	DE_DET_2	DE_DET_1	DE_DET_0
0x11F1	HS_DET[7:0]	HS_DET_7	HS_DET_6	HS_DET_5	HS_DET_4	HS_DET_3	HS_DET_2	HS_DET_1	HS_DET_0
0x11F2	VS_DET[7:0]	VS_DET_7	VS_DET_6	VS_DET_5	VS_DET_4	VS_DET_3	VS_DET_2	VS_DET_1	VS_DET_0
0x11F3	HS_POL[7:0]	HS_POL_7	HS_POL_6	HS_POL_5	HS_POL_4	HS_POL_3	HS_POL_2	HS_POL_1	HS_POL_0
0x11F4	VS_POL[7:0]	VS_POL_7	VS_POL_6	VS_POL_5	VS_POL_4	VS_POL_3	VS_POL_2	VS_POL_1	VS_POL_0
<b>WM</b>									
0x1200	WM_0[7:0]	WM_LE_N	WM_MODE[2:0]			WM_DET[1:0]		-	WM_EN
0x1201	WM_1[7:0]	-	-	WM_KO[1:0]		-	-	-	-
0x1202	WM_2[7:0]	-	-	-	-	HsyncPo_I	VsyncPol	WM_NPFILT[1:0]	
0x1203	WM_3[7:0]	-	WM_TH[6:0]						
0x1204	WM_4[7:0]	-	-	WM_YUV_IN[1:0]		WM_CO_LORADJ	-	WM_MASKMODE[1:0]	
0x1205	WM_5[7:0]	-	-	-	-	-	-	WM_DE_TOUT	WM_ER_ROR
0x1206	WM_6[7:0]	WM_TIMER[7:0]							
0x121E	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x121F	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
<b>WM1</b>									
0x1220	WM_0[7:0]	WM1_LE_N	WM1_MODE[2:0]			WM1_DET[1:0]		-	WM1_E_N
0x1221	WM_1[7:0]	-	-	WM1_KO[1:0]		-	-	-	-
0x1222	WM_2[7:0]	-	-	-	-	HsyncPo_I1	VsyncPol_1	-	-
0x1224	WM_4[7:0]	-	-	WM1_YUV_IN[1:0]		WM1_COLORA_DJ	-	WM1_MASKMODE[1:0]	
0x1225	WM_5[7:0]	-	-	-	-	-	-	WM1_DE_TOUT	WM1_E_RROR
0x1226	WM_6[7:0]	WM1_TIMER[7:0]							
0x123E	WM_WREN_0[7:0]	WM1_WREN_L[7:0]							
0x123F	WM_WREN_1[7:0]	WM1_WREN_H[7:0]							
<b>MEM_ECC</b>									
0x1250	MEM_ECC0[7:0]	MEM_ECC_ERR2THR[2:0]			MEM_ECC_ERR1THR[2:0]			RESET_MEM_E_CC_ERR2_CNT	RESET_MEM_E_CC_ERR1_CNT

ADDRESS	NAME	MSB							LSB			
0x1251	<a href="#">MEM_ECC1[7:0]</a>	MEM_ECC_ERR1_CNT[7:0]										
0x1252	<a href="#">MEM_ECC2[7:0]</a>	MEM_ECC_ERR2_CNT[7:0]										
0x1253	<a href="#">MEM_ECC_ERR_DEB UG[7:0]</a>	-	-	-	-	-	-	MEM_IN J_E2A	MEM_IN J_E1A			
0x1254	<a href="#">MEM_ECC_ERR_FLAG [7:0]</a>	BACKTO P8_ECC _ERR_F LAG	BACKTO P7_ECC _ERR_F LAG	BACKTO P6_ECC _ERR_F LAG	BACKTO P5_ECC _ERR_F LAG	BACKTO P4_ECC _ERR_F LAG	BACKTO P3_ECC _ERR_F LAG	BACKTO P2_ECC _ERR_F LAG	BACKTO P1_ECC _ERR_F LAG			
<b>SPARE_SIGNALS</b>												
0x12A1	<a href="#">SPARE_DIGITAL[7:0]</a>	-	-	-	-	-	-	RESET_ MEM_FL USH	BACKTO P_ECC_ ERR_SE L			
<b>RLMS A</b>												
0x1403	<a href="#">RLMS3[7:0]</a>	AdaptEn	-	-	-	-	-	-	-			
0x1404	<a href="#">RLMS4[7:0]</a>	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0 ]	EOM_PE R_MOD E	EOM_E N				
0x1405	<a href="#">RLMS5[7:0]</a>	EOM_M AN_TRG _REQ	EOM_MIN_THR[6:0]									
0x1406	<a href="#">RLMS6[7:0]</a>	EOM_PV _MODE	EOM_RST_THR[6:0]									
0x1407	<a href="#">RLMS7[7:0]</a>	EOM_D ONE	EOM[6:0]									
0x1434	<a href="#">RLMS34[7:0]</a>	EyeMonPerCntL[7:0]										
0x1435	<a href="#">RLMS35[7:0]</a>	EyeMonPerCntH[7:0]										
0x1437	<a href="#">RLMS37[7:0]</a>	-	-	-	EyeMon Done	EyeMon CntClr	EyeMon Start	EyeMon Ph	EyeMon DPol			
0x1438	<a href="#">RLMS38[7:0]</a>	EyeMonErrCntL[7:0]										
0x1439	<a href="#">RLMS39[7:0]</a>	EyeMonErrCntH[7:0]										
0x143A	<a href="#">RLMS3A[7:0]</a>	EyeMonValCntL[7:0]										
0x143B	<a href="#">RLMS3B[7:0]</a>	EyeMonValCntH[7:0]										
0x143D	<a href="#">RLMS3D[7:0]</a>	ErrChPh[6:0]							ErrChPh TogEn			
0x143E	<a href="#">RLMS3E[7:0]</a>	ErrChPh SecTA	ErrChPhSec[6:0]									
0x143F	<a href="#">RLMS3F[7:0]</a>	ErrChPh PriTA	ErrChPhPri[6:0]									
0x1445	<a href="#">RLMS45[7:0]</a>	RSVD	RSVD	-	-	-	RSVD[2:0]					
0x1449	<a href="#">RLMS49[7:0]</a>	-	-	-	-	-	ErrChPw rUp	-	-			
0x1458	<a href="#">RLMS58[7:0]</a>	-	ErrChVTh1[6:0]									
0x1459	<a href="#">RLMS59[7:0]</a>	-	ErrChVTh0[6:0]									
0x1464	<a href="#">RLMS64[7:0]</a>	-	-	-	-	-	-	TxSSCMode[1:0]				
0x1470	<a href="#">RLMS70[7:0]</a>	-	TxSSCFrqCtrl[6:0]									

ADDRESS	NAME	MSB							LSB			
0x1471	<a href="#">RLMS71[7:0]</a>	-	TxSSCCenSprSt[5:0]						TxSSCEn			
0x1472	<a href="#">RLMS72[7:0]</a>	TxSSCPresClL[7:0]										
0x1473	<a href="#">RLMS73[7:0]</a>	-	-	-	-	-	TxSSCPresClH[2:0]					
0x1474	<a href="#">RLMS74[7:0]</a>	TxSSCPH[7:0]										
0x1475	<a href="#">RLMS75[7:0]</a>	-	TxSSCPH[6:0]									
0x1476	<a href="#">RLMS76[7:0]</a>	-	-	-	-	-	-	TxSSCPHQuad[1:0]				
0x1495	<a href="#">RLMS95[7:0]</a>	TxAmpL ManEn	-	-	-	-	-	-	-			
0x14A4	<a href="#">RLMSA4[7:0]</a>	AEQ_PER_MULT[1: 0]		AEQ_PER[5:0]								
0x14AC	<a href="#">RLMSAC[7:0]</a>	ErrChPh SecTAF R3G	ErrChPhSecFR3G[6:0]									
0x14AD	<a href="#">RLMSAD[7:0]</a>	ErrChPh PriTAFR 3G	ErrChPhPriFR3G[6:0]									
0x14B6	<a href="#">RLMSB6[7:0]</a>	ErrChPh SecTAS RG1875	ErrChPhSecSRG1875[6:0]									
0x14B7	<a href="#">RLMSB7[7:0]</a>	ErrChPh PriTASR G1875	ErrChPhPriSRG1875[6:0]									
0x14C4	<a href="#">RLMSC4[7:0]</a>	-	-	-	-	-	RevFast	-	-			
0x14C5	<a href="#">RLMSC5[7:0]</a>	RevLen ManEn	RevFLenMan[6:0]									
0x14D1	<a href="#">RLMSD1[7:0]</a>	RSVD[2:0]			RSVD[2:0]			RSVD	RSVD			
<b>RLMS B</b>												
0x1503	<a href="#">RLMS3[7:0]</a>	AdaptEn	-	-	-	-	-	-	-			
0x1504	<a href="#">RLMS4[7:0]</a>	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]	EOM_PE R_MOD E	EOM_E N				
0x1505	<a href="#">RLMS5[7:0]</a>	EOM_M AN_TRG _REQ	EOM_MIN_THR[6:0]									
0x1506	<a href="#">RLMS6[7:0]</a>	EOM_PV _MODE	EOM_RST_THR[6:0]									
0x1507	<a href="#">RLMS7[7:0]</a>	EOM_D ONE	EOM[6:0]									
0x1534	<a href="#">RLMS34[7:0]</a>	EyeMonPerCntL[7:0]										
0x1535	<a href="#">RLMS35[7:0]</a>	EyeMonPerCntH[7:0]										
0x1537	<a href="#">RLMS37[7:0]</a>	-	-	-	EyeMon Done	EyeMon CntClr	EyeMon Start	EyeMon Ph	EyeMon DPol			
0x1538	<a href="#">RLMS38[7:0]</a>	EyeMonErrCntL[7:0]										
0x1539	<a href="#">RLMS39[7:0]</a>	EyeMonErrCntH[7:0]										
0x153A	<a href="#">RLMS3A[7:0]</a>	EyeMonValCntL[7:0]										

ADDRESS	NAME	MSB							LSB			
0x153B	<a href="#">RLMS3B[7:0]</a>		EyeMonValCntH[7:0]									
0x153D	<a href="#">RLMS3D[7:0]</a>		ErrChPh[6:0]									
0x153E	<a href="#">RLMS3E[7:0]</a>	ErrChPh SecTA	ErrChPhSec[6:0]									
0x153F	<a href="#">RLMS3F[7:0]</a>	ErrChPh PriTA	ErrChPhPri[6:0]									
0x1545	<a href="#">RLMS45[7:0]</a>	RSVD	RSVD	-	-	-	RSVD[2:0]					
0x1549	<a href="#">RLMS49[7:0]</a>	-	-	-	-	-	ErrChPw rUp	-	-			
0x1558	<a href="#">RLMS58[7:0]</a>	-	ErrChVTh1[6:0]									
0x1559	<a href="#">RLMS59[7:0]</a>	-	ErrChVTh0[6:0]									
0x1564	<a href="#">RLMS64[7:0]</a>	-	-	-	-	-	TxSSCMode[1:0]					
0x1570	<a href="#">RLMS70[7:0]</a>	-	TxSSCFrqCtrl[6:0]									
0x1571	<a href="#">RLMS71[7:0]</a>	-	TxSSCCenSprSt[5:0]									
0x1572	<a href="#">RLMS72[7:0]</a>	TxSSCPresClL[7:0]										
0x1573	<a href="#">RLMS73[7:0]</a>	-	-	-	-	-	TxSSCPresClH[2:0]					
0x1574	<a href="#">RLMS74[7:0]</a>	TxSSCPPhL[7:0]										
0x1575	<a href="#">RLMS75[7:0]</a>	-	TxSSCPPhH[6:0]									
0x1576	<a href="#">RLMS76[7:0]</a>	-	-	-	-	-	TxSSCPPhQuad[1:0]					
0x1595	<a href="#">RLMS95[7:0]</a>	TxAmpl ManEn	-	-	-	-	-	-	-			
0x15A4	<a href="#">RLMSA4[7:0]</a>	AEQ_PER_MULT[1: 0]	AEQ_PER[5:0]									
0x15AC	<a href="#">RLMSAC[7:0]</a>	ErrChPh SecTAF R3G	ErrChPhSecFR3G[6:0]									
0x15AD	<a href="#">RLMSAD[7:0]</a>	ErrChPh PriTAFR 3G	ErrChPhPriFR3G[6:0]									
0x15B6	<a href="#">RLMSB6[7:0]</a>	ErrChPh SecTAS RG1875	ErrChPhSecSRG1875[6:0]									
0x15B7	<a href="#">RLMSB7[7:0]</a>	ErrChPh PriTASR G1875	ErrChPhPriSRG1875[6:0]									
0x15C4	<a href="#">RLMSC4[7:0]</a>	-	-	-	-	-	RevFast	-	-			
0x15C5	<a href="#">RLMSC5[7:0]</a>	RevLen ManEn	RevFLenMan[6:0]									
0x15D1	<a href="#">RLMSD1[7:0]</a>	RSVD[2:0]			RSVD[2:0]			RSVD	RSVD			
<b>RLMS C</b>												
0x1603	<a href="#">RLMS3[7:0]</a>	AdaptEn	-	-	-	-	-	-	-			
0x1604	<a href="#">RLMS4[7:0]</a>	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]	EOM_PE R_MOD E	EOM_E N				

ADDRESS	NAME	MSB							LSB
0x1605	<a href="#">RLMS5[7:0]</a>	EOM_M AN_TRG _REQ	EOM_MIN_THR[6:0]						
0x1606	<a href="#">RLMS6[7:0]</a>	EOM_PV _MODE	EOM_RST_THR[6:0]						
0x1607	<a href="#">RLMS7[7:0]</a>	EOM_D ONE	EOM[6:0]						
0x1634	<a href="#">RLMS34[7:0]</a>	EyeMonPerCntL[7:0]							
0x1635	<a href="#">RLMS35[7:0]</a>	EyeMonPerCntH[7:0]							
0x1637	<a href="#">RLMS37[7:0]</a>	-	-	-	EyeMon Done	EyeMon CntClr	EyeMon Start	EyeMon Ph	EyeMon DPol
0x1638	<a href="#">RLMS38[7:0]</a>	EyeMonErrCntL[7:0]							
0x1639	<a href="#">RLMS39[7:0]</a>	EyeMonErrCntH[7:0]							
0x163A	<a href="#">RLMS3A[7:0]</a>	EyeMonValCntL[7:0]							
0x163B	<a href="#">RLMS3B[7:0]</a>	EyeMonValCntH[7:0]							
0x163D	<a href="#">RLMS3D[7:0]</a>	ErrChPh[6:0]						ErrChPh TogEn	
0x163E	<a href="#">RLMS3E[7:0]</a>	ErrChPh SecTA	ErrChPhSec[6:0]						
0x163F	<a href="#">RLMS3F[7:0]</a>	ErrChPh PriTA	ErrChPhPri[6:0]						
0x1645	<a href="#">RLMS45[7:0]</a>	RSVD	RSVD	-	-	-	RSVD[2:0]		
0x1649	<a href="#">RLMS49[7:0]</a>	-	-	-	-	-	ErrChPw rUp	-	-
0x1658	<a href="#">RLMS58[7:0]</a>	-	ErrChVTh1[6:0]						
0x1659	<a href="#">RLMS59[7:0]</a>	-	ErrChVTh0[6:0]						
0x1664	<a href="#">RLMS64[7:0]</a>	-	-	-	-	-	TxSSCMode[1:0]		
0x1670	<a href="#">RLMS70[7:0]</a>	-	TxSSCFrqCtrl[6:0]						
0x1671	<a href="#">RLMS71[7:0]</a>	-	TxSSCCenSprSt[5:0]						TxSSCE n
0x1672	<a href="#">RLMS72[7:0]</a>	TxSSCPresclL[7:0]							
0x1673	<a href="#">RLMS73[7:0]</a>	-	-	-	-	-	TxSSCPresclH[2:0]		
0x1674	<a href="#">RLMS74[7:0]</a>	TxSSCPPhL[7:0]							
0x1675	<a href="#">RLMS75[7:0]</a>	-	TxSSCPPhH[6:0]						
0x1676	<a href="#">RLMS76[7:0]</a>	-	-	-	-	-	TxSSCPPhQuad[1:0]		
0x1695	<a href="#">RLMS95[7:0]</a>	TxAmpl ManEn	-	-	-	-	-	-	-
0x16A4	<a href="#">RLMSA4[7:0]</a>	AEQ_PER_MULT[1: 0]	AEQ_PER[5:0]						
0x16AC	<a href="#">RLMSAC[7:0]</a>	ErrChPh SecTAF R3G	ErrChPhSecFR3G[6:0]						
0x16AD	<a href="#">RLMSAD[7:0]</a>	ErrChPh PriTAFR 3G	ErrChPhPriFR3G[6:0]						

ADDRESS	NAME	MSB							LSB
0x16B6	<a href="#">RLMSB6[7:0]</a>	ErrChPh SecTAS RG1875	ErrChPhSecSRG1875[6:0]						
0x16B7	<a href="#">RLMSB7[7:0]</a>	ErrChPh PriTASR G1875	ErrChPhPriSRG1875[6:0]						
0x16C4	<a href="#">RLMSC4[7:0]</a>	-	-	-	-	-	RevFast	-	-
0x16C5	<a href="#">RLMSC5[7:0]</a>	RevLen ManEn	RevFLenMan[6:0]						
0x16D1	<a href="#">RLMSD1[7:0]</a>	RSVD[2:0]			RSVD[2:0]		RSVD	RSVD	
<b>RLMS D</b>									
0x1703	<a href="#">RLMS3[7:0]</a>	AdaptEn	-	-	-	-	-	-	-
0x1704	<a href="#">RLMS4[7:0]</a>	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]	EOM_PE R_MOD E	EOM_E N	
0x1705	<a href="#">RLMS5[7:0]</a>	EOM_M AN_TRG _REQ	EOM_MIN_THR[6:0]						
0x1706	<a href="#">RLMS6[7:0]</a>	EOM_PV _MODE	EOM_RST_THR[6:0]						
0x1707	<a href="#">RLMS7[7:0]</a>	EOM_D ONE	EOM[6:0]						
0x1734	<a href="#">RLMS34[7:0]</a>	EyeMonPerCntL[7:0]							
0x1735	<a href="#">RLMS35[7:0]</a>	EyeMonPerCntH[7:0]							
0x1737	<a href="#">RLMS37[7:0]</a>	-	-	-	EyeMon Done	EyeMon CntClr	EyeMon Start	EyeMon Ph	EyeMon DPol
0x1738	<a href="#">RLMS38[7:0]</a>	EyeMonErrCntL[7:0]							
0x1739	<a href="#">RLMS39[7:0]</a>	EyeMonErrCntH[7:0]							
0x173A	<a href="#">RLMS3A[7:0]</a>	EyeMonValCntL[7:0]							
0x173B	<a href="#">RLMS3B[7:0]</a>	EyeMonValCntH[7:0]							
0x173D	<a href="#">RLMS3D[7:0]</a>	ErrChPh[6:0]						ErrChPh TogEn	
0x173E	<a href="#">RLMS3E[7:0]</a>	ErrChPh SecTA	ErrChPhSec[6:0]						
0x173F	<a href="#">RLMS3F[7:0]</a>	ErrChPh PriTA	ErrChPhPri[6:0]						
0x1745	<a href="#">RLMS45[7:0]</a>	RSVD	RSVD	-	-	-	RSVD[2:0]		
0x1749	<a href="#">RLMS49[7:0]</a>	-	-	-	-	-	ErrChPw rUp	-	-
0x1758	<a href="#">RLMS58[7:0]</a>	-	ErrChVTh1[6:0]						
0x1759	<a href="#">RLMS59[7:0]</a>	-	ErrChVTh0[6:0]						
0x1764	<a href="#">RLMS64[7:0]</a>	-	-	-	-	-	TxSSCMode[1:0]		
0x1770	<a href="#">RLMS70[7:0]</a>	-	TxSSCFrqCtrl[6:0]						
0x1771	<a href="#">RLMS71[7:0]</a>	-	TxSSCCenSprSt[5:0]						TxSSCE n
0x1772	<a href="#">RLMS72[7:0]</a>	TxSSCPresclL[7:0]							

ADDRESS	NAME	MSB							LSB
0x1773	<a href="#">RLMS73[7:0]</a>	-	-	-	-	-	-	TxSSCPreSclH[2:0]	
0x1774	<a href="#">RLMS74[7:0]</a>							TxSSCPhL[7:0]	
0x1775	<a href="#">RLMS75[7:0]</a>	-						TxSSCPhH[6:0]	
0x1776	<a href="#">RLMS76[7:0]</a>	-	-	-	-	-	-	TxSSCPhQuad[1:0]	
0x1795	<a href="#">RLMS95[7:0]</a>	TxAmpl ManEn	-	-	-	-	-	-	-
0x17A4	<a href="#">RLMSA4[7:0]</a>	AEQ_PER_MULT[1: 0]						AEQ_PER[5:0]	
0x17AC	<a href="#">RLMSAC[7:0]</a>	ErrChPh SecTAF R3G						ErrChPhSecFR3G[6:0]	
0x17AD	<a href="#">RLMSAD[7:0]</a>	ErrChPh PriTAFR 3G						ErrChPhPriFR3G[6:0]	
0x17B6	<a href="#">RLMSB6[7:0]</a>	ErrChPh SecTAS RG1875						ErrChPhSecSRG1875[6:0]	
0x17B7	<a href="#">RLMSB7[7:0]</a>	ErrChPh PriTASR G1875						ErrChPhPriSRG1875[6:0]	
0x17C4	<a href="#">RLMSC4[7:0]</a>	-	-	-	-	-	RevFast	-	-
0x17C5	<a href="#">RLMSC5[7:0]</a>	RevLen ManEn						RevFLenMan[6:0]	
0x17D1	<a href="#">RLMSD1[7:0]</a>		RSVD[2:0]		RSVD[2:0]		RSVD	RSVD	
<b>DPLL CSI1</b>									
0x1C00	<a href="#">DPLL_0[7:0]</a>	-	-	-	-	-	-	-	config_s oft_rst_n
<b>DPLL CSI2</b>									
0x1D00	<a href="#">DPLL_0[7:0]</a>	-	-	-	-	-	-	-	config_s oft_rst_n
<b>DPLL CSI3</b>									
0x1E00	<a href="#">DPLL_0[7:0]</a>	-	-	-	-	-	-	-	config_s oft_rst_n
<b>DPLL CSI4</b>									
0x1F00	<a href="#">DPLL_0[7:0]</a>	-	-	-	-	-	-	-	config_s oft_rst_n

## Register Details

### [REG0 \(0x0\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>				DEV_ADDR[6:0]				CFG_BLOCK
<b>Reset</b>				0b1001000				0b0
<b>Access Type</b>				Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	<p>Device Address</p> <p>Default address is set by the CFG0 pin at power-up. Refer to data sheet discussion of the CFG0 pin for further information. Address can be changed following power-up by updating the contents of this register.</p>	0b0000000: I <sup>2</sup> C write/read address is 0x00/0x01 0b0000001: I <sup>2</sup> C write/read address is 0x02/0x03 . 0b1001000: I <sup>2</sup> C write/read address is 0x90/0x91 0b1001010: I <sup>2</sup> C write/read address is 0x94/0x95 0b1001100: I <sup>2</sup> C write/read address is 0x98/0x99 0b1101000: I <sup>2</sup> C write/read address is 0xD0/0xD1 0b1101010: I <sup>2</sup> C write/read address is 0xD4/0xD5 0b1101100: I <sup>2</sup> C write/read address is 0xD8/0xD9 0b0101000: I <sup>2</sup> C write/read address is 0x50/0x51 0b0101010: I <sup>2</sup> C write/read address is 0x54/0x55 . 0b1111111: I <sup>2</sup> C write/read address is 0xFE/0xFF
CFG_BLOCK	0	<p>Configuration Block</p> <p>When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.</p>	0b0: Not blocked 0b1: Blocked

**REG1 (0x1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	IIC_SEL[1:0]		DIS_LOC_CC[1:0]		IIC_SEL_P2	DIS_LOC_CC_P2	ALT_IIC_SEL	FAILOVER
<b>Reset</b>	0x0		0b00		0x0	0x0	0x0	0x0
<b>Access Type</b>	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IIC_SEL	7:6	<p>Selects control channel port type for Ports 1 and 0.</p> <p>Bit 0 selects type of Port 0 (RX0/SDA0, TX0/SCL0)  Bit 1 selects type of Port 1 (RX1/SDA1, TX1/SCL1)  Bits are set according to the latched CFG pin value at power-up.</p> <p>See bit 3 for selection control for Port 2.</p>	0bX0: Port 0 UART 0bX1: Port 0 I <sup>2</sup> C 0b0X: Port 1 UART 0b1X: Port 1 I <sup>2</sup> C
DIS_LOC_C_C	5:4	<p>Disables control channel connection to I<sup>2</sup>C/UART Ports 1 and 0</p> <p>Bit 4 controls Port 0.  Bit 5 controls Port 1.</p> <p>See bit 2 for control of control channel Port 2.</p>	0bx0: Port 0 Rx/SDA and Tx/SCL connected to control channel 0bx1: Port 0 Rx/SDA and Tx/SCL disconnected from control channel 0b0x: Port 1 Rx1/SDA1 and Tx1/SCL1 connected to control channel 0b1x: Port 1 Rx1/SDA1 and Tx1/SCL1 disconnected from control channel

BITFIELD	BITS	DESCRIPTION	DECODE
IIC_SEL_P2	3	Selects Port 2 control channel port type.  Selects type for Port 2 (RX2/SDA2, TX2/SCL2).  Bit is set according to the latched CFG pin value at power-up.  See bits [7:6] for selection control for Ports 1 and 0.	0b0: UART 0b1: I <sup>2</sup> C
DIS_LOC_CC_P2	2	Disables control channel connection to Port 2.  See bits [5:4] for control of control channel for Ports 1 and 0.	0b0: Enable 0b1: Disable
ALT_IIC_SEL	1	Selects whether or not to use the alternate I <sup>2</sup> C pins for I <sup>2</sup> C Port 1.  When set, the original Port 1 I <sup>2</sup> C pins revert to GPIO's.	0b0: Disable selection of alternative I <sup>2</sup> C pins for use as I <sup>2</sup> C Port 1 0b1: Enable selection of alternative I <sup>2</sup> C pins for use as I <sup>2</sup> C Port 1
FAILOVER	0	I <sup>2</sup> C and UART Port 0 failover to Port 1.  When set to 1, this control bit provides a failover multiplexing of Port 0 I <sup>2</sup> C/UART I/O onto Port 1. The purpose of this control bit is to provide redundancy for Port 0. If a primary controller connected to Port 0 is disabled, a secondary controller connected to Port 0 can assume the primary controller's duties through Port 1.	0b0: Disable failover multiplexing of Port 0 to Port 1 0b1: Enable failover multiplexing of Port 0 to Port 1

REG3 (0x3)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DIS_Rem_CC_D[1:0]		DIS_Rem_CC_C[1:0]		DIS_Rem_CC_B[1:0]		DIS_Rem_CC_A[1:0]	
<b>Reset</b>	0b10		0b10		0b10		0b10	
<b>Access Type</b>	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_Rem_CC_D	7:6	Disable GMSL2 remote control channel link from each CC port to Link D Bit 0 disables the connection from Port 0. Bit 1 disables the connection from Port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
DIS_Rem_CC_C	5:4	Disable GMSL2 remote control channel link from each CC port to Link C Bit 0 disables the connection from Port 0. Bit 1 disables the connection from Port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
DIS_Rem_CC_B	3:2	Disable GMSL2 remote control channel link from each CC port to Link B Bit 0 disables the connection from Port 0. Bit 1 disables the connection from Port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_Rem_C_C_A	1:0	Disable GMSL2 remote control channel link from each CC port to Link A Bit 0 disables the connection from Port 0. Bit 1 disables the connection from Port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled

**REG4 (0x4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VID_EN_7	VID_EN_6	VID_EN_5	VID_EN_4	VID_EN_3	VID_EN_2	VID_EN_1	VID_EN_0
<b>Reset</b>	0b1							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_7	7	Video Enable	0b0: Video transmit Channel 7 disabled 0b1: Video transmit Channel 7 enabled
VID_EN_6	6	Video Enable	0b0: Video transmit Channel 6 disabled 0b1: Video transmit Channel 6 enabled
VID_EN_5	5	Video Enable	0b0: Video transmit Channel 5 disabled 0b1: Video transmit Channel 5 enabled
VID_EN_4	4	Video Enable	0b0: Video transmit Channel 4 disabled 0b1: Video transmit Channel 4 enabled
VID_EN_3	3	Video Enable	0b0: Video transmit Channel 3 disabled 0b1: Video transmit Channel 3 enabled
VID_EN_2	2	Video Enable	0b0: Video transmit Channel 2 disabled 0b1: Video transmit Channel 2 enabled
VID_EN_1	1	Video Enable	0b0: Video transmit Channel 1 disabled 0b1: Video transmit Channel 1 enabled
VID_EN_0	0	Video Enable	0b0: Video transmit Channel 0 disabled 0b1: Video transmit Channel 0 enabled

**REG5 (0x5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	LOCK_EN	ERRB_EN	LOCK_CFG	—	—	—	—	—
<b>Reset</b>	0x1	0x1	0b0	—	—	—	—	—
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	—	—	—	—	—
BITFIELD	BITS	DESCRIPTION			DECODE			
LOCK_EN	7	Enables LOCK output to GPIO			0b0: LOCK output disabled 0b1: LOCK output enabled			
ERRB_EN	6	Enables ERRB output to GPIO			0b0: ERRB output disabled 0b1: ERRB output enabled			
LOCK_CFG	5	Configures LOCK pin behavior			0b0: GMSL2 link locked 0b1: GMSL2 link locked and MIPI output started			

**REG6 (0x6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	GMSL2_D	GMSL2_C	GMSL2_B	GMSL2_A	LINK_EN_D	LINK_EN_C	LINK_EN_B	LINK_EN_A
<b>Reset</b>	0b1	0b1	0b1	0b1	0x1	0x1	0x1	0x1
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>					<b>DECODE</b>	
GMSL2_D	7	GMSL1/GMSL2 Selection for Link D Bit is set according to the latched CFG1 pin value at power-up					0b0: GMSL1 0b1: GMSL2	
GMSL2_C	6	GMSL1/GMSL2 Selection for Link C Bit is set according to the latched CFG1 pin value at power-up					0b0: GMSL1 0b1: GMSL2	
GMSL2_B	5	GMSL1/GMSL2 Selection for Link B Bit is set according to the latched CFG1 pin value at power-up					0b0: GMSL1 0b1: GMSL2	
GMSL2_A	4	GMSL1/GMSL2 Selection for Link A Bit is set according to the latched CFG1 pin value at power-up					0b0: GMSL1 0b1: GMSL2	
LINK_EN_D	3	Enables Link D					0b0: Disable link D 0b1: Enable link D	
LINK_EN_C	2	Enables Link C					0b0: Disable link C 0b1: Enable link C	
LINK_EN_B	1	Enables Link B					0b0: Disable link B 0b1: Enable link B	
LINK_EN_A	0	Enables Link A					0b0: Disable link A 0b1: Enable link A	

**REG7 (0x7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CC_CROSSOVER_SEL[7:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CROSSOVER_SEL	7:0	<p>Control Channel Port Crossover Selector</p> <p>Bit pairs in this register select whether control channel port crossover is disabled or enabled between Port 0 and Port 1 or Port 0 and Port 2</p> <p>The primary microcontroller must be connected to I<sup>2</sup>C/UART Port 0. The secondary microcontroller(s) should be connected to I<sup>2</sup>C/UART Port 1 or Port 2.</p> <p>Each of the links is controlled by a set of two bits in the bitfield. Note that these bit sets are not contiguous.</p> <p>The description of each link's pair of bits is as follows:</p> <p>Link A</p> <p>bit[4], bit[0]: 00—No Crossover 10—Enable Crossover between Port 0 and Port 1 01—Enable Crossover between Port 0 and Port 2</p> <p>Link B</p> <p>bit[5], bit[1]: 00—No Crossover 10—Enable Crossover between Port 0 and Port 1 01—Enable Crossover between Port 0 and Port 2</p> <p>Link C</p> <p>bit[6], bit[2]: 00—No Crossover 10—Enable Crossover between Port 0 and Port 1 01—Enable Crossover between Port 0 and Port 2</p> <p>Link D</p> <p>bit[7], bit[3]: 00—No Crossover 10—Enable Crossover between Port 0 and Port 1 01—Enable Crossover between Port 0 and Port 2</p>	0bXXX0XXX0: Link A—No Crossover 0bXXX1XXX0: Link A—Enable Crossover between Port 0 and Port 1 0bXXX0XXX1: Link A—Enable Crossover between Port 0 and Port 2 0bXX0XXX0X: Link B—No Crossover 0bXX1XXX0X: Link B—Enable Crossover between Port 0 and Port 1 0bXX0XXX1X: Link B—Enable Crossover between Port 0 and Port 2 0bX0XXX0XX: Link C—No Crossover 0bX1XXX0XX: Link C—Enable Crossover between Port 0 and Port 1 0bX0XXX1XX: Link C—Enable Crossover between Port 0 and Port 2 0b0XXX0XXX: Link D—No Crossover 0b1XXX0XXX: Link D—Enable Crossover between Port 0 and Port 1 0b0XXX1XXX: Link D—Enable Crossover between Port 0 and Port 2

**DEBUG\_EXTRA\_1 (0x8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PATGEN_S YNC	—	—	—	—	—	—	—
<b>Reset</b>	0x0	—	—	—	—	—	—	—
<b>Access Type</b>	Write, Read	—	—	—	—	—	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
PATGEN_SY NC	7	Synchronizes multiple pattern generators.						0b0: Do not synchronize 0b1: Synchronize

**DEBUG\_EXTRA (0x9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DEBUG_EXTRA[7:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
DEBUG_EXT RA	7:0	Pattern CLK Frequency Register  Bits[1:0] set the video pattern PCLK frequency. Bits[7:2] are reserved. Note that bit[1] works in conjunction with the corresponding PATGEN_CLK_SRC bitfield to set the PCLK frequency.  A PATGEN_CLK_SRC bit is present in the VPRBS register of each of the eight VRX blocks.  See registers 0x1DC, 0x1FC, 0x21C, 0x23C, 0x25C, 0x27C, 0x29C, and 0x2BC.						0bXXXXXX00: 25MHz 0bXXXXXX01: 75MHz 0bXXXXXX10: 150MHz (when PATGEN_CLK_SRC = 0b0) 0bXXXXXX11: 375MHz (when PATGEN_CLK_SRC = 0b1)

**CTRL12 (0xA)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	LOCKED_B	—	—	—
<b>Reset</b>	—	—	—	—	0b0	—	—	—
<b>Access Type</b>	—	—	—	—	Read Only	—	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
LOCKED_B	3	GMSL2 Link Locked (bidirectional)						0b0: GMSL2 link not locked 0b1: GMSL2 link locked

**CTRL13 (0xB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	LOCKED_C	—	—	—
<b>Reset</b>	—	—	—	—	0b0	—	—	—
<b>Access Type</b>	—	—	—	—	Read Only	—	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
LOCKED_C	3	GMSL2 Link Locked (bidirectional)						0b0: GMSL2 link not locked 0b1: GMSL2 link locked

**CTRL14 (0xC)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	LOCKED_D	—	—	—
<b>Reset</b>	—	—	—	—	0b0	—	—	—
<b>Access Type</b>	—	—	—	—	Read Only	—	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
LOCKED_D	3	GMSL2 Link Locked (bidirectional)						0b0: GMSL2 link not locked 0b1: GMSL2 link locked

**REG13 (0xD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DEV_ID[7:0]							
<b>Reset</b>	0xA0							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
DEV_ID	7:0	Device Identifier						0xA1: MAX96722

**REG14 (0xE)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	DIS_LOCAL_WAKE_P2	—	AUTO_SLE_EP_DIS	—	DIS_Rem_CC_P2[3:0]				
<b>Reset</b>	0b0	—	0b0	—	0b1111				
<b>Access Type</b>	Write, Read	—	Write, Read	—	Write, Read				
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>	
DIS_LOCAL_WAKE_P2	7	Disables wake-up by local µC from SDA_RX pin on Port 2.  Bit [7] - Controls the local wake-up for Port 2  See the DIS_LOCAL_WAKE bitfield in the description for the TOP_CTRL/CTRL0 register (Address 0x17) for Port 1 and 0 local wake-up control.						0b0: Local wake-up enabled 0b1: Local wake-up disabled	

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_SLEE_P_DIS	5	Disables the 8ms auto-sleep timeout after wake-up.	0b0: 8ms auto-sleep enabled 0b1: 8ms auto-sleep disabled
DIS_Rem_C_C_P2	3:0	Disables GMSL2 remote control channel link from CC Port 2 for all Links (A, B, C, and D)  Bit 0 disables the Port 2 connection to Link A. Bit 1 disables the Port 2 connection to Link B. Bit 2 disables the Port 2 connection to Link C. Bit 3 disables the Port 2 connection to Link D.	0bXXX0: Remote control channel enabled— Link A 0bXXX1: Remote control channel disabled— Link A 0bXX0X: Remote control channel enabled— Link B 0bXX1X: Remote control channel disabled— Link B 0bX0XX: Remote control channel enabled— Link C 0bX1XX: Remote control channel disabled— Link C 0b0XXX: Remote control channel enabled— Link D 0b1XXX: Remote control channel disabled— Link D

**REG26 (0x10)**

BIT	7	6	5	4	3	2	1	0
Field	TX_RATE_PHYB[1:0]			—	—	TX_RATE_PHYA[1:0]		
Reset	0x0			—	—	0x0		
Access Type	Write, Read			—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_RATE_PHYB	7:6	Transmitter Rate (when changed, becomes active after next link reset)				0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved		
TX_RATE_PHYA	3:2	Transmitter Rate (when changed, becomes active after next link reset)				0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved		

**REG27 (0x11)**

BIT	7	6	5	4	3	2	1	0
Field	TX_RATE_PHYD[1:0]			—	—	TX_RATE_PHYC[1:0]		
Reset	0x0			—	—	0x0		
Access Type	Write, Read			—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_RATE_PHYD	7:6	Transmitter Rate (when changed, becomes active after next link reset)				0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved		
TX_RATE_PHYC	3:2	Transmitter Rate (when changed, becomes active after next link reset)				0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved		

**PWR0 (0x12)**

BIT	7	6	5	4	3	2	1	0
Field	VDBBAD_STATUS[2:0]				CMP_STATUS[4:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			
BITFIELD	BITS	DESCRIPTION				DECODE		
VDBBAD_STATUS	7:5	Core 1V V <sub>DD</sub> _sw Status  Bits 0 and 1 are identical latched high flags that indicate V <sub>DD</sub> _sw < 0.82V when set. Status will clear when read if V <sub>DD</sub> _sw > 0.82V. This status indicator drives VDDBAD_INT_FLAG.				0bX00: V <sub>DD</sub> _sw > 0.82 V 0bX11: V <sub>DD</sub> _sw < 0.82 V observed since last read (latched, read to clear)		
CMP_STATUS	4:0	Power Manager Comparator Status  Status indicators are latched low if an undervoltage occurs on the specified supply. Clear to read. Combined status indicators drive VDDCMP_INT_FLAG.				0bXXXX0: V <sub>DD</sub> 18 < 1.617V (latched, read to clear) 0bXXXX1: V <sub>DD</sub> 18 > 1.617V 0bXXX0X: V <sub>DD</sub> IO < 1.617V (latched, read to clear) 0bXXX1X: V <sub>DD</sub> IO > 1.617V 0bXX0XX: V <sub>DD</sub> _sw < 0.802V (latched, read to clear) 0bXX1XX: V <sub>DD</sub> _sw > 0.802V		

**PWR1 (0x13)**

BIT	7	6	5	4	3	2	1	0
Field	—	RESET_ALL	—	—	—	—	—	—
Reset	—	0b0	—	—	—	—	—	—
Access Type	—	Write, Read	—	—	—	—	—	—
BITFIELD	BITS	DESCRIPTION				DECODE		
RESET_ALL	6	Device Reset  Writing 1 to this bit resets the device. All blocks and registers are reset to defaults.  This is equivalent to toggling the PWDNB pin. The bit is cleared when written.				0b0: No action 0b1: Activate chip reset		

**CTRL0 (0x17)**

BIT	7	6	5	4	3	2	1	0		
Field	WAKE_EN_D	WAKE_EN_C	WAKE_EN_B	WAKE_EN_A	SLEEP	REG_ENABLE	DIS_LOCAL_WAKE[1:0]			
Reset	0b0	0b0	0b0	0b1	0b0	0x0	0b0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE				
WAKE_EN_D	7	Enable wake-up by remote chip connected to Link D.				0b0: Link D remote wake-up disabled 0b1: Link D remote wake-up enabled				

BITFIELD	BITS	DESCRIPTION	DECODE
WAKE_EN_C	6	Enable wake-up by remote chip connected to Link C	0b0: Link C remote wake-up disabled 0b1: Link C remote wake-up enabled
WAKE_EN_B	5	Enable wake-up by remote chip connected to Link B	0b0: Link B remote wake-up disabled 0b1: Link B remote wake-up enabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to Link A	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled
SLEEP	3	Activates sleep mode.	0b0: Sleep mode disabled 0b1: Sleep mode enabled
REG_ENABLE	2	V <sub>DD</sub> LDO Regulator Enable  Works in conjunction with bitfield REG_MNL (0x19). Enable function is available when REG_MNL = 1. If REG_MNL = 0, manual control using REG_ENABLE is not available.	0b0: V <sub>DD</sub> LDO regulator disabled (bypassed) when REG_MNL = 1 0b1: V <sub>DD</sub> LDO regulator enabled when REG_ENABLE = 1 and REG_MNL = 1. When V <sub>DD</sub> = 1.2V, first set REG_ENABLE = 1, and then write REG_MNL = 1
DIS_LOCAL_WAKE	1:0	Disables wake-up by local µC from SDA_RX pin for Ports 1 and 0  bit [1] - Controls the local wake-up for Port 1 bit [0] - Controls the local wake-up for Port 0  See the description for DEV_REG14 (at address 0xE) for Port 2 local wake-up control.	0bX0: Local wake-up enabled—Port 0 0bX1: Local wake-up disabled—Port 0 0b0X: Local wake-up enabled—Port 1 0b1X: Local wake-up disabled—Port 1

CTRL1 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	RESET_LIN_K_D	RESET_LIN_K_C	RESET_LIN_K_B	RESET_LIN_K_A	RESET_ON_ESHOT_D	RESET_ON_ESHOT_C	RESET_ON_ESHOT_B	RESET_ON_ESHOT_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_LIN_K_D	7	Link D Reset  Resets whole data path (keep register settings).  Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_LIN_K_C	6	Link C Reset  Resets whole data path (keep register settings).  Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_LIN_K_B	5	Link B Reset  Resets whole data path (keep register settings).  Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_LIN_K_A	4	Link A Reset  Resets whole data path (keep register settings).  Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONE_SHOT_D	3	Link D One-Shot Reset  Resets whole data path (keep register settings) one shot.  Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path
RESET_ONE_SHOT_C	2	Link C One-Shot Reset  Resets whole data path (keep register settings) one shot.  Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path
RESET_ONE_SHOT_B	1	Link B One-Shot Reset  Resets whole data path (keep register settings) one shot.  Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path
RESET_ONE_SHOT_A	0	Link A One-Shot Reset  Resets whole data path (keep register settings) one shot.  Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path

CTRL2 (0x19)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	REG_MNL	—	—	—	—
<b>Reset</b>	—	—	—	0b0	—	—	—	—
<b>Access Type</b>	—	—	—	Write, Read	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
REG_MNL	4	Enables V <sub>DD</sub> LDO regulator manual on/bypass control via REG_ENABLE bitfield (0x10).	0b0: V <sub>DD</sub> LDO regulator range sensing on. 0b1: V <sub>DD</sub> LDO regulator range sensing off. V <sub>DD</sub> LDO regulator on/bypass state controlled by REG_ENABLE. When V <sub>DD</sub> = 1.2V, enable V <sub>DD</sub> LDO regulator by first setting REG_ENABLE = 1 and then setting REG_MNL = 1.

**CTRL3 (0x1A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	LOCKED	ERROR	CMU_LOCKED	—
<b>Reset</b>	—	—	—	—	0b0	0b0	0b0	—
<b>Access Type</b>	—	—	—	—	Read Only	Read Only	Read Only	—

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED	3	GMSL2 link lock (bidirectional)—Link A only	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock Multiplier Unit (CMU) lock	0b0: CMU not locked 0b1: CMU locked

**CTRL11 (0x22)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CXTP_D	—	CXTP_C	—	CXTP_B	—	CXTP_A
<b>Reset</b>	—	0b0	—	0b0	—	0b0	—	0b0
<b>Access Type</b>	—	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_D	6	Coax/Twisted-Pair Cable Select for Link D Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_C	4	Coax/Twisted-Pair Cable Select for Link C Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_B	2	Coax/Twisted-Pair Cable Select for Link B Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/Twisted-Pair Cable Select for Link A Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

**INTR0 (0x23)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
<b>Reset</b>	—	—	—	—	0b0	0x0		
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A (0x35), DEC_ERR_B (0x36), DEC_ERR_C (0x37) DEC_ERR_D (0x38) and IDLE_ERR_A (0x39), IDLE_ERR_B (0x3A), IDLE_ERR_C (0x3B), IDLE_ERR_D (0x3C) bitfields after ERRB pin is asserted for 1μs.	0b0: Auto reset disabled 0b1: Auto reset enabled
DEC_ERR_T HR	2:0	<p>Decoding and Idle Error Reporting Threshold DEC_ERR_FLAG_A (0x26) is asserted when DEC_ERR_A (0x35) ≥ DEC_ERR_THR.</p> <p>DEC_ERR_FLAG_B (0x26) is asserted when DEC_ERR_B (0x36) ≥ DEC_ERR_THR.</p> <p>DEC_ERR_FLAG_C (0x26) is asserted when DEC_ERR_C (0x37) ≥ DEC_ERR_THR.</p> <p>DEC_ERR_FLAG_D (0x26) is asserted when DEC_ERR_D (0x38) ≥ DEC_ERR_THR.</p> <p>IDLE_ERR_FLAG_A (0x2C) is asserted when IDLE_ERR_A (0x39) ≥ DEC_ERR_THR.</p> <p>IDLE_ERR_FLAG_B (0x2C) is asserted when IDLE_ERR_B (0x3A) ≥ DEC_ERR_THR.</p> <p>IDLE_ERR_FLAG_C (0x2C) is asserted when IDLE_ERR_C (0x3B) ≥ DEC_ERR_THR.</p> <p>IDLE_ERR_FLAG_D (0x2C) is asserted when IDLE_ERR_D (0x3C) ≥ DEC_ERR_THR.</p>	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

**INTR1 (0x24)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
<b>Reset</b>	0x0				0b0	0x0		
<b>Access Type</b>	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet Count Multiplier Exponent  See the description of PKT_CNT_x (0x40—0x43) bitfield.	0xX: PKT_CNT_x exponent
AUTO_CNT_RST_EN	3	Automatically resets PKT_CNT_x bitfield (0x40—0x43) after ERRB pin is asserted for 1μs.	0b0: Do not automatically reset PKT_CNT_x register after ERRB pin is asserted for 1μs 0b1: Automatically reset PKT_CNT_x register after ERRB pin is asserted for 1μs
PKT_CNT THR	2:0	Packet Count Reporting Threshold  PKT_CNT_FLAG_A (0x2C) is asserted when PKT_CNT_A (0x40) ≥ PKT_CNT_THR.  PKT_CNT_FLAG_B (0x2C) is asserted when PKT_CNT_B (0x41) ≥ PKT_CNT_THR.  PKT_CNT_FLAG_C (0x2C) is asserted when PKT_CNT_C (0x42) ≥ PKT_CNT_THR.  PKT_CNT_FLAG_D (0x2C) is asserted when PKT_CNT_D (0x43) ≥ PKT_CNT_THR.	0b000: 1 packet 0b001: 2 packets 0b010: 4 packets 0b011: 8 packets 0b100: 16 packets 0b101: 32 packets 0b110: 64 packets 0b111: 128 packets

**INTR2 (0x25)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	DEC_ERR_OEN_D	DEC_ERR_OEN_C	DEC_ERR_OEN_B	DEC_ERR_OEN_A
<b>Reset</b>	—	—	—	—	0b1	0b1	0b1	0b1
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_OEN_D	3	Enables reporting of decoding errors (DEC_ERR_FLAG_D—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_D) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_D) at ERRB pin
DEC_ERR_OEN_C	2	Enables reporting of decoding errors (DEC_ERR_FLAG_C—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_C) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_C) at ERRB pin
DEC_ERR_OEN_B	1	Enables reporting of decoding errors (DEC_ERR_FLAG_B—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_B) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_B) at ERRB pin
DEC_ERR_OEN_A	0	Enables reporting of decoding errors (DEC_ERR_FLAG_A—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_A) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_A) at ERRB pin

**INTR3 (0x26)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	DEC_ERR_FLAG_D	DEC_ERR_FLAG_C	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
<b>Reset</b>	—	—	—	—	0b0	0b0	0b0	0b0
<b>Access Type</b>	—	—	—	—	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_FLAG_D	3	Decoding error flag for Link D, asserted when DEC_ERR_D ≥ DEC_ERR_THR.	0b0: DEC_ERR_D < DEC_ERR_THR 0b1: DEC_ERR_D ≥ DEC_ERR_THR
DEC_ERR_FLAG_C	2	Decoding error flag for Link C, asserted when DEC_ERR_C ≥ DEC_ERR_THR.	0b0: DEC_ERR_C < DEC_ERR_THR 0b1: DEC_ERR_C ≥ DEC_ERR_THR
DEC_ERR_FLAG_B	1	Decoding error flag for Link B, asserted when DEC_ERR_B ≥ DEC_ERR_THR.	0b0: DEC_ERR_B < DEC_ERR_THR 0b1: DEC_ERR_B ≥ DEC_ERR_THR
DEC_ERR_FLAG_A	0	Decoding error flag for Link A, asserted when DEC_ERR_A ≥ DEC_ERR_THR.	0b0: DEC_ERR_A < DEC_ERR_THR 0b1: DEC_ERR_A ≥ DEC_ERR_THR

**INTR4 (0x27)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EOM_ERR_OEN_D	EOM_ERR_OEN_C	EOM_ERR_OEN_B	EOM_ERR_OEN_A	RTTN_CRC_ERR_OEN	LFLT_INT_OEN	WM1_ERR_OEN	WM_ERR_OEN
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0x1	0b1	0b1
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_D	7	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_D—0x28) for Link D at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_D) for Link D at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_D) for Link D at ERRB pin
EOM_ERR_OEN_C	6	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_C—0x28) for Link C at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_C) for Link C at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_C) for Link C at ERRB pin
EOM_ERR_OEN_B	5	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_B—0x28) for Link B at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_B) for Link B at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_B) for Link B at ERRB pin
EOM_ERR_OEN_A	4	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_A—0x28) for Link A at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_A) for Link A at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_A) for Link A at ERRB pin
RTTN_CRC_ERR_OEN	3	Enables reporting of retention restoration CRC error (RTTN_CRC_ERR_FLAG) at ERRB pin.	0b0: Disable reporting of retention restoration CRC error (RTTN_CRC_ERR_FLAG) at ERRB pin 0b1: Enable reporting of retention restoration CRC error (RTTN_CRC_ERR_FLAG) at ERRB pin
LFLT_INT_OEN	2	Enable reporting of line fault interrupt (LFLT_INT) at ERRB pin	0b0: Disable reporting of line fault interrupt (LFLT_INT) at ERRB pin 0b1: Enable reporting of line fault interrupt (LFLT_INT) at ERRB pin

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
WM1_ERR_OEN	1	Enables reporting of watermark errors (WM1_ERR_FLAG) at ERRB pin.	0b0: Disable reporting of watermark errors (WM1_ERR_FLAG) at ERRB pin 0b1: Enable reporting of watermark errors (WM1_ERR_FLAG) at ERRB pin
WM_ERR_OEN	0	Enables reporting of watermark errors (WM_ERR_FLAG) at ERRB pin.	0b0: Disable reporting of watermark errors (WM_ERR_FLAG) at ERRB pin 0b1: Enable reporting of watermark errors (WM_ERR_FLAG) at ERRB pin

**INTR5 (0x28)**

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_D	EOM_ERR_FLAG_C	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	RTTN_CRC_INT	LFLT_INT	WM1_ERR_FLAG	WM_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0x0	0x0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_D	7	Link D Eye-opening Threshold Status  Indicates whether or not eye-opening is below configured threshold for Link D.	0b0: Eye-opening is above configured threshold for Link D 0b1: Eye-opening is below configured threshold for Link D
EOM_ERR_FLAG_C	6	Link C Eye-opening Threshold Status  Indicates whether or not eye-opening is below configured threshold for Link c.	0b0: Eye-opening is above configured threshold for Link C 0b1: Eye-opening is below configured threshold for Link C
EOM_ERR_FLAG_B	5	Link B Eye-opening Threshold Status  Indicates whether or not eye-opening is below configured threshold for Link B.	0b0: Eye-opening is above configured threshold for Link B 0b1: Eye-opening is below configured threshold for Link B
EOM_ERR_FLAG_A	4	Link A Eye-opening Threshold Status  Indicates whether or not eye-opening is below configured threshold for Link A.	0b0: Eye-opening is above configured threshold for Link A 0b1: Eye-opening is below configured threshold for Link A
RTTN_CRC_INT	3	Retention Memory Restore CRC Error Interrupt  Asserted when an error is detected in the CRC calculation during a retention memory restore. Reading this register bit will clear the retention CRC error register.	0b0: No error detected in the CRC calculation during a retention memory restore. 0b1: An error was detected in the CRC calculation during a retention memory restore.
LFLT_INT	2	Line Fault Interrupt  Asserted when either one of line fault monitors indicates a fault status.  <i>See LF_0 and LF_1 registers for more info.</i>	0b0: No fault status indicated for either line fault monitor 0b1: One (or both) of the line fault monitors indicate a fault status.
WM1_ERR_FLAG	1	Watermark Error Flag (watermark detector 1)  Asserted when a watermark error is detected by watermark detector 1.	0b0: No watermark error detected 0b1: Watermark error detected

BITFIELD	BITS	DESCRIPTION	DECODE
WM_ERR_FLAG	0	Watermark Error Flag (watermark detector 0)  Asserted when a watermark error is detected by watermark detector 0.	0b0: No watermark error detected 0b1: Watermark error detected

**INTR6 (0x29)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	G1_D_ERR_OEN	G1_C_ERR_OEN	G1_B_ERR_OEN	G1_A_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	REM_ERR_OEN	FSYNC_ERR_OEN
<b>Reset</b>	0x1	0x1	0x1	0x1	0b1	0b1	0b0	0b1
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
G1_D_ERR_OEN	7	Enables reporting of GMSL1 Link D errors (G1_D_ERR_FLAG) at ERRB pin.	0b0: Disable GMSL1 Link D error reporting (G1_D_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link D error reporting (G1_D_ERR_FLAG) at ERRB pin
G1_C_ERR_OEN	6	Enables reporting of GMSL1 Link C errors (G1_C_ERR_FLAG) at ERRB pin.	0b0: Disable GMSL1 Link C error reporting (G1_C_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link C error reporting (G1_C_ERR_FLAG) at ERRB pin
G1_B_ERR_OEN	5	Enables reporting of GMSL1 Link B errors (G1_B_ERR_FLAG) at ERRB pin.	0b0: Disable GMSL1 Link B error reporting (G1_B_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link B error reporting (G1_B_ERR_FLAG) at ERRB pin
G1_A_ERR_OEN	4	Enables reporting of GMSL1 Link A errors (G1_A_ERR_FLAG) at ERRB pin.	0b0: Disable GMSL1 Link A error reporting (G1_A_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link A error reporting (G1_A_ERR_FLAG) at ERRB pin
LCRC_ERR_OEN	3	Enables reporting of video line CRC errors (LCRC_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable video line CRC error reporting (LCRC_ERR_FLAG) at ERRB pin 0b1: Enable video line CRC error reporting (LCRC_ERR_FLAG) at ERRB pin
VPRBS_ERR_OEN	2	Enables reporting of video PRBS errors (VPRBS_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable video PRBS error reporting (VPRBS_ERR_FLAG) at ERRB pin 0b1: Enable video PRBS error reporting (VPRBS_ERR_FLAG) at ERRB pin
REM_ERR_OEN	1	Enables reporting of remote error status (REM_ERR—0x2A) at ERRB pin.	0b0: Disable remote error status (REM_ERR) reporting at ERRB pin 0b1: Enable remote error status (REM_ERR) reporting at ERRB pin
FSYNC_ERR_OEN	0	Enables reporting of frame sync errors (FSYNC_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable frame sync error reporting (FSYNC_ERR_FLAG) at ERRB pin 0b1: Enable frame sync error reporting (FSYNC_ERR_FLAG) at ERRB pin

**INTR7 (0x2A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	G1_D_ERR_FLAG	G1_C_ERR_FLAG	G1_B_ERR_FLAG	G1_A_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ER_R_FLAG	REM_ERR_FLAG	FSYNC_ERR_FLAG
<b>Reset</b>	0x0	0x0	0x0	0x0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Read Only	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
G1_D_ERR_FLAG	7	<p>GMSL1 Link D Error Flag</p> <p>When PRBS test is enabled, this bit is asserted if at least one PRBS error has been detected.</p> <p>When PRBS test is not enabled, this flag is asserted when any of these conditions is true:</p> <ul style="list-style-type: none"> <li>1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) &gt; DET_THR (0xCOE)).</li> <li>2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)).</li> <li>3. The adaptive EQ has detected an under boost.</li> <li>4. A video line CRC error is detected.</li> <li>5. The maximum retransmission count in PKTCC communication has been exceeded.</li> <li>6. A CRC errors was detected in PKTCC communication.</li> </ul>	<p>0b0: No error detected 0b1: Error detected</p>

**PRELIMINARY**

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
G1_C_ERR_FLAG	6	<p>GMSL1 Link C Error Flag</p> <p>When PRBS test is enabled, this bit is asserted if at least one PRBS error has been detected.</p> <p>When PRBS test is not enabled, this flag is asserted when any of these conditions is true:</p> <ol style="list-style-type: none"> <li>1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) &gt; DET_THR (0xCOE)).</li> <li>2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)).</li> <li>3. The adaptive EQ has detected an under boost.</li> <li>4. A video line CRC error is detected.</li> <li>5. The maximum retransmission count in PKTCC communication has been exceeded.</li> <li>6. A CRC errors was detected in PKTCC communication.</li> </ol>	<p>0b0: No error detected 0b1: Error detected</p>
G1_B_ERR_FLAG	5	<p>GMSL1 Link B Error Flag</p> <p>When PRBS test is enabled, this bit is asserted if at least one PRBS error has been detected.</p> <p>When PRBS test is not enabled, this flag is asserted when any of these conditions is true:</p> <ol style="list-style-type: none"> <li>1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) &gt; DET_THR (0xCOE)).</li> <li>2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)).</li> <li>3. The adaptive EQ has detected an under boost.</li> <li>4. A video line CRC error is detected.</li> <li>5. The maximum retransmission count in PKTCC communication has been exceeded.</li> <li>6. A CRC errors was detected in PKTCC communication.</li> </ol>	<p>0b0: No error detected 0b1: Error detected</p>

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
G1_A_ERR_FLAG	4	<p>GMSL1 Link A Error Flag</p> <p>When PRBS test is enabled, this bit is asserted if at least one PRBS error has been detected.</p> <p>When PRBS test is not enabled, this flag is asserted when any of these conditions is true:</p> <ol style="list-style-type: none"> <li>1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) &gt; DET_THR (0xCOE)).</li> <li>2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)).</li> <li>3. The adaptive EQ has detected an under boost.</li> <li>4. A video line CRC error is detected.</li> <li>5. The maximum retransmission count in PKTCC communication has been exceeded.</li> <li>6. A CRC errors was detected in PKTCC communication.</li> </ol>	<p>0b0: No error detected 0b1: Error detected</p>
LCRC_ERR_FLAG	3	<p>Video Line CRC Error Flag</p> <p>Assert when a video line CRC error is detected.</p>	<p>0b0: No video line CRC error detected 0b1: Video line CRC error detected</p>
VPRBS_ERR_FLAG	2	<p>Video PRBS Error Flag</p> <p>Asserted when VPRBS_ERR (0x1D8) &gt; 0.</p>	<p>0b0: VPRBS_ERR ≤ 0 0b1: VPRBS_ERR &gt; 0</p>
REM_ERR_FLAG	1	Receives remote side error status (inverse of remote side ERRB pin level).	<p>0b0: No remote side error status received 0b1: Remote side error status received</p>
FSYNC_ERR_FLAG	0	<p>Frame Sync Error Flag</p> <p>Asserted when FSYNC_ERR_CNT (0x4B0) ≥ FSYNC_ERR_THR (0x4B1).</p>	<p>0b0: FSYNC_ERR_CNT &lt; FSYNC_ERR_THR 0b1: FSYNC_ERR_CNT ≥ FSYNC_ERR_THR</p>

**INTR8 (0x2B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	IDLE_ERR_OEN_D	IDLE_ERR_OEN_C	IDLE_ERR_OEN_B	IDLE_ERR_OEN_A
<b>Reset</b>	—	—	—	—	0b0	0b0	0b0	0b0
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_OEN_D	3	Enables reporting of Idle word errors (IDLE_ERR_FLAG_D) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_D) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_D) at ERRB pin
IDLE_ERR_OEN_C	2	Enables reporting of idle word errors (IDLE_ERR_FLAG_C) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_C) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_C) at ERRB pin
IDLE_ERR_OEN_B	1	Enables reporting of idle word errors (IDLE_ERR_FLAG_B) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_B) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_B) at ERRB pin
IDLE_ERR_OEN_A	0	Enables reporting of idle word errors (IDLE_ERR_FLAG_A) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_A) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_A) at ERRB pin

**INTR9 (0x2C)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	IDLE_ERR_FLAG_D	IDLE_ERR_FLAG_C	IDLE_ERR_FLAG_B	IDLE_ERR_FLAG_A
<b>Reset</b>	—	—	—	—	0b0	0b0	0b0	0b0
<b>Access Type</b>	—	—	—	—	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_FLAG_D	3	Idle Word Error Flag D Asserted when IDLE_ERR_D (0x3C) ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_D < DEC_ERR_THR 0b1: IDLE_ERR_D ≥ DEC_ERR_THR
IDLE_ERR_FLAG_C	2	Idle Word Error Flag C Asserted when IDLE_ERR_C (0x3B) ≥ DEC_ERR_THR.	0b0: IDLE_ERR_C < DEC_ERR_THR 0b1: IDLE_ERR_C ≥ DEC_ERR_THR
IDLE_ERR_FLAG_B	1	Idle Word Error Flag B Asserted when IDLE_ERR_B (0x3A0 ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_B < DEC_ERR_THR 0b1: IDLE_ERR_B ≥ DEC_ERR_THR
IDLE_ERR_FLAG_A	0	Idle Word Error Flag A Asserted when IDLE_ERR_A (0x39) ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_A < DEC_ERR_THR 0b1: IDLE_ERR_A ≥ DEC_ERR_THR

**INTR10 (0x2D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RT_CNT_O_EN_D	RT_CNT_O_EN_C	RT_CNT_O_EN_B	RT_CNT_O_EN_A	MAX_RT_O_EN_D	MAX_RT_O_EN_C	MAX_RT_O_EN_B	MAX_RT_O_EN_A
<b>Reset</b>	0b0	0b0	0b0	0b0	0b1	0b1	0b1	0b1
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OE_N_D	7	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D) at ERRB pin
RT_CNT_OE_N_C	6	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C) at ERRB pin
RT_CNT_OE_N_B	5	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B) at ERRB pin
RT_CNT_OE_N_A	4	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A) at ERRB pin
MAX_RT_OE_N_D	3	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D) at ERRB pin
MAX_RT_OE_N_C	2	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C) at ERRB pin
MAX_RT_OE_N_B	1	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B) at ERRB pin
MAX_RT_OE_N_A	0	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A) at ERRB pin

**INTR11 (0x2E)**

BIT	7	6	5	4	3	2	1	0
Field	RT_CNT_F LAG_D	RT_CNT_F LAG_C	RT_CNT_F LAG_B	RT_CNT_F LAG_A	MAX_RT_F LAG_D	MAX_RT_F LAG_C	MAX_RT_F LAG_B	MAX_RT_F LAG_A
Reset	0b0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_FL AG_D	7	Combined ARQ Retransmission Event Flag D  Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_D (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
RT_CNT_FL AG_C	6	Combined ARQ Retransmission Event Flag C  Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_C (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
RT_CNT_FL AG_B	5	Combined ARQ Retransmission Event Flag B  Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_B (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
RT_CNT_FL AG_A	4	Combined ARQ Retransmission Event Flag A  Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_A (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
MAX_RT_FL AG_D	3	Combined ARQ Maximum Retransmission Limit Error Flag D  Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_D (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit
MAX_RT_FL AG_C	2	Combined ARQ Maximum Retransmission Limit Error Flag C  Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_C (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit
MAX_RT_FL AG_B	1	Combined ARQ Maximum Retransmission Limit Error Flag B  Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_B (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_FL AG_A	0	Combined ARQ Maximum Retransmission Limit Error Flag A  Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_A (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit

**INTR12 (0x2F)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ERR_TX_E N	MEM_ERR _OEN	–	–	–	–	–	ERR_TX_ID[4:0]
<b>Reset</b>	0b1	0b0	–	–	–	–	–	0x1F
<b>Access Type</b>	Write, Read	Write, Read	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmits local error status (inverse of ERRB pin level) to remote side through GPIO channel.	0b0: Do not transmit local error status to remote side through GPIO channel 0b1: Transmit local error status to remote side through GPIO channel
MEM_ERR_ OEN	6	Enables reporting of line memory read/write errors at ERRB pin.	0b0: Disable MEM_ERR error reporting at ERRB pin 0b1: Enable MEM_ERR error reporting at ERRB pin
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX.	0bXXXXX: GPIO ID used for transmitting ERR_TX

**INTR13 (0x30)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ERR_RX_E N_A	–	–	–	–	–	–	ERR_RX_ID_A[4:0]
<b>Reset</b>	0b1	–	–	–	–	–	–	0x1F
<b>Access Type</b>	Write, Read	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN _A	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link A.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link A 0b1: Receive remote error status through GPIO channel for GMSL2 Link A
ERR_RX_ID _A	4:0	GPIO ID used for receiving ERR_RX for GMSL2 Link A.	0bXXXXX: GPIO ID used for receiving ERR_RX Link A

**INTR14 (0x31)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ERR_RX_E N_B	–	–	–	–	–	–	ERR_RX_ID_B[4:0]
<b>Reset</b>	0b1	–	–	–	–	–	–	0x1F
<b>Access Type</b>	Write, Read	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_B	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link B.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link B 0b1: Receive remote error status through GPIO channel for GMSL2 Link B
ERR_RX_ID_B	4:0	GPIO ID used for receiving ERR_RX for GMSL2 Link B.	0bXXXXX: GPIO ID used for receiving ERR_RX Link B

**INTR15 (0x32)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ERR_RX_E_N_C	–	–					ERR_RX_ID_C[4:0]
<b>Reset</b>	0b1	–	–					0x1F
<b>Access Type</b>	Write, Read	–	–					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_C	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link C.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link C 0b1: Receive remote error status through GPIO channel for GMSL2 Link C
ERR_RX_ID_C	4:0	GPIO ID used for receiving ERR_RX for GMSL2 link C	0bXXXXX: GPIO ID used for receiving ERR_RX link C

**INTR16 (0x33)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ERR_RX_E_N_D	–	–					ERR_RX_ID_D[4:0]
<b>Reset</b>	0b1	–	–					0x1F
<b>Access Type</b>	Write, Read	–	–					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_D	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link D.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link D 0b1: Receive remote error status through GPIO channel for GMSL2 Link D
ERR_RX_ID_D	4:0	GPIO ID used for receiving ERR_RX for GMSL2 link D	0bXXXXX: GPIO ID used for receiving ERR_RX link D

**CNT0 (0x35)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DEC_ERR_A[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	The number of decoding (disparity) errors detected at Link A  Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

**CNT1 (0x36)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DEC_ERR_B[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Clears All							
BITFIELD	BITS	DESCRIPTION						DECODE
DEC_ERR_B	7:0	The number of decoding (disparity) errors detected at Link B  Reset after reading or with the rising edge of LOCK.						0xXX: Number of Link B decoding errors detected

**CNT2 (0x37)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DEC_ERR_C[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Clears All							
BITFIELD	BITS	DESCRIPTION						DECODE
DEC_ERR_C	7:0	The number of decoding (disparity) errors detected at Link C  Reset after reading or with the rising edge of LOCK.						0xXX: Number of Link C decoding errors detected

**CNT3 (0x38)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DEC_ERR_D[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Clears All							
BITFIELD	BITS	DESCRIPTION						DECODE
DEC_ERR_D	7:0	The number of decoding (disparity) errors detected at Link D  Reset after reading or with the rising edge of LOCK.						0xXX: Number of Link D decoding errors detected

CNT4 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BITFIELD	BITS	DESCRIPTION				DECODE		
IDLE_ERR_A	7:0	The number of idle word errors detected at Link A Reset after reading or with the rising edge of LOCK.				0xXX: Number of idle word errors detected		

CNT5 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BITFIELD	BITS	DESCRIPTION				DECODE		
IDLE_ERR_B	7:0	The number of idle word errors detected at Link B Reset after reading or with the rising edge of LOCK.				0xXX: Number of idle word errors detected		

CNT6 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_C[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BITFIELD	BITS	DESCRIPTION				DECODE		
IDLE_ERR_C	7:0	The number of idle word errors detected at Link C Reset after reading or with the rising edge of LOCK.				0xXX: Number of idle word errors detected		

CNT7 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_D[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BITFIELD	BITS	DESCRIPTION				DECODE		

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_D	7:0	Number of idle word errors detected at Link D Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

**CNT8 (0x40)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PKT_CNT_A[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_A	7:0	The Number of Received Packets of a Selected Type at Link A  Packet type is selected with the associated PKT_CNT_SEL bitfield (0x1004).  Reported packet count is a scaled value, such that actual packet count is $\geq$ $PKT\_CNT\_A \times (2^{PKT\_CNT\_EXP})$ and $<$ $(PKT\_CNT\_A + 1) \times (2^{PKT\_CNT\_EXP})$ . (PKT_CNT_EXP bitfield is at 0x24.)  When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

**CNT9 (0x41)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PKT_CNT_B[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_B	7:0	The Number of Received Packets of a Selected Type at Link B  Packet type is selected with the associated PKT_CNT_SEL bitfield (0x1014).  Reported packet count is a scaled value, such that actual packet count is $\geq$ $PKT\_CNT\_B \times (2^{PKT\_CNT\_EXP})$ and $<$ $(PKT\_CNT\_B + 1) \times (2^{PKT\_CNT\_EXP})$ . (PKT_CNT_EXP bitfield is at 0x24.)  When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

CNT10 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_C[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BITFIELD	BITS	DESCRIPTION			DECODE			
PKT_CNT_C	7:0	The Number of Received Packets of a Selected Type at Link C  Packet type is selected with the associated PKT_CNT_SEL bitfield (0x1024).  Reported packet count is a scaled value, such that actual packet count is $\geq$ $PKT\_CNT\_C \times (2^{PKT\_CNT\_EXP})$ and $<$ $(PKT\_CNT\_C + 1) \times (2^{PKT\_CNT\_EXP})$ . (PKT_CNT_EXP bitfield is at 0x24.)  When maximum value is reported, packet count is greater or equal to the reported value.			0xXX: Scaled number of received packets			

CNT11 (0x43)

BIT	7	6	5	4	3	2	1	0	
Field	PKT_CNT_D[7:0]								
Reset	0x00								
Access Type	Read Clears All								
BITFIELD	BITS	DESCRIPTION			DECODE				
PKT_CNT_D	7:0	The Number of Received Packets of a Selected Type at Link D  Packet type is selected with the associated PKT_CNT_SEL bitfield (0x1034).  Reported packet count is a scaled value, such that actual packet count is $\geq$ $PKT\_CNT\_D \times (2^{PKT\_CNT\_EXP})$ and $<$ $(PKT\_CNT\_D + 1) \times (2^{PKT\_CNT\_EXP})$ . (PKT_CNT_EXP bitfield is at 0x24.)  When maximum value is reported, packet count is greater or equal to the reported value.				0xXX: Scaled number of received packets			

VID\_PXL\_CRC\_ERR\_OEN (0x44)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MEM_ECC_ERR2_OEN	MEM_ECC_ERR1_OEN	–	–	VID_PXL_C_RC_ERR_OEN_D	VID_PXL_C_RC_ERR_OEN_C	VID_PXL_C_RC_ERR_OEN_B	VID_PXL_C_RC_ERR_OEN_A
<b>Reset</b>	0x1	0x0	–	–	0x1	0x1	0x1	0x1
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ECC_ERR2_OEN	7	Enables reporting of memory ECC 2-bit uncorrectable errors at ERRB pin.	0b0: Disable reporting of 2b ECC memory errors 0b1: Enable reporting of 2b ECC memory errors
MEM_ECC_ERR1_OEN	6	Enables reporting of memory ECC 1-bit correctable errors at ERRB pin.	0b0: Disable reporting of 1b ECC memory errors 0b1: Enable reporting of 1b ECC memory errors
VID_PXL_C_RC_ERR_OEN_D	3	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_C_RC_ERR_OEN_C	2	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_C_RC_ERR_OEN_B	1	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_C_RC_ERR_OEN_A	0	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output

VID\_PXL\_CRC\_ERR\_INT (0x45)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MEM_ECC_ERR2_INT	MEM_ECC_ERR1_INT	–	–	VID_PXL_C_RC_ERR_D	VID_PXL_C_RC_ERR_C	VID_PXL_C_RC_ERR_B	VID_PXL_C_RC_ERR_A
<b>Reset</b>	0b0	0b0	–	–	0x0	0x0	0x0	0x0
<b>Access Type</b>	Read Only	Read Only	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ECC_ERR2_INT	7	Decoding Error Flag for 2-bit Uncorrectable Memory ECC Errors  Asserted when $\text{MEM\_ECC\_ERR2\_CNT} (0x1252) \geq \text{MEM\_ECC\_ERR2\_THR} (0x1250)$ .	0b0: 2b ECC memory error not detected 0b1: 2b ECC memory error detected
MEM_ECC_ERR1_INT	6	Decoding Error Flag for 1-bit Correctable Memory ECC Errors  Asserted when $\text{MEM\_ECC\_ERR1\_CNT} (0x1251) \geq \text{MEM\_ECC\_ERR1\_THR} (0x1250)$ .	0b0: 1b ECC memory error not detected 0b1: 1b ECC memory error detected

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_D	3	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected
VID_PXL_CRC_ERR_C	2	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected
VID_PXL_CRC_ERR_B	1	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected
VID_PXL_CRC_ERR_A	0	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected

PWR\_STATUS\_OEN (0x46)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_IN_T_OEN	—	VDBBAD_IN_T_OEN	—	—	—	—	—
Reset	0x1	—	0x1	—	—	—	—	—
Access Type	Write, Read	—	Write, Read	—	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_IN_T_OEN	7	Enables reporting of V <sub>DD</sub> comparator interrupt (VDDCMP_INT_FLAG) at ERRB pin	0b0: ERRB reporting disabled 0b1: ERRB reporting enabled
VDBBAD_IN_T_OEN	5	Enables reporting of VDBBAD interrupt (VDBBAD_INT_FLAG) at ERRB pin	0b0: ERRB reporting disabled 0b1: ERRB reporting enabled

PWR\_STATUS\_FLAG (0x47)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_IN_T_FLAG	—	VDBBAD_IN_T_FLAG	—	—	—	—	—
Reset	0x0	—	0x0	—	—	—	—	—
Access Type	Read Clears All	—	Read Clears All	—	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_IN_T_FLAG	7	Combined V <sub>DD</sub> Comparator Output Flag.  See CMP_STATUS for details of error states that drive this flag. To clear, first read CMP_STATUS and then read VDDCMP_INT_FLAG.	0b0: No V <sub>DD</sub> comparator error 0b1: V <sub>DD</sub> comparator error state asserted

BITFIELD	BITS	DESCRIPTION	DECODE
VDBBAD_IN_T_FLAG	5	Combined V <sub>DD</sub> Bad Indicator.  See VDBBAD_STATUS for details for error states that drive this flag. To clear, first read VDBBAD_STATUS and then read VDBBAD_INT_FLAG.	0b0: No V <sub>DD</sub> bad error 0b1: V <sub>DD</sub> bad error state asserted

PM OV\_STAT (0x48)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	OV_LEVEL[1:0]	
<b>Reset</b>	—	—	—	—	—	—	0x1	
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
OV_LEVEL	1:0	V <sub>DD</sub> _sw overvoltage comparator trip level V <sub>trip_ov</sub>						0x0: 1.12 0x1: 1.14 0x2: 1.17 0x3: 1.20

VIDEO\_MASKED\_OEN (0x49)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	CMP_VTER_M_MASK	VDD_OV_OEN	VIDEO_MASKED_3_OEN	VIDEO_MASKED_2_OEN	VIDEO_MASKED_1_OEN	VIDEO_MASKED_0_OEN
<b>Reset</b>	—	—	0x1	0x0	0x1	0x1	0x1	0x1
<b>Access Type</b>	—	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION						DECODE
CMP_VTER_M_MASK	5	Select V <sub>DD</sub> comparator V <sub>TERM</sub> status to drive VDDCMP error flag and ERRB pin						0b0: Disable V <sub>TERM</sub> comparator error reporting 0b1: Enable V <sub>TERM</sub> comparator error reporting
VDD_OV_OEN	4	Enable V <sub>DD</sub> overvoltage status on ERRB						0b0: Do not enable V <sub>DD</sub> overvoltage status 0b1: Enable V <sub>DD</sub> overvoltage status
VIDEO_MASKED_3_OEN	3	Enable Video Masked 3 status on ERRB						0b0: Disable reporting of Video Masked 3 Interrupt at ERRB pin 0b1: Enable reporting of Video Masked 3 Interrupt at ERRB pin
VIDEO_MASKED_2_OEN	2	Enable Video Masked 2 status on ERRB						0b0: Disable reporting of Video Masked 2 Interrupt at ERRB pin 0b1: Enable reporting of Video Masked 2 Interrupt at ERRB pin
VIDEO_MASKED_1_OEN	1	Enable Video Masked 1 status on ERRB						0b0: Disable reporting of Video Masked 1 Interrupt at ERRB pin 0b1: Enable reporting of Video Masked 1 Interrupt at ERRB pin
VIDEO_MASKED_0_OEN	0	Enable Video Masked 0 status on ERRB						0b0: Disable reporting of Video Masked 0 Interrupt at ERRB pin 0b1: Enable reporting of Video Masked 0 Interrupt at ERRB pin

VIDEO\_MASKED\_FLAG (0x4A)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	CMP_VTER_M_STATUS	VDD_OV_FLAG	VIDEO_MA_SKED_3_FLAG	VIDEO_MA_SKED_2_FLAG	VIDEO_MA_SKED_1_FLAG	VIDEO_MA_SKED_0_FLAG
<b>Reset</b>	—	—	0x0	0x0	0x0	0x0	0x0	0x0
<b>Access Type</b>	—	—	Read Only	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
CMP_VTER_M_STATUS	5	Power Manager VTERM Comparator Status.  Latched low when switched VTERM supply < 1V. Cleared when the CMP_STATUS word (register 0x12) is read and the switched VTERM supply is > 1V.	0b0: VTERM < 1V (latched low, read to clear) 0b1: VTERM > 1V
VDD_OV_FLAG	4	VDD Overvoltage Indication.  This bit is sticky. It is set when VDD is over the overvoltage threshold. It is cleared when read.  See OV_LEVEL register for overvoltage threshold value.	0b0: VDD_sw overvoltage condition not detected 0b1: VDD_sw overvoltage condition detected (latched, read to clear)
VIDEO_MAS_KED_3_FLAG	3	Sticky Status value for Video Masked 3.  Flag will be set if any of the video pipes used in Controller 3 synchronous aggregation lose video lock.  See video_masked registers in MIPI_TX_x registers to determine which video pipe has been masked.	0b0: Video not masked in Controller 3 synchronous aggregation 0b1: Video masked in at least one pipe in Controller 3 synchronous aggregation
VIDEO_MAS_KED_2_FLAG	2	Sticky Status value for Video Masked 2.  Flag will be set if any of the video pipes used in Controller 2 synchronous aggregation lose video lock.  See video_masked registers in MIPI_TX_x registers to determine which video pipe has been masked.	0b0: Video not masked in Controller 2 synchronous aggregation 0b1: Video masked in at least one pipe in Controller 2 synchronous aggregation
VIDEO_MAS_KED_1_FLAG	1	Sticky Status value for Video Masked 1.  Flag will be set if any of the video pipes used in Controller 1 synchronous aggregation lose video lock.  See video_masked registers in MIPI_TX_x registers to determine which video pipe has been masked.	0b0: Video not masked in Controller 1 synchronous aggregation 0b1: Video masked in at least one pipe in Controller 1 synchronous aggregation

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_MAS KED_0_FLA G	0	<p>Sticky Status value for Video Masked 0.</p> <p>Flag will be set if any of the video pipes used in Controller 0 synchronous aggregation lose video lock.</p> <p>See video_masked registers in MIPI_TX_x registers to determine which video pipe has been masked.</p>	<p>0b0: Video not masked in Controller 0 synchronous aggregation</p> <p>0b1: Video masked in at least one pipe in Controller 0 synchronous aggregation</p>

**DEV\_REV (0x4C)**

BIT	7	6	5	4	3	2	1	0				
<b>Field</b>	—	—	—	—	DEV_REV[3:0]							
<b>Reset</b>	—	—	—	—	0x5							
<b>Access Type</b>	—	—	—	—	Read Only							
BITFIELD	BITS	DESCRIPTION				DECODE						
DEV_REV	3:0	Device Revision A1 -0 A2 -1 B1 -2 C1 -3 D1 -4 E1 -5				0xX: Device revision number						

**RX0 (0x50)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	—	—	—	—	—	—	STR_SEL[1:0]				
<b>Reset</b>	—	—	—	—	—	—	0x0				
<b>Access Type</b>	—	—	—	—	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE					
STR_SEL	1:0	Receives packets with selected stream ID.				0bXX: Receive packets with this stream ID					

**RX0 (0x51)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	—	—	—	—	—	—	STR_SEL[1:0]				
<b>Reset</b>	—	—	—	—	—	—	0x1				
<b>Access Type</b>	—	—	—	—	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE					
STR_SEL	1:0	Receives packets with selected stream ID.				0bXX: Receive packets with this stream ID					

RX0 (0x52)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL[1:0]	
<b>Reset</b>	—	—	—	—	—	—	—	0x2
<b>Access Type</b>	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
STR_SEL	1:0	Receives packets with selected stream ID.				0bXX: Receive packets with this stream ID		

RX0 (0x53)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL[1:0]	
<b>Reset</b>	—	—	—	—	—	—	—	0x3
<b>Access Type</b>	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
STR_SEL	1:0	Receives packets with selected stream ID.				0bXX: Receive packets with this stream ID		

RX0 (0x54)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL_B[1:0]	
<b>Reset</b>	—	—	—	—	—	—	—	0x0
<b>Access Type</b>	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
STR_SEL_B	1:0	Receives packets with selected stream ID.				0bXX: Receive packets with this stream ID		

RX0 (0x55)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL_B[1:0]	
<b>Reset</b>	—	—	—	—	—	—	—	0x1
<b>Access Type</b>	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
STR_SEL_B	1:0	Receives packets with selected stream ID.				0bXX: Receive packets with this stream ID		

RX0 (0x56)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL_B[1:0]	
<b>Reset</b>	—	—	—	—	—	—	—	0x2
<b>Access Type</b>	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_B	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

**RX0 (0x57)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL_B[1:0]	
<b>Reset</b>	—	—	—	—	—	—		0x3
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
STR_SEL_B	1:0	Receives packets with selected stream ID.						0bXX: Receive packets with this stream ID

**RX0 (0x58)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL_C[1:0]	
<b>Reset</b>	—	—	—	—	—	—		0x0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
STR_SEL_C	1:0	Receives packets with selected stream ID.						0bXX: Receive packets with this stream ID

**RX0 (0x59)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL_C[1:0]	
<b>Reset</b>	—	—	—	—	—	—		0x1
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
STR_SEL_C	1:0	Receives packets with selected stream ID.						0bXX: Receive packets with this stream ID

**RX0 (0x5A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	STR_SEL_C[1:0]	
<b>Reset</b>	—	—	—	—	—	—		0x2
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
STR_SEL_C	1:0	Receives packets with selected stream ID.						0bXX: Receive packets with this stream ID

RX0 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	STR_SEL_C[1:0]	
Reset	—	—	—	—	—	—	0x3	
Access Type	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
STR_SEL_C	1:0	Receives packets with selected stream ID.						0bXX: Receive packets with this stream ID

RX0 (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	STR_SEL_D[1:0]	
Reset	—	—	—	—	—	—	0x0	
Access Type	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
STR_SEL_D	1:0	Receives packets with selected stream ID.						0bXX: Receive packets with this stream ID

RX0 (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	STR_SEL_D[1:0]	
Reset	—	—	—	—	—	—	0x1	
Access Type	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
STR_SEL_D	1:0	Receives packets with selected stream ID.						0bXX: Receive packets with this stream ID

RX0 (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	STR_SEL_D[1:0]	
Reset	—	—	—	—	—	—	0x2	
Access Type	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE
STR_SEL_D	1:0	Receives packets with selected stream ID.						0bXX: Receive packets with this stream ID

RX0 (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	STR_SEL_D[1:0]	
Reset	—	—	—	—	—	—	0x3	
Access Type	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION						DECODE

BITFIELD	BITS	DESCRIPTION	DECODE
STR_SEL_D	1:0	Receives packets with selected stream ID.	0bXX: Receive packets with this stream ID

CFGH\_VIDEO\_CRC0 (0x60)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_CRC_EN_A_B[7:0]							
<b>Reset</b>	0b0							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION		DECODE				
RX_CRC_EN_A_B	7:0	Received Packet CRC Enable for Ports A and B  Each bit enables CRC for one pipe within a GMSL link as described below. Setting a given bit indicates that packets received at the corresponding port/pipe have appended CRC and CRC checking must be performed at each packet.  bit 0: RX_CRC_EN_A_VIDEO_X bit 1: RX_CRC_EN_A_VIDEO_Y bit 2: RX_CRC_EN_A_VIDEO_Z bit 3: RX_CRC_EN_A_VIDEO_U bit 4: RX_CRC_EN_B_VIDEO_X bit 5: RX_CRC_EN_B_VIDEO_Y bit 6: RX_CRC_EN_B_VIDEO_Z bit 7: RX_CRC_EN_B_VIDEO_U		0bXXXXXXXX0: No CRC on received packets—RX_CRC_EN_A_VIDEO_X 0bXXXXXXXX1: Received packets have CRC and checking is enabled—RX_CRC_EN_A_VIDEO_X 0bXXXXXXXX0X: No CRC on received packets—RX_CRC_EN_A_VIDEO_Y 0bXXXXXXXX1X: Received packets have CRC and checking is enabled—RX_CRC_EN_A_VIDEO_Y . . . 0b0XXXXXXXX: No CRC on received packets—RX_CRC_EN_B_VIDEO_U 0b1XXXXXXXX: Received packets have CRC and checking is enabled—RX_CRC_EN_B_VIDEO_U				

CFGH\_VIDEO\_CRC1 (0x61)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_CRC_EN_C_D[7:0]							
<b>Reset</b>	0b0							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION		DECODE				

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_C_D	7:0	<p>Received Packet CRC Enable for Ports C and D</p> <p>Each bit enables CRC for one pipe within a GMSL link as described below. Setting a given bit indicates that packets received at the corresponding port/pipe have appended CRC and CRC checking must be performed at each packet.</p> <p>bit 0: RX_CRC_EN_C_VIDEO_X            bit 1: RX_CRC_EN_C_VIDEO_Y            bit 2: RX_CRC_EN_C_VIDEO_Z            bit 3: RX_CRC_EN_C_VIDEO_U            bit 4: RX_CRC_EN_D_VIDEO_X            bit 5: RX_CRC_EN_D_VIDEO_Y            bit 6: RX_CRC_EN_D_VIDEO_Z            bit 7: RX_CRC_EN_D_VIDEO_U</p>	<p>0bXXXXXXXX0: No CRC on received packets—RX_CRC_EN_C_VIDEO_X            0bXXXXXXXX1: Received packets have CRC and checking is enabled—RX_CRC_EN_C_VIDEO_X            0bXXXXXXXX0X: No CRC on received packets—RX_CRC_EN_C_VIDEO_Y            0bXXXXXXXX1X: Received packets have CRC and checking is enabled—RX_CRC_EN_C_VIDEO_Y            .            .            .            0bXXXXXXXX: No CRC on received packets—RX_CRC_EN_D_VIDEO_U            0b1XXXXXXXX: Received packets have CRC and checking is enabled—RX_CRC_EN_D_VIDEO_U</p>

TR0 (0x70)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_E_N	RX_CRC_E_N	—	—	PRIO_VAL[1:0]	—	—	—
Reset	0b1	0b1	—	—	0x0	—	—	—
Access Type	Write, Read	Write, Read	—	—	Write, Read	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0x71)

BIT	7	6	5	4	3	2	1	0			
Field	BW_MULT[1:0]					BW_VAL[5:0]					
Reset	0x2					0x30					
Access Type	Write, Read					Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE						
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.			0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16						

BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base.  Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

**TR2 (0x72)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	TX_SRC_ID[2:0]		
<b>Reset</b>	—	—	—	—	—	0x0		
<b>Access Type</b>	—	—	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

**TR3 (0x73)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_SRC_SEL[7:0]							
<b>Reset</b>	0xFF							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
RX_SRC_SEL	7:0	Receives packets from selected sources  Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.				0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received		

**TR0 (0x74)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_B	RX_CRC_E_N_B	—	—	PRIO_VAL_B[1:0]		—	—
<b>Reset</b>	0b1	0b1	—	—	0x0		—	—
<b>Access Type</b>	Write, Read	Write, Read	—	—	Write, Read		—	—
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port.				0b0: Transmit CRC disabled 0b1: Transmit CRC enabled		

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIOR_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

**TR1 (0x75)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT_B[1:0]							BW_VAL_B[5:0]
<b>Reset</b>	0x2							0x30
<b>Access Type</b>	Write, Read			Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor.			0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16			
BW_VAL_B	5:0	Channel bandwidth-allocation base.  Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth			0bXXXXXX: Channel base-bandwidth value			

**TR2 (0x76)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	—	—	—	—	—	TX_SRC_ID_B[2:0]					
<b>Reset</b>	—	—	—	—	—	0x0					
<b>Access Type</b>	—	—	—	—	—	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE						
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.			0bXXX: Source ID for packets from this channel						

**TR3 (0x77)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_SRC_SEL_B[7:0]							
<b>Reset</b>	0xFF							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SE_L_B	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

**TR0 (0x78)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_C	RX_CRC_E_N_C	—	—	PRIO_VAL_C[1:0]	—	—	—
<b>Reset</b>	0b1	0b1	—	—	0x0	—	—	—
<b>Access Type</b>	Write, Read	Write, Read	—	—	Write, Read	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

**TR1 (0x79)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
<b>Reset</b>	0x2		0x30					
<b>Access Type</b>	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR2 (0x7A)

BIT	7	6	5	4	3	2	1	0			
Field	—	—	—	—	—	TX_SRC_ID_C[2:0]					
Reset	—	—	—	—	—	0x0					
Access Type	—	—	—	—	—	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE						
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.			0bXXX: Source ID for packets from this channel						

TR3 (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
RX_SRC_SEL_C	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.			0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received			

TR0 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_E_N_D	RX_CRC_E_N_D	—	—	PRIO_VAL_D[1:0]		—	—
Reset	0b1	0b1	—	—	0x0		—	—
Access Type	Write, Read	Write, Read	—	—	Write, Read		—	—
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port			0b0: Transmit CRC disabled 0b1: Transmit CRC enabled			
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.			0b0: Receive CRC disabled 0b1: Receive CRC enabled			
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests.			0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority			

TR1 (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]							
Reset	0x2							
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor				0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16		
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value		

TR2 (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID_D[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR3 (0x7F)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
RX_SRC_SEL_D	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.				0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received		

PRELIMINARY

TR0 (0x80)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]			
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0			
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE				
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port.				0b0: Transmit CRC disabled 0b1: Transmit CRC enabled				
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.				0b0: Receive CRC disabled 0b1: Receive CRC enabled				
PRIO_VAL	3:2	Sets the priority for this channel's packet requests				0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority				
PRIO_CFG	1:0	Adjust the priority used for this channel.				0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting				

TR1 (0x81)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT[1:0]			BW_VAL[5:0]				
<b>Reset</b>	0x2			0x30				
<b>Access Type</b>	Write, Read			Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.				0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16		
BW_VAL	5:0	Channel bandwidth allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT / 10 as a percentage of total link bandwidth.				0bXXXXXX: Channel base-bandwidth value		

TR3 (0x83)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	–	–	–	TX_SRC_ID[2:0]		
<b>Reset</b>	–	–	–	–	–	0x0		
<b>Access Type</b>	–	–	–	–	–	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR4 (0x84)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_SRC_SEL[7:0]							
<b>Reset</b>	0xFF							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.			0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received			

ARQ0 (0x85)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	ACK_SRC_ID	ARQ_EN	ARQ_EN	—	—
<b>Reset</b>	—	—	—	0b1	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	Write, Read	Write, Read	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION			DECODE			
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets			0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register			
ARQ_EN	3	Enable ARQ			0b0: ARQ disabled 0b1: ARQ enabled			
ARQ_EN	2	Disables retransmission due to receiving same ACK twice			0b0: Enabled 0b1: Disabled			

ARQ1 (0x86)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MAX_RT[2:0]					MAX_RT_E RR_OEN	RT_CNT_O EN
<b>Reset</b>	—	0x7					0b1	0b0
<b>Access Type</b>	—	Write, Read					Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION			DECODE			
MAX_RT	6:4	Maximum Retransmit Limit ARQ will stop retransmission after trying retransmit for this many times for a single packet.			0bXXX: Maximum retransmit limit			

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_R_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0x87) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OE_N	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0x87) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x87)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR	RT_CNT[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						
BITFIELD	BITS	DESCRIPTION			DECODE			
MAX_RT_ER_R	7	Reached maximum retransmit limit (MAX_RT—0x86) for one packet in this channel.			0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached			
RT_CNT	6:0	Total retransmission count in this channel.			0bXXXXXXXX: Count of retransmissions for this channel			

TR0 (0x90)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		–	–
<b>Reset</b>	0b1	0b1	–	–	0x0		–	–
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		–	–
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.			0b0: Transmit CRC disabled 0b1: Transmit CRC enabled			
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.			0b0: Receive CRC disabled 0b1: Receive CRC enabled			
PRIO_VAL	3:2	Sets the priority for this channel's packet requests			0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority			

TR1 (0x91)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]				BW_VAL[5:0]			
Reset	0x2				0x30			
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor				0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16		
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value		

TR3 (0x93)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR4 (0x94)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.				0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received		

PRELIMINARY

**ARQ0 (0x95)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	ARQ_EN	ARQ_EN	—	—
<b>Reset</b>	—	—	—	—	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
ARQ_EN	3	Enables ARQ					0b0: ARQ disabled 0b1: ARQ enabled	
ARQ_EN	2	Disables retransmission due to receiving same ACK twice					0b0: Enabled 0b1: Disabled	

**ARQ1 (0x96)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MAX_RT[2:0]					MAX_RT_E_RR_OEN	RT_CNT_O_EN
<b>Reset</b>	—	0x7					0b1	0b0
<b>Access Type</b>	—	Write, Read					Write, Read	Write, Read
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAX_RT	6:4	Maximum Retransmit Limit  ARQ will stop retransmission after trying retransmit for this many times for a single packet.					0bXXX: Maximum retransmit limit	
MAX_RT_ER_R_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0x97) for this channel at ERRB pin					0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled	
RT_CNT_OE_N	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0x97) of this channel is greater than 0.					0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled	

**ARQ2 (0x97)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR	RT_CNT[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAX_RT_ER_R	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel					0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached	
RT_CNT	6:0	Total retransmission count in this channel					0bXXXXXXXX: Count of retransmissions for this channel	

TR0 (0xA0)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	TX_CRC_E N	RX_CRC_E N	–	–	PRIO_VAL[1:0]		–	–		
<b>Reset</b>	0b1	0b1	–	–	0x0		–	–		
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		–	–		
BITFIELD	BITS	DESCRIPTION					DECODE			
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.					0b0: Transmit CRC disabled 0b1: Transmit CRC enabled			
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.					0b0: Receive CRC disabled 0b1: Receive CRC enabled			
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.					0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority			

TR1 (0xA1)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT[1:0]				BW_VAL[5:0]			
<b>Reset</b>	0x2				0x30			
<b>Access Type</b>	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION					DECODE	
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor					0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16	
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth					0bXXXXXX: Channel base-bandwidth value	

TR3 (0xA3)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	–	–	–	TX_SRC_ID[2:0]		
<b>Reset</b>	–	–	–	–	–	0x0		
<b>Access Type</b>	–	–	–	–	–	Write, Read		
BITFIELD	BITS	DESCRIPTION					DECODE	
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.					0bXXX: Source ID for packets from this channel	

[TR4 \(0xA4\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_SRC_SEL[7:0]							
<b>Reset</b>	0xFF							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
RX_SRC_SEL	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.			0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . .0xFF: Packets from all source IDs received			

[ARQ0 \(0xA5\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	ARQ_EN	ARQ_EN	—	—
<b>Reset</b>	—	—	—	—	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION			DECODE			
ARQ_EN	3	Enables ARQ			0b0: ARQ disabled 0b1: ARQ enabled			
ARQ_EN	2	Disables retransmission due to receiving same ACK twice			0b0: Enabled 0b1: Disabled			

[ARQ1 \(0xA6\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	MAX_RT_ER_R_OEN	RT_CNT_OEN
<b>Reset</b>	—	—	—	—	—	—	0b1	0b0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION			DECODE			
MAX_RT_ER_R_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0xA7) for this channel at ERRB pin			0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled			
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0xA7) of this channel is greater than 0.			0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled			

**PRELIMINARY**

**ARQ2 (0xA7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E RR	RT_CNT[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER R	7	Reached maximum retransmit limit (MAX_RT—0xA6) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0bXXXXXXXX: Count of retransmissions for this channel

**TR0 (0xA8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E N_B	RX_CRC_E N_B	–	–	PRIO_VAL_B[1:0]		–	–
<b>Reset</b>	0b1	0b1	–	–	0x0		–	–
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN _B	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN _B	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

**TR1 (0xA9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
<b>Reset</b>	0x2		0x30					
<b>Access Type</b>	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXXXX: Channel base-bandwidth value

TR3 (0xAB)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID_B[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR4 (0xAC)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
RX_SRC_SEL_B	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.				0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received		

ARQ0 (0xAD)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	ARQ_EN_B	ARQ_EN	—	—
Reset	—	—	—	—	0b1	0b0	—	—
Access Type	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION				DECODE		
ARQ_EN_B	3	Enables ARQ				0b0: ARQ disabled 0b1: ARQ enabled		
ARQ_EN	2	Disables retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

ARQ1 (0xAE)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	MAX_RT_E RR_OEN_B	RT_CNT_O EN_B
Reset	—	—	—	—	—	—	0b1	0b0
Access Type	—	—	—	—	—	—	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_R_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_B—0xAF) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OE_N_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_B (0xAF) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xAF)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_ER_B	RT_CNT_B[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						
BITFIELD	BITS	DESCRIPTION			DECODE			
MAX_RT_ER_B	7	Reached maximum retransmit limit (MAX_RT_B—0xAE) for one packet in this channel.			0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached			
RT_CNT_B	6:0	Total retransmission count in this channel.			0bXXXXXXXX: Count of retransmissions for this channel			

TR0 (0xB0)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_EN_C	RX_CRC_EN_C	—	—	PRIO_VAL_C[1:0]		—	—
<b>Reset</b>	0b1	0b1	—	—	0x0		—	—
<b>Access Type</b>	Write, Read	Write, Read	—	—	Write, Read		—	—
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port.			0b0: Transmit CRC disabled 0b1: Transmit CRC enabled			
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.			0b0: Receive CRC disabled 0b1: Receive CRC enabled			
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests.			0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority			

TR1 (0xB1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]							
Reset	0x2							
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor.				0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16		
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value		

TR3 (0xB3)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID_C[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR4 (0xB4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
RX_SRC_SEL_C	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.				0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received		

PRELIMINARY

**ARQ0 (0xB5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	ARQ_EN_C	ARQ_EN	—	—
<b>Reset</b>	—	—	—	—	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN_C	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled
ARQ_EN	2	Disables retransmission due to receiving same ACK twice	0b0: Enabled 0b1: Disabled

**ARQ1 (0xB6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	MAX_RT_E_RR_OEN_C	RT_CNT_O_EN_C
<b>Reset</b>	—	—	—	—	—	—	0b1	0b0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_R_OEN_C	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0xB7) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OE_N_C	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0xB7) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

**ARQ2 (0xB7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR_C	RT_CNT_C[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_R_C	7	Reached maximum retransmit limit (MAX_RT_C—0xB6) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel.	0bXXXXXXXX: Count of retransmissions for this channel

**PRELIMINARY**

TR0 (0xB8)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_D	RX_CRC_E_N_D	–	–	PRIO_VAL_D[1:0]		–	–
<b>Reset</b>	0b1	0b1	–	–	0x0		–	–
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		–	–
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port.				0b0: Transmit CRC disabled 0b1: Transmit CRC enabled		
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.				0b0: Receive CRC disabled 0b1: Receive CRC enabled		
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests.				0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority		

TR1 (0xB9)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT_D[1:0]					BW_VAL_D[5:0]		
<b>Reset</b>	0x2					0x30		
<b>Access Type</b>	Write, Read					Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor.				0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16		
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value		

TR3 (0xBB)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	–	–	–	TX_SRC_ID_D[2:0]		
<b>Reset</b>	–	–	–	–	–	0x0		
<b>Access Type</b>	–	–	–	–	–	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR4 (0xBC)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_SRC_SEL_D[7:0]							
<b>Reset</b>	0xFF							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
RX_SRC_SEL_D	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.			0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . .0xFF: Packets from all source IDs received			

ARQ0 (0xBD)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ARQ_EN_D							
<b>Reset</b>	0b1							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
ARQ_EN_D	3	Enables ARQ			0b0: ARQ disabled 0b1: ARQ enabled			
ARQ_EN	2	Disables retransmission due to receiving same ACK twice.			0b0: Enabled 0b1: Disabled			

ARQ1 (0xBE)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_ER_R_OEN_D							
<b>Reset</b>	0b1							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAX_RT_ER_R_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_D—0xBF) for this channel at ERRB pin			0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled			
RT_CNT_OE_N_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0xBF) of this channel is greater than 0.			0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled			

**ARQ2 (0xBF)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E RR_D	RT_CNT_D[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER R_D	7	Reached maximum retransmit limit (MAX_RT_D—0xBE) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel.	0bXXXXXXXX: Count of retransmissions for this channel

**I2C\_7 (0xC7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	I2C_REGSL V_1_TIMED _OUT	I2C_INTREG_SLV_1_TO[2:0]			I2C_REGSL V_0_TIMED _OUT	I2C_INTREG_SLV_0_TO[2:0]		
<b>Reset</b>	0x0	0x6			0x0	0x6		
<b>Access Type</b>	Read Only	Write, Read			Read Only	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSL V_1_TIMED _OUT	7	Internal I <sup>2</sup> C-to-register slave for Port 1 has timed out while waiting for the master or the internal register access FSM.	0b0: Internal I <sup>2</sup> C-to-register slave for Port 1 has not timed out 0b1: Internal I <sup>2</sup> C-to-register slave for Port 1 has timed out
I2C_INTREG _SLV_1_TO	6:4	I <sup>2</sup> C-to-Internal Register Slave 1 Timeout Setting  Internal register I <sup>2</sup> C Slave 1 times out after the configured duration if it does not receive any response from the external master or internal register FSM. This slave serves I <sup>2</sup> C Port 1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled
I2C_REGSL V_0_TIMED _OUT	3	Internal I <sup>2</sup> C-to-register slave for Port 0 has timed out while waiting for the master or the internal register access FSM.	0b0: Internal I <sup>2</sup> C-to-register slave for Port 0 has not timed out 0b1: Internal I <sup>2</sup> C-to-register slave for Port 0 has timed out
I2C_INTREG _SLV_0_TO	2:0	I <sup>2</sup> C-to-Internal Register Slave 0 Timeout Setting  Internal register I <sup>2</sup> C Slave 0 times out after the configured duration if it does not receive any response from the external master or internal register FSM. This slave serves I <sup>2</sup> C Port 0.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**PRELIMINARY**

**UART\_0 (0xC8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	REM_MS_E_N_0	LOC_MS_E_N_0	BYPASS_D_IS_PAR_0	BYPASS_TO_0[1:0]	BYPASS_E_N_0	
<b>Reset</b>	—	—	0x0	0x0	0x0	0x1	0x0	
<b>Access Type</b>	—	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_E_N_0	5	Enables UART Port 0 bypass mode control by remote GPIO pin.  When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_0	4	Enables UART Port 0 bypass mode control by local GPIO pin.  Set to use GPIO0 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR_0	3	Does not receive and send parity bit in bypass mode (for UART Port 0)	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO_0	2:1	UART Port 0 Soft-Bypass Timeout Duration	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Reserved
BYPASS_EN_0	0	Enables UART Port 0 soft-bypass mode.  Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO_0 bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

**UART\_1 (0xC9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BITLEN_LSB_0[7:0]							
<b>Reset</b>	0x96							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
BITLEN_LSB_0	7:0	UART Port 0 detected bit length, low 8 bits			0XX: UART Port 0 detected bit length, low 8 bits			

UART\_2 (0xCA)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OUT_DELAY_0[1:0]		BITLEN_MSB_0[5:0]					
<b>Reset</b>	0x2		0x0					
<b>Access Type</b>	Write, Read		Read Only					
BITFIELD	BITS	DESCRIPTION			DECODE			
OUT_DELAY_0	7:6	UART Port 0 Initial Output Delay  In base mode, first received UART byte of a packet (SYNC or ACK frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back-to-back on remote side.			0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit			
BITLEN_MS_B_0	5:0	UART Port 0 detected bit length, high 6 bits			0bXXXXXX: UART Port 0 detected bit length, high 6 bits			

UART\_3 (0xCB)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	ARB_TO_LEN_1[1:0]		REM_MS_E_N_1	LOC_MS_E_N_1	BYPASS_D_IS_PAR_1	BYPASS_TO_1[1:0]		BYPASS_E_N_1		
<b>Reset</b>	0x1		0x0	0x0	0x0	0x1		0x0		
<b>Access Type</b>	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		
BITFIELD	BITS	DESCRIPTION			DECODE					
ARB_TO_LEN_1	7:6	UART Port 1 Rx Source Arbitration Timeout Duration  UART Rx processes packets from a single UART source at any time. When UART Rx does not receive any UART packets for this duration, it will select the next UART source according to the source ID of the next following received packet.			0bXX: Arbitration timeout duration					
REM_MS_E_N_1	5	Enables UART Port 1 bypass mode control by remote GPIO pin.  When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is High, chip is in bypass mode, otherwise, chip is in base mode.			0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin					
LOC_MS_EN_1	4	Enables UART Port 1 bypass mode control by local GPIO pin.  Set to use GPIO0 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise chip is in base mode.			0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin					
BYPASS_D_IS_PAR_1	3	Does not receive and send parity bit in bypass mode (for UART Port 1)			0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode					

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
BYPASS_TO_1	2:1	UART Port 1 Soft-Bypass Timeout Duration	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Reserved
BYPASS_EN_1	0	Enables UART Port 1 Soft-Bypass Mode  Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO_1 bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

**UART\_4 (0xCC)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BITLEN_LSB_1[7:0]							
<b>Reset</b>	0x96							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION				DECODE		
BITLEN_LSB_1	7:0	UART Port 1 detected bit length, low 8 bits				0xXX: UART Port 1 detected bit length, low 8 bits		

**UART\_5 (0xCD)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	OUT_DELAY_1[1:0]									
<b>Reset</b>	0x2									
<b>Access Type</b>	Write, Read						Read Only			
BITFIELD	BITS	DESCRIPTION				DECODE				
OUT_DELAY_1	7:6	UART Port 1 Initial Output Delay  In base mode, first received UART byte of a packet (SYNC or ACK frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back-to-back on remote side.				0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit				
BITLEN_MS_B_1	5:0	UART Port 1 detected bit length, high 6 bits				0bXXXXXX: UART Port 1 detected bit length, high 6 bits				

**UART\_6 (0xCE)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	UART_2_LINK_SELECT[1:0]		GMSL1_UART_ARB_TO	GMSL1_UART_ARB_E_N	UART_1_LINK_SELECT[1:0]	UART_0_LINK_SELECT[1:0]		
<b>Reset</b>	0x0		0x0	0x0	0x1	0x0		
<b>Access Type</b>	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
UART_2_LIN_K_SELECT	7:6	<p>UART Port 2 Link Connection Select</p> <p>Note that the GMSL2 UART connections are point-to-point only (this is different from GMSL1 operation).</p> <p>In mixed link operation (i.e. some links enabled for GMSL1 and other links enabled for GMSL2), a UART port will be considered dedicated to GMSL2 if the UART Port 2 link connection decode above matches a link which is enabled for GMSL2 operation. Otherwise, the UART port will operate in GMSL1 mode.</p> <p>See REG6 (0x6) of the DEV register block.</p>	0b00: Link A 0b01: Link B 0b10: Link C 0b11: Link D
GMSL1_UART_ARB_TO	5	GMSL1 UART Arbitration Timeout Value	0b0: 256µs 0b1: 4ms
GMSL1_UART_ARB_EN	4	UART Arbitration Enable on GMSL1 Forward Control Channel Links	0b0: UART arbitration not enabled on GMSL1 forward control channel links 0b1: UART arbitration enabled on GMSL1 forward control channel links
UART_1_LIN_K_SELECT	3:2	<p>UART Port 1 Link Connection Select</p> <p>Note that the GMSL2 UART connections are point-to-point only (this is different from GMSL1 operation).</p> <p>In mixed link operation (i.e. some links enabled for GMSL1 and other links enabled for GMSL2), a UART port will be considered dedicated to GMSL2 if the UART Port 1 link connection decode above matches a link which is enabled for GMSL2 operation. Otherwise, the UART port will operate in GMSL1 mode.</p> <p>See REG6 (0x6) of the DEV register block.</p>	0b00: Link A 0b01: Link B 0b10: Link C 0b11: Link D
UART_0_LIN_K_SELECT	1:0	<p>UART Port 0 Link Connection Select</p> <p>Please note that the GMSL2 UART connections are point-to-point only (this is different from GMSL1 operation).</p> <p>In mixed link operation (i.e. some links enabled for GMSL1 and other links enabled for GMSL2) a UART port will be considered dedicated to GMSL2 if the UART Port 0 link connection decode above matches a link which is enabled for GMSL2 operation. Otherwise, the UART port will operate in GMSL1 mode.</p> <p>See REG6 (0x6) of the DEV register block.</p>	0b00: Link A 0b01: Link B 0b10: Link C 0b11: Link D

**UART\_7 (0xD0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	UART_2_T_X_OVERFL_OW	UART_2_R_X_OVERFL_OW	UART_1_T_X_OVERFL_OW	UART_1_R_X_OVERFL_OW	UART_0_T_X_OVERFL_OW	UART_0_R_X_OVERFL_OW
<b>Reset</b>	—	—	0x0	0x0	0x0	0x0	0x0	0x0
<b>Access Type</b>	—	—	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
UART_2_TX_OVERFLOW	5	UART Port 2 Tx Overflow	0b0: No overflow 0b1: Overflow
UART_2_RX_OVERFLOW	4	UART Port 2 Rx Overflow	0b0: No overflow 0b1: Overflow
UART_1_TX_OVERFLOW	3	UART Port 1 Tx Overflow	0b0: No overflow 0b1: Overflow
UART_1_RX_OVERFLOW	2	UART Port 1 Rx Overflow	0b0: No overflow 0b1: Overflow
UART_0_TX_OVERFLOW	1	UART Port 0 Tx Overflow	0b0: No overflow 0b1: Overflow
UART_0_RX_OVERFLOW	0	UART Port 0 Rx Overflow	0b0: No overflow 0b1: Overflow

**UART\_8 (0xD1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	REM_MS_E_N_2	LOC_MS_E_N_2	BYPASS_D_IS_PAR_2	BYPASS_TO_2[1:0]	BYPASS_E_N_2	
<b>Reset</b>	—	—	0x0	0x0	0x0	0x1	0x0	
<b>Access Type</b>	—	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_E_N_2	5	Enable UART Port 2 bypass mode control by remote GPIO pin.  When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode. Otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN_2	4	Enable UART Port 2 bypass mode control by local GPIO pin.  Set to use GPIO0 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode. Otherwise, chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin

BITFIELD	BITS	DESCRIPTION	DECODE
BYPASS_DI_S_PAR_2	3	Does not receive and send parity bit in bypass mode (for UART Port 2)	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO_2	2:1	UART Port 2 Soft-Bypass Timeout Duration	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Reserved
BYPASS_EN_2	0	Enable UART Port 2 Soft-Bypass Mode  Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO_2 bitfield), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

**UART\_9 (0xD2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BITLEN_LSB_2[7:0]							
<b>Reset</b>	0x96							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION				DECODE		
BITLEN_LSB_2	7:0	UART Port 2 detected bit length, low 8 bits				0xXX: UART Port 2 detected bit length, low 8 bits		

**UART\_10 (0xD3)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	OUT_DELAY_2[1:0]			BITLEN_MSB_2[5:0]					
<b>Reset</b>	0x2			0x0					
<b>Access Type</b>	Write, Read			Read Only					
BITFIELD	BITS	DESCRIPTION				DECODE			
OUT_DELAY_2	7:6	UART Port 2 initial output delay  In base mode, first received UART byte of a packet (SYNC or ACK frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back-to-back on remote side.				0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit			
BITLEN_MS_B_2	5:0	UART Port 2 detected bit length, high 6 bits				0bXXXXXX: UART Port 2 detected bit length, high 6 bits			

**PRELIMINARY**

I2C\_8 (0xD4)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	I2C_REGSL V_2_TIMED _OUT	I2C_INTREG_SLV_2_TO[2:0]		
<b>Reset</b>	—	—	—	—	0x0		0x6	
<b>Access Type</b>	—	—	—	—	Read Only		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSL V_2_TIMED _OUT	3	Internal I <sup>2</sup> C-to-register slave for Port 2 has timed out while waiting for the master or the internal register access FSM.	0b0: Internal I <sup>2</sup> C-to-register slave for Port 2 has not timed out 0b1: Internal I <sup>2</sup> C-to-register slave for Port 2 has timed out
I2C_INTREG _SLV_2_TO	2:0	I <sup>2</sup> C-to-Internal Register Slave 2 Timeout Setting  Internal register I <sup>2</sup> C Slave 2 times out after the configured duration if it does not receive any response from the external master or internal register FSM. This slave serves I <sup>2</sup> C Port 2.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

REG0 (0xE0)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PU_LF7	PU_LF6	PU_LF5	PU_LF4	PU_LF3	PU_LF2	PU_LF1	PU_LF0
<b>Reset</b>	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION					DECODE	
PU_LF7	7	Power-Up Line Fault Monitor 7					0b0: Line fault monitor 7 disabled 0b1: Line fault monitor 7 enabled	
PU_LF6	6	Power-Up Line Fault Monitor 6					0b0: Line fault monitor 6 disabled 0b1: Line fault monitor 6 enabled	
PU_LF5	5	Power-Up Line Fault Monitor 5					0b0: Line fault monitor 5 disabled 0b1: Line fault monitor 5 enabled	
PU_LF4	4	Power-Up Line Fault Monitor 4					0b0: Line fault monitor 4 disabled 0b1: Line fault monitor 4 enabled	
PU_LF3	3	Power-Up Line Fault Monitor 3					0b0: Line fault monitor 3 disabled 0b1: Line fault monitor 3 enabled	
PU_LF2	2	Power-Up Line Fault Monitor 2					0b0: Line fault monitor 2 disabled 0b1: Line fault monitor 2 enabled	
PU_LF1	1	Power-Up Line Fault Monitor 1					0b0: Line fault monitor 1 disabled 0b1: Line fault monitor 1 enabled	
PU_LF0	0	Power-Up Line Fault Monitor 0					0b0: Line fault monitor 0 disabled 0b1: Line fault monitor 0 enabled	

**REG1 (0xE1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	LF_1[2:0]			–	LF_0[2:0]		
<b>Reset</b>	–	0x2			–	0x2		
<b>Access Type</b>	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_1	6:4	Line Fault Status of Wire Connected to LMN1 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short
LF_0	2:0	Line Fault Status of Wire Connected to LMN0 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

**REG2 (0xE2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	LF_3[2:0]			–	LF_2[2:0]		
<b>Reset</b>	–	0x2			–	0x2		
<b>Access Type</b>	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_3	6:4	Line Fault Status of Wire Connected to LMN3 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short
LF_2	2:0	Line Fault Status of Wire Connected to LMN2 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

**REG3 (0xE3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	LF_5[2:0]			–	LF_4[2:0]		
<b>Reset</b>	–	0x2			–	0x2		
<b>Access Type</b>	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_5	6:4	Line Fault Status of Wire Connected to LMN5 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
LF_4	2:0	Line Fault Status of Wire Connected to LMN4 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

**REG4 (0xE4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	LF_7[2:0]					—	LF_6[2:0]
<b>Reset</b>	—	0x2					—	0x2
<b>Access Type</b>	—	Read Only					—	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LF_7	6:4	Line Fault Status of Wire Connected to LMN7 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short
LF_6	2:0	Line Fault Status of Wire Connected to LMN6 Pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

**REG5 (0xE5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	LFLT_INT_FLAG[7:0]							
<b>Reset</b>								
<b>Access Type</b>	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_FLAG	7:0	<p>Latched Line Fault Monitor Error Flags</p> <p>Each bit corresponds to one of the line fault monitor status indicators as detailed in the decode. A line fault is flagged if a given line fault detector is enabled via the PU_LF* bits and the associated LF_* status indicator has a value other than 0b010.</p> <p>Routing of the LFLT_INT_FLAG flags to ERRB is controlled via the MASK_LF* bits. Read LFLT_INT_FLAG register to clear the latched error flag.</p>	0xxxxxxxx0: No Error, Line Fault Monitor 0 0xxxxxxxx1: Error, Line Fault Monitor 0 0xxxxxxxx0x: No Error, Line Fault Monitor 1 0xxxxxxxx1x: Error, Line Fault Monitor 1 0xxxxxx0xx: No Error, Line Fault Monitor 2 0xxxxxx1xx: Error, Line Fault Monitor 2 0xxxxx0xxx: No Error, Line Fault Monitor 3 0xxxxx1xxx: Error, Line Fault Monitor 3 0xxx0xxxx: No Error, Line Fault Monitor 4 0xxx1xxxx: Error, Line Fault Monitor 4 0xx0xxxx: No Error, Line Fault Monitor 5 0xx1xxxx: Error, Line Fault Monitor 5 0bx0xxxx: No Error, Line Fault Monitor 6 0bx1xxxx: Error, Line Fault Monitor 6 0b0xxxxxx: No Error, Line Fault Monitor 7 0b1xxxxxx: Error, Line Fault Monitor 7

**REG6 (0xE6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MASK_LF7	MASK_LF6	MASK_LF5	MASK_LF4	MASK_LF3	MASK_LF2	MASK_LF1	MASK_LF0
<b>Reset</b>	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MASK_LF7	7	Mask Line Fault Monitor 7 Interrupt					0b0: Line fault monitor 7 interrupt enabled 0b1: Line fault monitor 7 interrupt masked	
MASK_LF6	6	Mask Line Fault Monitor 6 Interrupt					0b0: Line fault monitor 6 interrupt enabled 0b1: Line fault monitor 6 interrupt masked	
MASK_LF5	5	Mask Line Fault Monitor 5 Interrupt					0b0: Line fault monitor 5 interrupt enabled 0b1: Line fault monitor 5 interrupt masked	
MASK_LF4	4	Mask Line Fault Monitor 4 Interrupt					0b0: Line fault monitor 4 interrupt enabled 0b1: Line fault monitor 4 interrupt masked	
MASK_LF3	3	Mask Line Fault Monitor 3 Interrupt					0b0: Line fault monitor 3 interrupt enabled 0b1: Line fault monitor 3 interrupt masked	
MASK_LF2	2	Mask Line Fault Monitor 2 Interrupt					0b0: Line fault monitor 2 interrupt enabled 0b1: Line fault monitor 2 interrupt masked	
MASK_LF1	1	Mask Line Fault Monitor 1 Interrupt					0b0: Line fault monitor 1 interrupt enabled 0b1: Line fault monitor 1 interrupt masked	
MASK_LF0	0	Mask Line Fault Monitor 0 Interrupt					0b0: Line fault monitor 0 interrupt enabled 0b1: Line fault monitor 0 interrupt masked	

**VIDEO\_PIPE\_SEL\_0 (0xF0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VIDEO_PIPE_SEL_1[3:0]					VIDEO_PIPE_SEL_0[3:0]		
<b>Reset</b>	0x6					0x2		
<b>Access Type</b>	Write, Read					Write, Read		

BITFIELD	BITS	<b>DESCRIPTION</b>	<b>DECODE</b>
VIDEO_PIPE_SEL_1	7:4	Video Pipe 1 Input Selection Control  bits [7:6]: GMSL2 Phy Link selection for Pipe 1 bits [5:4]: Input Pipe selection for Pipe 1	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_0	3:0	Video Pipe 0 Input Selection Control bits [3:2]: GMSL2 Phy Link selection for Pipe 0 bits [1:0]: Input Pipe selection for Pipe 0	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO PIPE SEL\_1 (0xF1)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VIDEO_PIPE_SEL_3[3:0]						VIDEO_PIPE_SEL_2[3:0]	
<b>Reset</b>	0xe						0xa	
<b>Access Type</b>	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_3	7:4	Video Pipe 3 Selection bits [7:6]: GMSL2 Phy Link selection for Pipe 3 bits [5:4]: Input Pipe selection for Pipe 3	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U
VIDEO_PIPE_SEL_2	3:0	Video Pipe 2 Selection bits [3:2]: GMSL2 Phy Link selection for Pipe 2 bits [1:0]: Input Pipe selection for Pipe 2	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO\_PIPE\_SEL\_2 (0xF2)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VIDEO_PIPE_SEL_5[3:0]						VIDEO_PIPE_SEL_4[3:0]	
<b>Reset</b>	0x4						0x0	
<b>Access Type</b>	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_5	7:4	Video Pipe 5 Selection bits [7:6]: GMSL2 Phy Link selection for Pipe 5 bits [5:4]: Input Pipe selection for Pipe 5	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U
VIDEO_PIPE_SEL_4	3:0	Video Pipe 4 Selection bits [3:2]: GMSL2 Phy Link selection for Pipe 4 bits [1:0]: Input Pipe selection for Pipe 4	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO\_PIPE\_SEL\_3 (0xF3)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VIDEO_PIPE_SEL_7[3:0]					VIDEO_PIPE_SEL_6[3:0]		
<b>Reset</b>	0xc					0x8		
<b>Access Type</b>	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_7	7:4	Video Pipe 7 Selection bits [7:6]: GMSL2 Phy Link selection for Pipe 7 bits [5:4]: Input Pipe selection for Pipe 7	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U
VIDEO_PIPE_SEL_6	3:0	Video Pipe 6 Selection bits [3:2]: GMSL2 Phy Link selection for Pipe 6 bits [1:0]: Input Pipe selection for Pipe 6	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO PIPE EN (0xF4)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VIDEO_PIPE_EN[7:0]							
<b>Reset</b>	0x0F							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
VIDEO_PIPE_EN	7:0	Video Pipe Enable Register			0bXXXXXXXX0: Disable Pipe 0 0bXXXXXXXX1: Enable Pipe 0 0bXXXXXX0X: Disable Pipe 1 0bXXXXXX1X: Enable Pipe 1 0bXXXXXX0XX: Disable Pipe 2 0bXXXXXX1XX: Enable Pipe 2 0bXXXX0XXX: Disable Pipe 3 0bXXXX1XXX: Enable Pipe 3 0bXXX0XXXX: Disable Pipe 4 0bXXX1XXXX: Enable Pipe 4 0bXX0XXXXX: Disable Pipe 5 0bXX1XXXXX: Enable Pipe 5 0bX0XXXXXX: Disable Pipe 6 0bX1XXXXXX: Enable Pipe 6 0b0XXXXXXX: Disable Pipe 7 0b1XXXXXXX: Enable Pipe 7			

HVD GPIO CTRL\_0 (0xFA)

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	—	DE_EN	HS_EN	VS_EN	—	HVD_SEL[2:0]					
<b>Reset</b>	—	0x0	0x0	0x0	—	0x0					
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read	—	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE						
DE_EN	6	DE Enable Enables DE to be muxed out to GPIO.			0b0: Disable multiplexing of DE out to GPIO 0b1: Enable multiplexing of DE out to GPIO						
HS_EN	5	HS Enable Enables HS to be muxed out to GPIO.			0b0: Disable multiplexing of HS out to GPIO 0b1: Enable multiplexing of HS out to GPIO						
VS_EN	4	Enable VS Enables VS to be muxed out to GPIO.			0b0: Disable multiplexing of VS out to GPIO 0b1: Enable multiplexing of VS out to GPIO						
HVD_SEL	2:0	HVD Select Selects 1 of 8 pipes to view HS, VS, and/or DE			0b000: Select Pipe 0 0b001: Select Pipe 1 0b010: Select Pipe 2 0b011: Select Pipe 3 0b100: Select Pipe 4 0b101: Select Pipe 5 0b110: Select Pipe 6 0b111: Select Pipe 7						

VIDEO\_RX0 (0x100, 0x112, 0x124, 0x136, 0x148, 0x160, 0x172, 0x184)

BIT	7	6	5	4	3	2	1	0
Field	LCRC_ERR	—	—	SEQ_MISS_EN	—	—	LINE_CRC_EN	DIS_PKT_DET
Reset	0x0	—	—	0b1	—	—	0b1	0b0
Access Type	Read Clears All	—	—	Write, Read	—	—	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR	7	Video Line CRC Error Flag  Asserted when a video line CRC error is detected	0b0: No video line CRC error detected 0b1: Video line CRC error detected
SEQ_MISS_EN	4	Video sequence miss detection enable	0b0: Disable Video Sequence Miss Detection 0b1: Video Sequence Miss Detection Enabled (Default)
LINE_CRC_EN	1	Video Line CRC Enable	0b0: Disable video line CRC 0b1: Enable video line CRC
DIS_PKT_DET	0	Disable Packet Detector  If the video is restarted with a different BPP when the packet detector is disabled, toggle this register or the video receive enable register to make sure the video link restarts.	0b0: Enable packet detect (default) 0b1: Disable packet detect

VIDEO\_RX3 (0x103, 0x115, 0x127, 0x139, 0x14B, 0x163, 0x175, 0x187)

BIT	7	6	5	4	3	2	1	0
Field	—	HD_TR_MO DE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
Reset	—	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	—	Write, Read	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HD_TR_MO DE	6	HD Tracking Mode  HS and DE tracking enables full periodic pattern.	0b0: Allow only partial periodic HS, DE 0b1: Allow partial periodic and full periodic HS, DE
DLOCKED	5	DE Tracking Locked	0b0: DE tracking not locked 0b1: DE tracking locked
VLOCKED	4	VS Tracking Locked	0b0: VS tracking unlocked 0b1: VS tracking locked
HLOCKED	3	HS Tracking Locked	0b0: HS tracking unlocked 0b1: HS tracking locked
DTRACKEN	2	DE Tracking Enable (disable if FSYNC = 1)  The system observes DE pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: DE tracking disabled (default) 0b1: DE tracking enabled

BITFIELD	BITS	DESCRIPTION	DECODE
VTRACKEN	1	VSYNC tracking enable (disable if FSYNC = 1). The system observes VS pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: VSYNC tracking disabled (default) 0b1: VSYNC tracking enabled
HTRACKEN	0	HSYNC tracking enable (disable if FSYNC = 1). The system observes HS pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: HSYNC tracking disabled (default) 0b1: HSYNC tracking enabled

VIDEO\_RX6 (0x106, 0x118, 0x12A, 0x13C, 0x14E, 0x166, 0x178, 0x18A)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	LIM_HEART	—	—	—
<b>Reset</b>	—	—	—	—	0b0	—	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	—	—	—
BITFIELD	BITS		DESCRIPTION					
LIM_HEART	3		If enabled, there is a 10ms timeout to detect loss of video lock. If disabled, there is a 100us timeout to detect loss of video lock. Set to 10ms timeout if Heartbeat is disabled (LIM_HEART = 1 on Serializer) Use together with SEQ_MISS_EN and DIS_PKT_DET registers in Deserializer. Embedded Data should use the heartbeat to ensure loss of video lock timeout does not occur.					

VIDEO\_RX8 (0x108, 0x11A, 0x12C, 0x13E, 0x150, 0x168, 0x17A, 0x18C)

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	VID_BLK_L EN_ERR	VID_LOCK	VID_PKT_D ET	VID_SEQ_E RR	—	—	—	—			
<b>Reset</b>	0b0	0b0	0b0	0b0	—	—	—	—			
<b>Access Type</b>	Read Clears All	Read Only	Read Only	Read Clears All	—	—	—	—			
BITFIELD	BITS		DESCRIPTION			DECODE					
VID_BLK_L EN_ERR	7	Video Rx block length error detected.			0b0: No video Rx block length error detected 0b1: Video Rx block length error detected						
VID_LOCK	6	Video pipeline locked			0b0: Video pipeline not locked 0b1: Video pipeline locked						
VID_PKT_D ET	5	Video Rx sufficient packet throughput detection.			0b0: Insufficient packet throughput 0b1: Sufficient packet throughput						
VID_SEQ_E RR	4	Video Rx sequence error detection.			0b0: No video Rx sequence error detected 0b1: Video Rx sequence error detected						

VIDEO\_RX10 (0x10A, 0x11C, 0x12E, 0x140, 0x152, 0x16A, 0x17C, 0x18E)

BIT	7	6	5	4	3	2	1	0	
Field	—	MASK_VID EO_DE	—	—	—	—	—	—	
Reset	—	0b0	—	—	—	—	—	—	
Access Type	—	Write, Read	—	—	—	—	—	—	
BITFIELD	BITS	DESCRIPTION				DECODE			
MASK_VIDE_O_DE	6	Mask video when DE is low				0b0: Do not mask video with DE 0b1: Mask video with DE			

CROSS\_0 (0x1C0, 0x1E0, 0x200, 0x220, 0x240, 0x260, 0x280, 0x2A0)

BIT	7	6	5	4	3	2	1	0
Field	—	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	—	0x0	0x0	0x00				
Access Type	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
CROSS0_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit		
CROSS0_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero		
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0				0bXXXXXX: Incoming bit position		

CROSS\_1 (0x1C1, 0x1E1, 0x201, 0x221, 0x241, 0x261, 0x281, 0x2A1)

BIT	7	6	5	4	3	2	1	0
Field	—	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	—	0x0	0x0	0x01				
Access Type	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
CROSS1_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit		
CROSS1_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero		
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1				0bXXXXXX: Incoming bit position		

CROSS\_2 (0x1C2, 0x1E2, 0x202, 0x222, 0x242, 0x262, 0x282, 0x2A2)

BIT	7	6	5	4	3	2	1	0
Field	—	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	—	0x0	0x0	0x02				
Access Type	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
CROSS2_I	6	Inverts CrossX			0b0: Do not invert bit 0b1: Invert bit				
CROSS2_F	5	Forces CrossX to 0 before inversion			0b0: Do not force bit to zero 0b1: Force bit to zero				
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2			0bXXXXXX: Incoming bit position				

**CROSS\_3 (0x1C3, 0x1E3, 0x203, 0x223, 0x243, 0x263, 0x283, 0x2A3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS3_I	CROSS3_F	CROSS3[4:0]				
<b>Reset</b>	—	0x0	0x0	0x03				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
CROSS3_I	6	Inverts CrossX			0b0: Do not invert bit 0b1: Invert bit				
CROSS3_F	5	Forces CrossX to 0 before inversion			0b0: Do not force bit to zero 0b1: Force bit to zero				
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3			0bXXXXXX: Incoming bit position				

**CROSS\_4 (0x1C4, 0x1E4, 0x204, 0x224, 0x244, 0x264, 0x284, 0x2A4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS4_I	CROSS4_F	CROSS4[4:0]				
<b>Reset</b>	—	0x0	0x0	0x04				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
CROSS4_I	6	Inverts CrossX			0b0: Do not invert bit 0b1: Invert bit				
CROSS4_F	5	Forces CrossX to 0 before inversion			0b0: Do not force bit to zero 0b1: Force bit to zero				
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4			0bXXXXXX: Incoming bit position				

**CROSS\_5 (0x1C5, 0x1E5, 0x205, 0x225, 0x245, 0x265, 0x285, 0x2A5)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	—	CROSS5_I	CROSS5_F	CROSS5[4:0]					
<b>Reset</b>	—	0x0	0x0	0x05					
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE				
CROSS5_I	6	Inverts CrossX			0b0: Do not invert bit 0b1: Invert bit				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS5_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5				0bXXXXXX: Incoming bit position			

CROSS\_6 (0x1C6, 0x1E6, 0x206, 0x226, 0x246, 0x266, 0x286, 0x2A6)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS6_I	CROSS6_F	CROSS6[4:0]				
<b>Reset</b>	—	0x0	0x0	0x06				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS6_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS6_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6				0bXXXXXX: Incoming bit position			

CROSS\_7 (0x1C7, 0x1E7, 0x207, 0x227, 0x247, 0x267, 0x287, 0x2A7)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS7_I	CROSS7_F	CROSS7[4:0]				
<b>Reset</b>	—	0x0	0x0	0x07				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS7_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS7_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7				0bXXXXXX: Incoming bit position			

CROSS\_8 (0x1C8, 0x1E8, 0x208, 0x228, 0x248, 0x268, 0x288, 0x2A8)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	—	CROSS8_I	CROSS8_F	CROSS8[4:0]					
<b>Reset</b>	—	0x0	0x0	0x08					
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read					
BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS8_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS8_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8				0bXXXXXX: Incoming bit position			

**CROSS\_9 (0x1C9, 0x1E9, 0x209, 0x229, 0x249, 0x269, 0x289, 0x2A9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS9_I	CROSS9_F	CROSS9[4:0]				
<b>Reset</b>	—	0x0	0x0	0x09				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
CROSS9_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit		
CROSS9_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero		
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9				0bXXXXXX: Incoming bit position		

**CROSS\_10 (0x1CA, 0x1EA, 0x20A, 0x22A, 0x24A, 0x26A, 0x28A, 0x2AA)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS10_I	CROSS10_F	CROSS10[4:0]				
<b>Reset</b>	—	0x0	0x0	0x0A				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
CROSS10_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit		
CROSS10_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero		
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10				0bXXXXXX: Incoming bit position		

**CROSS\_11 (0x1CB, 0x1EB, 0x20B, 0x22B, 0x24B, 0x26B, 0x28B, 0x2AB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS11_I	CROSS11_F	CROSS11[4:0]				
<b>Reset</b>	—	0x0	0x0	0x0B				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
CROSS11_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit		
CROSS11_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero		

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11				0bXXXXXX: Incoming bit position			

**CROSS\_12 (0x1CC, 0x1EC, 0x20C, 0x22C, 0x24C, 0x26C, 0x28C, 0x2AC)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS12_I	CROSS12_F	CROSS12[4:0]				
<b>Reset</b>	—	0x0	0x0	0x0C				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS12_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS12_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12				0bXXXXXX: Incoming bit position			

**CROSS\_13 (0x1CD, 0x1ED, 0x20D, 0x22D, 0x24D, 0x26D, 0x28D, 0x2AD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS13_I	CROSS13_F	CROSS13[4:0]				
<b>Reset</b>	—	0x0	0x0	0x0D				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS13_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS13_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13				0bXXXXXX: Incoming bit position			

**CROSS\_14 (0x1CE, 0x1EE, 0x20E, 0x22E, 0x24E, 0x26E, 0x28E, 0x2AE)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS14_I	CROSS14_F	CROSS14[4:0]				
<b>Reset</b>	—	0x0	0x0	0x0E				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS14_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS14_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14				0bXXXXXX: Incoming bit position			

**CROSS\_15 (0x1CF, 0x1EF, 0x20F, 0x22F, 0x24F, 0x26F, 0x28F, 0x2AF)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS15_I	CROSS15_F	CROSS15[4:0]				
<b>Reset</b>	—	0x0	0x0	0x0F				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS15_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS15_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15				0bXXXXXX: Incoming bit position			

**CROSS\_16 (0x1D0, 0x1F0, 0x210, 0x230, 0x250, 0x270, 0x290, 0x2B0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS16_I	CROSS16_F	CROSS16[4:0]				
<b>Reset</b>	—	0x0	0x0	0x10				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS16_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS16_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16				0bXXXXXX: Incoming bit position			

**CROSS\_17 (0x1D1, 0x1F1, 0x211, 0x231, 0x251, 0x271, 0x291, 0x2B1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS17_I	CROSS17_F	CROSS17[4:0]				
<b>Reset</b>	—	0x0	0x0	0x11				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS17_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS17_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17				0bXXXXX: Incoming bit position			

**CROSS\_18 (0x1D2, 0x1F2, 0x212, 0x232, 0x252, 0x272, 0x292, 0x2B2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS18_I	CROSS18_F	CROSS18[4:0]				
<b>Reset</b>	—	0x0	0x0	0x12				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS18_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS18_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18				0bXXXXX: Incoming bit position			

**CROSS\_19 (0x1D3, 0x1F3, 0x213, 0x233, 0x253, 0x273, 0x293, 0x2B3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS19_I	CROSS19_F	CROSS19[4:0]				
<b>Reset</b>	—	0x0	0x0	0x13				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS19_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS19_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19				0bXXXXX: Incoming bit position			

**CROSS\_20 (0x1D4, 0x1F4, 0x214, 0x234, 0x254, 0x274, 0x294, 0x2B4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS20_I	CROSS20_F	CROSS20[4:0]				
<b>Reset</b>	—	0x0	0x0	0x14				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS20_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS20_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20				0bXXXXXX: Incoming bit position			

**CROSS\_21 (0x1D5, 0x1F5, 0x215, 0x235, 0x255, 0x275, 0x295, 0x2B5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS21_I	CROSS21_F	CROSS21[4:0]				
<b>Reset</b>	—	0x0	0x0	0x15				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS21_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS21_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21				0bXXXXXX: Incoming bit position			

**CROSS\_22 (0x1D6, 0x1F6, 0x216, 0x236, 0x256, 0x276, 0x296, 0x2B6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS22_I	CROSS22_F	CROSS22[4:0]				
<b>Reset</b>	—	0x0	0x0	0x16				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS22_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS22_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22				0bXXXXXX: Incoming bit position			

**CROSS\_23 (0x1D7, 0x1F7, 0x217, 0x237, 0x257, 0x277, 0x297, 0x2B7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS23_I	CROSS23_F	CROSS23[4:0]				
<b>Reset</b>	—	0x0	0x0	0x17				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS23_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS23_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23				0bXXXXXX: Incoming bit position			

**CROSS\_HS (0x1D8, 0x1F8, 0x218, 0x238, 0x258, 0x278, 0x298, 0x2B8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
<b>Reset</b>	—	0x0	0x0	0x18				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS_HS_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS_HS_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS_HS	4:0	Maps selected internal signal to Cross X				0bXXXXXX: Incoming bit position			

**CROSS\_VS (0x1D9, 0x1F9, 0x219, 0x239, 0x259, 0x279, 0x299, 0x2B9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
<b>Reset</b>	—	0x0	0x0	0x19				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS_VS_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS_VS_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS_VS	4:0	Maps selected internal signal to Cross X				0bXXXXXX: Incoming bit position			

**CROSS\_DE (0x1DA, 0x1FA, 0x21A, 0x23A, 0x25A, 0x27A, 0x29A, 0x2BA)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
<b>Reset</b>	—	0x0	0x0	0x1A				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS_DE_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS_DE_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS_DE	4:0	Maps selected internal signal to Cross X				0bXXXXXX: Incoming bit position			

**PRBS\_ERR (0x1DB, 0x1FB, 0x21B, 0x23B, 0x25B, 0x27B, 0x29B, 0x2BB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VPRBS_ERR[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Clears All							
BITFIELD	BITS	DESCRIPTION					DECODE	
VPRBS_ERR	7:0	Video PRBS error counter, clears on read					0xXX: Number of video PRBS errors since last read	

**VPRBS (0x1DC, 0x1FC, 0x21C, 0x23C, 0x25C, 0x27C, 0x29C, 0x2BC)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PATGEN_C_LK_SRC	–	–	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
<b>Reset</b>	0x1	–	–	0b0	0b0	0b0	0x0	0b0
<b>Access Type</b>	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Read Only
BITFIELD	BITS	DESCRIPTION					DECODE	
PATGEN_CL_K_SRC	7	Pattern generator clock source for video PRBS7, PRBS9, PRBS24, checkerboard, and gradient patterns. 0 = 150MHz, 1 = 375MHz (default).					0b0: 150MHz 0b1: 375MHz (default)	
VPRBS24_GENCHK_EN	4	Enables video PRBS24 generator/checker					0b0: Video PRBS24 generator/checker disabled 0b1: Video PRBS24 generator/checker enabled	
VPRBS7_GENCHK_EN	3	Enables video PRBS7 generator/checker					0b0: Video PRBS7 generator/checker disabled 0b1: Video PRBS7 generator/checker enabled	
VPRBS9_GENCHK_EN	2	Enables video PRBS9 generator/checker					0b0: Video PRBS9 generator/checker disabled 0b1: Video PRBS9 generator/checker enabled	
DIS_GLITCH_FILT	1	Disables HS, VS, and DE glitch filtering					0b0: Glitch filter enabled 0b1: Glitch filter disabled	
VIDEO_LOCK	0	Video channel is locked and outputting valid video data					0b0: Video channel is not locked 0b1: Video channel is locked	

**CROSS\_27 (0x1DD, 0x1FD, 0x21D, 0x23D, 0x25D, 0x27D, 0x29D, 0x2BD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ALT_CROS_SBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
<b>Reset</b>	0x0	0x0	0x0	0x1B				
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION					DECODE	
ALT_CROSS_BAR	7	Selects whether to use the crossbar in the VRX block or the alternative crossbar in the RDP.					0b0: Use crossbar in VRX block 0b1: Use crossbar in RDP	
CROSS27_I	6	Inverts CrossX					0b0: Do not invert bit 0b1: Invert bit	

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS27_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS27	4:0	Maps selected internal signal to Cross X				0bXXXXXX: Incoming bit position			

**CROSS\_28 (0x1DE, 0x1FE, 0x21E, 0x23E, 0x25E, 0x27E, 0x29E, 0x2BE)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
<b>Reset</b>	–	0x0	0x0	0x1C				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS28_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS28_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS28	4:0	Maps selected internal signal to Cross X				0bXXXXXX: Incoming bit position			

**CROSS\_29 (0x1DF, 0x1FF, 0x21F, 0x23F, 0x25F, 0x27F, 0x29F, 0x2BF)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
<b>Reset</b>	–	0x0	0x0	0x1D				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
CROSS29_I	6	Inverts CrossX				0b0: Do not invert bit 0b1: Invert bit			
CROSS29_F	5	Forces CrossX to 0 before inversion				0b0: Do not force bit to zero 0b1: Force bit to zero			
CROSS29	4:0	Maps selected internal signal to Cross X				0bXXXXXX: Incoming bit position			

**GPIO\_A (0x300)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS	
<b>Reset</b>	0b1	–	0x0	0b0	0b0	0b0	0b1	0b1	
<b>Access Type</b>	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read	
BITFIELD	BITS	DESCRIPTION				DECODE			
RES_CFG	7	Resistor pullup/pulldown strength				0b0: 40kΩ 0b1: 1MΩ			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N	5	GPIO_REV_CDLY_AJitter minimization compensation enable Note: In delay compensation mode, a fixed delay is guaranteed once the link is locked. But each link reset could change the delay between two values which are 1.7us apart. Note: Use GPIO_REV_CDLY to adjust comp time.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO\_B (0x301)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x2	0b1	0x00					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO\_C (0x302)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	–	–	0x00				
<b>Access Type</b>	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x300) and PULL_UPDN_SEL (0x301) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_A (0x303)**

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	–	0x0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION						DECODE
RES_CFG	7	Resistor pullup/pulldown strength						0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable						0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0						0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level						0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control						0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control						0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver						0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x304)**

BIT	7	6	5	4	3	2	1	0	
Field	PULL_UPDN_SEL[1:0]			OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2			0b1	0x01				
Access Type	Write, Read			Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION						DECODE	
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration						0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x305)**

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	—	—	GPIO_RX_ID[4:0]				
Reset	0x0	—	—	0x01				
Access Type	Write, Read	—	—	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x303) and PULL_UPDN_SEL (0x304) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_A (0x306)**

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	—	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_E_N	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x307)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x2	0b1	0x02					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x308)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	—	—	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	—	—	0x02				
<b>Access Type</b>	Write, Read	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x306) and PULL_UPDN_SEL (0x307) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.		0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration				
GPIO_RX_ID	4:0	GPIO ID for pin while receiving		0bXXXXX: This GPIO receive ID				

**GPIO\_A (0x309)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	—	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION		DECODE				
RES_CFG	7	Resistor pullup/pulldown strength		0b0: 40kΩ 0b1: 1MΩ				
TX_COMP_EN	5	Jitter minimization compensation enable		0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0		0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1				
GPIO_IN	3	GPIO pin input level		0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x30A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
<b>Reset</b>	0x0		0b1	0x03				
<b>Access Type</b>	Write, Read		Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration			0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved			
OUT_TYPE	5	Driver type selection			0b0: Open-drain 0b1: Push-pull			
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x30B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG		—	—	GPIO_RX_ID[4:0]			
<b>Reset</b>	0x0		—	—	0x03			
<b>Access Type</b>	Write, Read		—	—	Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE			
OVR_RES_C_FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x309) and PULL_UPDN_SEL (0x30A) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.			0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration			
GPIO_RX_ID	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

GPIO\_A (0x30C)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	—	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_E_N	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO\_B (0x30D)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x2	0b1	0x04					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO\_C (0x30E)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	–	–	0x04				
<b>Access Type</b>	Write, Read	–	–	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
OVR_RES_C FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x30C) and PULL_UPDN_SEL (0x30D) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.				0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration		
GPIO_RX_ID	4:0	GPIO ID for pin while receiving				0bXXXXX: This GPIO receive ID		

GPIO\_A (0x310)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	–	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
RES_CFG	7	Resistor pullup/pulldown strength				0b0: 40kΩ 0b1: 1MΩ		
TX_COMP_E N	5	Jitter minimization compensation enable				0b0: Jitter compensation disabled 0b1: Jitter compensation enabled		
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0				0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1		
GPIO_IN	3	GPIO pin input level				0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1		
GPIO_RX_E N	2	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception		
GPIO_TX_E N	1	GPIO Tx source control				0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission		
GPIO_OUT_DIS	0	Enable/disable GPIO output driver				0b0: Output driver enabled 0b1: Output driver disabled		

PRELIMINARY

**GPIO\_B (0x311)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x2	0b1	0x05					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x312)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	—	—	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	—	—	0x05				
<b>Access Type</b>	Write, Read	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x310) and PULL_UPDN_SEL (0x311) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.		0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration				
GPIO_RX_ID	4:0	GPIO ID for pin while receiving		0bXXXXX: This GPIO receive ID				

**GPIO\_A (0x313)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	—	0x0	0b0	0b0	0b0	0b1	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION		DECODE				
RES_CFG	7	Resistor pullup/pulldown strength		0b0: 40kΩ 0b1: 1MΩ				
TX_COMP_EN	5	Jitter minimization compensation enable		0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0		0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1				
GPIO_IN	3	GPIO pin input level		0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x314)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x2	0b1	0x06					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE			
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration			0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved			
OUT_TYPE	5	Driver type selection			0b0: Open-drain 0b1: Push-pull			
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x315)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	—	—	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	—	—	0x06				
<b>Access Type</b>	Write, Read	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
OVR_RES_C_FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x313) and PULL_UPDN_SEL (0x314) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.			0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration			
GPIO_RX_ID	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

GPIO\_A (0x316)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	—	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_E_N	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO\_B (0x317)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x2	0b1	0x07					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO\_C (0x318)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	–	–	0x07				
<b>Access Type</b>	Write, Read	–	–	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
OVR_RES_C FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x316) and PULL_UPDN_SEL (0x317) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.				0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration		
GPIO_RX_ID	4:0	GPIO ID for pin while receiving				0bXXXXX: This GPIO receive ID		

GPIO\_A (0x319)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	–	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
RES_CFG	7	Resistor pullup/pulldown strength				0b0: 40kΩ 0b1: 1MΩ		
TX_COMP_E N	5	Jitter minimization compensation enable				0b0: Jitter compensation disabled 0b1: Jitter compensation enabled		
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0				0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1		
GPIO_IN	3	GPIO pin input level				0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1		
GPIO_RX_E N	2	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception		
GPIO_TX_E N	1	GPIO Tx source control				0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission		
GPIO_OUT_DIS	0	Enable/disable GPIO output driver				0b0: Output driver enabled 0b1: Output driver disabled		

PRELIMINARY

**GPIO\_B (0x31A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x2	0b1	0x08					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x31B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	—	—	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	—	—	0x08				
<b>Access Type</b>	Write, Read	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x319) and PULL_UPDN_SEL (0x31A) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.		0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration				
GPIO_RX_ID	4:0	GPIO ID for pin while receiving		0bXXXXX: This GPIO receive ID				

**GPIO\_A (0x31C)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	—	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION		DECODE				
RES_CFG	7	Resistor pullup/pulldown strength		0b0: 40kΩ 0b1: 1MΩ				
TX_COMP_EN	5	Jitter minimization compensation enable		0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0		0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1				
GPIO_IN	3	GPIO pin input level		0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x31D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
<b>Reset</b>	0x2		0b1	0x09				
<b>Access Type</b>	Write, Read		Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration			0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved			
OUT_TYPE	5	Driver type selection			0b0: Open-drain 0b1: Push-pull			
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x31E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG		—	—	GPIO_RX_ID[4:0]			
<b>Reset</b>	0x0		—	—	0x09			
<b>Access Type</b>	Write, Read		—	—	Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE			
OVR_RES_C_FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x31C) and PULL_UPDN_SEL (0x31D) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.			0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration			
GPIO_RX_ID	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

GPIO\_A (0x320)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	—	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION					DECODE	
RES_CFG	7	Resistor pullup/pulldown strength					0b0: 40kΩ 0b1: 1MΩ	
TX_COMP_E_N	5	Jitter minimization compensation enable					0b0: Jitter compensation disabled 0b1: Jitter compensation enabled	
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0					0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1	
GPIO_IN	3	GPIO pin input level					0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1	
GPIO_RX_E_N	2	GPIO out source control					0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception	
GPIO_TX_E_N	1	GPIO Tx source control					0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission	
GPIO_OUT_DIS	0	Enable/disable GPIO output driver					0b0: Output driver enabled 0b1: Output driver disabled	

GPIO\_B (0x321)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
<b>Reset</b>	0x2		0b1	0x0A				
<b>Access Type</b>	Write, Read		Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION					DECODE	
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration					0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved	
OUT_TYPE	5	Driver type selection					0b0: Open-drain 0b1: Push-pull	
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting					0bXXXXXX: This GPIO transmit ID	

GPIO\_C (0x322)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	–	–	0x0A				
<b>Access Type</b>	Write, Read	–	–	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
OVR_RES_C FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x320) and PULL_UPDN_SEL (0x321) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.				0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration		
GPIO_RX_ID	4:0	GPIO ID for pin while receiving				0bXXXXX: This GPIO receive ID		

GPIO\_A (0x323)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	–	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
RES_CFG	7	Resistor pullup/pulldown strength				0b0: 40kΩ 0b1: 1MΩ		
TX_COMP_E N	5	Jitter minimization compensation enable				0b0: Jitter compensation disabled 0b1: Jitter compensation enabled		
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0				0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1		
GPIO_IN	3	GPIO pin input level				0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1		
GPIO_RX_E N	2	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception		
GPIO_TX_E N	1	GPIO Tx source control				0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission		
GPIO_OUT_DIS	0	Enable/disable GPIO output driver				0b0: Output driver enabled 0b1: Output driver disabled		

**PRELIMINARY**

**GPIO\_B (0x324)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x0	0b1	0x0B					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x325)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	—	—	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	—	—	0x0B				
<b>Access Type</b>	Write, Read	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x323) and PULL_UPDN_SEL (0x324) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.		0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration				
GPIO_RX_ID	4:0	GPIO ID for pin while receiving		0bXXXXX: This GPIO receive ID				

**GPIO\_A (0x326)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	—	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION		DECODE				
RES_CFG	7	Resistor pullup/pulldown strength		0b0: 40kΩ 0b1: 1MΩ				
TX_COMP_EN	5	Jitter minimization compensation enable		0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0		0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1				
GPIO_IN	3	GPIO pin input level		0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x327)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x0	0b1	0x0C					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE			
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration			0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved			
OUT_TYPE	5	Driver type selection			0b0: Open-drain 0b1: Push-pull			
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x328)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	—	—	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	—	—	0x0C				
<b>Access Type</b>	Write, Read	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
OVR_RES_C_FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x326) and PULL_UPDN_SEL (0x327) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.			0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration			
GPIO_RX_ID	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

GPIO\_A (0x329)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	—	0x0	0b0	0b0	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_E_N	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO\_B (0x32A)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
<b>Reset</b>	0x0		0b1	0x0D				
<b>Access Type</b>	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO\_C (0x32B)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	–	–	0x0D				
<b>Access Type</b>	Write, Read	–	–	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
OVR_RES_C FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x329) and PULL_UPDN_SEL (0x32A) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.				0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration		
GPIO_RX_ID	4:0	GPIO ID for pin while receiving				0bXXXXX: This GPIO receive ID		

GPIO\_A (0x32C)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b1	–	0x0	0b1	0b1	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
RES_CFG	7	Resistor pullup/pulldown strength				0b0: 40kΩ 0b1: 1MΩ		
TX_COMP_E N	5	Jitter minimization compensation enable				0b0: Jitter compensation disabled 0b1: Jitter compensation enabled		
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0				0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1		
GPIO_IN	3	GPIO pin input level				0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1		
GPIO_RX_E N	2	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception		
GPIO_TX_E N	1	GPIO Tx source control				0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission		
GPIO_OUT_DIS	0	Enable/disable GPIO output driver				0b0: Output driver enabled 0b1: Output driver disabled		

**GPIO\_B (0x32D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PULL_UPDN_SEL[1:0]	OUT_TYPE	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x2	0b1	0x0E					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x32E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	OVR_RES_CFG	—	—	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0	—	—	0x0E				
<b>Access Type</b>	Write, Read	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x32C) and PULL_UPDN_SEL (0x32D) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.		0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration				
GPIO_RX_ID	4:0	GPIO ID for pin while receiving		0bXXXXX: This GPIO receive ID				

**GPIO\_A (0x330)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	—	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b0	—	0x0	0b1	0b1	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	—	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION		DECODE				
RES_CFG	7	Resistor pullup/pulldown strength		0b0: 40kΩ 0b1: 1MΩ				
TX_COMP_EN	5	Jitter minimization compensation enable		0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0		0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1				
GPIO_IN	3	GPIO pin input level		0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x331)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	PULL_UPDN_SEL[1:0]		–	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x0		–	0x0F					
<b>Access Type</b>	Write, Read		–	Write, Read					
BITFIELD	BITS	DESCRIPTION				DECODE			
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration				0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved			
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting				0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x332)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	OVR_RES_CFG		–	–	GPIO_RX_ID[4:0]				
<b>Reset</b>	0x0		–	–	0x0F				
<b>Access Type</b>	Write, Read		–	–	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE			
OVR_RES_C FG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x330) and PULL_UPDN_SEL (0x331) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.				0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration			
GPIO_RX_ID	4:0	GPIO ID for pin while receiving				0bXXXXX: This GPIO receive ID			

**GPIO\_A (0x333)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
<b>Reset</b>	0b0	–	0x0	0b1	0b1	0b0	0b0	0b1
<b>Access Type</b>	Write, Read	–	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_E_N	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_E_N	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_E_N	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

**GPIO\_B (0x334)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	PULL_UPDN_SEL[1:0]	–	–	–	GPIO_TX_ID[4:0]					
<b>Reset</b>	0x0	–	–	–	0x10					
<b>Access Type</b>	Write, Read	–	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x335)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	OVR_RES_CFG	–	–	–	GPIO_RX_ID[4:0]					
<b>Reset</b>	0x0	–	–	–	0x10					
<b>Access Type</b>	Write, Read	–	–	–	Write, Read					
BITFIELD	BITS	DESCRIPTION	DECODE							
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES-CFG (0x333) and PULL_UPDN_SEL (0x334) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration							
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID							

**GPIO\_B (0x337)**

BIT	7	6	5	4	3	2	1	0
Field	-	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	-	0x0	0b0	0x00				
Access Type	-	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_B	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_B	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x338)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	-	-	0b0	0x00				
Access Type	-	-	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_B	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x33A)**

BIT	7	6	5	4	3	2	1	0
Field	-	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	-	0x0	0b0	0x01				
Access Type	-	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_B	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_B	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x33B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x01				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x33D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x02				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x33E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x02				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x341)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x03				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x342)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x03				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x344)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x04				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x345)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x04				
<b>Access Type</b>	—	—	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_B	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x347)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x05				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_B	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_B	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

GPIO\_C (0x348)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	–	–	0b0	0x05				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
GPIO_RX_E_N_B	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID				

GPIO\_B (0x34A)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	–	0x0	0b0	0x06				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
TX_COMP_E_N_B	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_TX_E_N_B	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission				
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID				

GPIO\_C (0x34B)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	–	–	0b0	0x06				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
GPIO_RX_E_N_B	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID				

PRELIMINARY

**GPIO\_B (0x34D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	–	0x0	0b0	0x07				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x34E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	–	–	0b0	0x07				
<b>Access Type</b>	–	–	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
GPIO_RX_E_N_B	5	GPIO out source control		0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving		0bXXXXX: This GPIO receive ID				

**GPIO\_B (0x351)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	–	0x0	0b0	0x08				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
TX_COMP_E_N_B	6	Jitter minimization compensation enable		0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_TX_E_N_B	5	GPIO Tx source control		0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission				

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x352)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x08				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x354)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x09				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x355)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x09				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x357)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x0a				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x358)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x0a				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x35A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x0b				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x35B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x0b				
<b>Access Type</b>	—	—	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_B	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x35D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x0c				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_B	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_B	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

GPIO\_C (0x35E)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	–	–	0b0	0x0c				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
GPIO_RX_E_N_B	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID				

GPIO\_B (0x361)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	–	0x0	0b0	0x0d				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
TX_COMP_E_N_B	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_TX_E_N_B	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission				
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID				

GPIO\_C (0x362)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	–	–	0b0	0x0d				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
GPIO_RX_E_N_B	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID				

PRELIMINARY

**GPIO\_B (0x364)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	–	0x0	0b0	0x0e				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x365)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	–	–	0b0	0x0e				
<b>Access Type</b>	–	–	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
GPIO_RX_E_N_B	5	GPIO out source control		0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving		0bXXXXX: This GPIO receive ID				

**GPIO\_B (0x367)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	–	0x0	0b0	0x0F				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
TX_COMP_E_N_B	6	Jitter minimization compensation enable		0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_TX_E_N_B	5	GPIO Tx source control		0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission				

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x368)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x0F				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x36A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
<b>Reset</b>	—	0x0	0b0	0x10				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x36B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
<b>Reset</b>	—	—	0b0	0x10				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x36D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C					GPIO_TX_ID_C[4:0]
<b>Reset</b>	—	0x0	0b0					0x00
<b>Access Type</b>	—	Write, Read	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x36E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C					GPIO_RX_ID_C[4:0]
<b>Reset</b>	—	—	0b0					0x00
<b>Access Type</b>	—	—	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x371)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C					GPIO_TX_ID_C[4:0]
<b>Reset</b>	—	0x0	0b0					0x01
<b>Access Type</b>	—	Write, Read	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x372)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	—	—	0b0	0x01				
<b>Access Type</b>	—	—	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_C	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x374)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	—	0x0	0b0	0x02				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

GPIO\_C (0x375)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	–	–	0b0	0x02				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
GPIO_RX_E_N_C	5	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving				0bXXXXXX: This GPIO receive ID			

GPIO\_B (0x377)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	–	0x0	0b0	0x03				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable				0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control				0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting				0bXXXXXX: This GPIO transmit ID			

GPIO\_C (0x378)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	–	–	0b0	0x03				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
GPIO_RX_E_N_C	5	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving				0bXXXXXX: This GPIO receive ID			

PRELIMINARY

**GPIO\_B (0x37A)**

BIT	7	6	5	4	3	2	1	0
Field	-	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	-	0x0	0b0	0x04				
Access Type	-	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x37B)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	-	-	0b0	0x04				
Access Type	-	-	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_C	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x37D)**

BIT	7	6	5	4	3	2	1	0
Field	-	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	-	0x0	0b0	0x05				
Access Type	-	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXXX: This GPIO transmit ID

**GPIO\_C (0x37E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	—	—	0b0	0x05				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXXX: This GPIO receive ID

**GPIO\_B (0x381)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	—	0x0	0b0	0x06				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXXX: This GPIO transmit ID

**GPIO\_C (0x382)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	—	—	0b0	0x06				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x384)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	–	0x0	0b0	0x07				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x385)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	–	–	0b0	0x07				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x387)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	–	0x0	0b0	0x08				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x388)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	—	—	0b0	0x08				
<b>Access Type</b>	—	—	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_C	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x38A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	—	0x0	0b0	0x09				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

GPIO\_C (0x38B)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	–	–	0b0	0x09				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
GPIO_RX_E_N_C	5	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving				0bXXXXXX: This GPIO receive ID			

GPIO\_B (0x38D)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	–	0x0	0b0	0x0a				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable				0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control				0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting				0bXXXXXX: This GPIO transmit ID			

GPIO\_C (0x38E)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	–	–	0b0	0x0a				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
GPIO_RX_E_N_C	5	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving				0bXXXXXX: This GPIO receive ID			

PRELIMINARY

**GPIO\_B (0x391)**

BIT	7	6	5	4	3	2	1	0
Field	-	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	-	0x0	0b0	0x0b				
Access Type	-	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x392)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	-	-	0b0	0x0b				
Access Type	-	-	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_C	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x394)**

BIT	7	6	5	4	3	2	1	0
Field	-	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	-	0x0	0b0	0x0c				
Access Type	-	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXXX: This GPIO transmit ID

**GPIO\_C (0x395)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	—	—	0b0	0x0c				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXXX: This GPIO receive ID

**GPIO\_B (0x397)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	—	0x0	0b0	0x0d				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXXX: This GPIO transmit ID

**GPIO\_C (0x398)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	—	—	0b0	0x0d				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x39A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	—	0x0	0b0	0x0e				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x39B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	—	—	0b0	0x0e				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x39D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	—	0x0	0b0	0x0f				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x39E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	—	—	0b0	0x0f				
<b>Access Type</b>	—	—	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_C	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x3A1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
<b>Reset</b>	—	0x0	0b0	0x10				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_C	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_C	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

GPIO\_C (0x3A2)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
<b>Reset</b>	–	–	0b0	0x10				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
GPIO_RX_E_N_C	5	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving				0bXXXXX: This GPIO receive ID			

GPIO\_B (0x3A4)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	–	0x0	0b0	0x00				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
TX_COMP_E_N_D	6	Jitter minimization compensation enable				0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_D	5	GPIO Tx source control				0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting				0bXXXXX: This GPIO transmit ID			

GPIO\_C (0x3A5)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	–	–	0b0	0x00				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION				DECODE			
GPIO_RX_E_N_D	5	GPIO out source control				0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving				0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x3A7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	–	0x0	0b0	0x01				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x3A8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	–	–	0b0	0x01				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x3AA)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	–	0x0	0b0	0x02				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXXX: This GPIO transmit ID

**GPIO\_C (0x3AB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	—	—	0b0	0x02				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXXX: This GPIO receive ID

**GPIO\_B (0x3AD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	—	0x0	0b0	0x03				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXXX: This GPIO transmit ID

**GPIO\_C (0x3AE)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	—	—	0b0	0x03				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x3B1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	—	0x0	0b0	0x04				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x3B2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	—	—	0b0	0x04				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x3B4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	—	0x0	0b0	0x05				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x3B5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	—	—	0b0	0x05				
<b>Access Type</b>	—	—	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_D	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x3B7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	—	0x0	0b0	0x06				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_D	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_D	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

GPIO\_C (0x3B8)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	–	–	0b0	0x06				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
GPIO_RX_E_N_D	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving			0bXXXXXX: This GPIO receive ID				

GPIO\_B (0x3BA)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	–	0x0	0b0	0x07				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
TX_COMP_E_N_D	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_TX_E_N_D	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission				
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting			0bXXXXXX: This GPIO transmit ID				

GPIO\_C (0x3BB)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	–	–	0b0	0x07				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
GPIO_RX_E_N_D	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving			0bXXXXXX: This GPIO receive ID				

**GPIO\_B (0x3BD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	–	0x0	0b0	0x08				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x3BE)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	–	–	0b0	0x08				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x3C1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	–	0x0	0b0	0x09				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x3C2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	—	—	0b0	0x09				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x3C4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	—	0x0	0b0	0x0a				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x3C5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	—	—	0b0	0x0a				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x3C7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_D	GPIO_TX_EN_D					GPIO_TX_ID_D[4:0]
<b>Reset</b>	—	0x0	0b0					0x0b
<b>Access Type</b>	—	Write, Read	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x3C8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D					GPIO_RX_ID_D[4:0]
<b>Reset</b>	—	—	0b0					0x0b
<b>Access Type</b>	—	—	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_E_N_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

**GPIO\_B (0x3CA)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_D	GPIO_TX_EN_D					GPIO_TX_ID_D[4:0]
<b>Reset</b>	—	0x0	0b0					0x0c
<b>Access Type</b>	—	Write, Read	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_E_N_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_E_N_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

**GPIO\_C (0x3CB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	—	—	0b0	0x0c				
<b>Access Type</b>	—	—	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_D	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x3CD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	—	0x0	0b0	0x0d				
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_D	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_D	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

GPIO\_C (0x3CE)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	–	–	0b0	0x0d				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
GPIO_RX_E_N_D	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID				

GPIO\_B (0x3D1)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
<b>Reset</b>	–	0x0	0b0	0x0e				
<b>Access Type</b>	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
TX_COMP_E_N_D	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled				
GPIO_TX_E_N_D	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission				
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID				

GPIO\_C (0x3D2)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	–	–	0b0	0x0e				
<b>Access Type</b>	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION			DECODE				
GPIO_RX_E_N_D	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception				
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID				

**GPIO\_B (0x3D4)**

BIT	7	6	5	4	3	2	1	0
Field	-	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	-	0x0	0b0	0x0f				
Access Type	-	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_D	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_D	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting			0bXXXXX: This GPIO transmit ID			

**GPIO\_C (0x3D5)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	-	-	0b0	0x0f				
Access Type	-	-	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
GPIO_RX_E_N_D	5	GPIO out source control			0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception			
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving			0bXXXXX: This GPIO receive ID			

**GPIO\_B (0x3D7)**

BIT	7	6	5	4	3	2	1	0
Field	-	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	-	0x0	0b0	0x10				
Access Type	-	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
TX_COMP_E_N_D	6	Jitter minimization compensation enable			0b0: Jitter compensation disabled 0b1: Jitter compensation enabled			
GPIO_TX_E_N_D	5	GPIO Tx source control			0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission			

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXXX: This GPIO transmit ID

GPIO\_C (0x3D8)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
<b>Reset</b>	—	—	0b0	0x10				
<b>Access Type</b>	—	—	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXXX: This GPIO receive ID

MS\_ID\_A (0x3F0)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	RX_MS_ID_A[4:0]				
<b>Reset</b>	—	—	—	0x1D				
<b>Access Type</b>	—	—	—	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RX_MS_ID_A	4:0	GPIO ID for remote MS pin for Link A	0bXXXXXX: This GPIO transmit ID

MS\_ID\_B (0x3F1)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	RX_MS_ID_B[4:0]				
<b>Reset</b>	—	—	—	0x1D				
<b>Access Type</b>	—	—	—	Write, Read				
BITFIELD	BITS	DESCRIPTION		DECODE				
RX_MS_ID_B	4:0	GPIO ID for remote MS pin for Link B		0bXXXXXX: This GPIO transmit ID				

MS\_ID\_C (0x3F2)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	RX_MS_ID_C[4:0]				
<b>Reset</b>	—	—	—	0x1D				
<b>Access Type</b>	—	—	—	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
RX_MS_ID_C	4:0	GPIO ID for remote MS pin for Link C	0bXXXXX: This GPIO transmit ID

MS\_ID\_D (0x3F3)

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	—	—	—	RX_MS_ID_D[4:0]							
<b>Reset</b>	—	—	—	0x1D							
<b>Access Type</b>	—	—	—	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_MS_ID_D	4:0	GPIO ID for remote MS pin for Link D	0bXXXXX: This GPIO transmit ID

BACKTOP1 (0x400)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CSIPLL3_L_OCK	CSIPLL2_L_OCK	CSIPLL1_L_OCK	CSIPLL0_L_OCK	LINE_SPL2	LINE_SPL0	—	BACKTOP_EN
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b0	—	0b1
<b>Access Type</b>	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read	—	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLL3_LOCK	7	CSIPLL3 lock	0b0: PLL not locked 0b1: PLL locked
CSIPLL2_LOCK	6	CSIPLL2 lock	0b0: PLL not locked 0b1: PLL locked
CSIPLL1_LOCK	5	CSIPLL1 lock	0b0: PLL not locked 0b1: PLL locked
CSIPLL0_LOCK	4	CSIPLL0 lock	0b0: CSI2 0 PLL not locked 0b1: CSI2 0 PLL locked
LINE_SPL2	3	Enables line-based distribution to line memories for Video Pipe 2	0b0: Disable 0b1: Enable
LINE_SPL0	2	Enables line-based distribution to line memories for Video Pipe 0	0b0: Disable 0b1: Enable
BACKTOP_EN	0	Backtop write logic enable	0b0: Disable writes to BACKTOP register block 0b1: Enable writes to BACKTOP register block

BACKTOP11 (0x40A)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	cmd_overflow_w3	cmd_overflow_w2	cmd_overflow_w1	cmd_overflow_w0	LMO_3	LMO_2	LMO_1	LMO_0
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_overflow3	7	Pipe 3 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow2	6	Pipe 2 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow1	5	Pipe 1 command FIFO overflow	0b0: No overflow 0b1: Overflow
cmd_overflow0	4	Pipe 0 command FIFO overflow	0b0: No overflow 0b1: Overflow
LMO_3	3	Pipe 3 line memory overflow sticky register	0b0: No overflow 0b1: Overflow
LMO_2	2	Pipe 2 line memory overflow sticky register	0b0: No overflow 0b1: Overflow
LMO_1	1	Pipe 1 line memory overflow sticky register	0b0: No overflow 0b1: Overflow
LMO_0	0	Pipe 0 line memory overflow sticky register	0b0: No overflow 0b1: Overflow

**BACKTOP12 (0x40B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	soft_bpp_0[4:0]						—	CSI_OUT_EN
<b>Reset</b>	0x00						0b1	—
<b>Access Type</b>	Write, Read						Write, Read	—

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_0	7:3	Pipe 0 BPP software-override: Software-override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30 All other values: Reserved
CSI_OUT_E_N	1	Enables MIPI CSI output	0b0: CSI output disabled 0x1: CSI output enabled

**BACKTOP13 (0x40C)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	soft_vc_1[3:0]						soft_vc_0[3:0]				
<b>Reset</b>	0x0						0x0				
<b>Access Type</b>	Write, Read						Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE					
soft_vc_1	7:4	Pipe 1 VC software-override				0XX: Software-defined virtual channel for Pipe 1					
soft_vc_0	3:0	Pipe 0 VC software-override				0XX: Software-defined virtual channel for Pipe 0					

**BACKTOP14 (0x40D)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	soft_vc_3[3:0]					soft_vc_2[3:0]			
<b>Reset</b>	0x0					0x0			
<b>Access Type</b>	Write, Read					Write, Read			
BITFIELD	BITS	DESCRIPTION					DECODE		
soft_vc_3	7:4	Pipe 3 VC software-override					0xX: Software-defined virtual channel for Pipe 3		
soft_vc_2	3:0	Pipe 2 VC software-override					0xX: Software-defined virtual channel for Pipe 2		

**BACKTOP15 (0x40E)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	soft_dt_1_h[1:0]					soft_dt_0[5:0]			
<b>Reset</b>	0x0					0x00			
<b>Access Type</b>	Write, Read					Write, Read			
BITFIELD	BITS	DESCRIPTION					DECODE		
soft_dt_1_h	7:6	Pipe 1 DT (high bits) software-override bitfield. Works together with soft_dt_1_l in BACKTOP16 register (0x40F).					0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8		

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_0	5:0	Pipe 0 DT software-override.	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP16 (0x40F)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>								soft_dt_1_l[3:0]
<b>Reset</b>								0x0
<b>Access Type</b>								Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_2_h	7:4	Pipe 2 DT (high bits) software-override bitfield. Works together with soft_dt_2_l in BACKTOP17 register (0x410).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_1_l	3:0	Pipe 1 DT (low bits) software-override bitfield. Works together with soft_dt_1_h in BACKTOP16 register (0x40E).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP17 (0x410)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	soft_dt_3[5:0]						soft_dt_2_l[1:0]	
<b>Reset</b>	0x00						0x0	
<b>Access Type</b>	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_3	7:2	Pipe 3 DT software-override	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_2_l	1:0	Pipe 2 DT (low bits) software-override. Works together with soft_dt_2_h in BACKTOP16 register (0x40F).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP18 (0x411)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	soft_bpp_2_h[2:0]				soft_bpp_1[4:0]			
<b>Reset</b>	0x0						0x00	
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_2_h	7:5	Pipe 2 BPP (high bits) software-override bitfield: Works together with soft_bpp_2_l in BACKTOP19 register (0x412).	0bXX: High bits of software-defined BPP for Pipe 2
soft_bpp_1	4:0	Pipe 1 BPP software-override bitfield: Software override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30

BACKTOP19 (0x412)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	soft_bpp_3[4:0]						soft_bpp_2_l[1:0]
<b>Reset</b>	—	0x00						0x0
<b>Access Type</b>	—	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_3	6:2	Pipe 3 BPP software-override bitfield: Software override video data BPP.	0x8: Datatypes = 0xA, 0x10-12, 0x31-37 0xA: Datatypes = 0xB 0xC: Datatypes = 0xC 0xE: Datatypes = 0xD 0x10: Datatypes = 0x22, 0x1E, 0x2E 0x12: Datatypes = 0x23 0x14: Datatypes = 0xF, 0x2F 0x18: Datatypes = 0x24, 0x30 0bXX: New BPP for Pipe 4
soft_bpp_2_l	1:0	Pipe 2 BPP software-override register: Software override video data BPP (low bits). Works together with soft_bpp_2_h in BACKTOP18 register (0x412).	0bXX: Low bits of software-defined BPP for Pipe 2

BACKTOP20 (0x413)

BIT	7	6	5	4	3	2	1	0
Field	phy0_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
phy0_csi_tx_dpll_fb_fracti on_in_l	7:0	Low byte of software-override value for CSI PHY0 frequency fine tuning				0xXX: PHY frequency fine tuning override low byte		

BACKTOP21 (0x414)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dbl3	bpp8dbl2	bpp8dbl1	bpp8dbl0	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
bpp8dbl3	7	Pipe 3 BPP8 double-pixel register: BPP = 8 processed as 16-bit color				0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color		
bpp8dbl2	6	Pipe 2 BPP8 double-pixel register: BPP = 8 processed as 16-bit color				0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color		
bpp8dbl1	5	Pipe 1 BPP8 double-pixel register: BPP = 8 processed as 16-bit color				0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color		
bpp8dbl0	4	Pipe 0 BPP8 double-pixel register: BPP = 8 processed as 16-bit color				0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color		
phy0_csi_tx_dpll_fb_fracti on_in_h	3:0	High nibble of software-override value for CSI PHY0 frequency fine tuning				0X: PHY0 frequency fine tuning override high nibble		

**BACKTOP22 (0x415)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	override_bpp_p_vc_dt_1	override_bpp_p_vc_dt_0	phy0_csi_tx_dpll_fb_fraction_predef_en		phy0_csi_tx_dpll_predef_freq[4:0]					
<b>Reset</b>	0b0	0b0	0b1		0x0F					
<b>Access Type</b>	Write, Read	Write, Read	Write, Read		Write, Read					
BITFIELD	BITS	<b>DESCRIPTION</b>				<b>DECODE</b>				
override_bpp_p_vc_dt_1	7	Pipe 1 software-override enable bitfield				0b0: Disable 0b1: Enable				
override_bpp_p_vc_dt_0	6	Pipe 0 software-override enable bitfield				0b0: Disable 0b1: Enable				
phy0_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY0 software-override disable for frequency fine tuning				0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning				
phy0_csi_tx_dpll_predef_freq	4:0	MIPI PHY0 DPLL frequency bitfield: Set DPLL frequency on multiple of 100MHz.  DPHY: Clock frequency is half, data rate is equivalent bps/lane.  CPHY: 2.28bits/symbol.				DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane  CPHY data rate/trio 0x02: 200MHz DPLL, 456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane				

**BACKTOP23 (0x416)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>		phy1_csi_tx_dpll_fb_fraction_in_l[7:0]							
<b>Reset</b>		0x00							
<b>Access Type</b>		Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>				<b>DECODE</b>			
phy1_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY1 frequency fine tuning				0XX: PHY1 frequency fine tuning override low byte			

**BACKTOP24 (0x417)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	bpp8dbl3_mode	bpp8dbl2_mode	bpp8dbl1_mode	bpp8dbl0_mode	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]				
<b>Reset</b>	0b0	0b0	0b0	0b0	0x0				
<b>Access Type</b>	Write, Read								

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl3_mode	7	Pipe 3 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl2_mode	6	Pipe 2 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl1_mode	5	Pipe 1 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl0_mode	4	Pipe 0 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
phy1_csi_tx_dpll_fb_fracti on_in_h	3:0	High nibble of software-override value for CSI PHY1 frequency fine tuning	0xX: PHY1 frequency fine tuning override high nibble

**BACKTOP25 (0x418)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	override_bp_p_vc_dt_3	override_bp_p_vc_dt_2	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
<b>Reset</b>	0b0	0b0	0b1	0x0F				
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_3	7	Pipe 3 software-override enable bitfield	0b0: Disable 0b1: Enable
override_bpp_vc_dt_2	6	Pipe 2 software-override enable bitfield	0b0: Disable 0b1: Enable
phy1_csi_tx_dpll_fb_fracti on_predef_e n	5	MIPI PHY1 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning
phy1_csi_tx_dpll_predef_f req	4:0	MIPI PHY1 DPLL frequency bitfield: Set DPLL frequency on multiple of 100MHz.  DPHY: Clock frequency is half; data rate is equivalent bps/lane.  CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane  CPHY data rate/trio 0x02: 200MHz DPLL, 456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

**BACKTOP26 (0x419)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	phy2_csi_tx_dpll_fb_fraction_in_l[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dpll_fb_fracti on_in_l	7:0	Low byte of software-override value for CSI PHY2 frequency fine tuning	0xXX: PHY2 frequency fine tuning override low byte

**BACKTOP27 (0x41A)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	yuv_8_10_mux_mode0	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]				
<b>Reset</b>	0x0	0x0	0x0	0x0	0x0				
<b>Access Type</b>	Write, Read								

BITFIELD	BITS	DESCRIPTION	DECODE
yuv_8_10_mux_mode3	7	Pipe 3 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode2	6	Pipe 2 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode1	5	Pipe 1 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode0	4	Pipe 0 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
phy2_csi_tx_dpll_fb_fracti on_in_h	3:0	High nibble of software-override value for CSI PHY2 frequency fine tuning	0XX: PHY2 frequency fine tuning override high nibble

**BACKTOP28 (0x41B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	override_bp_p_vc_dt_5	override_bp_p_vc_dt_4	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]				
<b>Reset</b>	0b0	0b0	0b1	0x0F				
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_5	7	Pipe 5 software-override enable for BPP, VC, and DT	0b0: Disable 0b1: Enable
override_bpp_vc_dt_4	6	Pipe 4 software-override enable for BPP, VC, and DT	0b0: Disable 0b1: Enable
phy2_csi_tx_dpll_fb_fracti on_predef_en	5	MIPI PHY2 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dpll_predef_f_req	4:0	<p>MIPI PHY2 DPLL frequency register: Set DPLL frequency on multiple of 100MHz.</p> <p>DPHY: Clock frequency is half; data rate is equivalent bps/lane.</p> <p>CPHY: 2.28bits/symbol.</p>	<p>DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane</p> <p>CPHY data rate/trio 0x02: 200MHz DPLL, 456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane</p>

**BACKTOP29 (0x41C)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION				DECODE			
phy3_csi_tx_dpll_fb_fracti_on_in_l	7:0	Low byte of software-override value for CSI PHY3 frequency fine tuning				0XX: PHY3 frequency fine tuning override low byte			

**BACKTOP30 (0x41D)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	override_bpp_p_vc_dt_7	override_bp_p_vc_dt_6	bpp10dbl3_mode	bpp10dbl3	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]				
<b>Reset</b>	0b0	0b0	0b0	0b0	0x0				
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE			
override_bpp_vc_dt_7	7	Pipe 7 software-override enable for BPP, VC, and DT				0b0: Disable 0b1: Enable			
override_bpp_vc_dt_6	6	Pipe 6 software-override enable for BPP, VC, and DT				0b0: Disable 0b1: Enable			
bpp10dbl3_mode	5	Pipe 3 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams				0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected			
bpp10dbl3	4	Pipe 3 BPP10 double-pixel register: BPP = 10 processed as 20-bit color				0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color			
phy3_csi_tx_dpll_fb_fracti_on_in_h	3:0	High nibble of software-override value for CSI PHY3 frequency fine tuning				0X: PHY3 frequency fine tuning override high nibble			

**BACKTOP31 (0x41E)**

BIT	7	6	5	4	3	2	1	0
Field	bpp10dbl2_mode	bpp10dbl2	phy3_csi_tx_dpll_fb_fracti_on_predef_en		phy3_csi_tx_dpll_predef_freq[4:0]			
Reset	0b0	0b0	0b1		0x0F			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE			
bpp10dbl2_mode	7	Pipe 2 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams			0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected			
bpp10dbl2	6	Pipe 2 BPP10 double-pixel register: BPP = 10 processed as 20-bit color			0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color			
phy3_csi_tx_dpll_fb_fracti_on_predef_en	5	MIPI PHY3 software-override disable for frequency fine tuning			0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning			
phy3_csi_tx_dpll_predef_req	4:0	MIPI PHY3 DPLL frequency register: Set DPLL frequency on multiple of 100MHz.  DPHY: Clock frequency is half; data rate is equivalent bps/lane.  CPHY: 2.28bits/symbol.			DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane  CPHY data rate/trio 0x02: 200MHz DPLL, 456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane			

**BACKTOP32 (0x41F)**

BIT	7	6	5	4	3	2	1	0
Field	bpp10dbl1_mode	bpp10dbl1	bpp10dbl0_mode	bpp10dbl0	bpp12dbl3	bpp12dbl2	bpp12dbl1	bpp12dbl0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION			DECODE			
bpp10dbl1_mode	7	Pipe 1 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams			0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected			
bpp10dbl1	6	Pipe 1 BPP10 double-pixel register: BPP = 10 processed as 20-bit color			0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color			
bpp10dbl0_mode	5	Pipe 0 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams			0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected			
bpp10dbl0	4	Pipe 0 BPP10 double-pixel register: BPP = 10 processed as 20-bit color			0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color			
bpp12dbl3	3	Pipe 3 BPP12 double-pixel register: BPP = 12 processed as 24-bit color			0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color			
bpp12dbl2	2	Pipe 2 BPP12 double-pixel register: BPP = 12 processed as 24-bit color			0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp12dbl1	1	Pipe 1 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color
bpp12dbl0	0	Pipe 0 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color

**BACKTOP1 (0x420)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	LINE_SPL6	LINE_SPL4	—	—
<b>Reset</b>	—	—	—	—	0b0	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_SPL6	3	Enables line-based distribution to line memories for Video Pipe 6	0b0: Disable 0b1: Enable
LINE_SPL4	2	Enables line-based distribution to line memories for Video Pipe 4	0b0: Disable 0b1: Enable

**BACKTOP10 (0x429)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DE_SEL7	DE_SEL6	DE_SEL5	DE_SEL4	LS_LE_EN7	LS_LE_EN6	LS_LE_EN5	LS_LE_EN4
<b>Reset</b>	0b0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_SEL7	7	Uses HS for creation of long packets instead of DE	0b0: Use DE for creation of long packets 0b1: Use HS for creation of long packets
DE_SEL6	6	Uses HS for creation of long packets instead of DE	0b0: Use DE for creation of long packets 0b1: Use HS for creation of long packets
DE_SEL5	5	Uses HS for creation of long packets instead of DE	0b0: Use DE for creation of long packets 0b1: Use HS for creation of long packets
DE_SEL4	4	Uses HS for creation of long packets instead of DE	0b0: Use DE for creation of long packets 0b1: Use HS for creation of long packets
LS_LE_EN7	3	Enables line start line end short packets	0b0: Disable line start line end short packets 0b1: Enable line start line end short packets
LS_LE_EN6	2	Enables line start line end short packets	0b0: Disable line start line end short packets 0b1: Enable line start line end short packets
LS_LE_EN5	1	Enables line start line end short packets	0b0: Disable line start line end short packets 0b1: Enable line start line end short packets
LS_LE_EN4	0	Enables line start line end short packets	0b0: Disable line start line end short packets 0b1: Enable line start line end short packets

**BACKTOP11 (0x42A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	cmd_overflow_w7	cmd_overflow_w6	cmd_overflow_w5	cmd_overflow_w4	LMO_7	LMO_6	LMO_5	LMO_4
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>					<b>DECODE</b>	
cmd_overflow_w7	7	Pipe 7 command FIFO overflow					0b0: No overflow 0b1: Overflow	
cmd_overflow_w6	6	Pipe 6 command FIFO overflow					0b0: No overflow 0b1: Overflow	
cmd_overflow_w5	5	Pipe 5 command FIFO overflow					0b0: No overflow 0b1: Overflow	
cmd_overflow_w4	4	Pipe 4 command FIFO overflow					0b0: No overflow 0b1: Overflow	
LMO_7	3	Pipe 7 line memory overflow sticky bitfield					0b0: No overflow 0b1: Overflow	
LMO_6	2	Pipe 6 line memory overflow sticky bitfield					0b0: No overflow 0b1: Overflow	
LMO_5	1	Pipe 5 line memory overflow sticky bitfield					0b0: No overflow 0b1: Overflow	
LMO_4	0	Pipe 4 line memory overflow sticky bitfield					0b0: No overflow 0b1: Overflow	

**BACKTOP12 (0x42B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	soft_bpp_4[4:0]					–	–	–
<b>Reset</b>	0x00					–	–	–
<b>Access Type</b>	Write, Read					–	–	–
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>					<b>DECODE</b>	
soft_bpp_4	7:3	Pipe 4 BPP software-override: Software override video data BPP.					0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E, 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30	

**BACKTOP13 (0x42C)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	soft_vc_5[3:0]					soft_vc_4[3:0]		
<b>Reset</b>	0x0					0x0		
<b>Access Type</b>	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_5	7:4	Pipe 5 VC software-override	0xX: Software-defined virtual channel for Pipe 5
soft_vc_4	3:0	Pipe 4 VC software-override	0xX: Software-defined virtual channel for Pipe 4

**BACKTOP14 (0x42D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	soft_vc_7[3:0]					soft_vc_6[3:0]		
<b>Reset</b>	0x0					0x0		
<b>Access Type</b>	Write, Read					Write, Read		
BITFIELD	BITS	DESCRIPTION					DECODE	
soft_vc_7	7:4	Pipe 7 VC software-override					0xX: Software-defined virtual channel for Pipe 7	
soft_vc_6	3:0	Pipe 6 VC software-override					0xX: Software-defined virtual channel for Pipe 6	

**BACKTOP15 (0x42E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	soft_dt_5_h[1:0]					soft_dt_4[5:0]		
<b>Reset</b>	0x0					0x00		
<b>Access Type</b>	Write, Read					Write, Read		
BITFIELD	BITS	DESCRIPTION					DECODE	
soft_dt_5_h	7:6	Pipe 5 DT software-override (high nibble). Works together with soft_dt_5_l.					0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8	

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_4	5:0	Pipe 4 DT software-override	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP16 (0x42F)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>								soft_dt_5_l[3:0]
<b>Reset</b>								0x0
<b>Access Type</b>								Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_6_h	7:4	Pipe 6 DT software-override (high nibble). Works together with soft_dt_6_l.	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_5_l	3:0	Pipe 5 DT software-override (low nibble)	0xXX: Low bits of software-defined data type for Pipeline 5

**BACKTOP17 (0x430)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	soft_dt_7[5:0]						soft_dt_6_l[1:0]			
<b>Reset</b>	0x00						0x0			
<b>Access Type</b>	Write, Read						Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE					
soft_dt_7	7:2	Pipe 7 DT software-override			0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8					
soft_dt_6_l	1:0	Pipe 6 DT software-override (low nibble)			0xXX: Low bits of software-defined data type for Pipeline 6					

**BACKTOP18 (0x431)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	soft_bpp_6_h[2:0]				soft_bpp_5[4:0]			
<b>Reset</b>	0x0				0x00			
<b>Access Type</b>	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE			
soft_bpp_6_h	7:5	Pipe 6 BPP software-override (high bits): Software-override video data BPP. Works together with soft_bpp_6_l.			0x8: Datatypes = 0xA, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E, 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_5	4:0	Pipe 5 BPP software-override: Software override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E, 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30

**BACKTOP19 (0x432)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	soft_bpp_7[4:0]						soft_bpp_6_I[1:0]
<b>Reset</b>	—	0x00						0x0
<b>Access Type</b>	—	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_7	6:2	Pipe 7 BPP software-override: Software override video data BPP.	0x8: Datatypes = 0x2A, 0x10-12, 0x31-37 0xA: Datatypes = 0x2B 0xC: Datatypes = 0x2C 0xE: Datatypes = 0x2D 0x10: Datatypes = 0x22, 0x1E, 0x2E, 0x12: Datatypes = 0x23 0x14: Datatypes = 0x1F, 0x2F 0x18: Datatypes = 0x24, 0x30
soft_bpp_6_I	1:0	Pipe 6 BPP software-override (low nibble): Software override video data BPP	0bXX: Low bits of software-defined BPP

**BACKTOP21 (0x434)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	bpp8dbl7	bpp8dbl6	bpp8dbl5	bpp8dbl4	—	—	—	—
<b>Reset</b>	0b0	0b0	0b0	0b0	—	—	—	—
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl7	7	Pipe 7 BPP8 double-pixel: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl6	6	Pipe 6 BPP8 double-pixel: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl5	5	Pipe 5 BPP8 double-pixel: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl4	4	Pipe 4 BPP8 double-pixel: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color

**BACKTOP22 (0x435)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	n_vs_block[3:0]			
<b>Reset</b>	—	—	—	—	0b1			
<b>Access Type</b>	—	—	—	—	Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
n_vs_block	3:0	Frame block: Block the first 1-15 frames after video lock				0x0: All frames out 0x1: Block the first frame . . . 0xF: Block the first 15 frames		

**BACKTOP23 (0x436)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	dis_vs7	dis_vs6	dis_vs5	dis_vs4	dis_vs3	dis_vs2	dis_vs1	dis_vs0
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
dis_vs7	7	Pipe 7 disable VS: Disable the transmission of VS to MIPI output.				0b0: Enable VS out 0b1: Disable VS out		
dis_vs6	6	Pipe 6 disable VS: Disable the transmission of VS to MIPI output.				0b0: Enable VS out 0b1: Disable VS out		
dis_vs5	5	Pipe 5 disable VS: Disable the transmission of VS to MIPI output.				0b0: Enable VS out 0b1: Disable VS out		
dis_vs4	4	Pipe 4 disable VS: Disable the transmission of VS to MIPI output.				0b0: Enable VS out 0b1: Disable VS out		
dis_vs3	3	Pipe 3 disable VS: Disable the transmission of VS to MIPI output.				0b0: Enable VS out 0b1: Disable VS out		
dis_vs2	2	Pipe 2 disable VS: Disable the transmission of VS to MIPI output.				0b0: Enable VS out 0b1: Disable VS out		
dis_vs1	1	Pipe 1 disable VS: Disable the transmission of VS to MIPI output.				0b0: Enable VS out 0b1: Disable VS out		
dis_vs0	0	Pipe 0 disable VS: Disable the transmission of VS to MIPI output.				0b0: Enable VS out 0b1: Disable VS out		

**PRELIMINARY**

**BACKTOP24 (0x437)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	bpp8dbl7_m ode	bpp8dbl6_m ode	bpp8dbl5_m ode	bpp8dbl4_m ode	—	—	—	—
<b>Reset</b>	0b0	0b0	0b0	0b0	—	—	—	—
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl7_mo de	7	Pipe 7 BPP8 double-pixel mode: 8-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl6_mo de	6	Pipe 6 BPP8 double-pixel mode: 8-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl5_mo de	5	Pipe 5 BPP8 double-pixel mode: 8-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl4_mo de	4	Pipe 4 BPP8 double-pixel mode: 8-bit alternate bit mapping to memory	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected

**BACKTOP25 (0x438)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	mem_err7	mem_err6	mem_err5	mem_err4	mem_err3	mem_err2	mem_err1	mem_err0
<b>Reset</b>	0b0							
<b>Access Type</b>	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_err7	7	Pipe 7 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err6	6	Pipe 6 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err5	5	Pipe 5 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err4	4	Pipe 4 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err3	3	Pipe 3 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err2	2	Pipe 2 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err1	1	Pipe1 line memory error	0b0: No MEM error 0b1: MEM error detected
mem_err0	0	Pipe 0 line memory error	0b0: No MEM error 0b1: MEM error detected

**BACKTOP27 (0x43A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	yuv_8_10_mux_mode7	yuv_8_10_mux_mode6	yuv_8_10_mux_mode5	yuv_8_10_mux_mode4	–	–	–	–
<b>Reset</b>	0x0	0x0	0x0	0x0	–	–	–	–
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–
BITFIELD	BITS	DESCRIPTION				DECODE		
yuv_8_10_mux_mode7	7	Pipe 7 YUV422 8-bit and 10-bit mux				0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux		
yuv_8_10_mux_mode6	6	Pipe 6 YUV422 8-bit and 10-bit mux				0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux		
yuv_8_10_mux_mode5	5	Pipe 5 YUV422 8-bit and 10-bit mux				0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux		
yuv_8_10_mux_mode4	4	Pipe 4 YUV422 8-bit and 10-bit mux				0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux		

**BACKTOP30 (0x43D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	bpp10dbl7_mode	bpp10dbl7	–	–	–	–
<b>Reset</b>	–	–	0b0	0b0	–	–	–	–
<b>Access Type</b>	–	–	Write, Read	Write, Read	–	–	–	–
BITFIELD	BITS	DESCRIPTION				DECODE		
bpp10dbl7_mode	5	Pipe 7 BPP10 double-pixel mode: 10-bit alternate bit mapping to memory				0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected		
bpp10dbl7	4	Pipe 7 BPP10 double-pixel: BPP = 10 processed as 20-bit color				0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color		

**BACKTOP31 (0x43E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	bpp10dbl6_mode	bpp10dbl6	–	–	–	–	–	–
<b>Reset</b>	0b0	0b0	–	–	–	–	–	–
<b>Access Type</b>	Write, Read	Write, Read	–	–	–	–	–	–
BITFIELD	BITS	DESCRIPTION				DECODE		
bpp10dbl6_mode	7	Pipe 6 BPP10 double-pixel mode: 10-bit write map alternate mode to memory				0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected		
bpp10dbl6	6	Pipe 6 BPP10 double-pixel: BPP = 10 processed as 20-bit color				0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color		

**BACKTOP32 (0x43F)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	bpp10dbl5_mode	bpp10dbl5	bpp10dbl4_mode	bpp10dbl4	bpp12dbl7	bpp12dbl6	bpp12dbl5	bpp12dbl4
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION			DECODE			
bpp10dbl5_mode	7	Pipe 5 BPP10 double-pixel mode: 10-bit write map alternate mode to memory			0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected			
bpp10dbl5	6	Pipe 5 BPP10 double-pixel: BPP = 10 processed as 20-bit color			0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color			
bpp10dbl4_mode	5	Pipe 4 BPP10 double-pixel mode: 10-bit write map alternate mode to memory			0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected			
bpp10dbl4	4	Pipe 4 BPP10 double-pixel: BPP = 10 processed as 20-bit color			0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color			
bpp12dbl7	3	Pipe 7 BPP12 double-pixel: BPP = 12 processed as 24-bit color			0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color			
bpp12dbl6	2	Pipe 6 BPP12 double-pixel: BPP = 12 processed as 24-bit color			0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color			
bpp12dbl5	1	Pipe 5 BPP12 double-pixel: BPP = 12 processed as 24-bit color			0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color			
bpp12dbl4	0	Pipe 4 BPP12 double-pixel: BPP = 12 processed as 24bit color			0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color			

**FSYNC\_0 (0x4A0)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	—	—	FSYNC_OUT_PIN	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]			
<b>Reset</b>	—	—	0b0	0x0	0x3		0x1			
<b>Access Type</b>	—	—	Write, Read	Write, Read	Write, Read		Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE					
FSYNC_OUT_PIN	5	Selects pin to output frame sync signal (effective only when FSYNC_METH = 01)			0b0: MFP2 0b1: MFP10					
EN_VS_GEN	4	Selects whether or not VS is generated internally by the frame sync generator (not effective when FSYNC_MODE = 11)			0b0: VS is not generated internally by the frame sync generator 0b1: VS is generated internally by the frame sync generator					
FSYNC_MODE	3:2	Frame Synchronization Mode			0b00: Frame sync generation is on. GPIO is not used as FSYNC input or output 0b01: Frame sync generation is on. GPIO is used as FSYNC output and drives a slave device 0b10: Frame sync generation is off. GPIO is used as FSYNC input driven by a master device for GMSL1 links. Any enabled GPIO input can be used as FSYNC input for GMSL2 links. 0b11: Frame sync generation is off. GPIO is not used as FSYNC input or output					

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_METH	1:0	Frame Synchronization Method	0b00: Manual 0b01: Semi-auto 0b10: Auto 0b11: Reserved

**FSYNC\_1 (0x4A1)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	—	—	—	—	FSYNC_PER_DIV[3:0]				
<b>Reset</b>	—	—	—	—	0x0				
<b>Access Type</b>	—	—	—	—	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PER_DIV	3:0	Frame sync transmission period in terms of VSYNC periods	0x0: 1 0x1: 2 0x2: 3 0x3: 6 0x4: 8 0x5: 10 0x6: 12 0x7: 16 0x8: 20 0x9: 24 0xA: 32 0xB: 48 0xC: 64 0xD: 80 0xE: 96 0xF: 128

**FSYNC\_2 (0x4A2)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MST_LINK_SEL[2:0]			K_VAL_SIG_N	K_VAL[3:0]				
<b>Reset</b>	0x4			0x0	0x1				
<b>Access Type</b>	Write, Read			Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
MST_LINK_SEL	7:5	Master link select for frame sync generation	0b000: Video 0 0b001: Video 1 0b010: Video 2 0b011: Video 3 0b100: Auto select 0b101: Auto select 0b110: Auto select 0b111: Auto select
K_VAL_SIG_N	4	Sign bit of K_VAL	0b0: K_VAL is positive 0b1: K_VAL is negative

BITFIELD	BITS	DESCRIPTION	DECODE
K_VAL	3:0	Desired frame sync margin with respect to either the VSYNC of the slowest link in automatic mode or the VSYNC of the master link in semi-automatic mode.	0x0: 0.85µs 0x1: 1.71µs 0x2: 2.56µs 0x3: 3.41µs 0x4: 4.27µs 0x5: 5.12µs 0x6: 5.97µs 0x7: 6.83µs 0x8: 8.53µs 0x9: 10.24µs 0xA: 11.95µs 0xB: 13.65µs 0xC: 17.07µs 0xD: 20.48µs 0xE: 23.89µs 0xF: 27.31µs

FSYNC\_3 (0x4A3)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	P_VAL_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION						DECODE
P_VAL_L	7:0	Low byte of desired frame sync margin in terms of PCLK cycles with respect to the VSYNC of the slowest link in automatic mode or with respect to the VSYNC of the master link in semi-automatic mode						0bXXXXXXXX: Low byte of desired frame sync margin

FSYNC\_4 (0x4A4)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	P_VAL_SIG_N	P_VAL_H[4:0]				
<b>Reset</b>	—	—	0x0	0x00				
<b>Access Type</b>	—	—	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION						DECODE
P_VAL_SIG_N	5	Sign bit of P_VAL						0b0: P_VAL is positive 0b1: P_VAL is negative
P_VAL_H	4:0	High bits of desired frame sync margin in terms of PCLK cycles with respect to the VSYNC of the slowest link in automatic mode or with respect to the VSYNC of the master link in semi-automatic mode						0bXXXXX: High bits of desired frame sync margin

**FSYNC\_5 (0x4A5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FSYNC_PERIOD_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FSYNC_PER_IOD_L	7:0	Low byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)			0xXX: Low byte of number of PLCK cycles in FSYNC period			

**FSYNC\_6 (0x4A6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FSYNC_PERIOD_M[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FSYNC_PER_IOD_M	7:0	Middle byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)			0xXX: Middle byte of number of PLCK cycles in FSYNC period			

**FSYNC\_7 (0x4A7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FSYNC_PERIOD_H[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FSYNC_PER_IOD_H	7:0	High byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)			0xXX: High byte of number of PLCK cycles in FSYNC period			

**FSYNC\_8 (0x4A8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FRM_DIFF_ERR_THR_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FRM_DIFF_ERR_THR_L	7:0	Low byte of the error threshold for the difference between the earliest and latest VSyncs in terms of PCLK cycles (default is 40µs for 96MHz PCLK) (disabled when all 13 bits are 0's)			0xXX: Low byte of number of PLCK cycles in VSYNC error threshold			

[FSYNC\\_9 \(0x4A9\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	—	—	—	FRM_DIFF_ERR_THR_H[4:0]					
<b>Reset</b>	—	—	—	0x0F					
<b>Access Type</b>	—	—	—	Write, Read					
BITFIELD	BITS	DESCRIPTION				DECODE			
FRM_DIFF_ERR_THR_H	4:0	High bits of the error threshold for the difference between the earliest and latest VSYNCs in terms of PCLK cycles (default is 40µs for 96MHz PCLK) (disabled when all 13 bits are 0's)				0bXXXXX: High bits of number of PCLK cycles in VSYNC error threshold			

[FSYNC\\_10 \(0x4AA\)](#)

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	OVLP_WINDOW_L[7:0]										
<b>Reset</b>	0x00										
<b>Access Type</b>	Write, Read										
BITFIELD	BITS	DESCRIPTION				DECODE					
OVLP_WIND OW_L	7:0	Low byte of the overlap window value in terms of PCLK cycles (default is 60µs for 96MHz PCLK) (disabled when all 13 bits are 0's)				0xXX: Low byte of number of PCLK cycles in the VSYNC-FSYNC overlap window					

[FSYNC\\_11 \(0x4AB\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	EN_FGIN_L AST	—	—	OVLP_WINDOW_H[4:0]					
<b>Reset</b>	0x0	—	—	0x00					
<b>Access Type</b>	Write, Read	—	—	Write, Read					
BITFIELD	BITS	DESCRIPTION				DECODE			
EN_FGIN_LA ST	7	When set to 0, FSIN can occur anywhere with respect to VS rising edges When set to 1, FSIN should occur after all VS rising edges				0b0: FSIN can occur anywhere with respect to VS rising edges 0b1: FSIN occurs after all rising edges			
OVLP_WIND OW_H	4:0	High bits of the overlap window value in terms of PCLK cycles (default is 60µs for 96MHz PCLK) (disabled when all 13 bits are 0's)				0bXXXXX: High bits of number of PCLK cycles in the VSYNC-FSYNC overlap window			

**FSYNC\_15 (0x4AF)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FS_GPIO_TYPE	FS_USE_XTAL	—	AUTO_FS_LINKS	FS_LINK_3	FS_LINK_2	FS_LINK_1	FS_LINK_0
<b>Reset</b>	0x1	0x0	—	0x1	0x1	0x1	0x1	0x1
<b>Access Type</b>	Write, Read	Write, Read	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FS_GPIO_TYPE	7	Selects the type of FSYNC signal to output from GPIO	0b0: GSML1 type 0b1: GMSL2 type
FS_USE_XTAL	6	Uses crystal oscillator clock for generating frame sync signal	0b0: Disabled 0b1: Enabled
AUTO_FS_LINKS	4	Selects how links are selected for frame sync generation	0b0: Include links selected by FS_LINK_x register bits in frame sync generation 0b1: Include all enabled links in frame sync generation
FS_LINK_3	3	Includes Video Pipe 3 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 3 in frame sync generation 0b1: Include Video Pipe 3 in frame sync generation
FS_LINK_2	2	Includes Video Pipe 2 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 2 in frame sync generation 0b1: Include Video Pipe 2 in frame sync generation
FS_LINK_1	1	Includes Video Pipe 1 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 1 in frame sync generation 0b1: Include Video Pipe 1 in frame sync generation
FS_LINK_0	0	Includes Video Pipe 0 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 0 in frame sync generation 0b1: Include Video Pipe 0 in frame sync generation

**FSYNC\_16 (0x4B0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FSYNC_ERR_CNT[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Clears All							
BITFIELD	BITS	DESCRIPTION			DECODE			
FSYNC_ERR_CNT	7:0	Frame Sync Error Counter (resets to 0 when read or when FSYNC_LOCKED (0x4b6) goes high)			0XX: Number of frame sync errors detected since last error counter reset			

**FSYNC\_17 (0x4B1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FSYNC_TX_ID[4:0]							
<b>Reset</b>	0x1E							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_TX_ID	7:3	GPIO ID used for transmitting FSYNC signal	0bXXXXX: GPIO ID associated with FSYNC transmission
FSYNC_ERR_THR	2:0	Frame sync error reporting threshold. FSYNC_ERR_FLAG is asserted when FSYNC_ERR_CNT $\geq$ FSYNC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

**FSYNC\_18 (0x4B2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CALC_FRM_LEN_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
CALC_FRM_LEN_L	7:0	Low byte of calculated VS period of master link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)			0XX: Low byte of number of PCLKs in VS period in master link auto or semi-auto synchronization mode.			

**FSYNC\_19 (0x4B3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CALC_FRM_LEN_M[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
CALC_FRM_LEN_M	7:0	Middle byte of calculated VS period of master link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)			0XX: Middle byte of number of PCLKs in VS period in master link auto or semi-auto synchronization mode			

**FSYNC\_20 (0x4B4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CALC_FRM_LEN_H[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_H	7:0	High byte of calculated VS period of master link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)	0xXX: High byte of number of PCLKs in VS period in master link auto or semi-auto synchronization mode

**FSYNC\_21 (0x4B5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FRM_DIFF_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION					DECODE	
FRM_DIFF_L	7:0	Low byte of the difference between the fastest and the slowest frame in terms of master PCLK cycles					0xXX: Low byte of the difference between the fastest and the slowest frame	

**FSYNC\_22 (0x4B6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	FSYNC_LO_SS_OF_LO_CK	FSYNC_LO_CKED	FRM_DIFF_H[5:0]					
<b>Reset</b>	0x0	0x0	0x00					
<b>Access Type</b>	Read Clears All	Read Only	Read Only					
BITFIELD	BITS	DESCRIPTION					DECODE	
FSYNC_LOS_SS_OF_LOCK	7	Frame Synchronization Lost Lock  This bit is set to 1 when frame synchronization loses lock, it is cleared when read.					0b0: Frame synchronization loss of lock has not been detected or has been cleared by a previous read operation 0b1: Frame synchronization loss of lock has been detected	
FSYNC_LOCKED	6	Frame Synchronization Lock					0b0: Frame synchronization is not locked 0b1: Frame synchronization is locked	
FRM_DIFF_H	5:0	High bits of the difference between the fastest and the slowest frame in terms of master PCLK cycles					0bXXXXX: High bits of the difference between the fastest and the slowest frame	

**SPI\_0 (0x4E0)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	SPI_LOC_ID[1:0]			SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN		
<b>Reset</b>	0x0			0x0		0x1	0x0	0x0		
<b>Access Type</b>	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		
BITFIELD	BITS	DESCRIPTION					DECODE			
SPI_LOC_ID	7:6	Program to local ID if we are filtering packets based on header ID.					0bXX: Program to local ID			

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_CC_TR_G_ID	5:4	ID for GMSL2 header when in SPI CC bridge mode	0bXX: ID for GMSL2 header
SPI_IGNR_ID	3	Indicates whether to accept all packets regardless of header ID	0b0: Accept only packets with designated ID 0b1: Accept all packets regardless of header ID
SPI_CC_EN	2	Enables CC to SPI bridge function	0b0: Disable CC to SPI bridge function 0b1: Enable CC to SPI bridge function
MST_SLVN	1	Selects whether this chip is SPI master or SPI slave	0b0: Chip is on the near side of the GMSL2 link (near the µC), internal SPI slave is enabled 0b1: Chip is on the far side of the GMSL2 link (away from the µC), internal SPI master is enabled
SPI_EN	0	Enables SPI channel	0b0: Disable SPI channel 0b1: Enable SPI channel

**SPI\_1 (0x4E1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SPI_LOC_N[5:0]						–	–
<b>Reset</b>	0x07						–	–
<b>Access Type</b>	Write, Read						–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Maximum packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value more than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes . . . 0b111110: Packet size is 125 bytes 0b111111: Packet size is 127 bytes

**SPI\_2 (0x4E2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
<b>Reset</b>	0x0			0x0	0x0	0x0	0x1	0x1
<b>Access Type</b>	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Holds off GMSL2 request until this number of extra bytes are received on SPI port.	0bXXX: Number of extra bytes received on SPI port
FULL_SCK_SETUP	4	Samples MISO after full SCK period, rather than only half SCK period as per defacto spec	0b0: Sample MISO after half SCK period 0b1: Sample MISO after full SCK period
SPI_MOD3_F	3	Suppresses extra SCK prior to SS deassertion	0b0: Do not suppress extra SCK prior to SS deassertion 0b1: Suppress extra SCK prior to SS deassertion
SPI_MOD3	2	Enables SPI mode 3	0b0: Disable SPI mode 3 0b1: Enable SPI mode 3

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS2_ACT_H	1	Slave Select 2 (SS2) polarity	0b0: Active low 0b1: Active high
SPIM_SS1_ACT_H	0	Slave Select 1 (SS1) polarity	0b0: Active low 0b1: Active high

**SPI\_3 (0x4E3)**

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION						DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between: 1. Assertion of SS and start of SCK pulses 2. End of SCK pulses and deassertion of SS 3. Deassertion of SS and reassertion of SS (if necessary)						0xXX: Number of clocks delays

**SPI\_4 (0x4E4)**

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION						DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time						0xXX: Number of clocks for SCK low time

**SPI\_5 (0x4E5)**

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION						DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time						0xXX: Number of clocks for SCK high time

**SPI\_6 (0x4E6)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_E_N	RWN_IO_E_N
Reset	-	-	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	-	-	Read Only	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	BNE indicates the buffer not empty status.	0b0: Buffer is empty 0b1: Buffer is not empty
SPIS_RWN	4	Works in conjunction with RWN_IO_EN (Bit 0, this register) to act as a Rd/WrN control when GPIO is not available for that purpose. When RWN_IO_EN is set to 1 (GPIO enabled), SPIS_RWN is ignored. When RWN_IO_EN is set to 0 (GPIO disabled), SPIS_RWN indicates either a read or a write function.	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enables GPIO for use as Slave Select 2 output	0b0: Disable GPIO for use as Slave Select 2 output 0b1: Enable GPIO for use as Slave Select 2 output
SS_IO_EN_1	2	Enables GPIO for use as Slave Select 1 output	0b0: Disable GPIO for use as Slave Select 1 output 0b1: Enable GPIO for use as Slave Select 1 output
BNE_IO_EN	1	Enables GPIO for use as Rx buffer not empty output for SPI data available status	0b0: Disable GPIO for use as Rx buffer not empty output 0b1: Enable GPIO for use as Rx buffer not empty output
RWN_IO_EN	0	Enables GPIO for use as Rd/WrN input for control of SPI data movement.  See description of SPIS_RWN (bit 4, this register) for alternative when GPIO is disabled.	0b0: Disable GPIO for use as Rd/WrN input 0b1: Enable GPIO for use as Rd/WrN input

**SPI\_7 (0x4E7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SPI_RX_O VRFLW	SPI_TX_OV RFLW	–	SPIS_BYTE_CNT[4:0]				
<b>Reset</b>	0b0	0b0	–	0x0				
<b>Access Type</b>	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OV RFLW	7	Status flag indicating buffer overflow was detected on GMSL2 Rx buffer.	0b0: No buffer overflow detected 0b1: Buffer overflow detected
SPI_TX_OV RFLW	6	Status flag indicating buffer overflow was detected on GMSL2 Tx buffer	0b0: No buffer overflow detected 0b1: Buffer overflow detected
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer.	0bXXXXX: Number of SPI data bytes available for reading from Rx buffer

**SPI\_8 (0x4E8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	REQ_HOLD_OFF_TO[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE	
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100nS increments) for GMSL2 request hold off (0 is disable).	0xXX: Number of 100nS delay increments for GMSL2 request hold off	

SPI\_9 (0x4E9)

BIT			1	0
<b>Field</b>			SPI_0_LINK_SELECT[1:0]	
<b>Reset</b>			0x00	
<b>Access Type</b>			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE	
SPI_0_LINK_SELECT	1:0	Selects link connection for SPI Port 0	0b00: Selects GMSL2 Link A 0b01: Selects GMSL2 Link B 0b10: Selects GMSL2 Link C 0b11: Selects GMSL2 Link D	

SPI\_0 (0x4F0)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SPI_LOC_ID_1[1:0]	SPI_CC_TRG_ID_1[1:0]	SPI_IGNR_ID_1	SPI_CC_E_N_1	MST_SLVN_1	SPI_EN_1		
<b>Reset</b>	0x0	0x0	0x1	0x0	0x0	0x0		
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE	
SPI_LOC_ID_1	7:6	Programs to local ID if packets are to be filtered based on the header ID.	0bXX: Program to local ID	
SPI_CC_TRG_ID_1	5:4	ID for GMSL2 header when in SPI CC bridge mode	0bXX: GMSL2 header ID	
SPI_IGNR_ID_1	3	Indicates whether all packets are to be accepted regardless of header ID.	0b0: Accept only packets with designated ID 0b1: Accept all packets regardless of ID	
SPI_CC_EN_1	2	Enables CC to SPI bridge function	0b0: CC to SPI bridge function disabled 0b1: CC to SPI bridge function enabled	
MST_SLVN_1	1	Selects whether this chip is SPI master or SPI slave	0b0: Chip is on the near side of the GMSL2 link (near the µC), internal SPI slave is enabled 0b1: Chip is on the far side of the GMSL2 link (away from the µC), internal SPI master is enabled	
SPI_EN_1	0	Enables SPI channel	0b0: Disable SPI channel 0b1: Enable SPI channel	

SPI\_1 (0x4F1)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SPI_LOC_N_1[5:0]							—
<b>Reset</b>	0x07							—
<b>Access Type</b>	Write, Read							—

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE				
SPI_LOC_N_1	7:2	Maximum packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value more than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes . . . 0b111110: Packet size is 125 bytes 0b111111: Packet size is 127 bytes				

**SPI\_2 (0x4F2)**

BIT	7	6	5	4	3	2	1	0
Field		REQ_HOLD_OFF_1[2:0]		FULL_SCK_SETUP_1	SPI_MOD3_F_1	SPI_MOD3_1	SPIM_SS2_ACT_H_1	SPIM_SS1_ACT_H_1
Reset		0x0		0x0	0x0	0x0	0x1	0x1
Access Type		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_1	7:5	Holds off GMSL2 request until this number of extra bytes are received on SPI port.	0bXX: Number of extra bytes received on SPI port
FULL_SCK_SETUP_1	4	Samples MISO after full SCK period, rather than only half SCK period as per defacto spec	0b0: Sample MISO after half SCK period 0b1: Sample MISO after full SCK period
SPI_MOD3_F_1	3	Suppresses extra SCK prior to SS deassertion	0b0: Do not suppress extra SCK prior to SS deassertion 0b1: Suppress extra SCK prior to SS deassertion
SPI_MOD3_1	2	Enables SPI mode 3	0b0: Disable SPI mode 3 0b1: Enable SPI mode 3
SPIM_SS2_ACT_H_1	1	Slave Select 2 (SS2) polarity	0b0: Active low 0b1: Active high
SPIM_SS1_ACT_H_1	0	Slave Select 1 (SS1) polarity	0b0: Active low 0b1: Active high

**SPI\_3 (0x4F3)**

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS_1[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION					DECODE	
SPIM_SS_DLY_CLKS_1	7:0	Number of 300MHz clocks to delay between: 1. Assertion of SS and start of SCK pulses 2. End of SCK pulses and deassertion of SS 3. Deassertion of SS and reassertion of SS (if necessary)					0XXX: Number of clocks delays	

SPI\_4 (0x4F4)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	SPIM_SCK_LO_CLKS_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
SPIM_SCK_LO_CLKS_1	7:0	Number of 300MHz clocks for SCK low time							0xXX: Number of clocks for SCK low time

SPI\_5 (0x4F5)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	SPIM_SCK_HI_CLKS_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
SPIM_SCK_HI_CLKS_1	7:0	Number of 300MHz clocks for SCK high time							0xXX: Number of clocks for SCK high time

SPI\_6 (0x4F6)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	BNE_1	SPIS_RWN_1	SS_IO_EN_2_1	SS_IO_EN_1_1	BNE_IO_E_N_1	RWN_IO_E_N_1
<b>Reset</b>	—	—	0x0	0x0	0x0	0x0	0x0	0x0
<b>Access Type</b>	—	—	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION					DECODE	
BNE_1	5	BNE_1 indicates the buffer not empty status.					0b0: Buffer is empty 0b1: Buffer is not empty	
SPIS_RWN_1	4	Works in conjunction with RWN_IO_EN_1 (Bit 0, this register) to act as a Rd/WrN control when GPIO is not available for that purpose. When RWN_IO_EN is set to 1 (GPIO enabled), SPIS_RWN is ignored. When RWN_IO_EN is set to 0 (GPIO disabled), SPIS_RWN indicates either a read or a write function.					0b0: Write 0b1: Read	
SS_IO_EN_2_1	3	Enables GPIO for use as slave select 2 output					0b0: Disable GPIO for use as slave select 2 output 0b1: Enable GPIO for use as slave select 2 output	
SS_IO_EN_1_1	2	Enables GPIO for use as slave select 1 output					0b0: Disable GPIO for use as slave select 1 output 0b1: Enable GPIO for use as slave select 1 output	
BNE_IO_E_N_1	1	Enables GPIO for use as Rx buffer not empty output for SPI data available status					0b0: Disable GPIO for use as Rx buffer not empty output 0b1: Enable GPIO for use as Rx buffer not empty output	

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
RWN_IO_EN_1	0	Enables GPIO for use as Rd/WrN input for control of SPI data movement control.  See description of SPIS_RWN_1 (bit 4, this register) for alternative when GPIO is disabled.	0b0: Disable GPIO for use as Rd/WrN input 0b1: Enable GPIO for use as Rd/WrN input

**SPI\_7 (0x4F7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SPI_RX_OV_RFLW_1	SPI_TX_OV_RFLW_1	–	SPIS_BYTE_CNT_1[4:0]				
<b>Reset</b>	0b0	0b0	–	0x0				
<b>Access Type</b>	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OV_RFLW_1	7	Status flag indicating buffer overflow was detected on GMSL2 Rx buffer.	0b0: No buffer overflow detected 0b1: Buffer overflow detected
SPI_TX_OV_RFLW_1	6	Status flag indicating buffer overflow was detected on GMSL2 Tx buffer	0b0: No buffer overflow detected 0b1: Buffer overflow detected
SPIS_BYTE_CNT_1	4:0	Number of SPI data bytes available for reading from Rx buffer.	0bXXXXX: Number of SPI data bytes available for reading from Rx buffer

**SPI\_8 (0x4F8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	REQ_HOLD_OFF_TO_1[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
REQ_HOLD_OFF_TO_1	7:0	Timeout delay (in 100nS increments) for GMSL2 request hold off (0 is disable).			0xXX: Number of 100nS delay increments for GMSL2 request hold off			

**SPI\_9 (0x4F9)**

BIT			1	0
<b>Field</b>			SPI_1_LINK_SELECT[1:0]	
<b>Reset</b>			0x01	
<b>Access Type</b>			Write, Read	
BITFIELD	BITS	DESCRIPTION		DECODE
SPI_1_LINK_SELECT	1:0	Selects link connection for SPI Port 1		0b00: Selects GMSL2 link A 0b01: Selects GMSL2 link B 0b10: Selects GMSL2 link C 0b11: Selects GMSL2 link D

TR0 (0x500, 0x560)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]			
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0			
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE				
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port				0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet				
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.				0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet				
PRIO_VAL	3:2	Sets the priority for this channel's packet requests				0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority				
PRIO_CFG	1:0	Adjusts the priority to be used for requests from this channel				0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used				

TR1 (0x501, 0x561)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT[1:0]			BW_VAL[5:0]				
<b>Reset</b>	0x2			0x30				
<b>Access Type</b>	Write, Read			Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor				0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16		
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT / 10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value		

TR3 (0x503, 0x563)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	–	–	–	TX_SRC_ID[2:0]		
<b>Reset</b>	–	–	–	–	–	0x0		
<b>Access Type</b>	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x504, 0x564)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x505, 0x565)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	EN	DIS_DBL_A CK_RETX	—	—
Reset	—	—	—	—	0b1	0b0	—	—
Access Type	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION				DECODE		
EN	3	Enable ARQ				0b0: Disable ARQ 0b1: Enable ARQ		
DIS_DBL_A CK_RETX	2	Disables retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

ARQ1 (0x506, 0x566)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	MAX_RT_E RR_OEN	RT_CNT_O EN
Reset	—	—	—	—	—	—	0b1	0b0
Access Type	—	—	—	—	—	—	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER R_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—ARQ2 register) for this channel at ERRB pin				0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors		

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OE_N	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

**ARQ2 (0x507, 0x567)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR	RT_CNT[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_R	7	Reached maximum retransmit limit (MAX_RT—ARQ1) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0bXXXXXXXX: Count of retransmission for this channel

**TR0 (0x510)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_B	RX_CRC_E_N_B	–	–	PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0	
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjusts the priority to be used for requests from this channel	00: Priority from Tx adapter is used 01: Priority from Tx adapter is increased 10: Priority from Tx adapter is decreased 11: Priority in PRIO_VAL register is used

**TR1 (0x511)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	BW_MULT_B[1:0]						BW_VAL_B[5:0]			
<b>Reset</b>	0x2						0x30			
<b>Access Type</b>	Write, Read			Write, Read						
BITFIELD	BITS	DESCRIPTION			DECODE					
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor			0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16					
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth			0bXXXXXX: Channel base-bandwidth value					

**TR3 (0x513)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	—	—	—	—	—	TX_SRC_ID_B[2:0]					
<b>Reset</b>	—	—	—	—	—	0x0					
<b>Access Type</b>	—	—	—	—	—	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE						
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.			0bXXX: Source ID for packets from this channel						

**TR4 (0x514)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_SRC_SEL_B[7:0]							
<b>Reset</b>	0xFF							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
RX_SRC_SEL_B	7:0	Received Packets from Selected Sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.			0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received			

**PRELIMINARY**

**ARQ0 (0x515)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	EN_B	DIS_DBL_A CK_RETX_B	—	—
<b>Reset</b>	—	—	—	—	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
EN_B	3	Enables ARQ						0b0: Disable ARQ 0b1: Enable ARQ
DIS_DBL_A CK_RETX_B	2	Disables retransmission due to receiving same ACK twice						0b0: Enabled 0b1: Disabled

**ARQ1 (0x516)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	MAX_RT_E RR_OEN_B	RT_CNT_O EN_B
<b>Reset</b>	—	—	—	—	—	—	0b1	0b0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
MAX_RT_ER RR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_B—0x517) for this channel at ERRB pin						0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OE N_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_B—0x517 of this channel is greater than 0.						0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

**ARQ2 (0x517)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E RR_B	RT_CNT_B[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
MAX_RT_ER R_B	7	Reached maximum retransmit limit (MAX_RT_B—0x516) for one packet in this channel						0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel						0bXXXXXXXX: Count of retransmission for this channel

TR0 (0x520)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	TX_CRC_E_N_C	RX_CRC_E_N_C	–	–	PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]			
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0			
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE					
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port			0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet					
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.			0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet					
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests			0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority					
PRIO_CFG_C	1:0	Adjusts the priority to be used for requests from this channel			0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used					

TR1 (0x521)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	BW_MULT_C[1:0]			BW_VAL_C[5:0]						
<b>Reset</b>	0x2		0x30							
<b>Access Type</b>	Write, Read		Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE					
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor			0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16					
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth			0bXXXXXX: Channel base-bandwidth value					

TR3 (0x523)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	–	–	–	TX_SRC_ID_C[2:0]		
<b>Reset</b>	–	–	–	–	–	0x0		
<b>Access Type</b>	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x524)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Received packets from selected sources  Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x525)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	EN_C	DIS_DBL_A CK_RETX_C	-	-
Reset	-	-	-	-	0b1	0b0	-	-
Access Type	-	-	-	-	Write, Read	Write, Read	-	-
BITFIELD	BITS	DESCRIPTION				DECODE		
EN_C	3	Enables ARQ				0b0: Disable ARQ 0b1: Enable ARQ		
DIS_DBL_A CK_RETX_C	2	Disables retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

ARQ1 (0x526)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	MAX_RT_E RR_OEN_C	RT_CNT_O EN_C
Reset	-	-	-	-	-	-	0b1	0b0
Access Type	-	-	-	-	-	-	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER RR_OEN_C	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0x527) for this channel at ERRB pin				0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors		

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OE_N_C	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0x527) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

**ARQ2 (0x527)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR_C	RT_CNT_C[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_C	7	Reached maximum retransmit limit (MAX_RT_C—0x526) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel	0bXXXXXXXX: Count of retransmission for this channel

**TR0 (0x530)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_D	RX_CRC_E_N_D	–	–	PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0	
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_D	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x531)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]							
Reset	0x2							
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor				0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16		
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value		

TR3 (0x533)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID_D[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR4 (0x534)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
RX_SRC_SEL_D	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.				0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received		

PRELIMINARY

**ARQ0 (0x535)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	EN_D	DIS_DB <sub>L</sub> _A CK_R <sub>E</sub> TX_D	—	—
<b>Reset</b>	—	—	—	—	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
EN_D	3	Enables ARQ					0b0: Disable ARQ 0b1: Enable ARQ	
DIS_DB <sub>L</sub> _A CK_R <sub>E</sub> TX_D	2	Disables retransmission due to receiving same ACK twice					0b0: Enabled 0b1: Disabled	

**ARQ1 (0x536)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	MAX_RT_E RR_OEN_D	RT_CNT_O EN_D
<b>Reset</b>	—	—	—	—	—	—	0b1	0b0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAX_RT_E RR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_D—0x537) for this channel at ERRB pin					0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors	
RT_CNT_OE N_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0x537) of this channel is greater than 0.					0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event	

**ARQ2 (0x537)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E RR_D	RT_CNT_D[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAX_RT_E RR_D	7	Reached maximum retransmit limit (MAX_RT_D—0x536) for one packet in this channel					0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached	
RT_CNT_D	6:0	Total retransmission count in this channel					0bXXXXXXXX: Count of retransmission for this channel	

TR0 (0x570)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_B	RX_CRC_E_N_B	–	–	PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0	
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x571)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
<b>Reset</b>	0x2		0x30					
<b>Access Type</b>	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 64
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x573)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	–	–	–	TX_SRC_ID_B[2:0]		
<b>Reset</b>	–	–	–	–	–	0x0		
<b>Access Type</b>	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x574)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources  Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

ARQ0 (0x575)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	EN_B	DIS_DBL_A CK_RETX_B	-	-
Reset	-	-	-	-	0b1	0b0	-	-
Access Type	-	-	-	-	Write, Read	Write, Read	-	-
BITFIELD	BITS	DESCRIPTION				DECODE		
EN_B	3	Enable ARQ				0b0: Disable ARQ 0b1: Enable ARQ		
DIS_DBL_A CK_RETX_B	2	Disables retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

ARQ1 (0x576)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	MAX_RT_E RR_OEN_B	RT_CNT_O EN_B
Reset	-	-	-	-	-	-	0b1	0b0
Access Type	-	-	-	-	-	-	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER RR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0x577) for this channel at ERRB pin				0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors		

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OE_N_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0x577) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

**ARQ2 (0x577)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR_B	RT_CNT_B[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_B	7	Reached maximum retransmit limit (MAX_RT_B—0x576) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0bXXXXXXXX: Count of retransmission for this channel

**TR0 (0x580)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_C	RX_CRC_E_N_C	–	–	PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0	
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_C	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x581)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]							
Reset	0x2							
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor				0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16		
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value		

TR3 (0x583)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID_C[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR4 (0x584)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
RX_SRC_SEL_C	7:0	Receive packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.				0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received		

PRELIMINARY

**ARQ0 (0x585)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	EN_C	DIS_DBL_A CK_RETX_C	—	—
<b>Reset</b>	—	—	—	—	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION				DECODE		
EN_C	3	Enable ARQ				0b0: Disable ARQ 0b1: Enable ARQ		
DIS_DBL_A CK_RETX_C	2	Disable retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

**ARQ1 (0x586)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	MAX_RT_E RR_OEN_C	RT_CNT_O EN_C
<b>Reset</b>	—	—	—	—	—	—	0b1	0b0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER R_OEN_C	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0x587) for this channel at ERRB pin				0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors		
RT_CNT_OE N_C	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0x587) of this channel is greater than 0.				0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event		

**ARQ2 (0x587)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E RR_C	RT_CNT_C[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER R_C	7	Reached maximum retransmit limit (MAX_RT_C—0x586) for one packet in this channel				0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached		
RT_CNT_C	6:0	Total retransmission count in this channel				0bXXXXXXXX: Count of retransmission for this channel		

TR0 (0x590)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_D	RX_CRC_E_N_D	–	–	PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0	
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_D	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x591)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
<b>Reset</b>	0x2		0x30					
<b>Access Type</b>	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x593)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	–	–	–	TX_SRC_ID_D[2:0]		
<b>Reset</b>	–	–	–	–	–	0x0		
<b>Access Type</b>	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

**TR4 (0x594)**

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Received packets from selected sources  Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

**ARQ0 (0x595)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	EN_D	DIS_DBL_A CK_RETX_D	-	-
Reset	-	-	-	-	0b1	0b0	-	-
Access Type	-	-	-	-	Write, Read	Write, Read	-	-
BITFIELD	BITS	DESCRIPTION				DECODE		
EN_D	3	Enables ARQ				0b0: Disable ARQ 0b1: Enable ARQ		
DIS_DBL_A CK_RETX_D	2	Disables retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

**ARQ1 (0x596)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	MAX_RT_E RR_OEN_D	RT_CNT_O EN_D
Reset	-	-	-	-	-	-	0b1	0b0
Access Type	-	-	-	-	-	-	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER RR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0x597) for this channel at ERRB pin				0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors		

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OE_N_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0x597) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

**ARQ2 (0x597)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR_D	RT_CNT_D[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_D	7	Reached maximum retransmit limit (MAX_RT_D—0x596) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel	0bXXXXXXXX: Count of retransmission for this channel

**TR0 (0x5A0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_EN	RX_CRC_EN	PRIO_VAL[1:0]			PRIO_CFG[1:0]		
<b>Reset</b>	0b1	0b1	0x0			0x0		
<b>Access Type</b>	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority to be used for requests from this channel.	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

**TR1 (0x5A1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT[1:0]					BW_VAL[5:0]		
<b>Reset</b>	0x2					0x30		
<b>Access Type</b>	Write, Read					Write, Read		
BITFIELD	BITS	DESCRIPTION					DECODE	
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor					0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16	
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth					0bXXXXXX: Channel base-bandwidth value	

**TR3 (0x5A3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—					TX_SRC_ID[2:0]		
<b>Reset</b>	—					0x0		
<b>Access Type</b>	—					Write, Read		
BITFIELD	BITS	DESCRIPTION					DECODE	
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.					0bXXX: Source ID for packets from this channel	

**TR4 (0x5A4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RX_SRC_SEL[7:0]							
<b>Reset</b>	0xFF							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION					DECODE	
RX_SRC_SEL	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.					0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received	

**PRELIMINARY**

**ARQ0 (0x5A5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	EN	DIS_DBL_A CK_RETX	—	—
<b>Reset</b>	—	—	—	—	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
EN	3	Enables ARQ					0b0: Disable ARQ 0b1: Enable ARQ	
DIS_DBL_A CK_RETX	2	Disables retransmission due to receiving same ACK twice					0b0: Enabled 0b1: Disabled	

**ARQ1 (0x5A6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	MAX_RT_E RR_OEN	RT_CNT_O EN
<b>Reset</b>	—	—	—	—	—	—	0b1	0b0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAX_RT_ER R_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin					0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors	
RT_CNT_OE N	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.					0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event	

**ARQ2 (0x5A7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E RR	RT_CNT[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAX_RT_ER R	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel					0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached	
RT_CNT	6:0	Total retransmission count in this channel					0bXXXXXXXX: Count of retransmission for this channel	

TR0 (0x5B0)

BIT	7	6	5	4	3	2	1	0		
Field	TX_CRC_E_N_B	RX_CRC_E_N_B	—	—	PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]			
Reset	0b1	0b1	—	—	0x0		0x0			
Access Type	Write, Read	Write, Read	—	—	Write, Read		Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE				
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port				0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet				
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.				0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet				
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests				0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority				
PRIO_CFG_B	1:0	Adjusts the priority to be used for requests from this channel				0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used				

TR1 (0x5B1)

BIT	7	6	5	4	3	2	1	0		
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]							
Reset	0x2		0x30							
Access Type	Write, Read		Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE				
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor				0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 64				
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value				

TR3 (0x5B3)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID_B[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

**TR4 (0x5B4)**

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources  Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

**ARQ0 (0x5B5)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	EN_B	DIS_DBL_A CK_RETX_B	-	-
Reset	-	-	-	-	0b1	0b0	-	-
Access Type	-	-	-	-	Write, Read	Write, Read	-	-
BITFIELD	BITS	DESCRIPTION				DECODE		
EN_B	3	Enables ARQ				0b0: Disable ARQ 0b1: Enable ARQ		
DIS_DBL_A CK_RETX_B	2	Disables retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

**ARQ1 (0x5B6)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	MAX_RT_E RR_OEN_B	RT_CNT_O EN_B
Reset	-	-	-	-	-	-	0b1	0b0
Access Type	-	-	-	-	-	-	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER R_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_B—0x5B7) for this channel at ERRB pin				0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors		

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OE_N_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_B (0x5B7) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

**ARQ2 (0x5B7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR_B	RT_CNT_B[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_B	7	Reached maximum retransmit limit (MAX_RT_B—0x5B6) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0xXXXXXXXX: Count of retransmission for this channel

**TR0 (0x5C0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_C	RX_CRC_E_N_C	–	–	PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0	
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_C	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x5C1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]							
Reset	0x2							
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor				0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16		
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth				0bXXXXXX: Channel base-bandwidth value		

TR3 (0x5C3)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	TX_SRC_ID_C[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE		
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.				0bXXX: Source ID for packets from this channel		

TR4 (0x5C4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
RX_SRC_SEL_C	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.				0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received		

PRELIMINARY

**ARQ0 (0x5C5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	EN_C	DIS_DBL_A CK_RETX_C	—	—
<b>Reset</b>	—	—	—	—	0b1	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION				DECODE		
EN_C	3	Enables ARQ				0b0: Disable ARQ 0b1: Enable ARQ		
DIS_DBL_A CK_RETX_C	2	Disables retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

**ARQ1 (0x5C6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	MAX_RT_E RR_OEN_C	RT_CNT_O EN_C
<b>Reset</b>	—	—	—	—	—	—	0b1	0b0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER R_OEN_C	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0xC5C7) for this channel at ERRB pin				0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors		
RT_CNT_OE N_C	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0xC5C7) of this channel is greater than 0.				0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event		

**ARQ2 (0x5C7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E RR_C	RT_CNT_C[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER R_C	7	Reached maximum retransmit limit (MAX_RT_C—0x5C6) for one packet in this channel				0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached		
RT_CNT_C	6:0	Total retransmission count in this channel				0xXXXXXXXX: Count of retransmission for this channel		

TR0 (0x5D0)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TX_CRC_E_N_D	RX_CRC_E_N_D	–	–	PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
<b>Reset</b>	0b1	0b1	–	–	0x0		0x0	
<b>Access Type</b>	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_D	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x5D1)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
<b>Reset</b>	0x2		0x30					
<b>Access Type</b>	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 64
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x5D3)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	–	–	–	TX_SRC_ID_D[2:0]		
<b>Reset</b>	–	–	–	–	–	0x0		
<b>Access Type</b>	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

**TR4 (0x5D4)**

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Received packets from selected sources  Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . . 0xFF: Packets from all source IDs received

**ARQ0 (0x5D5)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	EN_D	DIS_DBL_A CK_RETX_D	-	-
Reset	-	-	-	-	0b1	0b0	-	-
Access Type	-	-	-	-	Write, Read	Write, Read	-	-
BITFIELD	BITS	DESCRIPTION				DECODE		
EN_D	3	Enables ARQ				0b0: Disable ARQ 0b1: Enable ARQ		
DIS_DBL_A CK_RETX_D	2	Disables retransmission due to receiving same ACK twice				0b0: Enabled 0b1: Disabled		

**ARQ1 (0x5D6)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	MAX_RT_E RR_OEN_D	RT_CNT_O EN_D
Reset	-	-	-	-	-	-	0b1	0b0
Access Type	-	-	-	-	-	-	Write, Read	Write, Read
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER R_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_D—0x5D7) for this channel at ERRB pin				0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors		

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OE_N_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0x5D7) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

**ARQ2 (0x5D7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAX_RT_E_RR_D	RT_CNT_D[6:0]						
<b>Reset</b>	0b0	0x0						
<b>Access Type</b>	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ER_D	7	Reached maximum retransmit limit (MAX_RT_D—5D6) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel	0xXXXXXXXX: Count of retransmission for this channel

**I2C\_0 (0x640)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	—	—	SLV_SH_P0_A[1:0]	—	SLV_TO_P0_A[2:0]						
<b>Reset</b>	—	—	0x2	—	0x6						
<b>Access Type</b>	—	—	Write, Read	—	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_A	5:4	<p>Link A GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Setup and Hold Time Setting (setup, hold)</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p> <p>Set this according to the I<sup>2</sup>C speed mode. This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	<p>0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved</p>

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO_P0_A	2:0	<p>Link A GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Timeout Setting</p> <p>Internal I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I<sup>2</sup>C\_1 (0x641)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MST_BT_P0_A[2:0]			—	MST_TO_P0_A[2:0]		
<b>Reset</b>	—	0x5			—	0x6		
<b>Access Type</b>	—	Write, Read			—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_A	6:4	<p>Link A GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device or remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2 Link A</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1 Link A.</p> <p>Set this according to the I<sup>2</sup>C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010</p>	3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed
MST_TO_P0_A	2:0	<p>Link A GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C\_2 (0x642)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_A[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-
BITFIELD	BITS	DESCRIPTION			DECODE			
SRC_A_P0_A	7:1	Link A GMSL1 AND GMSL2 I <sup>2</sup> C AddressTranslator Source A When I <sup>2</sup> C device address matches SRC_A_P0_A, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_A_P0_A. This setting applies only to I <sup>2</sup> C Port 0 for GMSL2. This setting applies to all I <sup>2</sup> C Ports for GMSL1.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_3 (0x643)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_A[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-
BITFIELD	BITS	DESCRIPTION			DECODE			
DST_A_P0_A	7:1	Link A GMSL1 AND GMSL2 I <sup>2</sup> C Address Translator Destination A This setting applies only to I <sup>2</sup> C Port 0 for GMSL2. This setting applies to all I <sup>2</sup> C Ports for GMSL1. See the description of SRC_A_P0_A.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_4 (0x644)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_A[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_A	7:1	<p>Link A GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Source B</p> <p>When I<sup>2</sup>C device address matches SRC_B_P0_A, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_B_P0_A.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . 0b1111111: Write/read device address is 0xFE/0xFF

I<sup>2</sup>C\_5 (0x645)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P0_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_A	7:1	<p>Link A GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Destination B</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p> <p>See the description of SRC_B_P0_A.</p>	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . 0b1111111: Write/read device address is 0xFE/0xFF

I<sup>2</sup>C\_0 (0x650)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	SLV_SH_P0_B[1:0]		—	SLV_TO_P0_B[2:0]		
<b>Reset</b>	—	—	0x2		—	0x6		
<b>Access Type</b>	—	—	Write, Read		—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_B	5:4	<p>Link B GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Setup and Hold Time Setting (setup, hold)</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p> <p>Set this according to the I<sup>2</sup>C speed mode.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	<p>0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved</p>
SLV_TO_P0_B	2:0	<p>Link B GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Timeout Setting</p> <p>Internal I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	<p>0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled</p>

I<sup>2</sup>C\_1 (0x651)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MST_BT_P0_B[2:0]			—	MST_TO_P0_B[2:0]		
<b>Reset</b>	—	0x5			—	0x6		
<b>Access Type</b>	—	Write, Read			—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_B	6:4	<p>Link B GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device or remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2 Link B.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1 Link B.</p> <p>Set this according to the I<sup>2</sup>C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010</p>	<p>3b000: 9.92Kbps - Set for I<sup>2</sup>C Standard-mode speed 3b001: 33.2Kbps - Set for I<sup>2</sup>C Standard-mode speed 3b010: 99.2Kbps - Set for I<sup>2</sup>C Standard or Fast-mode speed 3b011: 123Kbps - Set for I<sup>2</sup>C Fast-mode speed 3b100: 203Kbps - Set for I<sup>2</sup>C Fast-mode speed 3b101: 397Kbps - Set for I<sup>2</sup>C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I<sup>2</sup>C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I<sup>2</sup>C Fast-mode Plus speed</p>

BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P0_B	2:0	<p>Link B GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_2 (0x652)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_A_P0_B[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_B	7:1	<p>Link B GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Source A</p> <p>When I<sup>2</sup>C device address matches SRC_A_P0_B, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_A_P0_B.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_3 (0x653)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_A_P0_B[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_B	7:1	<p>Link B GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Destination A.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p> <p>See the description of SRC_A_P0_B.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C\_4 (0x654)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_B_P0_B[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
SRC_B_P0_B	7:1	Link B GMSL1 AND GMSL2 I <sup>2</sup> C Address Translator Source B When I <sup>2</sup> C device address matches SRC_B_P0_B, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P0_B. This setting applies only to I <sup>2</sup> C Port 0 for GMSL2. This setting applies to all I <sup>2</sup> C Ports for GMSL1.				0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF		

I2C\_5 (0x655)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P0_B[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
DST_B_P0_B	7:1	Link B GMSL1 AND GMSL2 I <sup>2</sup> C Address Translator Destination B This setting applies only to I <sup>2</sup> C Port 0 for GMSL2. This setting applies to all I <sup>2</sup> C Ports for GMSL1. See the description of SRC_B_P0_B.				0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF		

I2C\_0 (0x660)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	SLV_SH_P0_C[1:0]		—	SLV_TO_P0_C[2:0]		
<b>Reset</b>	—	—	0x2		—	0x6		
<b>Access Type</b>	—	—	Write, Read		—	Write, Read		

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_C	5:4	<p>Link C GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Setup and Hold Time Setting (setup, hold).</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p> <p>Set this according to the I<sup>2</sup>C speed mode. This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_C	2:0	<p>Link C GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Timeout Setting</p> <p>Internal I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I<sup>2</sup>C\_1 (0x661)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MST_BT_P0_C[2:0]			—	MST_TO_P0_C[2:0]		
<b>Reset</b>	—	0x5			—	0x6		
<b>Access Type</b>	—	Write, Read			—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_C	6:4	<p>Link C GMSL1 <b>AND</b> GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device or remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2 Link C.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1 Link C.</p> <p>Set this according to the I<sup>2</sup>C speed mode:  Fast-mode Plus = 101 to 111  Fast-mode = 010 to 101  Standard-mode = 000 to 010</p>	3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed

BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P0_C	2:0	<p>Link C GMSL1 AND GMSL2 I<sup>2</sup>C Master Timeout Setting</p> <p>Internal I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I2C\_2 (0x662)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_A_P0_C[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_C	7:1	<p>Link C GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Source A</p> <p>When I<sup>2</sup>C device address matches SRC_A_P0_C, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_A_P0_C.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I2C\_3 (0x663)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_A_P0_C[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_C	7:1	<p>Link C GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Destination A</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p> <p>See the description of SRC_A_P0_C.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C 4 (0x664)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_B_P0_C[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_C	7:1	<p>Link C GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Source B</p> <p>When I<sup>2</sup>C device address matches SRC_B_P0_C, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_B_P0_C.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C 5 (0x665)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P0_C[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_C	7:1	<p>Link C GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Destination B</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p> <p>See the description of SRC_B_P0_C.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I<sup>2</sup>C\_0 (0x670)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	SLV_SH_P0_D[1:0]	—	—	SLV_TO_P0_D[2:0]	—	—
<b>Reset</b>	—	—	0x2	—	—	0x6	—	—
<b>Access Type</b>	—	—	Write, Read	—	—	Write, Read	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_D	5:4	<p>Link D GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Setup and Hold Time Setting (setup, hold)</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p> <p>Set this according to the I<sup>2</sup>C speed mode.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	<p>0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved</p>
SLV_TO_P0_D	2:0	<p>Link D GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Timeout Setting</p> <p>Internal I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	<p>0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled</p>

I<sup>2</sup>C\_1 (0x671)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	MST_BT_P0_D[2:0]	—	—	MST_TO_P0_D[2:0]	—	—
<b>Reset</b>	—	—	0x5	—	—	0x6	—	—
<b>Access Type</b>	—	—	Write, Read	—	—	Write, Read	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_D	6:4	<p>Link D GMSL1 AND GMSL2 I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device on remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2 Link D.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1 Link D.</p> <p>Set this according to the I<sup>2</sup>C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010</p>	3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed
MST_TO_P0_D	2:0	<p>Link D GMSL1 AND GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b000: 16μs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I<sup>2</sup>C\_2 (0x672)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_D[6:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_D	7:1	<p>Link D GMSL1 AND GMSL2 I<sup>2</sup>C Address Translator Source A.</p> <p>When I<sup>2</sup>C device address matches SRC_A_P0_D, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_A_P0_D.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C\_3 (0x673)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_A_P0_D[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read			—				
BITFIELD	BITS	DESCRIPTION			DECODE			
DST_A_P0_D	7:1	Link D GMSL1 AND GMSL2 I <sup>2</sup> C Address Translator Destination A This setting applies only to I <sup>2</sup> C Port 0 for GMSL2. This setting applies to all I <sup>2</sup> C Ports for GMSL1. See the description of SRC_A_P0_D.			0b00000000: Write/read device address is 0x00/ 0x01 0b00000001: Write/read device address is 0x02/ 0x03 . . 0b11111111: Write/read device address is 0xFE/ 0xFF			

I2C\_4 (0x674)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_B_P0_D[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read			—				
BITFIELD	BITS	DESCRIPTION			DECODE			
SRC_B_P0_D	7:1	Link D GMSL1 AND GMSL2 I <sup>2</sup> C Address Translator Source B When I <sup>2</sup> C device address matches SRC_B_P0_D, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P0_D. This setting applies only to I <sup>2</sup> C Port 0 for GMSL2. This setting applies to all I <sup>2</sup> C Ports for GMSL1.			0b00000000: Write/read device address is 0x00/ 0x01 0b00000001: Write/read device address is 0x02/ 0x03 . . 0b11111111: Write/read device address is 0xFE/ 0xFF			

I2C\_5 (0x675)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P0_D[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read			—				

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_D	7:1	<p>Link D GMSL1 AND GMSL2 I<sup>2</sup>C address translator destination B.</p> <p>This setting applies only to I<sup>2</sup>C Port 0 for GMSL2.</p> <p>This setting applies to all I<sup>2</sup>C Ports for GMSL1.</p> <p>See the description of SRC_B_P0_D.</p>	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 . . . 0b1111111: Write/read device address is 0xFE/0xFF

**I2C\_0 (0x680)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	SLV_SH_P1_A[1:0]	—	—	SLV_TO_P1_A[2:0]	—	—
<b>Reset</b>	—	—	0x2	—	—	0x6	—	—
<b>Access Type</b>	—	—	Write, Read	—	—	Write, Read	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_A	5:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Setup and Hold Time Setting (setup, hold)</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p> <p>Set this according to the I<sup>2</sup>C speed mode.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link A.</p>	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_A	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link A.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I2C\_1 (0x681)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	MST_BT_P1_A[2:0]	—	—	MST_TO_P1_A[2:0]	—	—
<b>Reset</b>	—	—	0x5	—	—	0x6	—	—
<b>Access Type</b>	—	—	Write, Read	—	—	Write, Read	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_A	6:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device on remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link A.</p> <p>Set this according to the I<sup>2</sup>C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010</p>	3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed
MST_TO_P1_A	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link A.</p>	0b000: 16μs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_2 (0x682)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_A_P1_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_A	7:1	<p>GMSL2 I<sup>2</sup>C Address Translator Source A.</p> <p>When I<sup>2</sup>C device address matches SRC_A_P1_A, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_A_P1_A.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link A.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_3 (0x683)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_A_P1_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_A	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination A.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link A.  See the description of SRC_A_P1_A	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I2C\_4 (0x684)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_B_P1_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_A	7:1	GMSL2 I <sup>2</sup> C Address Translator Source B  When I <sup>2</sup> C device address matches SRC_B_P1_A, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P1_A.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link A.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I2C\_5 (0x685)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P1_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_A	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination B.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link A.  See the description of SRC_B_P1_A.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C\_0 (0x688)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	—	—	SLV_SH_P2_A[1:0]		—	SLV_TO_P2_A[2:0]				
<b>Reset</b>	—	—	0x2		—	0x6				
<b>Access Type</b>	—	—	Write, Read		—	Write, Read				
BITFIELD	BITS	DESCRIPTION					DECODE			
SLV_SH_P2_A	5:4	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I <sup>2</sup> C slave. Set this according to the I <sup>2</sup> C speed mode. This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link A.					0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved			
SLV_TO_P2_A	2:0	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Timeout Setting Internal GMSL2 I <sup>2</sup> C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link A.					0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled			

I2C\_1 (0x689)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MST_BT_P2_A[2:0]			—	MST_TO_P2_A[2:0]		
<b>Reset</b>	—	0x5			—	0x6		
<b>Access Type</b>	—	Write, Read			—	Write, Read		
BITFIELD	BITS	DESCRIPTION					DECODE	
MST_BT_P2_A	6:4	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Master Bit Rate Setting Configures the I <sup>2</sup> C bit rate used by the internal I <sup>2</sup> C master (in the device on remote side from the external I <sup>2</sup> C master). This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link A. Set this according to the I <sup>2</sup> C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010					3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed	

BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P2_A	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link A.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I2C\_2 (0x68A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_A_P2_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P2_A	7:1	<p>GMSL2 I<sup>2</sup>C Address Translator Source A</p> <p>When I<sup>2</sup>C device address matches SRC_A_P2_A, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_A_P2_A.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link A.</p>	0b00000000: Write/read device address is 0x00/ 0x01 0b00000001: Write/read device address is 0x02/ 0x03 . . 0b11111111: Write/read device address is 0xFE/ 0xFF

**I2C\_3 (0x68B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_A_P2_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P2_A	7:1	<p>GMSL2 I<sup>2</sup>C Address Translator Destination A.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link A.</p> <p>See the description of SRC_A_P2_A.</p>	0b00000000: Write/read device address is 0x00/ 0x01 0b00000001: Write/read device address is 0x02/ 0x03 . . 0b11111111: Write/read device address is 0xFE/ 0xFF

I2C\_4 (0x68C)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_B_P2_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
SRC_B_P2_A	7:1	GMSL2 I <sup>2</sup> C Address Translator Source B When I <sup>2</sup> C device address matches SRC_B_P2_A, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P2_A. This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link A.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_5 (0x68D)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P2_A[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
DST_B_P2_A	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination B. This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link A. See the description of SRC_B_P2_A.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_0 (0x690)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	SLV_SH_P1_B[1:0]			SLV_TO_P1_B[2:0]		
<b>Reset</b>	—	—	0x2			0x6		
<b>Access Type</b>	—	—	Write, Read			Write, Read		

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_B	5:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Setup and Hold Time Setting (setup, hold)</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p> <p>Set this according to the I<sup>2</sup>C speed mode.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link B.</p>	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_B	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link B.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_1 (0x691)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MST_BT_P1_B[2:0]					MST_TO_P1_B[2:0]	
<b>Reset</b>	—	0x5					0x6	
<b>Access Type</b>	—	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_B	6:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device or remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link B.</p> <p>Set this according to the I<sup>2</sup>C speed mode:  Fast-mode Plus = 101 to 111  Fast-mode = 010 to 101  Standard-mode = 000 to 010</p>	3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed
MST_TO_P1_B	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link B.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C\_2 (0x692)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_B[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-
BITFIELD	BITS	DESCRIPTION			DECODE			
SRC_A_P1_B	7:1	GMSL2 I <sup>2</sup> C Address Translator Source A.  When I <sup>2</sup> C device address matches SRC_A_P1_B, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_A_P1_B  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link B.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_3 (0x693)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_B[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-
BITFIELD	BITS	DESCRIPTION			DECODE			
DST_A_P1_B	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination A.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link B.  See the description of SRC_A_P1_B.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_4 (0x694)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_B[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_B	7:1	<p>GMSL2 I<sup>2</sup>C Address Translator Source B.</p> <p>When I<sup>2</sup>C device address matches SRC_B_P1_B, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_B_P1_B.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link B.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_5 (0x695)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	DST_B_P1_B[6:0]									
<b>Reset</b>	0x0									
<b>Access Type</b>	Write, Read						—			
BITFIELD	BITS	DESCRIPTION				DECODE				
DST_B_P1_B	7:1	<p>GMSL2 I<sup>2</sup>C Address Translator Destination B.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link B.</p> <p>See the description of SRC_B_P1_B.</p>				0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF				

**I<sup>2</sup>C\_0 (0x698)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	SLV_SH_P2_B[1:0]			—		
<b>Reset</b>	—	—	0x2			—		
<b>Access Type</b>	—	—	Write, Read			—		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P2_B	5:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Setup and Hold Time Setting (setup, hold)</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p> <p>Set this according to the I<sup>2</sup>C speed mode.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link B.</p>	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO_P2_B	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link B.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_1 (0x699)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MST_BT_P2_B[2:0]			—	MST_TO_P2_B[2:0]		
<b>Reset</b>	—	0x5			—	0x6		
<b>Access Type</b>	—	Write, Read			—	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P2_B	6:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device or remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link B.</p> <p>Set this according to the I<sup>2</sup>C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010</p>	3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed
MST_TO_P2_B	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link B.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_2 (0x69A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_A_P2_B[6:0]						—	—
<b>Reset</b>	0x0						—	—
<b>Access Type</b>	Write, Read						—	—

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P2_B	7:1	GMSL2 I <sup>2</sup> C Address Translator Source A.  When I <sup>2</sup> C device address matches SRC_A_P2_B, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_A_P2_B  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link B.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_3 (0x69B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_A_P2_B[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P2_B	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination A.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link B.  See the description of SRC_A_P2_B.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_4 (0x69C)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_B_P2_B[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P2_B	7:1	GMSL2 I <sup>2</sup> C Address Translator Source B  When I <sup>2</sup> C device address matches SRC_B_P2_B, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P2_B.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link B.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C\_5 (0x69D)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P2_B[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P2_B	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination B.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link B.  See the description of SRC_B_P2_B.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C\_0 (0x6A0)

BIT	7	6	5	4	3	2	1	0
Field	-	-	SLV_SH_P1_C[1:0]		-	SLV_TO_P1_C[2:0]		
Reset	-	-	0x2		-	0x6		
Access Type	-	-	Write, Read		-	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_C	5:4	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Setup and Hold Time Setting (setup, hold)  Configures the interval between SDA and SCL transitions when driven by the internal I <sup>2</sup> C slave.  Set this according to the I <sup>2</sup> C speed mode.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link C.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_C	2:0	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Timeout Setting  Internal GMSL2 I <sup>2</sup> C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link C.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

PRELIMINARY

I2C\_1 (0x6A1)

BIT	7	6	5	4	3	2	1	0			
Field	—	MST_BT_P1_C[2:0]			—	MST_TO_P1_C[2:0]					
Reset	—	0x5			—	0x6					
Access Type	—	Write, Read			—	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE						
MST_BT_P1_C	6:4	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Master Bit Rate Setting Configures the I <sup>2</sup> C bit rate used by the internal I <sup>2</sup> C master (in the device or remote side from the external I <sup>2</sup> C master). This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link C. Set this according to the I <sup>2</sup> C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010			3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed						
MST_TO_P1_C	2:0	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Master Timeout Setting Internal GMSL2 I <sup>2</sup> C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link C.			0b000: 16μs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled						

I2C\_2 (0x6A2)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_C[6:0]							—
Reset	0x0							—
Access Type	Write, Read							—
BITFIELD	BITS	DESCRIPTION			DECODE			
SRC_A_P1_C	7:1	GMSL2 I <sup>2</sup> C Address Translator Source A. When I <sup>2</sup> C device address matches SRC_A_P1_C, internal I <sup>2</sup> C mAstEr (on remote side) replaces the device address by DST_A_P1_C. This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link C.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_3 (0x6A3)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_C[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_C	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination A.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link C.  See the description of SRC_A_P1_C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C\_4 (0x6A4)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_C[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_C	7:1	GMSL2 I <sup>2</sup> C Address Translator Source B.  When I <sup>2</sup> C device address matches SRC_B_P1_C, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P1_C.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C\_5 (0x6A5)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_C[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_C	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination B.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link C.  See the description of SRC_B_P1_C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_0 (0x6A8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	SLV_SH_P2_C[1:0]	—	—	SLV_TO_P2_C[2:0]	—	—
<b>Reset</b>	—	—	0x2	—	—	0x6	—	—
<b>Access Type</b>	—	—	Write, Read	—	—	Write, Read	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P2_C	5:4	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Setup and Hold Time Setting (setup, hold)  Configures the interval between SDA and SCL transitions when driven by the internal I <sup>2</sup> C slave.  Set this according to the I <sup>2</sup> C speed mode.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link C.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P2_C	2:0	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Timeout Setting  Internal GMSL2 I <sup>2</sup> C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link C.	0b000: 16μs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_1 (0x6A9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	MST_BT_P2_C[2:0]	—	—	MST_TO_P2_C[2:0]	—	—
<b>Reset</b>	—	—	0x5	—	—	0x6	—	—
<b>Access Type</b>	—	—	Write, Read	—	—	Write, Read	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P2_C	6:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device on remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link C.</p> <p>Set this according to the I<sup>2</sup>C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010</p>	3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed
MST_TO_P2_C	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link C.</p>	0b000: 16μs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_2 (0x6AA)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_A_P2_C[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P2_C	7:1	<p>GMSL2 I<sup>2</sup>C Address Translator Source A.</p> <p>When I<sup>2</sup>C device address matches SRC_A_P2_C, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_A_P2_C.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link C.</p>	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_3 (0x6AB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_A_P2_C[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P2_C	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination A.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link C.  See the description of SRC_A_P2_C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I2C\_4 (0x6AC)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_B_P2_C[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P2_C	7:1	GMSL2 I <sup>2</sup> C Address Translator Source B.  When I <sup>2</sup> C device address matches SRC_B_P2_C, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P2_C.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I2C\_5 (0x6AD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P2_C[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P2_C	7:1	GMSL2 I <sup>2</sup> C address translator destination B.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link C.  See the description of SRC_B_P2_C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C\_0 (0x6B0)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	—	—	SLV_SH_P1_D[1:0]		—	SLV_TO_P1_D[2:0]				
<b>Reset</b>	—	—	0x2		—	0x6				
<b>Access Type</b>	—	—	Write, Read		—	Write, Read				
BITFIELD	BITS	DESCRIPTION					DECODE			
SLV_SH_P1_D	5:4	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I <sup>2</sup> C slave. Set this according to the I <sup>2</sup> C speed mode. This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link D.					0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved			
SLV_TO_P1_D	2:0	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Slave Timeout Setting Internal GMSL2 I <sup>2</sup> C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link D.					0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled			

I2C\_1 (0x6B1)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MST_BT_P1_D[2:0]			—	MST_TO_P1_D[2:0]		
<b>Reset</b>	—	0x5			—	0x6		
<b>Access Type</b>	—	Write, Read			—	Write, Read		
BITFIELD	BITS	DESCRIPTION					DECODE	
MST_BT_P1_D	6:4	GMSL2 I <sup>2</sup> C-to-I <sup>2</sup> C Master Bit Rate Setting Configures the I <sup>2</sup> C bit rate used by the internal I <sup>2</sup> C master (in the device or remote side from the external I <sup>2</sup> C master). This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link D. Set this according to the I <sup>2</sup> C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010					3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed	

BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P1_D	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link D.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_2 (0x6B2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_A_P1_D[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_D	7:1	<p>GMSL2 I<sup>2</sup>C Address Translator Source A</p> <p>When I<sup>2</sup>C device address matches SRC_A_P1_D, internal I<sup>2</sup>C master (on remote side) replaces the device address by DST_A_P1_D.</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link D.</p>	0b00000000: Write/read device address is 0x00/ 0x01 0b00000001: Write/read device address is 0x02/ 0x03 . . 0b11111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_3 (0x6B3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_A_P1_D[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_D	7:1	<p>GMSL2 I<sup>2</sup>C Address Translator Destination A</p> <p>This setting applies only to I<sup>2</sup>C Port 1 for GMSL2 Link D.</p> <p>See the description of SRC_A_P1_D.</p>	0b00000000: Write/read device address is 0x00/ 0x01 0b00000001: Write/read device address is 0x02/ 0x03 . . 0b11111111: Write/read device address is 0xFE/ 0xFF

I2C\_4 (0x6B4)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	SRC_B_P1_D[6:0]							-
<b>Reset</b>	0x0							-
<b>Access Type</b>	Write, Read							-
BITFIELD	BITS	DESCRIPTION			DECODE			
SRC_B_P1_D	7:1	GMSL2 I <sup>2</sup> C Address Translator Source B  When I <sup>2</sup> C device address matches SRC_B_P1_D, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P1_D.  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link D.				0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . . 0b1111111: Write/read device address is 0xFE/ 0xFF		

I2C\_5 (0x6B5)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P1_D[6:0]							-
<b>Reset</b>	0x0							-
<b>Access Type</b>	Write, Read							-
BITFIELD	BITS	DESCRIPTION			DECODE			
DST_B_P1_D	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination B  This setting applies only to I <sup>2</sup> C Port 1 for GMSL2 Link D.  See the description of SRC_B_P1_D.				0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . . 0b1111111: Write/read device address is 0xFE/ 0xFF		

I2C\_0 (0x6B8)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	-	-	SLV_SH_P2_D[1:0]			SLV_TO_P2_D[2:0]		
<b>Reset</b>	-	-	0x2			0x6		
<b>Access Type</b>	-	-	Write, Read			Write, Read		

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P2_D	5:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Setup and Hold Time Setting (setup, hold)</p> <p>Configures the interval between SDA and SCL transitions when driven by the internal I<sup>2</sup>C slave.</p> <p>Set this according to the I<sup>2</sup>C speed mode.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link D.</p>	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P2_D	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Slave Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link D.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

**I<sup>2</sup>C\_1 (0x6B9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	MST_BT_P2_D[2:0]					MST_TO_P2_D[2:0]	
<b>Reset</b>	—	0x5					0x6	
<b>Access Type</b>	—	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P2_D	6:4	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Bit Rate Setting</p> <p>Configures the I<sup>2</sup>C bit rate used by the internal I<sup>2</sup>C master (in the device or remote side from the external I<sup>2</sup>C master).</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link D.</p> <p>Set this according to the I<sup>2</sup>C speed mode:  Fast-mode Plus = 101 to 111  Fast-mode = 010 to 101  Standard-mode = 000 to 010</p>	3b000: 9.92Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b001: 33.2Kbps - Set for I <sup>2</sup> C Standard-mode speed 3b010: 99.2Kbps - Set for I <sup>2</sup> C Standard or Fast-mode speed 3b011: 123Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b100: 203Kbps - Set for I <sup>2</sup> C Fast-mode speed 3b101: 397Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I <sup>2</sup> C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I <sup>2</sup> C Fast-mode Plus speed
MST_TO_P2_D	2:0	<p>GMSL2 I<sup>2</sup>C-to-I<sup>2</sup>C Master Timeout Setting</p> <p>Internal GMSL2 I<sup>2</sup>C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.</p> <p>This setting applies only to I<sup>2</sup>C Port 2 for GMSL2 Link D.</p>	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C\_2 (0x6BA)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P2_D[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-
BITFIELD	BITS	DESCRIPTION			DECODE			
SRC_A_P2_D	7:1	GMSL2 I <sup>2</sup> C Address Translator Source A When I <sup>2</sup> C device address matches SRC_A_P2_D, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_A_P2_D. This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link D.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_3 (0x6BB)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P2_D[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-
BITFIELD	BITS	DESCRIPTION			DECODE			
DST_A_P2_D	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination A. This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link D. See the description of SRC_A_P2_D.			0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF			

I2C\_4 (0x6BC)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P2_D[6:0]							-
Reset	0x0							-
Access Type	Write, Read							-

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P2_D	7:1	GMSL2 I <sup>2</sup> C Address Translator Source B  When I <sup>2</sup> C device address matches SRC_B_P2_D, internal I <sup>2</sup> C master (on remote side) replaces the device address by DST_B_P2_D.  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link D.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**I<sup>2</sup>C\_5 (0x6BD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DST_B_P2_D[6:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P2_D	7:1	GMSL2 I <sup>2</sup> C Address Translator Destination B  This setting applies only to I <sup>2</sup> C Port 2 for GMSL2 Link D.  See the description of SRC_B_P2_D.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 . . . 0b1111111: Write/read device address is 0xFE/ 0xFF

**CMU2 (0x6C2)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	RSVD	RSVD[2:0]				RSVD	RSVD[1:0]		RSVD
<b>Reset</b>	0x0	0x00				0x00	0x00		0x00
<b>Access Type</b>	Write, Read	Write, Read				Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	Must write value of 0.
RSVD	6:4	Reserved	Must write value of 1.
RSVD	3	Reserved	Must write value of 0.
RSVD	2:1	Reserved	Must write value of 0.
RSVD	0	Reserved	Must write value of 0.

**CMU4 (0x6C4)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	A_SPEED[1:0]			B_SPEED[1:0]			C_SPEED[1:0]		D_SPEED[1:0]
<b>Reset</b>	0b00			0b00			0b00		0b00
<b>Access Type</b>	Write, Read			Write, Read			Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
A_SPEED	7:6	GPIO Slew Rate for MFP10 to MFP12  First value in the table is the typical rise/fall time for V <sub>DDIO</sub> = 1.8V, second value is for V <sub>DDIO</sub> = 3.3V.	0b00: 2ns, 1ns 0011: 4ns, 2ns 0b10: 8ns, 4ns 0b11: 16ns, 8ns
B_SPEED	5:4	GPIO Slew Rate for MFP8, MFP9, MFP13, and MFP14  First value in the table is the typical rise/fall time for V <sub>DDIO</sub> = 1.8V, second value is for V <sub>DDIO</sub> = 3.3V.	0b00: 2ns, 1ns 0b01: 4ns, 2ns 0b10: 8ns, 4ns 0b11: 16ns, 8ns
C_SPEED	3:2	GPIO Slew Rate for MFP5 to MFP7  First value in the table is the typical rise/fall time for V <sub>DDIO</sub> = 1.8V, second value is for V <sub>DDIO</sub> = 3.3V.	0b00: 2ns, 1ns 0b01: 4ns, 2ns 0b10: 8ns, 4ns 0b11: 16ns, 8ns
D_SPEED	1:0	GPIO Slew Rate for MFP0 to MFP4  First value in the table is the typical rise/fall time for V <sub>DDIO</sub> = 1.8V, second value is for V <sub>DDIO</sub> = 3.3V.	0b00: 2ns, 1ns 0b01: 4ns, 2ns 0b10: 8ns, 4ns 0b11: 16ns, 8ns

DP\_ORSTB\_CTL (0x6DF)

BIT	7	6	5	4	3	2	1	0
Field	-	DP_RST_M_IPI3	DP_RST_S_TABLE	DP_RST_M_IPI2	DP_RST_M_IPI	DP_RST_V_P	DP_RST_F_S	DP_RST_C_C
Reset	-	0x1	0x1	0x0	0x0	0x0	0x0	0x0
Access Type	-	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DP_RST_MIPI3	6	Selects RST mode CMD FIFO read pointer	0b0: Rev B behavior – CMD FIFO read pointer is not reset automatically when video lock is lost 0b1: (Default) Rev C behavior – CMD FIFO read pointer is reset automatically when video lock is lost
DP_RST_STABLE	5	Selects RST mode	0b0: Do not prevent reset glitches when changing reset behavior between individualized resets (Rev C behavior) vs. non-individualized resets (Rev B behavior) 0b1: (Default) Prevent reset glitches when changing reset behavior between individualized resets (Rev C behavior) vs. non-individualized resets (Rev B behavior)
DP_RST_MIPI2	4	Selects RST mode to MIPI controllers.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset automatically based on the associated GMSL PHY and Video Pipe reset during a one-shot reset or link reset

BITFIELD	BITS	DESCRIPTION	DECODE
DP_RST_MIPI	3	Selects RST mode to MIPI controllers.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset individually based on RST_MIPITX_LOC[3:0] (0x8C9)
DP_RST_VP	2	Selects RST mode to video_rx, vrx blocks.	0b0: (Default) Rev B behavior – All video pipes will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each video pipe will be reset individually based on the associated GMSL PHY reset during a one-shot reset or link reset
DP_RST_FS	1	Selects reset mode to frame sync block	0b0: (Default) Rev B behavior – Frame sync block will be reset during any one-shot reset or link reset 0b1: Rev C behavior – The internal frame sync block will not be reset during a one-shot reset or link reset
DP_RST_CC	0	Selects reset mode for iic_mux_uart blocks	0b0: (Default) Rev B behavior – All I <sup>2</sup> C/UART ports will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each I <sup>2</sup> C/UART port will be reset individually based on the associated GMSL PHY reset during a one-shot reset or link reset

**MIPI TX EXT0 (0x800, 0x810, 0x820, 0x830, 0x840, 0x850, 0x860, 0x870)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_0_H[2:0]				MAP_DST_0_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0_H	7:5	<p>Video Pipe Extended VC Source Mapping register 0:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_0, for use in VC extended mode. Please see MAP_SRC_0 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_0_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 0th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_0

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 0:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_0, for use in VC extended mode. Please see MAP_DST_0 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_0_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 0th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_0

**MIPI\_TX\_EXT1 (0x801, 0x811, 0x821, 0x831, 0x841, 0x851, 0x861, 0x871)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_1_H[2:0]				MAP_DST_1_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1_H	7:5	<p>Video Pipe Extended VC Source Mapping register 1:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_1, for use in VC extended mode. Please see MAP_SRC_1 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_1_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 1st mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_1

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 1:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_1, for use in VC extended mode. Please see MAP_DST_1 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_1_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 1st mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_1

**MIPI\_TX\_EXT2 (0x802, 0x812, 0x822, 0x832, 0x842, 0x852, 0x862, 0x872)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_2_H[2:0]				MAP_DST_2_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2_H	7:5	<p>Video Pipe Extended VC Source Mapping register 2:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_2, for use in VC extended mode. Please see MAP_SRC_2 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_2_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 2nd mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_2

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 2:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_2, for use in VC extended mode. Please see MAP_DST_2 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_2_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 2nd mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_2

**MIPI\_TX\_EXT3 (0x803, 0x813, 0x823, 0x833, 0x843, 0x853, 0x863, 0x873)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_3_H[2:0]				MAP_DST_3_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3_H	7:5	<p>Video Pipe Extended VC Source Mapping register 3:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_3, for use in VC extended mode. Please see MAP_SRC_3 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_3_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 3rd mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_3

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 3:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_3, for use in VC extended mode. Please see MAP_DST_3 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_3_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 3rd mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_3

**MIPI\_TX\_EXT4 (0x804, 0x814, 0x824, 0x834, 0x844, 0x854, 0x864, 0x874)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_4_H[2:0]				MAP_DST_4_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4_H	7:5	<p>Video Pipe Extended VC Source Mapping register 4:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_4, for use in VC extended mode. Please see MAP_SRC_4 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_4_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 4th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_4

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 4:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_4, for use in VC extended mode. Please see MAP_DST_4 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_4_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 4th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_4

**MIPI\_TX\_EXT5 (0x805, 0x815, 0x825, 0x835, 0x845, 0x855, 0x865, 0x875)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_5_H[2:0]				MAP_DST_5_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5_H	7:5	<p>Video Pipe Extended VC Source Mapping register 5:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_5, for use in VC extended mode. Please see MAP_SRC_5 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_5_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 5th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_5

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 5:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_5, for use in VC extended mode. Please see MAP_DST_5 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_5_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 5th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_5

**MIPI\_TX\_EXT6 (0x806, 0x816, 0x826, 0x836, 0x846, 0x856, 0x866, 0x876)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_6_H[2:0]				MAP_DST_6_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6_H	7:5	<p>Video Pipe Extended VC Source Mapping register 6:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_6, for use in VC extended mode. Please see MAP_SRC_6 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_6_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 6th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_6

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 6:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_6, for use in VC extended mode. Please see MAP_DST_6 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_6_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 6th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_6

**MIPI\_TX\_EXT7 (0x807, 0x817, 0x827, 0x837, 0x847, 0x857, 0x867, 0x877)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_7_H[2:0]				MAP_DST_7_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7_H	7:5	<p>Video Pipe Extended VC Source Mapping register 7:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_7, for use in VC extended mode. Please see MAP_SRC_7 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_7_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 7th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_7

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 7:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_7, for use in VC extended mode. Please see MAP_DST_7 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_7_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 7th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_7

**MIPI\_TX\_EXT8 (0x808, 0x818, 0x828, 0x838, 0x848, 0x858, 0x868, 0x878)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_8_H[2:0]				MAP_DST_8_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8_H	7:5	<p>Video Pipe Extended VC Source Mapping register 8:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_8, for use in VC extended mode. Please see MAP_SRC_8 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_8_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 8th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_8

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 8:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_8, for use in VC extended mode. Please see MAP_DST_8 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_8_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 8th mapping pair.</p>	0XXX: MS 3 bits of VC destination mapping for MAP_DST_8

**MIPI\_TX\_EXT9 (0x809, 0x819, 0x829, 0x839, 0x849, 0x859, 0x869, 0x879)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]				
<b>Reset</b>	0x0			0x0				
<b>Access Type</b>	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9_H	7:5	<p>Video Pipe Extended VC Source Mapping register 9:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_9, for use in VC extended mode. Please see MAP_SRC_9 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_9_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 9th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_9

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 9:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_9, for use in VC extended mode. Please see MAP_DST_9 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_9_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 9th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_9

**MIPI\_TX\_EXT10 (0x80A, 0x81A, 0x82A, 0x83A, 0x84A, 0x85A, 0x86A, 0x87A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_10_H[2:0]				MAP_DST_10_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10_H	7:5	<p>Video Pipe Extended VC Source Mapping register 10:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_10, for use in VC extended mode. Please see MAP_SRC_10 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_10_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 10th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_10

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 10:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_10, for use in VC extended mode. Please see MAP_DST_10 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_10_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 10th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_10

**MIPI\_TX\_EXT11 (0x80B, 0x81B, 0x82B, 0x83B, 0x84B, 0x85B, 0x86B, 0x87B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_11_H[2:0]				MAP_DST_11_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11_H	7:5	<p>Video Pipe Extended VC Source Mapping register 11:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_11, for use in VC extended mode. Please see MAP_SRC_11 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_11_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 11th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_11

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 11:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_11, for use in VC extended mode. Please see MAP_DST_11 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_11_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 11th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_11

**MIPI\_TX\_EXT12 (0x80C, 0x81C, 0x82C, 0x83C, 0x84C, 0x85C, 0x86C, 0x87C)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_12_H[2:0]				MAP_DST_12_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12_H	7:5	<p>Video Pipe Extended VC Source Mapping register 12:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_12, for use in VC extended mode. Please see MAP_SRC_12 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_12_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 12th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_12

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 12:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_12, for use in VC extended mode. Please see MAP_DST_12 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_12_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 12th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_12

**MIPI\_TX\_EXT13 (0x80D, 0x81D, 0x82D, 0x83D, 0x84D, 0x85D, 0x86D, 0x87D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_13_H[2:0]				MAP_DST_13_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13_H	7:5	<p>Video Pipe Extended VC Source Mapping register 13:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_13, for use in VC extended mode. Please see MAP_SRC_13 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_13_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 13th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_13

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 13:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_13, for use in VC extended mode. Please see MAP_DST_13 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_13_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 13th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_13

**MIPI\_TX\_EXT14 (0x80E, 0x81E, 0x82E, 0x83E, 0x84E, 0x85E, 0x86E, 0x87E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_14_H[2:0]				MAP_DST_14_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14_H	7:5	<p>Video Pipe Extended VC Source Mapping register 14:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_14, for use in VC extended mode. Please see MAP_SRC_14 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_14_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 14th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_14

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 14:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_14, for use in VC extended mode. Please see MAP_DST_14 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_14_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 14th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_14

**MIPI\_TX\_EXT15 (0x80F, 0x81F, 0x82F, 0x83F, 0x84F, 0x85F, 0x86F, 0x87F)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_15_H[2:0]				MAP_DST_15_H[2:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15_H	7:5	<p>Video Pipe Extended VC Source Mapping register 15:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_15, for use in VC extended mode. Please see MAP_SRC_15 register associated with this Video Pipe.</p> <p>Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_15_H.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 15th mapping pair.</p>	0bXXX: MS 3 bits of VC mapping for MAP_SRC_15

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15_H	4:2	<p>Video Pipe Extended VC Destination Mapping register 15:</p> <p>Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_15, for use in VC extended mode. Please see MAP_DST_15 register associated with this Video Pipe.</p> <p>This setting provides the corresponding destination map associated with the MAP_SRC_15_H register.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 15th mapping pair.</p>	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_15

**MIPI\_PHY0 (0x8A0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	force_csi_o_ut_en	force_clk3_en	force_clk0_en	phy_1x4b_22	phy_1x4a_22	phy_2x4	—	phy_4x2
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b1	—	0b0
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	—	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
force_csi_out_en	7	Set to force all MIPI clocks running.	0b0: Normal mode 0b1: Force all MIPI clocks running
force_clk3_en	6	Set to force PHY3 MIPI clock running.	0b0: DPHY3 not enabled as clock 0b1: DPHY3 enabled as clock
force_clk0_en	5	Set to force PHY0 MIPI clock running.	0b0: DPHY0 not enabled as clock 0b1: DPHY0 not enabled as clock
phy_1x4b_22	4	MIPI PHY 1x4b + 2x2 mode: MIPI output configured as one 4-lane port and two 2-lane ports. PHY2 and PHY3 combined as 4-lane. PHY0 and PHY1 are 2-lane ports.	0b0: 1x4b_22 not selected 0b1: 1x4b_22 selected
phy_1x4a_22	3	MIPI PHY 1x4a + 2x2 mode: MIPI output configured as one 4-lane port and two 2-lane ports. PHY0 and PHY1 combined as 4-lane. PHY2 and PHY3 are 2-lane ports.	0b0: 1x4a_22 not selected 0b1: 1x4a_22 selected
phy_2x4	2	MIPI PHY 2x4 mode: MIPI output configured as two ports with four data lanes each. PHY0 and PHY1 combined, and PHY2 and PHY3 combined.	0b0: 2x4 not selected 0b1: 2x4 selected
phy_4x2	0	MIPI PHY 4x2 mode: MIPI output configured as four 2-lane MIPI ports.	0b0: 4x2 configuration not selected 0b1: 4x2 configuration selected

MIPI PHY1 (0x8A1)

BIT	7	6	5	4	3	2	1	0				
Field	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]					
Reset	0x0		0x0		0x0		0x0					
Access Type	Write, Read		Write, Read		Write, Read		Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE							
t_hs_przero	7:6	Typical DPHY data lane HS_prep + HS_zero timing			0b00: 146ns + 24UI 0b01: 160ns + 24UI 0b10: 173ns + 24UI 0b11: 200ns + 24UI							
t_hs_prep	5:4	Typical DPHY data lane HS_prepare timing			0b00: 46.7ns + 4UI 0b01: 53.4ns + 4UI 0b10: 60.0ns + 4UI 0b11: 66.7ns + 4UI							
t_clk_trail	3:2	Typical DPHY clock HS_trail timing			0b00: 160ns 0b01: 167ns 0b10: 173ns 0b11: 180ns							
t_clk_przero	1:0	Typical DPHY clock lane HS_prepare + HS_zero timing			0b00: 306ns 0b01: 600ns 0b10: 900ns 0b11: 1200ns							

MIPI PHY2 (0x8A2)

BIT	7	6	5	4	3	2	1	0		
Field	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]			
Reset	0xF				0x1		0x0			
Access Type	Write, Read				Write, Read		Write, Read			
BITFIELD	BITS	DESCRIPTION			DECODE					
phy_Stdby_n	7:4	MIPI PHY Enable  bit [7]: Enable MIPI PHY3 bit [6]: Enable MIPI PHY2 bit [5]: Enable MIPI PHY1 bit [4]: Enable MIPI PHY0			0bXXX0: Put MIPI PHY0 in standby mode 0bXXX1: Enable MIPI PHY0 0bXX0X: Put MIPI PHY1 in standby mode 0bXX1X: Enable MIPI PHY1 0bX0XX: Put MIPI PHY2 in standby mode 0bX1XX: Enable MIPI PHY2 0b0XXX: Put MIPI PHY3 in standby mode 0b1XXX: Enable MIPI PHY3					
t_lpx	3:2	Typical DPHY Tlpx timing			0b00: 53.4ns 0b01: 106.7ns 0b10: 160ns 0b11: 213.4ns					
t_hs_trail	1:0	Typical DPHY data lane HS_trail timing			0b00: 66.7ns + 8UI 0b01: 80ns + 8UI 0b10: 93.4ns + 8UI 0b11: 106.7ns + 8UI					

MIPI\_PHY3 (0x8A3)

BIT	7	6	5	4	3	2	1	0
Field	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
Reset	0x4				0xE			
Access Type	Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE		
phy1_lane_map	7:4	<p>MIPI PHY1 lane mapping register:            bits [5:4]: Set PHY1 D0 Output mapping            bits [7:6]: Set PHY1 D1 Output mapping</p> <p>The settings for these bit fields are dependent upon the settings for the MIPI configuration (Please see register fields at Address 0x8A0)</p> <p>For MIPI configurations 4x2 and (1x4b+2x2), the following mappings apply:</p> <ul style="list-style-type: none"> <li>2'b00 = Map PHY Output to data lane D0</li> <li>2'b01 = Map PHY Output to data lane D1</li> <li>2'b10 = Map PHY Output to data lane D2</li> <li>2'b11 = Map PHY Output to data lane D3</li> </ul> <p>Please Note: CSI-2 Controller 1 is mapped to PHY1 for MIPI configurations 4x2 and (1x4b+2x2).</p> <p>For MIPI configurations 2x4 and (1x4a+2x2), the following mappings apply:</p> <ul style="list-style-type: none"> <li>2'b00 = Map PHY Output to data lane D0</li> <li>2'b01 = Map PHY Output to data lane D1</li> <li>2'b10 = Map PHY Output to data lane D2</li> <li>2'b11 = Map PHY Output to data lane D3</li> </ul> <p>Please Note: CSI-2 Controller 1 is mapped to both PHY0 and PHY1 for MIPI configurations 2x4 and (1x4a+2x2). CSI-2 Controller 0 is unused.</p>				0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3		

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_lane_map	3:0	<p>MIPI PHY0 lane mapping register: bits [1:0]: Set PHY0 D0 Output mapping bits [3:2]: Set PHY0 D1 Output mapping</p> <p>The settings for these bit fields are dependent upon the settings for the MIPI configuration (Please see register fields at Address 0x8A0).</p> <p>For MIPI configurations 4x2 and (1x4b+2x2), the following mappings apply:</p> <ul style="list-style-type: none"> <li>2'b00 = Map PHY Output to data lane D0</li> <li>2'b01 = Map PHY Output to data lane D1</li> <li>2'b10 = RSVD, do not use</li> <li>2'b11 = RSVD, do not use</li> </ul> <p>Please Note: CSI-2 Controller 0 is mapped to PHY0 for MIPI configurations 4x2 and (1x4b+2x2).</p> <p>For MIPI configurations 2x4 and (1x4a+2x2), the following mappings apply:</p> <ul style="list-style-type: none"> <li>2'b00 = Map PHY Output to data lane D0</li> <li>2'b01 = Map PHY Output to data lane D1</li> <li>2'b10 = Map PHY Output to data lane D2</li> <li>2'b11 = Map PHY Output to data lane D3</li> </ul> <p>Please Note: CSI-2 Controller 1 is mapped to both PHY0 and PHY1 for MIPI configurations 2x4 and (1x4a+2x2). CSI-2 Controller 0 is unused.</p>	<p>0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3</p>

MIPI\_PHY4 (0x8A4)

BIT	7	6	5	4	3	2	1	0	
Field	phy3_lane_map[3:0]					phy2_lane_map[3:0]			
Reset	0xE					0x4			
Access Type	Write, Read					Write, Read			

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_lane_map	7:4	<p>MIPI PHY3 lane mapping register: bits [5:4]: Set PHY3 D0 Output mapping bits [7:6]: Set PHY3 D1 Output mapping</p> <p>The settings for these bit fields are dependent upon the settings for the MIPI configuration (Please see register fields at Address 0x8A0).</p> <p>For MIPI configurations 4x2 and (1x4a+2x2), the following mappings apply:</p> <ul style="list-style-type: none"> <li>2'b00 = Map PHY Output to data lane D0</li> <li>2'b01 = Map PHY Output to data lane D1</li> <li>2'b10 = RSVD, do not use</li> <li>2'b11 = RSVD, do not use</li> </ul> <p>Please Note: CSI-2 Controller 3 is mapped to PHY3 for MIPI configurations 4x2 and (1x4a+2x2).</p> <p>For MIPI configurations 2x4 and (1x4b+2x2), the following mappings apply:</p> <ul style="list-style-type: none"> <li>2'b00 = Map PHY Output to data lane D0</li> <li>2'b01 = Map PHY Output to data lane D1</li> <li>2'b10 = Map PHY Output to data lane D2</li> <li>2'b11 = Map PHY Output to data lane D3</li> </ul> <p>Please Note: CSI-2 Controller 2 is mapped to both PHY2 and PHY3 for MIPI configurations 2x4 and (1x4b+2x2). CSI-2 Controller 3 is unused.</p>	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3
phy2_lane_map	3:0	<p>MIPI PHY2 lane mapping register: bits [1:0]: Set PHY2 D0 Output mapping bits [3:2]: Set PHY2 D1 Output mapping</p> <p>The settings for these bit fields are dependent upon the settings for the MIPI configuration (Please see register fields at Address 0x8A0)</p> <p>For MIPI configurations 4x2 and (1x4a+2x2), the following mappings apply:</p> <ul style="list-style-type: none"> <li>2'b00 = Map PHY Output to data lane D0</li> <li>2'b01 = Map PHY Output to data lane D1</li> <li>2'b10 = Map PHY Output to data lane D2</li> <li>2'b11 = Map PHY Output to data lane D3</li> </ul> <p>Please Note: CSI-2 Controller 2 is mapped to PHY2 for MIPI configurations 4x2 and (1x4a+2x2).</p> <p>For MIPI configurations 2x4 and (1x4b+2x2), the following mappings apply:</p> <ul style="list-style-type: none"> <li>2'b00 = Map PHY Output to data lane D0</li> <li>2'b01 = Map PHY Output to data lane D1</li> <li>2'b10 = Map PHY Output to data lane D2</li> <li>2'b11 = Map PHY Output to data lane D3</li> </ul> <p>Please Note: CSI-2 Controller 2 is mapped to both PHY2 and PHY3 for MIPI configurations 2x4 and (1x4b+2x2). CSI-2 Controller 3 is unused.</p>	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3

MIPI\_PHY5 (0x8A5)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	t_clk_prep[1:0]		phy1_pol_map[2:0]				phy0_pol_map[2:0]			
<b>Reset</b>	0x0		0x0				0x0			
<b>Access Type</b>	Write, Read		Write, Read				Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE				
t_clk_prep	7:6	Typical DPHY clock lane HS_prepare timing				0b00: 40ns 0b01: 46.7ns 0b10: 53.4ns 0b11: 60ns				
phy1_pol_map	5:3	MIPI PHY1 lane polarity register: bit [5]: Set polarity on PHY1 CLK lane bit [4]: Set polarity on PHY1 D1 lane bit [3]: Set polarity on PHY1 D0 lane 1'b0 = normal polarity, 1'b1 = inverted polarity				0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive				
phy0_pol_map	2:0	MIPI PHY0 lane polarity register: bit [2]: Set polarity on PHY0 CLK lane bit [1]: Set polarity on PHY0 D1 lane bit [0]: Set polarity on PHY0 D0 lane 1'b0 = normal polarity, 1'b1 = inverted polarity				0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive				

MIPI\_PHY6 (0x8A6)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	phy3_pol_map[2:0]			phy2_pol_map[2:0]		
<b>Reset</b>	—	—	0x0			0x0		
<b>Access Type</b>	—	—	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_pol_ma p	5:3	MIPI PHY3 lane polarity register: bit [5]: Set polarity on PHY3 CLK lane bit [4]: Set polarity on PHY3 D1 lane bit [3]: Set polarity on PHY3 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive
phy2_pol_ma p	2:0	MIPI PHY2 lane polarity register: bit [2]: Set polarity on PHY2 CLK lane bit [1]: Set polarity on PHY2 D1 lane bit [0]: Set polarity on PHY2 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive

MIPI\_PHY8 (0x8A8)

BIT	7	6	5	4	3	2	1	0
Field	t_lpxesc[2:0]			—	—	—	—	—
Reset	0x0			—	—	—	—	—
Access Type	Write, Read			—	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
t_lpxesc	7:5	Typical DPHY Tlpx timing in escape mode	0b000: 66.67ns 0b001: 80ns 0b010: 100ns 0b011: 133ns 0b100: 200ns 0b101: 400ns 0b110: 1000ns 0b111: 2000ns

MIPI\_PHY9 (0x8A9)

BIT	7	6	5	4	3	2	1	0
Field	t_lpxesc[2:0]				—	—	—	—
Reset	0x00				—	—	—	—
Access Type	Write, Read				—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp0	7:3	PHY copy 0, replicates data from source PHY to destination PHY	[4:3]: PHY copy 0 source [6:5]: PHY copy 0 destination [7]: PHY copy 0 enable

MIPI\_PHY10 (0x8AA)

BIT	7	6	5	4	3	2	1	0
Field				phy_cp1[4:0]		–	–	–
Reset				0x00		–	–	–
Access Type				Write, Read		–	–	–
BITFIELD	BITS	DESCRIPTION						DECODE
phy_cp1	7:3	PHY copy 1, replicates data from source PHY to destination PHY						[4:3]: PHY copy 1 source [6:5]: PHY copy 1 destination [7]: PHY copy 1 enable

MIPI\_PHY11 (0x8AB)

BIT	7	6	5	4	3	2	1	0
Field				phy_cp_err[3:0]		–	–	–
Reset				0x00		–	–	–
Access Type				Read Only		–	–	–
BITFIELD	BITS	DESCRIPTION						DECODE
phy_cp_err	7:4							0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow

MIPI\_PHY13 (0x8AD)

BIT	7	6	5	4	3	2	1	0
Field	–	–			t_t3_prebegin[5:0]			
Reset	–	–			0x00			
Access Type	–	–			Write, Read			
BITFIELD	BITS	DESCRIPTION						DECODE
t_t3_prebegin	5:0	CPHY pre-begin phase of the preamble (t3_prebegin + 1) x 7UI						0b000000: 7UI 0b000001: 14UI · · · 0b111110: 441UI 0B111111: 448UI

[MIPI\\_PHY14 \(0x8AE\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	t_t3_post[4:0]					t_t3_prep[1:0]	
<b>Reset</b>	—	0x00					0x1	
<b>Access Type</b>	—	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_t3_post	6:2	CPHY post length after HS data = (t3_post + 1) x 7UI	0bXXXXXX: CPHY post length
t_t3_prep	1:0	CPHY Ths_prepare timing	0b00: 40ns 0b01: 55ns 0b10: 66.7ns 0b11: 86.7ns

[MIPI\\_PRBS\\_0 \(0x8C0\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MIPI_PRBS_EN_P1_LN1[1:0]	MIPI_PRBS_EN_P1_LN0[1:0]	MIPI_PRBS_EN_P0_LN1[1:0]	MIPI_PRBS_EN_P0_LN0[1:0]				
<b>Reset</b>	0x0	0x0	0x0	0x0				
<b>Access Type</b>	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_PRBS_EN_P1_LN1	7:6	PRBS enable for PHY1 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P1_LN0	5:4	PRBS enable for PHY1 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P0_LN1	3:2	PRBS enable for PHY0 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P0_LN0	1:0	PRBS enable for PHY0 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled

[MIPI\\_PRBS\\_1 \(0x8C1\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MIPI_PRBS_EN_P3_LN1[1:0]	MIPI_PRBS_EN_P3_LN0[1:0]	MIPI_PRBS_EN_P2_LN1[1:0]	MIPI_PRBS_EN_P2_LN0[1:0]				
<b>Reset</b>	0x0	0x0	0x0	0x0				
<b>Access Type</b>	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_PRBS_EN_P3_LN1	7:6	PRBS enable for PHY3 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P3_LN0	5:4	PRBS enable for PHY3 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P2_LN1	3:2	PRBS enable for PHY2 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P2_LN0	1:0	PRBS enable for PHY2 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled

**MIPI\_PRBS\_3 (0x8C3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	MIPI_CUSTOM_SEED_2[1:0]	
<b>Reset</b>	—	—	—	—	—	—	0x2	
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUST OM_SEED_2	1:0	Custom seed [17:16] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [17:16]: Reset value for PRBS if enabled by MIPI custom seed enable register

**MIPI\_PRBS\_4 (0x8C4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MIPI_CUSTOM_SEED_1[7:0]							
<b>Reset</b>	0x78							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUST OM_SEED_1	7:0	Custom seed [15:8] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [15:8]: Reset value for PRBS if enabled by MIPI custom seed enable register

**MIPI\_PRBS\_5 (0x8C5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MIPI_CUSTOM_SEED_0[7:0]							
<b>Reset</b>	0x9a							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUST OM_SEED_0	7:0	Custom seed [7:0] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [7:0]: Reset value for PRBS if enabled by MIPI custom seed enable register

**MIPI PHY 15 (0x8C6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	Force_Video_Mask[3:0]						Auto_Mask_En[3:0]	
<b>Reset</b>	0x0						0xF	
<b>Access Type</b>	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
Force_Video_Mask	7:4	Forces video output to be masked (send all 0's) in 4WxH or Wx4H synchronous aggregation modes.  Masking impacts video streams from video pipes 0-3.	0bXXX1: Force video from Video Pipe 0 to be masked. 0bXX1X: Force video from Video Pipe 1 to be masked. 0bX1XX: Force video from Video Pipe 2 to be masked. 0b1XXX: Force video from Video Pipe 3 to be masked.
Auto_Mask_En	3:0	Auto Video Mask Enable  Automatically insert 0's into synchronized aggregated video outputs if a Video Pipe 0-3 video lock is lost. This allows the other video streams to continue being transmitted on the MIPI interface.	0bXXX1: Auto video mask enabled for Video Pipe 0 0bXX1X: Auto video mask enabled for Video Pipe 1 0bX1XX: Auto video mask enabled for Video Pipe 2 0b1XXX: Auto video mask enabled for Video Pipe 3

**MIPI PHY 16 (0x8C7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	Video_Mask_Restart_En[3:0]			
<b>Reset</b>	—	—	—	—	0xF			
<b>Access Type</b>	—	—	—	—	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Video_Mask_Restart_En	3:0	Automatically restarts video streams that were previously masked off due to loss of video lock	0bXXX1: Restart video from Video Pipe 0 0bXX1X: Restart video from Video Pipe 1 0bX1XX: Restart video from Video Pipe 2 0b1XXX: Restart video from Video Pipe 3

**MIPI PHY 18 (0x8C9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	RST_MIPITX_LOC[3:0]			
<b>Reset</b>	—	—	—	—	0x0			
<b>Access Type</b>	—	—	—	—	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RST_MIPITX_LOC	3:0	Active high reset to MIPI controllers. New for Rev C. Disabled by asserting DP_RST_MIPI. Bit 0: Controller 0 reset Bit 1: Controller 1 reset Bit 2: Controller 2 reset Bit 3: Controller 3 reset	0bxxx0: Controller 0 reset not asserted 0bxxx1: Controller 0 reset asserted 0bxx0x: Controller 1 reset not asserted 0bxx1x: Controller 1 reset asserted 0bx0xx: Controller 2 reset not asserted 0bx1xx: Controller 2 reset asserted 0b0xxx: Controller 3 reset not asserted 0b1xxx: Controller 3 reset asserted

**MIPI PHY\_19 (0x8D0)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	csi2_tx1_pkt_cnt[3:0]					csi2_tx0_pkt_cnt[3:0]			
<b>Reset</b>	0x00					0x00			
<b>Access Type</b>	Read Only					Read Only			
BITFIELD	BITS	DESCRIPTION			DECODE				
csi2_tx1_pkt_cnt	7:4	Packet count of CSI2 Controller 1			0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow				
csi2_tx0_pkt_cnt	3:0	Packet count of CSI2 Controller 0			0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow				

**MIPI PHY\_20 (0x8D1)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	csi2_tx3_pkt_cnt[3:0]					csi2_tx2_pkt_cnt[3:0]			
<b>Reset</b>	0x00					0x00			
<b>Access Type</b>	Read Only					Read Only			
BITFIELD	BITS	DESCRIPTION			DECODE				
csi2_tx3_pkt_cnt	7:4	Packet count of CSI2 Controller 3			0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow				
csi2_tx2_pkt_cnt	3:0	Packet count of CSI2 Controller 2			0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow				

**MIPI PHY\_21 (0x8D2)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	phy1_pkt_cnt[3:0]					phy0_pkt_cnt[3:0]			
<b>Reset</b>	0x00					0x00			
<b>Access Type</b>	Read Only					Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_pkt_cnt	7:4	Packet count of MIPI PHY1	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow
phy0_pkt_cnt	3:0	Packet count of MIPI PHY0	0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow

**MIPI\_PHY\_22 (0x8D3)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	phy3_pkt_cnt[3:0]						phy2_pkt_cnt[3:0]			
<b>Reset</b>	0x00						0x00			
<b>Access Type</b>	Read Only			Read Only						
BITFIELD	BITS	DESCRIPTION			DECODE					
phy3_pkt_cnt	7:4	Packet count of MIPI PHY3			0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow					
phy2_pkt_cnt	3:0	Packet count of MIPI PHY2			0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow					

**MIPI\_TX1 (0x901, 0x941, 0x981, 0x9C1)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	MODE[7:0]									
<b>Reset</b>	0x00									
<b>Access Type</b>	Write, Read									
BITFIELD	BITS	DESCRIPTION			DECODE					
MODE	7:0	MIPI Tx mode: b0 = 1: Enables MIPI VS short packet counter, cyclic 1~16.			0bXXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXXX1: Enable MIPI VS short packet counter					

**MIPI\_TX2 (0x902, 0x942, 0x982, 0x9C2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	STATUS[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
STATUS	7:0	MIPI Tx Status Register	0bXXXXXXXX0: SYNC mode disabled 0bXXXXXXXX1: SYNC mode enabled 0bXXXXXX0X: Video channels not in-sync 0bXXXXXX1X: Video channels in-sync 0xXXXXX0XX: No loss of video sync 0xXXXXX1XX: Video sync lost after last read of this register or reset.

MIPI\_TX3 (0x903, 0x943, 0x983, 0x9C3)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_INIT	7:0	DPHY Deskew Initial Calibration Control  The register is split into six decode segments: bit [7]: Selects auto-initial deskew calibration on or off bit [6]: Reserved bit [5]: Any bit change initiates an initial calibration if bit 4 = 1 bit [4]: Selects manual initial on or off bit [3]: Reserved bits [2:0]: Selects initial deskew width	0bXXXXXX000: Initial deskew width = 1 x 32k UI 0bXXXXXX001: Initial deskew width = 2 x 32k UI 0bXXXXXX010: Initial deskew width = 3 x 32k UI 0bXXXXXX011: Initial deskew width = 4 x 32k UI 0bXXXXXX100: Initial deskew width = 5 x 32k UI 0bXXXXXX101: Initial deskew width = 6 x 32k UI 0bXXXXXX110: Initial deskew width = 7 x 32k UI 0bXXXXXX111: Initial deskew width = 8 x 32k UI 0bXXXX0XXX: Reserved 0bXXXX1XXX: Reserved 0bXXX0XXXX: Manual initial off 0bXXX1XXXX: Manual initial on 0bXX0XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bXX1XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bXX0XXXXX: Reserved 0bX1XXXXXX: Reserved 0b0XXXXXXX: Auto initial deskew off 0b1XXXXXXX: Auto initial deskew on

MIPI\_TX4 (0x904, 0x944, 0x984, 0x9C4)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_P ER	7:0	<p>DPHY Periodic Deskew Calibration Control</p> <p>The register is split into four decode segments:</p> <p>bit [7]: Selects periodic deskew calibration on or off</p> <p>bit [6]: Selects generation on rising or falling edge of VS</p> <p>bits [5:3]: Selects periodic interval</p> <p>bits [2:0]: Selects periodic deskew width</p>	0bXXXXXX000: Periodic deskew width = 1k UI 0bXXXXXX001: Periodic deskew width = 2k UI 0bXXXXXX010: Periodic deskew width = 3k UI 0bXXXXXX011: Periodic deskew width = 4k UI 0bXXXXXX100: Periodic deskew width = 5k UI 0bXXXXXX101: Periodic deskew width = 6k UI 0bXXXXXX110: Periodic deskew width = 7k UI 0bXXXXXX111: Periodic deskew width = 8k UI 0bXX000XXX: Periodic deskew calibration generated every frame 0bXX001XXX: Periodic deskew calibration generated every 2 frames 0bXX010XXX: Periodic deskew calibration generated every 4 frames 0bXX011XXX: Periodic deskew calibration generated every 8 frames 0bXX100XXX: Periodic deskew calibration generated every 16 frames 0bXX101XXX: Periodic deskew calibration generated every 32 frames 0bXX110XXX: Periodic deskew calibration generated every 64 frames 0bXX111XXX: Periodic deskew calibration generated every 128 frames 0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS 0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS 0b0XXXXXXXX: Periodic deskew calibration off 0b1XXXXXXXX: Periodic deskew calibration on

**MIPI\_TX5 (0x905, 0x945, 0x985, 0x9C5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CSI2_T_PRE[7:0]							
<b>Reset</b>	0x71							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CSI2_T_PRE	7:0	Number of clock cycles to wait before enabling HS data			0xXX: Number of MIPI byte clocks			

**MIPI\_TX6 (0x906, 0x946, 0x986, 0x9C6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CSI2_T_POST[7:0]							
<b>Reset</b>	0x19							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CSI2_T_POS T	7:0	Number of byte clocks to hold clock active after data			0xXX: Number of MIPI byte clocks			

**MIPI\_TX7 (0x907, 0x947, 0x987, 0x9C7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CSI2_TX_GAP[7:0]							
<b>Reset</b>	0x1C							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CSI2_TX_GA_P	7:0	Sets the number of clocks to wait after the HS CLK has entered LP before enabling it again for the next transmission			0xXX: Number of MIPI byte clocks			

**MIPI\_TX8 (0x908, 0x948, 0x988, 0x9C8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CSI2_TWAKEUP_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CSI2_TWAK_EUP_L	7:0	Sets DPHY timing parameter T_wakeup. Set the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.			0xXX: Number of MIPI byte clocks			

**MIPI\_TX9 (0x909, 0x949, 0x989, 0x9C9)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CSI2_TWAKEUP_M[7:0]							
<b>Reset</b>	0x01							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CSI2_TWAK_EUP_M	7:0	Sets DPHY timing parameter T_wakeup. Set the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.			0xXX: Number of MIPI byte clocks			

**MIPI\_TX10 (0x90A, 0x94A, 0x98A, 0x9CA)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CSI2_LANE_CNT[1:0]			CSI2_CPH_Y_EN	csi2_vcx_en	—	CSI2_TWAKEUP_H[2:0]	
<b>Reset</b>	0x3			0b0	0x0	—	0x0	
<b>Access Type</b>	Write, Read			Write, Read	Write, Read	—	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	MIPI Lane Count	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes ( <b>Reserved</b> for registers 0x90A and 0x9CA) 0b11: Four data lanes ( <b>Reserved</b> for registers 0x90A and 0x9CA)
CSI2_CPHY_EN	5	CPHY Enable	0b0: DPHY mode 0b1: CPHY mode
csi2_vcx_en	4	Enables virtual channel extension	0b0: Select 2-bit VC 0b1: Select 5-bit VC (CPHY) or 4-bit VC (DPHY)
CSI2_TWAK_EUP_H	2:0	High bits of DPHY timing parameter T_wakeup. Sets the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0bXXX: Number of MIPI byte clocks

**MIPI TX11 (0x90B, 0x94B, 0x98B, 0x9CB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_EN_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION		DECODE				
MAP_EN_L	7:0	Mapping enable low byte [7:0].  Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.		0b00000000: No mapping enabled 0bXXXXXXXX1: Map SRC_0 to DES_0 0bXXXXXXXX1X: Map SRC_1 to DES_1 0bXXXXXX1XX: Map SRC_2 to DES_2 0bXXXX1XXXX: Map SRC_3 to DES_3 0bXXX1XXXX: Map SRC_4 to DES_4 0bXX1XXXXX: Map SRC_5 to DES_5 0bX1XXXXXX: Map SRC_6 to DES_6 0b1XXXXXXX: Map SRC_7 to DES_7				

**MIPI TX12 (0x90C, 0x94C, 0x98C, 0x9CC)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_EN_H[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION		DECODE				
MAP_EN_H	7:0	Mapping enable high byte [15:8].  Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.		0b00000000: No mapping enabled 0bXXXXXXXX1: Map SRC_8 to DES_8 0bXXXXXXXX1X: Map SRC_9 to DES_9 0bXXXXXX1XX: Map SRC_10 to DES_10 0bXXXX1XXXX: Map SRC_11 to DES_11 0bXXX1XXXX: Map SRC_12 to DES_12 0bXX1XXXXX: Map SRC_13 to DES_13 0bX1XXXXXX: Map SRC_14 to DES_14 0b1XXXXXXX: Map SRC_15 to DES_15				

[MIPI\\_TX13 \(0x90D, 0x94D, 0x98D, 0x9CD\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_0[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_SRC_0	7:0	Video Pipe Source Mapping Register 0 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type  In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_0_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 0th mapping pair. See register, MAP_DST_0, to program the destination setting.			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

[MIPI\\_TX14 \(0x90E, 0x94E, 0x98E, 0x9CE\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_0[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	<p>Video Pipe Destination Mapping Register 0 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_0_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 0th mapping pair. See register, MAP_SRC_0, to program the source setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX15 (0x90F, 0x94F, 0x98F, 0x9CF)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_1[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	<p>Video Pipe Source Mapping Register 1 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_1_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 1st mapping pair. See register, MAP_DST_1, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX16 \(0x910, 0x950, 0x990, 0x9D0\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_1[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_DST_1	7:0	Video Pipe Destination Mapping Register 1 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type  In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_1_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 1st mapping pair. See register, MAP_SRC_1, to program the source setting			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

[MIPI\\_TX17 \(0x911, 0x951, 0x991, 0x9D1\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_2[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	<p>Video Pipe Source Mapping Register 2 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_2_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 2nd mapping pair. See register, MAP_DST_2, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI TX18 (0x912, 0x952, 0x992, 0x9D2)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_2[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	<p>Video Pipe Destination Mapping Register 2 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_2_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 2nd mapping pair. See register, MAP_SRC_2, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX19 \(0x913, 0x953, 0x993, 0x9D3\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_3[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_SRC_3	7:0	Video Pipe Source Mapping Register 3 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type  In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_3_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 3rd mapping pair. See register, MAP_DST_3, to program the destination setting.			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

[MIPI\\_TX20 \(0x914, 0x954, 0x994, 0x9D4\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_3[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	<p>Video Pipe Destination Mapping Register 3 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_3_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 3rd mapping pair. See register, MAP_SRC_3, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX21 (0x915, 0x955, 0x995, 0x9D5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_4[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	<p>Video Pipe Source Mapping Register 4 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_4_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 4th mapping pair. See register, MAP_DST_4, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX22 \(0x916, 0x956, 0x996, 0x9D6\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_4[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION		DECODE				
MAP_DST_4	7:0	Video Pipe Destination Mapping Register 4 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type		In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_4_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 4th mapping pair. See register, MAP_SRC_4, to program the source setting				

[MIPI\\_TX23 \(0x917, 0x957, 0x997, 0x9D7\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_5[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	<p>Video Pipe Source Mapping Register 5 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_5_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 5th mapping pair. See register, MAP_DST_5, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX24 (0x918, 0x958, 0x998, 0x9D8)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_5[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	<p>Video Pipe Destination Mapping Register 5 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_5_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 5th mapping pair. See register, MAP_SRC_5, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX25 \(0x919, 0x959, 0x999, 0x9D9\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_6[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
MAP_SRC_6	7:0	Video Pipe Source Mapping Register 6 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type  In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_6_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 6th mapping pair. See register, MAP_DST_6, to program the destination setting.			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

[MIPI\\_TX26 \(0x91A, 0x95A, 0x99A, 0x9DA\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_6[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	<p>Video Pipe Destination Mapping Register 6 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_6_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 6th mapping pair. See register, MAP_SRC_6, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX27 (0x91B, 0x95B, 0x99B, 0x9DB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_7[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	<p>Video Pipe Source Mapping Register 7 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_7_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 7th mapping pair. See register, MAP_DST_7, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX28 \(0x91C, 0x95C, 0x99C, 0x9DC\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_7[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION		DECODE				
MAP_DST_7	7:0	Video Pipe Destination Mapping Register 7 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type		In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_7_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 7th mapping pair. See register, MAP_SRC_7, to program the source setting				

[MIPI\\_TX29 \(0x91D, 0x95D, 0x99D, 0x9DD\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_8[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	<p>Video Pipe Source Mapping Register 8 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_8_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 8th mapping pair. See register, MAP_DST_8, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI TX30 (0x91E, 0x95E, 0x99E, 0x9DE)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_8[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	<p>Video Pipe Destination Mapping Register 8 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_8_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 8th mapping pair. See register, MAP_SRC_8, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX31 \(0x91F, 0x95F, 0x99F, 0x9DF\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_9[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_SRC_9	7:0	Video Pipe Source Mapping Register 9 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type  In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_9_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 9th mapping pair. See register, MAP_DST_9, to program the destination setting.			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

[MIPI\\_TX32 \(0x920, 0x960, 0x9A0, 0x9E0\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_9[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	<p>Video Pipe Destination Mapping Register 9 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_9_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 9th mapping pair. See register, MAP_SRC_9, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX33 (0x921, 0x961, 0x9A1, 0x9E1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_10[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	<p>Video Pipe Source Mapping Register 10 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_10_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 10th mapping pair. See register, MAP_DST_10, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX34 \(0x922, 0x962, 0x9A2, 0x9E2\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_10[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION			DECODE				
MAP_DST_10	7:0	Video Pipe Destination Mapping Register 10 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type  In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_10_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 10th mapping pair. See register, MAP_SRC_10, to program the source setting				[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

[MIPI\\_TX35 \(0x923, 0x963, 0x9A3, 0x9E3\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_11[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	<p>Video Pipe Source Mapping Register 11 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_11_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 11th mapping pair. See register, MAP_DST_11, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX36 (0x924, 0x964, 0x9A4, 0x9E4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_11[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	<p>Video Pipe Destination Mapping Register 11 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_11_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 11th mapping pair. See register, MAP_SRC_11, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI TX37 \(0x925, 0x965, 0x9A5, 0x9E5\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_12[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION		DECODE				
MAP_SRC_12	7:0	Video Pipe Source Mapping Register 12 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type		In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_12_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 12th mapping pair. See register, MAP_DST_12, to program the destination setting.				

[MIPI TX38 \(0x926, 0x966, 0x9A6, 0x9E6\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_12[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

PRELIMINARY

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	<p>Video Pipe Destination Mapping Register 12 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments:</p> <ul style="list-style-type: none"> <li>bits [7:6]: VC - Virtual channel</li> <li>bits [5:0]: DT - Data type</li> </ul> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_12_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 12th mapping pair. See register, MAP_SRC_12, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX39 (0x927, 0x967, 0x9A7, 0x9E7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_13[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	<p>Video Pipe Source Mapping Register 13 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments:</p> <ul style="list-style-type: none"> <li>bits [7:6]: VC - Virtual channel</li> <li>bits [5:0]: DT - Data type</li> </ul> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_13_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 13th mapping pair. See register, MAP_DST_13, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX40 \(0x928, 0x968, 0x9A8, 0x9E8\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_13[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION		DECODE				
MAP_DST_13	7:0	Video Pipe Destination Mapping Register 13 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type		In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_13_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 13th mapping pair. See register, MAP_SRC_13, to program the source setting				
				[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX				

[MIPI\\_TX41 \(0x929, 0x969, 0x9A9, 0x9E9\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_14[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	<p>Video Pipe Source Mapping Register 14 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_14_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 14th mapping pair. See register, MAP_DST_14, to program the destination setting.</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX42 (0x92A, 0x96A, 0x9AA, 0x9EA)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_14[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	<p>Video Pipe Destination Mapping Register 14 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_14_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 14th mapping pair. See register, MAP_SRC_14, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

[MIPI\\_TX43 \(0x92B, 0x96B, 0x9AB, 0x9EB\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_15[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_SRC_15	7:0	Video Pipe Source Mapping Register 15 - Virtual Channel / Data Type  The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type  In addition, the VC field can be extended using VC extended mode. Please see register MAP_SRC_15_H associated with this Video Pipe.  The Data Type field decode matches that in the MIPI specification.  Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the 15th mapping pair. See register, MAP_DST_15, to program the destination setting.			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

[MIPI\\_TX44 \(0x92C, 0x96C, 0x9AC, 0x9EC\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_15[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	<p>Video Pipe Destination Mapping Register 15 - Virtual Channel / Data Type</p> <p>The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type</p> <p>In addition, the VC field can be extended using VC extended mode. Please see register MAP_DST_15_H associated with this Video Pipe.</p> <p>The Data Type field decode matches that in the MIPI specification.</p> <p>Please Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the 15th mapping pair. See register, MAP_SRC_15, to program the source setting</p>	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI TX45 (0x92D, 0x96D, 0x9AD, 0x9ED)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DPHY_DEST_3[1:0]			MAP_DPHY_DEST_2[1:0]			MAP_DPHY_DEST_1[1:0]	
<b>Reset</b>	0x0			0x0			0x0	
<b>Access Type</b>	Write, Read			Write, Read			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	<p>DPHY and CPHY Mapping destination controller register.</p> <p>CSI2 PHY destination for MAP_SRC_3 and MAP_DST_3 mapping registers.</p>	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_2	5:4	<p>DPHY and CPHY Mapping destination controller register.</p> <p>CSI2 PHY destination for MAP_SRC_2 and MAP_DST_2 mapping registers.</p>	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_1	3:2	<p>DPHY and CPHY Mapping destination controller register.</p> <p>CSI2 PHY destination for MAP_SRC_1 and MAP_DST_1 mapping registers</p>	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_0	1:0	<p>DPHY and CPHY Mapping destination controller register.</p> <p>CSI2 PHY destination for MAP_SRC_0 and MAP_DST_0 mapping registers.</p>	0b00: Map to controller 0 0b01: Map to controller 1 0b10: Map to controller 2 0b11: Map to controller 3

**MIPI\_TX46 (0x92E, 0x96E, 0x9AE, 0x9EE)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_7 and MAP_DST_7 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_6	5:4	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_6 and MAP_DST_6 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_5	3:2	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_5 and MAP_DST_5 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_4	1:0	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_4 and MAP_DST_4 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

**MIPI\_TX47 (0x92F, 0x96F, 0x9AF, 0x9EF)**

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_11 and MAP_DST_11 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_10	5:4	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_10 and MAP_DST_10 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_9	3:2	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_9 and MAP_DST_9 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_8	1:0	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_8 and MAP_DST_8 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

**MIPI\_TX48 (0x930, 0x970, 0x9B0, 0x9F0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
<b>Reset</b>	0x0			0x0			0x0	
<b>Access Type</b>	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_15 and MAP_DST_15 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_14	5:4	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_14 and MAP_DST_14 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_13	3:2	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_13 and MAP_DST_13 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_12	1:0	DPHY and CPHY Mapping destination controller register.  CSI2 PHY destination for MAP_SRC_12 and MAP_DST_12 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

**MIPI\_TX49 (0x931, 0x971, 0x9B1, 0x9F1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_CON[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_CON	7:0	<p>MIPI controller SYNC concatenation register.</p> <p>The register is split into four decode segments:</p> <p>bit [7]: 1'b1 = 4WxH, 1'b0 = Wx4H</p> <p>bit [6]: Reserved</p> <p>bits [5:4]: Select the first line to concatenate. All others follow in order bits [3:0].</p> <p>2'b00 = Select Pipe 0 to be the master</p> <p>2'b01 = Select Pipe 1 to be the master</p> <p>2'b10 = Select Pipe 2 to be the master</p> <p>2'b11 = Select Pipe 3 to be the master</p> <p>bit [3]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 3</p> <p>bit [2]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 2</p> <p>bit [1]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 1</p> <p>bit [0]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 0</p>	<p>0bXXXXXXXX1: Concatenate Video Pipeline 0</p> <p>0bXXXXXX1X: Concatenate Video Pipeline 1</p> <p>0bXXXXX1XX: Concatenate Video Pipeline 2</p> <p>0bXXX1XXX: Concatenate Video Pipeline 3</p> <p>0bXX00XXXX: Select Video Pipeline 0 as master</p> <p>0bXX01XXXX: Select Video Pipeline 1 as master</p> <p>0bXX10XXXX: Select Video Pipeline 2 as master</p> <p>0bXX11XXXX: Select Video Pipeline 3 as master</p> <p>0b0XXXXXXX: Enable Wx4H mode</p> <p>0b1XXXXXXX: Enable 4WxH mode</p>

**MIPI\_TX50 (0x932, 0x972, 0x9B2, 0x9F2)**

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	Periodic deskew select register. The register is split into three decode segments: bit [7]: Select periodic deskew calibration for one or all virtual channels bits [6:5]: Reserved bits [4:0]: Virtual channel to generate periodic deskew calibration when only one channel is selected by bit 7	0bxxxxxxxx: Generate periodic calibration deskew calibration on all virtual channels 0b1xx00000: Periodic deskew calibration generated by virtual Channel 0 0b1xx00001: Periodic deskew calibration generated by virtual Channel 1 0b1xx00010: Periodic deskew calibration generated by virtual Channel 2 0b1xx00011: Periodic deskew calibration generated by virtual Channel 3 0b1xx00100: Periodic deskew calibration generated by virtual Channel 4 0b1xx00101: Periodic deskew calibration generated by virtual Channel 5 0b1xx00110: Periodic deskew calibration generated by virtual Channel 6 0b1xx00111: Periodic deskew calibration generated by virtual Channel 7 0b1xx01000: Periodic deskew calibration generated by virtual Channel 8 0b1xx01001: Periodic deskew calibration generated by virtual Channel 9 0b1xx01010: Periodic deskew calibration generated by virtual Channel 10 0b1xx01011: Periodic deskew calibration generated by virtual Channel 11 0b1xx01100: Periodic deskew calibration generated by virtual Channel 12 0b1xx01101: Periodic deskew calibration generated by virtual Channel 13 0b1xx01110: Periodic deskew calibration generated by virtual Channel 14 0b1xx01111: Periodic deskew calibration generated by virtual Channel 15

MIPI TX51 (0x933, 0x973, 0x9B3, 0x9F3)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
<b>Reset</b>	—	—	—	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	—	—	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALT2_MEM_MAP8	4	Alternative memory read mapping enable for 8-bit DT when sharing the same video pipe with RAW16	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
MODE_DT	3	Select 24-bit mode for user-defined data types	0b0: 24-bit mode for user-defined data types not enabled 0b1: 24-bit mode for user-defined data types enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_MEM_MAP10	2	Alternative memory read mapping enable for 10-bit DT	0b0: Alternative memory read mapping not enabled for 10-bit DT 0b1: Alternative memory read mapping enabled for 10-bit DT
ALT_MEM_MAP8	1	Alternative memory read mapping enable for 8-bit DT	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
ALT_MEM_MAP12	0	Alternative memory read mapping enable for 12-bit DT	0b0: Alternative memory read mapping not enabled for 12-bit DT 0b1: Alternative memory read mapping enabled for 12-bit DT

**MIPI TX52 (0x934, 0x974, 0x9B4, 0x9F4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	video_masked_latched[3:0]							video_masked[3:0]
<b>Reset</b>	0x0							0x0
<b>Access Type</b>	Read Only							Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
video_masked_latched	7:4	Indicates video pipes 0-3 were masked off at one point while in 4WxH or Wx4H synchronous aggregation mode.	0bXXXX1: Video pipe 0 previously masked off 0bXX1X: Video pipe 1 previously masked off 0bX1XX: Video pipe 2 previously masked off 0b1XXX: Video pipe 3 previously masked off
video_masked	3:0	Video pipe currently masked off while in 4WxH or Wx4H synchronous aggregation mode.	0bXXXX1: Video pipe 0 previously masked off 0bXX1X: Video pipe 1 previously masked off 0bX1XX: Video pipe 2 previously masked off 0b1XXX: Video pipe 3 previously masked off

**MIPI TX11 (0xA0B, 0xA4B, 0xA8B, 0xACB)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_EN_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. MAP_EN[15:0]: each bit enable 1 of maximum 16 mapping and distribution entries for current video stream. Non-matched VC/DT pass to corresponding CSI2 controller.	0b00000000: No mapping enabled 0bXXXXXXXX1: Map SRC_0 to DES_0 0bXXXXXX1X: Map SRC_1 to DES_1 0bXXXXXX1XX: Map SRC_2 to DES_2 0bXXXXXX1XXX: Map SRC_3 to DES_3 0bXXX1XXXX: Map SRC_4 to DES_4 0bXX1XXXXX: Map SRC_5 to DES_5 0bX1XXXXXX: Map SRC_6 to DES_6 0b1XXXXXXX: Map SRC_7 to DES_7

**MIPI\_TX12 (0xA0C, 0xA4C, 0xA8C, 0xACC)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_EN_H[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_EN_H	7:0	Mapping enable high byte [15:8]. MAP_EN[15:0]: each bit enable 1 of maximum 16 mapping and distribution entries for current video stream. Non-matched VC/DT pass to corresponding CSI2 controller.			0b0000000: No mapping enabled 0bXXXXXXXX1: Map SRC_8 to DES_8 0bXXXXXXXX1X: Map SRC_9 to DES_9 0bXXXXXX1XX: Map SRC_10 to DES_10 0bXXXXX1XXX: Map SRC_11 to DES_11 0bXXX1XXXX: Map SRC_12 to DES_12 0bXX1XXXXX: Map SRC_13 to DES_13 0bX1XXXXXX: Map SRC_14 to DES_14 0b1XXXXXXX: Map SRC_15 to DES_15			

**MIPI\_TX13 (0xA0D, 0xA4D, 0xA8D, 0xACD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_0[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_SRC_0	7:0	Mapping Regulator Source - Virtual Channel / Data Type			[7:6]: VC – 0bXX [5:0]: DT – 0bXXXXXX			

**MIPI\_TX14 (0xA0E, 0xA4E, 0xA8E, 0xACE)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_0[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_DST_0	7:0	Mapping Regulator Target - Virtual Channel / Data Type			[7:6]: VC – 0bXX [5:0]: DT – 0bXXXXXX			

**MIPI\_TX15 (0xA0F, 0xA4F, 0xA8F, 0xAF)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_1[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
MAP_SRC_1	7:0	Mapping Regulator Source - Virtual Channel / Data Type			[7:6]: VC – 0bXX [5:0]: DT – 0bXXXXXX			

MIPI\_TX16 (0xA10, 0xA50, 0xA90, 0xAD0)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_1	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX17 (0xA11, 0xA51, 0xA91, 0xAD1)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_2[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_2	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX18 (0xA12, 0xA52, 0xA92, 0xAD2)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_2[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_2	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX19 (0xA13, 0xA53, 0xA93, 0xAD3)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_3[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_3	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI\_TX20 (0xA14, 0xA54, 0xA94, 0xAD4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_3[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAP_DST_3	7:0	Mapping Regulator Source - Virtual Channel / Data Type					[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX	

**MIPI\_TX21 (0xA15, 0xA55, 0xA95, 0xAD5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_4[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAP_SRC_4	7:0	Mapping Regulator Source - Virtual Channel / Data Type					[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX	

**MIPI\_TX22 (0xA16, 0xA56, 0xA96, 0xAD6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_4[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAP_DST_4	7:0	Mapping Regulator Source - Virtual Channel / Data Type					[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX	

**MIPI\_TX23 (0xA17, 0xA57, 0xA97, 0xAD7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_5[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>					<b>DECODE</b>	
MAP_SRC_5	7:0	Mapping Regulator Source - Virtual Channel / Data Type					[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX	

MIPI\_TX24 (0xA18, 0xA58, 0xA98, 0xAD8)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_5[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_5	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX25 (0xA19, 0xA59, 0xA99, 0xAD9)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_6[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_6	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX26 (0xA1A, 0xA5A, 0xA9A, 0ADA)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_6[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_6	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX27 (0xA1B, 0xA5B, 0xA9B, 0ADB)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_7[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_7	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX28 (0xA1C, 0xA5C, 0xA9C, 0xADC)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_7[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_7	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX29 (0xA1D, 0xA5D, 0xA9D, 0xADD)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_8[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_8	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX30 (0xA1E, 0xA5E, 0xA9E, 0xADE)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_8[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_8	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX31 (0xA1F, 0xA5F, 0xA9F, 0xAFD)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_9[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_9	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX32 (0xA20, 0xA60, 0xAA0, 0xAE0)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_9[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_9	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX33 (0xA21, 0xA61, 0xAA1, 0xAE1)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_10[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_10	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX34 (0xA22, 0xA62, 0xAA2, 0xAE2)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_10[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_10	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX35 (0xA23, 0xA63, 0xAA3, 0xAE3)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_11[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_11	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI\_TX36 (0xA24, 0xA64, 0xAA4, 0xAE4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_11[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
MAP_DST_11	7:0	Mapping Regulator Source - Virtual Channel / Data Type			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

**MIPI\_TX37 (0xA25, 0xA65, 0xAA5, 0xAE5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_12[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
MAP_SRC_12	7:0	Mapping Regulator Source - Virtual Channel / Data Type			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

**MIPI\_TX38 (0xA26, 0xA66, 0xAA6, 0xAE6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_12[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
MAP_DST_12	7:0	Mapping Regulator Source - Virtual Channel / Data Type			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

**MIPI\_TX39 (0xA27, 0xA67, 0xAA7, 0xAE7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_SRC_13[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
MAP_SRC_13	7:0	Mapping Regulator Source - Virtual Channel / Data Type			[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX			

MIPI\_TX40 (0xA28, 0xA68, 0xAA8, 0xAE8)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_13[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_13	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX41 (0xA29, 0xA69, 0xAA9, 0xAE9)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_14[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_14	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX42 (0xA2A, 0xA6A, 0xAAA, 0xEA)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_DST_14[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_DST_14	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI\_TX43 (0xA2B, 0xA6B, 0xAAB, 0xEAB)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MAP_SRC_15[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
MAP_SRC_15	7:0	Mapping Regulator Source - Virtual Channel / Data Type							[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

**MIPI\_TX44 (0xA2C, 0xA6C, 0xAAC, 0xAEC)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DST_15[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION					DECODE	
MAP_DST_15	7:0	Mapping Regulator Source - Virtual Channel / Data Type					[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX	

**MIPI\_TX45 (0xA2D, 0xA6D, 0xAAD, 0xAED)**

BIT	7	6	5	4	3	2	1	0				
<b>Field</b>	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]					
<b>Reset</b>	0x0		0x0		0x0		0x0					
<b>Access Type</b>	Write, Read		Write, Read		Write, Read		Write, Read					
BITFIELD	BITS	DESCRIPTION					DECODE					
MAP_DPHY_DEST_3	7:6	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers					0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3					
MAP_DPHY_DEST_2	5:4	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers					0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3					
MAP_DPHY_DEST_1	3:2	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers					0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3					
MAP_DPHY_DEST_0	1:0	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers					0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3					

**MIPI\_TX46 (0xA2E, 0xA6E, 0xAAE, 0xAEE)**

BIT	7	6	5	4	3	2	1	0				
<b>Field</b>	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]					
<b>Reset</b>	0x0		0x0		0x0		0x0					
<b>Access Type</b>	Write, Read		Write, Read		Write, Read		Write, Read					
BITFIELD	BITS	DESCRIPTION					DECODE					
MAP_DPHY_DEST_7	7:6	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers					0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3					

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_6	5:4	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_5	3:2	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_4	1:0	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

**MIPI TX47 (0xA2F, 0xA6F, 0xAAF, 0xAF0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
<b>Reset</b>	0x0		0x0		0x0		0x0	
<b>Access Type</b>	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_10	5:4	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_9	3:2	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_8	1:0	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

**MIPI TX48 (0xA30, 0xA70, 0xAB0, 0xAF0)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
<b>Reset</b>	0x0		0x0		0x0		0x0	
<b>Access Type</b>	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_14	5:4	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_13	3:2	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_12	1:0	Destination of CSI2 controller 0, 1, 2, and 3 for 16 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

**MIPI\_TX49 (0xA31, 0xA71, 0xAB1, 0xAF1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
<b>Reset</b>	—	—	—	—	0b0	0b0	0b0	0b0
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MODE_DT	3	Selects 24-bit mode for user-defined data types	0b0: 24-bit mode for user-defined data types not enabled 0b1: 24-bit mode for user-defined data types enabled
ALT_MEM_MAP10	2	Alternative memory read mapping enable for 10-bit DT	0b0: Alternative memory read mapping not enabled for 10-bit DT 0b1: Alternative memory read mapping enabled for 10-bit DT
ALT_MEM_MAP8	1	Alternative memory read mapping enable for 8-bit DT	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
ALT_MEM_MAP12	0	Alternative memory read mapping enable for 12-bit DT	0b0: Alternative memory read mapping not enabled for 12-bit DT 0b1: Alternative memory read mapping enabled for 12-bit DT

**GMSL1\_4 (0xB04, 0xC04, 0xD04, 0xE04)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	PRBSEN	CC_PORT_SEL[1:0]	—	—	—	FWDCCEN
<b>Reset</b>	—	—	0x0	0x0	—	—	—	0x1
<b>Access Type</b>	—	—	Write, Read	Write, Read	—	—	—	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PRBSEN	5	PRBS test enable (in HIBW mode, PRBS_TYPE—0xB0F must be set to zero)	0b0: Set device normal operation 0b1: Enable PRBS test
CC_PORT_SEL	4:3	Selects which I <sup>2</sup> C/UART port is connected to this link	0b00: Port 0 (RX0_SDA0, TX0_SCL0) 0b01: Port 1 (RX1_SDA1, TX1_SCL1) 0b10: Port 2 (RX2_SDA2, TX2_SCL2)
FWDCCEN	0	Enables forward control channel to deserializer	0b0: Disable forward control channel transmitter 0b1: Enable forward control channel transmitter

GMSL1\_5 (0xB05, 0xC05, 0xD05, 0xE05)

BIT	7	6	5	4	3	2	1	0
Field	I2CMETHO D	NO_Rem_MST	HVTR_MO DE	EN_EQ	EQTUNE[3:0]			
Reset	0x0	0x0	0x1	0x1	0x9			
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
I2CMETHOD	7	I <sup>2</sup> C method, skips register address when converting UART-to-I <sup>2</sup> C	0b0: Send the register address during UART-to-I <sup>2</sup> C conversion 0b1: Do not send the register address during UART-to-I <sup>2</sup> C conversion
NO_Rem_MST	6	Set to 1 to indicate that there is no I <sup>2</sup> C master on remote side so this (local) chip should ignore any I <sup>2</sup> C packet initiation (start condition) from remote side	0b0: Master 0b1: No master
HVTR_MODE	5	HV tracking allows continuous HSYNC format	0b0: Use partial periodic HV tracking 0b1: Use partial and full periodic HV tracking
EN_EQ	4	Enables equalizer for manual and adaptive modes	0b0: Disable equalization 0b1: Enable equalization
EQTUNE	3:0	Equalizer boost level at 750 MHz (effective when adaptive EQ is turned off)	0b0000: 1.6dB manual EQ setting 0b0001: 2.1dB manual EQ setting 0b0010: 2.8dB manual EQ setting 0b0011: 3.5dB manual EQ setting 0b0100: 4.3dB manual EQ setting 0b0101: 5.2dB manual EQ setting 0b0110: 6.3dB manual EQ setting 0b0111: 7.3dB manual EQ setting 0b1000: 8.5dB manual EQ setting 0b1001: 9.7dB manual EQ setting 0b1010: 11dB manual EQ setting 0b1011: 12.2dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

PRELIMINARY

**GMSL1\_6 (0xB06, 0xC06, 0xD06, 0xE06)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	HIGHIMM	MAX_RT_E_N	I2C_RT_EN	GPI_COMP_EN	GPI_RT_E_N	HV_SRC[2:0]		
<b>Reset</b>	0x0	0x1	0x1	0x0	0x1	0x7		
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse channel high immunity mode (initial value set by the CFG1 pin state at power-up)	0b0: Reverse channel high immunity mode disabled 0b1: Reverse channel high immunity mode enabled
MAX_RT_EN	6	Maximum retransmission limit enable	0b0: Disable maximum retransmission limit 0b1: Enable maximum retransmission limit
I2C_RT_EN	5	I <sup>2</sup> C retransmission enable	0b0: Disable I <sup>2</sup> C retransmission 0b1: Enable I <sup>2</sup> C retransmission enable
GPI_COMP_EN	4	Reverse channel high immunity mode (initial value set by the CFG1 pin state at power-up)	0b0: Disable GPI skew compensation 0b1: Enable GPI skew compensation
GPI_RT_EN	3	GPI retransmission enable	0b0: Disable GPI retransmission 0b1: Enable GPI retransmission
HV_SRC	2:0	HS_VS bit selection	0b000: Use D18/D19 for HS/VS (use this setting when the serializer is a 3.12Gbps device or if HIBW mode is used; otherwise, this setting is for use with the MAX9273 when DBL = 0 or HVEN = 1) 0b001: Use D14/D15 for HS/VS (for use with the MAX9271/ MAX96705 when DBL = 0 or HVEN = 1) 0b010: Use D12/D13 for HS/VS (for use with the MAX96707 when DBL = 0 or HVEN = 1) 0b011: Use D0/D1 for HS/VS (for use with the MAX9271/ MAX9273/MAX96705/MAX96707 when DBL = 1 and HVEN = 0) 0b100: Reserved 0b101: Reserved 0b110: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96707) 0b111: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96705)

**GMSL1\_7 (0xB07, 0xC07, 0xD07, 0xE07)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DBL	DRS	BWS	—	HIBW	HVEN	—	PXL_CRC
<b>Reset</b>	0x0	0x0	0x0	—	0x0	0x0	—	0x0
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	—	Write, Read	Write, Read	—	Write, Read

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
DBL	7	Double-output mode	0b0: Use single-rate output 0b1: Use double-rate output (2x word rate at 1/2x width)
DRS	6	Data rate select	0b0: Use normal data rate output 0b1: Use 1/2 rate data output (for use with low data rates)
BWS	5	Bus width select	0b0: Set bus width for 22-/24-bit bus, 24-/27-bit mode (depending on HIBW setting) 0b1: Set bus width for 30-bit bus (32-bit mode)
HIBW	3	High-bandwidth mode	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS = 0)
HVEN	2	HS/VS encoding enable	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel error detection type (this is controllable by pin when LCCEN = 0)	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

**GMSL1\_8 (0xB08, 0xC08, 0xD08, 0xE08)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>		GPI_SEL[1:0]	GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
<b>Reset</b>		0x0	0x1	0x0	–	0x0	0x1	
<b>Access Type</b>		Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_SEL	7:6	Selects GPI pin to transmit to serializer	0b00: GPIO_0 0b01: GPIO_1 0b10: GPIO_2 0b11: GPIO_3
GPI_EN	5	Enables GPIO-to-GPO signal transmission to serializer	0b0: Disable GPIO-to-GPO transmission 0b1: Enable GPIO-to-GPO transmission
EN_FSYNC_TX	4	Enables frame sync signal transmission	0b0: Disable frame sync signal transmission 0b1: Enable frame sync signal transmission
PKTCC_EN	2	Packet-based control-channel mode enable	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode
CC_CRC_LENGTH	1:0	Control channel CRC length	0b00: 1-bit CRC 0b01: 5-bit CRC 0b10: 8-bit CRC 0b11: Reserved

**GMSL1\_D (0xB0D, 0xC0D, 0xD0D, 0xE0D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	I2C_LOC_A CK	–	–	–	–	HS_TRACK_FSYNC	–	–
<b>Reset</b>	0x0	–	–	–	–	0x0	–	–
<b>Access Type</b>	Write, Read	–	–	–	–	Write, Read	–	–

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	Enables I <sup>2</sup> C-to-I <sup>2</sup> C slave local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available
HS_TRACK_FSYNC	2	0 = Allow infinite length vertical blanking 1 = Lose HLOCKED with VLOCKED	0x0: Allow infinite length vertical blanking 0x1: Lose HLOCKED with VLOCKED

**GMSL1\_E (0xB0E, 0xC0E, 0xD0E, 0xE0E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DET_THR[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION					DECODE	
DET_THR	7:0	Threshold for detected errors					0XX: Number of errors for detected error threshold	

**GMSL1\_F (0xB0F, 0xC0F, 0xD0F, 0xE0F)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	—	—	PRBS_TYPE
<b>Reset</b>	—	0x0	0x0	0x0	0x1	—	—	0x1
<b>Access Type</b>	—	Write, Read	Write, Read	Write, Read	Write, Read	—	—	Write, Read
BITFIELD	BITS	DESCRIPTION					DECODE	
EN_DE_FILT	6	Enables glitch filtering on DE					0b0: Disable DE glitch filtering 0b1: Enable DE glitch filtering	
EN_HS_FILT	5	Enables glitch filtering on HS					0b0: Disable HS glitch filtering 0b1: Enable HS glitch filtering	
EN_VS_FILT	4	Enables glitch filtering on VS					0b0: Disable VS glitch filtering 0b1: Enable VS glitch filtering	
DE_EN	3	Enables processing separate HS and DE signals					0b0: Disable processing HS and DE signals 0b1: Enable processing HS and DE signals	
PRBS_TYPE	0	PRBS type select (in HIBW mode, set PRBS_TYPE = 0)					0b0: GMSL legacy style PRBS test 0b1: MAX9272 style PRBS test	

**GMSL1\_10 (0xB10, 0xC10, 0xD10, 0xE10)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				
<b>Reset</b>	0x0		0x0	0x1				
<b>Access Type</b>	Write, Read		Write, Read	Write, Read				

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_TYPE	7:6	Reverse channel generated error type	0b00: Random 0b01: Short burst 0b10: Long burst 0b11: Long burst
RCEG_BOUND	5	Reverse channel generated error boundary (effective when RCEG_TYPE = 0x)	0b0: Errors are unbounded to symbols 0b1: Errors are bounded to symbols
RCEG_ERR_NUM	4:1	Number of RCEG errors generated with each request (effective when RCEG_TYPE = 0x)	0XX: Number of errors generated per request
RCEG_EN	0	Enable reverse channel error generator	0b0: Disable reverse channel error generator 0b1: Enable reverse channel error generator enabled

**GMSL1\_11 (0xB11, 0xC11, 0xD11, 0xE11)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RCEG_ERR_RATE[3:0]					RCEG_LO_BST_PRB[1:0]	RCEG_LO_BST_LEN[1:0]	
<b>Reset</b>	0xF					0x0	0x0	
<b>Access Type</b>	Write, Read					Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_RATE	7:4	Error generation rate in terms of bit time = $2^{-(RCEG\_ERR\_RATE + 3)}$ . Effective when RCEG_TYPE = 0X.	0x0: Rate is $2^{-3}$ 0x1: Rate is $2^{-4}$ 0x2: Rate is $2^{-5}$ . . . 0xF: Rate is $2^{-18}$
RCEG_LO_BST_PRB	3:2	Long burst error probability. Effective when RCEG_TYPE = 10.	0b00: 1/1024 0b01: 1/128 0b10: 1/32 0b11: 1/8
RCEG_LO_BST_LEN	1:0	Long burst error length in terms of bit time. Effective when RCEG_TYPE = 10.	0b00: Continuous 0b01: 128 (~150μs) 0b10: 8192 (~9.83ms) 0b11: 1048576 (~1.26s)

**GMSL1\_12 (0xB12, 0xC12, 0xD12, 0xE12)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	-	MAX_RT_ERR_EN	RCEG_ER_R_PER_EN		
<b>Reset</b>	0x0	0x1	0x1		0x0	-	0x1	0x0		
<b>Access Type</b>	Write, Read	Write, Read	Write, Read		Write, Read	-	Write, Read	Write, Read		
BITFIELD	BITS	DESCRIPTION				DECODE				
UNDERBST_DET_EN	7	Allows underboost detection driving ERRORB pin				0b0: Disable underboost detection driving ERRORB pin 0b1: Enable underboost detection driving ERRORB pin				

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_E RR_EN	6	Enables reporting of (CC_CRC_ERR_CNT > 0) on the ERRORB pin	0b0: Disable reporting of errors on ERRORB 0b1: Enable reporting of errors on ERRORB
LINE_CRC_L OC	5:4	Video line CRC insertion location	0b00: [1..4] 0b01: [5..8] 0b10: [9..12] 0b11: [13..16]
LINE_CRC_ EN_GMSL1	3	Video line CRC enable	0b0: Disable video line CRC 0b1: Enable video line CRC
MAX_RT_ER R_EN	1	Enables reflection of maximum retransmission error on the ERRORB pin	0b0: Disable maximum retransmission error on the ERROR pin 0b1: Enable maximum retransmission error on the ERROR pin
RCEG_ERR _PER_EN	0	Periodic error generation enable. Effective when RCEG_TYPE (0xB10) = 0x.	0b0: Disable periodic error generator 0b1: Enable periodic error generator

**GMSL1\_13 (0xB13, 0xC13, 0xD13, 0xE13)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
<b>Reset</b>	0x1	0x1	0x0	0x00				
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read				
BITFIELD	BITS	DESCRIPTION			DECODE			
EOM_EN_G1	7	Eye-opening monitor enable			0b0: Disable EOM 0b1: Enable EOM			
EOM_PER_MODE_G1	6	Eye-opening monitor periodic mode select			0b0: Set EOM to use nonperiodic mode 0b1: Set EOM to use periodic mode			
EOM_MAN_TRG_REQ_G1	5	Eye-opening monitor (EOM) manual trigger request. Valid on the rising edge of this bit when not in periodic mode.			0b0: Do not trigger EOM 0b1: Manually trigger the EOM			
EOM_MIN_THR_G1	4:0	Eye-opening minimum threshold (in terms of percent) for flagging ERRORB pin			0b00000: Disabled 0b00001: 3.125% 0b00010: 6.25% . . . 0b11111: 100%			

**GMSL1\_14 (0xB14, 0xC14, 0xD14, 0xE14)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
<b>Reset</b>	0x1	0x0	0x0	0x00				
<b>Access Type</b>	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_EN	7	Adaptive equalization enable	0b0: Disable AEQ 0b1: Enable AEQ
AEQ_PER_MODE	6	Adaptive equalizer periodic mode select	0b0: Set AEQ to use nonperiodic mode 0b1: Set AEQ to use periodic mode
AEQ_MAN_TRG_REQ	5	Adaptive equalizer manual fine-tune request enable. Valid on the rising edge of this bit when not in periodic mode.	0b0: Do not trigger AEQ fine tuning 0b1: Manually trigger the AEQ fine tuning
EOM_PERTHR	4:0	Eye-opening threshold to trigger a fine-tune operation	0b0000: Eye-opening threshold is disabled 0b10000: 50% eye-opening triggers fine-tune operation All other values: Reserved

**GMSL1\_15 (0xB15, 0xC15, 0xD15, 0xE15)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DET_ERR[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION				DECODE		
DET_ERR	7:0	Detected error counter				0xXX: Number of detected errors		

**GMSL1\_16 (0xB16, 0xC16, 0xD16, 0xE16)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PRBS_ERR[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION				DECODE		
PRBS_ERR	7:0	PRBS error counter				0xXX: Number of detected PRBS errors		

**GMSL1\_17 (0xB17, 0xC17, 0xD17, 0xE17)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	-	MAX_RT_E_RR_I2C	PRBS_OK	GPI_IN	MAX_RT_E_RR_GPI	-	-	-
<b>Reset</b>	-	0x0	0x0	0x0	0x0	-	-	-
<b>Access Type</b>	-	Read Only	Read Only	Read Only	Read Only	-	-	-
BITFIELD	BITS	DESCRIPTION				DECODE		
MAX_RT_ER_R_I2C	6	Maximum retransmission error flag. Cleared when read.				0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached		
PRBS_OK	5	MAX9271/73 compatible PRBS test for link is completed normally. Check PRBS_ERR register for the PRBS success. For other SERDES read PRBS_ERR registers.				0b0: No MAX9271/MAX9273 compatible PRBS test completed 0b1: MAX9271/MAX9273 compatible PRBS test completed normally		

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_IN	4	GPI pin level	0b0: GPI is input low 0b1: GPI is input high
MAX_RT_ER R_GPI	3	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

**GMSL1\_18 (0xB18, 0xC18, 0xD18, 0xE18)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CC_RETR_CNT[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION						DECODE
CC_RETR_CNT	7:0	I <sup>2</sup> C packet retransmit count						0xXX: Number of I <sup>2</sup> C packets retransmitted

**GMSL1\_19 (0xB19, 0xC19, 0xD19, 0xE19)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CC_CRC_ERRCNT[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION						DECODE
CC_CRC_E RRCNT	7:0	Packet-based control-channel CRC error counter						0xXX: Number of control-channel CRC errors

**GMSL1\_1A (0xB1A, 0xC1A, 0xD1A, 0xE1A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RCEG_ERR_CNT[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION						DECODE
RCEG_ERR_CNT	7:0	Control-channel number of generated errors						0xXX: Number of control-channel generated errors

**GMSL1\_1B (0xB1B, 0xC1B, 0xD1B, 0xE1B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	LINE_CRC_ERR	—	—
<b>Reset</b>	—	—	—	—	—	0x0	—	—
<b>Access Type</b>	—	—	—	—	—	Read Only	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_ERR	2	CRC error bit. Latched on error, cleared to 0 when read.	0b0: Video line CRC ok 0b1: Video line CRC mismatch detected

**GMSL1\_1C (0xB1C, 0xC1C, 0xD1C, 0xE1C)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	—	—	EOM_EYE_WIDTH[5:0]							
<b>Reset</b>	—	—	0x00							
<b>Access Type</b>	—	—	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EYE_WIDTH	5:0	Measured eye opening. Opening width = EOM_EYE_WIDTH/63 x 100%	0b000000: Width is 0% 0b000001: Width is 1/63 x 100% 0b000010: Width is 2/63 x 100% . . . 0b11111: Width is 63/63 x 100%

**GMSL1\_1D (0xB1D, 0xC1D, 0xD1D, 0xE1D)**

BIT	7	6	5	4	3	2	1	0				
<b>Field</b>	—	—	—	UNDERBOOST_DET	AEQ_BST[3:0]							
<b>Reset</b>	—	—	—	0x0	0x0							
<b>Access Type</b>	—	—	—	Read Only	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBOOST_DET	4	Underboost detected	0b0: Normal operation 0b1: Underboost (at maximum AEQ gain) detected
AEQ_BST	3:0	Adaptive equalizer boost value. Selected adaptive equalizer value; settings correspond to gain at 750MHz	0b0000: 1.6dB manual EQ setting 0b0001: 2.1dB manual EQ setting 0b0010: 2.8dB manual EQ setting 0b0011: 3.5dB manual EQ setting 0b0100: 4.3dB manual EQ setting 0b0101: 5.2dB manual EQ setting 0b0110: 6.3dB manual EQ setting 0b0111: 7.3dB manual EQ setting 0b1000: 8.5dB manual EQ setting 0b1001: 9.7dB manual EQ setting 0b1010: 11dB manual EQ setting 0b1011: 12.2dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

**GMSL1\_20 (0xB20, 0xC20, 0xD20, 0xE20)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CRC_VALUE_0[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Only								
BITFIELD	BITS	DESCRIPTION							DECODE
CRC_VALUE_0	7:0	Bits [7:0] of CRC output for the latest line							0xXX: CRC[7:0] of latest line

**GMSL1\_21 (0xB21, 0xC21, 0xD21, 0xE21)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CRC_VALUE_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Only								
BITFIELD	BITS	DESCRIPTION							DECODE
CRC_VALUE_1	7:0	Bits [15:8] of CRC output for the latest line							0xXX: CRC[15:8] of latest line

**GMSL1\_22 (0xB22, 0xC22, 0xD22, 0xE22)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CRC_VALUE_2[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Only								
BITFIELD	BITS	DESCRIPTION							DECODE
CRC_VALUE_2	7:0	Bits [23:16] of CRC output for the latest line							0xXX: CRC[23:16] of latest line

**GMSL1\_23 (0xB23, 0xC23, 0xD23, 0xE23)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CRC_VALUE_3[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Only								
BITFIELD	BITS	DESCRIPTION							DECODE
CRC_VALUE_3	7:0	Bits [31:24] of CRC output for the latest line							0xXX: CRC[31:24] of latest line

**PRELIMINARY****GMSL1\_96 (0xB96, 0xC96, 0xD96, 0xE96)**

BIT	7	6	5	4	3	2	1	0	
Field	CONV_GMSL1_DATATYPE[4:0]						-	-	
Reset	0x00						-	-	
Access Type	Write, Read						-	-	
BITFIELD	BITS	DESCRIPTION				DECODE			
CONV_GMSL1_DATATYPE	7:3	Converts from GMSL1 color format mapping to GMSL2 CSI transmitter color format				0x0: RGB888 OLDI 0x1: RGB565 0x2: RGB666 0x3: YUV422 8-bit mux mode (use yuv_8_10_mux_mode) 0x4: YUV422 10-bit mux mode (use yuv_8_10_mux_mode) 0x5: RAW8 single 0x6: RAW10 single 0x7: RAW12 single 0x8: RAW14 0x9: User-defined generic 24-bit 0xA: User-defined YUV422 12-bit 0xB: User-defined generic 8-bit 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved 0x10: RGB888 VESA 0x11: Reserved 0x12: Reserved 0x13: YUV422 8-bit normal mode 0x14: YUV422 10-bit normal mode 0x15: RAW8 double (use alt_mem_map8) 0x16: RAW10 double (use alt_mem_map10) 0x17: RAW12 double (use alt_mem_map12) 0x18: Reserved 0x19: Reserved 0x1A: Reserved 0x1B: Reserved 0x1C: Reserved 0x1D: Reserved 0x1E: Reserved 0x1F: Reserved			

**GMSL1\_CB (0xBCB, 0xCCB, 0xDCB, 0xECB)**

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	LOCKED_G1
Reset	-	-	-	-	-	-	-	0x0
Access Type	-	-	-	-	-	-	-	Read Only
BITFIELD	BITS	DESCRIPTION				DECODE		
LOCKED_G1	0	Link Locked				0b0: Link not locked 0b1: Link locked		

**TX1 (0x1001)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	ERRG_EN	—	—	—	—
<b>Reset</b>	—	—	—	0b0	—	—	—	—
<b>Access Type</b>	—	—	—	Write, Read	—	—	—	—
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>
ERRG_EN	4	Error generator enable						0b0: Disable error generator for Link A 0b1: Enable error generator for Link A

**TX2 (0x1002)**

BIT	7	6	5	4	3	2	1	0					
<b>Field</b>	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER					
<b>Reset</b>	0x0		0x2		0x0			0b0					
<b>Access Type</b>	Write, Read		Write, Read		Write, Read			Write, Read					
BITFIELD	BITS	<b>DESCRIPTION</b>						<b>DECODE</b>					
ERRG_CNT	7:6	Number of errors to be generated						0b00: Continuous 0b01: 16 0b10: 128 0b11: 1024					
ERRG_RATE	5:4	Error generator average bit error rate						0b00: 1/5120 bits 0b01: 1/81920 bits 0b10: 1/1310720 bits 0b11: 1/20971520 bits					
ERRG_BURST	3:1	Error generator burst error length						0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20					
ERRG_PER	0	Error generator error distribution selection						0b0: Pseudorandom 0b1: Periodic					

**TX3 (0x1003)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	TIMEOUT[2:0]		
<b>Reset</b>	—	—	—	—	—	0x4		
<b>Access Type</b>	—	—	—	—	—	Write, Read		

**PRELIMINARY**

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	Link ARQ Timeout Duration Multiplier  Multiplies a timeout base constant to set the ARQ timeout.  Timeout Base = 8µs	0b000: 0.5 x Timeout Base 0b001: 1.0 x Timeout Base 0b010: 1.5 x Timeout Base 0b011: 2.0 x Timeout Base 0b100: 2.5 x Timeout Base 0b101: 3.0 x Timeout Base 0b110: 3.5 x Timeout Base 0b111: 4.0 x Timeout Base

**RX0 (0x1004)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PKT_CNT_LBW[1:0]					PKT_CNT_SEL[3:0]		
<b>Reset</b>	0x0					0x0		
<b>Access Type</b>	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Select the sub-type of low-bandwidth packets to count at PKT_CNT register	0b00: Count data packets 0b01: Count acknowledge packets 0b10: Count data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Select the type of received packets to count at PKT_CNT(0x40 – 0x43)	0b0000: None 0b0001: Video 0b0010: Reserved 0b0011: INFOFR 0b0100: SPI 0b0101: I <sup>2</sup> C 0b0110: UART 0b0111: GPIO 0b1000: Reserved 0b1001: Reserved 0b1010: Reserved 0b1011: Reserved 0b1100: Reserved 0b1101: Reserved 0b1110: All non-idle packets 0b1111: Unknown/Error

**GPIOA (0x1008)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	–	–	GPIO_FWD_CDLY[5:0]					
<b>Reset</b>	–	–	0x01					
<b>Access Type</b>	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	<p>Compensation delay multiplier for the forward direction.</p> <p>This must be same value as GPIO_FWD_CDLY of the chip on the other side of the link.</p> <p>Total delay is the (value + 1) multiplied by 1.7μs. Default delay is 3.4μs.</p>	0bXXXXXX: Forward compensation delay multiplier value

**GPIOB (0x1009)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]						
<b>Reset</b>	0x2		0x08						
<b>Access Type</b>	Write, Read		Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	<p>Wait time after a GPIO transition to create a packet. This allows grouping transitions of different GPIO inputs in a single packet and so increases GPIO bandwidth usage efficiency.</p>	<p>0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns</p>
GPIO_REV_CDLY	5:0	<p>Compensation delay multiplier for the reverse direction.</p> <p>This must be same value as GPIO_REV_CDLY of the chip on the other side of the link.</p> <p>Total delay is the (value + 1) multiplied by 1.7μs. Default delay is 15.3μs.</p> <p>Note: In delay compensation mode, a fixed delay is guaranteed once the link is locked. But each link reset could change the delay between two values which are 1.7us apart.</p>	0bXXXXXX: Reverse compensation delay multiplier value

**TX1 (0x1011, 0x1021, 0x1031)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	ERRG_EN	—	—	—	—
<b>Reset</b>	—	—	—	0b0	—	—	—	—
<b>Access Type</b>	—	—	—	Write, Read	—	—	—	—
BITFIELD	BITS	DESCRIPTION					DECODE	
ERRG_EN	4	Error generator enable					0b0: Disable error generator 0b1: Enable error generator	

**TX2 (0x1012, 0x1022, 0x1032)**

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]					
<b>Reset</b>	0x0		0x2		0x0					
<b>Access Type</b>	Write, Read		Write, Read		Write, Read					
BITFIELD	BITS	DESCRIPTION				DECODE				
ERRG_CNT	7:6	Number of errors to be generated				0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors				
ERRG_RATE	5:4	Error generator average bit error rate				0b00: 1/5120 bits 0b01: 1/81920 bits 0b10: 1/1310720 bits 0b11: 1/20971520 bits				
ERRG_BURST	3:1	Error generator burst error length				0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20				
ERRG_PER	0	Error generator error distribution selection				0b0: Pseudorandom 0b1: Periodic				

**TX3 (0x1013, 0x1023, 0x1033)**

BIT	7	6	5	4	3	2	1	0				
<b>Field</b>	-		-		-		TIMEOUT[2:0]					
<b>Reset</b>	-		-		-		0x4					
<b>Access Type</b>	-		-		-		Write, Read					
BITFIELD	BITS	DESCRIPTION				DECODE						
TIMEOUT	2:0	Link ARQ Timeout Duration Multiplier  Multiplies a timeout base constant to set the ARQ timeout.  Timeout Base = 8μs				0b000: 0.5 x Timeout Base 0b001: 1.0 x Timeout Base 0b010: 1.5 x Timeout Base 0b011: 2.0 x Timeout Base 0b100: 2.5 x Timeout Base 0b101: 3.0 x Timeout Base 0b110: 3.5 x Timeout Base 0b111: 4.0 x Timeout Base						

**RX0 (0x1014, 0x1024, 0x1034)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	PKT_CNT_LBW[1:0]		-		PKT_CNT_SEL[3:0]			
<b>Reset</b>	0x0		-		0x0			
<b>Access Type</b>	Write, Read		-		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_L_BW	7:6	Selects the sub-type of low-bandwidth packets to count at PKT_CNT_x bitfield (0x40—0x43).	0b00: Count data packets 0b01: Count acknowledge packets 0b10: Count data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Selects the type of received packets to count at PKT_CNT_x bitfield (0x40—0x43)	0x0: None 0x1: Video 0x2: Reserved 0x3: INFOFR 0x4: SPI 0x5: I2C 0x6: UART 0x7: GPIO 0x8: Reserved 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All non-idle packets 0xF: Unknown/Error

**GPIOA (0x1018, 0x1028, 0x1038)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	GPIO_FWD_CDLY[5:0]					
<b>Reset</b>	—	—	0x01					
<b>Access Type</b>	—	—	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction.  This must be same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.  Note: In delay compensation mode, a fixed delay is guaranteed once the link is locked. But each link reset could change the delay between two values which are 1.7us apart.	0bXXXXXXXX: Forward compensation delay multiplier value

**GPIOB (0x1019, 0x1029, 0x1039)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
<b>Reset</b>	0x2		0x08					
<b>Access Type</b>	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_W_NDW	7:6	Wait time after a GPIO transition to create a packet. This allows grouping transitions of different GPIO inputs in a single packet and so increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200 ns 0b10: 500 ns 0b11: 1000 ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction.  This must be same value as GPIO_REV_CDLY of the chip on the other side of the link.  Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

PATGEN\_0 (0x1050, 0x1080)

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x3	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	
BITFIELD	BITS	DESCRIPTION				DECODE		
GEN_VS	7	Enable to generate VS output according to the timing definition				0b0: Do not generate VS 0b1: Generate VS		
GEN_HS	6	Enable to generate HS output according to the timing definition				0b0: Do not generate HS 0b1: Generate HS		
GEN_DE	5	Enable to generate DE output according to the timing definition				0b0: Do not generate DE 0b1: Generate DE		
VS_INV	4	Inverts VSYNC output of video timing generator				0b0: Do not invert VS 0b1: Invert VS		
HS_INV	3	Inverts HSYNC output of video timing generator				0b0: Do not invert HS 0b1: Invert HS		
DE_INV	2	Inverts DE output of video timing generator				0b0: Do not invert DE 0b1: Invert DE		

BITFIELD	BITS	DESCRIPTION	DECODE
VTG_MODE	1:0	<p>Video interface timing generation mode.</p> <p>00 or 11 = VS tracking mode. VS input's period (VS_HIGH + VS_LOW) is tracked. After VS tracking is locked, any VS input edge (glitches) not in the expected PCLK cycle is ignored. VS tracking is locked with three consecutive matches and unlocked by three consecutive mismatches. When unlocked or power-up, the next VS input edge is assumed to be the right VS edge.</p> <p>01 = VS one-trigger mode One VS input edge will trigger the generation of ONE frame of VSO/HSO/DEO. If next VS input edge comes earlier or later than expected by VS period, the newly generated frame will be correct. The current VSO/HSO/DEO will be cut or extended at the time point of rising edge of the newly generated VSO/HSO/DEO.</p> <p>10 = Auto-repeat mode (default) VS input edge will trigger the generation of continuous frames of VSO/HSO/DEO even if no more VS input edges. If next VS input edge comes earlier or later than expected by VS period, the newly generated frame will be correct. The current VSO/HSO/DEO will be cut or extended at the time point of rising edge of the newly generated VSO/HSO/DEO.</p>	<p>0b00: VS tracking mode 0b01: VS on trigger mode 0b10: Auto-repeat mode 0b11: Free-running mode</p>

PATGEN\_1 (0x1051, 0x1081)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	GRAD_MODE	—	PATGEN_MODE[1:0]		—	—	—	VS_TRIGGER
<b>Reset</b>	0x0	—	0x0		—	—	—	0x0
<b>Access Type</b>	Write, Read	—	Write, Read		—	—	—	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_MODE	7	Gradient pattern generator mode	<p>0b0: Gradient mode increasing. Each gradient color starts from a value of 0x00 and increases to 0xFF</p> <p>0b1: Gradient mode decreasing. Each gradient color starts from a value of 0xFF and decreases to 0x00</p>
PATGEN_MODE	5:4	Pattern generator mode	<p>0b00: Pattern generator disabled - use video from the serializer input (default)</p> <p>0b01: Generate checkerboard pattern</p> <p>0b10: Generate gradient pattern</p> <p>0b11: Reserved</p>
VS_TRIGGER	0	Select VS trigger edge	<p>0b0: Falling edge</p> <p>0b1: Rising edge</p>

**VS\_DLY\_2 (0x1052, 0x1082)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VS_DLY_2[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
VS_DLY_2	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [23:16])			0xXX: Most significant byte of VS delay			

**VS\_DLY\_1 (0x1053, 0x1083)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VS_DLY_1[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
VS_DLY_1	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [15:8])			0xXX: Middle significant byte of VS delay			

**VS\_DLY\_0 (0x1054, 0x1084)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VS_DLY_0[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
VS_DLY_0	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [7:0])			0xXX: Least significant byte of VS delay			

**VS\_HIGH\_2 (0x1055, 0x1085)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VS_HIGH_2[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
VS_HIGH_2	7:0	VS high period in terms of PCLK cycles (bits [23:16])			0xXX: Most significant byte of VS high period			

[VS\\_HIGH\\_1 \(0x1056, 0x1086\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VS_HIGH_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
VS_HIGH_1	7:0	VS high period in terms of PCLK cycles (bits [15:8])							0xXX: Middle significant byte of VS high period

[VS\\_HIGH\\_0 \(0x1057, 0x1087\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VS_HIGH_0[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
VS_HIGH_0	7:0	VS high period in terms of PCLK cycles (bits [7:0])							0xXX: Least significant byte of VS high period

[VS\\_LOW\\_2 \(0x1058, 0x1088\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VS_LOW_2[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
VS_LOW_2	7:0	VS low period in terms of PCLK cycles (bits [23:16])							0xXX: Most significant byte of VS low period

[VS\\_LOW\\_1 \(0x1059, 0x1089\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VS_LOW_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
VS_LOW_1	7:0	VS low period in terms of PCLK cycles (bits [15:8])							0xXX: Middle significant byte of VS low period

**VS\_LOW\_0 (0x105A, 0x108A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VS_LOW_0[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>				<b>DECODE</b>		
VS_LOW_0	7:0	VS low period in terms of PCLK cycles (bits [7:0])				0xXX: Least significant byte of VS low period		

**V2H\_2 (0x105B, 0x108B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	V2H_2[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>				<b>DECODE</b>		
V2H_2	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [23:16])				0xXX: Most significant byte of VS edge to first HS rising edge		

**V2H\_1 (0x105C, 0x108C)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	V2H_1[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>				<b>DECODE</b>		
V2H_1	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [15:8])				0xXX: Middle significant byte of VS edge to first HS rising edge		

**V2H\_0 (0x105D, 0x108D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	V2H_0[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>				<b>DECODE</b>		
V2H_0	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [7:0])				0xXX: Least significant byte of VS edge to first HS rising edge		

[HS\\_HIGH\\_1 \(0x105E, 0x108E\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	HS_HIGH_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
HS_HIGH_1	7:0	HS high period in terms of PCLK cycles (bits [15:8])							0xXX: Most significant byte of HS high period

[HS\\_HIGH\\_0 \(0x105F, 0x108F\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	HS_HIGH_0[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
HS_HIGH_0	7:0	HS high period in terms of PCLK cycles (bits [7:0])							0xXX: Least significant byte of HS high period

[HS\\_LOW\\_1 \(0x1060, 0x1090\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	HS_LOW_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
HS_LOW_1	7:0	HS low period in terms of PCLK cycles (bits [15:8])							0xXX: Most significant byte of HS low period

[HS\\_LOW\\_0 \(0x1061, 0x1091\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	HS_LOW_0[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
HS_LOW_0	7:0	HS low period in terms of PCLK cycles (bits [7:0])							0xXX: Least significant byte of HS low period

[HS\\_CNT\\_1 \(0x1062, 0x1092\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	HS_CNT_1[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
HS_CNT_1	7:0	HS pulses per frame (bits [15:8])			0xXX: Most significant byte of HS pulses per frame			

[HS\\_CNT\\_0 \(0x1063, 0x1093\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	HS_CNT_0[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
HS_CNT_0	7:0	HS pulses per frame (bits [7:0])			0xXX: Least significant byte of HS pulses per frame			

[V2D\\_2 \(0x1064, 0x1094\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	V2D_2[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
V2D_2	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])			0xXX: Most significant byte of VS edge to first DE			

[V2D\\_1 \(0x1065, 0x1095\)](#)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	V2D_1[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
V2D_1	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [15:8])			0xXX: Middle significant byte of VS edge to first DE			

V2D\_0 (0x1066, 0x1096)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	V2D_0[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
V2D_0	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])							0xXX: Least significant byte of VS edge to first DE

DE\_HIGH\_1 (0x1067, 0x1097)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	DE_HIGH_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
DE_HIGH_1	7:0	DE high period in terms of PCLK cycles (bits [15:8])							0xXX: Most significant byte of DE high period

DE\_HIGH\_0 (0x1068, 0x1098)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	DE_HIGH_0[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
DE_HIGH_0	7:0	DE high period in terms of PCLK cycles (bits [7:0])							0xXX: Least significant byte of DE high period

DE\_LOW\_1 (0x1069, 0x1099)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	DE_LOW_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
DE_LOW_1	7:0	DE low period in terms of PCLK cycles (bits [15:8])							0xXX: Most significant byte of DE low period

[DE\\_LOW\\_0 \(0x106A, 0x109A\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	DE_LOW_0[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
DE_LOW_0	7:0	DE low period in terms of PCLK cycles (bits [7:0])							0xXX: Least significant byte of DE low period

[DE\\_CNT\\_1 \(0x106B, 0x109B\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	DE_CNT_1[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
DE_CNT_1	7:0	Active lines per frame (bits [15:8])							0xXX: Most significant byte of DE pulses per frame

[DE\\_CNT\\_0 \(0x106C, 0x109C\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	DE_CNT_0[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
DE_CNT_0	7:0	Active lines per frame (bits [7:0])							0xXX: Least significant byte of DE pulses per frame

[GRAD\\_INCR \(0x106D, 0x109D\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	GRAD_INCR[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
GRAD_INCR	7:0	Gradient mode increment amount (increment amount is the register value divided by 4)							0xXX: Gradient increment base

[CHKR\\_COLOR\\_A\\_L \(0x106E, 0x109E\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CHKR_COLOR_A_L[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
CHKR_COL_OR_A_L	7:0	Checkerboard mode color A low byte							0xXX: Least significant byte of checkerboard mode color A

[CHKR\\_COLOR\\_A\\_M \(0x106F, 0x109F\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CHKR_COLOR_A_M[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
CHKR_COL_OR_A_M	7:0	Checkerboard mode color A middle byte							0xXX: Middle significant byte of checkerboard mode color A

[CHKR\\_COLOR\\_A\\_H \(0x1070, 0x10A0\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CHKR_COLOR_A_H[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
CHKR_COL_OR_A_H	7:0	Checkerboard mode color A high byte							0xXX: Most significant byte of checkerboard mode color A

[CHKR\\_COLOR\\_B\\_L \(0x1071, 0x10A1\)](#)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CHKR_COLOR_B_L[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
CHKR_COL_OR_B_L	7:0	Checkerboard mode color B low byte							0xXX: Least significant byte of checkerboard mode color B

**CHKR\_COLOR\_B\_M (0x1072, 0x10A2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CHKR_COLOR_B_M[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_COL_OR_B_M	7:0	Checkerboard mode color B middle byte			0xXX: Middle significant byte of checkerboard mode color B			

**CHKR\_COLOR\_B\_H (0x1073, 0x10A3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CHKR_COLOR_B_H[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_COL_OR_B_H	7:0	Checkerboard mode color B high byte			0xXX: Most significant byte of checkerboard mode color B			

**CHKR\_RPT\_A (0x1074, 0x10A4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CHKR_RPT_A[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_RPT_A	7:0	Checkerboard mode color A repeat count			0xXX: Repeat count of checkerboard mode color A			

**CHKR\_RPT\_B (0x1075, 0x10A5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	CHKR_RPT_B[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
CHKR_RPT_B	7:0	Checkerboard mode color B repeat count			0xXX: Repeat count of checkerboard mode color B			

**CHKR\_ALT (0x1076, 0x10A6)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	CHKR_ALT[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Write, Read								
BITFIELD	BITS	DESCRIPTION							DECODE
CHKR_ALT	7:0	Checkerboard mode alternate line count							0xXX: Checkerboard mode alternate line count

**CNT\_AX (0x11D0)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_AX[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_AX	7:0	Total number of video pixel CRC errors detected at video stream AX. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream AX

**CNT\_AY (0x11D1)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_AY[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_AY	7:0	Total number of video pixel CRC errors detected at video stream AY. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream AY

**CNT\_AZ (0x11D2)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_AZ[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_AZ	7:0	Total number of video pixel CRC errors detected at video stream AZ. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream AZ

CNT\_AU (0x11E0)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_AU[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_AU	7:0	Total number of video pixel CRC errors detected at video stream AU. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream AU

CNT\_BX (0x11E1)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_BX[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_BX	7:0	Total number of video pixel CRC errors detected at video stream BX. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream BX

CNT\_BY (0x11E2)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_BY[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_BY	7:0	Total number of video pixel CRC errors detected at video stream BY. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream BY

CNT\_BZ (0x11E3)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_BZ[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_BZ	7:0	Total number of video pixel CRC errors detected at video stream BZ. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream BZ

CNT\_BU (0x11E4)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_BU[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_BU	7:0	Total number of video pixel CRC errors detected at video stream BU. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream BU

CNT\_CX (0x11E5)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_CX[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_CX	7:0	Total number of video pixel CRC errors detected at video stream CX. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream CX

CNT\_CY (0x11E6)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_CY[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_CY	7:0	Total number of video pixel CRC errors detected at video stream CY. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream CY

CNT\_CZ (0x11E7)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR_CZ[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_CZ	7:0	Total number of video pixel CRC errors detected at video stream CZ. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream CZ

CNT CU (0x11E8)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR CU[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_C U	7:0	Total number of video pixel CRC errors detected at video stream CU. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream CU

CNT DX (0x11E9)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR DX[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_DX	7:0	Total number of video pixel CRC errors detected at video stream DX. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream DX

CNT DY (0x11EA)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR DY[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_DY	7:0	Total number of video pixel CRC errors detected at video stream DY. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream DY

CNT DZ (0x11EB)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	VID_PXL_CRC_ERR DZ[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Clears All								
BITFIELD	BITS	DESCRIPTION							DECODE
VID_PXL_C RC_ERR_DZ	7:0	Total number of video pixel CRC errors detected at video stream DZ. Reset after reading or with the rising edge of LOCK.							0xXX: Total number of video pixel CRC errors detected at video stream DZ

CNT\_DU (0x11EC)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>								VID_PXL_CRC_ERR_DU[7:0]
<b>Reset</b>								0x00
<b>Access Type</b>								Read Clears All
BITFIELD	BITS	DESCRIPTION						
VID_PXL_CRC_ERR_DU	7:0	Total number of video pixel CRC errors detected at video stream DU. Reset after reading or with the rising edge of LOCK.						0xXX: Total number of video pixel CRC errors detected at video stream DU

DE\_DET (0x11F0)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	DE_DET_7	DE_DET_6	DE_DET_5	DE_DET_4	DE_DET_3	DE_DET_2	DE_DET_1	DE_DET_0
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
BITFIELD	BITS	DESCRIPTION					DECODE	
DE_DET_7	7	DE activity is detected in Video Pipe 7					0b0: DE is not detected 0b1: DE is detected	
DE_DET_6	6	DE activity is detected in Video Pipe 6					0b0: DE is not detected 0b1: DE is detected	
DE_DET_5	5	DE activity is detected in Video Pipe 5					0b0: DE is not detected 0b1: DE is detected	
DE_DET_4	4	DE activity is detected in Video Pipe 4					0b0: DE is not detected 0b1: DE is detected	
DE_DET_3	3	DE activity is detected in Video Pipe 3					0b0: DE is not detected 0b1: DE is detected	
DE_DET_2	2	DE activity is detected in Video Pipe 2					0b0: DE is not detected 0b1: DE is detected	
DE_DET_1	1	DE activity is detected in Video Pipe 1					0b0: DE is not detected 0b1: DE is detected	
DE_DET_0	0	DE activity is detected in Video Pipe 0					0b0: DE is not detected 0b1: DE is detected	

HS\_DET (0x11F1)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	HS_DET_7	HS_DET_6	HS_DET_5	HS_DET_4	HS_DET_3	HS_DET_2	HS_DET_1	HS_DET_0
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
BITFIELD	BITS	DESCRIPTION					DECODE	
HS_DET_7	7	HS activity is detected in Video Pipe 7					0b0: HS is not detected 0b1: HS is detected	
HS_DET_6	6	HS activity is detected in Video Pipe 6					0b0: HS is not detected 0b1: HS is detected	

BITFIELD	BITS	DESCRIPTION	DECODE
HS_DET_5	5	HS activity is detected in Video Pipe 5	0b0: HS is not detected 0b1: HS is detected
HS_DET_4	4	HS activity is detected in Video Pipe 4	0b0: HS is not detected 0b1: HS is detected
HS_DET_3	3	HS activity is detected in Video Pipe 3	0b0: HS is not detected 0b1: HS is detected
HS_DET_2	2	HS activity is detected in Video Pipe 2	0b0: HS is not detected 0b1: HS is detected
HS_DET_1	1	HS activity is detected in Video Pipe 1	0b0: HS is not detected 0b1: HS is detected
HS_DET_0	0	HS activity is detected in Video Pipe 0	0b0: HS is not detected 0b1: HS is detected

**VS\_DET (0x11F2)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VS_DET_7	VS_DET_6	VS_DET_5	VS_DET_4	VS_DET_3	VS_DET_2	VS_DET_1	VS_DET_0
<b>Reset</b>	0b0							
<b>Access Type</b>	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DET_7	7	VS activity is detected in Video Pipe 7	0b0: VS is not detected 0b1: VS is detected
VS_DET_6	6	VS activity is detected in Video Pipe 6	0b0: VS is not detected 0b1: VS is detected
VS_DET_5	5	VS activity is detected in Video Pipe 5	0b0: VS is not detected 0b1: VS is detected
VS_DET_4	4	VS activity is detected in Video Pipe 4	0b0: VS is not detected 0b1: VS is detected
VS_DET_3	3	VS activity is detected in Video Pipe 3	0b0: VS is not detected 0b1: VS is detected
VS_DET_2	2	VS activity is detected in Video Pipe 2	0b0: VS is not detected 0b1: VS is detected
VS_DET_1	1	VS activity is detected in Video Pipe 1	0b0: VS is not detected 0b1: VS is detected
VS_DET_0	0	VS activity is detected in Video Pipe 0	0b0: VS is not detected 0b1: VS is detected

**HS\_POL (0x11F3)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	HS_POL_7	HS_POL_6	HS_POL_5	HS_POL_4	HS_POL_3	HS_POL_2	HS_POL_1	HS_POL_0
<b>Reset</b>	0b0							
<b>Access Type</b>	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_POL_7	7	Detected HS polarity in Video Pipe 7	0b0: Active low 0b1: Active high

BITFIELD	BITS	DESCRIPTION	DECODE
HS_POL_6	6	Detected HS polarity in Video Pipe 6	0b0: Active low 0b1: Active high
HS_POL_5	5	Detected HS polarity in Video Pipe 5	0b0: Active low 0b1: Active high
HS_POL_4	4	Detected HS polarity in Video Pipe 4	0b0: Active low 0b1: Active high
HS_POL_3	3	Detected HS polarity in Video Pipe 3	0b0: Active low 0b1: Active high
HS_POL_2	2	Detected HS polarity in Video Pipe 2	0b0: Active low 0b1: Active high
HS_POL_1	1	Detected HS polarity in Video Pipe 1	0b0: Active low 0b1: Active high
HS_POL_0	0	Detected HS polarity in Video Pipe 0	0b0: Active low 0b1: Active high

**VS\_POL (0x11F4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	VS_POL_7	VS_POL_6	VS_POL_5	VS_POL_4	VS_POL_3	VS_POL_2	VS_POL_1	VS_POL_0
<b>Reset</b>	0b0							
<b>Access Type</b>	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_POL_7	7	Detected VS polarity in Video Pipe 7	0b0: Active low 0b1: Active high
VS_POL_6	6	Detected VS polarity in Video Pipe 6	0b0: Active low 0b1: Active high
VS_POL_5	5	Detected VS polarity in Video Pipe 6	0b0: Active low 0b1: Active high
VS_POL_4	4	Detected VS polarity in Video Pipe 4	0b0: Active low 0b1: Active high
VS_POL_3	3	Detected VS polarity in Video Pipe 3	0b0: Active low 0b1: Active high
VS_POL_2	2	Detected VS polarity in Video Pipe 2	0b0: Active low 0b1: Active high
VS_POL_1	1	Detected VS polarity in Video Pipe 1	0b0: Active low 0b1: Active high
VS_POL_0	0	Detected VS polarity in Video Pipe 0	0b0: Active low 0b1: Active high

**WM\_0 (0x1200)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	WM_LEN	WM_MODE[2:0]				WM_DET[1:0]	—	WM_EN
<b>Reset</b>	0x0	0x0				0x0	—	0x0
<b>Access Type</b>	Write, Read	Write, Read				Write, Read	—	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_LEN	7	Watermark Length	0b0: Watermark length is 32 bits 0b1: Watermark length is 64 bits
WM_MODE	6:4	Select watermark generation mode	0b000: Default generator mode - cycle through all four watermarks in video stream 0b001: Error generator mode - cycle through only two watermarks to replicate a frozen frame 0b010 to 0b111: Reserved
WM_DET	3:2	Watermark Detection/Generation	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WM_EN	0	Enable/Disable of watermarking generation/detection block	0b0: Watermarking block disabled 0b1: Watermarking block enabled

**WM\_1 (0x1201)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	WM_KO[1:0]		—	—	—	—
<b>Reset</b>	—	—	0x1		—	—	—	—
<b>Access Type</b>	—	—	Write, Read		—	—	—	—
BITFIELD	BITS		DESCRIPTION					
WM_KO	5:4		Watermark Gain					

**WM\_2 (0x1202)**

BIT	7	6	5	4	3	2	1	0					
<b>Field</b>	—	—	—	—	HsyncPol	VsyncPol	WM_NPFILT[1:0]						
<b>Reset</b>	—	—	—	—	0b0	0b0	0x0						
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	Write, Read						
BITFIELD	BITS		DESCRIPTION			DECODE							
HsyncPol	3	HS Polarity			0b0: Non-inverting 0b1: Invert								
VsyncPol	2	VS Polarity			0b0: Non-inverting 0b1: Invert								
WM_NPFILT	1:0	Phase accumulator terminal count			0bXX: Phase accumulator terminal count								

**WM\_3 (0x1203)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	WM_TH[6:0]						
<b>Reset</b>	—	0x14						
<b>Access Type</b>	—	Write, Read						
BITFIELD	BITS		DESCRIPTION			DECODE		
WM_TH	6:0	Matched-filter threshold			0bXXXXXXXX: Matched-filter threshold			

WM\_4 (0x1204)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	—	—	WM_YUV_IN[1:0]		WM_COLO RADJ	—	WM_MASKMODE[1:0]			
<b>Reset</b>	—	—	0x01		0x0	—	0x0			
<b>Access Type</b>	—	—	Write, Read		Write, Read	—	Write, Read			
BITFIELD	BITS	DESCRIPTION					DECODE			
WM_YUV_IN	5:4	Input color format					0b00: RGB 8-bit color data 0b01: YUV444 8-bits each 0b10: Reserved 0b11: Reserved			
WM_COLOR ADJ	3	Color adjust					0b0: Masked off LSBs of U. Use if temporal dithering is enabled. 0b1: Set U[Ko:0] = 1/2 WM gain. Use this mode if temporal dithering is disabled			
WM_MASKM ODE	1:0	Sets watermark mask for the device					0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved 0b11: Reserved			

WM\_5 (0x1205)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	WM_DETO UT	WM_ERRO R
<b>Reset</b>	—	—	—	—	—	—	0x0	0x0
<b>Access Type</b>	—	—	—	—	—	—	Read Only	Read Only
BITFIELD	BITS	DESCRIPTION					DECODE	
WM_DETOU T	1	Live frame based detection output					0b0: Watermark not detected 0b1: Watermark detected	
WM_ERROR	0	Live active high watermark error					0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.	

WM\_6 (0x1206)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	WM_TIMER[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION					DECODE	
WM_TIMER	7:0	Time in 2ms steps the frozen frame condition must be observed before an error is generated. 0 = No filter					0XX: Number of milliseconds	

**WM\_WREN\_0 (0x121E)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	WM_WREN_L[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
WM_WREN_L	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read only.			0xBA: Enable writing to watermark registers others: Disable - Read Only			

**WM\_WREN\_1 (0x121F)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	WM_WREN_H[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
WM_WREN_H	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.			0xBA: Enable writing to watermark registers others: Disable - Read Only			

**WM\_0 (0x1220)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	WM1_LEN	WM1_MODE[2:0]			WM1_DET[1:0]		–	WM1_EN
<b>Reset</b>	0x0	0x0			0x0		–	0x0
<b>Access Type</b>	Write, Read	Write, Read			Write, Read		–	Write, Read
BITFIELD	BITS	<b>DESCRIPTION</b>			<b>DECODE</b>			
WM1_LEN	7	Watermark Length			0b0: Watermark length is 32 bits 0b1: Watermark length is 64 bits			
WM1_MODE	6:4	Select watermark generation mode			0b000: Default generator mode - cycle through all four watermarks in video stream 0b001: Error generator mode - cycle through only two watermarks to replicate a frozen frame 0b010 to 0b111: Reserved			
WM1_DET	3:2	Watermark Detection/Generation			0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved			
WM1_EN	0	Enable/Disable of watermarking generation/detection block			0b0: Watermarking block disabled 0b1: Watermarking block enabled			

WM\_1 (0x1221)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	—	—	WM1_KO[1:0]		—	—	—	—		
<b>Reset</b>	—	—	0x1		—	—	—	—		
<b>Access Type</b>	—	—	Write, Read		—	—	—	—		
BITFIELD	BITS	DESCRIPTION					DECODE			
WM1_KO	5:4	Watermark Gain					0b00: 1 bit 0b01: 2 bits 0b10: 3 bits 0b11: 4 bits			

WM\_2 (0x1222)

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	HsyncPol1	VsyncPol1	—	—
<b>Reset</b>	—	—	—	—	0b0	0b0	—	—
<b>Access Type</b>	—	—	—	—	Write, Read	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION					DECODE	
HsyncPol1	3	HS Polarity					0b0: Non-inverting 0b1: Invert	
VsyncPol1	2	VS Polarity					0b0: Non-inverting 0b1: Invert	

WM\_4 (0x1224)

BIT	7	6	5	4	3	2	1	0		
<b>Field</b>	—	—	WM1_YUV_IN[1:0]		WM1_COL_ORADJ	—	WM1_MASKMODE[1:0]			
<b>Reset</b>	—	—	0x01		0x0	—	0x0			
<b>Access Type</b>	—	—	Write, Read		Write, Read	—	Write, Read			
BITFIELD	BITS	DESCRIPTION					DECODE			
WM1_YUV_IN	5:4	Input color format					0b00: RGB 8-bit color data 0b01: YUV444 8-bits each 0b10: Reserved 0b11: Reserved			
WM1_COLRADJ	3	Color adjust					0b0: Masked off LSbs of U. Use if temporal dithering is enabled. 0b1: Set U [Ko:0] = 1/2 WM gain. Use this mode if temporal dithering is disabled			
WM1_MASKMODE	1:0	Sets watermark mask for the device					0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved 0b11: Reserved			

WM\_5 (0x1225)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	WM1_DET_OUT	WM1_ERR_OR
Reset	—	—	—	—	—	—	0x0	0x0
Access Type	—	—	—	—	—	—	Read Only	Read Only
BITFIELD	BITS	DESCRIPTION					DECODE	
WM1_DETO UT	1	Live frame based detection output					0b0: Watermark not detected 0b1: Watermark detected	
WM1_ERRO R	0	Live active high watermark error					0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.	

WM\_6 (0x1226)

BIT	7	6	5	4	3	2	1	0
Field	WM1_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION					DECODE	
WM1_TIMER	7:0	Time in 2ms steps the frozen frame condition must be observed before an error is generated. 0 = No filter					0xXX: Number of milliseconds	

WM\_WREN\_0 (0x123E)

BIT	7	6	5	4	3	2	1	0
Field	WM1_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION					DECODE	
WM1_WREN _L	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.					0xBA: Enable writing to watermark registers Others: Disable - Read Only	

WM\_WREN\_1 (0x123F)

BIT	7	6	5	4	3	2	1	0
Field	WM1_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM1_WREN_H	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.	0xBA: Enable writing to watermark registers Others: Disable - Read Only

**MEM\_ECC0 (0x1250)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MEM_ECC_ERR2_THR[2:0]				MEM_ECC_ERR1_THR[2:0]				
<b>Reset</b>	0x0				0x0				
<b>Access Type</b>	Write, Read				Write, Read				
BITFIELD	BITS	DESCRIPTION				DECODE			
MEM_ECC_ERR2_THR	7:5	Decoding and error reporting threshold. MEM_ECC_ERR2 is asserted when MEM_ECC_ERR2_CNT ≥ MEM_ECC_ERR2_THR.				0b000: 1 0b001: 2 0b010: 4 0b011: 8 0b100: 16 0b101: 32 0b110: 64 0b111: 128			
MEM_ECC_ERR1_THR	4:2	Decoding and error reporting threshold. MEM_ECC_ERR1 is asserted when MEM_ECC_ERR1_CNT ≥ MEM_ECC_ERR1_THR.				0b000: 1 0b001: 2 0b010: 4 0b011: 8 0b100: 16 0b101: 32 0b110: 64 0b111: 128			
RESET_ME_M_ECC_ER_R2_CNT	1	Reset memory ECC 2-bit error count to 0				0b0: Do not reset ECC 2-bit error count 0b1: Reset ECC 2-bit error count			
RESET_ME_M_ECC_ER_R1_CNT	0	Reset memory ECC 1-bit error count to 0				0b0: Do not reset ECC 1-bit error count 0b1: Reset ECC 1-bit error count			

**MEM\_ECC1 (0x1251)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MEM_ECC_ERR1_CNT[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Only								
BITFIELD	BITS	DESCRIPTION				DECODE			
MEM_ECC_ERR1_CNT	7:0	Number of 1-bit correctable memory ECC errors seen				0XXX: Number of 1-bit memory ECC errors			

MEM\_ECC2 (0x1252)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	MEM_ECC_ERR2_CNT[7:0]								
<b>Reset</b>	0x00								
<b>Access Type</b>	Read Only								
BITFIELD	BITS	DESCRIPTION							DECODE
MEM_ECC_ERR2_CNT	7:0	Number of 2-bit uncorrectable memory ECC errors seen							0xXX: Number of 2-bit memory ECC errors

MEM\_ECC\_ERR\_DEBUG (0x1253)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	—	—	—	—	—	—	MEM_INJ_E2A	MEM_INJ_E1A	
<b>Reset</b>	—	—	—	—	—	—	0b0	0b0	
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read	
BITFIELD	BITS	DESCRIPTION							DECODE
MEM_INJ_E2A	1	Injects 2 error bits for every 39-bit write into all 64 ECC memories in backtop							0b0: Do not inject error bits 0b1: Inject error bits
MEM_INJ_E1A	0	Injects 1 error bit for every 39-bit write into all 64 ECC memories in backtop							0b0: Do not inject error bits 0b1: Inject error bits

MEM\_ECC\_ERR\_FLAG (0x1254)

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	BACKTOP8_ECC_ERR_FLAG	BACKTOP7_ECC_ERR_FLAG	BACKTOP6_ECC_ERR_FLAG	BACKTOP5_ECC_ERR_FLAG	BACKTOP4_ECC_ERR_FLAG	BACKTOP3_ECC_ERR_FLAG	BACKTOP2_ECC_ERR_FLAG	BACKTOP1_ECC_ERR_FLAG	
<b>Reset</b>	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0	
<b>Access Type</b>	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	
BITFIELD	BITS	DESCRIPTION							DECODE
BACKTOP8_ECC_ERR_FLAG	7	Flag reads out 1-bit or 2-bit error in BACKTOP8, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error							0b0: No error detected 0b1: Error detected
BACKTOP7_ECC_ERR_FLAG	6	Flag reads out 1-bit or 2-bit error in BACKTOP7, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error							0b0: No error detected 0b1: Error detected
BACKTOP6_ECC_ERR_FLAG	5	Flag reads out 1-bit or 2-bit error in BACKTOP6, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error							0b0: No error detected 0b1: Error detected

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP5_ECC_ERR_FLAG	4	Flag reads out 1-bit or 2-bit error in BACKTOP5, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP4_ECC_ERR_FLAG	3	Flag reads out 1-bit or 2-bit error in BACKTOP4, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP3_ECC_ERR_FLAG	2	Flag reads out 1-bit or 2-bit error in BACKTOP3, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP2_ECC_ERR_FLAG	1	Flag reads out 1-bit or 2-bit error in BACKTOP2, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected
BACKTOP1_ECC_ERR_FLAG	0	Flag reads out 1-bit or 2-bit error in BACKTOP1, selected by ECC_ERR_FLAG_SEL. ECC_ERR_FLAG_SEL = 0 selects 2-bit error ECC_ERR_FLAG_SEL = 1 selects 1-bit error	0b0: No error detected 0b1: Error detected

**SPARE\_DIGITAL (0x12A1)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	—	RESET_ME_M_FLUSH	BACKTOP_ECC_ERR_SEL
<b>Reset</b>	—	—	—	—	—	—	0x0	0x0
<b>Access Type</b>	—	—	—	—	—	—	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ME_M_FLUSH	1	Write to 1 then 0 to reset memory flushed register in all BACKTOPs	0b0: Do not reset backtop memory flags 0b1: Reset backtop memory flags
BACKTOP_ECC_ERR_SEL	0	Selection bit for 1-bit or 2-bit ECC error flag read-out from BACKTOPx_ECC_ERR_FLAG register. Defaults to 2-bit error.	0b0: 2-bit errors reported 0b1: 1-bit errors reported

**RLMS3 (0x1403, 0x1503, 0x1603, 0x1703)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	AdaptEn	—	—	—	—	—	—	—
<b>Reset</b>	0x0	—	—	—	—	—	—	—
<b>Access Type</b>	Write, Read	—	—	—	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE				
AdaptEn	7	Adapt process enable	0b0: Timing adjust disabled 0b1: Timing adjust enabled				

**RLMS4 (0x1404, 0x1504, 0x1604, 0x1704)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
<b>Reset</b>	0x4				0x2		0x1	0x1
<b>Access Type</b>	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE				
EOM_CHK_AMOUNT	7:4	Number of samples collected in a measurement window (unit: millions)	0xx: N factor				
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits to allow in a measurement window	0b00: Allow no errors 0b01: Allow one error 0b10: Allow two errors 0b11: Allow three errors				
EOM_PER_MODE	1	Eye-opening monitor periodic mode enable	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled				
EOM_EN	0	Eye-opening monitor enable	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled				

**RLMS5 (0x1405, 0x1505, 0x1605, 0x1705)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	EOM_MAN_TRG_REQ	EOM_MIN THR[6:0]									
<b>Reset</b>	0x0	0x10									
<b>Access Type</b>	Write Only	Write, Read									
BITFIELD	BITS	DESCRIPTION			DECODE						
EOM_MAN_TRG_REQ	7	Eye-opening monitor manual trigger. For use when periodic mode is disabled.			0b0: No action 0b1: EOM manual trigger request						
EOM_MIN_T HR	6:0	Eye-opening measurement result lower than this flag's warning interrupt			0bXXXXXXXX: EOM minimum threshold factor						

**RLMS6 (0x1406, 0x1506, 0x1606, 0x1706)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	EOM_PV_MODE	EOM_RST_THR[6:0]									
<b>Reset</b>	0x1	0x00									
<b>Access Type</b>	Write, Read	Write, Read									
BITFIELD	BITS	DESCRIPTION			DECODE						
EOM_PV_MODE	7	Eye-opening is measured vertically or horizontally			0b0: Vertical opening mode 0b1: Horizontal opening mode						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_RST_T HR	6:0	Eye-opening measurement lower than this value resets the link. Disabled when set to 0.	0bXXXXXXXX: EOM refresh threshold factor

**RLMS7 (0x1407, 0x1507, 0x1607, 0x1707)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EOM_DON E	EOM[6:0]						
<b>Reset</b>	0x0	0x00						
<b>Access Type</b>	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-opening monitor measurement done	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Eye-opening measurement result	0bXXXXXXXX: EOM measurement result

**RLMS34 (0x1434, 0x1534, 0x1634, 0x1734)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EyeMonPerCntL[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
EyeMonPerC ntL	7:0	Eye-monitor period count (RxClk20) LSb			0xXX: Eye-monitor period count (least significant byte)			

**RLMS35 (0x1435, 0x1535, 0x1635, 0x1735)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EyeMonPerCntH[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
EyeMonPerC ntH	7:0	Eye-monitor period count (RxClk20) MSb			0xXX: Eye-monitor period count (most significant byte)			

**RLMS37 (0x1437, 0x1537, 0x1637, 0x1737)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	EyeMonDon e	EyeMonCnt Clr	EyeMonStar t	EyeMonPh	EyeMonDP ol
<b>Reset</b>	—	—	—	0x0	0x0	0x0	0x0	0x0
<b>Access Type</b>	—	—	—	Read Only	Write Only	Write Only	Write, Read	Write, Read

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonDone	4	Eye-monitor period complete (read-only, reset on start)	0b0: Eye-monitor data collection not complete 0b1: Eye-monitor data collection complete
EyeMonCntC lr	3	Eye-monitor error/valid count clear (one-shot) Read-back is EyeMonClrPL from long-pulse generation	0b0: NA 0b1: Clear eye-monitor data collection counters
EyeMonStart	2	Eye-monitor start (one-shot) Read-back is EyeMonStClrPL from long-pulse generation for both start and clear	0b0: NA 0b1: Start eye-monitor data collection
EyeMonPh	1	Eye-monitor phase	0b0: Eye-monitor search early phase 0b1: Eye-monitor search late phase
EyeMonDPol	0	Eye-monitor data polarity	0b0: Eye-monitor search for 1's 0b1: Eye-monitor search for 0's

**RLMS38 (0x1438, 0x1538, 0x1638, 0x1738)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EyeMonErrCntL[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION				DECODE		
EyeMonErrC ntL	7:0	Eye-monitor error count (read-only)				0xFF: Eye-monitor error count (least significant byte)		

**RLMS39 (0x1439, 0x1539, 0x1639, 0x1739)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EyeMonErrCntH[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION				DECODE		
EyeMonErrC ntH	7:0	Eye-monitor error count (read-only)				0xFF: Eye-monitor error count (most significant byte)		

**RLMS3A (0x143A, 0x153A, 0x163A, 0x173A)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EyeMonValCntL[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION				DECODE		
EyeMonValC ntL	7:0	Eye-monitor valid (hit) count (read-only)				0xFF: Eye-monitor valid count (least significant byte)		

**RLMS3B (0x143B, 0x153B, 0x163B, 0x173B)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	EyeMonValCntH[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
EyeMonValCnTH	7:0	Eye-monitor valid (hit) count (read-only)			0xXX: Eye-monitor valid count (most significant byte)			

**RLMS3D (0x143D, 0x153D, 0x163D, 0x173D)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ErrChPh[6:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							
BITFIELD	BITS	DESCRIPTION			DECODE			
ErrChPh	7:1	Error channel phase (read-only)			0bXXXXXXXX: 5.6 degrees per step			
ErrChPhTogEn	0	Error channel phase toggle enable			0b0: Use primary phase only 0b1: Auto toggle phase between primary and secondary			

**RLMS3E (0x143E, 0x153E, 0x163E, 0x173E)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	ErrChPhSecCTA	ErrChPhSec[6:0]							
<b>Reset</b>	0x1	0x33							
<b>Access Type</b>	Write, Read	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE				
ErrChPhSecTA	7	Error channel phase secondary timing adjust			0b0: Timing adjust disabled 0b1: Timing adjust enabled				
ErrChPhSec	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. Value: 7'h3A			0bxxxxxxxx: Error channel phase secondary (odd)				

**RLMS3F (0x143F, 0x153F, 0x163F, 0x173F)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	ErrChPhPriTA	ErrChPhPri[6:0]							
<b>Reset</b>	0x0	0x72							
<b>Access Type</b>	Write, Read	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTA	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPri	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. Value 7'h79	0bxxxxxx: Error channel phase primary (even)

**RLMS45 (0x1445, 0x1545, 0x1645, 0x1745)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RSVD	RSVD	—	—	—	RSVD[2:0]		
<b>Reset</b>	0x0	0x0	—	—	—	0x1		
<b>Access Type</b>	Write, Read	Write, Read	—	—	—	Write, Read		
BITFIELD	BITS	DESCRIPTION						DECODE
RSVD	7	Reserved						Must write value of 0.
RSVD	6	Reserved						Must write value of 0.
RSVD	2:0	Reserved						Must write value of 0.

**RLMS49 (0x1449, 0x1549, 0x1649, 0x1749)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	ErrChPwrUp	—	—
<b>Reset</b>	—	—	—	—	—	0x0	—	—
<b>Access Type</b>	—	—	—	—	—	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION						DECODE
ErrChPwrUp	2	Error channel power-down						0b0: Error channel power disabled 0b1: Error channel power enabled

**RLMS58 (0x1458, 0x1558, 0x1658, 0x1758)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	ErrChVTh1[6:0]						—
<b>Reset</b>	—	0x28						—
<b>Access Type</b>	—	Write, Read						—
BITFIELD	BITS	DESCRIPTION						DECODE
ErrChVTh1	6:0	Error channel target amplitude for ones. Bits 7, 5:0						0b0: Error channel power disabled 0b1: Error channel power enabled

**PRELIMINARY**

**RLMS59 (0x1459, 0x1559, 0x1659, 0x1759)**

BIT	7	6	5	4	3	2	1	0
Field	—	ErrChVTh0[6:0]						
Reset	—	0x68						
Access Type	—	Write, Read						
BITFIELD	BITS	DESCRIPTION				DECODE		
ErrChVTh0	6:0	Error channel target amplitude for zeros Bits 7, 5:0				0bxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count		

**RLMS64 (0x1464, 0x1564, 0x1664, 0x1764)**

BIT	7	6	5	4	3	2	1	0		
Field	—	—	—	—	—	—	TxSSCMode[1:0]			
Reset	—	—	—	—	—	—	0x0			
Access Type	—	—	—	—	—	—	Write, Read			
BITFIELD	BITS	DESCRIPTION				DECODE				
TxSSCMode	1:0	Tx spread spectrum mode				0b00: No spread spectrum (manual phase) 0b01: Center spread 0b10: Down spread 0b11: Reserved				

**RLMS70 (0x1470, 0x1570, 0x1670, 0x1770)**

BIT	7	6	5	4	3	2	1	0
Field	—	TxSSCFrqCtrl[6:0]						
Reset	—	0x01						
Access Type	—	Write, Read						
BITFIELD	BITS	DESCRIPTION				DECODE		
TxSSCFrqCtr	6:0	Tx spread spectrum frequency control				0bXXXXXXXX: Tx spread spectrum center frequency control		

**RLMS71 (0x1471, 0x1571, 0x1671, 0x1771)**

BIT	7	6	5	4	3	2	1	0
Field	—	TxSSCCenSprSt[5:0]						
Reset	—	0x01						
Access Type	—	Write, Read						
BITFIELD	BITS	DESCRIPTION				DECODE		
TxSSCCenSprSt	6:1	Tx spread spectrum center spread startup control				0bXXXXXXXX: Tx spread spectrum center spread startup control		
TxSSCEn	0	Tx spread spectrum enable				0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled		

**RLMS72 (0x1472, 0x1572, 0x1672, 0x1772)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TxSSCPreSclL[7:0]							
<b>Reset</b>	0xCF							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
TxSSCPreSclL	7:0	Tx spread spectrum frequency pre-scaler			0xXX: Tx spread spectrum frequency pre-scaler low byte			

**RLMS73 (0x1473, 0x1573, 0x1673, 0x1773)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	—	—	—	—	—	TxSSCPreSclH[2:0]					
<b>Reset</b>	—	—	—	—	—	0x0					
<b>Access Type</b>	—	—	—	—	—	Write, Read					
BITFIELD	BITS	DESCRIPTION			DECODE						
TxSSCPreSclH	2:0	Tx spread spectrum frequency pre-scaler			0bXXX: Tx spread spectrum frequency pre-scaler high bits						

**RLMS74 (0x1474, 0x1574, 0x1674, 0x1774)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	TxSSCPhL[7:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
TxSSCPhL	7:0	Tx spread spectrum interpolator phase			0xXX: Tx spread spectrum frequency interpolator phase low byte			

**RLMS75 (0x1475, 0x1575, 0x1675, 0x1775)**

BIT	7	6	5	4	3	2	1	0	
<b>Field</b>	—	TxSSCPhH[6:0]							
<b>Reset</b>	—	0x0							
<b>Access Type</b>	—	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE				
TxSSCPhH	6:0	Tx spread spectrum interpolator phase			0bXXXXXXXX: Tx spread spectrum frequency interpolator phase high bits				

**RLMS76 (0x1476, 0x1576, 0x1676, 0x1776)**

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	TxSSCPhQuad[1:0]	
Reset	—	—	—	—	—	—	0x0	
Access Type	—	—	—	—	—	—	Write, Read	
BITFIELD	BITS	DESCRIPTION					DECODE	
TxSSCPhQuad	1:0	Tx spread spectrum interpolator phase quadrant					0xbXX: Tx spread spectrum interpolator phase quadrant	

**RLMS95 (0x1495, 0x1595, 0x1695, 0x1795)**

BIT	7	6	5	4	3	2	1	0
Field	TxAmpManEn	—	—	—	—	—	—	—
Reset	0x0	—	—	—	—	—	—	—
Access Type	Write, Read	—	—	—	—	—	—	—
BITFIELD	BITS	DESCRIPTION					DECODE	
TxAmpManEn	7	Tx amplitude manual override					0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude	

**RLMSA4 (0x14A4, 0x15A4, 0x16A4, 0x17A4)**

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0x2		0x3D					
Access Type	Write, Read		Write, Read					
BITFIELD	BITS	DESCRIPTION					DECODE	
AEQ_PER_MULT	7:6	Adaptive EQ period multiplier					0b00: 1ms 0b01: 4ms 0b10: 16ms 0b11: 64ms	
AEQ_PER	5:0	Adaptive EQ Period  Periodic adaptation is disabled when value is zero.  Adaptive EQ period is (AEQ_PER value times AEQ_PER_MULT)					0bXXXXXX: Only zeros have a special meaning	

**RLMSAC (0x14AC, 0x15AC, 0x16AC, 0x17AC)**

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecCTAFR3G		ErrChPhSecFR3G[6:0]					
Reset	0x1		0x4D					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSec TAFR3G	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSec FR3G	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Fast Receive, Secondary Phase, 3Gbps)	0bXXXXXXXX: 7'h4D

**RLMSAD (0x14AD, 0x15AD, 0x16AD, 0x17AD)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ErrChPhPri TAFR3G	ErrChPhPriFR3G[6:0]						
<b>Reset</b>	0x0	0x0D						
<b>Access Type</b>	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriT AFR3G	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriF R3G	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Fast Receive, Primary Phase, 3Gbps)	0bXXXXXXXX: 7'h0D

**RLMSB6 (0x14B6, 0x15B6, 0x16B6, 0x17B6)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ErrChPhSe cTASRG1875	ErrChPhSecSRG1875[6:0]						
<b>Reset</b>	0x1	0x3B						
<b>Access Type</b>	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSec TASRG1875	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSec SRG1875	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Secondary Phase, 187.5Mbps)	0bXXXXXXXX: 7'h3B

**RLMSB7 (0x14B7, 0x15B7, 0x16B7, 0x17B7)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	ErrChPhPri TASRG1875	ErrChPhPriSRG1875[6:0]						
<b>Reset</b>	0x0	0x7A						
<b>Access Type</b>	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriT ASRG1875	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriS RG1875	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Primary Phase, 187.5Mbps)	0bXXXXXXXX: 7'h7A

**RLMSC4 (0x14C4, 0x15C4, 0x16C4, 0x17C4)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	—	—	—	—	—	RevFast	—	—
<b>Reset</b>	—	—	—	—	—	0b0	—	—
<b>Access Type</b>	—	—	—	—	—	Write, Read	—	—
BITFIELD	BITS	DESCRIPTION						DECODE
RevFast	2	GMSL1 reverse channel fast mode						0b0: Reverse channel fast mode disabled 0b1: Reverse channel fast mode enabled

**RLMSC5 (0x14C5, 0x15C5, 0x16C5, 0x17C5)**

BIT	7	6	5	4	3	2	1	0
<b>Field</b>	RevLenMan En	RevFLenMan[6:0]						
<b>Reset</b>	0b0	0x40						
<b>Access Type</b>	Write, Read	Write, Read						
BITFIELD	BITS	DESCRIPTION						DECODE
RevLenManEn	7	Enable manual override of reverse channel pulse length						0b0: Disable manual override 0b1: Enable manual override
RevFLenMan	6:0	GMSL1 reverse channel first pulse length (x 6.666 ns)						0bXXXXXXXX: GMSL1 reverse channel first pulse length (x 6.666 ns)

**RLMSD1 (0x14D1, 0x15D1, 0x16D1, 0x17D1)**

BIT	7	6	5	4	3	2	1	0			
<b>Field</b>	RSVD[2:0]				RSVD[2:0]			RSVD			
<b>Reset</b>	0x4				0x2			0x0			
<b>Access Type</b>	Write, Read				Write, Read			Write, Read			
BITFIELD	BITS	DESCRIPTION						DECODE			
RSVD	7:5	Reserved						Must write value of 0.			
RSVD	4:2	Reserved						Must write value of 0.			
RSVD	1	Reserved						Must write value of 1.			
RSVD	0	Reserved						Must write value of 1.			

DPLL\_0 (0x1C00)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	—	config_soft_rst_n
Reset	—	—	—	—	—	—	—	0x1
Access Type	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS		DESCRIPTION					
config_soft_rst_n	0		Setting this to 1 will reset the PLL functional registers, config_regs are not reset.					

DPLL\_0 (0x1D00)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	—	config_soft_rst_n
Reset	—	—	—	—	—	—	—	0x1
Access Type	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS		DESCRIPTION					
config_soft_rst_n	0		Setting this to 1 will reset the PLL functional registers, config_regs are not reset.					

DPLL\_0 (0x1E00)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	—	config_soft_rst_n
Reset	—	—	—	—	—	—	—	0x1
Access Type	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS		DESCRIPTION					
config_soft_rst_n	0		Setting this to 1 will reset the PLL functional registers, config_regs are not reset.					

DPLL\_0 (0x1F00)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	—	config_soft_rst_n
Reset	—	—	—	—	—	—	—	0x1
Access Type	—	—	—	—	—	—	—	Write, Read
BITFIELD	BITS		DESCRIPTION					
config_soft_rst_n	0		Setting this to 1 will reset the PLL functional registers, config_regs are not reset.					

PRELIMINARY

## Applications Information

### Control-Channel Programming

MAX96722 internal registers can be accessed locally via any of the three available I<sup>2</sup>C/UART ports. Lower indexed ports have higher priority in the case of simultaneous queries. By default, remote GMSL serializer register access is available via I<sup>2</sup>C/UART port 0 only. However, the internal I<sup>2</sup>C/UART routing mux enables any of the three ports to connect to the control channel, which thereby provides access to remote serializer registers. Only one of the three ports can access the control channel at a given time, and the other two I<sup>2</sup>C/UART ports then function essentially as remote pass-throughs from the perspective of the serializer. See I<sup>2</sup>C/UART for further details regarding the routing of I<sup>2</sup>C/UART ports in the MAX96722. For multimaster configurations with microcontrollers connected to both the serializer and deserializer, bus contention can be avoided by using register settings to disable the remote control channel. In all cases register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

### Device Address

Each device on the I<sup>2</sup>C/UART control channel must have a unique address. This includes both peripherals and GMSL devices. The GMSL2 device address is set to one of several 7-bit addresses according to the voltage level of the CFG0 pin at power-up. See CFG Latch at Power-up Pins for further details. Note that device address can be changed after power-up by writing to the DEV\_ADDR register.

### I<sup>2</sup>C Programming

Each device has an internal I<sup>2</sup>C slave for register access. The internal registers can be written and read according to the I<sup>2</sup>C protocol using the packet formats below. Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition. SDA and SCL lines operate as both an input and an open-drain output. External pullup resistors are required on SDA and SCL.

### Main I<sup>2</sup>C Host-to-GMSL2 Device Communication

The host I<sup>2</sup>C master has access to GMSL2 serializer and deserializer registers. Any of the MAX96722's I<sup>2</sup>C interfaces can be used to access local GMSL2 device registers. In the case of contention, the lower indexed port has precedence. Remote GMSL2 device registers can be accessed by any one of the three available ports. Only one port can access remote device registers via a given GMSL link at a time. By default, port 0 is configured to have remote device register access.

### I<sup>2</sup>C Write Packet Format

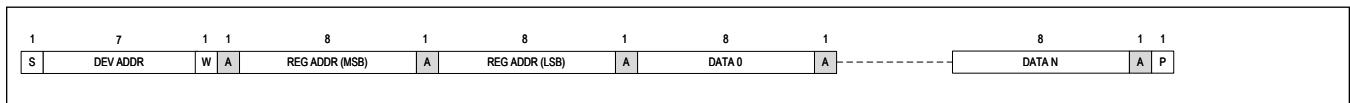


Figure 38. I<sup>2</sup>C Write Packet Format

### I<sup>2</sup>C Read Packet Format

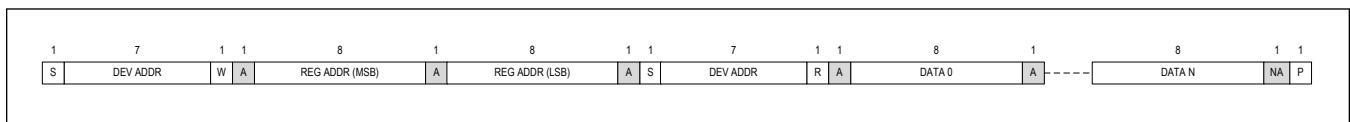


Figure 39. I<sup>2</sup>C Read Packet Format

### Host-to-Peripheral Main I<sup>2</sup>C and Pass-Through I<sup>2</sup>C Communication

When communicating between a host and peripheral, main and pass-through I<sup>2</sup>C operation is the same. An I<sup>2</sup>C tunnel

across the GMSL2 link connects the host's I<sup>2</sup>C master to the remote I<sup>2</sup>C slave. This logically connects separated I<sup>2</sup>C buses, enabling I<sup>2</sup>C transactions across the serial link to occur (with some delay) as if performed on the same physical I<sup>2</sup>C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I<sup>2</sup>C master connects to a GMSL2 device I<sup>2</sup>C slave, and the peripheral I<sup>2</sup>C slave connects to a GMSL2 device I<sup>2</sup>C master.

For example, when the host I<sup>2</sup>C master transacts on one side of the link (local-side), the I<sup>2</sup>C slave of the local-side GMSL2 device forwards data to the other side (remote-side). Data is then received by the I<sup>2</sup>C master of the remote-side GMSL2 device, which in turn generates the same I<sup>2</sup>C transaction with the peripheral slave I<sup>2</sup>C. The remote-side GMSL2 device sends back any I<sup>2</sup>C data expected by the local-side.

The I<sup>2</sup>C interface uses clock stretching (holding SCL low) to account for timing differences between master and slave and to allow time for data to be forwarded and received across the serial link. The host I<sup>2</sup>C master and peripheral I<sup>2</sup>C slave must support clock stretching by the GMSL2 device.

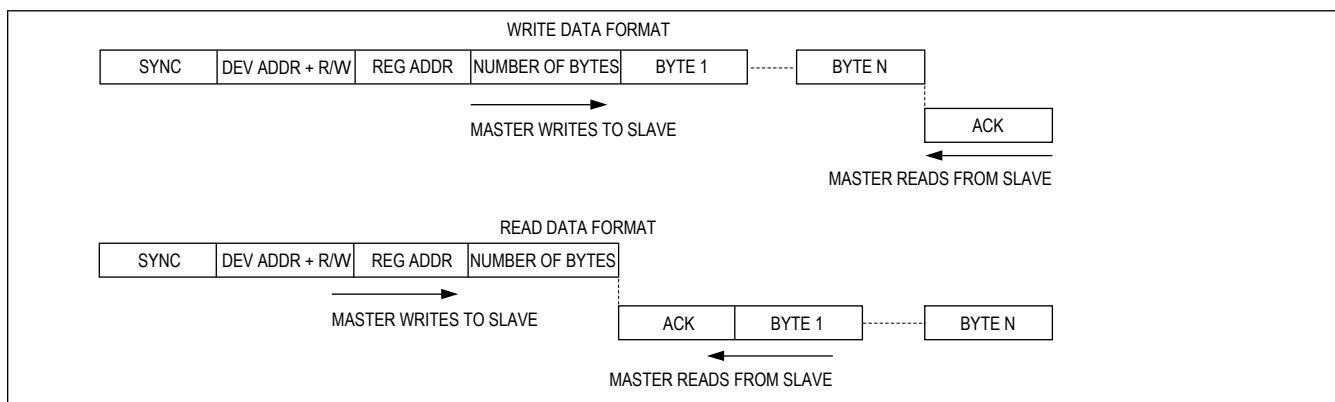
The host device can program GMSL2 device registers to independently configure the pass-through I<sup>2</sup>C/UART interfaces for communication over specified GMSL links as either I<sup>2</sup>C or UART.

## UART Programming

When the main I<sup>2</sup>C/UART interface is configured as UART, there are two operating modes: base and bypass.

### UART Base Mode

Base mode is the means of μC communication with the serializer and deserializer in which internal registers in these devices can be accessed in addition to registers in peripheral devices. Base mode is enabled by default at power-up. In base mode, the μC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL2 UART packet protocol (see [Figure 40](#)). The μC can also communicate with compatible peripherals on the remote side when the remote side GMSL2 device's local control channel is enabled. The device addresses of the serializer and deserializer in this mode are programmable.



*Figure 40. GMSL2 UART Protocol for Base Mode*

### UART Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the μC, allowing the μC to communicate only with peripheral devices. The μC cannot access the serializer/deserializer registers in this mode, and as a result the addresses of the GMSL devices are not programmable. The UART transitions are simply sent over the GMSL link and routed directly to the attached peripherals. Ignoring UART transactions prevents inadvertent misprogramming of serializer and deserializer registers.

### Switching Between UART Base and Bypass Modes

Selection of the UART mode can be specified by either register programming or appropriate control of the MS pin.

When register programmed, bypass mode is active only as long as there is UART activity. When there is no UART activity

for a selected timeout, both devices exit bypass mode and the bit is automatically cleared.

When set by the MS pin, a high pin level puts the device into bypass mode, and a low level puts the device in base mode. MS is set on-the-fly and is not latched on power-up.

### UART Frame Format

Regular UART frames with an even parity bit are used to carry 1 byte of data each. A frame consists of a low start bit followed by 8 data bits, a parity bit, and a high stop bit. The parity bit is high if the number of ones in the 8 bits of data is odd, otherwise, the parity bit is low. There must be at least 1 high stop bit. If the next frame is in the same packet, there can be at most 4 high bits from the end of the stop bit to the beginning of the next start bit. Note that in the case of a parity bit error, the packet, starting from the frame with the error, is discarded. The start of each frame is always a high-to-low transition (i.e., the stop bit is high and the start bit is low). The phase of the internal UART bit clock is adjusted using the synchronization frame (i.e., the first frame of a UART packet transmission). In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions; the recipient of the data must perform error checking. Optionally, the parity bit can be disabled before entering bypass mode. Note that the bit rate in bypass mode must be the same bit rate last used in base mode.

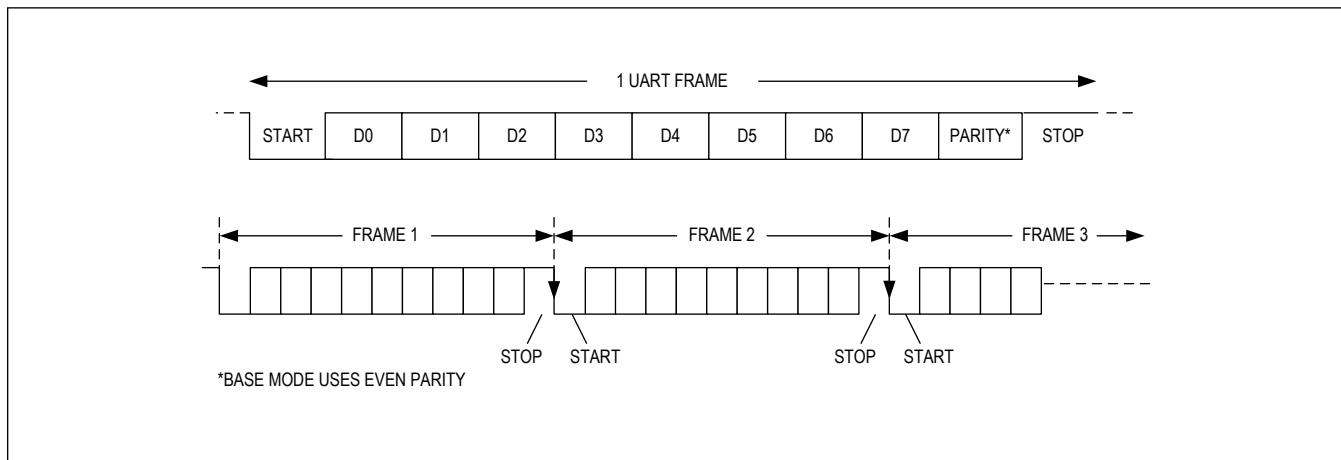


Figure 41. UART Data Format for Base Mode

### Synchronization Frame

The serializer/deserializer must calibrate internal bit length counters with the UART bit rate for proper recovery of UART frames. A sync frame (a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal 150MHz clock. Sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next sync frame.

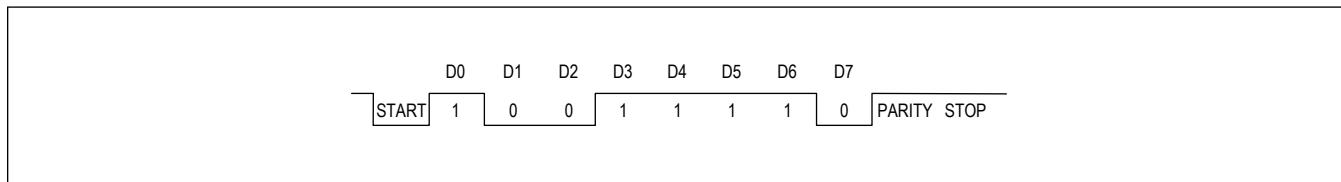


Figure 42. UART Synchronization Frame

**Acknowledge Frame**

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors were detected in the transmitted packet, and it was recognized as valid. This is sent after the last bit of a successfully recognized packet has been received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

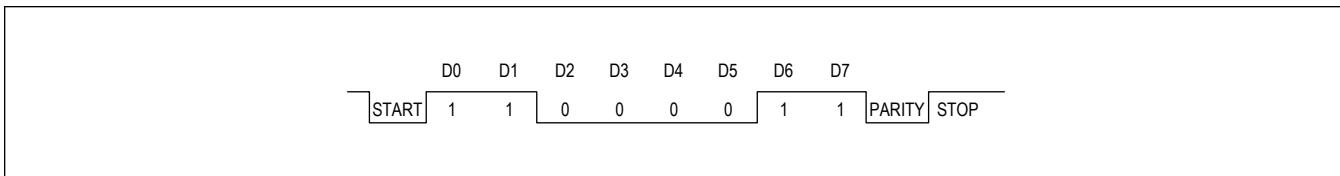


Figure 43. UART Acknowledge Frame

**Write Packet**

A write packet consists of a 5 byte packet header followed by 1 or more data bytes. A packet is recognized as a write packet when the LSB of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors were detected while receiving the packet. Byte count indicates the number of data bytes to be written and this number cannot be zero.

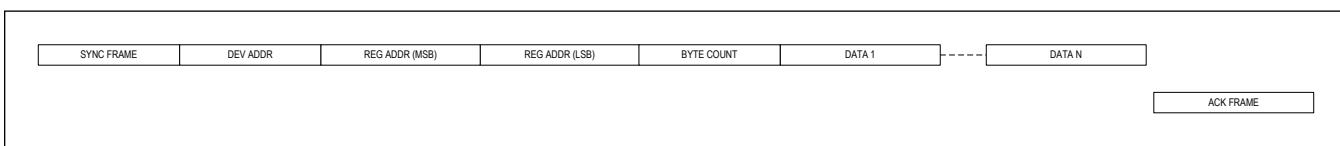


Figure 44. UART Write Packet Format

**Read Packet**

A read packet consists of 5 bytes. The LSB of the device address frame is 1 for read packets. If no errors were detected while receiving a valid read packet, the addressed device responds with an acknowledge frame followed by 1 or more data bytes. Byte count indicates the number of data bytes to be read and this number cannot be zero.

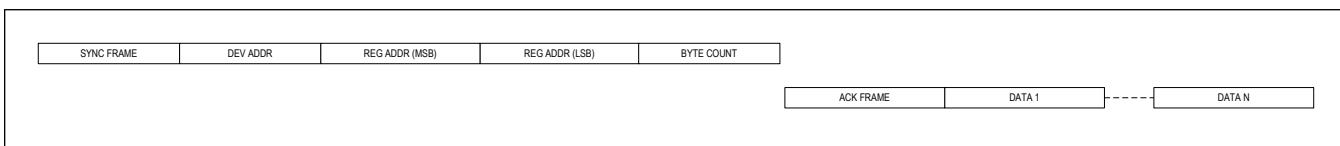


Figure 45. UART Read Packet Format

**Ordering Information**

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX96722GTB/V+	-40°C to +105°C	64 TQFN-EP
MAX96722GTB/V+T	-40°C to +105°C	64 TQFN-EP (Tape and Reel)
MAX96722GTB/VY+	-40°C to +105°C	64 TQFN-SW-EP
MAX96722GTB/VY+T	-40°C to +105°C	64 TQFN-SW-EP (Tape and Reel)

/V Denotes an Automotive Qualified Product.

+ Denotes a lead(Pb)-free/RoHS-compliant Package.

T Denotes tape-and-reel.

EP Denotes Exposed Pad.

Y Denotes Wettable Flank.

**PRELIMINARY**

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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