

MAX96860/MAX96862/MAX96864

GMSL3/2 eDP Deserializers with Optional Decompression, HDCP, Daisy Chain, and Ethernet

General Description

The MAX96860/MAX96862/MAX96864 deserializers convert single- or dual-link GMSL™ serial input to embedded DisplayPort (eDP) v1.4a. The devices support uncompressed 24bpp video up to 820MHz PCLK and 30bpp up to 660MHz.

The GMSL video input links operate at fixed rates of 12Gbps PAM4 in GMSL3™ mode and 6Gbps NRZ in GMSL2™ mode. The reverse link data rate is 187.5Mbps.

The devices also send and receive side-channel and peripheral control data to enable full-duplex single-wire transmission of video and bidirectional data.

DSC decompression, which supports maximum PCLKs of 1080MHz at 24bpp and 864MHz at 30bpp, over a single coax or twisted pair link is supported on certain part numbers.

Specific part numbers support HDCP 1.4 and HDCP 2.3 decryption of the locally-output video stream.

GMSL3/2 daisy chaining of up to 3 video streams and HDCP pass-through to downstream deserializers is supported on specific part numbers. The video streams can have different resolutions and timings.

Specific part numbers support a bidirectional SGMII pass-through interface for 100Mbps Ethernet, enabling high-speed data transmission concurrent with the video stream.

The concurrent control channel supports I²C or UART. Two additional pass-through I²C or UART channels and a pass-through SPI channel are provided for peripheral control. The audio channel supports forward I²S stereo.

Applications

- Ultra-Wide Front Seat Infotainment Displays
- 4K Rear-Seat Infotainment Displays

Benefits and Features

- eDP Output Supports up to 1080MHz PCLK at 24bpp and 864MHz PCLK at 30bpp
- Multiple GMSL Link Rates for System Flexibility
 - 12, 6, or 3Gbps Single Lane Forward Link Rates
 - 12Gbps Dual Link Rate (24Gbps in even/odd pixel splitter)
 - 187Mbps Reverse Link Rate
 - Over 1230MHz PCLK over Daisy-Chain Output (Optional)
- Bandwidth Support
 - Up to 215MHz PCLK Uncompressed 24bpp Video per GMSL2 Link
 - Up to 410MHz PCLK Uncompressed 24bpp Video per GMSL3 Link
 - Up to 430MHz PCLK Uncompressed 24bpp Video over Dual GMSL2 Links
 - Up to 600MHz PCLK Compressed 24bpp Video over single GMSL2 Link
 - Up to 1080MHz PCLK Compressed 24bpp Video over single GMSL3 Link
 - Up to 864MHz PCLK Compressed 30bpp Video over single GMSL3 Link
- Supports 24-Bit and 30-Bit Color Depth
- Decompression of 3:1 and 3.75:1 DSC (Optional)
- Full-Duplex Capability over a Single Wire
- HDCP 1.4 and 2.3 Decryption (Optional)
- SGMII Bidirectional Pass-Through Interface for 100Mbps Ethernet over Side Channel (Optional)
- Two Pass-Through I²C/UART Channels, in Addition to Main I²C/UART Channel
- Local Forward I²S Audio Output
- 8:10 Bit Color LUTs with FRC
- Concurrent Control Channel for Device Configuration and Communicating with Remote Peripherals
- Tunneled or Register-Programmable GPIOs
- Low-Current Sleep Mode
- Compact 8mm x 8mm TQFN Package with EP
- Operation Specified over Automotive Ambient Temperature Range of -40°C to +105°C
- AEC-Q100 Qualified
- Data Can be Transmitted Over Low-Cost 50Ω Coax or 100Ω STP Cables that Meet the GMSL3/2 Channel Specification.

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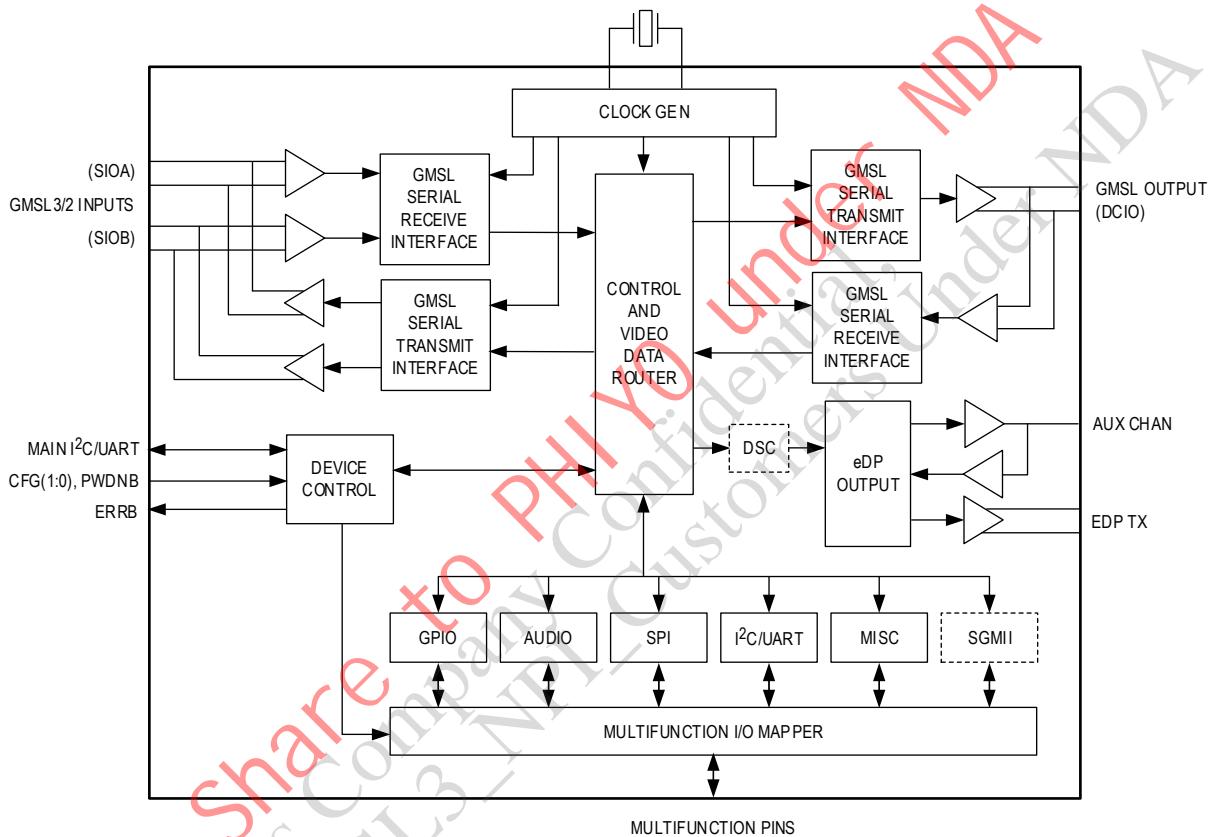
Table 1. Typical Maximum Cable Length

	3.2mm Ø 50Ω Coax, Foam Dielectric	2.7mm Ø 50Ω Coax, Solid Dielectric	100Ω Shielded Twisted Pair, AWG26
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m

Attenuation at 3GHz (Max, Aged, 105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	Typical Maximum Cable Length at 105°C		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m

Contact the factory to receive the GMSL2 Channel Specification document.

Simplified Block Diagram



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Absolute Maximum Ratings

(All voltages with respect to ground.)
V _{DDIO}-0.3V to +3.9V
V _{DD18}-0.3V to +2.0V
V _{DD}-0.3V to +1.1V
CAP_VDD-0.3V to +1.1V
SIO_ (Active State) (Note 1).....(V _{DD18} - 1.1V) V to V _{DD18} V
SIO_ (Inactive State) (Note 1)-0.3V to +1.1V

DCIO_.....	-0.3VV to (CAP_VDD + 0.3V)V
eTX_	-0.3V to +1.1V
AUXP/N	-0.3V V to (V _{DD18} + 0.3V) V
XRES, X2, DIS_Rem_CC.....	-0.3V V to (V _{DD18} + 0.3V) V
All Other Pins (Note 2)	-0.3V V to (V _{DDIO} + 0.3V) V
Storage Temperature Range	-40°C to +150°C
Soldering Temperature (reflow)	+260°C

Note 1: Active state means the device is powered up and not in sleep or power-down modes. Inactive means the device is not powered up, or powered up in sleep or power-down mode.

Note 2: Specified maximum voltage or 3.9V, whichever is lower

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56TQFN-EP

Package Code	T5688+5C
Outline Number	21-0135
Land Pattern Number	90-0046
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	21°C/W
Junction to Case (θ_{JA})	1°C/W

SW-56TQFN-EP

Package Code	T5688Y+5C
Outline Number	21-100046
Land Pattern Number	90-100023
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	21°C/W
Junction to Case (θ_{JA})	1°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board in still air. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

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Electrical Characteristics

($V_{DD18} = 1.7V$ to $1.9V$, $V_{DDIO} = 1.7V$ to $3.6V$, $V_{DD} = 0.95V$ to $1.05V$, $T_A = -40^\circ C$ to $+105^\circ C$, EP connected to PCB ground. Typical values are at $V_{DD18} = V_{DDIO} = 1.8V$, $V_{DD} = 1.0V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / REVERSE CHANNEL SERIAL OUTPUTS (SIO_)							
Output Voltage Swing (Single-Ended)	V_O	$R_L = 50\Omega \pm 1\%$	12Gbps Link Rate	110	150	190	mV
			6Gbps Link Rate	190	250	310	
Output Voltage Swing (Differential)	V_{ODT}	$R_L = 100\Omega \pm 1\%$, peak-to-peak differential voltage	12Gbps Link Rate	220	300	380	mV
			6Gbps Link Rate	380	500	620	
Change in V_{OD} between Complementary Output States	ΔV_{OD}	$R_L = 100\Omega \pm 1\%$, $ V_{OD(H)} - V_{OD(L)} $			25		mV
Differential Output Offset Voltage	V_{OS}	$R_L = 100\Omega \pm 1\%$, offset voltage in each output state	$V_{DD18} - 0.45$	$V_{DD18} - 0.05$			V
Change in V_{OS} between Complementary Output States	ΔV_{OS}	$R_L = 100\Omega \pm 1\%$, $ V_{OS(H)} - V_{OS(L)} $			25		mV
Termination Resistance (Internal)	R_T	Any Pin to V_{DD18}	50	55	60		Ω
DC ELECTRICAL CHARACTERISTICS / GMSL DAISY-CHAIN FORWARD-CHANNEL SERIAL OUTPUTS (DCIO_)							
Output Voltage Swing (Single-Ended)	$ V_{O1} $	$R_L = 50\Omega \pm 1\%$, $(V_{OH} - V_{OL})$ for both outputs	PAM4	400	500	600	mV
			NRZ	300	400	500	
Output Voltage Swing (Differential)	V_{OD}	$R_L = 100\Omega \pm 1\%$, peak-to-peak differential voltage	PAM4	800	1000	1200	mV_{P-P}
			NRZ	600	800	1000	
Change in V_{OD} Between Complementary Output States	$\Delta V_{OD} $	$R_L = 100\Omega \pm 1\%$, $ V_{OD(H)} - V_{OD(L)} $			25		mV
Differential Output Offset Voltage	V_{OS}	$R_L = 100\Omega \pm 1\%$, offset voltage in each output state	0.4	0.5	0.6		V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	$R_L = 100\Omega \pm 1\%$, $ V_{OS(H)} - V_{OS(L)} $			25		mV
Termination Resistance (Internal)	R_T	Incremental resistance around V_{OS}	43	50	57		Ω
DC ELECTRICAL CHARACTERISTICS / SGMII RX AND TX LANES (Note 6)							
Output Differential Voltage	$ V_{odl} $	For default TX signal swing settings. Programmable options exist for higher and lower swing levels	300	400	500		mV
Output Offset Voltage	V_{os}	For default TX signal swing settings	400		600		mV
Output Ringing	V_{ring}	Note 4	For default TX signal swing settings		10		%
Output Impedance (Differential)	R_o			80	120		Ω
Impedance Mismatch in an Output Pair	ΔR_o	Note 4			10		%
Change in V_{od} Between Complementary States	$\Delta V_{odl} $	Note 4			25		mV

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Change in V_{os} between Complementary States	ΔV_{os}	Note 4			25	mV
Power-Off Leakage Current for Outputs	I_{xa}, I_{xb}	Notes 4, 9	TBD	TBD	TBD	mA
Input Common-Mode Input Voltage Range	V_{CM}	Notes 4, 10	0.6	1.4	1.4	V
Input Common Mode Voltage (AC-coupled)	V_{cm}	Note 4		1.2		V
Differential Input Swing Voltage (Differential Peak)	V_{DIFF}		125	500	500	mV
Input Differential Termination Resistance	R_{TERM}		80	120	120	Ω
Power-Down Mode Input Current		$V_{IN} = TBDV$ to $TBDV$, both inputs at same voltage			$\pm TBD$	μA

DC ELECTRICAL CHARACTERISTICS / eDP OUTPUTS (eTX_)

Differential Peak-to-Peak Output Voltage	V_{OD}	$R_L = 100\Omega \pm 1\%$ $V_{DD} = 1.0V$	Amplitude Setting 0	175	200	225	mV
			Amplitude Setting 1	305	350	395	
			Amplitude Setting 2	350	400	450	
			Amplitude Setting 3	395	450	505	
Termination Resistance (Internal)	R_T	Single-ended measurement		40	50	60	Ω

DC ELECTRICAL CHARACTERISTICS / eDP AUX CHANNEL (AUX_)

Differential Peak-to-Peak Output Voltage	V_{OD}	$R_L = 100\Omega \pm 1\%$	Amplitude Setting 0	200	mV	
			Amplitude Setting 1	400		
			Amplitude Setting 2	600		
			Amplitude Setting 3	800		
			Amplitude Setting 4	1000		
			Amplitude Setting 5	1200		
			Amplitude Setting 6	1380		
Input Peak-to-Peak Voltage	V_{ID}			140	1360	mV
Input Common-Mode Voltage	V_{CMI}	Register setting at mid-scale		800		mV
Termination Resistance (Internal)	R_T	Single-ended measurement		50		Ω

DC ELECTRICAL CHARACTERISTICS / I/O PINS

High-Level Input Voltage	V_{IH}		0.7 $\times V_{DDIO}$		V
Low-Level Input Voltage	V_{IL}		0.3 $\times V_{DDIO}$		V
High-Level Output Voltage	V_{OH}	$I_{OH} = -4mA$	$V_{DDIO} - 0.4$		V
Low-Level Output Voltage	V_{OL}	$I_{OL} = 4mA$		0.4	V
Input Current	I_{IN}	All pull-up/pull-down devices disabled, $V_{IN} = 0V$ to V_{DDIO}		1	μA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}		3			pF
Internal Pull-Up/Pull-Down Resistance	R_{IN}	40k Ω enabled	40			k Ω
		1M Ω enabled	1			M Ω
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 $\times V_{DDIO}$			V
Low-Level Input Voltage	V_{IL}		0.3 $\times V_{DDIO}$			V
Low-Level Open-Drain Output Voltage	V_{OL}	$I_{OL} = 4mA$	0.4			V
Input Current	I_{IN}	All pull-up/pull-down devices disabled, $V_{IN} = 0V$ to V_{DDIO}	1			μA
Input Capacitance	C_{IN}		3			pF
Internal Pull-Up Resistance	R_{PU}	40k Ω enabled	40			k Ω
		1M Ω enabled	1			M Ω
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 $\times V_{DDIO}$			V
Low-Level Input Voltage	V_{IL}		0.3 $\times V_{DDIO}$			V
Input Current	I_{IN}	$V_{IN} = 0V$ to V_{DDIO}	6			μA
Internal Pull-Down Resistance	R_{PD}		1			M Ω
Input Capacitance	C_{IN}		3			pF
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held low to reset the chip.	1			ms
DC ELECTRICAL CHARACTERISTICS / DIS_Rem_CC INPUT						
High-Level Input Voltage	V_{IH}		1.6			V
Low-Level Input Voltage	V_{IL}		1.4			V
Input Current	I_{IN}	$V_{IN} = 0V$ to V_{DD18}	30			μA
Internal Pull-Down Resistance	R_{PD}		100			k Ω
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	$I_{OH} = -4mA$	$V_{DDIO} - 0.4$			V
Low-Level Output Voltage	V_{OL}	$I_{OL} = 4mA$	0.4			V
DC ELECTRICAL CHARACTERISTICS / LINE FAULT DETECTION INPUTS (LMN0, LMN1)						
Open Pin Voltage	V_{O0}	LMN0	1.25			V
	V_{O1}	LMN1	0.75			
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2)						
X1 Input Capacitance	C_{IN_X1}		3			pF
X2 Input Capacitance	C_{IN_X2}		1			pF
Internal X2 Limit Resistor	R_{LIM}		1.2			k Ω

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Feedback Resistor	R_{FB}			10		kΩ
Transconductance	g_m			28		mA/V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1, X2 UNCONNECTED)						
High-Level Input Voltage	V_{IH}		0.9			V
Low-Level Input Voltage	V_{IL}			0.4		V
Input Impedance	R_{IN}			10		kΩ
X1 Input Capacitance	C_{IN_X1}			3		pF
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS (MAX96860/MAX96862/MAX96864)						
Supply Current	I_{DD}	V_{DD}	TBD	630	TBD	mA
		V_{DD18}	TBD	220	TBD	
AC ELECTRICAL CHARACTERISTICS / FORWARD CHANNEL SWITCHING CHARACTERISTICS (SIO_)						
Lock Time	t_{LOCK}	From power-up, release of RESET_LINK, or rising edge of PWDNB to rising edge of LOCK.		TBD	TBD	ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from GMSL2 video packet input at SIO± input to when pixels appear at video outputs. Assumes link is already established and eDP link training is complete.		5		ms
Maximum Video Latency	t_{VL}	Time from pixel within GMSL2 packet at SIO± to output at eDP interface.		50		μs
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip.		1		ms
AC ELECTRICAL CHARACTERISTICS / REVERSE CHANNEL SERIAL OUTPUTS (SIO_)—(Note 4)						
GMSL Reverse Channel Transmitter Rise/Fall Time	t_R, t_F	20% to 80%, $V_O = 250mV$, $R_L = 100\Omega$		2300		ps
Total Serial Output P-P Jitter	t_{TSOJ}	PRBS7, single-ended or differential output		0.15		UI
Deterministic Serial Output P-P Jitter	t_{DSOJ}	PRBS7, single-ended or differential output		0.1		UI
AC ELECTRICAL CHARACTERISTICS / GMSL DAISY-CHAIN FORWARD-CHANNEL SERIAL OUTPUTS (DCIO_)						
Serial Output Rise Time	t_R	20% to 80%, $V_O = 40mV$, NRZ, $R_L = 100\Omega \pm 1\%$		50		ps
Serial Output Fall Time	t_F	80% to 20%, $V_O = 40mV$, NRZ, $R_L = 100\Omega \pm 1\%$		50		ps
Total Serial Output Jitter	t_{TSOJ}	PRBS7, single-ended or differential output		0.15		UI (p-p)
Deterministic Serial Output Jitter	t_{DSOJ}	PRBS7, single-ended or differential output		0.10		UI (p-p)
Lock Time	t_{LOCK}			TBD	TBD	ms
Maximum Video Latency	t_{VL}	Time from pixel within GMSL packet at SIO input to same pixel at DCIO output, FEC enabled.		480		ns
AC ELECTRICAL CHARACTERISTICS / SGMII RX AND TX LANES (Note 6)						

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency Offset Between Devices	FSGMII_OFF			± 100		ppm
Clock Signal Duty Cycle	Clock	Clock signal duty cycle at 625MHz	48	52		%
V_{OD} Rise/Fall Time	t_{rf}	20% - 80%	100	200		ps
Skew Between Two Members of a Differential Pair	t_{skew}	Skew measured at 50% of the transition. $T_{pHL} =$ propagation delay high to low transition, $T_{pLH} =$ propagation delay low to high transition	$ T_{pHAI} - T_{pLHB} $ or $ T_{pHAI} - T_{pHLB} $	20		ps
Clock to Data Relationship from either Edges of the Clock to Valid Data	$t_{clock2q}$	Skew measured at 0V differential.	250	550		ps
Setup Time when RXCLK is used	t_{setup}	Measured at 50% of the transition	100			ps
Hold Time when RXCLK is used	t_{hold}	Measured at 50% of the transition	100			ps
Total Output Jitter (BER = $1e-12$)	$J_{it,out}$	When data is tracked with a CDR using 4MHz bandwidth		300		ps
Input Jitter Tolerance	$J_{it,in}$	For jitter frequency component higher than 637kHz	480			ps
AC ELECTRICAL CHARACTERISTICS / eDP OUTPUTS (eDP __) —(Note 4)						
Unit Interval	UI_Rate	1.62 Gbps/lane (RBR)	617			ps
		2.7 Gbps/lane (HBR)	370			
		5.4 Gbps/lane (HBR2)	185			
		8.1 Gbps/lane (HBR3)	123			
Preemphasis		All output voltage settings	Preemphasis Setting 0	0		dB
			Preemphasis Setting 1	2		
			Preemphasis Setting 2	4		
			Preemphasis Setting 3	6		
Total Jitter (Note 7)	t_{TJO}	Lane rate ≤ 5.4 Gbps	0.27			UI
		Lane rate = 8.1Gbps	0.28			
Deterministic Jitter (Note 7)	t_{DJO}	Lane rate ≤ 5.4 Gbps	0.17			UI
		Lane rate = 8.1Gbps	0.2			
Output Skew	t_{SKEW}	Intrapair	30			ps
		Lane-to-Lane	1250			
SSC Downspread				0.55		%
SSC Modulation Rate			30	33		kHz
AC ELECTRICAL CHARACTERISTICS / eDP AUX CHANNEL (AUX __) —(Note 4)						

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Unit Interval	UI		0.4	0.6		μs
Cycle-to-Cycle Jitter	t_{JCC}	UI variation within a single transaction		0.08		UI
		UI variation between adjacent bits		0.04		
AC ELECTRICAL CHARACTERISTICS / DP HPD						
HPD IRQ Pulse Width		(Note 2)	0.5	1		ms
IRQ_HPD Minimum Spacing				<1		μs
AC ELECTRICAL CHARACTERISTICS / I²C / UART PORT TIMING (Note 2)						
Output Fall Time	t_f	70% to 30%, $C_L = 20pF$ to $100pF$, $1k\Omega$ pull-up to V_{DDIO}	$20 \times V_{DDIO} / 5.5V$	150		ns
I ² C/UART Wake Time	t_{CC_WAKE}	From power-up or rising edge of PWDNB to local register access. For remote register access, I ² C/UART wake time is the same as lock time (t_{PUL_LOCK}).		2.25	4	ms
AC ELECTRICAL CHARACTERISTICS / I²C TIMING						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range	9.6	100		kHz
		Mid f_{SCL} range	100	400		
		High f_{SCL} range	400	1000		
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			μs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			μs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			μs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			μs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			μs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			μs
		f_{SCL} range, mid	1.3			

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**GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet**

MAX96860/MAX96862/MAX96864

($V_{DD18} = 1.7V$ to $1.9V$, $V_{DDIO} = 1.7V$ to $3.6V$, $V_{DD} = 0.95V$ to $1.05V$, $T_A = -40^\circ C$ to $+105^\circ C$, EP connected to PCB ground. Typical values are at $V_{DD18} = V_{DDIO} = 1.8V$, $V_{DD} = 1.0V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, high	0.5			
		f_{SCL} range, low		3.45		μs
		f_{SCL} range, mid		0.9		
		f_{SCL} range, high		0.45		
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low		3.45		μs
		f_{SCL} range, mid		0.9		
		f_{SCL} range, high		0.45		
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low		50		ns
		f_{SCL} range, mid		50		
		f_{SCL} range, high		50		
Capacitive Load on Each Bus Line	C_B			100		pF
AC ELECTRICAL CHARACTERISTICS / SPI MAIN						
Operating Frequency	f_{MCK}		0.588	50		MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	(Note 4, Note 8)	$t_{MCK}/2$ - 3.4	$t_{MCK}/2$		ns
MOSI Data Output Delay	t_{MOD}	After SCLK falling edge (Note 4, Note 8)	-2.3	2.3		ns
MISO Input Setup Time	t_{MIS}	Before programmed sampling edge (Note 4, Note 8)	13.5			ns
MISO Input Hold Time	t_{MIH}	After programmed sampling edge (Note 4, Note 8)	-2			ns
AC ELECTRICAL CHARACTERISTICS / SPI SUBORDINATE						
Operating Frequency	f_{SCK}			50		MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
MISO Data Output Delay	t_{SOD}	After SCLK falling edge (Note 4, Note 8)	2.0	11.3		ns
MOSI Input Setup Time	t_{SIS}	Before SCLK rising edge (Note 8)	5			ns
MOSI Input Hold Time	t_{SIH}	After SCLK rising edge (Note 8)	3			ns
AC ELECTRICAL CHARACTERISTICS / I²S/TDM MAIN TIMING (Note 4, Note 8)						
WS Frequency	f_{WS}	$C_L = 5pF$	8	192		kHz
Sample Word Length	n_{WS}	$C_L = 5pF$	8	32		Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8), C_L = 5pF$	0.512	49.152		MHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}, t_{SCK} = 1/f_{SCK}, C_L = 5pF$	$0.35 \times t_{SCK}$			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}, t_{SCK} = 1/f_{SCK}, C_L = 5pF$	$0.35 \times t_{SCK}$			ns
SD, WS Valid Time Before SCK	t_{MAVS}	$t_{SCK} = 1/f_{SCK}, C_L = 5pF$	$0.2 \times t_{SCK}$	$0.5 \times t_{SCK}$		ns
SD, WS Valid Time After SCK	t_{MAVH}	$t_{SCK} = 1/f_{SCK}, C_L = 5pF$	$0.2 \times t_{SCK}$	$0.5 \times t_{SCK}$		ns
AC ELECTRICAL CHARACTERISTICS / I²S/TDM SUBORDINATE TIMING (Note 8)						

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GMSL3/2 eDP Deserializers with Optional Decompression, HDCP, Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

($V_{DD18} = 1.7V$ to $1.9V$, $V_{DDIO} = 1.7V$ to $3.6V$, $V_{DD} = 0.95V$ to $1.05V$, $T_A = -40^\circ C$ to $+105^\circ C$, EP connected to PCB ground. Typical values are at $V_{DD18} = V_{DDIO} = 1.8V$, $V_{DD} = 1.0V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WS Frequency	f_{WS}		8		192	kHz
Sample Word Length	n_{WS}		8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$ (Note 4)	0.512		49.152	MHz
SD, WS Setup Time	t_{SAS}		4			ns
SD, WS Hold Time	t_{SAH}		4			ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2)—(Note 4)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				± 200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1, X2 UNCONNECTED)—(Note 4)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				± 200	ppm
Input Jitter		Sinusoidal jitter < 1MHz (rising edge), downstream deserializer using crystal reference			TBD	ps
Input Duty Cycle	t_{DUTY}		40	60		%
Input Fall Time	t_F	80% to 20%			4	ns

Note 3: Limits are 100% tested at $T_A = +105^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 4: Not production tested. Guaranteed by design and characterization.

Note 5: Color Bar pattern, 60Hz frame rate

Note 6: All parameters are measured with $100\Omega \pm 1\%$ load

Note 7: 300mVp-p, 2dB preemphasis, CP2520 compliance pattern, measured at TP2

Note 8: Measured at 50MHz.

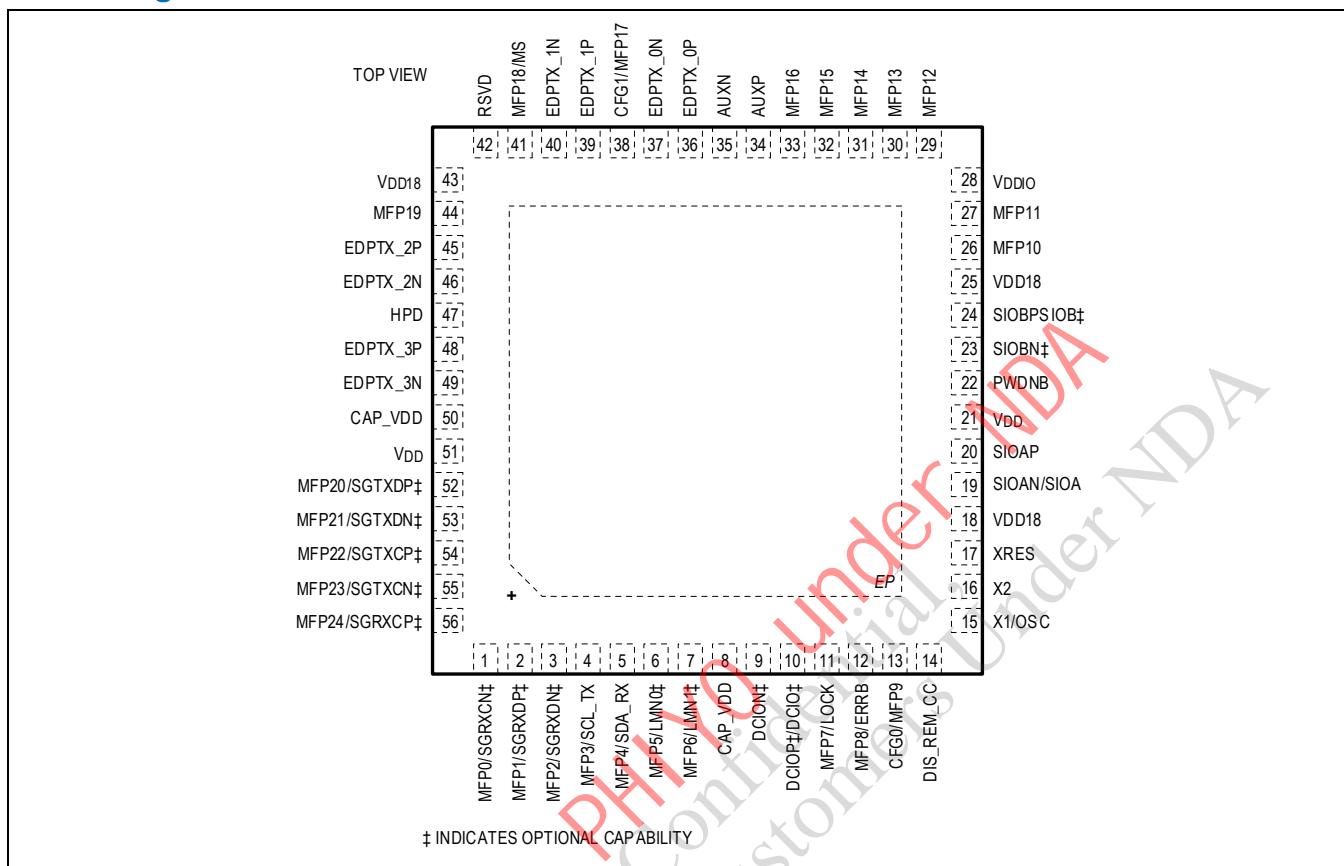
Note 9: SGMII supports AC-coupled use cases and differentially terminated DC-coupled use cases with minimum $X\ k\Omega$ bias resistance to a Y Volts receiver supply. In DC-coupled use cases, single ended termination to a supply is not supported.

Note 10: Connection using AC coupling capacitors recommended. DC-coupled connections should maintain compliance to input common mode voltage range.

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Analog Devices
Provided to GMSL3/2 eDP Customers Under NDA

Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION MODE	FUNCTION
		SIGNAL NAME	
GMSL3/2 SERIAL LINK (Leave DCIO_ output pins unconnected when daisy-chaining is not used)			
19	SIOAN/SIOA	SIOAN SIOA	SIOAN: GMSL3/2 Link A Inverted Twisted-Pair Serial-Data Input. State of CFG1 on power-up determines configuration. SIOA: GMSL3/2 Link A Coax Serial-Data Input. State of CFG1 on power-up determines configuration.
20	SIOAP	SIOAP	SIOAP: GMSL3/2 Link A Noninverted Twisted-Pair Serial-Data Input. State of CFG1 on power-up determines configuration.
24	SIOBP/SIOB	SIOBP SIOB	SIOBP: GMSL3/2 Link B Noninverted Twisted-Pair Serial-Data Input. State of CFG1 on power-up determines configuration. SIOB: GMSL3/2 Link B Coax Serial-Data Input. State of CFG1 on power-up determines configuration.
23	SIOBN	SIOBN	SIOBN: GMSL3/2 Link B Inverted Twisted-Pair Serial-Data Input. State of CFG1 on power-up determines configuration.

9	DCION	DCION	DCION: GMSL3/2 Daisy-Chain Inverted Twisted-Pair Serial-Data Output. State of CFG[1:0] on power-up determines configuration.
10	DCIOP/DCIO	DCIOP DCIO	DCIOP: GMSL3/2 Daisy-Chain Noninverted Twisted-Pair Serial-Data Output. State of CFG[1:0] on power-up determines configuration. DCIO: GMSL3/2 Daisy-Chain Coax Serial-Data Output. State of CFG[1:0] on power-up determines configuration.
eDP INTERFACE			
47	HPD	HPD	eDP Hot-Plug Detect Input. Configured as open-drain I/O with $1M\Omega$ pull-down to ground.
34	AUXN	AUXN	eDP Inverted AUX Channel.
35	AUXP	AUXP	eDP Noninverted AUX Channel.
36	EDPTX_0P	EDPTX_0P	eDP Noninverted Data Output Channel 0.
37	EDPTX_0N	EDPTX_0N	eDP Inverted Data Output Channel 0.
39	EDPTX_1P	EDPTX_1P	eDP Noninverted Data Output Channel 1.
40	EDPTX_1N	EDPTX_1N	eDP Inverted Data Output Channel 1.
45	EDPTX_2P	EDPTX_2P	eDP Noninverted Data Output Channel 2.
46	EDPTX_2N	EDPTX_2N	eDP Inverted Data Output Channel 2.
48	EDPTX_3P	EDPTX_3P	eDP Noninverted Data Output Channel 3.
49	EDPTX_3N	EDPTX_3N	eDP Inverted Data Output Channel 3.
MULTIFUNCTION PINS (*DENOTES DEFAULT STATE AFTER POWER-UP)			
1	MFP0/SGRXCN	SGRXCN SCLK GPIO0*	SGRXCN: SGMII RXC- Clock Input. Coupling capacitors may be required depending on the paired device. SCLK: SPI Clock. When configured as main, push-pull clock output. When configured as subordinate, clock input with internal $1M\Omega$ pull-down to ground. GPIO0: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, $1M\Omega$ pull-down. Note: Leave pin unconnected when not used.
2	MFP1/SGRXDP	SGRXDP MOSI GPIO1*	SGRXDP: SGMII RXD+ Data Input. Coupling capacitors may be required depending on the paired device. MOSI: SPI Main-Out Subordinate-In. When configured as main, push-pull output that drives data to external subordinate. When configured as subordinate, input with internal $1M\Omega$ pull-down to ground that receives data from external main. GPIO1: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, $1M\Omega$ pull-down. Note: Leave pin unconnected when not used.
3	MFP2/SGRXDN	SGRXDN MISO GPIO2*	SGRXDN: SGMII RXD- Data Input. Coupling capacitors may be required depending on the paired device. MISO: SPI Main-In Subordinate-Out. When configured as main, input with internal $1M\Omega$ pull-down to ground that receives data from external subordinate. When configured as subordinate, push-pull output that drives data to an external main. GPIO2: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output

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			disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
4	MFP3/SCL_TX	SCL* TX* GPIO3	SCL: I ² C Clock Input/Open-Drain Output with Internal 40kΩ Pull-Up to V _{DDIO} (SCL or TX selected by CFG0 at power-up). TX: UART Open-Drain Output with Internal 40kΩ Pull-Up to V _{DDIO} (SCL or TX selected by CFG0 at power-up). GPIO3: Configurable General-Purpose Input/Output. Open-drain output with internal 40kΩ pull-up, CMOS input enabled, output disabled.
5	MFP4/SDA_RX	SDA* RX* GPIO4	SDA: I ² C Data Input/Open-Drain Output with Internal 40kΩ Pull-Up to V _{DDIO} (SDA or RX selected by CFG0 at power-up). RX: UART Input (SDA or RX selected by CFG0 at power-up). GPIO4: Configurable General-Purpose Input/Output. Open-drain output with internal 40kΩ pull-up, CMOS input enabled, output disabled.
6	MFP5	LMN0 GPIO5*	LMN0: Line Fault Monitor Input. GPIO5: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
7	MFP6	LMN1 GPIO6*	LMN1: Line Fault Monitor Input. GPIO6: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
11	MFP7/LOCK	LOCK* GPIO7	LOCK: Open-Drain Lock Indication Output with Internal 40kΩ Pull-Up to V _{DDIO} . LOCK = HIGH indicates that GMSL link has locked and is ready to send/receive data. See LOCK_CFG register description. LOCK is HIGH when PWDNB is LOW. GPIO7: Configurable General-Purpose Input/Output. Open-drain output with internal 40kΩ pull-up.
12	MFP8/ERRB	ERRB* GPIO8	ERRB: Open-Drain Error Indication Output with Internal 40kΩ Pull-Up to V _{DDIO} . ERRB = LOW indicates a data error, line fault, or interrupt is detected. ERRB is HIGH when PWDNB is LOW. GPIO8: Configurable General-Purpose Input/Output. Open-drain output with internal 40kΩ pull-up.
13	CFG0/MFP9	CFG0* WMD GPO9	CFG0: Configuration Pin 1. Voltage at pin sets device mode, which is latched at power-up. Connect a resistor divider between V _{DDIO} and ground. WMD: Watermark Detect Push-Pull Output. High when watermark is detected. GPO9: Configurable General-Purpose Output.
26	MFP10	SDA1 RX1 GPIO10*	SDA1: Pass-Through Port 1 I ² C Data Input/Open-Drain Output with Internal 40kΩ Pull-Up to V _{DDIO} . RX1: Pass-Through Port 1 UART Input. GPIO10: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output

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**GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet**

MAX96860/MAX96862/MAX96864

			disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
27	MFP11	SCL1 TX1 GPIO11*	SCL1: Pass-Through Port 1 I ² C Clock Input/Open-Drain Output with Internal 40kΩ Pull-Up to V _{DDIO} . TX1: Pass-Through Port 1 UART Output with Internal 40kΩ Pull-Up to V _{DDIO} . GPIO11: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
29	MFP12	DE_OUT_X WS GPIO12*	DE_OUT_X: Data Enable Output of Video Pipe X. WS: I ² S/TDM Word-Select Push-Pull Output. Supports forward-path audio. GPIO12: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
30	MFP13	HS_X SD GPIO13*	HS_X: Pipe X Horizontal Sync Input or Push-Pull Output. SD: I ² S/TDM FWD Audio Channel Serial-Data Push-Pull Output. Supports forward audio from serializer to deserializer. GPIO13: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
31	MFP14	VS_X SCK GPIO14*	VS_X: Pipe X Vertical Sync Input or Push-Pull Output. SCK: I ² S/TDM FWD Audio Channel Clock Push-Pull Output. Supports forward-path audio. GPIO14: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
32	MFP15	MDIO SDA2 RX2 GPIO15*	MDIO: SGMII Serial Management Data Input or Output. Output is open-drain by default with an internal 40kΩ pull-up to V _{DDIO} . SDA2: Pass-Through Port 2 I ² C Data Input/Open-Drain Output with Internal 40kΩ Pull-Up to V _{DDIO} . RX2: Pass-Through Port 2 UART Input. GPIO15: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
33	MFP16	MDC SCL2 TX2 GPIO16*	MDC: SGMII Serial Management Clock Push-Pull Output. SCL2: Pass-Through Port 2 I ² C Clock Input/Open-Drain Output with Internal 40kΩ Pull-Up to V _{DDIO} . TX2: Pass-Through Port 2 UART Output with Internal 40kΩ Pull-Up to V _{DDIO} . GPIO16: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down.

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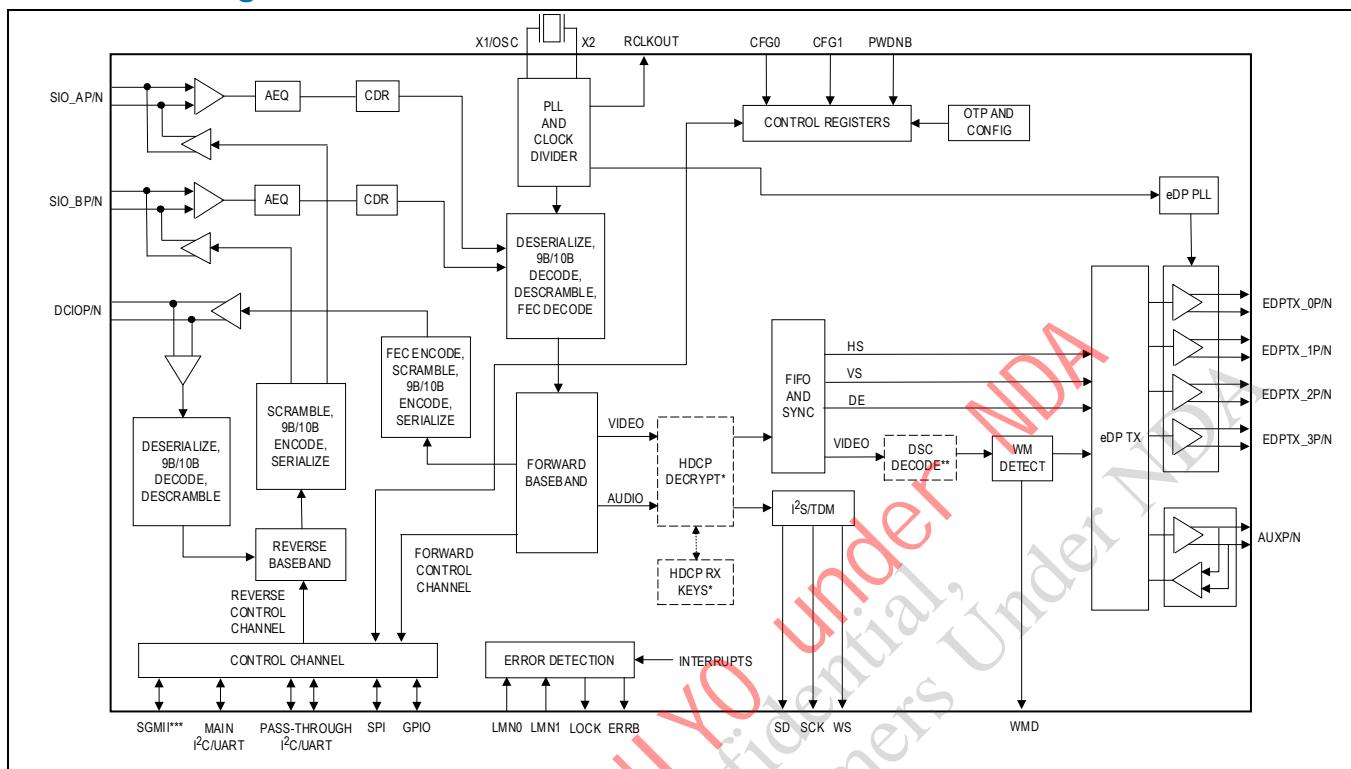
			Note: Leave pin unconnected when not used.
38	CFG1/MFP17	CFG1* VA_DONE GPIO17	CFG1: Configuration Pin 2. Voltage at pin sets device modes, which are latched at power-up. Connect a resistor divider between V _{DDIO} and ground. VA_DONE: Video Authentication CRC/SHA Calculation Complete Push-Pull Interrupt Output. GPIO17: Configurable General-Purpose Input/Output.
41	MFP18/MS	VS_X_ALT MS GPIO18*	VS_X_ALT: Alternate Pipe X Vertical Sync Input or Push-Pull Output. MS: UART Mode Select with Internal 1MΩ Pull-Down to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be temporarily overwritten by a register write. GPIO18: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
44	MFP19	HS_X_ALT GPIO19	HS_X_ALT: Alternate Pipe X Horizontal Sync Input or Push-Pull Output. GPIO19: Configurable General-Purpose Input/Output. Power-up default.
52	MFP20/SGTXDP	SGTXDP VS_OUT_Y GPIO20*	SGTXDP: SGMII TXD+ Data Output. Coupling capacitors may be required depending on the paired device. VS_OUT_Y: Vertical Sync Output of Video Pipe Y. GPIO20: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
53	MFP21/SGTXDN	SGTXDN HS_OUT_Y GPIO21*	SGTXDN: SGMII TXD- Data Output. Coupling capacitors may be required depending on the paired device. HS_OUT_Y: Horizontal Sync Output of Video Pipe Y. GPIO21: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
54	MFP22/SGTXCP	SGTXCP DE_OUT_Y RCLKOUT GPIO22*	SGTXCP: SGMII TXC+ Clock Output. Coupling capacitors may be required depending on the paired device. DE_OUT_Y: Data Enable Output of Video Pipe Y. RCLKOUT: 25MHz Reference Clock Push-Pull Output. GPIO22: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
55	MFP23/SGTXCN	SGTXCN BNE SS1 GPIO23*	SGTXCN: SGMII TXC- Clock Output. Coupling capacitors may be required depending on the paired device. BNE: When Configured as Subordinate, SPI Buffer-Not-Empty Push-Pull Output. BNE = high indicates SPI data is available. SS1: SPI Subordinate Select. When configured as main, Subordinate 1 select push-pull output. GPIO23: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output

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			disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
56	MFP24/SGRXCP	SGRXCP RO SS2 GPIO24*	SGRXCP: SGMII RXC+ Clock Input. Coupling capacitors may be required depending on the paired device. RO: When Configured as Subordinate, SPI Mode-Select Input with Internal 1MΩ Pull-Down to Ground. RO = high enables main read from MISO. RO = low enables main write to MOSI. SS2: SPI Subordinate Select. When configured as main, Subordinate 2 select push-pull output. GPIO24: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pull-down. Note: Leave pin unconnected when not used.
MISCELLANEOUS			
14	DIS_Rem_CC	DIS_Rem_CC	Active-High Latch at Power-Up Input. Internal 100kΩ pull-down to ground. Disables the remote-control channel in multimaster configurations (only the local ECU can control the deserializer). Connect to VDD18 to disable the remote-control channel (sets DIS_Rem_CC register bits to logic-1). Connect to ground or leave floating to enable the remote-control channel function (sets DIS_Rem_CC register bits to default logic-0 state). After power-up latch, writing to DIS_Rem_CC can change the state of the remote-control channel enable. Note: Leave pin unconnected when not used.
15	X1/OSC	X1/OSC	X1/OSC: Crystal/Oscillator Input. Connect to either terminal of a ±200ppm 25MHz crystal or a 25MHz external clock source. If crystal is used, connect a load capacitor from X1/OSC to ground (load capacitor value depends on crystal used).
16	X2	X2	X2: Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal. If crystal is used, connect a load capacitor from X2 to ground (Load capacitor value depends on crystal used). If external oscillator is connected to X1/OSC, leave X2 floating.
17	XRES	XRES	Output Reference Resistor. Connect a 402Ω ±1% resistor between XRES and ground.
22	PWDNB	PWDNB	Active-Low, Power-Down Input with Internal 1MΩ Pull-Down to Ground. Apply logic low to place device in power-down mode. Connect to V _{DDIO} /logic high for normal operation.
42	RSVD	RSVD	Reserved. Make no electrical connection to this pin.
POWER SUPPLIES (See Error! Reference source not found. 2 and Table 3)			
8, 50	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1V Core Supply. Connect the two CAP_VDD pins together based on design's recommendation.
18, 25, 43	V _{DD18}	V _{DD18}	1.8V I/O Supply
21, 51	V _{DD}	V _{DD}	Core Supply. Connect 1.0V external power supply
28	V _{DDIO}	V _{DDIO}	1.8-3.3V I/O Power Supply

Functional Diagrams



* Available only in parts that support HDCP.

** Available only in parts that support DSC.

*** Available only in parts that support SGMII.

DCIO is optional. Refer to the Selection Guide for part options.

Recommended Operating Conditions

Table 2. Recommended Operating Conditions

PARAMETER	PIN NAME	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V _{DD18}		1.7	1.8	1.9	V
	V _{DD}		0.95	1.00	1.05	V
	V _{DDIO}	1.8V	1.7	1.8		V
		3.3V		3.3	3.6	V
Maximum Supply Noise Supply Noise < 1MHz	V _{DD18}			25		mVp-p
	V _{DD}			25		mVp-p
	V _{DDIO}	1.8V		50		mVp-p
		3.3V		100		mVp-p
Operating Junction Temperature, T _J			-40		+125	°C

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External Component Requirements

Table 3. External Component Requirements

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
XRES	R _{XRES}	Connect to pin 17.	402 ±1%. Use a single resistor	Ω
Crystal		Place as close as possible to pins 15 and 16.	25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values which compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible to pins 15 (X1/OSC) and 16 (X2).	Application specific	
Link Isolation Capacitors	C _{LINK}	Place close to the SIO (19, 20, 23, 24) and DCIO pins (9, 10) used in the application.	0.1	μF
Coax Mode Termination Resistor	R _{TERM}	In coax mode, connect R _{TERM} between unused SIO (20, 23) and DCIO (9) pin and ground on each coax link.	49.9 ±1%	Ω
SIO Line Fault Pull-Down Resistor	R _{PD}	Install at each used pin (19, 20, 23, 24) if attached Serializer is using the Line Fault Monitor.	49.9 ±1%	kΩ
DCIO Line Fault Resistor – Coax Mode	R _{EXT1}	LMN0 or LMN1	48.7 ±1%	kΩ
	R _{EXT2}		DNI	
DCIO Line Fault Resistor – STP Mode	R _{EXT1}		48.7 ±1%	kΩ
	R _{EXT2}		42.2 ±1%	kΩ
V _{DD} Decoupling Capacitors*		Place 0.1μF capacitors as close as possible to V _{DD} pins 21 and 51. Include a minimum of 10μF bulk decoupling on the PCB.	(2x) 0.1 + 10	μF
CAP_VDD Decoupling Capacitors		Place 0.1μF capacitors as close as possible to CAP_VDD pins 8 and 50. Include a 10μF capacitor on the PCB.	(2x) 0.1 + 10	μF
V _{DD18} Decoupling Capacitors*		Place 0.01μF and 0.01μF capacitors as close as possible to V _{DD18} pins 18, 25, and 43. Include a minimum of 10μF bulk decoupling on the PCB.	(3x) 0.01 + (3x) 0.1 + 10	μF
V _{DDIO} Decoupling Capacitors*		Place 0.1μF and 0.01μF capacitors as close as possible to V _{DDIO} pin 28. Include a minimum of 10μF bulk decoupling on the PCB.	0.01 + 0.1 + 10	μF
eDP Source Isolation Capacitors	C _{TX}	Two required per lane.	75–265	nF
eDP Sink Isolation Capacitors	C _{RX}	Optional. Two required per lane if used.	75–265	nF
eDP Pull-Down Resistors	R _{EPD}	Required only if C _{RX} are used. Two required per lane if used.	100k–1M	Ω
eDP AUX Isolation Capacitors	C _{AUX}	Two required.	75–200	nF

PRELIMINARY

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
Open-Drain Pull-Up Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations.	Application specific	

* With exception of CAP_VDD, power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

Detailed Description

Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews and register definitions. Designers must also have the following information to correctly design using this device:

- The GMSL3/GMSL2 Channel Specifications contains physical layer requirements for the PCB traces, cables and connectors that constitute the GMSL2 link.
- The GMSL3/GMSL2 Hardware Design Guides contains recommendations for PCB design, applications circuits, selection of external components and guidelines for use of GMSL2 signal integrity tools.
- The GMSL3/GMSL2 User Guides contains detailed programming guidelines for GMSL2 device features.
- Errata sheets contain deviations from published device specifications, and are specific to part number and revision ID.

Contact the factory to receive these documents, and for additional guidance on MAX96860/MAX96862/MAX96864 features.

Introduction

Analog Devices' GMSL3/2 serializers and deserializers provide sophisticated link management for high-speed, low bit error rate, serial data transport. They support a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL2 provides up to 6Gbps forward and 187.5Mbps reverse packetized NRZ data transmission over each fixed-speed link. Devices with two GMSL2 links provide a total capacity of up to 12Gbps and 3Gbps reverse in specific configurations.

GMSL3 provides 12Gbps forward and 187.5Mbps reverse packetized PAM4 data transmission over each fixed-speed link. Devices with two GMSL2 links provide a total capacity of up to 24Gbps and 375Mbps reverse.

The following sections provide a brief overview of the device functions and features. Contact the factory for additional information and details on the configuration of each function and feature.

Product Overview

Other Functions

GMSL2 and GMSL3 serializers and deserializers have a main I²C/UART control channel interface that an ECU uses to access serializer and deserializer registers, as well as peripheral devices, from either end of the link. Each device also has 2 pass-through I²C/UART channels available for local or remote peripheral control. The pass-through I²C/UART channels do not have access to serializer and deserializer registers.

The MAX96860/MAX96862/MAX96864 support a single forward (serializer to deserializer) audio channel. It supports I²S stereo and up to 8 channels in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 bits to 32 bits. Product variants with daisy-chain capability support an additional, bidirectional audio channel with the same specifications.

The MAX96860/MAX96862/MAX96864 include an SPI interface for peripheral control. The SPI interface enables a host on one side of the GMSL link to control a peripheral on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL devices (a GMSL device can be configured as an SPI host or peripheral).

The MAX96860/MAX96862/MAX96864 provide up to 25 multifunction pins (MFPs). Multiple functions are assigned to each pin, including pass-through I²C/UART, SPI, SGMII, Audio, and monitoring signals, and GPIOs. GPIOs are typically used to tunnel low speed (< 100kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward or reverse direction. See the Pin Descriptions, MFP section for more information.

PRELIMINARY

Deserializer Operating Modes

The serializers in the following use cases do not show the entire suite of capabilities. Contact the factory for information on all serializer capabilities.

Single Link Without Compression

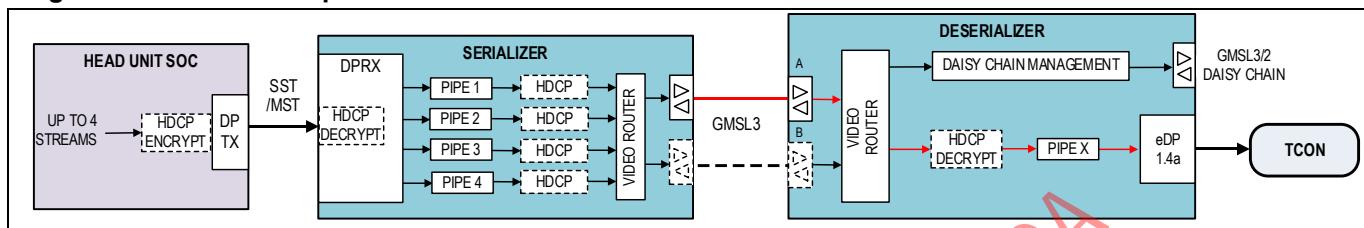


Figure 1.

A video stream of up to approximately 410MHz PCLK (24-bit color depth) or 330MHz (30-bit color depth) can be transported over a single GMSL3 link and locally output. Up to 215MHz PCLK (24-bit color depth only) can be transported over a single GMSL2 link. Deserializer GMSL Link A must be used. Video Pipe X is used in the deserializer. Excess bandwidth on this link, or on Link B (MAX96860/MAX96864 only), can be routed to the daisy-chain output.

Legacy GMSL2 Dual-Link Mode

MAX96860/MAX96864 support even/odd pixel mode, in which even and odd pixels are separated into 2 sub-streams by the serializer and routed over 2 GMSL links. They do not support legacy GMSL2 dual-link mode, in which video packets of a single video stream are routed over 2 links to divide the bandwidth loading.

Even/Odd Pixel Splitter Mode (MAX96860/MAX96864 only)

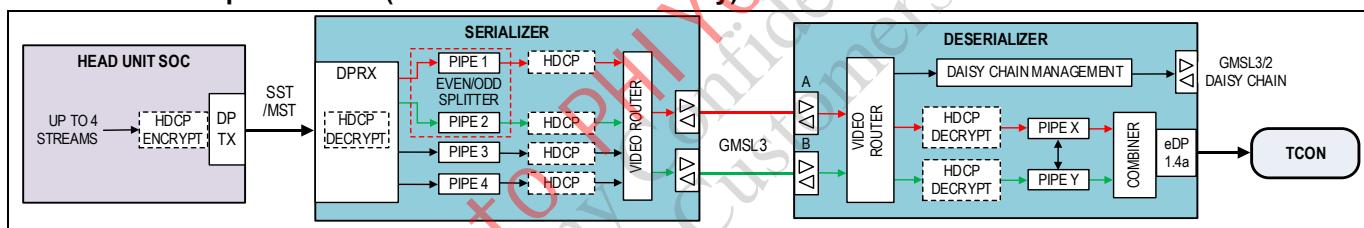


Figure 2.

A video stream of up to approximately 820MHz PCLK (24-bit color depth) or 660MHz (30-bit) can be split by the serializer into even- and odd-pixel substreams, transported over two GMSL links, and recombined by the MAX96860/MAX96864. Even/odd pixel splitter mode can only be used with an uncompressed video stream. The even pixel stream must be input on GMSL SIOA and the odd stream on SIOB. The definition of even and odd is such that the first pixel in a line is 0 and the second pixel is 1.

Up to 2 other video streams can be daisy-chained.

Compressed Video (MAX96862/MAX96864 only)

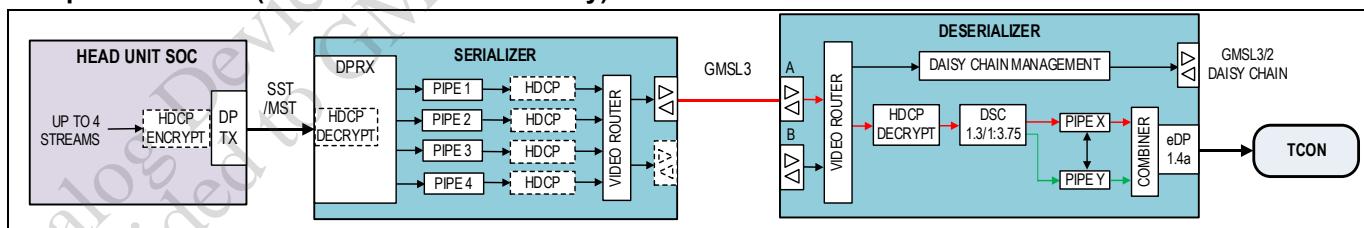


Figure 3.

A single video stream of up to 1080MHz PCLK (24bpp) or 864MHz (30bpp) can be output by the deserializer. The stream is compressed by the SOC using DSC 3:1 for 24-bit video and 3.75:1 for 30-bit video. The stream is decompressed by the deserializer. Deserializer GMSL Link A must be used. It can be configured as GMSL2 or GMSL3. Excess bandwidth on the link, or Link B (MAX96860/MAX96864 only), can be routed to the daisy-chain output. The other streams can be compressed or uncompressed.

Compressed Video with Parallel Deserializers (MAX96862/MAX96864 only)

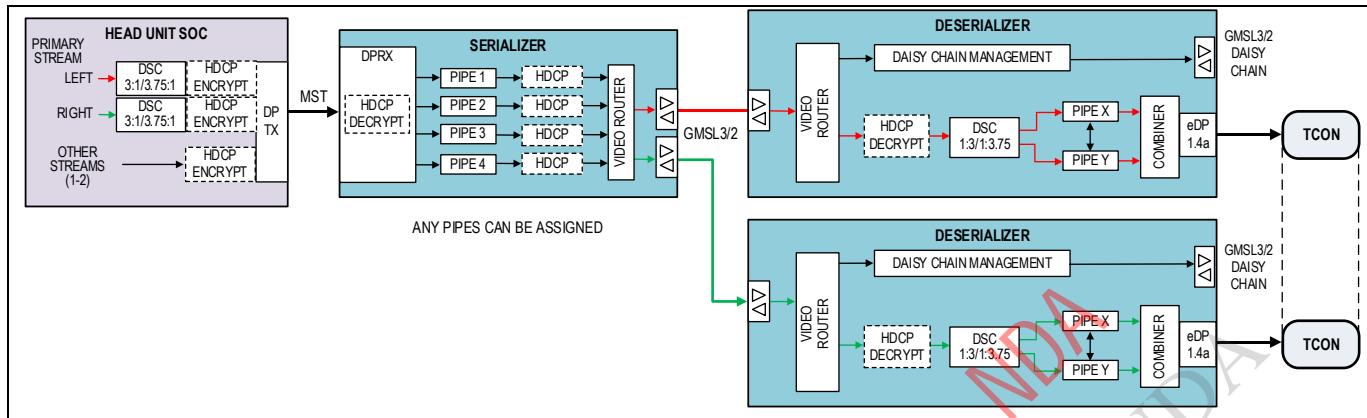


Figure 4.

Using a single serializer, the MAX96862/MAX96864 support up to approximately 2160MHz PCLK using compression, GMSL3, and paralleled deserializers. The limiting constraint is eDP output bandwidth. Separate substreams are compressed in the head unit SOC and are routed separately in the serializer and deserializers. Physically separate deserializers and TCONs may be used to shorten the trace lengths from the TCONs to the panels. Alternatively, the deserializers can be co-located to drive a single 2-port TCON. Up to 2 other video streams can be daisy-chained, either both from the same deserializer or one from each deserializer.

Daisy-Chaining

Daisy-Chaining Compressed Video with Daisy-Chained Deserializer (MAX96862/MAX96864 only)

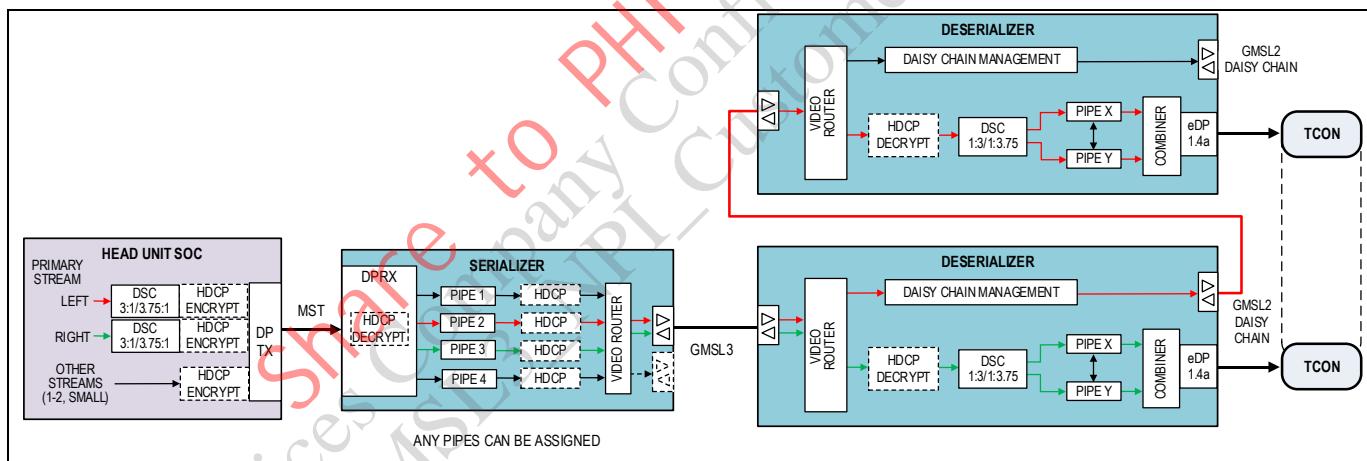


Figure 5.

To support ultra-high resolution displays, two MAX96862/MAX96864 deserializers can be daisy-chained. The advantages are that only one cable is needed between the head unit and display, with one less connector on the head unit.

The limiting constraint is the bandwidth of the GMSL3 link between the serializer and the first deserializer. This limits maximum total PCLK to approximately 1230MHz. Up to 2 other video streams can be daisy-chained from the second deserializer.

PRELIMINARY

Daisy Chained Deserializer(s) Between Serializer and MAX96860/MAX96864

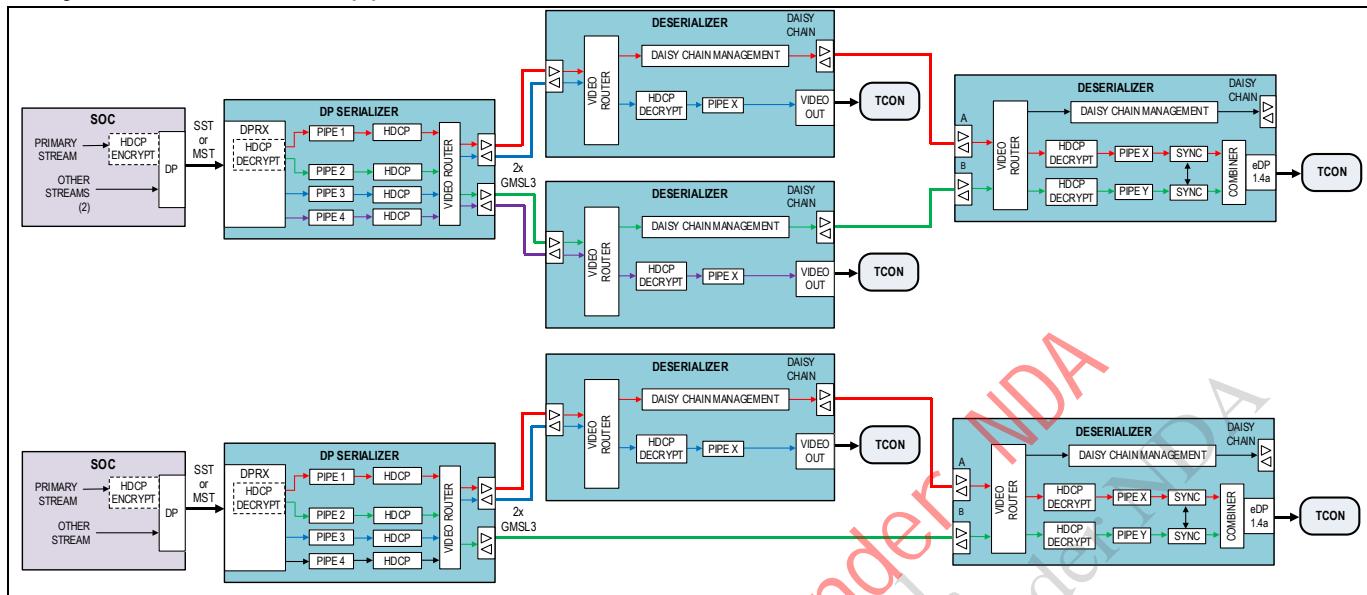


Figure 6.

When in even/odd pixel splitter mode, MAX96860/MAX96864 will support inline daisy-chain deserializers in both GMSL links, or a single daisy-chain deserializer in just one link. If only one link includes an in-line deserializer, it must be in Link A (input to the MAX96860/MAX96864 on SIOA). If even-odd pixel splitter mode is not used, then a single in-line deserializer may be inserted in either link.

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Daisy Chain of HDCP-Encrypted Video Streams (MAX96862/MAX96864)

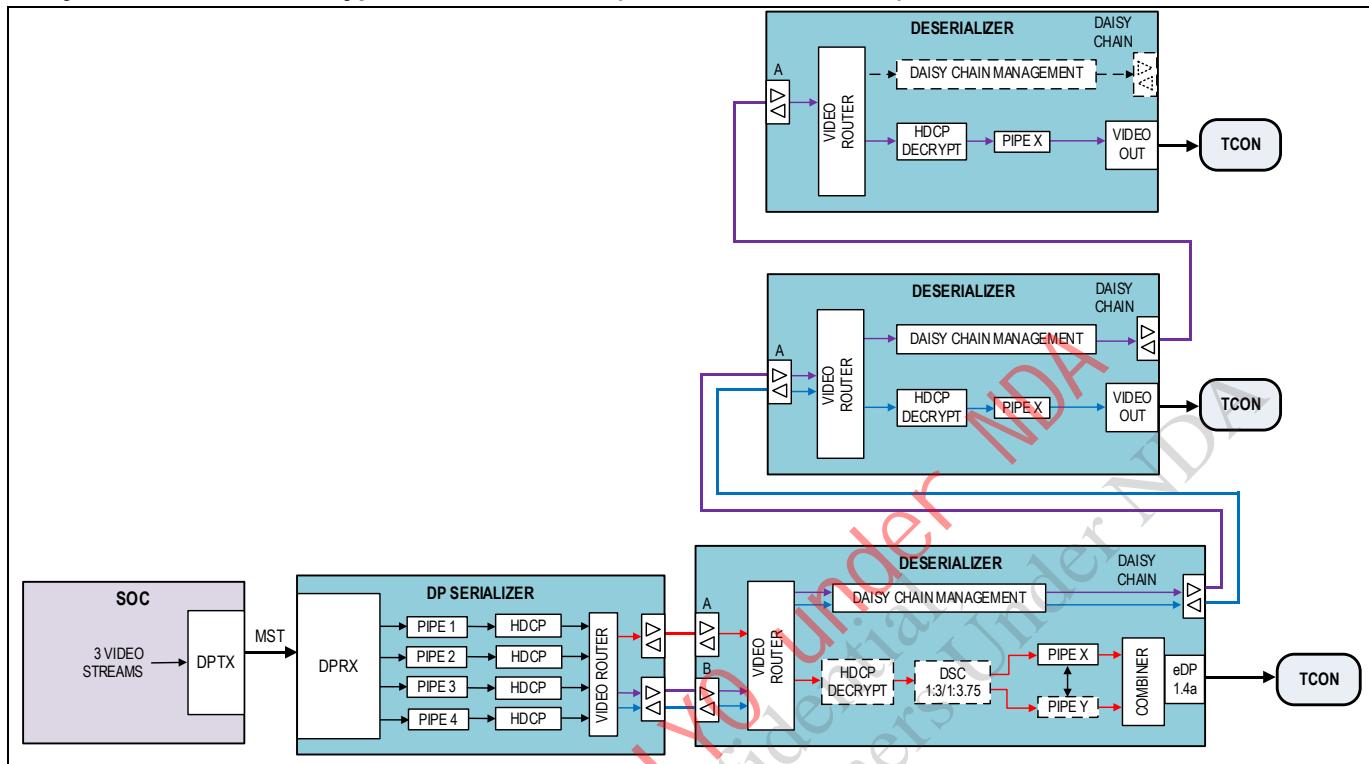


Figure 7.

If 2 video streams with HDCP encryption are daisy-chained from MAX96860/MAX96864, they must route from the serializer to the MAX96860/MAX96864 on the same GMSL link, i.e., both streams must be input on the same SIO port of MAX96860/MAX96864. The exception to this rule is if the second-rank deserializer is a MAX96860/MAX96862/MAX96864, then the 2 HDCP-encrypted streams can arrive from the serializer on different GMSL links.

Selection Guide

PART NUMBER	DSC	DAISY CHAIN/ END POINT	SGMII	GMSL Input	HDCP
MAX96860AS	No	Daisy Chain	No	2xGMSL3	Yes
MAX96862RS	Yes	Daisy Chain	No	1xGMSL3	Yes
MAX96864AS	Yes	Daisy Chain	Yes	2xGMSL3	Yes

CFG[1:0] Pins

The CFG[1:0] pins are used to set initial register values and functional modes of the device at power-up. At power-up, the voltage levels at the CFG[1:0] input pins are latched. The decoded levels set initial register values and functional modes that might not be easily programmed through I²C or UART after the IC powers up. The configuration tables provide the exact details on how to choose resistor values for the CFG[1:0] pins.

The CFG[1:0] pins are shared with MFP pins. The chip does not drive the pin before the pin levels are latched. Connect a properly valued precision resistor network (according to the needed setting) to each CFG pin. Use the MFP pins (which double function as CFG pins) only as outputs after power-up.

See [Table 4](#).

Table 4. CFG[1:0] Pin Configuration Table

CFG[1:0] INPUT VOLTAGE (PERCENTAGE OF V _{DDIO}) (NOTES A, B)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (NOTE C)		CFG0 MAPPED CONFIGURATION (NOTE D)			CFG1 MAPPED CONFIGURATION (NOTE E)		
MIN	TYP	MAX	R1 (Ω)	R1 (Ω)	DCIO OUTPUT RATE	DEVICE ADDRESS	GMSL STREAM ID	I ² CSEL	CXTP	SIO INPUT RATE
0.0%	0.0%	11.7%	OPEN	10,000	12G PAM4	0x90	0	I ² C	Coax	12G PAM4
16.9%	20.2%	23.6%	80,600	20,500		0x94	1			6G NRZ
28.8%	32.1%	35.5%	68,100	32,400		0x98	2		STP	12G PAM4
40.7%	44.0%	47.4%	56,200	44,200		0xD0	3			6G NRZ
52.6%	56.0%	59.3%	44,200	56,200	6G NRZ	0xD4	0	UART	Coax	12G PAM4
64.5%	67.9%	71.2%	32,400	68,100		0xD8	1			6G NRZ
76.4%	79.8%	83.1%	20,500	80,600		0x50	2	STP	12G PAM4	12G PAM4
88.3%	100%	100%	10,000	OPEN		0x54	3			6G NRZ

Notes:

- A. Resistor divider tolerance, V_{DDIO} supply ripple, and external loading must not cause CFG[1:0] input voltage to exceed the maximum or minimum limits.
- B. Other than the CFG[1:0] input resistor divider, any load on CFG[1:0] must be $\geq 25 \times (R1 + R2)$.
- C. Each resistor in the voltage divider must be $\leq 100\text{k}\Omega$.
- D. DCIO OUTPUT RATE: GMSL daisy-chain output link rate
 - DEVICE ADDRESS: Device I²C/UART address
 - GMSL STREAM ID: Default GMSL stream ID associated with device address
- E. I²CSEL: I²C or UART interface for SDA_RX and SCL_TX
- CXTP: Shielded-Twisted-Pair/Coax mode serial link
- SIO INPUT RATE: Forward channel serial rate in bits-per-second

Power Supplies

V_{DD} is the digital supply and should be connected to a 1.0V external power supply. V_{DD18} is the analog supply and should be connected to a 1.8V external power supply. Supplies should comply with the supply minimums, maximums and noise specifications defined in [Table 2](#).

Proper power supply bypassing of all supplies is essential for high-frequency circuit stability. See [Table 3](#). Contact factory for guidance on sharing supplies and optimizing supply decoupling.

Power supply ramp-time recommendation: 20μs < ramp time < 2ms. Power supply ramps should be monotonic. Once the supply voltage has reached the minimum supply voltage limit, it should not be allowed to drop below the specification.

Maxim/Analog Devices provides power management ICs (PMICs) optimized for supporting serial link devices. Contact factory for information.

Thermal Management

Power consumption of GMSL2 devices varies depending on the device configuration. Care must be taken by the user to provide sufficient heat dissipation with proper board and cooling design techniques. The package exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below 125°C to meet electrical specifications and avoid impacting device reliability.

Refer to [Tutorial 4083, Thermal Characterization of IC Packages](#) for guidance.

PRELIMINARY

Embedded DisplayPort (eDP) Output

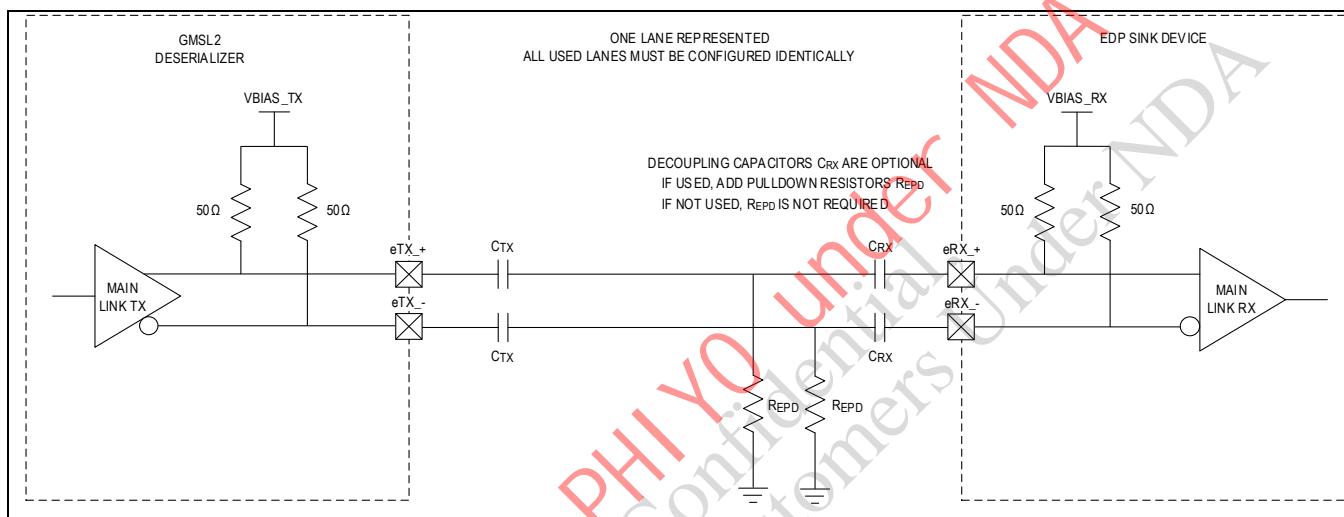
Overview

The MAX96860/MAX96862/MAX96864 provide a subset of eDP features specifically to drive single displays in automotive applications. Only single-stream transport (SST) mode is supported. Hot-plug detect (HPD) functionality is supported. For detailed information about eDP and DP, refer to the VESA Embedded DisplayPort (eDP) Standard and the VESA DisplayPort (DP) Standard.

eDP Transmitter

The eDP transmitter sources isochronous data with 8b/10b encoding on 1, 2, or 4 lanes. It supports per-lane data rates over the range of 1.62Gbps to 8.1Gbps.

Spread-spectrum clocking (SSC) can optionally be used to reduce radiated EMI. The drivers include internal 100Ω differential source termination. The transmitter includes a disable feature.

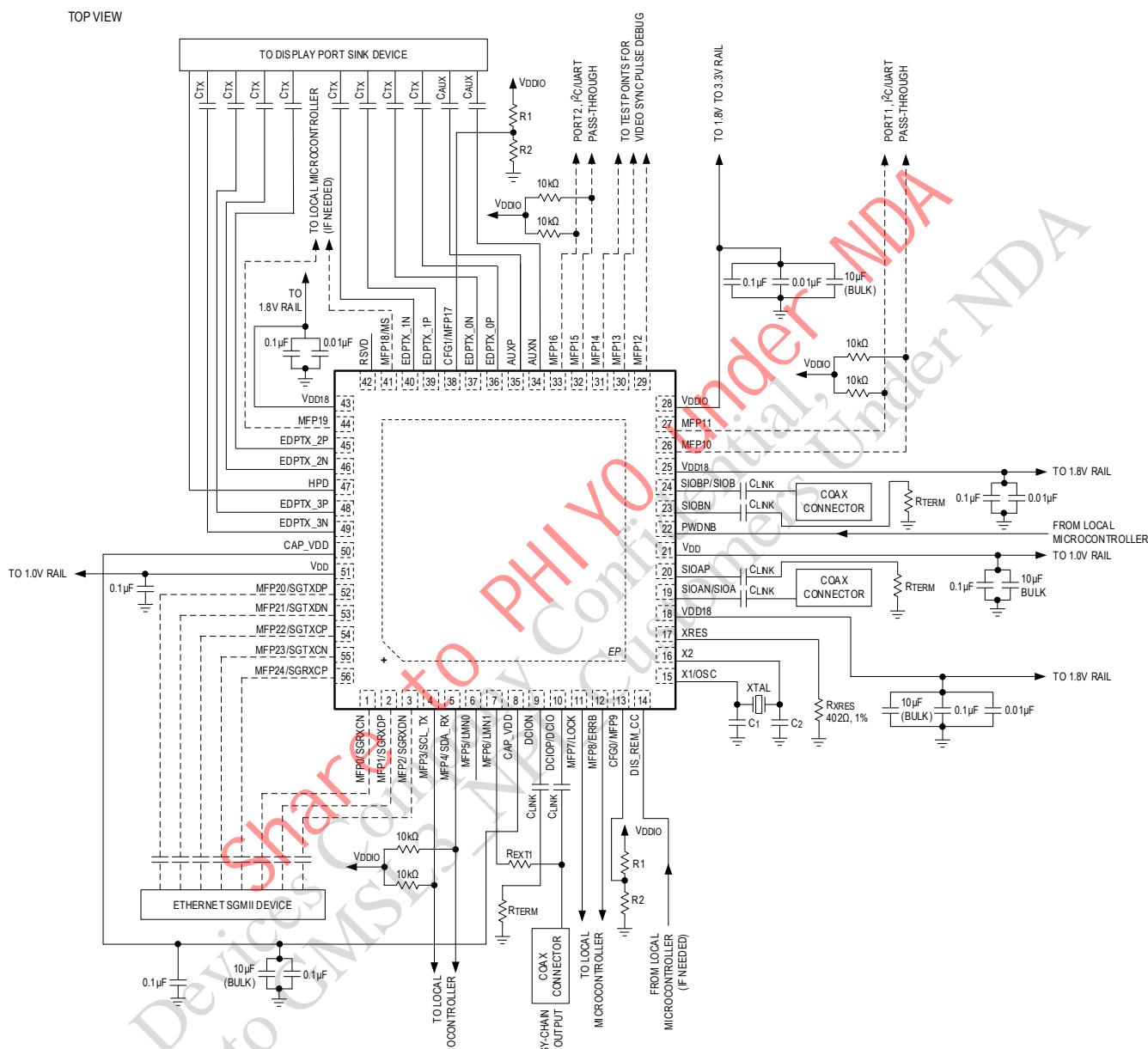


PRELIMINARY

Typical Application Circuits

Application Circuit (Coax)

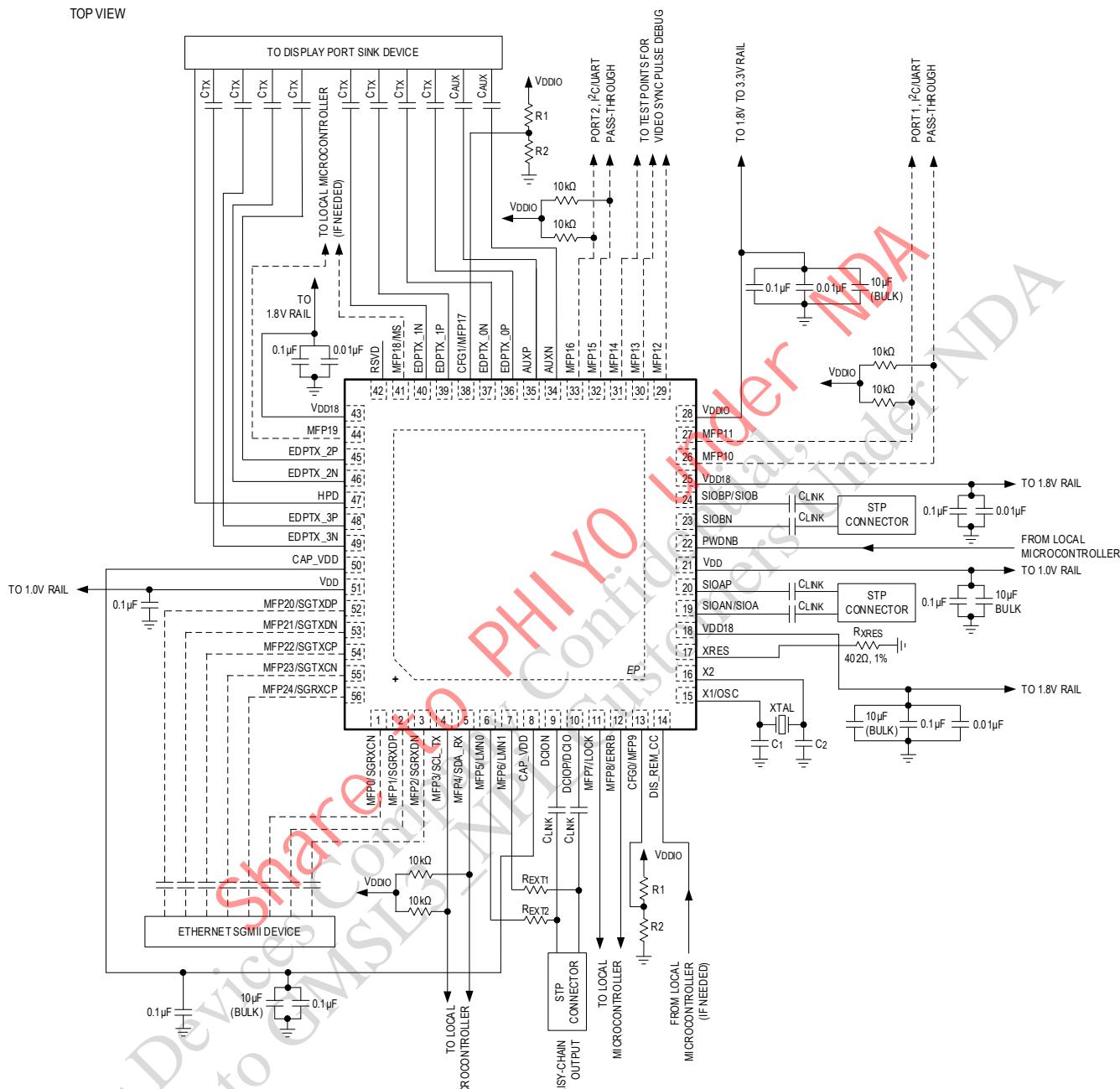
See [Table 3](#) for additional information.



PRELIMINARY

Application Circuit (STP)

See [Table 3](#) for additional information.



PRELIMINARY

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	DSC	DAISY CHAIN	GMSL INPUTS	SGMII	HDCP
MAX96860ASGTN/V+*	-40°C to +105°C	56-lead TQFN-EP	No	Yes	2xGMSL3	No	Yes**
MAX96860ASGTN/V+T*	-40°C to +105°C	56-lead TQFN-EP					
MAX96860ASGTN/VY+*	-40°C to +105°C	56-lead SW TQFN-EP					
MAX96860ASGTN/VY+T*	-40°C to +105°C	56-lead SW TQFN-EP					
MAX96862RSGTN/V+*	-40°C to +105°C	56-lead TQFN-EP	Yes	Yes	1xGMSL3	No	Yes**
MAX96862RSGTN/V+T*	-40°C to +105°C	56-lead TQFN-EP					
MAX96862RSGTN/VY+*	-40°C to +105°C	56-lead SW TQFN-EP					
MAX96862RSGTN/VY+T*	-40°C to +105°C	56-lead SW TQFN-EP					
MAX96864ASGTN/V+*	-40°C to +105°C	56-lead TQFN-EP	Yes	Yes	2xGMSL3	Yes	Yes**
MAX96864ASGTN/V+T*	-40°C to +105°C	56-lead TQFN-EP					
MAX96864ASGTN/VY+*	-40°C to +105°C	56-lead SW TQFN-EP					
MAX96864ASGTN/VY+T*	-40°C to +105°C	56-lead SW TQFN-EP					

/V Denotes an automotive qualified part

+ Denotes a lead(Pb)-free/RoHS-compliant package

T Denotes tape and reel

Y Denotes Side-Wettable package

EP Denotes Exposed Pad

**HDCP parts require registration with Digital Content Protection, LLC

*Future product—contact factory for availability.

PRELIMINARY

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Register Map

Reserved and Unused Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write).

In this document, default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

HDCP Register Blocks

BLOCK NAME		REGISTER ADDRESS RANGE							
HDCP_STATUS		0x90							
HDCP_CFG		0x1C7 - 0x1CA							

Note: * Indicates that the register is stored when entering sleep mode and is restored upon exit from sleep mode.

A D D R E S S	R E S E T	NAME	MSB							LSB
DEV_CFG										
0x00	0x90	<u>DEV_CFG_0[7:0]</u>								
0x01	0x00	<u>DEV_CFG_1[7:0]</u>	RESET_AL_L	RESET_LIN_K_ALL	RESET_LINK_SIOAB	RESET_LINK_SIOA	-	RESET_LIN_K_DCIO	-	-
0x02	0x00	<u>DEV_CFG_2[7:0]</u>	RESET_ONESHOT_AL_L	RESET_ONESHOT_SI_OAB	RESET_ONESHOT_SIOA	RESET_ONESHOT_SIOB	RESET_ONESHOT_DCIO	-	-	-
ERR_STATUS										
0x04	0x00	<u>ERROR_STA_TUS[0:7]</u>	ERR_OUTPUT_STATUS	LINK_SIOA_ERR	LINK_SIOB_ERR	LINK_DCIO_ERR	-	-	-	PSM_STAT_E_ERR

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x 05	0 x 0 0	<u>ERROR STA TUS 1[7:0]</u>	SIOA_FEC _ERR	SIOB_FEC _ERR	RETENTION_ MEMORY_C RC_ERR	CONTROL_C HANNEL_MS G_COUNT_E RR	-	LINEFAULT _0_ERR	LINEFAULT_ 1_ERR	CLOCK_MO NITOR_ER R
0x 06	0 x 0 0	<u>ERROR STA TUS 2[7:0]</u>	REMOTE_ ERR	ARQ_ERR	INFOFRAME _CRC_ERR	VIDEO_PRB S_ERR	AUDIO_PR BS_ERR	OVERROLT AGE_ERR	UNDERVOL TAGE_ERR	-
0x 07	0 x 0 0	<u>ERROR STA TUS 3[7:0]</u>	VIDEO_SE QUENCE_ ERR	LOSS_OF_ VIDEO_LO CK_ERR	HDCP_ERR	REGISTER_ CRC_ERR	DSC_ERR	WATERMA RK_ERR	VIDEO_BLO CK_LENGTH _ERR	-
0x 08	0 x 0 0	<u>ERROR STA TUS 4[7:0]</u>	FRAME_C RC_ERR	FEEDFOR WARD_CR C_ERR	FEEDFORWA RD_COMBIN ED_FRAME_ CRC_ERR	LINE_CRC_E RR	VIDEO_PA CKET_CRC _ERR	-	-	-
0x 09	0 x 0 0	<u>ERROR STA TUS 5[7:0]</u>	DP_INPUT _FIFO_CR C_ERR	WM_BYPA SS_ERR	LUT_FRC_E RR	DPTX_FIFO_ OVERFLOW _ERR	REGIONAL_ COLOR_E RR	LOSS_OF_L OCK_ERR	SGMII_ERR	CONTROL_ CHANNEL_ CRC_ERR
0x 0A	0 x 0 0	<u>ERROR STA TUS 6[7:0]</u>	OTP_CRC_ ERR	-	VIDEO_CFG_ ERR	DP_LINK_T AINING_ERR	DP_SINK_ CAPABILIT Y_ERR	AUX_ERR	HPD IRQ_E RR	HPD_DISC ONNECT_E RR
DEV_INFO										
0x 0D	0 x F F	<u>DEV_INFO_0[7:0]</u>	DEV_ID[7:0]							
0x 0E	0 x 0 0	<u>DEV_INFO_1[7:0]</u>	DEV_REV[3:0]				-	-	-	-
0x 0F	0 x	<u>DEV_INFO_2[7:0]</u>	SPEED_CPBL[1:0]	SGMII_CPBL	DSC_CPBL	SIOB_CPB L	DAISYCHAI N_CPBL	GMSL_12G_ CPBL	HDCP_CPB L	

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	3 F									
0x 11	0 x 0 1	<u>DEV_INFO_4[7:0]</u>								OTP_REV[7:0]
0x 24	0 x C 3	<u>DEV_ID16_L SB[7:0]</u>								DEV_ID16_BYTE_0[7:0]
0x 25	0 x 0 0	<u>DEV_ID16_M SB[7:0]</u>								DEV_ID16_BYTE_1[7:0]
LINK_STATUS										
0x 30	0 x 0 0	<u>LINK_STATU S_0[7:0]</u>	LOCKED_S IOA	LOCKED_S IOB	LOCKED_DC I_O	-	-	FEC_STAT US_SIOA	FEC_STATU S_SIOB	FEC_STAT US_DCIO
0x 31	0 x 0 0	<u>LINK_STATU S_1[7:0]</u>								DEC_ERROR_COUNT_SIOA[7:0]
0x 32	0 x 0 0	<u>LINK_STATU S_2[7:0]</u>								DEC_ERROR_COUNT_SIOP[7:0]
0x 33	0 x 0 0	<u>LINK_STATU S_3[7:0]</u>								DEC_ERROR_COUNT_DCIO[7:0]
FEC_STATUS										
0x 37	0 x 0 0	<u>FEC_STATU S_0[7:0]</u>								FEC_UNCORRECTABLE_ERRORS_SIOA[7:0]

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 38	0 x 0 0	<u>FEC_STATU S_1[7:0]</u>								FEC_UNCORRECTABLE_ERRORS_SIOB[7:0]
0x 39	0 x 0 0	<u>FEC_STATU S_2[7:0]</u>								FEC_BLOCKS_PROCESSED_SIOA_BYTE_0[7:0]
0x 3A	0 x 0 0	<u>FEC_STATU S_3[7:0]</u>								FEC_BLOCKS_PROCESSED_SIOA_BYTE_1[7:0]
0x 3B	0 x 0 0	<u>FEC_STATU S_4[7:0]</u>								FEC_BLOCKS_PROCESSED_SIOA_BYTE_2[7:0]
0x 3C	0 x 0 0	<u>FEC_STATU S_5[7:0]</u>								FEC_BLOCKS_PROCESSED_SIOA_BYTE_3[7:0]
0x 3D	0 x 0 0	<u>FEC_STATU S_6[7:0]</u>								FEC_BLOCKS_PROCESSED_SIOB_BYTE_0[7:0]
0x 3E	0 x 0 0	<u>FEC_STATU S_7[7:0]</u>								FEC_BLOCKS_PROCESSED_SIOB_BYTE_1[7:0]
0x 3F	0 x 0 0	<u>FEC_STATU S_8[7:0]</u>								FEC_BLOCKS_PROCESSED_SIOB_BYTE_2[7:0]
0x 40	0 x 0 0	<u>FEC_STATU S_9[7:0]</u>								FEC_BLOCKS_PROCESSED_SIOB_BYTE_3[7:0]
0x 41	0 x	<u>FEC_STATU S_10[7:0]</u>								FEC_CORRECTED_ERRORS_SIOA_BYTE_0[7:0]

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x 42	0 x 0 0	<u>FEC_STATU S_11[7:0]</u>								FEC_Corrected_Error_SIOA_BYTE_1[7:0]
0x 43	0 x 0 0	<u>FEC_STATU S_12[7:0]</u>								FEC_Corrected_Error_SIOA_BYTE_2[7:0]
0x 44	0 x 0 0	<u>FEC_STATU S_13[7:0]</u>								FEC_Corrected_Error_SIOB_BYTE_0[7:0]
0x 45	0 x 0 0	<u>FEC_STATU S_14[7:0]</u>								FEC_Corrected_Error_SIOB_BYTE_1[7:0]
0x 46	0 x 0 0	<u>FEC_STATU S_15[7:0]</u>								FEC_Corrected_Error_SIOB_BYTE_2[7:0]
COMM_STATUS										
0x 48	0 x 0 0	<u>CC_STATUS _0[7:0]</u>	UART_TX_OV ERFLOW	UART_RX_OV ERFLOW	I2C_ACK RECEIVED	I2C_TIMED_OUT	-	-	-	-
0x 4A	0 x 0 0	<u>PT_STATUS _0[7:0]</u>	PT1_UART_TX_OV ERFLOW	PT1_UART_RX_OV ERFLOW	-	-	-	-	-	-
0x 4B	0 x 0 0	<u>PT_STATUS _1[7:0]</u>	PT2_UART_TX_OV ERFLOW	PT2_UART_RX_OV ERFLOW	-	-	-	-	-	-
0x 4D	0 x	<u>SPI_STATUS _0[7:0]</u>	SPI_TX_OVERFLOW	SPI_RX_OVERFLOW	-					SPI_BUFFER_LEVEL[4:0]

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x 4F	0 x 0 0	<u>SGMII_STAT</u> <u>US_0[7:0]</u>	SGMII_TX_ OVERFLO W	SGMII_RX_ OVERFLO W	SGMII_FRAM E_UNDERFL OW	SGMII_LINK_ STATUS	SGMII_DLL _LOCK	AUTONEGO TIATION_S TATUS	MDIO_READ _VALID	MDIO_BUS Y
0x 50	0 x 0 0	<u>SGMII_STAT</u> <u>US_1[7:0]</u>	-	-	-	-	SGMII_INT	SGMII_DEC _ERR_FLA G	SGMII_STO P_ERR	SGMII_PRB S_ERROR
0x 51	0 x 0 0	<u>SGMII_STAT</u> <u>US_2[7:0]</u>	SGMII_PRBS_ERROR_COUNT[7:0]							
0x 52	0 x 0 0	<u>SGMII_STAT</u> <u>US_3[7:0]</u>	SGMII_DEC_ERROR_COUNT[7:0]							
0x 54	0 x 0 0	<u>AUDIO_STAT</u> <u>US_0[7:0]</u>	-	-	-	-	AUDIO_LO CK	-	-	AUDIO_BLO CK_LENGTH H_ERROR
0x 55	0 x 0 0	<u>AUDIO_STAT</u> <u>US_1[7:0]</u>	AUDIO_RX_CLOCK_FREQUENCY[7:0]							
0x 58	0 x 0 0	<u>CFG_PIN_ST</u> <u>ATUS_0[7:0]</u>	-	CFG_PIN_0_VALUE[2:0]			-	CFG_PIN_1_VALUE[2:0]		
0x 59	0 x 0 0	<u>GPIO_STATU</u> <u>S_0[7:0]</u>	GPIO_VAL UE_7	GPIO_VAL UE_6	GPIO_VALUE _5	GPIO_VALU E_4	GPIO_VAL UE_3	GPIO_VALU E_2	GPIO_VALU E_1	GPIO_VALU E_0
0x 5A	0 x 0 0	<u>GPIO_STATU</u> <u>S_1[7:0]</u>	GPIO_VAL UE_15	GPIO_VAL UE_14	GPIO_VALUE _13	GPIO_VALU E_12	GPIO_VAL UE_11	GPIO_VALU E_10	GPIO_VALU E_9	GPIO_VALU E_8

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 5B	0 x 0 0	<u>GPIO_STATU S_2[7:0]</u>	GPIO_VAL UE_23	GPIO_VAL UE_22	GPIO_VALUE _21	GPIO_VALU E_20	GPIO_VAL UE_19	GPIO_VALU E_18	GPIO_VALU E_17	GPIO_VALU E_16
0x 5C	0 x 0 0	<u>GPIO_STATU S_3[7:0]</u>	-	-	-	-	-	-	-	GPIO_VALU E_24
CRC_STATUS										
0x 5E	0 x 0 0	<u>REGIONAL CRC STATU S_0[7:0]</u>	BANK_A_D ONE	BANK_B_D ONE	ACTIVE_A_O R_B	VA_DONE_S TATUS	-	-	-	-
0x 5F	0 x 0 0	<u>REGIONAL CRC STATU S_1[7:0]</u>	FRAME_COUNT_BYTE_0[7:0]							
0x 60	0 x 0 0	<u>REGIONAL CRC STATU S_2[7:0]</u>	-	-	-	-	-	-	-	FRAME_COUNT_BYTE_1[:0]
0x 61	0 x 0 0	<u>REGIONAL CRC STATU S_3[7:0]</u>	REGIONAL_CRC_A_BYTE_0[7:0]							
0x 62	0 x 0 0	<u>REGIONAL CRC STATU S_4[7:0]</u>	REGIONAL_CRC_A_BYTE_1[7:0]							
0x 63	0 x 0 0	<u>REGIONAL CRC STATU S_5[7:0]</u>	REGIONAL_CRC_A_BYTE_2[7:0]							
0x 64	0 x 0 0	<u>REGIONAL CRC STATU S_6[7:0]</u>	REGIONAL_CRC_A_BYTE_3[7:0]							

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 65	0 x 0 0	<u>REGIONAL_CRC_STATU S_7[7:0]</u>								REGIONAL_CRC_B_BYTE_0[7:0]
0x 66	0 x 0 0	<u>REGIONAL_CRC_STATU S_8[7:0]</u>								REGIONAL_CRC_B_BYTE_1[7:0]
0x 67	0 x 0 0	<u>REGIONAL_CRC_STATU S_9[7:0]</u>								REGIONAL_CRC_B_BYTE_2[7:0]
0x 68	0 x 0 0	<u>REGIONAL_CRC_STATU S_10[7:0]</u>								REGIONAL_CRC_B_BYTE_3[7:0]
REGIONAL_COLOR_STATUS										
0x 6D	0 x 0 0	<u>REGIONAL COLOR_DET ECTION STA TUS_0[7:0]</u>	REGIONAL _COLOR_E RR_0	REGIONAL _COLOR_E RR_1	REGIONAL_ COLOR_ERR _2	REGIONAL_ COLOR_ERR _3	-	-	-	-
CRC_MISC_STATUS										
0x 6E	0 x 0 0	<u>CRC_MISC STATUS_0[7: 0]</u>	WM_BYPA SS_ERRO R_X	WM_BYPA SS_ERROR Y	LUT_FRC_E RROR_X	LUT_FRC_E RROR_Y	FRAME_C RC_ERRO R_X	FRAME_CR C_ERROR_ Y	-	-
0x 6F	0 x 0 0	<u>CRC_MISC STATUS_1[7: 0]</u>	LINE_CRC _ERROR_X	LINE_CRC_ ERROR_Y	VIDEO_PACK ET_CRC_ER ROR_X	VIDEO_PAC KET_CRC_E RROR_Y	-	-	INFOFRAME _CRC_ERR OR_SIOB	INFOFRAM E_CRC_ER ROR_SIOA
MISC_STATUS										
0x 71	0 x 0 0	<u>ARQ_STATU S_0[7:0]</u>	MAX_RT_E RROR_INF OFRAME_ CC	MAX_RT_E RR_CC	MAX_RT_ER R_PT_1	MAX_RT_ER R_PT_2	MAX_RT_E RR_SPI	MAX_RT_E RR_GPIO	-	MAX_RT_E RR_HDCP

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 73	0 x 4 8	<u>LF_STATUS</u> <u>0[7:0]</u>	LINEFAULT_0_STATUS[2:0]			LINEFAULT_1_STATUS[2:0]			-	-
DP_STATUS										
0x 75	0 x 0 0	<u>DP_STATUS</u> <u>0[7:0]</u>	DP_OVERFL LOW	DP_UNDER FLOW	DP_INPUT_FI FO_OVERFL OW	DP_VBI_ERR OR	-	-	-	-
0x 76	0 x 0 0	<u>DP_STATUS</u> <u>1[7:0]</u>	-	-	-	-	LINK_RET RAINED	HPD_EVEN T_DETECT ED	HPD_IRQ_D ETECTED	HPD_CONN ECT_STAT E
0x 77	0 x 0 F	<u>DP_STATUS</u> <u>2[7:0]</u>	DPTX_VID EO_OUTP UT_ACTIV E	LINK_TRAI NING_PAS SED	LINK_TRAINI NG_FAILED	LINK_TRAINI NG_IN_PRO GRESS	LINK_TRAI NING_NOT STARTED	WAITING_F OR_VIDEO_ LOCK	WAITING_F OR_PSM_ST ATE	WAITING_F OR_HPD
0x 78	0 x 0 0	<u>DP_STATUS</u> <u>3[7:0]</u>	-	-	-	-	-	-	EDID_TRAN SFER_TO_S ER_DONE	SINK_EDID _READ_DO NE
0x 79	0 x 0 0	<u>DP_STATUS</u> <u>4[7:0]</u>	MAJOR_REV[3:0]				MINOR_REV[3:0]			
0x 7A	0 x 0 0	<u>DP_STATUS</u> <u>5[7:0]</u>	EXTENDED _CAPS_FIE LD	-	-	LOCAL_EDID _PRESENT	TPS4_SUP PORTED	TPS3_SUP PORTED	MAX_DOWN SPREAD	ENHANCED _FRAME_C AP
0x 7B	0 x 0 0	<u>DP_STATUS</u> <u>6[7:0]</u>	MAX_LINK_RATE[7:0]							
0x 7C	0 x 0 0	<u>DP_STATUS</u> <u>7[7:0]</u>	-	-	-	MAX_LANE_COUNT[4:0]				

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 7D	0 x 0 0	DP_STATUS _8[7:0]	-	TRAINING_AUX_RD_INTERVAL[6:0]						
0x 7E	0 x 0 0	DP_STATUS _9[7:0]		I2C_SPEED_CAP[7:0]						
0x 80	0 x 0 0	DP_STATUS _12[7:0]	-	LANE1_SY MBOL_LOC KED	LANE1_CHA NNEL_EQ_D ONE	LANE1_CR_ DONE	-	LANE0_SY MBOL_LOC KED	LANE0_CHA NNEL_EQ_D ONE	LANE0_CR_ DONE
0x 81	0 x 0 0	DP_STATUS _13[7:0]	-	LANE3_SY MBOL_LOC KED	LANE3_CHA NNEL_EQ_D ONE	LANE3_CR_ DONE	-	LANE2_SY MBOL_LOC KED	LANE2_CHA NNEL_EQ_D ONE	LANE2_CR_ DONE
0x 82	0 x 0 0	DP_STATUS _14[7:0]	LINK_STAT US_UPDAT ED	-	-	-	-	-	-	INTERLANE _ALIGN_DO NE
0x 83	0 x 0 0	DP_STATUS _15[7:0]	-	-	-	I2C_OVER_A UX_ERROR	AUX_NACK _ERROR	AUX_TIME OUT_ERRO R	AUX_RETRY _ERROR	AUX_DEFE R_ERROR
0x 84	0 x 0 0	DP_STATUS _16[7:0]	OTP_CRC_ ERROR_ST ATUS	-	VIDEO_CFG_ ERROR_STA TUS	-	-	DP_SINK_C HEQ_TPS_ CAPABILIT Y_ERROR	DP_SINK_LA NE_COUNT_ CAPABILIT Y_ERROR	DP_SINK_LI NK_RATE_ CAPABILIT Y_ERROR
0x 85	0 x 0 0	DP_STATUS _17[7:0]	-	-	-	-	DP_LINK_I NTERLANE _ALIGN_E RROR	DP_LINK_C HANNEL_E Q_ERROR	DP_LINK_SY MBOL_LOC K_ERROR	DP_LINK_C R_ERROR
WM_STATUS										
0x 88	0 x 0 0	WATERMAR K_STATUS_0 [7:0]	WM_ERRO R_LIVE	WM_DETE CT	-	-	-	-	-	-

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
DSC_STATUS										
0x 8A	0 0 0	<u>DSC_STATU S_0[7:0]</u>	DSC_OVE RFLOW	DSC_UNDE RFLOW	DSC_PARITY _ERROR	DSC_TRANS PORT_CHUN K_SIZE_ERR OR	DSC_MBIS T_ERROR	-	-	-
PRBS_STATUS										
0x 8C	0 0 0	<u>PRBS_STAT US_0[7:0]</u>	-	-	-	APRBS_VALI D	-	-	-	VPRBS_FA L
0x 8D	0 0 0	<u>PRBS_STAT US_1[7:0]</u>	VPRBS_ERROR_COUNT[7:0]							
0x 8E	0 0 0	<u>PRBS_STAT US_2[7:0]</u>	APRBS_ERROR_COUNT[7:0]							
HDCP_STATUS										
0x 90	0 0 0	<u>HDCP_STAT US_0[7:0]</u>	DECRIPTI ON_ON_X	DECRIPTI ON_ON_Y	HDCP_LINK INTEGRITY_ X	HDCP_LINK INTEGRITY_ Y	HDCP2_AU THENTICA TED_X	HDCP2_AU THENTICAT ED_Y	-	-
VIDEO_STATUS										
0x 92	0 0 0	<u>VIDEO_STAT US_0[7:0]</u>	-	-	VTRG_OVER FLOW_X	VTRG_UNDE RFLOW_X	VIDEO_ALI GN_OVER FLOW_X	VIDEO_SE QUENCE_E RROR_X	VIDEO_BLO CK_LENGTH _ERROR_X	LOSS_OF_ VIDEO_LOC K_X
0x 93	0 0 0	<u>VIDEO_STAT US_1[7:0]</u>	-	-	VTRG_OVER FLOW_Y	VTRG_UNDE RFLOW_Y	VIDEO_ALI GN_OVER FLOW_Y	VIDEO_SE QUENCE_E RROR_Y	VIDEO_BLO CK_LENGTH _ERROR_Y	LOSS_OF_ VIDEO_LOC K_Y
0x 94	0 0 0	<u>VIDEO_STAT US_2[7:0]</u>	VIDEO_PA CKETS_LO CK_Y	VIDEO_PA CKETS_LO CK_X	VIDEO_LOCK _Y	VIDEO_LOC K_X	ODD_EVE N_SPLIT_S TATUS	DETECTED _30_BPP	PPS PARA MS RECEIV ED	AUTO_TIMI NG RECEIV ED

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 95	0 x 0 0	<u>VIDEO_STAT</u> <u>US_3[7:0]</u>								RECEIVED_PCLK_FREQUENCY_BYTE_0[7:0]
0x 96	0 x 0 0	<u>VIDEO_STAT</u> <u>US_4[7:0]</u>								RECEIVED_PCLK_FREQUENCY_BYTE_1[7:0]
0x 97	0 x 0 0	<u>VIDEO_STAT</u> <u>US_5[7:0]</u>								RECEIVED_PCLK_FREQUENCY_BYTE_2[7:0]
0x 98	0 x 0 0	<u>VIDEO_STAT</u> <u>US_6[7:0]</u>								RECEIVED_H_ACTIVE_BYTE_0[7:0]
0x 99	0 x 0 0	<u>VIDEO_STAT</u> <u>US_7[7:0]</u>								RECEIVED_H_ACTIVE_BYTE_1[7:0]
0x 9A	0 x 0 0	<u>VIDEO_STAT</u> <u>US_8[7:0]</u>								RECEIVED_H_FP_BYTE_0[7:0]
0x 9B	0 x 0 0	<u>VIDEO_STAT</u> <u>US_9[7:0]</u>								RECEIVED_H_FP_BYTE_1[7:0]
0x 9C	0 x 0 0	<u>VIDEO_STAT</u> <u>US_10[7:0]</u>								RECEIVED_H_SW_BYTE_0[7:0]
0x 9D	0 x 0 0	<u>VIDEO_STAT</u> <u>US_11[7:0]</u>								RECEIVED_H_SW_BYTE_1[7:0]
0x 9E	0 x	<u>VIDEO_STAT</u> <u>US_12[7:0]</u>								RECEIVED_H_BP_BYTE_0[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x 9F	0 x 0 0	<u>VIDEO_STAT</u> <u>US 13[7:0]</u>			RECEIVED_H_BP_BYTE_1[7:0]					
0x A0	0 x 0 0	<u>VIDEO_STAT</u> <u>US 14[7:0]</u>			RECEIVED_V_ACTIVE_BYTE_0[7:0]					
0x A1	0 x 0 0	<u>VIDEO_STAT</u> <u>US 15[7:0]</u>			RECEIVED_V_ACTIVE_BYTE_1[7:0]					
0x A2	0 x 0 0	<u>VIDEO_STAT</u> <u>US 16[7:0]</u>			RECEIVED_V_FP[7:0]					
0x A3	0 x 0 0	<u>VIDEO_STAT</u> <u>US 17[7:0]</u>			RECEIVED_V_SW[7:0]					
0x A4	0 x 0 0	<u>VIDEO_STAT</u> <u>US 18[7:0]</u>			RECEIVED_V_BP[7:0]					
0x A5	0 x 0 0	<u>VIDEO_STAT</u> <u>US 19[7:0]</u>			DETECTED_PCLK_FREQUENCY_BYTE_0[7:0]					
0x A6	0 x 0 0	<u>VIDEO_STAT</u> <u>US 20[7:0]</u>			DETECTED_PCLK_FREQUENCY_BYTE_1[7:0]					
0x A7	0 x 0 0	<u>VIDEO_STAT</u> <u>US 21[7:0]</u>	-	-	-	-	DETECTED_PCLK_FREQUENCY_BYTE_2[3:0]			

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x A8	0 x 0 0	<u>VIDEO_STAT</u> <u>US 22[7:0]</u>								DETECTED_H_ACTIVE_BYTE_0[7:0]
0x A9	0 x 0 0	<u>VIDEO_STAT</u> <u>US 23[7:0]</u>								DETECTED_H_ACTIVE_BYTE_1[7:0]
0x AA	0 x 0 0	<u>VIDEO_STAT</u> <u>US 24[7:0]</u>								DETECTED_V_ACTIVE_BYTE_0[7:0]
0x AB	0 x 0 0	<u>VIDEO_STAT</u> <u>US 25[7:0]</u>								DETECTED_V_ACTIVE_BYTE_1[7:0]
0x AC	0 x 0 0	<u>VIDEO_STAT</u> <u>US 26[7:0]</u>	RECEIVED _HS_POLARITY	RECEIVED _VS_POLARITY	-	-	-	-	DETECTED_ _HS_POLARITY	DETECTED_ _VS_POLARITY
0x AD	0 x 0 0	<u>VIDEO_STAT</u> <u>US 27[7:0]</u>								RECEIVED_PPS_PIC_WIDTH_BYTE_0[7:0]
0x AE	0 x 0 0	<u>VIDEO_STAT</u> <u>US 28[7:0]</u>								RECEIVED_PPS_PIC_WIDTH_BYTE_1[7:0]
0x AF	0 x 0 0	<u>VIDEO_STAT</u> <u>US 29[7:0]</u>								RECEIVED_PPS_PIC_HEIGHT_BYTE_0[7:0]
0x B0	0 x 0 0	<u>VIDEO_STAT</u> <u>US 30[7:0]</u>								RECEIVED_PPS_PIC_HEIGHT_BYTE_1[7:0]
0x B1	0 x	<u>VIDEO_STAT</u> <u>US 31[7:0]</u>								RECEIVED_PPS_SLICE_WIDTH_BYTE_0[7:0]

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x B2	0 x 0 0	<u>VIDEO_STAT</u> <u>US_32[7:0]</u>			RECEIVED_PPS_SLICE_WIDTH_BYTE_1[7:0]					
0x B3	0 x 0 0	<u>VIDEO_STAT</u> <u>US_33[7:0]</u>			RECEIVED_PPS_SLICE_HEIGHT_BYTE_0[7:0]					
0x B4	0 x 0 0	<u>VIDEO_STAT</u> <u>US_34[7:0]</u>			RECEIVED_PPS_SLICE_HEIGHT_BYTE_1[7:0]					
PSM_STATE_STATUS										
0x B6	0 x 0 0	<u>PSM_STATE</u> <u>STATUS_0[7:0]</u>	-	PSM_ACCE SS_ERROR	PSM_STATE _TIMER_ERR OR	PSM_DATA_ _TIMER_ERR OR	-	-	PSM_START UP_MBIST_ FAILED	PSM_STAR TUP_MBIST _DONE
POWER_STATUS										
0x BA	0 x 0 0	<u>POWER_STA</u> <u>TUS_0[7:0]</u>	-	VDDIO_UN DERVOLTA GE_ERRO R	VDD18_UND ERVOLTAGE _ERROR	VDD_BIAS_U NDERVOLTA GE_ERROR	VDD_UND ERVOLTA GE_ERRO R	VDDIO_OV ERVOLTAG E_ERROR	VDD18_OVE RVOLTAGE_ ERROR	VDD_OVER VOLTAGE_ ERROR
ERR_LINK_CFG										
0x 10 3	0 x 0 0	<u>CFG_PIN_CF</u> <u>G_0[7:0]</u>	CFG_PIN_0 _OVR_EN	CFG_PIN_0_SET[2:0]			CFG_PIN_1 _OVR_EN	CFG_PIN_1_SET[2:0]		
LINK_CFG										
0x 10 5	0 x A 7	<u>LINK CFG_0[7:0]</u>	LINK_EN_S IOA	LINK_EN_S IOB	LINK_EN_DC IO	-	-	-	-	-

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 10 6	0 x 2 2	<u>LINK_CFG_1[7:0]</u>	CX_TP_SIO	-	GMSL3_MOD_E_SIO	GMSL_FEC_EN_SIO	RSVD[1:0]		RX_RATE_SIO[1:0]	
0x 10 7	0 x 3 8	<u>LINK_CFG_2[7:0]</u>	CX_TP_DCIO	-	GMSL3_MOD_E_DCIO	GMSL_FEC_EN_DCIO	TX_RATE_DCIO[1:0]	-	-	-
0x 10 8	0 x 0 0	<u>LINK_CFG_3[7:0]</u>	-	-	-	-	-	FEC_STATS_RESET_SI OA	FEC_STATS_RESET_SI OB	

ERRG_CFG

0x 10 A	0 x 0 0	<u>ERRG_CFG_0[7:0]</u>	ERRG_EN_SIOA	ERRG_EN_SIOB	ERRG_EN_DCIO	-	-	-	-	-
0x 10 B	0 x 0 8	<u>ERRG_CFG_1[7:0]</u>	ERRG_MO DE		ERRG_BURST[2:0]		ERRG_BER[1:0]		ERRG_COUNT[1:0]	

ERROR_CFG

0x 10 D	0 x F 1	<u>ERROR_CFG_0[7:0]</u>	ERRB_PIN_OUTPUT_EN	LINK_SIOA_ERR_OEN	LINK_SIOB_E RR_OEN	LINK_DCIO_ER R_OEN	-	-	-	PSM_STAT E_ERR_OE N
0x 10 E	0 x E 7	<u>ERROR_CFG_1[7:0]</u>	SIOA_FEC_ERR_OEN	SIQB_FEC_ERR_OEN	RETENTION_MEMORY_C RC_ERR_OE N	CONTROL_C HANNEL_MS G_COUNT_E RR_OEN	-	LINEFAULT_0_ERR_O EN	LINEFAULT_1_ERR_O EN	CLOCK_MONITOR_ER R_OEN
0x 10 F	0 x 7 E	<u>ERROR_CFG_2[7:0]</u>	REMOTE_ERR_OEN	ARQ_ERR_OEN	INFOFRAME_CRC_ERR_OEN	VIDEO_PRB_S_ERR_OEN	AUDIO_PRBS_ERR_O EN	OVERTVOLTAGE_ERR_O EN	UNDERVOLTAG E_ERR_OEN	-
0x 11 0	0 x	<u>ERROR_CFG_3[7:0]</u>	VIDEO_SEQUENCE_ERR_OEN	LOSS_OF_VIDEO_LO	HDCP_ERR_OEN	REG_CRC_E RR_OEN	DSC_ERR_O EN	WATERMARK_ERR_O EN	VIDEO_BLOCK_LENGTH_ERR_OEN	-

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB			
	C E			CK_ERR_O EN									
0x 11 1	0 x 9 8	<u>ERROR_CFG _4[7:0]</u>	FRAME_C RC_ERR_O EN	FEEDFOR WARD_FR AME_CRC_ ERR_OEN	COMBINED_ FRAME_CRC _ERR_OEN	LINE_CRC_E RR_OEN	VIDEO_PA CKET_CRC _ERR_OEN	-	-	-			
0x 11 2	0 x F 0	<u>ERROR_CFG _5[7:0]</u>	DP_INPUT _FIFO_CR C_ERR_OE N	WM_BYPA SS_ERR_O EN	LUT_FRC_E RR_OEN	DPTX_FIFO_ OVERFLOW _ERR_OEN	REGIONAL _COLOR_E RR_OEN	LOSS_OF_L OCK_OEN	SGMII_ERR_ OEN	CONTROL_ CHANNEL_ CRC_ERR_ OEN			
0x 11 3	0 x B F	<u>ERROR_CFG _6[7:0]</u>	OTP_CRC_ ERR_OEN	-	VIDEO_CFG_ ERR_OEN	DP_LINK_T RAINING_ERR _OEN	DP_SINK_ CAPABILIT Y_ERR_OE N	AUX_ERR_ OEN	HPD IRQ_E RR_OEN	HPD_DISC ONNECT_E RR_OEN			
CC_CFG													
0x 11 6	0 x 8 0	<u>CC_CFG_0[7: 0]</u>	CC_LOCAL _OUT_EN	DIS_Rem_ CC	I2CSEL	UART_BYPA SS_EN	-	-	CC_CRC_E N	CC_MESSA GE_COUNT _EN			
0x 11 7	0 x 2 0	<u>CC_CFG_1[7: 0]</u>	CC_LINK_ SEL	CC_PRIORITY[1:0]		-	-	-	-	-			
0x 11 8	0 x 2 D	<u>CC_CFG_2[7: 0]</u>	-	-	CC_I2C_SPEED_SLV[2:0]			CC_I2C_SPEED_MST[2:0]					
0x 11 9	0 x 0 0	<u>CC_CFG_3[7: 0]</u>	CC_I2C_TRANSLATION_0_SOURCE[6:0]							-			
0x 11 A	0 x 0 0	<u>CC_CFG_4[7: 0]</u>	CC_I2C_TRANSLATION_0_DESTINATION[6:0]							-			

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 11 B	0 x 0 0	<u>CC_CFG_5[7: 0]</u>								-
0x 11 C	0 x 0 0	<u>CC_CFG_6[7: 0]</u>								-
0x 11 D	0 x 0 0	<u>CC_CFG_7[7: 0]</u>	-	-	-	RESET_MSG CNTR	-	-	RESET_MS GCNTR_ER R_CNT	RESET_CC _CRC_ERR _CNT
PT_CFG										
0x 11 E	0 x 0 0	<u>PT_CFG_0[7: 0]</u>	PT1_EN	PT2_EN	PT1_I2CSEL	PT2_I2CSEL	PT1_LINK_SEL	PT2_LINK_SEL	PT1_MANUA L_MODE_EN	PT2_MANUA L_MODE_EN
0x 12 0	0 x D C	<u>PT_CFG_2[7: 0]</u>								PT1_UART_BIT_LENGTH_BYTE_0[7:0]
0x 12 1	0 x 0 5	<u>PT_CFG_3[7: 0]</u>	-	-						PT1_UART_BIT_LENGTH_BYTE_1[5:0]
0x 12 2	0 x 2 D	<u>PT_CFG_4[7: 0]</u>	-	-		PT1_I2C_SPEED_SLV[2:0]				PT1_I2C_SPEED_MST[2:0]
0x 12 3	0 x 0 0	<u>PT_CFG_5[7: 0]</u>								-
0x 12 4	0 x 0 0	<u>PT_CFG_6[7: 0]</u>				PT1_I2C_TRANSLATION_0_DESTINATION[6:0]				-

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 12 5	0 x 0 0	<u>PT_CFG_7[7: 0]</u>								-
0x 12 6	0 x 0 0	<u>PT_CFG_8[7: 0]</u>								-
0x 12 8	0 x D C	<u>PT_CFG_10[7:0]</u>								
0x 12 9	0 x 0 5	<u>PT_CFG_11[7:0]</u>	-	-						
0x 12 A	0 x 2 D	<u>PT_CFG_12[7:0]</u>	-	-						
0x 12 B	0 x 0 0	<u>PT_CFG_13[7:0]</u>								-
0x 12 C	0 x 0 0	<u>PT_CFG_14[7:0]</u>								-
0x 12 D	0 x 0 0	<u>PT_CFG_15[7:0]</u>								-
0x 12 E	0 x 0 0	<u>PT_CFG_16[7:0]</u>								-
SPI_CFG										

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x130	0x48	<u>SPI_CFG_0[7:0]</u>	SPI_EN	MST_SEL	SPI_MODE[1:0]		SPI_IGNORE_ID	-	SPI_LOCAL_ID[1:0]	
0x131	0x00	<u>SPI_CFG_1[7:0]</u>	SPI_LINK_SEL	SPI_PRIORITY[1:0]		MISO_SAMPLE_EDGE	-	-	MST_SS_1_POL	MST_SS_2_POL
0x132	0xC	<u>SPI_CFG_2[7:0]</u>	-	-	-	-	MST_SS_1_EN	MST_SS_2_EN	RO_INPUT_EN	BNE_OUTPUT_EN
0x133	0x01	<u>SPI_CFG_3[7:0]</u>	SPI_SLAVE_SEL_DELAY[7:0]							
0x134	0xF	<u>SPI_CFG_4[7:0]</u>	SPI_SCLK_LOW_CLKS[7:0]							
0x135	0xF	<u>SPI_CFG_5[7:0]</u>	SPI_SCLK_HIGH_CLKS[7:0]							
SGMII_CFG										
0x138	0x20	<u>SGMII_CFG_0[7:0]</u>	SGMII_EN	SGMII_RESET	SGMII_SPEED	LOOPBACK_LOCAL_EN	LOOPBACK_REMOTE_EN	SGMII_TX_POLARITY	SGMII_RX_POLARITY	SGMII_CMD_RST_N
0x139	0x20	<u>SGMII_CFG_1[7:0]</u>	SGMII_LIN_K_SEL	SGMII_PRIORITY[1:0]		-	-	-	-	-
0x13A	0x4	<u>SGMII_CFG_2[7:0]</u>	MDIO_CLOCK_DIVIDER[7:0]							

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB					
0x13B	0x00	<u>SGMII_CFG_3[7:0]</u>	MDIO_PHY_ADDRESS[4:0]			-			MDIO_EN						
0x13C	0x00	<u>SGMII_CFG_4[7:0]</u>	MDIO_REGISTER_ADDRESS[4:0]			ADD_PREAMBLE_EN	MDIO_READ_WRITE	MDIO_START							
0x13D	0x00	<u>SGMII_CFG_5[7:0]</u>	MDIO_DATA_BYTE_0[7:0]												
0x13E	0x00	<u>SGMII_CFG_6[7:0]</u>	MDIO_DATA_BYTE_1[7:0]												
0x13F	0x00	<u>SGMII_CFG_7[7:0]</u>	-	-	-	-	-	SGMII_INT_EN	SGMII_PRBS_RX_CHECKER_EN	SGMII_PRBS_TX_EN					
AUDIO_CFG															
0x143	0x20	<u>AUDIO_CFG_0[7:0]</u>	AUDIO_LINK_SEL	AUDIO_PRIORITY[1:0]	I2S_MODE	AUDIO_RX_ID[1:0]	AUDIO_PRBS_CHECKER_EN	AUDIO_RX_EN							
GPIO_CFG															
0x145	0x00	<u>GPIO_CFG_0[7:0]</u>	GPIO_LINK_SEL	GPIO_PRIORITY[1:0]	-	-	-	-	-	-					
GPIO_CFG_0															
0x146	0x80	<u>GPIO_CFG_1[7:0]</u>	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_CODE_MPENSATION_EN	GPIO_TX_ID[4:0]									

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 14 7	0 x C 4	GPIO_CFG_2 [7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	GPIO_EDGE_RATE[1:0]		-
0x 14 8	0 x 2 0	GPIO_CFG_3 [7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNNEL _EN	GPIO_OUTP UT_TYPE			GPIO_RX_ID[4:0]		
GPIO_CFG 1										
0x 14 9	0 x 8 1	GPIO_CFG_4 [7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN			GPIO_TX_ID[4:0]		
0x 14 A	0 x C 4	GPIO_CFG_5 [7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	GPIO_EDGE_RATE[1:0]		-
0x 14 B	0 x 2 1	GPIO_CFG_6 [7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNNEL _EN	GPIO_OUTP UT_TYPE			GPIO_RX_ID[4:0]		
GPIO_CFG 2										
0x 14 C	0 x 8 2	GPIO_CFG_7 [7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN			GPIO_TX_ID[4:0]		
0x 14 D	0 x C 4	GPIO_CFG_8 [7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	GPIO_EDGE_RATE[1:0]		-
0x 14 E	0 x 2 2	GPIO_CFG_9 [7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNNEL _EN	GPIO_OUTP UT_TYPE			GPIO_RX_ID[4:0]		
GPIO_CFG 5										

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 15 5	0 x 8 5	GPIO_CFG_1 0[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 15 6	0 x C 6	GPIO_CFG_1 1[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 15 7	0 x 2 5	GPIO_CFG_1 2[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 6										
0x 15 8	0 x 8 6	GPIO_CFG_1 3[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 15 9	0 x C 6	GPIO_CFG_1 4[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 15 A	0 x 2 6	GPIO_CFG_1 5[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 9										
0x 16 1	0 x 0 9	GPIO_CFG_1 6[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 16 2	0 x 8 6	GPIO_CFG_1 7[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 16 3	0 x	GPIO_CFG_1 8[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	2 9									
GPIO_CFG 10										
0x 16 4	0 x 8 A	GPIO_CFG_1 9[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 16 5	0 x C 6	GPIO_CFG_2 0[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 16 6	0 x 2 A	GPIO_CFG_2 1[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 11										
0x 16 7	0 x 8 B	GPIO_CFG_2 2[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 16 8	0 x C 6	GPIO_CFG_2 3[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 16 9	0 x 2 B	GPIO_CFG_2 4[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 12										
0x 16 A	0 x 8 C	GPIO_CFG_2 5[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 16 B	0 x	GPIO_CFG_2 6[7:0]	GPIO_INPU T_RESISTA	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	C 4		NCE_VALU E							
0x 16 C	0 x 2 C	GPIO_CFG_2 7[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 13										
0x 16 D	0 x 8 D	GPIO_CFG_2 8[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 16 E	0 x C 4	GPIO_CFG_2 9[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	GPIO_EDGE_RATE[1:0]	-	
0x 16 F	0 x 2 D	GPIO_CFG_3 0[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 14										
0x 17 0	0 x 8 E	GPIO_CFG_3 1[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 17 1	0 x C 4	GPIO_CFG_3 2[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	GPIO_EDGE_RATE[1:0]	-	
0x 17 2	0 x 2 E	GPIO_CFG_3 3[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 15										
0x 17 3	0 x	GPIO_CFG_3 4[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	8 F									
0x 17 4	0 x C 6	GPIO_CFG_3 5[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 17 5	0 x 2 F	GPIO_CFG_3 6[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE					
GPIO_CFG 16										
0x 17 6	0 x 9 0	GPIO_CFG_3 7[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN					GPIO_TX_ID[4:0]
0x 17 7	0 x C 6	GPIO_CFG_3 8[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-		GPIO_EDGE_RATE[1:0]	-
0x 17 8	0 x 3 0	GPIO_CFG_3 9[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE					GPIO_RX_ID[4:0]
GPIO_CFG 17										
0x 17 9	0 x 1 1	GPIO_CFG_4 0[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN					GPIO_TX_ID[4:0]
0x 17 A	0 x 8 6	GPIO_CFG_4 1[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 17 B	0 x 3 1	GPIO_CFG_4 2[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE					GPIO_RX_ID[4:0]

A D D R E S S	R E S E T	NAME	MSB							LSB
GPIO_CFG 18										
0x 17 C	0 x 9 2	GPIO_CFG_4 3[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 17 D	0 x C 6	GPIO_CFG_4 4[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 17 E	0 x 3 2	GPIO_CFG_4 5[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 19										
0x 17 F	0 x 9 3	GPIO_CFG_4 6[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 18 0	0 x C 6	GPIO_CFG_4 7[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-
0x 18 1	0 x 3 3	GPIO_CFG_4 8[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNN EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 20										
0x 18 2	0 x 9 4	GPIO_CFG_4 9[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]				
0x 18 3	0 x C 4	GPIO_CFG_5 0[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB	
0x 18 4	0 x 3 4	GPIO_CFG_5 1[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNNEL EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]					
GPIO_CFG 21											
0x 18 5	0 x 9 5	GPIO_CFG_5 2[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]					
GPIO_CFG 22											
0x 18 8	0 x 9 6	GPIO_CFG_5 5[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]					
0x 18 9	0 x C 4	GPIO_CFG_5 6[7:0]	GPIO_INPU T_RESISTA NCE_VALU E	GPIO_INPUT_RESISTANCE _CONFIG[1:0]		-	-	-	-	-	
0x 18 A	0 x 3 6	GPIO_CFG_5 7[7:0]	GPIO_OUT PUT_PIN_E N	GPIO_OUT PUT_TUNNEL EL_EN	GPIO_OUTP UT_TYPE	GPIO_RX_ID[4:0]					
GPIO_CFG 23											
0x 18 B	0 x 9 7	GPIO_CFG_5 8[7:0]	GPIO_INPU T_PIN_EN	GPIO_INPU T_TUNNEL _EN	GPIO_TX_CO MPENSATIO N_EN	GPIO_TX_ID[4:0]					

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x18C	0xC4	<u>GPIO_CFG_5</u> 9[7:0]	GPIO_INPUT_RESISTANCE_VALU E	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		-	-	-	-	-
0x18D	0x37	<u>GPIO_CFG_6</u> 0[7:0]	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
GPIO_CFG 24										
0x18E	0x98	<u>GPIO_CFG_6</u> 1[7:0]	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_CONFIGURATION_EN	GPIO_TX_ID[4:0]				
0x18F	0xC4	<u>GPIO_CFG_6</u> 2[7:0]	GPIO_INPUT_RESISTANCE_VALU E	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		-	-	-	-	-
0x190	0x38	<u>GPIO_CFG_6</u> 3[7:0]	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
OUTPUT_CFG										
0x192	0x00	<u>OUTPUT_CFG_0</u> 0[7:0]	WMD_INT_EN	VA_DONE_INT_EN	-	VIDEO_LOCK_OUTPUT_EN	LOCK_PIN_CONTROL[1:0]	-	-	RCLKOUT_EN
CRC_CFG										
0x195	0x05	<u>CRC_CFG_0</u> 7[0]	-	-	-	-	-	VIDEO_LANE_CRC_EN	VIDEO_PACKET_CRC_EN	FRAME_CRC_EN
0x196	0x00	<u>CRC_CFG_1</u> 7[0]	-	-	-	-	FCRC_INF_OFRA ME_CC_EN	-	RGB_FRA ME_CRC_EN	DP_SINK_R GB_FRAME_CRC_EN
LF_TEMP_CFG										

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 19 9	0 x 0 0	<u>LINEFAULT</u> <u>CFG_0[7:0]</u>	LINEFAULT _0_EN	LINEFAULT _1_EN	-	-	-	-	-	-
0x 19 B	0 x 0 0	<u>ARQ_CFG_0[7:0]</u>	-	-	-	-	-	-	-	MAX_RT_E RROR_RES ET
VIDEO_PIPE_CFG										
0x 1A 0	0 x 8 0	<u>VIDEO_PIPE</u> <u>CFG_0[7:0]</u>	VID_EN_X	STREAM_SEL_X[1:0]	-	SUPPORT_BLACK_VI DEO_ENA BLE	BLANK_VID EO	COLOR_LUT _EN	VPRBS_CH ECKER_EN _X	
0x 1A 1	0 x 3 0	<u>VIDEO_PIPE</u> <u>CFG_1[7:0]</u>	VID_EN_Y	STREAM_SEL_Y[1:0]	LINK_SEL_Y	-	-	-	VPRBS_CH ECKER_EN _Y	
0x 1A 2	0 x 0 0	<u>VIDEO_PIPE</u> <u>CFG_2[7:0]</u>	VS_HS_PI N_EN_X	VS_HS_INP UT_MODE_X	DE_OUTPUT _EN_X	-	VS_HS_OU TPUT_EN_Y	DE_OUTPUT _EN_Y	SYNC_LOCATION_SEL[1:0]	
0x 1A 3	0 x 0 0	<u>VIDEO_PIPE</u> <u>CFG_3[7:0]</u>	VS_HS_AL T_PIN_EN_X	VS_HS_AL T_INPUT_MODE_X	-	-	-	-	-	-
DC_VIDEO_CFG										
0x 1A 5	0 x 0 8	<u>DC_VIDEO_C</u> <u>FG_0[7:0]</u>	DROP_VIDEO[3:0]			AUTO_DR OP_VIDEO _EN	-	-	-	-
DP_CFG										
0x 1A 8	0 x 8 4	<u>DP_CFG_0[7: 0]</u>	AUTO_RET RAIN_ON_ LOSS_OF_ LINK_EN	-	DP_SINK_ED ID_TIMING_E N	DP_SINK_RE AD_EDID_E N	DP_SPREA DSPECTR UM_EN	AUTO_TIMI NG_EN	AUTO_DP_L INK_CONFI G	-

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 1A A	0 x 4 2	<u>DP_CFG_2[7:0]</u>	-	DP_LANE_COUNT[2:0]			-	DP_RATE[2:0]		
WM_CFG										
0x 1B 0	0 x 0 0	<u>WATERMAR K_LOCK_CE G_0[7:0]</u>								WATERMARK_KEY_BYTE_0[7:0]
0x 1B 1	0 x 0 0	<u>WATERMAR K_LOCK_CE G_1[7:0]</u>								WATERMARK_KEY_BYTE_1[7:0]
0x 1B 2	0 x 4 8	<u>WATERMAR K_CFG_0[7:0]</u>	WATERMA RK_DET_E N	WATERMA RK_REMO VE	WATERMAR K_REGIONAL _MODE	WATERMAR K_BLANK	WATERMA RK_REGIO NAL_BLAN K_MODE	-	-	-
0x 1B 3	0 x 0 0	<u>WATERMAR K_CFG_1[7:0]</u>								WM_REGION_XMIN_BYTE_0[7:0]
0x 1B 4	0 x 0 0	<u>WATERMAR K_CFG_2[7:0]</u>								WM_REGION_XMIN_BYTE_1[7:0]
0x 1B 5	0 x 0 0	<u>WATERMAR K_CFG_3[7:0]</u>								WM_REGION_XMAX_BYTE_0[7:0]
0x 1B 6	0 x 0 0	<u>WATERMAR K_CFG_4[7:0]</u>								WM_REGION_XMAX_BYTE_1[7:0]
0x 1B 7	0 x 0 0	<u>WATERMAR K_CFG_5[7:0]</u>								WM_REGION_YMIN_BYTE_0[7:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 1B 8	0 x 0 0	<u>WATERMAR</u> <u>K CFG_6[7:0]</u>								WM_REGION_YMIN_BYTE_1[7:0]
0x 1B 9	0 x 0 0	<u>WATERMAR</u> <u>K CFG_7[7:0]</u>								WM_REGION_YMAX_BYTE_0[7:0]
0x 1B A	0 x 0 0	<u>WATERMAR</u> <u>K CFG_8[7:0]</u>								WM_REGION_YMAX_BYTE_1[7:0]
VPG_CFG										
0x 1B C	0 x 0 0	<u>PATTERN_G</u> <u>ENERATOR</u> <u>CFG_0[7:0]</u>								CUSTOM_COLOR_RED[7:0]
0x 1B D	0 x 0 0	<u>PATTERN_G</u> <u>ENERATOR</u> <u>CFG_1[7:0]</u>								CUSTOM_COLOR_GREEN[7:0]
0x 1B E	0 x 0 0	<u>PATTERN_G</u> <u>ENERATOR</u> <u>CFG_2[7:0]</u>								CUSTOM_COLOR_BLUE[7:0]
0x 1B F	0 x 0 0	<u>PATTERN_G</u> <u>ENERATOR</u> <u>CFG_3[7:0]</u>	CUSTOM_COLOR_RED_ 30BIT_LSBS[1:0]	CUSTOM_COLOR_GREEN_3 0BIT_LSBS[1:0]	CUSTOM_COLOR_BLUE_ 30BIT_LSBS[1:0]		-			MODE_30BT T_EN
0x 1C 0	0 x 0 0	<u>PATTERN_G</u> <u>ENERATOR</u> <u>CFG_4[7:0]</u>								PATTERN_SIZE_X[7:0]
0x 1C 1	0 x 0 0	<u>PATTERN_G</u> <u>ENERATOR</u> <u>CFG_5[7:0]</u>								PATTERN_SIZE_Y[7:0]

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 1C 2	0 x 0 0	PATTERN_G <u>ENERATOR</u> CFG_6[7:0]								GRADIENT_COLOR_STEP_SIZE[7:0]
0x 1C 3	0 x 0 0	PATTERN_G <u>ENERATOR</u> CFG_7[7:0]								PATTERN_SELECT[7:0]
DSC_CFG										
0x 1C 5	0 x 0 0	DSC_CFG_0[7:0]	DSC_DEC ODE_EN	-	-	-	-	-	-	-
HDCP_CFG										
0x 1C 7	0 x C 1	HDCP_CFG_0[7:0]	HDCP_EN_X	HDCP_EN_Y	-	-	HDCP_ER R_RESET	HDCP_GPIO_ID_Y[1:0]	HDCP_VER	
0x 1C 8	0 x 9 4	HDCP_CFG_1[7:0]								HDCP_ADDRESS_Y[6:0]
FRC_CFG										
0x 1D 2	0 x 0 0	FRC_CFG_0[7:0]	FRC_EN	-	-	-	-	-	-	-
VIDEO_TIMING_CFG										
0x 1D 6	0 x 1 4	VIDEO_TIMIN G_CFG_0[7:0]								PCLK_FREQUENCY_BYTE_0[7:0]
0x 1D 7	0 x 4 4	VIDEO_TIMIN G_CFG_1[7:0]								PCLK_FREQUENCY_BYTE_1[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 1D 8	0 x 0 2	<u>VIDEO_TIMIN</u> <u>G_CFG_2[7:0]</u> 1								PCLK_FREQUENCY_BYTE_2[7:0]
0x 1D 9	0 x 8 0	<u>VIDEO_TIMIN</u> <u>G_CFG_3[7:0]</u> 1								H_ACTIVE_BYTE_0[7:0]
0x 1D A	0 x 0 7	<u>VIDEO_TIMIN</u> <u>G_CFG_4[7:0]</u> 1								H_ACTIVE_BYTE_1[7:0]
0x 1D B	0 x 5 8	<u>VIDEO_TIMIN</u> <u>G_CFG_5[7:0]</u> 1								H_FP_BYTE_0[7:0]
0x 1D C	0 x 0 0	<u>VIDEO_TIMIN</u> <u>G_CFG_6[7:0]</u> 1								H_FP_BYTE_1[7:0]
0x 1D D	0 x 2 C	<u>VIDEO_TIMIN</u> <u>G_CFG_7[7:0]</u> 1								H_SW_BYTE_0[7:0]
0x 1D E	0 x 0 0	<u>VIDEO_TIMIN</u> <u>G_CFG_8[7:0]</u> 1								H_SW_BYTE_1[7:0]
0x 1D F	0 x 9 4	<u>VIDEO_TIMIN</u> <u>G_CFG_9[7:0]</u> 1								H_BP_BYTE_0[7:0]
0x 1E 0	0 x 0 0	<u>VIDEO_TIMIN</u> <u>G_CFG_10[7:0]</u> 1								H_BP_BYTE_1[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 1E 1	0 x 3 8	<u>VIDEO_TIMIN</u> <u>G_CFG_11[7:0]</u>								V_ACTIVE_BYTE_0[7:0]
0x 1E 2	0 x 0 4	<u>VIDEO_TIMIN</u> <u>G_CFG_12[7:0]</u>								V_ACTIVE_BYTE_1[7:0]
0x 1E 3	0 x 0 4	<u>VIDEO_TIMIN</u> <u>G_CFG_13[7:0]</u>								V_FP[7:0]
0x 1E 4	0 x 0 5	<u>VIDEO_TIMIN</u> <u>G_CFG_14[7:0]</u>								V_SW[7:0]
0x 1E 5	0 x 2 4	<u>VIDEO_TIMIN</u> <u>G_CFG_15[7:0]</u>								V_BP[7:0]
0x 1E 6	0 x 0 3	<u>VIDEO_TIMIN</u> <u>G_CFG_16[7:0]</u>	-	FORCE_EV ENODD_PI XEL_MODE _EN	COLOR_DEP TH_MANUAL _MODE	COLOR_DEP TH_30BIT_S ELECT	-	HS_VS_POLARITY_MA NUAL_MODE	VS_POLARITY	HS_POLARITY
PSM_STATE_CFG										
0x 1E 7	0 x 0 0	<u>PSM_STATE</u> <u>CFG_0[7:0]</u>								PSM_STATE[7:0]
0x 1E 8	0 x 0 0	<u>PSM_STATUS</u> <u>S_0[7:0]</u>								PSM_STATUS[7:0]
VRX X										
0x 50 2	0 x	<u>LUT_CTRL</u> [7: 0]	-	-	LUT_MSB_DATA[1:0]	LUT_10_BIT_OUT	-	-	-	-

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB				
	0 8													
0x 51 F 0	0 x 0 0	<u>VRX_ASIL_IN</u> <u>J[7:0]</u>	-	-	FRC_DATAP ATH_FAIL_IN J	LUT_CRC_B LUE_FAIL_IN J	LUT_CRC_ GREEN_FA IL_INJ	LUT_CRC_ RED_FAIL_I NJ	LUT_DATAP ATH_FAIL_I NJ	WM_DATAP ATH_FAIL_I NJ				
VRX Y														
0x 54 2	0 x 0 8	<u>LUT_CTRL[7: 0]</u>	-	-	LUT_MSB_DATA[1:0]		LUT_10_BI T_OUT	-	-	-				
0x 55 B	0 x 0 0	<u>PRBS_ERR[7: 0]</u>	VPRBS_ERROR_COUNT[7:0]											
0x 55 F	0 x 0 0	<u>VRX_ASIL_IN</u> <u>J[7:0]</u>	-	-	FRC_DATAP ATH_FAIL_IN J	LUT_CRC_B LUE_FAIL_IN J	LUT_CRC_ GREEN_FA IL_INJ	LUT_CRC_ RED_FAIL_I NJ	LUT_DATAP ATH_FAIL_I NJ	WM_DATAP ATH_FAIL_I NJ				
VIDEO_AUTH														
0x 60 0	0 x 0 5	<u>AUTH0[7:0]</u>	FRAME_CYCLE_MODUL O_H[1:0]	LOCAL_CHALLENGE_MAX[1: 0]		-	AUTH_GLO BAL_PERIO DIC	AUTH_GLOB AL_TRIG	AUTH_EN					
0x 60 1	0 x 0 4	<u>AUTH1[7:0]</u>	FRAME_CYCLE_MODULO_L[7:0]											
0x 60 2	0 x 0 0	<u>XMINL0a[7:0]</u>	XMIN0a LSB[7:0]											
0x 60 3	0 x 0 0	<u>XMINH0a[7:0]</u>	-	-	XMIN0a_MSB[5:0]									

GMSL3/2 eDP Deserializers with
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MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 60 4	0 x 0 1	XMAXL0a[7:0]								XMAX0a_LSB[7:0]
0x 60 5	0 x 0 0	XMAXH0a[7:0]		-	-					XMAX0a_MSB[5:0]
0x 60 6	0 x 0 0	XMINL1a[7:0]								XMIN1a_LSB[7:0]
0x 60 7	0 x 0 0	XMINH1a[7:0]		-	-					XMIN1a_MSB[5:0]
0x 60 8	0 x 0 0	XMAXL1a[7:0]								XMAX1a_LSB[7:0]
0x 60 9	0 x 0 0	XMAXH1a[7:0]		-	-					XMAX1a_MSB[5:0]
0x 60 A	0 x 0 0	XMINL2a[7:0]								XMIN2a_LSB[7:0]
0x 60 B	0 x 0 0	XMINH2a[7:0]		-	-					XMIN2a_MSB[5:0]
0x 60 C	0 x 0 0	XMAXL2a[7:0]								XMAX2a_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 60 D	0 x 0 0	XMAXH2a[7:0]	-	-						XMAX2a_MSB[5:0]
0x 60 E	0 x 0 0	XMINL3a[7:0]								XMIN3a_LSB[7:0]
0x 60 F	0 x 0 0	XMINH3a[7:0]	-	-						XMIN3a_MSB[5:0]
0x 61 0	0 x 0 0	XMAXL3a[7:0]								XMAX3a_LSB[7:0]
0x 61 1	0 x 0 0	XMAXH3a[7:0]	-	-						XMAX3a_MSB[5:0]
0x 61 2	0 x 0 0	XMINL0b[7:0]								XMIN0b_LSB[7:0]
0x 61 3	0 x 0 0	XMINH0b[7:0]	-	-						XMIN0b_MSB[5:0]
0x 61 4	0 x 0 1	XMAXL0b[7:0]								XMAX0b_LSB[7:0]
0x 61 5	0 x 0 0	XMAXH0b[7:0]	-	-						XMAX0b_MSB[5:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 61 6	0 x 0 0	XMINL1b[7:0]								XMIN1b_LSB[7:0]
0x 61 7	0 x 0 0	XMINH1b[7:0]		-	-					XMIN1b_MSB[5:0]
0x 61 8	0 x 0 0	XMAXL1b[7:0] 1								XMAX1b_LSB[7:0]
0x 61 9	0 x 0 0	XMAXH1b[7:0] 1		-	-					XMAX1b_MSB[5:0]
0x 61 A	0 x 0 0	XMINL2b[7:0]								XMIN2b_LSB[7:0]
0x 61 B	0 x 0 0	XMINH2b[7:0]		-	-					XMIN2b_MSB[5:0]
0x 61 C	0 x 0 0	XMAXL2b[7:0] 1								XMAX2b_LSB[7:0]
0x 61 D	0 x 0 0	XMAXH2b[7:0] 1		-	-					XMAX2b_MSB[5:0]
0x 61 E	0 x 0 0	XMINL3b[7:0]								XMIN3b_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 61 F	0 x 0 0	XMINH3b[7:0]	–	–						XMIN3b_MSB[5:0]
0x 62 0	0 x 0 0	XMAXL3b[7:0]								XMAX3b_LSB[7:0]
0x 62 1	0 x 0 0	XMAXH3b[7:0]	–	–						XMAX3b_MSB[5:0]
0x 62 2	0 x 0 0	YMINL0a[7:0]								YMIN0a_LSB[7:0]
0x 62 3	0 x 0 0	YMINH0a[7:0]	–	–						YMIN0a_MSB[5:0]
0x 62 4	0 x 0 1	YMAXL0a[7:0]								YMAX0a_LSB[7:0]
0x 62 5	0 x 0 0	YMAXH0a[7:0]	FRAME0a_MSB[1:0]							YMAX0a_MSB[5:0]
0x 62 6	0 x 0 1	frame0a[7:0]								FRAME0a_LSB[7:0]
0x 62 7	0 x 0 0	YMINL1a[7:0]								YMIN1a_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 62 8	0 x 0 0	YMINH1a[7:0]	–	–						YMIN1a_MSB[5:0]
0x 62 9	0 x 0 0	YMAXL1a[7:0] 1								YMAX1a_LSB[7:0]
0x 62 A	0 x 0 0	YMAXH1a[7:0] 1	FRAME1a_MSB[1:0]							YMAX1a_MSB[5:0]
0x 62 B	0 x 0 0	frame1a[7:0]								FRAME1a_LSB[7:0]
0x 62 C	0 x 0 0	YMINL2a[7:0]								YMIN2a_LSB[7:0]
0x 62 D	0 x 0 0	YMINH2a[7:0]	–	–						YMIN2a_MSB[5:0]
0x 62 E	0 x 0 0	YMAXL2a[7:0] 1								YMAX2a_LSB[7:0]
0x 62 F	0 x 0 0	YMAXH2a[7:0] 1	FRAME2a_MSB[1:0]							YMAX2a_MSB[5:0]
0x 63 0	0 x 0 0	frame2a[7:0]								FRAME2a_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 63 1	0 x 0 0	<u>YMINL3a[7:0]</u>								YMIN3a_LSB[7:0]
0x 63 2	0 x 0 0	<u>YMINH3a[7:0]</u>		-	-					YMIN3a_MSB[5:0]
0x 63 3	0 x 0 0	<u>YMAXL3a[7:0]</u> 1								YMAX3a_LSB[7:0]
0x 63 4	0 x 0 0	<u>YMAXH3a[7:0]</u> 1	FRAME3a_MSB[1:0]							YMAX3a_MSB[5:0]
0x 63 5	0 x 0 0	<u>frame3a[7:0]</u>								FRAME3a_LSB[7:0]
0x 63 6	0 x 0 0	<u>YMINL0b[7:0]</u>								YMIN0b_LSB[7:0]
0x 63 7	0 x 0 0	<u>YMINH0b[7:0]</u>		-	-					YMIN0b_MSB[5:0]
0x 63 8	0 x 0 1	<u>YMAXL0b[7:0]</u> 1								YMAX0b_LSB[7:0]
0x 63 9	0 x 0 0	<u>YMAXH0b[7:0]</u> 1	FRAME0b_MSB[1:0]							YMAX0b_MSB[5:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 63 A	0 x 0 1	frame0b[7:0]								FRAME0b_LSB[7:0]
0x 63 B	0 x 0 0	YMINL1b[7:0]								YMIN1b_LSB[7:0]
0x 63 C	0 x 0 0	YMINH1b[7:0]		-	-					YMIN1b_MSB[5:0]
0x 63 D	0 x 0 0	YMAXL1b[7:0]								YMAX1b_LSB[7:0]
0x 63 E	0 x 0 0	YMAXH1b[7:0]		FRAME1b_MSB[1:0]						YMAX1b_MSB[5:0]
0x 63 F	0 x 0 0	frame1b[7:0]								FRAME1b_LSB[7:0]
0x 64 0	0 x 0 0	YMINL2b[7:0]								YMIN2b_LSB[7:0]
0x 64 1	0 x 0 0	YMINH2b[7:0]		-	-					YMIN2b_MSB[5:0]
0x 64 2	0 x 0 0	YMAXL2b[7:0]								YMAX2b_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB						
0x 64 3	0 x 0 0	<u>YMAXH2b[7:0]</u> 1	FRAME2b_MSB[1:0]	YMAX2b_MSB[5:0]												
0x 64 4	0 x 0 0	<u>frame2b[7:0]</u>		FRAME2b_LSB[7:0]												
0x 64 5	0 x 0 0	<u>YMINL3b[7:0]</u>		YMIN3b_LSB[7:0]												
0x 64 6	0 x 0 0	<u>YMINH3b[7:0]</u>	-	-	YMIN3b_MSB[5:0]											
0x 64 7	0 x 0 0	<u>YMAXL3b[7:0]</u> 1		YMAX3b_LSB[7:0]												
0x 64 8	0 x 0 0	<u>YMAXH3b[7:0]</u> 1	FRAME3b_MSB[1:0]	YMAX3b_MSB[5:0]												
0x 64 9	0 x 0 0	<u>frame3b[7:0]</u>		FRAME3b_LSB[7:0]												
0x 64 A	0 x 0 0	<u>out1[7:0]</u>	FRAME_C NT_MSB	-	VA_DONE_F LAG	-	VA_DONE_ PIN	A_OR_B	AUTH_DON E_B	AUTH_DON E_A						
0x 64 B	0 x 0 0	<u>out1a[7:0]</u>		FRAME_CNT_LSB[7:0]												

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 64 C	0 x 0 0	<u>out2[7:0]</u>								CRC_OUT_A_0[7:0]
0x 64 D	0 x 0 0	<u>out3[7:0]</u>								CRC_OUT_A_1[7:0]
0x 64 E	0 x 0 0	<u>out4[7:0]</u>								CRC_OUT_A_2[7:0]
0x 64 F	0 x 0 0	<u>out5[7:0]</u>								CRC_OUT_A_3[7:0]
0x 65 0	0 x 0 0	<u>out6[7:0]</u>								CRC_OUT_B_0[7:0]
0x 65 1	0 x 0 0	<u>out7[7:0]</u>								CRC_OUT_B_1[7:0]
0x 65 2	0 x 0 0	<u>out8[7:0]</u>								CRC_OUT_B_2[7:0]
0x 65 3	0 x 0 0	<u>out9[7:0]</u>								CRC_OUT_B_3[7:0]
0x 65 4	0 x 0 0	<u>outa[7:0]</u>								FULL_FRAME_CRC_0[7:0]

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 65 5	0 x 0 0	<u>outb[7:0]</u>								FULL_FRAME_CRC_1[7:0]
0x 65 6	0 x 0 0	<u>outc[7:0]</u>								FULL_FRAME_CRC_2[7:0]
0x 65 7	0 x 0 0	<u>outd[7:0]</u>								FULL_FRAME_CRC_3[7:0]
PMX_TASK_REGS										
0x E7 6	0 x 0 0	<u>PSM_TRIM REV_0[7:0]</u>								PSM_TRIM_MINOR_REV[7:0]
0x E7 7	0 x 0 0	<u>PSM_TRIM REV_1[7:0]</u>								PSM_TRIM_MAJOR_REV[7:0]
FUNC_SAFE										
0x 1F 00	0 x 0 0	<u>REGCRC0[7: 0]</u>		-	-	GEN_ROLLI NG_CRC	I2C_WR_C OMPUTE	PERIODIC_ COMPUTE	CHECK_CR C	RESET_CR C
0x 1F 01	0 x 0 0	<u>REGCRC1[7: 0]</u>								CRC_PERIOD[7:0]
0x 1F 02	0 x 0 0	<u>REGCRC2[7: 0]</u>								REGCRC_LSB[7:0]
0x 1F 03	0 x	<u>REGCRC3[7: 0]</u>								REGCRC_MSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x 1F 20	0 x 0 0	<u>CC_CRC0[7:0]</u> 1								CC_CRC_VAL[7:0]
0x 1F 21	0 x 0 0	<u>CC_CRC1[7:0]</u> 1								MSGCNTR_LSB[7:0]
0x 1F 22	0 x 0 0	<u>CC_CRC2[7:0]</u> 1								MSGCNTR_MSB[7:0]
0x 1F 23	0 x 0 0	<u>CC_CRC3[7:0]</u> 1								CC_CRC_ERR_CNT[7:0]
0x 1F 24	0 x 0 0	<u>CC_CRC4[7:0]</u> 1								MSGCNTR_ERR_CNT[7:0]
0x 1F 26	0 x 0 0	<u>CC_RTTN_C</u> <u>RC_ERR[7:0]</u>	-	-	-	-	-	-	-	INJECT_RT TN_CRC_E RR
COLOR_A_LUT X										
0x 20 00	0 x 0 0	<u>LUT_A[7:0]</u>	-	-	-	-	-	-	-	-
COLOR_B_LUT X										
0x 21 00	0 x 0 0	<u>LUT_B[7:0]</u>	-	-	-	-	-	-	-	-

A D D R E S S	R E S E T	NAME	MSB							LSB
COLOR_C_LUT X										
0x 22 00	0 x 0 0	LUT_C[7:0]	-	-	-	-	-	-	-	-
TELLTALE_DETECTOR_GEN_CSR										
0x 30 00	0 x 0 4	TELLTALE_C TRL_REG_0[7:0]	-	-	-	TELLTALE_F ORCE_BANK _B	TELLTALE_F ORCE_BANK_A	TELLTALE_P ERIODIC_M ODE	TELLTALE_T RIGGER_M ODE	TELLTALE_D ET_EN
0x 30 01	0 x F F	TELLTALE_C TRL_REG_1[7:0]	BANK_B_ROI_INTERRUPT_EN[3:0]					BANK_A_ROI_INTERRUPT_EN[3:0]		
0x 30 02	0 x 0 0	TELLTALE_S STATUS_REG_0[7:0]	BANK_B_ROI_ERROR[3:0]					BANK_A_ROI_ERROR[3:0]		
0x 30 03	0 x 0 0	TELLTALE_S STATUS_REG_1[7:0]	TELLTALE_B ANK_A OR LC_DONE	TELLTALE_A CTIVE_BA NK_A OR B	-	-	-	-	-	-
REFERENCE_RED_COLOR 0										
0x 30 08	0 x 8 2	REF_COLOR GENERAL[7: 0]	REF_COLO R_INV_HU E	REF_COLO R_INV_SAT	REF_COLOR _INV_LUM	-	-	-	REF_COLO R_HUE_MA X_H	REF_COLO R_HUE_M IN_H
0x 30 09	0 x 4 A	REF_COLOR HUE_MAX L[7:0]	REF_COLOR_HUE_MAX_L[7:0]							
0x 30 0A	0 x 0 A	REF_COLOR HUE_MIN[7: 0]	REF_COLOR_HUE_MIN_L[7:0]							

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 0B	0 x 6 4	<u>REF_COLOR</u> <u>SAT_MAX[7: 0]</u>	–	REF_COLOR_SAT_MAX[6:0]						
0x 30 0C	0 x 2 8	<u>REF_COLOR</u> <u>SAT_MIN[7: 0]</u>	–	REF_COLOR_SAT_MIN[6:0]						
0x 30 0D	0 x 4 B	<u>REF_COLOR</u> <u>LUM_MAX[7: 0]</u>	–	REF_COLOR_LUM_MAX[6:0]						
0x 30 0E	0 x 1 9	<u>REF_COLOR</u> <u>LUM_MIN[7: 0]</u>	–	REF_COLOR_LUM_MIN[6:0]						
REFERENCE_ORANGE_COLOR 1										
0x 30 10	0 x 0 0	<u>REF_COLOR</u> <u>GENERAL[7: 0]</u>	REF_COLO R_INV_HU E	REF_COLO R_INV_SAT	REF_COLOR _INV_LUM	–	–	–	REF_COLO R_HUE_MA X_H	REF_COLO R_HUE_MI N_H
0x 30 11	0 x 3 3	<u>REF_COLOR</u> <u>HUE_MAX_</u> <u>L[7:0]</u>	REF_COLOR_HUE_MAX_L[7:0]							
0x 30 12	0 x 0 E	<u>REF_COLOR</u> <u>HUE_MIN[7: 0]</u>	REF_COLOR_HUE_MIN_L[7:0]							
0x 30 13	0 x 6 4	<u>REF_COLOR</u> <u>SAT_MAX[7: 0]</u>	–	REF_COLOR_SAT_MAX[6:0]						
0x 30 14	0 x 2 8	<u>REF_COLOR</u> <u>SAT_MIN[7: 0]</u>	–	REF_COLOR_SAT_MIN[6:0]						

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 15	0 x 4 B	<u>REF_COLOR_LUM_MAX[7:0]</u>	–	REF_COLOR_LUM_MAX[6:0]						
0x 30 16	0 x 1 9	<u>REF_COLOR_LUM_MIN[7:0]</u>	–	REF_COLOR_LUM_MIN[6:0]						
REFERENCE_GREEN_COLOR 2										
0x 30 18	0 x 0 0	<u>REF_COLOR_GENERAL[7:0]</u>	REF_COLO R_INV_HU E	REF_COLO R_INV_SAT	REF_COLOR _INV_LUM	–	–	–	REF_COLO R_HUE_MA X_H	REF_COLO R_HUE_MI N_H
0x 30 19	0 x A 7	<u>REF_COLOR_HUE_MAX_L[7:0]</u>	REF_COLOR_HUE_MAX_L[7:0]							
0x 30 1A	0 x 5 7	<u>REF_COLOR_HUE_MIN[7:0]</u>	REF_COLOR_HUE_MIN_L[7:0]							
0x 30 1B	0 x 6 4	<u>REF_COLOR_SAT_MAX[7:0]</u>	–	REF_COLOR_SAT_MAX[6:0]						
0x 30 1C	0 x 2 8	<u>REF_COLOR_SAT_MIN[7:0]</u>	–	REF_COLOR_SAT_MIN[6:0]						
0x 30 1D	0 x 4 B	<u>REF_COLOR_LUM_MAX[7:0]</u>	–	REF_COLOR_LUM_MAX[6:0]						
0x 30 1E	0 x 1 9	<u>REF_COLOR_LUM_MIN[7:0]</u>	–	REF_COLOR_LUM_MIN[6:0]						

A D D R E S S	R E S E T	NAME	MSB							LSB
REFERENCE_BLUE_COLOR 3										
0x 30 20	0 x 0 2	<u>REF_COLOR</u> <u>GENERAL[7:0]</u>	REF_COLO R_INV_HU E	REF_COLO R_INV_SAT	REF_COLOR _INV_LUM	-	-	-	REF_COLO R_HUE_MA X_H	REF_COLO R_HUE_MI N_H
0x 30 21	0 x 0 B	<u>REF_COLOR</u> <u>HUE_MAX</u> <u>L[7:0]</u>				REF_COLOR_HUE_MAX_L[7:0]				
0x 30 22	0 x B C	<u>REF_COLOR</u> <u>HUE_MIN[7:0]</u>				REF_COLOR_HUE_MIN_L[7:0]				
0x 30 23	0 x 6 4	<u>REF_COLOR</u> <u>SAT_MAX[7:0]</u>	-			REF_COLOR_SAT_MAX[6:0]				
0x 30 24	0 x 2 8	<u>REF_COLOR</u> <u>SAT_MIN[7:0]</u>	-			REF_COLOR_SAT_MIN[6:0]				
0x 30 25	0 x 4 B	<u>REF_COLOR</u> <u>LUM_MAX[7:0]</u>	-			REF_COLOR_LUM_MAX[6:0]				
0x 30 26	0 x 1 9	<u>REF_COLOR</u> <u>LUM_MIN[7:0]</u>	-			REF_COLOR_LUM_MIN[6:0]				
REFERENCE_WHITE_COLOR 4										
0x 30 28	0 x 0 2	<u>REF_COLOR</u> <u>GENERAL[7:0]</u>	REF_COLO R_INV_HU E	REF_COLO R_INV_SAT	REF_COLOR _INV_LUM	-	-	-	REF_COLO R_HUE_MA X_H	REF_COLO R_HUE_MI N_H
0x 30 29	0 x	<u>REF_COLOR</u> <u>HUE_MAX</u> <u>L[7:0]</u>				REF_COLOR_HUE_MAX_L[7:0]				

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	6 8									
0x 30 2A	0 x 0 0	<u>REF_COLOR</u> <u>HUE_MIN[7: 0]</u>								REF_COLOR_HUE_MIN_L[7:0]
0x 30 2B	0 x 6 4	<u>REF_COLOR</u> <u>SAT_MAX[7: 0]</u>	–							REF_COLOR_SAT_MAX[6:0]
0x 30 2C	0 x 0 0	<u>REF_COLOR</u> <u>SAT_MIN[7: 0]</u>	–							REF_COLOR_SAT_MIN[6:0]
0x 30 2D	0 x 6 4	<u>REF_COLOR</u> <u>LUM_MAX[7: 0]</u>	–							REF_COLOR_LUM_MAX[6:0]
0x 30 2E	0 x 5 F	<u>REF_COLOR</u> <u>LUM_MIN[7: 0]</u>	–							REF_COLOR_LUM_MIN[6:0]
REFERENCE_GRAY_COLOR 5										
0x 30 30	0 x 0 2	<u>REF_COLOR</u> <u>GENERAL[7: 0]</u>	REF_COLO R_INV_HU E	REF_COLO R_INV_SAT	REF_COLOR _INV_LUM	–	–	–	REF_COLO R_HUE_MA X_H	REF_COLO R_HUE_MI N_H
0x 30 31	0 x 6 8	<u>REF_COLOR</u> <u>HUE_MAX L[7:0]</u>								REF_COLOR_HUE_MAX_L[7:0]
0x 30 32	0 x 0 0	<u>REF_COLOR</u> <u>HUE_MIN[7: 0]</u>								REF_COLOR_HUE_MIN_L[7:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 33	0 x 1 9	<u>REF_COLOR_SAT_MAX[7:0]</u>	–	REF_COLOR_SAT_MAX[6:0]						
0x 30 34	0 x 0 0	<u>REF_COLOR_SAT_MIN[7:0]</u>	–	REF_COLOR_SAT_MIN[6:0]						
0x 30 35	0 x 4 B	<u>REF_COLOR_LUM_MAX[7:0]</u>	–	REF_COLOR_LUM_MAX[6:0]						
0x 30 36	0 x 1 9	<u>REF_COLOR_LUM_MIN[7:0]</u>	–	REF_COLOR_LUM_MIN[6:0]						
TELLTALE_BANK_A										
0x 30 38	0 x 0 0	<u>BANK_A_STATUS[7:0]</u>	–	–	–	–	–	BANK_A_C ALC_DONE	BANK_A_FRAME_COUNT[1:0]	
0x 30 39	0 x 0 0	<u>BANK_A_ROI_1_0_ERROR[7:0]</u>	–	BANK_A_R OI_1_COL OR_2_ERR OR	BANK_A_ROI _1_COLOR_1 _ERROR	BANK_A_RO I_1_COLOR_0 _ERROR	–	BANK_A_R OI_0_COLO R_2_ERRO R	BANK_A_RO I_0_COLOR_1 _ERROR	BANK_A_R OI_0_COLO R_0_ERRO R
0x 30 3A	0 x 0 0	<u>BANK_A_ROI_3_2_ERROR[7:0]</u>	–	BANK_A_R OI_3_COL OR_2_ERR OR	BANK_A_ROI _3_COLOR_1 _ERROR	BANK_A_RO I_3_COLOR_0 _ERROR	–	BANK_A_R OI_2_COLO R_2_ERRO R	BANK_A_RO I_2_COLOR_1 _ERROR	BANK_A_R OI_2_COLO R_0_ERRO R
BANK_A_ROI_COORDINATES 0										
0x 30 40	0 x 0 0	<u>BANK_A_ROI_0_XMIN_LSB[7:0]</u>	BANK_A_ROI0_XMIN_LSB[7:0]							
0x 30 41	0 x	<u>BANK_A_ROI_0_XMIN_MSB[7:0]</u>	–	–	BANK_A_ROI0_XMIN_MSB[5:0]					

GMSL3/2 eDP Deserializers with
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Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x 30 42	0 x 0 0	<u>BANK_A_ROI_0_XMAX_LSB[7:0]</u>								BANK_A_ROI0_XMAX LSB[7:0]
0x 30 43	0 x 0 0	<u>BANK_A_ROI_0_XMAX_MS_B[7:0]</u>	-	-						BANK_A_ROI0_XMAX_MSB[5:0]
0x 30 44	0 x 0 0	<u>BANK_A_ROI_0_YMIN_LSB[7:0]</u>								BANK_A_ROI0_YMIN LSB[7:0]
0x 30 45	0 x 0 0	<u>BANK_A_ROI_0_YMIN_MSB[7:0]</u>	-	-						BANK_A_ROI0_YMIN_MSB[5:0]
0x 30 46	0 x 0 0	<u>BANK_A_ROI_0_YMAX_LSB[7:0]</u>								BANK_A_ROI0_YMAX LSB[7:0]
0x 30 47	0 x 0 0	<u>BANK_A_ROI_0_YMAX_MS_B[7:0]</u>	-	-						BANK_A_ROI0_YMAX_MSB[5:0]
BANK_A_ROI_0_COLOR 0										
0x 30 48	0 x 0 0	<u>BANK_A_ROI_0_COLOR_S_ELECT[7:0]</u>	-	-	-	-	-	-		BANK_A_ROI0_COLOR_SELECT[2:0]
0x 30 49	0 x 0 0	<u>BANK_A_ROI_0_COLOR_MI_N_THR_LSB[7:0]</u>								BANK_A_ROI0_COLOR_MIN_THR LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 4A	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_MI</u> <u>N THR MSB[7:0]</u>								BANK_A_ROI0_COLOR_MIN_THR_MSB[7:0]
0x 30 4B	0 x F F	<u>BANK_A_ROI</u> <u>0_COLOR_M</u> <u>AX THR LSB[7:0]</u>								BANK_A_ROI0_COLOR_MAX_THR_LSB[7:0]
0x 30 4C	0 x F F	<u>BANK_A_ROI</u> <u>0_COLOR_M</u> <u>AX THR MSB[7:0]</u>								BANK_A_ROI0_COLOR_MAX_THR_MSB[7:0]
0x 30 4D	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_C</u> <u>OUNT LSB[7:0]</u>								BANK_A_ROI0_COLOR_COUNT_LSB[7:0]
0x 30 4E	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_C</u> <u>OUNT MSB[7:0]</u>								BANK_A_ROI0_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_0_COLOR 1										
0x 30 50	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-		BANK_A_ROI0_COLOR_SELECT[2:0]
0x 30 51	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_MI</u> <u>N THR LSB[7:0]</u>								BANK_A_ROI0_COLOR_MIN_THR_LSB[7:0]
0x 30 52	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_MI</u> <u>N THR MSB[7:0]</u>								BANK_A_ROI0_COLOR_MIN_THR_MSB[7:0]
0x 30 53	0 x F F	<u>BANK_A_ROI</u> <u>0_COLOR_M</u> <u>AX THR LSB[7:0]</u>								BANK_A_ROI0_COLOR_MAX_THR_LSB[7:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 54	0 x F F	<u>BANK_A_ROI</u> <u>0_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_A_ROI0_COLOR_MAX_THR_MSB[7:0]
0x 30 55	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_C</u> <u>OUNT LSB[7:</u> <u>0]</u>								BANK_A_ROI0_COLOR_COUNT_LSB[7:0]
0x 30 56	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_C</u> <u>OUNT MSB[7</u> <u>:0]</u>								BANK_A_ROI0_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_0_COLOR 2										
0x 30 58	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_A_ROI0_COLOR_SELECT[2:0]
0x 30 59	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_M</u> <u>IN THR LSB[</u> <u>7:0]</u>								BANK_A_ROI0_COLOR_MIN_THR_LSB[7:0]
0x 30 5A	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_M</u> <u>IN THR MSB[</u> <u>7:0]</u>								BANK_A_ROI0_COLOR_MIN_THR_MSB[7:0]
0x 30 5B	0 x F F	<u>BANK_A_ROI</u> <u>0_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>								BANK_A_ROI0_COLOR_MAX_THR_LSB[7:0]
0x 30 5C	0 x F F	<u>BANK_A_ROI</u> <u>0_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_A_ROI0_COLOR_MAX_THR_MSB[7:0]
0x 30 5D	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_C</u> <u>OUNT LSB[7:</u> <u>0]</u>								BANK_A_ROI0_COLOR_COUNT_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 5E	0 x 0 0	<u>BANK_A_ROI</u> <u>0_COLOR_C</u> <u>OUNT_MSB[7:0]</u>								
BANK_A_ROI_COORDINATES 1										
0x 30 60	0 x 0 0	<u>BANK_A_ROI</u> <u>1_XMIN LSB[7:0]</u>								
BANK_A_ROI1_XMIN LSB[7:0]										
0x 30 61	0 x 0 0	<u>BANK_A_ROI</u> <u>1_XMIN MSB[7:0]</u>	-	-						
BANK_A_ROI1_XMIN MSB[5:0]										
0x 30 62	0 x 0 0	<u>BANK_A_ROI</u> <u>1_XMAX LSB[7:0]</u>								
BANK_A_ROI1_XMAX LSB[7:0]										
0x 30 63	0 x 0 0	<u>BANK_A_ROI</u> <u>1_XMAX MSB[7:0]</u>	-	-						
BANK_A_ROI1_XMAX MSB[5:0]										
0x 30 64	0 x 0 0	<u>BANK_A_ROI</u> <u>1_YMIN LSB[7:0]</u>								
BANK_A_ROI1_YMIN LSB[7:0]										
0x 30 65	0 x 0 0	<u>BANK_A_ROI</u> <u>1_YMIN MSB[7:0]</u>	-	-						
BANK_A_ROI1_YMIN MSB[5:0]										
0x 30 66	0 x 0 0	<u>BANK_A_ROI</u> <u>1_YMAX LSB[7:0]</u>								
BANK_A_ROI1_YMAX LSB[7:0]										
0x 30 67	0 x 0 0	<u>BANK_A_ROI</u> <u>1_YMAX MSB[7:0]</u>	-	-						
BANK_A_ROI1_YMAX MSB[5:0]										

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
BANK_A_ROI_1_COLOR 0										
0x 30 68	0 x 0 0	<u>BANK A ROI</u> <u>1 COLOR S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_A_ROI1_COLOR_SELECT[2:0]
0x 30 69	0 x 0 0	<u>BANK A ROI</u> <u>1 COLOR MI</u> <u>N THR LSB[7:0]</u>								BANK_A_ROI1_COLOR_MIN_THR LSB[7:0]
0x 30 6A	0 x 0 0	<u>BANK A ROI</u> <u>1 COLOR MI</u> <u>N THR MSB[7:0]</u>								BANK_A_ROI1_COLOR_MIN_THR_MSB[7:0]
0x 30 6B	0 x F F	<u>BANK A ROI</u> <u>1 COLOR M</u> <u>AX THR LSB[7:0]</u>								BANK_A_ROI1_COLOR_MAX_THR LSB[7:0]
0x 30 6C	0 x F F	<u>BANK A ROI</u> <u>1 COLOR M</u> <u>AX THR MSB[7:0]</u>								BANK_A_ROI1_COLOR_MAX_THR_MSB[7:0]
0x 30 6D	0 x 0 0	<u>BANK A ROI</u> <u>1 COLOR C</u> <u>OUNT LSB[7:0]</u>								BANK_A_ROI1_COLOR_COUNT LSB[7:0]
0x 30 6E	0 x 0 0	<u>BANK A ROI</u> <u>1 COLOR C</u> <u>OUNT MSB[7:0]</u>								BANK_A_ROI1_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_1_COLOR 1										
0x 30 70	0 x 0 0	<u>BANK A ROI</u> <u>1 COLOR S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_A_ROI1_COLOR_SELECT[2:0]
0x 30 71	0 x	<u>BANK A ROI</u> <u>1 COLOR MI</u>								BANK_A_ROI1_COLOR_MIN_THR LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0	N THR LSB[7:0]								
0x 30 72	0 x 0 0	BANK A ROI 1 COLOR MI N THR MSB[7:0]								BANK_A_ROI1_COLOR_MIN_THR_MSB[7:0]
0x 30 73	0 x F F	BANK A ROI 1 COLOR M AX THR LSB [7:0]								BANK_A_ROI1_COLOR_MAX_THR_LSB[7:0]
0x 30 74	0 x F F	BANK A ROI 1 COLOR M AX THR MS B[7:0]								BANK_A_ROI1_COLOR_MAX_THR_MSB[7:0]
0x 30 75	0 x 0 0	BANK A ROI 1 COLOR C OUNT LSB[7: 0]								BANK_A_ROI1_COLOR_COUNT_LSB[7:0]
0x 30 76	0 x 0 0	BANK A ROI 1 COLOR C OUNT MSB[7: 0]								BANK_A_ROI1_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_1_COLOR 2										
0x 30 78	0 x 0 0	BANK A ROI 1 COLOR S ELECT[7:0]	-	-	-	-	-	-		BANK_A_ROI1_COLOR_SELECT[2:0]
0x 30 79	0 x 0 0	BANK A ROI 1 COLOR MI N THR LSB[7:0]								BANK_A_ROI1_COLOR_MIN_THR_LSB[7:0]
0x 30 7A	0 x 0 0	BANK A ROI 1 COLOR MI N THR MSB[7:0]								BANK_A_ROI1_COLOR_MIN_THR_MSB[7:0]

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 7B	0 x F F	<u>BANK_A_ROI</u> <u>1_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>								BANK_A_ROI1_COLOR_MAX_THR_LSB[7:0]
0x 30 7C	0 x F F	<u>BANK_A_ROI</u> <u>1_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_A_ROI1_COLOR_MAX_THR_MSB[7:0]
0x 30 7D	0 x 0 0	<u>BANK_A_ROI</u> <u>1_COLOR_C</u> <u>COUNT LSB[7:</u> <u>0]</u>								BANK_A_ROI1_COLOR_COUNT_LSB[7:0]
0x 30 7E	0 x 0 0	<u>BANK_A_ROI</u> <u>1_COLOR_C</u> <u>COUNT MSB[7</u> <u>:0]</u>								BANK_A_ROI1_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_COORDINATES 2										
0x 30 80	0 x 0 0	<u>BANK_A_ROI</u> <u>2_XMIN LSB[</u> <u>7:0]</u>								BANK_A_ROI2_XMIN_LSB[7:0]
0x 30 81	0 x 0 0	<u>BANK_A_ROI</u> <u>2_XMIN MSB</u> <u>[7:0]</u>	-	-						BANK_A_ROI2_XMIN_MSB[5:0]
0x 30 82	0 x 0 0	<u>BANK_A_ROI</u> <u>2_XMAX LSB</u> <u>[7:0]</u>								BANK_A_ROI2_XMAX_LSB[7:0]
0x 30 83	0 x 0 0	<u>BANK_A_ROI</u> <u>2_XMAX MS</u> <u>B[7:0]</u>	-	-						BANK_A_ROI2_XMAX_MSB[5:0]
0x 30 84	0 x 0 0	<u>BANK_A_ROI</u> <u>2_YMIN LSB[</u> <u>7:0]</u>								BANK_A_ROI2_YMIN_LSB[7:0]

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB		
0x 30 85	0 x 0 0	<u>BANK_A_ROI</u> <u>2_YMIN_MSB</u> <u>[7:0]</u>	-	-	BANK_A_ROI2_YMIN_MSB[5:0]							
0x 30 86	0 x 0 0	<u>BANK_A_ROI</u> <u>2_YMAX_LSB</u> <u>[7:0]</u>			BANK_A_ROI2_YMAX_LSB[7:0]							
BANK_A_ROI_2_COLOR_0												
0x 30 88	0 x 0 0	<u>BANK_A_ROI</u> <u>2_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	BANK_A_ROI2_COLOR_SELECT[2:0]			
0x 30 89	0 x 0 0	<u>BANK_A_ROI</u> <u>2_COLOR_MI</u> <u>N_THR LSB[7:0]</u>			BANK_A_ROI2_COLOR_MIN_THR_LSB[7:0]							
0x 30 8A	0 x 0 0	<u>BANK_A_ROI</u> <u>2_COLOR_MI</u> <u>N_THR MSB[7:0]</u>			BANK_A_ROI2_COLOR_MIN_THR_MSB[7:0]							
0x 30 8B	0 x F F	<u>BANK_A_ROI</u> <u>2_COLOR_M</u> <u>AX THR LSB[7:0]</u>			BANK_A_ROI2_COLOR_MAX_THR_LSB[7:0]							
0x 30 8C	0 x F F	<u>BANK_A_ROI</u> <u>2_COLOR_M</u> <u>AX THR MSB[7:0]</u>			BANK_A_ROI2_COLOR_MAX_THR_MSB[7:0]							
0x 30 8D	0 x 0 0	<u>BANK_A_ROI</u> <u>2_COLOR_C</u> <u>OUNT LSB[7:0]</u>			BANK_A_ROI2_COLOR_COUNT_LSB[7:0]							
0x 30 8E	0 x 0 0	<u>BANK_A_ROI</u> <u>2_COLOR_C</u> <u>OUNT MSB[7:0]</u>			BANK_A_ROI2_COLOR_COUNT_MSB[7:0]							

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
BANK_A_ROI_2_COLOR 1										
0x 30 90	0 x 0 0	<u>BANK A ROI</u> <u>2 COLOR S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_A_ROI2_COLOR_SELECT[2:0]
0x 30 91	0 x 0 0	<u>BANK A ROI</u> <u>2 COLOR MI</u> <u>N THR LSB[7:0]</u>								BANK_A_ROI2_COLOR_MIN_THR_LSB[7:0]
0x 30 92	0 x 0 0	<u>BANK A ROI</u> <u>2 COLOR MI</u> <u>N THR MSB[7:0]</u>								BANK_A_ROI2_COLOR_MIN_THR_MSB[7:0]
0x 30 93	0 x F F	<u>BANK A ROI</u> <u>2 COLOR M</u> <u>AX THR LSB[7:0]</u>								BANK_A_ROI2_COLOR_MAX_THR_LSB[7:0]
0x 30 94	0 x F F	<u>BANK A ROI</u> <u>2 COLOR M</u> <u>AX THR MSB[7:0]</u>								BANK_A_ROI2_COLOR_MAX_THR_MSB[7:0]
0x 30 95	0 x 0 0	<u>BANK A ROI</u> <u>2 COLOR C</u> <u>OUNT LSB[7:0]</u>								BANK_A_ROI2_COLOR_COUNT_LSB[7:0]
0x 30 96	0 x 0 0	<u>BANK A ROI</u> <u>2 COLOR C</u> <u>OUNT MSB[7:0]</u>								BANK_A_ROI2_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_2_COLOR 2										
0x 30 98	0 x 0 0	<u>BANK A ROI</u> <u>2 COLOR S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_A_ROI2_COLOR_SELECT[2:0]
0x 30 99	0 x	<u>BANK A ROI</u> <u>2 COLOR MI</u>								BANK_A_ROI2_COLOR_MIN_THR_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0	N THR LSB[7:0]								
0x 30 9A	0 x 0 0	BANK A ROI 2 COLOR MI N THR MSB[7:0]								BANK_A_ROI2_COLOR_MIN_THR_MSB[7:0]
0x 30 9B	0 x F F	BANK A ROI 2 COLOR M AX THR LSB [7:0]								BANK_A_ROI2_COLOR_MAX_THR_LSB[7:0]
0x 30 9C	0 x F F	BANK A ROI 2 COLOR M AX THR MS B[7:0]								BANK_A_ROI2_COLOR_MAX_THR_MSB[7:0]
0x 30 9D	0 x 0 0	BANK A ROI 2 COLOR C OUNT LSB[7: 0]								BANK_A_ROI2_COLOR_COUNT_LSB[7:0]
0x 30 9E	0 x 0 0	BANK A ROI 2 COLOR C OUNT MSB[7: 0]								BANK_A_ROI2_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_COORDINATES 3										
0x 30 A0	0 x 0 0	BANK A ROI 3 XMIN LSB[7:0]								BANK_A_ROI3_XMIN_LSB[7:0]
0x 30 A1	0 x 0 0	BANK A ROI 3 XMIN MSB [7:0]	-	-						BANK_A_ROI3_XMIN_MSB[5:0]
0x 30 A2	0 x 0 0	BANK A ROI 3 XMAX LSB [7:0]								BANK_A_ROI3_XMAX_LSB[7:0]

GMSL3/2 eDP Deserializers with
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Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB		
0x 30 A3	0 x 0 0	<u>BANK_A_ROI</u> <u>3_XMAX_MS</u> <u>B[7:0]</u>	-	-	BANK_A_ROI3_XMAX_MSB[5:0]							
0x 30 A4	0 x 0 0	<u>BANK_A_ROI</u> <u>3_YMIN LSB</u> <u>I7:0]</u>			BANK_A_ROI3_YMIN_LSB[7:0]							
0x 30 A5	0 x 0 0	<u>BANK_A_ROI</u> <u>3_YMIN MSB</u> <u>I7:0]</u>	-	-	BANK_A_ROI3_YMIN_MSB[5:0]							
0x 30 A6	0 x 0 0	<u>BANK_A_ROI</u> <u>3_YMAX LSB</u> <u>I7:0]</u>			BANK_A_ROI3_YMAX_LSB[7:0]							
0x 30 A7	0 x 0 0	<u>BANK_A_ROI</u> <u>3_YMAX MS</u> <u>B[7:0]</u>	-	-	BANK_A_ROI3_YMAX_MSB[5:0]							
BANK_A_ROI_3_COLOR 0												
0x 30 A8	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	BANK_A_ROI3_COLOR_SELECT[2:0]			
0x 30 A9	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_MI</u> <u>N THR LSB</u> <u>I7:0]</u>			BANK_A_ROI3_COLOR_MIN_THR_LSB[7:0]							
0x 30 AA	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_MI</u> <u>N THR MSB</u> <u>I7:0]</u>			BANK_A_ROI3_COLOR_MIN_THR_MSB[7:0]							
0x 30 AB	0 x F F	<u>BANK_A_ROI</u> <u>3_COLOR_M</u> <u>AX THR LSB</u> <u>I7:0]</u>			BANK_A_ROI3_COLOR_MAX_THR_LSB[7:0]							

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GMSL3/2 eDP Deserializers with
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Daisy Chain, and Ethernet

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A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 A C	0 x F F	<u>BANK_A_ROI</u> <u>3_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_A_ROI3_COLOR_MAX_THR_MSB[7:0]
0x 30 A D	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_C</u> <u>OUNT LSB[7:</u> <u>0]</u>								BANK_A_ROI3_COLOR_COUNT_LSB[7:0]
0x 30 AE	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_C</u> <u>OUNT MSB[7</u> <u>:0]</u>								BANK_A_ROI3_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_3_COLOR 1										
0x 30 B0	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_A_ROI3_COLOR_SELECT[2:0]
0x 30 B1	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_M</u> <u>IN THR LSB[</u> <u>7:0]</u>								BANK_A_ROI3_COLOR_MIN_THR_LSB[7:0]
0x 30 B2	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_M</u> <u>IN THR MSB[</u> <u>7:0]</u>								BANK_A_ROI3_COLOR_MIN_THR_MSB[7:0]
0x 30 B3	0 x F F	<u>BANK_A_ROI</u> <u>3_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>								BANK_A_ROI3_COLOR_MAX_THR_LSB[7:0]
0x 30 B4	0 x F F	<u>BANK_A_ROI</u> <u>3_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_A_ROI3_COLOR_MAX_THR_MSB[7:0]
0x 30 B5	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_C</u> <u>OUNT LSB[7:</u> <u>0]</u>								BANK_A_ROI3_COLOR_COUNT_LSB[7:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
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MAX96860/MAX96862/MAX96864

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A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 B6	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_C</u> <u>OUNT_MSB[7:0]</u>								BANK_A_ROI3_COLOR_COUNT_MSB[7:0]
BANK_A_ROI_3_COLOR 2										
0x 30 B8	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-			BANK_A_ROI3_COLOR_SELECT[2:0]
0x 30 B9	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_MI</u> <u>N_THR LSB[7:0]</u>								BANK_A_ROI3_COLOR_MIN_THR LSB[7:0]
0x 30 BA	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_MI</u> <u>N_THR_MSB[7:0]</u>								BANK_A_ROI3_COLOR_MIN_THR_MSB[7:0]
0x 30 BB	0 x F F	<u>BANK_A_ROI</u> <u>3_COLOR_M</u> <u>AX_THR LSB[7:0]</u>								BANK_A_ROI3_COLOR_MAX_THR LSB[7:0]
0x 30 BC	0 x F F	<u>BANK_A_ROI</u> <u>3_COLOR_M</u> <u>AX_THR MSB[7:0]</u>								BANK_A_ROI3_COLOR_MAX_THR MSB[7:0]
0x 30 BD	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_C</u> <u>OUNT_LSB[7:0]</u>								BANK_A_ROI3_COLOR_COUNT LSB[7:0]
0x 30 BE	0 x 0 0	<u>BANK_A_ROI</u> <u>3_COLOR_C</u> <u>OUNT_MSB[7:0]</u>								BANK_A_ROI3_COLOR_COUNT_MSB[7:0]
TELLTALE_BANK_B										
0x 30 C0	0 x	<u>BANK_B_ST</u> <u>ATUS[7:0]</u>	-	-	-	-	-	BANK_B_C ALC_DONE	BANK_B_FRAME_COUNT[1:0]	

GMSL3/2 eDP Deserializers with
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A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x 30 C1	0 x 0 0	<u>BANK_B_ROI</u> <u>1_0_ERROR</u> [7:0]	-	BANK_B_R OI_1_COL OR_2_ERR OR	BANK_B_ROI _1_COLOR_1 _ERROR	BANK_B_RO I_1_COLOR_0 _ERROR	-	BANK_B_R OI_0_COLO R_2_ERRO R	BANK_B_RO I_0_COLOR_1 _ERROR	BANK_B_R OI_0_COLO R_0_ERRO R
0x 30 C2	0 x 0 0	<u>BANK_B_ROI</u> <u>3_2_ERROR</u> [7:0]	-	BANK_B_R OI_3_COL OR_2_ERR OR	BANK_B_ROI _3_COLOR_1 _ERROR	BANK_B_RO I_3_COLOR_0 _ERROR	-	BANK_B_R OI_2_COLO R_2_ERRO R	BANK_B_RO I_2_COLOR_1 _ERROR	BANK_B_R OI_2_COLO R_0_ERRO R
BANK_B_ROI_COORDINATES 0										
0x 30 C8	0 x 0 0	<u>BANK_B_ROI</u> <u>0_XMIN LSB</u> [7:0]								BANK_B_ROI0_XMIN_LSB[7:0]
0x 30 C9	0 x 0 0	<u>BANK_B_ROI</u> <u>0_XMIN MSB</u> [7:0]	-	-						BANK_B_ROI0_XMIN_MSB[5:0]
0x 30 CA	0 x 0 0	<u>BANK_B_ROI</u> <u>0_XMAX LSB</u> [7:0]								BANK_B_ROI0_XMAX_LSB[7:0]
0x 30 CB	0 x 0 0	<u>BANK_B_ROI</u> <u>0_XMAX MSB</u> [7:0]	-	-						BANK_B_ROI0_XMAX_MSB[5:0]
0x 30 CC	0 x 0 0	<u>BANK_B_ROI</u> <u>0_YMIN LSB</u> [7:0]								BANK_B_ROI0_YMIN_LSB[7:0]
0x 30 CD	0 x 0 0	<u>BANK_B_ROI</u> <u>0_YMIN MSB</u> [7:0]	-	-						BANK_B_ROI0_YMIN_MSB[5:0]

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A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 C E	0 x 0 0	<u>BANK_B_ROI</u> <u>0_YMAX_LSB</u> <u>[7:0]</u>								BANK_B_ROI0_YMAX_LSB[7:0]
0x 30 CF	0 x 0 0	<u>BANK_B_ROI</u> <u>0_YMAX_MS</u> <u>B[7:0]</u>	-	-						BANK_B_ROI0_YMAX_MSB[5:0]
BANK_B_ROI_0_COLOR 0										
0x 30 D0	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-			BANK_B_ROI0_COLOR_SELECT[2:0]
0x 30 D1	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_MI</u> <u>N_THR LSB[7:0]</u>								BANK_B_ROI0_COLOR_MIN_THR_LSB[7:0]
0x 30 D2	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_MI</u> <u>N_THR_MSB[7:0]</u>								BANK_B_ROI0_COLOR_MIN_THR_MSB[7:0]
0x 30 D3	0 x F F	<u>BANK_B_ROI</u> <u>0_COLOR_M</u> <u>AX THR LSB[7:0]</u>								BANK_B_ROI0_COLOR_MAX_THR_LSB[7:0]
0x 30 D4	0 x F F	<u>BANK_B_ROI</u> <u>0_COLOR_M</u> <u>AX THR MSB[7:0]</u>								BANK_B_ROI0_COLOR_MAX_THR_MSB[7:0]
0x 30 D5	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_C</u> <u>OUNT LSB[7:0]</u>								BANK_B_ROI0_COLOR_COUNT_LSB[7:0]
0x 30 D6	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_C</u> <u>OUNT MSB[7:0]</u>								BANK_B_ROI0_COLOR_COUNT_MSB[7:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
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PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
BANK_B_ROI_0_COLOR 1										
0x 30 D8	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_B_ROI0_COLOR_SELECT[2:0]
0x 30 D9	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_MI</u> <u>N THR LSB[7:0]</u>								BANK_B_ROI0_COLOR_MIN_THR_LSB[7:0]
0x 30 D0 A0	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_MI</u> <u>N THR MSB[7:0]</u>								BANK_B_ROI0_COLOR_MIN_THR_MSB[7:0]
0x 30 D B	0 x F F	<u>BANK_B_ROI</u> <u>0_COLOR_M</u> <u>AX THR LSB[7:0]</u>								BANK_B_ROI0_COLOR_MAX_THR_LSB[7:0]
0x 30 D C	0 x F F	<u>BANK_B_ROI</u> <u>0_COLOR_M</u> <u>AX THR MSB[7:0]</u>								BANK_B_ROI0_COLOR_MAX_THR_MSB[7:0]
0x 30 D D	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_C</u> <u>OUNT LSB[7:0]</u>								BANK_B_ROI0_COLOR_COUNT_LSB[7:0]
0x 30 D E	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_C</u> <u>OUNT MSB[7:0]</u>								BANK_B_ROI0_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_0_COLOR 2										
0x 30 E0	0 x 0 0	<u>BANK_B_ROI</u> <u>0_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_B_ROI0_COLOR_SELECT[2:0]
0x 30 E1	0 x	<u>BANK_B_ROI</u> <u>0_COLOR_MI</u>								BANK_B_ROI0_COLOR_MIN_THR_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0	N THR LSB[7:0]								
0x 30 E2	0 x 0 0	BANK_B_ROI 0_COLOR_MI N THR MSB[7:0]								BANK_B_ROI0_COLOR_MIN_THR_MSB[7:0]
0x 30 E3	0 x F F	BANK_B_ROI 0_COLOR_M AX THR LSB [7:0]								BANK_B_ROI0_COLOR_MAX_THR_LSB[7:0]
0x 30 E4	0 x F F	BANK_B_ROI 0_COLOR_M AX THR MS B[7:0]								BANK_B_ROI0_COLOR_MAX_THR_MSB[7:0]
0x 30 E5	0 x 0 0	BANK_B_ROI 0_COLOR_C OUNT LSB[7: 0]								BANK_B_ROI0_COLOR_COUNT_LSB[7:0]
0x 30 E6	0 x 0 0	BANK_B_ROI 0_COLOR_C OUNT MSB[7: 0]								BANK_B_ROI0_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_COORDINATES 1										
0x 30 E8	0 x 0 0	BANK_B_ROI 1_XMIN LSB[7:0]								BANK_B_ROI1_XMIN_LSB[7:0]
0x 30 E9	0 x 0 0	BANK_B_ROI 1_XMIN MSB [7:0]	-	-						BANK_B_ROI1_XMIN_MSB[5:0]
0x 30 EA	0 x 0 0	BANK_B_ROI 1_XMAX LSB [7:0]								BANK_B_ROI1_XMAX_LSB[7:0]

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A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 EB	0 x 0 0	<u>BANK_B_ROI</u> <u>1_XMAX_MS</u> <u>B[7:0]</u>	-	-	BANK_B_ROI1_XMAX_MSB[5:0]					
0x 30 EC	0 x 0 0	<u>BANK_B_ROI</u> <u>1_YMIN LSB</u> <u>[7:0]</u>	BANK_B_ROI1_YMIN_LSB[7:0]							
0x 30 ED	0 x 0 0	<u>BANK_B_ROI</u> <u>1_YMIN MSB</u> <u>[7:0]</u>	-	-	BANK_B_ROI1_YMIN_MSB[5:0]					
0x 30 EE	0 x 0 0	<u>BANK_B_ROI</u> <u>1_YMAX LSB</u> <u>[7:0]</u>	BANK_B_ROI1_YMAX_LSB[7:0]							
0x 30 EF	0 x 0 0	<u>BANK_B_ROI</u> <u>1_YMAX MS</u> <u>B[7:0]</u>	-	-	BANK_B_ROI1_YMAX_MSB[5:0]					
BANK_B_ROI_1_COLOR 0										
0x 30 F0	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	BANK_B_ROI1_COLOR_SELECT[2:0]	
0x 30 F1	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_MI</u> <u>N THR LSB</u> <u>[7:0]</u>	BANK_B_ROI1_COLOR_MIN_THR_LSB[7:0]							
0x 30 F2	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_MI</u> <u>N THR MSB</u> <u>[7:0]</u>	BANK_B_ROI1_COLOR_MIN_THR_MSB[7:0]							
0x 30 F3	0 x F F	<u>BANK_B_ROI</u> <u>1_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>	BANK_B_ROI1_COLOR_MAX_THR_LSB[7:0]							

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 F4	0 x F F	<u>BANK_B_ROI</u> <u>1_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_B_ROI1_COLOR_MAX_THR_MSB[7:0]
0x 30 F5	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_C</u> <u>OUNT LSB[7:</u> <u>0]</u>								BANK_B_ROI1_COLOR_COUNT_LSB[7:0]
0x 30 F6	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_C</u> <u>OUNT MSB[7</u> <u>:0]</u>								BANK_B_ROI1_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_1_COLOR 1										
0x 30 F8	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	-	BANK_B_ROI1_COLOR_SELECT[2:0]
0x 30 F9	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_M</u> <u>IN THR LSB[</u> <u>7:0]</u>								BANK_B_ROI1_COLOR_MIN_THR_LSB[7:0]
0x 30 FA	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_M</u> <u>IN THR MSB[</u> <u>7:0]</u>								BANK_B_ROI1_COLOR_MIN_THR_MSB[7:0]
0x 30 FB	0 x F F	<u>BANK_B_ROI</u> <u>1_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>								BANK_B_ROI1_COLOR_MAX_THR_LSB[7:0]
0x 30 FC	0 x F F	<u>BANK_B_ROI</u> <u>1_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_B_ROI1_COLOR_MAX_THR_MSB[7:0]
0x 30 FD	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_C</u> <u>OUNT LSB[7:</u> <u>0]</u>								BANK_B_ROI1_COLOR_COUNT_LSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 30 FE	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_C</u> <u>OUNT_MSB[7:0]</u>								BANK_B_ROI1_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_1_COLOR 2										
0x 31 00	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_S</u> <u>ELECT[7:0]</u>		-	-	-	-	-		BANK_B_ROI1_COLOR_SELECT[2:0]
0x 31 01	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_MI</u> <u>N_THR LSB[7:0]</u>								BANK_B_ROI1_COLOR_MIN_THR LSB[7:0]
0x 31 02	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_MI</u> <u>N_THR_MSB[7:0]</u>								BANK_B_ROI1_COLOR_MIN_THR_MSB[7:0]
0x 31 03	0 x F F	<u>BANK_B_ROI</u> <u>1_COLOR_M</u> <u>AX_THR LSB[7:0]</u>								BANK_B_ROI1_COLOR_MAX_THR LSB[7:0]
0x 31 04	0 x F F	<u>BANK_B_ROI</u> <u>1_COLOR_M</u> <u>AX_THR MSB[7:0]</u>								BANK_B_ROI1_COLOR_MAX_THR_MSB[7:0]
0x 31 05	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_C</u> <u>OUNT_LSB[7:0]</u>								BANK_B_ROI1_COLOR_COUNT_LSB[7:0]
0x 31 06	0 x 0 0	<u>BANK_B_ROI</u> <u>1_COLOR_C</u> <u>OUNT_MSB[7:0]</u>								BANK_B_ROI1_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_COORDINATES 2										
0x 31 08	0 x	<u>BANK_B_ROI</u> <u>2_XMIN LSB[7:0]</u>								BANK_B_ROI2_XMIN LSB[7:0]

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB		
	0 0											
0x 31 09	0 x 0 0	<u>BANK_B_ROI</u> <u>2_XMIN_MSB</u> <u>[7:0]</u>	-	-	BANK_B_ROI2_XMIN_MSB[5:0]							
0x 31 0A	0 x 0 0	<u>BANK_B_ROI</u> <u>2_XMAX_LSB</u> <u>[7:0]</u>	BANK_B_ROI2_XMAX_LSB[7:0]									
0x 31 0B	0 x 0 0	<u>BANK_B_ROI</u> <u>2_XMAX_MS</u> <u>B[7:0]</u>	-	-	BANK_B_ROI2_XMAX_MSB[5:0]							
0x 31 0C	0 x 0 0	<u>BANK_B_ROI</u> <u>2_YMIN_LSB</u> <u>[7:0]</u>	BANK_B_ROI2_YMIN_LSB[7:0]									
0x 31 0D	0 x 0 0	<u>BANK_B_ROI</u> <u>2_YMIN_MSB</u> <u>[7:0]</u>	-	-	BANK_B_ROI2_YMIN_MSB[5:0]							
0x 31 0E	0 x 0 0	<u>BANK_B_ROI</u> <u>2_YMAX_LSB</u> <u>[7:0]</u>	BANK_B_ROI2_YMAX_LSB[7:0]									
0x 31 0F	0 x 0 0	<u>BANK_B_ROI</u> <u>2_YMAX_MS</u> <u>B[7:0]</u>	-	-	BANK_B_ROI2_YMAX_MSB[5:0]							
BANK_B_ROI_2_COLOR 0												
0x 31 10	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	BANK_B_ROI2_COLOR_SELECT[2:0]			

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 31 11	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_MI</u> <u>N THR LSB[</u> <u>7:0]</u>								BANK_B_ROI2_COLOR_MIN_THR_LSB[7:0]
0x 31 12	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_MI</u> <u>N THR MSB[</u> <u>7:0]</u>								BANK_B_ROI2_COLOR_MIN_THR_MSB[7:0]
0x 31 13	0 x F F	<u>BANK_B_ROI</u> <u>2_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>								BANK_B_ROI2_COLOR_MAX_THR_LSB[7:0]
0x 31 14	0 x F F	<u>BANK_B_ROI</u> <u>2_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_B_ROI2_COLOR_MAX_THR_MSB[7:0]
0x 31 15	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_C</u> <u>OUNT LSB[7:</u> <u>0]</u>								BANK_B_ROI2_COLOR_COUNT_LSB[7:0]
0x 31 16	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_C</u> <u>OUNT MSB[7</u> <u>:0]</u>								BANK_B_ROI2_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_2_COLOR 1										
0x 31 18	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-		BANK_B_ROI2_COLOR_SELECT[2:0]
0x 31 19	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_MI</u> <u>N THR LSB[</u> <u>7:0]</u>								BANK_B_ROI2_COLOR_MIN_THR_LSB[7:0]
0x 31 1A	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_MI</u> <u>N THR MSB[</u> <u>7:0]</u>								BANK_B_ROI2_COLOR_MIN_THR_MSB[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 31 1B	0 x F F	<u>BANK_B_ROI</u> <u>2_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>								BANK_B_ROI2_COLOR_MAX_THR_LSB[7:0]
0x 31 1C	0 x F F	<u>BANK_B_ROI</u> <u>2_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_B_ROI2_COLOR_MAX_THR_MSB[7:0]
0x 31 1D	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_C</u> <u>COUNT LSB[7:</u> <u>0]</u>								BANK_B_ROI2_COLOR_COUNT_LSB[7:0]
0x 31 1E	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_C</u> <u>COUNT MSB[7</u> <u>:0]</u>								BANK_B_ROI2_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_2_COLOR 2										
0x 31 20	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-		BANK_B_ROI2_COLOR_SELECT[2:0]
0x 31 21	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_MI</u> <u>N THR LSB[</u> <u>7:0]</u>								BANK_B_ROI2_COLOR_MIN_THR_LSB[7:0]
0x 31 22	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_MI</u> <u>N THR MSB[</u> <u>7:0]</u>								BANK_B_ROI2_COLOR_MIN_THR_MSB[7:0]
0x 31 23	0 x F F	<u>BANK_B_ROI</u> <u>2_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>								BANK_B_ROI2_COLOR_MAX_THR_LSB[7:0]
0x 31 24	0 x F F	<u>BANK_B_ROI</u> <u>2_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_B_ROI2_COLOR_MAX_THR_MSB[7:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 31 25	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_C</u> <u>OUNT LSB[7:0]</u>								BANK_B_ROI2_COLOR_COUNT_LSB[7:0]
0x 31 26	0 x 0 0	<u>BANK_B_ROI</u> <u>2_COLOR_C</u> <u>OUNT MSB[7:0]</u>								BANK_B_ROI2_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_COORDINATES 3										
0x 31 28	0 x 0 0	<u>BANK_B_ROI</u> <u>3_XMIN LSB[7:0]</u>								BANK_B_ROI3_XMIN_LSB[7:0]
0x 31 29	0 x 0 0	<u>BANK_B_ROI</u> <u>3_XMIN MSB[7:0]</u>	-	-						BANK_B_ROI3_XMIN_MSB[5:0]
0x 31 2A	0 x 0 0	<u>BANK_B_ROI</u> <u>3_XMAX LSB[7:0]</u>								BANK_B_ROI3_XMAX_LSB[7:0]
0x 31 2B	0 x 0 0	<u>BANK_B_ROI</u> <u>3_XMAX MSB[7:0]</u>	-	-						BANK_B_ROI3_XMAX_MSB[5:0]
0x 31 2C	0 x 0 0	<u>BANK_B_ROI</u> <u>3_YMIN LSB[7:0]</u>								BANK_B_ROI3_YMIN_LSB[7:0]
0x 31 2D	0 x 0 0	<u>BANK_B_ROI</u> <u>3_YMIN MSB[7:0]</u>	-	-						BANK_B_ROI3_YMIN_MSB[5:0]
0x 31 2E	0 x 0 0	<u>BANK_B_ROI</u> <u>3_YMAX LSB[7:0]</u>								BANK_B_ROI3_YMAX_LSB[7:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 31 2F	0 x 0 0	<u>BANK_B_ROI</u> <u>3_YMAX_MS</u> <u>B[7:0]</u>	-	-	BANK_B_ROI3_YMAX_MSB[5:0]					
BANK_B_ROI_3_COLOR 0										
0x 31 30	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	BANK_B_ROI3_COLOR_SELECT[2:0]	
0x 31 31	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_MI</u> <u>N THR LSB[7:0]</u>	BANK_B_ROI3_COLOR_MIN_THR_LSB[7:0]							
0x 31 32	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_MI</u> <u>N THR MSB[7:0]</u>	BANK_B_ROI3_COLOR_MIN_THR_MSB[7:0]							
0x 31 33	0 x F F	<u>BANK_B_ROI</u> <u>3_COLOR_M</u> <u>AX THR LSB[7:0]</u>	BANK_B_ROI3_COLOR_MAX_THR_LSB[7:0]							
0x 31 34	0 x F F	<u>BANK_B_ROI</u> <u>3_COLOR_M</u> <u>AX THR MSB[7:0]</u>	BANK_B_ROI3_COLOR_MAX_THR_MSB[7:0]							
0x 31 35	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_C</u> <u>OUNT LSB[7:0]</u>	BANK_B_ROI3_COLOR_COUNT_LSB[7:0]							
0x 31 36	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_C</u> <u>OUNT MSB[7:0]</u>	BANK_B_ROI3_COLOR_COUNT_MSB[7:0]							
BANK_B_ROI_3_COLOR 1										
0x 31 38	0 x	<u>BANK_B_ROI</u> <u>3_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-	BANK_B_ROI3_COLOR_SELECT[2:0]	

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

A D D R E S S	R E S E T	NAME	MSB							LSB
	0 0									
0x 31 39	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_MI</u> <u>N_THR_LSB[</u> <u>7:0]</u>								BANK_B_ROI3_COLOR_MIN_THR LSB[7:0]
0x 31 3A	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_MI</u> <u>N_THR_MSB[</u> <u>7:0]</u>								BANK_B_ROI3_COLOR_MIN_THR_MSB[7:0]
0x 31 3B	0 x F F	<u>BANK_B_ROI</u> <u>3_COLOR_M</u> <u>AX_THR_LSB</u> <u>[7:0]</u>								BANK_B_ROI3_COLOR_MAX_THR_LSB[7:0]
0x 31 3C	0 x F F	<u>BANK_B_ROI</u> <u>3_COLOR_M</u> <u>AX_THR_MS</u> <u>B[7:0]</u>								BANK_B_ROI3_COLOR_MAX_THR_MSB[7:0]
0x 31 3D	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_C</u> <u>OUNT_LSB[7:</u> <u>0]</u>								BANK_B_ROI3_COLOR_COUNT_LSB[7:0]
0x 31 3E	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_C</u> <u>OUNT_MSB[7</u> <u>:0]</u>								BANK_B_ROI3_COLOR_COUNT_MSB[7:0]
BANK_B_ROI_3_COLOR 2										
0x 31 40	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_S</u> <u>ELECT[7:0]</u>	-	-	-	-	-	-		BANK_B_ROI3_COLOR_SELECT[2:0]
0x 31 41	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_MI</u> <u>N_THR_LSB[</u> <u>7:0]</u>								BANK_B_ROI3_COLOR_MIN_THR_LSB[7:0]

PRELIMINARY

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 31 42	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_MI</u> <u>N THR MSB[</u> <u>7:0]</u>								BANK_B_ROI3_COLOR_MIN_THR_MSB[7:0]
0x 31 43	0 x F F	<u>BANK_B_ROI</u> <u>3_COLOR_M</u> <u>AX THR LSB</u> <u>[7:0]</u>								BANK_B_ROI3_COLOR_MAX_THR_LSB[7:0]
0x 31 44	0 x F F	<u>BANK_B_ROI</u> <u>3_COLOR_M</u> <u>AX THR MS</u> <u>B[7:0]</u>								BANK_B_ROI3_COLOR_MAX_THR_MSB[7:0]
0x 31 45	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_C</u> <u>COUNT LSB[7:</u> <u>0]</u>								BANK_B_ROI3_COLOR_COUNT_LSB[7:0]
0x 31 46	0 x 0 0	<u>BANK_B_ROI</u> <u>3_COLOR_C</u> <u>COUNT MSB[7</u> <u>:0]</u>								BANK_B_ROI3_COLOR_COUNT_MSB[7:0]
DSC_DEC										
0x 45 20	0 x 0 0	<u>DEC_PPS0_3</u> <u>_B0[7:0]</u>		dsc_version_major[3:0]						dsc_version_minor[3:0]
0x 45 21	0 x 0 0	<u>DEC_PPS0_3</u> <u>_B1[7:0]</u>								pps_identifier[7:0]
0x 45 22	0 x 0 0	<u>DEC_PPS0_3</u> <u>_B2[7:0]</u>	-	-	-	-	-	-	-	-
0x 45 23	0 x 0 0	<u>DEC_PPS0_3</u> <u>_B3[7:0]</u>		bits_per_component[3:0]						linebuf_depth[3:0]

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 24	0 x 0 0	<u>DEC_PPS4_7</u> <u>_B0[7:0]</u>	–	–	block_pred_enable	convert_rgb	simple_422	vbr_enable	bits_per_pixel_h[1:0]	
0x 45 25	0 x 0 0	<u>DEC_PPS4_7</u> <u>_B1[7:0]</u>							bits_per_pixel_l[7:0]	
0x 45 26	0 x 0 0	<u>DEC_PPS4_7</u> <u>_B2[7:0]</u>							pic_height_h[7:0]	
0x 45 27	0 x 0 0	<u>DEC_PPS4_7</u> <u>_B3[7:0]</u>							pic_height_l[7:0]	
0x 45 28	0 x 0 0	<u>DEC_PPS8_1</u> <u>_B0[7:0]</u>							pic_width_h[7:0]	
0x 45 29	0 x 0 0	<u>DEC_PPS8_1</u> <u>_B1[7:0]</u>							pic_width_l[7:0]	
0x 45 2A	0 x 0 0	<u>DEC_PPS8_1</u> <u>_B2[7:0]</u>							slice_height_h[7:0]	
0x 45 2B	0 x 0 0	<u>DEC_PPS8_1</u> <u>_B3[7:0]</u>							slice_height_l[7:0]	
0x 45 2C	0 x 0 0	<u>DEC_PPS12</u> <u>_B0[7:0]</u>							slice_width_h[7:0]	

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 2D	0 x 0 0	<u>DEC_PPS12_15_B1[7:0]</u>								slice_width_l[7:0]
0x 45 2E	0 x 0 0	<u>DEC_PPS12_15_B2[7:0]</u>								chunk_size_h[7:0]
0x 45 2F	0 x 0 0	<u>DEC_PPS12_15_B3[7:0]</u>								chunk_size_l[7:0]
0x 45 30	0 x 0 0	<u>DEC_PPS16_19_B0[7:0]</u>	-	-	-	-	-	-	-	initial_xmit_delay_h[1:0]
0x 45 31	0 x 0 0	<u>DEC_PPS16_19_B1[7:0]</u>								initial_xmit_delay_l[7:0]
0x 45 32	0 x 0 0	<u>DEC_PPS16_19_B2[7:0]</u>								initial_dec_delay_h[7:0]
0x 45 33	0 x 0 0	<u>DEC_PPS16_19_B3[7:0]</u>								initial_dec_delay_l[7:0]
0x 45 35	0 x 0 0	<u>DEC_PPS20_23_B1[7:0]</u>	-	-						initial_scale_value[5:0]
0x 45 36	0 x 0 0	<u>DEC_PPS20_23_B2[7:0]</u>								scale_increment_interval_h[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 37	0 x 0 0	<u>DEC_PPS20</u> <u>23_B3[7:0]</u>								scale_increment_interval_l[7:0]
0x 45 38	0 x 0 0	<u>DEC_PPS24</u> <u>27_B0[7:0]</u>		-	-	-	-			scale_decrement_interval_h[3:0]
0x 45 39	0 x 0 0	<u>DEC_PPS24</u> <u>27_B1[7:0]</u>								scale_decrement_interval_l[7:0]
0x 45 3B	0 x 0 0	<u>DEC_PPS24</u> <u>27_B3[7:0]</u>		-	-	-				first_line_bpg_offset[4:0]
0x 45 3C	0 x 0 0	<u>DEC_PPS28</u> <u>31_B0[7:0]</u>								nfl_bpg_offset_h[7:0]
0x 45 3D	0 x 0 0	<u>DEC_PPS28</u> <u>31_B1[7:0]</u>								nfl_bpg_offset_l[7:0]
0x 45 3E	0 x 0 0	<u>DEC_PPS28</u> <u>31_B2[7:0]</u>								slice_bpg_offset_h[7:0]
0x 45 3F	0 x 0 0	<u>DEC_PPS28</u> <u>31_B3[7:0]</u>								slice_bpg_offset_l[7:0]
0x 45 40	0 x 0 0	<u>DEC_PPS32</u> <u>35_B0[7:0]</u>								initial_offset_h[7:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 41	0 x 0 0	<u>DEC_PPS32</u> <u>35_B1[7:0]</u>								initial_offset_l[7:0]
0x 45 42	0 x 0 0	<u>DEC_PPS32</u> <u>35_B2[7:0]</u>								final_offset_h[7:0]
0x 45 43	0 x 0 0	<u>DEC_PPS32</u> <u>35_B3[7:0]</u>								final_offset_l[7:0]
0x 45 44	0 x 0 0	<u>DEC_PPS36</u> <u>39_B0[7:0]</u>	-	-	-					flatness_min_qp[4:0]
0x 45 45	0 x 0 0	<u>DEC_PPS36</u> <u>39_B1[7:0]</u>	-	-	-					flatness_max_qp[4:0]
0x 45 46	0 x 0 0	<u>DEC_PPS36</u> <u>39_B2[7:0]</u>				rc_model_size_h[7:0]				
0x 45 47	0 x 0 0	<u>DEC_PPS36</u> <u>39_B3[7:0]</u>				rc_model_size_l[7:0]				
0x 45 48	0 x 0 0	<u>DEC_PPS40</u> <u>43_B0[7:0]</u>	-	-	-	-				rc_edge_factor[3:0]
0x 45 49	0 x 0 0	<u>DEC_PPS40</u> <u>43_B1[7:0]</u>	-	-	-					rc_quant_incr_limit0[4:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB				
0x 45 4A	0 x 0 0	<u>DEC_PPS40</u> <u>43_B2[7:0]</u>	-	-	-	rc_quant_incr_limit1[4:0]								
0x 45 4B	0 x 0 0	<u>DEC_PPS40</u> <u>43_B3[7:0]</u>	rc_tgt_offset_hi[3:0]				rc_tgt_offset_lo[3:0]							
0x 45 4C	0 x 0 0	<u>DEC_PPS44</u> <u>47_B0[7:0]</u>	rc_buff_thresh0[7:0]											
0x 45 4D	0 x 0 0	<u>DEC_PPS44</u> <u>47_B1[7:0]</u>	rc_buf_thresh1[7:0]											
0x 45 4E	0 x 0 0	<u>DEC_PPS44</u> <u>47_B2[7:0]</u>	rc_buf_thresh2[7:0]											
0x 45 4F	0 x 0 0	<u>DEC_PPS44</u> <u>47_B3[7:0]</u>	rc_buf_thresh3[7:0]											
0x 45 50	0 x 0 0	<u>DEC_PPS48</u> <u>51_B0[7:0]</u>	rc_buf_thresh4[7:0]											
0x 45 51	0 x 0 0	<u>DEC_PPS48</u> <u>51_B1[7:0]</u>	rc_buf_thresh5[7:0]											
0x 45 52	0 x 0 0	<u>DEC_PPS48</u> <u>51_B2[7:0]</u>	rc_buf_thresh6[7:0]											

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 53	0 x 0 0	<u>DEC_PPS48</u> <u>51_B3[7:0]</u>								rc_buf_thresh7[7:0]
0x 45 54	0 x 0 0	<u>DEC_PPS52</u> <u>55_B0[7:0]</u>								rc_buf_thresh8[7:0]
0x 45 55	0 x 0 0	<u>DEC_PPS52</u> <u>55_B1[7:0]</u>								rc_buf_thresh9[7:0]
0x 45 56	0 x 0 0	<u>DEC_PPS52</u> <u>55_B2[7:0]</u>								rc_buf_thresh10[7:0]
0x 45 57	0 x 0 0	<u>DEC_PPS52</u> <u>55_B3[7:0]</u>								rc_buf_thresh11[7:0]
0x 45 58	0 x 0 0	<u>DEC_PPS56</u> <u>59_B0[7:0]</u>								rc_buf_thresh12[7:0]
0x 45 59	0 x 0 0	<u>DEC_PPS56</u> <u>59_B1[7:0]</u>								rc_buf_thresh13[7:0]
0x 45 5A	0 x 0 0	<u>DEC_PPS56</u> <u>59_B2[7:0]</u>			range_min_qp0[4:0]					range_max_qp0_h[2:0]
0x 45 5B	0 x 0 0	<u>DEC_PPS56</u> <u>59_B3[7:0]</u>		range_max_qp0_l[1:0]						range_bpg_offset0[5:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 5C	0 x 0 0	<u>DEC_PPS60</u> <u>63_B0[7:0]</u>		range_min_qp1[4:0]						range_max_qp1_h[2:0]
0x 45 5D	0 x 0 0	<u>DEC_PPS60</u> <u>63_B1[7:0]</u>		range_max_qp1_l[1:0]	range_bpg_offset1[5:0]					
0x 45 5E	0 x 0 0	<u>DEC_PPS60</u> <u>63_B2[7:0]</u>		range_min_qp2[4:0]						range_max_qp2_h[2:0]
0x 45 5F	0 x 0 0	<u>DEC_PPS60</u> <u>63_B3[7:0]</u>		range_max_qp2_l[1:0]	range_bpg_offset2[5:0]					
0x 45 60	0 x 0 0	<u>DEC_PPS64</u> <u>67_B0[7:0]</u>		range_min_qp3[4:0]						range_max_qp3_h[2:0]
0x 45 61	0 x 0 0	<u>DEC_PPS64</u> <u>67_B1[7:0]</u>		range_max_qp3_l[1:0]	range_bpg_offset3[5:0]					
0x 45 62	0 x 0 0	<u>DEC_PPS64</u> <u>67_B2[7:0]</u>		range_min_qp4[4:0]						range_max_qp4_h[2:0]
0x 45 63	0 x 0 0	<u>DEC_PPS64</u> <u>67_B3[7:0]</u>		range_max_qp4_l[1:0]	range_bpg_offset4[5:0]					
0x 45 64	0 x 0 0	<u>DEC_PPS68</u> <u>71_B0[7:0]</u>		range_min_qp5[4:0]						range_max_qp5_h[2:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 65	0 x 0 0	<u>DEC_PPS68</u> <u>71_B1[7:0]</u>		range_max_qp5_l[1:0]						range_bpg_offset5[5:0]
0x 45 66	0 x 0 0	<u>DEC_PPS68</u> <u>71_B2[7:0]</u>			range_min_qp6[4:0]					range_max_qp6_h[2:0]
0x 45 67	0 x 0 0	<u>DEC_PPS68</u> <u>71_B3[7:0]</u>		range_max_qp6_l[1:0]						range_bpg_offset6[5:0]
0x 45 68	0 x 0 0	<u>DEC_PPS72</u> <u>75_B0[7:0]</u>			range_min_qp7[4:0]					range_max_qp7_h[2:0]
0x 45 69	0 x 0 0	<u>DEC_PPS72</u> <u>75_B1[7:0]</u>		range_max_qp7_l[1:0]						range_bpg_offset7[5:0]
0x 45 6A	0 x 0 0	<u>DEC_PPS72</u> <u>75_B2[7:0]</u>			range_min_qp8[4:0]					range_max_qp8_h[2:0]
0x 45 6B	0 x 0 0	<u>DEC_PPS72</u> <u>75_B3[7:0]</u>		range_max_qp8_l[1:0]						range_bpg_offset8[5:0]
0x 45 6C	0 x 0 0	<u>DEC_PPS76</u> <u>79_B0[7:0]</u>			range_min_qp9[4:0]					range_max_qp9_h[2:0]
0x 45 6D	0 x 0 0	<u>DEC_PPS76</u> <u>79_B1[7:0]</u>		range_max_qp9_l[1:0]						range_bpg_offset9[5:0]

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 6E	0 x 0 0	<u>DEC_PPS76</u> <u>79_B2[7:0]</u>		range_min_qp10[4:0]						range_max_qp10_h[2:0]
0x 45 6F	0 x 0 0	<u>DEC_PPS76</u> <u>79_B3[7:0]</u>		range_max_qp10_l[1:0]	range_bpg_offset10[5:0]					
0x 45 70	0 x 0 0	<u>DEC_PPS80</u> <u>83_B0[7:0]</u>		range_min_qp11[4:0]						range_max_qp11_h[2:0]
0x 45 71	0 x 0 0	<u>DEC_PPS80</u> <u>83_B1[7:0]</u>		range_max_qp11_l[1:0]	range_bpg_offset11[5:0]					
0x 45 72	0 x 0 0	<u>DEC_PPS80</u> <u>83_B2[7:0]</u>		range_min_qp12[4:0]						range_max_qp12_h[2:0]
0x 45 73	0 x 0 0	<u>DEC_PPS80</u> <u>83_B3[7:0]</u>		range_max_qp12_l[1:0]	range_bpg_offset12[5:0]					
0x 45 74	0 x 0 0	<u>DEC_PPS84</u> <u>87_B0[7:0]</u>		range_min_qp13[4:0]						range_max_qp13_h[2:0]
0x 45 75	0 x 0 0	<u>DEC_PPS84</u> <u>87_B1[7:0]</u>		range_max_qp13_l[1:0]	range_bpg_offset13[5:0]					
0x 45 76	0 x 0 0	<u>DEC_PPS84</u> <u>87_B2[7:0]</u>		range_min_qp14[4:0]						range_max_qp14_h[2:0]

PRELIMINARY

PRELIMINARY

A D D R E S S	R E S E T	NAME	MSB							LSB
0x 45 77	0 x 0 0	<u>DEC_PPS84</u> <u>87_B3[7:0]</u>	range_max_qp14_l[1:0]							range_bpg_offset14[5:0]
0x 45 78	0 x 0 0	<u>DEC_PPS88</u> <u>91_B0[7:0]</u>		-	-	-	-	-	native_420	native_422
0x 45 79	0 x 0 0	<u>DEC_PPS88</u> <u>91_B1[7:0]</u>		-	-	-				second_line_bpg_offset[4:0]
0x 45 7A	0 x 0 0	<u>DEC_PPS88</u> <u>91_B2[7:0]</u>					nsl_bpg_offset_h[7:0]			
0x 45 7B	0 x 0 0	<u>DEC_PPS88</u> <u>91_B3[7:0]</u>					nsl_bpg_offset_l[7:0]			
0x 45 7C	0 x 0 0	<u>DEC_PPS92</u> <u>95_B0[7:0]</u>					second_line_offset_adj_h[7:0]			
0x 45 7D	0 x 0 0	<u>DEC_PPS92</u> <u>95_B1[7:0]</u>					second_line_offset_adj_l[7:0]			

Register Details

DEV_CFG_0 (0x0)

BIT	7	6	5	4	3	2	1	0	
Field	DEV_ADDR[6:0]								CFG_BLOCK
Reset	0b1001000								0b0

Access Type	Write, Read	Write, Read
--------------------	-------------	-------------

BITFIELD	BITS	DESCRIPTION	DECODE																		
DEV_ADDR	7:1	<p>Device Address for I²C or UART addressing Default value is set by the CFG0 pin encoded voltage level as follows:</p> <table> <thead> <tr> <th>CFG0 voltage level</th> <th>Device Address</th> </tr> </thead> <tbody> <tr><td>000</td><td>0b1001000</td></tr> <tr><td>001</td><td>0b1001010</td></tr> <tr><td>010</td><td>0b1001100</td></tr> <tr><td>011</td><td>0b1101000</td></tr> <tr><td>100</td><td>0b1101010</td></tr> <tr><td>101</td><td>0b1101100</td></tr> <tr><td>110</td><td>0b0101000</td></tr> <tr><td>111</td><td>0b0101010</td></tr> </tbody> </table>	CFG0 voltage level	Device Address	000	0b1001000	001	0b1001010	010	0b1001100	011	0b1101000	100	0b1101010	101	0b1101100	110	0b0101000	111	0b0101010	0b0000000: I ² C write/read address is 0x00/0x01 0b0000001: I ² C write/read address is 0x02/0x03 ... 0b1001000: I ² C write/read address is 0x90/0x91 0b1001010: I ² C write/read address is 0x94/0x95 0b1001100: I ² C write/read address is 0x98/0x99 0b1101000: I ² C write/read address is 0xD0/0xD1 0b1101010: I ² C write/read address is 0xD4/0xD5 0b1101100: I ² C write/read address is 0xD8/0xD9 0b0101000: I ² C write/read address is 0x50/0x51 0b0101010: I ² C write/read address is 0x54/0x55 0b1111111: I ² C write/read address is 0xFE/0xFF
CFG0 voltage level	Device Address																				
000	0b1001000																				
001	0b1001010																				
010	0b1001100																				
011	0b1101000																				
100	0b1101010																				
101	0b1101100																				
110	0b0101000																				
111	0b0101010																				
CFG_BLOCK	0	Sets all registers as read only to block further device configuration.	0: Configuration not blocked 1: Configuration blocked (all registers are read only)																		

DEV_CFG_1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK_ALL	RESET_LINK_SIOAB	RESET_LINK_SIOA	-	RESET_LINK_DCIO	-	-
Reset	0b0	0b0	0b0	0b0	-	0b0	-	-
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	-	Write, Read	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Resets all registers to default values and resets all blocks in device. Equivalent to toggling the PWDNB pin. This bit self-clears when written to a 1.	0b0: No action 0b1: Activate chip reset
RESET_LINK_ALL	6	Resets the GMSL links connected to SIOA, SIOB and DCIO. Register settings and other blocks are not reset. When set to 1, this bit holds the link in reset and does not self-clear. Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset or no action 0b1: Hold GMSL links in reset
RESET_LINK_SIOAB	5	Resets the GMSL links connected to SIOA and SIOB. Register settings and other blocks are not reset. When set to 1, this bit holds the link in reset and does not self-clear. Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset or no action 0b1: Hold GMSL links in reset
RESET_LINK_SIOA	4	Resets the GMSL link connected to SIOA. Register settings and other blocks are not reset. When set to 1, this bit holds the link in reset and	0b0: Release link reset or no action 0b1: Hold GMSL in reset

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		does not self-clear. Write 1 to activate reset, write 0 to release reset.	
RESET_LINK_DCIO	2	Resets the GMSL link connected to DCIO. Register settings and other blocks are not reset. When set to 1, this bit holds the link in reset and does not self-clear. Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset or no action 0b1: Hold GMSL link in reset

DEV_CFG_2 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	RESET_ONESHOT_ALL	RESET_ONESHOT_SIO_AB	RESET_ONESHOT_SI_OA	RESET_ONESHOT_SI_OB	RESET_ONESHOT_DCIO	-	-	-
Reset	0b0	0b0	0b0	0b0	0b0	-	-	-
Access Type	Write Clears All, Read	-	-	-				

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ONESHOT_ALL	7	Resets the GMSL links connected to SIOA, SIOB and DCIO (same as RESET_LINK_ALL). Register settings and other blocks are not reset. When set to 1, this bit resets the link and then self-clears to automatically release reset.	0b0: No action 0b1: Reset GMSL links
RESET_ONESHOT_SIOAB	6	Resets the GMSL links connected to SIOA and SIOB (same as RESET_LINK_ALL). Register settings and other blocks are not reset. When set to 1, this bit resets the link and then self-clears to automatically release reset.	0b0: No action 0b1: Reset GMSL links
RESET_ONESHOT_SI_OA	5	Resets the GMSL link connected to SIOA (same as RESET_LINK_ALL). Register settings and other blocks are not reset. When set to 1, this bit resets the link and then self-clears to automatically release reset.	0b0: No action 0b1: Reset GMSL link
RESET_ONESHOT_SI_OB	4	Resets the GMSL link connected to SIOB (same as RESET_LINK_ALL). Register settings and other blocks are not reset. When set to 1, this bit resets the link and then self-clears to automatically release reset.	0b0: No action 0b1: Reset GMSL link
RESET_ONESHOT_DCIO	3	Resets the GMSL link connected to DCIO (same as RESET_LINK_ALL). Register settings and other blocks are not reset. When set to 1, this bit resets the link and then self-clears to automatically release reset.	0b0: No action 0b1: Reset GMSL link

ERROR_STATUS_0 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	ERR_OUTPUT_STATUS	LINK_SIOA_ERR	LINK_SI_OB_ERR	LINK_DCIO_ERR	-	-	-	PSM_STATE_ERR

Reset	0b0	0b0	0b0	0b0	-	-	-	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	-	-	-	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_OUTPUT_STATUS	7	Overall error status that is output to ERRB pin if enabled (if ERR_OUTPUT_OEN = 1). This status is calculated by ANDing each error status (XXXX_ERR) with its corresponding output enable (XXXX_ERR_OEN), and ORing together all the outcomes (i.e., if any error and its corresponding output enable is high, this value will be high.)	0b0: No overall errors, ERRB pin will be driven high (if ERR_OUTPUT_OEN = 1). 0b1: There is an error, ERRB pin will be driven low (if ERR_OUTPUT_OEN = 1).
LINK_SIOA_ERR	6	Decode error status on received data on SIOA link. Cleared when DEC_ERROR_COUNT_SIOA at 0x31 is read or at rising edge of LOCK on SIOA.	0b0: No significant link errors on SIOA 0b1: Link errors exist on SIOA
LINK_SIOB_ERR	5	Decode error status on received data on SIOB link. Cleared when DEC_ERROR_COUNT_SIOB at 0x32 is read or at rising edge of LOCK on SIOB.	0b0: No significant link errors on SIOB 0b1: Link errors exist on SIOB
LINK_DCIO_ERR	4	Decode error status on received data on DCIO link. Cleared when DEC_ERROR_COUNT_DCIO at 0x33 is read or at rising edge of LOCK on DCIO link.	0b0: No significant link errors on DCIO 0b1: Link errors exist on DCIO
PSM_STATE_ERR	0	PSM (Programmable State Machine) Error Flag Asserted when programmable state machine signals it detected an error or when MBIST of ROM at startup failed. Cleared when PSM_STATE_STATUS_0 at 0xB6 is read.	0x0: Error flag not asserted 0x1: Error flag asserted

ERROR STATUS 1 (0x5)

BIT	7	6	5	4	3	2	1	0
Field	SIOA_FEC_ERR	SIOB_FEC_ERR	RETENTION_MEMORY_CRC_ERR	CONTROL_CHANNEL_MSG_COUNT_ERR	-	LINFAULT_0_ERR	LINFAULT_1_ERR	CLOCK_MONITOR_ERR
Reset	0b0	0b0	0b0	0b0	-	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	-	Read Only	Read Only	Read Clears All

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SIOA_FEC_ERR	7	FEC receiver error flag for SIOA link. Asserted when FEC receive errors exceed the threshold. Cleared on LOCK rising edge or by setting FEC_STATS_RESET_SIOA high.	0b0: Flag not asserted 0b1: Flag asserted
SIOB_FEC_ERR	6	FEC receiver error flag for SIOB link. Asserted when FEC receive errors exceed the threshold. Cleared on LOCK rising edge or by setting FEC_STATS_RESET_SIOB high.	0b0: Flag not asserted 0b1: Flag asserted
RETENTION_MEMORY_CRC_ERR	5	CRC check error detected on retention memory during restore operation	0b0: No error detected 0b1: Error detected
CONTROL_CHANNEL_MSG_COUNT_ERR	4	I ² C/UART message count error flag. Asserted when MSGCNTR_ERR_CNT is non-zero. Cleared when RESET_MSGCNTR_ERR_CNT at 0x11D is written with 1.	0b0: No error detected 0b1: Error detected
LINEFAULT_0_ERR	2	Line-fault status of wire connected to LMN0 pin. See register LINEFAULT_0_STATUS for fault condition.	0b0: No linefault error 0b1: Linefault error active
LINEFAULT_1_ERR	1	Line-fault status of wire connected to LMN1 pin. See register LINEFAULT_1_STATUS for fault condition.	0b0: No line-fault error 0b1: Line-fault error active
CLOCK_MONITOR_ERR	0	Discrepancy error detected between 25MHz reference clock frequency and 150MHz CMU clock.	0b0: No error detected 0b1: Error detected

ERROR STATUS 2 (0x6)

BIT	7	6	5	4	3	2	1	0
Field	REMOTE_E RR	ARQ_ER R	INFOFRAME_CRC_ ERR	VIDEO_PRBS_E RR	AUDIO_PRBS_E RR	OVERVOLTAGE_E RR	UNDERVOLTAGE_ ERR	-
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	-
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Clears All	Read Only	-

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
REMOTE_ERR	7	Received Remote GMSL Serializer Error Status (inverse of remote side ERRB pin level). Clear remote GMSL Serializer ERRB pin to clear this error status.	0b0: No remote side error 0b1: Remote side error
ARQ_ERR	6	ARQ retransmissions has exceeded threshold for 1 of the ARQ protected channels. Refer to the ARQ_STATUS_0 (0x71) register for details on which interface has caused this error. Cleared when MAX_RT_ERROR_RESET at 0x19B is written with 1.	0b0: No ARQ error 0b1: ARQ errors have exceeded the threshold for at least 1 of the channels
INFOFRAME_CRC_ERR	5	INFOFR CRC Error Flag. Asserted when INFOFR CRC error count > 0. Cleared when CRC_MISC_STATUS_1 at 0x6F is read.	0b0: No CRC errors 0b1: CRC error detected
VIDEO_PRBS_ERR	4	Video PRBS Error Flag Asserted when VPRBS_ERR > 0. Cleared when VPRBS_ERROR_COUNT at 0x8D and VPRBS_ERROR_COUNT_Y at 0x55B are read.	0b0: Flag not asserted 0b1: Flag asserted
AUDIO_PRBS_ERR	3	Audio PRBS Error Flag Asserted when APRBS_ERR (0x143) > 0. Read APRBS_ERROR_COUNT at 0x8E to clear.	0b0: Flag not asserted 0b1: Flag asserted
OVERVOLTAGE_ERR	2	V _{DD} Overvoltage Indication This bit stays high when asserted and must be cleared by the user. It is set when V _{DD} exceeds the overvoltage threshold. It is cleared when POWER_STATUS_0 at 0xBA is read. See OV_LEVEL register for overvoltage threshold value. Read this bitfield to clear. Reported when video is present.	0b0: Flag not asserted 0b1: Flag asserted
UNDERVOLTAGE_ERR	1	Undervoltage condition occurred on V _{DD} rail (V _{DD} < 0.806). Cleared when POWER_STATUS_0 is read.	0b0: No undervoltage condition 0b1: Undervoltage condition occurred on V _{DD} rail

ERROR STATUS 3 (0x7)

BIT	7	6	5	4	3	2	1	0
Field	VIDEOSEQUENC E_ERR	LOSSOFVIDEOLOC K_ERR	HDCPE RR	REGISTERCRC _ERR	DSC_E RR	WATERMARK_ ERR	VIDEOBLOCKLENGT H_ERR	-
Reset	0b0	0b0	0b0	0x0	0b0	0b0	0b0	-
Access Type	Read Only	Read Only	Read Only	Read Clears All	Read Only	Read Only	Read Clears All	-

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_SEQUENCE_ERR	7	Sequence error detected on received video packets. Cleared when VIDEO_STATUS_0 and VIDEO_STATUS_1 at 0x92, 0x93 are read.	0b0: Error not detected 0b1: Error detected
LOSS_OF_VIDEO_LOCK_ERR	6	Loss of video error is detected. Cleared when VIDEO_STATUS_0 at 0x92 is read.	0b0: No error detected 0b1: Error detected
HDCP_ERR	5	HDCP error detected. Triggered by video line CRC errors on 3 consecutive lines. Cleared when this ERROR_STATUS_3 is read.	0b0: No HDCP interrupt 0b1: HDCP interrupt
REGISTER_CRC_ERR	4	CRC check error detected on register block. Cleared when register RESET_CRC at 0x1F00 is written with 1.	0b0: No error detected 0b1: Error detected
DSC_ERR	3	DSC Decoder Error Flag Asserted when any DSC decoder error occurs. This flag is set by assertion of any bit in DSC_STATUS. This flag is cleared when DSC_STATUS_0 at 0x8A is read.	0b0: Flag not asserted 0b1: Flag asserted
WATERMARK_ERR	2	Watermark Error Flag Asserted when a watermark error is detected. Read ERROR_STATUS_3 to clear.	0b0: Flag not asserted 0b1: Flag asserted
VIDEO_BLOCK_LENGTH_ERR	1	Combined Video Rx Block Length Error Detection. If the received video packet length is shorter than expected, this interrupt is asserted. Read VIDEO_STATUS_0 and VIDEO_STATUS_1 at 0x92, 0x93 to clear.	0b0: No error detected 0b1: Video RX block length error detected

ERROR STATUS 4 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CRC_ERR	FEEDFORWARD_CRC_ERR	FEEDFORWARD_COMBINED_FRAME_CRC_ERR	LINE_CRC_ERR	VIDEO_PACKET_CRC_ERR	-	-	-
Reset	0b0	0b0	0x0	0b0	0b0	-	-	-
Access Type	Read Only	Read Only	Read Clears All	Read Only	Read Only	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CRC_ERR	7	Video Frame CRC Error Detected Asserted when a video frame CRC error is detected. This feature is enabled when the video region CRC block is programmed and enabled. Cleared when CRC_MISC_STATUS_0 at 0x6E is	0b0: No frame CRC error detected 0b1: Frame CRC errors occurred

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		read. Also cleared by rising edge of video lock.	
FEEDFORWARD_CRC_ERR	6	Feed-Forward Frame CRC error detected. Cleared when CRC_MISC_STATUS_0 (0x6E) is read.	0b0: No error 0b1: Error
FEEDFORWARD_COMBINED_FRAME_CRC_ERR	5	CRC check error detected on feed-forward CRC of combined X and Y frames. Cleared when CRC_MISC_STATUS_0 at 0x6E is read.	0b0: No CRC error detected 0b1: CRC error detected
LINE_CRC_ERR	4	Video Line CRC Error Flag. Read to clear. Asserted when a video line CRC error is detected. Cleared when CRC_MISC_STATUS_1 at 0x6F is read or at rising edge of video lock.	0b0: Flag not asserted 0b1: Flag asserted
VIDEO_PACKET_CRC_ERR	3	Video Pixel CRC Error Flag. Read VID_PXL_CRC_ERR to clear. Asserted when video CRC error count > 0. Read CRC_MISC_STATUS_1 (0x6F) to clear. Also cleared by rising edge of video lock.	0b0: Flag not asserted 0b1: Flag asserted

ERROR STATUS 5 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	DP_INPUT_FIFO_CRC_ERR	WM_BYPASS_ERR	LUT_FRC_ERR	DPTX_FIFO_OVERFLOW_ERR	REGIONAL_COLOR_ERR	LOSS_OF_LOCK_ERR	SGMII_ERR	CONTROL_CHANNEL_CRC_ERR
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
DP_INPUT_FIFO_CRC_ERR	7	Video Align block detected CRC error on its FIFO. Cleared when this ERROR_STATUS_5 is read.	0b0: No CRC error detected 0b1: CRC error detected
WM_BYPASS_ERR	6	Error detected on Watermark redundant datapath. Cleared when CRC_MISC_STATUS_0 at 0x6E is read.	0b0: Error not detected 0b1: Error detected
LUT_FRC_ERR	5	Error detected in LUT and FRC ASIL redundancy check. Cleared when CRC_MISC_STATUS_0 at 0x6E is read.	0b0: Error not detected 0b1: Error detected

BITFIELD	BITS	DESCRIPTION	DECODE
DPTX_FIFO_OVERFLOW_ERR	4	DPTX controller detected overflow in its FIFO. Cleared when this ERROR_STATUS_5 is read.	0b0: FIFO overflow detected 0b1: No FIFO overflow detected
REGIONAL_COLOR_ERR	3	Regional color error detected. Cleared when REGIONAL_COLOR_DETECTION_STATUS_0 at 0x6D is read.	0b0: No error detected 0b1: Error detected
LOSS_OF_LOCK_ERR	2	Loss of GMSL link lock detected. Cleared when this ERROR_STATUS_5 is read.	0b0: Loss of lock detected on GMSL link(s) 0b1: No loss of lock detected on GMSL link(s)
SGMII_ERR	1	SGMII controller detected error. Cleared when this ERROR_STATUS_5 is read.	0b0: No error detected 0b1: Error detected
CONTROL_CHANNEL_CRC_ERR	0	Control Channel CRC error detected. Cleared when RESET_CC_CRC_ERR_CNT is written with 1.	0b0: No CRC check error detected 0b1: CRC check error detected

ERROR STATUS 6 (0xA)

BIT	7	6	5	4	3	2	1	0
Field	OTP_CRC_E RR	—	VIDEO_CFG_E RR	DP_LINK_TRAINING_ ERR	DP_SINK_CAPABILITY_ ERR	AUX_E RR	HPD_IRQ_E RR	HPD_DISCONNECT_ ERR
Reset	0x0	—	0x0	0b0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	—	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
OTP_CRC_ERR	7	OTP CRC check error detected by PMX control state machine. Cleared when ERROR_STATUS_6 is read.	0b0: No error detected 0b1: Error detected
VIDEO_CFG_ERR	5	PSM Control State detected invalid video configuration. Cleared when ERROR_STATUS_6 is read.	0b0: No invalid video configuration detected 0b1: Invalid video configuration detected
DP_LINK_TRAINING_ERR	4	Error occurred during DP link training. Refer to DP_STATUS_0 and DP_STATUS_1 registers for details. Cleared when ERROR_STATUS_6 is read.	0b0: Flag not asserted 0b1: Flag asserted
DP_SINK_CAPABILITY_ERR	3	Incompatible DP sink capability detected. Cleared when ERROR_STATUS_6 is read.	0b0: No error detected 0b1: Error detected
AUX_ERR	2	Error detected on Auxiliary channel communication with DP sink. Cleared when ERROR_STATUS_6 is read.	0b0: No error detected 0b1: Error detected

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ_ERR	1	Hot-plug interrupt from external DP sink detected. Cleared when ERROR_STATUS_6 is read.	0b0: No hot-plug interrupt detected 0b1: Hot-plug interrupt detected
HPD_DISCONNECT_ERR	0	Hot-plug disconnect error detected. Cleared when ERROR_STATUS_6 is read.	0b0: No error detected 0b1: Error detected

DEV_INFO_0 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Use DEV_ID16 for Device identifier	0xFF: Fixed value

DEV_INFO_1 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	DEV_REV[3:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	7:4	Device Revision	0XX: Revision number

DEV_INFO_2 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	SPEED_CPBL[1:0]		SGMII_CPBL	DSC_CPBL	SIOB_CPBL	DAISYCHAIN_CPBL	GMSL_12G_CPBL	HDCP_CPBL
Reset	0b00		0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Read Only		Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPEED_CPBL	7:6	Video Resolution PCLK Rate Capability	0b00: No PCLK frequency limit 0b01: Reserved 0b10: Reserved 0b11: Reserved
SGMII_CPBL	5	SGMII Capable	0b0: Not capable of SGMII operation 0b1: Capable of SGMII operation
DSC_CPBL	4	DSC Decoder Capable	0b0: Not capable of DSC decode 0b1: Capable of DSC decode
SIOB_CPBL	3	Dual GSML Link Capable	0b0: Not capable of Dual-link operation 0b1: Capable of Dual-link operation
DAISYCHAIN_CPBL	2	Daisy-Chain Capable	0b0: Not capable of daisy chain 0b1: Capable of daisy chain
GMSL_12G_CPBL	1	GMSL3 12G Rate Capable	0b0: Not capable of GMSL3 12G operation 0b1: Capable of GMSL3 12G operation
HDCP_CPBL	0	HDCP Capable	0b0: Not capable of HDCP 0b1: Capable of HDCP

DEV_INFO_4 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	OTP_REV[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OTP_REV	7:0	This register shows the revision of the data burned into the OTP. Every time a register default is changed through OTP, this revision will be incremented as a notification. Default value seen in the document may be overwritten by OTP.

DEV_ID16_LSB (0x24)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID16_BYTE_0[7:0]							
Reset	0xC3							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID16_BYTE_0	7:0	16-Bit Device Identifier See DEV_ID16_BYTE_1for decode information.	0x00: Fixed value

GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

DEV_ID16_MSB (0x25)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID16_BYTE_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID16_BYTE_1	7:0	16-Bit Device Identifier	0xC0: MAX96860AS 0xC1: MAX96862RS 0xC2: MAX96764RS 0xC3: MAX96864AS

LINK_STATUS_0 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	LOCKED_SIOA	LOCKED_SIOB	LOCKED_DCIO	—	—	FEC_STATUS_SIOA	FEC_STATUS_SIOB	FEC_STATUS_DCIO
Reset	0b0	0b0	0b0	—	—	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	—	—	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_SIOA	7	SIOA GMSL Link Locked This is a bidirectional lock and the LOCKED status in the serializer connected to SIOA will reflect the same value.	0b0: GMSL link not locked 0b1: GMSL link locked
LOCKED_SIOB	6	SIOB GMSL Link Locked This is a bidirectional lock and the LOCKED status in the serializer connected to SIOB will reflect the same value.	0b0: GMSL link not locked 0b1: GMSL link locked
LOCKED_DCIO	5	DCIO GMSL Link Locked This is a bidirectional lock and the LOCKED status in the serializer connected to DCIO will reflect the same value.	0b0: GMSL link not locked 0b1: GMSL link locked
FEC_STATUS_SIOA	2	SIOA FEC Status	0b0: FEC not enabled 0b1: FEC enabled and active
FEC_STATUS_SIOB	1	SIOB FEC Status	0b0: FEC not enabled 0b1: FEC enabled and active
FEC_STATUS_DCIO	0	DCIO FEC Status	0b0: FEC not enabled 0b1: FEC enabled and active

PRELIMINARY

LINK STATUS 1 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERROR_COUNT_SIOA[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERROR_COUNT_SIOA	7:0	Decode errors counted on SIOA forward channel. This field clears on read and when LOCKED_SIOA transitions from low to high (resets on rising edge of link lock).	0xXX: Number of Link SIO decoding errors detected

LINK STATUS 2 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERROR_COUNT_SIOB[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERROR_COUNT_SIOB	7:0	Decode errors counted on SIOB forward channel. This field clears on read and when LOCKED_SIOB transitions from low to high (resets on rising edge of link lock).	0xXX: Number of Link SIO decoding errors detected

LINK STATUS 3 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERROR_COUNT_DCIO[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERROR_COUNT_DCIO	7:0	Decode errors counted on DCIO forward channel. This field clears on read and when LOCKED_DCIO transitions from low to high (resets on rising edge of link lock).	0xXX: Number of Link DCIO decoding errors detected

PRELIMINARY

FEC STATUS 0 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	FEC_UNCORRECTABLE_ERRORS_SIOA[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_UNCORRECTABLE_ERRORS_SIOA	7:0	Number of errors the FEC block cannot correct on SIOA	0xXX: Number of Link SIO decoding errors detected

FEC STATUS 1 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	FEC_UNCORRECTABLE_ERRORS_SIOB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FEC_UNCORRECTABLE_ERRORS_SIOB	7:0	Number of errors the FEC block cannot correct on SIOB

FEC STATUS 2 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	FEC_BLOCKS_PROCESSED_SIOA_BYTE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BLOCKS_PROCESSED_SIOA_BYTE_0	7:0	Number of blocks processed by the SIOA FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOA), divided by 32768. (Byte 0)	0xXX: Count of blocks processed [7:0]

PRELIMINARY

FEC STATUS 3 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	FEC_BLOCKS_PROCESSED_SIOA_BYTE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BLOCKS_PROCESSED_SIOA_BYTE_1	7:0	Number of blocks processed by the SIOA FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOA), divided by 32768. (Byte 1)	0xXX: Count of blocks processed [15:8]

FEC STATUS 4 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	FEC_BLOCKS_PROCESSED_SIOA_BYTE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BLOCKS_PROCESSED_SIOA_BYTE_2	7:0	Number of blocks processed by the SIOA FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOA), divided by 32768. (Byte 2)	0xXX: Count of blocks processed [23:16]

FEC STATUS 5 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	FEC_BLOCKS_PROCESSED_SIOA_BYTE_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BLOCKS_PROCESSED_SIOA_BYTE_3	7:0	Number of blocks processed by the SIOA FEC decoder since the last FEC stats	0xXX: Count of blocks processed [31:24]

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		reset (FEC_STATS_RESET_SIOA), divided by 32768. (Byte 3)	

FEC STATUS 6 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	FEC_BLOCKS_PROCESSED_SIOB_BYTE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BLOCKS_PROCESSED_SIOB_BYTE_0	7:0	Number of blocks processed by the SIOB FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOB), divided by 32768. (Byte 0)	0xXX: Count of blocks processed [7:0]

FEC STATUS 7 (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	FEC_BLOCKS_PROCESSED_SIOB_BYTE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BLOCKS_PROCESSED_SIOB_BYTE_1	7:0	Number of blocks processed by the SIOB FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOB), divided by 32768. (Byte 1)	0xXX: Count of blocks processed [15:8]

FEC STATUS 8 (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	FEC_BLOCKS_PROCESSED_SIOB_BYTE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BLOCKS_PROCESSED_SIOB_BYTE_2	7:0	Number of blocks processed by the SIOB FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOB), divided by 32768. (Byte 2)	0xXX: Count of blocks processed [23:16]

FEC STATUS 9 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	FEC_BLOCKS_PROCESSED_SIOB_BYTE_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BLOCKS_PROCESSED_SIOB_BYTE_3	7:0	Number of blocks processed by the SIOB FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOB), divided by 32768. (Byte 3)	0xXX: Count of blocks processed [31:24]

FEC STATUS 10 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	FEC_CORRECTED_ERRORS_SIOA_BYTE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_CORRECTED_ERRORS_SIOA_BYTE_0	7:0	Number of bit errors corrected in the SIOA FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOA). Note that this does not map directly to the number of bit errors on the serial link. (Byte 0)	0xXX: Count of bit errors corrected [7:0]

FEC STATUS 11 (0x42)

BIT	7	6	5	4	3	2	1	0

PRELIMINARY

Field	FEC_CORRECTED_ERRORS_SIOA_BYTE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_CORRECTED_ERRORS_SIOA_BYTE_1	7:0	Number of bit errors corrected in the SIOA FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOA). Note that this does not map directly to the number of bit errors on the serial link. (Byte 1)	0xXX: Count of bit errors corrected [15:8]

FEC STATUS 12 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	FEC_CORRECTED_ERRORS_SIOA_BYTE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_CORRECTED_ERRORS_SIOA_BYTE_2	7:0	Number of bit errors corrected in the SIOA FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOA). Note that this does not map directly to the number of bit errors on the serial link. (Byte 2)	0xXX: Count of bit errors corrected [23:16]

FEC STATUS 13 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	FEC_CORRECTED_ERRORS_SIOB_BYTE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_CORRECTED_ERRORS_SIOB_BYTE_0	7:0	Number of bit errors corrected in the SIOB FEC decoder since the last FEC	0xXX: Count of bit errors corrected [7:0]

BITFIELD	BITS	DESCRIPTION	DECODE
		stats reset (FEC_STATS_RESET_SIOB). Note that this does not map directly to the number of bit errors on the serial link. (Byte 0)	

FEC STATUS 14 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	FEC_CORRECTED_ERRORS_SIOB_BYTE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_CORRECTED_ERRORS_SIOB_BYTE_1	7:0	Number of bit errors corrected in the SIOB FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOB). Note that this does not map directly to the number of bit errors on the serial link. (Byte 1)	0XXX: Count of bit errors corrected [15:8]

FEC STATUS 15 (0x46)

BIT	7	6	5	4	3	2	1	0
Field	FEC_CORRECTED_ERRORS_SIOB_BYTE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_CORRECTED_ERRORS_SIOB_BYTE_2	7:0	Number of bit errors corrected in the SIOB FEC decoder since the last FEC stats reset (FEC_STATS_RESET_SIOB). Note that this does not map directly to the number of bit errors on the serial link. (Byte 2)	0XXX: Count of bit errors corrected [23:16]

CC STATUS 0 (0x48)

BIT	7	6	5	4	3	2	1	0

PRELIMINARY

PRELIMINARY

Field	UART_TX_OVERFLOW	UART_RX_OVERFLOW	I2C_ACK RECEIVED	I2C_TIMED_OUT	-	-	-	-
Reset	0b0	0b0	0b0	0b0	-	-	-	-
Access Type	Read Clears All	Read Clears All	Read Only	Read Only	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
UART_TX_OVERFLOW	7	UART transmit buffer overflow	0b0: Buffer not overflowed 0b1: Buffer overflowed
UART_RX_OVERFLOW	6	UART receive buffer overflow	0b0: Buffer not overflowed 0b1: Buffer overflowed
I2C_ACK RECEIVED	5	I ² C acknowledge bit for any I ² C byte has been received from the remote side for the previous I ² C packet.	0b0: I ² C acknowledge bit not received 0b1: I ² C acknowledge bit received
I2C_TIMED_OUT	4	Internal I ² C-to-I ² C subordinate or main has timed out while receiving packet from remote device.	0b0: I ² C not timed out 0b1: I ² C timeout has occurred

PT_STATUS_0 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	PT1_UART_TX_OVERFLOW	PT1_UART_RX_OVERFLOW	-	-	-	-	-	-
Reset	0b0	0b0	-	-	-	-	-	-
Access Type	Read Clears All	Read Clears All	-	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_UART_TX_OVERFLOW	7	Pass-Through UART Channel 1 Transmit FIFO Overflow Flag	0b0: No overflow occurred 0b1: Overflow occurred
PT1_UART_RX_OVERFLOW	6	Pass-Through UART Channel 1 Receive FIFO Overflow Flag	0b0: No overflow occurred 0b1: Overflow occurred

PT_STATUS_1 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	PT2_UART_TX_OVERFLOW	PT2_UART_RX_OVERFLOW	-	-	-	-	-	-
Reset	0b0	0b0	-	-	-	-	-	-
Access Type	Read Clears All	Read Clears All	-	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
PT2_UART_TX_OVERFLOW	7	Pass-Through UART Channel 2 Transmit FIFO Overflow Flag	0b0: No overflow occurred 0b1: Overflow occurred
PT2_UART_RX_OVERFLOW	6	Pass-Through UART Channel 2 Receive FIFO Overflow Flag	0b0: No overflow occurred 0b1: Overflow occurred

SPI STATUS 0 (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	SPI_TX_OVERFLOW	SPI_RX_OVERFLOW	–	SPI_BUFFER_LEVEL[4:0]				
Reset	0b0	0b0	–	0b00000				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_TX_OVERFLOW	7	SPI transmit buffer overflow	0b0: Buffer not overflowed 0b1: Buffer overflowed
SPI_RX_OVERFLOW	6	SPI receive buffer overflow	0b0: Buffer not overflowed 0b1: Buffer overflowed
SPI_BUFFER_LEVEL	4:0	Number of SPI data bytes available for reading from Rx buffer	0bXXXXX: Number of bytes available

SGMII STATUS 0 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	SGMII_TX_OVERFLOW	SGMII_RX_OVERFLOW	SGMII_FRAME_UNDERFLOW	SGMII_LINK_STATUS	SGMII_DLL_LOCK	AUTONEGOTIATION_STATUS	MDIO_READ_VALID	MDIO_BUSY
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_TX_OVERFLOW	7	Status flag indicating buffer overflow was detected on GMSL2 Tx buffer.	0b0: Buffer not overflowed 0b1: Buffer overflowed
SGMII_RX_OVERFLOW	6	Status flag indicating buffer overflow was detected on GMSL2 Rx buffer.	0b0: Buffer not overflowed 0b1: Buffer overflowed

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BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_FRAME_UNDERFLOW	5	Status flag indicating buffer underflow during SGMII frame.	0b0: Buffer not overflowed 0b1: Buffer overflowed
SGMII_LINK_STATUS	4	Indicates whether or not audio pipeline frequency is locked.	0b0: SGMII link down 0b1: SGMII link up
SGMII_DLL_LOCK	3	SGMII clock DLL locked.	0b0: Not locked 0b1: Locked
AUTONEGOTIATION_STATUS	2	SGMII Auto-Negotiation Status	0b0: Auto-negotiation has not occurred 0b1: Auto-negotiation has occurred
MDIO_READ_VALID	1	If MDIO used, status of MDIO read.	0b0: MDIO read data not valid 0b1: MDIO read valid and data is ready to be read from MDIO_DATA_BYTE_0[7:0] and MDIO_DATA_BYTE_1[7:0].
MDIO_BUSY	0	Status bit indicating MDIO transaction is in progress.	0b0: MDIO transaction not in progress 0b1: MDIO transaction in progress

SGMII STATUS 1 (0x50)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	SGMII_INT	SGMII_DEC_ERR_FLAG	SGMII_STOP_ERR	SGMII_PRBS_ERROR
Reset	—	—	—	—	0b0	0b0	0b0	0b0
Access Type	—	—	—	—	Read Only	Read Only	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_INT	3	Interrupt status of SGMII IP. Drives ERRB pin when SGMII_INT_OEN = 1.	0b0: No SGMII interrupt 0b1: SGMII interrupt
SGMII_DEC_ERR_FLAG	2	SGMII Decoding Error Status. Clears when SGMII_DEC_ERROR_COUNT is read.	0b0: No SGMII decoding error detected 0b1: SGMII decoding error detected
SGMII_STOP_ERR	1	SGMII Stop Error Status. Clears when read.	0b0: No SGMII stop error detected 0b1: SGMII stop error detected
SGMII_PRBS_ERROR	0	Status flag indicating error detected on PRBS transmission. Clears when SGMII_PRBS_ERROR_COUNT is read.	0b0: No error detected 0b1: Error detected

SGMII STATUS 2 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	SGMII_PRBS_ERROR_COUNT[7:0]							
Reset	0x0							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_PRBS_ERROR_COUNT	7:0	Number of SGMII PRBS errors detected	0bXXXXX: Number of PRBS errors detected

SGMII STATUS 3 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	SGMII_DEC_ERROR_COUNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_DEC_ERROR_COUNT	7:0	SGMII decoding error counter. Cleared when read.	0bXXXXX: Number of decoding errors detected

AUDIO STATUS 0 (0x54)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	AUDIO_LOCK	—	—	AUDIO_BLOCK_LENGTH_ERROR
Reset	—	—	—	—	0b0	—	—	0b0
Access Type	—	—	—	—	Read Only	—	—	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_LOCK	3	Indicates whether or not audio pipeline frequency is locked to audio clock.	0b0: Audio pipeline frequency is not locked 0b1: Audio pipeline frequency is locked
AUDIO_BLOCK_LENGTH_ERROR	0	Detected packet length error in received audio packet.	0b0: No error detected 0b1: Error detected

AUDIO STATUS 1 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_RX_CLOCK_FREQUENCY[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_RX_CLOCK_FREQUENCY	7:0	Audio clock frequency detected in audio receive block from connected serializer, measured to nearest MHz.	0x0: 0MHz audio clock detected (no clock detected) 0x1: 1MHz audio clock detected 0x2: 2MHz audio clock detected 0x3: 3MHz audio clock detected ... 0xFD: 253MHz audio clock detected 0xFE: 254MHz audio clock detected 0xFF: 255MHz audio clock detected

CFG PIN STATUS 0 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	-		CFG_PIN_0_VALUE[2:0]	-		CFG_PIN_1_VALUE[2:0]		
Reset	-		0b0	-		-	0b0	
Access Type	-		Read Clears All	-		-	Read Clears All	

BITFIELD	BITS	DESCRIPTION	DECODE
CFG_PIN_0_VALUE	6:4	Status of the CFG0 pin on device power-up	0b000: CFG state 0 0b001: CFG state 1 0b010: CFG state 2 0b011: CFG state 3 0b100: CFG state 4 0b101: CFG state 5 0b110: CFG state 6 0b111: CFG state 7
CFG_PIN_1_VALUE	2:0	Status of the CFG1 pin on device power-up	0b000: CFG state 0 0b001: CFG state 1 0b010: CFG state 2 0b011: CFG state 3 0b100: CFG state 4 0b101: CFG state 5 0b110: CFG state 6 0b111: CFG state 7

GPIO STATUS 0 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_VALUE_7	GPIO_VALUE_6	GPIO_VALUE_5	GPIO_VALUE_4	GPIO_VALUE_3	GPIO_VALUE_2	GPIO_VALUE_1	GPIO_VALUE_0
Reset	0b0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_VALUE_7	7	<p>Value of GPIO 7. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p> <p>If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if <code>GPIO_OUTPUT_CONFIG_x[1:0]</code> = 0b01 or 0b10.</p>	<p>0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1</p>
GPIO_VALUE_6	6	<p>Value of GPIO 6. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p> <p>If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if <code>GPIO_OUTPUT_CONFIG_x[1:0]</code> = 0b01 or 0b10.</p>	<p>0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1</p>
GPIO_VALUE_5	5	<p>Value of GPIO 5. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p> <p>If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if <code>GPIO_OUTPUT_CONFIG_x[1:0]</code> = 0b01 or 0b10.</p>	<p>0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1</p>
GPIO_VALUE_4	4	<p>Value of GPIO 4. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p> <p>If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if <code>GPIO_OUTPUT_CONFIG_x[1:0]</code> = 0b01 or 0b10.</p>	<p>0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1</p>
GPIO_VALUE_3	3	<p>Value of GPIO 3. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p> <p>If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if <code>GPIO_OUTPUT_CONFIG_x[1:0]</code> = 0b01 or 0b10.</p>	<p>0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1</p>
GPIO_VALUE_2	2	<p>Value of GPIO 2. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p> <p>If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if <code>GPIO_OUTPUT_CONFIG_x[1:0]</code> = 0b01 or 0b10.</p>	<p>0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1</p>
GPIO_VALUE_1	1	<p>Value of GPIO 1. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p> <p>If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if <code>GPIO_OUTPUT_CONFIG_x[1:0]</code> = 0b01 or 0b10.</p>	<p>0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1</p>
GPIO_VALUE_0	0	<p>Value of GPIO 0. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p>	<p>0b0: This GPIO pin is low 0b1: This GPIO pin is high</p>

BITFIELD	BITS	DESCRIPTION	DECODE
		If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if $\text{GPIO_OUTPUT_CONFIG}_x[1:0] = 0b01$ or $0b10$.	

GPIO_STATUS_1 (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_VALUE_15	GPIO_VALUE_14	GPIO_VALUE_13	GPIO_VALUE_12	GPIO_VALUE_11	GPIO_VALUE_10	GPIO_VALUE_9	GPIO_VALUE_8
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_VALUE_15	7	Value of GPIO 15. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the $\text{GPIO_TX_ID}_x[4:0]$ that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if $\text{GPIO_OUTPUT_CONFIG}_x[1:0] = 0b01$ or $0b10$.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_14	6	Value of GPIO 14. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the $\text{GPIO_TX_ID}_x[4:0]$ that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if $\text{GPIO_OUTPUT_CONFIG}_x[1:0] = 0b01$ or $0b10$.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_13	5	Value of GPIO 13. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the $\text{GPIO_TX_ID}_x[4:0]$ that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if $\text{GPIO_OUTPUT_CONFIG}_x[1:0] = 0b01$ or $0b10$.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_12	4	Value of GPIO 12. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the $\text{GPIO_TX_ID}_x[4:0]$ that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if $\text{GPIO_OUTPUT_CONFIG}_x[1:0] = 0b01$ or $0b10$.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_11	3	Value of GPIO 11. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

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BITFIELD	BITS	DESCRIPTION	DECODE
		GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	
GPIO_VALUE_10	2	Value of GPIO 10. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_9	1	Value of GPIO 9. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_8	0	Value of GPIO 8. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

GPIO_STATUS_2 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_VALUE_23	GPIO_VALUE_22	GPIO_VALUE_21	GPIO_VALUE_20	GPIO_VALUE_19	GPIO_VALUE_18	GPIO_VALUE_17	GPIO_VALUE_16
Reset	0b0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_VALUE_23	7	Value of GPIO 23. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_22	6	Value of GPIO 22. If GPIO is configured as a GPIO input, this is the state of the local pin and is the	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

BITFIELD	BITS	DESCRIPTION	DECODE
		value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	
GPIO_VALUE_21	5	Value of GPIO 21. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_20	4	Value of GPIO 20. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_19	3	Value of GPIO 19. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_18	2	Value of GPIO 18. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_17	1	Value of GPIO 17. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_VALUE_16	0	Value of GPIO 16. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the GPIO_TX_ID_x[4:0] that is configured. If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

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GPIO_STATUS_3 (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	GPIO_VALUE_24
Reset	-	-	-	-	-	-	-	0b0
Access Type	-	-	-	-	-	-	-	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_VALUE_24	0	<p>Value of GPIO 24. If GPIO is configured as a GPIO input, this is the state of the local pin and is the value transmitted across the link at the <code>GPIO_TX_ID_x[4:0]</code> that is configured.</p> <p>If GPIO is configured as a GPIO output, this is the value that is received over the link, and will be driven to the pin if <code>GPIO_OUTPUT_CONFIG_x[1:0] = 0b01 or 0b10</code>.</p>	<p>0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1</p>

REGIONAL_CRC_STATUS_0 (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_DONE	BANK_B_DONE	ACTIVE_A_OR_B	VA_DONE_STATUS	-	-	-	-
Reset	0b0	0b0	0b0	0b0	-	-	-	-
Access Type	Read Only	Read Only	Read Only	Read Only	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
BANK_A_DONE	7	Regional CRC Bank A calculation done.	0b0: Not finished 0b1: Finished
BANK_B_DONE	6	Regional CRC Bank B calculation done.	0b0: Not finished 0b1: Finished
ACTIVE_A_OR_B	5	Which Bank is actively calculating regional CRC.	0b0: Bank A 0b1: Bank B
VA_DONE_STATUS	4	<p>Video authentication done status flag.</p> <p>This flag is automatically cleared when the next set of authentication challenge starts.</p>	0b0: Running 0b1: Challenge complete

REGIONAL_CRC_STATUS_1 (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_COUNT_BYTE_0[7:0]							
Reset	0x00							

Access Type	Read Only							
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BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_COUNT_BYTE_0	7:0	Frame count for regional CRC.	0xXX: LSB bits for frame cycle counter value

REGIONAL_CRC_STATUS_2 (0x60)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	FRAME_COUNT_BYTE_1[1:0]	
Reset	-	-	-	-	-	-	0x00	
Access Type	-	-	-	-	-	-	Read Only	

BITFIELD	BITS	DESCRIPTION
FRAME_COUNT_BYTE_1	1:0	Frame count for regional CRC for bits 9:8

REGIONAL_CRC_STATUS_3 (0x61)

BIT	7	6	5	4	3	2	1	0
Field	REGIONAL_CRC_A_BYTE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGIONAL_CRC_A_BYTE_0	7:0	Value of regional CRC Bank A. (Byte 0)

REGIONAL_CRC_STATUS_4 (0x62)

BIT	7	6	5	4	3	2	1	0
Field	REGIONAL_CRC_A_BYTE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
REGIONAL_CRC_A_BYTE_1	7:0	Value of regional CRC Bank A. (Byte 1)

REGIONAL CRC STATUS 5 (0x63)

BIT	7	6	5	4	3	2	1	0
Field	REGIONAL_CRC_A_BYTE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGIONAL_CRC_A_BYTE_2	7:0	Value of regional CRC Bank A. (Byte 2)

REGIONAL CRC STATUS 6 (0x64)

BIT	7	6	5	4	3	2	1	0
Field	REGIONAL_CRC_A_BYTE_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGIONAL_CRC_A_BYTE_3	7:0	Value of regional CRC Bank A. (Byte 3)

REGIONAL CRC STATUS 7 (0x65)

BIT	7	6	5	4	3	2	1	0
Field	REGIONAL_CRC_B_BYTE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGIONAL_CRC_B_BYTE_0	7:0	Value of regional CRC Bank B. (Byte 0)

REGIONAL_CRC_STATUS_8 (0x66)

BIT	7	6	5	4	3	2	1	0
Field	REGIONAL_CRC_B_BYTE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGIONAL_CRC_B_BYTE_1	7:0	Value of regional CRC Bank B. (Byte 1)

REGIONAL_CRC_STATUS_9 (0x67)

BIT	7	6	5	4	3	2	1	0
Field	REGIONAL_CRC_B_BYTE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGIONAL_CRC_B_BYTE_2	7:0	Value of regional CRC Bank B. (Byte 2)

REGIONAL_CRC_STATUS_10 (0x68)

BIT	7	6	5	4	3	2	1	0
Field	REGIONAL_CRC_B_BYTE_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGIONAL_CRC_B_BYTE_3	7:0	Value of regional CRC Bank B. (Byte 3)

REGIONAL_COLOR_DETECTION_STATUS_0 (0x6D)

BIT	7	6	5	4	3	2	1	0
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Field	REGIONAL_COLOR_ERR_0	REGIONAL_COLOR_ERR_1	REGIONAL_COLOR_ERR_2	REGIONAL_COLOR_ERR_3	-	-	-	-
Reset	0b0	0b0	0b0	0b0	-	-	-	-
Access Type	Read Only	Read Only	Read Only	Read Only	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
REGIONAL_COLOR_ERR_0	7	Telltale region 0 color error detected. Cleared by reading this REGIONAL_COLOR_DETECTION_STATUS_0.	0b0: No error detected 0b1: Error detected
REGIONAL_COLOR_ERR_1	6	Telltale region 1 color error detected. Cleared by reading this REGIONAL_COLOR_DETECTION_STATUS_0.	0b0: No error detected 0b1: Error detected
REGIONAL_COLOR_ERR_2	5	Telltale region 2 color error detected. Cleared by reading this REGIONAL_COLOR_DETECTION_STATUS_0.	0b0: No error detected 0b1: Error detected
REGIONAL_COLOR_ERR_3	4	Telltale region 3 color error detected. Cleared by reading this REGIONAL_COLOR_DETECTION_STATUS_0.	0b0: No error detected 0b1: Error detected

CRC_MISC_STATUS_0 (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	WM_BYPASS_ERR_OR_X	WM_BYPASS_ERR_OR_Y	LUT_FRC_ERROR_X	LUT_FRC_ERROR_Y	FRAME_CRC_ERR_OR_X	FRAME_CRC_ERR_OR_Y	-	-
Reset	0b0	0b0	0x0	0x0	0x0	0x0	-	-
Access Type	Read Only	Read Only	Read Clears All	Read Clears All	Read Clears All	Read Clears All	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
WM_BYPASS_ERROR_X	7	Pipe X watermark bypass redundancy error detected. Cleared by reading this CRC_MISC_STATUS_0.	0b0: No error detected 0b1: Error detected
WM_BYPASS_ERROR_Y	6	Pipe Y watermark bypass redundancy error detected. Cleared by reading this CRC_MISC_STATUS_0.	0b0: No error detected 0b1: Error detected
LUT_FRC_ERROR_X	5	Pipe X ASIL error detected through LUT and FRC. Cleared when this CRC_MISC_STATUS_0 is read.	0b0: No error detected 0b1: Error detected

BITFIELD	BITS	DESCRIPTION	DECODE
LUT_FRC_ERROR_Y	4	Pipe Y ASIL error detected through LUT and FRC. Cleared when this CRC_MISC_STATUS_0 is read.	0b0: No error detected 0b1: Error detected
FRAME_CRC_ERROR_X	3	Pipe X video frame CRC check error detected. Cleared when this CRC_MISC_STATUS_0 is read.	0b0: No error detected 0b1: Error detected
FRAME_CRC_ERROR_Y	2	Pipe Y video frame CRC check error detected. Cleared when this CRC_MISC_STATUS_0 is read.	0b0: No error detected 0b1: Error detected

CRC_MISC_STATUS_1 (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	LINE_CRC_E RROR_X	LINE_CRC_E RROR_Y	VIDEO_PACKET_CR C_ERROR_X	VIDEO_PACKET_CR C_ERROR_Y	—	—	INFOFRAME_CRC_E RROR_SIOB	INFOFRAME_CRC_E RROR_SIOA
Reset	0x0	0x0	0x0	0x0	—	—	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	—	—	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_ERROR_X	7	Pipe X video line CRC error detected. Cleared when this CRC_MISC_STATUS_1 is read. Also cleared at rising edge of video lock.	0x0: No error detected 0x1: Error detected
LINE_CRC_ERROR_Y	6	Pipe Y video line CRC error detected. Cleared when this CRC_MISC_STATUS_1 is read. Also cleared at rising edge of video lock.	0x0: No error detected 0x1: Error detected
VIDEO_PACKET_CRC_ERROR_X	5	Pipe X video packet CRC error detected. Cleared when this CRC_MISC_STATUS_1 is read. Also cleared at rising edge of video lock.	0x0: No error detected 0x1: Error detected
VIDEO_PACKET_CRC_ERROR_Y	4	Pipe Y video packet CRC error detected. Cleared when this CRC_MISC_STATUS_1 is read. Also cleared at rising edge of video lock.	0x0: No error detected 0x1: Error detected
INFOFRAME_CRC_ERROR_SIOB	1	Link SIOB Infoframe CRC error. Cleared when this CRC_MISC_STATUS_1 is read.	0x0: No error detected 0x1: Error detected

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
INFOFRAME_CRC_ERROR_SIOA	0	Link SIOA Infoframe CRC error. Cleared when this CRC_MISC_STATUS_1 is read.	0x0: No error detected 0x1: Error detected

ARQ_STATUS_0 (0x71)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERROR_INFOFRAME_CC	MAX_RT_ER_R_CC	MAX_RT_ERR_PT_1	MAX_RT_ERR_PT_2	MAX_RT_ER_R_SPI	MAX_RT_ERR_GPIO	-	MAX_RT_ERR_HDCP
Reset	0x0	0b0	0b0	0b0	0b0	0b0	-	0b0
Access Type	Write, Read	Read Only	Read Only	Read Only	Read Only	Read Only	-	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERROR_INFOFRAME_CC	7	Maximum retry attempts reached on infoframe CC transmission	0x0: Maximum retry attempts not reached 0x1: Maximum retry attempts reached
MAX_RT_ERR_CC	6	Control channel (CC) packets retransmission error. CRC has detected errors and ARQ block has retransmitted more times than the threshold (X).	0x0: Retransmission threshold not exceeded 0x1: Retransmission threshold exceeded
MAX_RT_ERR_PT_1	5	Pass-through Channel 1 (I ² C or UART) packets retransmission error. CRC has detected errors and ARQ block has retransmitted more times than the threshold (X).	0x0: Retransmission threshold not exceeded 0x1: Retransmission threshold exceeded
MAX_RT_ERR_PT_2	4	Pass-through Channel 2 (I ² C or UART) packets retransmission error. CRC has detected errors and ARQ block has retransmitted more times than the threshold (X).	0x0: Retransmission threshold not exceeded 0x1: Retransmission threshold exceeded
MAX_RT_ERR_SPI	3	SPI packets retransmission error. CRC has detected errors and ARQ block has retransmitted more times than the threshold (X).	0x0: Retransmission threshold not exceeded 0x1: Retransmission threshold exceeded
MAX_RT_ERR_GPIO	2	GPIO packets retransmission error. CRC has detected errors and ARQ block has retransmitted more times than the threshold (X).	0x0: Retransmission threshold not exceeded 0x1: Retransmission threshold exceeded
MAX_RT_ERR_HDCP	0	HDCP packets retransmission error. CRC has detected errors and ARQ block has	0x0: Retransmission threshold not exceeded 0x1: Retransmission threshold exceeded

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		retransmitted more times than the threshold (X).	

LF_STATUS_0 (0x73)

BIT	7	6	5	4	3	2	1	0
Field	LINEFAULT_0_STATUS[2:0]					LINEFAULT_1_STATUS[2:0]	–	–
Reset	0b010					0b010	–	–
Access Type	Read Only					Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINEFAULT_0_STATUS	7:5	Line fault status of GMSL link connected to LMN0 pin.	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short
LINEFAULT_1_STATUS	4:2	Line fault status of GMSL link connected to LMN1 pin.	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

DP_STATUS_0 (0x75)

BIT	7	6	5	4	3	2	1	0
Field	DP_OVERFLOW	DP_UNDERFLOW	DP_INPUT_FIFO_OVERFLOW	DP_VBI_ERROR	–	–	–	–
Reset	0b0	0b0	0b0	0b0	–	–	–	–
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DP_OVERFLOW	7	DP Tx controller buffer overflow	0b0: Buffer not overflowed 0b1: Buffer overflowed
DP_UNDERFLOW	6	DP Tx controller buffer underflow	0b0: Buffer not underflowed 0b1: Buffer underflowed
DP_INPUT_FIFO_OVERFLOW	5	DP input FIFO buffer overflow	0b0: Buffer not overflowed 0b1: Buffer overflowed
DP_VBI_ERROR	4	DP vertical blanking interval timing error detected.	0b0: No error detected 0b1: Error detected

PRELIMINARY

DP_STATUS_1 (0x76)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	LINK_RETRAINED	HPD_EVENT_DETECTED	HPD_IRQ_DETECTED	HPD_CONNECT_STATE
Reset	-	-	-	-	0x0	0x0	0x0	0x0
Access Type	-	-	-	-	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RETRAINED	3	DP Link retraining has started	0b0: DP link retraining has not started 0b1: DP link retraining has started
HPD_EVENT_DETECTED	2	HPD event detected	0b0: No event detected 0b1: Event detected
HPD_IRQ_DETECTED	1	DP HPD interrupt event detected	0b0: No interrupt detected 0b1: Interrupt detected
HPD_CONNECT_STATE	0	DP HPD connection state	0b0: Not connected 0b1: Connected

DP_STATUS_2 (0x77)

BIT	7	6	5	4	3	2	1	0
Field	DPTX_VIDEO_O UTPUT_ACTIVE	LINK_TRAINING_PASSED	LINK_TRAINING_FAILED	LINK_TRAINING_IN_PROGRESS	LINK_TRAINING_NOT_STARTED	WAITING_FOR_VIDEO_LOCK	WAITING_FOR_PSM_STATE	WAITING_FOR_HPD
Reset	0x0	0x0	0x0	0x0	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DPTX_VIDEO_OUTPUT_ACTIVE	7	DPTX controller transmitting video to DP sink	0b0: Not transmitting video 0b1: Transmitting video
LINK_TRAINING_PASSED	6	DP link training passed	0b0: Link training did not pass 0b1: Link training passed
LINK_TRAINING_FAILED	5	DP link training has failed	0b0: Link training did not fail 0b1: Link training failed
LINK_TRAINING_IN_PROGRESS	4	DP link training is in progress	0b0: Link training not in progress 0b1: Link training in progress
LINK_TRAINING_NOT_STARTED	3	State of DP link training	0b0: Link training started 0b1: Link training not started
WAITING_FOR_VIDEO_LOCK	2	Waiting for video configuration and video lock before starting DP link training	0b0: Not waiting 0b1: Waiting

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
WAITING_FOR_PSM_STATE	1	Waiting for training PSM state before proceeding with video/DP link training configuration	0b0: Not waiting 0b1: Waiting
WAITING_FOR_HPD	0	DP TX Controller waiting for HPD connection from DP sink	0b0: Not waiting for HPD 0b1: Waiting for HPD

DP_STATUS_3 (0x78)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	EDID_TRANSFER_TO_SER_DONE	SINK_EDID_READ_DONE
Reset	-	-	-	-	-	-	0x0	0x0
Access Type	-	-	-	-	-	-	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EDID_TRANSFER_TO_SER_DONE	1	Transfer of DisplayID EDID data read from DP sink to GMSL Serializer is done	0b0: Transfer not done 0b1: Transfer done
SINK_EDID_READ_DONE	0	Read of DisplayID EDID data from DP sink completed	0b0: EDID read not completed 0b1: EDID read completed

DP_STATUS_4 (0x79)

BIT	7	6	5	4	3	2	1	0
Field	MAJOR_REV[3:0]				MINOR_REV[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MAJOR_REV	7:4	DPCD major revision number Decode shows Major Revision, together with Minor Revision	0x10h: DPCD r1.0 0x11h: DPCD r1.1 0x12h: DPCD r1.2 0x13h: DPCD r1.3 (for eDP v1.4 DPRX only) 0x14h: DPCD r1.4 All others: Reserved
MINOR_REV	3:0	DPCD minor revision number Decode shows Major Revision, together with Minor Revision	0x10h: DPCD r1.0 0x11h: DPCD r1.1 0x12h: DPCD r1.2 0x13h: DPCD r1.3 (for eDP v1.4 DPRX only) 0x14h: DPCD r1.4 All others: Reserved

DP_STATUS 5 (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	EXTENDED_CAPS_FIELD	-	-	LOCAL_EDID_PRESENT	TPS4_SUPPORTED	TPS3_SUPPORTED	MAX_DOWNSPREAD	ENHANCED_FRAME_CAP
Reset	0x0	-	-	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	-	-	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EXTENDED_CAPS_FIELD	7	DPCD EXTENDED_RECEIVER_CAPABILITY_FIELD_PRESENT	0b0: Not present 0b1: Present
LOCAL_EDID_PRESENT	4	DPCD LOCAL_EDID_PRESENT	0b0: This receiver port does not have a local DisplayID or legacy EDID 0b1: This receiver port has a local DisplayID or legacy EDID
TPS4_SUPPORTED	3	DPCD bit which Indicates Link Training Pattern Sequence 4 (TPS4) support	0b0: TPS4 is not supported 0b1: TPS4 is supported
TPS3_SUPPORTED	2	DPCD bit which indicates Link Training Pattern Sequence 3 (TPS3) support	0b0: TPS3 is not supported 0b1: TPS3 is supported
MAX_DOWNSPREAD	1	DPCD MAX_DOWNSPREAD	0b0: No down spread supported 0b1: Up to 0.5% down spread supported
ENHANCED_FRAME_CAP	0	DPCD Enhanced_Frame_CAP	0b0: Enhanced Framing symbol sequence for BS and SR is not supported 0b1: Enhanced Framing symbol sequence for BS and SR is supported

DP_STATUS 6 (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	MAX_LINK_RATE[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_LINK_RATE	7:0	DPCD MAX_LINK_RATE Four values are supported.	.

PRELIMINARY

DP_STATUS 7 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MAX_LANE_COUNT[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_LANE_COUNT	4:0	DPCD MAX_LANE_COUNT	0x01h: One lane (Lane 0 only) 0x02h: Two lanes (Lane 0 and 1 only) 0x04h: Three lanes (Lane 0, 1, 2 and 3) All others: Reserved

DP_STATUS 8 (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	–	TRAINING_AUX_RD_INTERVAL[6:0]						
Reset	–	0x0						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TRAINING_AUX_RD_INTERVAL	6:0	DPCD TRAINING_AUX_RD_INTERVAL Link Status/Adjust Request read interval during Main-Link Training. 02h = 03h = 04h = All other values are Reserved.	0x00h: 100µs for the Main-Link LANEx_CR_DONE sequence; 400µs for the Main-Link LANEx_CHANNEL_EQ_DONE sequence. 0x01h: 100µs for the Main-Link LANEx_CR_DONE sequence; 4ms for the Main-Link LANEx_CHANNEL_EQ_DONE sequence. 0x02h: 100µs for the Main-Link LANEx_CR_DONE sequence; 8ms for the Main-Link LANEx_CHANNEL_EQ_DONE sequence. 0x03h: 100µs for the Main-Link LANEx_CR_DONE sequence; 12ms for the Main-Link LANEx_CHANNEL_EQ_DONE sequence. 0x04h: 100µs for the Main-Link LANEx_CR_DONE sequence; 16ms for the Main-Link LANEx_CHANNEL_EQ_DONE sequence. All others: Reserved

DP_STATUS 9 (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	I2C_SPEED_CAP[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_SPEED_CAP	7:0	DPCD I ² C Speed Control Capabilities Bit Map. Bits to indicated I ² C speed control capabilities.	.

DP_STATUS_12 (0x80)

BIT	7	6	5	4	3	2	1	0
Field	-	LANE1_SYMBOL_LOCKED	LANE1_CHANNEL_EQ_DONE	LANE1_CR_DONE	-	LANE0_SYMBOL_LOCKED	LANE0_CHANNEL_EQ_DONE	LANE0_CR_DONE
Reset	-	0x0	0x0	0x0	-	0x0	0x0	0x0
Access Type	-	Write, Read	Write, Read	Write, Read	-	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LANE1_SYMBOL_LOCKED	6	DPCD LANE1_SYMBOL_LOCKED	0x0: Not locked 0x1: Locked
LANE1_CHANNEL_EQ_DONE	5	DPCD LANE1_CHANNEL_EQ_DONE	0x0: Not done 0x1: Done
LANE1_CR_DONE	4	DPCP LANE1_CR_DONE. DP lane 1 clock recovery done status	0x0: Not done 0x1: Done
LANE0_SYMBOL_LOCKED	2	DPCD LANE0_SYMBOL_LOCKED	0x0: Not locked 0x1: Locked
LANE0_CHANNEL_EQ_DONE	1	DPCD LANE0_CHANNEL_EQ_DONE	0x0: Not done 0x1: Done
LANE0_CR_DONE	0	DPCP LANE0_CR_DONE. DP lane 0 clock recovery done status.	0x0: Not done 0x1: Done

DP_STATUS_13 (0x81)

BIT	7	6	5	4	3	2	1	0
Field	-	LANE3_SYMBOL_LOCKED	LANE3_CHANNEL_EQ_DONE	LANE3_CR_DONE	-	LANE2_SYMBOL_LOCKED	LANE2_CHANNEL_EQ_DONE	LANE2_CR_DONE
Reset	-	0x0	0x0	0x0	-	0x0	0x0	0x0
Access Type	-	Write, Read	Write, Read	Write, Read	-	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LANE3_SYMBOL_LOCKED	6	DPCD LANE3_SYMBOL_LOCKED	0x0: Not locked 0x1: Locked
LANE3_CHANNEL_EQ_DONE	5	DPCD LANE3_CHANNEL_EQ_DONE	0x0: Not done 0x1: Done
LANE3_CR_DONE	4	DPCP LANE3_CR_DONE. DP lane 3 clock recovery done status	0x0: Not done 0x1: Done
LANE2_SYMBOL_LOCKED	2	DPCD LANE2_SYMBOL_LOCKED	0x0: Not locked 0x1: Locked
LANE2_CHANNEL_EQ_DONE	1	DPCD LANE2_CHANNEL_EQ_DONE	0x0: Not done 0x1: Done
LANE2_CR_DONE	0	DPCP LANE2_CR_DONE. DP lane 2 clock recovery done status	0x0: Not done 0x1: Done

DP_STATUS_14 (0x82)

BIT	7	6	5	4	3	2	1	0
Field	LINK_STATUS_UPDATED	-	-	-	-	-	-	INTERLANE_ALIGN_DONE
Reset	0x0	-	-	-	-	-	-	0x0
Access Type	Write, Read	-	-	-	-	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_STATUS_UPDATED	7	DPCD LINK_STATUS_UPDATED. Link Status and Adjust Request updated since the last read. Set when updated.	0x0: Not updated 0x1: Updated
INTERLANE_ALIGN_DONE	0	DPCD INTERLANE_ALIGN_DONE	0x0: Not done 0x1: Done

DP_STATUS_15 (0x83)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	I2C_OVER_AUX_ERRO R	AUX_NACK_ERRO R	AUX_TIMEOUT_ERRO R	AUX_RETRY_ERRO R	AUX_DEFER_ERRO R
Reset	-	-	-	0x0	0x0	0x0	0x0	0x0
Access Type	-	-	-	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_OVER_AUX_ERROR	4	Error detected in I ² C-over-Aux transaction	0x0: No error detected 0x1: Error detected

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BITFIELD	BITS	DESCRIPTION	DECODE
AUX_NACK_ERROR	3	Error detected in AUX_NACK	0x0: No error detected 0x1: Error detected
AUX_TIMEOUT_ERROR	2	Aux response timeout detected	0x0: No timeout detected 0x1: Timeout detected
AUX_RETRY_ERROR	1	Error detected on AUX_RETRY	0x0: No error detected 0x1: Error detected
AUX_DEFER_ERROR	0	Error detected on AUX_DEFER	0x0: No error detected 0x1: Error detected

DP_STATUS 16 (0x84)

BIT	7	6	5	4	3	2	1	0
Field	OTP_CRC_ERR OR_STATUS	-	VIDEO_CFG_ERR OR_STATUS	-	-	DP_SINK_CHEQ_TPS_CA PABILITY_ERROR	DP_SINK_LANE_COUNT_C APABILITY_ERROR	DP_SINK_LINK_RATE_CA PABILITY_ERROR
Reset	0x0	-	0x0	-	-	0x0	0x0	0x0
Access Type	Write, Read	-	Write, Read	-	-	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OTP_CRC_ERROR_STATUS	7	Error detected on CRC of PMX control OTP	0x0: No error detected 0x1: Error detected
VIDEO_CFG_ERROR_STATUS	5	PSM detected an error in video configuration.	0x0: No error detected 0x1: Error detected
DP_SINK_CHEQ_TPS_CAPABILITY_ERROR	2	Error detected with DP sink CHEQ, TPS capabilities	0x0: No error detected 0x1: Error detected
DP_SINK_LANE_COUNT_CAPABILITY_ERROR	1	Error detected with DP sink lane count capability.	0x0: No error detected 0x1: Error detected
DP_SINK_LINK_RATE_CAPABILITY_ERROR	0	Error detected with DP sink link rate capability	0x0: No error detected 0x1: Error detected

DP_STATUS 17 (0x85)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	DP_LINK_INTERLANE_ALIGN_E RROR	DP_LINK_CHANNEL_EQ_ER ROR	DP_LINK_SYMBOL_LOCK_ER ROR	DP_LINK_CR_ERR OR
Reset	-	-	-	-	0x0	0x0	0x0	0x0

Access Type	-	-	-	-	Write, Read	Write, Read	Write, Read	Write, Read
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BITFIELD	BITS	DESCRIPTION	DECODE
DP_LINK_INTERLANE_ALIGN_ERROR	3	Error detected in interlane alignment during DP link training.	0x0: No error detected 0x1: Error detected
DP_LINK_CHANNEL_EQ_ERROR	2	Error detected in channel equalization during DP link training.	0x0: No error detected 0x1: Error detected
DP_LINK_SYMBOL_LOCK_ERROR	1	Error detected in symbol lock during DP link training.	0x0: No error detected 0x1: Error detected
DP_LINK_CR_ERROR	0	Error detected on clock recovery during DP link training.	0x0: No error detected 0x1: Error detected

WATERMARK STATUS 0 (0x88)

BIT	7	6	5	4	3	2	1	0
Field	WM_ERROR_LIVE	WM_DETECT	-	-	-	-	-	-
Reset	0b0	0b0	-	-	-	-	-	-
Access Type	Read Only	Read Only	-	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
WM_ERROR_LIVE	7	Live active-high watermark error	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.
WM_DETECT	6	Watermark Detected Status If WMD_INT_EN is 1, this value is output to GPIO9	0b0: Watermark detected 0b1: Watermark not detected

DSC STATUS 0 (0x8A)

BIT	7	6	5	4	3	2	1	0
Field	DSC_OVERFLOW	DSC_UNDERFLOW	DSC_PARITY_ERR	DSC_TRANSPORT_CHUNK_SIZE_ER	DSC_MBIST_ERR	-	-	-
Reset	0b0	0b0	0b0	0b0	0b0	-	-	-
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	-	-	-

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_OVERFLOW	7	DSC buffer overflow	0b0: Buffer not overflowed 0b1: Buffer overflowed
DSC_UNDERFLOW	6	DSC buffer underflow	0b0: Buffer not underflowed 0b1: Buffer underflowed
DSC_PARITY_ERROR	5	DSC decode memories detected parity error	0b0: Parity error not detected 0b1: Parity error detected
DSC_TRANSPORT_CHUNK_SIZE_ERROR	4	DSC decode engine detected transport chunk size error	0b0: No error detected 0b1: Error detected
DSC_MBIST_ERROR	3	Start-up MBIST check for DSC memories failed	0b0: MBIST did not fail 0b1: MBIST failed

PRBS_STATUS_0 (0x8C)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	APRBS_VALID	—	—	—	VPRBS_FAIL
Reset	—	—	—	0b0	—	—	—	0b0
Access Type	—	—	—	Read Only	—	—	—	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_VALID	4	Indicates whether or not audio PRBS is running	0b0: Audio PRBS is not running 0b1: Audio PRBS is running
VPRBS_FAIL	0	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register	0b0: Video PRBS check passed 0b1: Video check failed

PRBS_STATUS_1 (0x8D)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERROR_COUNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_ERROR_COUNT	7:0	Video PRBS Error Counter Clears on read.	0XXX: Number of video PRBS errors since last read

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PRBS STATUS 2 (0x8E)

BIT	7	6	5	4	3	2	1	0
Field	APRBS_ERROR_COUNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_ERROR_COUNT	7:0	Audio PRBS Error Counter Clears on read.	0xXX: Number of audio PRBS errors since last read

HDCP STATUS 0 (0x90)

BIT	7	6	5	4	3	2	1	0
Field	DECRYPTION_ON_X	DECRYPTION_ON_Y	HDCP_LINK_INTEG_RITY_X	HDCP_LINK_INTEG_RITY_Y	HDCP2_AUTHENTICATED_X	HDCP2_AUTHENTICATED_Y	-	-
Reset	0x0	0x0	0x0	0x0	0x0	0x0	-	-
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
DECRYPTION_ON_X	7	Decryption active for audio and video for Pipe X	0b0: Decryption is not active 0b1: Decryption is active
DECRYPTION_ON_Y	6	Decryption active for audio and video for Pipe Y	0b0: Decryption is not active 0b1: Decryption is active
HDCP_LINK_INTEGRITY_X	5	HDCP Link integrity status for Pipe X. Indicates decryption is active and no video line CRC errors have occurred.	0b0: Link integrity is bad (video line CRC errors have occurred) or decryption is not active 0b1: Link integrity is good
HDCP_LINK_INTEGRITY_Y	4	HDCP Link integrity status for Pipe Y. Indicates decryption is active and no video line CRC errors have occurred.	0b0: Link integrity is bad (video line CRC errors have occurred) or decryption is not active 0b1: Link integrity is good
HDCP2_AUTHENTICATED_X	3	Authentication status (only valid for HDCP2) for Pipe X	0b0: HDCP2 is not authenticated 0b1: HDCP2 is authenticated
HDCP2_AUTHENTICATED_Y	2	Authentication status (only valid for HDCP2) for Pipe Y	0b0: HDCP2 is not authenticated 0b1: HDCP2 is authenticated

PRELIMINARY

VIDEO STATUS 0 (0x92)

BIT	7	6	5	4	3	2	1	0
Field	-	-	VTRG_OVERFLOW_LOW_X	VTRG_UNDERFLOW_X	VIDEO_ALIGN_OVERFLOW_X	VIDEO_SEQUENCE_ERROR_X	VIDEO_BLOCK_LENGTH_ERROR_X	LOSS_OF_VIDEO_LOCK_X
Reset	-	-	0x0	0x0	0x0	0b0	0b0	0x0
Access Type	-	-	Read Clears All	Read Clears All	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VTRG_OVERFLOW_X	5	Pipe X video timing regenerator (VTRG) buffer overflow	0x0: Buffer not overflowed 0x1: Buffer overflowed
VTRG_UNDERFLOW_X	4	Pipe X video timing regenerator (VTRG) buffer underflow	0x0: Buffer not underflowed 0x1: Buffer underflowed
VIDEO_ALIGN_OVERFLOW_X	3	Sticky flag of video align block overflow detected	0x0: No overflow detected 0x1: Overflow detected
VIDEO_SEQUENCE_ERROR_X	2	Pipe X video packet sequence error detected. Asserted when any received video packets arrive out of order.	0b0: No video packet sequence error 0b1: Video packet sequence error
VIDEO_BLOCK_LENGTH_ERROR_X	1	Pipe X video block length error detected. Asserted when a received video block has too many or too few pixels.	0b0: No video block length error 0b1: Video block length error
LOSS_OF_VIDEO_LOCK_X	0	Indicates that the deserializer has lost video (VIDEO_LOCK has transitioned from high to low) on pipe X. Sticky bit that remains high after a loss of video event.	0x0: Video not lost 0x1: Video lost

VIDEO STATUS 1 (0x93)

BIT	7	6	5	4	3	2	1	0
Field	-	-	VTRG_OVERFLOW_Y	VTRG_UNDERFLOW_Y	VIDEO_ALIGN_OVERFLOW_Y	VIDEO_SEQUENCE_ERROR_Y	VIDEO_BLOCK_LENGTH_ERROR_Y	LOSS_OF_VIDEO_LOCK_Y
Reset	-	-	0x0	0x0		0b0	0b0	0x0
Access Type	-	-	Read Clears All	Read Clears All	Read Only	Read Only	Read Only	Read Only

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
VTRG_OVERFLOW_Y	5	Pipe Y video timing regenerator (VTRG) buffer overflow	0x0: Buffer not overflowed 0x1: Buffer overflowed
VTRG_UNDERFLOW_Y	4	Pipe Y video timing regenerator (VTRG) buffer underflow	0x0: Buffer not underflowed 0x1: Buffer underflowed
VIDEO_ALIGN_OVERFLOW_Y	3	Sticky flag of video align block overflow detected	0x0: No overflow detected 0x1: Overflow detected
VIDEO_SEQUENCE_ERROR_Y	2	Pipe Y video packet sequence error detected. Asserted when any received video packets arrive out of order.	0b0: No video packet sequence error 0b1: Video packet sequence error
VIDEO_BLOCK_LENGTH_ERROR_Y	1	Pipe X video block length error detected. Asserted when a received video block has too many or too few pixels.	0b0: No video block length error 0b1: Video block length error
LOSS_OF_VIDEO_LOCK_Y	0	Indicates that the deserializer has lost video (VIDEO_LOCK has transitioned from high to low) on pipe Y. Sticky bit that remains high after a loss of video event.	0x0: Video not lost 0x1: Video lost

VIDEO_STATUS_2 (0x94)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_PACKET_S_LOCK_Y	VIDEO_PACKET_S_LOCK_X	VIDEO_LOCK_Y	VIDEO_LOCK_X	ODD_EVEN_SPLIT_STATUS	DETECTED_30_BPP	PPS_PARAMS_RECEIVED	AUTO_TIMING_RECEIVED
Reset	0b0	0b0	0b0	0b0	0x0	0x0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PACKETS_LOCK_Y	7	Video lock status. Video locked is defined as video pipe receiving valid video packets from the serializer. In simple video mode, this is VIDEO_LOCK for pipe Y.	0b0: Video not locked 0b1: Video locked
VIDEO_PACKETS_LOCK_X	6	Video lock status. Video locked is defined as video pipe receiving valid video packets from the serializer. In simple video mode, this is VIDEO_LOCK for pipe X.	0b0: Video not locked 0b1: Video locked
VIDEO_LOCK_Y	5	Stable video is being received from the serializer.	0b0: Video not stable 0b1: Video stable

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_LOCK_X	4	Stable video is being received from the serializer.	0b0: Video not stable 0b1: Video stable
ODD_EVEN_SPLIT_STATUS	3	Status of even/odd split combiner usage	0x0: Even/odd split combiner not in use 0x1: Even/odd split combiner in use
DETECTED_30_BPP	2	Detected 30bpp video	0x0: 24bpp 0x1: 30bpp
PPS_PARAMS_RECEIVED	1	DSC PPS parameters received from the serializer	0b0: No PPS parameters received 0b1: PPS parameters received
AUTO_TIMING RECEIVED	0	Auto timing received from the serializer (if supported and enabled). Values are populated in register VIDEO_STATUS_18.	0b0: Video timing not received from serializer 0b1: Video timing received from serializer

VIDEO STATUS 3 (0x95)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PCLK_FREQUENCY_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_PCLK_FREQUENCY_BYTE_0	7:0	Received pixel clock (PCLK) frequency from serializer (to the nearest kHz). (Byte 0)	.

VIDEO STATUS 4 (0x96)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PCLK_FREQUENCY_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_PCLK_FREQUENCY_BYTE_1	7:0	Received pixel clock (PCLK) frequency from serializer (to the nearest kHz). (Byte 1)	.

VIDEO STATUS 5 (0x97)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PCLK_FREQUENCY_BYTE_2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_PCLK_FREQUENCY_BYTE_2	7:0	Received pixel clock (PCLK) frequency from serializer (to the nearest kHz). (Byte 2)	.

VIDEO STATUS 6 (0x98)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_H_ACTIVE_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_H_ACTIVE_BYTE_0	7:0	Received horizontal active (Hactive) resolution from serializer. Measured in pixels. (Byte 0)	.

VIDEO STATUS 7 (0x99)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_H_ACTIVE_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_H_ACTIVE_BYTE_1	7:0	Received horizontal active (Hactive) resolution from serializer. Measured in pixels. (Byte 1)	.

PRELIMINARY

VIDEO STATUS 8 (0x9A)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_H_FP_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_H_FP_BYTE_0	7:0	Received horizontal front porch (Hfp) from serializer. Measured in pixels.	.

VIDEO STATUS 9 (0x9B)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_H_FP_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_H_FP_BYTE_1	7:0	Received horizontal front porch (Hfp) from serializer. Measured in pixels.	.

VIDEO STATUS 10 (0x9C)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_H_SW_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_H_SW_BYTE_0	7:0	Received horizontal sync width (Hsw) from serializer. Measured in pixels.	.

PRELIMINARY

VIDEO STATUS 11 (0x9D)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_H_SW_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_H_SW_BYTE_1	7:0	Received horizontal sync width (Hsw) from serializer. Measured in pixels.	.

VIDEO STATUS 12 (0x9E)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_H_BP_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_H_BP_BYTE_0	7:0	Received horizontal back porch (Hfp) from serializer. Measured in pixels.	.

VIDEO STATUS 13 (0x9F)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_H_BP_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_H_BP_BYTE_1	7:0	Received horizontal back porch (Hfp) from serializer. Measured in pixels.	.

PRELIMINARY

VIDEO STATUS 14 (0xA0)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_V_ACTIVE_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_V_ACTIVE_BYTE_0	7:0	Received vertical active (Vactive) resolution from serializer. Measured in lines. (Byte 0)	.

VIDEO STATUS 15 (0xA1)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_V_ACTIVE_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_V_ACTIVE_BYTE_1	7:0	Received vertical active (Vactive) resolution from serializer. Measured in lines. (Byte 1)	.

VIDEO STATUS 16 (0xA2)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_V_FP[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_V_FP	7:0	Received vertical front porch (Vfp) from serializer. Measured in pixels.	.

PRELIMINARY

VIDEO STATUS 17 (0xA3)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_V_SW[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_V_SW	7:0	Received vertical sync width (Vsw) from serializer. Measured in pixels.	.

VIDEO STATUS 18 (0xA4)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_V_BP[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_V_BP	7:0	Received vertical back porch (Vfp) from serializer. Measured in pixels.	.

VIDEO STATUS 19 (0xA5)

BIT	7	6	5	4	3	2	1	0
Field	DETECTED_PCLK_FREQUENCY_BYTE_0[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DETECTED_PCLK_FREQUENCY_BYTE_0	7:0	Detected pixel clock (PCLK) frequency (in kHz) in deserializer video pipe. (Byte 0)	.

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VIDEO STATUS 20 (0xA6)

BIT	7	6	5	4	3	2	1	0
Field	DETECTED_PCLK_FREQUENCY_BYTE_1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DETECTED_PCLK_FREQUENCY_BYTE_1	7:0	Detected pixel clock (PCLK) frequency (in kHz) in deserializer video pipe. (Byte 1)	.

VIDEO STATUS 21 (0xA7)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	DETECTED_PCLK_FREQUENCY_BYTE_2[3:0]			
Reset	—	—	—	—	0x0			
Access Type	—	—	—	—	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DETECTED_PCLK_FREQUENCY_BYTE_2	3:0	Detected pixel clock (PCLK) frequency (in kHz) in deserializer video pipe. (Byte 2)	.

VIDEO STATUS 22 (0xA8)

BIT	7	6	5	4	3	2	1	0
Field	DETECTED_H_ACTIVE_BYTE_0[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DETECTED_H_ACTIVE_BYTE_0	7:0	Detected horizontal active (Hactive) resolution from serializer. Measured in pixels. (Byte 0)	.

PRELIMINARY

VIDEO STATUS 23 (0xA9)

BIT	7	6	5	4	3	2	1	0
Field	DETECTED_H_ACTIVE_BYTE_1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DETECTED_H_ACTIVE_BYTE_1	7:0	Detected horizontal active (Hactive) resolution from serializer. Measured in pixels. (Byte 1)	.

VIDEO STATUS 24 (0xAA)

BIT	7	6	5	4	3	2	1	0
Field	DETECTED_V_ACTIVE_BYTE_0[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DETECTED_V_ACTIVE_BYTE_0	7:0	Detected vertical active (Vactive) resolution from serializer. Measured in lines. (Byte 0)	.

VIDEO STATUS 25 (0xAB)

BIT	7	6	5	4	3	2	1	0
Field	DETECTED_V_ACTIVE_BYTE_1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DETECTED_V_ACTIVE_BYTE_1	7:0	Detected vertical active (Vactive) resolution from serializer. Measured in lines. (Byte 1)	.

PRELIMINARY

VIDEO STATUS 26 (0xAC)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_HS_POLARITY	RECEIVED_VS_POLARITY	-	-	-	-	DETECTED_HS_POLARITY	DETECTED_VS_POLARITY
Reset	0x0	0x0	-	-	-	-	0x0	0x0
Access Type	Write, Read	Write, Read	-	-	-	-	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVED_HS_POLARITY	7	HSYNC polarity of received video stream from GMSL Serializer	0x0: Negative HSYNC received 0x1: Positive HSYNC received
RECEIVED_VS_POLARITY	6	VSYNC polarity of received video stream from GMSL Serializer	0x0: Negative VSYNC polarity 0x1: Positive VSYNC polarity
DETECTED_HS_POLARITY	1	Detected HS signal polarity	0x0: Negative HS polarity 0x1: Positive HS polarity
DETECTED_VS_POLARITY	0	Detected VS pulse polarity	0x0: Negative VS polarity 0x1: Positive VS polarity

VIDEO STATUS 27 (0xAD)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PPS_PICTURE_WIDTH_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RECEIVED_PPS_PICTURE_WIDTH_BYTE_0	7:0	Received PPS value for picture width from serializer. This is the horizontal active resolution measured in pixels used by the compression engine and should match with the expected horizontal resolution (Hactive). (Byte 0)

VIDEO STATUS 28 (0xAE)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PPS_PICTURE_WIDTH_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

VIDEO STATUS 29 (0xAF)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PPS_PIC_HEIGHT_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RECEIVED_PPS_PIC_HEIGHT_BYTE_0	7:0	Received PPS value for picture height from serializer. This is the horizontal active resolution measured in lines used by the compression engine and should match with the expected vertical resolution (Vactive). (Byte 0)

VIDEO STATUS 30 (0xB0)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PPS_PIC_HEIGHT_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RECEIVED_PPS_PIC_HEIGHT_BYTE_1	7:0	Received PPS value for picture height from serializer. This is the horizontal active resolution measured in lines used by the compression engine and should match with the expected vertical resolution (Vactive). (Byte 1)

VIDEO STATUS 31 (0xB1)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PPS_SLICE_WIDTH_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RECEIVED_PPS_SLICE_WIDTH_BYTE_0	7:0	Received PPS value for slice width from serializer. This is the horizontal slice width measured in pixels used by the compression engine. (Byte 0)

VIDEO STATUS 32 (0xB2)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PPS_SLICE_WIDTH_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RECEIVED_PPS_SLICE_WIDTH_BYTE_1	7:0	Received PPS value for picture width from serializer. This is the horizontal slice width measured in pixels used by the compression engine. (Byte 1)

VIDEO STATUS 33 (0xB3)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PPS_SLICE_HEIGHT_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RECEIVED_PPS_SLICE_HEIGHT_BYTE_0	7:0	Received PPS value for slice height from serializer. This is the horizontal slice height measured in lines used by the compression engine. (Byte 0)

VIDEO STATUS 34 (0xB4)

BIT	7	6	5	4	3	2	1	0
Field	RECEIVED_PPS_SLICE_HEIGHT_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

BITFIELD		BITS	DESCRIPTION					
RECEIVED_PPS_SLICE_HEIGHT_BYTE_1		7:0	Received PPS value for slice height from serializer. This is the horizontal slice height measured in lines used by the compression engine. (Byte 0)					

PSM STATE STATUS 0 (0xB6)

BIT	7	6	5	4	3	2	1	0
Field	-	PSM_ACCESS_E RROR	PSM_STATE_TIMER_E RROR	PSM_DATA_TIMER_E RROR	-	-	PSM_STARTUP_MBIST_FAILED	PSM_STARTUP_MBIST_DONE
Reset	-	0x0	0x0	0x0	-	-	0x0	0x0
Access Type	-	Read Only	Read Only	Read Only	-	-	Read Only	Read Only

BITFIELD		BITS	DESCRIPTION			DECODE		
PSM_ACCESS_ERROR		6	PSM access error			0b0: No error occurred 0b1: Error occurred		
PSM_STATE_TIMER_ERROR		5	PSM state timer error			0b0: No timeout occurred 0b1: Timeout occurred		
PSM_DATA_TIMER_ERROR		4	PSM data access timer error			0b0: No timeout occurred 0b1: Timeout occurred		
PSM_STARTUP_MBIST_FAILED		1	MBIST of PSM memory at startup error status			0b0: No error detected 0b1: Error detected		
PSM_STARTUP_MBIST_DONE		0	MBIST of PSM ROM at startup completion status			0b0: Not done 0b1: Done		

POWER STATUS 0 (0xBA)

BIT	7	6	5	4	3	2	1	0
Field	-	VDDIO_UNDERV OLTAGE_ERRO R	VDD18_UNDERV OLTAGE_ERRO R	VDD_BIAS_UNDE RVOLTAGE_ERRO R	VDD_UNDERV OLTAGE_ERRO R	VDDIO_OVERV OLTAGE_ERRO R	VDD18_OVERV OLTAGE_ERRO R	VDD_OVERV LTAGE_ERRO R
Reset	-	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	-	Read Only	Read Only	Read Clears All	Read Only	Read Clears All	Read Clears All	Read Clears All

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
VDDIO_UNDERVOLTAGE_ERROR	6	Latched when switched V _{DDIO} supply < 1.625V. Cleared on read of this POWER_STATUS_0.	0x0: No error detected 0x1: Error detected
VDD18_UNDERVOLTAGE_ERROR	5	Latched when V _{DD18} < 1.625V. Cleared on read of this POWER_STATUS_0.	0x0: No error detected 0x1: Error detected
VDD_BIAS_UNDERVOLTAGE_ERROR	4	Power Manager switched 1V supply comparator value fell below 0.806v. Cleared on read of this POWER_STATUS_0.	0x0: o V _{DD} undervoltage detected 0x1: V _{DD} undervoltage detected
VDD_UNDERVOLTAGE_ERROR	3	Latched when V _{DD_sw} < 0.806V. Cleared on read of this POWER_STATUS_0.	0x0: No error detected 0x1: Error detected
VDDIO_OVERTVOLTAGE_ERROR	2	V _{DDIO} overvoltage detected. Cleared on read of this POWER_STATUS_0.	0x0: No overvoltage detected 0x1: Overvoltage detected
VDD18_OVERTVOLTAGE_ERROR	1	V _{DD18} overvoltage detected. Cleared on read of this POWER_STATUS_0.	0x0: No overvoltage detected 0x1: Overvoltage detected
VDD_OVERTVOLTAGE_ERROR	0	V _{DD} overvoltage detected. Cleared on read of this POWER_STATUS_0.	0x0: No overvoltage detected 0x1: Overvoltage detected

CFG PIN CFG 0 (0x103)

BIT	7	6	5	4	3	2	1	0
Field	CFG_PIN_0_OVR_EN	CFG_PIN_0_SET[2:0]				CFG_PIN_1_OVR_EN	CFG_PIN_1_SET[2:0]	
Reset	0x0	0x000				0x0	0x000	
Access Type	Write, Read	Write, Read				Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CFG_PIN_0_OVR_EN	7	Override enable of CFG0 value	0b0: Override not enabled 0b1: Override enabled
CFG_PIN_0_SET	6:4	Value to override CFG0 if enabled	
CFG_PIN_1_OVR_EN	3	Override enable of CFG1 value	0b0: Override not enabled 0b1: Override enabled
CFG_PIN_1_SET	2:0	Value to override CFG1 if enabled	

LINK CFG 0 (0x105)

BIT	7	6	5	4	3	2	1	0
Field	LINK_EN_SIOA	LINK_EN_SIOB	LINK_EN_DCIO	-	-	-	-	-

Reset	0b1	0b0	0x1	-	-	-	-	-
Access Type	Write, Read	Write, Read	Write, Read	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_EN_SIOA	7	Enables GMSL Link SIOA	0b0: Link A disabled 0b1: Link A enabled
LINK_EN_SIOB	6	Enables GMSL Link SIOB	0b0: Link B disabled 0b1: Link B enabled
LINK_EN_DCIO	5	Enable DCIO Link	0b0: Disable 0b1: Enable

LINK_CFG_1 (0x106)

BIT	7	6	5	4	3	2	1	0
Field	CX_TP_SIO	-	GMSL3_MODE_SIO	GMSL_FEC_EN_SIO	RSVD[1:0]		RX_RATE_SIO[1:0]	
Reset	0b0	-	0x1	0b0	0b00		0b10	
Access Type	Write, Read	-	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CX_TP_SIO	7	Coax vs. Twisted Pair (single ended vs. differential) selection for the SIO PHYs (SIOA and SIOB). Bit is set according to the latched CFG pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
GMSL3_MODE_SIO	5	Selects which mode SIOA and SIOB PHYs are operating in. You cannot select different modes for SIOA vs. SIOB.	0b0: GMSL2 mode 0b1: GMSL3 mode
GMSL_FEC_EN_SIO	4	Enables FEC on the SIOA and SIOB PHYs. FEC is mandatory for GMSL3 operation and is optional (but recommended) for GMSL2 operation if the corresponding serializer supports FEC. This bit is set high when the device is put into GMSL3 mode via CFG pins. Change activated upon link reset.	0b0: Disable FEC receive operation 0b1: Enable FEC receive operation
RSVD	3:2	Selects the Tx rate for the SIOA and SIOB GMSL links (reverse channel). You cannot select different rates for SIOA vs. SIOB When changed, becomes active after next link reset.	00: 187.5Mbps 01: Reserved 10: Reserved 11: Reserved
RX_RATE_SIO	1:0	Selects the Rx rate for the SIOA and SIOB GMSL links (forward channel). SIOA and SIOB are set to the same Rx rate. When changed, becomes active after next link reset.	00: Reserved 01: 3Gbps 10: 6Gbps 11: 12Gbps

PRELIMINARY

LINK CFG 2 (0x107)

BIT	7	6	5	4	3	2	1	0
Field	CX_TP_DCIO	–	GMSL3_MODE_DCIO	GMSL_FEC_EN_DCIO	TX_RATE_DCIO[1:0]	–	–	–
Reset	0b0	–	0x1	0b1	0b10	–	–	–
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CX_TP_DCIO	7	Coax/twisted-pair cable select for Link DCIO Bit is set according to the latched CFG pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
GMSL3_MODE_DCIO	5	Selects which mode DCIO PHY is operating in.	0x0: GMSL2 mode 0x1: GMSL3 mode
GMSL_FEC_EN_DCIO	4	Enables FEC on the DCIO PHY. FEC is mandatory for GMSL3 operation and is optional (but recommended) for GMSL2 operation if the corresponding serializer supports FEC. This bit is set high when the device is put into GMSL3 mode via CFG pins. Change activated upon link reset.	0b0: FEC is off 0b1: FEC is on
TX_RATE_DCIO	3:2	Transmit Rate on DCIO link When changing this value, restart the link with a write to the RESET_ONESHOT or RESET_LINK register for the new value to take effect. Default value is set by CFG pin at power-up.	00: Reserved 01: 3Gbps 10: 6Gbps 11: 12Gbps

LINK CFG 3 (0x108)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	FEC_STATS_RESET_SIOA	FEC_STATS_RESET_SIOP
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_STATS_RESET_SIOA	1	Reset the FEC statistics on blocks processed, corrected bit errors and uncorrectable bit errors on SIOA link. This bit is self-clearing.	0b0: Counters not cleared 0b1: Counters cleared
FEC_STATS_RESET_SIOP	0	Reset the FEC statistics on blocks processed, corrected bit errors and uncorrectable bit errors	0b0: Counters not cleared 0b1: Counters cleared

BITFIELD	BITS	DESCRIPTION	DECODE
		on SIOB link. This bit is self-clearing.	

ERRG_CFG_0 (0x10A)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_EN_SIOA	ERRG_EN_SIOB	ERRG_EN_DCIO	–	–	–	–	–
Reset	0b0	0b0	0b0	–	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_EN_SIOA	7	Enable error generator on SIOA, using settings defined in register ERRG_CFG_1	0b0: Link SIOA error generator disabled 0b1: Link SIOA error generator enabled
ERRG_EN_SIOB	6	Enable error generator on SIOB, using settings defined in register ERRG_CFG_1	0b0: Link SIOB error generator disabled 0b1: Link SIOB error generator enabled
ERRG_EN_DCIO	5	Enable error generator on DCIO, using settings defined in register ERRG_CFG_1	0b0: Link DCIO error generator disabled 0b1: Link DCIO error generator enabled

ERRG_CFG_1 (0x10B)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_MODE	ERRG_BURST[2:0]				ERRG_BER[1:0]	ERRG_COUNT[1:0]	
Reset	0b0	0b000				0b10	0b00	
Access Type	Write, Read	Write, Read				Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_MODE	7	Selects the error generation distribution between a pseudorandom distribution vs. a periodic distribution	0b0: Pseudorandom 0b1: Periodic
ERRG_BURST	6:4	For each error trigger (at rate selected by ERRG_BER[1:0]), selects the number of burst errors to generate. For a burst error window, the first and last bit will be flipped and the middle bits in the window will have a 50% chance of being flipped. For example, if the bitfield value is 0b100, the burst-error length is 8 bits. Thus, each time an 8-bit error	0b000: 1 bit 0b001: 2 bits 0b010: 3 bits 0b011: 4 bits 0b100: 8 bits 0b101: 12 bits 0b110: 16 bits 0b111: 20 bits

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		burst is generated, there is an error in the first and last bit of the 8-bit window, and the probability of an error in each of the remaining 6 bits is 50%.	
ERRG_BER	3:2	Bit error rate for the error generator	0x0: 1 error triggered in 5120 bits (BER approx. 2.0×10^{-4}) 0x1: 1 error triggered in 81920 bits (BER approx. 1.2×10^{-5}) 0x2: 1 error triggered in 1310720 bits (BER approx. 7.6×10^{-7}) 0x3: 1 error triggered in 20971520 bits (BER approx. 4.8×10^{-8})
ERRG_COUNT	1:0	Number of errors to be generated when error generator is enabled (ERRG_EN_XXX transitions from 0 to 1)	0b00: Continuous error generation. Use this mode to get continuous errors at the BER defined in ERRG_BER[1:0]. 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors

ERROR CFG 0 (0x10D)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PIN_OUTPUT_EN	LINK_SIOA_ERR_OE_N	LINK_SIOB_ERR_OE_N	LINK_DCIO_ERR_OE_N	-	-	-	PSM_STATE_ERR_OE_N
Reset	0b1	0x1	0x1	0x1	-	-	-	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	-	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PIN_OUTPUT_EN	7	Enables overall error status (reported in ERR_OUTPUT) to the ERRB pin.	0b0: ERRB output disabled 0b1: ERRB output enabled
LINK_SIOA_ERR_OEN	6	Output enable to report link SIOA errors to overall error status. NOTE: the reset value of this register changes based on whether FEC on the link is enabled or not. If FEC is enabled, the reset value of this register is 0. User must explicitly write 1 to this register to enable SIOA link error to be reported to ERRB pin. If FEC is not enabled, the reset value of this register is 1.	0b0: Error not output to overall error status 0b1: Error output to overall error status
LINK_SIOB_ERR_OEN	5	Output enable to report link SIOB errors to overall error status. NOTE: the reset value of this register changes based on whether FEC on the link is enabled or not. If FEC is enabled, the reset value of this register is 0. User must explicitly write 1 to this register to enable SIOB link error to be reported to ERRB pin.	0b0: Error not output to overall error status 0b1: Error output to overall error status

BITFIELD	BITS	DESCRIPTION	DECODE
		If FEC is not enabled, the reset value of this register is 1.	
LINK_DCIO_ERR_OEN	4	Output enable to report link DCIO errors to overall error status	0b0: Error not output to overall error status 0b1: Error output to overall error status
PSM_STATE_ERR_OEN	0	Output enable to report PSM state errors to overall error status	0x0: Error not output to overall error status 0x1: Error output to overall error status

ERROR CFG 1 (0x10E)

BIT	7	6	5	4	3	2	1	0
Field	SIOA_FEC_ERR_OEN	SIOB_FEC_ERR_OEN	RETENTION_MEMORY_CRC_ERR_OEN	CONTROL_CHANNEL_MSG_COUNT_ERR_OEN	-	LINEFAULT_0_ERR_OEN	LINEFAULT_1_ERR_OEN	CLOCK_MONITOR_ERR_OEN
Reset	0b1	0b1	0x1	0b0	-	0b1	0b1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	-	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SIOA_FEC_ERR_OEN	7	Output enable to report SIOA FEC errors to overall error status. When FEC is enabled, this bit is automatically set.	0x0: Error not output to overall error status 0x1: Error output to overall error status
SIQB_FEC_ERR_OEN	6	Output enable to report SIOB FEC errors to overall error status. When FEC is enabled, this bit is automatically set.	0x0: Error not output to overall error status 0x1: Error output to overall error status
RETENTION_MEMORY_CRC_ERR_OEN	5	Enables reporting on retention memory CRC check error to ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
CONTROL_CHANNEL_MSG_COUNT_ERR_OEN	4	Enables reporting of I ² C/UART message count errors (I ² C_UART_MSGCNTERR_FLAG) at ERRB pin.	0x0: Error not output to overall error status 0x1: Error output to overall error status
LINEFAULT_0_ERR_OEN	2	Output enable to report Linefault 0 errors to overall error status	0x0: Error not output to overall error status 0x1: Error output to overall error status
LINEFAULT_1_ERR_OEN	1	Output enable to report Linefault 1 errors to overall error status	0x0: Error not output to overall error status 0x1: Error output to overall error status
CLOCK_MONITOR_ERR_OEN	0	Enable reporting of clock monitor error on ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status

ERROR CFG 2 (0x10F)

BIT	7	6	5	4	3	2	1	0
Field	REMOTE_ERR_R_OEN	ARQ_ERR_OEN	INFOFRAME_CRC_ERR_OEN	VIDEO_PRBS_ERR_OEN	AUDIO_PRBS_ERR_OEN	OVERTVOLTAGE_ERR_OEN	UNDERVOLTAGE_ERR_OEN	-
Reset	0b0	0b1	0x1	0b1	0b1	0b1	0b1	-
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	-

BITFIELD	BITS	DESCRIPTION	DECODE
REMOTE_ERR_OEN	7	Output enable to report remote device ERRB to overall error status	0b0: Error not output to overall error status 0b1: Error output to overall error status
ARQ_ERR_OEN	6	Output enable to report ARQ errors to overall error status	0b0: Error not output to overall error status 0b1: Error output to overall error status
INFOFRAME_CRC_ERR_OEN	5	Enable reporting of infoframe CRC error to ERRB pin.	0x0: Error not output to overall error status 0x1: Error output to overall error status
VIDEO_PRBS_ERR_OEN	4	Enables reporting of video PRBS error at ERRB pin	0b0: Error not output to overall error status 0b1: Error output to overall error status
AUDIO_PRBS_ERR_OEN	3	Enables reporting of audio PRBS errors at ERRB pin	0b0: Error not output to overall error status 0b1: Error output to overall error status
OVERTVOLTAGE_ERR_OEN	2	Enables V _{DD} overvoltage status on ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
UNDERVOLTAGE_ERR_OEN	1	Enables reporting of V _{DD} undervoltage interrupt at ERRB pin	0b0: Error not output to overall error status 0b1: Error output to overall error status

ERROR CFG 3 (0x110)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_SEQUENCE_ERR_OEN	LOSS_OF_VIDEO_LOCK_ERR_OEN	HDCP_ER_R_OEN	REG_CRC_ERR_OEN	DSC_ER_R_OEN	WATERMARK_ERR_OEN	VIDEO_BLOCK_LENGTH_ERR_OEN	-
Reset	0b1	0b1	0b0	0b0	0x1	0b1	0b1	-
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	-

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_SEQUENCE_ERR_OEN	7	Enables reporting of combined video sequence error flag at ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
LOSS_OF_VIDEO_LOCK_ERR_OEN	6	Enables reporting loss of video lock on ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
HDCP_ERR_OEN	5	Enables reporting of GMSL HDCP interrupt (HDCP_ERR) at ERRB pin.	0b0: Error not output to overall error status 0b1: Error output to overall error status
REG_CRC_ERR_OEN	4	Enable reporting register CRC at ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
DSC_ERR_OEN	3	Enables reporting of DSC decoder errors (DSC_ERR) at ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
WATERMARK_ERR_OEN	2	Enables reporting of watermark errors (WM_ERR) at ERRB pin.	0b0: Error not output to overall error status 0b1: Error output to overall error status
VIDEO_BLOCK_LENGTH_ERR_OEN	1	Enables reporting of video block length error flag at ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status

ERROR CFG 4 (0x111)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CRC_ER R_OEN	FEEDFORWARD_FRAME_CR C_ERR_OEN	COMBINED_FRAME_CRC _ERR_OEN	LINE_CRC_ER R_OEN	VIDEO_PACKET_CRC_ ERR_OEN	-	-	-
Rese t	0b1	0b0	0x0	0b1	0b1	-	-	-
Acce ss Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CRC_ERR_OEN	7	Enables reporting of video frame CRC errors (FRAME_CRC_ERR) at ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
FEEDFORWARD_FRAME_CRC_ERR_OEN	6	Enables reporting of video frame CRC errors (FEEDFORWARD_FRAME_CRC_ERR) at ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
COMBINED_FRAME_CRC_ERR_OEN	5	Enables reporting of feed-forward frame CRC error detected on combined even and odd pixel frames to ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
LINE_CRC_ERR_OEN	4	Enables reporting of video line CRC errors (LINE_CRC_ERR) at ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
VIDEO_PACKET_CRC_ERR_OEN	3	Enables reporting of video pixel CRC errors (VIDEO_PACKET_CRC_ERR) at ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status

ERROR CFG 5 (0x112)

BIT	7	6	5	4	3	2	1	0

PRELIMINARY

Field	DP_INPUT_FIFO_CRC_ERR_OEN	WM_BYPASS_ERR_OEN	LUT_FRC_ERR_OEN	DPTX_FIFO_OVERFLOW_ERR_OEN	REGIONAL_COLOR_ERR_OEN	LOSS_OF_LOCK_OEN	SGMII_ERR_OEN	CONTROL_CHANNEL_CRC_ERR_OEN
Reset	0x1	0x1	0x1	0b1	0b0	0b0	0b0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DP_INPUT_FIFO_CRC_ERR_OEN	7	Enables reporting on ASIL CRC error detected on the align FIFOs to ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
WM_BYPASS_ERR_OEN	6	Enables reporting of Watermark ASIL bypass error on ERRB	0x0: Error not output to overall error status 0x1: Error output to overall error status
LUT_FRC_ERR_OEN	5	Enables reporting of LUT and FRC ASIL datapath errors to ERBB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
DPTX_FIFO_OVERFLOW_ERR_OEN	4	Enables reporting of DPTX controller FIFO overflow error on ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
REGIONAL_COLOR_ERR_OEN	3	Enables reporting of regional color error on ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
LOSS_OF_LOCK_OEN	2	Enables reporting loss of lock on ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
SGMII_ERR_OEN	1	Enables reporting of SGMII error on ERRB pin.	0x0: Error not output to overall error status 0x1: Error output to overall error status
CONTROL_CHANNEL_CRC_ERR_OEN	0	Enables reporting of detected CRC check error on control channel packets to ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status

ERROR CFG 6 (0x113)

BIT	7	6	5	4	3	2	1	0
Field	OTP_CRC_ERR_OEN	—	VIDEO_CFG_EERR_OEN	DP_LINK_TRAINING_ERR_OEN	DP_SINK_CAPABILITY_ERR_OEN	AUX_ERR_OEN	HPD_IRQ_ERR_OEN	HPD_DISCONNECT_ERR_OEN
Reset	0x1	—	0x1	0b1	0x1	0x1	0x1	0x1
Access Type	Write, Read	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
OTP_CRC_ERR_OEN	7	Enable reporting of OTP CRC check to ERRB pin	0x0: Error not output to overall error status 0x1: Error output to overall error status
VIDEO_CFG_ERR_OEN	5	Enables reporting of video configuration error detected by control state	0x0: Error not output to overall error status 0x1: Error output to overall error status
DP_LINK_TRAINING_ERR_OEN	4	When this bit is enabled, ERRB will be asserted when DP link training error occurs	0x0: Error not output to overall error status 0x1: Error output to overall error status
DP_SINK_CAPABILITY_ERR_OEN	3	Enable reporting of DP_SINK_CAPABILITY_ERR on ERRB	0x0: Error not output to overall error status 0x1: Error output to overall error status
AUX_ERR_OEN	2	Enable reporting of DP_AUX_ERR on ERRB	0x0: Error not output to overall error status 0x1: Error output to overall error status
HPD_IRQ_ERR_OEN	1	Enable reporting of HPD_IRQ_ERR on ERRB	0x0: Error not output to overall error status 0x1: Error output to overall error status
HPD_DISCONNECT_ERR_OEN	0	Enable reporting of HPD_DISCONNECT_ERR on ERRB	0x0: Error not output to overall error status 0x1: Error output to overall error status

CC_CFG_0 (0x116)

BIT	7	6	5	4	3	2	1	0
Field	CC_LOCAL_OUT_EN	DIS_Rem_CC	I2CSEL	UART_BYPASS_EN	—	—	CC_CRC_EN	CC_MESSAGE_COUNT_EN
Reset	0x1	0b0	0b0	0b0	—	—	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	—	—	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC_LOCAL_OUT_EN	7	Enable local control-channel output to SDA_RX and SCL_TX pins. Note that when this bit is enabled, it prevents any further local communication with the device until this bit is set back high. (which can only be done by the remote device)	0x0: Control channel disabled to local pins 0x1: Control channel enabled to local pins
DIS_Rem_CC	6	Disable remote control-channel connection to serializer across the SIO link.	0b0: Control channel enabled to remote serializer 0b1: Control channel disabled to remote serializer
I2CSEL	5	I ² C/UART selection Bit is set according to the latched CFG pin value at power-up.	0b0: UART 0b1: I ² C
UART_BYPASS_EN	4	Enables UART soft-bypass mode. Bypass mode remains active as long as there is UART activity. When there is no UART activity for the selected duration (configured by	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

BITFIELD	BITS	DESCRIPTION	DECODE
		BYPASS_TO), device exits bypass mode and the bit is automatically cleared.	
CC_CRC_EN	1	Enable I ² C/UART CRC	0x0: I ² C/UART CRC disabled 0x1: I ² C/UART CRC enabled
CC_MESSAGE_COUNT_EN	0	Enable I ² C/UART message counter	0x0: I ² C/UART Message Counter disabled 0x1: I ² C/UART Message Counter enabled

CC_CFG_1 (0x117)

BIT	7	6	5	4	3	2	1	0
Field	CC_LINK_SEL	CC_PRIORITY[1:0]	–	–	–	–	–	–
Reset	0x0	0b01	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CC_LINK_SEL	7	Selects the link that the control channel is connected to	0x0: Connect to SIOA 0x1: Connect to SIOB
CC_PRIORITY	6:5	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

CC_CFG_2 (0x118)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CC_I2C_SPEED_SLV[2:0]			CC_I2C_SPEED_MST[2:0]		
Reset	–	–	0b101			0b101		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CC_I2C_SPEED_SLV	5:3	I ² C-to-I ² C Subordinate Speed Select	0x0: 9.92Kbps (I ² C Standard) 0x1: 33.2Kbps (I ² C Standard) 0x2: 99.2Kbps (I ² C Standard or Fast mode) 0x3: 123Kbps (I ² C Fast mode) 0x4: 203Kbps (I ² C Fast mode) 0x5: 397Kbps (I ² C Fast mode or Fast-mode Plus) 0x6: 625Kbps (I ² C Fast-mode Plus) 0x7: 980Kbps (I ² C Fast-mode Plus)
CC_I2C_SPEED_MST	2:0	I ² C-to-I ² C Main Bit-Rate Setting. Configures the I ² C bit rate used by the internal I ² C main (in the device on the remote side from	0b000: 9.92Kbps - Set for I ² C Standard mode speed 0b001: 33.2Kbps - Set for I ² C Standard mode speed 0b010: 99.2Kbps - Set for I ² C Standard or Fast-mode speed 0b011: 123Kbps - Set for I ² C Fast-mode speed 0b100: 203Kbps - Set for I ² C Fast-mode speed

PRELIMINARY

CC_CFG_3 (0x119)

BIT	7	6	5	4	3	2	1	0
Field	CC_I2C_TRANSLATION_0_SOURCE[6:0]							
Reset	0b00000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_I2C_TRANSLATION_0_SOURCE	7:1	I ² C-to-I ² C Main Bit-Rate Setting. Configures the I ² C bit rate used by the internal I ² C main (in the device or the remote side from the external I ² C main). Set this according to the I ² C speed mode.	0bXXXXXXXX: Value of I ² C SRC_A

CC_CFG_4 (0x11A)

BIT	7	6	5	4	3	2	1	0
Field	CC_I2C_TRANSLATION_0_DESTINATION[6:0]							
Reset	0b00000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_I2C_TRANSLATION_0_DESTINATION	7:1	I ² C Address Translator Destination 0 See the description of I ² C_TRANSLATION_0_SOURCE.	0bXXXXXXXX: Value of I ² C DST_A

CC_CFG_5 (0x11B)

BIT	7	6	5	4	3	2	1	0
Field	CC_I2C_TRANSLATION_1_SOURCE[6:0]							
Reset	0b00000000							

Access Type	Write, Read		-
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BITFIELD	BITS	DESCRIPTION	DECODE
CC_I2C_TRANSLATION_1_SOURCE	7:1	I ² C Address Translator Source 1 When I ² C device address matches I ² C TRANSLATE_1_SOURCE, internal I ² C main (on remote side) replaces the device address by I ² C TRANSLATION_1_DESTINATION.	0bXXXXXXXX: Value of I ² C SRC_B

CC_CFG_6 (0x11C)

BIT	7	6	5	4	3	2	1	0
Field	CC_I2C_TRANSLATION_1_DESTINATION[6:0]							
Reset	0b0000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_I2C_TRANSLATION_1_DESTINATION	7:1	I ² C Address Translator Destination 1 See the description of I ² C_TRANSLATION_1_SOURCE	0bXXXXXXXX: Value of I ² C DST_B

CC_CFG_7 (0x11D)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	RESET_MSGCNTR	-	-	RESET_MSGCNTR_ERR_CNT	RESET_CC_CRC_ERR_CNT
Reset	-	-	-	0b0	-	-	0b0	0b0
Access Type	-	-	-	Write Clears All, Read				Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_MSGCNTR	4	Reset MSGCNTR_MSB (0x1D22) and MSGCNTR_LSB (0x1D21) to 0x00 (this bit automatically clears).	0b0: Disabled 0b1: Enabled
RESET_MSGCNTR_ERR_CNT	1	Reset MSGCNTR_ERR_CNT (0x1D24) to 0x00 (this bit automatically clears).	0b0: Disabled 0b1: Enabled
RESET_CC_CRC_ERR_CNT	0	Reset CC_CRC_ERR_CNT (0x1D23) to 0x00 (this bit automatically clears).	0b0: Disabled 0b1: Enabled

PRELIMINARY

PT_CFG_0 (0x11E)

BIT	7	6	5	4	3	2	1	0
Field	PT1_E_N	PT2_E_N	PT1_I2CSEL	PT2_I2CSEL	PT1_LINK_SE_L	PT2_LINK_SE_L	PT1_MANUAL_MODE_EN	PT2_MANUAL_MODE_EN
Reset	0b0	0b0	0b0	0b0	0x0	0x0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_EN	7	Enables pass-through Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: Disable I ² C pass-through Channel 1 0b1: Enable I ² C pass-through Channel 1
PT2_EN	6	Enables pass-through Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: Disable I ² C pass-through Channel 2 0b1: Enable I ² C pass-through Channel 2
PT1_I2CSEL	5	Configures I ² C or UART pass-through Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: Pass-through Channel 1 in UART mode 0b1: Pass-through Channel 1 in I ² C mode
PT2_I2CSEL	4	Configures I ² C or UART pass-through Channel 2 (SDA1/RX1, SCL1/TX1)	0b0: Pass-through Channel 2 in UART mode 0b1: Pass-through Channel 2 in I ² C mode
PT1_LINK_SEL	3	Selects the link that the PT1 is connected to	0x0: Connect to SIOA 0x1: Connect to SIOB
PT2_LINK_SEL	2	Selects the link that the PT2 is connected to	0x0: Connect to SIOA 0x1: Connect to SIOB
PT1_MANUAL_MODE_EN	1	Uses the custom UART bit rate (selected by the BITLEN_PT_1_L and BITLEN_PT_1_H registers) in pass-through UART Channel 1	0b0: Use standard bit rate 0b1: Use custom bit rate
PT2_MANUAL_MODE_EN	0	Enable UART manual mode. Use internal registers to override the defaults for UART rate, timeouts, etc.	0b0: UART manual mode disabled 0b1: UART manual mode enabled

PT_CFG_2 (0x120)

BIT	7	6	5	4	3	2	1	0
Field	PT1_UART_BIT_LENGTH_BYTE_0[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_UART_BIT_LENGTH_BYTE_0	7:0	Low byte of custom UART bit length for pass-through UART Channel 1	0xXX: Low byte of custom UART bit length for pass-through UART Channel 1

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		Set this register to the UART bit length divided by 6.666ns (LSb 8 bits). Set PT_MANUAL_MODE to 1 to use this value.	

PT_CFG_3 (0x121)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PT1_UART_BIT_LENGTH_BYTE_1[5:0]					
Reset	–	–	0b000101					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_UART_BIT_LENGTH_BYTE_1	5:0	High byte of custom UART bit length for pass-through UART Channel 1 Set this register to the UART bit length divided by 6.666ns (LSb 8 bits). Set PT1_MANUAL_MODE to 1 to use this value.	0xXX: High byte of custom UART bit length for pass-through UART Channel 1

PT_CFG_4 (0x122)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PT1_I2C_SPEED_SLV[2:0]			PT1_I2C_SPEED_MST[2:0]		
Reset	–	–	0b101			0b101		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_I2C_SPEED_SLV	5:3	Pass-through channel I ² C-to-I ² C subordinate speed select	0x0: 9.92Kbps (I ² C Standard) 0x1: 33.2Kbps (I ² C Standard) 0x2: 99.2Kbps (I ² C Standard or Fast mode) 0x3: 123Kbps (I ² C Fast mode) 0x4: 203Kbps (I ² C Fast mode) 0x5: 397Kbps (I ² C Fast mode or Fast-mode Plus) 0x6: 625Kbps (I ² C Fast-mode Plus) 0x7: 980Kbps (I ² C Fast-mode Plus)
PT1_I2C_SPEED_MST	2:0	Pass-through I ² C-to-I ² C main bit rate setting Configures the I ² C bit rate used by the internal I ² C main (in the device on remote side from the external I ² C main)	0b000: 9.92Kbps - Set for I ² C Standard mode speed 0b001: 33.2Kbps - Set for I ² C Standard mode speed 0b010: 99.2Kbps - Set for I ² C Standard or Fast-mode speed 0b011: 123Kbps - Set for I ² C Fast-mode speed 0b100: 203Kbps - Set for I ² C Fast-mode speed 0b101: 397Kbps - Set for I ² C Fast or Fast-mode Plus speed

PRELIMINARY

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PT_CFG_5 (0x123)

BIT	7	6	5	4	3	2	1	0
Field	PT1_I2C_TRANSLATION_0_SOURCE[6:0]							
Reset	0b00000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PT1_I2C_TRANSLATION_0_SOURCE	7:1	I ² C address translation 0 source address. Program this bitfield with the address to be translated from. Keep at default when not using address translation. LSB RSVD bit should always be set to 0.

PT_CFG_6 (0x124)

BIT	7	6	5	4	3	2	1	0
Field	PT1_I2C_TRANSLATION_0_DESTINATION[6:0]							
Reset	0b00000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PT1_I2C_TRANSLATION_0_DESTINATION	7:1	I ² C address translation 0 destination address. Program this bitfield with the address to be translated to. Keep at default when not using address translation. LSB RSVD bit should always be set to 0.

PT_CFG_7 (0x125)

BIT	7	6	5	4	3	2	1	0
Field	PT1_I2C_TRANSLATION_1_SOURCE[6:0]							
Reset	0b00000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PT1_I2C_TRANSLATION_1_SOURCE	7:1	I ² C address translation 1 source address. Program this bitfield with the address to be translated from. Keep at default when not using address translation. LSB RSVD bit should always be set to 0.

PT_CFG_8 (0x126)

BIT	7	6	5	4	3	2	1	0
Field	PT1_I2C_TRANSLATION_1_DESTINATION[6:0]							
Reset	0b0000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PT1_I2C_TRANSLATION_1_DESTINATION	7:1	I ² C address translation 1 destination address. Program this bitfield with the address to be translated to. Keep at default when not using address translation. LSB RSVD bit should always be set to 0.

PT_CFG_10 (0x128)

BIT	7	6	5	4	3	2	1	0
Field	PT2_UART_BIT_LENGTH_BYTE_0[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PT2_UART_BIT_LENGTH_BYTE_0	7:0	Low byte of custom UART bit length for pass-through UART Channel 2 Set this register to the UART bit length divided by 6.666ns (LSb 8 bits). Set PT2_MANUAL_MODE to 1 to use this value.	0xXX: Low byte of custom UART bit length for pass-through UART Channel 2

PT_CFG_11 (0x129)

BIT	7	6	5	4	3	2	1	0
Field	-	-	PT2_UART_BIT_LENGTH_BYTE_1[5:0]					

Reset	–	–	0b000101
Access Type	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PT2_UART_BIT_LENGTH_BYTE_1	5:0	<p>High byte of custom UART bit length for pass-through UART Channel 2</p> <p>Set this register to the UART bit length divided by 6.666ns (LSb 8 bits). Set PT2_MANUAL_MODE to 2 to use this value.</p>	0xXX: High byte of custom UART bit length for pass-through UART Channel 2

PT_CFG_12 (0x12A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PT2_I2C_SPEED_SLV[2:0]					PT2_I2C_SPEED_MST[2:0]
Reset	–	–	0b101					0b101
Access Type	–	–	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PT2_I2C_SPEED_SLV	5:3	Pass-through channel I ² C-to-I ² C subordinate speed select	0x0: 9.92Kbps (I ² C Standard) 0x1: 33.2Kbps (I ² C Standard) 0x2: 99.2Kbps (I ² C Standard) or Fast mode 0x3: 123Kbps (I ² C Fast mode) 0x4: 203Kbps (I ² C Fast mode) 0x5: 397Kbps (I ² C Fast mode or Fast-mode Plus) 0x6: 625Kbps (I ² C Fast-mode Plus) 0x7: 980Kbps (I ² C Fast-mode Plus)
PT2_I2C_SPEED_MST	2:0	Pass-through I ² C-to-I ² C main bit rate setting Configures the I ² C bit rate used by the internal I ² C main (in the device on remote side from the external I ² C main) Set this according to the I ² C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	0b000: 9.92Kbps - Set for I ² C Standard mode speed 0b001: 33.2Kbps - Set for I ² C Standard mode speed 0b010: 99.2Kbps - Set for I ² C standard or Fast-mode speed 0b011: 123Kbps - Set for I ² C Fast-mode speed 0b100: 203Kbps - Set for I ² C Fast-mode speed 0b101: 397Kbps - Set for I ² C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I ² C Fast-mode Plus speed 0b111: 980Kbps - Set for I ² C Fast-mode Plus speed

PT_CFG_13 (0x12B)

BIT	7	6	5	4	3	2	1	0
Field	PT2_I2C_TRANSLATION_0_SOURCE[6:0]							
Reset	0b0000000							

PRELIMINARY

Access Type	Write, Read	-
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BITFIELD	BITS	DESCRIPTION
PT2_I2C_TRANSLATION_0_SOURCE	7:1	I ² C address translation 0 source address. Program this bitfield with the address to be translated from. Keep at default when not using address translation. LSB RSVD bit should always be set to 0.

PT_CFG_14 (0x12C)

BIT	7	6	5	4	3	2	1	0
Field	PT2_I2C_TRANSLATION_0_DESTINATION[6:0]							
Reset	0b0000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PT2_I2C_TRANSLATION_0_DESTINATION	7:1	I ² C address translation 0 destination address. Program this bitfield with the address to be translated to. Keep at default when not using address translation. LSB RSVD bit should always be set to 0.

PT_CFG_15 (0x12D)

BIT	7	6	5	4	3	2	1	0
Field	PT2_I2C_TRANSLATION_1_DESTINATION[6:0]							
Reset	0b0000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PT2_I2C_TRANSLATION_1_DESTINATION	7:1	I ² C address translation 1 destination address. Program this bitfield with the address to be translated to. Keep at default when not using address translation. LSB RSVD bit should always be set to 0.

PT_CFG_16 (0x12E)

BIT	7	6	5	4	3	2	1	0
Field	PT2_I2C_TRANSLATION_1_SOURCE[6:0]							

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GMSL3/2 eDP Deserializers with Optional Decompression, HDCP, Daisy Chain, and Ethernet

MAX96860/MAX96862/MAX96864

Reset	0b0000000	-
Access Type	Write, Read	-

BITFIELD	BITS	DESCRIPTION
PT2_I2C_TRANSLATION_1_SOURCE	7:1	I ² C address translation 1 source address. Program this bitfield with the address to be translated from. Keep at default when not using address translation. LSB RSVD bit should always be set to 0.

SPI_CFG_0 (0x130)

BIT	7	6	5	4	3	2	1	0
Field	SPI_EN	MST_SEL	SPI_MODE[1:0]	SPI_IGNORE_ID	-	-	SPI_LOCAL_ID[1:0]	
Reset	0b0	0b1	0b00	0b1	-	-	0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	-	-	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_EN	7	Enables SPI channel	0b0: SPI channel disabled 0b1: SPI channel enabled
MST_SEL	6	Selects if SPI is Main or Subordinate	0b0: SPI subordinate 0b1: SPI main
SPI_MODE	5:4	Bit 0 selects mode 0 or 3. Bit 1 enables the suppression of an extra SCK prior to SS deassertion when SPI mode 3 is selected.	0b01: SPI mode 3 with extra SCK present prior to SS deassertion 0b10: Reserved 0b11: SPI mode 3 with extra SCK suppressed prior to SS deassertion
SPI_IGNORE_ID	3	Selects if SPI should use or ignore header ID to determine packet acceptance	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_LOCAL_ID	1:0	Program to local ID if filtering packets based on header ID	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3

SPI_CFG_1 (0x131)

BIT	7	6	5	4	3	2	1	0
Field	SPI_LINK_SEL	SPI_PRIORITY[1:0]	MISO_SAMPLE_EDGE	-	-	MST_SS_1_POL	MST_SS_2_POL	
Reset	0x0	0b00	0b0	-	-	0x0	0x0	
Access Type	Write, Read	Write, Read	Write, Read	-	-	Write, Read	Write, Read	

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LINK_SEL	7	Selects the link that the adapter is connected to	0x0: Connect to SIOA 0x1: Connect to SIOB
SPI_PRIORITY	6:5	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
MISO_SAMPLE_EDGE	4	Sample MISO after half or full SCK period	0b0: MISO sampled after half SCK period 0b1: MISO sampled after full SCK period
MST_SS_1_POL	1	Select the polarity for SS1 when SPI is a main	0x0: SS1 is active low 0x1: SS1 is active high
MST_SS_2_POL	0	Select the polarity for SS2 when SPI is a main	0x0: SS2 is active low 0x1: SS2 is active high

SPI_CFG_2 (0x132)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	MST_SS_1_EN	MST_SS_2_EN	RO_INPUT_EN	BNE_OUTPUT_EN
Reset	—	—	—	—	0b1	0b1	0b0	0b0
Access Type	—	—	—	—	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MST_SS_1_EN	3	Enables GPIO for use as Subordinate Select 1 output	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
MST_SS_2_EN	2	Enables GPIO for use as Subordinate Select 2 output	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
RO_INPUT_EN	1	Enables GPIO for use as RO input for control of SPI data movement	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function
BNE_OUTPUT_EN	0	Enables GPIO for use as BNE output for SPI data available status	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function

SPI_CFG_3 (0x133)

BIT	7	6	5	4	3	2	1	0
Field	SPI_SLAVE_SEL_DELAY[7:0]							
Reset	0x01							
Access Type	Write, Read							

SPI_CFG_4 (0x134)

BIT	7	6	5	4	3	2	1	0
Field	SPI_SCLK_LOW_CLKS[7:0]							
Reset	0x0F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_SCLK_LOW_CLKS	7:0	Number of 300MHz clocks for SCK low time	0XXX: Number of clocks for SCK low time

SPI_CFG_5 (0x135)

BIT	7	6	5	4	3	2	1	0
Field	SPI_SCLK_HIGH_CLKS[7:0]							
Reset	0x0F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_SCLK_HIGH_CLKS	7:0	Number of 300MHz clocks for SCK high time	0XXX: Number of clocks for SCK high time

SGMII_CFG_0 (0x138)

BIT	7	6	5	4	3	2	1	0
Field	SGMII_EN	SGMII_RESET	SGMII_SP_EED	LOOPBACK_LOC_AL_EN	LOOPBACK_REMO_TE_EN	SGMII_TX_POLARITY	SGMII_RX_POLARITY	SGMII_CMD_RST_N
Reset	0b0	0b0	0x1	0b0	0b0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_EN	7	Enable the SGMII block	0x0: SGMII block is disabled 0x1: SGMII block is enabled
SGMII_RESET	6	Reset the SGMII block. Set this bit high for at least X ms and back low to reset the SGMII block. Perform a reset after any SGMII configuration changes.	0x0: No action 0x1: SGMII block in reset
SGMII_SPEED	5	Set the SGMII speed	0x0: Reserved 0x1: 100Mbps speed
LOOPBACK_LOCAL_EN	4	Enable local loopback test. The SGMII PHY will receive packets on its Rx and transmit those exact packets on its Tx. Received packets are not transmitted across the GMSL link.	0x0: Local loopback test disabled 0x1: Local loopback test enabled
LOOPBACK_REMOTE_EN	3	Enable remote loopback test. All ethernet packets received across the GMSL link are retransmitted back to the remote device (serializer).	0b0: Remote loopback test disabled 0b1: Remote loopback test enabled
SGMII_TX_POLARITY	2	Swap positive and negative pins on SGMII TX	0x0: No action 0x1: Swap positive and negative pins
SGMII_RX_POLARITY	1	Swap positive and negative pins on SGMII RX	0x0: No action 0x1: Swap positive and negative pins
SGMII_CMD_RST_N	0	Active-low signal to hold SGMII function in reset	0x0: Hold in reset 0x1: Release from reset

SGMII_CFG_1 (0x139)

BIT	7	6	5	4	3	2	1	0
Field	SGMII_LINK_SEL	SGMII_PRIORITY[1:0]	–	–	–	–	–	–
Reset	0x0	0b01	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_LINK_SEL	7	Selects the link that the adapter is connected to	0x0: Connect to SIOA 0x1: Connect to SIOB
SGMII_PRIORITY	6:5	Starting GMSL2 request priority advances by one (if room) if Tx buffer is over half full.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

SGMII_CFG_2 (0x13A)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_CLOCK_DIVIDER[7:0]							

Reset	0x64							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_CLOCK_DIVIDER	7:0	Number of SGMII clocks for MDC low/high time.	0xXX: Number of SGMII clocks

SGMII_CFG_3 (0x13B)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_PHY_ADDRESS[4:0]						-	-
Reset	0b00000						-	-
Access Type	Write, Read						-	-

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_PHY_ADDRESS	7:3	Index selecting 1 of 32 potential PHYs on the MDIO bus	0bXXXXX: PHY index
MDIO_EN	0	SGMII MDIO enable	0x0: SGMII MDIO is disabled 0x1: SGMII MDIO is enabled

SGMII_CFG_4 (0x13C)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_REGISTER_ADDRESS[4:0]						ADD_PREAMBLE_EN	MDIO_READ_WRITE
Reset	0b00000						0b0	0b0
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_REGISTER_ADDRESS	7:3	Register address for targeted PHY.	0bXXXXX: PHY address
ADD_PREAMBLE_EN	2	Add 1B preamble to start of frame. Needed if other side of link is RMII.	0x0: Do not add 1 byte preamble to start of frame 0x1: Add 1 byte preamble to start of frame
MDIO_READ_WRITE	1	Assert to indicate write operation.	0b0: MDIO read 0b1: MDIO write
MDIO_START	0	Assert to start MDIO transaction. Must clear and set to start another transaction. Ignored if MDIO_BUSY status bit is asserted.	0b0: No action 0b1: Start MDIO transaction

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		Starts read if MDIO_READ_WRITE = 0 or write if MDIO_READ_WRITE = 1.	

SGMII_CFG_5 (0x13D)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_DATA_BYTE_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_DATA_BYTE_0	7:0	If read performed, the data is populated here after MDIO_START is set high. If write is performed, the data to be written should be placed here before MDIO_START is set high.	0xXX: LSB of MDIO_DATA_BYTE

SGMII_CFG_6 (0x13E)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_DATA_BYTE_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_DATA_BYTE_1	7:0	If read performed, the data is populated here after MDIO_START is set high. If write is performed, the data to be written should be placed here before MDIO_START is set high.	0xXX: MSB of MDIO_DATA_BYTE

SGMII_CFG_7 (0x13F)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	SGMII_INT_EN	SGMII_PRBS_RX_CHECKER_EN	SGMII_PRBS_TX_EN
Reset	-	-	-	-	-	0x0	0b0	0b0

PRELIMINARY

Access Type	-	-	-	-	-	Write, Read	Write, Read	Write, Read
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BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_INT_EN	2	Enable SGMII Auto-Negotiation Interrupt	0x0: Disable 0x1: Enable
SGMII_PRBS_RX_CHECKER_EN	1	SGMII PRBS Checker Enable	0x0: SGMII PRBS checker disabled 0x1: SGMII PRBS checker enabled
SGMII_PRBS_TX_EN	0	SGMII PRBS_TX Enable	0x0: SGMII PRBS pattern transmission disabled 0x1: SGMII PRBS pattern transmission enabled

AUDIO_CFG_0 (0x143)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_LINK_SEL	AUDIO_PRIORITY[1:0]	I2S_MODE	AUDIO_RX_ID[1:0]	AUDIO_PRBS_CHECKER_EN	AUDIO_RX_EN		
Reset	0x0	0b01	0b0	0b00	0b0	0b0		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_LINK_SEL	7	Selects the link that the adapter is connected to	0x0: Connect to SIOA 0x1: Connect to SIOB
AUDIO_PRIORITY	6:5	Sets the priority for this channel's packet requests	0x0: Connect to Link A 0x1: Connect to Link B
I2S_MODE	4	Invert WS at I ² S output	0b0: Do not invert WS (I ² S mode) 0b1: Invert WS (TDM mode)
AUDIO_RX_ID	3:2	Selects audio stream for reception	0b00: Receive stream ID 0 0b01: Receive stream ID 1 0b10: Receive stream ID 2 0b11: Receive stream ID 3
AUDIO_PRBS_CHECKER_EN	1	Enables audio PRBS checker	0b0: Audio PRBS checker disabled 0b1: Audio PRBS checker enabled
AUDIO_RX_EN	0	Audio receiver adapter enable	0b0: Audio receiver disabled 0b1: Audio receiver enabled

GPIO_CFG_0 (0x145)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_LINK_SEL	GPIO_PRIORITY[1:0]	-	-	-	-	-	-
Reset	0x0	0b00	-	-	-	-	-	-
Access Type	Write, Read	Write, Read	-	-	-	-	-	-

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_LINK_SEL	7	Selects the link that the adapter is connected to	0x0: Connect to SIOA 0x1: Connect to SIOB
GPIO_PRIORITY	6:5	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

GPIO_CFG_1 (0x146)

GPIO0

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_2 (0x147)

GPIO0

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]	-	-	GPIO_EDGE_RATE[1:0]	-	-	-
Reset	0b1	0b10	-	-	0b10	-	-	-

PRELIMINARY

Access Type	Write, Read	Write, Read	-	-	Write, Read	-
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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
GPIO_EDGE_RATE	2:1	Adjusts the edge rate of IO buffers when in GPIO mode.	0b00: 1ns 0b01: 2ns 0b10: 4ns 0b11: 8ns

GPIO_CFG_3 (0x148)

GPIO0

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

PRELIMINARY

GPIO_CFG_4 (0x149)

GPIO1

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b00001				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0x0: GPIO state not transmitted over the GMSL link 0x1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_5 (0x14A)

GPIO1

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]			–	–	GPIO_EDGE_RATE[1:0]	
Reset	0b1	0b10			–	–	0b10	
Access Type	Write, Read	Write, Read			–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when	0b0: 40kΩ 0b1: 1MΩ

BITFIELD	BITS	DESCRIPTION	DECODE
		GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
GPIO_EDGE_RATE	2:1	Adjusts the edge rate of IO buffers when in GPIO mode.	0b00: 1ns 0b01: 2ns 0b10: 4ns 0b11: 8ns

GPIO_CFG_6 (0x14B)

GPIO1

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b00001				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_7 (0x14C)

GPIO2

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				

PRELIMINARY

Reset	0b1	0x0	0b0	0b00010
Access Type	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0x0: GPIO state not transmitted over the GMSL link 0x1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_8 (0x14D)

GPIO2

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		–	–	GPIO_EDGE_RATE[1:0]	–	
Reset	0b1	0b10		–	–	0b10	–	
Access Type	Write, Read	Write, Read		–	–	Write, Read	–	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
GPIO_EDGE_RATE	2:1	Adjusts the edge rate of IO buffers when in GPIO mode.	0b00: 1ns 0b01: 2ns 0b10: 4ns 0b11: 8ns

GPIO_CFG_9 (0x14E)

GPIO2

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b00010				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_10 (0x155)

GPIO5

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b00101				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_11 (0x156)

GPIO5

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		–	–	–	–	–
Reset	0b1	0b10		–	–	–	–	–
Access Type	Write, Read	Write, Read		–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_12 (0x157)

GPIO5

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b00101				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_13 (0x158)

GPIO6

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b00110				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0x0: GPIO state not transmitted over the GMSL link 0x1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_14 (0x159)

GPIO6

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE		GPIO_INPUT_RESISTANCE_CONFIG[1:0]	-	-	-	-	-
Reset	0b1		0b10	-	-	-	-	-
Access Type	Write, Read		Write, Read	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_15 (0x15A)

GPIO6

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b00110				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_16 (0x161)

GPIO9

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b0	0x0	0b0	0b01001				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_17 (0x162)

GPIO9

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]					–	–
Reset	0b1	0b00					–	–
Access Type	Write, Read	Write, Read					–	–

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_18 (0x163)

GPIO9

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b01001				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_19 (0x164)

GPIO10

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				

PRELIMINARY

Reset	0b1	0x0	0b0	0b01010
Access Type	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_20 (0x165)

GPIO10

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		–	–	–	–	–
Reset	0b1	0b10		–	–	–	–	–
Access Type	Write, Read	Write, Read		–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_21 (0x166)

GPIO10

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b01010				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_22 (0x167)

GPIO11

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b01011				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link

BITFIELD	BITS	DESCRIPTION	DECODE
		transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_23 (0x168)

GPIO11

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE		GPIO_INPUT_RESISTANCE_CONFIG[1:0]	-	-	-	-	-
Reset	0b1		0b10	-	-	-	-	-
Access Type	Write, Read		Write, Read	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_24 (0x169)

GPIO11

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b01011				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output

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BITFIELD	BITS	DESCRIPTION	DECODE
		configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_25 (0x16A)

GPIO12

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b01100				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_26 (0x16B)

GPIO12

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE		GPIO_INPUT_RESISTANCE_CONFIG[1:0]	-	-	-	-	-
Reset	0b1		0b10	-	-	-	-	-
Access Type	Write, Read		Write, Read	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_27 (0x16C)

GPIO12

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b01100				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link

PRELIMINARY

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_28 (0x16D)

GPIO13

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b01101				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_29 (0x16E)

GPIO13

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]			–	–	GPIO_EDGE_RATE[1:0]	
Reset	0b1	0b10			–	–	0b10	
Access Type	Write, Read	Write, Read			–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
GPIO_EDGE_RATE	2:1	Adjusts the edge rate of IO buffers when in GPIO mode.	0b00: 1ns 0b01: 2ns 0b10: 4ns 0b11: 8ns

GPIO_CFG_30 (0x16F)

GPIO13

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b01101				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_31 (0x170)

GPIO14

PRELIMINARY

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BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b01110				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPIO). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_32 (0x171)

GPIO14

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]			–	–	GPIO_EDGE_RATE[1:0]	
Reset	0b1	0b10			–	–	0b10	
Access Type	Write, Read	Write, Read			–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_EDGE_RATE	2:1	Adjusts the edge rate of IO buffers when in GPIO mode.	0b00: 1ns 0b01: 2ns 0b10: 4ns 0b11: 8ns

GPIO_CFG_33 (0x172)

GPIO14

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b01110				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_34 (0x173)

GPIO15

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b01111				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_35 (0x174)

GPIO15

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		–	–	–	–	–
Reset	0b1	0b10		–	–	–	–	–
Access Type	Write, Read	Write, Read		–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	00: No input resistance enabled 01: pull up resistor enabled 10: pull down resistor enabled 11: RXVD

GPIO_CFG_36 (0x175)

GPIO15

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				

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Reset	0b0	0x0	0x1	0b01111
Access Type	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_37 (0x176)

GPIO16

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b10000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_38 (0x177)

GPIO16

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		–	–	GPIO_EDGE_RATE[1:0]	–	–
Reset	0b1	0b10		–	–	0b11	–	–
Access Type	Write, Read	Write, Read		–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
GPIO_EDGE_RATE	2:1	Adjusts the edge rate of IO buffers when in GPIO mode.	0b00: 1ns 0b01: 2ns 0b10: 4ns 0b11: 8ns

GPIO_CFG_39 (0x178)

GPIO16

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b10000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving,	0bXXXXX: GPIO receive ID

GPIO_CFG_40 (0x179)

GPIO17

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b0	0x0	0b0	0b10001				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_41 (0x17A)

GPIO17

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE		GPIO_INPUT_RESISTANCE_CONFIG[1:0]	-	-	-	-	-
Reset	0b1		0b00	-	-	-	-	-
Access Type	Write, Read		Write, Read	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_42 (0x17B)

GPIO17

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b10001				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_43 (0x17C)

GPIO18

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b10010				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_44 (0x17D)

GPIO18

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]					–	–
Reset	0b1	0b10					–	–
Access Type	Write, Read	Write, Read					–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_45 (0x17E)

GPIO18

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b10010				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_46 (0x17F)

GPIO19

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				

PRELIMINARY

Reset	0b1	0x0	0b0	0b10011
Access Type	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_47 (0x180)

GPIO19

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		–	–	–	–	–
Reset	0b1	0b10		–	–	–	–	–
Access Type	Write, Read	Write, Read		–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_48 (0x181)

GPIO19

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b10011				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_49 (0x182)

GPIO20

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b10100				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link

BITFIELD	BITS	DESCRIPTION	DECODE
		transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_50 (0x183)

GPIO20

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE		GPIO_INPUT_RESISTANCE_CONFIG[1:0]	-	-	-	-	-
Reset	0b1		0b10	-	-	-	-	-
Access Type	Write, Read		Write, Read	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_51 (0x184)

GPIO20

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b10100				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_52 (0x185)

GPIO21

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b10101				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

PRELIMINARY

GPIO_CFG_53 (0x186)

GPIO21

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE		GPIO_INPUT_RESISTANCE_CONFIG[1:0]	-	-	-	-	-
Reset	0b1		0b10	-	-	-	-	-
Access Type	Write, Read		Write, Read	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set Input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	

GPIO_CFG_54 (0x187)

GPIO21

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b10101				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_55 (0x188)

GPIO22

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b10110				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPIO). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_56 (0x189)

GPIO22

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]			–	–	–	–
Reset	0b1	0b10			–	–	–	–
Access Type	Write, Read	Write, Read			–	–	–	–

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_57 (0x18A)

GPIO22

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b10110				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_58 (0x18B)

GPIO23

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				

PRELIMINARY

Reset	0b1	0x0	0b0	0b10111
Access Type	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_59 (0x18C)

GPIO23

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE	GPIO_INPUT_RESISTANCE_CONFIG[1:0]		–	–	–	–	–
Reset	0b1	0b10		–	–	–	–	–
Access Type	Write, Read	Write, Read		–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_60 (0x18D)

GPIO23

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b10111				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

GPIO_CFG_61 (0x18E)

GPIO24

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_PIN_EN	GPIO_INPUT_TUNNEL_EN	GPIO_TX_COMPENSATION_EN	GPIO_TX_ID[4:0]				
Reset	0b1	0x0	0b0	0b11000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_PIN_EN	7	Enable GPIO pin as an input (GPI). This enables the pin's input buffer, and the driven state of the pin can be read from GPIO_VALUE_0. Also enables the pull-up or pull-down resistor as configured in GPIO_INPUT_RESISTANCE_VALUE and GPIO_INPUT_RESISTANCE_CONFIG[1:0].	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_INPUT_TUNNEL_EN	6	Enables GPIO state tunneling over the GMSL link, requires GPIO_INPUT_PIN_EN = 1. This will take the driven state of the GPIO pin and	0b0: GPIO state not transmitted over the GMSL link 0b1: GPIO state transmitted over the GMSL link

BITFIELD	BITS	DESCRIPTION	DECODE
		transmit it over the GMSL link using the GPIO TX ID set in GPIO_TX_ID[4:0] bitfield.	
GPIO_TX_COMPENSATION_EN	5	Enable TX compensation mode to minimize GPIO jitter. This mode adds additional latency to GPIO transmission across the GMSL link.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_ID	4:0	Set GPIO transmit ID for the value of this GPIO pin. If GPIO_INPUT_PIN_EN = 1 and GPIO_INPUT_TUNNEL_EN = 1.	0bXXXXX: GPIO transmit ID

GPIO_CFG_62 (0x18F)

GPIO24

BIT	7	6	5	4	3	2	1	0
Field	GPIO_INPUT_RESISTANCE_VALUE		GPIO_INPUT_RESISTANCE_CONFIG[1:0]	-	-	-	-	-
Reset	0b1		0b10	-	-	-	-	-
Access Type	Write, Read		Write, Read	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_INPUT_RESISTANCE_VALUE	7	Select the pull-up or pull-down resistance value when GPIO_INPUT_RESISTANCE_CONFIG[1:0] = 0b01 or 0b10.	0b0: 40kΩ 0b1: 1MΩ
GPIO_INPUT_RESISTANCE_CONFIG	6:5	Set input resistance for the GPIO. Only active if GPIO_INPUT_EN = 1.	0b00: No input resistance enabled - Hi-Z 0b01: Pull-up 0b10: Pull-down 0b11: Reserved

GPIO_CFG_63 (0x190)

GPIO24

BIT	7	6	5	4	3	2	1	0
Field	GPIO_OUTPUT_PIN_EN	GPIO_OUTPUT_TUNNEL_EN	GPIO_OUTPUT_TYPE	GPIO_RX_ID[4:0]				
Reset	0b0	0x0	0x1	0b11000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUTPUT_PIN_EN	7	Enable GPIO pin as an output (GPO). Activates GPIO output driver as	0b0: GPIO pin not enabled as an output 0b1: GPIO pin enabled as an output

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		configured by GPIO_OUTPUT_TYPE and outputs either the value received over the link (if GPIO_OUTPUT_TUNNEL_EN = 1) or the value programmed in GPIO_MANUAL_OUTPUT_VALUE (if GPIO_OUTPUT_TUNNEL_EN = 0).	
GPIO_OUTPUT_TUNNEL_EN	6	Enables receiving tunneled value of the GPIO from across the GMSL link from the GPIO RX ID set in GPIO_RX_ID[4:0] bitfield, which can be read from GPIO_VALUE. Outputs this received value on the local GPIO if GPIO_OUTPUT_PIN_EN = 1.	0b0: GPIO tunnel value not being received across GMSL link 0b1: GPIO tunnel value is received across GMSL link
GPIO_OUTPUT_TYPE	5	Configures GPIO output to push-pull or open drain.	0b0: Open drain 0b1: Push-pull
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: GPIO receive ID

OUTPUT_CFG_0 (0x192)

BIT	7	6	5	4	3	2	1	0
Field	WMD_INT_EN	VA_DONE_INT_EN	–	VIDEO_LOCK_OUTPUT_EN	LOCK_PIN_CONTROL[1:0]	–	RCLKOUT_EN	
Reset	0b0	0b0	–	0b0	0b0	–	0b0	
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WMD_INT_EN	7	Enables watermark detected status to be driven to GPIO pin.	0b0: Disabled 0b1: Enabled
VA_DONE_INT_EN	6	Enables video authentication done status to be reflected to the ERRB pin.	0b0: Disabled 0b1: Enabled
VIDEO_LOCK_OUTPUT_EN	4	Enable VIDEO_LOCK output to the LOCK pin	0b0: LOCK pin driven by GMSL LOCK status 0b1: LOCK pin driven by VIDEO_LOCK and GMSL LOCK status
LOCK_PIN_CONTROL	3:2	Controls which GMSL link lock status controls the LOCK pin status	0b00: LOCK_SIOA and (LOCK_SIOB ~LINK_EN_B) 0b01: LOCK_SIOA and (LOCK_SIOB ~LINK_EN_B) and LOCK_DCIO 0b10: LOCK_SIOA 0b11: LOCK_SIOA and LOCK_DCIO
RCLKOUT_EN	0	Enable 25MHz reference clock output to RCLKOUT pin	0b0: RCLK output is disabled 0b1: RCLK output is enabled

CRC_CFG_0 (0x195)

BIT	7	6	5	4	3	2	1	0

PRELIMINARY

Field	–	–	–	–	–	VIDEO_LINE_CRC_EN	VIDEO_PACKET_CRC_EN	FRAME_CRC_EN
Reset	–	–	–	–	–	0b1	0b0	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_LINE_CRC_EN	2	Enables Video Line CRC checking	0b0: Video line CRC checking disabled 0b1: Video line CRC checking enabled
VIDEO_PACKET_CRC_EN	1	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
FRAME_CRC_EN	0	When set, indicates that video frames received are accompanied by Frame CRC in infoframe and frame CRC needs to be checked.	0b0: No frame CRC from infoframe expected 0b1: Received video frame has accompanying frame CRC infoframe.

CRC_CFG_1 (0x196)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	FCRC_INFOFRAME_CC_EN	–	RGB_FRAME_CRC_EN	DP_SINK_RGB_FRAME_CRC_EN
Reset	–	–	–	–	0x0	–	0x0	0x0
Access Type	–	–	–	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FCRC_INFOFRAME_CC_EN	3	Enables using DP FCRC values received by infoframe_cc	0b0: Disable 0b1: Enable
RGB_FRAME_CRC_EN	1	Enable frame CRC check on RGB video	0x0: Disable 0x1: Enable
DP_SINK_RGB_FRAME_CRC_EN	0	Enable frame CRC check of video displayed by DP sink	0x0: Disable 0x1: Enable

LINEFAULT_CFG_0 (0x199)

BIT	7	6	5	4	3	2	1	0
Field	LINEFAULT_0_EN	LINEFAULT_1_EN	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINEFAULT_0_EN	7	Powers up line-fault monitor 0 (LF0 pin)	0x0: Line-fault monitor 0 disabled 0x1: Line-fault monitor 0 enabled
LINEFAULT_1_EN	6	Powers up line-fault monitor 1 (LF1 pin)	0x0: Line-fault monitor 1 disabled 0x1: Line-fault monitor 1 enabled

ARQ CFG 0 (0x19B)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	MAX_RT_ERROR_RESET
Reset	-	-	-	-	-	-	-	0x0
Access Type	-	-	-	-	-	-	-	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERROR_RESET	0	Write 1 to clear maximum retry error. Self-clearing.	0x0: No action 0x1: Reset Maximum Retry error

VIDEO PIPE CFG 0 (0x1A0)

BIT	7	6	5	4	3	2	1	0
Field	VID_EN_X	STREAM_SEL_X[1:0]	-	SUPPORT_BLACK_VIDEO_ENABLE	BLANK_VIDEO	COLOR_LUT_EN	VPRBS_CHECKER_EN_X	
Reset	0b1	0b00	-	0x0	0b0	0b0	0b0	
Access Type	Write, Read	Write, Read	-	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_X	7	Enable video on Pipe X	0b0: Video receive is disabled 0b1: Video receive is enabled
STREAM_SEL_X	6:5	Select the stream ID that Pipe X is receiving video from. Default depends on the selected I ² C address through CFG pins.	0b00: Stream 0 0b01: Stream 1 0b10: Stream 2 0b11: Stream 3
SUPPORT_BLACK_VIDEO_ENABLE	3	This bit indicates whether the eDP BLACK_VIDEO_ENABLE feature is supported or not. If supported, it allows the DPTX in this device to set the DPCD BLACK_VIDEO_ENABLE register in the DP sink when there is no video present in the DPTX.	0b0: Not supported 0b1: Supported

BITFIELD	BITS	DESCRIPTION	DECODE
BLANK_VIDEO	2	Blank video output from device by setting all active video pixels to black. Affects Pipe X and Pipe Y.	0b0: Do not blank video output 0b1: Blank video output
COLOR_LUT_EN	1	Enable the color LUT on pipe X. Refer to internal registers to configure the LUT.	0b0: Color LUT disabled 0b1: Color LUT enabled
VPRBS_CHECKER_EN_X	0	Enable video PRBS checker on Pipe X. Results reported to registers VIDEO_PRBS_STATUS_0 and VIDEO_PRBS_STATUS_1.	0b0: Video PRBS checker disabled 0b1: Video PRBS checker enabled

VIDEO PIPE CFG 1 (0x1A1)

BIT	7	6	5	4	3	2	1	0
Field	VID_EN_Y	STREAM_SEL_Y[1:0]		LINK_SEL_Y	–	–	–	VPRBS_CHECKER_EN_Y
Reset	0b0	0b01		0x1	–	–	–	0b0
Access Type	Write, Read	Write, Read		Write, Read	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_Y	7	Enable video on Pipe Y. Set to 1 when using even/odd pixel splitter mode.	0b0: Video receive on pipe Y disabled 0b1: Video receive on pipe Y enabled
STREAM_SEL_Y	6:5	Select the stream ID that Pipe Y is receiving video from. Default depends on the selected I ² C address through CFG pins.	0b00: Stream 0 0b01: Stream 1 0b10: Stream 2 0b11: Stream 3
LINK_SEL_Y	4	Selects which link Pipe Y receives video from.	0b0: Pipe Y receiving video from SIOA 0b1: Pipe Y receiving video from SIOB
VPRBS_CHECKER_EN_Y	0	Enable video PRBS checker on Pipe Y. Results reported to registers VIDEO_PRBS_STATUS_0 and VIDEO_PRBS_STATUS_1.	0b0: Video PRBS checker disabled 0b1: Video PRBS checker enabled

VIDEO PIPE CFG 2 (0x1A2)

BIT	7	6	5	4	3	2	1	0
Field	VS_HS_PIN_EN_X	VS_HS_INPUT_MOD_E_X	DE_OUTPUT_EN_X	–	VS_HS_OUTPUT_E_N_Y	DE_OUTPUT_EN_Y	SYNC_LOCATION_SEL[1:0]	
Reset	0x0	0x0	0x0	–	0x0	0x0	0x00	
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HS_PIN_EN_X	7	Enable VS and HS signals from Pipe X to be output on respective GPIO pins. Overrides other GPIO configurations.	0x0: No action 0x1: VS and HS outputs enabled to respective GPIO pins
VS_HS_INPUT_MODE_X	6	Configures VS and HS GPIO pins as input.	0x0: VS, HS pins are output 0x1: VS, HS pins are input
DE_OUTPUT_EN_X	5	Enable DE signal from Pipe X to be output on GPIO x for debug purposes. Overrides other GPIO configurations.	0x0: No action 0x1: DE output enabled to GPIO
VS_HS_OUTPUT_EN_Y	3	Enable VS and HS signals from Pipe Y to be output on their respective GPIO pins. Overrides other GPIO configurations.	0x0: No action 0x1: VS, HS outputs enabled to GPIO pins
DE_OUTPUT_EN_Y	2	Enable DE signal from Pipe Y to be output on its GPIO pin, when RCLKOUT is not being output on the shared GPIO pin. Overrides other GPIO configurations.	0x0: No action 0x1: DE output enabled to GPIO
SYNC_LOCATION_SEL	1:0	Selects the location for video sync signals (HS, VS, DE) to be output to GPIO.pin(s)	0b00: DPTX input 0b01: VTRG input 0b10: VTRG output 0b11: Align blocks input

VIDEO PIPE CFG 3 (0x1A3)

BIT	7	6	5	4	3	2	1	0
Field	VS_HS_ALT_PIN_EN_X	VS_HS_ALT_INPUT_MODE_X	—	—	—	—	—	—
Reset	0x0	0x0	—	—	—	—	—	—
Access Type	Write, Read	Write, Read	—	—	—	—	—	—

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HS_ALT_PIN_EN_X	7	Enable VS and HS signals to/ from Pipe X on respective alternate GPIO pins. Direction is specified by VS_HS_ALT_INPUT_MODE_X register. Overrides other GPIO configurations.	0b0: Alternate GPIO pins not allocated for VS, HS 0b1: Alternate GPIO pins are allocated for VS, HS
VS_HS_ALT_INPUT_MODE_X	6	Configures alternate VS and HS GPIO pins as input	0b0: Alternate VS, HS pins are output 0b1: Alternate VS, HS pins are input

DC VIDEO CFG 0 (0x1A5)

BIT	7	6	5	4	3	2	1	0	
Field	DROP_VIDEO[3:0]					AUTO_DROP_VIDEO_EN	—	—	—

Reset	0x0		0x1		-	-	-
Access Type	Write, Read		Write, Read		-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
DROP_VIDEO	7:4	Selects which video stream is dropped while forwarding in the daisy-chain output. Default is selected by I ² C address. The video stream shown by default on the OLDI output is dropped by default. Default OLDI output video stream is selected by the CFG0 pin.	0bxxx1: Drop stream ID = 0 0bxx1x: Drop stream ID = 1 0bx1xx: Drop stream ID = 2 0b1xxx: Drop stream ID = 3
AUTO_DROP_VIDEO_EN	3	Enable automatic dropping of video stream	0b0: Disable 0b1: Enable

DP_CFG_0 (0x1A8)

BIT	7	6	5	4	3	2	1	0
Field	AUTO_RETRAIN_ON LOSS_OF_LINK_EN	-	DP_SINK_EDID_TIMING_EN	DP_SINK_READ_EDID_EN	DP_SPREADSPECTRUM_TRUM_EN	AUTO_TIMING_EN	AUTO_DP_LINK_CONFIG	-
Reset	0x1	-	0x0	0x0	0x0	0x1	0x0	-
Access Type	Write, Read	-	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	-

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_RETRAIN_ON LOSS_OF_LINK_EN	7	Enable automatic DP link retraining upon loss of link integrity	0b0: Not enabled 0b1: Enabled
DP_SINK_EDID_TIMING_EN	5	Read DP sink EDID and populate video timing information	0b0: No action 0b1: Read DP sink EDID to derive video timing information
DP_SINK_READ_EDID_EN	4	Read DP sink EDID and send to GMSL serializer	0b0: No action 0b1: Read DP sink EDID and send to SER
DP_SPREADSPECTRUM_EN	3	Enable DP spread-spectrum clocking	0b0: DP spread-spectrum clocking disabled 0b1: DP spread-spectrum clocking enabled
AUTO_TIMING_EN	2	Enable auto timing. Receives detected video timing from a DP serializer and automatically configures the output video timing VIDEO_TIMING_CFG_x registers.	0b0: Auto timing disabled 0b1: Auto timing enabled
AUTO_DP_LINK_CONFIG	1	Auto-set the DP rate and lane count based on video timing and sink capability	0b0: No action 0b1: Auto-set DP rate and lane count

PRELIMINARY

DP_CFG_2 (0x1AA)

BIT	7	6	5	4	3	2	1	0
Field	–	DP_LANE_COUNT[2:0]				–	DP_RATE[2:0]	
Reset	–	0x4				–	0b010	
Access Type	–	Write, Read				–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DP_LANE_COUNT	6:4	Configure the number of DP lanes	0b00: One lane (lane 0 only) 0b01: Two lanes (lanes 0 and 1 only) 0x4: Four lanes (lanes 0, 1, 2, and 3) Others: Reserved
DP_RATE	2:0	DP Link rate	0x0: 1.62Gbps 0x1: 2.7Gbps 0x2: 5.4Gbps 0x3: 8.1Gbps 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

WATERMARK_LOCK_CFG_0 (0x1B0)

BIT	7	6	5	4	3	2	1	0
Field	WATERMARK_KEY_BYTE_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WATERMARK_KEY_BYTE_0	7:0	Write 0xBA to WATERMARK_KEY_BYTE_0 and 0xDC to WATERMARK_KEY_BYTE_1 registers to enable writing to watermark registers. Otherwise watermark registers are read-only.

WATERMARK_LOCK_CFG_1 (0x1B1)

BIT	7	6	5	4	3	2	1	0
Field	WATERMARK_KEY_BYTE_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
WATERMARK_KEY_BYTE_1	7:0	Write 0xBA to WATERMARK_KEY_BYTE_0 and 0xDC to WATERMARK_KEY_BYTE_1 registers to enable writing to watermark registers. Otherwise watermark registers are read-only.

WATERMARK CFG 0 (0x1B2)

BIT	7	6	5	4	3	2	1	0
Field	WATERMARK_DE_T_EN	WATERMARK_REMOVE	WATERMARK_REGIONAL_MODE	WATERMARK_BLANK	WATERMARK_REGIONAL_BLANK_MODE	-	-	-
Reset	0b0	0x1	0b0	0b0	0x1	-	-	-
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
WATERMARK_DET_EN	7	Watermark detection is enabled	0b0: Watermark detection is disabled 0b1: Watermark detection is enabled
WATERMARK_REMOVE	6	Indicates if the detected watermark should be removed or not from the video	0x0: Do not remove detected watermark from video 0x1: Remove detected watermark from video
WATERMARK_REGIONAL_MODE	5	Watermark regional mode is enabled	0b0: Watermark regional mode is disabled 0b1: Watermark regional mode is enabled
WATERMARK_BLANK	4	Enable blanking of video when watermark error detected (frozen frame condition occurs).	0b0: Video stream not blanked on watermark error 0b1: Video stream blanked on watermark error
WATERMARK_REGIONAL_BLANK_MODE	3	Selects blanking mode for watermark operation.	0x0: Blank full frame 0x1: Blank watermarked region

WATERMARK CFG 1 (0x1B3)

BIT	7	6	5	4	3	2	1	0
Field	WM_REGION_XMIN_BYTE_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WM_REGION_XMIN_BYTE_0	7:0	First pixel of defined regional watermark removal, measured in pixels from the beginning of the video line. (Byte 0)

WATERMARK CFG 2 (0x1B4)

BIT	7	6	5	4	3	2	1	0
Field	WM_REGION_XMIN_BYTE_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WM_REGION_XMIN_BYTE_1	7:0	First pixel of defined regional watermark removal, measured in pixels from the beginning of the video line. (Byte 1)

WATERMARK CFG 3 (0x1B5)

BIT	7	6	5	4	3	2	1	0
Field	WM_REGION_XMAX_BYTE_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WM_REGION_XMAX_BYTE_0	7:0	Last pixel of defined region for regional watermark removal, measured in pixels from the beginning of the video line. (Byte 0)

WATERMARK CFG 4 (0x1B6)

BIT	7	6	5	4	3	2	1	0
Field	WM_REGION_XMAX_BYTE_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WM_REGION_XMAX_BYTE_1	7:0	Last pixel of defined region for regional watermark removal, measured in pixels from the beginning of the video line. (Byte 1)

PRELIMINARY

WATERMARK CFG 5 (0x1B7)

BIT	7	6	5	4	3	2	1	0
Field	WM_REGION_YMIN_BYTE_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WM_REGION_YMIN_BYTE_0	7:0	First line of defined region for regional watermark removal, measured in lines from the beginning of the frame. (Byte 0)

WATERMARK CFG 6 (0x1B8)

BIT	7	6	5	4	3	2	1	0
Field	WM_REGION_YMIN_BYTE_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WM_REGION_YMIN_BYTE_1	7:0	First line of defined region for regional watermark removal, measured in lines from the beginning of the frame. (Byte 1)

WATERMARK CFG 7 (0x1B9)

BIT	7	6	5	4	3	2	1	0
Field	WM_REGION_YMAX_BYTE_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WM_REGION_YMAX_BYTE_0	7:0	Last line of defined region for regional watermark removal, measured in lines from the beginning of the frame. (Byte 0)

PRELIMINARY

WATERMARK CFG 8 (0x1BA)

BIT	7	6	5	4	3	2	1	0
Field	WM_REGION_YMAX_BYTE_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WM_REGION_YMAX_BYTE_1	7:0	Last line of defined region for regional watermark removal, measured in lines from the beginning of the frame. (Byte 1)

PATTERN GENERATOR CFG 0 (0x1BC)

BIT	7	6	5	4	3	2	1	0
Field	CUSTOM_COLOR_RED[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CUSTOM_COLOR_RED	7:0	Video pattern generator first custom-color pixel red component value

PATTERN GENERATOR CFG 1 (0x1BD)

BIT	7	6	5	4	3	2	1	0
Field	CUSTOM_COLOR_GREEN[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CUSTOM_COLOR_GREEN	7:0	Video pattern generator first custom-color pixel green component value

PATTERN GENERATOR CFG 2 (0x1BE)

BIT	7	6	5	4	3	2	1	0

PRELIMINARY

Field	CUSTOM_COLOR_BLUE[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CUSTOM_COLOR_BLUE	7:0	Video pattern generator first custom-color pixel blue component value

PATTERN GENERATOR CFG 3 (0x1BF)

BIT	7	6	5	4	3	2	1	0
Field	CUSTOM_COLOR_RED_30BIT_LS BS[1:0]	CUSTOM_COLOR_GREEN_30BIT_L SBS[1:0]	CUSTOM_COLOR_BLUE_30BIT_LS BS[1:0]	—	—	—	—	MODE_30BIT_EN
Reset	0x00	0x00	0x00	—	—	—	—	0x0
Access Type	Write, Read	Write, Read	Write, Read	—	—	—	—	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CUSTOM_COLOR_RED_30BIT_LSB	7:6	Specifies the 2 LSBs for the R value for the custom RGB color if 30-bit mode is used (MODE_30BIT_EN = 1).	
CUSTOM_COLOR_GREEN_30BIT_LSB	5:4	Specifies the 2 LSBs for the G value for the custom RGB color if 30-bit mode is used (MODE_30BIT_EN = 1).	
CUSTOM_COLOR_BLUE_30BIT_LSB	3:2	Specifies the 2 LSBs for the B value for the custom RGB color if 30-bit mode is used (MODE_30BIT_EN = 1).	
MODE_30BIT_EN	0	Enables the pattern generator in 30-bit color mode	0x0: 24-bit pixel mode 0x1: 30-bit pixel mode

PATTERN GENERATOR CFG 4 (0x1C0)

BIT	7	6	5	4	3	2	1	0
Field	PATTERN_SIZE_X[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
PATTERN_SIZE_X	7:0	X-dimension size of checkerboard pattern.	.

PATTERN GENERATOR CFG 5 (0x1C1)

BIT	7	6	5	4	3	2	1	0
Field	PATTERN_SIZE_Y[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PATTERN_SIZE_Y	7:0	Y-dimension size of checkerboard pattern.	.

PATTERN GENERATOR CFG 6 (0x1C2)

BIT	7	6	5	4	3	2	1	0
Field	GRADIENT_COLOR_STEP_SIZE[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
GRADIENT_COLOR_STEP_SIZE	7:0	Defines the increment value to the pixel value for color gradient patterns.

PATTERN GENERATOR CFG 7 (0x1C3)

BIT	7	6	5	4	3	2	1	0
Field	PATTERN_SELECT[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
PATTERN_SELECT	7:0	Select the pattern for the video pattern generator. Leave at default to disable the video pattern generator (VPG).	0x0: Pattern generator disabled 0x1: Solid color pattern 0x2: Checker board pattern 0x3: Horizontal gradient pattern 0x4: Vertical gradient pattern 0x5: Color bars pattern 0x6: Color bars gradient pattern 0x7: Two-color frame 0x8: Red gradient 0x9: Green gradient 0xA: Blue gradient 0xB: Reserved 0xC: Reserved

DSC_CFG_0 (0x1C5)

BIT	7	6	5	4	3	2	1	0
Field	DSC_DECODE_EN	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_DECODE_EN	7	Configure DSC decoder to be enabled	0b0: Do not enable DSC decoder operation 0b1: Enable DSC decoder operation

HDCP_CFG_0 (0x1C7)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_EN_X	HDCP_EN_Y	–	–	HDCP_ERR_RESET	HDCP_GPIO_ID_Y[1:0]	HDCP_VER	
Reset	0b1	0b1	–	–	0x0	0x0	0b1	
Access Type	Write, Read	Write, Read	–	–	Write Only Clears All	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_EN_X	7	Enable HDCP decryption on SIOA	0b0: HDCP encryption disabled 0b1: HDCP encryption enabled
HDCP_EN_Y	6	Enable HDCP decryption on SIOA	0b0: HDCP encryption disabled 0b1: HDCP encryption enabled
HDCP_ERR_RESET	3	Write 1 to clear HDCP_ERR.	0x0: No action 0x1: Clears HDCP_ERR
HDCP_GPIO_ID_Y	2:1	Selector for hdcp2_tun_y_gpio_id	0x0: HDCP2 pipe Y GPIO ID = 27 0x1: HDCP2 pipe Y GPIO ID = 26 0x2: HDCP2 pipe Y GPIO ID = 25 0x3: HDCP2 pipe Y GPIO ID = 28
HDCP_VER	0	Selects the HDCP version	0b0: HDCP 1.4 0b1: HDCP 2.3

HDCP_CFG_1 (0x1C8)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_ADDRESS_Y[6:0]							-
Reset	0b1001010							-
Access Type	Write, Read							-

BITFIELD	BITS	DESCRIPTION	DECODE																		
HDCP_ADDRESS_Y	7:1	<p>Device Address for I2C or UART addressing for pipe Y HDCP</p> <p>NOTE: Other DES in system must NOT use the same value selected here. for either DEV_ADDR or DEV_ADDR_Y.</p> <p>Default value is set by the ADD[2:0] pins as follows:</p> <table> <tr> <td>ADD[2:0]</td> <td>Device Address</td> </tr> <tr> <td>000</td> <td>0b1001010</td> </tr> <tr> <td>001</td> <td>0b1001100</td> </tr> <tr> <td>010</td> <td>0b1101000</td> </tr> <tr> <td>011</td> <td>0b1001000</td> </tr> <tr> <td>100</td> <td>0b1101100</td> </tr> <tr> <td>101</td> <td>0b0101000</td> </tr> <tr> <td>110</td> <td>0b0101010</td> </tr> <tr> <td>111</td> <td>0b1101010</td> </tr> </table>	ADD[2:0]	Device Address	000	0b1001010	001	0b1001100	010	0b1101000	011	0b1001000	100	0b1101100	101	0b0101000	110	0b0101010	111	0b1101010	<p>0b0000000: I²C write/read address is 0x00/0x01</p> <p>0b0000001: I²C write/read address is 0x02/0x03</p> <p>...</p> <p>...</p> <p>0b1001000: I²C write/read address is 0x90/0x91</p> <p>0b1001010: I²C write/read address is 0x94/0x95</p> <p>0b1001100: I²C write/read address is 0x98/0x99</p> <p>0b1101000: I²C write/read address is 0xD0/0xD1</p> <p>0b1101010: I²C write/read address is 0xD4/0xD5</p> <p>0b1101100: I²C write/read address is 0xD8/0xD9</p> <p>0b0101000: I²C write/read address is 0x50/0x51</p> <p>0b0101010: I²C write/read address is 0x54/0x55</p> <p>...</p> <p>...</p> <p>0b1111111: I²C write/read address is 0xFE/0xFF</p>
ADD[2:0]	Device Address																				
000	0b1001010																				
001	0b1001100																				
010	0b1101000																				
011	0b1001000																				
100	0b1101100																				
101	0b0101000																				
110	0b0101010																				
111	0b1101010																				

FRC_CFG_0 (0x1D2)

BIT	7	6	5	4	3	2	1	0
Field	FRC_EN	-	-	-	-	-	-	-
Reset	0b0	-	-	-	-	-	-	-
Access Type	Write, Read	-	-	-	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
FRC_EN	7	Frame-rate control enable	0b0: Disabled 0b1: Enabled

VIDEO_TIMING_CFG_0 (0x1D6)

BIT	7	6	5	4	3	2	1	0
Field	PCLK_FREQUENCY_BYTE_0[7:0]							

PRELIMINARY

Reset	0x14							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PCLK_FREQUENCY_BYTE_0	7:0	Configure pixel clock (PCLK) frequency (to the nearest kHz). If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.

VIDEO_TIMING_CFG_1 (0x1D7)

BIT	7	6	5	4	3	2	1	0
Field	PCLK_FREQUENCY_BYTE_1[7:0]							
Reset	0x44							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PCLK_FREQUENCY_BYTE_1	7:0	Configure pixel clock (PCLK) frequency (to the nearest kHz). If AUTO_TIMING_EN = 1, this field will be zeroed out. Default value is for 1080p.

VIDEO_TIMING_CFG_2 (0x1D8)

BIT	7	6	5	4	3	2	1	0
Field	PCLK_FREQUENCY_BYTE_2[7:0]							
Reset	0x02							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PCLK_FREQUENCY_BYTE_2	7:0	Configure pixel clock (PCLK) frequency (to the nearest kHz). If AUTO_TIMING_EN = 1, this field will be zeroed out. Default value is for 1080p.

VIDEO_TIMING_CFG_3 (0x1D9)

BIT	7	6	5	4	3	2	1	0
Field	H_ACTIVE_BYTE_0[7:0]							
Reset	0x80							

PRELIMINARY

Access Type	Write, Read							
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BITFIELD	BITS	DESCRIPTION	DECODE
H_ACTIVE_BYTE_0	7:0	Configure horizontal active (Hactive) resolution. Measured in pixels. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0xXX: Lower 8 bits of the horizontal resolution of the mainstream video source

VIDEO_TIMING_CFG_4 (0x1DA)

BIT	7	6	5	4	3	2	1	0
Field	H_ACTIVE_BYTE_1[7:0]							
Reset	0x07							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
H_ACTIVE_BYTE_1	7:0	Configure horizontal active (Hactive) resolution. Measured in pixels. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0xXX: Upper 8 bits of the horizontal resolution of the mainstream video source

VIDEO_TIMING_CFG_5 (0x1DB)

BIT	7	6	5	4	3	2	1	0
Field	H_FP_BYTE_0[7:0]							
Reset	0x58							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
H_FP_BYTE_0	7:0	Configure horizontal front porch (Hfp). Measured in pixels. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0xXX: Lower 8 bits of the horizontal front porch of the mainstream video source

VIDEO_TIMING_CFG_6 (0x1DC)

BIT	7	6	5	4	3	2	1	0
Field	H_FP_BYTE_1[7:0]							

PRELIMINARY

Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
H_FP_BYTE_1	7:0	Configure horizontal front porch (Hfp). Measured in pixels. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0XXX: Lower 8 bits of the horizontal front porch of the mainstream video source

VIDEO TIMING CFG 7 (0x1DD)

BIT	7	6	5	4	3	2	1	0
Field	H_SW_BYTE_0[7:0]							
Reset	0x2C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
H_SW_BYTE_0	7:0	Configure horizontal sync width (Hsw). Measured in pixels. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0XXX: Lower 8 bits of the horizontal sync width of the mainstream video source

VIDEO TIMING CFG 8 (0x1DE)

BIT	7	6	5	4	3	2	1	0
Field	H_SW_BYTE_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
H_SW_BYTE_1	7:0	Configure horizontal sync width (Hsw). Measured in pixels. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0XXX: Lower 8 bits of the horizontal sync width of the mainstream video source

VIDEO TIMING CFG 9 (0x1DF)

BIT	7	6	5	4	3	2	1	0
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PRELIMINARY

Field	H_BP_BYTE_0[7:0]							
Reset	0x94							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
H_BP_BYTE_0	7:0	Configure horizontal back porch (Hbp). Measured in pixels. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0XX: Lower 8 bits of the horizontal back porch of the mainstream video source

VIDEO TIMING CFG 10 (0x1E0)

BIT	7	6	5	4	3	2	1	0
Field	H_BP_BYTE_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
H_BP_BYTE_1	7:0	Configure horizontal back porch (Hbp). Measured in pixels. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0XX: Lower 8 bits of the horizontal back porch of the mainstream video source

VIDEO TIMING CFG 11 (0x1E1)

BIT	7	6	5	4	3	2	1	0
Field	V_ACTIVE_BYTE_0[7:0]							
Reset	0x38							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_ACTIVE_BYTE_0	7:0	Configure vertical active (Vactive) resolution. Measured in lines. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0XX: Lower 8 bits of the vertical resolution of the mainstream video source

PRELIMINARY

VIDEO TIMING CFG 12 (0x1E2)

BIT	7	6	5	4	3	2	1	0
Field	V_ACTIVE_BYTE_1[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_ACTIVE_BYTE_1	7:0	Configure vertical active (Vactive) resolution. Measured in lines. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0xXX: Upper 8 bits of the vertical resolution of the main stream video source

VIDEO TIMING CFG 13 (0x1E3)

BIT	7	6	5	4	3	2	1	0
Field	V_FP[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_FP	7:0	Configure vertical front porch (Vfp). Measured in lines. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0xXX: Lower 8 bits of the vertical front porch of the mainstream video source

VIDEO TIMING CFG 14 (0x1E4)

BIT	7	6	5	4	3	2	1	0
Field	V_SW[7:0]							
Reset	0x05							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_SW	7:0	Configure vertical sync width (Vsw). Measured in lines. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0xXX: Lower 8 bits of the vertical sync width of the mainstream video source

PRELIMINARY

VIDEO TIMING CFG 15 (0x1E5)

BIT	7	6	5	4	3	2	1	0
Field	V_BP[7:0]							
Reset	0x24							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_BP	7:0	Configure vertical back porch (Vbp). Measured in lines. If AUTO_TIMING_EN = 1, this field is zeroed out. Default value is for 1080p.	0xXX: Lower 8 bits of the vertical back porch of the mainstream video source

VIDEO TIMING CFG 16 (0x1E6)

BIT	7	6	5	4	3	2	1	0
Field	—	FORCE_EVENODD_PIXEL_MODE_EN	COLOR_DEPTH_MANUAL_MODE	COLOR_DEPTH_30BIT_SELECT	—	HS_VS_POLARITY_MANUAL_MODE	VS_POLARITY	HS_POLARITY
Reset	—	0x0	0x0	0x0	—	0x0	0x1	0x1
Access Type	—	Write, Read	Write, Read	Write, Read	—	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FORCE_EVENODD_PIXEL_MODE_EN	6	Force even-odd split mode	0x0: No action 0x1: force to even-odd split mode
COLOR_DEPTH_MANUAL_MODE	5	Enables color depth override to manually program the color depth to the value in register COLOR_DEPTH_30BIT_SELECT.	0x0: No action 0x1: Color depth override enabled
COLOR_DEPTH_30BIT_SELECT	4	Selects the color depth for the video stream if register COLOR_DEPTH_OVERRIDE_EN = 0b1.	0x0: Color depth override to 24 bpp (8 bits per color) 0x1: Color depth override to 30 bpp (10 bits per color)
HS_VS_POLARITY_MANUAL_MODE	2	Enables manual overwrite of VS/HS polarities	0x0: Use detected VS/HS polarities 0x1: Use VS/HS polarities specified in VS_POLARITY/HS_POLARITY bitfields
VS_POLARITY	1	VS pulse polarity	0x0: Negative VS polarity 0x1: Positive VS polarity
HS_POLARITY	0	HS signal polarity	0x0: Negative HS polarity 0x1: Positive HS polarity

PRELIMINARY

PSM STATE CFG_0 (0x1E7)

BIT	7	6	5	4	3	2	1	0
Field	PSM_STATE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PSM_STATE	7:0	<p>This register contains the desired state request to the PSM state machine by the user. After the PSM starts processing the user request, it changes the value in this register to either 0x00 or to 0x01.</p> <p>A value of 0x00 indicates that the user request was completed successfully by the PSM without error. A value of 0x01 indicates that the user request was not completed successfully by the PSM. That is, an error occurred. For more detailed status, refer to PSM_STATUS_STATUS_0 at 0x1E8.</p> <p>A value of 0x00 or 0x01 returned by the PSM serves as a handshake to the user to indicate that a new request can now be submitted.</p> <p>Rows in the table that do not have a Decode entry are reserved. Do not use these reserved values.</p> <p>Rows with entries in the Decode column show the user requests that are currently supported by the PSM.</p>	<p>0x0: Idle/previous state completed with no error 0x1: Idle/previous state completed with error 0x2 0x3 0x4 0x5: Train link, set up video, enable video 0x6 0x7: Set up/wait video, train link, enable video 0x8 0x9 0xA 0xB 0xC 0xD 0xE 0xF: Re-initialize (like HPD disconnect) 0x10: Disable VPG (use to stop VPG after VPG was set up) 0x11: Set up VPG, using registers or EDID for video timing (override timing received from GMSL serializer) 0x12: Set up VPG, using current video timing received from GMSL serializer 0x13 0x80: Set up HDCP (use to reinitialize HDCP after HDCP registers have been re-programmed)</p>

PSM STATUS_0 (0x1E8)

BIT	7	6	5	4	3	2	1	0
Field	PSM_STATUS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PSM_STATUS	7:0	<p>Contains detailed status of the processing of the user request at PSM_STATE (0x1E7) by the PSM. This register is only valid when PSM_STATE is either 0x00 or 0x01.</p> <p>The following are valid status values from the processing of the user request by the PSM:</p>	.

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
		<p>0xFF = Request is invalid or not supported</p> <p>0xFE = Request overrun. Proper handshake not followed and user request in PSM_STATE register updated by user before the PSM returned an idle status (0x00 or 0x01).</p> <p>0x01 = DP link not trained. For example, user requesting 0x12 without previously requesting DP link to be trained.</p> <p>0x02 = Invalid training parameters encountered</p> <p>0x03 = DP link training failed.</p> <p>Other values are illegal.</p>	

LUT_CTRL (0x502)

BIT	7	6	5	4	3	2	1	0
Field	–	–	LUT_MSB_DATA[1:0]	LUT_10_BIT_OUT	–	–	–	–
Reset	–	–	0x0	0b1	–	–	–	–
Access Type	–	–	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LUT_MSB_DATA	5:4	<p>These 2 bits are used as the MSB bits of the color LUT.</p> <p>When filling the LUT, write to this register first for each address and then write the LUT bits [7:0]. When LSB bits are written, these 2 bits are used as the MSB 2 bits for that address.</p>	<p>0x0: Write 00 to 2 MSB of 10-bit LUT</p> <p>0x1: Write 01 to 2 MSB of 10-bit LUT</p> <p>0x2: Write 10 to 2 MSB of 10-bit LUT</p> <p>0x3: Write 11 to 2 MSB of 10-bit LUT</p>
LUT_10_BIT_OUT	3	Selects if the color LUT should have an 8-bit or 10-bit output.	<p>0x0: 8-bit output</p> <p>0x1: 10-bit output</p>

VRX ASIL INJ (0x51F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FRC_DATAPATH_FAIL_INJ	LUT_CRC_BLUE_FAIL_INJ	LUT_CRC_GREEN_FAIL_INJ	LUT_CRC_RED_FAIL_INJ	LUT_DATAPATH_FAIL_INJ	WM_DATAPATH_FAIL_INJ
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0

Access Type	-	Write, Read					
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BITFIELD	BITS	DESCRIPTION	DECODE
FRC_DATAPATH_FAIL_INJ	5	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
LUT_CRC_BLUE_FAIL_INJ	4	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
LUT_CRC_GREEN_FAIL_INJ	3	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
LUT_CRC_RED_FAIL_INJ	2	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
LUT_DATAPATH_FAIL_INJ	1	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
WM_DATAPATH_FAIL_INJ	0	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected

LUT_CTRL (0x542)

BIT	7	6	5	4	3	2	1	0
Field	-	-	LUT_MSB_DATA[1:0]	LUT_10_BIT_OUT	-	-	-	-
Reset	-	-	0x0	0b1	-	-	-	-
Access Type	-	-	Write, Read	Write, Read	-	-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
LUT_MSB_DATA	5:4	These 2 bits are used as the MSB bits of the color LUT. When filling the LUT, write to this register first for each address and then write the LUT bits [7:0]. When LSB bits are written, these 2 bits are used as the MSB 2 bits for that address.	0x0: Write 00 to 2 MSB of 10-bit LUT 0x1: Write 01 to 2 MSB of 10-bit LUT 0x2: Write 10 to 2 MSB of 10-bit LUT 0x3: Write 11 to 2 MSB of 10-bit LUT
LUT_10_BIT_OUT	3	Selects if the color LUT should have an 8-bit or 10-bit output.	0x0: 8-bit output 0x1: 10-bit output

PRELIMINARY

PRBS_ERR (0x55B)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERROR_COUNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_ERROR_COUNT	7:0	Video PRBS Error Counter Clears on read.	0xxx: Number of video PRBS errors since last read

VRX_ASIL_INJ (0x55F)

BIT	7	6	5	4	3	2	1	0
Field	-	-	FRC_DATAPATH_FAIL_INJ	LUT_CRC_BLUE_FAIL_INJ	LUT_CRC_GREEN_FAIL_INJ	LUT_CRC_RED_FAIL_INJ	LUT_DATAPATH_FAIL_INJ	WM_DATAPATH_FAIL_INJ
Reset	-	-	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	-	-	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FRC_DATAPATH_FAIL_INJ	5	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
LUT_CRC_BLUE_FAIL_INJ	4	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
LUT_CRC_GREEN_FAIL_INJ	3	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
LUT_CRC_RED_FAIL_INJ	2	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected
LUT_DATAPATH_FAIL_INJ	1	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
WM_DATAPATH_FAIL_INJ	0	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: No error injected 0b1: Error injected

AUTH0 (0x600)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CYCLE_MODULO_H[1:0]	LOCAL_CHALLENGE_MAX[1:0]	—	—	AUTH_GLOBAL_PERIODIC	AUTH_GLOBAL_TRIGGER	AUTH_EN	
Reset	0b00	0b00	—	—	0b1	0b0	0b1	
Access Type	Write, Read	Write, Read	—	—	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CYCLE_MODULO_H	7:6	Modulo value for the frame cycle counter	0bxx: MSB bits for frame cycle modulo value
LOCAL_CHALLENGE_MAX	5:4	Selects desired number of local challenges.	0b00: One local challenge 0b01: Two local challenges 0b10: Three local challenges 0b11: Four local challenges
AUTH_GLOBAL_PERIODIC	2	Enables video authentication feature periodic global challenge mode.	0b0: Disabled 0b1: Enabled
AUTH_GLOBAL_TRIG	1	Enables video authentication feature global challenge trigger. User needs to create a rising edge.	0b0: Disabled 0b1: Enabled
AUTH_EN	0	Enables video authentication feature.	0b0: Disabled 0b1: Enabled

AUTH1 (0x601)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CYCLE_MODULO_L[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CYCLE_MODULO_L	7:0	Modulo value for the frame cycle counter	0XX: LSB bits for frame cycle modulo value

XMINL0a (0x602)

BIT	7	6	5	4	3	2	1	0
Field	XMIN0a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN0a_LSB	7:0	Local Challenge X coordinate minimum value least significant 8 bits. Minimum allowed value is 0x02.

XMINH0a (0x603)

BIT	7	6	5	4	3	2	1	0
Field	—	—	XMIN0a_MSB[5:0]					
Reset	—	—	0b000000					
Access Type	—	—	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN0a_MSB	5:0	Local Challenge X coordinate minimum value most significant 6 bits. Minimum allowed value is 0x02.

XMAXL0a (0x604)

BIT	7	6	5	4	3	2	1	0
Field	XMAX0a_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX0a_LSB	7:0	Local Challenge X coordinate maximum value least significant 8 bits.

XMAXH0a (0x605)

BIT	7	6	5	4	3	2	1	0

Field	-	-	XMAX0a_MSB[5:0]
Reset	-	-	0b000000
Access Type	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION
XMAX0a_MSB	5:0	Local Challenge X coordinate maximum value most significant 6 bits.

XMINL1a (0x606)

BIT	7	6	5	4	3	2	1	0
Field	XMIN1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN1a_LSB	7:0	Local Challenge X coordinate minimum value least significant 8 bits.

XMINH1a (0x607)

BIT	7	6	5	4	3	2	1	0
Field	-	-	XMIN1a_MSB[5:0]					
Reset	-	-	0b000000					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN1a_MSB	5:0	Local Challenge X coordinate minimum value most significant 6 bits.

XMAXL1a (0x608)

BIT	7	6	5	4	3	2	1	0
Field	XMAX1a_LSB[7:0]							
Reset	0x00							

PRELIMINARY

Access Type	Write, Read							
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BITFIELD	BITS	DESCRIPTION
XMAX1a_LSB	7:0	Local Challenge X coordinate maximum value least significant 8 bits.

XMAXH1a (0x609)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	XMAX1a_MSB[5:0]						
Reset	–	–	0b000000						
Access Type	–	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
XMAX1a_MSB	5:0	Local Challenge X coordinate maximum value most significant 6 bits.

XMINL2a (0x60A)

BIT	7	6	5	4	3	2	1	0
Field	XMIN2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN2a_LSB	7:0	Local Challenge X coordinate minimum value least significant 8 bits.

XMINH2a (0x60B)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	XMIN2a_MSB[5:0]						
Reset	–	–	0b000000						
Access Type	–	–	Write, Read						

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
XMIN2a_MSB	5:0	Local Challenge X coordinate minimum value most significant 6 bits.

XMAXL2a (0x60C)

BIT	7	6	5	4	3	2	1	0
Field	XMAX2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX2a_LSB	7:0	Local Challenge X coordinate maximum value least significant 8 bits.

XMAXH2a (0x60D)

BIT	7	6	5	4	3	2	1	0
Field	-	-	XMAX2a_MSB[5:0]					
Reset	-	-	0b000000					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX2a_MSB	5:0	Local Challenge X coordinate maximum value most significant 6 bits.

XMINL3a (0x60E)

BIT	7	6	5	4	3	2	1	0
Field	XMIN3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN3a_LSB	7:0	Local Challenge X coordinate minimum value least significant 8 bits.

XMINH3a (0x60F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN3a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN3a_MSB	5:0	Local Challenge X coordinate minimum value most significant 6 bits.

XMAXL3a (0x610)

BIT	7	6	5	4	3	2	1	0
Field	XMAX3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX3a_LSB	7:0	Local Challenge X coordinate maximum value least significant 8 bits.

XMAXH3a (0x611)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX3a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX3a_MSB	5:0	Local Challenge X coordinate maximum value most significant 6 bits.

XMINL0b (0x612)

BIT	7	6	5	4	3	2	1	0
Field	XMIN0b_LSB[7:0]							

PRELIMINARY

Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN0b_LSB	7:0	Local Challenge X coordinate minimum value least significant 8 bits. Minimum allowed value is 0x02.

XMINH0b (0x613)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	XMIN0b_MSB[5:0]						
Reset	–	–	0b000000						
Access Type	–	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
XMIN0b_MSB	5:0	Local Challenge X coordinate minimum value most significant 6 bits. Minimum allowed value is 0x02.

XMAXL0b (0x614)

BIT	7	6	5	4	3	2	1	0
Field	XMAX0b_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX0b_LSB	7:0	Local Challenge X coordinate maximum value least significant 8 bits.

XMAXH0b (0x615)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	XMAX0b_MSB[5:0]						
Reset	–	–	0b000000						

PRELIMINARY

Access Type	-	-	Write, Read
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BITFIELD	BITS	DESCRIPTION
XMAX0b_MSB	5:0	Local Challenge X coordinate maximum value most significant 6 bits.

XMINL1b (0x616)

BIT	7	6	5	4	3	2	1	0
Field	XMIN1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN1b_LSB	7:0	Local Challenge X coordinate minimum value least significant 8 bits.

XMINH1b (0x617)

BIT	7	6	5	4	3	2	1	0
Field	-	-	XMIN1b_MSB[5:0]					
Reset	-	-	0b000000					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN1b_MSB	5:0	Local Challenge X coordinate minimum value most significant 6 bits.

XMAXL1b (0x618)

BIT	7	6	5	4	3	2	1	0
Field	XMAX1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
XMAX1b_LSB	7:0	Local Challenge X coordinate maximum value least significant 8 bits.

XMAXH1b (0x619)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX1b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX1b_MSB	5:0	Local Challenge X coordinate maximum value most significant 6 bits.

XMINL2b (0x61A)

BIT	7	6	5	4	3	2	1	0
Field	XMIN2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN2b_LSB	7:0	Local Challenge X coordinate minimum value least significant 8 bits.

XMINH2b (0x61B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN2b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN2b_MSB	5:0	Local Challenge X coordinate minimum value most significant 6 bits.

PRELIMINARY

XMAXL2b (0x61C)

BIT	7	6	5	4	3	2	1	0
Field	XMAX2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX2b_LSB	7:0	Local Challenge X coordinate maximum value least significant 8 bits.

XMAXH2b (0x61D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX2b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX2b_MSB	5:0	Local Challenge X coordinate maximum value most significant 6 bits.

XMINL3b (0x61E)

BIT	7	6	5	4	3	2	1	0
Field	XMIN3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN3b_LSB	7:0	Local Challenge X coordinate minimum value least significant 8 bits.

XMINH3b (0x61F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN3b_MSB[5:0]					

Reset	-	-	0b000000
Access Type	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION
XMIN3b_MSB	5:0	Local Challenge X coordinate minimum value most significant 6 bits.

XMAXL3b (0x620)

BIT	7	6	5	4	3	2	1	0
Field	XMAX3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX3b_LSB	7:0	Local Challenge X coordinate maximum value least significant 8 bits.

XMAXH3b (0x621)

BIT	7	6	5	4	3	2	1	0
Field	-	-	XMAX3b_MSB[5:0]					
Reset	-	-	0b000000					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX3b_MSB	5:0	Local Challenge X coordinate maximum value most significant 6 bits.

YMINL0a (0x622)

BIT	7	6	5	4	3	2	1	0
Field	YMIN0a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
YMIN0a_LSB	7:0	Local Challenge Y coordinate minimum value least significant 8 bits.

YMINH0a (0x623)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN0a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN0a_MSB	5:0	Local Challenge Y coordinate minimum value most significant 6 bits.

YMAXL0a (0x624)

BIT	7	6	5	4	3	2	1	0
Field	YMAX0a_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX0a_LSB	7:0	Local Challenge Y coordinate maximum value least significant 8 bits.

YMAXH0a (0x625)

BIT	7	6	5	4	3	2	1	0
Field	FRAME0a_MSB[1:0]							
Reset	0b00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME0a_MSB	7:6	Local challenge frame number most significant 2 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

BITFIELD	BITS	DESCRIPTION
YMAX0a_MSB	5:0	Local Challenge Y coordinate maximum value most significant 6 bits.

frame0a (0x626)

BIT	7	6	5	4	3	2	1	0
Field	FRAME0a_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME0a_LSB	7:0	Local challenge frame number least significant 8 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

YMINL1a (0x627)

BIT	7	6	5	4	3	2	1	0
Field	YMIN1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN1a_LSB	7:0	Local Challenge Y coordinate minimum value least significant 8 bits.

YMINH1a (0x628)

BIT	7	6	5	4	3	2	1	0
Field	—	—	YMIN1a_MSB[5:0]					
Reset	—	—	0b000000					
Access Type	—	—	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN1a_MSB	5:0	Local Challenge Y coordinate minimum value most significant 6 bits.

PRELIMINARY

YMAXL1a (0x629)

BIT	7	6	5	4	3	2	1	0
Field	YMAX1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX1a_LSB	7:0	Local Challenge Y coordinate maximum value least significant 8 bits.

YMAXH1a (0x62A)

BIT	7	6	5	4	3	2	1	0
Field	FRAME1a_MSB[1:0]							
Reset	0b00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME1a_MSB	7:6	Local challenge frame number most significant 2 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).
YMAX1a_MSB	5:0	Local Challenge Y coordinate maximum value most significant 6 bits.

frame1a (0x62B)

BIT	7	6	5	4	3	2	1	0
Field	FRAME1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME1a_LSB	7:0	Local challenge frame number least significant 8 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

PRELIMINARY

YMINL2a (0x62C)

BIT	7	6	5	4	3	2	1	0
Field	YMIN2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN2a_LSB	7:0	Local Challenge Y coordinate minimum value least significant 8 bits.

YMINH2a (0x62D)

BIT	7	6	5	4	3	2	1	0		
Field	–	–	YMIN2a_MSB[5:0]							
Reset	–	–	0b000000							
Access Type	–	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN2a_MSB	5:0	Local Challenge Y coordinate minimum value most significant 6 bits.

YMAXL2a (0x62E)

BIT	7	6	5	4	3	2	1	0
Field	YMAX2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX2a_LSB	7:0	Local Challenge Y coordinate maximum value least significant 8 bits.

YMAXH2a (0x62F)

BIT	7	6	5	4	3	2	1	0
Field	FRAME2a_MSB[1:0]							

**GMSL3/2 eDP Deserializers with
Optional Decompression, HDCP,
Daisy Chain, and Ethernet**

MAX96860/MAX96862/MAX96864

Reset	0b00	0b000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
FRAME2a_MSB	7:6	Local challenge frame number most significant 2 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).
YMAX2a_MSB	5:0	Local Challenge Y coordinate maximum value most significant 6 bits.

frame2a (0x630)

BIT	7	6	5	4	3	2	1	0
Field	FRAME2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME2a_LSB	7:0	Local challenge frame number least significant 8 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

YMINL3a (0x631)

BIT	7	6	5	4	3	2	1	0
Field	YMIN3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN3a_LSB	7:0	Local Challenge Y coordinate minimum value least significant 8 bits.

YMINH3a (0x632)

BIT	7	6	5	4	3	2	1	0
Field	YMIN3a_MSB[5:0]							

PRELIMINARY

Reset	-	-	0b000000
Access Type	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION
YMIN3a_MSB	5:0	Local Challenge Y coordinate minimum value most significant 6 bits.

YMAXL3a (0x633)

BIT	7	6	5	4	3	2	1	0
Field	YMAX3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX3a_LSB	7:0	Local Challenge Y coordinate maximum value least significant 8 bits.

YMAXH3a (0x634)

BIT	7	6	5	4	3	2	1	0
Field	FRAME3a_MSB[1:0]							
Reset	0b00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME3a_MSB	7:6	Local challenge frame number most significant 2 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).
YMAX3a_MSB	5:0	Local Challenge Y coordinate maximum value most significant 6 bits.

frame3a (0x635)

BIT	7	6	5	4	3	2	1	0
Field	FRAME3a_LSB[7:0]							
Reset	0x00							

PRELIMINARY

Access Type	Write, Read							
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BITFIELD	BITS	DESCRIPTION
FRAME3a_LSB	7:0	Local challenge frame number least significant 8 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

YMINL0b (0x636)

BIT	7	6	5	4	3	2	1	0
Field	YMIN0b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN0b_LSB	7:0	Local Challenge Y coordinate minimum value least significant 8 bits.

YMINH0b (0x637)

BIT	7	6	5	4	3	2	1	0
Field	—	—	YMIN0b_MSB[5:0]					
Reset	—	—	0b000000					
Access Type	—	—	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN0b_MSB	5:0	Local Challenge Y coordinate minimum value most significant 6 bits.

YMAXL0b (0x638)

BIT	7	6	5	4	3	2	1	0
Field	YMAX0b_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
YMAX0b_LSB	7:0	Local Challenge Y coordinate maximum value least significant 8 bits.

YMAXH0b (0x639)

BIT	7	6	5	4	3	2	1	0
Field	FRAME0b_MSB[1:0]							YMAX0b_MSB[5:0]
Reset	0b00							0b000000
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
FRAME0b_MSB	7:6	Local challenge frame number most significant 2 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).
YMAX0b_MSB	5:0	Local Challenge Y coordinate maximum value most significant 6 bits.

frame0b (0x63A)

BIT	7	6	5	4	3	2	1	0
Field	FRAME0b_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME0b_LSB	7:0	Local challenge frame number least significant 8 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

YMINL1b (0x63B)

BIT	7	6	5	4	3	2	1	0
Field	YMIN1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN1b_LSB	7:0	Local Challenge Y coordinate minimum value least significant 8 bits.

YMINH1b (0x63C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN1b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN1b_MSB	5:0	Local Challenge Y coordinate minimum value most significant 6 bits.

YMAXL1b (0x63D)

BIT	7	6	5	4	3	2	1	0
Field	YMAX1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX1b_LSB	7:0	Local Challenge Y coordinate maximum value least significant 8 bits.

YMAXH1b (0x63E)

BIT	7	6	5	4	3	2	1	0
Field	FRAME1b_MSB[1:0]							
Reset	0b00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME1b_MSB	7:6	Local challenge frame number most significant 2 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

BITFIELD	BITS	DESCRIPTION
YMAX1b_MSB	5:0	Local Challenge Y coordinate maximum value most significant 6 bits.

frame1b (0x63F)

BIT	7	6	5	4	3	2	1	0
Field	FRAME1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME1b_LSB	7:0	Local challenge frame number least significant 8 bit. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

YMINL2b (0x640)

BIT	7	6	5	4	3	2	1	0
Field	YMIN2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN2b_LSB	7:0	Local Challenge Y coordinate minimum value least significant 8 bits.

YMINH2b (0x641)

BIT	7	6	5	4	3	2	1	0
Field	—	—	YMIN2b_MSB[5:0]					
Reset	—	—	0b000000					
Access Type	—	—	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN2b_MSB	5:0	Local Challenge Y coordinate minimum value most significant 6 bits.

PRELIMINARY

YMAXL2b (0x642)

BIT	7	6	5	4	3	2	1	0
Field	YMAX2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX2b_LSB	7:0	Local Challenge Y coordinate maximum value least significant 8 bits.

YMAXH2b (0x643)

BIT	7	6	5	4	3	2	1	0
Field	FRAME2b_MSB[1:0]							
Reset	0b00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME2b_MSB	7:6	Local challenge frame number most significant 2 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).
YMAX2b_MSB	5:0	Local Challenge Y coordinate maximum value most significant 6 bits.

frame2b (0x644)

BIT	7	6	5	4	3	2	1	0
Field	FRAME2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME2b_LSB	7:0	Local challenge frame number least significant 8 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

PRELIMINARY

YMINL3b (0x645)

BIT	7	6	5	4	3	2	1	0
Field	YMIN3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN3b_LSB	7:0	Local Challenge Y coordinate minimum value least significant 8 bits.

YMINH3b (0x646)

BIT	7	6	5	4	3	2	1	0		
Field	—	—	YMIN3b_MSB[5:0]							
Reset	—	—	0b000000							
Access Type	—	—	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN3b_MSB	5:0	Local Challenge Y coordinate minimum value most significant 6 bits.

YMAXL3b (0x647)

BIT	7	6	5	4	3	2	1	0
Field	YMAX3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX3b_LSB	7:0	Local Challenge Y coordinate maximum value least significant 8 bits.

YMAXH3b (0x648)

BIT	7	6	5	4	3	2	1	0
Field	FRAME3b_MSB[1:0]							

PRELIMINARY

Reset	0b00	0b000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
FRAME3b_MSB	7:6	Local challenge frame number most significant 2 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).
YMAX3b_MSB	5:0	Local Challenge Y coordinate maximum value most significant 6 bits.

frame3b (0x649)

BIT	7	6	5	4	3	2	1	0
Field	FRAME3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME3b_LSB	7:0	Local challenge frame number least significant 8 bits. Decimal 511 value is reserved (combined 10-bit value of the frame _MSB and _LSB).

out1 (0x64A)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CNT_MSB	–	VA_DONE_FLAG	–	VA_DONE_PIN	A_OR_B	AUTH_DONE_B	AUTH_DONE_A
Reset	0b0	–	0b0	–	0b0	0b0	0b0	0b0
Access Type	Read Only	–	Read Only	–	Write, Read	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CNT_MSB	7	Frame counter value MSB bit.	0bx: MSB bit for frame cycle counter value
VA_DONE_FLAG	5	Video authentication done status flag. This flag is automatically cleared when the next set of authentication challenge starts.	0b0: Running 0b1: Challenge complete
VA_DONE_PIN	3	Enables video authentication done status to be shown on GPIO pins.	0b0: Disabled 0b1: Enabled

PRELIMINARY

PRELIMINARY

out1a (0x64B)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CNT_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CNT_LSB	7:0	Frame counter value LSB bits.	0xXX: LSB bits for frame cycle counter value

out2 (0x64C)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_A_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_A_0	7:0	CRC result for Challenge A. Valid only at the rising edge of done signal.

out3 (0x64D)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_A_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_A_1	7:0	CRC result for Challenge A. Valid only at the rising edge of done signal.

out4 (0x64E)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_A_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_A_2	7:0	CRC result for Challenge A. Valid only at the rising edge of done signal.

out5 (0x64F)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_A_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_A_3	7:0	CRC result for Challenge A. Valid only at the rising edge of done signal.

out6 (0x650)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_B_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_B_0	7:0	CRC result for Challenge B. Valid only at the rising edge of done signal.

out7 (0x651)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_B_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_B_1	7:0	CRC result for Challenge B. Valid only at the rising edge of done signal.

out8 (0x652)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_B_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_B_2	7:0	CRC result for Challenge B. Valid only at the rising edge of done signal.

out9 (0x653)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_B_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_B_3	7:0	CRC result for Challenge B. Valid only at the rising edge of done signal.

outa (0x654)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_0[7:0]							

Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_0	7:0	Full-Frame CRC Result. Valid only when VID_LOCK = 0b1.

outb (0x655)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_1	7:0	Full-Frame CRC Result. Valid only when VID_LOCK = 0b1.

outc (0x656)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_2	7:0	Full-Frame CRC Result. Valid only when VID_LOCK = 0b1.

outd (0x657)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_3[7:0]							
Reset	0x00							
Access Type	Read Only							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_3	7:0	Full-Frame CRC Result. Valid only when VID_LOCK = 0b1.

PSM TRIM REV 0 (0xE76)

BIT	7	6	5	4	3	2	1	0
Field	PSM_TRIM_MINOR_REV[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSM_TRIM_MINOR_REV	7:0	Minor revision of PMX patch OTP

PSM TRIM REV 1 (0xE77)

BIT	7	6	5	4	3	2	1	0
Field	PSM_TRIM_MAJOR_REV[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSM_TRIM_MAJOR_REV	7:0	Major revision of PMX patch OTP

REGCRC0 (0x1F00)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	GEN_ROLLING_CRC	I2C_WR_COMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
Reset	—	—	—	0b0	0b0	0b0	0b0	0b0
Access Type	—	—	—	Write, Read	Write Only Clears All	Write, Read	Write, Read	Write Clears All, Read

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_ROLLING_CRC	4	Calculates CRC using additional 4-bit counter, so CRC value cycles every 16 invocations	0b0: Disabled 0b1: Enabled
I2C_WR_COMPUTE	3	CRC computing trigger. Self-clearing.	0b0: Disabled 0b1: Enabled
PERIODIC_COMPUTE	2	CRC checking on periodic basis, based on CRC_PERIOD value.	0b0: Disabled 0b1: Enabled
CHECK_CRC	1	Upon calculation of CRC, compare with previous calculation except on first time through. On mismatch, issue ERRB.	0b0: Disabled 0b1: Enabled
RESET_CRC	0	Reset CRC value to 0xFFFF.	0b0: Reserved 0b1: One shot trigger for Reset

REGCRC1 (0x1F01)

BIT	7	6	5	4	3	2	1	0
Field	CRC_PERIOD[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CRC_PERIOD	7:0	Period for CRC recomputation Period = (value + 1) * 2ms

REGCRC2 (0x1F02)

BIT	7	6	5	4	3	2	1	0
Field	REGCRC LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGCRC LSB	7:0	CRC result LSB

REGCRC3 (0x1F03)

BIT	7	6	5	4	3	2	1	0

Field	REGCRC_MSB[7:0]
Reset	0x00
Access Type	Read Only

BITFIELD	BITS	DESCRIPTION
REGCRC_MSB	7:0	CRC result MSB

CC_CRC0 (0x1F20)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_VAL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CC_CRC_VAL	7:0	Calculated CRC value for the last write transaction

CC_CRC1 (0x1F21)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_LSB	7:0	Bits [7:0] of current message counter value

CC_CRC2 (0x1F22)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_MSB[7:0]							
Reset	0x00							

PRELIMINARY

Access Type	Read Only							
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BITFIELD	BITS	DESCRIPTION
MSGCNTR_MSB	7:0	Bits [15:8] of current message counter value

CC_CRC3 (0x1F23)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CC_CRC_ERR_CNT	7:0	Number of CC CRC errors detected

CC_CRC4 (0x1F24)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_ERR_CNT	7:0	Number of Message Counter errors detected

CC_RTTN_CRC_ERR (0x1F26)

BIT	7	6	5	4	3	2	1	0
Field	INJECT_RTTN_CRC_ERR							
Reset	0b0							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
INJECT_RTTN_CRC_ERR	0	Set this bit before going into sleep mode to inject error to RTTN CRC value. Use for ASIL evaluation purposes. Do not add this register to RTTN map.

LUT_A (0x2000)

Start address for color lookup table COLOR_A LUT_X for Video Pipeline X.

LUT_B (0x2100)

Start address for color lookup table COLOR_B LUT_X for Video Pipeline X.

LUT_C (0x2200)

Start address for color lookup table COLOR_C LUT_X for Video Pipeline X.

TELLTALE CTRL REG 0 (0x3000)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	TELLTALE_FORCE_BA_NK_B	TELLTALE_FORCE_BA_NK_A	TELLTALE_PERIODIC_MODE	TELLTALE_TRIGGER_MODE	TELLTALE_DET_EN
Reset	-	-	-	0b0	0b0	0b1	0b0	0b0
Access Type	-	-	-	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TELLTALE_FORCE_BANK_B	4	Force state machine to work on Bank B only	
TELLTALE_FORCE_BANK_A	3	Force state machine to work on Bank A only	
TELLTALE_PERIODIC_MODE	2	Periodic mode selection	0x0: Not periodic mode 0x1: Periodic mode
TELLTALE_TRIGGER_MODE	1	Trigger mode control signal	0x0: No action 0x1: Trigger telltale detection
TELLTALE_DET_EN	0	Enable telltale detection block	0x0: Disabled 0x1: Enabled

TELLTALE CTRL REG 1 (0x3001)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI_INTERRUPT_EN[3:0]							BANK_A_ROI_INTERRUPT_EN[3:0]
Reset	0xF							0xF

Access Type	Write, Read	Write, Read
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BITFIELD	BITS	DESCRIPTION
BANK_B_ROI_INTERRUPT_EN	7:4	Mask (Enable) for Bank-specific ROI operations
BANK_A_ROI_INTERRUPT_EN	3:0	Mask (Enable) for Bank-specific ROI operations

TELLTALE STATUS REG 0 (0x3002)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI_ERROR[3:0]						BANK_A_ROI_ERROR[3:0]	
Reset	0x0						0x0	
Access Type	Read Only						Read Only	

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI_ERROR	7:4	Error indicator bits per region for Bank B
BANK_A_ROI_ERROR	3:0	Error indicator bits per region for Bank A

TELLTALE STATUS REG 1 (0x3003)

BIT	7	6	5	4	3	2	1	0
Field	TELLTALE_BANK_CALC_DONE	TELLTALE_ACTIVE_BANK_A_OR_B				-	-	-
Reset	0b0	0b0				-	-	-
Access Type	Read Only	Read Only				-	-	-

BITFIELD	BITS	DESCRIPTION	DECODE
TELLTALE_BANK_CALC_DONE	7	Telltale detection completion indicator	0x0: Not complete 0x1: Complete
TELLTALE_ACTIVE_BANK_A_OR_B	6	Indicates Bank A or Bank B active signal	

REF COLOR GENERAL (0x3008)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_INV_H UE	REF_COLOR_INV_S AT	REF_COLOR_INV_L UM	-	-	-	REF_COLOR_HUE_MAX _H	REF_COLOR_HUE_MIN _H

PRELIMINARY

Reset	0x1	0x0	0x0	-	-	-	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	-	-	-	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_INV_HUE	7	Reference color hue values inversion enable
REF_COLOR_INV_SAT	6	Reference color saturation values inversion enable
REF_COLOR_INV_LUM	5	Reference color luminance values inversion enable
REF_COLOR_HUE_MAX_H	1	Reference color hue maximum value
REF_COLOR_HUE_MIN_H	0	Reference color hue minimum value

REF COLOR HUE MAX L (0x3009)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MAX_L[7:0]							
Reset	0x4A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MAX_L	7:0	Reference color hue maximum value

REF COLOR HUE MIN (0x300A)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MIN_L[7:0]							
Reset	0x0A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MIN_L	7:0	Reference color hue minimum value

PRELIMINARY

REF COLOR SAT MAX (0x300B)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_COLOR_SAT_MAX[6:0]						
Reset	–	0x64						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MAX	6:0	Reference color saturation maximum value

REF COLOR SAT MIN (0x300C)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_COLOR_SAT_MIN[6:0]						
Reset	–	0x28						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MIN	6:0	Reference color saturation minimum value

REF COLOR LUM MAX (0x300D)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_COLOR_LUM_MAX[6:0]						
Reset	–	0x4B						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MAX	6:0	Reference color luminance maximum value

REF COLOR LUM MIN (0x300E)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_COLOR_LUM_MIN[6:0]						

Reset	-	0x19
Access Type	-	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MIN	6:0	Reference color luminance minimum value

REF COLOR GENERAL (0x3010)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_INV_HUE	REF_COLOR_INV_SAT	REF_COLOR_INV_LUM	-	-	-	REF_COLOR_HUE_MAX_H	REF_COLOR_HUE_MIN_H
Reset	0x0	0x0	0x0	-	-	-	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	-	-	-	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_INV_HUE	7	Reference color hue values inversion enable
REF_COLOR_INV_SAT	6	Reference color saturation values inversion enable
REF_COLOR_INV_LUM	5	Reference color luminance values inversion enable
REF_COLOR_HUE_MAX_H	1	Reference color hue maximum value
REF_COLOR_HUE_MIN_H	0	Reference color hue minimum value

REF COLOR HUE MAX L (0x3011)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MAX_L[7:0]							
Reset	0x33							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MAX_L	7:0	Reference color hue maximum value

PRELIMINARY

REF COLOR HUE MIN (0x3012)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MIN_L[7:0]							
Reset	0x0E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MIN_L	7:0	Reference color hue minimum value

REF COLOR SAT MAX (0x3013)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_SAT_MAX[6:0]							
Reset	–	0x64							
Access Type	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MAX	6:0	Reference color saturation maximum value

REF COLOR SAT MIN (0x3014)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_SAT_MIN[6:0]							
Reset	–	0x28							
Access Type	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MIN	6:0	Reference color saturation minimum value

REF COLOR LUM MAX (0x3015)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_LUM_MAX[6:0]							

PRELIMINARY

Reset	-	0x4B
Access Type	-	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MAX	6:0	Reference color luminance maximum value

REF_COLOR_LUM_MIN (0x3016)

BIT	7	6	5	4	3	2	1	0
Field	-	REF_COLOR_LUM_MIN[6:0]						
Reset	-	0x19						
Access Type	-	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MIN	6:0	Reference color luminance minimum value

REF_COLOR_GENERAL (0x3018)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_INV_HUE	REF_COLOR_INV_SAT	REF_COLOR_INV_LUM	-	-	-	REF_COLOR_HUE_MAX_H	REF_COLOR_HUE_MIN_H
Reset	0x0	0x0	0x0	-	-	-	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	-	-	-	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_INV_HUE	7	Reference color hue values inversion enable
REF_COLOR_INV_SAT	6	Reference color saturation values inversion enable
REF_COLOR_INV_LUM	5	Reference color luminance values inversion enable
REF_COLOR_HUE_MAX_H	1	Reference color hue maximum value
REF_COLOR_HUE_MIN_H	0	Reference color hue minimum value

PRELIMINARY

REF COLOR HUE MAX L (0x3019)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MAX_L[7:0]							
Reset	0xA7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MAX_L	7:0	Reference color hue maximum value

REF COLOR HUE MIN (0x301A)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MIN_L[7:0]							
Reset	0x57							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MIN_L	7:0	Reference color hue minimum value

REF COLOR SAT MAX (0x301B)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_SAT_MAX[6:0]							
Reset	–	0x64							
Access Type	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MAX	6:0	Reference color saturation maximum value

REF COLOR SAT MIN (0x301C)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_SAT_MIN[6:0]							

Reset	–	0x28
Access Type	–	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MIN	6:0	Reference color saturation minimum value

REF COLOR LUM MAX (0x301D)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_COLOR_LUM_MAX[6:0]						
Reset	–	0x4B						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MAX	6:0	Reference color luminance maximum value

REF COLOR LUM MIN (0x301E)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_COLOR_LUM_MIN[6:0]						
Reset	–	0x19						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MIN	6:0	Reference color luminance minimum value

REF COLOR GENERAL (0x3020)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_INV_HUE	REF_COLOR_INV_SAT	REF_COLOR_INV_LUM	–	–	–	REF_COLOR_HUE_MAX_H	REF_COLOR_HUE_MIN_H
Reset	0x0	0x0	0x0	–	–	–	0b1	0b0

PRELIMINARY

Access Type	Write, Read	Write, Read	Write, Read	-	-	-	Write, Read	Write, Read
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BITFIELD	BITS	DESCRIPTION
REF_COLOR_INV_HUE	7	Reference color hue values inversion enable
REF_COLOR_INV_SAT	6	Reference color saturation values inversion enable
REF_COLOR_INV_LUM	5	Reference color luminance values inversion enable
REF_COLOR_HUE_MAX_H	1	Reference color hue maximum value
REF_COLOR_HUE_MIN_H	0	Reference color hue minimum value

REF COLOR HUE MAX L (0x3021)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MAX_L[7:0]							
Reset	0x0B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MAX_L	7:0	Reference color hue maximum value

REF COLOR HUE MIN (0x3022)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MIN_L[7:0]							
Reset	0xBC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MIN_L	7:0	Reference color hue minimum value

REF COLOR SAT MAX (0x3023)

BIT	7	6	5	4	3	2	1	0
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Field	-	REF_COLOR_SAT_MAX[6:0]
Reset	-	0x64
Access Type	-	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MAX	6:0	Reference color saturation maximum value

REF_COLOR_SAT_MIN (0x3024)

BIT	7	6	5	4	3	2	1	0
Field	-	REF_COLOR_SAT_MIN[6:0]						
Reset	-	0x28						
Access Type	-	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MIN	6:0	Reference color saturation minimum value

REF_COLOR_LUM_MAX (0x3025)

BIT	7	6	5	4	3	2	1	0
Field	-	REF_COLOR_LUM_MAX[6:0]						
Reset	-	0x4B						
Access Type	-	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MAX	6:0	Reference color luminance maximum value

REF_COLOR_LUM_MIN (0x3026)

BIT	7	6	5	4	3	2	1	0
Field	-	REF_COLOR_LUM_MIN[6:0]						
Reset	-	0x19						

PRELIMINARY

Access Type	-	Write, Read
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BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MIN	6:0	Reference color luminance minimum value

REF COLOR GENERAL (0x3028)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_INV_HUE	REF_COLOR_INV_SAT	REF_COLOR_INV_LUM	-	-	-	REF_COLOR_HUE_MAX_H	REF_COLOR_HUE_MIN_H
Reset	0x0	0x0	0x0	-	-	-	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	-	-	-	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_INV_HUE	7	Reference color hue values inversion enable
REF_COLOR_INV_SAT	6	Reference color saturation values inversion enable
REF_COLOR_INV_LUM	5	Reference color luminance values inversion enable
REF_COLOR_HUE_MAX_H	1	Reference color hue maximum value
REF_COLOR_HUE_MIN_H	0	Reference color hue minimum value

REF COLOR HUE MAX_L (0x3029)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MAX_L[7:0]							
Reset	0x68							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MAX_L	7:0	Reference color hue maximum value

PRELIMINARY

REF COLOR HUE MIN (0x302A)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MIN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MIN_L	7:0	Reference color hue minimum value

REF COLOR SAT MAX (0x302B)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_SAT_MAX[6:0]							
Reset	–	0x64							
Access Type	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MAX	6:0	Reference color saturation maximum value

REF COLOR SAT MIN (0x302C)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_SAT_MIN[6:0]							
Reset	–	0x00							
Access Type	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MIN	6:0	Reference color saturation minimum value

REF COLOR LUM MAX (0x302D)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_LUM_MAX[6:0]							

Reset	-	0x64
Access Type	-	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MAX	6:0	Reference color luminance maximum value

REF_COLOR_LUM_MIN (0x302E)

BIT	7	6	5	4	3	2	1	0
Field	-	REF_COLOR_LUM_MIN[6:0]						
Reset	-	0x5F						
Access Type	-	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MIN	6:0	Reference color luminance minimum value

REF_COLOR_GENERAL (0x3030)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_INV_HUE	REF_COLOR_INV_SAT	REF_COLOR_INV_LUM	-	-	-	REF_COLOR_HUE_MAX_H	REF_COLOR_HUE_MIN_H
Reset	0x0	0x0	0x0	-	-	-	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	-	-	-	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_INV_HUE	7	Reference color hue values inversion enable
REF_COLOR_INV_SAT	6	Reference color saturation values inversion enable
REF_COLOR_INV_LUM	5	Reference color luminance values inversion enable
REF_COLOR_HUE_MAX_H	1	Reference color hue maximum value
REF_COLOR_HUE_MIN_H	0	Reference color hue minimum value

PRELIMINARY

REF COLOR HUE MAX L (0x3031)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MAX_L[7:0]							
Reset	0x68							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MAX_L	7:0	Reference color hue maximum value

REF COLOR HUE MIN (0x3032)

BIT	7	6	5	4	3	2	1	0
Field	REF_COLOR_HUE_MIN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_HUE_MIN_L	7:0	Reference color hue minimum value

REF COLOR SAT MAX (0x3033)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_SAT_MAX[6:0]							
Reset	–	0x19							
Access Type	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MAX	6:0	Reference color saturation maximum value

REF COLOR SAT MIN (0x3034)

BIT	7	6	5	4	3	2	1	0	
Field	–	REF_COLOR_SAT_MIN[6:0]							

Reset	–	0x00
Access Type	–	Write, Read

BITFIELD	BITS	DESCRIPTION
REF_COLOR_SAT_MIN	6:0	Reference color saturation minimum value

REF COLOR LUM MAX (0x3035)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_COLOR_LUM_MAX[6:0]						
Reset	–	0x4B						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MAX	6:0	Reference color luminance maximum value

REF COLOR LUM MIN (0x3036)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_COLOR_LUM_MIN[6:0]						
Reset	–	0x19						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
REF_COLOR_LUM_MIN	6:0	Reference color luminance minimum value

BANK A STATUS (0x3038)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_A_CALC_DONE	BANK_A_FRAME_COUNT[1:0]	
Reset	–	–	–	–	–	0b0	0x0	
Access Type	–	–	–	–	–	Read Only	Read Only	

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
BANK_A_CALC_DONE	2	Telltale detection completion indicator for Bank A	0x0: Not complete 0x1: Complete
BANK_A_FRAME_COUNT	1:0	Frame counter value indicating active frame number for Bank A	

BANK A ROI 1 0 ERROR (0x3039)

BIT	7	6	5	4	3	2	1	0
Field	-	BANK_A_ROI_1_C OLOR_2_ERROR	BANK_A_ROI_1_C OLOR_1_ERROR	BANK_A_ROI_1_C OLOR_0_ERROR	-	BANK_A_ROI_0_C OLOR_2_ERROR	BANK_A_ROI_0_C OLOR_1_ERROR	BANK_A_ROI_0_C OLOR_0_ERROR
Reset	-	0x0	0x0	0x0	-	0x0	0x0	0x0
Access Type	-	Read Only	Read Only	Read Only	-	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BANK_A_ROI_1_COLOR_2_ERROR	6	Bank A color 0 ROI 1 color 2 errors	0x0: No error detected 0x1: Error detected
BANK_A_ROI_1_COLOR_1_ERROR	5	Bank A color 0 ROI 1 color 1 error	0x0: No error detected 0x1: Error detected
BANK_A_ROI_1_COLOR_0_ERROR	4	Bank A color 0 ROI 1 color 0 error	0x0: No error detected 0x1: Error detected
BANK_A_ROI_0_COLOR_2_ERROR	2	Bank A color 0 ROI 0 color 2 errors	0x0: No error detected 0x1: Error detected
BANK_A_ROI_0_COLOR_1_ERROR	1	Bank A color 0 ROI 0 color 1 error	0x0: No error detected 0x1: Error detected
BANK_A_ROI_0_COLOR_0_ERROR	0	Bank A color 0 ROI 0 color 0 error	0x0: No error detected 0x1: Error detected

BANK A ROI 3 2 ERROR (0x303A)

BIT	7	6	5	4	3	2	1	0
Field	-	BANK_A_ROI_3_C OLOR_2_ERROR	BANK_A_ROI_3_C OLOR_1_ERROR	BANK_A_ROI_3_C OLOR_0_ERROR	-	BANK_A_ROI_2_C OLOR_2_ERROR	BANK_A_ROI_2_C OLOR_1_ERROR	BANK_A_ROI_2_C OLOR_0_ERROR
Reset	-	0x0	0x0	0x0	-	0x0	0x0	0x0
Access Type	-	Read Only	Read Only	Read Only	-	Read Only	Read Only	Read Only

PRELIMINARY

BITFIELD	BITS	DESCRIPTION	DECODE
BANK_A_ROI_3_COLOR_2_ERROR	6	Bank A color 0 ROI 3 color 2 errors	0x0: No error detected 0x1: Error detected
BANK_A_ROI_3_COLOR_1_ERROR	5	Bank A color 0 ROI 3 color 1 error	0x0: No error detected 0x1: Error detected
BANK_A_ROI_3_COLOR_0_ERROR	4	Bank A color 0 ROI 3 color 0 error	0x0: No error detected 0x1: Error detected
BANK_A_ROI_2_COLOR_2_ERROR	2	Bank A color 0 ROI 2 color 2 errors	0x0: No error detected 0x1: Error detected
BANK_A_ROI_2_COLOR_1_ERROR	1	Bank A color 0 ROI 2 color 1 error	0x0: No error detected 0x1: Error detected
BANK_A_ROI_2_COLOR_0_ERROR	0	Bank A color 0 ROI 2 color 0 error	0x0: No error detected 0x1: Error detected

BANK_A_ROI0_XMIN_LSB (0x3040)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_XMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_XMIN_LSB	7:0	Bank A color 0 ROI 0 X Coordinates minimum value LSB

BANK_A_ROI0_XMIN_MSB (0x3041)

BIT	7	6	5	4	3	2	1	0
Field	-	-	BANK_A_ROI0_XMIN_MSB[5:0]					
Reset	-	-	0x0					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_XMIN_MSB	5:0	Bank A color 0 ROI 0 X Coordinates minimum value MSB

BANK_A_ROI0_XMAX_LSB (0x3042)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_XMAX_LSB[7:0]							

Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_XMAX_LSB	7:0	Bank A color 0 ROI 0 X Coordinates maximum value LSB

BANK A ROI0 XMAX MSB (0x3043)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	BANK_A_ROI0_XMAX_MSB[5:0]						
Reset	–	–	0x0						
Access Type	–	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_XMAX_MSB	5:0	Bank A color 0 ROI 0 X Coordinates maximum value MSB

BANK A ROI0 YMIN LSB (0x3044)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_YMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_YMIN_LSB	7:0	Bank A color 0 ROI 0 Y Coordinates minimum value LSB

BANK A ROI0 YMIN MSB (0x3045)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	BANK_A_ROI0_YMIN_MSB[5:0]						
Reset	–	–	0x0						
Access Type	–	–	Write, Read						

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_YMIN_MSB	5:0	Bank A color 0 ROI 0 Y Coordinates minimum value M SB

BANK A ROI0 YMAX LSB (0x3046)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_YMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_YMAX_LSB	7:0	Bank A color 0 ROI 0 Y Coordinates maximum value LSB

BANK A ROI0 YMAX MSB (0x3047)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_A_ROI0_YMAX_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_YMAX_MSB	5:0	Bank A color 0 ROI 0 Y Coordinates maximum value MSB

BANK A ROI0 COLOR SELECT (0x3048)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_A_ROI0_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_SELECT	2:0	Bank A Color 0 ROI 0 Color Set selection bits

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BANK A ROI0 COLOR MIN THR LSB (0x3049)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MIN_THR LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MIN_THR LSB	7:0	Bank A color 0 ROI 0 minimum threshold value LSB

BANK A ROI0 COLOR MIN THR MSB (0x304A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MIN_THR MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MIN_THR MSB	7:0	Bank A color 0 ROI 0 minimum threshold value MSB

BANK A ROI0 COLOR MAX THR LSB (0x304B)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MAX_THR LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MAX_THR LSB	7:0	Bank A color 0 ROI 0 maximum threshold value LSB

BANK A ROI0 COLOR MAX THR MSB (0x304C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MAX_THR MSB[7:0]							

Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MAX_THR_MSB	7:0	Bank A color 0 ROI 0 maximum threshold value MSB

BANK A ROI0 COLOR COUNT LSB (0x304D)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_COUNT_LSB	7:0	Bank A Color 0 ROI 0 detected number of color (LSB)

BANK A ROI0 COLOR COUNT MSB (0x304E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_COUNT_MSB	7:0	Bank A Color 0 ROI 0 detected number of color (MSB)

BANK A ROI0 COLOR SELECT (0x3050)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_A_ROI0_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_SELECT	2:0	Bank A Color 1 ROI 0 Color Set selection bits

BANK A ROI0 COLOR MIN THR LSB (0x3051)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MIN_THR LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MIN_THR LSB	7:0	Bank A color 1 ROI 0 minimum threshold value LSB

BANK A ROI0 COLOR MIN THR MSB (0x3052)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MIN_THR MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MIN_THR MSB	7:0	Bank A color 1 ROI 0 minimum threshold value MSB

BANK A ROI0 COLOR MAX THR LSB (0x3053)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MAX_THR LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MAX_THR LSB	7:0	Bank A color 1 ROI 0 maximum threshold value LSB

BANK A ROI0 COLOR MAX THR MSB (0x3054)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MAX_THR_MSB	7:0	Bank A color 1 ROI 0 maximum threshold value MSB

BANK A ROI0 COLOR COUNT LSB (0x3055)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_COUNT_LSB	7:0	Bank A Color 1 ROI 0 detected number of color (LSB)

BANK A ROI0 COLOR COUNT MSB (0x3056)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_COUNT_MSB	7:0	Bank A Color 1 ROI 0 detected number of color (MSB)

BANK A ROI0 COLOR SELECT (0x3058)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	BANK_A_ROI0_COLOR_SELECT[2:0]		

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Reset	-	-	-	-	-	-	0x0
Access Type	-	-	-	-	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_SELECT	2:0	Bank A Color 2 ROI 0 Color Set selection bits

BANK A ROI0 COLOR MIN THR LSB (0x3059)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MIN_THR LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MIN_THR LSB	7:0	Bank A color 2 ROI 0 minimum threshold value LSB

BANK A ROI0 COLOR MIN THR MSB (0x305A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MIN_THR MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MIN_THR MSB	7:0	Bank A color 2 ROI 0 minimum threshold value MSB

BANK A ROI0 COLOR MAX THR LSB (0x305B)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MAX_THR LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MAX_THR_LSB	7:0	Bank A color 2 ROI 0 maximum threshold value LSB

BANK A ROI0 COLOR MAX THR MSB (0x305C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_MAX_THR_MSB	7:0	Bank A color 2 ROI 0 maximum threshold value MSB

BANK A ROI0 COLOR COUNT LSB (0x305D)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_COUNT LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_COUNT LSB	7:0	Bank A Color 2 ROI 0 detected number of color (LSB)

BANK A ROI0 COLOR COUNT MSB (0x305E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI0_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI0_COLOR_COUNT_MSB	7:0	Bank A Color 2 ROI 0 detected number of color (MSB)

BANK A ROI1 XMIN LSB (0x3060)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_XMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_XMIN_LSB	7:0	Bank A color 0 ROI 1 X Coordinates minimum value LSB

BANK A ROI1 XMIN MSB (0x3061)

BIT	7	6	5	4	3	2	1	0		
Field	–	–	BANK_A_ROI1_XMIN_MSB[5:0]							
Reset	–	–	0x0							
Access Type	–	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_XMIN_MSB	5:0	Bank A color 0 ROI 1 X Coordinates minimum value MSB

BANK A ROI1 XMAX LSB (0x3062)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_XMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_XMAX_LSB	7:0	Bank A color 0 ROI 1 X Coordinates maximum value LSB

BANK A ROI1 XMAX MSB (0x3063)

BIT	7	6	5	4	3	2	1	0		
Field	–	–	BANK_A_ROI1_XMAX_MSB[5:0]							

Reset	-	-	0x0
Access Type	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_XMAX_MSB	5:0	Bank A color 0 ROI 1 X Coordinates maximum value MSB

BANK A ROI1 YMIN LSB (0x3064)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_YMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_YMIN_LSB	7:0	Bank A color 1 ROI 0 Y Coordinates minimum value LSB

BANK A ROI1 YMIN MSB (0x3065)

BIT	7	6	5	4	3	2	1	0
Field	-	-	BANK_A_ROI1_YMIN_MSB[5:0]					
Reset	-	-	0x0					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_YMIN_MSB	5:0	Bank A color 0 ROI 1 Y Coordinates minimum value M SB

BANK A ROI1 YMAX LSB (0x3066)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_YMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_YMAX_LSB	7:0	Bank A color 0 ROI 1 Y Coordinates maximum value LSB

BANK A ROI1 YMAX MSB (0x3067)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_A_ROI1_YMAX_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_YMAX_MSB	5:0	Bank A color 0 ROI 1 Y Coordinates maximum value MSB

BANK A ROI1 COLOR SELECT (0x3068)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_A_ROI1_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_SELECT	2:0	Bank A Color 0 ROI 1 Color Set selection bits

BANK A ROI1 COLOR MIN THR LSB (0x3069)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MIN_THR LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MIN_THR LSB	7:0	Bank A color 0 ROI 0 minimum threshold value LSB

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BANK A ROI1 COLOR MIN THR MSB (0x306A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MIN_THR_MSB	7:0	Bank A color 0 ROI 1 minimum threshold value MSB

BANK A ROI1 COLOR MAX THR LSB (0x306B)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MAX_THR_LSB	7:0	Bank A color 0 ROI 1 maximum threshold value LSB

BANK A ROI1 COLOR MAX THR MSB (0x306C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MAX_THR_MSB	7:0	Bank A color 0 ROI 1maximum threshold value MSB

BANK A ROI1 COLOR COUNT LSB (0x306D)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_COUNT_LSB[7:0]							

Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_COUNT_LSB	7:0	Bank A Color 0 ROI 1 detected number of color (LSB)

BANK A ROI1 COLOR COUNT MSB (0x306E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_COUNT_MSB	7:0	Bank A Color 0 ROI 1 detected number of color (MSB)

BANK A ROI1 COLOR SELECT (0x3070)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_A_ROI1_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_SELECT	2:0	Bank A Color 0 ROI 1 Color Set selection bits

BANK A ROI1 COLOR MIN THR LSB (0x3071)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MIN_THR LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MIN_THR_LSB	7:0	Bank A color 0 ROI 1 minimum threshold value LSB

BANK A ROI1 COLOR MIN THR MSB (0x3072)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MIN_THR_MSB	7:0	Bank A color 0 ROI 1 minimum threshold value MSB

BANK A ROI1 COLOR MAX THR LSB (0x3073)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MAX_THR_LSB	7:0	Bank A color 0 ROI 1 maximum threshold value LSB

BANK A ROI1 COLOR MAX THR MSB (0x3074)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MAX_THR_MSB	7:0	Bank A color 0 ROI 1 maximum threshold value MSB

BANK A ROI1 COLOR COUNT LSB (0x3075)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_COUNT_LSB	7:0	Bank A Color 0 ROI 1 detected number of color (LSB)

BANK A ROI1 COLOR COUNT MSB (0x3076)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_COUNT_MSB	7:0	Bank A Color 0 ROI 1 detected number of color (MSB)

BANK A ROI1 COLOR SELECT (0x3078)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_A_ROI1_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_SELECT	2:0	Bank A Color 2 ROI 1 Color Set selection bits

BANK A ROI1 COLOR MIN THR LSB (0x3079)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MIN_THR LSB[7:0]							

Reset	0x0
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MIN_THR_LSB	7:0	Bank A color 2 ROI 1 minimum threshold value LSB

BANK A ROI1 COLOR MIN THR MSB (0x307A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MIN_THR_MSB	7:0	Bank A color 2 ROI 1 minimum threshold value MSB

BANK A ROI1 COLOR MAX THR LSB (0x307B)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MAX_THR_LSB	7:0	Bank A color 2 ROI 1 maximum threshold value LSB

BANK A ROI1 COLOR MAX THR MSB (0x307C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_MAX_THR_MSB	7:0	Bank A color 2 ROI 1 maximum threshold value MSB

BANK A ROI1 COLOR COUNT LSB (0x307D)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_COUNT_LSB	7:0	Bank A Color 2 ROI 1 detected number of color (LSB)

BANK A ROI1 COLOR COUNT MSB (0x307E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI1_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI1_COLOR_COUNT_MSB	7:0	Bank A Color 2 ROI 1 detected number of color (MSB)

BANK A ROI2 XMIN LSB (0x3080)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_XMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_XMIN_LSB	7:0	Bank A color 0 ROI 2 X Coordinates minimum value LSB

BANK A ROI2 XMIN MSB (0x3081)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_A_ROI2_XMIN_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_XMIN_MSB	5:0	Bank A color 0 ROI 2 X Coordinates minimum value MSB

BANK A ROI2 XMAX LSB (0x3082)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_XMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_XMAX_LSB	7:0	Bank A color 0 ROI 2 X Coordinates maximum value LSB

BANK A ROI2 XMAX MSB (0x3083)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_A_ROI2_XMAX_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_XMAX_MSB	5:0	Bank A color 0 ROI 2 X Coordinates maximum value MSB

BANK A ROI2 YMIN LSB (0x3084)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_YMIN_LSB[7:0]							

Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_YMIN_LSB	7:0	Bank A color 1 ROI 2 Y Coordinates minimum value LSB

BANK A ROI2 YMIN MSB (0x3085)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	BANK_A_ROI2_YMIN_MSB[5:0]						
Reset	–	–	0x0						
Access Type	–	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_YMIN_MSB	5:0	Bank A color 0 ROI 2 Y Coordinates minimum value MSB

BANK A ROI2 YMAX LSB (0x3086)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_YMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_YMAX_LSB	7:0	Bank A color 0 ROI 2 Y Coordinates maximum value LSB

BANK A ROI2 COLOR SELECT (0x3088)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_A_ROI2_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

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BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_SELECT	2:0	Bank A Color 0 ROI 2 Color Set selection bits

BANK A ROI2 COLOR MIN THR LSB (0x3089)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MIN_THR_LSB	7:0	Bank A color 0 ROI 2 minimum threshold value LSB

BANK A ROI2 COLOR MIN THR MSB (0x308A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MIN_THR_MSB	7:0	Bank A color 0 ROI 2 minimum threshold value MSB

BANK A ROI2 COLOR MAX THR LSB (0x308B)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MAX_THR_LSB	7:0	Bank A color 0 ROI 2 maximum threshold value LSB

BANK A ROI2 COLOR MAX THR MSB (0x308C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MAX_THR_MSB	7:0	Bank A color 0 ROI 2 maximum threshold value MSB

BANK A ROI2 COLOR COUNT LSB (0x308D)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_COUNT_LSB	7:0	Bank A Color 0 ROI 2 detected number of color (LSB)

BANK A ROI2 COLOR COUNT MSB (0x308E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_COUNT_MSB	7:0	Bank A Color 0 ROI 2 detected number of color (MSB)

BANK A ROI2 COLOR SELECT (0x3090)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	BANK_A_ROI2_COLOR_SELECT[2:0]		

Reset	-	-	-	-	-	-	0x0
Access Type	-	-	-	-	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_SELECT	2:0	Bank A Color 0 ROI 2 Color Set selection bits

BANK A ROI2 COLOR MIN THR LSB (0x3091)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MIN_THR_LSB	7:0	Bank A color 0 ROI 2 minimum threshold value LSB

BANK A ROI2 COLOR MIN THR MSB (0x3092)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MIN_THR_MSB	7:0	Bank A color 0 ROI 2 minimum threshold value MSB

BANK A ROI2 COLOR MAX THR LSB (0x3093)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MAX_THR_LSB	7:0	Bank A color 0 ROI 2 maximum threshold value LSB

BANK A ROI2 COLOR MAX THR MSB (0x3094)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MAX_THR_MSB	7:0	Bank A color 0 ROI 2 maximum threshold value MSB

BANK A ROI2 COLOR COUNT LSB (0x3095)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_COUNT LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_COUNT LSB	7:0	Bank A Color 0 ROI 2 detected number of color (LSB)

BANK A ROI2 COLOR COUNT MSB (0x3096)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_COUNT_MSB	7:0	Bank A Color 0 ROI 2 detected number of color (MSB)

BANK A ROI2 COLOR SELECT (0x3098)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_A_ROI2_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_SELECT	2:0	Bank A Color 2 ROI 2 Color Set selection bits

BANK A ROI2 COLOR MIN THR LSB (0x3099)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MIN_THR_LSB	7:0	Bank A color 2 ROI 2 minimum threshold value LSB

BANK A ROI2 COLOR MIN THR MSB (0x309A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MIN_THR_MSB	7:0	Bank A color 2 ROI 2 minimum threshold value MSB

BANK A ROI2 COLOR MAX THR LSB (0x309B)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MAX_THR_LSB[7:0]							

Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MAX_THR_LSB	7:0	Bank A color 2 ROI 2 maximum threshold value LSB

BANK A ROI2 COLOR MAX THR MSB (0x309C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_MAX_THR_MSB	7:0	Bank A color 2 ROI 2 maximum threshold value MSB

BANK A ROI2 COLOR COUNT LSB (0x309D)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_COUNT_LSB	7:0	Bank A Color 2 ROI 2 detected number of color (LSB)

BANK A ROI2 COLOR COUNT MSB (0x309E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI2_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
BANK_A_ROI2_COLOR_COUNT_MSB	7:0	Bank A Color 2 ROI 2 detected number of color (MSB)

BANK A ROI3 XMIN LSB (0x30A0)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_XMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_XMIN_LSB	7:0	Bank A color 0 ROI 3 X Coordinates minimum value LSB

BANK A ROI3 XMIN MSB (0x30A1)

BIT	7	6	5	4	3	2	1	0
Field	-	-	BANK_A_ROI3_XMIN_MSB[5:0]					
Reset	-	-	0x0					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_XMIN_MSB	5:0	Bank A color 0 ROI 3 X Coordinates minimum value MSB

BANK A ROI3 XMAX LSB (0x30A2)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_XMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_XMAX_LSB	7:0	Bank A color 0 ROI 3 X Coordinates maximum value LSB

BANK A ROI3 XMAX MSB (0x30A3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_A_ROI3_XMAX_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_XMAX_MSB	5:0	Bank A color 0 ROI 3 X Coordinates maximum value MSB

BANK A ROI3 YMIN LSB (0x30A4)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_YMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_YMIN_LSB	7:0	Bank A color 1 ROI 3 Y Coordinates minimum value LSB

BANK A ROI3 YMIN MSB (0x30A5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_A_ROI3_YMIN_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_YMIN_MSB	5:0	Bank A color 0 ROI 3 Y Coordinates minimum value M SB

BANK A ROI3 YMAX LSB (0x30A6)

BIT	7	6	5	4	3	2	1	0

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Field	BANK_A_ROI3_YMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_YMAX_LSB	7:0	Bank A color 0 ROI 3 Y Coordinates maximum value LSB

BANK_A_ROI3_YMAX_MSB (0x30A7)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	BANK_A_ROI3_YMAX_MSB[5:0]						
Reset	–	–	0x0						
Access Type	–	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_YMAX_MSB	5:0	Bank A color 0 ROI 1 Y Coordinates maximum value MSB

BANK_A_ROI3_COLOR_SELECT (0x30A8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_A_ROI3_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_SELECT	2:0	Bank A Color 0 ROI 3 Color Set selection bits

BANK_A_ROI3_COLOR_MIN_THR_LSB (0x30A9)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							

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Access Type	Write, Read							
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BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MIN_THR_LSB	7:0	Bank A color 0 ROI 3 minimum threshold value LSB

BANK A ROI3 COLOR MIN THR MSB (0x30AA)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MIN_THR_MSB	7:0	Bank A color 0 ROI 3 minimum threshold value MSB

BANK A ROI3 COLOR MAX THR LSB (0x30AB)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MAX_THR_LSB	7:0	Bank A color 0 ROI 3 maximum threshold value LSB

BANK A ROI3 COLOR MAX THR MSB (0x30AC)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MAX_THR_MSB	7:0	Bank A color 0 ROI 3 maximum threshold value MSB

BANK A ROI3 COLOR COUNT LSB (0x30AD)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_COUNT_LSB	7:0	Bank A Color 0 ROI 3 detected number of color (LSB)

BANK A ROI3 COLOR COUNT MSB (0x30AE)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_COUNT_MSB	7:0	Bank A Color 0 ROI 3 detected number of color (MSB)

BANK A ROI3 COLOR SELECT (0x30B0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_A_ROI3_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_SELECT	2:0	Bank A Color 0 ROI 3 Color Set selection bits

BANK A ROI3 COLOR MIN THR LSB (0x30B1)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MIN_THR_LSB	7:0	Bank A color 0 ROI 2 minimum threshold value LSB

BANK A ROI3 COLOR MIN THR MSB (0x30B2)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MIN_THR_MSB	7:0	Bank A color 0 ROI 3 minimum threshold value MSB

BANK A ROI3 COLOR MAX THR LSB (0x30B3)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MAX_THR_LSB	7:0	Bank A color 0 ROI 3 maximum threshold value LSB

BANK A ROI3 COLOR MAX THR MSB (0x30B4)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MAX_THR_MSB[7:0]							

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Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MAX_THR_MSB	7:0	Bank A color 0 ROI 3 maximum threshold value MSB

BANK A ROI3 COLOR COUNT LSB (0x30B5)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_COUNT_LSB	7:0	Bank A Color 0 ROI 3 detected number of color (LSB)

BANK A ROI3 COLOR COUNT MSB (0x30B6)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_COUNT_MSB	7:0	Bank A Color 0 ROI 3 detected number of color (MSB)

BANK A ROI3 COLOR SELECT (0x30B8)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_A_ROI3_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

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BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_SELECT	2:0	Bank A Color 2 ROI 3 Color Set selection bits

BANK A ROI3 COLOR MIN THR LSB (0x30B9)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MIN_THR_LSB	7:0	3Bank A color 2 ROI 2 minimum threshold value LSB

BANK A ROI3 COLOR MIN THR MSB (0x30BA)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MIN_THR_MSB	7:0	Bank A color 2 ROI 3 minimum threshold value MSB

BANK A ROI3 COLOR MAX THR LSB (0x30BB)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MAX_THR_LSB	7:0	Bank A color 2 ROI 3 maximum threshold value LSB

BANK A ROI3 COLOR MAX THR MSB (0x30BC)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_MAX_THR_MSB	7:0	Bank A color 2 ROI 3 maximum threshold value MSB

BANK A ROI3 COLOR COUNT LSB (0x30BD)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_COUNT_LSB	7:0	Bank A Color 2 ROI 3 detected number of color (LSB)

BANK A ROI3 COLOR COUNT MSB (0x30BE)

BIT	7	6	5	4	3	2	1	0
Field	BANK_A_ROI3_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_A_ROI3_COLOR_COUNT_MSB	7:0	Bank A Color 2 ROI 3 detected number of color (MSB)

BANK_B STATUS (0x30C0)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	BANK_B_CALC_DONE	BANK_B_FRAME_COUNT[1:0]	

PRELIMINARY

Reset	-	-	-	-	-	0b0	0x0
Access Type	-	-	-	-	-	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BANK_B_CALC_DONE	2	Telltale detection completion indicator for Bank B	0x0: Not complete 0x1: Complete
BANK_B_FRAME_COUNT	1:0	Frame counter value indicating active frame number for Bank B	

BANK B ROI 1 0 ERROR (0x30C1)

BIT	7	6	5	4	3	2	1	0
Field	-	BANK_B_ROI_1_COLOR_2_ERROR	BANK_B_ROI_1_COLOR_1_ERROR	BANK_B_ROI_1_COLOR_0_ERROR	-	BANK_B_ROI_0_COLOR_2_ERROR	BANK_B_ROI_0_COLOR_1_ERROR	BANK_B_ROI_0_COLOR_0_ERROR
Reset	-	0x0	0x0	0x0	-	0x0	0x0	0x0
Access Type	-	Read Only	Read Only	Read Only	-	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BANK_B_ROI_1_COLOR_2_ERROR	6	Bank B color 0 ROI 1 color 2 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_1_COLOR_1_ERROR	5	Bank B color 0 ROI 1 color 1 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_1_COLOR_0_ERROR	4	Bank B color 0 ROI 1 color 0 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_0_COLOR_2_ERROR	2	Bank B color 0 ROI 0 color 2 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_0_COLOR_1_ERROR	1	Bank B color 0 ROI 0 color 1 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_0_COLOR_0_ERROR	0	Bank B color 0 ROI 0 color 0 error	0x0: No error detected 0x1: Error detected

BANK B ROI 3 2 ERROR (0x30C2)

BIT	7	6	5	4	3	2	1	0
Field	-	BANK_B_ROI_3_COLOR_2_ERROR	BANK_B_ROI_3_COLOR_1_ERROR	BANK_B_ROI_3_COLOR_0_ERROR	-	BANK_B_ROI_2_COLOR_2_ERROR	BANK_B_ROI_2_COLOR_1_ERROR	BANK_B_ROI_2_COLOR_0_ERROR
Reset	-	0x0	0x0	0x0	-	0x0	0x0	0x0

PRELIMINARY

Access Type	-	Read Only	Read Only	Read Only	-	Read Only	Read Only	Read Only
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BITFIELD	BITS	DESCRIPTION	DECODE
BANK_B_ROI_3_COLOR_2_ERROR	6	Bank B color 0 ROI 3 color 2 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_3_COLOR_1_ERROR	5	Bank B color 0 ROI 3 color 1 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_3_COLOR_0_ERROR	4	Bank B color 0 ROI 3 color 0 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_2_COLOR_2_ERROR	2	Bank B color 0 ROI 2 color 2 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_2_COLOR_1_ERROR	1	Bank B color 0 ROI 2 color 1 error	0x0: No error detected 0x1: Error detected
BANK_B_ROI_2_COLOR_0_ERROR	0	Bank B color 0 ROI 2 color 0 error	0x0: No error detected 0x1: Error detected

BANK_B_ROI0_XMIN_LSB (0x30C8)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_XMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_XMIN_LSB	7:0	Bank B color 0 ROI 0 X Coordinates minimum value LSB

BANK_B_ROI0_XMIN_MSB (0x30C9)

BIT	7	6	5	4	3	2	1	0
Field	-	-	BANK_B_ROI0_XMIN_MSB[5:0]					
Reset	-	-	0x0					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_XMIN_MSB	5:0	Bank B color 0 ROI 0 X Coordinates minimum value MSB

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BANK_B_ROI0_XMAX_LSB (0x30CA)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_XMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_XMAX_LSB	7:0	Bank B color 0 ROI 0 X Coordinates maximum value LSB

BANK_B_ROI0_XMAX_MSB (0x30CB)

BIT	7	6	5	4	3	2	1	0		
Field	–	–	BANK_B_ROI0_XMAX_MSB[5:0]							
Reset	–	–	0x0							
Access Type	–	–	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_XMAX_MSB	5:0	Bank B color 0 ROI 0 X Coordinates maximum value MSB

BANK_B_ROI0_YMIN_LSB (0x30CC)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_YMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_YMIN_LSB	7:0	Bank B color 0 ROI 0 Y Coordinates minimum value LSB

BANK_B_ROI0_YMIN_MSB (0x30CD)

BIT	7	6	5	4	3	2	1	0		
Field	–	–	BANK_B_ROI0_YMIN_MSB[5:0]							

Reset	—	—	0x0
Access Type	—	—	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_YMIN_MSB	5:0	Bank B color 0 ROI 0 Y Coordinates minimum value M SB

BANK_B_ROI0_YMAX_LSB (0x30CE)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_YMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_YMAX_LSB	7:0	Bank B color 0 ROI 0 Y Coordinates maximum value LSB

BANK_B_ROI0_YMAX_MSB (0x30CF)

BIT	7	6	5	4	3	2	1	0
Field	—	—	BANK_B_ROI0_YMAX_MSB[5:0]					
Reset	—	—	0x0					
Access Type	—	—	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_YMAX_MSB	5:0	Bank B color 0 ROI 0 Y Coordinates maximum value MSB

BANK_B_ROI0_COLOR_SELECT (0x30D0)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_B_ROI0_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_SELECT	2:0	Bank B Color 0 ROI 0 Color Set selection bits

BANK_B_ROI0_COLOR_MIN_THR_LSB (0x30D1)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MIN_THR_LSB	7:0	Bank B color 0 ROI 0 minimum threshold value LSB

BANK_B_ROI0_COLOR_MIN_THR_MSB (0x30D2)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MIN_THR_MSB	7:0	Bank B color 0 ROI 0 minimum threshold value MSB

BANK_B_ROI0_COLOR_MAX_THR_LSB (0x30D3)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MAX_THR_LSB	7:0	Bank B color 0 ROI 0 maximum threshold value LSB

BANK_B_ROI0_COLOR_MAX_THR_MSB (0x30D4)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MAX_THR_MSB	7:0	Bank B color 0 ROI 0 maximum threshold value MSB

BANK_B_ROI0_COLOR_COUNT_LSB (0x30D5)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_COUNT_LSB	7:0	Bank B Color 0 ROI 0 detected number of color (LSB)

BANK_B_ROI0_COLOR_COUNT_MSB (0x30D6)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_COUNT_MSB	7:0	Bank B Color 0 ROI 0 detected number of color (MSB)

BANK_B_ROI0_COLOR_SELECT (0x30D8)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	BANK_B_ROI0_COLOR_SELECT[2:0]		

PRELIMINARY

Reset	-	-	-	-	-	-	0x0
Access Type	-	-	-	-	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_SELECT	2:0	Bank B Color 1 ROI 0 Color Set selection bits

BANK B ROI0 COLOR MIN THR LSB (0x30D9)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MIN_THR_LSB	7:0	Bank B color 1 ROI 0 minimum threshold value LSB

BANK B ROI0 COLOR MIN THR MSB (0x30DA)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MIN_THR_MSB	7:0	Bank B color 1 ROI 0 minimum threshold value MSB

BANK B ROI0 COLOR MAX THR LSB (0x30DB)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MAX_THR_LSB	7:0	Bank B color 1 ROI 0 maximum threshold value LSB

BANK B ROI0 COLOR MAX THR MSB (0x30DC)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MAX_THR_MSB	7:0	Bank B color 1 ROI 0 maximum threshold value MSB

BANK B ROI0 COLOR COUNT LSB (0x30DD)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_COUNT LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_COUNT LSB	7:0	Bank B Color 1 ROI 0 detected number of color (LSB)

BANK B ROI0 COLOR COUNT MSB (0x30DE)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_COUNT MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_COUNT MSB	7:0	Bank B Color 1 ROI 0 detected number of color (MSB)

BANK_B_ROI0_COLOR_SELECT (0x30E0)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_B_ROI0_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_SELECT	2:0	Bank B Color 2 ROI 0 Color Set selection bits

BANK_B_ROI0_COLOR_MIN_THR_LSB (0x30E1)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MIN_THR_LSB	7:0	Bank B color 2 ROI 0 minimum threshold value LSB

BANK_B_ROI0_COLOR_MIN_THR_MSB (0x30E2)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MIN_THR_MSB	7:0	Bank B color 2 ROI 0 minimum threshold value MSB

BANK_B_ROI0_COLOR_MAX_THR_LSB (0x30E3)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MAX_THR_LSB[7:0]							

PRELIMINARY

Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MAX_THR_LSB	7:0	Bank B color 2 ROI 0 maximum threshold value LSB

BANK B ROI0 COLOR MAX THR MSB (0x30E4)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_MAX_THR_MSB	7:0	Bank B color 2 ROI 0 maximum threshold value MSB

BANK B ROI0 COLOR COUNT LSB (0x30E5)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_COUNT_LSB	7:0	Bank B Color 2 ROI 0 detected number of color (LSB)

BANK B ROI0 COLOR COUNT MSB (0x30E6)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI0_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI0_COLOR_COUNT_MSB	7:0	Bank B Color 2 ROI 0 detected number of color (MSB)

BANK B ROI1 XMIN LSB (0x30E8)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_XMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_XMIN_LSB	7:0	Bank B color 0 ROI 1 X Coordinates minimum value LSB

BANK B ROI1 XMIN MSB (0x30E9)

BIT	7	6	5	4	3	2	1	0
Field	-	-	BANK_B_ROI1_XMIN_MSB[5:0]					
Reset	-	-	0x0					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_XMIN_MSB	5:0	Bank B color 0 ROI 1 X Coordinates minimum value MSB

BANK B ROI1 XMAX LSB (0x30EA)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_XMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_XMAX_LSB	7:0	Bank B color 0 ROI 1 X Coordinates maximum value LSB

BANK_B_ROI1_XMAX_MSB (0x30EB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_B_ROI1_XMAX_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_XMAX_MSB	5:0	Bank B color 0 ROI 1 X Coordinates maximum value MSB

BANK_B_ROI1_YMIN_LSB (0x30EC)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_YMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_YMIN_LSB	7:0	Bank B color 1 ROI 1 Y Coordinates minimum value LSB

BANK_B_ROI1_YMIN_MSB (0x30ED)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_B_ROI1_YMIN_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_YMIN_MSB	5:0	Bank B color 0 ROI 1 Y Coordinates minimum value M SB

BANK_B_ROI1_YMAX_LSB (0x30EE)

BIT	7	6	5	4	3	2	1	0

PRELIMINARY

Field	BANK_B_ROI1_YMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_YMAX_LSB	7:0	Bank B color 0 ROI 1 Y Coordinates maximum value LSB

BANK_B_ROI1_YMAX_MSB (0x30EF)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	BANK_B_ROI1_YMAX_MSB[5:0]						
Reset	–	–	0x0						
Access Type	–	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_YMAX_MSB	5:0	Bank B color 0 ROI 1 Y Coordinates maximum value MSB

BANK_B_ROI1_COLOR_SELECT (0x30F0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_B_ROI1_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_SELECT	2:0	Bank B Color 0 ROI 1 Color Set selection bits

BANK_B_ROI1_COLOR_MIN_THR_LSB (0x30F1)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							

PRELIMINARY

Access Type	Write, Read							
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BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MIN_THR_LSB	7:0	Bank B color 0 ROI 1 minimum threshold value LSB

BANK_B_ROI1_COLOR_MIN_THR_MSB (0x30F2)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MIN_THR_MSB	7:0	Bank B color 0 ROI 1 minimum threshold value MSB

BANK_B_ROI1_COLOR_MAX_THR_LSB (0x30F3)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MAX_THR_LSB	7:0	Bank B color 0 ROI 1 maximum threshold value LSB

BANK_B_ROI1_COLOR_MAX_THR_MSB (0x30F4)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MAX_THR_MSB	7:0	Bank B color 0 ROI 1maximum threshold value MSB

BANK B ROI1 COLOR COUNT LSB (0x30F5)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_COUNT_LSB	7:0	Bank B Color 0 ROI 1 detected number of color (LSB)

BANK B ROI1 COLOR COUNT MSB (0x30F6)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_COUNT_MSB	7:0	Bank B Color 0 ROI 1 detected number of color (MSB)

BANK B ROI1 COLOR SELECT (0x30F8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_B_ROI1_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_SELECT	2:0	Bank B Color 0 ROI 1 Color Set selection bits

BANK_B_ROI1_COLOR_MIN_THR_LSB (0x30F9)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MIN_THR_LSB	7:0	Bank B color 0 ROI 1 minimum threshold value LSB

BANK_B_ROI1_COLOR_MIN_THR_MSB (0x30FA)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MIN_THR_MSB	7:0	Bank B color 0 ROI 1 minimum threshold value MSB

BANK_B_ROI1_COLOR_MAX_THR_LSB (0x30FB)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MAX_THR_LSB	7:0	Bank B color 0 ROI 1 maximum threshold value LSB

BANK_B_ROI1_COLOR_MAX_THR_MSB (0x30FC)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MAX_THR_MSB[7:0]							

PRELIMINARY

Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MAX_THR_MSB	7:0	Bank B color 0 ROI 1 maximum threshold value MSB

BANK B ROI1 COLOR COUNT LSB (0x30FD)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_COUNT_LSB	7:0	Bank B Color 0 ROI 1detected number of color (LSB)

BANK B ROI1 COLOR COUNT MSB (0x30FE)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_COUNT_MSB	7:0	Bank B Color 0 ROI 1 detected number of color (MSB)

BANK B ROI1 COLOR SELECT (0x3100)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_B_ROI1_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_SELECT	2:0	Bank B Color 2 ROI 1 Color Set selection bits

BANK B ROI1 COLOR MIN THR LSB (0x3101)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MIN_THR_LSB	7:0	Bank B color 2 ROI 1 minimum threshold value LSB

BANK B ROI1 COLOR MIN THR MSB (0x3102)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MIN_THR_MSB	7:0	Bank B color 2 ROI 1 minimum threshold value MSB

BANK B ROI1 COLOR MAX THR LSB (0x3103)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MAX_THR_LSB	7:0	Bank B color 2 ROI 1 maximum threshold value LSB

BANK_B_ROI1_COLOR_MAX_THR_MSB (0x3104)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_MAX_THR_MSB	7:0	Bank B color 2 ROI 1 maximum threshold value MSB

BANK_B_ROI1_COLOR_COUNT_LSB (0x3105)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_COUNT_LSB	7:0	Bank B Color 2 ROI 1 detected number of color (LSB)

BANK_B_ROI1_COLOR_COUNT_MSB (0x3106)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI1_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI1_COLOR_COUNT_MSB	7:0	Bank B Color 2 ROI 1 detected number of color (MSB)

BANK_B_ROI2_XMIN_LSB (0x3108)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_XMIN_LSB[7:0]							

Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_XMIN_LSB	7:0	Bank B color 0 ROI 2 X Coordinates minimum value LSB

BANK_B_ROI2_XMIN_MSB (0x3109)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	BANK_B_ROI2_XMIN_MSB[5:0]						
Reset	–	–	0x0						
Access Type	–	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_XMIN_MSB	5:0	Bank B color 0 ROI 2 X Coordinates minimum value MSB

BANK_B_ROI2_XMAX_LSB (0x310A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_XMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_XMAX_LSB	7:0	Bank B color 0 ROI 2 X Coordinates maximum value LSB

BANK_B_ROI2_XMAX_MSB (0x310B)

BIT	7	6	5	4	3	2	1	0	
Field	–	–	BANK_B_ROI2_XMAX_MSB[5:0]						
Reset	–	–	0x0						
Access Type	–	–	Write, Read						

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_XMAX_MSB	5:0	Bank B color 0 ROI 2 X Coordinates maximum value MSB

BANK B ROI2 YMIN LSB (0x310C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_YMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_YMIN_LSB	7:0	Bank B color 1 ROI 2 Y Coordinates minimum value LSB

BANK B ROI2 YMIN MSB (0x310D)

BIT	7	6	5	4	3	2	1	0
Field	-	-	BANK_B_ROI2_YMIN_MSB[5:0]					
Reset	-	-	0x0					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_YMIN_MSB	5:0	Bank B color 0 ROI 2 Y Coordinates minimum value M SB

BANK B ROI2 YMAX LSB (0x310E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_YMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_YMAX_LSB	7:0	Bank B color 0 ROI 2 Y Coordinates maximum value LSB

BANK_B_ROI2_YMAX_MSB (0x310F)

BIT	7	6	5	4	3	2	1	0
Field	—	—	BANK_B_ROI2_YMAX_MSB[5:0]					
Reset	—	—	0x0					
Access Type	—	—	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_YMAX_MSB	5:0	Bank B color 0 ROI 2 Y Coordinates maximum value MSB

BANK_B_ROI2_COLOR_SELECT (0x3110)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_B_ROI2_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_SELECT	2:0	Bank BColor 0 ROI 2 Color Set selection bits

BANK_B_ROI2_COLOR_MIN_THR_LSB (0x3111)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MIN_THR_LSB	7:0	Bank B color 0 ROI 2 minimum threshold value LSB

BANK_B_ROI2_COLOR_MIN_THR_MSB (0x3112)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MIN_THR_MSB[7:0]							

PRELIMINARY

Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MIN_THR_MSB	7:0	Bank B color 0 ROI 2 minimum threshold value MSB

BANK B ROI2 COLOR MAX THR LSB (0x3113)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MAX_THR_LSB	7:0	Bank B color 0 ROI 2 maximum threshold value LSB

BANK B ROI2 COLOR MAX THR MSB (0x3114)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MAX_THR_MSB	7:0	Bank B color 0 ROI 2 maximum threshold value MSB

BANK B ROI2 COLOR COUNT LSB (0x3115)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_COUNT_LSB	7:0	Bank B Color 0 ROI 2 detected number of color (LSB)

BANK B ROI2 COLOR COUNT MSB (0x3116)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_COUNT_MSB	7:0	Bank B Color 0 ROI 2 detected number of color (MSB)

BANK B ROI2 COLOR SELECT (0x3118)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	BANK_B_ROI2_COLOR_SELECT[2:0]		
Reset	-	-	-	-	-	0x0		
Access Type	-	-	-	-	-	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_SELECT	2:0	Bank B Color 0 ROI 2 Color Set selection bits

BANK B ROI2 COLOR MIN THR LSB (0x3119)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MIN_THR LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MIN_THR LSB	7:0	Bank B color 0 ROI 2 minimum threshold value LSB

BANK_B_ROI2_COLOR_MIN_THR_MSB (0x311A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MIN_THR_MSB	7:0	Bank B color 0 ROI 2 minimum threshold value MSB

BANK_B_ROI2_COLOR_MAX_THR_LSB (0x311B)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MAX_THR_LSB	7:0	Bank B color 0 ROI 2 maximum threshold value LSB

BANK_B_ROI2_COLOR_MAX_THR_MSB (0x311C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MAX_THR_MSB	7:0	Bank B color 0 ROI 2 maximum threshold value MSB

BANK_B_ROI2_COLOR_COUNT_LSB (0x311D)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_COUNT_LSB[7:0]							

Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_COUNT_LSB	7:0	Bank B Color 0 ROI 2 detected number of color (LSB)

BANK B ROI2 COLOR COUNT MSB (0x311E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_COUNT_MSB	7:0	Bank B Color 0 ROI 2 detected number of color (MSB)

BANK B ROI2 COLOR SELECT (0x3120)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_B_ROI2_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_SELECT	2:0	Bank B Color 2 ROI 2 Color Set selection bits

BANK B ROI2 COLOR MIN THR LSB (0x3121)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MIN_THR LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MIN_THR_LSB	7:0	Bank B color 2 ROI 2 minimum threshold value LSB

BANK B ROI2 COLOR MIN THR MSB (0x3122)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MIN_THR_MSB	7:0	Bank B color 2 ROI 2 minimum threshold value MSB

BANK B ROI2 COLOR MAX THR LSB (0x3123)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MAX_THR_LSB	7:0	Bank B color 2 ROI 2 maximum threshold value LSB

BANK B ROI2 COLOR MAX THR MSB (0x3124)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_MAX_THR_MSB	7:0	Bank B color 2 ROI 2 maximum threshold value MSB

BANK_B_ROI2_COLOR_COUNT_LSB (0x3125)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_COUNT_LSB	7:0	Bank B Color 2 ROI 2 detected number of color (LSB)

BANK_B_ROI2_COLOR_COUNT_MSB (0x3126)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI2_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI2_COLOR_COUNT_MSB	7:0	Bank B Color 2 ROI 2 detected number of color (MSB)

BANK_B_ROI3_XMIN_LSB (0x3128)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_XMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_XMIN_LSB	7:0	Bank B color 0 ROI 3 X Coordinates minimum value LSB

BANK_B_ROI3_XMIN_MSB (0x3129)

BIT	7	6	5	4	3	2	1	0
Field	-	-	BANK_B_ROI3_XMIN_MSB[5:0]					

Reset	-	-	0x0
Access Type	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_XMIN_MSB	5:0	Bank B color 0 ROI 3 X Coordinates minimum value MSB

BANK B ROI3 XMAX LSB (0x312A)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_XMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_XMAX_LSB	7:0	Bank B color 0 ROI 3 X Coordinates maximum value LSB

BANK B ROI3 XMAX MSB (0x312B)

BIT	7	6	5	4	3	2	1	0
Field	-	-	BANK_B_ROI3_XMAX_MSB[5:0]					
Reset	-	-	0x0					
Access Type	-	-	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_XMAX_MSB	5:0	Bank B color 0 ROI 3 X Coordinates maximum value MSB

BANK B ROI3 YMIN LSB (0x312C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_YMIN_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_YMIN_LSB	7:0	Bank B color 1 ROI 3 Y Coordinates minimum value LSB

BANK_B_ROI3_YMIN_MSB (0x312D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_B_ROI3_YMIN_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_YMIN_MSB	5:0	Bank B color 0 ROI 3 Y Coordinates minimum value MSB

BANK_B_ROI3_YMAX_LSB (0x312E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_YMAX_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_YMAX_LSB	7:0	Bank B color 0 ROI 3 Y Coordinates maximum value LSB

BANK_B_ROI3_YMAX_MSB (0x312F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BANK_B_ROI3_YMAX_MSB[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_YMAX_MSB	5:0	Bank B color 0 ROI 1 Y Coordinates maximum value MSB

PRELIMINARY

BANK_B_ROI3_COLOR_SELECT (0x3130)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	BANK_B_ROI3_COLOR_SELECT[2:0]		
Reset	—	—	—	—	—	0x0		
Access Type	—	—	—	—	—	Write, Read		

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_SELECT	2:0	Bank B Color 0 ROI 3 Color Set selection bits

BANK_B_ROI3_COLOR_MIN_THR_LSB (0x3131)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_MIN_THR_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MIN_THR_LSB	7:0	Bank B color 0 ROI 3 minimum threshold value LSB

BANK_B_ROI3_COLOR_MIN_THR_MSB (0x3132)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_MIN_THR_MSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MIN_THR_MSB	7:0	Bank B color 0 ROI 3 minimum threshold value MSB

BANK_B_ROI3_COLOR_MAX_THR_LSB (0x3133)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_MAX_THR_LSB[7:0]							

PRELIMINARY

Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MAX_THR_LSB	7:0	Bank B color 0 ROI 3 maximum threshold value LSB

BANK B ROI3 COLOR MAX THR MSB (0x3134)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MAX_THR_MSB	7:0	Bank B color 0 ROI 3 maximum threshold value MSB

BANK B ROI3 COLOR COUNT LSB (0x3135)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_COUNT_LSB	7:0	Bank B Color 0 ROI 3 detected number of color (LSB)

BANK B ROI3 COLOR COUNT MSB (0x3136)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_COUNT_MSB	7:0	Bank B Color 0 ROI 3 detected number of color (MSB)

BANK B ROI3 COLOR SELECT (0x3138)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BANK_B_ROI3_COLOR_SELECT[2:0]		
Reset	–	–	–	–	–			0x0
Access Type	–	–	–	–	–			Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_SELECT	2:0	Bank B Color 0 ROI 3 Color Set selection bits

BANK B ROI3 COLOR MIN THR LSB (0x3139)

BIT	7	6	5	4	3	2	1	0
Field					BANK_B_ROI3_COLOR_MIN_THR_LSB[7:0]			
Reset						0x0		
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MIN_THR_LSB	7:0	Bank B color 0 ROI 2 minimum threshold value LSB

BANK B ROI3 COLOR MIN THR MSB (0x313A)

BIT	7	6	5	4	3	2	1	0
Field					BANK_B_ROI3_COLOR_MIN_THR_MSB[7:0]			
Reset						0x0		
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MIN_THR_MSB	7:0	Bank B color 0 ROI 3 minimum threshold value MSB

BANK_B_ROI3_COLOR_MAX_THR_LSB (0x313B)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MAX_THR_LSB	7:0	Bank B color 0 ROI 3 maximum threshold value LSB

BANK_B_ROI3_COLOR_MAX_THR_MSB (0x313C)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MAX_THR_MSB	7:0	Bank B color 0 ROI 3 maximum threshold value MSB

BANK_B_ROI3_COLOR_COUNT_LSB (0x313D)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_COUNT_LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_COUNT_LSB	7:0	Bank B Color 0 ROI 3 detected number of color (LSB)

BANK_B_ROI3_COLOR_COUNT_MSB (0x313E)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_COUNT_MSB[7:0]							

Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_COUNT_MSB	7:0	Bank B Color 0 ROI 3 detected number of color (MSB)

BANK B ROI3 COLOR SELECT (0x3140)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BANK_B_ROI3_COLOR_SELECT[2:0]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_SELECT	2:0	Bank B Color 2 ROI 3 Color Set selection bits

BANK B ROI3 COLOR MIN THR LSB (0x3141)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BANK_B_ROI3_COLOR_MIN_THR_LSB[7:0]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MIN_THR_LSB	7:0	Bank B color 2 ROI 2 minimum threshold value LSB

BANK B ROI3 COLOR MIN THR MSB (0x3142)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BANK_B_ROI3_COLOR_MIN_THR_MSB[7:0]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

PRELIMINARY

PRELIMINARY

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MIN_THR_MSB	7:0	Bank B color 2 ROI 3 minimum threshold value MSB

BANK B ROI3 COLOR MAX THR LSB (0x3143)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_MAX_THR_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MAX_THR_LSB	7:0	Bank B color 2 ROI 3 maximum threshold value LSB

BANK B ROI3 COLOR MAX THR MSB (0x3144)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_MAX_THR_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_MAX_THR_MSB	7:0	Bank B color 2 ROI 3 maximum threshold value MSB

BANK B ROI3 COLOR COUNT LSB (0x3145)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_COUNT LSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_COUNT LSB	7:0	Bank B Color 2 ROI 3 detected number of color (LSB)

BANK_B_ROI3_COLOR_COUNT_MSB (0x3146)

BIT	7	6	5	4	3	2	1	0
Field	BANK_B_ROI3_COLOR_COUNT_MSB[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BANK_B_ROI3_COLOR_COUNT_MSB	7:0	Bank B Color 2 ROI 3 detected number of color (MSB)

DEC_PPS0_3_B0 (0x4520)

DSC Decoder PPS 0-3 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	dsc_version_major[3:0]				dsc_version_minor[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
dsc_version_major	7:4	DSC Version Major
dsc_version_minor	3:0	DSC Version Minor

DEC_PPS0_3_B1 (0x4521)

DSC Decoder PPS 0-3 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	pps_identifier[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pps_identifier	7:0	PPS Identifier

PRELIMINARY

DEC PPS0_3_B2 (0x4522)

DSC Decoder PPS 0-3 Register Byte 2

DEC PPS0_3_B3 (0x4523)

DSC Decoder PPS0-3 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	bits_per_component[3:0]				linebuf_depth[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
bits_per_component	7:4	Bits per component 0x0 = 16 bpc (allowed only when dsc_version_minor = 0x2). 0x8 = 8 bpc. 0xA = 10 bpc. 0xC = 12 bpc. 0xE = 14 bpc (allowed only when dsc_version_minor = 0x2).
linebuf_depth	3:0	Line Buffer Depth

DEC PPS4_7_B0 (0x4524)

DSC Decoder Core PPS4-7 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	—	—	block_pred_enable	convert_rgb	simple_422	vbr_enable	bits_per_pixel_h[1:0]	
Reset	—	—	0b0	0b0	0b0	0b0	0b00	
Access Type	—	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
block_pred_enable	5	Block Prediction Enable
convert_rgb	4	Convert RGB
simple_422	3	Simple 422
vbr_enable	2	VBR Enable mode
bits_per_pixel_h	1:0	Higher bits of bits_per_pixel [9:8]

PRELIMINARY

DEC PPS4_7_B1 (0x4525)

DSC Decoder Core PPS4-7 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	bits_per_pixel_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
bits_per_pixel_l	7:0	Lower bits of bits_per_pixel [7:0]

DEC PPS4_7_B2 (0x4526)

DSC Decoder PPS4-7 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	pic_height_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pic_height_h	7:0	Picture Height (vertical active) High Byte [15:8]

DEC PPS4_7_B3 (0x4527)

DSC Decoder PPS4-7 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	pic_height_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pic_height_l	7:0	Picture Height (vertical active) Low Byte [7:0]

PRELIMINARY

DEC PPS8_11_B0 (0x4528)

DSC Decoder PPS8-11 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	pic_width_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pic_width_h	7:0	Picture Width (horizontal active) High Byte [15:8]

DEC PPS8_11_B1 (0x4529)

DSC Decoder PPS8-11 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	pic_width_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pic_width_l	7:0	Picture Width (horizontal active) Low Byte [7:0]

DEC PPS8_11_B2 (0x452A)

DSC Decoder PPS8-11 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	slice_height_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_height_h	7:0	Slice Height High Byte [15:8]

PRELIMINARY

DEC PPS8_11_B3 (0x452B)

DSC Decoder PPS8-11 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	slice_height_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_height_l	7:0	Slice Height Low Byte [7:0]

DEC PPS12_15_B0 (0x452C)

DSC Decoder PPS12-15 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	slice_width_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_width_h	7:0	Slice Width High Byte [15:8]

DEC PPS12_15_B1 (0x452D)

DSC Decoder PPS12-15 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	slice_width_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_width_l	7:0	Slice Width Low Byte [7:0]

PRELIMINARY

DEC PPS12_15_B2 (0x452E)

DSC Decoder PPS12-15 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	chunk_size_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
chunk_size_h	7:0	Chunk Size High Byte [15:8]

DEC PPS12_15_B3 (0x452F)

DSC Decoder PPS12-15 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	chunk_size_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
chunk_size_l	7:0	Chunk Size Low Byte [7:0]

DEC PPS16_19_B0 (0x4530)

DSC Decoder PPS16_19 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	initial_xmit_delay_h[1:0]	
Reset	—	—	—	—	—	—	0b00	
Access Type	—	—	—	—	—	—	Write, Read	

BITFIELD	BITS	DESCRIPTION
initial_xmit_delay_h	1:0	Initial Encoder Transmit Delay High Bits [9:8].

PRELIMINARY

DEC PPS16_19_B1 (0x4531)

DSC Decoder PPS16_19 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	initial_xmit_delay_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
initial_xmit_delay_l	7:0	Initial Encoder Transmit Delay High Byte [9:8]

DEC PPS16_19_B2 (0x4532)

DSC Decoder PPS16_19 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	initial_dec_delay_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
initial_dec_delay_h	7:0	Initial Decoder Delay High Byte [15:8]

DEC PPS16_19_B3 (0x4533)

DSC Decoder PPS16_19 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	initial_dec_delay_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
initial_dec_delay_l	7:0	Initial Decoder Delay High Byte [15:8]

PRELIMINARY

DEC PPS20_23_B1 (0x4535)

DSC Decoder PPS20-23 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	initial_scale_value[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
initial_scale_value	5:0	Initial Scale Value

DEC PPS20_23_B2 (0x4536)

DSC Decoder PPS20-23 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	scale_increment_interval_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
scale_increment_interval_h	7:0	Scale Increment Interval High Byte [15:8]

DEC PPS20_23_B3 (0x4537)

DSC Decoder PPS20-23 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	scale_increment_interval_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
scale_increment_interval_l	7:0	Scale Increment Interval Low Byte [7:0]

PRELIMINARY

DEC PPS24_27_B0 (0x4538)

DSC Decoder PPS24-27 Register Byte 0

BIT	7	6	5	4	3	2	1	0		
Field	–	–	–	–	scale_decrement_interval_h[3:0]					
Reset	–	–	–	–	0x0					
Access Type	–	–	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
scale_decrement_interval_h	3:0	Scale Decrement Interval High Bits [11:8]

DEC PPS24_27_B1 (0x4539)

DSC Decoder PPS24-27 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	scale_decrement_interval_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
scale_decrement_interval_l	7:0	Scale Decrement Interval Low Byte [7:0]

DEC PPS24_27_B3 (0x453B)

DSC Decoder PPS24-27 Register Byte 3

BIT	7	6	5	4	3	2	1	0	
Field	–	–	–	first_line_bpg_offset[4:0]					
Reset	–	–	–	0b00000					
Access Type	–	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
first_line_bpg_offset	4:0	First Line Band Gap Offset

PRELIMINARY

DEC PPS28_31_B0 (0x453C)

DSC Decoder PPS28-31 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	nfl_bpg_offset_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
nfl_bpg_offset_h	7:0	NFL BPG Offset High Byte

DEC PPS28_31_B1 (0x453D)

DSC Decoder PPS28-31 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	nfl_bpg_offset_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
nfl_bpg_offset_l	7:0	NFL BPG Offset Low Byte

DEC PPS28_31_B2 (0x453E)

DSC Decoder PPS28-31 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	slice_bpg_offset_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_bpg_offset_h	7:0	Slice BPG Offset High Byte [15:8]

PRELIMINARY

DEC PPS28_31_B3 (0x453F)

DSC Decoder PPS28-31 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	slice_bpg_offset_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_bpg_offset_l	7:0	Slice BPG Offset Low Byte [7:0]

DEC PPS32_35_B0 (0x4540)

DSC Decoder PPS32-35 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	initial_offset_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
initial_offset_h	7:0	Initial Offset High Byte [15:8]

DEC PPS32_35_B1 (0x4541)

DSC Decoder PPS 32-35 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	initial_offset_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
initial_offset_l	7:0	Initial Offset Low Byte [7:0]

PRELIMINARY

DEC PPS32_35_B2 (0x4542)

DSC Decoder PPS 32-35 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	final_offset_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
final_offset_h	7:0	Final Offset High Byte [15:0]

DEC PPS32_35_B3 (0x4543)

DSC Decoder PPS 32-35 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	final_offset_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
final_offset_l	7:0	Final Offset Low Byte [7:0]

DEC PPS36_39_B0 (0x4544)

DSC Decoder PPS 36-39 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	flatness_min_qp[4:0]				
Reset	—	—	—	0b00000				
Access Type	—	—	—	Write, Read				

BITFIELD	BITS	DESCRIPTION
flatness_min_qp	4:0	Flatness Minimum QP

PRELIMINARY

DEC PPS36_39_B1 (0x4545)

DSC Decoder PPS 36-39 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	flatness_max_qp[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
flatness_max_qp	4:0	Flatness Maximum QP

DEC PPS36_39_B2 (0x4546)

DSC Decoder PPS 36-39 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	rc_model_size_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_model_size_h	7:0	RC Model Size High Byte [15:8]

DEC PPS36_39_B3 (0x4547)

DSC Decoder PPS 36-39 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	rc_model_size_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_model_size_l	7:0	RC Model Size Low Byte [7:0]

PRELIMINARY

DEC PPS40_43_B0 (0x4548)

DSC Decoder PPS40-43 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	rc_edge_factor[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
rc_edge_factor	3:0	RC Edge Factor

DEC PPS40_43_B1 (0x4549)

DSC Decoder PPS40-43 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	rc_quant_incr_limit0[4:0]			
Reset	–	–	–	–	0b00000			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
rc_quant_incr_limit0	4:0	RC Quant Incremental Limit 0

DEC PPS40_43_B2 (0x454A)

DSC Decoder PPS40-43 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	rc_quant_incr_limit1[4:0]			
Reset	–	–	–	–	0b00000			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
rc_quant_incr_limit1	4:0	RC Quant Incremental Limit 1

PRELIMINARY

DEC_PPS40_43_B3 (0x454B)

DSC Decoder PPS40-43 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	rc_tgt_offset_hi[3:0]						rc_tgt_offset_lo[3:0]	
Reset	0x0						0x0	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
rc_tgt_offset_hi	7:4	RC Target Offset High
rc_tgt_offset_lo	3:0	RC Target Offset Low

DEC_PPS44_47_B0 (0x454C)

DSC Decoder PPS44-47 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	rc_buff_thresh0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buff_thresh0	7:0	RC Buffer Threshold 0

DEC_PPS44_47_B1 (0x454D)

DSC Decoder PPS44-47 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh1	7:0	RC Buffer Threshold 1

PRELIMINARY

DEC PPS44_47_B2 (0x454E)

DSC Decoder PPS44-47 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh2	7:0	RC Buffer Threshold 2

DEC PPS44_47_B3 (0x454F)

DSC Decoder PPS44-47 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh3	7:0	RC Buffer Threshold 3

DEC PPS48_51_B0 (0x4550)

DSC Decoder PPS48-51 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh4	7:0	RC Buffer Threshold 4

PRELIMINARY

DEC PPS48 51 B1 (0x4551)

DSC Decoder PPS48-51 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh5	7:0	RC Buffer Threshold 5

DEC PPS48 51 B2 (0x4552)

DSC Decoder PPS48-51 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh6	7:0	RC Buffer Threshold 6

DEC PPS48 51 B3 (0x4553)

DSC Decoder PPS48-51 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh7	7:0	RC Buffer Threshold 7

PRELIMINARY

DEC PPS52_55_B0 (0x4554)

DSC Decoder PPS52-55 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh8	7:0	RC Buffer Threshold 8

DEC PPS52_55_B1 (0x4555)

DSC Decoder PPS52-55 Register byte 1

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh9	7:0	RC Buffer Threshold 9

DEC PPS52_55_B2 (0x4556)

DSC Decoder PPS52-55 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh10	7:0	RC Buffer Threshold 10

PRELIMINARY

DEC PPS52_55_B3 (0x4557)

DSC Decoder PPS52-55 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh11	7:0	RC Buffer Threshold 11

DEC PPS56_59_B0 (0x4558)

DSC Decoder PPS56-59 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh12	7:0	RC Buffer Threshold 12

DEC PPS56_59_B1 (0x4559)

DSC Decoder PPS56-59 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	rc_buf_thresh13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
rc_buf_thresh13	7:0	RC Buffer Threshold 13

PRELIMINARY

DEC PPS56_59_B2 (0x455A)

DSC Decoder PPS56-59 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp0[4:0]						range_max_qp0_h[2:0]	
Reset	0b000						0b00000	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
range_min_qp0	7:3	Range Minimum QP0
range_max_qp0_h	2:0	Range Maximum QP0 High Bits [4:2]

DEC PPS56_59_B3 (0x455B)

DSC Decoder PPS56-59 Register Byte 3

BIT	7	6	5	4	3	2	1	0	
Field	range_max_qp0_l[1:0]			range_bpg_offset0[5:0]					
Reset	0b000000			0b00					
Access Type	Write, Read			Write, Read					

BITFIELD	BITS	DESCRIPTION
range_max_qp0_l	7:6	Range Maximum QP0 Low Bits [1:0]
range_bpg_offset0	5:0	Range BPG Offset 0

DEC PPS60_63_B0 (0x455C)

DSC Decoder PPS60-63 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp1[4:0]						range_max_qp1_h[2:0]	
Reset	0b000						0b00000	
Access Type	Write, Read						Write, Read	

PRELIMINARY

DEC_PPS60_63_B1 (0x455D)

DSC Decoder PPS60-63 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp1_l[1:0]				range_bpg_offset1[5:0]			
Reset	0b00				0b000000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
range_max_qp1_l	7:6	Range Maximum Low Bits [1:0]
range_bpg_offset1	5:0	Range BPG Offset 1

DEC_PPS60_63_B2 (0x455E)

DSC Decoder PPS60-63 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp2[4:0]						range_max_qp2_h[2:0]	
Reset	0b00000						0b000	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
range_min_qp2	7:3	Range Minimum QP2
range_max_qp2_h	2:0	Range Maximum QP2 High Bits [4:2]

DEC_PPS60_63_B3 (0x455F)

DSC Decoder PPS60-63 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp2_l[1:0]						range_bpg_offset2[5:0]	

Reset	0b00	0b000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
range_max_qp2_l	7:6	Range Maximum QP2 Low Bits [1:0]
range_bpg_offset2	5:0	Range BPG Offset 2

DEC PPS64_67_B0 (0x4560)

DSC Decoder PPS64-67 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp3[4:0]							range_max_qp3_h[2:0]
Reset	0b00000							0b00
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
range_min_qp3	7:3	Range Minimum QP3
range_max_qp3_h	2:0	Range Maximum QP3 Low Bits [1:0]

DEC PPS64_67_B1 (0x4561)

DSC Decoder PPS64-67 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp3_l[1:0]							range_bpg_offset3[5:0]
Reset	0b00							0b000000
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
range_max_qp3_l	7:6	Range Maximum QP3 Low Bits [1:0]
range_bpg_offset3	5:0	Range BPG Offset 3

DEC PPS64_67_B2 (0x4562)

DSC Decoder PPS64-67 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp4[4:0]						range_max_qp4_h[2:0]	
Reset	0b00000						0b000	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
range_min_qp4	7:3	Range Minimum QP4
range_max_qp4_h	2:0	Range Maximum QP4 High Bits [4:2]

DEC PPS64 67 B3 (0x4563)

DSC Decoder PPS64-67 Register Byte 3

BIT	7	6	5	4	3	2	1	0	
Field	range_max_qp4_l[1:0]			range_bpg_offset4[5:0]					
Reset	0b00			0b000000					
Access Type	Write, Read			Write, Read					

BITFIELD	BITS	DESCRIPTION
range_max_qp4_l	7:6	Range Maximum QP4 Low Bits [1:0]
range_bpg_offset4	5:0	Range BPG Offset 4

DEC PPS68 71 B0 (0x4564)

DSC Decoder PPS68-71 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp5[4:0]						range_max_qp5_h[2:0]	
Reset	0b00000						0b000	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
range_min_qp5	7:3	Range Minimum QP5
range_max_qp5_h	2:0	Range Maximum QP5 High Bits [4:2]

DEC PPS68 71 B1 (0x4565)

DSC Decoder PPS68-71 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp5_l[1:0]						range_bpg_offset5[5:0]	
Reset	0b0000						0b000000	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
range_max_qp5_l	7:6	Range Maximum QP5 Low Bits [1:0]
range_bpg_offset5	5:0	Range BPG Offset 5

DEC PPS68 71 B2 (0x4566)

DSC Decoder PPS68-71 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp6[4:0]						range_max_qp6_h[2:0]	
Reset	0b00000						0b000	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
range_min_qp6	7:3	Range Minimum QP6
range_max_qp6_h	2:0	Range Maximum QP6 High Bits [4:2]

DEC PPS68 71 B3 (0x4567)

DSC Decoder PPS68-71 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp6_l[1:0]						range_bpg_offset6[5:0]	
Reset	0b00						0b000000	
Access Type	Write, Read						Write, Read	

PRELIMINARY

DEC PPS72 75 B0 (0x4568)

DSC Decoder PPS72-75 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field				range_min_qp7[4:0]				range_max_qp7_h[2:0]
Reset				0b00000				0b000
Access Type				Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION
range_min_qp7	7:3	Range Minimum QP7
range_max_qp7_h	2:0	Range Maximum QP7 High Bits [4:2]

DEC PPS72 75 B1 (0x4569)

DSC Decoder PPS72-75 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field			range_max_qp7_l[1:0]			range_bpg_offset7[5:0]		
Reset			0b000			0b000000		
Access Type			Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
range_max_qp7_l	7:6	Range Maximum QP7 Low Bits [1:0]
range_bpg_offset7	5:0	Range BPG Offset 7

DEC PPS72 75 B2 (0x456A)

DSC Decoder PPS72-75 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field				range_min_qp8[4:0]				range_max_qp8_h[2:0]

Reset	0b00000	0b000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
range_min_qp8	7:3	Range Minimum QP8
range_max_qp8_h	2:0	Range Maximum QP8 High Bits [4:2]

DEC PPS72 75 B3 (0x456B)

DSC Decoder PPS72-75 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp8_l[1:0]							range_bpg_offset8[5:0]
Reset	0b00							0b000000
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
range_max_qp8_l	7:6	Range Maximum QP8 Low Bits [1:0]
range_bpg_offset8	5:0	Rang BPG Offset 8

DEC PPS76 79 B0 (0x456C)

DSC Decoder PPS76-79 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp9[4:0]							range_max_qp9_h[2:0]
Reset	0b00000							0b000
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
range_min_qp9	7:3	Range Minimum QP9
range_max_qp9_h	2:0	Range Maximum QP9 High Bits [4:2]

DEC PPS76 79 B1 (0x456D)

DSC Decoder PPS76-79 Register Byte 1

PRELIMINARY

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp9_l[1:0]		range_bpg_offset9[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
range_max_qp9_l	7:6	Range Maximum QP9 Low Bits [1:0]
range_bpg_offset9	5:0	Range BPG Offset 9

DEC PPS76 79 B2 (0x456E)

DSC Decoder PPS76-79 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp10[4:0]						range_max_qp10_h[2:0]	
Reset	0b00000						0b000	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
range_min_qp10	7:3	Range Minimum QP10
range_max_qp10_h	2:0	Range Maximum QP10 High Bits[4:2]

DEC PPS76 79 B3 (0x456F)

DSC Decoder PPS76-79 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp10_l[1:0]		range_bpg_offset10[5:0]					
Reset	0b000		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
range_max_qp10_l	7:6	Range Maximum QP10 Low Bits [1:0]
range_bpg_offset10	5:0	Range BPG Offset 10

DEC_PPS80_83_B0 (0x4570)

DSC Decoder PPS80-83 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp11[4:0]						range_max_qp11_h[2:0]	
Reset	0b00000						0b000	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION
range_min_qp11	7:3	Range Minimum QP11
range_max_qp11_h	2:0	Range Maximum QP11 High Bit [4:2]

DEC_PPS80_83_B1 (0x4571)

DSC Decoder PPS80-83 Register Byte 1

BIT	7	6	5	4	3	2	1	0	
Field	range_max_qp11_l[1:0]			range_bpg_offset11[5:0]					
Reset	0b00			0b000000					
Access Type	Write, Read			Write, Read					

BITFIELD	BITS	DESCRIPTION
range_max_qp11_l	7:6	Range Maximum QP11 Low Bits [1:0]
range_bpg_offset11	5:0	Range BPG Offset 11

DEC_PPS80_83_B2 (0x4572)

DSC Decoder PPS80-83 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp12[4:0]						range_max_qp12_h[2:0]	
Reset	0b00000						0b000	
Access Type	Write, Read						Write, Read	

PRELIMINARY

DEC PPS80_83_B3 (0x4573)

DSC Decoder PPS80-83 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp12_l[1:0]				range_bpg_offset12[5:0]			
Reset	0b000				0b000000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
range_max_qp12_l	7:6	Range Maximum Qp12 Low Bits[1:0]
range_bpg_offset12	5:0	Range BPG Offset 12

DEC PPS84_87_B0 (0x4574)

DSC Decoder PPS84_87 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp13[4:0]				range_max_qp13_h[2:0]			
Reset	0b00000				0b000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
range_min_qp13	7:3	Range Minimum QP13
range_max_qp13_h	2:0	Range Maximum QP13 High Bits [4:2]

DEC PPS84_87_B1 (0x4575)

DSC Decoder PPS84_87 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp13_l[1:0]			range_bpg_offset13[5:0]				

Reset	0b00	0b000000
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
range_max_qp13_l	7:6	Range Maximum QP13 Low Bits [1:0]
range_bpg_offset13	5:0	Range BPG Offset 13

DEC PPS84_87_B2 (0x4576)

DSC Decoder PPS84_87 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field	range_min_qp14[4:0]							range_max_qp14_h[2:0]
Reset	0b00000							0b000
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
range_min_qp14	7:3	Range Minimum QP14
range_max_qp14_h	2:0	Range Maximum QP14 High Bits [4:2]

DEC PPS84_87_B3 (0x4577)

DSC Decoder PPS84_87 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	range_max_qp14_l[1:0]							range_bpg_offset14[5:0]
Reset	0b00							0b000000
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
range_max_qp14_l	7:6	Range Maximum QP14 Low Bits [1:0]
range_bpg_offset14	5:0	Range BPG Offset 14

DEC PPS88_91_B0 (0x4578)

DSC Decoder PPS88-91 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	native_420	native_422
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
native_420	1	Native 420
native_422	0	Native 422

DEC PPS88_91_B1 (0x4579)

DSC Decoder PPS88-91 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	–		second_line_bpg_offset[4:0]			
Reset	–	–	–		0b00000			
Access Type	–	–	–			Write, Read		

BITFIELD	BITS	DESCRIPTION
second_line_bpg_offset	4:0	Second Line BPG Offset

DEC PPS88_91_B2 (0x457A)

DSC Decoder PPS88-91 Register Byte 2

BIT	7	6	5	4	3	2	1	0
Field				nsl_bpg_offset_h[7:0]				
Reset				0x00				
Access Type					Write, Read			

BITFIELD	BITS	DESCRIPTION
nsl_bpg_offset_h	7:0	NSL BPG Offset High Byte [15:8]

DEC PPS88_91_B3 (0x457B)

DSC Decoder PPS88-91 Register Byte 3

BIT	7	6	5	4	3	2	1	0
Field	nsl_bpg_offset_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
nsl_bpg_offset_l	7:0	NSL BPG Offset Low Byte [7:0]

DEC PPS92_95_B0 (0x457C)

DSC Decoder PPS92-95 Register Byte 0

BIT	7	6	5	4	3	2	1	0
Field	second_line_offset_adj_h[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
second_line_offset_adj_h	7:0	Second Line Offset Adjustment High Byte [15:8]

DEC PPS92_95_B1 (0x457D)

DSC Decoder PPS92-95 Register Byte 1

BIT	7	6	5	4	3	2	1	0
Field	second_line_offset_adj_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
second_line_offset_adj_l	7:0	Second Line Offset Adjustment Low Byte [7:0]

PRELIMINARY

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
-	03/23	Absolute Maximum Ratings: CAP_VDD updated, DCIO_rating added, DIS_Rem_CC added to the XRES, X2 line, and added AUXP/N ratings of (-0.3V to VDD18 + 0.3V) Package Information: added Thermal Resistance information EC Characteristics table: Output Voltage Swing (Single Ended); RL to be changed to 50Ω to 100Ω, SGMII RX and TX Lanes; VOD: Changed from 300mV to 500mV; VOS: TBD to change to 600mV, PWDNB INPUT; added PWDNB Hold Time of 1ms, DIS_Rem_CC; added Input Capacitance of 3pF Typ, Reference Clock Requirements; VIH min from 0.92V to 0.9V, SGMII RX and TX LANES; updated max value to ±100ppm, changed units from pSec to ps; Input Jitter Tolerance min from 450ps to 480ps, Data Valid Acknowledge Time: Corrected units from Ms to us. Added I2C / UART PORT TIMING section; SCLK Output Pulse Width High/Low: changed min from tMCK/2 – 3 to tMCK/2-3.4; SPI Subordinate; MISO Data Output Delay:changed min of -1.5ns to +2.0ns; AC Characteristics/ I2S /TDM MASTER TIMING; Added condition CL= 5pF for All Parameters; Added DP HPD AC Characteristics Pin Descriptions: GPIO 19: Added Up Default information, VDD: remove Internal 1.0V regulator function Added sections to Detailed Descriptions: eDP Output, Power Supplies, Thermal Management	—
-	5/23	Removed MAX96764RS part number from datasheet Front Page: Updated Benefits and Features for more clarification EC Table: Added Typical specifications for Power Supply Current Deserializer Operating Modes: Added note regarding Serializer Capabilities Pin Configuration & Typical Applications Circuit: Removed part number from diagrams Ordering Information table: Removed MAX96764 part number	—

PRELIMINARY

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