Click here to ask an associate for production status of specific part numbers.

MAX96781/MAX96783 GMSL2/1 Serializer with eDP1.4a/DP1.4 Input and Optional HDCP

General Description

The MAX96781/MAX96783 serializers convert 1 or 2 stream DP1.4/eDP1.4a input to single or dual GMSL2 or GMSL1 links. They also send and receive control-channel and peripheral-control data, enabling transmission of video and bidirectional data over a single cable.

The MAX96781/MAX96783 accept 1 or 2 video streams in DP MST mode or 1 video stream in DP/eDP SST mode. The 2-lane DP interface supports up to 360MHz total PCLK at HBR2 data rate or 430MHz at HBR3 data rate. RGB888 format is supported.

Each GMSL2 link operates at a fixed rate of 3Gbps or 6Gbps in the forward direction and 187.5Mbps in reverse for a maximum total 12Gbps forward and 375Mbps reverse (in dual-link mode). Both GMSL links are backward compatible with ADI's GMSL1 technology with forward-link rates from 500Mbps to 3.12Gbps and 1Mbps reverse.

The MAX96783 provides HDCP 1.4 encryption capability for each GMSL link.

A concurrent I^{2}C/UART control channel is provided. Using the control channel, an ECU can program the serializer, deserializers, and peripheral devices. Two additional pass-through I^{2}C/UART channels, two forward I^{2}S/TDM audio channels, and an SPI channel are also provided.

Data can be transmitted over low-cost 50Ω coax or 100Ω STP cables that meet the GMSL2 channel specification.

Table 1. Typical Maximum Cable Length

	3.2mm Ø 50Ω Coax, Foam Dielectric	2.7mm Ø 50Ω Coax, Solid Dielectric	100Ω Shielded Twisted Pair, AWG26
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, +105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL2 Fwd/Rev Data Rate	**Typical Maximum Cable Length at +105ºC**		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m

Contact the factory to receive the GMSL2 Channel Specification document.

Applications

- Medium- to High-Resolution Automotive Displays

Benefits and Features

- DP1.4 and eDP1.4a Input Interface
  - Two DP/eDP Lanes
  - Supports SST and 2-Stream MST Modes
  - Supports HBR, HBR2, and HBR3 DP Data Rates
- Multiple GMSL2 Data Rates for System and Power Flexibility
  - 3Gbps or 6Gbps Forward, 187.5Mbps Reverse
  - 12Gbps/375Mbps in Dual-Link Mode
- GMSL1 Backwards Compatible on Each GMSL Link
  - 500Mbps to 3.12Gbps Forward, 1Mbps Reverse
- Ideal for High-Resolution Video Applications
  - Up to 215MHz on Each Link
  - Up to 430MHz with Dual Link
- Uses Low-Cost 50Ω Coax or 100Ω STP Cables
- HDCP 1.4 Encryption on GMSL Links (MAX96783)
- Two Forward I^{2}S/TDM Audio Channels
- GMSL Line-Fault Monitor
- ASIL-Relevant GMSL2 Functional Safety Features
  - ASIL-B Compliant GMSL2 Mode
  - 16-bit CRC Protection of Control-Channel Data (I^{2}C, UART, SPI, GPIO, Audio)
  - Optional 32-Bit Video Line CRC
  - Retransmission of All Control-Channel Data (I^{2}C, UART, SPI, GPIO, Audio) Upon Error Detection
  - Video Watermark Generation and Detection
- Performance Tools Ensure High Link Margin
  - Continuous Adaptive Equalization on GMSL Links
  - Forward and Reverse Channel PRBS Generator and Checker for BER Testing of Serial I/O Links
- Concurrent Control Channel for Device Configuration and Communicating with Remote Peripherals
  - Main I^{2}C/UART, Two Pass-Through I^{2}C/UART, SPI, and Tunneled or Register-Programmable GPIO
  - Up To 19 Programmable GPIOs
  - Four Hardware-Programmable Device Addresses
  - Sleep Mode with Register State Retention
- Operation Specified Over -40°C to +105°C Automotive Temperature Range
- AEC-Q100 Qualified
- 8x8mm 56-TQFN Package with Exposed Pad

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Ordering Information appears at end of datasheet.

19-101559; Rev A

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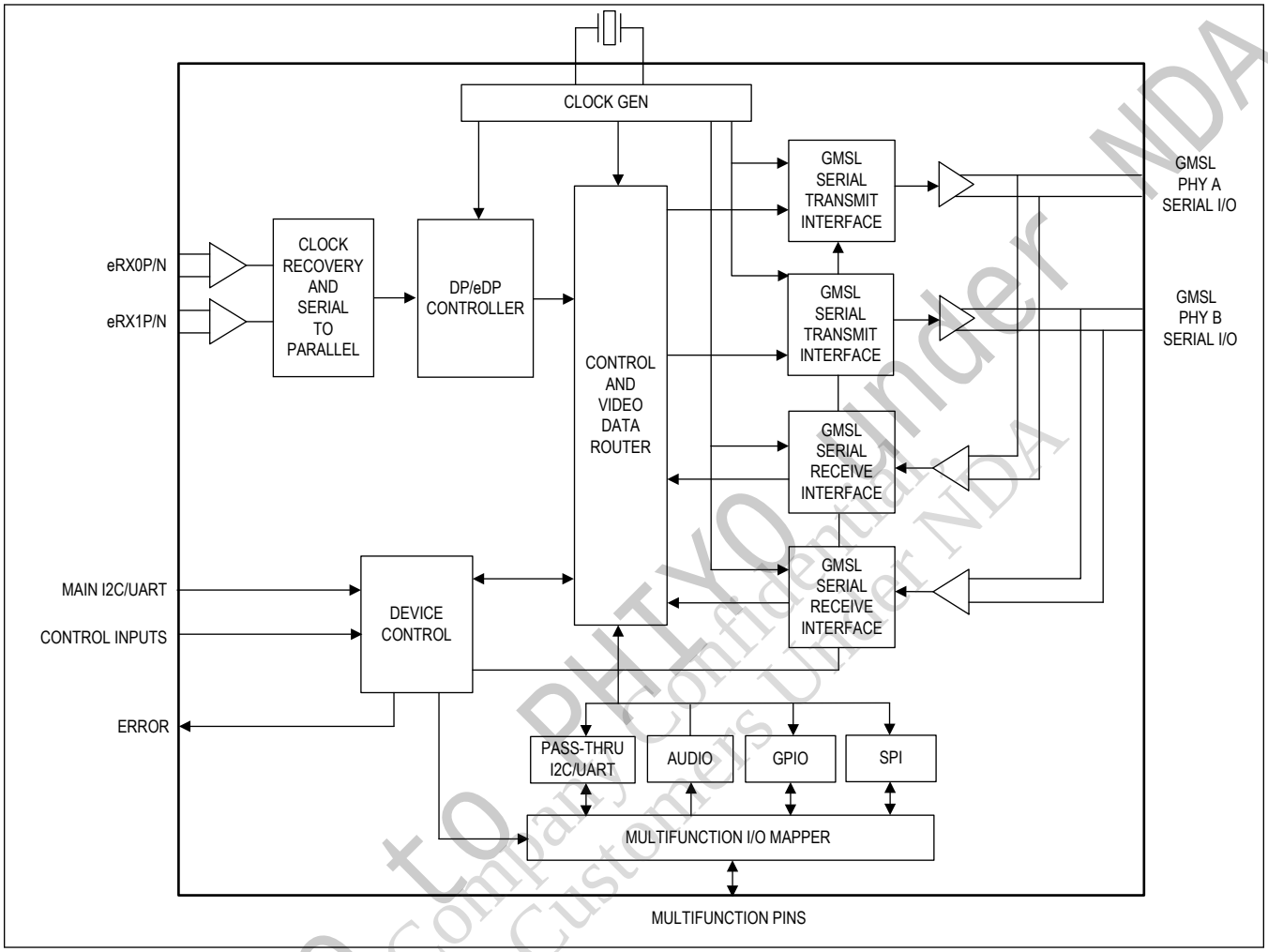
Simplified Block Diagram



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Absolute Maximum Ratings

(All voltages with respect to ground.) .....
V_{DDIO} ..... −0.3V to +3.9V
V_{DD18}, V_{DD18_eDP}..... −0.3V to +2.0V
V_{DD}, CAP_VDD..... −0.3V to +1.1V
SIO_ pins (Active State) (*Note a*) ..... (V_{DD18} - 1.1V) to V_{DD18}
SIO_ pins (Inactive State) (*Note a*) ..... -0.3V to +1.1V
eRX_, AUXP/N ..... -0.3V to (V_{DD18_eDP} + 0.3)V
XRES, X2, DIS_REM_CC.....-0.3V to (V_{DD18} + 0.3)V
All Other Pins (*Note b*).....−0.3V to (V_{DDIO} + 0.3V)V
Continuous Power Dissipation (T_A = +70ºC) TQFN (Multilayer board, derate 40mW/ºC above +70ºC) 2200mW
Storage Temperature Range .....-40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note a: Active state means the device is powered up and not in sleep or power-down mode. Inactive means the device is not powered up, or is powered up in sleep or power-down mode.

Note b: Specified maximum voltage or 3.9V, whichever is lower.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56TQFN-EP

Package Code	T5688+6C
Outline Number	**21-0135**
Land Pattern Number	**90-100041**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

SW-56TQFN-EP

Package Code	T5688Y+6C
Outline Number	**21-100046**
Land Pattern Number	**90-100048**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

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Electrical Characteristics

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD CHANNEL SERIAL OUTPUTS (SIO_)—SEE Figure 1						
Output Voltage Swing (Single-Ended)	V_O	R_L = 100Ω ±1%, (V_{OH}-V_{OL}) for both outputs	300	400	500	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, peak-to-peak differential voltage	600	800	1000	mVp-p
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)} - V_{OD(L)} \rvert$			25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state	V_{DD18} − 0.65	V_{DD18} − 0.45	V_{DD18} − 0.25	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)} \rvert$			25	mV
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}	50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / GMSL1 FORWARD CHANNEL SERIAL OUTPUTS (SIO_)—SEE Figure 1						
Output Voltage Swing (Single-Ended)	V_O	R_L = 100Ω ±1%, coax mode	375	500	625	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, STP mode	600	800	1000	mVp-p
Output Offset Voltage (Single-Ended)	V_{OS}	R_L = 100Ω ±1%, Coax mode	V_{DD18} - 0.75	V_{DD18} - 0.55	V_{DD18} - 0.35	V
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, STP mode	V_{DD18} - 0.65	V_{DD18} - 0.45	V_{DD18} - 0.25	V
Change in V_{OD} Between Complimentary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)} - V_{OD(L)} \rvert$, STP Mode			25	mV
Change in V_{OS} Between Complimentary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)} \rvert$, STP mode			25	mV
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}	50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / GMSL1 REVERSE CONTROL CHANNEL RECEIVER (SIO_)						
High Switching Threshold	V_{CHR}	HIM disabled			27	mV
		HIM enabled			40	
Low Switching Threshold	V_{CLR}	HIM disabled	-27			mV
		HIM enabled	-40			
DC ELECTRICAL CHARACTERISTICS / DP INPUTS (eRX__)						
Input Common-Mode Voltage	V_{CM_eRX}			0.5		V
Input Termination Resistance	R_I	Differential Measurement	90	100	110	Ω

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Electrical Characteristics (continued)

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / DP AUX CHANNEL							
Differential Peak-to-Peak Output Voltage	V_{OD}	V_{DD} = 1.0V, R_L = 100Ω ± 1%	Amplitude Setting 0		200		mV
			Amplitude Setting 1		400		
			Amplitude Setting 2		600		
			Amplitude Setting 3		800		
			Amplitude Setting 4		1000		
			Amplitude Setting 5		1200		
			Amplitude Setting 6		1380		
Input Peak-to-Peak Voltage	V_{ID}			140		1360	mV
Input Common-Mode Voltage	V_{CMI}				800		mV
Termination Resistance	R_I	Differential Measurement			105		Ω
DC ELECTRICAL CHARACTERISTICS / DP HPD							
HPD Driven Voltage	V_{OH_HPD}	Driven HPD Voltage, I_{OH_HPD} = -4mA		V_{DDIO} - 0.4			V
DC ELECTRICAL CHARACTERISTICS / I/O PINS							
High-Level Input Voltage	V_{IH}			0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA		V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA				0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}				1	µA
Input Capacitance	C_{IN}				3		pF
Internal Pullup/Pulldown Resistance	R_{IN}	40kΩ enabled			40		kΩ
		1MΩ enabled			1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS							
High-Level Input Voltage	V_{IH}			0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{DDIO}	V
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA				0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}				1	µA
Input Capacitance	C_{IN}				3		pF
Internal Pullup Resistance	R_{PU}	40kΩ enabled			40		kΩ
		1MΩ enabled			1		MΩ

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Electrical Characteristics (continued)

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Input Capacitance	C_{IN}			3		pF
Internal Pulldown Resistance	R_{PD}			1		MΩ
DC ELECTRICAL CHARACTERISTICS / DIS_REM_CC INPUT						
High-Level Input Voltage	V_{IH}		1.6			V
Low-Level Input Voltage	V_{IL}				1.4	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DD18}			30	µA
Input Capacitance	C_{IN}			3		pF
Internal Pulldown Resistance	R_{PD}			100		kΩ
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / LINE-FAULT DETECTION INPUTS (LMN_)						
Open Pin Voltage	V_{O0}	LMN0 or LMN2		1.25		V
	V_{O1}	LMN1 or LMN3		0.75		
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (CRYSTAL) (X1/OSC, X2)						
X1 Input Capacitance	C_{IN_X1}			3		pF
X2 Input Capacitance	C_{IN_X2}			1		pF
Internal X2 Limit Resistor	R_{LIM}			1.2		kΩ
Internal Feedback Resistor	R_{FB}			10		kΩ
Transconductance	g_m			28		mA/V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED)						
High-Level Input Voltage	V_{IH}		0.9			V
Low-Level Input Voltage	V_{IL}				0.4	V
Input Impedance	R_{IN}			10		kΩ
X1 Input Capacitance	C_{IN_X1}			3		pF

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Electrical Characteristics (continued)

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY (GMSL2 MODE)							
Supply Current	I_{DD}	2-lane HBR2 2-MST input, 2 6Gbps links each with 1920x1080, 148.5MHz PCLK	V_{DD18}		280	340	mA
			V_{DD}		250	740	
		2-lane HBR3 2-MST input, 2 6Gbps links, each with 2560x1080, 198MHz PCLK	V_{DD18}		280	340	
			V_{DD}		275	770	
Maximum V_{DDIO} Supply Current	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} at 1.9V		44		µA/MHz
			V_{DDIO} at 3.6V		81		
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY (GMSL1 MODE)							
Supply Current	I_{DD}	2-lane HBR2 2-MST input, 2x GMSL1 links, each with 1920x720, 95MHz PCLK, HIBW mode	V_{DD18}		215	260	mA
			V_{DD}		140	560	
Maximum V_{DDIO} Supply Current	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} at 1.9V		44		µA/MHz
			V_{DDIO} at 3.6V		81		
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENTS							
Maximum Power-Down Current	I_{DD}	V_{DDIO} at 3.6V	T_A = +25ºC		6		µA
			T_A = +105ºC		7		
		V_{DD18} at 1.9V	T_A = +25ºC		1		
			T_A = +105ºC		15		
		V_{DD} at 1.05V	T_A = +25ºC		<1		
			T_A = +105ºC		<1		
DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENTS							
Maximum Sleep Current	I_{DD}	V_{DDIO} at 3.6V	T_A = +25ºC		9		µA
			T_A = +105ºC		10		
		V_{DD18} at 1.9V	T_A = +25ºC		30		
			T_A = +105ºC		45		
		V_{DD} at 1.05V	T_A = +25ºC		< 1		
			T_A = +105ºC		< 1		
AC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD CHANNEL SWITCHING CHARACTERISTICS (SIO_)							
Serial Output Rise Time	t_R	20% to 80%, V_O = 400mV, R_L = 100Ω ±1%			50		ps
Serial Output Fall Time	t_F	80% to 20%, V_O = 400mV, R_L = 100Ω ±1%			50		ps
Total Serial Output Jitter	t_{TSOJ}	PRBS7, single-ended or differential output			0.15		UI (p-p)

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Electrical Characteristics (continued)

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Deterministic Serial Output Jitter	t_{DSOJ}	PRBS7, single-ended or differential output		0.10		UI (p-p)
Lock Time	t_{LOCK}	(*Note 6*, *Note 10*)		50	70	ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from video applied to input to when the first video packet appears at GMSL2 outputs, assuming link is already established. t_{FRM}=VS period Figure 2		6.05 x t_{FRM}		s
Maximum Video Latency	t_{VL}	Time from DisplayPort input to SIO_ output in GMSL2 packet. t_{PCLK}=pixel clock period Figure 3		5000 x t_{PCLK}		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip.		1		ms
AC ELECTRICAL CHARACTERISTICS / GMSL1 FORWARD CHANNEL SERIAL OUTPUTS (SIO_)						
Serial Output RiseTime	t_R	20% to 80%, R_L = 100Ω ±1%		50		ps
Serial Ouput Fall Time	t_F	80% to 20%, R_L = 100Ω ±1%		50		ps
Total Serial Output Jitter	t_{TSOJ1}	PRBS7, single-ended or differential output		0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	PRBS7, single-ended or differential output		0.15		UI
Maximum Link Startup Time	t_{LOCK}	Measured from when the DP Source starts sending video on the DP Link (after link training is complete) to when the deserializer asserts its LOCK pin. t_{FRM}=VS period See Figure 4		9 x t_{FRM}		s
Maximum Video Latency	t_{VL}	Time from high-speed signal received at input until it appears on GMSL1 output during active video. t_{PCLK}=pixel clock period See Figure 5		5000 x t_{PCLK}		s
AC ELECTRICAL CHARACTERISTICS / DP INPUTS (eRX__) (*Note 2*, *Note 3*)						
Supported Link Rates	f_{eDP}	Per Lane, HBR3		8.1		Gbps
		Per Lane, HBR2		5.4		Gbps
		Per Lane, HBR		2.7		Gbps
Unit Interval	UI_Rate	HBR3		123		ps
		HBR2		185.2		ps
	UI_Rate	HBR		370.4		ps
Unit Interval Tolerance	UI_TOL		-300		+300	ppm
CDR Tracking Bandwidth	$f_{CDR_Track_BW}$	HBR3		>15		MHz
		HBR2		>10		MHz
		HBR		>10		MHz

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Electrical Characteristics (continued)

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Jitter Tolerance	T_J	Jitter Frequency 5MHz	HBR3	0.77			UI
			HBR2	0.69			
			HBR	0.673			
SSC Downspread				0		0.5	%
SSC Modulation Rate				30		33	kHz
AC Coupling Capacitor	C_{AC}				150		nF
AC ELECTRICAL CHARACTERISTICS / DP AUX CHANNEL (*Note 2*)							
Unit Interval	UI			0.4		0.6	µs
Cycle-to-Cycle Jitter	t_{JCC}	UI Variation Within a Single Transaction				0.08	UI
		UI Variation Between Adjacent Bits				0.04	
AC ELECTRICAL CHARACTERISTICS / DP HPD							
HPD_IRQ Pulse Width				0.5		1	ms
IRQ_HPD Minimum Spacing				2			ms
AC ELECTRICAL CHARACTERISTICS / I²C/UART PORT TIMING							
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO} (*Note 2*)		20 x V_{DDIO} / 5.5V		150	ns
I²C/UART Wake Time	t_{CC_WAKE}	From power-up or rising edge of PWDNB to local I²C/UART access available. For remote register access, I²C/UART wake time is the same as lock time (t_{LOCK}). See Figure 7. (*Note 2*, *Note 7*, *Note 10*)				4	ms
AC ELECTRICAL CHARACTERISTICS / I²C TIMING—SEE Figure 6							
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I²C MST_BT = 010, I²C SLV_SH = 10)		9.6		100	kHz
		Mid f_{SCL} range: (I²C MST_BT = 101, I²C SLV_SH = 01)		100		400	
		High f_{SCL} range: (I²C MST_BT = 111, I²C SLV_SH = 00)		400		1000	
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low		4			µs
		f_{SCL} range, mid		0.6			
		f_{SCL} range, high		0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low		4.7			µs
		f_{SCL} range, mid		1.3			
		f_{SCL} range, high		0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low		4			µs
		f_{SCL} range, mid		0.6			
		f_{SCL} range, high		0.26			

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Electrical Characteristics (continued)

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load On Each Bus Line	C_B	(*Note 2*)			100	pF
AC ELECTRICAL CHARACTERISTICS / SPI MASTER—SEE Figure 8 (*Note 4*)						
Operating Frequency	f_{MCK}	(*Note 2*)	0.588		25	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	C_L = 5pF (*Note 2*)	$t_{MCK}/2$ - 3.4	$t_{MCK}/2$		ns
MOSI Data Output Delay	t_{MOD}	After SCLK falling edge (*Note 2*)	-2.3		2.3	ns
MISO Input Setup Time	t_{MIS}	Before programmed sampling edge (*Note 2*)	13.5			ns
MISO Input Hold Time	t_{MIH}	After programmed sampling edge, (*Note 2*)	-2			ns
AC ELECTRICAL CHARACTERISTICS / SPI SLAVE—SEE Figure 9 (*Note 4*)						
Operating Frequency	f_{SCK}	(*Note 2*)			25	MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns

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Electrical Characteristics (continued)

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MISO Data Output Delay	t_{SOD}	After SCLK falling edge (Note 2)	2.0		11.3	ns
MOSI Input Setup Time	t_{SIS}	Before SCLK rising edge (Note 2)	5			ns
MOSI Input Hold Time	t_{SIH}	After SCLK rising edge (Note 2)	3			ns
AC ELECTRICAL CHARACTERISTICS / I²S/TDM SLAVE TIMING—SEE Figure 10 (Note 2)						
WS Frequency	f_{WS}		8		192	kHz
Sample Word Length	n_{WS}		8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$	0.512		49.152	MHz
SD, WS Setup Time	t_{SAS}		4			ns
SD, WS Hold Time	t_{SAH}		4			ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1/OSC, X2) (Note 2)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1/OSC, X2 UNCONNECTED) (Note 2)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
Input Jitter	t_J	Sinusoidal jitter < 1MHz (falling edge), downstream deserializer using crystal reference (Note 8)			150	ps (p-p)
Input Duty Cycle	t_{DUTY}		40		60	%
Input Fall Time	t_F	80% to 20%			4	ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK OUTPUT (RCLKOUT)						
Frequency	f_{REFOUT}	Crystal or reference clock input; f_{REF} / 1		25		MHz
		Crystal or reference clock input; f_{REF} / 2		12.5		MHz
		Crystal or reference clock input; f_{REF} / 4		6.25		MHz
Rise Time	t_R	20% to 80%, C_L = 10pF, 25MHz divided by 1, 2, or 4, (Note 2, Note 5)			4	ns
Fall Time	t_F	80% to 20%, C_L = 10pF, 25MHz divided by 1, 2, or 4 (Note 2, Note 5)			4	ns
Jitter	t_J	C_L = 10pF, rising or falling edge, f_{REFOUT} = 25MHz (Note 9)		260		ps (p-p)

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Electrical Characteristics (continued)

(V_{DD} = 0.95V to 1.05V, V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD} = 1.0V, V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION						
SIO__	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±8		kV
		ISO10605, R_D = 330Ω, C_S = 150pF, contact discharge, coax configuration		±6		kV
		ISO10605, R_D = 330Ω, C_S = 150pF, contact discharge, STP configuration		±6		kV
		ISO10605, R_D = 330Ω, C_S = 150pF, air discharge		±8		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Note 1: Limits are 100% tested at T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: In compliance with DisplayPort 1.4 CTS.

Note 4: MFP pin speed configured based on V_{DDIO}:
IO_EDGE_RATE = 00 for V_{DDIO} < 2.25V
IO_EDGE_RATE = 01 for V_{DDIO} ≥ 2.25V
See Table 20 for details regarding output speed programming.

Note 5: MFP pin speed configured based on V_{DDIO}:
IO_EDGE_RATE = 01 for V_{DDIO} < 3V
IO_EDGE_RATE = 10 for V_{DDIO} ≥ 3V
See Table 20 for details regarding output speed programming.

Note 6: From power-up, release of RESET_LINK, or rising edge of the PWDNB pin, to rising edge of the LOCK pin. t_{RD} must be <90ms. For more information, see the *GMSL2 Link Lock* section.

Note 7: The system controller must not initiate any communication prior to the specified wakeup time having elapsed.

Note 8: Reference clock source used during characterization included 30ps RMS (1σ) random jitter in addition to the specified sinusoidal jitter.

Note 9: Random jitter is dominant; deterministic jitter is negligible.

Note 10: Production tested using ECS ECS-250-18-33Q-DS crystal.

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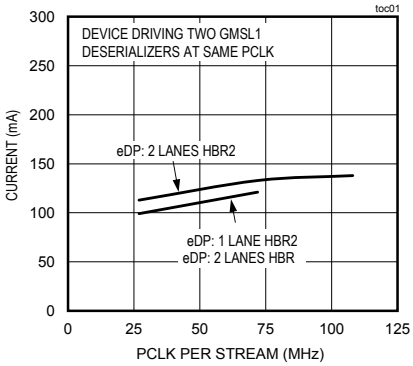
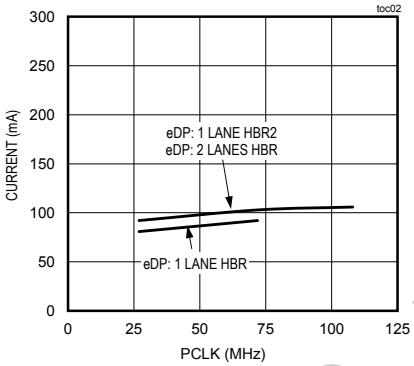
Typical Operating Characteristics

(V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, two PHY characteristics assume 2xMST video where the streams have identical timing, unless otherwise noted.)

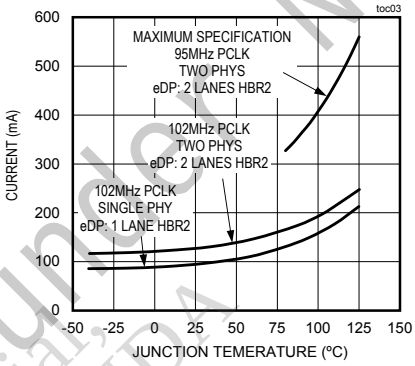
V_{DD} CURRENT TWO GMSL1 PHYS



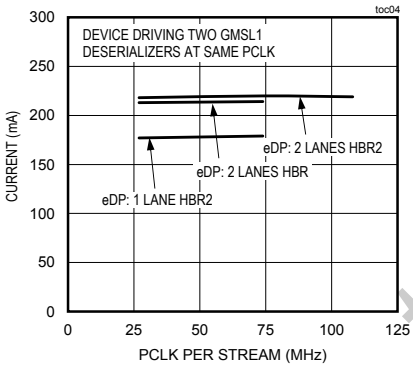
V_{DD} CURRENT SINGLE GMSL1 PHY



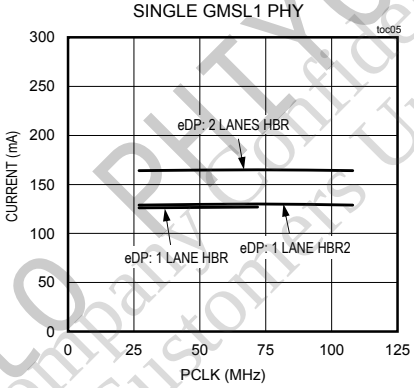
V_{DD} CURRENT vs. TEMPERATURE GMSL1



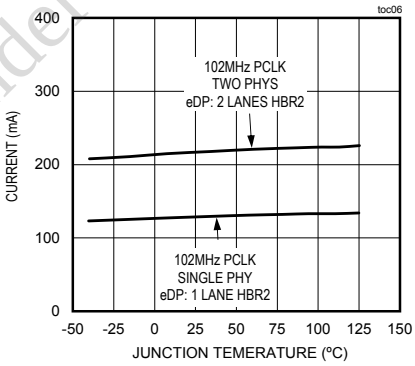
V_{DD18} CURRENT TWO GMSL1 PHYS



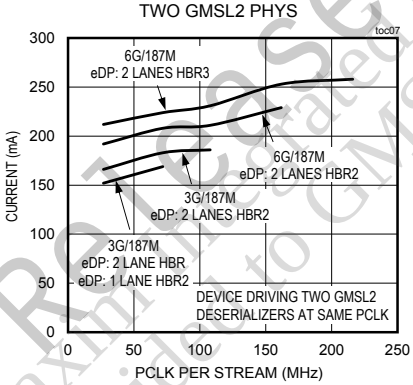
V_{DD18} CURRENT SINGLE GMSL1 PHY



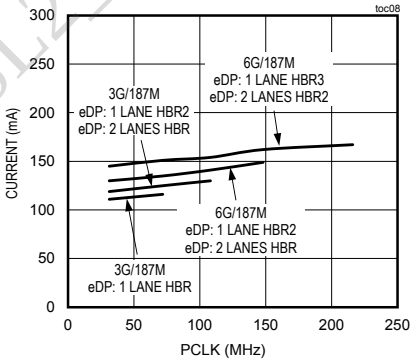
V_{DD18} CURRENT vs. TEMPERATURE GMSL1



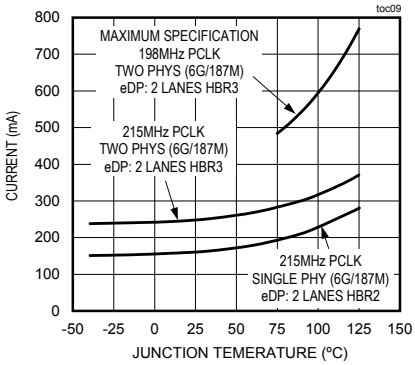
V_{DD} CURRENT TWO GMSL2 PHYS



V_{DD} CURRENT SINGLE GMSL2 PHY



V_{DD} CURRENT vs. TEMPERATURE GMSL2



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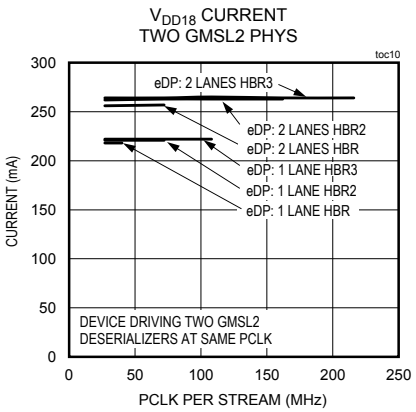
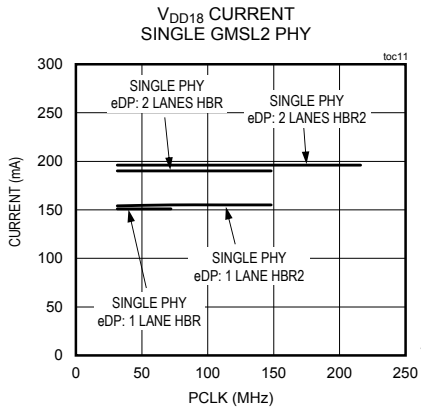
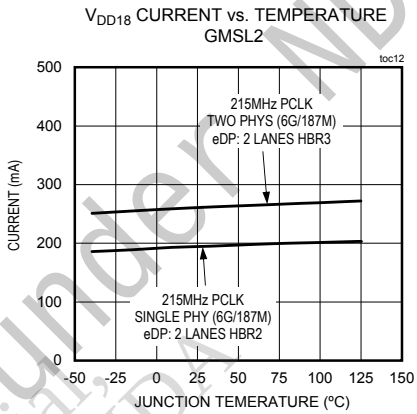
Typical Operating Characteristics (continued)

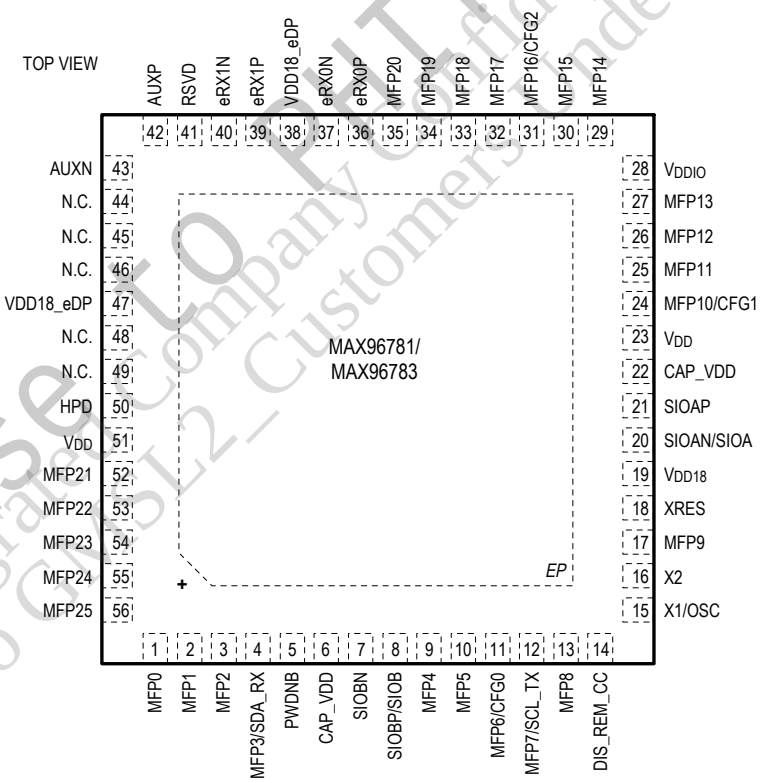
(V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, two PHY characteristics assume 2xMST video where the streams have identical timing, unless otherwise noted.)







Pin Configuration



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Pin Description

PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
GMSL SERIAL LINK				
7	SIOBN	SIOBN	SIOBN	SIOBN: GMSL Link-B Inverted Twisted-Pair Serial-Data Input/Output. State of CFG2 on power-up determines configuration.
8	SIOBP/SIOB	SIOBP SIOB	SIOBP SIOB	SIOBP: GMSL Link-B Noninverted Twisted-Pair Serial-Data Input/Output. State of CFG2 on power-up determines configuration. SIOB: GMSL Link-B Coax Serial-Data Input/Output. State of CFG2 on power-up determines configuration.
20	SIOAN/SIOA	SIOAN SIOA	SIOAN SIOA	SIOAN: GMSL Link-A Inverted Twisted-Pair Serial-Data Input/Output. State of CFG1 on power-up determines configuration. SIOA: GMSL Link-A Coax Serial-Data Input/Output. State of CFG1 on power-up determines configuration.
21	SIOAP	SIOAP	SIOAP	SIOAP: GMSL Link-A Noninverted Twisted-Pair Serial-Data Input/Output. State of CFG1 on power-up determines configuration.
DP INTERFACE				
36	eRX0P	eRX0P	eRX0P	eDP/DP Main Link Lane-0 Noninverted Input.
37	eRX0N	eRX0N	eRX0N	eDP/DP Main Link Lane-0 Inverted Input.
39	eRX1P	eRX1P	eRX1P	eDP/DP Main Link Lane-1 Noninverted Input.
40	eRX1N	eRX1N	eRX1N	eDP/DP Main Link Lane-1 Inverted Input.
42	AUXP	AUXP	AUXP	eDP/DP AUX Channel Noninverted Input/Output.
43	AUXN	AUXN	AUXN	eDP/DP AUX Channel Inverted Input/Output.
50	HPD	HPD	HPD	DP Hot Plug Detect Output. CMOS output. Default power-up is Logic-Low. Set LINK_ENABLE register bit at address 0x7000 to 1 after power-up to set HPD to Logic High. HPD = Logic Low with 1MΩ pulldown to GND when PWDNB is Low.
MULTIFUNCTION PINS (*Denotes default state after power-up.) (MFP functions which are blank in GMSL1 Mode are still available for a GMSL2 deserializer connected to the other link. GPIO functionality is always available through local register access)				
1	MFP0	SCK2 SCLK GPIO0*	SCK2	SCK2: I^2S/TDM Serial Clock Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. SCLK: SPI Clock. When configured as master, push-pull clock output. When configured as slave, clock input with internal 1MΩ pulldown to ground. GPIO0: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
2	MFP1	SD2 MOSI GPIO1*	SD2	SD2: I^2S/TDM Serial-Data Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. MOSI: SPI Master-Out Slave-In. When configured as master, push-pull output that drives data to external slave. When configured as slave, input with internal 1MΩ pulldown to ground that receives data from external master. GPIO1: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
3	MFP2	WS2 MISO GPIO2*	WS2	WS2: I^2S/TDM Serial-Word Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. MISO: SPI Master In Slave Out. When configured as master, input with internal 1MΩ pulldown to ground that receives data from external slave. When configured as slave, push-pull output that drives data to an external master. GPIO2: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
4	MFP3/SDA_RX	SDA* RX* GPIO3	SDA* RX*	SDA: I^2C Data Input/Open-drain Output with Internal 40kΩ Pullup to V_{DDIO} (SDA or RX selected by CFG0 at power-up). RX: UART Input (SDA or RX selected by CFG0 at power-up). GPIO3: Configurable General Purpose Input and Open-Drain Output.
9	MFP4	LMN0 GPIO4*	LMN0	LMN0: Line Fault Monitor Input. GPIO4: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
10	MFP5	LMN1 GPIO5*	LMN1	LMN1: Line Fault Monitor Input. GPIO5: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
11	MFP6/CFG0	CFG0 GPO6*	CFG0 GPOA*	CFG0: Configuration Pin 0. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between V_{DDIO} and ground. See Table 11. GPO6: General-Purpose Push-Pull Output. Disabled by default to accommodate CFG0 function. GPOA: Push-Pull Output. Output state corresponds to data received from GMSL1 deserializer on link A.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
12	MFP7/SCL_TX	SCL* TX* GPIO7	SCL* TX*	SCL: I^2C Clock Input/Open-Drain Output With Internal 40kΩ Pullup to V_{DDIO} (SCL or TX selected by CFG0 at power-up). TX: UART Open-drain Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX selected by CFG0 at power-up). GPIO7: Configurable General Purpose Input and Open-Drain Output.
13	MFP8	LOCK* GPIO8	—	LOCK: Open-Drain Lock Indication Output with Internal 40kΩ Pullup to V_{DDIO}. LOCK = high indicates that GMSL2 link has locked and is ready to send/receive data. See LOCK_CFG register description. LOCK is high when PWDNB is low. For GMSL1 mode links, the serializer LOCK function is not functional. GPIO8: Configurable General-Purpose Input/Output.
17	MFP9/ERRB	ERRB* GPIO9	ERRB*	ERRB: Open-drain Error Indication Output with Internal 40kΩ Pullup to V_{DDIO}. ERRB = low indicates that a data error, line fault, or interrupt has been detected. ERRB is high when PWDNB is low. GPIO9: Configurable General-Purpose Input/Output.
24	MFP10/CFG1	CFG1 GPO10*	CFG1 GPOB*	CFG1: Configuration Pin 1. Voltage at pin sets device modes, which are latched at power-up. Connect to a resistor divider between V_{DDIO} and ground. See Table 12. GPO10: General-Purpose Push-Pull Output. Disabled by default to accommodate CFG1 function. GPOB: Push-Pull Output. Output state corresponds to data received from GMSL1 deserializer on link B.
25	MFP11	WS1 GPIO11*	WS1 CNTL1*	WS1: I^2S/TDM Word-Select Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. GPIO11: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. CNTL1: Control Input which Tunnels Through to Assigned Pin on GMSL1 Deserializer. Power-up default, 1MΩ pulldown to ground.
26	MFP12	SD1 GPIO12*	SD1	SD1: I^2S/TDM FWD Audio Channel Serial Data Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. GPIO12: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
27	MFP13	SCK1 GPIO13*	SCK1	SCK1: I^2S/TDM FWD Audio Channel Clock Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. GPIO13: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
29	MFP14	GPIO14*	CNTL0*	GPIO14: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. CNTL0: Control Input which Tunnels Through to Assigned Pin on GMSL1 Deserializer. Power-up default, 1MΩ pulldown to ground.
30	MFP15	GPIO15*	—	GPIO15: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
31	MFP16/CFG2	CFG2 GPO16*	—	CFG2: Configuration Pin 2. Voltage at pin sets device modes, which are latched at power-up. Connect to a resistor divider between V_{DDIO} and ground. See Table 13. GPO16: General-Purpose Push-Pull Output. Disabled by default to accommodate CFG2 function.
32	MFP17	SDA1 RX1 GPIO17*	SDA1 RX1	SDA1: Pass-Through Port 1 (GMSL2) or alternative remote main control channel (GMSL1) I^2C Data Input/ Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. RX1: Pass-Through Port 1 (GMSL2) or alternative remote main control channel (GMSL1) UART Input. GPIO17: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
33	MFP18	SCL1 TX1 GPIO18*	SCL1 TX1	SCL1: Pass-Through Port 1 (GMSL2) or alternative remote main control channel (GMSL1) I^2C Clock Input/ Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. TX1: Pass-Through Port 1 (GMSL2) or alternative remote main control channel (GMSL1) UART Open Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO18: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
34	MFP19	LMN2 GPIO19*	LMN2	LMN2: Line Fault Monitor Input. GPIO19: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
35	MFP20	LMN3 GPIO20*	LMN3	LMN3: Line Fault Monitor Input. GPIO20: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
52	MFP21	BNE SS1 GPIO21*	—	BNE: SPI Buffer Not Empty. When configured as slave, SPI push-pull output. BNE = high indicates SPI data is available. SS1: SPI Slave Select. When configured as master, slave 1 select push-pull output. GPIO21: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
53	MFP22	PCLKOUT RO SS2 GPIO22*	PCLKOUT CNTL2*	PCLKOUT: Video Pixel Clock Push-pull Output. RO: When Configured as Slave, SPI Mode-Select Input with Internal 1MΩ Pulldown to Ground. RO = high enables master read from MISO. RO = low enables master write to MOSI. SS2: SPI Slave Select. When configured as master, slave 2 select push-pull output. GPIO22: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. CNTL2: Control Input which Tunnels Through to Assigned Pin on GMSL1 Deserializer. Power-up default, 1MΩ pulldown to ground.
54	MFP23	DEOUT SDA2 RX2 GPIO23*	DEOUT SDA2 RX2 CNTL3*	DEOUT: Video Date Enable Timing Signal Push-pull Output. SDA2: Pass-Through Port 2 (GMSL2) or alternative remote main control channel (GMSL1) I^2C Data Input/ Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. RX2: Pass-Through Port 2 (GMSL2) or alternative remote main control channel (GMSL1) UART Input. GPIO23: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. CNTL3: Control Input which Tunnels Through to Assigned Pin on GMSL1 Deserializer. Power-up default, 1MΩ pulldown to ground.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
55	MFP24	HSOUT MS RCLKOUT GPIO24*	HSOUT MS RCLKOUT	HSOUT: Video Horizontal Sync Timing Signal Push-pull Output. MS: UART Mode Select with Internal 1MΩ Pulldown to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be temporarily overwritten by a register write. RCLKOUT: 25MHz Frequency Reference Push-Pull Output. Enabled or disabled by register write. Can be divided by 1, 2 or 4. GPIO24: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown.
56	MFP25	VSOUT SCL2 TX2 GPIO25*	VSOUT SCL2 TX2 CNTL4	VSOUT: Video Vertical Sync Timing Signal Push-pull Output. SCL2: Pass-Through Port 2 (GMSL2) or alternative remote main control channel (GMSL1) I^2C Clock Input/ Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. TX2: Pass-Through Port 2 (GMSL2) or alternative remote main control channel (GMSL1) UART Open Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO25: Configurable General-Purpose Input/Output. Power-up default: CMOS in, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. CNTL4: Control Input which Tunnels Through to Assigned Pin on GMSL1 Deserializer. Power-up default, 1MΩ pulldown to ground.
MISCELLANEOUS—See Table 2				
5	PWDNB	PWDNB	PWDNB	Active-Low, Power-Down Input with Internal 1MΩ Pulldown to Ground. Apply logic low to place device in power-down mode. Connect to V_{DDIO}/logic high for normal operation.
14	DIS_REM_CC	DIS_REM_CC	DIS_REM_CC	Active-High, Disable Remote Control Channel Input with Internal 100kΩ Pulldown to Ground. Connect to V_{DD18} or logic high to disable the remote control channel. Apply logic low, connect to ground or leave floating to enable the remote control channel function. Latched at power-up only.
15	X1/OSC	X1/OSC	X1/OSC	X1/OSC: Crystal/Oscillator Input. Connect to either one terminal of a +/-200ppm 25MHz crystal or a 25MHz external clock source. If crystal is used, connect a load capacitor from X1/OSC to ground (Load capacitor value depends on crystal used).
16	X2	X2	X2	X2: Crystal Input. Connect to one terminal of a 25MHz +/-200ppm crystal. If crystal is used, connect a load capacitor from X2 to ground (Load capacitor value depends on crystal used). If external oscillator is connected to X1/OSC, leave X2 floating.

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PIN	NAME	FUNCTION MODE		FUNCTION
		GMSL2	GMSL1	
18	XRES	XRES	XRES	Output Reference Resistor. Connect a 402Ω +/-1% resistor between XRES and ground.
41	RSVD	RSVD	RSVD	Reserved. Make no electrical connection to this pin.
44, 45, 46, 48, 49	N.C.	NC	NC	No Connection. Make no electrical connection to this pin.
POWER SUPPLIES—See Table 2				
6, 22	CAP_VDD	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1V Core Supply (See Table 2). Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
19	VDD18	VDD18	VDD18	1.7V to 1.9V Analog supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
23, 51	VDD	VDD	VDD	1.0V Core Supply. Connect a 0.95V to 1.05V supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
28	VDDIO	VDDIO	VDDIO	1.7V to 3.6V I/O Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
38, 47	VDD18_eDP	VDD18_eDP	VDD18_eDP	1.7V to 1.9V eDP/DP Analog Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
EP	EP	EP	EP	Exposed Pad. EP is internally connected to device ground. EP MUST be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

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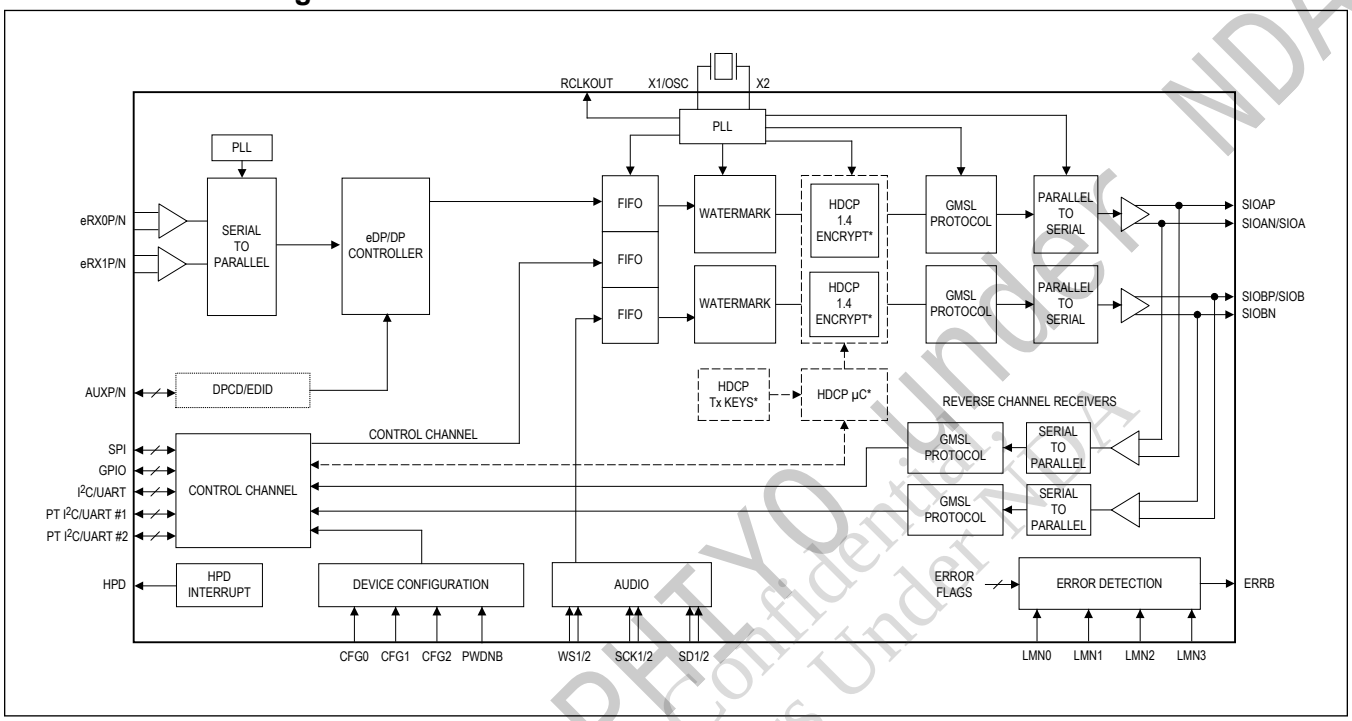
Functional Diagrams

Functional Block Diagram



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Detailed Description

External Component Requirements

See Figure 26 and Figure 27 for details on the minimum (application-specific) external component requirements.

Table 2. External Component Requirements

COMPONENT	SYMBOL	CONDITION		VALUE	UNIT
XRES	R_{XRES}			402 ±1%. Use a single resistor.	Ω
Configuration Setting Resistors		These resistors determine the startup configuration of the part. See Table 11, Table 12, and Table 13 for details.			
Line Fault Pulldown Resistor	R_{PD}			49.9 ±1%	kΩ
Line Fault Series Resistors - Coax Mode	R_{EXT1}	LMN0, LMN1, LMN2 or LMN3		48.7 ±1%	kΩ
	R_{EXT2}			DNI	
Line Fault Series Resistor - STP Mode	R_{EXT1}	See *Line Fault* section for STP Mode		48.7 ±1%	kΩ
	R_{EXT2}	See *Line Fault* section for STP Mode		42.2 ±1%	
Link Isolation Capacitors	C_{LINK}	Place close to the SIO_ pins (7, 8, 20, and 21) used in the application.	GMSL2, GMSL1 HIM	0.1	µF
			GMSL1 non-HIM	0.22	
Coax Mode Termination Resistor	R_{TERM}	In coax mode, connect R_{TERM} between unused SIO_ pin and ground on each coax link.		49.9 ±1%	Ω
eRXxx Isolation Capacitors and trace impedance	C_eRX_N/P	DP trace, maintain 50Ω characteristic impedance, 0.1µF AC capacitor required.		0.1	µF
AUX Interface Isolation Capacitors	C_AUX	Place series 0.1µF DC blocking capacitors on AUXP and AUXN interfaces		0.1	µF
Crystal		Place as close as possible to pins 15 and 16.		25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values which compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible to pins 15 (X1/OSC) and pin 16 (X2).			
V_{DDIO} Decoupling Capacitors*		Place 0.01µF and 0.1µF capacitors as close as possible to pin 28.		0.01 + 0.1	µF
V_{DD18} Decoupling Capacitors*		Place 0.01µF and 0.1µF capacitors as close as possible to pin 19.		0.01 + 0.1	µF

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Table 2. External Component Requirements (continued)

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
V_{DD18_eDP} Decoupling* Capacitors		Place one each of 0.01µF and 0.1µF capacitors as close as possible to pins 38 and 47. Run separate traces from each pin to the capacitors. For compatibility with other DP serializers, a pair of these capacitors may also be connected to pin 44.	(2) 0.01 + (2) 0.1	µF
V_{DD} Decoupling Capacitors*		Place one each of 0.1µF and 10µF capacitors as close as possible to pins 23 and 51. Run separate traces from each pin to the capacitors.	(2) 0.01 + (2) 10	µF
CAP_VDD Decoupling Capacitors		Place a 0.1µF capacitor as close as possible to pin 6. Place 0.1µF and 10µF capacitors as close as possible to pin 22.	(2) 0.1 + 10	µF
Open-Drain Pullup Resistors		Application-Specific. Quantity and values depend on multifunction GPIO pin configurations.		

* With exception of CAP_VDD, power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

Functional Diagrams

Serial Output Parameters

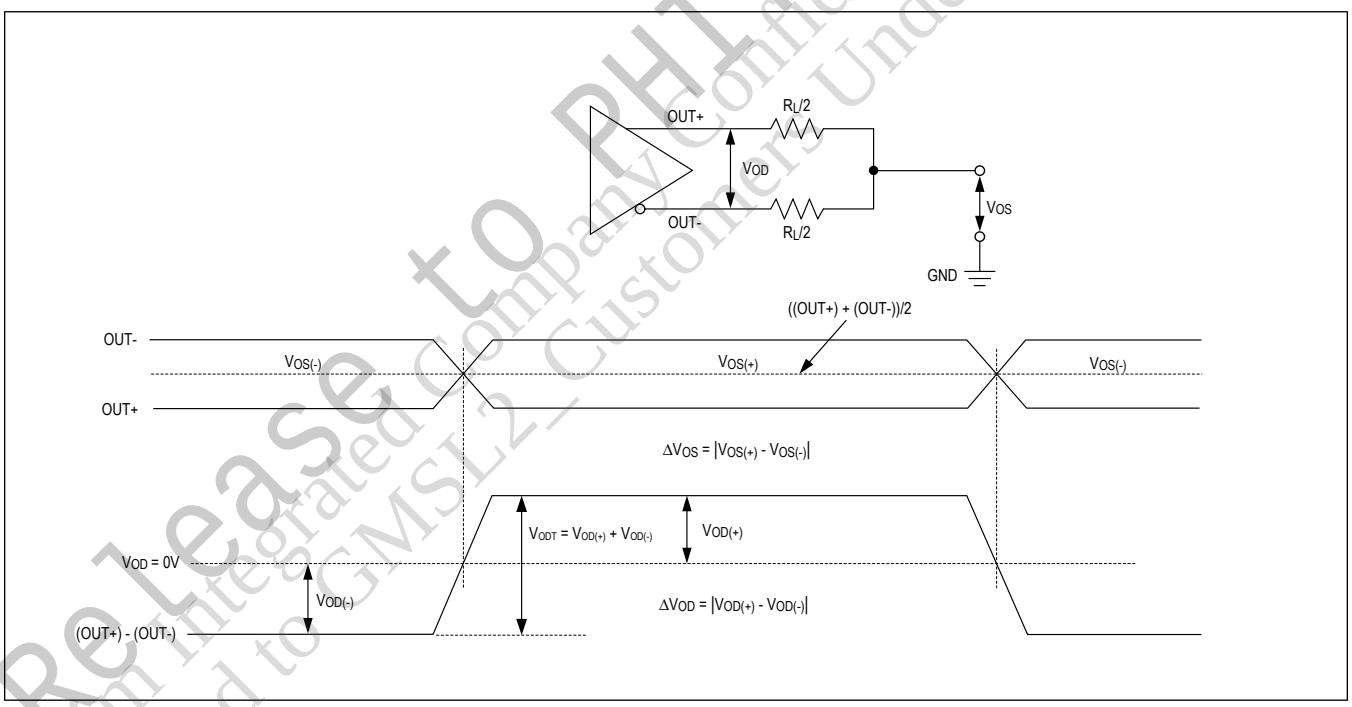

Figure 1. Serial Output Parameters

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GMSL2 Video Initialization Time

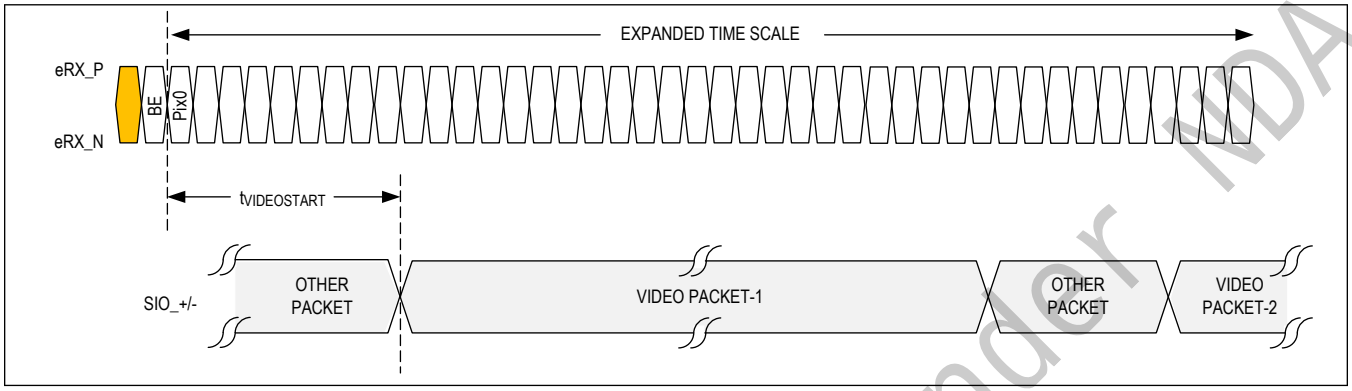

Figure 2. GMSL2 Video Initialization Time

GMSL2 Video Latency

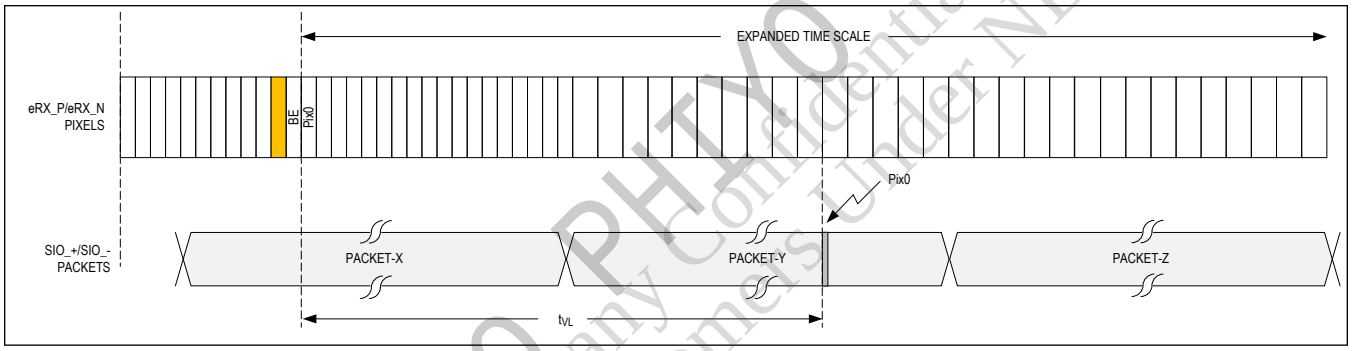

Figure 3. GMSL2 Video Latency

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GMSL1 Link Startup Time

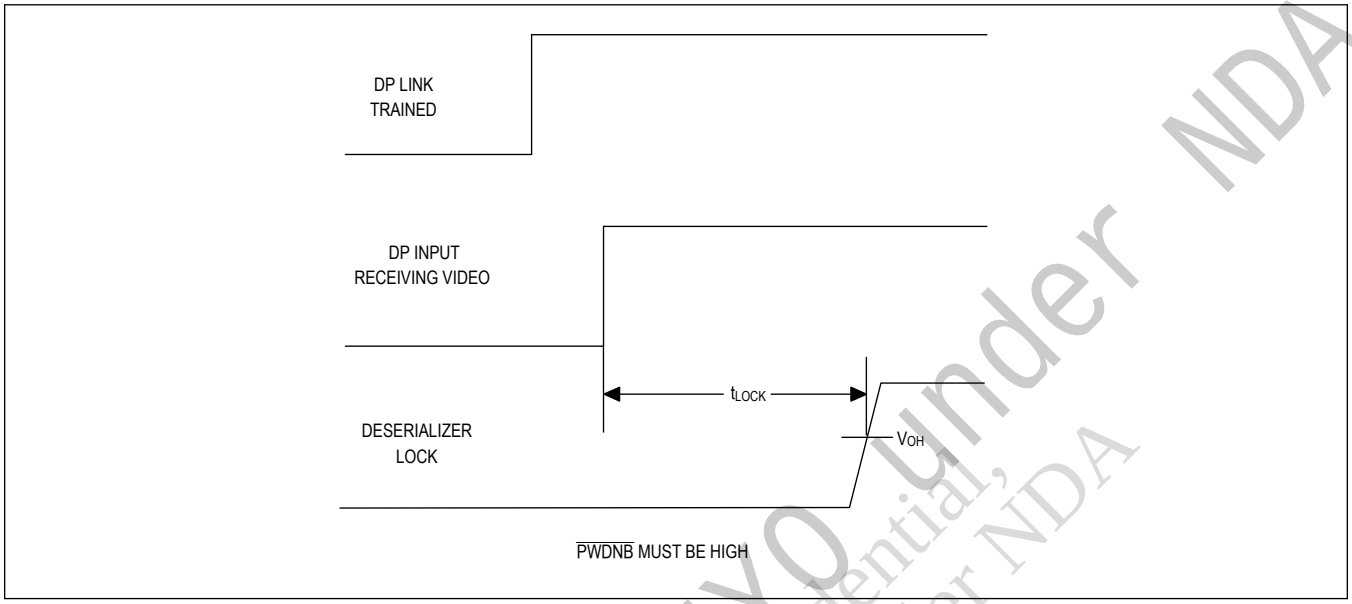

Figure 4. GMSL1 Link Startup Time

GMSL1 Video Latency

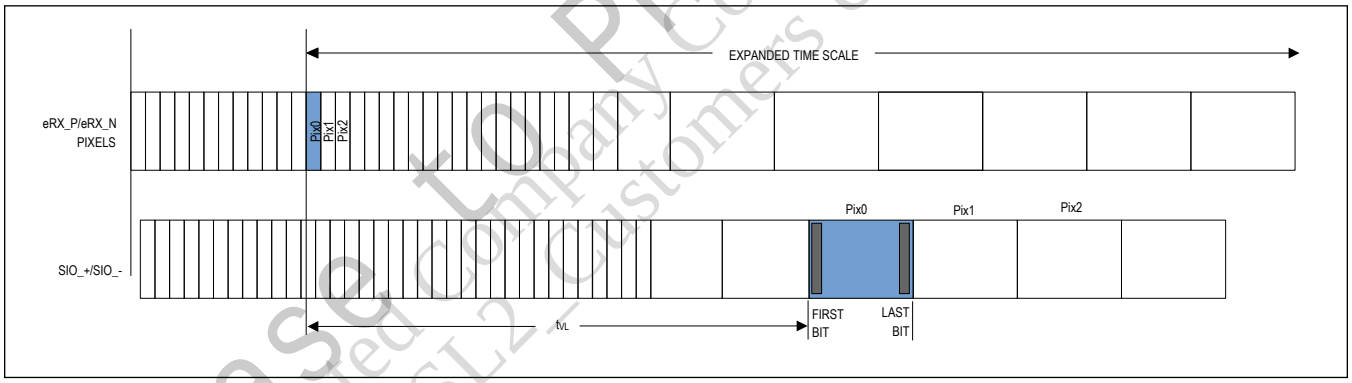

Figure 5. GMSL1 Video Latency

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I²C Timing Parameters

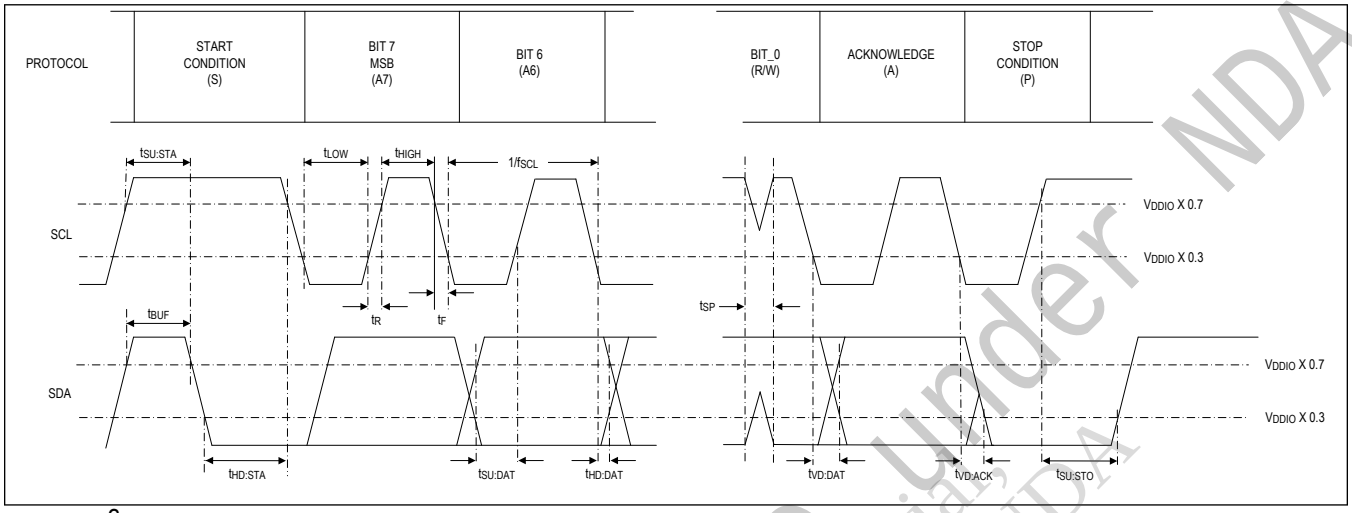

Figure 6. I²C Timing Parameters

I²C/UART Wake Time

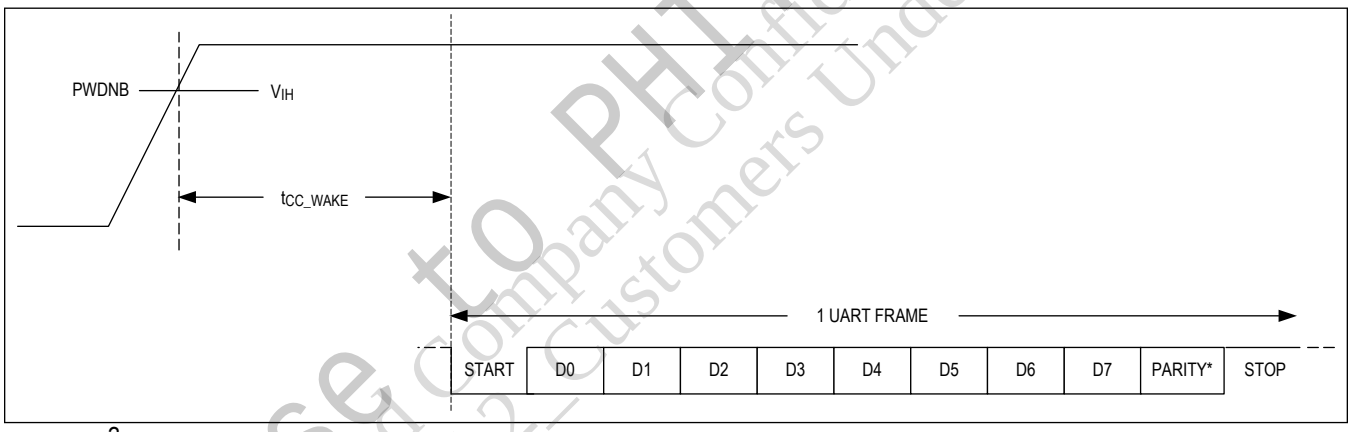

Figure 7. I²C/UART Wake Time

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SPI Master-Mode Timing Parameters

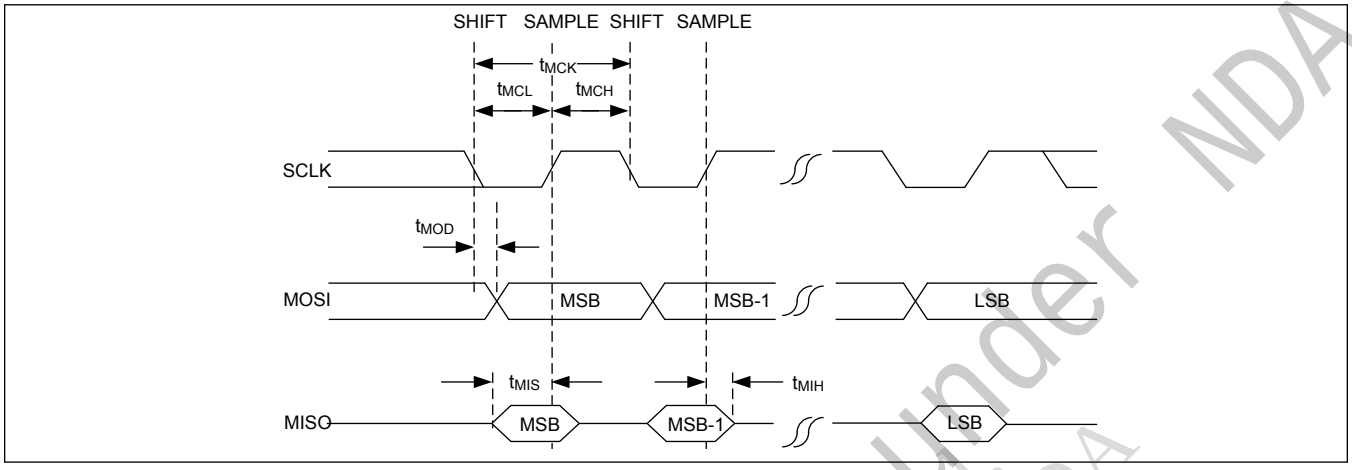

Figure 8. SPI Master-Mode Timing Parameters

SPI Slave Mode Timing Parameters

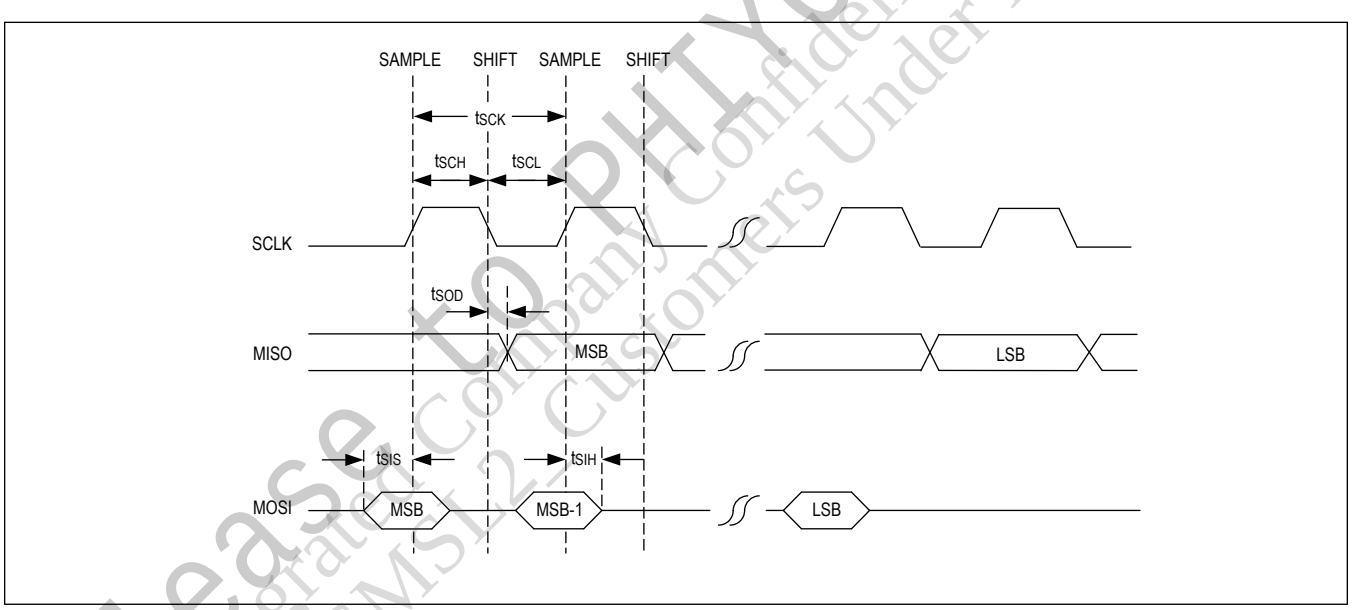

Figure 9. SPI Slave Mode Timing Parameters

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I²S Slave Mode Timing Parameters

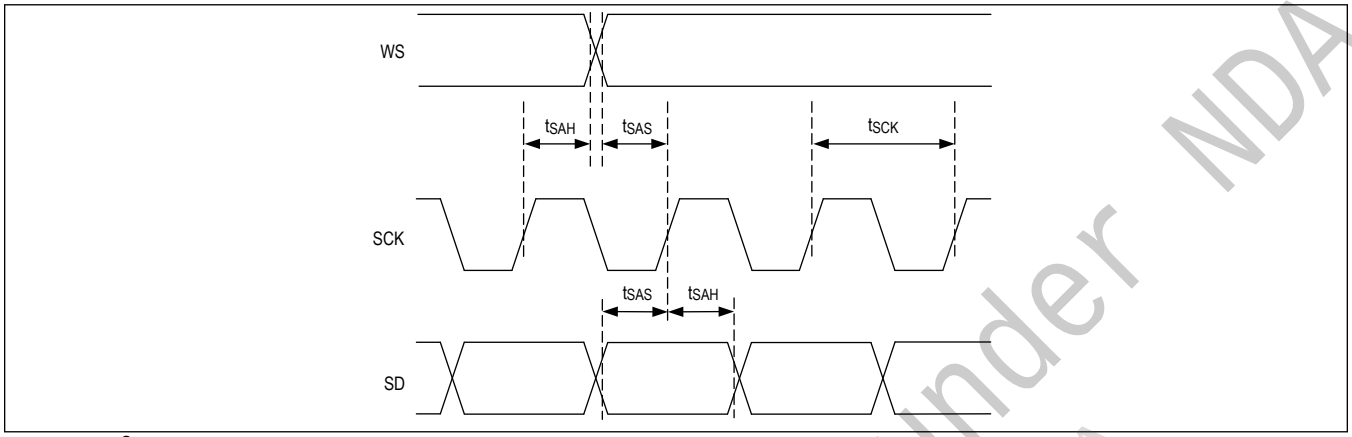

Figure 10. I²S Slave Mode Timing Parameters

Detailed Description

Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews and register definitions. Designers must also have the following information to correctly design using this device:

- The **GMSL2 Channel Specification** contains physical layer requirements for the PCB traces, cables and connectors that constitute the GMSL2 link.
- The **GMSL2 Hardware Design Guide** contains recommendations for PCB design, applications circuits, selection of external components and guidelines for use of GMSL2 signal integrity tools.
- The **GMSL2 User Guide** contains detailed programming guidelines for GMSL2 device features.
- **Errata sheets** contain deviations from published device specifications and are specific to part number and revision ID.

Contact the factory to receive these documents and for additional guidance on MAX96781/MAX96783 features.

Introduction

Gigabit Multimedia Serial Link™ serializers and deserializers provide high-speed, low bit-error-rate, serial-data transport supporting a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL2 provides fixed link rates of 6 or 3Gbps forward and 187.5Mbps reverse utilizing packetized data transmission.

GMSL1 provides link rates from 500Mbps to 3.12Gbps forward and 1Mbps reverse.

The following sections provide a brief overview of the device features and functions. A more comprehensive GMSL user's guide, various application notes, and other collateral are available to assist end users by describing the features and associated implementation details. Contact factory for this additional information and details on configuration of each function and feature.

Product Overview

The MAX96781/MAX96783 convert a 1- or 2-lane DP1.4 or eDP1.4a input to single or dual GMSL2/1 output. The input can consist of single stream SST or single/dual stream MST video.

The GMSL links can be independently configured to support GMSL2 or GMSL1 deserializers. In GMSL2 mode, each link provides 3Gbps or 6Gbps forward capacity and 187.5Mbps reverse-link bandwidth. In GMSL1 mode, each link provides up to 3.12Gbps forward and 1Mbps reverse bandwidth.

Up to approximately 360MHz combined PCLK can be supported at HBR2 data rate, limited by the DP link bandwidth. Up to approximately 430MHz combined PCLK can be supported at HBR3 data rate, limited by the total capacity of the 2

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GMSL2 links. Note that since the MAX96781/MAX96783 support asymmetric streams, the GMSL link utilization can be different. For example, a 200MHz stream on PHYA and a 160MHz stream on PHYB.

Each GMSL2 configured link can support up to two simultaneous video streams, each with independent timing. The combined equivalent PCLK of the two streams must be below the maximum available capacity of the link. GMSL1 links can support a single video stream.

The MAX96783 adds HDCP 1.4 encryption of either or both GMSL2/1 links. After HDCP is configured, the authentication and key exchange are fully automated without requiring additional external microcontroller (µC) involvement while operating in GMSL2 mode.

DisplayPort

The MAX96781/MAX96783 devices support DisplayPort 1.4 and embedded DisplayPort 1.4a input interfaces with lane rates of 2.7, 5.4 and 8.1 Gbps in 1- or 2-lane configurations. The serializer functions as a DP sink device capable of supporting both single-stream transport (SST) and multi-stream transport (MST) modes (2-streams max). DP AUX and HPD interfaces are also supported.

The MAX96781/MAX96783 devices do not support the MST mode DP Topology Assistant and associated topology discovery, topology maintenance, EDID discovery and messaging AUX client. Given the fixed nature of automotive infotainment platforms, the system topology, desired DP configuration and EDID details of each display are specified during system design and as a result there is no need to support these functions.

DP SST mode is fully supported.

The MAX96781/MAX96783 support legacy DP/eDP versions back to DP1.2 and eDP1.2.

Other Functions

The MAX96781/MAX96783 serializers have a main I^{2}C/UART control-channel interface that an ECU uses to access serializer and deserializer registers, as well as peripheral devices, from either end of the link. Each device also has two pass-through I^{2}C/UART channels available for remote peripheral control when used in conjunction with GMSL2 links. The dedicated pass-through I^{2}C/UART channels are not available in GMSL1 mode, but the pass-through ports can optionally be utilized as the main control channel for remote devices in GMSL1 links. See the *Pass-Through I^{2}C/UART* section.

The MAX96781/MAX96783 support 2 forward (serializer to deserializer) audio channels. The forward channels support audio from the local I^{2}S interfaces. The audio channels support I^{2}S stereo and up to 8 channels in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 bits to 32 bits. Each GMSL link can support one audio channel in either GMSL1 or GMSL2 mode.

Additionally, the MAX96781/MAX96783 include an SPI master/slave interface, including two slave-select pins, for peripheral control. The SPI interface enables a host SPI master on one side of a GMSL2 link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link or can swap ends with reprogramming of the GMSL2 devices (a GMSL device can be configured as an SPI master or slave). The SPI function is available only in links using GMSL2 mode.

The MAX96781/MAX96783 provide up to 26 GPIOs, depending on device feature utilization. GPIOs are typically used to tunnel low-speed (< 100kbps) signals over a GMSL2 link. A GPIO tunnel can be set up in the forward or reverse direction. It is also possible to locally read/write GPIOs instead of using the tunneling feature. GMSL1 operation has a unique set of tunneled GPIO pins.

The devices include a video crossbar and watermark generation or detection. The crossbar can be used to reorder the color and sync signals while the watermark generation is used for inserting an invisible watermark in the video image that can be used to identify a frozen video stream. Watermark detection is not supported by legacy GMSL1 deserializers.

The eDP/DP interface supports lane remapping and polarity swap to enable optimized interconnect routing.

The MAX96781/MAX96783 devices incorporate numerous link-margin optimization and monitoring functions to ensure high link margin. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. PRBS checking is supported to verify the correct link and video channel operation.

Serializer Modes

The MAX96781/MAX96783 include DP MST support, two internal video pipes, and two independently configurable GMSL

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links. Flexible configuration and video routing enables a variety of configurations, including replication, dual link, and splitter.

The user can configure each video pipeline to be routed to either GMSL output or to both outputs for replication (each GMSL1 link can support only one video stream at a time). Each GMSL output can be configured for either GMSL1 or GMSL2 operating mode. In applications using both GMSL links, powering off a deserializer or disconnecting the cable does not affect operation of the other link.

Single Video Stream, Single GMSL1 Link

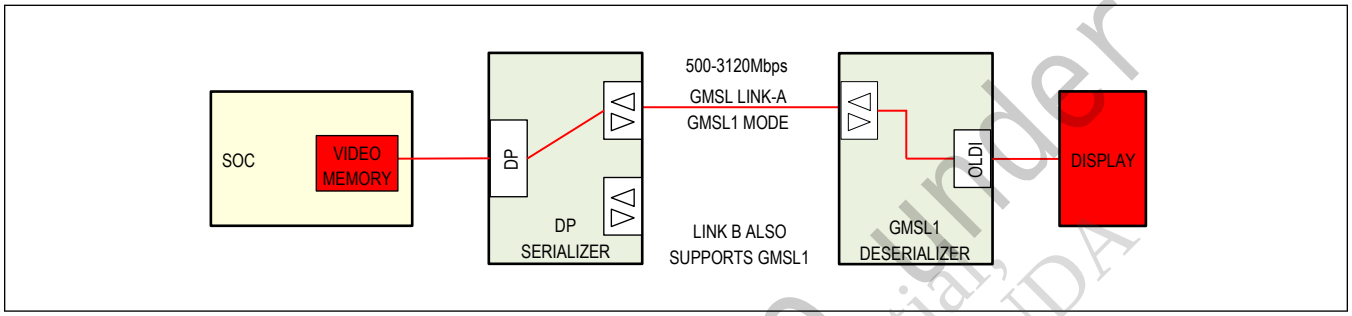

Figure 11. Single Video Stream in GMSL1 Mode

GMSL1 mode is supported by Link A and Link B. In single link GMSL1 applications, either link can be used. Any GMSL1 deserializer or GMSL2 deserializer with GMSL1 backwards compatibility can be paired. The maximum speed is determined by the specific deserializer used in the application. The maximum link rate supported by the MAX96781/MAX96783 is 3.12Gbps, which corresponds to a PCLK of up to 104MHz. The MAX96783 provides HDCP 1.4 support on both links in GMSL1 mode.

Single Video Stream, Single GMSL2 Link

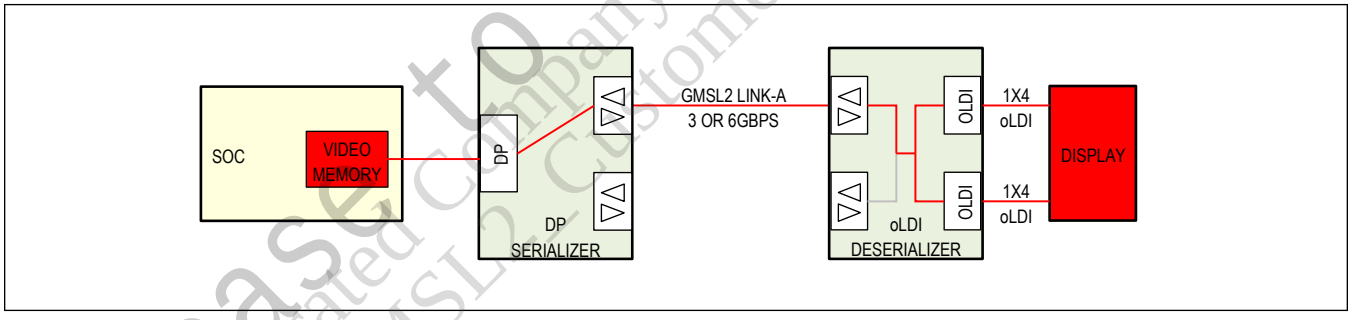

Figure 12. Single Video Stream in GMSL2 Mode

Any GMSL2-compatible deserializer can be paired on either link. The GMSL2 link can be configured with 3Gbps or 6Gbps bandwidth. A maximum of approximately 215MHz PCLK can be transmitted over a 6Gbps link. This supports 2560 x 1080, 24-bit, 60Hz or equivalent video. At 3Gbps, the 104MHz maximum PCLK supports 1920 x 720, 24-bit, 60Hz or equivalent video. The MAX96783 provides HDCP 1.4 on either link.

Single Video Stream with Dual GMSL2 Links

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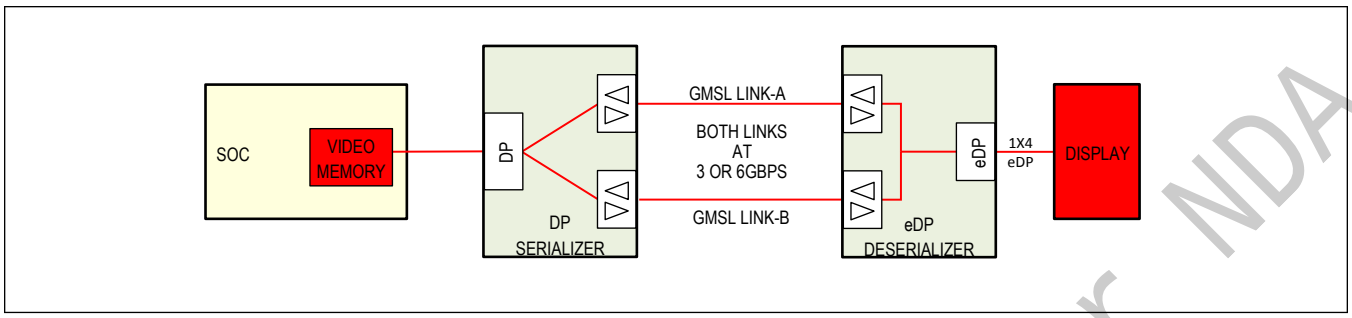

Figure 13. Single Video Stream with Dual GMSL2 Links and eDP Deserializer

The MAX96781/MAX96783 can be paired with any deserializer that supports dual-link GMSL2. The two links function logically as a single link with twice the throughput, enabling transmission of video streams with PCLK > 400MHz. A maximum of approximately 215MHz PCLK can be transmitted over each 6Gbps link, providing a total PCLK capacity of approximately 430MHz. At 3Gbps, each link can support a maximum PCLK of approximately 104MHz for a total of 208MHz PCLK.

The MAX96781/MAX96783 supports STQ interconnects with two differential pairs for the GMSL2 interface, enabling a single cable assembly to transfer data from both links. This is especially convenient in dual link applications.

The MAX96783 provides HDCP 1.4 for one stream up to the maximum PCLK supported by the link configuration.

Single Video Stream with Replication, GMSL1 Links

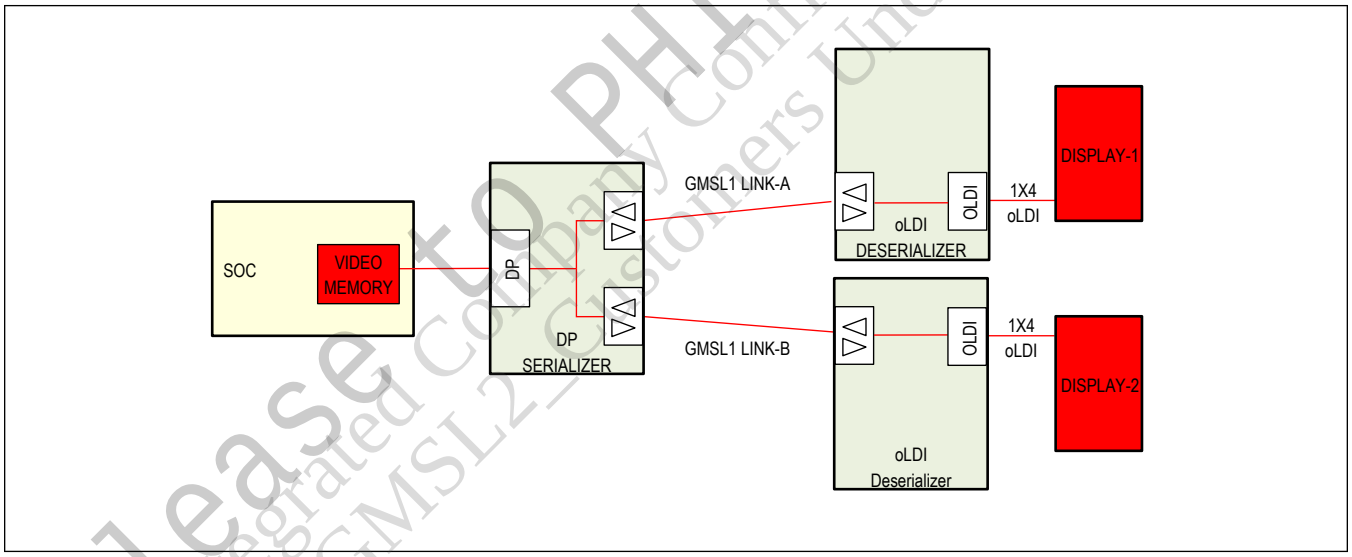

Figure 14. Serializer Single-Stream Replication in GMSL1 mode

An identical video stream is transmitted over both links. A maximum of approximately 104MHz PCLK can be transmitted over each GMSL1 link depending on configuration, which supports 1920 x 720, 24-bit, 60Hz or equivalent video.

Either GMSL2 deserializers operated in GMSL1 backward compatibility mode or legacy GMSL1 deserializers can be used.

The MAX96783 provides HDCP 1.4 on both links.

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Single Video Stream with Replication, GMSL2 Links

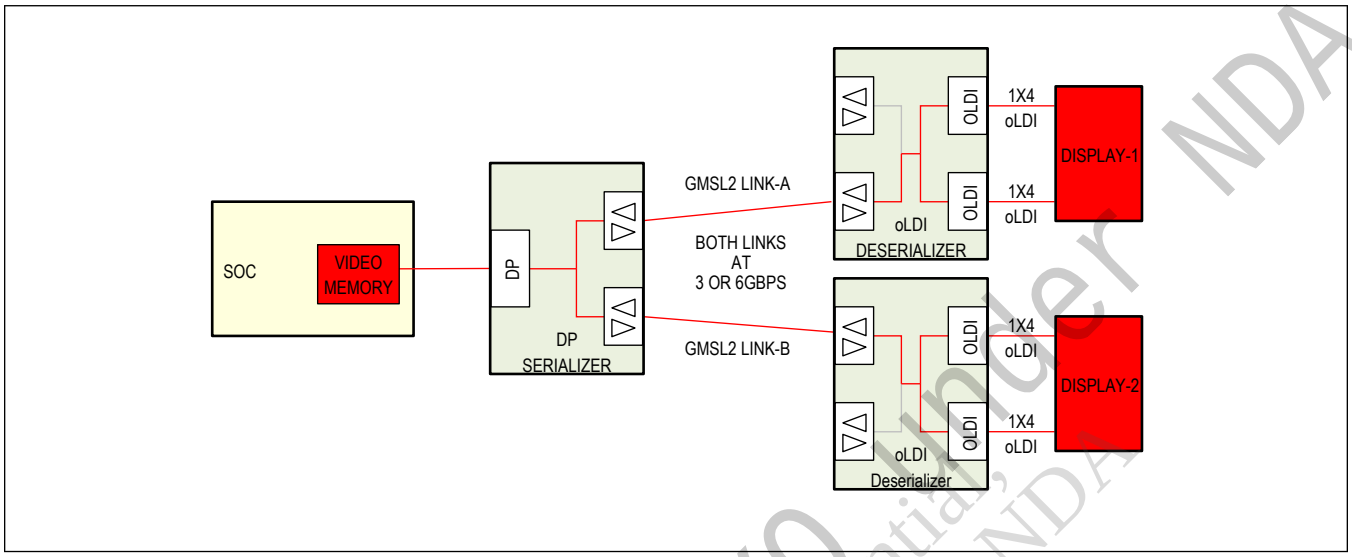

Figure 15. Serializer Single-Stream Replication in GMSL2 mode

An identical video stream is transmitted over both links. A maximum of approximately 215MHz PCLK can be transmitted over each 6Gbps link, which supports 2560 x 1080, 24-bit, 60Hz or equivalent video. 3Gbps links can support a maximum of approximately 104MHz PCLK, which enables 1920 x 720, 24-bit, 60Hz or equivalent video.

This mode is supported by all GMSL2 deserializers.

The MAX96783 provides HDCP 1.4 on both links.

Single Video Stream with Replication, mixed GMSL2 and GMSL1 Links

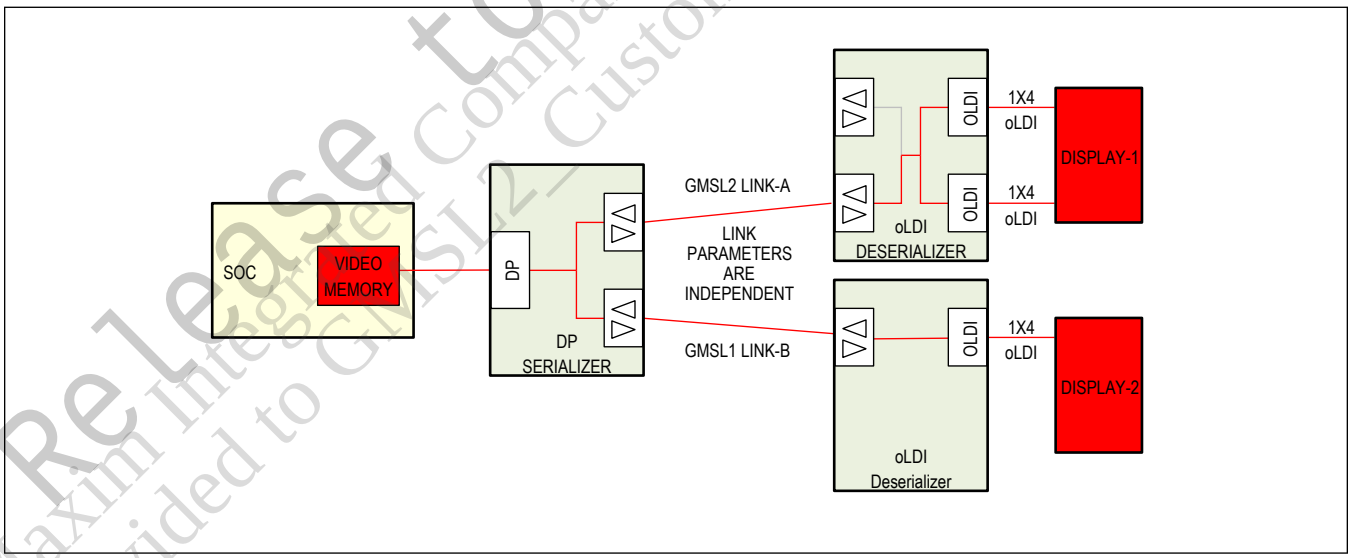

Figure 16. Serializer Single-Stream Replication with mixed GMSL2 and GMSL1 links

An identical video stream is transmitted over both links. A maximum of approximately 104MHz PCLK (limited by the GMSL1 bandwidth) can be transmitted over each link, which enables 1920 x 720, 24-bit, 60Hz or equivalent video.

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This mode is supported by all deserializers.

The MAX96783 provides HDCP 1.4 on both links.

2-Stream MST, GMSL1 Links

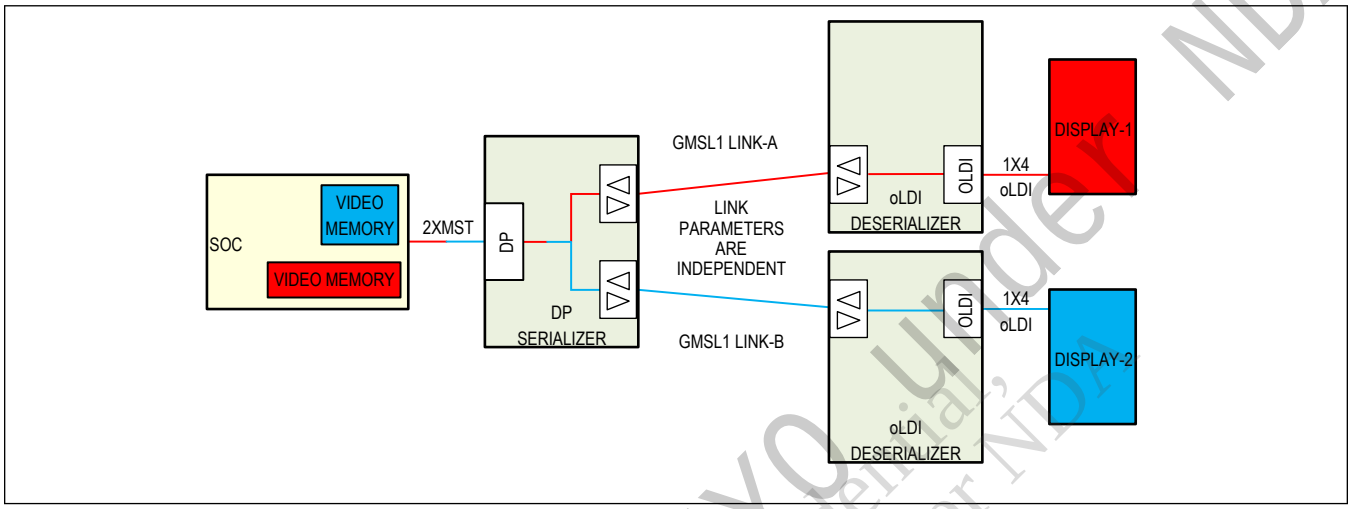

Figure 17. 2-Stream MST Splitter in GMSL1 Mode

The DP input receives two independent streams with unique timing and routes one stream to each link. Both links are configured for GMSL1 mode, and the specific configuration of the link parameters can be specified independently. GMSL link video bandwidth limitations are as described in the prior sections.

The MAX96783 provides HDCP 1.4 on both links.

2-Stream MST, GMSL2 Links

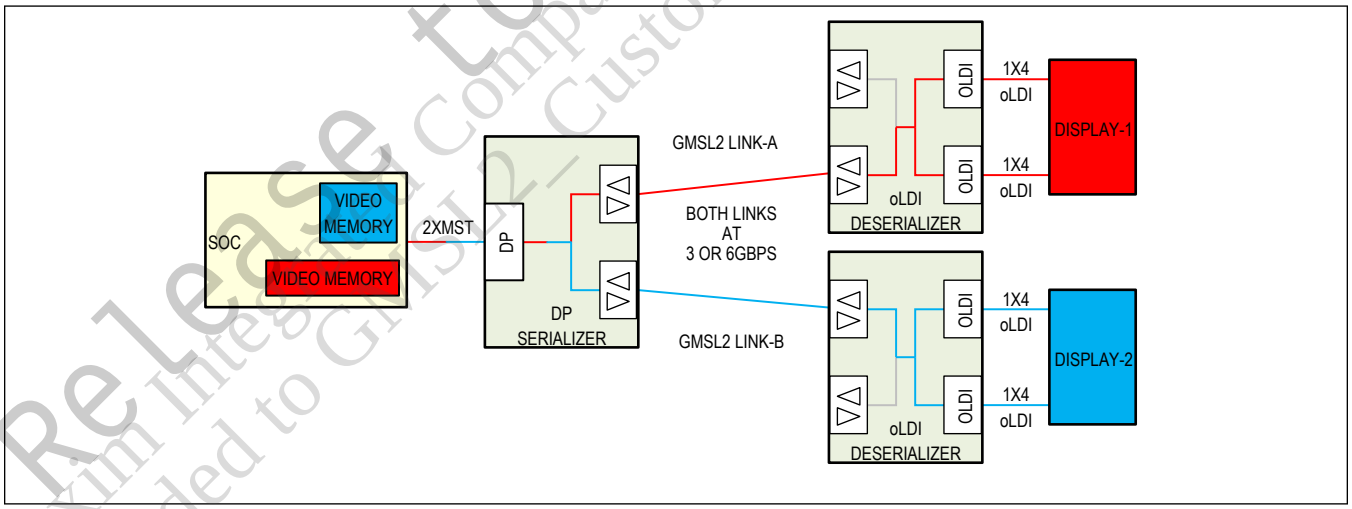

Figure 18. 2-Stream MST Splitter in GMSL2 mode

The DP input receives two independent streams with unique timing and routes one stream to each link. Both links are configured for GMSL2 mode. A common link speed must be used for both links. GMSL link video bandwidth limitations are as described in the prior sections.

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The MAX96783 provides HDCP 1.4 on both links.

2-Stream MST, mixed GMSL2 and GMSL1 links

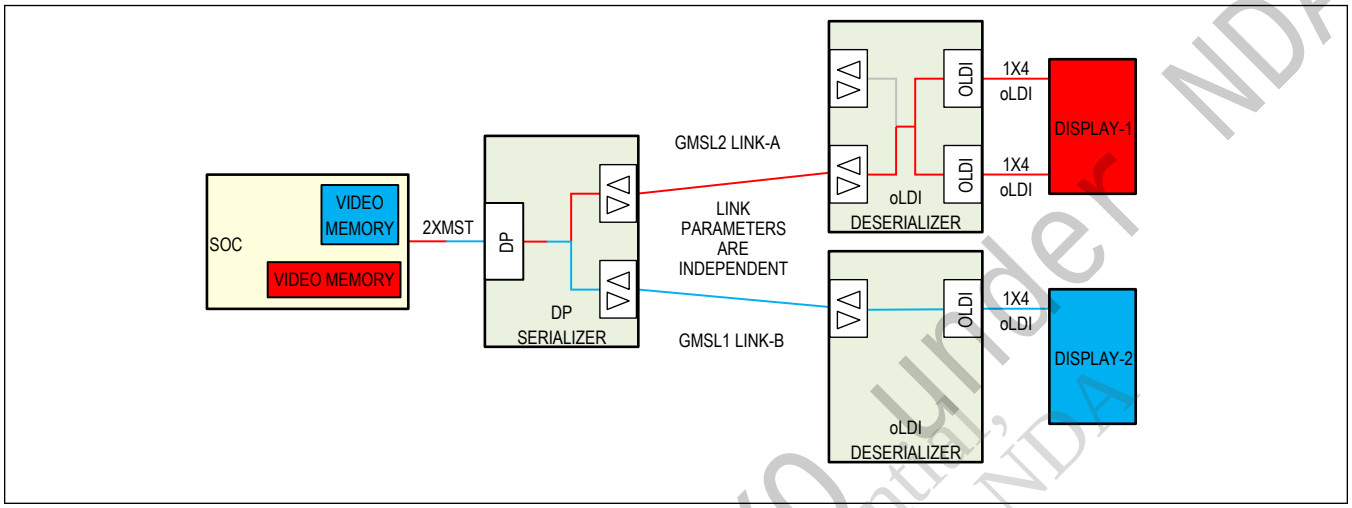

Figure 19. 2-Stream MST, Splitter with mixed GMSL1 and GMSL2 Links

The DP input receives two independent streams with unique timing and routes one stream to each link. One link is configured for GMSL2 operation while the other is configured for GMSL1 operation. Both links support either GMSL1 or GMSL2 operation, and the configuration of each link is independent. GMSL link video bandwidth limitations are as described in the prior sections.

The MAX96783 provides HDCP 1.4 on both links.

DisplayPort Receiver

The MAX96781/MAX96783 support DisplayPort 1.4 and Embedded DisplayPort 1.4a with lane rates of 2.7, 5.4 and 8.1Gbps in 1- and 2-lane configurations. They support both single stream transport (SST) and multi-stream transport (MST) modes (two streams max). DP AUX and HPD interfaces are also supported.

DP Sink Device

The MAX96781/MAX96783 function as a DP sink device capable of supporting both single-stream transport (SST) and multistream transport (MST) modes (2 streams).

The MAX96781/MAX96783 devices do not support the DP Topology Assistant and associated topology discovery, topology maintenance, EDID discovery and messaging AUX client. Given the fixed nature of automotive infotainment platforms, the system topology, desired DP configuration and EDID details of each display are known in advance and there is no need to support these functions.

Configuring MST Mode

Given that the MAX96781/MAX96783 devices do not support the DP Topology Assistant and associated topology discovery, topology maintenance, EDID discovery and messaging AUX client, it is necessary to modify the DP startup process as summarized in Table 3. The ECU should disable the topology manager.

Table 3. DisplayPort MST Setup

STEP	DESCRIPTION	INTERFACE	DIRECTION
1	Configure Serializer DP interface Configure Serializer video routing and video paths	I^2C	ECU → Serializer
2	Initiate DP Link Training	AUX	ECU ⇔ Serializer

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Table 3. DisplayPort MST Setup (continued)

3	Clear and load DP serializer payload allocation table	AUX	ECU → Serializer
4	Clear and load ECU payload allocation table	-	ECU Only
5	Generate ACT trigger sequence	DP Links	ECU → Serializer
6	Check for ACT trigger sequence recognition	AUX	Serializer → ECU
7	Start MST video stream transmission	DP Links	ECU → Serializer

Video Input Stream Format

Each SST or MST stream must be a standard single stream video using RGB888 format. Superframes are not supported. There is no practical limit to the video line width, as both the DP standard and MAX96781/MAX96783 support up to 65,535 pixels.

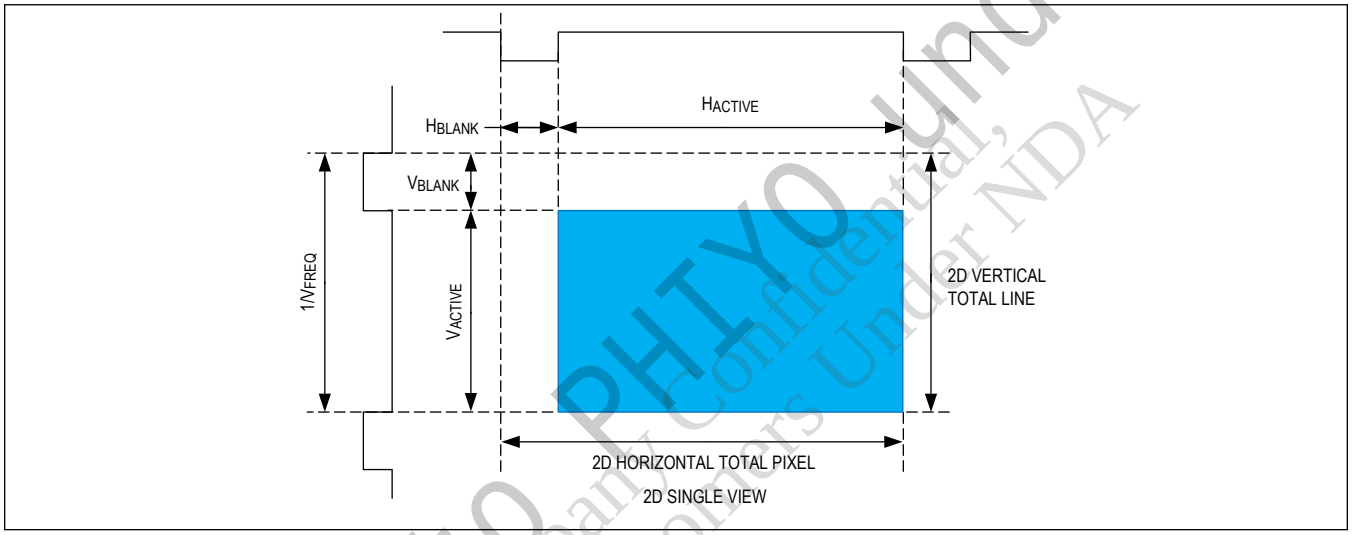

Figure 20. Single Video Stream

DP Link Training

MAX96781/MAX96783 link training is managed through AUX transactions from the DP source. Link training should be completed before the video is enabled. Link training recommendations are as follows:

- The MAX96781/MAX96783 devices are designed for use in embedded automotive applications where the link rate, lane count, and video resolutions are determined in advance (during system design) and strictly controlled by the DP source.
- Per the DP specification, if there are any link and/or signal integrity issues during the DP link training, the serializers properly signal to the DP source failures to obtain clock recovery, symbol lock, or lane alignment. Amplitude and/or pre-emphasis adjustment requests are issued if needed. If the link training fails after the amplitude/pre-emphasis adjustments, the serializer link training state machines stop and wait for further instructions from the DP source.
- Following a link training failure, consumer application DP sources proceed to reduce the lane count and/or link rate. The DP source programs the reduced values into the sink and restarts the training. As the link training is initiated and controlled by the DP source, the MAX96781/MAX96783 complies. While this is acceptable for consumer applications with flexible displays, in embedded applications with fixed displays/resolutions, DP sources should not perform the link rate and lane count reductions as it may cause insufficient link bandwidth for the video streams to be transported. In embedded applications, the failure to complete the link training should be reported as a hard error signaling hardware issues and requiring engineering debug.
- Link training status can be checked through registers 0x6418 (link rate), 0x6419 (lane count), and 0x641A (training status). It can also be checked using DisplayPort Configuration Data (DPCD) registers located at 0x202, 0x203, and 0x204.

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- Contact the factory for additional information on DP link training constraints.

DisplayPort PHY

The MAX96781/MAX96783 devices support DP lane rates of 2.7, 5.4 and 8.1 Gbps in 1- and 2-lane configurations. eDP/DP lanes can be remapped and/or phase inverted.

DP Main-Link Differential Input

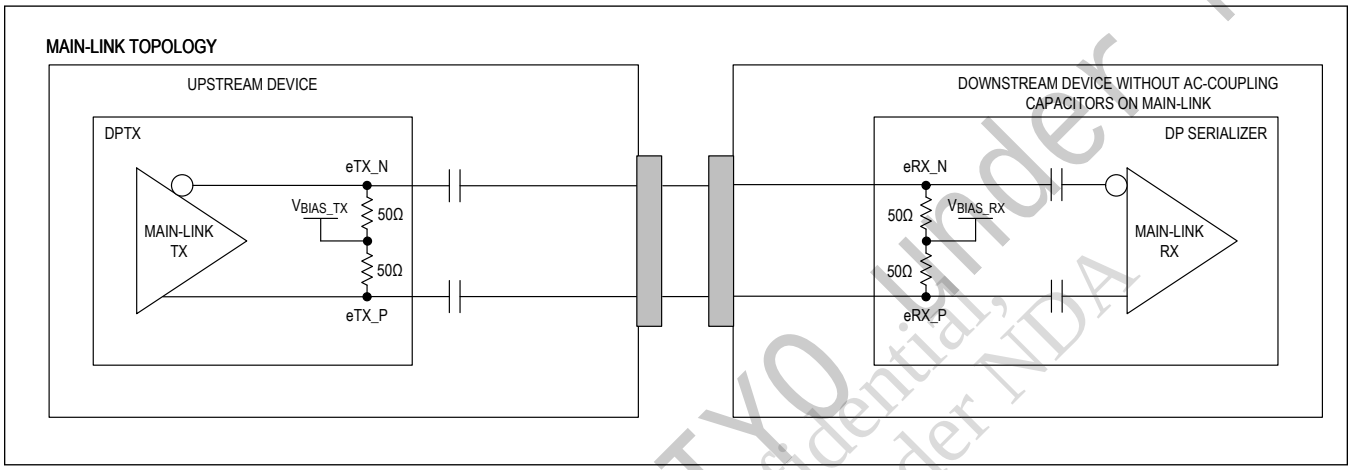

Figure 21. Main-Link Differential Pair

Spread-Spectrum

Spread Spectrum Modulation of the DP main link signal pairs is supported with a downspread of up to 0.5% at a modulation frequency of 30 to 33kHz.

DP Content Protection

HDCP decryption is not supported in the DP receiver. However, each GMSL link supports HDCP1.4 encryption of video streams (MAX96783 only).

AUX Channel

AUX channel read and write capabilities are supported in both native and I^2C over AUX modes.

DP Messaging AUX client functions are not supported.

AUX-Channel Differential Pair

The MAX96781/MAX96783 support both DP and eDP AUX Channel interface configurations, however they do not monitor AUX_CH_P and AUX_CH_N common mode voltage for source device Hot Plug/Unplug and powered/unpowered detection. Therefore, it is recommended that only the eDP AUX-Channel Differential Pair topology is required. There may however be special devices like test equipment, etc,. that need the DP AUX Channel configuration for one reason or another.

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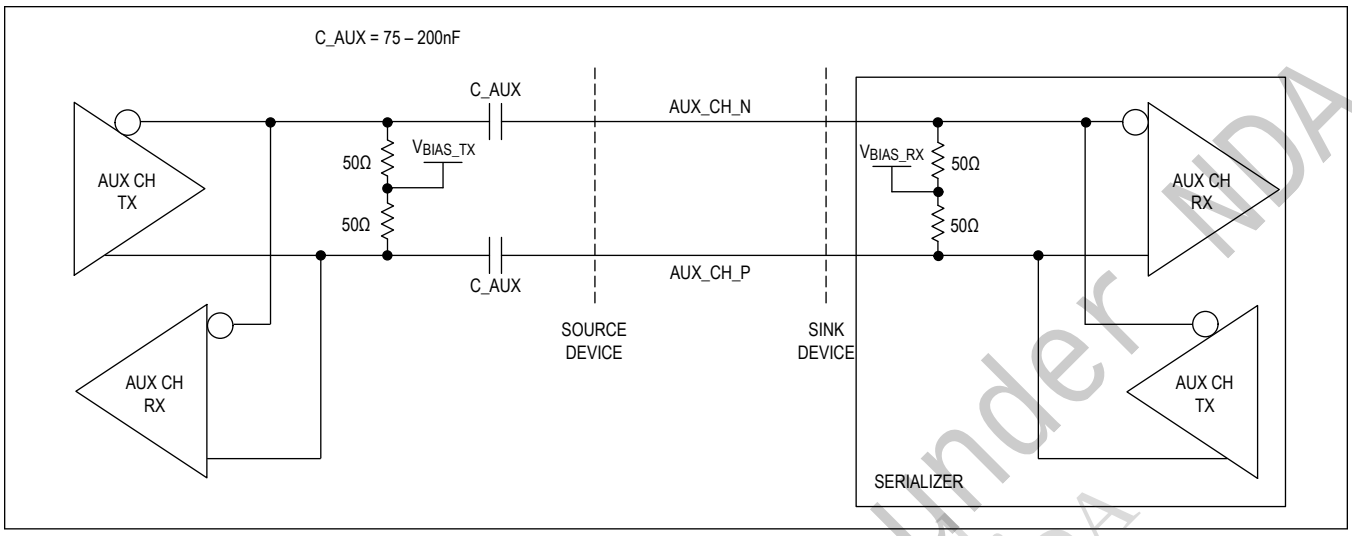

Figure 22. eDP AUX-Channel Differential Pair

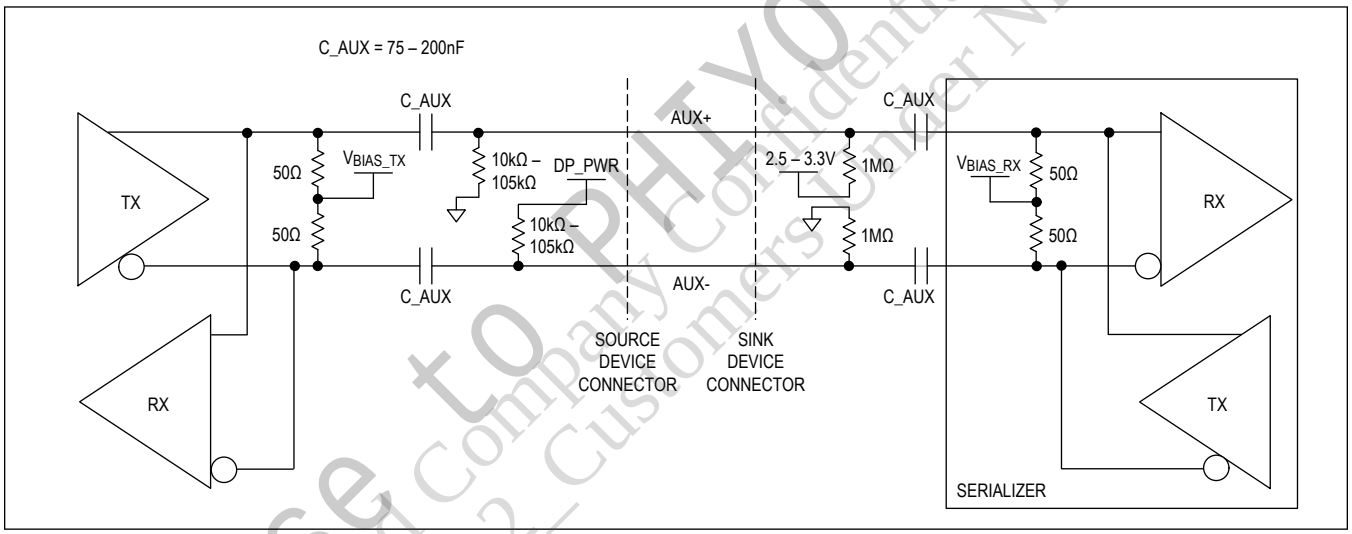

Figure 23. DP AUX-Channel Differential Pair

HPD Interface

The HPD pin supports both the hot plug detect and IRQ functions. The HPD signal is asserted by the serializer whenever it is connected to its main power supply. During normal operation, the serializer may notify a link status change, for example, loss of synchronization, by toggling the HPD signal for interrupt request signaling.

Notes:

HPD pin output logic levels are referenced to V_{DDIO}. For the most robust operation, use the same supply voltage for the DP source and the serializer V_{DDIO}. If different supply voltages are used, a level-shifting circuit may be required.

Extended Display Identification Data (EDID)

Extended Display Identification Data (EDID) is a standard communication method used by the DisplayPort to describe the video resolution and timings supported by a display. Without this data, the default resolution of 640 x 480 is all that can be supported. The MAX96781/MAX96783 devices contain two different EDID tables (read only and programmable) internal to the part. A user-supplied external source can provide the EDID table through one of the pass-through I²C

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ports. This is shown in Figure 24. The EDID feature is useful in SST mode applications when connecting to standard DP sources like laptops, in which the serializer appears as a standard DisplayPort display to the DP source. EDID is not needed for embedded automotive applications.

Three EDID sources can feed the I^{2}C over the AUX channel.

1. Internal ROM with a preprogrammed EDID table containing timing information for 1920 x 1080 full HD with standard VESA timing.
2. Programmable RAM, with an address range 0x6500 to 0x65FF.
3. Pass-through control-channel pins (PT1 or PT2).

Contact the factory for details regarding configuration and use of the various EDID functions.

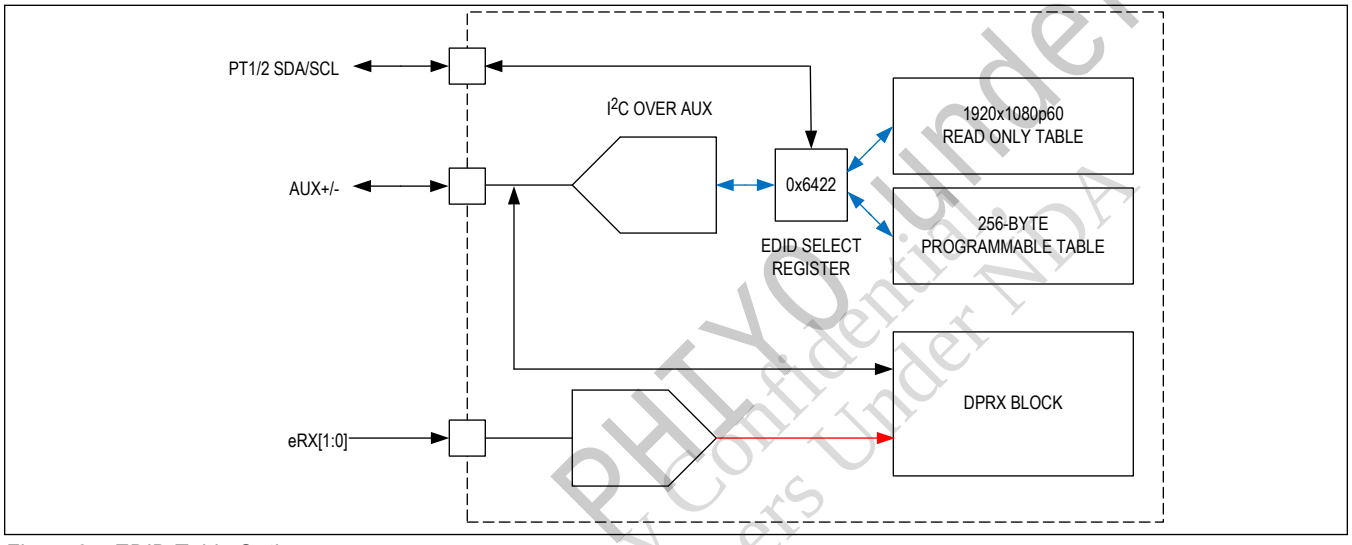

Figure 24. EDID Table Options

GMSL2 Protocol and Physical Layer

GMSL2 Protocol

GMSL2 is a fixed-rate transmission medium that is designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or external reference frequency. The link clock does not have any relation to the video pixel clock.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth.

The same data protocol is used on forward and reverse channels and for both video (forward path only) and control-channel data.

GMSL2 mode utilizes NRZ modulation at forward link rates of 6 and 3Gbps.

GMSL Physical Layer

ADI's GMSL2 family of serial links have transmitter and receiver capability enabled simultaneously, allowing full-duplex operation on a single wire. A single cable between the serializer and deserializer delivers data being transmitted from each end of the link. Forward transmission is data being sent from the serializer to the deserializer. Reverse transmission is data being sent from the deserializer to the serializer.

Available forward-rate options for both coax and STP links are fixed at 6Gbps and 3Gbps. If both links are being used in

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GMSL2 mode, the link rates must be set to the same value, with 6Gbps having priority.

GMSL Link Configurations

The MAX96781/MAX96783 devices have independent GMSL link-A/-B configuration options. The CFG1 (Link-A) and CFG2 (Link-B) latch on power-up pin functions set both links independently at power-up. Programmed GMSL2 settings include STP or Coax and 3Gbps or 6Gbps link operation. Programmed GMSL1 settings include STP or Coax and HIM or non-HIM mode.

The options provided by the CFG1 and CFG2 pins are detailed in Table 12 and Table 13.

The CFG1 and CFG2 settings can be overwritten via post-power-up register writes.

Dual-Link Mode

The MAX96781/MAX96783 devices support GMSL2 dual-link mode enabling a total of 12Gbps forward bandwidth (430MHz PCLK) with a compatible GMSL2 deserializer. In dual-link mode, the packet scheduler routes packets to both links to evenly distribute the bandwidth utilization. The video and control data is reconstructed by the deserializer.

Line Fault

GMSL serializers include a novel line-fault detection circuit. It detects and reports open-circuit, short-to-battery, short-to-ground, and line-to-line short conditions. The line fault monitor requires external resistors R_{EXT1} and R_{PD} in Coax mode and R_{EXT1}, R_{EXT2} and R_{PD} in STP mode as detailed in the following sections.

The line-fault monitor is disabled by default. Configuration options and status are available through registers. If unmasked, a line-fault condition asserts ERRB. Line-fault detection cannot be used in applications with power over coax (POC) or AC-coupled grounds.

The line-fault monitor pins offer flexible connection and programming in either Coax or STP applications.

Figure 25 illustrates the two configuration options for the location of line-fault detection. The local-side serializer configuration is typically used for display links and Local-Side deserializer Configuration is typically used for camera links. Both schemes can be used in either Coax or STP mode.

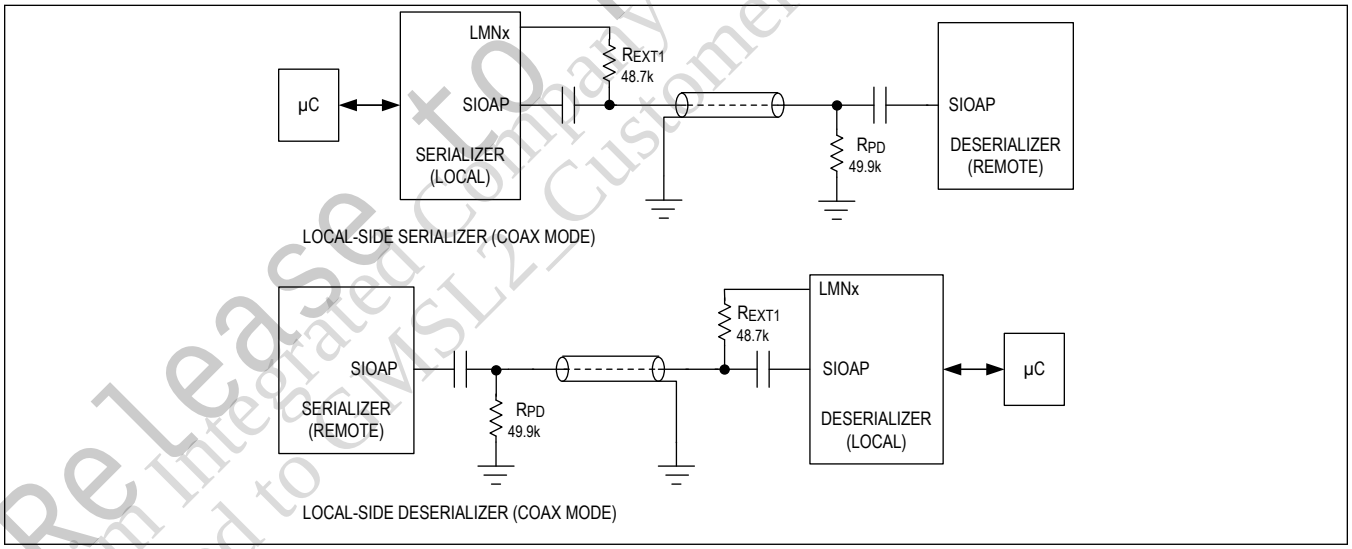

Figure 25. Line Fault Detection Location Options

Coax Mode

In Coax applications, any LMNx pin may be used. The MAX96781/MAX96783 source the line fault monitor. The serializer board requires a single 48.7kΩ resistor (R_{EXT1}) connected directly from any of the LMNx pins to the serial link. R_{EXT2} is not used in Coax applications. The deserializer end of the serial link requires a 49.9kΩ resistor (R_{PD}) connected from the serial link to GND.

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Table 4. Coax Mode Line Fault Configuration Options

SIGNAL	SIOA	SIOB
Line-Fault Pin	LMNx (Any LMN pin)	LMNx (Any LMN pin)
R_{EXT1}	48.7kΩ	48.7kΩ

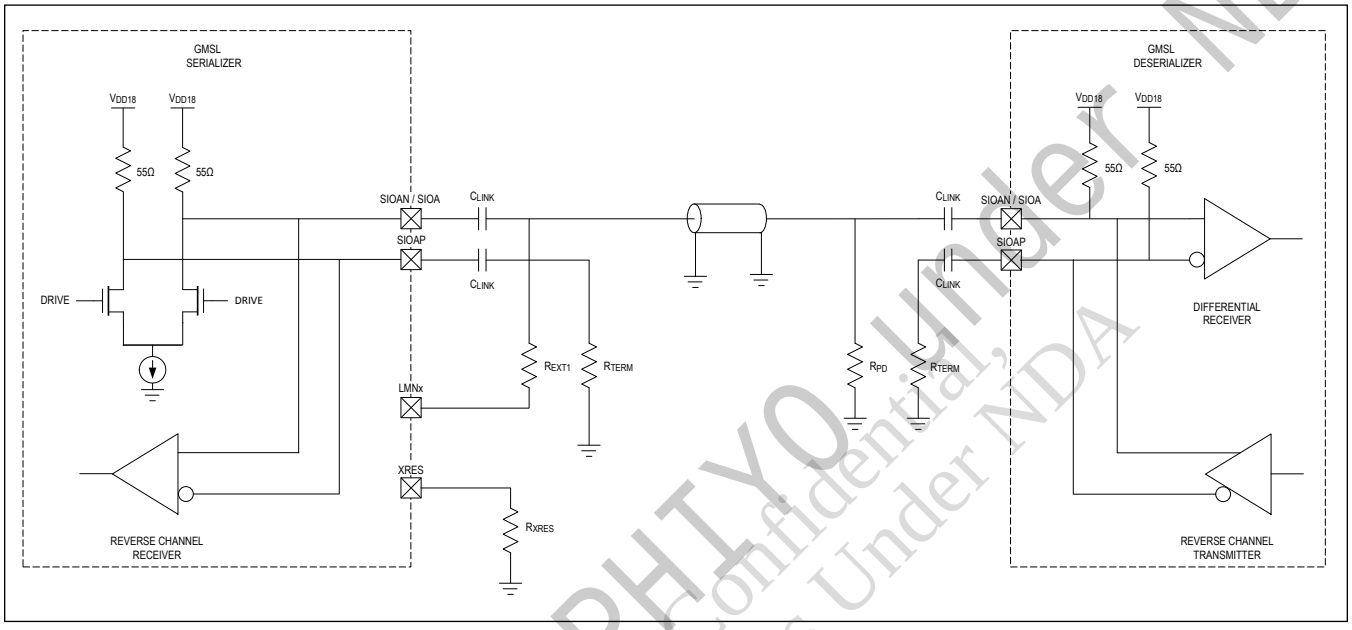

Figure 26. Typical GMSL Link Application Circuit for Coax Cable

STP Mode

If the serial link is operating in twisted-pair mode, it is recommended to connect one line to an even-numbered pin (LMN0/2) and the other line to an odd-numbered pin (LMN1/3) on the local side. For reliable line-fault detection, the even-numbered pins (i.e., LMN0 and LMN2) must be connected to the line using a 42.2kΩ resistor (R_{EXT2}); the odd-numbered pins (i.e., LMN1 and LMN3) must use a 48.7kΩ resistor (R_{EXT1}) to connect to the line (as with single-ended mode). On the remote side, both lines require a 49.9kΩ resistor (R_{PD}) connected to GND.

For full operation of line-fault detection in twisted-pair applications, ensure that either LMN0/1 or LMN2/3 pairs are used. This pairing is required for proper operation of the line-to-line short detection; however, this pairing is not necessary for the detection of other fault conditions.

Line Fault Pair #1 (LMN0/LMN1) Resistor Values and Connection Choices in STP Mode

Table 5. STP Mode Line Fault Configuration Options for LMN0/LMN1

LINE FAULT PAIR #1: LMN0 AND LMN1	SIOAN/SIOA	SIOAP
Option #1	LMN0: R_{EXT2} = 42.2kΩ to serial link	LMN1: R_{EXT1} = 48.7kΩ to serial link
Option #2	LMN1: R_{EXT1} = 48.7kΩ to serial link	LMN0: R_{EXT2} = 42.2kΩ to serial link

Line Fault Pair #2 (LMN2/LMN3) Resistor Values and Connection Choices in STP Mode

Table 6. STP Mode Line Fault Configuration Options for LMN2/LMN3

LINE FAULT PAIR #2: LMN2 AND LMN3	SIOAN/SIOA	SIOAP
Option #1	LMN2: R_{EXT2} = 42.2kΩ to serial link	LMN3: R_{EXT1} = 48.7kΩ to serial link
Option #2	LMN3: R_{EXT1} = 48.7kΩ to serial link	LMN2: R_{EXT2} = 42.2kΩ to serial link

Identical options apply to the GMSL B-port (SIOBP/SIOB and SIOBN pins)

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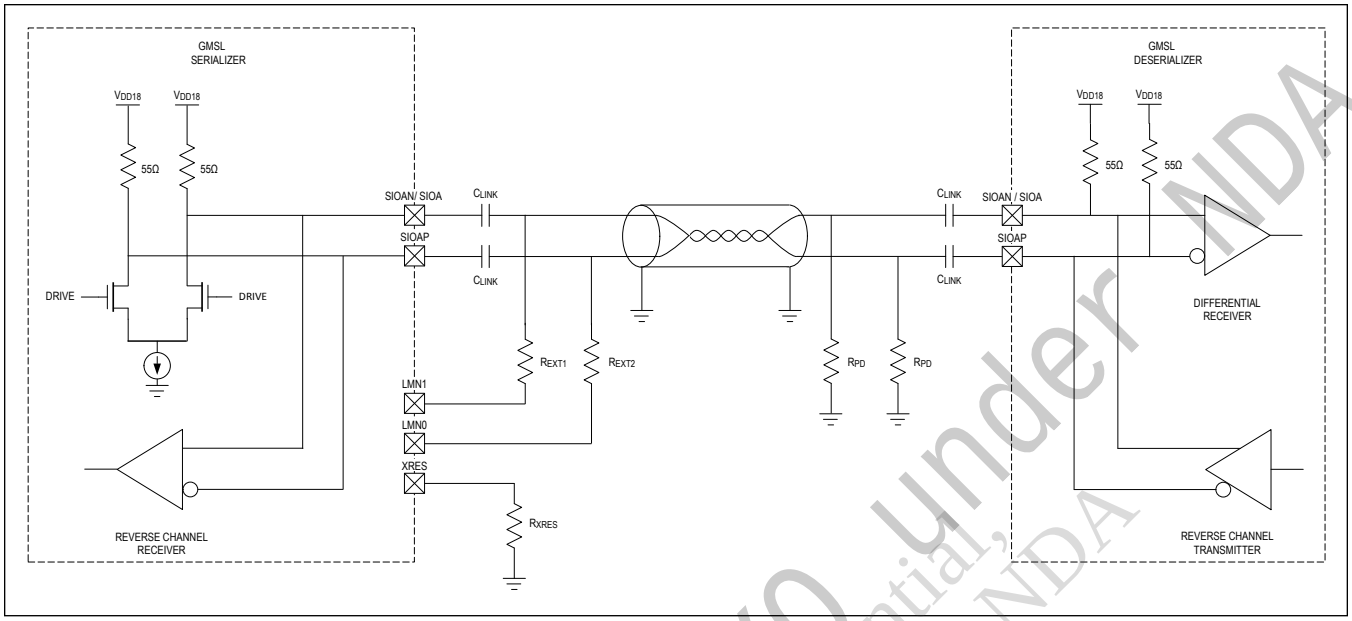

Figure 27. Typical GMSL Link Application Circuit for Twisted Pair (Line Fault Pair #1: LMN0 and LMN1, Option #2)

Line Fault in AC-Coupled Ground Applications

Use of the line fault function is NOT recommended in applications with a floating cable shield. Contact the factory for details.

GMSL Link Polarity Inversion

Both STP and COAX operating modes provide a polarity swap option that can be used for engineering purposes in prototype systems to maximize flexibility. It is, however, not possible to swap GMSL pins in production systems because GMSL2 channel specification compliance can only be guaranteed when the default polarities are used. Contact the factory for support.

Cabling Options

GMSL2 devices support 50Ω coax, 100Ω shielded twisted pair (STP), or 100Ω shielded parallel pair (SPP) cabling. Cable attenuation and return loss characteristics must stay within the requirements of the GMSL2 channel specification to achieve robust full-duplex link performance. These requirements vary with selected link rate. The available link rates and GMSL2's adaptive equalization enable support of a wide range of cabling options.

Coax or STP operation of the GMSL links is determined by the voltage at the CFG1 (Link-A) and CFG2 (Link-B) pins at power-up. See Table 11 and Table 12. This setting determines which cabling option applies. The operating mode can also be configured after power-up by appropriate register configuration. **In coax mode, use only the SIOAN/SIOA or SIOBP/SIOB pins.** AC-couple and terminate the unused SIOAP or SIOBN pin using the series connection of a 100nF capacitor and a 49.9Ω resistor. In STP configuration, both the non-inverted (SIOAP and SIOBP/SIOB) and inverted (SIOAN/SIOA or SIOBN) pins are enabled by default.

Maximum cable length is limited by the frequency-dependent attenuation of the cable. Additionally, PCB and inline connectors degrade the return loss characteristic of the cable assembly. The GMSL2 channel specifications allow two inline connectors and provide detailed requirements for cable attenuation and return loss, as well as insertion loss and return loss requirements for PCB traces. In general, any physical channel implementation that is compliant with the GMSL2 channel specification can be used with reliable results. Contact factory to receive the GMSL2 channel specification document.

A 100nF AC-coupling capacitor is used for a GMSL2 link or a GMSL1 link in High Immunity Mode (HIM). A 220nF AC-coupling capacitor is required for non-HIM GMSL1 links. A 220nF coupling capacitor can be used in designs that must support mixed GMSL2/GMSL1 HIM and GMSL1 non-HIM display modules.

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Spread-Spectrum Clocking

GMSL links provide exceptional EMI performance. Optional spread-spectrum clocking (SSC) is available to mitigate electromagnetic interference emitted from devices and inter-connections and provide additional margin. SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to ±1250ppm from the center frequency.

AC-Coupled Cable Ground Applications

Twisted pair links for GMSL channels can experience static or dynamic ground voltage shifts between one Electronic Control Unit (ECU) or display and other ECUs in a vehicle system. Static differences in ground voltage causes current to flow in the cable shield if it is grounded at both ends. In the case of a failure, such as a ground disconnect, the shield may carry the current of both the ECU1 and ECU2. This can result in amperes of current in the shield. The concept is illustrated in Figure 28.

To avoid the impacts this can have on EMI, EMC, and signal integrity, there are specific recommendations for AC-coupled cable ground applications including component selection and layout recommendations for a circuit that reduces the impedance between the shield and digital (ECU) ground. Following these recommendations provides a return path for the offset current that best mitigates the negative impacts of the effect. Contact the factory for associated application notes and technical support.

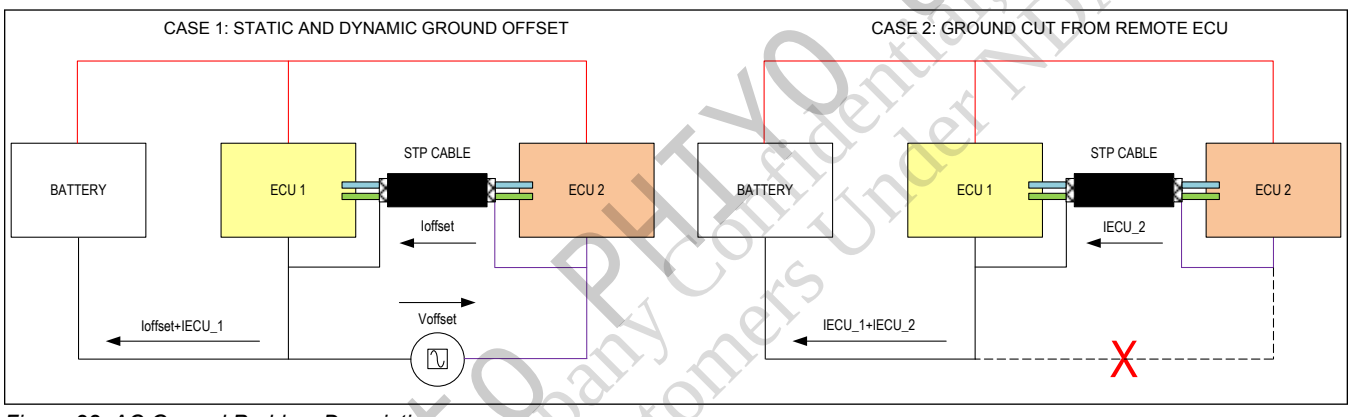

Figure 28. AC Ground Problem Description

GMSL Bandwidth Sharing

The GMSL forward bandwidth is shared between video, the I^{2}C/UART control channel, pass-through I^{2}C/UARTs, I^{2}S/TDM audio, SPI, and GPIOs, plus various protocol-specific data exchanges (i.e. info frames, sync, and acknowledgements). The reverse-channel bandwidth is also shared with all of the above, with the exception of video packets.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

Link bandwidth is shared flexibly between the various communication channels requesting the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation: if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol fulfills this sharing requirement. The maximum packet size is limited to prevent a single channel from monopolizing the link bandwidth and to ensure other channels are served.

The video and control-channel packets can be assigned one of four priority levels: low, normal, high, or urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with stringent latency requirements can be assigned an increased priority.

GMSL Bandwidth Calculations

The GMSL2 forward link has a fixed link rate of 3Gbps or 6Gbps. The reverse-link rate is fixed at 187.5Mbps. The GMSL2 protocol overhead is roughly 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

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The user must ensure that the worst-case use cases do not exceed the available throughput of the forward and reverse links. ADI's evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that can be used for initial bandwidth requirement estimates. ADI also has other tools that are useful for calculating link bandwidth utilization. It is recommended that users consult the factory for high bandwidth use cases to ensure error-free performance.

Table 7 provides accurate estimates of the bandwidth utilization for each of the communication channels.

GMSL1 bandwidth is directly related to the video PCLK and is either PCLK x 30 or PCLK x 40, depending on the setting of BWS.

Table 7. Forward and Reverse Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Display Video (Forward Path Only)	PCLK x (bpp + 0.5 + packet_CRC) x 10/9 x 2048/2047
I^2C	13 to 40 x I2C clock rate
UART	6 x UART bit rate
SPI	1.7 to 3.1 x SPI rate, depending on SPI byte length
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled
I^2S/TDM	sample_rate x 20 x (roundup(channel_cnt x sample_depth/18 + 0.5) + 2)

Definitions:

PCLK = Total Horizontal pixels x total Vertical lines x frame rate. Horizontal includes blanking pixels and Vertical includes blanking lines.

bpp = bits per pixel (24 for RGB888)

packet_CRC = 0.5 if packet CRC is enabled, 0 if not enabled. Packet CRC is disabled by default.

sample_rate = audio sample rate (samples per second)

channel_cnt = number of audio channels

sample_depth = bits per sample per audio channel (must be the same for all channels)

Video Pipe Details

Video Path Configuration

The MAX96781/MAX96783 video path details are as shown below in Figure 29. The high level details are as follows where the circled numbers in the diagram are outlined below accordingly.

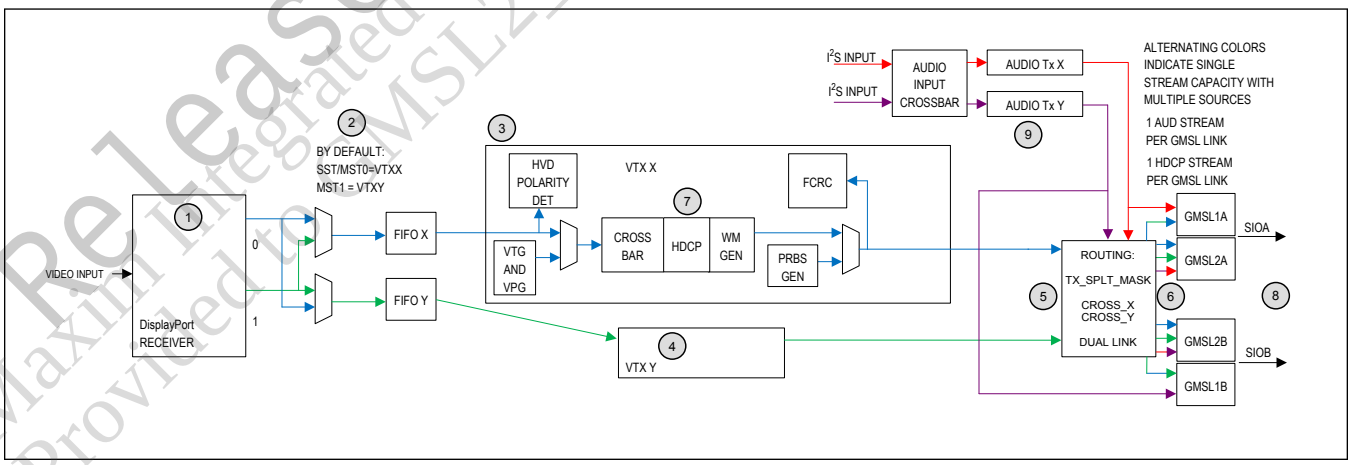

Figure 29. Video and Audio Signal Paths

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1. DisplayPort input block:
    - MST or SST
    - MST number: 1 or 2
    - Number of Lanes: 1 or 2
    - Lane Speeds: 2.7G, 5.4G, 8.1G
2. DP Receiver has 2 output ports, labeled 0 and 1. Each SST or MST stream can be routed to any selected DP output port.
    - By default, SST and 1xMST modes route video to pipe X while in 2-MST mode stream 0 is routed to pipe X and stream 1 is routed to pipe Y
    - Streams can be duplicated on multiple ports
3. Video Pipeline features such as Crossbar, WM, HDCP, VTG, and PRBS are disabled by default and video passes through unchanged.
4. Details shown in Video Pipeline X are duplicated for pipe Y.
5. Each video stream can be sent to GMSL Link A, GMSL Link B, both links simultaneously, or to a single dual link interconnect
6. Each GMSL2 link can carry up to 2 video streams.
7. Each link supports a single HDCP encrypted stream. Dual link applications can support a single HDCP stream.
8. GMSL Video output path
    - GMSL links A and B can be independently configured for GMSL1 or GMSL2 operation. In GMSL2 mode, both links are configured for the same speed. In GMSL1 mode, all common parameters are independent for each link
    - GMSL2 modes supported: 3Gbps or 6Gbps
    - GMSL1 modes supported: 27b (HIBW) or 32b (BWS=1)
9. Audio
    - Two forward audio channels sourced from two independent I^2S ports, each of which can route to either or both audio TX blocks.
    - Two Audio Tx blocks, suffixed X and Y. Each can be connected to Link A and/or B
    - Each link supports one audio stream in either GMSL1 or GMSL2 mode.
    - Audio can be HDCP encrypted

Video-Line CRC

A CRC32 polynomial is used to generate an optional 32-bit code at the end of each DE or HS pulse. This code is transferred to the receiver side using info frames. The CRC checker generates the same code on the receiver side and checks if the generated and received CRC codes are the same. If not, it asserts an error. The CRC check is done at every falling edge of DE on the receiver side, even if the info frame is not received.

End-to-End Video Line CRC

The data path from the serializer DisplayPort input to the GMSL deserializer is CRC-protected for data integrity. For safety purposes and to meet certain Automotive Safety Integrity Levels (ASIL), data is protected in three stages:

1. The DP receiver has an 8b/10b coding error detection mechanism for the received input. Errors can be reported to the interrupt (ERRB) output.
2. The signal path from DP receiver output to the GMSL link is covered by a CRC-protection mechanism. This starts from the output of the DP Receiver up to the input of video transmit block. It covers the large line memories. It is a video frame-based CRC. The CRC for each video frame is calculated at the output of the DP receiver and then recalculated before the video transmit block. The two CRC results are compared, and errors can be reported to the interrupt (ERRB) output.
3. Finally, the video data path over the GMSL link is covered by line-CRC, packet CRC, and frame-CRC mechanisms that report errors detected by the deserializer. Interrupts from the deserializer can be communicated to the serializer using GPIO tunnels.

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Video-Timing Generator

The video-timing generator (VTG) is an auxiliary block that can substitute HS, VS, and DE signals with the signals that it generates as defined by the configuration registers. The VTG can generate almost any type of SYNC-signal pattern using either an internally generated clock or the PCLK of the incoming video. Each video pipe includes a dedicated VTG.

Video-Pattern Generator

The video pattern generator (VPG) is an auxiliary block that can be used to replace the incoming video stream with a test pattern. The VPG can generate an RGB888 test pattern at any resolution with internally generated clocks/timing from the VTG or it can generate a test pattern using the clock and timing information of the incoming video stream. Each video pipe includes a dedicated VPG. The VPG and VTG can be used together to generate a video test pattern with any desired timing without the need to have a DP source connected.

Video Color Crossbar

Data from the video input is captured and optionally multiplexed with the generated patterns from the VTG or VPG. Final data goes into a crossbar multiplexer that allows any input bit to be mapped to any output bit using the configuration registers. The crossbar can be used to reorder the color and sync signals.

Each video pipe has a separate video crossbar, and each crossbar has its own configuration registers. If multiple crossbars exist, configuration register names have _X and _Y extensions indicating the video pipe they belong to.

It is possible to have one crossbar input connected to multiple outputs.

Watermark Generator

The watermarking block allows users to detect a frozen-frame failure in a frame-based processing system between the generator and detector. This feature is specifically targeted to detect frozen frames caused by SoCs in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector.

The watermark generator inserts a time-varying watermark that is highly redundant and robust to image processing. The watermark detector looks for this time-varying watermark, and failure to detect all the generated watermarks indicates a frozen-frame failure between the generator and detector. Upon detection of this error condition, the watermark detector can generate an interrupt and/or blank the output video returning the display to a safe-state in less than 500ms.

MAX96781/MAX96783 serializers provide a dedicated watermark generator in each video pipe. A downstream GMSL device with a watermark detector is required to enable the watermark functionality.

PRBS

The MAX96781/MAX96783 devices include both Video and Audio PRBS generators to support diagnostics of the audio and video channels.

Video PRBS

The video channel has a PRBS generator in the serializer and a PRBS checker in the deserializer for testing the video channel operation. The video PRBS generator can utilize the recovered PCLK from the DP input or an internally generated PCLK. Note that all link bandwidth is not used by the video channel alone in GMSL2 mode, so it is possible to have a bit error on the link which does not cause a video PRBS error.

Audio PRBS

The audio channel includes a PRBS generator on the transmitter side and a checker at the receiver side for testing the audio channel operation. The audio PRBS generator can operate using the incoming I^2S SCK and WS signals or using an internally generated reference clock. The detected audio-channel bit errors are reported through a status register at the receiver.

Full-Frame CRC

A frame CRC signature is generated at the end of each video frame and the signature is reported in registers on both ends of the link. Frame CRC value is also transmitted to the deserializer side using info frames (supported only by select deserializers). The frame CRC value received from serializer side is continuously compared to the CRC value generated at the deserializer side and an interrupt is set if there is a mismatch.

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HDCP (High-Bandwidth Digital Content Protection)

High-bandwidth digital content protection (HDCP) is an encryption scheme to protect digital audio and digital video content in various protocols. The MAX96783 includes two independent HDCP v1.4 engines to support HDCP on both links. Both GMSL2 and GMSL1 links support HDCP.

When HDCP is enabled, it automatically performs authentication and link integrity checks (GMSL2 only) through a dedicated control channel over the GMSL link. HDCP interrupts can be generated and status registers provide status of authentication progress, indicating success and a ready state to the upstream video source.

Each HDCP device has a factory-programmed unique device ID called a key selection vector (KSV) and associated private keys. They are licensed from DCP LLC.

Some GMSL2 devices include limitations regarding the supported HS timing when HDCP is enabled. Refer to the errata of the paired deserializer to confirm any limitations and ensure that the video timing used is compliant.

HDCP operation is dependent on the GMSL operating mode:

- GMSL1:
  - HDCP control uses manual mode with an external ECU driving the authentication and control via the main control channel.
  - GMSL1 mode does not support establishing HDCP operation automatically.
  - HDCP1.3 and HDCP1.4 are functionally identical and compatible in legacy GMSL1 and GMSL2 devices.
- GMSL2:
  - Includes internal controller to automate HDCP1.4 operation. This function is referred to as Auto HDCP1.4 or AHDCP.
  - It is also possible to configure and control the HDCP1.4 function without the auto controller and control HDCP1.4 manually via an external ECU like that in GMSL1 devices via the main control channel interface.
  - GMSL2 devices operated in GMSL1 mode must use manual GMSL1 HDCP control. AHDCP is only supported in GMSL2 operating mode.

HDCP and GMSL Link Configurations

Each GMSL1 or GMSL2 link can support a single HDCP encrypted video stream, and HDCP can be configured independently for each video pipe or GMSL link.

Mixed GMSL1/GMSL2 operation with HDCP on one or both links is supported.

GMSL2 dual link supports a single HDCP encrypted video stream.

DisplayPort HDCP Repeater Support

Given that HDCP decryption is not supported in the DP receiver the devices cannot be configured as HDCP repeaters. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits on one or more downstream links.

Automatic HDCP Operation

The MAX96783 devices have an automatic HDCP feature that fully automates GMSL link HDCP1.4 operation without requiring external ECU involvement. Authentication and link-integrity checks are done by hardware using a dedicated control channel over the GMSL link.

GMSL HDCP1.4 has an optional fast mode to perform a link-integrity check every frame.

Automatic HDCP is only supported when operating in GMSL2 mode.

Minimum Blanking and Other Video Limits

The MAX96781/MAX96783 support reduced blanking video timing parameters as specified in VESA Coordinated Video Timings Version 1.2, Reduced Blanking Timing Version 2.

Contact the factory regarding video timings with more stringent parameters than those specified in the VESA standard.

Video Timing Signal Outputs

The MAX96781/MAX96783 device can output video stream PCLK, HS, VS and DE timing signals on MFP22-MFP25.

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Timing signal outputs are enabled by programming the HVD_OUT_EN register. The specific video stream's timing to output and the video path stage of the video stream within the signal path can be selected via the DEBUG_EXTRA register. It is recommended that the edge rates of the timing outputs be reduced when outputting the timing signals.

Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL serial link simultaneously with high-speed video data. All GMSL2 devices support the following interfaces:

- Main I²C/UART (internal access)
- Pass-Through I²C/UART
- SPI
- GPIO
- I²S/TDM Audio

Data from all these interfaces tunnel through the GMSL link, but it is only through the main I²C /UART interface that the GMSL device registers can be accessed and configured.

The side channel, with its various interfaces, is accessed using multifunction GPIO pins (MFPs). Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit on the number of pins available on a given device, not all interfaces can be simultaneously supported. See Table 19 and the *Pin Description* section for default and alternate multifunction pin functions, as well as available combinations of interfaces.

Main I²C/UART

The main I²C/UART is located on the SDA_RX and SCL_TX pins of each GMSL device. The I²C (SDA, SCL) or UART (Tx, Rx) interface is selected by the CFG0 configuration pin state at power-up (see Table 11). The selected interface provides master access to GMSL device registers, as well as peripheral device registers, from either end of the link.

The master µC can reside on either end of the link (usually the serializer side for display applications and the deserializer side for camera applications). The MAX96781/MAX96783 support dual master µC controllers, provided that software arbitration (such as token passing) is used to prevent packet collisions. The control channel allows only one master µC to communicate at a time. Programming DIS_REM_CC=1 disables a remote µC from accessing the local registers. The status of pin DIS_REM_CC is latched at power-up. However, the state can be programmed using bit DIS_REM_CC after power-up.

To configure peripheral devices over the link, the GMSL serializer and deserializer must use the same control-channel interface (both I²C or both UART). Unlike legacy GMSL1 devices, there is no I²C-to-UART conversion capability. I²C/UART outputs are open-drain and require appropriately sized external pullup resistors for proper operation.

For detailed main-channel programming information, see the *Applications Information* section of this datasheet.

Multimaster I²C Operation

When a MAX96781/MAX96783 is connected to more than one deserializer in splitter mode, the MAX96781/MAX96783 can arbitrate and process I²C packets from I²C masters (ECUs) connected to each deserializer. The I²C packet from each deserializer-side ECU is processed in the order it is received and the non-selected I²C masters are put on hold by clock stretching by the respective deserializer.

Multimaster I²C operation is available on the Main I²C channel and pass-through channels.

Main I²C/UART Control Channel CRC

For improved ASIL-B functional safety requirements at the system level, there needs to be a mechanism to prevent hardware faults or random errors from miss-configuring the device. Therefore, optional CRC protection can be added to I²C and UART transactions. When CRC protection is enabled, the MAX96781/MAX96783 I²C/UART slave controller will expect and validate a CRC-8 byte for all communication messages to maintain data integrity. This ensures the proper write data is received and the device is configured properly.

For each serializer or deserializer device, there is a single counter incremented for both write and read transactions. For a system with both a serializer and deserializer, each of the two devices should keep their own counter. The device's counter will increment only when the ECU transaction is intended for that particular device and the I²C device address matches that device. Therefore, the ECU should maintain separate transaction counters for each serializer and

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deserializer and send the appropriate counter value when writing to each device.

By default, I^{2}C/UART CRC and Message Counter features are disabled. Legacy I^{2}C/UART packet format is the default. When desired, these functions can be enabled by a register write using the legacy packet format. All subsequent communication will then use the new CRC-protected format.

Further details of this functionality are provided in the *Applications Information* section.

Control Register CRC

Control Register CRC is a functional safety feature to ensure the MAX96781/MAX96783 are not placed into an undesired state through a fault.

Once the serializer is programmed, the Control and Status Register (CSR) bank is protected by a CRC calculation. After the serializer is set up through the CSR, the values should not change while the device is operating. Any change is considered a fault and ERRB is asserted if the OEN for Register CRC Flag is enabled. It is possible to exclude user-programmable register ranges that are anticipated to change during normal operation.

The serializer can report if the CSR values change due to faults (basic CRC mode). Alternatively, the CRC value can be polled by the ECU to check for changes (user-polling CRC).

Basic CRC Mode

The CRC is calculated iteratively on the CSR and a 16-bit CRC is written into registers REGCRC_MSB/REGCRC_LSB. Additionally, this value is logged internally. Periodically, the CRC is recomputed and compared with the stored value.

Procedure:

1. Functional registers are programmed.
2. Register CRC is set up:
   a. The I2C_WR_COMPUTE bit is written.
   b. The CRC_PERIOD register is written to specify the computation period as ~2ms to ~512ms.
   c. The PERIODIC_COMPUTE bit is written.
   d. The CHECK_CRC bit is written.
3. A new CRC is periodically calculated and compared with the previously-computed CRC. Any mismatches result in ERRB being indicated.

User-Polling CRC Mode

This mode calculates an incrementally changing CRC. In this case, the same CRC as above is calculated, with the addition of computing the CRC using the value from a periodically incrementing 2-bit counter. The CRC value changes periodically, with the values repeating with a period of four. This mode guards against ‘frozen’ CRC calculation logic.

Procedure:

1. Functional registers are programmed.
2. Register CRC programming is done as above.
   a. Additionally, GEN_ROLLING_CRC is set.
3. The CRC calculation is deposited in the REGCRC_MSB/LSB registers, and the ECU can periodically poll this value to check the CRC calculation is advancing as predicted.
   a. The ECU sees the CRC values repeat and knows the registers are remaining unchanged.

Note that in this mode, ERRB is not indicated as the CRC value is changing periodically, and the usage mode is to have the user poll the CRC register.

Pass-Through I^{2}C/UART

GMSL2 devices include 2 pass-through I^{2}C/UART channels (PT1 and PT2). By default, these channels do not have access to registers in either the GMSL serializer or the deserializer; they simply tunnel the I^{2}C or UART signal across the GMSL2 link. This can be useful for separating I^{2}C channels so that multimaster conflicts do not occur. Far-side peripherals can be interfaced using a different I^{2}C/UART channel than the one connected to the serializer and deserializer registers. This flexibility enables the serializer-side SOC to independently handle interrupts from remote peripherals.

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The passthrough channels support simultaneous communication to both deserializers in splitter applications.

In GMSL2 mode, the remote devices' registers can be accessed accessed directly using the main control channel only.

It is possible, by using a loop-back connection of a pass-through channel to the deserializer main channel, and disconnecting the GMSL2 link main channel with DIS_REM_CC, to interface to two identical display modules with two separate I^2C/UART controllers. In this configuration, any attached peripherals must have open-drain outputs.

In GMSL1 mode, any of the 3 I^2C/UART channels (Main, PT1, PT2) can be independently connected to the deserializer control channels for each GMSL1 PHY via bit fields LOC_CC_PT_EN.

Each of the 3 sets of physical I^2C/UART pins can be connected to any of the 3 available internal communication channels.

Further details of the I^2C/UART routing options are described in *Additional Control Channel Features*.

All I^2C/UART outputs are open drain and require appropriately-sized external pullup resistors for proper operation.

SPI

The MAX96781/MAX96783 devices additionally include an SPI master/slave interface, including two slave-select pins for peripheral control. The SPI interface enables a host SPI master on one side of the GMSL link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL devices (a GMSL device can be configured as a SPI master or slave). Normal SPI operation is a single device to device (point to point) tunnel (i.e. serializer to one deserializer and vice versa).

Although multiple SPI peripherals may be connected, it is recommended that only one be communicated with at a time. Contact factory for guidance on configuring SPI connections.

On the fly programming is possible to reconfigure the SPI master to switch between the two GMSL link outputs.

The SPI control channel may also be used in non-ACK broadcast mode to any number of SPI slave devices on both links.

I^2S/TDM Audio

The MAX96781/MAX96783 devices can support two forward (serializer to deserializer) audio channels. Supported formats are I^2S stereo and up to 8 channels of audio in TDM mode. Sample rates of 8kHz to 192kHz and sample depths of 8 to 32 bits are supported.

The device includes two independent I^2S input ports and two Audio Tx blocks, suffixed X and Y. Each audio TX block can be connected to Link A and/or link B. Replication is possible by configuring the same I^2S input to drive both Audio Tx blocks or by routing either one of the Audio Tx blocks to both links.

Each GMSL link can support transmission of one audio stream (one active Audio Tx block per link).

When HDCP encryption is enabled, it must be associated with a video stream and then optionally an audio stream. Both video and audio streams must then be decrypted by the same deserializer (i.e. encrypted audio cannot be decrypted if the deserializer is not also decrypting the associated video).

Speed Programming for SPI and I^2S

The SPI and I^2S interfaces may be used over a wide range of frequencies. The MAX96781/MAX96783 provide flexible GPIO speed programming to maintain timing margins while minimizing radiated EMI.

Table 8 and Table 9 provide guidance on recommended speed settings for various I^2S and SPI operating frequencies and V_{DDIO} supply voltages. See Table 20 for GPIO pin speed programming information.

At lower frequencies, SPI data is typically latched on the opposite clock edge than the edge on which it is shifted. See Figure 8 and Figure 9. At higher frequencies, however, the data must be latched on the same edge as the shift to meet setup and hold-time requirements. Table 9 provides guidance on programming the latching clock edge.

Table 8. Recommended I^2S Pin Programming

FREQUENCY	V_{DDIO}	RECOMMENDED SPEED SETTING
< 25MHz	1.7V–2.24V	01

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Table 8. Recommended I²S Pin Programming (continued)

	2.25V–3.6V	10
≥ 25MHz	1.7V–2.24V	00
	2.25V–3.6V	01

Table 9. Recommended SPI Pin Programming

FREQUENCY	V_{DDIO}	LATCHING EDGE	RECOMMENDED SPEED SETTING
< 12.5MHz	1.7V–2.24V	Opposite from Shift	01
	2.25V–3.6V		10
≥ 12.5MHz	1.7V–2.24V	Opposite from Shift	00
	2.25V–3.6V		01

CRC Error Detection and Correction

All GMSL serializers and deserializers provide 16-bit CRC protection of control-channel data (I²C, UART, SPI, GPIOs, Audio) to enable error detection and correction for all control channel packets on the forward and reverse channels.

Automatic Repeat Request (ARQ) / Automatic Retransmission

An automatic packet retransmission method, ARQ, is employed in GMSL serializers and deserializers for audio, SPI, I²C, UART, and GPIO channels. ARQ works in conjunction with 16-bit packet CRC to detect if packets are received without errors.

The ARQ mechanism allows the transmit side to automatically retransmit packets when it does not get notification from the receiver that data has been received error free. Therefore, all corrupted or dropped packets are corrected by retransmitting them. This enables very high robustness of mission-critical control functions in the system.

Each control packet is tagged by a 4-bit sequence number that continuously increments and rolls over. The transmitter saves the last 16 packets transmitted on a certain type of communication channel. When the receiver receives a control packet, it checks that its CRC and sequence number are correct. When the correctness of both is validated, it sends back an acknowledge packet, which notifies the transmitter that the packet with a certain sequence number is correctly received.

When the transmitter does not get an acknowledge packet for a data packet with a certain sequence number, it automatically retransmits the data packet reading it from the internal packet memory. A 4-bit sequence number allows the transmitter to transmit up to 15 packets without getting any acknowledgment, enabling pipelined operation, which minimizes the effect of round-trip latency and increases the continuous available bandwidth. This retransmission process repeats until the packet is either acknowledged or a maximum number of retransmissions is reached. Upon reaching the maximum, the packet is assumed as acknowledged and is dropped from the transmission queue. The transmission window moves forward to transmit subsequent packets.

A 3-bit register is allocated to set the maximum number of retransmissions for each channel. A packet can be retransmitted up to seven times depending on the register value set in the MAX_RT register for each communication channel.

Control Channel Latencies

Table 10. Typical Control Channel Latencies

FUNCTION	FORWARD	REVERSE	NOTES
I²C	< 10µs	< 10µs	
UART	< 10µs	< 10µs	
Audio	< 100µs		For typical use cases
SPI	< 10µs	< 10µs	Round trip

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Power-Up and Link Startup

GMSL2 ICs are in power-down mode when PWDNB pin is low or when any of the power supplies are disabled. When in power-down mode, device configuration is reset to the default power-up state.

The serializer and deserializer may power up in any order. After PWDNB is released and all power supplies have settled, each device starts its power-up sequence and performs the following operations:

1. CFG pin states are latched and internal registers are set accordingly. See Table 11, Table 12, and Table 13 for details.
2. The main control channel (I^2C or UART) is functional on local side. The device registers are writable and readable.
3. The link is established based on the following settings:
   1. Single-link auto selection mode (AUTO_LINK = 1): Automatically select which PHY to use to establish a GMSL2 link by periodically trying to handshake using PHY A and PHY B.
   2. Dual-link mode (AUTO_LINK=0, LINK_CFG = 0): Establish a link using both PHYs.
   3. Splitter mode (AUTO_LINK=0, LINK_CFG = 3): Establish a link using both PHYs.
4. Each enabled PHY performs link calibration, equalizer adaptation, and data-channel locking. Both devices set their LOCK pins high.
5. The control channel is available from or to the remote side.

After the link is established, all devices can be configured. This can be done locally or remotely over the control channel by a microcontroller on either side of the link.

Configuration Pins CFG[2:0]

The CFG[2:0] pins are used to set initial register values and functional modes of the device at power-up. At power-up, the settings dictated by the voltage levels at the CFG input pins are latched. The decoded levels set initial register values and functional modes that may not be easily programmed through I^2C or UART after the device powers up. Table 11, Table 12, and Table 13 provide the exact details of how to specify the CFG[2:0] pin connections to achieve the various available operating modes.

The CFG pins are shared with MFP pins. Before the pin levels are latched, the chip does not drive these pins and external loading must be minimized.

Configuration Tables

Table 11. CFG0 Mapped Configuration

CFG0 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (Note A)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note B)		MAPPED CONFIGURATION (Note C)	
MIN (%)	TYP (%)	MAX (%)	R1 (Ω)	R2 (Ω)	I2CSEL	DEVICE ADDRESS
0.0	0.0	11.7	OPEN	10,000	I^2C	0x80
16.9	20.2	23.6	80,600	20,500		0x84
28.8	32.1	35.5	68,100	32,400		0xC0
40.7	44.0	47.4	56,200	44,200		0xC4
52.6	56.0	59.3	44,200	56,200	UART	0xC4
64.5	67.9	71.2	32,400	68,100		0xC0
76.4	79.8	83.1	20,500	80,600		0x84
88.3	100	100	10,000	OPEN		0x80

Table 12. CFG1 Mapped Configuration

CFG1 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (Note A)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note B)		LINK A MAPPED CONFIGURATION (Notes D, E)		
MIN (%)	TYP (%)	MAX (%)	R1 (Ω)	R2 (Ω)	GMSL MODE	**CXTP**	LINK CONFIGURATION
0.0	0.0	11.7	OPEN	10,000	GMSL1	Twisted Pair	HIM disabled

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Table 12. CFG1 Mapped Configuration (continued)

CFG1 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (Note A)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note B)		LINK A MAPPED CONFIGURATION (Notes D, E)		
16.9	20.2	23.6	80,600	20,500			HIM enabled
28.8	32.1	35.5	68,100	32,400		Coax	HIM disabled
40.7	44.0	47.4	56,200	44,200			HIM enabled
52.6	56.0	59.3	44,200	56,200	GMSL2	Coax	3Gbps
64.5	67.9	71.2	32,400	68,100			6Gbps
76.4	79.8	83.1	20,500	80,600		Twisted Pair	3Gbps
88.3	100	100	10,000	OPEN			6Gbps

Table 13. CFG2 Mapped Configuration

CFG2 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (Note A)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (Note B)		LINK B MAPPED CONFIGURATION (Notes D, E)		
MIN (%)	TYP (%)	MAX (%)	R1 (Ω)	R2 (Ω)	GMSL MODE	**CXTP**	LINK CONFIGURATION
0.0	0.0	11.7	OPEN	10,000	GMSL1	Twisted Pair	HIM disabled
16.9	20.2	23.6	80,600	20,500			HIM enabled
28.8	32.1	35.5	68,100	32,400		Coax	HIM disabled
40.7	44.0	47.4	56,200	44,200			HIM enabled
52.6	56.0	59.3	44,200	56,200	GMSL2	Coax	3Gbps
64.5	67.9	71.2	32,400	68,100			6Gbps
76.4	79.8	83.1	20,500	80,600		Twisted Pair	3Gbps
88.3	100	100	10,000	OPEN			6Gbps

Notes:

A) Voltage divider resistor tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG_ input voltage to exceed the maximum or minimum limits.

B) Other than the voltage divider, any load on CFG_ must be ≥ 25 x (R1 + R2). Each resistor in the voltage divider must be ≤ 100kΩ.

C) I2CSEL: I^2C or UART interface for Main Control Channel SDA_RX and SCL_TX. DEVICE ADDRESS: device address.

D) GMSL MODE: GMSL1 or GMSL2. CXTP: Serial link configured to use Coax or shielded-twisted-pair. LINK CONFIGURATION: HIM enabled or disabled for GMSL1. Link rate of 3Gbps or 6Gbps for GMSL2. In GMSL1 mode, link rate is set by the pixel clock and bandwidth controls.

E) Although CFG1 and CFG2 each include GMSL2 bit rate programming, both links must be set the same in GMSL2 mode. Internal logic will set both links to 6Gbps if either link is programmed to 6Gbps.

All configuration settings for CFG[2:0] can be over-written by register programming.

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CFG Pin Schematic

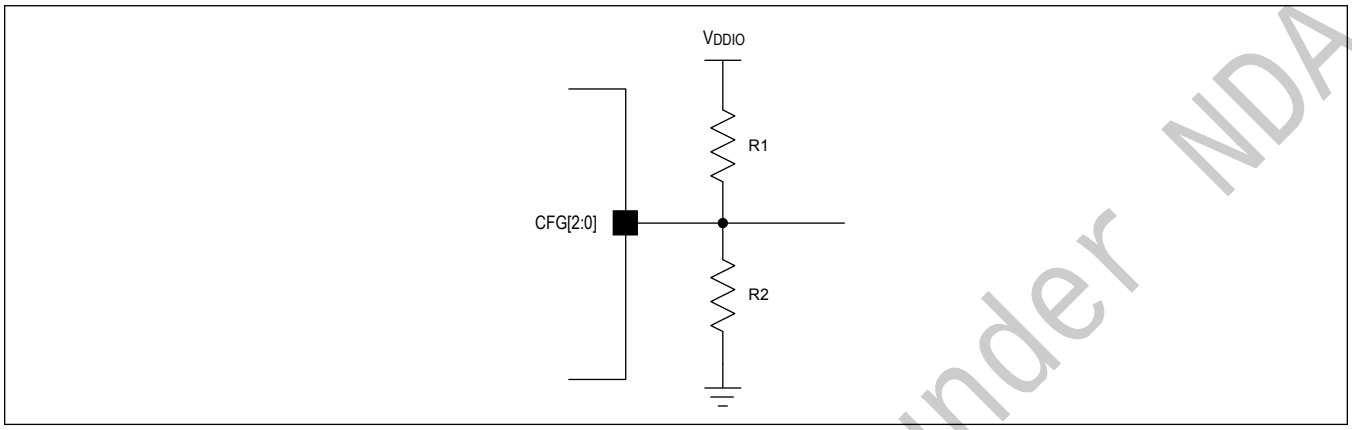

Figure 30. CFG Pin Schematic

Profile Configuration Control

The MAX96781/MAX96783 include a configuration mechanism called profile loading that can be employed to load common device configurations, such as GMSL operating mode and control channel routing, on a per link basis with minimal interaction from the ECU. Profiles can be selected from a list of predefined configuration sets or manually defined by specifying key parameters condensed into a small number of registers.

Preset Profiles

The MAX96781/MAX96783 include a group of preset configurations representing common link configurations. To specify one of the preset configuration profiles, the user must simply identify which of the profiles is most suitable for the specified application for either or both links and then trigger the profile controller to load the associated settings. Profiles for links A and B can be independently selected and loaded.

To load a profile configuration, the index of the desired profile must first be identified. Available profiles are detailed in Table 14, Table 15, and Table 16. Profile 0 is a special case. Specification of profile 0 selects the custom profile configuration for a given link as detailed in *Custom Profiles*.

After the appropriate profiles are identified, the corresponding indices are entered in the PROF_SEL_A (link A) or PROF_SEL_B (link B) registers. Finally, the profile load is initiated by informing the controller which links will utilize a profile via PROF_IN_USE_A (link A) and/or PROF_IN_USE_B (link B) and then triggering the profile load operation itself by setting EXEC_PROF=1. Profiles for both links can be loaded with a single command.

Table 14. GMSL1 Preset Profiles (high immunity mode disabled)

PROFILE	1	2	3	4	5	6
CATEGORY	GMSL1, HIM disabled, DES CC connected to SER PT I^{2}C/UART#1			GMSL1, HIM disabled, DES CC connected to SER CC		
DESCRIPTION	27-bit GMSL1, HPCLK, PT1	32-bit GMSL1, HPCLK, PT1	32-bit GMSL1, LPCLK, PT1	27-bit GMSL1, HPCLK, Main CC	32-bit GMSL1, HPCLK, Main CC	32-bit GMSL1, LPCLK, Main CC
GMSL MODE	GMSL1 HIBW=1 BWS=0 DRS=0	GMSL1 HIBW=0 BWS=1 DRS=0	GMSL1 HIBW=0 BWS=1 DRS=1	GMSL1 HIBW=1 BWS=0 DRS=0	GMSL1 HIBW=0 BWS=1 DRS=0	GMSL1 HIBW=0 BWS=1 DRS=1
REVERSE CC MODE	non-HIM	non-HIM	non-HIM	non-HIM	non-HIM	non-HIM
DESERIALIZER CC	SER PT1	SER PT1	SER PT1	SER CC	SER CC	SER CC

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Table 15. GMSL1 Preset Profiles (high immunity mode enabled)

PROFILE	7	8	9	10	11	12
CATEGORY	GMSL1, HIM enabled, DES CC connected to SER PT I²C/UART#1			GMSL1, HIM enabled, DES CC connected to SER CC		
DESCRIPTION	27-bit GMSL1, HPCLK, PT1	32-bit GMSL1, HPCLK, PT1	32-bit GMSL1, LPCLK, PT1	27-bit GMSL1, HPCLK, Main CC	32-bit GMSL1, HPCLK, Main CC	32-bit GMSL1, LPCLK, Main CC
GMSL MODE	GMSL1 HIBW=1 BWS=0 DRS=0	GMSL1 HIBW=0 BWS=1 DRS=0	GMSL1 HIBW=0 BWS=1 DRS=1	GMSL1 HIBW=1 BWS=0 DRS=0	GMSL1 HIBW=0 BWS=1 DRS=0	GMSL1 HIBW=0 BWS=1 DRS=1
REVERSE CC MODE	HIM w/o REV_FAST	HIM w/o REV_FAST	HIM w/o REV_FAST	HIM w/o REV_FAST	HIM w/o REV_FAST	HIM w/o REV_FAST
DESERIALIZER CC	SER PT1	SER PT1	SER PT1	SER CC	SER CC	SER CC

Notes:

1. HIM = high immunity mode reverse channel.
2. CC = main control channel.
3. HPCLK = high PCLK range (DRS=0) (typical PCLK ranges are described in Table 25).
4. LPCLK = low PCLK range (DRS=1) (typical PCLK ranges are described in Table 25).
5. All preset profiles enable line fault.

Table 16. GMSL2 Preset Profiles

PROFILE	17	18	19	20
DESCRIPTION	GMSL2, 3Gbps, PT1	GMSL2, 6Gbps, PT1	GMSL2, 3Gbps, Main CC	GMSL2, 6Gbps, Main CC
GMSL MODE	GMSL2 3G	GMSL2 6G	GMSL2 3G	GMSL2 6G
DESERIALIZER CC	SER PT1	SER PT1	SER CC	SER CC

Notes:

1. Using PT1 or PT2 for the deserializer main CC in GMSL2 mode requires special design considerations. Contact the factory for guidance.
2. All preset profiles enable line fault.
3. CC = main control channel.
4. When both link are configured for GMSL2 mode, the same link speed must be specified for both.

Custom Profiles

In addition to the preset configurations described in *Preset Profiles*, the profile controller also provides a custom profile configuration option. The custom profile mechanism enables individual selection of key device modes and functions for each link. To streamline setup, all parameters are combined in a pair of registers associated with each GMSL link, simultaneously maximizing flexibility and minimizing register configuration.

The parameters available for configuration in custom profiles are detailed in Table 17. Refer to the register map for configuration details. Commonly specified parameters include GMSL link operating mode, passthrough/main I²C/UART routing, and linefault. Less commonly specified parameters include sync polarity inversion and GMSL1 HV encoding.

When using both links in GMSL2 mode, the specified link rate should be the same for both links.

When routing a passthrough to the remote control channel, only PT1 **OR** PT2 should be specified as the remote control channel for a given link. The device does not support multiple passthrough ports concurrently connected to a single link's main control channel.

Special considerations must be accounted for when routing PT1 or PT2 to the remote control channel of a GMSL2 deserializer. Contact the factory for details.

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To configure a custom profile, PROF_SEL_A (link A) or PROF_SEL_B (link B) must be set to 0. This informs the profile controller that a custom profile is being used for the specified link. The available configuration options corresponding to the desired custom profile can then be specified in registers PROFILE_CFG_A_0/1 (link A) or PROFILE_CFG_B_0/1 (link B). After the custom profile is defined, it can be loaded by first setting PROF_IN_USE_A (link A) or PROF_IN_USE_B (link B) to inform the controller whether each link will use a profile and then triggering the load of the specified profiles to link A and/or link B by setting EXEC_PROF.

Table 17. Custom Profile Parameters

PARAMETER	OPTIONS
GMSL link mode	GMSL1 GMSL2
GMSL2 FWD speed	3Gbps 6Gbps
GMSL1 FWD configuration	27-bit mode, DRS=0 32-bit mode, DRS=0 32-bit mode, DRS=1 24-bit mode, DRS=0
GMSL1 REV configuration	high immunity disabled high immunity enabled
PT1 configuration	remote CC is main CC remote CC is PT1 remote CC is main CC and PT1 tunneled (GMSL2 only)
PT2 configuration	remote CC is main CC remote CC is PT2 remote CC is main CC and PT2 tunneled (GMSL2 only)
Line fault	disable line fault enable line fault
Sync polarity inversion (not typically specified)	invert syncs do not invert syncs
GMSL1 HV encoding (not typically specified)	encode HV do not encode HV

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GMSL2 Link Lock

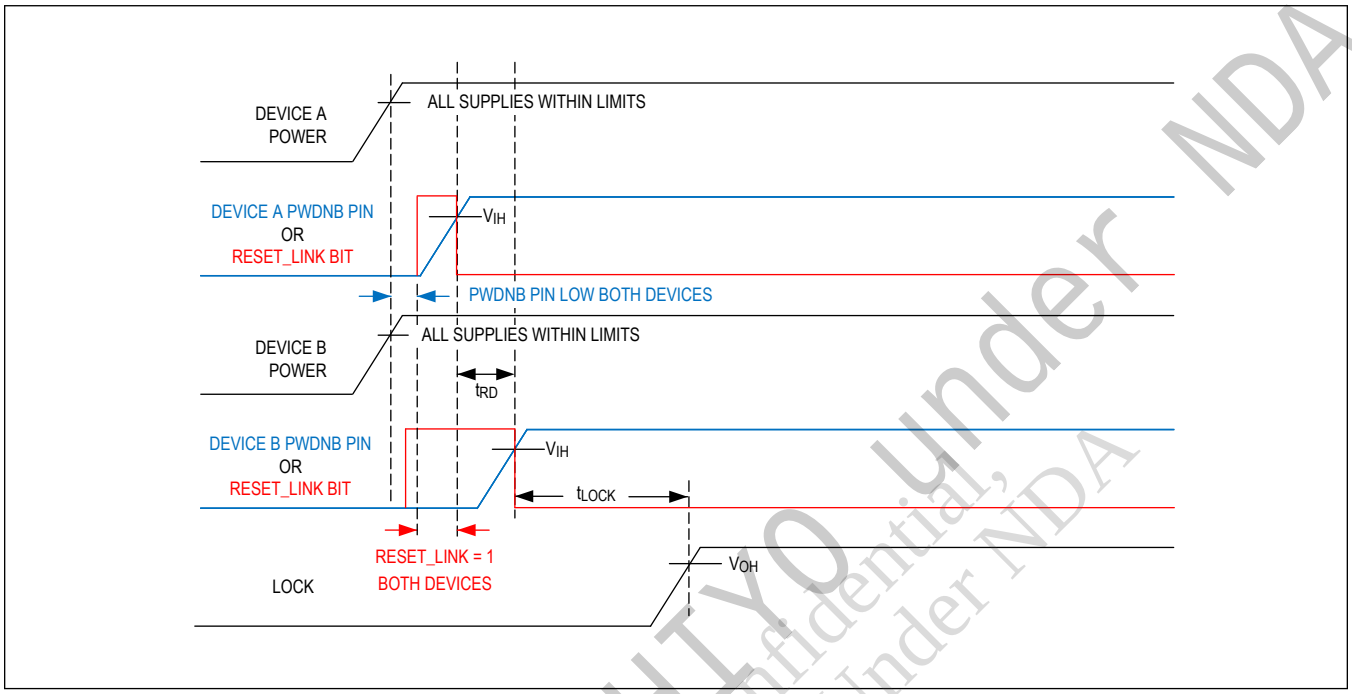

Figure 31. GMSL2 Lock Time

Figure 31 illustrates the sequence that is used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power-up or resume operation from a RESET_LINK state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I^2C/UART, SPI, GPIO, audio) can be used immediately after link lock is asserted.

The device will establish single link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in and the system is up and running. Lock is obtained with no interaction between the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

Dual-link and splitter configurations require additional user programming. For guidance on enabling these configurations and optimizing the lock time, contact the factory.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links, so a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes Regarding Lock Time:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. Lock time is measured from the later of PWDNB or RESET_LINK release in either the serializer or deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate lock, PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, RESET_LINK is assumed to be low after power-up (normal operation).
6. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices) must be less than the threshold specified in *Note 6*. Contact the factory for guidance if this timing cannot be

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guaranteed.

7. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and the deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permissible t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.
8. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This will minimize any disruptions caused by a transient loss in connectivity.

LOCK Reporting

In GMSL2 operating mode, MAX96781/MAX96783 devices can report the lock status of Link-A and/or Link-B at the LOCK pin. Lock pin behavior is configured by LOCK_CFG in REG5. Table 18 lists the available lock status reporting options. By default, the serializer asserts its lock pin when either link-A or link-B reports a locked stated (LOCK_CFG=0).

LOCK_CFG=1 should only be used in splitter or dual link configurations when the user anticipates that more than one link is locked.

In single link mode, LOCK_CFG should always be set to 0. If a value of LOCK_CFG=1 is used in single link mode, the LOCKED bit will always read back 0 because it is the combination of link A AND link B lock status, and one of those two will always be unlocked in single link mode.

For links configured in GMSL1 mode, the serializer does not report lock status.

Table 18. LOCK_CFG Register Decode Table

VALUE	DECODE
0x0	Link-A OR Link-B is locked.
0x1	Link-A AND Link-B are locked.

Device Reset

There are three general reset options available through register writes:

1. RESET_ALL resets all blocks, including all registers, digital blocks, and analog blocks. This process is similar to driving the PWDNB pin low and then high. **Note: If Sleep mode is being used, do not use RESET_ALL as it will return the device to Sleep mode.**
2. Setting RESET_LINK resets all GMSL PHY-related digital logic and the data pipeline. After this bit is set, all control registers are still accessible through local control channel. The link remains in RESET until RESET_LINK is cleared.
3. RESET_ONESHOT resets all GMSL PHY-related digital logic and the data pipeline and then automatically clears itself. This is similar to setting and clearing RESET_LINK.

Use RESET_LINK to hold the link in reset while programming registers that affect GMSL-2 link operation (i.e., TX_RATE, RX_RATE, CXTP, AUTO_LINK, LINK_CFG). After all link parameters are specified, release RESET_LINK to initiate the locking process.

Multifunction (MFP) Pin Assignments

Side-channel functions, such as pass-through I^{2}C/UART, SPI, and audio, are enabled by programming multifunction pins (MFP). Each pin has several possible functions, but only one can be used at a time. Some functions require only a single pin, but most are implemented across a group of pins. For example, MS is a single pin, but SPI requires several pins. The user selects pin functions to suit their use case by programming the appropriate registers. The *Pin Description* table shows default and alternate functions for each MFP pin, listed in order of priority (highest first).

The output transition time of each MFP can be changed from the default value by register programming. However, if the pass-through I^{2}C/UART function is selected, the transition time of these specific pins is fixed independent of the setting. The main channel I^{2}C/UART pins have a fixed speed. Transition times depend on the edge rate setting and V_{DDIO} supply voltage. See Table 20 for typical transition times.

Table 19 indicates how latch-on-power-up, I^{2}C/UART, audio, SPI, and other functions are mapped to the MFP pins. Some pins include unique physical I/O characteristics as noted in Table 19 and detailed in Table 21. Any pins that are

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not specifically identified as one of the special types detailed in Table 21 offer full GPIO input/output capability with configurable pullup/pulldown resistors and open drain or push-pull output with configurable edge rate.

Table 19. GMSL MFP Function Map

PIN	LATCH-ON POWER-UP	I²C/ UART	AUDIO	SPI	OTHER FUNCTIONS	GPIO (TYPE)	BASELINE (DEFAULT FUNCTION, I/O TYPE AND STATUS)	POWER DOWN	SLEEP	DEFAULT IO_EDGE_RATE
MFP0			SCK2	SCLK		GPIO0	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP1			SD2	MOSI		GPIO1	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP2			WS2	MISO		GPIO2	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP3/ SDA_RX		SDA, RX				GPIO3 (odo, slow)	SDA, RX ODO, 40k pullup CMOS in	Hi-Z	Latched	I²C
MFP4					LMN0	GPIO4 (slow)	GPI CMOS in, 1M pulldown	Hi-Z	Latched	11
MFP5					LMN1	GPIO5 (slow)	GPI CMOS in, 1M pulldown	Hi-Z	Latched	11
MFP6/ CFG0	CFG0				GPOA	GPO6 (out, slow)	Disabled Hi-Z	Hi-Z	Latched	11
MFP7/ SCL_TX		SCL, TX				GPIO7 (odo, slow)	SCL, TX ODO, 40k pullup CMOS in	Hi-Z	Latched	I²C
MFP8					LOCK	GPIO8 (slow)	LOCK ODO, 40k pullup	Hi-Z	Latched	11
MFP9					ERRB	GPIO9 (slow)	ERRB ODO, 40k pullup	Hi-Z	Latched	11
MFP10/ CFG1	CFG1				GPOB	GPO10 (out, slow)	Disabled Hi-Z	Hi-Z	Latched	11
MFP11			WS1		CNTL1	GPIO11	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP12			SD1			GPIO12	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP13			SCK1			GPIO13	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10

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Table 19. GMSL MFP Function Map (continued)

MFP14					CNTL0	GPIO14	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP15						GPIO15	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP16	CFG2					GPO16 (out)	Disabled Hi-Z	Hi-Z	Latched	10
MFP17		Pass-Through SDA1, RX1				GPIO17	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP18		Pass-Through SCL1, TX1				GPIO18	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP19					LMN2	GPIO19 (slow)	GPI CMOS in, 1M pulldown	Hi-Z	Latched	11
MFP20					LMN3	GPIO20 (slow)	GPI CMOS in, 1M pulldown	Hi-Z	Latched	11
MFP21				BNE, SS1		GPIO21	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP22				RO, SS2	PCLKOUT CNTL2	GPIO22	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP23		Pass-Through SDA2, RX2			DEOUT CNTL3	GPIO23	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP24				MS	RCLKOUT, HSOUT	GPIO24	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10
MFP25		Pass-Through SCL2, TX2			VSOUT CNTL4	GPIO25	GPI CMOS in, 1M pulldown	Hi-Z	Latched	10

Hi-Z - pull-up/pull-down is disabled and input/output is disabled

Latched – Value of input before sleep mode entered remains latched in sleep mode and after resume from sleep

Table 20. Control-Channel and Side-Channel Typical Rise and Fall Times

PIN TYPE OR GPIO IO_EDGE_RATE SETTING	RISE TIME*		FALL TIME**	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
HPD	2.1ns	1.1ns	2.0ns	1.1ns
00	1.0ns	0.6ns	0.8ns	0.5ns
01	2.1ns	1.1ns	2.0ns	1.1ns
10	4.0ns	2.3ns	4.3ns	2.3ns
11	9ns	5ns	10ns	5ns

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Table 20. Control-Channel and Side-Channel Typical Rise and Fall Times (continued)

I^2C	***	***	40ns	30ns

*20% to 80%, 10pF load.

**80% to 20%, 10pF load.

***Rise time for open-drain outputs depends on external pullup resistor value.

Table 21. SPECIAL GPIO TYPES

TYPE	DESCRIPTION
slow	Can only be used with slow edge rate setting (IO_EDGE_RATE = 3)
odo	output function supports only open drain operation
out	Output only

MFP I/O Properties

Table 22 defines the pin IO properties for each of the MFP functions. All pins are powered by V_{DDIO} except DIS_REM_CC, which is powered by V_{DD18}.

Table 22. MFP Pin IO Properties

MFP FUNCTION	PIN IO PROPERTIES
GPIOs	Push-pull, open drain, or no drive Pullup, Pulldown with selectable 1MΩ or 40kΩ Input or Output or Input/Output I^2C-only IO can only be open-drain output, all others can be open-drain or push-pull
SCLK, RO, MOSI, MISO, WS1, SD1, SCK1, WS2, SD2, SCK2, MS	CMOS in with 1MΩ pulldown
SCLK, BNE, SS1, SS2, MISO, MOSI, RCLKOUT	CMOS out
LOCK, ERRB	Open-drain output with 40kΩ pullup
SDA, SCL, SDA1, SCL1, SDA2, SCL2	Open-drain I^2C-filtered I/O with 40K pullup, CMOS input
TX, TX1, TX2	Open-drain UART output with 40k pullup
RX, RX1, RX2	UART Input
DIS_REM_CC	CMOS in with 100K pull-down (V_{DD18})

General-Purpose Inputs and Outputs (GPIO)

GPIOs are typically used to pass low-speed (< 100kbps) signals over the GMSL link. A GPIO tunnel can be set up in the forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based: a GPIO packet is created and transmitted on the GMSL link when a rising- or falling-edge transition is detected at a GPI pin. The transition is regenerated at a GPO on the other end of the link.

The multifunction pins can be programmed as GPI (input), GPO (push-pull output or open-drain output) or GPIO (bidirectional input/output). Each GPIO can also be programmed for 1MΩ or 40kΩ pullup or pulldown (or none). Although an internal pullup is provided, high-speed open-drain outputs require an appropriate-value external pullup resistor to V_{DDIO}. Inputs cannot be left unconnected. Always ensure that every pin configured as an input has a pullup or pulldown programmed or is driven by another IC.

A GPI on one side of the serial link can be mapped to a single GPO or multiple GPOs on the other side of the link. Each GPI is assigned a pin ID with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0–GPIO0, GPIO1–GPIO1, GPIO2–GPIO2, etc. However, GPIO mapping can be arbitrarily changed through register settings.

GPIO Transmission Modes and Delay

GPI transitions can be transmitted in two modes: delay-compensated and non-delay-compensated. When delay

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compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases, but jitter and skew decrease.

NOTE: When in splitter mode, reverse channel delay compensation can only be used on the GMSL link that locks first.

The state of each GPIO can be read or written by register either locally or remotely over the GMSL link by a µC using the control channel I^2C/UART interface.

When delay compensation is disabled, channel latency is not fixed. The GPI transition is sent as soon as possible based on available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Non-delay-compensated mode should be used with signals tolerant to delay variation (e.g., µC interrupts).

GPI transitions are transmitted in the order they occur.

Typical GMSL GPIO tunnel delays for 6Gbps forward and 187Mbps reverse-link rates are shown in Table 23.

Table 23. Typical GPIO Delays for Forward-Link and Reverse-Link Transmission

DIRECTION	DELAY COMPENSATION	DELAY
GPIO forwarding from serializer to deserializer (6Gbps forward channel)	disabled	720ns
	enabled	3.5µs
GPIO forwarding from deserializer to serializer (187Mbps reverse channel)	disabled	6µs
	enabled	15µs

Reserved GPIO Tunnel IDs

GPIO tunnel ID 29 (on forward and reverse) is used by the UART MS signal when the remote UART mode select function is enabled in that direction.

GPIO tunnel ID 31 is used for remote error transmission by default. An alternative GPIO ID can be specified for remote error transmission if desired.

Do not use the above reserved IDs for other purposes unless their reserved function is disabled or reconfigured for an alternative GPIO ID.

Forward GPIO Tunnels

All MAX96781/MAX96783 MFP pins supporting a GPIO input function can be driven to a remote deserializer via a forward GPIO tunnel.

When driving GPIO tunnels in the forward direction (from serializer MFPs to deserializer MFPs), each enabled MFP can be connected to a selected GPIO tunnel (with a specified ID). The forward GPIO tunnel ID must be programmed using GPIO_TX_ID for each MFP. The default GPIO tunnel IDs are the MFP index values, i.e., GPIO0 maps to tunnel 0, GPIO5 to tunnel 5, etc.

Reverse GPIO Tunnels

All MAX96781/MAX96783 MFP pins supporting a GPIO output function can be driven by the deserializer via a reverse GPIO tunnel.

Most MFPs can connect to a single reverse GPIO tunnel. The tunnel ID they connect to must be programmed using GPIO_RX_ID for each MFP. The default GPIO tunnel IDs are the MFP index values.

The MAX96781/MAX96783 also include an enhanced reverse multi-tunnel GPIO connection feature on a limited number of pins. The pins supporting this feature are MFP0, MFP1, MFP21, MFP22, MFP23, MFP24, and MFP25. These pins can connect to multiple reverse GPIO tunnels (up to four) and output the combined GPIO value received from each tunnel. For these MFPs, the four GPIO tunnels the pin connects to are programmed using GPIO_RX_ID, GPIO_RX_ID2, GPIO_RX_ID3, and GPIO_RX_ID4.

The connection to each tunnel is enabled by setting GPIO_RX_EN_A, GPIO_RX_EN2_A, GPIO_RX_EN3_A, and GPIO_RX_EN4_A. Each possible combination of these GPIO_RX_EN* is valid. The signals received through the connected tunnels are combined by AND-ing or OR-ing them (selected by GPIO_OUT_LGC) and the combined signal is output to the serializer pin. The same GPIO tunnel can be connected to multiple pins.

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When the SOC detects an edge on a multi-tunnel GPIO output, it can read GPIO_RECVED_* to determine the most recent received logic state from each GPIO tunnel.

MFP Pin Equivalent Circuits

In general, MFP pins can all be classified as either programmable high speed GPIO or programmable I^{2}C/ODO (Open Drain Output) GPIOs. Equivalent circuit representations are below.

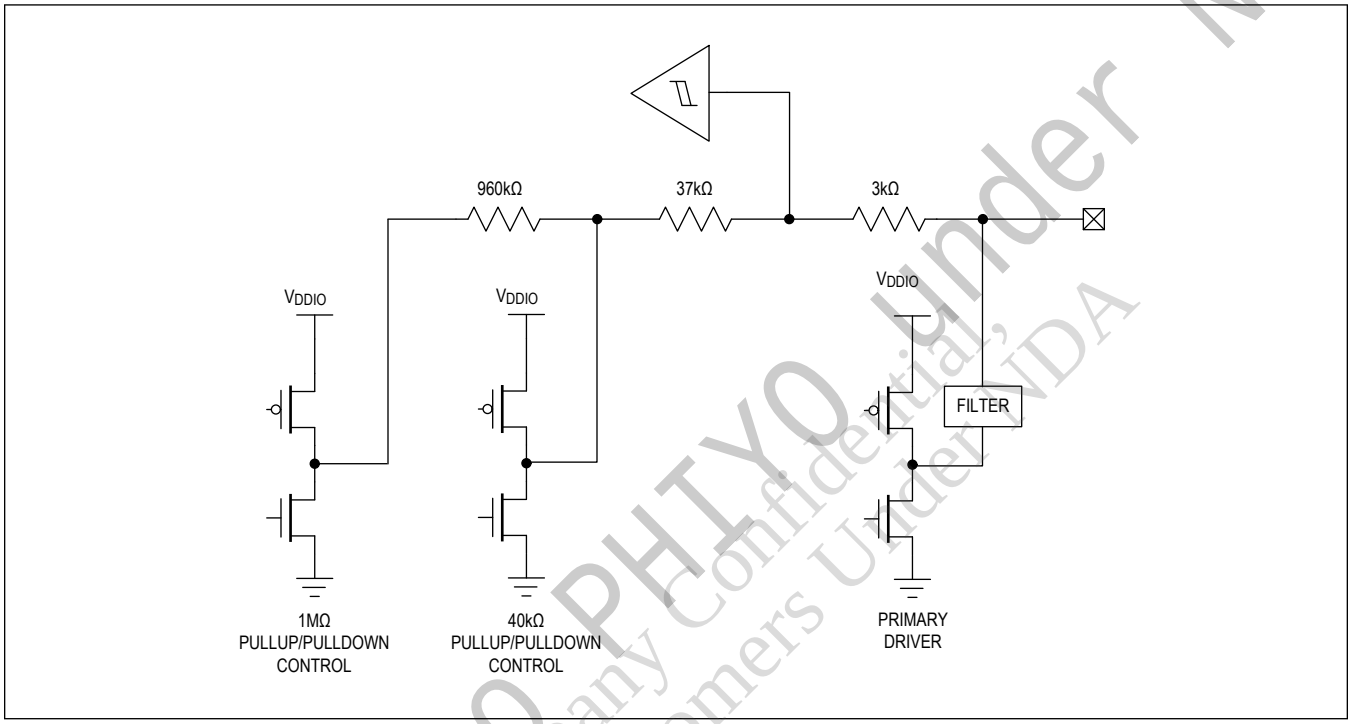

Figure 32. Standard High Speed GPIO

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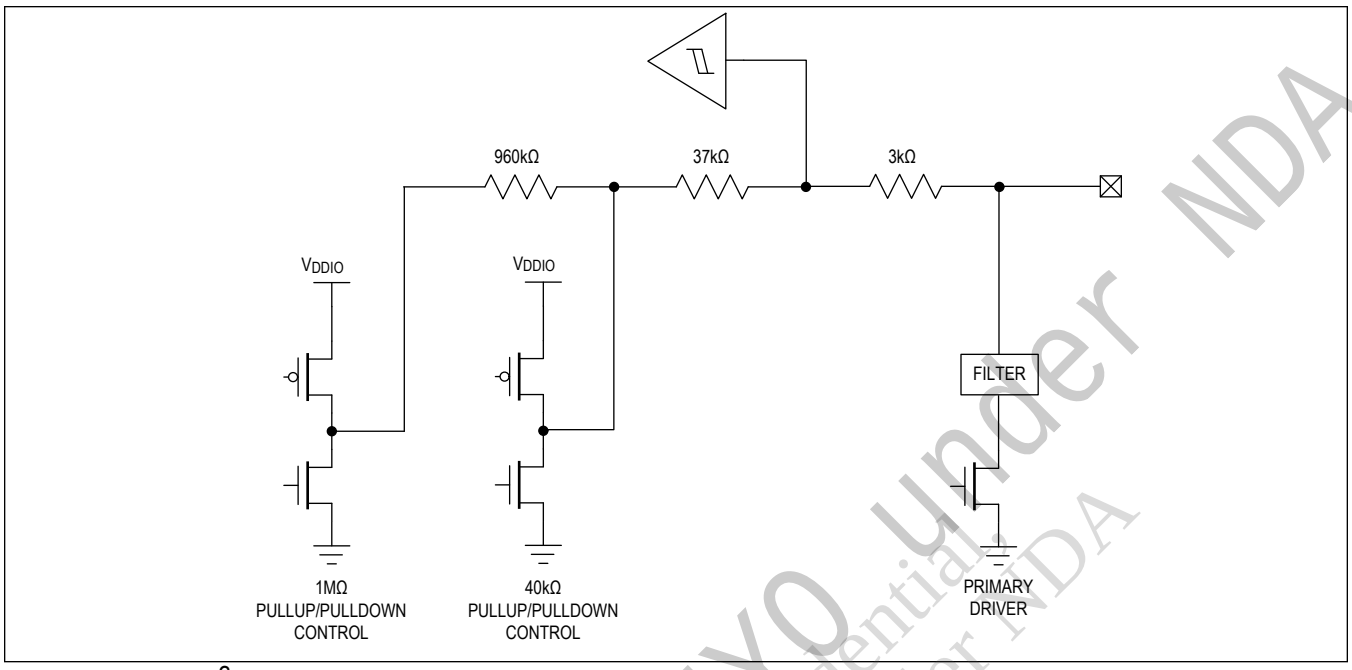

Figure 33. Standard I²C GPIO

Clocking

GMSL Reference Clock

The MAX96781/MAX96783 require either a 25MHz crystal or an external low-jitter clock source. RCLKOUT of another GMSL device can be utilized as the external clock source when multiple GMSL devices are located in close proximity. Care must be taken in the design of the reference clock source to ensure sufficiently low jitter.

Reference Clock Output

GMSL devices are designed such that the RCLKOUT of one device can drive the reference clock input of another nearby device. The MAX96781/MAX96783 RCLKOUT includes programmable division ratios of 1, 2, and 4.

System Diagnostics

Error and Fault Condition Monitoring

All GMSL2 devices have an open-drain multi-purpose error reporting and interrupt status output which can output detected error status and/or some events internal to the device which may be of interest to a host processor (interrupts). The ERRB function is assigned to a dedicated pin, or one of the MFPs as indicated in the *Pin Descriptions*. ERRB functionality of the MFP is enabled by default and it operates in open-drain output mode with 40K internal pull-up. ERRB is an active-low signal. Logic high indicates “no error and no interrupt event has happened” while logic low indicates “an error or interrupt event has happened.”

Several different error and event sources can drive the ERRB pin. Each error and event that can drive ERRB pin has a status flag in the registers, so the reason for assertion of ERRB pin can be read from registers when several different events can drive the ERRB pin. Each ERRB source can be individually enabled and disabled.

The main functions/typical usages of this feature are the following:

- Very fast routing of on-chip diagnostic or ASIL related function indicators to device pin to be used as an interrupt for the SoC.
- Remote side forwarding of diagnostics to local ERRB signal. This allows all devices connected to local SERDES device, via GMSL link, to forward their internal ERRB signal to the local device’s ERRB signal.

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ERRB Operation

There are many individual errors that can be output to the ERRB pin. Each error has a status register and an output enable (OEN) bit, which enables that error to be OR'd into the ERRB output at the ERRB pin. The ERRB ORing concept is the same in every GMSL device. However, the possible errors that are available may differ.

During normal operation, monitor the ERRB pin of the GMSL device to determine when an error has occurred. When an error occurs, it is reported in the local register of that specific feature. If there is a counter for that type of error, it tracks the number of errors that occurred. Most error status indicators can be routed to the ERRB pin. To find out if a specific error or status indicator can be routed to the ERRB pin, consult the safety-related documents for the MAX96781/MAX96783.

Disabling ERRB function

When error and interrupt reporting is not needed and/or the MFP pin which is used as ERRB by default is needed for another function, ERRB function of the MFP can be disabled. Set ERRB_EN=0 to disable the ERRB function of the MFP. When ERRB function is disabled the MFP operates as a standard GPIO pin.

Remote error reporting

GMSL devices can report the ERRB status of the remote device when the link is locked. Remote error status is transmitted over an internal GPIO tunnel using a programmable ID. Remote device transmits its ERRB status when ERR_TX_EN=1 using the GPIO ID programmed in ERR_TX_ID register. Local device receives the transmitted error status over the GPIO tunnel. Any of the MFPs can be connected to the GPIO tunnel and output the received remote error status. To do this, program GPIO_RX_EN=1, GPIO_TX_EN=0, GPIO_OUT_DIS=0, GPIO_RX_ID="Remote ERR_TX_ID value" for the MFP which will output the remote error status.

Remote error status can also be combined with local error status and output at ERRB pin like other local error and interrupt events. To do this, set ERR_TX_EN=1 in the remote device and check ERR_TX_ID register in the remote device and if needed change it to a value which is not shared by any other GPIO tunnel (default value is OK in most cases). Then in the local device, set ERR_RX_ID="Remote ERR_TX_ID value", ERR_RX_EN=1 and REM_ERR_OEN=1. Whenever remote ERRB status changes, it will be transmitted to the local device and ERRB pin of the local device will change (unless it was already active due to a local error or interrupt). Host controller can read the REM_ERR_FLAG register to see whether the error is due to a remote error/interrupt or a local error/interrupt and then act accordingly.

In GMSL2 splitter applications, remote ERRB status from each connected deserializer can be combined at the local ERRB pin.

Auto Error Reset

It is possible to automatically reset some error counters after ERRB is asserted. This allows continuous monitoring of the ERRB pin and tracking errors without any need to read registers. When AUTO_ERR_RST_EN=1, DEC_ERR_A, DEC_ERR_B, IDLE_ERR and VID_PXL_CRC_ERR counter registers are automatically reset after ERRB is asserted for 1µs.

Similarly, when AUTO_CNT_RST_EN=1, PKT_CNT counter register is automatically reset after ERRB is asserted for 1µs. This function is useful for counting the received packets by only observing the ERRB pin.

Link Integrity Features

The GMSL physical layer (PHY) provides diagnostic tools to aid in system bring up and debug. These tools leverage parts of the adaptive equalizer implementation. These diagnostic tools are not laboratory instrumentation nor are they designed to demonstrate channel compliance.

These tools provide a high degree of visibility of the link and system performance. The GMSL diagnostic tool set provides a market leading level of visibility. These diagnostic tools include:

1. Eye Mapping
2. BER bathtub curves
3. Link Margin

These tools are a mixture of hardware and supporting software for data collection and processing. The Graphical User Interface provides the required software and processing.

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GMSL1 Backwards Compatibility

The MAX96781/MAX96783 include two independently configurable GMSL1 capable serial links. Each of the two GMSL1 links can be configured separately to support the various GMSL1 functions that are described, enabling seamless connectivity of any GMSL1 deserializer to either link.

GMSL1 backwards compatibility supports forward link rates from 500Mbps to 3.12Gbps and a reverse link rate of 500Kbps or 1Mbps. When the MAX96781/MAX96783 are paired with a legacy GMSL1 only deserializer, the devices must be configured for GMSL1 compatibility mode, and the available forward link rate is reduced to the maximum supported by the deserializer. Pixel clocks of up to 104MHz are supported.

The MAX96781/MAX96783 may not support all features of a given GMSL1 deserializer.

Table 24 specifies the availability of common features of GMSL2 devices that are operated in GMSL1 mode. Note that some GMSL2 features, such as SPI, are only available in GMSL2 mode, and as a result they are never available in GMSL1 mode regardless of the devices used. Features not supported by both devices in a link should be disabled. All enabled features must be configured with the same settings at both ends of the link.

Most features specified in Table 24 can be enabled or disabled by appropriate register configuration or by the state of configuration input pins at power-up. Hardware design of both serializer and deserializer subsystems should account for the correct connection of configuration pins to achieve the desired settings. Interfacing coax interconnects to non-coax capable GMSL1 devices requires special hardware considerations to ensure reliable functionality.

Table 24. Feature Availability in GMSL1 Mode

FEATURE NAME	FEATURE AVAILABLE?
Coax	Yes
Bus Width Select (BWS)	Yes
High-Bandwidth Mode (HIBW)	Yes
Data Rate Select (DRS) (Low speed mode)	Yes
HSYNC/VSYNC Encoding	Yes
Pixel CRC (6 bits per pixel)	Yes
Hamming Error Correction	No
I^2C to I^2C	Yes
UART to UART	Yes
UART to I^2C	No
Pass-Through I^2C Channels	No
I^2C Address Translation	Yes
SPI Control Channel	No
High-Immunity Mode	Yes
REV_FAST with HIBW Mode	Yes
Packet Control Channel with CRC	Yes
Packet CC Retransmission	Yes
Configuration Link	Yes
I^2S on Forward Link	Yes
7.1 TDM	Yes
GPI to GPO on Reverse Channel	Yes
Delay Compensated GPI/GPO	No
Line Fault	Yes
UART Base Mode	Yes
UART Bypass Mode	Yes
Spread Spectrum	Yes

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Table 24. Feature Availability in GMSL1 Mode (continued)

FEATURE NAME	FEATURE AVAILABLE?
~~Serializer Pre/Deemphasis~~	No
Twisted Pair Splitter Mode	No
Auto HDCP	No
Watermark	Yes
Video Timing Generator	Yes
Video Crossbar	Yes
PRBS	Yes
CNTL[4:0] on Forward Channel	Yes
A/V Status Register Interrupt	No
HS/VS/DE Inversion	Yes
WS/SCK Inversion	Yes
Jitter-Filtering PLL	No
Sleep Mode	Yes

Software Configuration of GMSL Link Mode when using UART Control Channel

In designs that utilize software control to support both GMSL2 and GMSL1 links with UART control channel, the CFG pins must be used to set any link that may connect to a GMSL2 deserializer to GMSL2 mode initially. After start-up, the links can be set independently to GMSL1 as needed.

GMSL1 Serial Link Overview and Data Formatting

In GMSL1 mode, the GMSL link operates at a speed determined by the incoming video PCLK. Each PCLK cycle transmits one pixel of data that is packed into a 30-bit or 40-bit serial packet along with control-channel data and CRC/parity information. The resulting serial-link clock is either 30 or 40 times higher than the equivalent PCLK. At the receiving end of the link, a complementary deserializing operation is realized, and the incoming video stream at the serializer side of the link can be routed to a compatible display at the deserializer side of the link. The GMSL1 link itself is totally transparent, with the exception of its finite delay.

GMSL1 Video/Configuration Link

When the high-speed video link is not needed or is unavailable, a configuration link can be used in its place. In configuration-link mode, the video input is disabled and the serial link internally generates its own clock to allow full operation of the control channel.

In normal operation, the serializer runs in video link mode (serializer SEREN = 1) with video data and control data sent across the serial link. The serializer powers up in video-link mode and requires a valid PCLK for operation and link lock.

The configuration link is available to set up the serializer, deserializer, and peripherals when PCLK is not available. Set SEREN = 0 and CLINKEN = 1 in the serializer to enable the configuration link. Once PCLK has been established, turn on the video link (SEREN = 1).

Set AUTO_CLINK bit = 1 and SEREN = 1 in the serializer to have the device automatically switch between the video link and configuration link whenever PCLK is not present.

GMSL1 Link Modes

The GMSL1 serial link has multiple bus-width settings that determine the video bus width and the resulting number of bits per serial packet. The serial link operates to a maximum serial bit rate of 3.12Gbps. The BWS bit determines if the encoded length of each serial packet is 30 or 40 bits, which translates to a maximum serial packet rate and PCLK of 104MHz (when BWS = 0 and HIBW=1) or 78MHz (when BWS = 1 and HIBW=0). The 9-bit/10-bit (BWS = 0, HIBW = 1) or 8-bit/10-bit (BWS = 1, HIBW=0) encoding translates the 27 or 32 bits of video/CRC/audio/control-channel data associated with each PCLK cycle into 30- or 40-bit serial packets. One bit is used for parity, while a second is reserved for the control channel. An additional 6 bits are used for the optional 6-bit CRC. The remaining bits carry video data (including any sync

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bits if H/V encoding is not used).

GMSL1 27-Bit, High-Bandwidth Mode

When BWS = 0 and HIBW = 1 (high-bandwidth mode), the 30-bit serial packet consists of three 9-bit/10-bit symbols representing 27 bits. After the parity and control channel, this leaves 19 bits of video data if CRC is used, or 25 bits of video/audio data if CRC is not used, which enables efficient transmission RGB888 data and audio without packet CRC protection. For typical applications that include 24b color, CRC cannot be used.

High-bandwidth mode enables transmission of 24-bit RGB video at 104MHz pixel clock. Set BWS = 0 and HIBW = 1 in the serializer and deserializer to use high-bandwidth mode. In high-bandwidth mode, the serializer encodes HS, VS, DE, and CNTL[4:0] to special packets. Packets are sent by replacing a pixel before the rising edge and after the falling edge of HS, VS, and DE signals. Maintain HS, VS, and DE low pulse widths of at least two pixel clock cycles in duration. By default, CNTL[4:0] is sampled continuously when DE is low. CNTL[4:0] are sampled only on HS/VS transitions when DE is high. All CNTL signals can be tunneled in this mode.

When audio is enabled, data bit D24 is dedicated to transmission of the encoded audio stream. This does not impact video transmission because bit D24 is typically an empty bit for 24-bit RGB video transmission.

Not all GMSL1 deserializers support all GMSL1 functions. The data sheet of the paired GMSL1 deserializer describes the serial data format supported by the paired device.

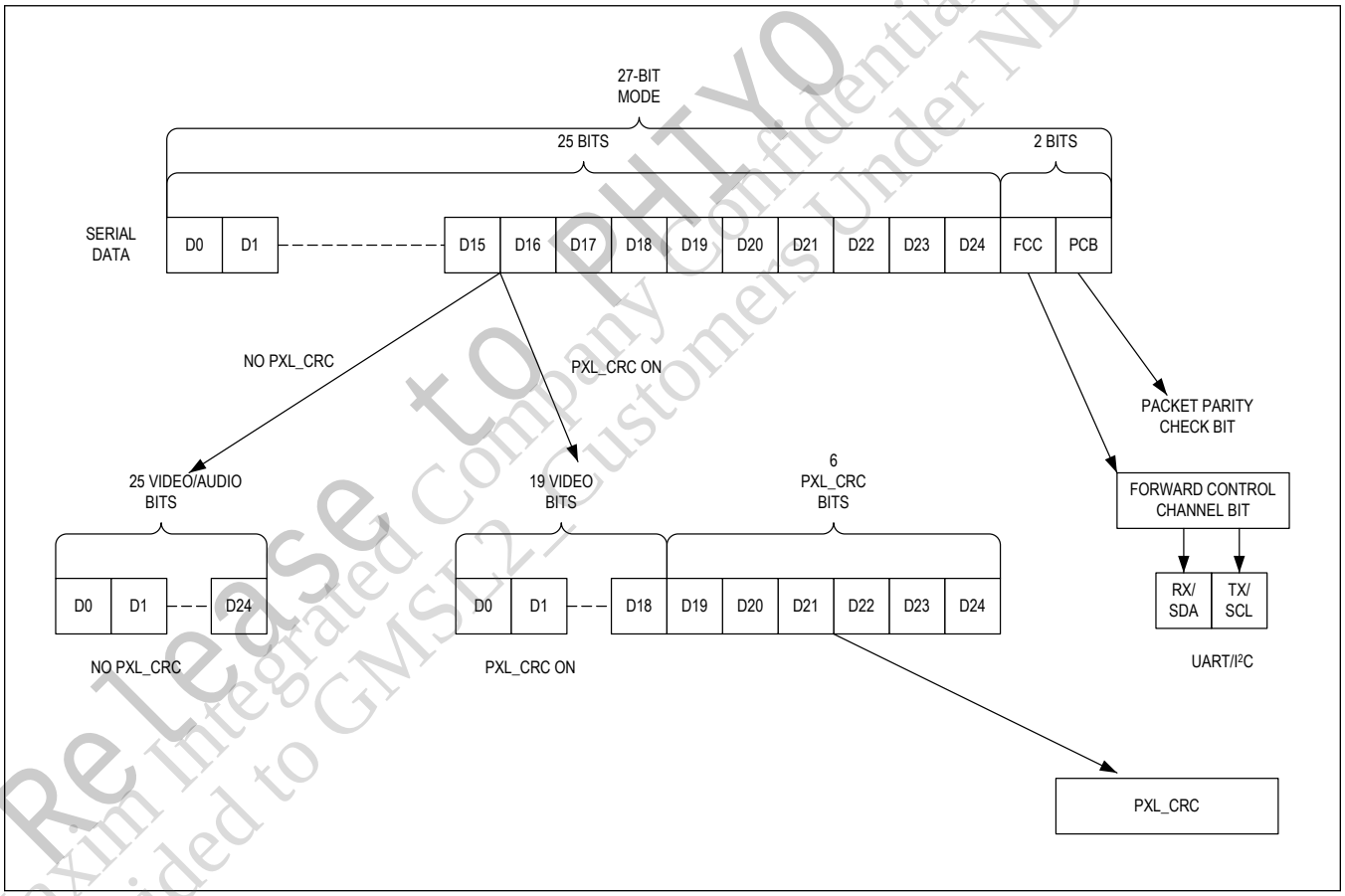

Figure 34. 27-Bit, High-Bandwidth Mode Serial-Data Format

GMSL1 32-Bit Mode

When BWS = 1, the 40-bit serial packet consists of four 8-bit/10-bit symbols representing 32 bits (32-bit mode). After

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parity and control channel, this leaves 24 bits of video data if CRC is used, or 30 bits of video data if CRC is not used, which enables transmission of RGB888 data with packet CRC protection. In this mode, HIBW must be set to 0.

Only CNTL1 and CNTL2 signals are available in this mode, although other CNTL signals can be routed to the two available bit slots.

When audio is enabled, data bit D29 is dedicated to transmission of the encoded audio stream. Tunneled CNTL1 and CNTL2 GPIOs use dedicated forward channel bit slots D27 and D28. Audio and CNTL data uses some of the same bit slots as PXL_CRC, and as a result simultaneous transmission of both CRC and audio/CNTL cannot be supported in this mode.

Not all GMSL1 deserializers support all GMSL1 functions. The data sheet of the paired GMSL1 deserializer describes the serial data format supported by the paired device.

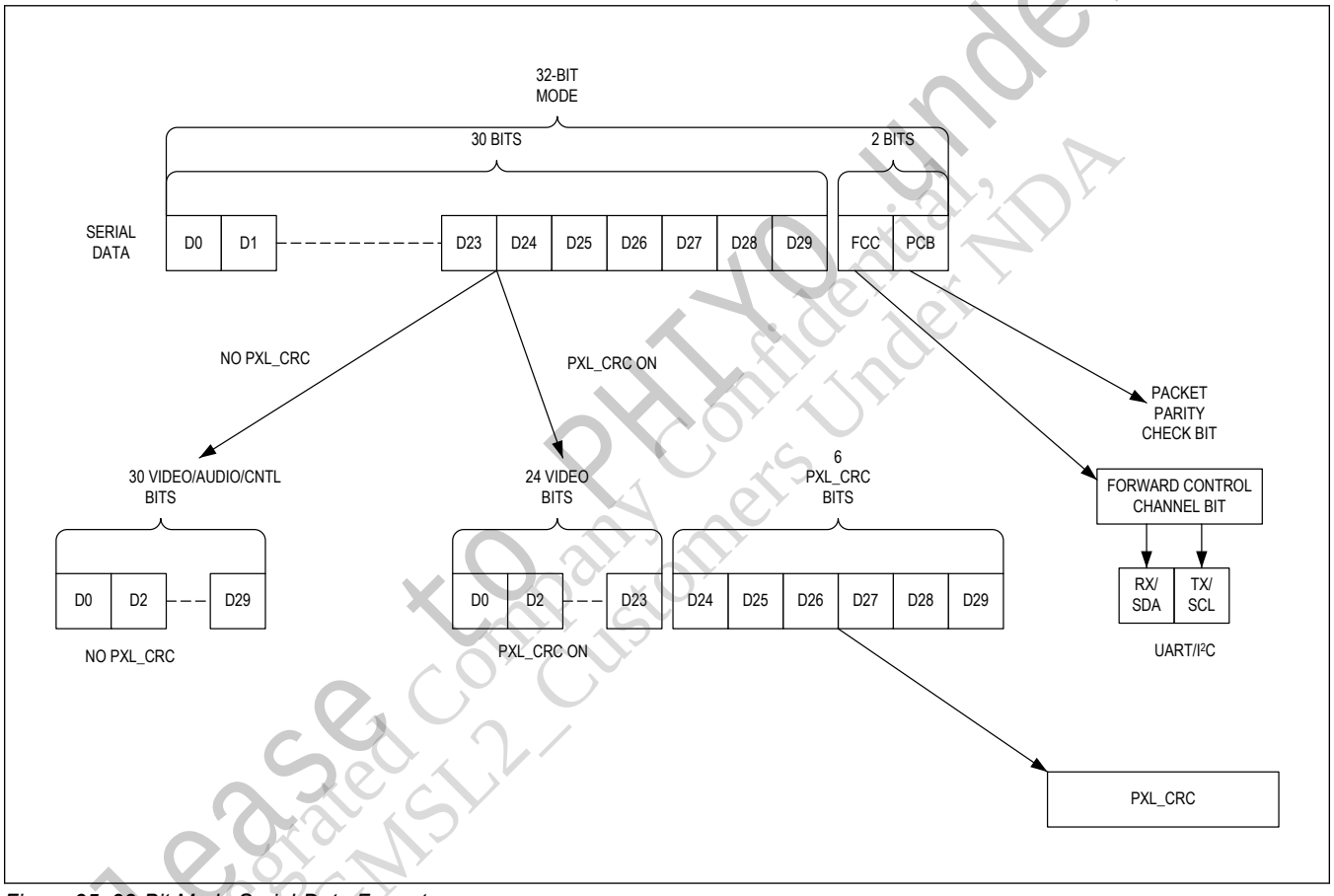

Figure 35. 32-Bit Mode Serial-Data Format

GMSL1 Data Transmission Error Detection

The serial link's 8-bit/10-bit or 9-bit/10-bit encoding/decoding and 1-bit parity detect bit errors that occur on the serial link. An optional 6-bit CRC check is available at the expense of 6 video bits. To activate 6-bit CRC mode, set PXL_CRC = 1 in the remote-side device first, then in the local-side device. In applications that require video pixel CRC, 32-Bit mode (BWS=1) is required to provide sufficient payload capacity to simultaneously accommodate 24b color data and pixel CRC.

GMSL1 HS/VS Encoding

By default, GMSL assigns a video-bit slot to HSYNC, VSYNC, and DE (if used). With HS/VS encoding enabled, the

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device instead encodes and transmits sync state changes using special packets to free up additional video bit slots. HS/VS encoding is on by default when the device is in high-bandwidth mode (HIBW = 1). DE is encoded only when HIBW = 1 and DIS_DE = 0. Set HVEN = 1 to turn on HS/VS encoding when HIBW = 0 (DE, if enabled, uses up a video bit). HS/VS encoding requires that HSYNC, VSYNC, and DE (if used) remain high during the active video and low during the blanking period. Use HS/VS inversion when using reverse-polarity sync signals.

GMSL1 PCLK Frequency Range

The range of supported PCLK frequencies depends on the setting of BWS, DRS, and HIBW. These parameters are detailed in the register table. DRS = 1 can be used if low data rates are desired. By default, DRS has a value of 0, which is required for most common video streams. In most cases, BWS = 0/HIBW = 1 (27-bit mode, RGB888 without CRC) or BWS = 1/HIBW = 0 (32-bit mode, RGB888 with CRC). The maximum PCLK frequency in 27-bit mode is 104MHz while the maximum PCLK frequency in 32-bit mode is 78MHz. Depending on the maximum link rate of the connected deserializer, the available PCLK range needs to be constrained such that the GMSL data rate is within the bounds supported by the deserializer. For example, if the device is connected to a 1.5Gbps GMSL1 legacy deserializer, the maximum PCLK is limited to either 50MHz (27-bit mode) or 37.5MHz (32-bit mode). The values given in the table assume a maximum link bandwidth of 3.12Gbps.

Table 25. GMSL1 PCLK Frequency Range

DRS SETTING	HIBW/BWS SETTING	PCLK RANGE (MHz)
0 (high data rate)	BWS = 0, HIBW = 1 (27-bit mode)	36.66 to 104
	BWS = 1, HIBW = 0 (32-bit mode)	12.5 to 78
1 (low data rate)	BWS = 0, HIBW = 1 (27-bit mode)	18.33 to 36.66
	BWS = 1, HIBW = 0 (32-bit mode)	6.25 to 12.5

GMSL1 Control Channel

GMSL1 operating mode includes a main I^{2}C/UART control channel with similar characteristics to the GMSL2 control channel along with the GMSL1 specific tunneled GPIO functions GPI-GPO and CNTL.

GMSL1 Forward Control Channel

Control data sent from the serializer to the deserializer is sent on the forward control channel. The data is encoded as one of the serial bits in the forward high-speed link. This data is extracted as part of the deserialization process and routed to the deserializer control channel. The forward control-channel bandwidth exceeds the maximum external control channel data rate, and all data sent on the forward control channel appears on the remote side after a brief delay.

GMSL1 Reverse Control Channel

Control data sent from the deserializer to the serializer is sent on the reverse control channel. The maximum data rate is 1Mbps when high-immunity mode is disabled. High-immunity mode is available to increase the robustness of the reverse control channel at a reduced bit rate of 500kbps. Setting the REV_FAST bit = 1 increases this rate back to 1Mbps. Table 26 details the available data rates for different GMSL1 reverse control channel configurations. In I^{2}C mode, when the input data rate (after encoding) exceeds the reverse data rate, the input clock is held through clock stretching to slow the external clock to match the internal bit rate.

GMSL1 High-Immunity Reverse Control-Channel Mode

The MAX96781/MAX96783 include a high-immunity reverse control-channel mode (HIM), which has increased robustness at half the bit rate versus the standard GMSL1 reverse control channel link as shown in Table 26.

Set the HIGHIMM bit high in both the serializer and deserializer to enable high-immunity mode at any time after power-up. Set the HIGHIMM bit low in both the serializer and deserializer to use the legacy reverse control-channel mode. The serializer reverse channel is not available for 500µs/1.92ms after the reverse control-channel mode is changed through the serializer/deserializer's HIGHIMM bit setting, respectively.

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A fast high-immunity reverse control-channel mode is available for applications requiring maximum robustness and reverse-channel bandwidth. This mode is enabled by setting HIGHIMM = 1 and REV_FAST = 1. When using the fast high-immunity reverse control-channel mode, the equivalent video PCLK must be above a specific minimum frequency that depends on the operating mode of the device. Table 27 details the PCLK frequency ranges that support fast high-immunity reverse control-channel functionality.

When enabling REV_FAST mode, set REV_FAST=1 in the deserializer first and then in the serializer.

Table 26. Reverse Control-Channel Modes

HIGHIMM BIT (HIM)	REV_FAST BIT	REVERSE CONTROL-CHANNEL MODE	MAX UART/I²C BITRATE (kbps)
Low	X	Legacy reverse control-channel mode (compatible with all GMSL1 devices)	1000
High	0	High-immunity mode	500
	1	Fast high-immunity mode	1000

X - Don't care

Table 27. Fast High-Immunity Mode PCLK Requirements (REV_FAST=1, HIGHIMM=1)

BWS	HIBW	GMSL1 MODE	ALLOWED PCLK RANGE (MHz)
0	1	27-Bit Figure 34	> 83.33
1	0	32-Bit Figure 35	> 30

GMSL1 GPI-GPO

The MAX96781/MAX96783 include a dedicated tunneled GPO output for each link. The state of the GPO output tracks the logic level applied to the GPI input on the deserializer side of the link. The GPO state can alternatively be controlled by register access if preferred. Typical delay between a state change on the GPI input of the deserializer and the associated transition on the corresponding GPO is < 350µs.

GMSL1 CNTL Pins

The CNTL inputs provide a means of transmitting up to five low bandwidth control signals from the serializer to deserializer(s) without any interaction from the primary I²C/UART. The MAX96781/MAX96783's five CNTL inputs are shared by the two GMSL1 links. All CNTL signals can be tunneled in 27b mode. In 32b mode, only CNTL1 and CNTL2 are available, and they share bit slots with PXL_CRC in this mode, preventing simultaneous use of PXL_CRC and CNTL. The CNTL bit slots can be rotated to enable various CNTL inputs to be mapped to different outgoing CNTL bit slots.

GMSL1 Spread Spectrum

To reduce the EMI generated by the transitions on the serial link, the serializer output includes programmable spread spectrum. The programmable spread-spectrum amplitudes are ±0.25%, ±0.5%, ±1%, ±2%, and ±4% with a modulation frequency of 25kHz as shown in Table 28. Some spread-spectrum amplitudes can only be used at lower PCLK frequencies as detailed in Table 29. There is no PCLK frequency limit for the ±0.5% spread rate.

Each GMSL1 link has independent spread spectrum control. Spread spectrum should be configured and enabled one time during initialization as needed for each link. Repeatedly toggling GMSL1 spread spectrum off and on in the serializer can disrupt link operation.

If GMSL1 mode is specified via software after power-up, the GMSL1 spread spectrum registers must be configured after GMSL1 mode has been specified because the associated registers are automatically reset when the device enters GMSL1 mode. If the CFG pins are used to select GMSL1 mode at power-up, then this sequencing consideration and be ignored.

Table 28. Spread-Spectrum Amplitude

config_spread_bit_ratio[2:0]	Spread Percentage
000	No spread

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Table 28. Spread-Spectrum Amplitude (continued)

config_spread_bit_ratio[2:0]	Spread Percentage
001	0.25%
010	0.5%
011	1%
100	2%
101	4%

Table 29. Spread Limitations

HIGH-BANDWIDTH MODE PCLK_FREQUENCY (MHz)	32-BIT MODE (BWS=1) PCLK_FREQUENCY (MHz)	AVAILABLE SPREAD RATES
<33.3	< 25	All rates available
33.3 to < 66.7	25 to < 50	1%, 0.5%
> 66.7	> 50	0.5%

GMSL1 Audio

Both I^2S audio inputs can be utilized in GMSL1 mode. Each GMSL1 link can transfer data from one audio stream, and the configuration of audio in each link is independent. Refer to the paired legacy GMSL1 device data sheet for detailed audio sub-system information that is unique to GMSL1 mode.

GMSL1 HDCP

Manual HDCP is supported by both GMSL1 links, and it can be independently configured for each. Refer to the paired legacy GMSL1 device data sheet for detailed HDCP sub-system information that is unique to GMSL1 mode.

Power Supplies and Thermal Management

Power Supplies

The 1.0V V_{DD} supply provides power to the digital core. Connect 1.0V ±5%.

The V_{DDIO} supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the part. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

V_{DD18} is the primary analog supply and is fixed at 1.8V. Connect 1.8V ±5%.

V_{DD18_eDP} is the supply for the DisplayPort interface and is fixed at 1.8V. Connect 1.8V ±5%.

Proper power-supply bypassing of all supplies is essential for high-frequency circuit stability. See Table 2. See Table 30 for power-supply tolerances and noise requirements. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

No specific power-supply ramp sequence is required, although recommended power supply ramp time is at least 20µs.

Recommended Operating Conditions

Table 30. Recommended Operating Conditions

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V_{DD18}		1.7	1.8	1.9	V
	V_{DD18_eDP}		1.7	1.8	1.9	
	V_{DD}		0.95	1.0	1.05	
	V_{DDIO}		1.7		3.6	
Supply Noise	V_{DD18}			25		mV_{P-P}
	V_{DD18_eDP}			25		
	V_{DD}			25		

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Table 30. Recommended Operating Conditions (continued)

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
	V_{DDIO}	1.8V		50		
		3.3V		100		
Operating Junction Temperature, T_J			-40		+125	ºC

Note: *Supply noise < 1MHz.*

Power Manager and Power Modes

The power manager exists in all GMSL2 products. The primary function is to control the internal switched supply domains during the full sequence of power states to ensure that the device powers up smoothly. After the internal supplies reach valid levels, the power manager relinquishes control to the digital core for normal operation. Another function of power manager is that it ensures the device consumes minimum standby current during sleep mode and can quickly restore configurations to full operation after waking up. Finally, the power manager monitors the power supplies for Under Voltage (UV) and Over Voltage (OV) conditions.

UV/OV Detection

The MAX96781/MAX96783 devices include overvoltage (OV) and undervoltage (UV) detection logic. Register programming is required to enable these features.

In the event of an OV condition on V_{DD18}, V_{DDIO} or V_{DD}, the ERRB pin is asserted but no further action is taken. The device will continue to remain powered with OV condition and may suffer damage. V_{DD18_eDP} is not monitored but if connected to the same supply as V_{DD18} it would be by extension.

In a UV condition on V_{DD18}, the ERRB pin will be asserted when V_{DD18} drops below an internal threshold level. The device will continue to function unless V_{DD18} drops further to an internal reset level, in which case the device will then reset. V_{DD18_eDP} is not protected but if connected to the same supply as V_{DD18} it would be by extension.

In a UV condition on V_{DDIO}, the ERRB pin will be asserted when V_{DDIO} drops below an internal threshold level. The device will continue to function unless V_{DDIO} drops further to an internal reset level, in which case the device will be reset.

In a UV condition on V_{DD}, the ERRB pin will be asserted when V_{DD} drops below an internal threshold level and the device will reset.

After recovery from a severe supply brownout that has triggered a reset, the device returns to the default power-up state with default register settings. The user must then re-initiate device startup and reprogram all registers.

Power-Down (Standby) Mode

Asserting the PWDNB pin (active-low) places the device in standby power mode and resets the digital registers and configurations to their default power-up condition. Any supply dropping below its internal threshold also places the device in power-down mode. In the event the power supply recovers or the PWDNB pin is released, the device returns to the default power-up state with default register settings. The user must then re-initiate device startup and reprogram all registers.

Sleep Mode

The sleep state provides a low power operating mode with preservation of all critical register settings and configurations. The device can be put into the sleep state through an I²C/UART command. The resume state restores the device back to the pre-sleep condition without the need for additional register writes. Resume is invoked by an I²C command on the main I²C inputs (SDA_RX/SCL_TX) or a low-frequency clock beacon transmitted from the master device over the GMSL link.

Sleep mode should not be used in conjunction with RESET_ALL because the device will unexpectedly enter sleep mode when recovering from a reset.

Thermal Management

Power consumption of GMSL devices varies based on their use case. Care must be taken by the user to provide sufficient

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heat dissipation with proper board and cooling design techniques. The package exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below 125°C to meet electrical specifications and avoid impacting device reliability.

Refer to Tutorial 4083, "Thermal Characterization of IC Packages," for guidance.

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Applications Information

Software Programming Model

GMSL serializers and deserializers are designed to follow a general software programming model. Except for features that require in-operation control-channel accesses such as the ASIL safety measures and interrupt handling, the following programming model should be followed:

1. Set the impacted functional blocks to disabled or reset mode. A general method to place the part in IDLE state is to stop all side-channel and video traffic followed by a register write (RESET_LINK = 1) to stop the GMSL link.
2. Fully configure the settings for each feature before it is enabled.
3. Establish the link by setting RESET_LINK = 0 and wait for the link to lock.
4. Start the video and side-channel traffic.

If the configuration of a feature is to be changed during the operation of other features, disable the reconfigured feature, change its settings, and re-enable it.

Conventional I^{2}C/UART Control-Channel Programming

GMSL device registers can, by default, only be accessed and configured through the main I^{2}C/UART interface, in either I^{2}C or UART modes, and through I^{2}C-over-AUX on DisplayPort serializers. By default, the main I^{2}C/UART control channel is also sent to the remote side device and any peripheral connections. This allows control of the GMSL devices from either end of the link. For multimaster configurations, with microcontrollers connected to both the serializer and deserializer, disable the remote control channel using the DIS_REM_CC pin or through register settings to prevent bus contention.

I^{2}C SDA and SCL operate as both input and open-drain output while in UART mode RX is an input and TX is an open drain output. Pullup resistors are required on SDA and SCL in I^{2}C mode and TX in UART mode.

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read.

Device Address

Each device on the I^{2}C/UART control channel must have a unique address. The GMSL device address is set to one of several 7-bit addresses according to the voltage level of the CFG0 pin at power-up. The device address can be changed after power-up via the control channel.

I^{2}C

Each device has an internal I^{2}C slave for register access. The internal registers can be written and read according to the I^{2}C protocol using the following packet formats.

Main I^{2}C Host-to-GMSL Device Communication

The host I^{2}C master has access to GMSL serializer and deserializer registers as well as remote peripherals.

I^{2}C Write-Packet Format

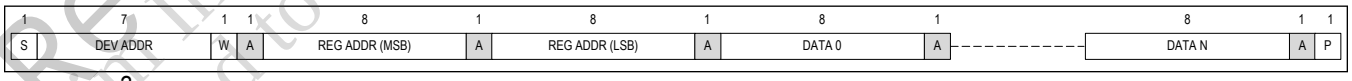

Figure 36. I^{2}C Write-Packet Format

I^{2}C Read-Packet Format

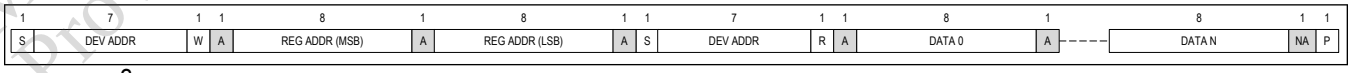

Figure 37. I^{2}C Read-Packet Format

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Host-to-Peripheral Main I²C and Pass-Through I²C Communication

When communicating between a host and peripheral, main and pass-through I²C operation is the same. An I²C tunnel across the GMSL link connects the host's I²C master to the remote I²C slave. This logically connects separated I²C buses, enabling I²C transactions across the serial link to occur (with some delay) as if performed on the same physical I²C bus. The GMSL serializer and deserializer are intermediary devices: the host I²C master connects to a GMSL device I²C slave, and the peripheral I²C slave connects to a GMSL device I²C master.

For example, when the host I²C master transacts on one side of the link (local-side), data is forwarded to the other side (remote-side) by the I²C slave of the local-side GMSL device. Data is then received by the I²C master of the remote-side GMSL device, which in turn generates the same I²C transaction with the peripheral slave I²C. The remote-side GMSL device sends back any I²C data expected by the local-side.

The I²C interface uses clock stretching (holding SCL low) to account for timing differences between the master and slave, and to allow time for data to be forwarded and received across the serial link. All local-side I²C devices must support clock stretching by the GMSL device; remote-side I²C devices are not required to support clock stretching.

UART

When the main I²C/UART interface is configured as Universal Asynchronous Receiver-Transmitter (UART), there are two operating modes: base and bypass.

UART Base Mode

The base mode is the means of ECU communication with the serializer and deserializer in which registers in these devices as well as in peripheral devices can be accessed. Base mode is enabled by default at power-up. In base mode, the ECU is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The ECU can also program peripherals on the remote side by sending UART packets to the serializer or deserializer. In base mode, the ECU communicates with a UART peripheral using the GMSL UART protocol. The device addresses of the serializer and deserializer in this mode are programmable.

In base mode, the serializer, deserializer, and peripheral registers can be written and read using the GMSL UART protocol.

Figure 38 shows the UART protocol to write and read in base mode.

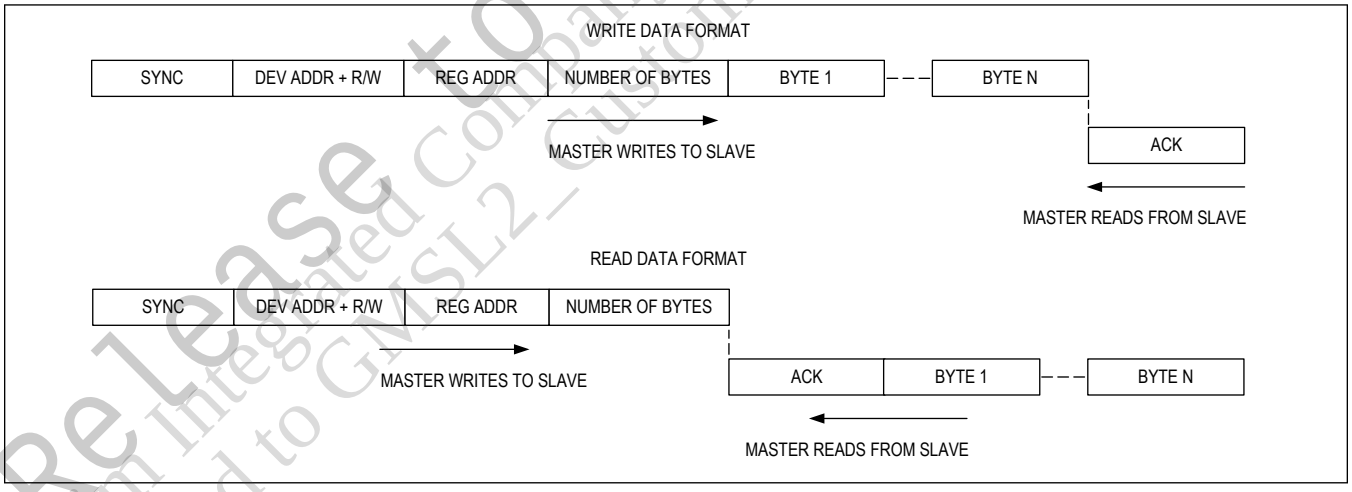

Figure 38. UART Protocol for Base Mode

UART Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the ECU, allowing the ECU to communicate only with peripheral devices. The ECU cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL link. Ignoring UART transactions prevents inadvertent miss-programming of serializer and deserializer registers. The device addresses of the serializer and deserializer in this mode are not

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programmable.

Switching Between UART Base and Bypass Modes

There are two ways to switch between base and bypass modes: programming the BYPASS_EN bit or using the device MS pin.

When setting bypass mode through the BYPASS_EN bit, BYPASS_TO is programmed for a user specified timeout (2ms, 8ms, 32ms, timeout disabled). Bypass mode is active only as long as there is UART activity. When there is no UART activity for the selected timeout, both the devices exit bypass mode and the bit is automatically cleared.

When set by the MS pin, a logic high puts the device into bypass mode while a logic low selects base mode. MS is set on the fly and is not latched on power-up.

UART Frame Format

Regular UART frames with an even parity bit are used to carry one byte of data each. A frame consists of a low start bit followed by eight data bits, a parity bit, and is finished with a high stop bit. The parity bit is high if the number of ones in the eight bits of data is odd. Otherwise, the parity bit is low. There must be at least one high stop bit. If the next frame is in the same packet, there can be at most four high bits from the end of the stop bit to the beginning of the next start bit. Note that for a parity bit error, the packet is discarded, starting from the frame with the error. The start of each frame is always a high-to-low transition (i.e., the stop bit is high and start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer calibrates the length of one UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions, and the recipient of the data must perform error checking. The parity bit (which is enabled by default in the bypass mode) can be disabled before entering the bypass mode. Note that the bit rate in the bypass mode must be the same bit rate last used in the base mode.

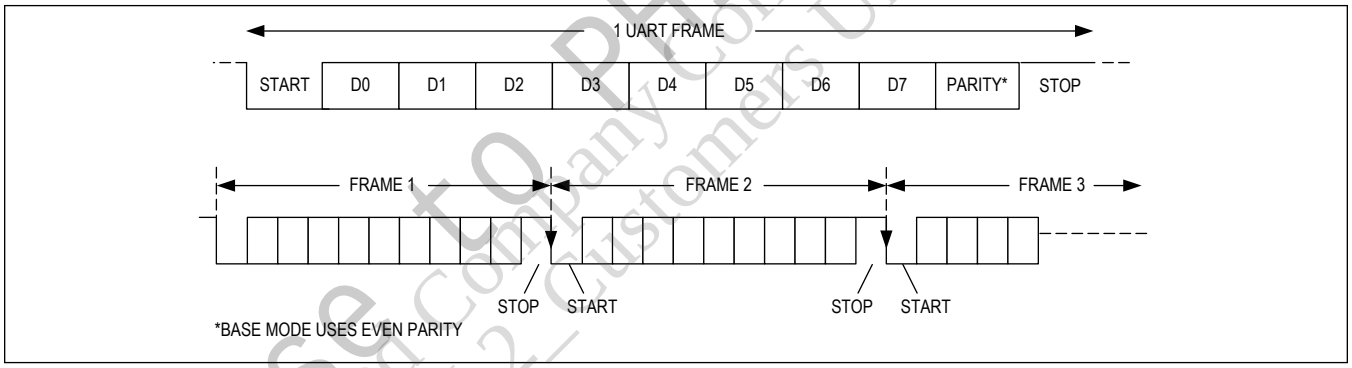

Figure 39. UART Data Format for Base Mode

Synchronization Frame

The serializer/deserializer must calibrate internal bit-length counters with the UART bit rate for proper recovery of UART frames. A sync frame (a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal 150MHz clock. Sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next sync frame.

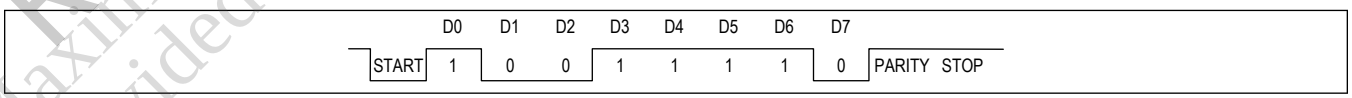

Figure 40. UART Synchronization Frame

Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC

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that no errors are detected in the transmitted packet, and it is recognized as valid. This is sent after the last bit of a successfully recognized packet is received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

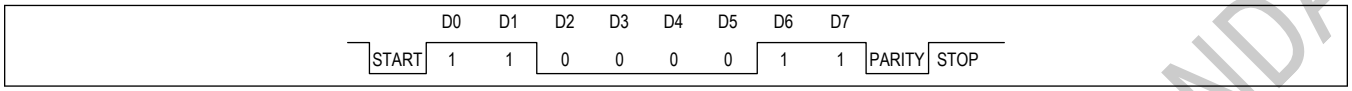

Figure 41. UART Acknowledge Frame

Write Packet

Write packets consist of a 5-byte packet header followed by one or more data bytes. A packet is recognized as a write packet when the LSB of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors are detected while receiving the write packet and the write packet is valid. Byte count indicates the number of data bytes to be written, and it cannot be 0.

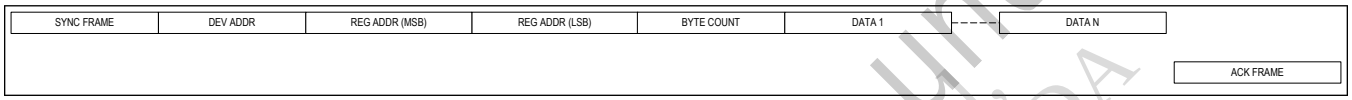

Figure 42. UART Write-Packet Format

Read Packet

Read packets consist of 5 bytes. The LSB of the device address frame is one for read packets. If no errors are detected while receiving the read packet and the packet is valid, the addressed device responds with an acknowledge frame followed by one or more data bytes. Byte count indicates the number of data bytes to be read, and it cannot be 0.

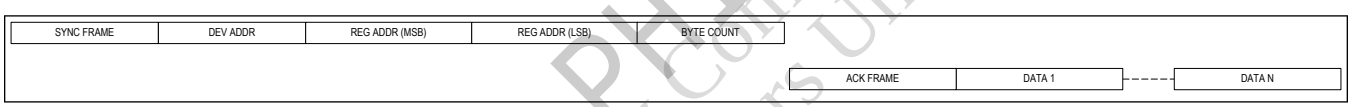

Figure 43. UART Read-Packet Format

I²C/UART Control-Channel Programming with CRC and Message Counter

By default, the I²C/UART CRC and Message Counter features are disabled in MAX96781/MAX96783. When desired, these functions are enabled using a legacy packet format register write. All subsequent transactions use the I²C/UART Control-Channel Programming with CRC and Message Counter format (ASIL-protected format).

I²C

To meet ASIL-B functional safety requirements, there must be a mechanism to prevent hardware faults or random errors from misconfiguring the device. Therefore, CRC is added to MAX96781/MAX96783 I²C transactions. The serializer I²C slave controller expects and validates an 8-bit Cyclic Redundancy Check (CRC-8) byte for all communication messages to maintain data integrity. This ensures the proper write data is received and the device is configured properly.

When directly communicating with the MAX96781/MAX96783 through the I²C interface, the ECU must compute and send a CRC byte protecting the data sent to the device. The incoming CRC byte is called a Packet Error Checking (PEC) byte. Likewise, for returned read packets (transactions), the ECU should store the received data, calculate the CRC, and compare the results to the received PEC byte provided by the MAX96781/MAX96783 before accepting the data received as valid.

To support PEC byte computation and checking, the ECU must implement a CRC-8 encoding and decoding algorithm based on the following polynomial (0xA6):

$$P(x) = x^8 + x^6 + x^3 + x^2 + 1$$

This polynomial protects a data stream of up to 247 bits with a Hamming Distance of 3, meaning any data stream of 247 bits or less in length with any combination of three bits of error or less is guaranteed to be identified. If more than three bits of error is encountered, the CRC operation is very likely to identify the problem, though this cannot be mathematically guaranteed.

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A hardware implementation of the CRC calculation is shown in Figure 44. The CRC engine shown is implemented internally within the MAX96781/MAX96783 I²C interface. A similar implementation is required in the ECU hardware or software to support direct I²C communication and generate the PEC bytes sent to the serializer or check the PEC bytes received from the serializer. The incoming I²C data stream is fed into the CRC engine, MSB first. Once the data stream is completely shifted into the engine, the CRC remainder is known; this becomes the PEC Byte for both the incoming write data and outgoing read data.

Note the ordering of the bits within the remainder. All I²C transactions supply the command and data stream, MSB first. Also, note the PEC byte itself is not included in the CRC calculation; it is only computed on the transaction header and data.

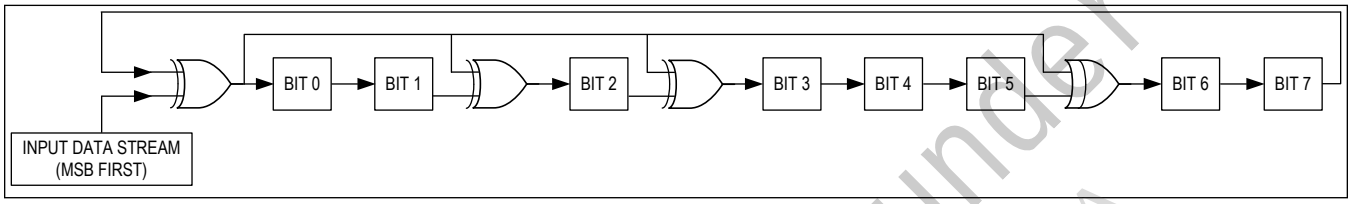

Figure 44. Hardware Implementation of CRC Calculation

I²C Write Transaction

For incoming I²C data streams, the MAX96781/MAX96783 first clear the CRC engine to 0 and then input the incoming data stream into the CRC engine, MSB first. After the final bit of data is processed (in this case, the LSB of the incoming data stream is applied to the engine), the engine is stopped, and the computed CRC remainder is known. The ECU calculates the PEC byte using its copy of the CRC engine and sends it within the I²C transaction (also MSB first). The serializer compares it against its calculated CRC remainder. If the PEC byte received matches the CRC remainder calculated for the incoming data stream, the PEC operation is successful, and the transaction is accepted and executed by the serializer.

If there is a mismatch:

- The write command is not executed.
- The slave controller NACKs the data packet.
- The transaction is retried.
- Readback of the serializer calculated PEC byte is possible (ACK/NACK can have errors).
- For critical writes, the ECU can also perform a readback of the written data to ensure success.
- The CRC mismatch triggers an error counter. The counter increments for each CRC error. Once the counter reaches a programmable threshold, ERRB asserts.

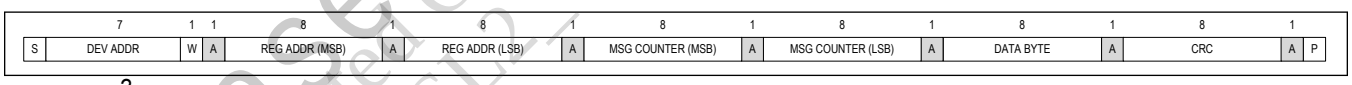

Figure 45. I²C Single-Byte Write Transactions with CRC

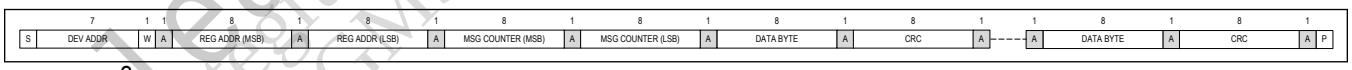

Figure 46. I²C Multiple-Byte Write Transactions with CRC

Figure 45 and Figure 46 show the I²C write transaction formatting with CRC PEC bytes added. The first CRC PEC byte covers the data for the first six bytes: Device Address, Register Address MSB, Register Address LSB, Message Counter MSB, Message Counter LSB, and the first data byte. If there are multiple data bytes after the first, then a CRC PEC byte is appended after each subsequent data byte. The CRC Engine is reset to 0 after each CRC calculation is completed, meaning a fresh CRC calculation is done each time. This prevents the number of data bits into the CRC engine from exceeding the 247 bits allowed by the polynomial.

I²C Read Transactions

For outgoing I²C data streams, the MAX96781/MAX96783 first clear the CRC engine to 0 and then provide the outgoing

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data stream to the CRC engine, MSB first. After the final bit of data is processed (in this case, the LSB of the outgoing data stream is applied to the engine), the engine is stopped. The CRC remainder is known, and this becomes the outgoing PEC byte. The outgoing PEC byte, as calculated by the serializer using its copy of the CRC engine, then follows within the I^{2}C transaction (also MSB first). As the ECU receives the data stream from the MAX96781/MAX96783, it should apply the data to its copy of the CRC engine (MSB first, in the order it arrives in the I^{2}C transaction, until the LSB of the data stream is applied to the engine). At this point, there are two equivalent ways the ECU can complete the PEC operation to establish the validity of the received data:

Direct Comparison Method: The ECU stops the CRC engine once the data stream MSB is applied and compares the resulting CRC remainder to the PEC byte supplied by the serializer (again, MSB first). If the two bytes match, the data is accepted as valid, otherwise, it should be rejected. This is the method employed by the MAX96781/MAX96783 internally during write transactions, as described above.

Zero Remainder Method: The ECU continues CRC engine computations after the data LSB is applied by appending the received PEC byte to the end of the data stream, MSB first (i.e., in the order received during the I^{2}C transaction). Once the LSB of the PEC byte arrives at the input of the CRC engine, if the resulting CRC remainder = 00h, the data is accepted as valid. Otherwise, it should be rejected.

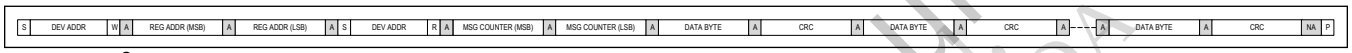

Figure 47. I^{2}C Multiple-Byte Read Transactions with CRC

Figure 47 shows the I^{2}C read transaction formatting with CRC PEC bytes added. The first CRC PEC byte covers the data for the first seven bytes: Device Address, Register Address MSB, Register Address LSB, repeated Device Address, Message Counter MSB, Message Counter LSB, and the first read data byte. If there are multiple read data bytes after the first, then a CRC PEC byte is appended after each subsequent read data byte. The CRC engine is reset to 0 after each CRC is calculated, meaning a fresh CRC calculation is done each time. This prevents the number of data bits into the CRC engine from exceeding the 247 bits allowed by the polynomial.

I^{2}C Message Counter

Another functional safety mechanism is a message counter that is part of each I^{2}C transaction. The ECU and MAX96781/MAX96783 devices must both keep a message counter. For each I^{2}C write or read transaction, each side increments their copy of the counter. For write transactions, the ECU sends the message count to the serializer as part of the I^{2}C transaction. The serializer then compares the received message count to its own. If it is a match, then the write command is accepted and executed as normal, assuming the CRC value also matches.

If the message count is mismatched, then the response is the same as the previously described case of a mismatched CRC:

- The write command is not executed.
- The slave controller NACKs the data packet.
- The transaction is retried.
- Readback of the serializer-calculated PEC byte is possible (ACK/NACK can have errors).
- For critical writes, the ECU can also perform a readback of the written data to ensure success.
- The CRC mismatch triggers an error counter. The counter increments for each CRC error. Once the counter reaches a programmable threshold, ERRB asserts.

For read transactions, the MAX96781/MAX96783 I^{2}C slave sends the message counter to the ECU, before the read data and CRC bytes. The ECU must then ensure its copy of the message counter matches the received value from the serializer. Also, the read transaction has a repeated start condition and device address byte. The message counter is incremented twice per read transaction, once when each device address byte matches. This is needed because a read can be initiated in two different ways. One is the way shown above, and the second is with only the second start condition and device address, immediately reading data from whatever is the last used register address. The MAX96781/MAX96783 support both types, therefore incrementing the message counter twice with the first way, and once with the second.

The safety feature described above can also be utilized between the MAX96781/MAX96783 and a compatible deserializer. It can also be used between the ECU and deserializer(s).

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I²C Additional Information

Communication transactions with other devices, such as deserializers or remote peripherals, can use the standard I²C protocol while the serializer is using the CRC and message counter protection. These transactions do not require the CRC PEC byte scheme or the message counter, and they are just passed through as-is. The ECU is free to communicate with the deserializer and remote peripherals using standard I²C protocol, the described PEC byte and message counter scheme, or another protection scheme if desired.

UART

From ASIL-B functional safety requirements, there must be a mechanism to prevent hardware faults or random errors from misconfiguring the device. Therefore, CRC is added to UART transactions. The MAX96781/MAX96783 UART slave controller expects and validates a CRC-8 byte for all communication messages to maintain data integrity. This ensures the proper write data is received and the device is configured properly.

When directly communicating with the serializer through the UART interface, the ECU must compute and send a CRC byte protecting the data sent to the device. The incoming CRC byte is called a Packet Error Checking (PEC) byte. Likewise, for returned read packets, the ECU should store the received data, perform the CRC calculation, and compare the results to the received PEC byte provided by the MAX96781/MAX96783 before accepting the data received as valid. To support PEC byte computation and checking, the ECU must implement a CRC-8 (8-bit Cyclic Redundancy Check) encoding and decoding algorithm based on the following polynomial (0xA6):

$$P(x) = x^8 + x^6 + x^3 + x^2 + 1$$

This polynomial is capable of protecting a data stream of up to 247 bits with a Hamming Distance of 3, meaning any data stream 247 bits or less in length with any combination of three bits of error or less is guaranteed to be identified. If more than three bits of error is encountered, the CRC operation is very likely to identify the problem, though this cannot be mathematically guaranteed. This Hamming Distance of 3 is in addition to the UART parity bit on each frame.

A hardware implementation of the CRC calculation is shown in Figure 44. The CRC Engine shown is implemented internally within the MAX96781/MAX96783 UART interface.

A similar implementation is required in the ECU hardware or software to support direct UART communication, to generate the PEC bytes sent to the serializer, or to check PEC bytes received from the serializer. The incoming UART data stream is fed into the CRC Engine LSB first. Once the data stream is completely shifted into the engine, the CRC remainder is known; this becomes the PEC byte for both incoming write data and outgoing read data. Note the ordering of the bits within the remainder. Note that all UART transactions supply the command and data stream LSB first. Also, note that the PEC byte itself is not included in the CRC calculation; it is only computed on the packet header and data.

UART Write Transactions

For incoming UART data streams, the MAX96781/MAX96783 first clear the CRC engine to 0 and then input the incoming data stream into the CRC engine, MSB first. After the final bit of data is processed (in this case, the LSB of the incoming data stream is applied to the engine), the engine is stopped, and the computed CRC remainder is known. The ECU calculates the PEC byte using its copy of the CRC engine and sends it within the UART transaction (also MSB first). The serializer compares it against its calculated CRC remainder. If the PEC byte received matches the CRC remainder calculated for the incoming data stream, the PEC operation is successful, and the transaction is accepted and executed by the serializer.

If there is a mismatch:

- The write command is not executed.
- The slave controller NACKs the data packet.
- The transaction is retried.
- Readback of the MAX96781/MAX96783 calculated PEC byte is possible (ACK/NACK can have errors).
- For critical writes, the ECU can also perform a readback of the written data to ensure success.
- The CRC mismatch triggers an error counter. The counter increments for each CRC error. Once the counter reaches a programmable threshold, ERRB asserts.

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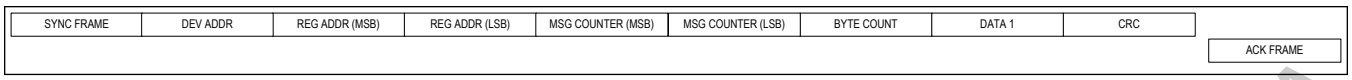

Figure 48. UART Single-Byte Write Packet with CRC

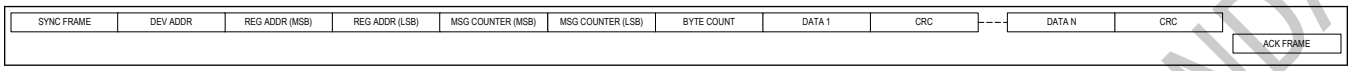

Figure 49. UART Multiple-Byte Write Packet with CRC

Figure 48 and Figure 49 show the UART write packet formatting with CRC PEC bytes added. The first CRC PEC byte covers the data for the first eight frames: Sync Frame, Dev Addr, Reg Addr MSB, Reg Addr LSB, Message Counter MSB, Message Counter LSB, Byte Count, and the first data byte. If there are multiple data bytes after the first, then a CRC PEC byte is appended after each subsequent data byte. The CRC engine is reset to 0 after each CRC is calculated, meaning a fresh CRC calculation is done each time. This prevents the number of data bits into the CRC engine from exceeding the 247 bits allowed by the polynomial.

UART Read Transactions

For outgoing UART data streams, the MAX96781/MAX96783 first clear the CRC engine to 0 and then provide the outgoing data stream to the CRC engine, MSB first. After the final bit of data is processed (in this case, the LSB of the outgoing data stream is applied to the engine), the engine is stopped. The CRC remainder is known, and this becomes the outgoing PEC byte. The outgoing PEC byte, as calculated by the serializer using its copy of the CRC engine, then follows within the UART transaction (also MSB first). As the ECU receives the data stream from the MAX96781/MAX96783, it should apply the data to its copy of the CRC engine (MSB first, in the order it arrives in the UART transaction, until the LSB of the data stream is applied to the engine). At this point, there are two equivalent ways the ECU can complete the PEC operation to establish the validity of the received data:

Direct Comparison Method: The ECU stops the CRC engine once the data stream MSB is applied and compares the resulting CRC remainder to the PEC byte supplied by the MAX96781/MAX96783 (again, LSB first). If the two bytes match, the data is accepted as valid. Otherwise, it should be rejected. This is the method employed by the serializer internally, as described above.

Zero Remainder Method: The ECU continues CRC engine computations after the data MSB is applied by appending the received PEC byte to the end of the data stream, LSB first (i.e., in the order received during the UART transaction). Once the MSB of the PEC byte arrives at the input of the CRC engine, if the resulting CRC remainder = 00h, the data is accepted as valid. Otherwise, it should be rejected.

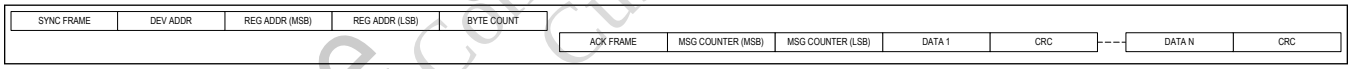

Figure 50. UART Multiple-Byte Read Packet with CRC

Figure 50 shows the UART read packet formatting with CRC PEC bytes added. The first CRC PEC byte covers the data for the first seven frames plus the first data byte: Sync Frame, Dev Addr, Reg Addr MSB, Reg Addr LSB, Message Counter MSB, Message Counter LSB, Byte Count, and the first data byte. If there are multiple read data bytes after the first, then a CRC PEC byte is appended after each subsequent read data byte. There is no CRC on the ACK Frame. This is because when the master waits for the ACK Frame, it waits for a specific value, 0xC3. If there is a bit error on the ACK Frame, the master does not detect the ACK, it is treated as a NACK, and the transaction is retried. The CRC engine is reset to 0 after each CRC is calculated, meaning a fresh CRC calculation is done each time. This prevents the number of data bits into the CRC engine from exceeding the 247 bits allowed by the polynomial.

UART Message Counter

Another functional safety mechanism is a message counter part of each UART packet. The ECU and MAX96781/MAX96783 device both keep a message counter. For each UART write or read packet, each side increments its copy of the counter. For write packets, the ECU sends the message count to the MAX96781/MAX96783 as part of the UART packet. The serializer then compares the received message count to its own. If it is a match, then the write command is accepted and executed as normal, assuming the CRC value also matches.

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If the message count is a mismatch (same as if a CRC mismatch):

- The write command is not executed.
- The slave controller NACKs the data packet.
- The transaction is retried.
- Readback of the MAX96781/MAX96783 calculated PEC byte is possible (ACK/NACK can have errors).
- For critical writes, the ECU can also perform a readback of the written data to ensure success.
- The CRC mismatch triggers an error counter. The counter increments for each CRC error. Once the counter reaches a programmable threshold, ERRB asserts.

For read packets, the MAX96781/MAX96783 UART slave sends the message counter to the ECU, before the read data and CRC bytes. The ECU must then ensure its copy of the message counter matches the received value from the serializer.

The safety feature described above can also be utilized between the MAX96781/MAX96783 and a compatible deserializer. It can also be used between the ECU and deserializer(s).

UART Additional Information

The UART can also operate in the bypass mode when CRC and message counter are enabled. In this case, UART packets are transferred from the ECU to the serializer, through the GMSL link to the deserializer and then to a peripheral. These packets do not have this CRC PEC byte scheme, nor the message counter, and are just passed through as-is. The ECU and peripheral are free to use some other CRC scheme if preferred, but the CRC described here only applies to packets to the serializer or deserializer registers.

Additional Control-Channel Features

GMSL1 Control Channel Options

Each GMSL1 link can support a single main remote control channel connection. This is consistent with the functionality of all legacy GMSL1 deserializers.

The local channel routed to each link's remote control channel can be configured independently. Any of the three internal I^2C/UART channels can be used. Regardless of the channel that is specified, it must use the same operating mode (I^2C vs. UART) as the main local control channel. The specified remote control channel does not have any impact on the local control channel or the remote control channel/passthrough configuration used by the other link.

In GMSL1 mode, only a single main remote control channel is available. There is not support for dedicated tunneled passthrough channels. As a result, the PT1 ASIL readback function is not available for remote devices. It is always available for local readback regardless of link configuration.

The I^2C/UART crossbar function can be used to route any pair of physical I^2C/UART pins to any internal communication channel.

Figure 51 details the available routing options. Note the presence of the remote control channel multiplexer associated with each GMSL1 link. This feature is unique to GMSL1 configured links.

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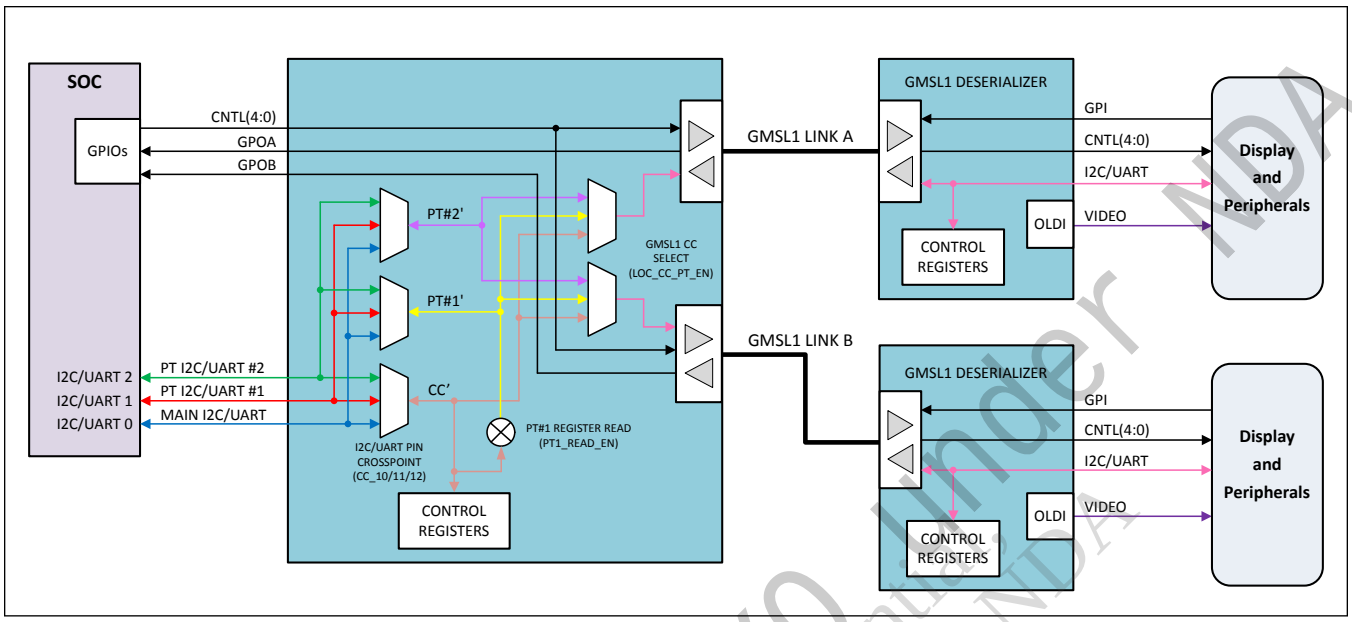

Figure 51. GMSL1 Control Channel Options

GMSL2 Control Channel Options

Each GMSL2 link can support a single main remote control channel connection. This is consistent with the functionality of all GMSL2 deserializers.

The MAX96781/MAX96783 does not support arbitrary routing of internal communication channels to the GMSL2 link main remote control channel. In GMSL2 mode, the remote control channel of each link must always be the main local control channel.

The I^{2}C/UART crossbar function enables flexible routing between the physical I^{2}C/UART pin pairs and each internal communication channel.

Two dedicated tunneled passthrough channels are available. For GMSL2 links, the operating mode of each port (I^{2}C vs. UART) can be independently configured.

PT1 ASIL register readback is available for local registers regardless of link configuration. Some GMSL2 deserializers also support remote PT1 register readback. This function is not available in GMSL1 mode.

Figure 52 details the available routing options.

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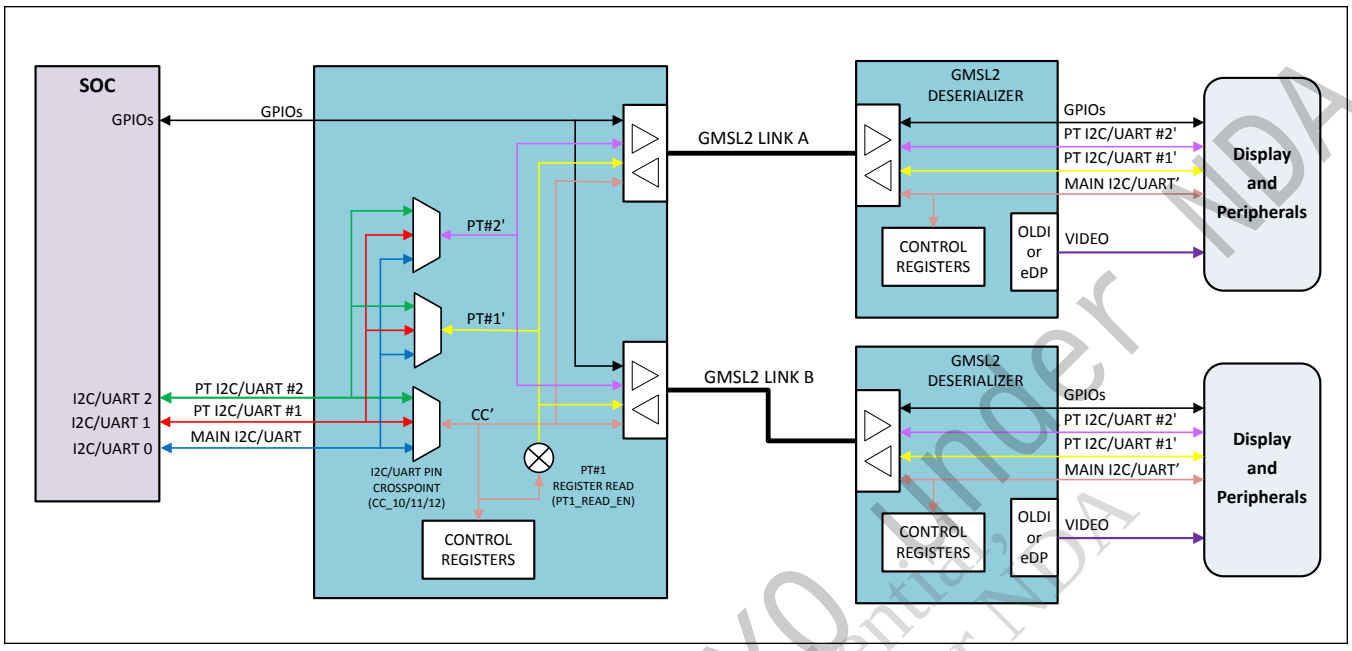

Figure 52. GMSL2 Control Channel Options

Full I²C Crossbar

There is a full crossbar between CC, PT1, and PT2 pins, and GMSL CC, PT1, and PT2 channels. This allows any one set of CC, PT1, and PT2 pins to connect to any internal channel. The I²C-over-AUX is also included in the crossbar, enabling it to connect to the internal CC, PT1, or PT2 channels or to the CC, PT1, or PT2 external pins.

PT1 Local/Remote Register Read

The pass-through I²C1/UART1 channel (PT1) has an additional feature in support of ASIL system design.

PT1 can be used to verify (read) the main local/remote registers to verify the main channel I²C/UART registers are correctly written. In compatible deserializers, the remote (deserializer) register read remains available even if the remote control channel is disabled (DIS_REM_CC pin). The maximum transaction length allowed for both the I²C main and PT1 is 32 bytes when this mode is used. Prior to using PT1 register read access, set SLV_TO = 110 (32ms) and SLV_TO_PT_1 = 110 (32ms).

When UART is used to read registers on PT1, the read response is delayed if another packet is active on the main control channel.

The allowed, collision-free configurations are as follows:

- Main I²C/UART read/write and local PT1 read.
- Main I²C/UART read/write and remote PT1 read.

See Figure 53 for details of the supported collision-free configurations.

When this function is disabled, the PT1 port functions as a normal I²C/UART passthrough.

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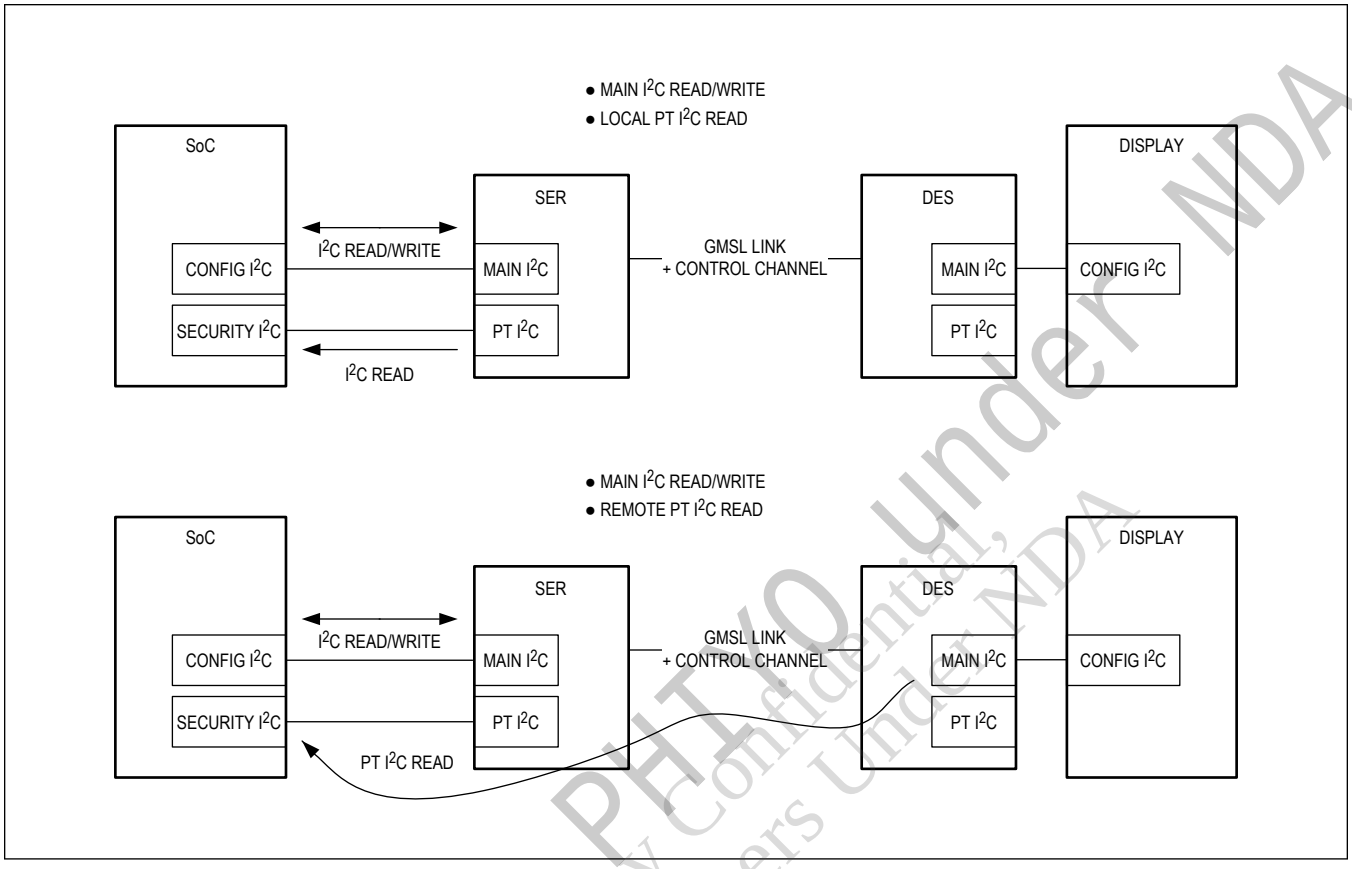

Figure 53. Collision-Free PT1 Register Reads

Bussed I2C Pass-Through

In legacy GMSL2 PT designs, it was only possible to support point-to-point I2C PT links between one serializer and one deserializer. If PT was enabled in multiple deserializers, the serializer could not differentiate the packets from different deserializers.

In MAX96781/MAX96783 designs using splitter mode, bussed connection is supported where each PT channel can be enabled in both deserializers if desired.

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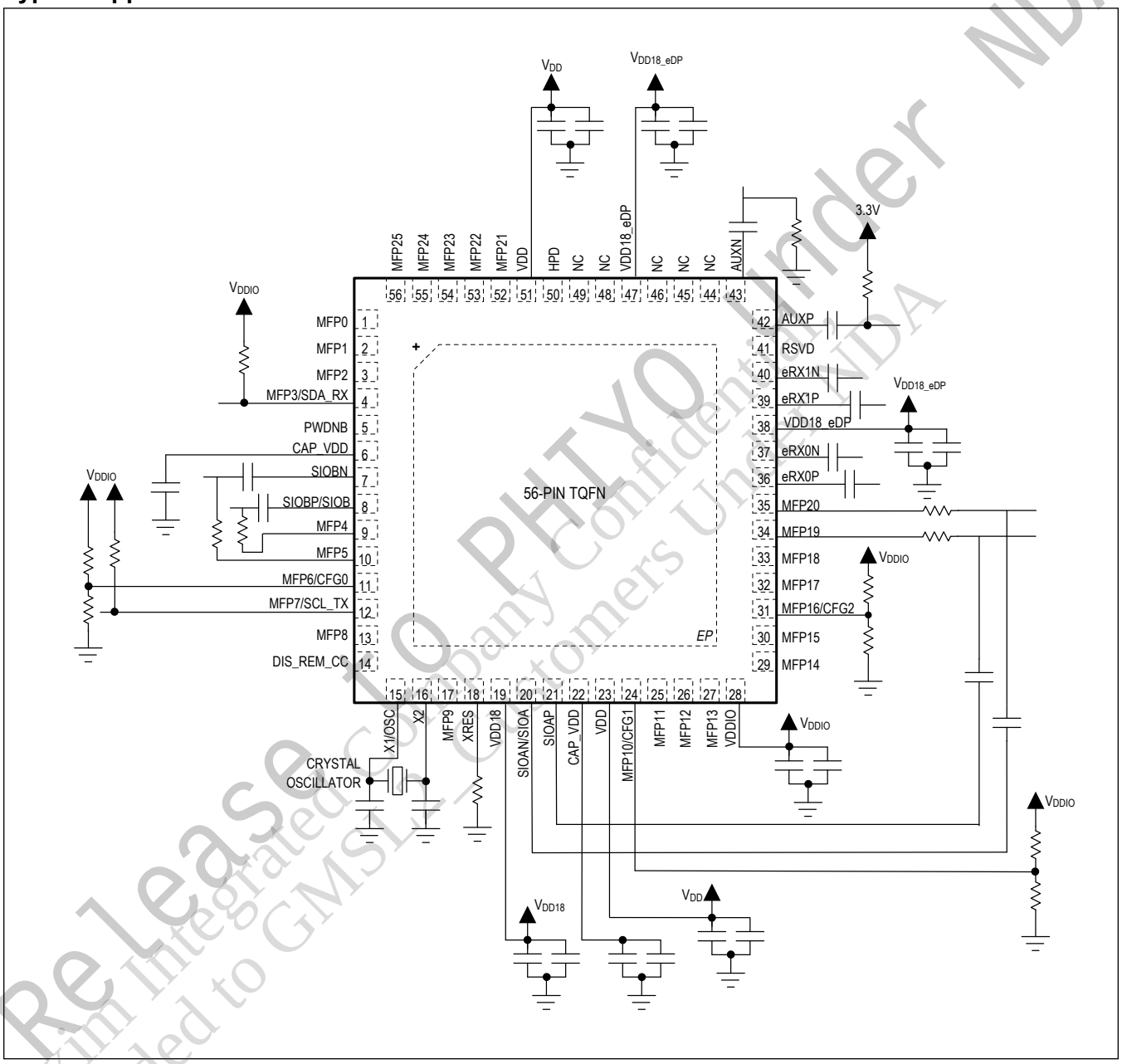
Typical Application Circuits

Typical Application Circuit



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Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	HDCP
MAX96781GTN/V+	-40°C to +105°C	56-lead TQFN-EP*	No
MAX96781GTN/V+T	-40°C to +105°C	56-lead TQFN-EP*	No
MAX96781GTN/VY+	-40°C to +105°C	56-Lead SWQFN-EP*	No
MAX96781GTN/VY+T	-40°C to +105°C	56-Lead SWQFN-EP*	No
MAX96783GTN/V+***	-40°C to +105°C	56-lead TQFN-EP*	Yes**
MAX96783GTN/V+T***	-40°C to +105°C	56-lead TQFN-EP*	Yes**
MAX96783GTN/VY+***	-40°C to +105°C	56-Lead SWQFN-EP*	Yes**
MAX96783GTN/VY+T***	-40°C to +105°C	56-Lead SWQFN-EP*	Yes**

/V Denotes an automotive qualified part

Y Denotes side-wettable package

+ Denotes a lead(Pb)-free/RoHS-compliant package

T Denotes tape and reel

EP Denotes Exposed Pad*

***HDCP parts require registration with Digital Content Protection, LLC*

****Future product – contact factory for availability*

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Register Map

Reserved, Unused, and Read-Only Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write).

In this document default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

Note: *Indicates the register is stored when entering sleep mode and is restored upon exit.

HDCP (MAX96783 Only)

The MAX96783 has HDCP while the MAX96781 does not. Register blocks (shown below), registers, and bitfields that refer to HDCP are reserved in the MAX96781 and should not be changed from the default state.

Table 31. **HDCP Register Blocks (MAX96783 Only)**

BLOCK NAME	REGISTER ADDRESS NAME
CFGL_AHDCP	0x00E0–0x00E7
HDCP_TX__HX	0x1600–0x16FF
HDCP_TX__HY	0x1700–0x17FF

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x80	REG0[7:0]*	DEV_ADDR[6:0]							CFG_BLOCK
0x02	0x83	REG2[7:0]*	AUD_TX_Y_SRC	AUD_TX_X_SRC	AUD_TX_EN_Y	AUD_TX_EN_X	–	–	RSVD	RSVD
0x03	0x00	REG3[7:0]*	–	–	–	I2CSEL	RCLKEN	–	RCLKSEL[1:0]	
0x04	0x0D	REG4[7:0]*	GMSL1_B	GMSL1_A	HVD_OUT_EN	DIS_LOCAL_CC	RSVD	RSVD	PAR_VID_EN	SW_INT
0x05	0xC0	REG5[7:0]*	LOCK_EN	ERRB_EN	–	LOCK_CFG	PU_LF3	PU_LF2	PU_LF1	PU_LF0
0x08	0x00	PWR0[7:0]	VDDBAD_STATUS[1:0]		CMP_STATUS[5:0]					
0x09	0x00	PWR1[7:0]	RSVD	VDDBAD_STATUS_H	RSVD[5:0]					
0x0C	0x35	PWR4[7:0]*	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			
0x0D	0xFF	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x00	REG14[7:0]	–	–	RSVD	RSVD	DEV_REV[3:0]			
0x0F	0x00	REG15[7:0]	RSVD	–	RSVD[1:0]		–	DUAL_CPBL_N	SPLTR_CPBL_N	HDCP_CPBL
TCTRL										
0x10	0x11	CTRL0[7:0]*	RESET_ALL	–	–	AUTO_LINK	SLEEP	RSVD	LINK_CFG[1:0]	
0x11	0x0A	CTRL1[7:0]*	RSVD	RSVD	RSVD	–	RSVD	CXTP_B	RSVD	CXTP_A

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ADDRESS	RESET	NAME	MSB							LSB
0x13	0x00	CTRL3[7:0]	HPD_IN	–	–	–	LOCKED	ERROR	CMU_LOCKED	–
0x18	0x00	INTR0[7:0]*	–	–	–	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x19	0x00	INTR1[7:0]*	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x1A	0x0B	INTR2[7:0]*	RSVD	RSVD	–	REM_ERR_OEN_A	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
0x1B	0x00	INTR3[7:0]	RSVD	RSVD	–	REM_ERR_FLAG_A	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x1C	0x08	INTR4[7:0]*	RSVD	RSVD	–	HDCP_INT_OEN_A	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	–
0x1D	0x00	INTR5[7:0]	RSVD	RSVD	–	HDCP_INT_FLAG_A	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	–
0x1E	0xE0	INTR6[7:0]*	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	VDD_OV_OEN	DPRX_INT_OEN	–	–	INT_ERR_OEN
0x1F	0x00	INTR7[7:0]	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	VDD_OV_FLAG	DPRX_INT	–	–	INT_ERR_FLAG
0x20	0x00	INTR8[7:0]*	SW_INT_OEN	VDDIO_OV_OEN	VDD1P8_OV_OEN	RSVD	LOCK_B_OEN	LOCK_A_OEN	LOCK_OEN	LOSS_OF_LOCK_OEN
0x21	0x00	INTR9[7:0]	SW_INT_FLAG	VDDIO_OV_FLAG	VDD1P8_OV_FLAG	VREG_OV_FLAG	LOCK_B_FLAG	LOCK_A_FLAG	LOCK_FLAG	LOSS_OF_LOCK_FLAG
0x22	0x00	INTR10[7:0]*	LFLT_INT_OPEN_OEN	LFLT_INT_L2LS_OEN	LFLT_INT_BAT_S_OEN	LFLT_INT_GND_S_OEN	REG_CRC_ERR_OEN	I2C_UART_MSG CNTR_ERR_OEN	I2C_UART_CRC_ERR_OEN	–
0x23	0x00	INTR11[7:0]	LFLT_INT_OPEN	LFLT_INT_L2LS	LFLT_INT_BAT_S	LFLT_INT_GND_S	REG_CRC_ERR_FLAG	I2C_UART_MSG CNTR_ERR_FLAG	I2C_UART_CRC_ERR_FLAG	–
0x24	0x30	DEV_ID16_LSB[7:0]*	DEV_ID16_LSB[7:0]							
0x25	0x00	DEV_ID16_MSB[7:0]*	DEV_ID16_MSB[7:0]							
0x26	0x22	LF0_LF1[7:0]	–	LF_1[2:0]			–	LF_0[2:0]		
0x27	0x22	LF2_LF3[7:0]	–	LF_3[2:0]			–	LF_2[2:0]		
LINK_CTRL A										
0x28	0x88	LCTRL0[7:0]*	LINK_EN	–	–	–	TX_RATE[1:0]		RSVD[1:0]	
0x29	0x00	LCTRL1[7:0]*	–	RSVD	RSVD	RSVD	–	–	RESET_ONESHOT	RESET_LINK

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ADDRESS	RESET	NAME	MSB							LSB
0x2A	0x00	LCTRL2[7:0]	–	–	–	–	–	RSVD	RSVD	LINK_LOCKED
0x2B	0x00	LCTRL3[7:0]	DEC_ERR[7:0]							
0x2C	0x00	LCTRL4[7:0]	IDLE_ERR[7:0]							
0x2D	0x00	LCTRL5[7:0]	PKT_CNT[7:0]							
0x2E	0x9F	LCTRL6[7:0]*	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x2F	0xDF	LCTRL7[7:0]*	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
0x30	0x5E	LCTRL8[7:0]*	ERR_RX_EN2	RSVD	–	ERR_RX_ID2[4:0]				
0x31	0x5B	LCTRL9[7:0]*	ERR_RX_EN3	RSVD	–	ERR_RX_ID3[4:0]				
LINK_CTRL B										
0x32	0x80	LCTRL0[7:0]*	LINK_EN	–	–	–	–	–	–	–
0x35	0x00	LCTRL3[7:0]	DEC_ERR[7:0]							
0x36	0x00	LCTRL4[7:0]	IDLE_ERR[7:0]							
0x37	0x00	LCTRL5[7:0]	PKT_CNT[7:0]							
GMSL A										
0x51	0x00	TX1[7:0]*	LINK_PRBS_GEN	–	–	ERRG_EN	–	–	RSVD	RSVD
0x52	0x20	TX2[7:0]*	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x53	0x54	TX3[7:0]*	RSVD[1:0]		RSVD	RSVD[1:0]		TIMEOUT[2:0]		
0x54	0x00	RX0[7:0]*	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
0x55	0x34	RX1[7:0]	LINK_PRBS_CHK	RSVD	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD
0x57	0x00	RX3[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FAILLOCK
0x58	0x41	GPIOA[7:0]*	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
0x59	0x88	GPIOB[7:0]*	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
GMSL__B										
0x61	0x00	TX1[7:0]	–	–	–	ERRG_EN	–	–	–	–
CC A										
0x70	0x23	I2C_0[7:0]*	–	I2C_HSM	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x71	0x52	I2C_1[7:0]*	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x72	0x00	I2C_2[7:0]*	SRC_A[6:0]							–
0x73	0x00	I2C_3[7:0]*	DST_A[6:0]							–
0x74	0x00	I2C_4[7:0]*	SRC_B[6:0]							–
0x75	0x00	I2C_5[7:0]*	DST_B[6:0]							–

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ADDRESS	RESET	NAME	MSB							LSB
0x76	0x18	I2C_6[7:0]*	DIS_REM_CC	–	–	RSVD	I2C_AUTO_CFG	–	I2C_SRC_CNT[1:0]	
0x78	0x60	UART_0[7:0]*	RSVD[1:0]		RSVD[1:0]		–	–	–	REM_MS_EN
0x79	0x00	PT_0[7:0]*	PT_I2C_SRC_CNT_2[1:0]		PT_I2C_SRC_CNT_1[1:0]		–	–	CC_2_EN	CC_1_EN
0x7B	0x00	PT_2[7:0]*	PT_SRC_1[6:0]							–
0x7C	0x00	PT_3[7:0]*	PT_DST_1[6:0]							–
0x7D	0x00	PT_4[7:0]*	PT_SRC_2[6:0]							–
0x7E	0x00	PT_5[7:0]*	PT_DST_2[6:0]							–
CC_CMN										
0x90	0x02	CC_0[7:0]*	–	–	EN_I2C_LOOPBACK	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
0x91	0x1D	CC_1[7:0]*	–	–	–	REM_MS_ID[4:0]				
0x94	0x96	CC_4[7:0]	BITLEN_LSB[7:0]							
0x95	0x00	CC_5[7:0]	–	–	BITLEN_MSB[5:0]					
0x96	0x2B	CC_6[7:0]*	BITLEN_MAN_CFG_1	DIS_PAR_1	SLV_SH_PT_1[1:0]		I2CSEL_1	SLV_TO_PT_1[2:0]		
0x97	0x52	CC_7[7:0]*	RSVD	MST_BT_PT_1[2:0]			I2C_HSM_PT_1	MST_TO_PT_1[2:0]		
0x98	0x2B	CC_8[7:0]*	BITLEN_MAN_CFG_2	DIS_PAR_2	SLV_SH_PT_2[1:0]		I2CSEL_2	SLV_TO_PT_2[2:0]		
0x99	0x52	CC_9[7:0]*	RSVD	MST_BT_PT_2[2:0]			I2C_HSM_PT_2	MST_TO_PT_2[2:0]		
0x9A	0x01	CC_10[7:0]*	–	I2C_OVER_AUX_TO_CC_PINS_EN	–	–	I2C_OVER_AUX_TO_GMSL_CC_EN	PT2_PINS_TO_GMSL_CC_EN	PT1_PINS_TO_GMSL_CC_EN	CC_PINS_TO_GMSL_CC_EN
0x9B	0x02	CC_11[7:0]*	–	I2C_OVER_AUX_TO_PT1_PINS_EN	–	PT1_LOOPBACK_TO_GMSL_CC_EN	I2C_OVER_AUX_TO_GMSL_PT1_EN	PT2_PINS_TO_GMSL_PT1_EN	PT1_PINS_TO_GMSL_PT1_EN	CC_PINS_TO_GMSL_PT1_EN
0x9C	0x04	CC_12[7:0]*	–	I2C_OVER_AUX_TO_PT2_PINS_EN	–	PT2_LOOPBACK_TO_GMSL_CC_EN	I2C_OVER_AUX_TO_GMSL_PT2_EN	PT2_PINS_TO_GMSL_PT2_EN	PT1_PINS_TO_GMSL_PT2_EN	CC_PINS_TO_GMSL_PT2_EN
0x9D	0x08	CC_13[7:0]*	–	–	–	–	AHCC_AUTO_CFG_A	–	–	AHCC_SRC_CNT_A
0x9E	0x03	CC_14[7:0]*	–	–	–	PT1_READ_EN	–	–	PT_I2C_AUTO_CFG_2	PT_I2C_AUTO_CFG_1

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ADDRESS	RESET	NAME	MSB							LSB
CFGV VIDEO_X										
0xA0	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA1	0xB0	TX1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xA3	0x10	TX3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	–	TX_STR_SEL[1:0]	
CFGV VIDEO_Y										
0xA4	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA5	0xB0	TX1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xA7	0x21	TX3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	–	TX_STR_SEL[1:0]	
CFGS AUDIO_X										
0xB0	0xF0	TR0[7:0]*	TX_CRC_EN	RSVD	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xB1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xB3	0x10	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xB5	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN
0xB6	0x22	ARQ1[7:0]*	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xB7	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGS AUDIO_Y										
0xB8	0xF0	TR0[7:0]*	TX_CRC_EN	RSVD	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xB9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xBB	0x21	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xBD	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN
0xBE	0x22	ARQ1[7:0]*	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xBF	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGI INFOFR										
0xC0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xC1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xC3	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0xC4	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
CFGS SPI										
0xC8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xC9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xCB	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xCC	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xCD	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN
0xCE	0x22	ARQ1[7:0]*	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xCF	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL CC										
0xD0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xD1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xD3	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xD4	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xD5	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN_A
0xD6	0x22	ARQ1[7:0]*	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xD7	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
CFGL GPIO										
0xD8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xD9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xDB	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xDC	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xDD	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN_A
0xDE	0x22	ARQ1[7:0]*	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xDF	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
CFGL AHDCP										
0xE0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xE1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					

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0xE3	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xE4	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xE5	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN_A
0xE6	0x22	ARQ1[7:0]*	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xE7	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
CFGL IIC_X										
0xE8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xE9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xEB	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xEC	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xED	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN_A
0xEE	0x22	ARQ1[7:0]*	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xEF	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
CFGL IIC_Y										
0xF0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xF1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xF3	0x30	TR3[7:0]*	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0xF4	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0xF5	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN_A
0xF6	0x22	ARQ1[7:0]*	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xF7	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
VID_TX X										
0x100	0x61	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	–	–	VID_TX_EN
0x102	0x0A	VIDEO_TX2[7:0]*	PCLKDET_A	DRIFT_ERR_A	OVERFLOW_A	FIFO_WARN_A	RSVD	LIM_HEART	RSVD	RSVD
0x106	0x00	VIDEO_TX6[7:0]*	RSVD	MASK_VIDEO_DE	RSVD[5:0]					

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ADDRESS	RESET	NAME	MSB							LSB
VID_TX Y										
0x110	0x61	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	–	–	VID_TX_EN
0x112	0x0A	VIDEO_TX2[7:0]*	PCLKDET_A	DRIFT_ERR_A	OVERFLOW_A	FIFO_WARN_A	RSVD	LIM_HEART	RSVD	RSVD
0x116	0x00	VIDEO_TX6[7:0]*	RSVD	MASK_VIDEO_DE	RSVD[5:0]					
AUD_TX X										
0x140	0x00	AUDIO_TX0[7:0]*	–	–	–	–	INV_SCK	INV_WS	FORCE_AUD	–
0x141	0x4C	AUDIO_TX1[7:0]*	RSVD[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	–	AUD_HDCP_SEL
0x145	0x00	AUDIO_TX5[7:0]	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
0x147	0x00	AUDIO_TX7[7:0]	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
0x148	0x40	AUDIO_TX8[7:0]	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
AUD_TX Y										
0x150	0x00	AUDIO_TX0[7:0]*	–	–	–	–	INV_SCK	INV_WS	FORCE_AUD	–
0x151	0x5C	AUDIO_TX1[7:0]*	RSVD[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	–	AUD_HDCP_SEL
0x155	0x00	AUDIO_TX5[7:0]	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
0x157	0x00	AUDIO_TX7[7:0]	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
0x158	0x40	AUDIO_TX8[7:0]	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
SPI										
0x1A0	0x08	SPI_0[7:0]*	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
0x1A1	0x1D	SPI_1[7:0]*	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
0x1A2	0x03	SPI_2[7:0]*	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
0x1A3	0x00	SPI_3[7:0]*	SPIM_SS_DLY_CLKS[7:0]							
0x1A4	0x00	SPI_4[7:0]*	SPIM_SCK_LO_CLKS[7:0]							
0x1A5	0x00	SPI_5[7:0]*	SPIM_SCK_HI_CLKS[7:0]							
0x1A6	0x03	SPI_6[7:0]*	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN

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ADDRESS	RESET	NAME	MSB							LSB
0x1A7	0x00	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
0x1A8	0x00	SPI_8[7:0]*	REQ_HOLD_OFF_TO[7:0]							
WM										
0x1C0	0x80	WM_0[7:0]*	WM_AUTO_SYNC_EN_X	WM_MODE_X[2:0]			–	–	–	WM_EN_X
0x1C1	0x19	WM_1[7:0]*	WM_HS POL_X	WM_VS POL_X	RSVD[1:0]		RSVD[3:0]			
0x1C2	0x80	WM_2[7:0]*	WM_AUTO_SYNC_EN_Y	WM_MODE_Y[2:0]			–	–	–	WM_EN_Y
0x1C3	0x19	WM_3[7:0]*	WM_HS POL_Y	WM_VS POL_Y	WM_KO_Y[1:0]		WM_NO_Y[3:0]			
0x1DE	0x00	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x1DF	0x00	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
GPIOC 0										
0x200	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x201	0x80	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x202	0x40	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x203	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
0x204	0x00	GPIO_E[7:0]*	–	–	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x205	0x00	GPIO_F[7:0]*	–	–	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x206	0x00	GPIO_G[7:0]*	–	–	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 1										
0x208	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x209	0x81	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x20A	0x41	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x20B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
0x20C	0x00	GPIO_E[7:0]*	–	–	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				

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0x20D	0x00	GPIO_F[7:0]*	–	–	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x20E	0x00	GPIO_G[7:0]*	–	–	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIO 2										
0x210	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x211	0x82	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x212	0x42	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x213	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 3										
0x218	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x219	0x83	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		–	GPIO_TX_ID[4:0]				
0x21A	0x03	GPIO_C[7:0]*	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
0x21B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 4										
0x220	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x221	0x84	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x222	0x64	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x223	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 5										
0x228	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x229	0x85	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x22A	0x65	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x22B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 6										
0x230	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x231	0x26	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x232	0x66	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x233	0x00	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 7										
0x238	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x239	0x87	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		–	GPIO_TX_ID[4:0]				
0x23A	0x07	GPIO_C[7:0]*	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
0x23B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 8										
0x240	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x241	0x88	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x242	0x68	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x243	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 9										
0x248	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x249	0x89	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x24A	0x69	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x24B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 10										
0x250	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x251	0x2A	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x252	0x6A	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x253	0x00	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 11										
0x258	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x259	0x8B	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x25A	0x4B	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x25B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A

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GPIO 12										
0x260	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x261	0x8C	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x262	0x4C	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x263	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 13										
0x268	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x269	0x8D	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x26A	0x4D	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x26B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 14										
0x270	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x271	0x8E	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x272	0x4E	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x273	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 15										
0x278	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x279	0x8F	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x27A	0x4F	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x27B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 16										
0x280	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x281	0x30	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x282	0x50	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x283	0x00	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 17										
0x288	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS

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0x289	0x91	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x28A	0x51	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x28B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 18										
0x290	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x291	0x92	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x292	0x52	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x293	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 19										
0x298	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x299	0x93	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x29A	0x73	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x29B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 20										
0x2A0	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2A1	0x94	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2A2	0x74	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2A3	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIOC 21										
0x2A8	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2A9	0x95	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2AA	0x55	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2AB	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
0x2AC	0x00	GPIO_E[7:0]*	–	–	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2AD	0x00	GPIO_F[7:0]*	–	–	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				

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0x2AE	0x00	GPIO_G[7:0]*	–	–	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 22										
0x2B0	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2B1	0x96	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B2	0x56	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2B3	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
0x2B4	0x00	GPIO_E[7:0]*	–	–	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2B5	0x00	GPIO_F[7:0]*	–	–	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2B6	0x00	GPIO_G[7:0]*	–	–	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 23										
0x2B8	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2B9	0x97	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2BA	0x57	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2BB	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
0x2BC	0x00	GPIO_E[7:0]*	–	–	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2BD	0x00	GPIO_F[7:0]*	–	–	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2BE	0x00	GPIO_G[7:0]*	–	–	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 24										
0x2C0	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2C1	0x98	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C2	0x58	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2C3	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A

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0x2C4	0x00	GPIO_E[7:0]*	–	–	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2C5	0x00	GPIO_F[7:0]*	–	–	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2C6	0x00	GPIO_G[7:0]*	–	–	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 25										
0x2C8	0x91	GPIO_A[7:0]*	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2C9	0x99	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CA	0x59	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2CB	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
0x2CC	0x00	GPIO_E[7:0]*	–	–	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2CD	0x00	GPIO_F[7:0]*	–	–	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2CE	0x00	GPIO_G[7:0]*	–	–	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIO_RECVED										
0x2F8	0xFF	GPIO_RX_0[7:0]*	GPIO_RECVED_A_7	GPIO_RECVED_A_6	GPIO_RECVED_A_5	GPIO_RECVED_A_4	GPIO_RECVED_A_3	GPIO_RECVED_A_2	GPIO_RECVED_A_1	GPIO_RECVED_A_0
0x2F9	0xFF	GPIO_RX_1[7:0]*	GPIO_RECVED_A_15	GPIO_RECVED_A_14	GPIO_RECVED_A_13	GPIO_RECVED_A_12	GPIO_RECVED_A_11	GPIO_RECVED_A_10	GPIO_RECVED_A_9	GPIO_RECVED_A_8
0x2FA	0xFF	GPIO_RX_2[7:0]*	GPIO_RECVED_A_23	GPIO_RECVED_A_22	GPIO_RECVED_A_21	GPIO_RECVED_A_20	GPIO_RECVED_A_19	GPIO_RECVED_A_18	GPIO_RECVED_A_17	GPIO_RECVED_A_16
0x2FB	0xDF	GPIO_RX_3[7:0]*	GPIO_RECVED_A_31	GPIO_RECVED_A_30	GPIO_RECVED_A_29	GPIO_RECVED_A_28	GPIO_RECVED_A_27	GPIO_RECVED_A_26	GPIO_RECVED_A_25	GPIO_RECVED_A_24
MISC										
0x304	0xDC	UART_PT_0[7:0]*	BITLEN_PT_1_L[7:0]							
0x305	0x05	UART_PT_1[7:0]*	–	–	BITLEN_PT_1_H[5:0]					
0x306	0xDC	UART_PT_2[7:0]*	BITLEN_PT_2_L[7:0]							
0x307	0x05	UART_PT_3[7:0]*	–	–	BITLEN_PT_2_H[5:0]					
0x312	0x00	MISC_2[7:0]	VDDIO_OV	VDD1P8_OV	VREG_OV	VDD_OV	RSVD[3:0]			

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ADDRESS	RESET	NAME	MSB							LSB
0x313	0x01	MISC_3[7:0]*	–	–	–	–	–	–	–	LFLT_STKY_INT
VTX X										
0x400	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x401	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x402	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x403	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x404	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x405	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x406	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x407	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x408	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x409	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x40A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x40B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x40C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x40D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x40E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x40F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x410	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x411	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x412	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x413	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x414	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x415	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x416	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x417	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x41F	0x00	HS_VS[7:0]	–	DE_DET	VS_DET	HS_DET	–	–	VS_POL	HS_POL
0x420	0x07	VTX0[7:0]	GEN_VS	GEN_HS	GEN_DE	VID_ACTIVE	PCLKDET_VTX	VS_TRIG	VTG_MODE[1:0]	
0x421	0x00	VTX1[7:0]*	USE_DE_AS_HS	USE_HS_AS_DE	FORCE_VS_LOW	FORCE_HS_LOW	FORCE_DE_LOW	VS_INVERT	HS_INVERT	DE_INVERT
0x422	0x00	VTX2[7:0]	V_VS_DLY_2[7:0]							
0x423	0x00	VTX3[7:0]	V_VS_DLY_1[7:0]							
0x424	0x00	VTX4[7:0]	V_VS_DLY_0[7:0]							
0x425	0x00	VTX5[7:0]	V_VS_HIGH_2[7:0]							
0x426	0x00	VTX6[7:0]	V_VS_HIGH_1[7:0]							
0x427	0x00	VTX7[7:0]	V_VS_HIGH_0[7:0]							
0x428	0x00	VTX8[7:0]	V_VS_LOW_2[7:0]							
0x429	0x00	VTX9[7:0]	V_VS_LOW_1[7:0]							
0x42A	0x00	VTX10[7:0]	V_VS_LOW_0[7:0]							
0x42B	0x00	VTX11[7:0]	V2H_2[7:0]							
0x42C	0x00	VTX12[7:0]	V2H_1[7:0]							
0x42D	0x00	VTX13[7:0]	V2H_0[7:0]							
0x42E	0x00	VTX14[7:0]	V_HS_HIGH_1[7:0]							
0x42F	0x00	VTX15[7:0]	V_HS_HIGH_0[7:0]							
0x430	0x00	VTX16[7:0]	V_HS_LOW_1[7:0]							
0x431	0x00	VTX17[7:0]	V_HS_LOW_0[7:0]							
0x432	0x00	VTX18[7:0]	V_HS_CNT_1[7:0]							
0x433	0x00	VTX19[7:0]	V_HS_CNT_0[7:0]							
0x434	0x00	VTX20[7:0]	V2D_2[7:0]							
0x435	0x00	VTX21[7:0]	V2D_1[7:0]							
0x436	0x00	VTX22[7:0]	V2D_0[7:0]							
0x437	0x00	VTX23[7:0]	V_DE_HIGH_1[7:0]							
0x438	0x00	VTX24[7:0]	V_DE_HIGH_0[7:0]							
0x439	0x00	VTX25[7:0]	V_DE_LOW_1[7:0]							
0x43A	0x00	VTX26[7:0]	V_DE_LOW_0[7:0]							
0x43B	0x00	VTX27[7:0]	V_DE_CNT_1[7:0]							
0x43C	0x00	VTX28[7:0]	V_DE_CNT_0[7:0]							
0x43D	0x00	VTX29[7:0]	VID_PRBS_EN	–	–	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
0x43E	0x04	VTX30[7:0]	GRAD_INC[7:0]							
0x43F	0x00	VTX31[7:0]	CHKR_A_L[7:0]							
0x440	0x00	VTX32[7:0]	CHKR_A_M[7:0]							
0x441	0x00	VTX33[7:0]	CHKR_A_H[7:0]							
0x442	0x00	VTX34[7:0]	CHKR_B_L[7:0]							
0x443	0x00	VTX35[7:0]	CHKR_B_M[7:0]							
0x444	0x00	VTX36[7:0]	CHKR_B_H[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x445	0x00	VTX37[7:0]	CHKR_RPT_A[7:0]							
0x446	0x00	VTX38[7:0]	CHKR_RPT_B[7:0]							
0x447	0x00	VTX39[7:0]	CHKR_ALT[7:0]							
0x448	0x05	VTX40[7:0]*	DIS_COLOR_CROSSBAR	RSVD	–	–	VA_BEFORE_WM	AUTO_COLOR_DEPTH	COLOR_DEPTH[1:0]	
0x449	0x09	VTX41[7:0]*	–	–	–	VID_ASIL_INJ_ERR	VID_ASIL_CRC_ERR_OEN	VID_ASIL_CRC_ERR	VID_ASIL_CRC_CHK_EARLY	VID_ASIL_CRC_CHK_EN
VIDEO_AUTH X										
0x4B4	0x00	outa[7:0]	FULL_FRAME_CRC_0[7:0]							
0x4B5	0x00	outb[7:0]	FULL_FRAME_CRC_1[7:0]							
0x4B6	0x00	outc[7:0]	FULL_FRAME_CRC_2[7:0]							
0x4B7	0x00	outd[7:0]	FULL_FRAME_CRC_3[7:0]							
VTX Y										
0x500	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x501	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x502	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x503	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x504	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x505	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x506	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x507	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x508	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x509	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x50A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x50B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x50C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x50D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x50E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x50F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x510	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x511	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x512	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x513	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x514	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x515	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x516	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x517	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x51F	0x00	HS_VS[7:0]	–	DE_DET	VS_DET	HS_DET	–	–	VS_POL	HS_POL
0x520	0x07	VTX0[7:0]	GEN_VS	GEN_HS	GEN_DE	VID_ACTIVE	PCLKDET_VTX	VS_TRIG	VTG_MODE[1:0]	
0x521	0x00	VTX1[7:0]*	USE_DE_AS_HS	USE_HS_AS_DE	FORCE_VS_LOW	FORCE_HS_LOW	FORCE_DE_LOW	VS_INVERT	HS_INVERT	DE_INVERT
0x522	0x00	VTX2[7:0]	V_VS_DLY_2[7:0]							
0x523	0x00	VTX3[7:0]	V_VS_DLY_1[7:0]							
0x524	0x00	VTX4[7:0]	V_VS_DLY_0[7:0]							
0x525	0x00	VTX5[7:0]	V_VS_HIGH_2[7:0]							
0x526	0x00	VTX6[7:0]	V_VS_HIGH_1[7:0]							
0x527	0x00	VTX7[7:0]	V_VS_HIGH_0[7:0]							
0x528	0x00	VTX8[7:0]	V_VS_LOW_2[7:0]							
0x529	0x00	VTX9[7:0]	V_VS_LOW_1[7:0]							
0x52A	0x00	VTX10[7:0]	V_VS_LOW_0[7:0]							
0x52B	0x00	VTX11[7:0]	V2H_2[7:0]							
0x52C	0x00	VTX12[7:0]	V2H_1[7:0]							
0x52D	0x00	VTX13[7:0]	V2H_0[7:0]							
0x52E	0x00	VTX14[7:0]	V_HS_HIGH_1[7:0]							
0x52F	0x00	VTX15[7:0]	V_HS_HIGH_0[7:0]							
0x530	0x00	VTX16[7:0]	V_HS_LOW_1[7:0]							
0x531	0x00	VTX17[7:0]	V_HS_LOW_0[7:0]							
0x532	0x00	VTX18[7:0]	V_HS_CNT_1[7:0]							
0x533	0x00	VTX19[7:0]	V_HS_CNT_0[7:0]							
0x534	0x00	VTX20[7:0]	V2D_2[7:0]							
0x535	0x00	VTX21[7:0]	V2D_1[7:0]							
0x536	0x00	VTX22[7:0]	V2D_0[7:0]							
0x537	0x00	VTX23[7:0]	V_DE_HIGH_1[7:0]							
0x538	0x00	VTX24[7:0]	V_DE_HIGH_0[7:0]							
0x539	0x00	VTX25[7:0]	V_DE_LOW_1[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x53A	0x00	VTX26[7:0]	V_DE_LOW_0[7:0]							
0x53B	0x00	VTX27[7:0]	V_DE_CNT_1[7:0]							
0x53C	0x00	VTX28[7:0]	V_DE_CNT_0[7:0]							
0x53D	0x00	VTX29[7:0]	VID_PRBS_EN	–	–	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
0x53E	0x04	VTX30[7:0]	GRAD_INC[7:0]							
0x53F	0x00	VTX31[7:0]	CHKR_A_L[7:0]							
0x540	0x00	VTX32[7:0]	CHKR_A_M[7:0]							
0x541	0x00	VTX33[7:0]	CHKR_A_H[7:0]							
0x542	0x00	VTX34[7:0]	CHKR_B_L[7:0]							
0x543	0x00	VTX35[7:0]	CHKR_B_M[7:0]							
0x544	0x00	VTX36[7:0]	CHKR_B_H[7:0]							
0x545	0x00	VTX37[7:0]	CHKR_RPT_A[7:0]							
0x546	0x00	VTX38[7:0]	CHKR_RPT_B[7:0]							
0x547	0x00	VTX39[7:0]	CHKR_ALT[7:0]							
0x548	0x05	VTX40[7:0]*	DIS_COLOR_CROSSBAR	RSVD	–	–	VA_BEFORE_WM	AUTO_COLOR_DEPTH	COLOR_DEPTH[1:0]	
0x549	0x09	VTX41[7:0]*	–	–	–	VID_ASIL_INJ_ERR	VID_ASIL_CRC_ERR_OEN	VID_ASIL_CRC_ERR	VID_ASIL_CRC_CHK_EARLY	VID_ASIL_CRC_CHK_EN
VIDEO_AUTH Y										
0x5B4	0x00	outa[7:0]	FULL_FRAME_CRC_0[7:0]							
0x5B5	0x00	outb[7:0]	FULL_FRAME_CRC_1[7:0]							
0x5B6	0x00	outc[7:0]	FULL_FRAME_CRC_2[7:0]							
0x5B7	0x00	outd[7:0]	FULL_FRAME_CRC_3[7:0]							
SPI_CC_WR										
SPI_CC_RD										
RLMS A										
0x1434	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1435	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1437	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1438	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x1439	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x143A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x143B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x143D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x1449	0x71	RLMS49[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x1458	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1459	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1464	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	

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ADDRESS	RESET	NAME	MSB							LSB
0x1470	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x1471	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1472	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x1473	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1474	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x1475	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x1476	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1495	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x14A4	0xBD	RLMSA4[7:0]*	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
0x14AC	0xCD	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
0x14AD	0x0D	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
RLMS B										
0x1534	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1535	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1537	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1538	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x1539	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x153A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x153B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x153D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x1549	0x71	RLMS49[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x1558	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1559	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1564	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x1570	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x1571	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1572	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x1573	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1574	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x1575	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x1576	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1595	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x15A4	0xBD	RLMSA4[7:0]*	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					

PRELIMINARY
Release to PHY0 under NDA
Maxim Integrated Company Confidential, Provided to MSL2_Customer under NDA

ADDRESS	RESET	NAME	MSB							LSB
0x15AC	0xCD	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
0x15AD	0x0D	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
HDCP_TX HX										
0x1676	0x80	HDCP_DES0[7:0]*	AH_DES_REG_OFFSET_L[7:0]							
0x1677	0x16	HDCP_DES1[7:0]*	AH_DES_REG_OFFSET_H[7:0]							
0x1678	0x00	HDCP_AS0[7:0]	ASEED_0[7:0]							
0x1679	0x00	HDCP_AS1[7:0]	ASEED_1[7:0]							
0x167A	0x00	HDCP_AS2[7:0]	ASEED_2[7:0]							
0x167B	0x00	HDCP_AS3[7:0]	ASEED_3[7:0]							
0x167C	0x00	HDCP_AS4[7:0]	ASEED_4[7:0]							
0x1680	0x00	HDCP_TX0[7:0]	GMSL_BKSV_0[7:0]							
0x1681	0x00	HDCP_TX1[7:0]	GMSL_BKSV_1[7:0]							
0x1682	0x00	HDCP_TX2[7:0]	GMSL_BKSV_2[7:0]							
0x1683	0x00	HDCP_TX3[7:0]	GMSL_BKSV_3[7:0]							
0x1684	0x00	HDCP_TX4[7:0]	GMSL_BKSV_4[7:0]							
0x1685	0xFF	HDCP_TX5[7:0]	RIP_0[7:0]							
0x1686	0xFF	HDCP_TX6[7:0]	RIP_1[7:0]							
0x1687	0xFF	HDCP_TX7[7:0]	PJP[7:0]							
0x1688	0x00	HDCP_TX8[7:0]	AN_0[7:0]							
0x1689	0x00	HDCP_TX9[7:0]	AN_1[7:0]							
0x168A	0x00	HDCP_TXA[7:0]	AN_2[7:0]							
0x168B	0x00	HDCP_TXB[7:0]	AN_3[7:0]							
0x168C	0x00	HDCP_TXC[7:0]	AN_4[7:0]							
0x168D	0x00	HDCP_TXD[7:0]	AN_5[7:0]							

PRELIMINARY
Release to PHTYO under NDA
Maxim Integrated Company Confidential, Provided to GMSL2_Customers Under NDA

ADDRESS	RESET	NAME	MSB							LSB
0x168E	0x00	HDCP_TXE[7:0]	AN_6[7:0]							
0x168F	0x00	HDCP_TXF[7:0]	AN_7[7:0]							
0x1690	0x00	HDCP_TX10[7:0]	AKSV_0[7:0]							
0x1691	0x00	HDCP_TX11[7:0]	AKSV_1[7:0]							
0x1692	0x00	HDCP_TX12[7:0]	AKSV_2[7:0]							
0x1693	0x00	HDCP_TX13[7:0]	AKSV_3[7:0]							
0x1694	0x00	HDCP_TX14[7:0]	AKSV_4[7:0]							
0x1695	0x00	HDCP_TX15[7:0]	–	EN_INT_COMP	–	–	HDCP_RESET	START_AUTH	VSYNC_DET	ENC_EN
0x1696	0x01	HDCP_TX16[7:0]	–	–	–	PJF_MATCH	V_MATCHED	PJ_MATCHED	RI_MATCHED	INVALID_BKSV
0x1697	0x00	HDCP_TX17[7:0]	RSVD[6:0]							HDCP_REPEATER
0x1698	0x00	HDCP_TX18[7:0]	AH_STATUS[7:0]							
0x1699	0x00	HDCP_TX19[7:0]	HIBW_PJ_CALC[1:0]		–	–	–	–	–	DIS_AUDIO_ENC
0x169A	0xFF	HDCP_TX1A[7:0]	PJFP_0[7:0]							
0x169B	0xFF	HDCP_TX1B[7:0]	PJFP_1[7:0]							
0x169C	0xFF	HDCP_TX1C[7:0]	PJFP_2[7:0]							
0x16A0	0x00	HDCP_TX20[7:0]	VH0_0[7:0]							
0x16A1	0x00	HDCP_TX21[7:0]	VH0_1[7:0]							
0x16A2	0x00	HDCP_TX22[7:0]	VH0_2[7:0]							
0x16A3	0x00	HDCP_TX23[7:0]	VH0_3[7:0]							
0x16A4	0x00	HDCP_TX24[7:0]	VH1_0[7:0]							
0x16A5	0x00	HDCP_TX25[7:0]	VH1_1[7:0]							
0x16A6	0x00	HDCP_TX26[7:0]	VH1_2[7:0]							
0x16A7	0x00	HDCP_TX27[7:0]	VH1_3[7:0]							
0x16A8	0x00	HDCP_TX28[7:0]	VH2_0[7:0]							

PRELIMINARY
Release to PHY Under NDA
Maxim Integrated Company Confidential
Provided to GMSL2_Customers Under NDA

ADDRESS	RESET	NAME	MSB							LSB
0x16A9	0x00	HDCP_TX29[7:0]	VH2_1[7:0]							
0x16AA	0x00	HDCP_TX2A[7:0]	VH2_2[7:0]							
0x16AB	0x00	HDCP_TX2B[7:0]	VH2_3[7:0]							
0x16AC	0x00	HDCP_TX2C[7:0]	VH3_0[7:0]							
0x16AD	0x00	HDCP_TX2D[7:0]	VH3_1[7:0]							
0x16AE	0x00	HDCP_TX2E[7:0]	VH3_2[7:0]							
0x16AF	0x00	HDCP_TX2F[7:0]	VH3_3[7:0]							
0x16B0	0x00	HDCP_TX30[7:0]	VH4_0[7:0]							
0x16B1	0x00	HDCP_TX31[7:0]	VH4_1[7:0]							
0x16B2	0x00	HDCP_TX32[7:0]	VH4_2[7:0]							
0x16B3	0x00	HDCP_TX33[7:0]	VH4_3[7:0]							
0x16B4	0x00	HDCP_TX34[7:0]	HDCP_MAX_DEV_EXCEEDED	HDCP_DEV_CNT[6:0]						
0x16B5	0x00	HDCP_TX35[7:0]	RSVD[3:0]				HDCP_MAX_CASCADE_EXCEEDED	HDCP_DEPTH[2:0]		
0x16B6	0x00	HDCP_TX36[7:0]	HDCP_GPMEM[7:0]							
0x16B7	0xC0	HDCP_TX37[7:0]*	HDCP_PD	FAST_PJ_EN	FORCE_AUDIO	FORCE_VIDEO	AH_MASK_ENCOFF	AH_MASK_NEWDEV	AH_MASK_KSVRDY	AH_MASK_FAIL
0x16B8	0x00	HDCP_TX38[7:0]	–	–	–	–	–	AH_RD_KSVL	AH_DISENC	AH_MODE
0x16B9	0x90	HDCP_TX39[7:0]*	AH_DES_ADDR[6:0]							–
0x16BA	0x00	HDCP_TX3A[7:0]	KSV_LIST_0[7:0]							
0x16BB	0x00	HDCP_TX3B[7:0]	KSV_LIST_1[7:0]							
0x16BC	0x00	HDCP_TX3C[7:0]	KSV_LIST_2[7:0]							
0x16BD	0x00	HDCP_TX3D[7:0]	KSV_LIST_3[7:0]							
0x16BE	0x00	HDCP_TX3E[7:0]	KSV_LIST_4[7:0]							

PRELIMINARY
Release to PHY0 under NDA
Maxim Integrated Company Confidential, Provided to GMSL2 Customers Under NDA

ADDRESS	RESET	NAME	MSB							LSB
0x16BF	0x00	HDCP_TX3F[7:0]	KSV_LIST_5[7:0]							
0x16C0	0x00	HDCP_TX40[7:0]	KSV_LIST_6[7:0]							
0x16C1	0x00	HDCP_TX41[7:0]	KSV_LIST_7[7:0]							
0x16C2	0x00	HDCP_TX42[7:0]	KSV_LIST_8[7:0]							
0x16C3	0x00	HDCP_TX43[7:0]	KSV_LIST_9[7:0]							
0x16C4	0x00	HDCP_TX44[7:0]	KSV_LIST_10[7:0]							
0x16C5	0x00	HDCP_TX45[7:0]	KSV_LIST_11[7:0]							
0x16C6	0x00	HDCP_TX46[7:0]	KSV_LIST_12[7:0]							
0x16C7	0x00	HDCP_TX47[7:0]	KSV_LIST_13[7:0]							
0x16C8	0x00	HDCP_TX48[7:0]	KSV_LIST_14[7:0]							
0x16C9	0x00	HDCP_TX49[7:0]	KSV_LIST_15[7:0]							
0x16CA	0x00	HDCP_TX4A[7:0]	KSV_LIST_16[7:0]							
0x16CB	0x00	HDCP_TX4B[7:0]	KSV_LIST_17[7:0]							
0x16CC	0x00	HDCP_TX4C[7:0]	KSV_LIST_18[7:0]							
0x16CD	0x00	HDCP_TX4D[7:0]	KSV_LIST_19[7:0]							
0x16CE	0x00	HDCP_TX4E[7:0]	KSV_LIST_20[7:0]							
0x16CF	0x00	HDCP_TX4F[7:0]	KSV_LIST_21[7:0]							
0x16D0	0x00	HDCP_TX50[7:0]	KSV_LIST_22[7:0]							
0x16D1	0x00	HDCP_TX51[7:0]	KSV_LIST_23[7:0]							
0x16D2	0x00	HDCP_TX52[7:0]	KSV_LIST_24[7:0]							
0x16D3	0x00	HDCP_TX53[7:0]	KSV_LIST_25[7:0]							
0x16D4	0x00	HDCP_TX54[7:0]	KSV_LIST_26[7:0]							
0x16D5	0x00	HDCP_TX55[7:0]	KSV_LIST_27[7:0]							
0x16D6	0x00	HDCP_TX56[7:0]	KSV_LIST_28[7:0]							
0x16D7	0x00	HDCP_TX57[7:0]	KSV_LIST_29[7:0]							

PRELIMINARY
Release to PHY2 under NDA
Maxim Integrated Company Confidential, Provided to GMSL2_Customers Under NDA

ADDRESS	RESET	NAME	MSB							LSB
0x16D8	0x00	HDCP_TX58[7:0]	KSV_LIST_30[7:0]							
0x16D9	0x00	HDCP_TX59[7:0]	KSV_LIST_31[7:0]							
0x16DA	0x00	HDCP_TX5A[7:0]	KSV_LIST_32[7:0]							
0x16DB	0x00	HDCP_TX5B[7:0]	KSV_LIST_33[7:0]							
0x16DC	0x00	HDCP_TX5C[7:0]	KSV_LIST_34[7:0]							
0x16DD	0x00	HDCP_TX5D[7:0]	KSV_LIST_35[7:0]							
0x16DE	0x00	HDCP_TX5E[7:0]	KSV_LIST_36[7:0]							
0x16DF	0x00	HDCP_TX5F[7:0]	KSV_LIST_37[7:0]							
0x16E0	0x00	HDCP_TX60[7:0]	KSV_LIST_38[7:0]							
0x16E1	0x00	HDCP_TX61[7:0]	KSV_LIST_39[7:0]							
0x16E2	0x00	HDCP_TX62[7:0]	KSV_LIST_40[7:0]							
0x16E3	0x00	HDCP_TX63[7:0]	KSV_LIST_41[7:0]							
0x16E4	0x00	HDCP_TX64[7:0]	KSV_LIST_42[7:0]							
0x16E5	0x00	HDCP_TX65[7:0]	KSV_LIST_43[7:0]							
0x16E6	0x00	HDCP_TX66[7:0]	KSV_LIST_44[7:0]							
0x16E7	0x00	HDCP_TX67[7:0]	KSV_LIST_45[7:0]							
0x16E8	0x00	HDCP_TX68[7:0]	KSV_LIST_46[7:0]							
0x16E9	0x00	HDCP_TX69[7:0]	KSV_LIST_47[7:0]							
0x16EA	0x00	HDCP_TX6A[7:0]	KSV_LIST_48[7:0]							
0x16EB	0x00	HDCP_TX6B[7:0]	KSV_LIST_49[7:0]							
0x16EC	0x00	HDCP_TX6C[7:0]	KSV_LIST_50[7:0]							
0x16ED	0x00	HDCP_TX6D[7:0]	KSV_LIST_51[7:0]							
0x16EE	0x00	HDCP_TX6E[7:0]	KSV_LIST_52[7:0]							
0x16EF	0x00	HDCP_TX6F[7:0]	KSV_LIST_53[7:0]							
0x16F0	0x00	HDCP_TX70[7:0]	KSV_LIST_54[7:0]							

PRELIMINARY
Release to PHY0 under NDA
Maxim Integrated Company Confidential, Provided to GMSL2_Customers Under NDA

ADDRESS	RESET	NAME	MSB							LSB
0x16F1	0x00	HDCP_TX71[7:0]	KSV_LIST_55[7:0]							
0x16F2	0x00	HDCP_TX72[7:0]	KSV_LIST_56[7:0]							
0x16F3	0x00	HDCP_TX73[7:0]	KSV_LIST_57[7:0]							
0x16F4	0x00	HDCP_TX74[7:0]	KSV_LIST_58[7:0]							
0x16F5	0x00	HDCP_TX75[7:0]	KSV_LIST_59[7:0]							
0x16F6	0x00	HDCP_TX76[7:0]	KSV_LIST_60[7:0]							
0x16F7	0x00	HDCP_TX77[7:0]	KSV_LIST_61[7:0]							
0x16F8	0x00	HDCP_TX78[7:0]	KSV_LIST_62[7:0]							
0x16F9	0x00	HDCP_TX79[7:0]	KSV_LIST_63[7:0]							
0x16FA	0x00	HDCP_TX7A[7:0]	KSV_LIST_64[7:0]							
0x16FB	0x00	HDCP_TX7B[7:0]	KSV_LIST_65[7:0]							
0x16FC	0x00	HDCP_TX7C[7:0]	KSV_LIST_66[7:0]							
0x16FD	0x00	HDCP_TX7D[7:0]	KSV_LIST_67[7:0]							
0x16FE	0x00	HDCP_TX7E[7:0]	KSV_LIST_68[7:0]							
0x16FF	0x00	HDCP_TX7F[7:0]	KSV_LIST_69[7:0]							
HDCP_TX HY										
0x1776	0x80	HDCP_DES0[7:0]*	AH_DES_REG_OFFSET_L[7:0]							
0x1777	0x16	HDCP_DES1[7:0]*	AH_DES_REG_OFFSET_H[7:0]							
0x1778	0x00	HDCP_AS0[7:0]	ASEED_0[7:0]							
0x1779	0x00	HDCP_AS1[7:0]	ASEED_1[7:0]							
0x177A	0x00	HDCP_AS2[7:0]	ASEED_2[7:0]							
0x177B	0x00	HDCP_AS3[7:0]	ASEED_3[7:0]							
0x177C	0x00	HDCP_AS4[7:0]	ASEED_4[7:0]							
0x1780	0x00	HDCP_TX0[7:0]	GMSL_BKSV_0[7:0]							
0x1781	0x00	HDCP_TX1[7:0]	GMSL_BKSV_1[7:0]							

Release to PHYO under NDA
Maxim Integrated Company Confidential, Provided to GMSL2_Customers Under NDA
PRELIMINARY

ADDRESS	RESET	NAME	MSB							LSB
0x1782	0x00	HDCP_TX2[7:0]	GMSL_BKSV_2[7:0]							
0x1783	0x00	HDCP_TX3[7:0]	GMSL_BKSV_3[7:0]							
0x1784	0x00	HDCP_TX4[7:0]	GMSL_BKSV_4[7:0]							
0x1785	0xFF	HDCP_TX5[7:0]	RIP_0[7:0]							
0x1786	0xFF	HDCP_TX6[7:0]	RIP_1[7:0]							
0x1787	0xFF	HDCP_TX7[7:0]	PJP[7:0]							
0x1788	0x00	HDCP_TX8[7:0]	AN_0[7:0]							
0x1789	0x00	HDCP_TX9[7:0]	AN_1[7:0]							
0x178A	0x00	HDCP_TXA[7:0]	AN_2[7:0]							
0x178B	0x00	HDCP_TXB[7:0]	AN_3[7:0]							
0x178C	0x00	HDCP_TXC[7:0]	AN_4[7:0]							
0x178D	0x00	HDCP_TXD[7:0]	AN_5[7:0]							
0x178E	0x00	HDCP_TXE[7:0]	AN_6[7:0]							
0x178F	0x00	HDCP_TXF[7:0]	AN_7[7:0]							
0x1790	0x00	HDCP_TX10[7:0]	AKSV_0[7:0]							
0x1791	0x00	HDCP_TX11[7:0]	AKSV_1[7:0]							
0x1792	0x00	HDCP_TX12[7:0]	AKSV_2[7:0]							
0x1793	0x00	HDCP_TX13[7:0]	AKSV_3[7:0]							
0x1794	0x00	HDCP_TX14[7:0]	AKSV_4[7:0]							
0x1795	0x00	HDCP_TX15[7:0]	–	EN_INT_COMP	–	–	HDCP_RESET	START_AUTH	VSYNC_DET	ENC_EN
0x1796	0x01	HDCP_TX16[7:0]	–	–	–	PJF_MATCH	V_MATCHED	PJ_MATCHED	RI_MATCHED	INVALID_BKSV
0x1797	0x00	HDCP_TX17[7:0]	RSVD[6:0]							HDCP_REPEATER
0x1798	0x00	HDCP_TX18[7:0]	AH_STATUS[7:0]							
0x1799	0x00	HDCP_TX19[7:0]	HIBW_PJ_CALC[1:0]		–	–	–	–	–	DIS_AUDIO_ENC

PRELIMINARY
Release to PHY0 under NDA
Maxim Integrated Company Confidential, Provided to GMSL2_Customers Under NDA

ADDRESS	RESET	NAME	MSB							LSB
0x179A	0xFF	HDCP_TX1A[7:0]	PJFP_0[7:0]							
0x179B	0xFF	HDCP_TX1B[7:0]	PJFP_1[7:0]							
0x179C	0xFF	HDCP_TX1C[7:0]	PJFP_2[7:0]							
0x17A0	0x00	HDCP_TX20[7:0]	VH0_0[7:0]							
0x17A1	0x00	HDCP_TX21[7:0]	VH0_1[7:0]							
0x17A2	0x00	HDCP_TX22[7:0]	VH0_2[7:0]							
0x17A3	0x00	HDCP_TX23[7:0]	VH0_3[7:0]							
0x17A4	0x00	HDCP_TX24[7:0]	VH1_0[7:0]							
0x17A5	0x00	HDCP_TX25[7:0]	VH1_1[7:0]							
0x17A6	0x00	HDCP_TX26[7:0]	VH1_2[7:0]							
0x17A7	0x00	HDCP_TX27[7:0]	VH1_3[7:0]							
0x17A8	0x00	HDCP_TX28[7:0]	VH2_0[7:0]							
0x17A9	0x00	HDCP_TX29[7:0]	VH2_1[7:0]							
0x17AA	0x00	HDCP_TX2A[7:0]	VH2_2[7:0]							
0x17AB	0x00	HDCP_TX2B[7:0]	VH2_3[7:0]							
0x17AC	0x00	HDCP_TX2C[7:0]	VH3_0[7:0]							
0x17AD	0x00	HDCP_TX2D[7:0]	VH3_1[7:0]							
0x17AE	0x00	HDCP_TX2E[7:0]	VH3_2[7:0]							
0x17AF	0x00	HDCP_TX2F[7:0]	VH3_3[7:0]							
0x17B0	0x00	HDCP_TX30[7:0]	VH4_0[7:0]							
0x17B1	0x00	HDCP_TX31[7:0]	VH4_1[7:0]							
0x17B2	0x00	HDCP_TX32[7:0]	VH4_2[7:0]							
0x17B3	0x00	HDCP_TX33[7:0]	VH4_3[7:0]							
0x17B4	0x00	HDCP_TX34[7:0]	HDCP_MAX_DEV_EXCEDED	HDCP_DEV_CNT[6:0]						

PRELIMINARY
Release to PHY0 under NDA
Maxim Integrated Company Confidential, Provided to GMSL2_Customers Under NDA

ADDRESS	RESET	NAME	MSB							LSB
0x17B5	0x00	HDCP_TX35[7:0]	RSVD[3:0]				HDCP_MAX_CASCADE_EXCEEDED	HDCP_DEPTH[2:0]		
0x17B6	0x00	HDCP_TX36[7:0]	HDCP_GPMEM[7:0]							
0x17B7	0xC0	HDCP_TX37[7:0]*	HDCP_PD	FAST_PJ_EN	FORCE_AUDIO	FORCE_VIDEO	AH_MASK_ENCOFF	AH_MASK_NEWDEV	AH_MASK_KSVRDY	AH_MASK_FAIL
0x17B8	0x00	HDCP_TX38[7:0]	–	–	–	–	–	AH_RD_KSVL	AH_DISENC	AH_MODE
0x17B9	0x90	HDCP_TX39[7:0]*	AH_DES_ADDR[6:0]							–
0x17BA	0x00	HDCP_TX3A[7:0]	KSV_LIST_0[7:0]							
0x17BB	0x00	HDCP_TX3B[7:0]	KSV_LIST_1[7:0]							
0x17BC	0x00	HDCP_TX3C[7:0]	KSV_LIST_2[7:0]							
0x17BD	0x00	HDCP_TX3D[7:0]	KSV_LIST_3[7:0]							
0x17BE	0x00	HDCP_TX3E[7:0]	KSV_LIST_4[7:0]							
0x17BF	0x00	HDCP_TX3F[7:0]	KSV_LIST_5[7:0]							
0x17C0	0x00	HDCP_TX40[7:0]	KSV_LIST_6[7:0]							
0x17C1	0x00	HDCP_TX41[7:0]	KSV_LIST_7[7:0]							
0x17C2	0x00	HDCP_TX42[7:0]	KSV_LIST_8[7:0]							
0x17C3	0x00	HDCP_TX43[7:0]	KSV_LIST_9[7:0]							
0x17C4	0x00	HDCP_TX44[7:0]	KSV_LIST_10[7:0]							
0x17C5	0x00	HDCP_TX45[7:0]	KSV_LIST_11[7:0]							
0x17C6	0x00	HDCP_TX46[7:0]	KSV_LIST_12[7:0]							
0x17C7	0x00	HDCP_TX47[7:0]	KSV_LIST_13[7:0]							
0x17C8	0x00	HDCP_TX48[7:0]	KSV_LIST_14[7:0]							
0x17C9	0x00	HDCP_TX49[7:0]	KSV_LIST_15[7:0]							
0x17CA	0x00	HDCP_TX4A[7:0]	KSV_LIST_16[7:0]							
0x17CB	0x00	HDCP_TX4B[7:0]	KSV_LIST_17[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x17CC	0x00	HDCP_TX4C[7:0]	KSV_LIST_18[7:0]							
0x17CD	0x00	HDCP_TX4D[7:0]	KSV_LIST_19[7:0]							
0x17CE	0x00	HDCP_TX4E[7:0]	KSV_LIST_20[7:0]							
0x17CF	0x00	HDCP_TX4F[7:0]	KSV_LIST_21[7:0]							
0x17D0	0x00	HDCP_TX50[7:0]	KSV_LIST_22[7:0]							
0x17D1	0x00	HDCP_TX51[7:0]	KSV_LIST_23[7:0]							
0x17D2	0x00	HDCP_TX52[7:0]	KSV_LIST_24[7:0]							
0x17D3	0x00	HDCP_TX53[7:0]	KSV_LIST_25[7:0]							
0x17D4	0x00	HDCP_TX54[7:0]	KSV_LIST_26[7:0]							
0x17D5	0x00	HDCP_TX55[7:0]	KSV_LIST_27[7:0]							
0x17D6	0x00	HDCP_TX56[7:0]	KSV_LIST_28[7:0]							
0x17D7	0x00	HDCP_TX57[7:0]	KSV_LIST_29[7:0]							
0x17D8	0x00	HDCP_TX58[7:0]	KSV_LIST_30[7:0]							
0x17D9	0x00	HDCP_TX59[7:0]	KSV_LIST_31[7:0]							
0x17DA	0x00	HDCP_TX5A[7:0]	KSV_LIST_32[7:0]							
0x17DB	0x00	HDCP_TX5B[7:0]	KSV_LIST_33[7:0]							
0x17DC	0x00	HDCP_TX5C[7:0]	KSV_LIST_34[7:0]							
0x17DD	0x00	HDCP_TX5D[7:0]	KSV_LIST_35[7:0]							
0x17DE	0x00	HDCP_TX5E[7:0]	KSV_LIST_36[7:0]							
0x17DF	0x00	HDCP_TX5F[7:0]	KSV_LIST_37[7:0]							
0x17E0	0x00	HDCP_TX60[7:0]	KSV_LIST_38[7:0]							
0x17E1	0x00	HDCP_TX61[7:0]	KSV_LIST_39[7:0]							
0x17E2	0x00	HDCP_TX62[7:0]	KSV_LIST_40[7:0]							
0x17E3	0x00	HDCP_TX63[7:0]	KSV_LIST_41[7:0]							
0x17E4	0x00	HDCP_TX64[7:0]	KSV_LIST_42[7:0]							

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0x17E5	0x00	HDCP_TX65[7:0]	KSV_LIST_43[7:0]							
0x17E6	0x00	HDCP_TX66[7:0]	KSV_LIST_44[7:0]							
0x17E7	0x00	HDCP_TX67[7:0]	KSV_LIST_45[7:0]							
0x17E8	0x00	HDCP_TX68[7:0]	KSV_LIST_46[7:0]							
0x17E9	0x00	HDCP_TX69[7:0]	KSV_LIST_47[7:0]							
0x17EA	0x00	HDCP_TX6A[7:0]	KSV_LIST_48[7:0]							
0x17EB	0x00	HDCP_TX6B[7:0]	KSV_LIST_49[7:0]							
0x17EC	0x00	HDCP_TX6C[7:0]	KSV_LIST_50[7:0]							
0x17ED	0x00	HDCP_TX6D[7:0]	KSV_LIST_51[7:0]							
0x17EE	0x00	HDCP_TX6E[7:0]	KSV_LIST_52[7:0]							
0x17EF	0x00	HDCP_TX6F[7:0]	KSV_LIST_53[7:0]							
0x17F0	0x00	HDCP_TX70[7:0]	KSV_LIST_54[7:0]							
0x17F1	0x00	HDCP_TX71[7:0]	KSV_LIST_55[7:0]							
0x17F2	0x00	HDCP_TX72[7:0]	KSV_LIST_56[7:0]							
0x17F3	0x00	HDCP_TX73[7:0]	KSV_LIST_57[7:0]							
0x17F4	0x00	HDCP_TX74[7:0]	KSV_LIST_58[7:0]							
0x17F5	0x00	HDCP_TX75[7:0]	KSV_LIST_59[7:0]							
0x17F6	0x00	HDCP_TX76[7:0]	KSV_LIST_60[7:0]							
0x17F7	0x00	HDCP_TX77[7:0]	KSV_LIST_61[7:0]							
0x17F8	0x00	HDCP_TX78[7:0]	KSV_LIST_62[7:0]							
0x17F9	0x00	HDCP_TX79[7:0]	KSV_LIST_63[7:0]							
0x17FA	0x00	HDCP_TX7A[7:0]	KSV_LIST_64[7:0]							
0x17FB	0x00	HDCP_TX7B[7:0]	KSV_LIST_65[7:0]							
0x17FC	0x00	HDCP_TX7C[7:0]	KSV_LIST_66[7:0]							
0x17FD	0x00	HDCP_TX7D[7:0]	KSV_LIST_67[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x17FE	0x00	HDCP_TX7E[7:0]	KSV_LIST_68[7:0]							
0x17FF	0x00	HDCP_TX7F[7:0]	KSV_LIST_69[7:0]							
DPLL AUD_X										
0x1B03	0x82	DPLL_3[7:0]*	RSVD	RSVD	RSVD	RSVD	config_force_enable_ss	config_spread_bit_ratio[2:0]		
DPLL AUD_Y										
0x1C03	0x82	DPLL_3[7:0]*	RSVD	RSVD	RSVD	RSVD	config_force_enable_ss	config_spread_bit_ratio[2:0]		
FUNC_SAFE										
0x1D00	0x00	REGCRC0[7:0]*	–	–	LIMIT_REG_RANGE	GEN_ROLLING_CRC	I2C_WR_COMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
0x1D01	0x00	REGCRC1[7:0]*	CRC_PERIOD[7:0]							
0x1D02	0x00	REGCRC2[7:0]	REGCRC_LSB[7:0]							
0x1D03	0x00	REGCRC3[7:0]	REGCRC_MSB[7:0]							
0x1D04	0x00	REGCRC4[7:0]*	MIN_RANGE_LSB[7:0]							
0x1D05	0x00	REGCRC5[7:0]*	MIN_RANGE_MSB[7:0]							
0x1D06	0xFF	REGCRC6[7:0]*	MAX_RANGE_LSB[7:0]							
0x1D07	0xFF	REGCRC7[7:0]*	MAX_RANGE_MSB[7:0]							
0x1D08	0xFF	REGCRC8[7:0]*	SKIP0_LSB[7:0]							
0x1D09	0xFF	REGCRC9[7:0]	SKIP0_MSB[7:0]							
0x1D0A	0xFF	REGCRC10[7:0]	SKIP1_LSB[7:0]							
0x1D0B	0xFF	REGCRC11[7:0]	SKIP1_MSB[7:0]							
0x1D0C	0xFF	REGCRC12[7:0]	SKIP2_LSB[7:0]							
0x1D0D	0xFF	REGCRC13[7:0]	SKIP2_MSB[7:0]							
0x1D0E	0xFF	REGCRC14[7:0]	SKIP3_LSB[7:0]							
0x1D0F	0xFF	REGCRC15[7:0]	SKIP3_MSB[7:0]							
0x1D10	0xFF	REGCRC16[7:0]	SKIP4_LSB[7:0]							
0x1D11	0xFF	REGCRC17[7:0]	SKIP4_MSB[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x1D12	0xFF	REGCRC18[7:0]	SKIP5_LSB[7:0]							
0x1D13	0xFF	REGCRC19[7:0]	SKIP5_MSB[7:0]							
0x1D14	0xFF	REGCRC20[7:0]	SKIP6_LSB[7:0]							
0x1D15	0xFF	REGCRC21[7:0]	SKIP6_MSB[7:0]							
0x1D16	0xFF	REGCRC22[7:0]	SKIP7_LSB[7:0]							
0x1D17	0xFF	REGCRC23[7:0]*	SKIP7_MSB[7:0]							
0x1D20	0x00	CC_CRC0[7:0]	CC_CRC_VAL[7:0]							
0x1D21	0x00	CC_CRC1[7:0]	MSGCNTR_LSB[7:0]							
0x1D22	0x00	CC_CRC2[7:0]	MSGCNTR_MSB[7:0]							
0x1D23	0x00	CC_CRC3[7:0]	CC_CRC_ERR_CNT[7:0]							
0x1D24	0x00	CC_CRC4[7:0]	MSGCNTR_ERR_CNT[7:0]							
0x1D25	0x00	CC_CRC5[7:0]	–	–	–	RESET_MSGCNTR	–	–	RESET_MSGCNTR_ERR_CNT	RESET_CC_CRC_ERR_CNT
0x1D26	0x20	CC_RTTN_ERR[7:0]	–	–	RTTN_CRC_INT_OEN	RTTN_CRC_ERR_FLAG	–	–	–	RSVD
RBB_CRC_ERR A										
0x1D80	0x00	INTR_CRC_0[7:0]*	AUDIO_Y_CRC_ERR_OEN	AUDIO_X_CRC_ERR_OEN	AHDCP_CRC_ERR_OEN	GPIO_CRC_ERR_OEN	SPI_CRC_ERR_OEN	RBB_CC_CRC_ERR_OEN	PT2_CRC_ERR_OEN	PT1_CRC_ERR_OEN
0x1D81	0x00	INTR_CRC_1[7:0]	AUDIO_Y_CRC_ERR_FLAG	AUDIO_X_CRC_ERR_FLAG	AHDCP_CRC_ERR_FLAG	GPIO_CRC_ERR_FLAG	SPI_CRC_ERR_FLAG	RBB_CC_CRC_ERR_FLAG	PT2_CRC_ERR_FLAG	PT1_CRC_ERR_FLAG
0x1D82	0x00	CNT0[7:0]	PT1_CRC_ERR[7:0]							
0x1D83	0x00	CNT1[7:0]	PT2_CRC_ERR[7:0]							
0x1D84	0x00	CNT2[7:0]	RBB_CC_CRC_ERR[7:0]							
0x1D85	0x00	CNT3[7:0]	SPI_CRC_ERR[7:0]							
0x1D86	0x00	CNT4[7:0]	GPIO_CRC_ERR[7:0]							
0x1D87	0x00	CNT5[7:0]	AHDCP_CRC_ERR[7:0]							
0x1D88	0x00	CNT6[7:0]	AUDIO_X_CRC_ERR[7:0]							
0x1D89	0x00	CNT7[7:0]	AUDIO_Y_CRC_ERR[7:0]							
FRONTTOP										
0x2326	0x04	FRONTTOP_30[7:0]*	–	–	–	–	–	CROSS_Y	–	CROSS_X

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ADDRESS	RESET	NAME	MSB							LSB
GMSL1 A										
0x2402	0x00	GMSL1_2[7:0]*	–	–	SSEN	–	–	–	–	–
0x2404	0x83	GMSL1_4[7:0]*	SEREN	CLINKEN	PRBSEN	AUDIO_EN	–	–	REVCCEN	FWDCCEN
0x2405	0x00	GMSL1_5[7:0]*	–	–	PRBS_LEN[1:0]		–	–	–	–
0x2407	0x00	GMSL1_7[7:0]*	RSVD	HIBW	BWS	–	DRS	HVEN	–	PXL_CRC
0x240D	0x01	GMSL1_D[7:0]*	I2C_LOC_ACK	–	–	–	–	LOC_CC_PT_EN[2:0]		
0x240F	0x7C	GMSL1_F[7:0]*	CNTL_IN_EN[4:0]					GPO_RX_EN	–	SET_GPO
0x2411	0x00	GMSL1_11[7:0]*	ERRG_RATE2[1:0]		ERRG_TYPE2[1:0]		ERRG_CNT2[1:0]		ERRG_PER2	ERRG_EN_G1
0x2412	0x00	GMSL1_12[7:0]*	–	–	–	–	–	CNTL_IN_ORD[2:0]		
0x2413	0x00	GMSL1_13[7:0]*	NO_REM_MST	ALLOW_PKTCC	–	RSVD	RSVD	RSVD	–	–
0x2414	0x00	GMSL1_14[7:0]	–	–	–	I2C_TIMED_OUT2	CC_WBLOCK_LOST	REV_BIT_LOCK	CC_WBLOCK	REM_CCLOCK
0x2415	0x03	GMSL1_15[7:0]*	–	–	–	–	–	–	SEL_VESA	SEL_RGB888
0x2416	0x00	GMSL1_16[7:0]	–	MAX_RT_ERR	–	–	–	–	–	–
0x241C	0x00	GMSL1_18[7:0]	CC_I2C_RETR_CNT[7:0]							
0x241D	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0x2438	0x18	GMSL1_39[7:0]*	–	CROSS24_I	CROSS24_F	CROSS24[4:0]				
0x2439	0x19	GMSL1_3A[7:0]*	–	CROSS25_I	CROSS25_F	CROSS25[4:0]				
0x243A	0x1A	GMSL1_3B[7:0]*	–	CROSS26_I	CROSS26_F	CROSS26[4:0]				
0x243B	0x1B	GMSL1_3C[7:0]*	–	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x243C	0x1C	GMSL1_3D[7:0]*	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x243D	0x1D	GMSL1_3E[7:0]*	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
0x243E	0x1E	GMSL1_3F[7:0]*	–	CROSS30_I	CROSS30_F	CROSS30[4:0]				
0x2442	0x5B	GMSL1_42[7:0]*	RSVD[1:0]		–	MAX_RT_EN	I2C_RT_EN	RSVD	RSVD	GPO_EN
0x244D	0x00	GMSL1_4D[7:0]*	HIGHIMM	–	–	–	–	–	–	–
0x2466	0x60	GMSL1_66[7:0]*	RSVD[1:0]		PRBS_TYPE	REV_FAST	DIS_DE	–	–	–

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ADDRESS	RESET	NAME	MSB							LSB
0x2467	0x07	GMSL1_67[7:0]*	CNTL_TRIG[1:0]		AUTO_CLINK	DE_RGB888_DBL	–	DBL_ALIGN_TO[2:0]		
0x2468	0x19	GMSL1_68[7:0]*	–	RSVD[2:0]			RSVD[1:0]		CC_CRC_LENGTH[1:0]	
0x2499	0x0C	GMSL1_99[7:0]*	RSVD	–	RSVD	REV_FILT_EN	RSVD	ALIGN_INFO	–	–
0x249A	0x10	GMSL1_9A[7:0]*	–	–	RSVD[1:0]		PKTCC_EN	RSVD[1:0]		RSVD
0x24C8	0x00	GMSL1_C8[7:0]	–	RSVD	I2C_ACK_RECVED	I2C_ACK_ACKED	–	–	–	–
MISC_GMSL1										
0x2575	0x25	G1_I2C_0[7:0]*	–	–	G1_SLV_SH[1:0]		–	G1_SLV_TO[2:0]		
0x2576	0x56	G1_I2C_1[7:0]*	–	G1_MST_BT[2:0]			–	G1_MST_TO[2:0]		
0x2577	0x00	G1_I2C_2[7:0]*	G1_SRC_A[6:0]							–
0x2578	0x00	G1_I2C_3[7:0]*	G1_DST_A[6:0]							–
0x2579	0x00	G1_I2C_4[7:0]*	G1_SRC_B[6:0]							–
0x257A	0x00	G1_I2C_5[7:0]*	G1_DST_B[6:0]							–
GMSL1 B										
0x2602	0x00	GMSL1_2[7:0]*	–	–	SSEN	–	–	–	–	–
0x2604	0x83	GMSL1_4[7:0]*	SEREN	CLINKEN	PRBSEN	AUDIO_EN	–	–	REVCCEN	FWDCCEN
0x2605	0x00	GMSL1_5[7:0]*	–	–	PRBS_LEN[1:0]		–	–	–	–
0x2607	0x00	GMSL1_7[7:0]*	RSVD	HIBW	BWS	–	DRS	HVEN	–	PXL_CRC
0x260D	0x01	GMSL1_D[7:0]*	I2C_LOC_ACK	–	–	–	–	LOC_CC_PT_EN[2:0]		
0x260F	0x7C	GMSL1_F[7:0]*	CNTL_IN_EN[4:0]					GPO_RX_EN	–	SET_GPO
0x2611	0x00	GMSL1_11[7:0]*	ERRG_RATE2[1:0]		ERRG_TYPE2[1:0]		ERRG_CNT2[1:0]		ERRG_PER2	ERRG_EN_G1
0x2612	0x00	GMSL1_12[7:0]*	–	–	–	–	–	CNTL_IN_ORD[2:0]		
0x2613	0x00	GMSL1_13[7:0]*	NO_REM_MST	ALLOW_PKTCC	–	RSVD	RSVD	RSVD	–	–
0x2614	0x00	GMSL1_14[7:0]	–	–	–	I2C_TIMED_OUT2	CC_WBLOCK_LOST	REV_BIT_LOCK	CC_WBLOCK	REM_CCLOCK
0x2615	0x03	GMSL1_15[7:0]*	–	–	–	–	–	–	SEL_VESA	SEL_RGB888
0x2616	0x00	GMSL1_16[7:0]	–	MAX_RT_ERR	–	–	–	–	–	–

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0x261C	0x00	GMSL1_18[7:0]	CC_I2C_RETR_CNT[7:0]							
0x261D	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0x2638	0x18	GMSL1_39[7:0]*	–	CROSS24_I	CROSS24_F	CROSS24[4:0]				
0x2639	0x19	GMSL1_3A[7:0]*	–	CROSS25_I	CROSS25_F	CROSS25[4:0]				
0x263A	0x1A	GMSL1_3B[7:0]*	–	CROSS26_I	CROSS26_F	CROSS26[4:0]				
0x263B	0x1B	GMSL1_3C[7:0]*	–	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x263C	0x1C	GMSL1_3D[7:0]*	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x263D	0x1D	GMSL1_3E[7:0]*	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
0x263E	0x1E	GMSL1_3F[7:0]*	–	CROSS30_I	CROSS30_F	CROSS30[4:0]				
0x2642	0x5B	GMSL1_42[7:0]*	RSVD[1:0]		–	MAX_RT_EN	I2C_RT_EN	RSVD	RSVD	GPO_EN
0x264D	0x00	GMSL1_4D[7:0]*	HIGHIMM	–	–	–	–	–	–	–
0x2666	0x60	GMSL1_66[7:0]*	RSVD[1:0]		PRBS_TYPE	REV_FAST	DIS_DE	–	–	–
0x2667	0x07	GMSL1_67[7:0]*	CNTL_TRIG[1:0]		AUTO_CLINK	DE_RGB888_DBL	–	DBL_ALIGN_TO[2:0]		
0x2668	0x19	GMSL1_68[7:0]*	–	RSVD[2:0]			RSVD[1:0]		CC_CRC_LENGTH[1:0]	
0x2699	0x0C	GMSL1_99[7:0]*	RSVD	–	RSVD	REV_FILT_EN	RSVD	ALIGN_INFO	–	–
0x269A	0x10	GMSL1_9A[7:0]*	–	–	RSVD[1:0]		PKTCC_EN	RSVD[1:0]		RSVD
0x26C8	0x00	GMSL1_C8[7:0]	–	RSVD	I2C_ACK_RECVED	I2C_ACK_ACKED	–	–	–	–
PROFILE										
0x3300	0x00	PROFILE_CTRL_0[7:0]*	–	–	–	PROF_SEL_A[4:0]				
0x3301	0x00	PROFILE_CTRL_1[7:0]*	–	–	–	PROF_SEL_B[4:0]				
0x3302	0x00	PROFILE_CTRL_2[7:0]	PROF_STATUS[7:0]							
0x3303	0x00	PROFILE_CTRL_3[7:0]*	EXEC_PROF	EXEC_PROF_ERR	–	DIS_LINK_RST	–	–	PROF_IN_USE_B	PROF_IN_USE_A
0x3308	0x00	PROFILE_CFG_A_0[7:0]*	TX_LRATE_A	GMSL_MODE_A	SYNC_POL_A	HV_ENC_A	HIM_EN_A	LINE_FAULT_A	GMSL1_WORD_A[1:0]	
0x3309	0x00	PROFILE_CFG_A_1[7:0]*	–	–	–	–	PT_I2CUART_2_A[1:0]		PT_I2CUART_1_A[1:0]	

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ADDRESS	RESET	NAME	MSB							LSB
0x330C	0x00	PROFILE_CFG_B_0[7:0]*	TX_LRATE_B	GMSL_MODE_B	SYNC_POL_B	HV_ENC_B	HIM_EN_B	LINE_FAULT_B	GMSL1_WORD_B[1:0]	
0x330D	0x00	PROFILE_CFG_B_1[7:0]*	–	–	–	–	PT_I2CUART_2_B[1:0]		PT_I2CUART_1_B[1:0]	
RLMS_EDP 0										
0x6064	0x0D	PHY_CTRL0_B0[7:0]	–	–	PHYC_AEQ_TIME_2G7[5:0]					
0x6065	0x0D	PHY_CTRL0_B1[7:0]	–	RSVD	PHYC_AEQ_TIME_5G4[5:0]					
0x6067	0x0D	PHY_CTRL0_B3[7:0]	–	–	PHYC_AEQ_TIME_8G1[5:0]					
RLMS_EDP 1										
0x6164	0x0D	PHY_CTRL0_B0[7:0]	–	–	PHYC_AEQ_TIME_2G7[5:0]					
0x6165	0x0D	PHY_CTRL0_B1[7:0]	–	RSVD	PHYC_AEQ_TIME_5G4[5:0]					
0x6167	0x0D	PHY_CTRL0_B3[7:0]	–	–	PHYC_AEQ_TIME_8G1[5:0]					
EDPRX_CTRL										
0x6418	0x00	DPRX_TRN_STATUS0[7:0]	DPRX_LINK_RATE[7:0]							
0x6419	0x00	DPRX_TRN_STATUS1[7:0]	–	–	–	DPRX_LANE_CNT[4:0]				
0x641A	0x00	DPRX_TRN_STATUS2[7:0]	DPRX_TRAIN_STATE[3:0]				–	DPRX_TRAIN_PAT[2:0]		
0x641B	0x05	DPRX_TRN_STATUS3[7:0]	–	–	–	–	–	SYM_LOCK_COMB	LQP_TRN_NOCLR	TPS4_DESCRAM_ON
0x6420	0x00	EDP_VIDEO_CTRL0[7:0]*	RSVD	RSVD	RSVD	–	–	–	VIDEO_OUT_EN[1:0]	
0x6422	0x05	EDP_VIDEO_CTRL2[7:0]*	–	–	–	–	RSVD	EDID_ROM_EN	EDID_RAM_EN	EDID_READ_ONLY
0x6430	0x00	EDP_GEN_INT_ST0[7:0]	RSVD	RSVD	DP_RLMS1_INT	DP_RLMS0_INT	DPRX_INT	–	RSVD	RSVD
0x6433	0x00	EDP_GEN_INT_ST3[7:0]	RSVD	APB_ERR_M0_IST	–	–	–	–	–	–
0x6434	0x00	EDP_GEN_INT_EN0[7:0]	RSVD	RSVD	DP_RLMS1_IEN	DP_RLMS0_IEN	DPRX_IEN	–	RSVD	RSVD
0x6437	0x00	EDP_GEN_INT_EN3[7:0]	RSVD	APB_ERR_M0_IEN	–	–	–	–	–	–
0x6444	0x00	HPD_CTRL0[7:0]	–	–	–	–	HPD_IRQ_HO_DIS	HPD_IRQ	HPD_ST	HPD_MODE

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ADDRESS	RESET	NAME	MSB							LSB
0x6445	0xFF	HPD_CTRL1[7:0]	HPD_IRQ_TIME[7:0]							
0x6446	0x00	HPD_CTRL2[7:0]	–	–	–	–	–	HPD_IRQ_HO	HOT_PLUG_DET	DPRX_HPD
0x6447	0xDC	HPD_CTRL3[7:0]	HPD_IRQ_HO_TIME[7:0]							
0x64C0	0x01	APB_CTRL_M0_B0[7:0]	–	–	–	–	–	APB_TO_SEL_M0[2:0]		
0x64C2	0x00	APB_CTRL_M0_B2[7:0]	APB_ERR_IEN_M0[7:0]							
0x64C4	0x00	APB_STATUS_M0_B0[7:0]	APB_STATUS_M0[7:0]							
0x64C6	0x00	APB_STATUS_M0_B2[7:0]	APB_STATUS_ERR_M0[7:0]							
0x64C8	0x00	APB_ADRCTL_ERR_M0_B0[7:0]	APB_ADR_ERR_M0_L[7:0]							
0x64C9	0x00	APB_ADRCTL_ERR_M0_B1[7:0]	APB_ADR_ERR_M0_H[7:0]							
0x64CA	0x00	APB_ADRCTL_ERR_M0_B2[7:0]	–	–	–	APB_WR_ERR_M0	APB_STB_ERR_M0[3:0]			
0x64D0	0x01	DPCD_CTRL_M0_B0[7:0]	DPCD_ADDR_HI_M0_L[7:0]							
0x64D1	0x00	DPCD_CTRL_M0_B1[7:0]	–	–	–	–	DPCD_ADDR_HI_M0_H[3:0]			
0x64D2	0x00	DPCD_CTRL_M0_B2[7:0]	–	–	–	–	–	–	DPCD_RDCLR_EN_M0	DPCD_APB_NOBLK_M0
EDID										
DPRX_LINK										
0x7000	0x01	LINK_ENABLE[7:0]	–	–	–	–	–	–	–	LINK_ENABLE
0x7004	0x96	AUX_CLOCK_DIV_B0[7:0]	AUX_CLOCK_DIV_L[7:0]							
0x7005	0x00	AUX_CLOCK_DIV_B1[7:0]	–	–	–	–	–	–	AUX_CLOCK_DIV_H[1:0]	
0x7018	0x16	MISC_CONFIG_B0[7:0]	DISABLE_AUX_FILTER	ALPM_ENABLE	EDP_FUNCTION_ENABLE	MAX_DOWNSPREAD_CONFIG	BRANCH_SUPPORT_ENABLE	DISABLE_INACTIVE_COUNT	DEFER_LONG_I2C	MSA_DELAY_BYPASS
0x7019	0x01	MISC_CONFIG_B1[7:0]	–	–	–	–	–	MSO_FUNCTION_EN	DISABLE_LINE_RESET	MST_FUNCTION_ENABLE
0x701C	0x14	DISPLAYPORT_VERSION[7:0]	DP_VERSION[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x7024	0x00	REQUEST_ERROR_COUNT[7:0]	REQUEST_ERROR_COUNT[7:0]							
0x7028	0x00	REQUEST_COUNT_L[7:0]	REQUEST_COUNT_L[7:0]							
0x7029	0x00	REQUEST_COUNT_H[7:0]	–	–	–	–	–	–	REQUEST_COUNT_H[1:0]	
0x702C	0x00	HPD_INTERRUPT[7:0]	–	–	–	–	–	–	RSVD	HPD_IRQ
0x702D	0x00	HPD_INTERRUPT_MASK[7:0]	–	HPD_INTERRUPT_MASK[6:0]						
0x7030	0x00	LANE_REMAP_B0[7:0]	RSVD[1:0]		RSVD[1:0]		REMAP_LANE_1[1:0]		REMAP_LANE_0[1:0]	
0x7031	0x00	LANE_REMAP_B1[7:0]	–	–	–	–	–	–	–	REMAP_ENABLE
0x7032	0x00	LANE_REMAP_B2[7:0]	–	–	–	–	RSVD	RSVD	INVERT_LANE_1	INVERT_LANE_0
0x7054	0x00	VIDEO_INPUT_RESET[7:0]	–	–	–	–	–	–	LINK_RESET	VIDEO_INPUT_RESET
0x7058	0x00	EDP_IGNORE_MSA[7:0]	–	–	–	–	–	–	–	EDP_IGNORE_MSA
0x7070	0x02	MAX_LANE_COUNT[7:0]	MAX_LANE_COUNT[7:0]							
0x7074	0x1E	MAX_LINK_RATE[7:0]	MAX_LINK_RATE[7:0]							
0x7084	0x00	LOCAL_EDID_VIDEO[7:0]	–	–	–	–	–	–	–	LOCAL_EDID_VIDEO
0x70A0	0x04	AUX_RD_INTERVAL[7:0]	–	AUX_RD_INTERVAL[6:0]						
0x70A4	0x38	I2C_SPEED_CAPABILITY[7:0]	–	–	I2C_SPEED_CAPABILITY[5:0]					
0x70A5	0x08	I2C_SCL_TO_SEL[7:0]	–	–	–	–	I2C_SCL_TO_SEL[3:0]			
0x7400	0x00	DPCD_LINK_BW_SET[7:0]	DPCD_LINK_BW_SET[7:0]							
0x7404	0x00	DPCD_LANE_COUNT_SET[7:0]	–	–	–	DPCD_LANE_COUNT_SET[4:0]				
0x7408	0x01	DPCD_ENHANCED_FRAME_EN[7:0]	–	–	–	–	–	–	–	DPCD_ENHANCED_FRAME_EN
0x740C	0x00	DPCD_TRAINING_PATTERN_SET[7:0]	–	–	–	–	–	DPCD_TRAINING_PATTERN_SET[2:0]		

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0x7410	0x00	DPCD_LINK_QUAL_PAT_SET_B0[7:0]	–	DPCD_LINK_QUAL_LANE1_SET[2:0]			–	DPCD_LINK_QUAL_LANE0_SET[2:0]		
0x7418	0x01	DPCD_SCRAMBLING_DISABLE[7:0]	–	–	–	–	–	–	–	DPCD_SCRAMBLING_DISABLE
0x741C	0x00	DPCD_SYMBOL_ERROR_COUNT_SELECT[7:0]	–	–	–	–	–	–	DPCD_SYMBOL_ERROR_COUNT_SELECT[1:0]	
0x7420	0x00	DPCD_TRAINING_LANE_0_SET[7:0]	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
0x7424	0x00	DPCD_TRAINING_LANE_1_SET[7:0]	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
0x7430	0x00	DPCD_DOWNSPREAD_CONTROL[7:0]	–	–	–	–	–	–	–	DPCD_DOWNSPREAD_CONTROL
0x7434	0x01	DPCD_MAIN_LINK_CHANNEL_CODING_SET[7:0]	–	–	–	–	–	–	–	DPCD_MAIN_LINK_CHANNEL_CODING_SET
0x7438	0x02	DPCD_SET_POWER_STATE[7:0]	–	–	–	–	–	DPCD_SET_POWER_STATE[2:0]		
0x743C	0x00	DPCD_LANE01_STATUS_B0[7:0]	–	LANE1_SYMBOL_LOCKED	LANE1_CHANNEL_EQ_DONE	LANE1_CLOCK_RECOVERY_DONE	–	LANE0_SYMBOL_LOCKED	LANE0_CHANNEL_EQ_DONE	LANE0_CLOCK_RECOVERY_DONE
0x743D	0x00	DPCD_LANE01_STATUS_B1[7:0]	–	–	–	–	–	–	LANE1_LANE_ALIGNED	LANE0_LANE_ALIGNED
0x743E	0x00	DPCD_LANE01_STATUS_B2[7:0]	–	–	–	–	–	–	LANE1_TRAINING_LOST	LANE0_TRAINING_LOST
0x7454	0x00	LANE0_TRAINING_LOST_CAUSE[7:0]	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
0x7455	0x00	LANE1_TRAINING_LOST_CAUSE[7:0]	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
0x7478	0x00	I2C_SPEED_CONTROL_SELECT[7:0]	–	–	I2C_SPEED_CAPABILITY[5:0]					

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0x747C	0x00	MSA_TIMING_IGNORE[7:0]	–	–	–	–	–	–	–	MSA_TIMING_IGNORE
0x748C	0x00	MST_MODE_CTRL[7:0]	–	–	–	–	–	UPSTREAM_IS_SRC	UP_REQ_EN	MST_EN
0x7490	0x00	DPCD_SER_COUNT_LANE0_B0[7:0]	SER_COUNT_LANE0_B0[7:0]							
0x7491	0x00	DPCD_SER_COUNT_LANE0_B1[7:0]	SER_COUNT_LANE0_B1[7:0]							
0x7494	0x00	DPCD_SER_COUNT_LANE1_B0[7:0]	SER_COUNT_LANE1_B0[7:0]							
0x7495	0x00	DPCD_SER_COUNT_LANE1_B1[7:0]	SER_COUNT_LANE1_B1[7:0]							
0x7500	0x00	MSA_HRES_B0[7:0]	MSA_HRES_B0[7:0]							
0x7501	0x00	MSA_HRES_B1[7:0]	MSA_HRES_B1[7:0]							
0x7504	0x00	MSA_HSPOL[7:0]	–	–	–	–	–	–	–	MSA_HSPOL
0x7508	0x00	MSA_HSWIDTH_B0[7:0]	MSA_HSWIDTH_B0[7:0]							
0x7509	0x00	MSA_HSWIDTH_B1[7:0]	–	MSA_HSWIDTH_B1[6:0]						
0x750C	0x00	MSA_HSTART_B0[7:0]	MSA_HSTART_B0[7:0]							
0x750D	0x00	MSA_HSTART_B1[7:0]	MSA_HSTART_B1[7:0]							
0x7510	0x00	MSA_HTOTAL_B0[7:0]	MSA_HTOTAL_B0[7:0]							
0x7511	0x00	MSA_HTOTAL_B1[7:0]	MSA_HTOTAL_B1[7:0]							
0x7514	0x00	MSA_VRES_B0[7:0]	MSA_VRES_B0[7:0]							
0x7515	0x00	MSA_VRES_B1[7:0]	MSA_VRES_B1[7:0]							
0x7518	0x00	MSA_VSPOL[7:0]	–	–	–	–	–	–	–	MSA_VSPOL
0x751C	0x00	MSA_VSWIDTH_B0[7:0]	MSA_VSWIDTH_B0[7:0]							
0x751D	0x00	MSA_VSWIDTH_B1[7:0]	–	MSA_VSWIDTH_B1[6:0]						
0x7520	0x00	MSA_VSTART_B0[7:0]	MSA_VSTART_B0[7:0]							
0x7521	0x00	MSA_VSTART_B1[7:0]	MSA_VSTART_B1[7:0]							

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0x7524	0x00	MSA_VTOTAL_B0[7:0]	MSA_VTOTAL_B0[7:0]							
0x7525	0x00	MSA_VTOTAL_B1[7:0]	MSA_VTOTAL_B1[7:0]							
0x7528	0x00	MSA_MISC0[7:0]	MSA_COLOR_DEPTH[2:0]			MSA_YCBCR_COLOR	MSA_DYNAMIC_RANGE	MSA_COMP_FORMAT[1:0]		MSA_CLOCKING_MODE
0x752C	0x00	MSA_MISC1[7:0]	MSA_Y_ONLY	–	–	–	–	MSA_STEREO_VIDEO[1:0]		MSA_INTERLACED_EVEN
0x7530	0x00	MSA_MVID_B0[7:0]	MSA_MVID_B0[7:0]							
0x7531	0x00	MSA_MVID_B1[7:0]	MSA_MVID_B1[7:0]							
0x7532	0x00	MSA_MVID_B2[7:0]	MSA_MVID_B2[7:0]							
0x7534	0x00	MSA_NVID_B0[7:0]	MSA_NVID_B0[7:0]							
0x7535	0x00	MSA_NVID_B1[7:0]	MSA_NVID_B1[7:0]							
0x7536	0x00	MSA_NVID_B2[7:0]	MSA_NVID_B2[7:0]							
0x7538	0x00	MSA_VBID[7:0]	–	RSVD	RSVD	RSVD	MSA_VBID_NO_VIDEO	MSA_VBID_INTERLACED	MSA_VBID_FIELD_ID	MSA_VBID_VERT_BLANK
0x7540	0x00	MSA_VIRTUAL_SINK_SELECT[7:0]	–	–	–	–	–	–	MSA_VIRTUAL_SINK_SELECT[1:0]	
0x7900	0x00	MST_SST_PORT_SELECT[7:0]	–	–	–	–	–	–	MST_SST_PORT_SELECT[1:0]	
0x7904	0x00	MST_PAYLOAD_ID_0[7:0]	–	MST_PAYLOAD_ID_0[6:0]						
0x7908	0x00	MST_PAYLOAD_ID_1[7:0]	–	MST_PAYLOAD_ID_1[6:0]						
0x790C	0x00	MST_PAYLOAD_ID_2[7:0]	–	MST_PAYLOAD_ID_2[6:0]						
0x7910	0x00	MST_PAYLOAD_ID_3[7:0]	–	MST_PAYLOAD_ID_3[6:0]						
0x7934	0x01	MST_CLEAR_PAYLOAD_ID_TABLE[7:0]	–	–	–	–	–	–	–	MST_CLEAR_PAYLOAD_ID_TABLE
0x7A00	0x01	MST_VS0_ENABLE[7:0]	–	–	–	–	–	–	–	VS_ENABLE
0x7A08	0x00	MST_VS0_SWAP_CBCR[7:0]	–	–	–	–	–	–	–	SWAP_CBCR

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0x7A10	0x00	MST_VS0_VIDEO_FIFO_OVERFLOW[7:0]	–	–	–	–	–	–	–	VIDEO_FIFO_OVERFLOW
0x7A14	0x00	MST_VS0_DTG_ENABLE[7:0]	–	–	–	–	–	–	–	DTG_ENABLE
0x7A24	0x3F	MST_VS0_DMA_VSYNC_B0[7:0]	DMA_VSYNC_PULSE_WIDTH[7:0]							
0x7A26	0xFF	MST_VS0_DMA_VSYNC_B2[7:0]	DMA_VSYNC_FRONT_PORCH_L[7:0]							
0x7A27	0x01	MST_VS0_DMA_VSYNC_B3[7:0]	–	–	–	–	DMA_VSYNC_FRONT_PORCH_H[3:0]			
0x7A28	0x0F	MST_VS0_DMA_HSYNC_B0[7:0]	DMA_HSYNC_PULSE_WIDTH_L[7:0]							
0x7A29	0x00	MST_VS0_DMA_HSYNC_B1[7:0]	–	–	–	–	DMA_HSYNC_PULSE_WIDTH_H[3:0]			
0x7A2A	0x0F	MST_VS0_DMA_HSYNC_B2[7:0]	DMA_HSYNC_FRONT_PORCH_L[7:0]							
0x7A2B	0x00	MST_VS0_DMA_HSYNC_B3[7:0]	–	–	–	–	DMA_HSYNC_FRONT_PORCH_H[3:0]			
0x7A38	0x00	MST_VS0_RED_CRC_B0[7:0]	RED_CRC_B0[7:0]							
0x7A39	0x00	MST_VS0_RED_CRC_B1[7:0]	RED_CRC_B1[7:0]							
0x7A3B	0x00	MST_VS0_RED_CRC_B3[7:0]	CRC_UPDATED	–	–	–	–	–	–	–
0x7A3C	0x00	MST_VS0_GRN_BLU_CRC_B0[7:0]	BLU_CRC_B0[7:0]							
0x7A3D	0x00	MST_VS0_GRN_BLU_CRC_B1[7:0]	BLU_CRC_B1[7:0]							
0x7A3E	0x00	MST_VS0_GRN_BLU_CRC_B2[7:0]	GRN_CRC_B0[7:0]							
0x7A3F	0x00	MST_VS0_GRN_BLU_CRC_B3[7:0]	GRN_CRC_B1[7:0]							
0x7A40	0x00	MST_VS0_MSA_IGNORE_HRES_B0[7:0]	MSA_IGNORE_HRES_B0[7:0]							

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0x7A41	0x00	MST_VS0_MSA_IGNORE_HRES_B1[7:0]	MSA_IGNORE_HRES_B1[7:0]							
0x7B00	0x00	MST_VS1_ENABLE[7:0]	–	–	–	–	–	–	–	VS_ENABLE
0x7B08	0x00	MST_VS1_SWAP_CBCR[7:0]	–	–	–	–	–	–	–	SWAP_CBCR
0x7B10	0x00	MST_VS1_VIDEO_FIFO_OVERFLOW[7:0]	–	–	–	–	–	–	–	VIDEO_FIFO_OVERFLOW
0x7B14	0x00	MST_VS1_DTG_ENABLE[7:0]	–	–	–	–	–	–	–	DTG_ENABLE
0x7B24	0x3F	MST_VS1_DMA_VSYNC_B0[7:0]	DMA_VSYNC_PULSE_WIDTH[7:0]							
0x7B26	0xFF	MST_VS1_DMA_VSYNC_B2[7:0]	DMA_VSYNC_FRONT_PORCH_L[7:0]							
0x7B27	0x01	MST_VS1_DMA_VSYNC_B3[7:0]	–	–	–	–	DMA_VSYNC_FRONT_PORCH_H[3:0]			
0x7B28	0x0F	MST_VS1_DMA_HSYNC_B0[7:0]	DMA_HSYNC_PULSE_WIDTH_L[7:0]							
0x7B29	0x00	MST_VS1_DMA_HSYNC_B1[7:0]	–	–	–	–	DMA_HSYNC_PULSE_WIDTH_H[3:0]			
0x7B2A	0x0F	MST_VS1_DMA_HSYNC_B2[7:0]	DMA_HSYNC_FRONT_PORCH_L[7:0]							
0x7B2B	0x00	MST_VS1_DMA_HSYNC_B3[7:0]	–	–	–	–	DMA_HSYNC_FRONT_PORCH_H[3:0]			
0x7B38	0x00	MST_VS1_RED_CRC_B0[7:0]	RED_CRC_B0[7:0]							
0x7B39	0x00	MST_VS1_RED_CRC_B1[7:0]	RED_CRC_B1[7:0]							
0x7B3B	0x00	MST_VS1_RED_CRC_B3[7:0]	CRC_UPDATED	–	–	–	–	–	–	–
0x7B3C	0x00	MST_VS1_GRN_BLU_CRC_B0[7:0]	BLU_CRC_B0[7:0]							
0x7B3D	0x00	MST_VS1_GRN_BLU_CRC_B1[7:0]	BLU_CRC_B1[7:0]							

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0x7B3E	0x00	MST_VS1_GRN_BLU_CRC_B2[7:0]	GRN_CRC_B0[7:0]							
0x7B3F	0x00	MST_VS1_GRN_BLU_CRC_B3[7:0]	GRN_CRC_B1[7:0]							
0x7B40	0x00	MST_VS1_MSA_IGNORE_HRES_B0[7:0]	MSA_IGNORE_HRES_B0[7:0]							
0x7B41	0x00	MST_VS1_MSA_IGNORE_HRES_B1[7:0]	MSA_IGNORE_HRES_B1[7:0]							
DPCD										

Register Details

REG0 (0x0)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	I^{2}C/UART Device Address Default value is set according to the latched CFG pin value at power-up. See CFG pin decoding table in the data sheet.	0b0000000: I^{2}C write/read address is 0x00/0x01 0b0000001: I^{2}C write/read address is 0x02/0x03 ... ... 0b1000000: I^{2}C write/read address is 0x80/0x81 0b1000010: I^{2}C write/read address is 0x84/0x85 0b1000100: I^{2}C write/read address is 0x88/0x89 0b1100000: I^{2}C write/read address is 0xC0/0xC1 0b1100010: I^{2}C write/read address is 0xC4/0xC5 0b1100100: I^{2}C write/read address is 0xC8/0xC9 0b0100000: I^{2}C write/read address is 0x40/0x41 0b0100010: I^{2}C write/read address is 0x44/0x45 ... ... 0b1111111: I^{2}C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.	0b0: Not Blocked 0b1: Blocked

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REG2 (0x2)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_TX_Y_SRC	AUD_TX_X_SRC	AUD_TX_EN_Y	AUD_TX_EN_X	–	–	RSVD	RSVD
Reset	0b1	0b0	0b0	0b0	–	–	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_TX_Y_SRC	7	Selects audio-input pins to use for forward audio engine Y	0b0: SCK1, SD1, WS1 0b1: SCK2, SD2, WS2
AUD_TX_X_SRC	6	Selects audio-input pins to use for forward audio engine X	0b0: SCK1, SD1, WS1 0b1: SCK2, SD2, WS2
AUD_TX_EN_Y	5	Audio Transmit Enable for GMSL2 Port Y	0b0: Audio transmit Channel Y disabled 0b1: Audio transmit Channel Y enabled
AUD_TX_EN_X	4	Audio Transmit Enable for GMSL2 Port X	0b0: Audio transmit Channel X disabled 0b1: Audio transmit Channel X enabled

REG3 (0x3)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	I2CSEL	RCLKEN	–	RCLKSEL[1:0]	
Reset	–	–	–	0b0	0b0	–	0b00	
Access Type	–	–	–	Write, Read	Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
I2CSEL	4	I^2C/UART selection. Initial value is set according to the latched CFG pin value at power-up.	0b0: UART selected 0b1: I^2C selected
RCLKEN	3	Enables RCLK Output	0b0: RCLK output disabled 0b1: RCLK output enabled
RCLKSEL	1:0	RCLKOUT Clock Selection	0b00: XTAL/1 = 25MHz 0b01: XTAL/2 = 12.5MHz 0b10: XTAL/4 = 6.25MHz 0b11: Reserved

REG4 (0x4)*

BIT	7	6	5	4	3	2	1	0
Field	GMSL1_B	GMSL1_A	HVD_OUT_EN	DIS_LOCAL_CC	RSVD	RSVD	PAR_VID_EN	SW_INT
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL1_B	7	GMSL1/GMSL2 selection for Link B Bit is set according to the latched GMSL2 pin value at power-up.	0b0: Link B is GMSL2 0b1: Link B is GMSL1

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BITFIELD	BITS	DESCRIPTION	DECODE
GMSL1_A	6	GMSL1/GMSL2 selection for Link A Bit is set according to the latched GMSL2 pin value at power-up.	0b0: Link A is GMSL2 0b1: Link A is GMSL1
HVD_OUT_EN	5	Enable HS,VS, DE, PCLK output from MFP22-MFP25. DEBUG_EXTRA in register TEST_1 selects the pipeline and HVD tap point.	0b0: HS, VS, DE, PCLK outputs disabled 0b1: HS, VS, DE, PCLK outputs enabled
DIS_LOCAL_CC	4	Disables control-channel connection to RX/SDA and TX/SCL pins	0b0: RX/SDA and TX/SCL pins are connected to control channel 0b1: RX/SDA and TX/SCL pins are disconnected from control channel, registers can be programmed from remote side
PAR_VID_EN	1	Enables parallel video PCLK input	0b0: Parallel video disabled 0b1: Parallel video enabled
SW_INT	0	Software interrupt to mark power-up Write 0 to clear after the part is configured.	0b0: Part is configured 0b1: Part is not configured

REG5 (0x5)*

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	–	LOCK_CFG	PU_LF3	PU_LF2	PU_LF1	PU_LF0
Reset	0b1	0b1	–	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enables LOCK output.	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enables ERRB output	0b0: ERRB output disabled 0b1: ERRB output enabled
LOCK_CFG	4	Controls the behavior of LOCK pin in splitter and dual-link modes.	0b0: Link A OR Link B is locked 0b1: Link A AND Link B are locked
PU_LF3	3	Powers Up Line-Fault Monitor 3	0b0: Line-fault monitor 3 disabled 0b1: Line-fault monitor 3 enabled
PU_LF2	2	Powers Up Line-Fault Monitor 2	0b0: Line-fault monitor 2 disabled 0b1: Line-fault monitor 2 enabled
PU_LF1	1	Powers Up Line-Fault Monitor 1	0b0: Line-fault monitor 1 disabled 0b1: Line-fault monitor 1 enabled
PU_LF0	0	Powers Up Line-Fault Monitor 0	0b0: Line-fault monitor 0 disabled 0b1: Line-fault monitor 0 enabled

PWR0 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[1:0]		CMP_STATUS[5:0]					
Reset	0b00		0b000000					
Access Type	Read Only		Read Only					

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BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:6	Power manager switched 1V supply comparator status bits [1:0]. Bits are latched high when V_{DD_sw} < 0.806V.	0b00: V_{DD_sw} ≥ 0.806V 0b01: V_{DD_sw} < 0.806V 0b01: V_{DD_sw} < 0.806V 0b11: V_{DD_sw} < 0.806V
CMP_STATUS	5:0	Power manager comparator status bits	Bit 0: latched low when V_{DD18} < 1.617V Bit 1: latched low when switched V_{DDIO} supply < 1.617V Bit 2: latched low when V_{DD_sw} < 0.82V Bit 3: 0 when V_{DD_sw} < 1.062V (live) Bit 4: 0 when V_{DD} < 1.103V (live) Bit 5: Reserved

PWR1 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	VDDBAD_STATUS_H	RSVD[5:0]					
Reset	0b0	0b0	0b000000					
Access Type		Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS_H	6	Switched 1V supply comparator status bit [2]	0b0: LDO not powered on 0b1: LDO powered on

PWR4 (0xC)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			
Reset	0b0	0b0	0b1	0b1	0x5			
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable wake-up by local µC from SDA_RX Pin	0b0: Local wake-up enabled 0b1: Local wake-up disabled
WAKE_EN_B	5	Enable wake-up by remote chip connected to Link B	0b0: Link B remote wake-up disabled 0b1: Link B remote wake-up enabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to Link A	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0xFF							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Instead of reading from here, read the 16-bit device ID register from DEV_ID16_MSB (0x25) and DEV_ID16_LSB (0x24).	0xFF: See DEV_ID16_LSB for Device ID

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	DEV_REV[3:0]			
Reset	–	–	0b0	0b0	0x0			
Access Type	–	–			Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision	0xX: Device revision number

REG15 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RSVD[1:0]		–	DUAL_CPBL_N	SPLTR_CPBL_N	HDCP_CPBL
Reset	0b0	–	0b00		–	0b0	0b0	0b0
Access Type		–			–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DUAL_CPBL_N	2	GMSL2 Dual-Link Capability	0b0: Dual-link mode is available 0b1: Dual-link mode is not available
SPLTR_CPBL_N	1	GMSL2 Splitter Mode Capability	0b0: Splitter mode is available 0b1: Splitter mode is not available
HDCP_CPBL	0	HDCP Capability	0b0: HDCP not enabled on this device 0b1: HDCP enabled on this device

CTRL0 (0x10)*

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	–	–	AUTO_LINK	SLEEP	RSVD	LINK_CFG[1:0]	
Reset	0b0	–	–	0b1	0b0	0b0	0b01	
Access Type	Write, Read	–	–	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Writing a 1 to this bit resets the device including all blocks, and registers are reset to defaults. Do not use if using sleep mode. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset

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BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_LINK	4	Automatically select link configuration (single A, single B or dual) Splitter mode is not automatic. For splitter mode, set LINK_CFG = 11.	0b0: Disable auto-link configuration 0b1: Enable auto-link configuration
SLEEP	3	Activates Sleep Mode	0b0: Sleep mode disabled 0b1: Sleep mode enabled
LINK_CFG	1:0	AUTO_LINK and this bitfield select the link configuration per the decode table	0b00: Dual Link 0b01: Single A 0b10: Single B 0b11: Splitter

CTRL1 (0x11)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	RSVD	CXTP_B	RSVD	CXTP_A
Reset	0b0	0b0	0b0	–	0b1	0b0	0b1	0b0
Access Type				–		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_B	2	Coax/twisted-pair cable select for Link B Bit is set according to the latched CFG pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/twisted-pair cable select for Link A Bit is set according to the latched CFG pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

CTRL3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	HPD_IN	–	–	–	LOCKED	ERROR	CMU_LOCKED	–
Reset	0b0	–	–	–	0b0	0b0	0b0	–
Access Type	Read Only	–	–	–	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IN	7	Reads back HPD pin level	0b0: Disabled 0b1: Enabled
LOCKED	3	GMSL link locked (bidirectional)	0b0: GMSL link not locked 0b1: GMSL link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = high) 0b1: ERRB asserted (ERRB pin = low)
CMU_LOCKED	1	Clock Multiplier Unit (CMU) Locked	0b0: CMU not locked 0b1: CMU locked

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INTR0 (0x18)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	–	–	–	–	0b0	0b000		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A, DEC_ERR_B, IDLE_ERR_A, and IDLE_ERR_B bitfields after ERRB pin is asserted for 1µs.	0b0: Auto reset disabled 0b1: Auto reset enabled
DEC_ERR_THR	2:0	Decoding and idle error reporting threshold. DEC_ERR_FLAG_A is asserted when DEC_ERR_A ≥ DEC_ERR_THR. DEC_ERR_FLAG_B is asserted when DEC_ERR_B ≥ DEC_ERR_THR. IDLE_ERR_FLAG is asserted when IDLE_ERR_A ≥ DEC_ERR_THR or IDLE_ERR_B ≥ DEC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

INTR1 (0x19)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0b0				0b0	0b000		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet Count Multiplier Exponent See the description of PKT_CNT bitfield (register LCTRL5).	0bXXX: PKT_CNT exponent
AUTO_CNT_RST_EN	3	Automatically resets PKT_CNT bitfield (register LCTRL5) after ERRB pin is asserted for 1µs.	0b0: Automatic reset disabled 0b1: Automatic reset enabled
PKT_CNT_THR	2:0	Packet count reporting threshold (see PKT_CNT description - register LCTRL5) PKT_CNT_FLAG is asserted when PKT_CNT_A ≥ PKT_CNT_THR or PKT_CNT_B ≥ PKT_CNT_THR.	0b000: 1 packet 0b001: 2 packets 0b010: 4 packets 0b011: 8 packets 0b100: 16 packets 0b101: 32 packets 0b110: 64 packets 0b111: 128 packets

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INTR2 (0x1A)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	REM_ERR_OEN_A	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0b0	0b0	–	0b0	0b1	0b0	0b1	0b1
Access Type			–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_OEN_A	4	Enables reporting of remote error status (REM_ERR_A—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_OEN	3	Enables reporting of line fault interrupt (LFLT_INT—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
IDLE_ERR_OEN	2	Enables reporting of idle word errors (IDLE_ERR_FLAG—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_B	1	Enables reporting of decoding errors (DEC_ERR_FLAG_B—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enables reporting of decoding errors (DEC_ERR_FLAG_A— 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	REM_ERR_FLAG_A	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0b0	0b0	–	0b0	0b0	0b0	0b0	0b0
Access Type			–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_FLAG_A	4	Received remote side error status (inverse of remote side ERRB pin level on Link A)	0b0: No remote side error 0b1: Remote side error
LFLT_INT	3	Line-Fault Interrupt Asserted when any of line fault monitors indicate a fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line fault condition needs to be cleared to clear this flag. Use LFLT_STKY_INT register to set interrupt behavior.	0b0: No line fault 0b1: Line fault
IDLE_ERR_FLAG	2	Idle Word Error Flag Asserted when IDLE_ERR_A ≥ DEC_ERR_THR or when IDLE_ERR_B ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_B	1	Decoding Error Flag for Link B Asserted when DEC_ERR_B ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted

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BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_FLAG_A	0	Decoding Error for Link A Asserted when DEC_ERR_A ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted

INTR4 (0x1C)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	HDCP_INT_OEN_A	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	–
Reset	0b0	0b0	–	0b0	0b1	0b0	0b0	–
Access Type			–	Write, Read	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_INT_OEN_A	4	Enables reporting of GMSL HDCP interrupt (HDCP_INT_A_FLAG—0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG—0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG—0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enables reporting of packet count flag (PKT_CNT_FLAG—0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	HDCP_INT_FLAG_A	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	–
Reset	0b0	0b0	–	0b0	0b0	0b0	0b0	–
Access Type			–	Read Only	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_INT_FLAG_A	4	HDCP Interrupt Status Asserted when there is a GMSL HDCP interrupt.	0b0: No HDCP interrupt 0b1: HDCP interrupt
MAX_RT_FLAG	3	Combined ARQ maximum retransmission limit error flag Asserted when any of the selected channels ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN (register ARQ1) bit.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG	2	Combined ARQ retransmission event flag Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN (0x1C) register bit.	0b0: Flag not asserted 0b1: Flag asserted

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BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_FLAG	1	Packet Count Flag Asserted when PKT_CNT_A ≥ PKT_CNT_THR (0x19) or PKT_CNT_B ≥ PKT_CNT_THR.	0b0: Flag not asserted 0b1: Flag asserted

INTR6 (0x1E)*

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	RSVD	VDDBAD_INT_OEN	VDD_OV_OEN	DPRX_INT_OEN	–	–	INT_ERR_OEN
Reset	0b1	0b1	0b1	0b0	0b0	–	–	0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	7	Enables reporting of combined V_{DD} comparator output (VDDCMP_INT_FLAG—0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VDDBAD_INT_OEN	5	Enable reporting of V_{DDBAD} interrupt (VDDBAD_INT_FLAG—0x1F) at ERRB pin	0b0: Disable V_{DDBAD} interrupt reporting 0b1: Enable V_{DDBAD} interrupt reporting
VDD_OV_OEN	4	Enables V_{DD} overvoltage status on ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DPRX_INT_OEN	3	Enables reporting of display port receiver interrupt (DPRX_INT—0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
INT_ERR_OEN	0	Enable reporting internal error conditions (INT_ERR_FLAG—0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	RSVD	VDDBAD_INT_FLAG	VDD_OV_FLAG	DPRX_INT	–	–	INT_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	–	–	0b0
Access Type	Read Clears All		Read Clears All	Read Clears All	Read Only	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	7	Combined V_{DD} comparator output	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	5	Combined V_{DDBAD} Indicator	0b0: Disable V_{DDBAD} interrupt reporting 0b1: Enable V_{DDBAD} interrupt reporting
VDD_OV_FLAG	4	V_{DD} Overvoltage Flag This bit stays high when asserted and must be cleared by the user. It is set when V_{DD} exceeds the overvoltage threshold. It is cleared when read.	0b0: V_{DD} overvoltage not detected 0b1: V_{DD} overvoltage detected
DPRX_INT	3	DPRX Interrupt	0b0: Flag not asserted 0b1: Flag asserted

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BITFIELD	BITS	DESCRIPTION	DECODE
INT_ERR_FLAG	0	Combined Internal Error flag This flag is asserted when any one of these is asserted: OVERFLOW_A_X/Y/Z/U OVERFLOW_B_X/Y/Z/U DRIFT_ERR_A_X/Y/Z/U DRIFT_ERR_B_X/Y/Z/U ASYM_OVERFLOW_X/Y/Z/U AUD_OVERFLOW_X/Y AUD_DRIFT_ERR_X/Y AUD_BLK_LEN_ERR_X/Y UART_TX_OVERFLOW_A/B UART_RX_OVERFLOW_A/B UART_TX_OVERFLOW_1_A/B UART_RX_OVERFLOW_1_A/B UART_TX_OVERFLOW_2_A/B UART_RX_OVERFLOW_2_A/B SPI_TX_OVRFLW SPI_RX_OVRFLW FAILLOCK_A/B	0b0: Flag not asserted 0b1: Flag asserted

INTR8 (0x20)*

BIT	7	6	5	4	3	2	1	0
Field	SW_INT_OEN	VDDIO_OV_OEN	VDD1P8_OV_OEN	RSVD	LOCK_B_OEN	LOCK_A_OEN	LOCK_OEN	LOSS_OF_LOCK_OEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SW_INT_OEN	7	Enables reporting of software interrupt on ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VDDIO_OV_OEN	6	Enables V_{DDIO} overvoltage status on ERRB.	0b0: Reporting disabled 0b1: Reporting enabled
VDD1P8_OV_OEN	5	Enables V_{DD1P8} overvoltage status on ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LOCK_B_OEN	3	Enables reporting of Link B lock status (LOCK_B_FLAG—0x21) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LOCK_A_OEN	2	Enables reporting of Link A lock status (LOCK_A_FLAG—0x21) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LOCK_OEN	1	Enables reporting of lock pin status (LOCK_FLAG—0x21) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LOSS_OF_LOCK_OEN	0	Enables reporting loss of lock at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

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INTR9 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	SW_INT_FLAG	VDDIO_OV_FLAG	VDD1P8_OV_FLAG	VREG_OV_FLAG	LOCK_B_FLAG	LOCK_A_FLAG	LOCK_FLAG	LOSS_OF_LOCK_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SW_INT_FLAG	7	Software Interrupt Read-Only Value Follows the value of writable SW_INT (0x4) register bit.	0b0: Flag not asserted 0b1: Flag asserted
VDDIO_OV_FLAG	6	Sticky status value for V_{DDIO} overvoltage	0b0: Flag not asserted 0b1: Flag asserted
VDD1P8_OV_FLAG	5	Sticky status value for V_{DD1P8} overvoltage	0b0: Flag not asserted 0b1: Flag asserted
VREG_OV_FLAG	4	Sticky status value for V_{REG} overvoltage	0b0: Flag not asserted 0b1: Flag asserted
LOCK_B_FLAG	3	Link B Lock Status	0b0: Flag not asserted 0b1: Flag asserted
LOCK_A_FLAG	2	Link A Lock Status	0b0: Flag not asserted 0b1: Flag asserted
LOCK_FLAG	1	Lock pin status	0b0: Flag not asserted 0b1: Flag asserted
LOSS_OF_LOCK_FLAG	0	Loss of lock on GMSL link is detected (sticky)	0b0: Not detected 0b1: Detected

INTR10 (0x22)*

BIT	7	6	5	4	3	2	1	0
Field	LFLT_INT_OPEN_OEN	LFLT_INT_L2LS_OEN	LFLT_INT_BAT_S_OEN	LFLT_INT_GND_S_OEN	REG_CRC_ERR_OEN	I2C_UART_MSGCNTR_ERR_OEN	I2C_UART_CRC_ERR_OEN	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_OPEN_OEN	7	Enables reporting of line fault open interrupt (LFLT_INT_OPEN—0x23) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_L2LS_OEN	6	Enables reporting of line-to-line short line-fault interrupt (LFLT_INT—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_BAT_S_OEN	5	Enables reporting of short-to-battery line-fault interrupt (LFLT_INT—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_GND_S_OEN	4	Enables reporting of short-to-ground line-fault interrupt (LFLT_INT—0x1B) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
REG_CRC_ERR_OEN	3	Enable reporting register CRC at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
I2C_UART_MSGCNTR_ERR_OEN	2	Enables reporting of I²C/UART message count errors (I2C_UART_MSGCNTR_ERR_FLAG—0x23) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
I2C_UART_CRC_ERR_OEN	1	Enables reporting of I²C/UART CRC errors (I2C_UART_CRC_ERR_FLAG—0x23) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

INTR11 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	LFLT_INT_OPEN	LFLT_INT_L2LS	LFLT_INT_BAT_S	LFLT_INT_GND_S	REG_CRC_ERR_FLAG	I2C_UART_MSGCNTR_ERR_FLAG	I2C_UART_CRC_ERR_FLAG	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_OPEN	7	Line Fault Interrupt Asserted when either one of line-fault monitors indicates an open-fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line fault condition needs to be cleared to clear this flag. Use LFLT_STKY_INT register to set interrupt behavior.	0b0: No line fault 0b1: Line fault
LFLT_INT_L2LS	6	Line-Fault Interrupt Asserted when either one of line-fault monitors indicates a line-to-line short fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line-fault condition needs to be cleared to clear this flag. Use LFLT_STKY_INT register to set interrupt behavior.	0b0: No line fault 0b1: Line fault
LFLT_INT_BAT_S	5	Line-Fault Interrupt Asserted when either one of line-fault monitors indicates a short-to-battery fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line-fault condition needs to be cleared to clear this flag. Use LFLT_STKY_INT register to set interrupt behavior.	0b0: No line fault 0b1: Line fault

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BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_GND_S	4	Line-Fault Interrupt Asserted when either one of line-fault monitors indicates a short-to-ground fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line-fault condition needs to be cleared to clear this flag. Use LFLT_STKY_INT register to set interrupt behavior.	0b0: No line fault 0b1: Line fault
REG_CRC_ERR_FLAG	3	An error occurred on the register CRC calculation	0b0: Flag not asserted 0b1: Flag asserted
I2C_UART_MSGCNTR_ERR_FLAG	2	I^2C/UART Message Count Error Flag Asserted when MSGCNTR_ERR_CNx is nonzero.	0b0: Flag not asserted 0b1: Flag asserted
I2C_UART_CRC_ERR_FLAG	1	I^2C/UART CRC Error Flag Asserted when CC_CRC_ERR_CNT is nonzero.	0b0: Flag not asserted 0b1: Flag asserted

DEV_ID16_LSB (0x24)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID16_LSB[7:0]							
Reset	0x30							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID16_LSB	7:0	16-Bit Device Identifier	0x30 - MAX96781 0x31 - MAX96783

DEV_ID16_MSB (0x25)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID16_MSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DEV_ID16_MSB	7:0	16-Bit Device Identifier

LF0_LF1 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_1[2:0]			–	LF_0[2:0]		
Reset	–	0b010			–	0b010		
Access Type	–	Read Only			–	Read Only		

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BITFIELD	BITS	DESCRIPTION	DECODE
LF_1	6:4	Line-fault status of wire connected to LMN1 pin	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short
LF_0	2:0	Line-fault status of wire connected to LMN0 pin	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

LF2_LF3 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_3[2:0]			–	LF_2[2:0]		
Reset	–	0b010			–	0b010		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_3	6:4	Line-fault status of wire connected to LMN3 pin	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short
LF_2	2:0	Line-fault status of wire connected to LMN2 pin	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

LCTRL0 (0x28)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_EN	–	–	–	TX_RATE[1:0]		RSVD[1:0]	
Reset	0b1	–	–	–	0b10		0b00	
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_EN	7	Enables GMSL link A	0b0: Link A is disabled 0b1: Link A is enabled
TX_RATE	3:2	Transmitter (forward channel) bit rate When changed, becomes active after the next link reset. Default value is set by the CFG pin at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

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LCTRL1 (0x29)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	–	–	RESET_ONESHOT	RESET_LINK
Reset	–	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	–				–	–	Write Clears All, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ONESHOT	1	Reset entire data path in one-shot (keep register settings) Write 1 to activate reset. Bit automatically clears and releases reset.	0b0: No action 0b1: Reset data path
RESET_LINK	0	Resets whole data path (keep register settings) Write a 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset

LCTRL2 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	RSVD	LINK_LOCKED
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	2	Reserved	
RSVD	1	Reserved	
LINK_LOCKED	0	GMSL link locked (bidirectional)	0b0: GMSL link not locked 0b1: GMSL link locked

LCTRL3 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR	7:0	Number of decoding (disparity) errors detected at this link Resets after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

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LCTRL4 (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of idle word errors detected on this link Resets after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

LCTRL5 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of received packets of a selected type at this link Packet type is selected with PKT_CNT_SEL register. Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT x ($2^{PKT_CNT_EXP}$) and < (PKT_CNT + 1) x ($2^{PKT_CNT_EXP}$). When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

LCTRL6 (0x2E)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0b1	–	–	0b11111				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmits local error status (inverse of ERRB pin level) to remote side through GPIO channel	0b0: Transmit error status disabled 0b1: Transmit error status enabled
ERR_TX_ID	4:0	GPIO ID used for transmitting error status	0bXXXXX: Value of GPIO ID for transmitting ERR_TX

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LCTRL7 (0x2F)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
Reset	0b1	0b1	–	0b11111				
Access Type	Write, Read	Read Only	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Receives remote error status (ERRB pin level) through GPIO channel with ERR_RX_ID	0b0: Receive error status disabled 0b1: Receive error status enabled
RSVD	6	Received error status value with ERR_RX_ID	0b0: Disabled 0b1: Enabled
ERR_RX_ID	4:0	First GPIO ID used for receiving error status	0bXXXXX: Value of GPIO ID for receiving ERR_TX

LCTRL8 (0x30)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN2	RSVD	–	ERR_RX_ID2[4:0]				
Reset	0b0	0b1	–	0b11110				
Access Type	Write, Read	Read Only	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN2	7	Receives remote error status (ERRB pin level) through GPIO channel with ERR_RX_ID2	0b0: Receive error status disabled 0b1: Receive error status enabled
RSVD	6	Received error status value with ERR_RX_ID2	0b0: Disabled 0b1: Enabled
ERR_RX_ID2	4:0	Second GPIO ID used for receiving error status	0bXXXXX: Value of GPIO ID for receiving ERR_TX

LCTRL9 (0x31)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN3	RSVD	–	ERR_RX_ID3[4:0]				
Reset	0b0	0b1	–	0b11011				
Access Type	Write, Read	Read Only	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN3	7	Receives remote error status (ERRB pin level) through GPIO channel with ERR_RX_ID3	0b0: Receive error status disabled 0b1: Receive error status enabled
RSVD	6	Received error status value with ERR_RX_ID3	0b0: Disabled 0b1: Enabled
ERR_RX_ID3	4:0	Third GPIO ID used for receiving error status	0bXXXXX: Value of GPIO ID for receiving ERR_TX

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LCTRL0 (0x32)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_EN	–	–	–	–	–	–	–
Reset	0b1	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_EN	7	Enables GMSL link B	0b0: Link B is disabled 0b1: Link B is enabled

LCTRL3 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR	7:0	Number of decoding (disparity) errors detected at this link Resets after reading or with the rising edge of LOCK.	0xXX: Number of Link B decoding errors detected

LCTRL4 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of idle word errors detected on this link Resets after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

LCTRL5 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

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BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of received packets of a selected type at this link Packet type is selected with PKT_CNT_SEL register. Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT x ($2^{PKT_CNT_EXP}$) and < (PKT_CNT + 1) x ($2^{PKT_CNT_EXP}$). When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

TX1 (0x51)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_GEN	–	–	ERRG_EN	–	–	RSVD	RSVD
Reset	0b0	–	–	0b0	–	–	0b0	0b0
Access Type	Write, Read	–	–	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_GEN	7	Enables link PRBS-7 generator	
ERRG_EN	4	Error Generator Enable	0b0: Error generator disabled 0b1: Error generator enabled

TX2 (0x52)*

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0b00		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error generator average bit-error rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits
ERRG_BURST	3:1	Selects the error generator burst-error length in bits For example, if the bitfield value is 0b100, the burst-error length is 8 bits. Thus, each time an 8-bit error burst is generated, there is an error in the first and the last bit of the 8-bit window and the probability of an error in each of the remaining 6 bits is 50%.	0b000: 1 bit 0b001: 2 bits 0b010: 3 bits 0b011: 4 bits 0b100: 8 bits 0b101: 12 bits 0b110: 16 bits 0b111: 20 bits

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BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_PER	0	Error generator error distribution selection	0b0: Pseudorandom 0b1: Periodic

TX3 (0x53)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD	RSVD[1:0]		TIMEOUT[2:0]		
Reset	0b01		0b0	0b10		0b100		
Access Type						Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	ARQ timeout duration multiplier Multiplies a timeout base constant to set the ARQ timeout.	0b000: 0.5 x timeout base 0b001: 1.0 x timeout base 0b010: 1.5 x timeout base 0b011: 2.0 x timeout base 0b100: 2.5 x timeout base 0b101: 3.0 x timeout base 0b110: 3.5 x timeout base 0b111: 4.0 x timeout base

RX0 (0x54)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
Reset	0b00		0b0	0b0	0b0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Selects the sub-type of low-bandwidth (LBW) packets to count at PKT_CNT (register LCTRL5)	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Selects the type of received packets to count at PKT_CNT (register LCTRL5).	0b0000: None 0b0001: VIDEO 0b0010: AUDIO 0b0011: INFO Frame 0b0100: SPI 0b0101: I^2C 0b0110: UART 0b0111: GPIO 0b1000: AHDCP 0b1001: Reserved 0b1010: Reserved 0b1011: Reserved 0b1100: Reserved 0b1011: Reserved 0b1110: All 0b1111: Unknown and packets with error

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RX1 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_CHK	RSVD	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD
Reset	0b0	0b0	0b11		0b01		0b0	0b0
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_CHK	7	Enable link PRBS-7 checker	0b0: Link PRBS checker disabled 0b1: Link PRBS checker enabled

RX3 (0x57)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FAILLOCK
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type								Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
FAILLOCK	0	Failed word boundary lock. The status register is latched.	0b0: Not failed during lock 0b1: Failed during lock

GPIOA (0x58)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0b1	0b000001					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_FAST_BIDIR_EN	7	GPIO fast-direction switch for bidirectional IO.	0b0: Fast-direction switch disabled 0b1: Fast-direction switch enabled
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward-compensation delay multiplier value

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GPIOB (0x59)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0b10		0b001000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet This allows grouping transitions of different GPIO inputs in a single packet and therefore increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse-compensation delay multiplier value

TX1 (0x61)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERRG_EN	–	–	–	–
Reset	–	–	–	0b0	–	–	–	–
Access Type	–	–	–	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_EN	4	Error Generator Enable	0b0: Error generator disabled 0b1: Error generator enabled

I2C_0 (0x70)*

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_HSM	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	0b0	0b10		–	0b011		
Access Type	–	Write, Read	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_HSM	6	I^2C High-Speed Mode Enable Set this to run I^2C at up to 5Mbps on local side and 3.4Mbps on the remote side.	0b0: I^2C bit rate ≤ 1Mbps 0b1: I^2C bit rate > 1Mbps

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I²C-to-I²C slave setup and hold-time setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C slave. Set this according to the I²C speed mode.	0b00: Set for I²C Fast-mode Plus speed 0b01: Set for I²C Fast-mode speed 0b10: Set for I²C Standard-mode speed 0b11: Reserved
SLV_TO	2:0	I²C-to-I²C slave timeout setting Internal GMSL I²C slave times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x71)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	0b0	0b101			–	0b010		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	I²C-to-I²C master bit-rate setting Configures the I²C bit rate used by the internal I²C master (in the device on the remote side from the external I²C master). Set this according to the I²C speed mode.	0b000: 9.92Kbps - Set for I²C standard-mode speed 0b001: 33.2Kbps - Set for I²C standard-mode speed 0b010: 99.2Kbps - Set for I²C standard- or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast- or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO	2:0	I²C-to-I²C master timeout setting Internal GMSL2 I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

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I2C_2 (0x72)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I^2C address translator source A When I^2C device address matches I^2C SRC_A, internal I^2C master (on remote side) replaces the device address by I^2C DST_A.	0bXXXXXXX: Value of I^2C SRC_A

I2C_3 (0x73)*

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I^2C address translator destination A See the description of I^2C SRC_A.	0bXXXXXXX: Value of I^2C DST_A

I2C_4 (0x74)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I^2C address translator source B When I^2C device address matches I^2C SRC_B, internal I^2C master (on remote side) replaces the device address by I^2C DST_B.	0bXXXXXXX: Value of I^2C SRC_B

I2C_5 (0x75)*

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I²C address translator destination B. See the description of I²C SRC_B.	0bXXXXXXX: Value of I²C DST_B

I2C_6 (0x76)*

BIT	7	6	5	4	3	2	1	0
Field	DIS_REM_CC	–	–	RSVD	I2C_AUTO_CFG	–	I2C_SRC_CNT[1:0]	
Reset	0b0	–	–	0b1	0b1	–	0b00	
Access Type	Write, Read	–	–		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_REM_CC	7	Disables remote control-channel over link	0b0: Remote control channel enabled 0b1: Remote control channel disabled
I2C_AUTO_CFG	3	When this bit is set to 1, splitter mode automatically determines the number of I²C-to-I²C links. In splitter mode, responses from all connected and locked I²C channels are expected, otherwise, a response from a single I²C channel is expected.	0b0: Number of I²C-to-I²C links is set by the I²C SRC_CNT setting 0b1: Lock status automatically determines the number of I²C-to-I²C links
I2C_SRC_CNT	1:0	I²C-to-I²C number of links (valid when I2C_AUTO_CFG = 0) Set this to (N - 1) when expecting I²C response from N remote I²C transmitters. (usually the same as the number of remote devices connected to this device).	0b00: One deserializer connected 0b01: Two deserializers connected 0b10: Reserved 0b11: Reserved

UART_0 (0x78)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		–	–	–	REM_MS_EN
Reset	0b01		0b10		–	–	–	0b0
Access Type	Write, Read				–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	UART Rx source arbitration timeout duration UART Rx processes packets from a single UART source at any time. When UART Rx does not receive any UART packets for this duration, it will select the next UART source according to the source ID of the next following received packet.	0b00: 2 ms 0b01: 8 ms 0b10: 32 ms 0b11: never

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BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN	0	Enables UART bypass-mode control by remote GPIO pin When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, the chip is in bypass mode, otherwise, the chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin

PT_0 (0x79)*

BIT	7	6	5	4	3	2	1	0
Field	PT_I2C_SRC_CNT_2[1:0]		PT_I2C_SRC_CNT_1[1:0]		–	–	CC_2_EN	CC_1_EN
Reset	0b00		0b00		–	–	0b0	0b0
Access Type	Write, Read		Write, Read		–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PT_I2C_SRC_CNT_2	7:6	I^2C-to-I^2C number of links (valid when PT_I2C_AUTO_CFG_2 = 0) Set this to (N - 1) when expecting I^2C response from N remote I^2C transmitters. (usually the same as the number of remote devices connected to this device)	0b00: One deserializer connected 0b01: Two deserializers connected 0b10: Three deserializers connected 0b11: Four deserializers connected
PT_I2C_SRC_CNT_1	5:4	I^2C-to-I^2C number of links (valid when PT_I2C_AUTO_CFG_1 = 0) Set this to (N - 1) when expecting I^2C response from N remote I^2C transmitters. (usually the same as the number of remote devices connected to this device)	0b00: One deserializer connected 0b01: Two deserializers connected 0b10: Three deserializers connected 0b11: Four deserializers connected
CC_2_EN	1	Enable pass-through control Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: Pass-through Channel 2 disabled 0b1: Pass-through Channel 2 enabled
CC_1_EN	0	Enable pass-through control Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: Pass-through Channel 1 disabled 0b1: Pass-through Channel 1 enabled

PT_2 (0x7B)*

BIT	7	6	5	4	3	2	1	0
Field	PT_SRC_1[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
PT_SRC_1	7:1	I^2C address translator source for pass-through I^2C Channel 1 When I^2C device address matches PT_SRC_1, internal I^2C master replaces the device address by PT_DST_1 (0x7C).	0bXXXXXXX: Value of I^2C PT_SRC_1

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PT_3 (0x7C)*

BIT	7	6	5	4	3	2	1	0
Field	PT_DST_1[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
PT_DST_1	7:1	I²C address translator destination for pass-through I²C Channel 1 When I²C device address matches PT_SRC_1 (0x7B), internal I²C master replaces the device address by PT_DST_1.	0bXXXXXXX: Value of I²C PT_DST_1

PT_4 (0x7D)*

BIT	7	6	5	4	3	2	1	0
Field	PT_SRC_2[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
PT_SRC_2	7:1	I²C address translator source for pass-through I²C Channel 2 When I²C device address matches PT_SRC_2, internal I²C master replaces the device address by PT_DST_2 (0x7E).	0bXXXXXXX: Value of I²C PT_SRC_2

PT_5 (0x7E)*

BIT	7	6	5	4	3	2	1	0
Field	PT_DST_2[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
PT_DST_2	7:1	I²C address translator destination for pass-through I²C Channel 2 When I²C device address matches PT_SRC_2 (0x7D), internal I²C master replaces the device address by PT_DST_2.	0bXXXXXXX: Value of I²C PT_DST_2

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CC_0 (0x90)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	EN_I2C_LOOPBACK	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	–	–	0b0	0b0	0b0	0b01		0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_I2C_LOOPBACK	5	Enable I2C loopback between links in G1+G2 or G1+G1 splitter mode. When I2C loopback is enabled, the I2C transactions generated at the leaf-end of on one link are reflected to the leaf-end of the other link	0b0: I2C loopback disabled 0b1: I2C loopback enabled
LOC_MS_EN	4	Enables UART bypass mode control by local MFP pin Set to use MFP24 pin as MS pin (UART mode select). When MS is high, the chip is in bypass mode, otherwise, the chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR	3	Selects whether or not to receive and send parity bit in bypass mode	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO	2:1	UART soft-bypass timeout duration When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power-down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled
BYPASS_EN	0	Enables UART soft-bypass mode Bypass mode remains active as long as there is UART activity. When there is no UART activity for a selected duration (configured by BYPASS_TO bitfield), the device exits bypass mode and the bit is automatically cleared.	0b0: UART soft bypass mode disabled 0b1: UART soft bypass mode enabled

CC_1 (0x91)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	REM_MS_ID[4:0]				
Reset	–	–	–	0b11101				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
REM_MS_ID	4:0	Remote mode select internal GPIO ID

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CC_4 (0x94)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB[7:0]							
Reset	0x96							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB	7:0	UART detected bit length, low 8 bits	0xXX: UART detected bit length, low 8 bits

CC_5 (0x95)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MSB	5:0	UART detected bit length, high 6 bits	0xXX: UART detected bit length, high 6 bits

CC_6 (0x96)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_1	DIS_PAR_1	SLV_SH_PT_1[1:0]		I2CSEL_1	SLV_TO_PT_1[2:0]		
Reset	0b0	0b0	0b10		0b1	0b011		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_1	7	Uses the custom UART bit rate (selected by the BITLEN_PT_1_L—0x304 and BITLEN_PT_1_H—0x305 bitfields) in pass-through UART Channel 1	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_1	6	Disables parity bit in pass-through UART Channel 1	0b0: Parity bit enabled 0b1: Parity bit disabled
SLV_SH_PT_1	5:4	Pass-through I^2C-to-I^2C slave setup and hold time setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I^2C slave. Set this according to the I^2C speed mode.	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C standard-mode speed 0b11: Reserved
I2CSEL_1	3	I^2C/UART mode selection for pass-through Channel 1 (SDA1/RX1, SCL1/TX1) in GMSL2 mode. In GMSL1 mode, Channel 1 pass-through should use the same setting as the main I2CSEL setting.	0b0: UART mode 0b1: I^2C mode

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO_PT_1	2:0	Pass-through I²C-to-I²C slave timeout setting Internal GMSL I²C slave times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

CC_7 (0x97)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_PT_1[2:0]			I2C_HSM_PT_1	MST_TO_PT_1[2:0]		
Reset	0b0	0b101			0b0	0b010		
Access Type		Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT_1	6:4	Pass-through I²C-to-I²C master bit rate setting, configures the I²C bit rate used by the internal I²C master (in the device on the remote side from the external I²C master). Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
I2C_HSM_PT_1	3	Pass-through I²C-to-I²C high-speed mode enabled Set this to run I²C at up to 5Mbps on local side and 3.4Mbps on remote side.	0b0: I²C bit rate ≤ 1Mbps 0b1: I²C bit rate > 1Mbps
MST_TO_PT_1	2:0	Pass-through I²C-to-I²C master timeout setting Internal GMSL I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

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CC_8 (0x98)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	SLV_SH_PT_2[1:0]		I2CSEL_2	SLV_TO_PT_2[2:0]		
Reset	0b0	0b0	0b10		0b1	0b011		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Uses the custom UART bit rate (selected by the BITLEN_PT_2_L—0x306 and BITLEN_PT_2_H—0x307 bitfields) in pass-through UART Channel 1.	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_2	6	Disables parity bit in pass-through UART Channel 2	0b0: Parity bit enabled 0b1: Parity bit disabled
SLV_SH_PT_2	5:4	Pass-through I^2C-to-I^2C slave setup and hold time setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I^2C slave. Set this according to the I^2C speed mode.	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C standard-mode speed 0b11: Reserved
I2CSEL_2	3	I^2C/UART mode selection for pass-through Channel 2 (SDA2/RX2, SCL2/TX2) in GMSL2 mode. In GMSL1 mode, Channel 2 pass-through should use the same setting as the main I2CSEL setting.	0b0: UART 0b1: I^2C
SLV_TO_PT_2	2:0	Pass-through I^2C-to-I^2C slave timeout setting Internal GMSL I^2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

CC_9 (0x99)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_PT_2[2:0]			I2C_HSM_PT_2	MST_TO_PT_2[2:0]		
Reset	0b0	0b101			0b0	0b010		
Access Type		Write, Read			Write, Read	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT_2	6:4	Pass-through I²C-to-I²C master bit-rate setting, configures the I²C bit rate used by the internal I²C master (in the device on the remote side from the external I²C master). Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
I2C_HSM_PT_2	3	Pass-through I²C-to-I²C high-speed mode enable Set this to run I²C at up to 5Mbps on local side and 3.4Mbps on the remote side.	0b0: I²C bit rate ≤ 1Mbps 0b1: I²C bit rate > 1Mbps
MST_TO_PT_2	2:0	Pass-through I²C-to-I²C master timeout setting Internal GMSL I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

CC_10 (0x9A)*

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_OVER_AUX_TO_CC_PINS_EN	–	–	I2C_OVER_AUX_TO_GMSL_CC_EN	PT2_PINS_TO_GMSL_CC_EN	PT1_PINS_TO_GMSL_CC_EN	CC_PINS_TO_GMSL_CC_EN
Reset	–	0b0	–	–	0b0	0b0	0b0	0b1
Access Type	–	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_OVER_AUX_TO_CC_PINS_EN	6	Connects I²C-over-AUX channel to CC pins	0b0: I²C-over-AUX is not connected to CC pins 0b1: I²C-over-AUX is connected to CC pins
I2C_OVER_AUX_TO_GMSL_CC_EN	3	Connects I²C-over-AUX channel to GMSL CC channel	0b0: I²C-over-AUX is not connected to GMSL CC 0b1: I²C-over-AUX is connected to GMSL CC
PT2_PINS_TO_GMSL_CC_EN	2	Connects PT2 pins (SDA2_RX2, SCL2_TX2) to GMSL CC channel	0b0: PT2 pins are not connected to GMSL CC 0b1: PT2 pins are connected to GMSL CC
PT1_PINS_TO_GMSL_CC_EN	1	Connects PT1 pins (SDA1_RX1, SCL1_TX1) to GMSL CC channel	0b0: PT1 pins are not connected to GMSL CC 0b1: PT1 pins are connected to GMSL CC
CC_PINS_TO_GMSL_CC_EN	0	Connects main CC pins (SDA_RX, SCL_TX) to GMSL CC channel	0b0: CC pins are not connected to GMSL CC 0b1: CC pins are connected to GMSL CC

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CC_11 (0x9B)*

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_OVER_AUX_TO_PT1_PINS_EN	–	PT1_LOOPBACK_TO_GMSL_CC_EN	I2C_OVER_AUX_TO_GMSL_PT1_EN	PT2_PINS_TO_GMSL_PT1_EN	PT1_PINS_TO_GMSL_PT1_EN	CC_PINS_TO_GMSL_PT1_EN
Reset	–	0b0	–	0b0	0b0	0b0	0b1	0b0
Access Type	–	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_OVER_AUX_TO_PT1_PINS_EN	6	Connects I^{2}C-over-AUX channel to PT1 pins	0b0: I^{2}C-over-AUX is not connected to PT1 pins 0b1: I^{2}C-over-AUX is connected to PT1 pins
PT1_LOOPBACK_TO_GMSL_CC_EN	4	Loopbacks from PT1 channel to main CC channel	0b0: Loopback disabled 0b1: Loopback enabled
I2C_OVER_AUX_TO_GMSL_PT1_EN	3	Connects I^{2}C-over-AUX channel to GMSL PT1 channel	0b0: I^{2}C-over-AUX is not connected to GMSL PT1 channel 0b1: I^{2}C-over-AUX is connected to GMSL PT1 channel
PT2_PINS_TO_GMSL_PT1_EN	2	Connects PT2 pins (SDA2_RX2, SCL2_TX2) to GMSL PT1 channel	0b0: PT2 pins are not connected to GMSL PT1 channel 0b1: PT2 pins are connected to GMSL PT1 channel
PT1_PINS_TO_GMSL_PT1_EN	1	Connects PT1 pins (SDA1_RX1, SCL1_TX1) to GMSL PT1 channel	0b0: PT1 pins are not connected to GMSL PT1 channel 0b1: PT1 pins are connected to GMSL PT1 channel
CC_PINS_TO_GMSL_PT1_EN	0	Connects main CC pins (SDA_RX, SCL_TX) to GMSL PT1 channel	0b0: CC pins are not connected to GMSL PT1 channel 0b1: CC pins are connected to GMSL PT1 channel

CC_12 (0x9C)*

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_OVER_AUX_TO_PT2_PINS_EN	–	PT2_LOOPBACK_TO_GMSL_CC_EN	I2C_OVER_AUX_TO_GMSL_PT2_EN	PT2_PINS_TO_GMSL_PT2_EN	PT1_PINS_TO_GMSL_PT2_EN	CC_PINS_TO_GMSL_PT2_EN
Reset	–	0b0	–	0b0	0b0	0b1	0b0	0b0
Access Type	–	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_OVER_AUX_TO_PT2_PINS_EN	6	Connects I^{2}C-over-AUX channel to PT2 pins	0b0: I^{2}C-over-AUX is not connected to PT2 pins 0b1: I^{2}C-over-AUX is connected to PT2 pins
PT2_LOOPBACK_TO_GMSL_CC_EN	4	Loopbacks from PT2 channel to main CC channel	0b0: Loopback disabled 0b1: Loopback enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
I2C_OVER_AUX_TO_GMSL_PT2_EN	3	Connects I²C-over-AUX channel to GMSL PT2 channel.	0b0: I²C-over-AUX is not connected to GMSL PT2 channel 0b1: I²C-over-AUX is connected to GMSL PT2 channel
PT2_PINS_TO_GMSL_PT2_EN	2	Connects PT2 pins (SDA2_RX2, SCL2_TX2) to GMSL PT2 channel.	0b0: PT2 pins are not connected to GMSL PT2 channel 0b1: PT2 pins are connected to GMSL PT2 channel
PT1_PINS_TO_GMSL_PT2_EN	1	Connects PT1 pins (SDA1_RX1, SCL1_TX1) to GMSL PT2 channel.	0b0: PT1 pins are not connected to GMSL PT2 channel 0b1: PT1 pins are connected to GMSL PT2 channel
CC_PINS_TO_GMSL_PT2_EN	0	Connects main CC pins (SDA_RX, SCL_TX) to GMSL PT2 channel.	0b0: CC pins are not connected to GMSL PT2 channel 0b1: CC pins are connected to GMSL PT2 channel

CC_13 (0x9D)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AHCC_AUTO_CFG_A	–	–	AHCC_SRC_CNT_A
Reset	–	–	–	–	0b1	–	–	0b0
Access Type	–	–	–	–	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AHCC_AUTO_CFG_A	3	When this bit is set to 1, splitter mode automatically determines the number Auto-HDCP sinks	**Value**: **Decode** 0b0: Number of Auto-HDCP sinks is set by the AHCC_SRC_CNT_A setting 0b1: Splitter Mode status automatically determines the number of Auto-HDCP sinks
AHCC_SRC_CNT_A	0	Auto-HDCP number of sinks (valid when AHCC_AUTO_CFG_A = 0) Set this to (N - 1) when expecting response from N remote Auto_HDCP transmitters	0b00: 1 deserializer connected 0b01: 2 deserializers connected

CC_14 (0x9E)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PT1_READ_EN	–	–	PT_I2C_AUTO_CFG_2	PT_I2C_AUTO_CFG_1
Reset	–	–	–	0b0	–	–	0b1	0b1
Access Type	–	–	–	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_READ_EN	4	Enable register read back with PT1 channel	
PT_I2C_AUTO_CFG_2	1	When set to 1, I²C-to-I²C number of links is determined automatically.	0b0: Number of PT2 I²C-to-I²C links is set by the PT_I2C_SRC_CNT_2 setting 0b1: Automatically determines the number of I²C-to-I²C links

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BITFIELD	BITS	DESCRIPTION	DECODE
PT_I2C_AUTO_CFG_1	0	When set to 1, I²C-to-I²C number of links is determined automatically.	0b0: Number of PT1 I²C-to-I²C links is set by the PT_I2C_SRC_CNT_1 setting 0b1: Automatically determines the number of I²C-to-I²C links

TX0 (0xA0, 0xA4)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Access Type	Write, Read	–			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Transmits CRC Enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TX1 (0xA1, 0xA5)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TX3 (0xA3, 0xA7)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	–	TX_STR_SEL[1:0]	
Access Type	–	–	Write, Read	Write, Read	–	–	Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In splitter mode: When 0, packets from this port are NOT transmitted from Port B, otherwise packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in splitter mode 0b1: Packets are transmitted over GMSLB in splitter mode
TX_SPLT_MASK_A	4	In splitter mode: When 0, packets from this port are NOT transmitted from Port A, otherwise packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in splitter mode 0b1: Packets are transmitted over GMSLA in splitter mode
TX_STR_SEL	1:0	Stream ID used in packets transmitted from this channel	0bXX: Stream ID for packets from this channel

TR0 (0xB0, 0xB8, 0xC8)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RSVD	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0xB1, 0xB9, 0xC9)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

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TR3 (0xB3, 0xBB, 0xCB)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In splitter mode: When 0, packets from this port are NOT transmitted from Port B, otherwise packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in splitter mode 0b1: Packets are transmitted over GMSLB in splitter mode
TX_SPLT_MASK_A	4	In splitter mode: When 0, packets from this port are NOT transmitted from Port A, otherwise packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in splitter mode 0b1: Packets are transmitted over GMSLA in splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel Default value is set by CFG0 at power-up.	0bXXX: Source ID for packets from this channel

ARQ0 (0xB5, 0xBD, 0xCD)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN
Access Type					–		–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN	0	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0xB6, 0xBE, 0xCE)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmission limit ARQ stops retransmitting after this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xB7, 0xBF, 0xCF)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmitting limit (MAX_RT) for one packet in this channel on Link A	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel on Link A	0bXX: Count of retransmissions for this channel

TR0 (0xC0)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

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TR1 (0xC1)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0xC3)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel Default value is set by CFG0 at power-up.	0bXXX: Source ID for packets from this channel

TR4 (0xC4)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from the selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: Block all packets 0x01: Receive packets from source ID 0 0x02: Receive packets from source ID 1 0x03: Receive packets from source IDs 0 and 1 . . 0xFF: Receive packets from all source IDs

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TR0 (0xD0, 0xD8, 0xE0, 0xE8, 0xF0)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0xD1, 0xD9, 0xE1, 0xE9, 0xF1)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0xD3, 0xDB, 0xE3, 0xEB, 0xF3)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In splitter mode: When 0, packets from this port are NOT transmitted from Port B, otherwise packets are transmitted from Port B.	0b0: Packets are not transmitted over GMSLB in splitter mode 0b1: Packets are transmitted over GMSLB in splitter mode
TX_SPLT_MASK_A	4	In splitter mode: When 0, packets from this port are NOT transmitted from Port A, otherwise packets are transmitted from Port A.	0b0: Packets are not transmitted over GMSLA in splitter mode 0b1: Packets are transmitted over GMSLA in splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel Default value is set by CFG0 at power-up.	0bXXX: Source ID for packets from this channel

TR4 (0xD4, 0xDC, 0xE4, 0xEC, 0xF4)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from the selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: Block all packets 0x01: Receive packets from source ID 0 0x02: Receive packets from source ID 1 0x03: Receive packets from source IDs 0 and 1 . . 0xFF: Receive packets from all source IDs

ARQ0 (0xD5, 0xDD, 0xE5, 0xED, 0xF5)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	–	RSVD	–	ARQ_EN_A
Access Type					–		–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN_A	0	Enables ARQ on Link A	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0xD6, 0xDE, 0xE6, 0xEE, 0xF6)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmission limit ARQ stops retransmitting after this many times for a single packet.	0bXXX: Maximum retransmit limit

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xD7, 0xDF, 0xE7, 0xEF, 0xF7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_A	RT_CNT_A[6:0]						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_A	7	Reached maximum retransmitting limit (MAX_RT) for one packet in this channel on Link A	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_A	6:0	Total retransmission count in this channel on Link A	0xXX: Count of retransmissions for this channel

VIDEO_TX0 (0x100, 0x110)*

BIT	7	6	5	4	3	2	1	0
Field	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	–	–	VID_TX_EN
Reset	0b0	0b1	0b10		–	–	–	0b1
Access Type	Write, Read	Write, Read	Write, Read		–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_SEL	7	Line-CRC checksum generation with DE or HS	0b0: Use DE for line CRC 0b1: Use HS for line CRC
LINE_CRC_EN	6	Line-CRC Enable Generates a CRC code for the video line and send it to the receiver side for comparison	0b0: Line CRC disabled 0b1: Line CRC enabled
ENC_MODE	5:4	HS, VS, and DE encoding mode	0b00: HS, VS, and DE encoding off 0b01: HS, VS, and DE encoding on, color bits always sent 0b10: HS, VS, and DE encoding on, color bits sent only when DE is high 0b11: HS, VS, and DE encoding on, color bits sent only when HS is high
VID_TX_EN	0	Video transmit enable for this video port	0b0: Video transmit port disabled 0b1: Video transmit port enabled

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VIDEO_TX2 (0x102, 0x112)*

BIT	7	6	5	4	3	2	1	0
Field	PCLKDET_A	DRIFT_ERR_A	OVERFLOW_A	FIFO_WARN_A	RSVD	LIM_HEART	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b1	0b0
Access Type	Read Only	Read Clears All	Read Clears All	Read Clears All		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PCLKDET_A	7	PCLK detected	0b0: Video transmit PCLK not detected 0b1: Video transmit PCLK detected
DRIFT_ERR_A	6	VID_TX PCLK drift error detected After the video pipeline starts, PCLK cannot drift more than a certain amount without restarting the subsystem.	0b0: Video transmit PCLK drift error not detected 0b1: Video transmit PCLK drift error detected
OVERFLOW_A	5	VID_TX FIFO has overflowed Video input throughput may be too high, bandwidth allocation on GMSL link for video may not be enough.	0b0: Video transmit FIFO has not overflowed 0b1: Video transmit FIFO has overflowed
FIFO_WARN_A	4	VID_TX FIFO is more than half full	0b0: Video transmit FIFO is less than or equal to half full 0b1: Video transmit FIFO is more than half full
LIM_HEART	2	Disables heartbeat during blanking Use together with SEQ_MISS_EN and DIS_PKT_DET registers in deserializer.	0b0: Heartbeat enabled during blanking 0b1: Hearbeat disabled during blanking

VIDEO_TX6 (0x106, 0x116)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MASK_VIDEO_DE	RSVD[5:0]					
Reset	0b0	0b0	0b000000					
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION
MASK_VIDEO_DE	6	Mask video with DE

AUDIO_TX0 (0x140)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	INV_SCK	INV_WS	FORCE_AUD	–
Reset	–	–	–	–	0b0	0b0	0b0	–
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	–

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BITFIELD	BITS	DESCRIPTION	DECODE
INV_SCK	3	Invert SCK (when using local I^{2}S interface)	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS	2	Invert WS (when using local I^{2}S interface). This inverts the edge on which an audio sample frame is defined and captured.	0b0: Low/High WS pulse marks sample 0b1: High/Low WS pulse marks sample
FORCE_AUD	1	Forces audio data to zero	0b0: Normal audio data 0b1: Audio data forced to zero

AUDIO_TX1 (0x141)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	–	AUD_HDCP_SEL
Reset	0b01		0b00		0b1	0b1	–	0b0
Access Type			Write, Read		Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_STR_TX	5:4	Audio stream ID	0b00: Use stream ID 0 0b01: Use stream ID 1 0b10: Use stream ID 2 0b11: Use stream ID 3
AUD_DRIFT_DET_EN	3	Enable audio clock drift detection Resets subsystem on SCK frequency drift and reports it.	0b0: Audio clock drift detection disabled 0b1: Audio clock drift detection enabled
AUD_INF_PER	2	Audio periodic info frame transmission enable	0b0: Audio periodic info frame transmission disabled 0b1: Audio periodic info frame transmission enabled
AUD_HDCP_SEL	0	Select the HDCP encryption engine that encrypts this audio channel	0b0: HDCP_X 0b1: HDCP_Y

AUDIO_TX5 (0x145)

BIT	7	6	5	4	3	2	1	0
Field	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_DRIFT_ERR	7	Audio clock frequency drift detected	0b0: Audio clock frequency drift not detected 0b1: Audio clock frequency drift detected
AUD_FIFO_WARN	6	Audio FIFO is more than half full	0b0: Audio FIFO is less than or equal to half full 0b1: Audio FIFO is more than half full
AUD_OVERFLOW	5	Audio buffer overflow detected	0b0: Audio buffer overflow not detected 0b1: Audio buffer overflow detected
ACLKDET	4	Audio clock detected	0b0: Audio clock not detected 0b1: Audio clock detected

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AUDIO_TX7 (0x147)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_SEL	7	Audio PRBS clock selection, set to 0 in sink-sourced mode	0b0: SCK selected 0b1: Internal oscillator clock selected (150MHz)
PRBSEN_AUD	6	Audio PRBS enable	0b0: Audio PRBS disabled 0b1: Audio PRBS enabled

AUDIO_TX8 (0x148)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
Reset	0b0	0b1	0b000000					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_WS_LEN	7	Selects the length of the generated WS pulse	0b0: 256 data bits per WS cycle 0b1: 32 data bits per WS cycle
PRBS_WS_GEN	6	Audio PRBS WS generation enable	0b0: Audio PRBS WS generation disabled 0b1: Audio PRBS WS generation enabled

AUDIO_TX0 (0x150)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	INV_SCK	INV_WS	FORCE_AUD	–
Reset	–	–	–	–	0b0	0b0	0b0	–
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
INV_SCK	3	Invert SCK (when using local I^2S interface)	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS	2	Invert WS (when using local I^2S interface) This inverts the edge on which an audio sample frame is defined and captured.	0b0: Low/High WS pulse marks sample 0b1: High/Low WS pulse marks sample
FORCE_AUD	1	Forces audio data to zero	0b0: Normal audio data 0b1: Audio data forced to zero

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AUDIO_TX1 (0x151)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	–	AUD_HDCP_SEL
Reset	0b01		0b01		0b1	0b1	–	0b0
Access Type			Write, Read		Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_STR_TX	5:4	Audio stream ID	0b00: Use stream ID 0 0b01: Use stream ID 1 0b10: Use stream ID 2 0b11: Use stream ID 3
AUD_DRIFT_DET_EN	3	Enable audio clock drift detection Resets subsystem on SCK frequency drift and reports it.	0b0: Audio clock drift detection disabled 0b1: Audio clock drift detection enabled
AUD_INF_PER	2	Audio periodic info frame transmission enable	0b0: Audio periodic info frame transmission disabled 0b1: Audio periodic info frame transmission enabled
AUD_HDCP_SEL	0	Select the HDCP encryption engine that encrypts this audio channel	0b0: HDCP_X 0b1: HDCP_Y

AUDIO_TX5 (0x155)

BIT	7	6	5	4	3	2	1	0
Field	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_DRIFT_ERR	7	Audio clock frequency drift detected	0b0: Audio clock frequency drift not detected 0b1: Audio clock frequency drift detected
AUD_FIFO_WARN	6	Audio FIFO is more than half full	0b0: Audio FIFO is less than or equal to half full 0b1: Audio FIFO is more than half full
AUD_OVERFLOW	5	Audio buffer overflow detected	0b0: Audio buffer overflow not detected 0b1: Audio buffer overflow detected
ACLKDET	4	Audio clock detected	0b0: Audio clock not detected 0b1: Audio clock detected

AUDIO_TX7 (0x157)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read						

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BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_SEL	7	Audio PRBS clock selection, set to 0 in sink-sourced mode	0b0: SCK selected 0b1: Internal oscillator clock selected (150MHz)
PRBSEN_AUD	6	Audio PRBS enable	0b0: Audio PRBS disabled 0b1: Audio PRBS enabled

AUDIO_TX8 (0x158)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
Reset	0b0	0b1	0b000000					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_WS_LEN	7	Selects the length of the generated WS pulse	0b0: 256 data bits per WS cycle 0b1: 32 data bits per WS cycle
PRBS_WS_GEN	6	Audio PRBS WS generation enable	0b0: Audio PRBS WS generation disabled 0b1: Audio PRBS WS generation enabled

SPI_0 (0x1A0)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0b00		0b00		0b1	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Programs to local ID if filtering packets based on header ID	0b00: ID = 0 0b01: ID = 1
SPI_CC_TRG_ID	5:4	ID for GMSL header in SPI control-channel bridge mode	0b00: ID = 0 0b01: ID = 1
SPI_IGNR_ID	3	Selects whether SPI should use or ignore header ID to decide on packet acceptance	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_CC_EN	2	Enables control-channel SPI bridge function	0b0: SPI bridge disabled 0b1: SPI bridge enabled
MST_SLVN	1	Selects whether SPI is master or slave	0b0: SPI slave 0b1: SPI master
SPI_EN	0	Enable SPI channel	0b0: SPI channel disabled 0b1: SPI channel enabled

SPI_1 (0x1A1)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
Reset	0b000111						0b01	
Access Type	Write, Read						Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Sets the packet size ((2N + 1) bytes) for GMSL SPI packet If this is programmed to a value greater than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes . . 0b111111: Packet size is 127 bytes
SPI_BASE_PRIO	1:0	Starting GMSL2 Request Priority, will advance by 1 (if room) if Tx Buffer is over half full.	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 0

SPI_2 (0x1A2)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0b000			0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Hold off GMSL2 request until this number of extra bytes are received on SPI port.	0b00: No extra bytes 0b01: 1 extra byte 0b10: 2 extra bytes 0b11: 3 extra bytes
FULL_SCK_SETUP	4	Sample MISO after half or full SCK period	0b0: MISO sampled after half SCK period 0b1: MISO sampled after full SCK period
SPI_MOD3_F	3	Allows the suppression of an extra SCK prior to SS deassertion when SPI mode 3 is selected.	0b0: Extra SCK present prior to SS deassertion when in SPI mode 3 0b1: Extra SCK suppressed prior to SS deassertion when in SPI mode 3
SPI_MOD3	2	Selects SPI mode 0 or 3	0b0: SPI mode 0 0b1: SPI mode 3
SPIM_SS2_ACT_H	1	Sets the polarity for SS2 when the SPI is a master.	0b0: Slave select 2 is active low 0b1: Slave select 2 is active high
SPIM_SS1_ACT_H	0	Sets the polarity for SS1 when the SPI is a master	0b0: Slave select 1 is active low 0b1: Slave select 1 is active high

SPI_3 (0x1A3)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between: 1. Assertion of SS and start of SCK pulses 2. End of SCK pulses and deassertion of SS 3. Deassertion of SS and reassertion of SS (if necessary)	0xXX: Number of clock delays

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SPI_4 (0x1A4)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time	0xXX: Number of clocks for SCK low time

SPI_5 (0x1A5)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time	0xXX: Number of clocks for SCK high time

SPI_6 (0x1A6)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0b0	0b0	0b0	0b0	0b1	0b1
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	Alternate GPU status register to use for BNE status if GPIO is not available	0b0: Buffer empty 0b1: Buffer not empty
SPIS_RWN	4	Alternate GPU control register to use for Read/Write control if GPIO is not available	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enable GPIO for use as Slave Select 2 output	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
SS_IO_EN_1	2	Enable GPIO for use as Slave Select 1 output	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
BNE_IO_EN	1	Enable GPIO for use as BNE output for SPI data available status	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function
RWN_IO_EN	0	Enable GPIO for use as RO input for control of SPI data movement	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function

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SPI_7 (0x1A7)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
Reset	0b0	0b0	–	0b00000				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	SPI Rx buffer overflow flag	0b0: No SPI Rx buffer overflow 0b1: SPI Rx buffer overflow
SPI_TX_OVRFLW	6	SPI Tx buffer overflow flag	0b0: No SPI Tx buffer overflow 0b1: SPI Tx buffer overflow
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer	0bXXXXX: Number of bytes available

SPI_8 (0x1A8)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100ns increments) for GMSL2 request hold off. 0x00: Disabled	0xXX: Number of 100nS delay increments for GMSL2 request hold off

WM_0 (0x1C0)*

BIT	7	6	5	4	3	2	1	0
Field	WM_AUTO_SYNC_EN_X	WM_MODE_X[2:0]			–	–	–	WM_EN_X
Reset	0b1	0b000			–	–	–	0b0
Access Type	Write, Read	Write, Read			–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_AUTO_SYNC_EN_X	7	Auto-sync polarity detection (only effective for watermark block)	0b0: Disabled 0x1: Enabled
WM_MODE_X	6:4	Watermark Mode	0b000: Default generator mode − cycle through all four watermarks in video stream (default). 0b001: Error generator mode − cycle through only two watermarks to replicate a stuck frame. 0b110: Reserved 0b111: Reserved
WM_EN_X	0	Watermark Enable	0b0: Watermarking disabled 0b1: Watermarking enabled

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WM_1 (0x1C1)*

BIT	7	6	5	4	3	2	1	0
Field	WM_HSPOL_X	WM_VSPOL_X	RSVD[1:0]		RSVD[3:0]			
Reset	0b0	0b0	0b01		0x9			
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
WM_HSPOL_X	7	HS Polarity (only effective for watermark block)	0b0: Noninverting 0b1: Invert
WM_VSPOL_X	6	VS Polarity (only effective for watermark block)	0b0: Noninverting 0b1: Invert

WM_2 (0x1C2)*

BIT	7	6	5	4	3	2	1	0
Field	WM_AUTO_SYNC_EN_Y	WM_MODE_Y[2:0]			–	–	–	WM_EN_Y
Reset	0b1	0b000			–	–	–	0b0
Access Type	Write, Read	Write, Read			–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_AUTO_SYNC_EN_Y	7	Auto-sync polarity detection (only effective for watermark block)	0b0: Disabled 0b1: Enabled
WM_MODE_Y	6:4	Watermark Mode	0b000: Default generator mode − cycle through all four watermarks in video stream (default). 0b001: Error generator mode − cycle through only two watermarks to replicate a stuck frame. 0b110: Reserved 0b111: Reserved
WM_EN_Y	0	Watermark Enable	0b0: Watermarking disabled 0b1: Watermarking enabled

WM_3 (0x1C3)*

BIT	7	6	5	4	3	2	1	0
Field	WM_HSPOL_Y	WM_VSPOL_Y	WM_KO_Y[1:0]		WM_NO_Y[3:0]			
Reset	0b0	0b0	0b01		0x9			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
WM_HSPOL_Y	7	HS Polarity (only effective for watermark block)	0b0: Noninverting 0b1: Invert
WM_VSPOL_Y	6	VS Polarity (only effective for watermark block)	0b0: Noninverting 0b1: Invert
WM_KO_Y	5:4	Watermark Gain	

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BITFIELD	BITS	DESCRIPTION	DECODE
WM_NO_Y	3:0	Watermark oversample rate (0 = 1x,1 = 2x, 2 = 3...)	

WM_WREN_0 (0x1DE)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_L	7:0	Writes 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.	0xBA: Enables writing to WM registers Others: WM registers remain read-only

WM_WREN_1 (0x1DF)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_H	7:0	Writes 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.	0xDC: Enables writing to WM registers Others: WM registers remain read-only

GPIO_A (0x200, 0x208, 0x2A8, 0x2B0, 0x2B8, 0x2C0, 0x2C8)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drives value when GPIO_OUT_DIS = 0, GPIO_RX_EN_A = 0, and GPIO_RX_EN_B = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x201, 0x209, 0x2A9, 0x2B1, 0x2B9, 0x2C1, 0x2C9)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffers pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x202, 0x20A, 0x2AA, 0x2B2, 0x2BA, 0x2C2, 0x2CA)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when the pin is configured as non-GPIO. When cleared, the non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
IO_EDGE_RATE	6:5	Selects IO output edge rate	0b00: 1ns 0b01: 2ns 0b10: 4ns 0b11: 8ns
GPIO_RX_ID	4:0	First GPIO ID to receive and output at this pin Combined with other received GPIO IDs using GPIO_OUT_LGC.	0bXXXXX: GPIO ID to receive

GPIO_D (0x203, 0x20B, 0x2AB, 0x2B3, 0x2BB, 0x2C3, 0x2CB)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
Access Type	–	–	Write, Read	Write, Read	–	–	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IO_RX_EN	5	Enables IO receiver	0b0: Disable 0b1: Enable
GPIO_OUT_LGC	4	When pin is used as GPIO, selects GPIO output drive logic function	0b0: AND the GPIO values received from both links 0b1: OR the GPIO values received from both links
GPIO_RX_EN_A	1	Enable receiving first GPIO ID (GPIO_RX_ID) at this pin from Link A	0b0: First GPIO ID disabled for reception 0b1: First GPIO ID enabled for reception
GPIO_TX_EN_A	0	Transmits GPIO to remote side on Link A	0b0: This GPIO source disabled for transmission 0b1: This GPIO source enabled for transmission

GPIO_E (0x204, 0x20C, 0x2AC, 0x2B4, 0x2BC, 0x2C4, 0x2CC)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN2_A	5	Enable receiving second GPIO ID (GPIO_RX_ID2) at this pin from Link A	0b0: Second GPIO ID disabled for reception 0b1: Second GPIO ID enabled for reception
GPIO_RX_ID2	4:0	Second GPIO ID to receive and output at this pin Combined with other received GPIO IDs using GPIO_OUT_LGC.	0bXXXXX: GPIO ID to receive

GPIO_F (0x205, 0x20D, 0x2AD, 0x2B5, 0x2BD, 0x2C5, 0x2CD)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN3_A	5	Enable receiving third GPIO ID (GPIO_RX_ID3) at this pin from Link A	0b0: Third GPIO ID disabled for reception 0b1: Third GPIO ID enabled for reception
GPIO_RX_ID3	4:0	Third GPIO ID to receive and output at this pin Combined with other received GPIO IDs using GPIO_OUT_LGC.	0bXXXXX: GPIO ID to receive

GPIO_G (0x206, 0x20E, 0x2AE, 0x2B6, 0x2BE, 0x2C6, 0x2CE)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
Access Type	–	–	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN4_A	5	Enable receiving fourth GPIO ID (GPIO_RX_ID4) at this pin from Link A	0b0: Fourth GPIO ID disabled for reception 0b1: Fourth GPIO ID enabled for reception
GPIO_RX_ID4	4:0	Fourth GPIO ID to receive and output at this pin Combined with other received GPIO IDs using GPIO_OUT_LGC.	0bXXXXX: GPIO ID to receive

GPIO_A (0x210, 0x218, 0x220, 0x228, 0x230, 0x238, 0x240, 0x248, 0x250, 0x258, 0x260, 0x268, 0x270, 0x278, 0x280, 0x288, 0x290, 0x298, 0x2A0)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	–	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
Access Type	Write, Read	–	Write, Read	Write, Read	Read Only	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drives value when GPIO_OUT_DIS = 0, GPIO_RX_EN_A = 0, and GPIO_RX_EN_B = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x211, 0x219, 0x221, 0x229, 0x231, 0x239, 0x241, 0x249, 0x251, 0x259, 0x261, 0x269, 0x271, 0x279, 0x281, 0x289, 0x291, 0x299, 0x2A1)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffers pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

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GPIO_C (0x212, 0x21A, 0x222, 0x22A, 0x232, 0x23A, 0x242, 0x24A, 0x252, 0x25A, 0x262, 0x26A, 0x272, 0x27A, 0x282, 0x28A, 0x292, 0x29A, 0x2A2)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when the pin is configured as non-GPIO. When cleared, the non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
IO_EDGE_RATE	6:5	Selects IO output edge rate	0b00: 1ns 0b01: 2ns 0b10: 4ns 0b11: 8ns
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_D (0x213, 0x21B, 0x223, 0x22B, 0x233, 0x23B, 0x243, 0x24B, 0x253, 0x25B, 0x263, 0x26B, 0x273, 0x27B, 0x283, 0x28B, 0x293, 0x29B, 0x2A3)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	–	–	GPIO_RX_EN_A	GPIO_TX_EN_A
Access Type	–	–	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IO_RX_EN	5	Enables IO receiver	0b0: Disable 0b1: Enable
GPIO_OUT_LGC	4	When pin is used as GPIO, selects GPIO output drive logic function.	0b0: AND the GPIO values received from both links 0b1: OR the GPIO values received from both links
GPIO_RX_EN_A	1	Receives GPIO from Link A	0b0: This GPIO source disabled for reception 0b1: This GPIO source enabled for reception
GPIO_TX_EN_A	0	Transmits GPIO to remote side on Link A	0b0: This GPIO source disabled for transmission 0b1: This GPIO source enabled for transmission

GPIO_RX_0 (0x2F8)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_A_7	GPIO_RECVED_A_6	GPIO_RECVED_A_5	GPIO_RECVED_A_4	GPIO_RECVED_A_3	GPIO_RECVED_A_2	GPIO_RECVED_A_1	GPIO_RECVED_A_0
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_7	7	Received GPIO value

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BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_6	6	Received GPIO value
GPIO_RECVED_A_5	5	Received GPIO value
GPIO_RECVED_A_4	4	Received GPIO value
GPIO_RECVED_A_3	3	Received GPIO value
GPIO_RECVED_A_2	2	Received GPIO value
GPIO_RECVED_A_1	1	Received GPIO value
GPIO_RECVED_A_0	0	Received GPIO value

GPIO_RX_1 (0x2F9)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_A_15	GPIO_RECVED_A_14	GPIO_RECVED_A_13	GPIO_RECVED_A_12	GPIO_RECVED_A_11	GPIO_RECVED_A_10	GPIO_RECVED_A_9	GPIO_RECVED_A_8
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_15	7	Received GPIO value
GPIO_RECVED_A_14	6	Received GPIO value
GPIO_RECVED_A_13	5	Received GPIO value
GPIO_RECVED_A_12	4	Received GPIO value
GPIO_RECVED_A_11	3	Received GPIO value
GPIO_RECVED_A_10	2	Received GPIO value
GPIO_RECVED_A_9	1	Received GPIO value
GPIO_RECVED_A_8	0	Received GPIO value

GPIO_RX_2 (0x2FA)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_A_23	GPIO_RECVED_A_22	GPIO_RECVED_A_21	GPIO_RECVED_A_20	GPIO_RECVED_A_19	GPIO_RECVED_A_18	GPIO_RECVED_A_17	GPIO_RECVED_A_16
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_23	7	Received GPIO value
GPIO_RECVED_A_22	6	Received GPIO value
GPIO_RECVED_A_21	5	Received GPIO value
GPIO_RECVED_A_20	4	Received GPIO value
GPIO_RECVED_A_19	3	Received GPIO value
GPIO_RECVED_A_18	2	Received GPIO value
GPIO_RECVED_A_17	1	Received GPIO value
GPIO_RECVED_A_16	0	Received GPIO value

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GPIO_RX_3 (0x2FB)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_A_31	GPIO_RECVED_A_30	GPIO_RECVED_A_29	GPIO_RECVED_A_28	GPIO_RECVED_A_27	GPIO_RECVED_A_26	GPIO_RECVED_A_25	GPIO_RECVED_A_24
Reset	0b1	0b1	0b0	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_31	7	Received GPIO value
GPIO_RECVED_A_30	6	Received GPIO value
GPIO_RECVED_A_29	5	Received GPIO value
GPIO_RECVED_A_28	4	Received GPIO value
GPIO_RECVED_A_27	3	Received GPIO value
GPIO_RECVED_A_26	2	Received GPIO value
GPIO_RECVED_A_25	1	Received GPIO value
GPIO_RECVED_A_24	0	Received GPIO value

UART_PT_0 (0x304)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_1_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_L	7:0	Low byte of custom UART bit length for pass-through UART Channel 1 Set this register to the UART bit length divided by 6.666ns (LSB 8 bits). Set BITLEN_MAN_CFG_1 (0x96) to 1 to use this value.	0xXX: Low byte of custom UART bit length for pass-through UART Channel 1

UART_PT_1 (0x305)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_1_H[5:0]					
Reset	–	–	0b000101					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_H	5:0	High byte of custom UART bit length for pass-through UART Channel 1. Set this register to the UART bit length divided by 6.666ns (LSB 8 bits). Set BITLEN_MAN_CFG_1 (0x96) to 1 to use this value.	0bXXXXXX: High byte of custom UART bit length for pass-through UART Channel 1

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UART_PT_2 (0x306)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_2_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_L	7:0	Low byte of custom UART bit length for pass-through UART Channel 2. Set this register to the UART bit length divided by 6.666ns (LSB 8 bits). Set BITLEN_MAN_CFG_2 (0x98) to 2 to use this value.	0xXX: Low byte of custom UART bit length for pass-through UART Channel 2

UART_PT_3 (0x307)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_2_H[5:0]					
Reset	–	–	0b000101					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_H	5:0	High byte of custom UART bit length for pass-through UART Channel 1. et this register to the UART bit length divided by 6.666ns (LSB 8 bits). Set BITLEN_MAN_CFG_2 (0x98) to 2 to use this value.	0bXXXXXX: High byte of custom UART bit length for pass-through UART Channel 2

MISC_2 (0x312)

BIT	7	6	5	4	3	2	1	0
Field	VDDIO_OV	VDD1P8_OV	VREG_OV	VDD_OV	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Read Only	Read Only	Read Only	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDIO_OV	7	Live V_{DDIO} overvoltage status V_{TRIP_0V} level set by OVDDIO_LEVEL in register MISC_8.	0b0: Overvoltage not detected 0b1: Overvoltage detected
VDD1P8_OV	6	Live V_{DD18} overvoltage status V_{TRIP_ov} level set by OV1P8_LEVEL in register MISC_1.	0b0: Overvoltage not detected 0b1: Overvoltage detected

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BITFIELD	BITS	DESCRIPTION	DECODE
VREG_OV	5	Live V_{REG} overvoltage status V_{TRIP_0V} level set by OVREG_LEVEL in register MISC_1.	0b0: Overvoltage not detected 0b1: Overvoltage detected
VDD_OV	4	Live V_{DD_sw} overvoltage status V_{TRIP_OV} set by OV_LEVEL in register MISC_0.	0b0: Overvoltage not detected 0b1: Overvoltage detected

MISC_3 (0x313)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LFLT_STKY_INT
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_STKY_INT	0	Selects if the line-fault interrupt should be sticky or live	0b0: Live 0b1: Sticky

CROSS_0 (0x400, 0x500)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0b0	0b0	0b00000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS0_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0.	0bXXXXX: Incoming bit position

CROSS_1 (0x401, 0x501)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0b0	0b0	0b00001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS1_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1.	0bXXXXX: Incoming bit position

CROSS_2 (0x402, 0x502)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0b0	0b0	0b00010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS2_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS2_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2.	0bXXXXX: Incoming bit position

CROSS_3 (0x403, 0x503)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0b0	0b0	0b00011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS3_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3.	0bXXXXX: Incoming bit position

CROSS_4 (0x404, 0x504)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0b0	0b0	0b00100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS4_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4.	0bXXXXX: Incoming bit position

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CROSS_5 (0x405, 0x505)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0b0	0b0	0b00101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS5_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS5_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5.	0bXXXXX: Incoming bit position

CROSS_6 (0x406, 0x506)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0b0	0b0	0b00110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS6_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS6_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6.	0bXXXXX: Incoming bit position

CROSS_7 (0x407, 0x507)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0b0	0b0	0b00111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS7_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7.	0bXXXXX: Incoming bit position

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CROSS_8 (0x408, 0x508)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0b0	0b0	0b01000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS8_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS8_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8.	0bXXXXX: Incoming bit position

CROSS_9 (0x409, 0x509)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0b0	0b0	0b01001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS9_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS9_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9.	0bXXXXX: Incoming bit position

CROSS_10 (0x40A, 0x50A)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0b0	0b0	0b01010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS10_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10.	0bXXXXX: Incoming bit position

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CROSS_11 (0x40B, 0x50B)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0b0	0b0	0b01011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS11_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS11_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11.	0bXXXXX: Incoming bit position

CROSS_12 (0x40C, 0x50C)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0b0	0b0	0b01100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS12_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS12_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12.	0bXXXXX: Incoming bit position

CROSS_13 (0x40D, 0x50D)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0b0	0b0	0b01101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS13_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13.	0bXXXXX: Incoming bit position

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CROSS_14 (0x40E, 0x50E)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0b0	0b0	0b01110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14.	0bXXXXX: Incoming bit position

CROSS_15 (0x40F, 0x50F)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0b0	0b0	0b01111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15.	0bXXXXX: Incoming bit position

CROSS_16 (0x410, 0x510)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0b0	0b0	0b10000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS16_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16.	0bXXXXX: Incoming bit position

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CROSS_17 (0x411, 0x511)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0b0	0b0	0b10001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17.	0bXXXXX: Incoming bit position

CROSS_18 (0x412, 0x512)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0b0	0b0	0b10010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS18_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18.	0bXXXXX: Incoming bit position

CROSS_19 (0x413, 0x513)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0b0	0b0	0b10011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19.	0bXXXXX: Incoming bit position

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CROSS_20 (0x414, 0x514)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0b0	0b0	0b10100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20.	0bXXXXX: Incoming bit position

CROSS_21 (0x415, 0x515)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0b0	0b0	0b10101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21.	0bXXXXX: Incoming bit position

CROSS_22 (0x416, 0x516)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0b0	0b0	0b10110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS22_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22.	0bXXXXX: Incoming bit position

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CROSS_23 (0x417, 0x517)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0b0	0b0	0b10111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS23_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS23_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23.	0bXXXXX: Incoming bit position

HS_VS (0x41F, 0x51F)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET	VS_DET	HS_DET	–	–	VS_POL	HS_POL
Reset	–	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET	6	DE activity is detected	0b0: DE is not detected 0b1: DE is detected
VS_DET	5	VS activity is detected	0b0: VS is not detected 0b1: VS is detected
HS_DET	4	HS activity is detected	0b0: HS is not detected 0b1: HS is detected
VS_POL	1	Detected VS polarity	0b0: VS is high when DE = 1 0b1: VS is low when DE = 1
HS_POL	0	Detected HS polarity	0b0: Active low 0b1: Active high

VTX0 (0x420, 0x520)

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VID_ACTIVE	PCLKDET_VTX	VS_TRIG	VTG_MODE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b1	0b11	
Access Type	Write, Read	Write, Read	Write, Read	Read Only	Read Only	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_VS	7	Enable to generate VS output according to the timing definition	0b0: Do not generate VS 0b1: Generate VS
GEN_HS	6	Enable to generate HS output according to the timing definition	0b0: Do not generate HS 0b1: Generate HS

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BITFIELD	BITS	DESCRIPTION	DECODE
GEN_DE	5	Enable to generate DE output according to the timing definition	0b0: Do not generate DE 0b1: Generate DE
VID_ACTIVE	4	Video active indicator	0b0: Video input is in reset 0b1: Video input is active
PCLKDET_VTX	3	PCLK detected	0b0: PCLK not detected 0b1: PCLK detected
VS_TRIG	2	Selects VS trigger edge	0b0: Falling edge 0b1: Rising edge
VTG_MODE	1:0	Video timing generator mode	0b00: VS tracking mode 0b01: VS on trigger mode 0b10: Auto repeat mode 0b11: Free running mode

VTX1 (0x421, 0x521)*

BIT	7	6	5	4	3	2	1	0
Field	USE_DE_AS_HS	USE_HS_AS_DE	FORCE_VS_LOW	FORCE_HS_LOW	FORCE_DE_LOW	VS_INVERT	HS_INVERT	DE_INVERT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
USE_DE_AS_HS	7	Replace HS with DE	0b0: HS is unchanged 0b1: Use DE as HS
USE_HS_AS_DE	6	Replace DE with HS	0b0: DE is unchanged 0b1: Use HS as DE
FORCE_VS_LOW	5	Force VS Low (before optional inversion)	0b0: VS is not forced 0b1: VS is forced low
FORCE_HS_LOW	4	Force HS Low (before optional inversion)	0b0: HS is not forced 0b1: HS is forced low
FORCE_DE_LOW	3	Force DE Low (before optional inversion)	0b0: DE is not forced 0b1: DE is forced low
VS_INVERT	2	Invert VS after video timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INVERT	1	Invert HS after video timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INVERT	0	Invert DE after video timing generator	0b0: Do not invert DE 0b1: Invert DE

VTX2 (0x422, 0x522)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_DLY_2	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DELAY cycles from the input VS. (bits [23:16])	0xXX: Most significant byte of VS delay

VTX3 (0x423, 0x523)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_DLY_1	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DELAY cycles from the input VS. (bits [15:8])	0xXX: Middle significant byte of VS delay

VTX4 (0x424, 0x524)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_DLY_0	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DELAY cycles from the input VS. (bits [7:0])	0xXX: Least significant byte of VS delay

VTX5 (0x425, 0x525)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_HIGH_2	7:0	VS high period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS high period

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VTX6 (0x426, 0x526)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_HIGH_1	7:0	VS high period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS high period

VTX7 (0x427, 0x527)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_HIGH_0	7:0	VS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS high period

VTX8 (0x428, 0x528)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_LOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_LOW_2	7:0	VS low period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS low period

VTX9 (0x429, 0x529)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_LOW_1	7:0	VS low period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS low period

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VTX10 (0x42A, 0x52A)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_LOW_0	7:0	VS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS low period

VTX11 (0x42B, 0x52B)

BIT	7	6	5	4	3	2	1	0
Field	V2H_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_2	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first HS rising edge

VTX12 (0x42C, 0x52C)

BIT	7	6	5	4	3	2	1	0
Field	V2H_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_1	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first HS rising edge

VTX13 (0x42D, 0x52D)

BIT	7	6	5	4	3	2	1	0
Field	V2H_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_0	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS edge to first HS rising edge

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VTX14 (0x42E, 0x52E)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_HIGH_1	7:0	HS high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS high period

VTX15 (0x42F, 0x52F)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_HIGH_0	7:0	HS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS high period

VTX16 (0x430, 0x530)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_LOW_1	7:0	HS low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS low period

VTX17 (0x431, 0x531)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_LOW_0	7:0	HS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS low period

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VTX18 (0x432, 0x532)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_CNT_1	7:0	HS pulses per frame (bits [15:8])	0xXX: Most significant byte of HS pulses per frame

VTX19 (0x433, 0x533)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_CNT_0	7:0	HS pulses per frame (bits [7:0])	0xXX: Least significant byte of HS pulses per frame

VTX20 (0x434, 0x534)

BIT	7	6	5	4	3	2	1	0
Field	V2D_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_2	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first DE

VTX21 (0x435, 0x535)

BIT	7	6	5	4	3	2	1	0
Field	V2D_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_1	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first DE

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VTX22 (0x436, 0x536)

BIT	7	6	5	4	3	2	1	0
Field	V2D_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_0	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS edge to first DE

VTX23 (0x437, 0x537)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_HIGH_1	7:0	DE high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE high period

VTX24 (0x438, 0x538)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_HIGH_0	7:0	DE high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE high period

VTX25 (0x439, 0x539)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_LOW_1	7:0	DE low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE low period

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VTX26 (0x43A, 0x53A)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_LOW_0	7:0	DE low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE low period

VTX27 (0x43B, 0x53B)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_CNT_1	7:0	Active lines per frame (bits [15:8])	0xXX: Most significant byte of DE pulses per frame

VTX28 (0x43C, 0x53C)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_CNT_0	7:0	Active lines per frame (bits [7:0])	0xXX: Least significant byte of DE pulses per frame

VTX29 (0x43D, 0x53D)

BIT	7	6	5	4	3	2	1	0
Field	VID_PRBS_EN	–	–	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
Reset	0b0	–	–	–	–	0b0	0b00	
Access Type	Write, Read	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PRBS_EN	7	Enables video PRBS generator	0b0: Video PRBS generator disabled 0b1: Video PRBS generator enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_MODE	2	Gradient pattern generator mode	0b0: 0b0: Gradient mode increasing. Each gradient color starts from a value of 0x00 and increases to 0xFF. 0b1: 0b1: Gradient mode decreasing. Each gradient color starts from a value of 0xFF and decreases to 0x00.
PATGEN_MODE	1:0	Pattern generator mode	0b00: Pattern generator disabled - use video from the serializer input 0b01: Generate checkerboard pattern 0b10: Generate gradient pattern 0b11: Reserved

VTX30 (0x43E, 0x53E)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_INC[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_INC	7:0	Gradient mode increment amount Increment amount is the register value divided by 4.	0xXX: Gradient increment base

VTX31 (0x43F, 0x53F)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_L	7:0	Checkerboard mode Color A lower byte	0xXX: Least significant byte of checkerboard mode Color A

VTX32 (0x440, 0x540)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_M	7:0	Checkerboard mode Color A middle byte	0xXX: Middle significant byte of checkerboard mode Color A

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VTX33 (0x441, 0x541)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_H	7:0	Checkerboard mode Color A high byte	0xXX: Most significant byte of checkerboard mode Color A

VTX34 (0x442, 0x542)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_L	7:0	Checkerboard mode Color B low byte	0xXX: Least significant byte of checkerboard mode Color B

VTX35 (0x443, 0x543)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_M	7:0	Checkerboard mode Color B middle byte	0xXX: Middle significant byte of checkerboard mode Color B

VTX36 (0x444, 0x544)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_H	7:0	Checkerboard mode Color B high byte	0xXX: Most significant byte of checkerboard mode Color B

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VTX37 (0x445, 0x545)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_A[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_A	7:0	Checkerboard mode Color A repeat count	0xXX: Repeat count of checkerboard mode Color A

VTX38 (0x446, 0x546)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_B	7:0	Checkerboard mode Color B repeat count	0xXX: Repeat count of checkerboard mode Color B

VTX39 (0x447, 0x547)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_ALT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_ALT	7:0	Checkerboard mode alternate line count	0xXX: Checkerboard mode alternate line count

VTX40 (0x448, 0x548)*

BIT	7	6	5	4	3	2	1	0
Field	DIS_COLOR_CROSSBAR	RSVD	–	–	VA_BEFORE_WM	AUTO_COLOR_DEPTH	COLOR_DEPTH[1:0]	
Reset	0b0	0b0	–	–	0b0	0b1	0b01	
Access Type	Write, Read		–	–	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_COLOR_CROSSBAR	7	Disable color crossbar	0b0: Enable color crossbar 0b1: Disable color crossbar, use GMSL1 crossbar
VA_BEFORE_WM	3	For tell-tale safety applications, generate CRC before the watermark block	0b0: After watermark 0b1: Before watermark

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BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_COLOR_DEPTH	2	Auto bits per color When set to 1, BPP register in Video Tx register block determines bits per color.	0b0: Disabled 0b1: Enabled
COLOR_DEPTH	1:0	Bits per color (used when AUTO_COLOR_DEPTH—VTX40 register = 0)	0b00: 6-bits color 0b01: 8-bits color 0b10: 10-bits color 0b11: Reserved

VTX41 (0x449, 0x549)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VID_ASIL_INJ_ERR	VID_ASIL_CRC_ERR_OEN	VID_ASIL_CRC_ERR	VID_ASIL_CRC_CHK_EARLY	VID_ASIL_CRC_CHK_EN
Reset	–	–	–	0b0	0b1	0b0	0b0	0b1
Access Type	–	–	–	Write, Read	Write, Read	Read Clears All	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VID_ASIL_INJ_ERR	4	Inject error to verify video pipeline CRC functionality	0b0: Do not inject error 0b1: Inject error
VID_ASIL_CRC_ERR_OEN	3	Enable reporting video pipeline CRC error flag (VID_ASIL_CRC_ERR) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VID_ASIL_CRC_ERR	2	Latched video pipeline CRC error status for functional safety	0b0: Error not detected 0b1: Error detected
VID_ASIL_CRC_CHK_EARLY	1	Check video pipeline CRC before WM, FRC and Crossbar blocks This bit shall be set if any one of these blocks is enabled.	0b0: Video pipeline CRC is performed at the output of VTX 0b1: Video pipeline CRC is performed at the input of VTX
VID_ASIL_CRC_CHK_EN	0	Enable video pipeline CRC for functional safety 32-bit CRC is generated for each video frame when writing data to the video line FIFO memory and checked after data is read at the input or at the output of the VTX block.	0b0: Disabled 0b1: Enabled

outa (0x4B4, 0x5B4)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_0	7:0	Frames CRC result

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outb (0x4B5, 0x5B5)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_1	7:0	Frames CRC result

outc (0x4B6, 0x5B6)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_2	7:0	Frames CRC result

outd (0x4B7, 0x5B7)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_3	7:0	Frames CRC result

RLMS34 (0x1434, 0x1534)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntL	7:0	Eye-monitor period count (RxClk20) LSb	0xXX: Eye-monitor period count (LSb)

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RLMS35 (0x1435, 0x1535)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntH	7:0	Eye-monitor period count (RxClk20) MSb	0xXX: Eye-monitor period count (MSb)

RLMS37 (0x1437, 0x1537)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–			Read Only	Write Only	Write Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonDone	4	Eye-monitor period complete (read-only, reset on start)	0b0: Eye-monitor data collection not complete 0b1: Eye-monitor data collection complete
EyeMonCntClr	3	Eye-monitor error/valid count clear (one-shot) Readback is EyeMonClrPL from long pulse generation	0b0: NA 0b1: Clear eye-monitor data collection counters
EyeMonStart	2	Eye-monitor start (one-shot) Readback is EyeMonStClrPL from long pulse generation for both start and clear	0b0: NA 0b1: Start eye-monitor data collection
EyeMonPh	1	Eye-monitor phase	0b0: Eye-monitor search early phase 0b1: Eye-monitor search late phase
EyeMonDPol	0	Eye-monitor data polarity	0b0: Eye-monitor search for ones 0b1: Eye-monitor search for zeros

RLMS38 (0x1438, 0x1538)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntL	7:0	Eye-monitor error count (read-only)	0xXX: Eye-monitor error count (LSb)

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RLMS39 (0x1439, 0x1539)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntH	7:0	Eye-monitor error count (read-only)	0xXX: Eye-monitor error count (MSb)

RLMS3A (0x143A, 0x153A)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntL	7:0	Eye-monitor valid (hit) count (read-only)	0xXX: Eye-monitor valid count (LSb)

RLMS3B (0x143B, 0x153B)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntH	7:0	Eye-monitor valid (hit) count (read-only)	0xXX: Eye-monitor valid count (MSb)

RLMS3D (0x143D, 0x153D)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPh[6:0]							ErrChPhTogEn
Reset	0b0000000							0b1
Access Type	Read Only							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPh	7:1	Error channel phase (read-only)	0bXXXXXXX: 5.6 degrees per step
ErrChPhTogEn	0	Enables error channel phase toggle	0: Use primary phase only 1: Auto toggle phase between primary and secondary

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RLMS49 (0x1449, 0x1549)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
Reset	0x0	0b1	0b1	0b1	0b0	0b0	–	0b1
Access Type						Write, Read	–	

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPwrUp	2	Error channel power-down	0b0: Error channel power disabled 0b1: Error channel power enabled

RLMS58 (0x1458, 0x1558)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh1[6:0]						
Reset	–	0b0101000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh1	6:0	Error channel threshold voltage for ones	0bXXXXXXX: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS59 (0x1459, 0x1559)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh0[6:0]						
Reset	–	0b1101000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh0	6:0	Error channel threshold voltage for zeros	0bXXXXXXX: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS64 (0x1464, 0x1564)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
Reset	–	–	–	–	–	0b0	0b00	
Access Type	–	–	–	–	–		Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx spread spectrum mode	0b00: No spread spectrum (manual phase) 0b01: Center spread 0b10: Reserved 0b11: Reserved

RLMS70 (0x1470, 0x1570)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0b0000001						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx spread spectrum frequency control	0bXXXXXXX: Tx spread spectrum center frequency control

RLMS71 (0x1471, 0x1571)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0b000001						0b0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx spread spectrum center spread startup control	0bXXXXXX: Tx spread spectrum center spread startup control
TxSSCEn	0	Enables Tx spread spectrum	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x1472, 0x1572)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx spread spectrum frequency pre-scaler low byte	0xXX: Tx spread spectrum frequency pre-scaler low byte

RLMS73 (0x1473, 0x1573)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreScIH	2:0	Tx spread spectrum frequency pre-scaler high bits	0bXXX: Tx spread spectrum frequency pre-scaler high bits

RLMS74 (0x1474, 0x1574)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx spread spectrum interpolator phase low byte	0xXX: Tx spread spectrum frequency interpolator phase low byte

RLMS75 (0x1475, 0x1575)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx spread spectrum interpolator phase high bits	0bXXXXXXX: Tx spread spectrum frequency interpolator phase high bits

RLMS76 (0x1476, 0x1576)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx spread spectrum interpolator phase quadrant	0bXX: Tx spread spectrum interpolator phase quadrant

RLMS95 (0x1495, 0x1595)

BIT	7	6	5	4	3	2	1	0
Field	TxAmplManEn	RSVD	TxAmplMan[5:0]					
Reset	0b0	0b1	0b101001					
Access Type	Write, Read		Write, Read					

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BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplManEn	7	Tx amplitude manual override	0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude
TxAmplMan	5:0	Tx amplitude	0bXXXXXX: Binary amplitude 10mV per count

RLMSA4 (0x14A4, 0x15A4)*-

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0b10		0b111101					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_PER_MULT	7:6	Adaptive EQ period multiplier	0b00: 1ms 0b01: 4ms 0b10: 16ms 0b11: 64ms
AEQ_PER	5:0	Adaptive EQ period Periodic adaptation is disabled when value is 0 Adaptive EQ period is (AEQ_PER value times AEQ_PER_MULT)	0bXXXXXX: Only zeros have a special meaning. See description

RLMSAC (0x14AC, 0x15AC)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
Reset	0b1	0b1001101						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTAFR3G	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecFR3G	6:0	Error channel phase secondary (odd)	0bXXXXXXX: 7'h4D

RLMSAD (0x14AD, 0x15AD)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
Reset	0b0	0b0001101						
Access Type	Write, Read	Write, Read						

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BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTAFR3G	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriFR3G	6:0	Error channel phase primary (even)	0bXXXXXXX: 7'h0D

HDCP_DES0 (0x1676, 0x1776)*

BIT	7	6	5	4	3	2	1	0
Field	AH_DES_REG_OFFSET_L[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AH_DES_REG_OFFSET_L	7:0	Low byte of the register offset of the HDCP register block of the paired deserializer	0xXX: Low byte (LSB) of the register offset of deserializer's HDCP register block

HDCP_DES1 (0x1677, 0x1777)*

BIT	7	6	5	4	3	2	1	0
Field	AH_DES_REG_OFFSET_H[7:0]							
Reset	0x16							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AH_DES_REG_OFFSET_H	7:0	High byte of the register offset of the HDCP register block of the paired deserializer	0xXX: High byte (MSB) of the register offset of deserializer's HDCP register block

HDCP_AS0 (0x1678, 0x1778)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_0	7:0	Optional seed for internal random number generator	0xXX: Byte 0 (LSB) of the internal random number generator seed

HDCP_AS1 (0x1679, 0x1779)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_1	7:0	Optional seed for internal random number generator	0xXX: Byte 1 of the internal random number generator seed

HDCP_AS2 (0x167A, 0x177A)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_2	7:0	Optional seed for internal random number generator	0xXX: Byte 2 of the internal random number generator seed

HDCP_AS3 (0x167B, 0x177B)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_3	7:0	Optional seed for internal random number generator	0xXX: Byte 3 of the internal random number generator seed

HDCP_AS4 (0x167C, 0x177C)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_4	7:0	Optional seed for internal random number generator	0xXX: Byte 4 (MSB) of the internal random number generator seed

HDCP_TX0 (0x1680, 0x1780)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_0	7:0	HDCP Receiver KSV	0xXX: Byte 0 (LSB) of the HDCP receiver KSV

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HDCP_TX1 (0x1681, 0x1781)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_1	7:0	HDCP Receiver KSV	0xXX: Byte 1 of the HDCP receiver KSV

HDCP_TX2 (0x1682, 0x1782)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_2	7:0	HDCP Receiver KSV	0xXX: Byte 2 of the HDCP receiver KSV

HDCP_TX3 (0x1683, 0x1783)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_3	7:0	HDCP Receiver KSV	0xXX: Byte 3 of the HDCP receiver KSV

HDCP_TX4 (0x1684, 0x1784)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_4	7:0	HDCP Receiver KSV	0xXX: Byte 4 (MSB) of the HDCP receiver KSV

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HDCP_TX5 (0x1685, 0x1785)

BIT	7	6	5	4	3	2	1	0
Field	RIP_0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RIP_0	7:0	Link verification response EN_INT_COMP = 0 → Ri of Tx (Read) EN_INT_COMP = 1 → Ri' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of Ri or Ri'

HDCP_TX6 (0x1686, 0x1786)

BIT	7	6	5	4	3	2	1	0
Field	RIP_1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RIP_1	7:0	Link verification response EN_INT_COMP = 0 → Ri of Tx (Read) EN_INT_COMP = 1 → Ri' of Rx (Write and Read)	0xXX: Byte 1 (MSB) of Ri or Ri'

HDCP_TX7 (0x1687, 0x1787)

BIT	7	6	5	4	3	2	1	0
Field	PJP[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PJP	7:0	Enhanced link verification response EN_INT_COMP = 0 → Pj of Tx (Read) EN_INT_COMP = 1 → Pj' of Rx (Write and Read)	0xXX: Value of Pj or Pj'

HDCP_TX8 (0x1688, 0x1788)

BIT	7	6	5	4	3	2	1	0
Field	AN_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_0	7:0	Session random number	0xXX: Byte 0 (LSB) of the session random number

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HDCP_TX9 (0x1689, 0x1789)

BIT	7	6	5	4	3	2	1	0
Field	AN_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_1	7:0	Session random number	0xXX: Byte 1 of the session random number

HDCP_TXA (0x168A, 0x178A)

BIT	7	6	5	4	3	2	1	0
Field	AN_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_2	7:0	Session random number	0xXX: Byte 2 of the session random number

HDCP_TXB (0x168B, 0x178B)

BIT	7	6	5	4	3	2	1	0
Field	AN_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_3	7:0	Session random number	0xXX: Byte 3 of the session random number

HDCP_TXC (0x168C, 0x178C)

BIT	7	6	5	4	3	2	1	0
Field	AN_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_4	7:0	Session random number	0xXX: Byte 4 of the session random number

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HDCP_TXD (0x168D, 0x178D)

BIT	7	6	5	4	3	2	1	0
Field	AN_5[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_5	7:0	Session random number	0xXX: Byte 5 of the session random number

HDCP_TXE (0x168E, 0x178E)

BIT	7	6	5	4	3	2	1	0
Field	AN_6[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_6	7:0	Session random number	0xXX: Byte 6 of the session random number

HDCP_TXF (0x168F, 0x178F)

BIT	7	6	5	4	3	2	1	0
Field	AN_7[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_7	7:0	Session random number	0xXX: Byte 7 (MSB) of the session random number

HDCP_TX10 (0x1690, 0x1790)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_0	7:0	HDCP transmitter KSV	0xXX: Byte 0 (LSB) of the HDCP transmitter KSV

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HDCP_TX11 (0x1691, 0x1791)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_1	7:0	HDCP transmitter KSV	0xXX: Byte 1 of the HDCP transmitter KSV

HDCP_TX12 (0x1692, 0x1792)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_2	7:0	HDCP transmitter KSV	0xXX: Byte 2 of the HDCP transmitter KSV

HDCP_TX13 (0x1693, 0x1793)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_3	7:0	HDCP transmitter KSV	0xXX: Byte 3 of the HDCP transmitter KSV

HDCP_TX14 (0x1694, 0x1794)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_4	7:0	HDCP transmitter KSV	0xXX: Byte 4 (MSB) of the HDCP transmitter KSV

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HDCP_TX15 (0x1695, 0x1795)

BIT	7	6	5	4	3	2	1	0
Field	–	EN_INT_COMP	–	–	HDCP_RESET	START_AUTH	VSYNC_DET	ENC_EN
Reset	–	0b0	–	–	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	–	–	Write, Read	Write Clears All, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_INT_COMP	6	Enable internal comparison mode	0b0: µC comparison mode 0b1: Internal comparison mode
HDCP_RESET	3	Automatically resets to 0 ~ 1µs after it has written 1	0b0: Normal operation 0b1: Reset HDCP circuits
START_AUTH	2	Start HDCP authentication. Automatically resets to 0 after written.	0b0: Normal operation 0b1: Start authentication
VSYNC_DET	1	Automatically sets to 1 when VSYNC falling edge is detected	0b0: VSYNC falling edge not detected 0b1: VSYNC falling edge detected
ENC_EN	0	Enable HDCP encryption	0b0: HDCP encryption disabled 0b1: HDCP encryption enabled

HDCP_TX16 (0x1696, 0x1796)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PJF_MATCH	V_MATCHED	PJ_MATCHED	RI_MATCHED	INVALID_BKSV
Reset	–	–	–	0b0	0b0	0b0	0b0	0b1
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PJF_MATCH	4	At least one byte of Fast-Pj matches Fast-Pj'	0b0: Fast-Pj does not match Fast-Pj' 0b1: Fast-Pj matches Fast-Pj'
V_MATCHED	3	V matched V'	0b0: V does not match V' 0b1: V matches V'
PJ_MATCHED	2	Pj matched Pj'	0b0: Pj does not match Pj' 0b1: Pj matches Pj'
RI_MATCHED	1	Ri matched Ri'	0b0: Ri did not match Ri' 0b1: Ri matched Ri'
INVALID_BKSV	0	Invalid BKSV detected	0b0: BKSV is valid 0b1: BKSV is invalid

HDCP_TX17 (0x1697, 0x1797)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[6:0]							HDCP_REPEATER
Reset	0b0000000							0b0
Access Type								Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_REPEATER	0	HDCP repeater enable	0b0: HDCP repeater not enabled 0b1: HDCP repeater enabled

HDCP_TX18 (0x1698, 0x1798)

BIT	7	6	5	4	3	2	1	0
Field	AH_STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AH_STATUS	7:0	Auto-HDCP status	0b0010: AHDCP in 1st part of authentication 0b0011: AHDCP in 2nd/3rd part of authentication 0b0100: V' not match 0b0101: Max devices or cascade exceeded. 0b0110: R0 not match 0b0111: Bad BKSV

HDCP_TX19 (0x1699, 0x1799)

BIT	7	6	5	4	3	2	1	0
Field	HIBW_PJ_CALC[1:0]		–	–	–	–	–	DIS_AUDIO_ENC
Reset	0b00		–	–	–	–	–	0b0
Access Type	Write, Read		–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HIBW_PJ_CALC	7:6	GMSL1 mode, Pj calculation pixel in high-bandwidth mode	0b00: VS and DE 0b01: VS and HS 0b10: VS only 0b11: Reserved
DIS_AUDIO_ENC	0	Disable encryption of audio	0b0: Audio encryption disabled 0b1: Audio encryption enabled

HDCP_TX1A (0x169A, 0x179A)

BIT	7	6	5	4	3	2	1	0
Field	PJFP_0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PJFP_0	7:0	Fast enhanced link verification response (low 8 bits) EN_INT_COMP = 0 → Pjf of Tx (Read) EN_INT_COMP = 1 → Pjf' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of Pjf or Pjf'

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HDCP_TX1B (0x169B, 0x179B)

BIT	7	6	5	4	3	2	1	0
Field	PJFP_1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PJFP_1	7:0	Fast enhanced link verification response (middle 8 bits) EN_INT_COMP = 0 → Pjf of Tx (Read) EN_INT_COMP = 1 → Pjf' of Rx (Write and Read)	0xXX: Byte 1 of Pjf or Pjf'

HDCP_TX1C (0x169C, 0x179C)

BIT	7	6	5	4	3	2	1	0
Field	PJFP_2[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PJFP_2	7:0	Fast enhanced link verification response (high 8 bits) EN_INT_COMP = 0 → Pjf of Tx (Read) EN_INT_COMP = 1 → Pjf' of Rx (Write and Read)	0xXX: Byte 2 (MSB) of Pjf or Pjf'

HDCP_TX20 (0x16A0, 0x17A0)

BIT	7	6	5	4	3	2	1	0
Field	VH0_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH0_0	7:0	H0 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H0 or V'.H0

HDCP_TX21 (0x16A1, 0x17A1)

BIT	7	6	5	4	3	2	1	0
Field	VH0_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
VH0_1	7:0	H0 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H0 or V'.H0

HDCP_TX22 (0x16A2, 0x17A2)

BIT	7	6	5	4	3	2	1	0
Field	VH0_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH0_2	7:0	H0 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H0 or V'.H0

HDCP_TX23 (0x16A3, 0x17A3)

BIT	7	6	5	4	3	2	1	0
Field	VH0_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH0_3	7:0	H0 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H0 or V'.H0

HDCP_TX24 (0x16A4, 0x17A4)

BIT	7	6	5	4	3	2	1	0
Field	VH1_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH1_0	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H1 or V'.H1

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HDCP_TX25 (0x16A5, 0x17A5)

BIT	7	6	5	4	3	2	1	0
Field	VH1_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH1_1	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H1 or V'.H1

HDCP_TX26 (0x16A6, 0x17A6)

BIT	7	6	5	4	3	2	1	0
Field	VH1_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH1_2	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H1 or V'.H1

HDCP_TX27 (0x16A7, 0x17A7)

BIT	7	6	5	4	3	2	1	0
Field	VH1_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH1_3	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H1 or V'.H1

HDCP_TX28 (0x16A8, 0x17A8)

BIT	7	6	5	4	3	2	1	0
Field	VH2_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
VH2_0	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H2 or V'.H2

HDCP_TX29 (0x16A9, 0x17A9)

BIT	7	6	5	4	3	2	1	0
Field	VH2_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH2_1	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H2 or V'.H2

HDCP_TX2A (0x16AA, 0x17AA)

BIT	7	6	5	4	3	2	1	0
Field	VH2_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH2_2	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H2 or V'.H2

HDCP_TX2B (0x16AB, 0x17AB)

BIT	7	6	5	4	3	2	1	0
Field	VH2_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH2_3	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H2 or V'.H2

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HDCP_TX2C (0x16AC, 0x17AC)

BIT	7	6	5	4	3	2	1	0
Field	VH3_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH3_0	7:0	H3 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H3 or V'.H3

HDCP_TX2D (0x16AD, 0x17AD)

BIT	7	6	5	4	3	2	1	0
Field	VH3_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH3_1	7:0	H3 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H3 or V'.H3

HDCP_TX2E (0x16AE, 0x17AE)

BIT	7	6	5	4	3	2	1	0
Field	VH3_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH3_2	7:0	H3 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H3 or V'.H3

HDCP_TX2F (0x16AF, 0x17AF)

BIT	7	6	5	4	3	2	1	0
Field	VH3_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
VH3_3	7:0	H3 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H3 or V'.H3

HDCP_TX30 (0x16B0, 0x17B0)

BIT	7	6	5	4	3	2	1	0
Field	VH4_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH4_0	7:0	H4 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H4 or V'.H4

HDCP_TX31 (0x16B1, 0x17B1)

BIT	7	6	5	4	3	2	1	0
Field	VH4_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH4_1	7:0	H4 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H4 or V'.H4

HDCP_TX32 (0x16B2, 0x17B2)

BIT	7	6	5	4	3	2	1	0
Field	VH4_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH4_2	7:0	H4 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H4 or V'.H4

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HDCP_TX33 (0x16B3, 0x17B3)

BIT	7	6	5	4	3	2	1	0
Field	VH4_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH4_3	7:0	H4 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H4 or V'.H4

HDCP_TX34 (0x16B4, 0x17B4)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_MAX_DEV_EXCEEDED	HDCP_DEV_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_MAX_DEV_EXCEEDED	7	Maximum device count exceeded in repeater mode	0b0: Maximum number of devices not exceeded (14 or less) 0b1: Maximum number of devices exceeded (more than 14)
HDCP_DEV_CNT	6:0	Repeater device count	0bXXXXXXX: Number of devices attached

HDCP_TX35 (0x16B5, 0x17B5)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				HDCP_MAX_CASCADE_EXCEEDED	HDCP_DEPTH[2:0]		
Reset	0x0				0b0	0b000		
Access Type					Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_MAX_CASCADE_EXCEEDED	3	HDCP repeater mode exceeded maximum depth	0b0: Maximum number of cascaded devices not exceeded (7 or less) 0b1: Maximum number of cascaded devices exceeded (more than 7)
HDCP_DEPTH	2:0	HDCP repeater depth	0bXXX: Depth of cascaded devices

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HDCP_TX36 (0x16B6, 0x17B6)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_GPMEM[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_GPMEM	7:0	General purpose memory byte. This has no effect on the operation of the device, it can be used for handshaking between more than one microcontroller in the system.	0xXX: General purpose memory byte

HDCP_TX37 (0x16B7, 0x17B7)*

BIT	7	6	5	4	3	2	1	0
Field	HDCP_PD	FAST_PJ_EN	FORCE_AUDIO	FORCE_VIDEO	AH_MASK_ENCOFF	AH_MASK_NEWDEV	AH_MASK_KSVRDY	AH_MASK_FAIL
Reset	0b1	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_PD	7	Power down HDCP blocks	0b0: HDCP blocks powered up 0b1: Power down HDCP blocks
FAST_PJ_EN	6	Enable Fast-Pj mode (fast-enhanced link integrity check)	0b0: Normal Pj mode 0b1: Fast-Pj mode enabled
FORCE_AUDIO	5	Force to static audio	0b0: Normal operation 0b1: Force audio data to 0
FORCE_VIDEO	4	Force to static video	0b0: Normal operation 0b1: Force video to static video
AH_MASK_ENCOFF	3	Disable auto-HDCP encryption-off interrupt	0b0: Auto-HDCP encryption off interrupt enabled 0b1: Auto-HDCP encryption off interrupt masked
AH_MASK_NEWDEV	2	Disable auto-HDCP new-device interrupt	0b0: Auto-HDCP new device interrupt enabled 0b1: Auto-HDCP new device interrupt masked
AH_MASK_KSVRDY	1	Disable auto-HDCP new-device interrupt	0b0: Auto-HDCP KSV ready interrupt enabled 0b1: Auto-HDCP KSV ready interrupt masked
AH_MASK_FAIL	0	Disable auto-HDCP fail interrupt	0b0: Auto-HDCP fail interrupt enabled 0b1: Auto-HDCP fail interrupt masked

HDCP_TX38 (0x16B8, 0x17B8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	AH_RD_KSVL	AH_DISENC	AH_MODE
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write Clears All, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
AH_RD_KSVL	2	Set this bit to 1 to begin Part 2 authentication for repeater DES. This bit is always read 0. In the DES repeater case, when the downstream KSV list is ready, the µC must set DES BSTATUS READY = 1 (and NEW_DEV_CONN = 1 if there is a new device attached), then write AH_RD_KSVLIS = 1 to trigger AHDCP to read the KSV list and check V's. If V' matches, AH_KSV_READY is set and DES BSTATUS is cleared.	0b0: Normal operation 0b1: Start Part 2 authentification for repeater deserializer
AH_DISENC	1	This bit is used to enable/disable cypher (encryption) in AHDCP mode without trigger reauthentication. 0: Enable cypher in next VS frame. 1: Disable cypher in next VS frame. Before changing AH_MODE from 1 to 0, make sure to set AH_DISENC = 1 and wait two VS frames to disable encyption for both SER and DES. Alternatively, set ENCRYPTION_ENABLE bit in both SER and DES to 0.	0b0: Enable encryption in next VS frame 0b1: Disable encryption in next VS frame
AH_MODE	0	Auto-HDCP enable. Before setting AH_MODE from 1 to 0, first set AH_DISENC from 0 to 1 and wait for about three VSYNC frame times so that encryption is turned off.	0b0: Manual HDCP or non-HDCP mode 0b1: Auto-HDCP mode

HDCP_TX39 (0x16B9, 0x17B9)*

BIT	7	6	5	4	3	2	1	0
Field	AH_DES_ADDR[6:0]							–
Reset	0b1001000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
AH_DES_ADDR	7:1	Device address of the connected deserializer	0bXXXXXXX: Device address of the connected deserializer

HDCP_TX3A (0x16BA, 0x17BA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_0	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 0

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HDCP_TX3B (0x16BB, 0x17BB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_1	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 1

HDCP_TX3C (0x16BC, 0x17BC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_2	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 2

HDCP_TX3D (0x16BD, 0x17BD)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_3	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 3

HDCP_TX3E (0x16BE, 0x17BE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_4	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 4

HDCP_TX3F (0x16BF, 0x17BF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_5	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 5

HDCP_TX40 (0x16C0, 0x17C0)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_6	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 6

HDCP_TX41 (0x16C1, 0x17C1)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_7	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 7

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HDCP_TX42 (0x16C2, 0x17C2)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_8	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 8

HDCP_TX43 (0x16C3, 0x17C3)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_9	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 9

HDCP_TX44 (0x16C4, 0x17C4)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_10	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 10

HDCP_TX45 (0x16C5, 0x17C5)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_11	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 11

HDCP_TX46 (0x16C6, 0x17C6)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_12	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 12

HDCP_TX47 (0x16C7, 0x17C7)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_13	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 13

HDCP_TX48 (0x16C8, 0x17C8)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_14	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 14

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HDCP_TX49 (0x16C9, 0x17C9)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_15	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 15

HDCP_TX4A (0x16CA, 0x17CA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_16[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_16	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 16

HDCP_TX4B (0x16CB, 0x17CB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_17[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_17	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 17

HDCP_TX4C (0x16CC, 0x17CC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_18[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_18	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 18

HDCP_TX4D (0x16CD, 0x17CD)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_19[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_19	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 19

HDCP_TX4E (0x16CE, 0x17CE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_20[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_20	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 20

HDCP_TX4F (0x16CF, 0x17CF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_21[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_21	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 21

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HDCP_TX50 (0x16D0, 0x17D0)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_22[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_22	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 22

HDCP_TX51 (0x16D1, 0x17D1)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_23[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_23	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 23

HDCP_TX52 (0x16D2, 0x17D2)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_24[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_24	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 24

HDCP_TX53 (0x16D3, 0x17D3)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_25[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_25	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 25

HDCP_TX54 (0x16D4, 0x17D4)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_26[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_26	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 26

HDCP_TX55 (0x16D5, 0x17D5)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_27[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_27	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 27

HDCP_TX56 (0x16D6, 0x17D6)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_28[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_28	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 28

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HDCP_TX57 (0x16D7, 0x17D7)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_29[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_29	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 29

HDCP_TX58 (0x16D8, 0x17D8)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_30[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_30	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 30

HDCP_TX59 (0x16D9, 0x17D9)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_31[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_31	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 31

HDCP_TX5A (0x16DA, 0x17DA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_32[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_32	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 32

HDCP_TX5B (0x16DB, 0x17DB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_33[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_33	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 33

HDCP_TX5C (0x16DC, 0x17DC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_34[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_34	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 34

HDCP_TX5D (0x16DD, 0x17DD)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_35[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_35	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 35

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HDCP_TX5E (0x16DE, 0x17DE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_36[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_36	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 36

HDCP_TX5F (0x16DF, 0x17DF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_37[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_37	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 37

HDCP_TX60 (0x16E0, 0x17E0)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_38[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_38	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 38

HDCP_TX61 (0x16E1, 0x17E1)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_39[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_39	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 39

HDCP_TX62 (0x16E2, 0x17E2)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_40[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_40	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 40

HDCP_TX63 (0x16E3, 0x17E3)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_41[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_41	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 41

HDCP_TX64 (0x16E4, 0x17E4)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_42[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_42	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 42

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HDCP_TX65 (0x16E5, 0x17E5)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_43[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_43	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 43

HDCP_TX66 (0x16E6, 0x17E6)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_44[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_44	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 44

HDCP_TX67 (0x16E7, 0x17E7)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_45[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_45	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 45

HDCP_TX68 (0x16E8, 0x17E8)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_46[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_46	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 46

HDCP_TX69 (0x16E9, 0x17E9)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_47[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_47	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 47

HDCP_TX6A (0x16EA, 0x17EA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_48[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_48	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 48

HDCP_TX6B (0x16EB, 0x17EB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_49[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_49	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 49

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HDCP_TX6C (0x16EC, 0x17EC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_50[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_50	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 50

HDCP_TX6D (0x16ED, 0x17ED)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_51[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_51	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 51

HDCP_TX6E (0x16EE, 0x17EE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_52[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_52	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 52

HDCP_TX6F (0x16EF, 0x17EF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_53[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_53	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 53

HDCP_TX70 (0x16F0, 0x17F0)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_54[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_54	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 54

HDCP_TX71 (0x16F1, 0x17F1)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_55[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_55	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 55

HDCP_TX72 (0x16F2, 0x17F2)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_56[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_56	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 56

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HDCP_TX73 (0x16F3, 0x17F3)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_57[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_57	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 57

HDCP_TX74 (0x16F4, 0x17F4)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_58[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_58	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 58

HDCP_TX75 (0x16F5, 0x17F5)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_59[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_59	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 59

HDCP_TX76 (0x16F6, 0x17F6)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_60[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_60	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 60

HDCP_TX77 (0x16F7, 0x17F7)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_61[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_61	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 61

HDCP_TX78 (0x16F8, 0x17F8)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_62[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_62	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 62

HDCP_TX79 (0x16F9, 0x17F9)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_63[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_63	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 63

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HDCP_TX7A (0x16FA, 0x17FA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_64[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_64	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 64

HDCP_TX7B (0x16FB, 0x17FB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_65[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_65	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 65

HDCP_TX7C (0x16FC, 0x17FC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_66[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_66	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 66

HDCP_TX7D (0x16FD, 0x17FD)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_67[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_67	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 67

HDCP_TX7E (0x16FE, 0x17FE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_68[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_68	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 68

HDCP_TX7F (0x16FF, 0x17FF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_69[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_69	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 69

DPLL_3 (0x1B03, 0x1C03)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	config_force_enable_ss	config_spread_bit_ratio[2:0]		
Reset	0b1	0b0	0b0	0b0	0b0	0b010		
Access Type					Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
config_force_enable_ss	3	Enables the output of the triangle wave generator (overrides en_ss to force triangle_wave on)	0b0: Spread output disabled 0b1: Spread output enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
config_spread_bit_ratio	2:0	Controls the magnitude of the triangle wave intput to the divider dsm as a percentage of the nominal divider value. If config registers are reset, the spread_bit_ratio value will not propagate to the triangle wave without rewriting to it. Likewise, if triangle wave module is reset, the user will need to rewrite to spread_bit_ratio to set it back to desired value.	0b000: Off 0b001: 0.25% 0b010: 0.5% 0b011: 1% 0b100: 2% 0b101: 4% 0b110: 4% 0b111: 4%

REGCRC0 (0x1D00)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	LIMIT_REG_RANGE	GEN_ROLLING_CRC	I2C_WR_COMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LIMIT_REG_RANGE	5	Limit the minimum and maximum range of registers that are calculated	
GEN_ROLLING_CRC	4	Calculate CRC using additional 4-bit counter, so CRC value cycles every 16 invocations	0b0: Disabled 0b1: Enabled
I2C_WR_COMPUTE	3	Do CRC compute after every I^2C register write	0b0: Disabled 0b1: Enabled
PERIODIC_COMPUTE	2	Do CRC checking on periodic basis, based on CRC_PERIOD value	0b0: Disabled 0b1: Enabled
CHECK_CRC	1	Upon calculation of CRC, compare with previous calculation, except on first time through. On miscompare, issue ERRB.	0b0: Do not check CRC 0b1: Check CRC
RESET_CRC	0	Reset CRC value to 16'FFFF	0b0: Do not reset CRC value 0b1: Reset CRC value

REGCRC1 (0x1D01)*

BIT	7	6	5	4	3	2	1	0
Field	CRC_PERIOD[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CRC_PERIOD	7:0	Period for CRC recomputation This allows for varying the CRC computation time. 0000_0000 - 2ms 0000_0000 - 4ms ...

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REGCRC2 (0x1D02)

BIT	7	6	5	4	3	2	1	0
Field	REGCRC_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGCRC_LSB	7:0	CRC result LSB

REGCRC3 (0x1D03)

BIT	7	6	5	4	3	2	1	0
Field	REGCRC_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGCRC_MSB	7:0	CRC result MSB

REGCRC4 (0x1D04)*

BIT	7	6	5	4	3	2	1	0
Field	MIN_RANGE_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MIN_RANGE_LSB	7:0	Minimum Range LSB

REGCRC5 (0x1D05)*

BIT	7	6	5	4	3	2	1	0
Field	MIN_RANGE_MSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MIN_RANGE_MSB	7:0	Minimum Range MSB

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REGCRC6 (0x1D06)*

BIT	7	6	5	4	3	2	1	0
Field	MAX_RANGE_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MAX_RANGE_LSB	7:0	Maximum Range LSB

REGCRC7 (0x1D07)*

BIT	7	6	5	4	3	2	1	0
Field	MAX_RANGE_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MAX_RANGE_MSB	7:0	Maximum Range MSB

REGCRC8 (0x1D08)*

BIT	7	6	5	4	3	2	1	0
Field	SKIP0_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP0_LSB	7:0	Address 0 to skip (LSB)

REGCRC9 (0x1D09)

BIT	7	6	5	4	3	2	1	0
Field	SKIP0_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP0_MSB	7:0	Address 0 to skip (MSB)

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REGCRC10 (0x1D0A)

BIT	7	6	5	4	3	2	1	0
Field	SKIP1_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP1_LSB	7:0	Address 1 to skip (LSB)

REGCRC11 (0x1D0B)

BIT	7	6	5	4	3	2	1	0
Field	SKIP1_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP1_MSB	7:0	Address 1 to skip (MSB)

REGCRC12 (0x1D0C)

BIT	7	6	5	4	3	2	1	0
Field	SKIP2_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP2_LSB	7:0	Address 2 to skip (LSB)

REGCRC13 (0x1D0D)

BIT	7	6	5	4	3	2	1	0
Field	SKIP2_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP2_MSB	7:0	Address 2 to skip (MSB)

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REGCRC14 (0x1D0E)

BIT	7	6	5	4	3	2	1	0
Field	SKIP3_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP3_LSB	7:0	Address 3 to skip (LSB)

REGCRC15 (0x1D0F)

BIT	7	6	5	4	3	2	1	0
Field	SKIP3_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP3_MSB	7:0	Address 3 to skip (MSB)

REGCRC16 (0x1D10)

BIT	7	6	5	4	3	2	1	0
Field	SKIP4_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP4_LSB	7:0	Address 4 to skip (LSB)

REGCRC17 (0x1D11)

BIT	7	6	5	4	3	2	1	0
Field	SKIP4_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP4_MSB	7:0	Address 4 to skip (MSB)

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REGCRC18 (0x1D12)

BIT	7	6	5	4	3	2	1	0
Field	SKIP5_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP5_LSB	7:0	Address 5 to skip (LSB)

REGCRC19 (0x1D13)

BIT	7	6	5	4	3	2	1	0
Field	SKIP5_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP5_MSB	7:0	Address 5 to skip (MSB)

REGCRC20 (0x1D14)

BIT	7	6	5	4	3	2	1	0
Field	SKIP6_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP6_LSB	7:0	Address 6 to skip (LSB)

REGCRC21 (0x1D15)

BIT	7	6	5	4	3	2	1	0
Field	SKIP6_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP6_MSB	7:0	Address 6 to skip (MSB)

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REGCRC22 (0x1D16)

BIT	7	6	5	4	3	2	1	0
Field	SKIP7_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP7_LSB	7:0	Address 7 to skip (LSB)

REGCRC23 (0x1D17)*

BIT	7	6	5	4	3	2	1	0
Field	SKIP7_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP7_MSB	7:0	Address 7 to skip (MSB)

CC_CRC0 (0x1D20)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_VAL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CC_CRC_VAL	7:0	Calculated CRC value for the last write transaction

CC_CRC1 (0x1D21)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_LSB	7:0	Bits 7:0 of current message counter value

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CC_CRC2 (0x1D22)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_MSB	7:0	Bits 15:8 of current message counter value

CC_CRC3 (0x1D23)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CC_CRC_ERR_CNT	7:0	Number of CC CRC errors detected

CC_CRC4 (0x1D24)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_ERR_CNT	7:0	Number of Message Counter errors detected

CC_CRC5 (0x1D25)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RESET_MSGCNTR	–	–	RESET_MSGCNTR_ERR_CNT	RESET_CC_CRC_ERR_CNT
Reset	–	–	–	0b0	–	–	0b0	0b0
Access Type	–	–	–	Write Clears All, Read	–	–	Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_MSGCNTR	4	Reset MSGCNTR_MSB and MSGCNTR_LSB to 0 (this bit automatically clears)	0b0: Do not reset 0b1: Reset
RESET_MSGCNTR_ERR_CNT	1	Reset MSGCNTR_ERR_CNT to 0 (this bit automatically clears)	0b0: Do not reset 0b1: Reset

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BITFIELD	BITS	DESCRIPTION	DECODE
RESET_CC_CRC_ERR_CNT	0	Reset CC_CRC_ERR_CNT to 0 (this bit automatically clears)	0b0: Do not reset 0b1: Reset

CC_RTTN_ERR (0x1D26)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RTTN_CRC_INT_OEN	RTTN_CRC_ERR_FLAG	–	–	–	RSVD
Reset	–	–	0b1	0b0	–	–	–	0b0
Access Type	–	–	Write, Read	Read Clears All	–	–	–	

BITFIELD	BITS	DESCRIPTION	DECODE
RTTN_CRC_INT_OEN	5	Retention memory CRC check error status reporting enable bit.	0b0: Reporting disabled 0b1: Reporting enabled
RTTN_CRC_ERR_FLAG	4	Sticky status value for retention memory CRC error.	0b0: Flag not asserted 0b1: Flag asserted

INTR_CRC_0 (0x1D80)*

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_Y_CRC_ERR_OEN	AUDIO_X_CRC_ERR_OEN	AHDCP_CRC_ERR_OEN	GPIO_CRC_ERR_OEN	SPI_CRC_ERR_OEN	RBB_CC_CRC_ERR_OEN	PT2_CRC_ERR_OEN	PT1_CRC_ERR_OEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_Y_CRC_ERR_OEN	7	Enables reporting of AUDIO Y CRC errors (AUDIO_Y_CRC_ERR_FLAG—0x1D81) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
AUDIO_X_CRC_ERR_OEN	6	Enables reporting of AUDIO X CRC errors (AUDIO_X_CRC_ERR_FLAG—0x1D81) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
AHDCP_CRC_ERR_OEN	5	Enables reporting of AHDCP CRC errors (AHDCP_CRC_ERR_FLAG—0x1D81) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
GPIO_CRC_ERR_OEN	4	Enables reporting of GPIO CRC errors (GPIO_CRC_ERR_FLAG—0x1D81) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
SPI_CRC_ERR_OEN	3	Enables reporting of SPI CRC errors (SPI_CRC_ERR_FLAG—0x1D81) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RBB_CC_CRC_ERR_OEN	2	Enables reporting of RBB CC CRC errors (RBB_CC_CRC_ERR_FLAG—0x1D81) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PT2_CRC_ERR_OEN	1	Enables reporting of PT2 CRC errors (PT2_CRC_ERR_FLAG—0x1D81) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
PT1_CRC_ERR_OEN	0	Enables reporting of PT1 CRC errors (PT1_CRC_ERR_FLAG—0x1D81) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR_CRC_1 (0x1D81)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_Y_CRC_ERR_FLAG	AUDIO_X_CRC_ERR_FLAG	AHDCP_CRC_ERR_FLAG	GPIO_CRC_ERR_FLAG	SPI_CRC_ERR_FLAG	RBB_CC_CRC_ERR_FLAG	PT2_CRC_ERR_FLAG	PT1_CRC_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_Y_CRC_ERR_FLAG	7	AUDIO Y CRC Error Flag Asserted when AUDIO Y CRC error count > 0. Read AUDIO_Y_CRC_ERR (register CNT7) to clear.	0b0: Flag not asserted 0b1: Flag asserted
AUDIO_X_CRC_ERR_FLAG	6	AUDIO X CRC Error Flag Asserted when AUDIO X CRC error count > 0. Read AUDIO_X_CRC_ERR (register CNT6) to clear.	0b0: Flag not asserted 0b1: Flag asserted
AHDCP_CRC_ERR_FLAG	5	AHDCP CRC Error Flag Asserted when AHDCP CRC error count > 0. Read AHDCP_CRC_ERR (register CNT5) to clear.	0b0: Flag not asserted 0b1: Flag asserted
GPIO_CRC_ERR_FLAG	4	GPIO CRC Error Flag Asserted when GPIO CRC error count > 0. Read GPIO_CRC_ERR (register CNT4) to clear.	0b0: Flag not asserted 0b1: Flag asserted
SPI_CRC_ERR_FLAG	3	SPI CRC Error Flag Asserted when SPI CRC error count > 0. Read SPI_CRC_ERR (register CNT3) to clear.	0b0: Flag not asserted 0b1: Flag asserted
RBB_CC_CRC_ERR_FLAG	2	RBB CC CRC Error Flag Asserted when RBB CC CRC error count > 0. Read RBB_CC_CRC_ERR (register CNT2) to clear.	0b0: Flag not asserted 0b1: Flag asserted
PT2_CRC_ERR_FLAG	1	PT2 CRC Error Flag Asserted when PT2 CRC error count > 0. Read PT2_CRC_ERR (register CNT1) to clear.	0b0: Flag not asserted 0b1: Flag asserted

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BITFIELD	BITS	DESCRIPTION	DECODE
PT1_CRC_ERR_FLAG	0	PT1 CRC Error flag Asserted when PT1 CRC error count > 0. Read PT1_CRC_ERR (register CNT0) to clear.	0b0: Flag not asserted 0b1: Flag asserted

CNT0 (0x1D82)

BIT	7	6	5	4	3	2	1	0
Field	PT1_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_CRC_ERR	7:0	Number of PT1 CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.	0xXXXXXXXX: Number of video pixel CRC errors detected

CNT1 (0x1D83)

BIT	7	6	5	4	3	2	1	0
Field	PT2_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PT2_CRC_ERR	7:0	Number of PT2 CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.	0xXXXXXXXX: Number of video pixel CRC errors detected

CNT2 (0x1D84)

BIT	7	6	5	4	3	2	1	0
Field	RBB_CC_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
RBB_CC_CRC_ERR	7:0	Number of RBB CC CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.	0xXXXXXXXX: Number of video pixel CRC errors detected

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CNT3 (0x1D85)

BIT	7	6	5	4	3	2	1	0
Field	SPI_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_CRC_ERR	7:0	Number of SPI CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.	0xXXXXXXXX: Number of video pixel CRC errors detected

CNT4 (0x1D86)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_CRC_ERR	7:0	Number of GPIO CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.	0xXXXXXXXX: Number of video pixel CRC errors detected

CNT5 (0x1D87)

BIT	7	6	5	4	3	2	1	0
Field	AHDCP_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
AHDCP_CRC_ERR	7:0	Number of AHDCP CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.	0xXXXXXXXX: Number of video pixel CRC errors detected

CNT6 (0x1D88)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_X_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

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BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_X_CRC_ERR	7:0	Number of AUDIO X CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.	0xXXXXXXXX: Number of video pixel CRC errors detected

CNT7 (0x1D89)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_Y_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_Y_CRC_ERR	7:0	Number of AUDIO Y CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.	0xXXXXXXXX: Number of video pixel CRC errors detected

FRONTTOP_30 (0x2326)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	CROSS_Y	–	CROSS_X
Reset	–	–	–	–	–	0b1	–	0b0
Access Type	–	–	–	–	–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_Y	2	Video Pipe Y output source select.	0b0: Route video source Pipe X to video output Pipe Y (X→Y) 0b1: Route video source Pipe Y to video output Pipe Y (Y→Y)
CROSS_X	0	Video Pipe X output source select.	0b0: Route video source Pipe X to video output Pipe X (X→X) 0b1: Route video source Pipe Y to video output Pipe X (Y→X)

GMSL1_2 (0x2402)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	SSEN	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SSEN	5	Enables Spread Spectrum	0b0: Spread spectrum disabled 0b1: Spread spectrum enabled

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GMSL1_4 (0x2404)*

BIT	7	6	5	4	3	2	1	0
Field	SEREN	CLINKEN	PRBSEN	AUDIO_EN	–	–	REVCCEN	FWDCCEN
Reset	0b1	0b0	0b0	0b0	–	–	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SEREN	7	Enables Serialization	0b0: Disable serialization 0b1: Enable serialization
CLINKEN	6	Enables Configuration Link	0b0: Disable configuration link 0b1: Enable configuration link
PRBSEN	5	Enables PRBS Test (in HIBW mode set PRBS_TYPE = 0).	0b0: Set device normal operation 0b1: Enable PRBS test
AUDIO_EN	4	Enables Forward Audio-Channel	0b0: Disable 0b1: Enable
REVCCEN	1	Enables reverse control-channel from deserializer	0b0: Disable reverse control-channel receiver 0b1: Enable reverse control-channel receiver
FWDCCEN	0	Enables forward control-channel to deserializer	0b0: Disable forward control-channel transmitter 0b1: Enable forward control-channel transmitter

GMSL1_5 (0x2405)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	PRBS_LEN[1:0]		–	–	–	–
Reset	–	–	0b00		–	–	–	–
Access Type	–	–	Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_LEN	5:4	PRBS Test Length	0b00: Continuous 0b01: 167.1Mbits 0b10: 9.83Mbits 0b11: 1341.5Mbits

GMSL1_7 (0x2407)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	HIBW	BWS	–	DRS	HVEN	–	PXL_CRC
Reset	0b0	0b0	0b0	–	0b0	0b0	–	0b0
Access Type		Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HIBW	6	Enables High-Bandwidth Mode	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS = 0)
BWS	5	Selects Bus-Width	0b0: Set bus width for 22-/24-bit bus, 24-/27-bit mode (depending on HIBW setting) 0b1: Set bus width for 30-bit bus (32-bit mode)

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BITFIELD	BITS	DESCRIPTION	DECODE
DRS	3	Selects Data-Rate	0b0: Use normal data-rate output 0b1: Use 1/2 rate-data output (for use with low-data rates)
HVEN	2	Enables HS/VS Encoding	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel CRC Type	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

GMSL1_D (0x240D)*

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ACK	–	–	–	–	LOC_CC_PT_EN[2:0]		
Reset	0b0	–	–	–	–	0b001		
Access Type	Write, Read	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	I^2C-to-I^2C slave generates local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available
LOC_CC_PT_EN	2:0	Enables GMSL1 Link A connection to CC/PT1/PT2 pins	0b0: Disable GMSL1 Link A connection 0b1: Enable GMSL1 Link A connection

GMSL1_F (0x240F)*

BIT	7	6	5	4	3	2	1	0
Field	CNTL_IN_EN[4:0]					GPO_RX_EN	–	SET_GPO
Reset	0b01111					0b1	–	0b0
Access Type	Write, Read					Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_IN_EN	7:3	Enables CNTL input for CNTL 0, 1, 2, 3, and 4. CNTL input enables for GMSL1 A and B are ORed together.	0bXXXX0: CNTL 0 input disabled 0bXXXX1: CNTL 0 input enabled 0bXXX0X: CNTL 1 input disabled 0bXXX1X: CNTL 1 input enabled 0bXX0XX: CNTL 2 input disabled 0bXX1XX: CNTL 2 input enabled 0bX0XXX: CNTL 3 input disabled 0bX1XXX: CNTL 3 input enabled 0b0XXXX: CNTL 4 input disabled 0b1XXXX: CNTL 4 input enabled
GPO_RX_EN	2	Enables receiving GPO signal from reverse channel	0b0: GPO signal reception disabled 0b1: GPO signal reception enabled
SET_GPO	0	Sets GPO output high or low	0b0: Set GPO output low 0b1: Set GPO output high

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GMSL1_11 (0x2411)*

BIT	7	6	5	4	3	2	1	0
Field	ERRG_RATE2[1:0]		ERRG_TYPE2[1:0]		ERRG_CNT2[1:0]		ERRG_PER2	ERRG_EN_G1
Reset	0b00		0b00		0b00		0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_RATE2	7:6	Average Error-Generation Rate	0b00: Every 2560 bits 0b01: Every 40960 bits 0b10: Every 655360 bit 0b11: Every 10485760 bits
ERRG_TYPE2	5:4	Type of Generated Errors	0b00: Single bit 0b01: Two 8b/10b symbols 0b10: Three 8b/10b symbols 0b11: Four 8b/10b symbols
ERRG_CNT2	3:2	Number of Generated Errors	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_PER2	1	Enables Periodic Error-Generation	0b0: Periodic error generator disabled 0b1: Periodic error generator enabled
ERRG_EN_G1	0	Enables error generator, auto clears when done	0b0: Disable error generator 0b1: Enable error generator

GMSL1_12 (0x2412)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	CNTL_IN_ORD[2:0]		
Reset	–	–	–	–	–	0x000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_IN_ORD	2:0	Internal CNTL_IN order from CNTL4 to CNTL0	0x0: 4,3,2,1,0 0x1: 3,2,1,0,4 0x2: 2,1,0,4,3 0x3: 1,0,4,3,2 0x4: 0,1,2,3,4 0x5: 1,2,3,4,0 0x6: 2,3,4,0,1 0x7: 3,4,0,1,2

GMSL1_13 (0x2413)*

BIT	7	6	5	4	3	2	1	0
Field	NO_REM_MST	ALLOW_PKTCC	–	RSVD	RSVD	RSVD	–	–
Reset	0b0	0b0	–	0b0	0b0	0b0	–	–
Access Type	Write, Read	Write, Read	–				–	–

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BITFIELD	BITS	DESCRIPTION	DECODE
NO_REM_MST	7	No Remote Master Indicator Set to 1 to indicate that there is no I²C master on remote side This (local) chip should ignore any I²C packet initiation (start condition) from remote side.	0b0: Do not ignore I²C packet initiation from remote master 0b1: Ignore I²C packet initiation from remote master
ALLOW_PKTCC	6	Allows Packet Control Channel Set this bit to 1 before turning on the packet-based control channel.	0b0: Do not allow packet control channel 0b1: Allow packet control channel

GMSL1_14 (0x2414)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	I2C_TIMED_OUT2	CC_WBLOCK_LOST	REV_BIT_LOCK	CC_WBLOCK	REM_CCLOCK
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TIMED_OUT2	4	I²C Channel Timed Out	0b0: I²C channel not timed out 0b1: I²C channel timed out
CC_WBLOCK_LOST	3	Word-Boundary Lock Lost	0b0: Word-boundary lock not lost 0b1: Word-boundary lock lost
REV_BIT_LOCK	2	Reverse-Channel Bit Locked	0b0: Reverse-channel bit not locked 0b1: Reverse-channel bit locked
CC_WBLOCK	1	Control-Channel Word Boundary Lock	0b0: Control-channel word boundary not locked 0b1: Control-channel word boundary locked
REM_CCLOCK	0	Remote-Control Channel Locked	0b0: Remote-control channel not locked 0b1: Remote-control channel locked

GMSL1_15 (0x2415)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SEL_VESA	SEL_RGB888
Reset	–	–	–	–	–	–	0b1	0b1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SEL_VESA	1	VESA or OLDI mapping selection	0b0: OLDI mapping 0b1: VESA mapping
SEL_RGB888	0	Select RGB888 bit mapping	0b0: Non-RGB888 0b1: RGB888

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GMSL1_16 (0x2416)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_ERR	–	–	–	–	–	–
Reset	–	0b0	–	–	–	–	–	–
Access Type	–	Read Only	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	6	Maximum Retransmission Error Flag Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

GMSL1_18 (0x241C)

BIT	7	6	5	4	3	2	1	0
Field	CC_I2C_RETR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_I2C_RETR_CNT	7:0	I^2C Packet Retransmit Count	0xXX: Number of I^2C packets retransmitted

GMSL1_19 (0x241D)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	Packet-Based Control-Channel CRC Error Counter	0xXX: Number of control-channel CRC errors

GMSL1_39 (0x2438)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS24_I	CROSS24_F	CROSS24[4:0]				
Reset	–	0b0	0b0	0b11000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS24_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS24_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS24	4:0	Maps incoming bit position set by this field to the outgoing bit position 24	0bXXXXX: Incoming bit position

GMSL1_3A (0x2439)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS25_I	CROSS25_F	CROSS25[4:0]				
Reset	–	0b0	0b0	0b11001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS25_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS25_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS25	4:0	Maps incoming bit position set by this field to the outgoing bit position 25	0bXXXXX: Incoming bit position

GMSL1_3B (0x243A)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS26_I	CROSS26_F	CROSS26[4:0]				
Reset	–	0b0	0b0	0b11010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS26_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS26_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS26	4:0	Maps incoming bit position set by this field to the outgoing bit position 26	0bXXXXX: Incoming bit position

GMSL1_3C (0x243B)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS27_I	CROSS27_F	CROSS27[4:0]				
Reset	–	0b0	0b0	0b11011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS27_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS27_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS27	4:0	Maps incoming bit position set by this field to the outgoing bit position 27	0bXXXXX: Incoming bit position

GMSL1_3D (0x243C)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
Reset	–	0b0	0b0	0b11100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS28_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS28_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS28	4:0	Maps incoming bit position set by this field to the outgoing bit position 28	0bXXXXX: Incoming bit position

GMSL1_3E (0x243D)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
Reset	–	0b0	0b0	0b11101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS29_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS29_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS29	4:0	Maps incoming bit position set by this field to the outgoing bit position 29	0bXXXXX: Incoming bit position

GMSL1_3F (0x243E)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS30_I	CROSS30_F	CROSS30[4:0]				
Reset	–	0b0	0b0	0b11110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS30_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS30_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS30	4:0	Maps incoming bit position set by this field to the outgoing bit position 30	0bXXXXX: Incoming bit position

GMSL1_42 (0x2442)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	MAX_RT_EN	I2C_RT_EN	RSVD	RSVD	GPO_EN
Reset	0b01		–	0b1	0b1	0b0	0b1	0b1
Access Type			–	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_EN	4	Enables Maximum Retransmission Limit	0b0: Maximum retransmission limit disabled 0b1: Maximum retransmission limit enabled
I2C_RT_EN	3	Enables I^2C Retransmission	0b0: I^2C retransmission disabled 0b1: I^2C retransmission enabled
GPO_EN	0	Enables General-Purpose Output Pin	0b0: GPO pin disabled 0b1: GPO pin enabled

GMSL1_4D (0x244D)*

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse-Channel High Immunity Mode	0b0: Reverse channel high immunity mode disabled 0b1: Reverse channel high immunity mode enabled

GMSL1_66 (0x2466)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		PRBS_TYPE	REV_FAST	DIS_DE	–	–	–
Reset	0b01		0b1	0b0	0b0	–	–	–
Access Type			Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_TYPE	5	PRBS type select (in HIBW mode set PRBS_TYPE = 0) PRBS_TYPE setting must match in serializer and deserializer.	0b0: GMSL1 legacy style PRBS test 0b1: Non-GMSL1 legacy style PRBS test
REV_FAST	4	Reverse-Channel Fast Mode	0b0: Disable reverse-channel fast mode 0b1: Enable reverse-channel fast mode

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BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DE	3	Disables processing separate HS and DE signals	0b0: Enable processing separate HS and DE signals 0b1: Disable processing separate HS and DE signals

GMSL1_67 (0x2467)*

BIT	7	6	5	4	3	2	1	0
Field	CNTL_TRIG[1:0]		AUTO_CLINK	DE_RGB888_DBL	–	DBL_ALIGN_TO[2:0]		
Reset	0b00		0b0	0b0	–	0b111		
Access Type	Write, Read		Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_TRIG	7:6	Selects CNTL trigger of encoded packets in high-bandwidth mode	0b00: No trigger 0b01: Always trigger 0b10: Trigger when DE is low 0b11: Trigger when HS is low
AUTO_CLINK	5	Automatic control of configuration link	0b0: Enable configuration link only when CLINKEN = 1 and SEREN = 0 0b1: Automatically enable configuration link when SEREN = 1 and PCLKDET = 0
DE_RGB888_DBL	4	Selects DBL DE RGB888 processing mode	0b0: Regular DBL DE processing while mapping input 0b1: Process DBL DE for RGB888 mode while mapping input
DBL_ALIGN_TO	2:0	Double Alignment Mode	0b000: Align at each rising edge of HS and turn off the alignment after HS is low 0b001: Reserved 0b010: Force align 0b011: Force align 0b100: Align at each rising edge of HS 0b101: Align at each rising edge of DE 0b110: Reserved 0b111: DBL-DBL mode with no alignment

GMSL1_68 (0x2468)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			RSVD[1:0]		CC_CRC_LENGTH[1:0]	
Reset	–	0b001			0b10		0b01	
Access Type	–						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_LENGTH	1:0	Control-Channel CRC Length	0b00: 1-bit 0b01: 5-bit 0b10: 8-bit 0b11: Reserved

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GMSL1_99 (0x2499)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RSVD	REV_FILT_EN	RSVD	ALIGN_INFO	–	–
Reset	0b0	–	0b0	0b0	0b1	0b1	–	–
Access Type		–		Write, Read		Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
REV_FILT_EN	4	Enables Reverse-Channel Digital Filter	0b0: Disable filter 0b1: Enable filter
ALIGN_INFO	2	Sends alignment information through CNTL signals in HBIW mode	0b0: Do not send alignment information 0b1: Send alignment information

GMSL1_9A (0x249A)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		PKTCC_EN	RSVD[1:0]		RSVD
Reset	–	–	0b01		0b0	0b00		0b0
Access Type	–	–			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKTCC_EN	3	Enables packet-based control-channel mode When enabled and the user enters sleep mode, it is required to reduce MST_TO.	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode

GMSL1_C8 (0x24C8)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	I2C_ACK_RECVED	I2C_ACK_ACKED	–	–	–	–
Reset	–	0b0	0b0	0b0	–	–	–	–
Access Type	–		Read Only	Read Only	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_ACK_RECVED	5	Remote Acknowledge Received	0b0: Remote acknowledge not received 0b1: Remote acknowledge received
I2C_ACK_ACKED	4	Remote ACK Acknowledged	0b0: Remote ACK not acknowledged 0b1: Remote ACK acknowledged

G1_I2C_0 (0x2575)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	G1_SLV_SH[1:0]		–	G1_SLV_TO[2:0]		
Reset	–	–	0b10		–	0b101		
Access Type	–	–	Write, Read		–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
G1_SLV_SH	5:4	GMSL1 I²C-to-I²C slave setup and hold time setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I²C slave. Set this according to the I²C speed mode: Fast-Mode Plus = 00 Fast-Mode = 01 Standard-Mode = 10	0b00: Fast-Mode Plus 0b01: Fast-Mode 0b10: Standard-Mode 0b11: Reserved
G1_SLV_TO	2:0	GMSL1 I²C-to-I²C slave timeout setting. Internal GMSL1 I²C slave times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

G1_I2C_1 (0x2576)*

BIT	7	6	5	4	3	2	1	0
Field	–	G1_MST_BT[2:0]			–	G1_MST_TO[2:0]		
Reset	–	0x5			–	0b110		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
G1_MST_BT	6:4	I²C-to-I²C master bit rate setting, configures the I²C bit rate used by the internal I²C master (in the device on remote side from the external I²C master) Set this according to the I²C speed mode.	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
G1_MST_TO	2:0	GMSL1 I²C-to-I²C master timeout setting Internal GMSL1 I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the local device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

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G1_I2C_2 (0x2577)*

BIT	7	6	5	4	3	2	1	0
Field	G1_SRC_A[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
G1_SRC_A	7:1	GMSL1 I²C Address Translator Source A When I²C device address matches G1_SRC_A, internal I²C master (on remote side) replaces the device address with G1_DST_A.	0xXX: Most significant byte of VS delay

G1_I2C_3 (0x2578)*

BIT	7	6	5	4	3	2	1	0
Field	G1_DST_A[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
G1_DST_A	7:1	GMSL1 I²C Address Translator Destination A See the description of G1_SRC_A	0xXX: Middle significant byte of VS delay

G1_I2C_4 (0x2579)*

BIT	7	6	5	4	3	2	1	0
Field	G1_SRC_B[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
G1_SRC_B	7:1	GMSL1 I²C Address Translator Source B When I²C device address matches G1_SRC_B, internal I²C master (on remote side) replaces the device address with G1_DST_B.	0xXX: Least significant byte of VS delay

G1_I2C_5 (0x257A)*

BIT	7	6	5	4	3	2	1	0
Field	G1_DST_B[6:0]							–
Reset	0x00							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
G1_DST_B	7:1	GMSL1 I²C Address Translator Destination B See the description of G1_SRC_B	0xXX: Most significant byte of VS delay

GMSL1_2 (0x2602)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	SSEN	–	–	–	–	–
Reset	–	–	0b0	–	–	–	–	–
Access Type	–	–	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SSEN	5	Enables Spread Spectrum	0b0: Spread spectrum disabled 0b1: Spread spectrum enabled

GMSL1_4 (0x2604)*

BIT	7	6	5	4	3	2	1	0
Field	SEREN	CLINKEN	PRBSEN	AUDIO_EN	–	–	REVCCEN	FWDCCEN
Reset	0b1	0b0	0b0	0b0	–	–	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SEREN	7	Enables Serialization	0b0: Disable serialization 0b1: Enable serialization
CLINKEN	6	Enables Configuration Link	0b0: Disable configuration link 0b1: Enable configuration link
PRBSEN	5	Enables PRBS Test (in HIBW mode set PRBS_TYPE = 0)	0b0: Set device normal operation 0b1: Enable PRBS test
AUDIO_EN	4	Enables Forward Audio Channel	0b0: Disable 0b1: Enable
REVCCEN	1	Enables reverse-control channel from deserializer	0b0: Disable reverse-control channel receiver 0b1: Enable reverse-control channel receiver
FWDCCEN	0	Enables forward-control channel to deserializer	0b0: Disable forward-control channel transmitter 0b1: Enable forward-control channel transmitter

GMSL1_5 (0x2605)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	PRBS_LEN[1:0]		–	–	–	–
Reset	–	–	0b00		–	–	–	–
Access Type	–	–	Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_LEN	5:4	PRBS Test Length	0b00: Continuous 0b01: 167.1Mbits 0b10: 9.83Mbits 0b11: 1341.5Mbits

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GMSL1_7 (0x2607)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	HIBW	BWS	–	DRS	HVEN	–	PXL_CRC
Reset	0b0	0b0	0b0	–	0b0	0b0	–	0b0
Access Type		Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HIBW	6	Enables High-Bandwidth Mode	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS = 0)
BWS	5	Selects Bus-Width	0b0: Set bus width for 22-/24-bit bus, 24-/27-bit mode (depending on HIBW setting) 0b1: Set bus width for 30-bit bus (32-bit mode)
DRS	3	Selects Data-Rate	0b0: Use normal data rate output 0b1: Use 1/2 rate data output (for use with low data rates)
HVEN	2	Enables HS/VS Encoding	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel CRC Type	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

GMSL1_D (0x260D)*

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ACK	–	–	–	–	LOC_CC_PT_EN[2:0]		
Reset	0b0	–	–	–	–	0b001		
Access Type	Write, Read	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	I^2C-to-I^2C slave generates local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available
LOC_CC_PT_EN	2:0	Enables GMSL1 Link B connection to CC/PT1/PT2 pins	0b0: Disable GMSL1 Link B connection 0b1: Enable GMSL1 Link B connection

GMSL1_F (0x260F)*

BIT	7	6	5	4	3	2	1	0
Field	CNTL_IN_EN[4:0]					GPO_RX_EN	–	SET_GPO
Reset	0b01111					0b1	–	0b0
Access Type	Write, Read					Write, Read	–	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_IN_EN	7:3	CNTL Input Enable for CNTL 0, 1, 2, 3, and 4. CNTL input enables for GMSL1 A and B are ORed together.	0bXXXX0: CNTL 0 input disabled 0bXXXX1: CNTL 0 input enabled 0bXXX0X: CNTL 1 input disabled 0bXXX1X: CNTL 1 input enabled 0bXX0XX: CNTL 2 input disabled 0bXX1XX: CNTL 2 input enabled 0bX0XXX: CNTL 3 input disabled 0bX1XXX: CNTL 3 input enabled 0b0XXXX: CNTL 4 input disabled 0b1XXXX: CNTL 4 input enabled
GPO_RX_EN	2	Enables receiving GPO signal from reverse channel	0b0: GPO signal reception disabled 0b1: GPO signal reception enabled
SET_GPO	0	Sets GPO output high or low	0b0: Set GPO output low 0b1: Set GPO output high

GMSL1_11 (0x2611)*

BIT	7	6	5	4	3	2	1	0
Field	ERRG_RATE2[1:0]		ERRG_TYPE2[1:0]		ERRG_CNT2[1:0]		ERRG_PER2	ERRG_EN_G1
Reset	0b00		0b00		0b00		0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_RATE2	7:6	Average Error-Generation Rate	0b00: Every 2,560 bits 0b01: Every 40,960 bits 0b10: Every 655,360 bit 0b11: Every 10,485,760 bits
ERRG_TYPE2	5:4	Type of generated errors	0b00: Single bit 0b01: Two 8b/10b symbols 0b10: Three 8b/10b symbols 0b11: Four 8b/10b symbols
ERRG_CNT2	3:2	Number of generated errors	0b00: Continuous 0b01: 16 0b10: 128 0b11: 1024
ERRG_PER2	1	Enables Periodic Error Generation	0b0: Periodic error generator disabled 0b1: Periodic error generator enabled
ERRG_EN_G1	0	Enables error generator	0b0: Disable error generator 0b1: Enable error generator

GMSL1_12 (0x2612)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	CNTL_IN_ORD[2:0]		
Reset	–	–	–	–	–	0x000		
Access Type	–	–	–	–	–	Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_IN_ORD	2:0	Internal CNTL_IN Order from CNTL4 to CNTL0	0x0: 4,3,2,1,0 0x1: 3,2,1,0,4 0x2: 2,1,0,4,3 0x3: 1,0,4,3,2 0x4: 0,1,2,3,4 0x5: 1,2,3,4,0 0x6: 2,3,4,0,1 0x7: 3,4,0,1,2

GMSL1_13 (0x2613)*

BIT	7	6	5	4	3	2	1	0
Field	NO_REM_MST	ALLOW_PKTCC	–	RSVD	RSVD	RSVD	–	–
Reset	0b0	0b0	–	0b0	0b0	0b0	–	–
Access Type	Write, Read	Write, Read	–				–	–

BITFIELD	BITS	DESCRIPTION	DECODE
NO_REM_MST	7	No Remote Master Indicator Set to 1 to indicate that there is no I²C master on remote side This (local) chip should ignore any I²C packet initiation (start condition) from remote side.	0b0: Do not ignore I²C packet initiation from remote master 0b1: Ignore I²C packet initiation from remote master
ALLOW_PKTCC	6	Allows Packet Control Channel Set this bit to 1 before turning on the packet-based control channel.	0b0: Do not allow packet control channel 0b1: Allow packet control channel

GMSL1_14 (0x2614)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	I2C_TIMED_OUT2	CC_WBLOCK_LOST	REV_BIT_LOCK	CC_WBLOCK	REM_CCLOCK
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TIMED_OUT2	4	I²C Channel Timed Out	0b0: I²C channel not timed out 0b1: I²C channel timed out
CC_WBLOCK_LOST	3	Word-Boundary Lock Lost	0b0: Word-boundary lock not lost 0b1: Word-boundary lock lost
REV_BIT_LOCK	2	Reverse-Channel Bit Locked	0b0: Reverse-channel bit not locked 0b1: Reverse-channel bit locked
CC_WBLOCK	1	Control-Channel Word Boundary Lock	0b0: Control-channel word boundary not locked 0b1: Control-channel word boundary locked
REM_CCLOCK	0	Remote-Control Channel Locked	0b0: Remote control channel not locked 0b1: Remote control channel locked

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GMSL1_15 (0x2615)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SEL_VESA	SEL_RGB888
Reset	–	–	–	–	–	–	0b1	0b1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SEL_VESA	1	VESA or OLDI mapping selection	0b0: OLDI mapping 0b1: VESA mapping
SEL_RGB888	0	Selects RGB888 bit mapping	0b0: Non-RGB888 0b1: RGB888

GMSL1_16 (0x2616)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_ERR	–	–	–	–	–	–
Reset	–	0b0	–	–	–	–	–	–
Access Type	–	Read Only	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	6	Maximum Retransmission Error Flag Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

GMSL1_18 (0x261C)

BIT	7	6	5	4	3	2	1	0
Field	CC_I2C_RETR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_I2C_RETR_CNT	7:0	I^2C Packet Retransmit Count	0xXX: Number of I^2C packets retransmitted

GMSL1_19 (0x261D)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	Packet-Based Control-Channel CRC Error Counter	0xXX: Number of control-channel CRC errors

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GMSL1_39 (0x2638)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS24_I	CROSS24_F	CROSS24[4:0]				
Reset	–	0b0	0b0	0b11000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS24_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS24_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS24	4:0	Maps incoming bit position set by this field to the outgoing bit position 24	0bXXXXX: Incoming bit position

GMSL1_3A (0x2639)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS25_I	CROSS25_F	CROSS25[4:0]				
Reset	–	0b0	0b0	0b11001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS25_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS25_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS25	4:0	Maps incoming bit position set by this field to the outgoing bit position 25	0bXXXXX: Incoming bit position

GMSL1_3B (0x263A)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS26_I	CROSS26_F	CROSS26[4:0]				
Reset	–	0b0	0b0	0b11010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS26_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS26_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS26	4:0	Maps incoming bit position set by this field to the outgoing bit position 26	0bXXXXX: Incoming bit position

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GMSL1_3C (0x263B)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS27_I	CROSS27_F	CROSS27[4:0]				
Reset	–	0b0	0b0	0b11011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS27_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS27_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS27	4:0	Maps incoming bit position set by this field to the outgoing bit position 27	0bXXXXX: Incoming bit position

GMSL1_3D (0x263C)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
Reset	–	0b0	0b0	0b11100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS28_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS28_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS28	4:0	Maps incoming bit position set by this field to the outgoing bit position 28	0bXXXXX: Incoming bit position

GMSL1_3E (0x263D)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
Reset	–	0b0	0b0	0b11101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS29_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS29_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS29	4:0	Maps incoming bit position set by this field to the outgoing bit position 29	0bXXXXX: Incoming bit position

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GMSL1_3F (0x263E)*

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS30_I	CROSS30_F	CROSS30[4:0]				
Reset	–	0b0	0b0	0b11110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS30_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS30_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS30	4:0	Maps incoming bit position set by this field to the outgoing bit position 30	0bXXXXX: Incoming bit position

GMSL1_42 (0x2642)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	MAX_RT_EN	I2C_RT_EN	RSVD	RSVD	GPO_EN
Reset	0b01		–	0b1	0b1	0b0	0b1	0b1
Access Type			–	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_EN	4	Enables Maximum Retransmission Limit	0b0: Maximum retransmission limit disabled 0b1: Maximum retransmission limit enabled
I2C_RT_EN	3	Enables I^2C Retransmission	0b0: I^2C retransmission disabled 0b1: I^2C retransmission enabled
GPO_EN	0	Enables General-Purpose Output Pin	0b0: GPO pin disabled 0b1: GPO pin enabled

GMSL1_4D (0x264D)*

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse-Channel High-Immunity Mode	0b0: Reverse-channel high-immunity mode disabled 0b1: Reverse-channel high-immunity mode enabled

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GMSL1_66 (0x2666)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		PRBS_TYPE	REV_FAST	DIS_DE	–	–	–
Reset	0b01		0b1	0b0	0b0	–	–	–
Access Type			Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_TYPE	5	PRBS type select (in HIBW mode set PRBS_TYPE = 0) PRBS_TYPE setting must match in serializer and deserializer.	0b0: GMSL legacy style PRBS test 0b1: Non-GMSL1 legacy style PRBS test
REV_FAST	4	Reverse-Channel Fast Mode	0b0: Disable reverse-channel fast mode 0b1: Enable reverse-channel fast mode
DIS_DE	3	Disables processing separate HS and DE signals	0b0: Enable processing separate HS and DE signals 0b1: Disable processing separate HS and DE signals

GMSL1_67 (0x2667)*

BIT	7	6	5	4	3	2	1	0
Field	CNTL_TRIG[1:0]		AUTO_CLINK	DE_RGB888_DBL	–	DBL_ALIGN_TO[2:0]		
Reset	0b00		0b0	0b0	–	0b111		
Access Type	Write, Read		Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_TRIG	7:6	Selects CNTL trigger of encoded packets in high-bandwidth mode	0b00: No trigger 0b01: Always trigger 0b10: Trigger when DE is low 0b11: Trigger when HS is low
AUTO_CLINK	5	Automatic Control of Configuration Link	0b0: Enable configuration link only when CLINKEN = 1 and SEREN = 0 0b1: Automatically enable configuration link when SEREN = 1 and PCLKDET = 0
DE_RGB888_DBL	4	Selects DBL DE RGB888 processing mode	0b0: Regular DBL DE processing while mapping input 0b1: Process DBL DE for RGB888 mode while mapping input
DBL_ALIGN_TO	2:0	Double Alignment Mode	0b000: Align at each rising edge of HS and turn off the alignment after HS is low (MAX9286) 0b001: Reserved 0b010: Force align 0b011: Force align 0b100: Align at each rising edge of HS 0b101: Align at each rising edge of DE 0b110: Reserved 0b111: DBL-DBL mode with no alignment

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GMSL1_68 (0x2668)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			RSVD[1:0]		CC_CRC_LENGTH[1:0]	
Reset	–	0b001			0b10		0b01	
Access Type	–						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_LENGTH	1:0	Control-Channel CRC Length	0b00: 1-bit 0b01: 5-bit 0b10: 8-bit 0b11: Reserved

GMSL1_99 (0x2699)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RSVD	REV_FILT_EN	RSVD	ALIGN_INFO	–	–
Reset	0b0	–	0b0	0b0	0b1	0b1	–	–
Access Type		–		Write, Read		Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
REV_FILT_EN	4	Enables Reverse-Channel Digital Filter	0b0: Disable filter 0b1: Enable filter
ALIGN_INFO	2	Sends alignment information through CNTL signals in HBIW mode	0b0: Do not send alignment information 0b1: Send alignment information

GMSL1_9A (0x269A)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		PKTCC_EN	RSVD[1:0]		RSVD
Reset	–	–	0b01		0b0	0b00		0b0
Access Type	–	–			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKTCC_EN	3	Enables packet-based control-channel mode, when enabled and the user enters sleep mode. Required to reduce MST_TO.	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode

GMSL1_C8 (0x26C8)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	I2C_ACK_RECVED	I2C_ACK_ACKED	–	–	–	–
Reset	–	0b0	0b0	0b0	–	–	–	–
Access Type	–		Read Only	Read Only	–	–	–	–

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BITFIELD	BITS	DESCRIPTION	DECODE
I2C_ACK_RECVED	5	Remote Acknowledge Received	0b0: Remote acknowledge not received 0b1: Remote acknowledge received
I2C_ACK_ACKED	4	Remote ACK Acknowledged	0b0: Remote acknowledge not acknowledged 0b1: Remote ACK acknowledged

PROFILE_CTRL_0 (0x3300)*

Provides profile selection and execution control

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PROF_SEL_A[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PROF_SEL_A	4:0	Profile select for PHY A to use when profile execution is triggered.	0: Use the settings defined in the Profile Cfg Phy A (PROF_CFG_A) register 1-31: Preselected profile

PROFILE_CTRL_1 (0x3301)*

Provides profile selection and execution control

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PROF_SEL_B[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PROF_SEL_B	4:0	Profile select for PHY B to use when profile execution is triggered.	0: Use the settings defined in the Profile Cfg Phy B (PROF_CFG_B) register 1-31: Preselected profile

PROFILE_CTRL_2 (0x3302)

Provides profile selection and execution control

BIT	7	6	5	4	3	2	1	0
Field	PROF_STATUS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PROF_STATUS	7:0	Profile status

PROFILE_CTRL_3 (0x3303)*

Provides profile selection and execution control

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BIT	7	6	5	4	3	2	1	0
Field	EXEC_PROF	EXEC_PROF_ERR	–	DIS_LINK_RST	–	–	PROF_IN_USE_B	PROF_IN_USE_A
Reset	0b0	0b0	–	0b0	–	–	0b0	0b0
Access Type	Write, Read	Write, Read	–	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EXEC_PROF	7	Triggers profile setup execution. It must only be set after the profile selections/ configurations have been setup for all PHYs. This bit is cleared after the profile setup completes.	0b0: Profile setup activity idle 0b1: Profile setup activity in progress
EXEC_PROF_ERR	6	Status indicating an error occurred during profile execution.	0b0: No error during profile execution 0b1: Error occurred during profile execution
DIS_LINK_RST	4	Disable the link reset that normally occurs after a profile execution.	0b0: Link reset enabled 0b1: Link reset disabled
PROF_IN_USE_B	1	Indicates that a profile is used to setup registers for PHY B	0b0: No profile-based register setup in use 0b1: Profile-based register setup in use
PROF_IN_USE_A	0	Indicates that a profile is used to setup registers for PHY A	0b0: No profile-base register setup in use 0b1: Profile-based register setup in use

PROFILE_CFG_A_0 (0x3308)*

Provides profile configuration for PHY A

BIT	7	6	5	4	3	2	1	0
Field	TX_LRATE_A	GMSL_MODE_A	SYNC_POL_A	HV_ENC_A	HIM_EN_A	LINE_FAULT_A	GMSL1_WORD_A[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_LRATE_A	7	Selects desired link rate for GMSL2 mode. The GMSL2 link rate for both link A and link B must be the same. The highest selected link rate of the two will be used.	0b0: 3Gbps 0b1: 6Gbps
GMSL_MODE_A	6	Selects GMSL1 or GMSL2 mode for link	0b0: GMSL2 mode 0b1: GMSL1 mode
SYNC_POL_A	5	Inverts HS and VS	0b0: Do not invert HS/VS 0b1: Invert HS/VS
HV_ENC_A	4	Enables HS and VS encoding	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
HIM_EN_A	3	Enables GMSL1 high immunity mode	0b0: Disable high immunity 0b1: Enable high immunity
LINE_FAULT_A	2	Enables all line faults	0b0: Disable line faults 0b1: Enable line faults
GMSL1_WORD_A	1:0	GMSL1 data rate selection	0b00: 27-bit, high bandwidth 0b01: 32-bit, 4-channel, high data rate 0b10: 32-bit, 4-channel, low data rate 0b11: 24-bit, 3-channel

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PROFILE_CFG_A_1 (0x3309)*

Provides profile configuration for PHY A

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PT_I2CUART_2_A[1:0]		PT_I2CUART_1_A[1:0]	
Reset	–	–	–	–	0b00		0b00	
Access Type	–	–	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PT_I2CUART_2_A	3:2	Selects the I2C/UART pass-through 2 mode. The mode of operation differs based on link mode, GMSL1/GMSL2.	0b00: GMSL1 - Main control channel GMSL2 - Main control channel 0b01: GMSL1 - Main control channel GMSL2 - Main control channel tunneled 0b10: GMSL1 - Pass-through GMSL2 - Pass-through 0b11: Reserved
PT_I2CUART_1_A	1:0	Selects the I2C/UART pass-through 1 mode. The mode of operation differs based on link mode, GMSL1/GMSL2.	0b00: GMSL1 - Main control channel GMSL2 - Main control channel 0b01: GMSL1 - Main control channel GMSL2 - Main control channel tunneled 0b10: GMSL1 - Pass-through GMSL2 - Pass-through 0b11: Reserved

PROFILE_CFG_B_0 (0x330C)*

Provides profile configuration for PHY B

BIT	7	6	5	4	3	2	1	0
Field	TX_LRATE_B	GMSL_MODE_B	SYNC_POL_B	HV_ENC_B	HIM_EN_B	LINE_FAULT_B	GMSL1_WORD_B[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_LRATE_B	7	Selects desired link rate for GMSL2 mode. The GMSL2 link rate for both link A and link B must be the same. The highest selected link rate of the two will be used.	0b0: 3Gbps 0b1: 6Gbps
GMSL_MODE_B	6	Selects GMSL1 or GMSL2 mode for link	0b0: GMSL2 mode 0b1: GMSL1 mode
SYNC_POL_B	5	Inverts HS and VS	0b0: Do not invert HS/VS 0b1: Invert HS/VS
HV_ENC_B	4	Enables HS and VS encoding	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
HIM_EN_B	3	Enables GMSL1 high immunity mode	0b0: Disable high immunity 0b1: Enable high immunity
LINE_FAULT_B	2	Enables all line faults	0b0: Disable line faults 0b1: Enable line faults
GMSL1_WORD_B	1:0	GMSL1 data rate selection	0b00: 27-bit, high bandwidth 0b01: 32-bit, 4-channel, high data rate 0b10: 32-bit, 4-channel, low data rate 0b11: 24-bit, 3-channel

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PROFILE_CFG_B_1 (0x330D)*

Provides profile configuration for PHY B

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PT_I2CUART_2_B[1:0]		PT_I2CUART_1_B[1:0]	
Reset	–	–	–	–	0b00		0b00	
Access Type	–	–	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PT_I2CUART_2_B	3:2	Selects the I^{2}C/UART pass-through 2 mode. The mode of operation differs based on link mode, GMSL1/GMSL2.	0b00: GMSL1 - Main control channel GMSL2 - Main control channel 0b01: GMSL1 - Main control channel GMSL2 - Main control channel tunneled 0b10: GMSL1 - Pass-through GMSL2 - Pass-through 0b11: Reserved
PT_I2CUART_1_B	1:0	Selects the I^{2}C/UART pass-through 1 mode. The mode of operation differs based on link mode, GMSL1/GMSL2.	0b00: GMSL1 - Main control channel GMSL2 - Main control channel 0b01: GMSL1 - Main control channel GMSL2 - Main control channel tunneled 0b10: GMSL1 - Pass-through GMSL2 - Pass-through 0b11: Reserved

PHY_CTRL0_B0 (0x6064, 0x6164)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PHYC_AEQ_TIME_2G7[5:0]					
Reset	–	–	0x0D					
Access Type	–	–	Write, Read					

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BITFIELD	BITS	DESCRIPTION
PHYC_AEQ_TIME_2G7	5:0	Set RLMS Adaptation time constants to be used for DPRX HBR Link training: 0 – no delay 1 – 100µs 2 – 200µs 3 – 300µs 4 – 400µs 5 – 3ms 6 - 4ms 7 – 6ms 8 – 7ms 9 – 10ms 10 – 11ms 12 – 12ms 13 – 14ms 14 – 15ms 15 – 16ms 16 – 30ms 17 – 31ms 18 – 32ms 19 – 46ms 20 – 47ms 21 – 48ms 22 – 62ms 23 – 63ms 24 – 64ms 25 – 128ms 26 – 192ms 27 – 256ms 28 – 384ms

PHY_CTRL0_B1 (0x6065, 0x6165)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	PHYC_AEQ_TIME_5G4[5:0]					
Reset	–	0b0	0x0D					
Access Type	–		Write, Read					

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BITFIELD	BITS	DESCRIPTION
PHYC_AEQ_TIME_5G4	5:0	Set RLMS Adaptation time constants to be used for DPRX HBR2 Link training: 0 – no delay 1 – 100µs 2 – 200µs 3 – 300µs 4 – 400µs 5 – 3ms 6 - 4ms 7 – 6ms 8 – 7ms 9 – 10ms 10 – 11ms 12 – 12ms 13 – 14ms 14 – 15ms 15 – 16ms 16 – 30ms 17 – 31ms 18 – 32ms 19 – 46ms 20 – 47ms 21 – 48ms 22 – 62ms 23 – 63ms 24 – 64ms 25 – 128ms 26 – 192ms 27 – 256ms 28 – 384ms

PHY_CTRL0_B3 (0x6067, 0x6167)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PHYC_AEQ_TIME_8G1[5:0]					
Reset	–	–	0x0D					
Access Type	–	–	Write, Read					

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BITFIELD	BITS	DESCRIPTION
PHYC_AEQ_TIME_8G1	5:0	Set RLMS Adaptation time constants to be used for DPRX HBR3 Link training: 0 – no delay 1 – 100µs 2 – 200µs 3 – 300µs 4 – 400µs 5 – 3ms 6 - 4ms 7 – 6ms 8 – 7ms 9 – 10ms 10 – 11ms 12 – 12ms 13 – 14ms 14 – 15ms 15 – 16ms 16 – 30ms 17 – 31ms 18 – 32ms 19 – 46ms 20 – 47ms 21 – 48ms 22 – 62ms 23 – 63ms 24 – 64ms 25 – 128ms 26 – 192ms 27 – 256ms 28 – 384ms

DPRX_TRN_STATUS0 (0x6418)

Provide status of DP Rx core link training operations.

BIT	7	6	5	4	3	2	1	0
Field	DPRX_LINK_RATE[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DPRX_LINK_RATE	7:0	DP link rate that is set in the link bandwidth DPCD register (0x0100).	06: 1.62Gbps (not supported) 0A: 2.7Gbps 14: 5.4Gbps 1E: 8.1Gbps XX: All other values reserved

DPRX_TRN_STATUS1 (0x6419)

Provide status of DP Rx core link training operations.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DPRX_LANE_CNT[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Read Only				

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BITFIELD	BITS	DESCRIPTION	DECODE
DPRX_LANE_CNT	4:0	DP lane count that is set in the lane count DPCD register (0x0101).	01: Lane 0 active 02: Lanes 0, 1 active XX: All other values reserved

DPRX_TRN_STATUS2 (0x641A)

Provide status of DP Rx core link training operations.

BIT	7	6	5	4	3	2	1	0
Field	DPRX_TRAIN_STATE[3:0]				–	DPRX_TRAIN_PAT[2:0]		
Reset	0x0				–	0b000		
Access Type	Read Only				–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
DPRX_TRAIN_STATE	7:4	DP Rx core training state. Each bit represents the competion of a training phase for all acitve lanes (active lane status ANDed together).	4: Clock recovery done 5: Channel equalization done 6: Symbol lock 7: Lane alignment
DPRX_TRAIN_PAT	2:0	DP training pattern that is set in the link training pattern DPCD register (0x102).	000: No training (normal data) 001: Training pattern 1 010: Training pattern 2 011: Training pattern 3 111: Training pattern 4 xxx: All other values reserved

DPRX_TRN_STATUS3 (0x641B)

Provide status of DP Rx core link training operations.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SYM_LOCK_COMB	LQP_TRN_NOCLR	TPS4_DESCRAM_ON
Reset	–	–	–	–	–	0b1	0b0	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SYM_LOCK_COMB	2	Combines all active lanes for symbol lock detection (AND). This is normal operation. Individual (not combined) symbol lock detection is used for link quality compliance testing.	0b0: No combining of active lane symbol lock 0b1: Combined active lane symbol lock
LQP_TRN_NOCLR	1	Disables clearing of link quality error counters (SER count) when training status changes. Reading the error counters will continue to clear them.	0b0: Error counters cleared both by reading and training status change 0b1: Error counters only cleared by reading
TPS4_DESCRAM_ON	0	Automatically enables descrambling when training pattern 4 (TPS4) is set. Normally, descrambling is set independently of the training pattern setting.	0b0: Descrambling set independent of training pattern 0b1: Descrambling automatically set when TPS4 set

EDP_VIDEO_CTRL0 (0x6420)*

Provides control of video out of EDP Rx.

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BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	–	–	VIDEO_OUT_EN[1:0]	
Reset	0b0	0b0	0b0	–	–	–	0b0	
Access Type				–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_OUT_EN	1:0	Enables video out for each of the four possible video streams. Each bit controls a corresponding video stream. Bit 0 → Pipe X Bit 1 → Pipe Y	0b0: Stream disabled 0b1: Stream enabled

EDP_VIDEO_CTRL2 (0x6422)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	EDID_ROM_EN	EDID_RAM_EN	EDID_READ_ONLY
Reset	–	–	–	–	0x0	0b1	0b0	0b1
Access Type	–	–	–	–		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EDID_ROM_EN	2	Connect EDID ROM to I²C-over-AUX	0b0: Disable EDID ROM See EDID_RAM_EN 0b1: EDID ROM is accessible through DisplayPort I²C-over-AUX using EDID_DEV_ADDR
EDID_RAM_EN	1	Connect EDID memory to I²C-over-AUX (automatically disconnected from I²C-over-AUX when EDID_ROM_EN = 1)	0b0: Disable EDID RAM EDID RAM can be accessed through CC using CC EDID address 0b1: If EDID_ROM_EN = 0, then EDID RAM memory is accessible through DisplayPort I²C-over-AUX using EDID_DEV_ADDR
EDID_READ_ONLY	0	Make EDID RAM read-only when it is connected to I²C-over-AUX	0b0: EDID is writable 0b1: EDID is read-only

EDP_GEN_INT_ST0 (0x6430)

Interrupt status for general EDP operations. This register consolidates all the EDP Rx interrupt sources allowing easier identification of the interrupt source.

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	DP_RLMS1_INT	DP_RLMS0_INT	DPRX_INT	–	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	–	0b0	0b0
Access Type			Read Only	Read Only	Read Only	–		

BITFIELD	BITS	DESCRIPTION	DECODE
DP_RLMS1_INT	5	DP RLMS lane 1 interrupt status. This is a pass-through interrupt from the DP RLMS for lane 1.	0b0: DP RLMS1 interrupt inactive 0b1: DP RLMS1 interrupt active

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BITFIELD	BITS	DESCRIPTION	DECODE
DP_RLMS0_INT	4	DP RLMS lane 0 interrupt status. This is a pass-through interrupt from the DP RLMS for lane 0.	0b0: DP RLMS0 interrupt inactive 0b1: DP RLMS0 interrupt active
DPRX_INT	3	DPRX interrupt status. This is a pass-through interrupt from the DPRX core.	0b0: DPRX interrupt inactive 0b1: DPRX interrupt active

EDP_GEN_INT_ST3 (0x6433)

Interrupt status for general EDP operations. This register consolidates all the EDP Rx interrupt sources allowing easier identification of the interrupt source.

BIT	7	6	5	4	3	2	1	0
Field	RSVD	APB_ERR_M0_IST	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type		Write 1 to Clear, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
APB_ERR_M0_IST	6	APB master 0 error interrupt status. This sticky status indicates that an error occurred on an APB transaction for master 0 (it is actually a pass-through of APB_STATUS_ERR_M0—0x64C6, bit 0). To clear, write 1 to this bit or write 1 to APB_STATUS_ERR_M0 bit 0.

EDP_GEN_INT_EN0 (0x6434)

Interrupt enable for each interrupt status bit defined in the EDP General Interrupt Status registers (EDP_GEN_INT_STx). Each bit enables (ANDed with) the corresponding bit of the EDP General Interrupt Status with the results ORed to create the level-sensitive EDP Rx Interrupt signal.

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	DP_RLMS1_IEN	DP_RLMS0_IEN	DPRX_IEN	–	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	–	0b0	0b0
Access Type			Write, Read	Write, Read	Write, Read	–		

BITFIELD	BITS	DESCRIPTION
DP_RLMS1_IEN	5	DP RLMS lane 1 interrupt enable. This enables a DP RLMS lane 1 interrupt event to assert the level-sensitive EDP Rx interrupt signal.
DP_RLMS0_IEN	4	DP RLMS lane 0 interrupt enable. This enables a DP RLMS lane 0 interrupt event to assert the level-sensitive EDP Rx interrupt signal.
DPRX_IEN	3	DPRX interrupt enable. This enables a DPRX interrupt event to assert the level-sensitive EDP Rx interrupt signal.

EDP_GEN_INT_EN3 (0x6437)

Interrupt enable for each interrupt status bit defined in the EDP General Interrupt Status registers (EDP_GEN_INT_STx). Each bit enables (ANDed with) the corresponding bit of the EDP General Interrupt Status with the results ORed to create the level-sensitive EDP Rx Interrupt signal.

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BIT	7	6	5	4	3	2	1	0
Field	RSVD	APB_ERR_M0_IEN	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type		Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
APB_ERR_M0_IEN	6	APB master 0 error interrupt enable. This enables a APB master 0 error event to assert the level-sensitive EDP Rx interrupt signal.

HPD_CTRL0 (0x6444)

Provides control for the hotplug detect (HPD) output.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HPD_IRQ_HO_DIS	HPD_IRQ	HPD_ST	HPD_MODE
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ_HO_DIS	3	HPD IRQ hold-off disable	
HPD_IRQ	2	HPD-IRQ assertion (normal and manual mode). Setting this bit causes HPD to be deasserted (low) for the time set by HPD_IRQ_TIME (assuming HPD would otherwise be active). This bit is self-clearing after the HPD IRQ time expires.	0b0: HPD normal/manual setting 0b1: HPD inactive (low)
HPD_ST	1	Controls HPD output state when in manual operation. It has no effect when operating in normal mode.	0b0: HPD inactive (low) 0b1: HPD active (high)
HPD_MODE	0	HPD mode selects between normal and manual HPD operation In normal mode, HPD is controlled by the DPRX core or the HPD_IRQ control. In manual mode, HPD is controlled by HPD_ST or the HPD_IRQ control.	0b0: Normal operation 0b1: Manual operation

HPD_CTRL1 (0x6445)

Provides control for the hotplug detect (HPD) output.

BIT	7	6	5	4	3	2	1	0
Field	HPD_IRQ_TIME[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ_TIME	7:0	HPD IRQ time sets the HPD IRQ active (low) time in 10µs (+1/-0) when activated by the HPD_IRQ control.	N: HPD is low for N*10µs (+1/-0) when HPD_IRQ is asserted

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HPD_CTRL2 (0x6446)

Provides control for the hotplug detect (HPD) output.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	HPD_IRQ_HO	HOT_PLUG_DET	DPRX_HPD
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ_HO	2	HPD IRQ hold-off	
HOT_PLUG_DET	1	HPD output. This is the result of the combination of all the HPD sources (DPRX_HPD, HPD_IRQ, HPD_ST). This signal is forced inactive when OSN calibration is active.	0b0: HPD output inactive (low) 0b1: HPD output active (high)
DPRX_HPD	0	HPD from DPRX core. This is the normal HPD control when not in manual mode (HPD_MODE) and HPD_IRQ inactive.	0b0: DPRX HPD inactive 0b1: DPRX HPD active

HPD_CTRL3 (0x6447)

Provides control for the hotplug detect (HPD) output.

BIT	7	6	5	4	3	2	1	0
Field	HPD_IRQ_HO_TIME[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HPD_IRQ_HO_TIME	7:0	HPD IRQ hold-off (high) time in 10µs (+1/-0)

APB_CTRL_M0_B0 (0x64C0)

Provides control for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	APB_TO_SEL_M0[2:0]		
Reset	–	–	–	–	–	0b001		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
APB_TO_SEL_M0	2:0	Timeout selection for APB master 0 access. This is a watchdog timer that returns the APB to the idle state when a timeout occurs to prevent bus hangups.	0b000: No timeout 0b001: 5-6µs 0b010: 10-11µs 0b011: 100µs 0b100: 500µs 0b101: 1ms 0b110: 2ms 0b111: 4ms

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APB_CTRL_M0_B2 (0x64C2)

Provides status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_ERR_IEN_M0[7:0]							
Reset	0x00							
Access Type	Write 1 to Clear, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
APB_ERR_IEN_M0	7:0	Interrupt enable for APB master 0 error interrupt APB_ERR_M0_IST (EDP_GEN_INT_ST3, bit 6). This register enables the individual APB error events (see APB_STATUS_ERR_M0) for generating the interrupt.	0x0: Slave error interrupt enable 0x1: Premature termination interrupt enable 0x2: Timeout interrupt enable 0x3: Decode error (no register at address) interrupt enable 0x4: Invalid access (non-byte write when byte only writes allowed) interrupt enable 0x5: Reserved for future use 0x6: Reserved for future use 0x7: Blocking (non-blocking mode) interrupt enable

APB_STATUS_M0_B0 (0x64C4)

Provides status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_STATUS_M0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
APB_STATUS_M0	7:0	Bus cycle status for APB master 0. This register holds the status returned at the end of each bus cycle. Reading this register immediately after an APB master 0 cycle returns the status of the bus cycle. Bit zero indicates the normal APB slave error with bits [7:1] indicating the cause when an error occurs.	0x0: Slave error 0x1: Premature termination 0x2: Timeout 0x3: Decode error (no register at address) 0x4: Invalid access (non-byte write when byte only writes allowed) 0x5: Reserved for future use 0x6: Reserved for future use 0x7: Blocking (non-blocking mode)

APB_STATUS_M0_B2 (0x64C6)

Provides status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_STATUS_ERR_M0[7:0]							
Reset	0x00							
Access Type	Write 1 to Clear, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
APB_STATUS_ERR_M0	7:0	Captured (sticky) status for first errored APB master 0 cycle since last clear. Write 1 to each bit to clear. Bit 0 is used as interrupt status (APB_ERR_M0_IST) and is also cleared when that interrupt bit is written to 1 (cleared). Individual events are enabled for causing the interrupt by APB_ERR_IEN_M0.	0x0: Slave error 0x1: Premature termination 0x2: Timeout 0x3: Decode error (no register at address) 0x4: Invalid access (non-byte write when byte only writes allowed) 0x5: Reserved for future use 0x6: Reserved for future use 0x7: Blocking (non-blocking mode)

APB_ADRCTL_ERR_M0_B0 (0x64C8)

Provides address/control error status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_ADR_ERR_M0_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
APB_ADR_ERR_M0_L	7:0	Captured address low (bits [7:0]) for first errored APB master 0 bus cycle since last error status clear (see APB_STATUS_ERR_M0).

APB_ADRCTL_ERR_M0_B1 (0x64C9)

Provides address/control error status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_ADR_ERR_M0_H[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
APB_ADR_ERR_M0_H	7:0	Captured address high (bits [15:8]) for first errored APB master 0 bus cycle since last error status clear (see APB_STATUS_ERR_M0).

APB_ADRCTL_ERR_M0_B2 (0x64CA)

Provides address/control error status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	APB_WR_ERR_M0	APB_STB_ERR_M0[3:0]			
Reset	–	–	–	0b0	0b0			
Access Type	–	–	–	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION
APB_WR_ERR_M0	4	Captured write cycle indicator for first errored APB master 0 bus cycle since last error status clear (see APB_STATUS_ERR_M0).

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BITFIELD	BITS	DESCRIPTION
APB_STB_ERR_M0	3:0	Captured write strobes for first errored APB master 0 bus cycle since last error status clear (see APB_STATUS_ERR_M0).

DPCD_CTRL_M0_B0 (0x64D0)

Provides control for DPCD access via APB master 0.

BIT	7	6	5	4	3	2	1	0
Field	DPCD_ADDR_HI_M0_L[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DPCD_ADDR_HI_M0_L	7:0	Lower 8 bits [7:0] of the DPCD high address (bits [19:8]) used for DPCD register access via APB master 0. The DPCD registers exist within the DPRX_LINK block at the display port define 20-bit address space. A defined 256-byte portal (DPCD) within the local address space provides the lower 8 bits of the DPCD address.

DPCD_CTRL_M0_B1 (0x64D1)

Provides control for DPCD access via APB master 0.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DPCD_ADDR_HI_M0_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DPCD_ADDR_HI_M0_H	3:0	Upper 4 bits [3:0] of the DPCD high address (bits [19:8]) used for DPCD register access via APB master 0. The DPCD registers exist within the DPRX_LINK block at the display port define 20-bit address space. A defined 256-byte portal (DPCD) within the local address space provides the lower 8 bits of the DPCD address.

DPCD_CTRL_M0_B2 (0x64D2)

Provides control for DPCD access via APB master 0.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DPCD_RD CLR_EN_M 0	DPCD_APB _NOBLK_M 0
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_RDCLR_EN_M0	1	Enables clearing of DPCD register bits when reading registers via APB master 0 that are defined as read-to-clear. When read-clearing is disabled, read-to-clear DPCD registers read via APB master 0 will not be cleared.	0b0: Clearing on read is disabled 0b1: Clearing on read is enabled
DPCD_APB_NOBLK_M0	0	Enable APB non-blocking mode. This allows APB master 0 accesses to the DPCD registers to terminate the bus cycle immediately with blocked status if the access would be delayed due to a competing AUX cycles. Retrying the access is necessary if the bus status indicates the access was blocked.	0b0: APB blocking mode active 0b1: APB non-blocking mode active

LINK_ENABLE (0x7000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LINK_ENABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_ENABLE	0	Enables DPRX for operation. When enabled, HPD is active (normally high, except when HPD IRQ is activated) and the DPRX is operational. When disabled, HPD is held low and the DPRX is disabled.	0b0: DPRX disabled - HPD = 0 0b1: DPRX enabled - HPD active

AUX_CLOCK_DIV_B0 (0x7004)

BIT	7	6	5	4	3	2	1	0
Field	AUX_CLOCK_DIV_L[7:0]							
Reset	0x96							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
AUX_CLOCK_DIV_L	7:0	AUX clock divider bits 7-0. This integer value is the divisor used to generate the internal 1Mhz AUX clock from the APB interface clock.

AUX_CLOCK_DIV_B1 (0x7005)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AUX_CLOCK_DIV_H[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

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BITFIELD	BITS	DESCRIPTION
AUX_CLOCK_DIV_H	1:0	AUX clock divider bits 9-8. This integer value is the divisor used to generate the internal 1Mhz AUX clock from the APB interface clock.

MISC_CONFIG_B0 (0x7018)

BIT	7	6	5	4	3	2	1	0
Field	DISABLE_AUX_FILTER	ALPM_ENABLE	EDP_FUNCTION_ENABLE	MAX_DOWNSPREAD_CONFIG	BRANCH_SUPPORT_ENABLE	DISABLE_INACTIVE_COUNT	DEFER_LONG_I2C	MSA_DELAY_BYPASS
Reset	0b0	0b0	0b0	0b1	0b0	0b1	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DISABLE_AUX_FILTER	7	Disables the AUX data glitch filtering used to improve the robustness of the AUX channel.	0b0: Normal operation 0b1: AUX glitch filtering disabled
ALPM_ENABLE	6	Enables Embedded DisplayPort (eDP) power management functionality. This functionality may be set independently from EDP_FUNCTION_ENABLE.	0b0: eDP PM capabilities disabled 0b1: eDP PM capabilities enabled
EDP_FUNCTION_ENABLE	5	Enables Embedded DisplayPort (eDP) functionality and reports eDP capability in DPCD.	0b0: eDP capabilities disabled 0b1: eDP capabilities enabled
MAX_DOWNSPREAD_CONFIG	4	Enables downspread capability reported in DPCD. Must be enabled for compliance with DisplayPort 1.2a and above.	0b0: Downspread capability disabled 0b1: Downspread capability enabled
BRANCH_SUPPORT_ENABLE	3	Enables DisplayPort branch device capabilities.	0b0: Branch device capabilities disabled 0b1: Branch device capabilities enabled
DISABLE_INACTIVE_COUNT	2	Disables the inactive video counter (timer) that will assert HPD-IRQ if the counter expires without detecting video or the NO_VIDEO signal.	0b0: Inactive counter enabled 0b1: Inactive counter disabled
DEFER_LONG_I2C	1	Enables sending DEFER response to I^2C-over-AUX transactions that will exceed the normal AUX timeout.	0b0: Respond with partial ACK 0b1: Respond with DEFER
MSA_DELAY_BYPASS	0	Disables validating Main Stream Attribute (MSA) values by checking for 2 consecutive matching values. Values are received each vertical blank period.	0: Normal MSA validation 1: MSA validation disabled

MISC_CONFIG_B1 (0x7019)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MSO_FUNCTION_EN	DISABLE_LINE_RESET	MST_FUNCTION_ENABLE
Reset	–	–	–	–	–	0b0	0b0	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
MSO_FUNCTION_EN	2	Enables a special multi-stream functionality for single-stream transport (multi-SST operation - MSO) mode and reports MSO capability in DPCD.	0b0: MSO capablity disabled 0b1: MSO capability enabled
DISABLE_LINE_RESET	1	Disables normal resetting video FIFOs after each line of received video data. This is primarily a debug feature.	0b0: Normal operation - line reset enabled 0b1: Line reset disabled
MST_FUNCTION_ENABLE	0	Enables multi-stream transport (MST) functionality and reports MST capability in DPCD.	0b0: MST capablity disabled 0b1: MST capability enabled

DISPLAYPORT_VERSION (0x701C)

BIT	7	6	5	4	3	2	1	0
Field	DP_VERSION[7:0]							
Reset	0x14							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DP_VERSION	7:0	DisplayPort revision level reported through DPCD. This can be used to inform a DP source of the level of compatibility desired.	0x10: DP version 1.0 supported 0x11: DP version 1.1 supported 0x12: DP version 1.2 supported 0x13: DP version 1.3 supported 0x14: DP version 1.4 supported ----: Other values reserved

REQUEST_ERROR_COUNT (0x7024)

BIT	7	6	5	4	3	2	1	0
Field	REQUEST_ERROR_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REQUEST_ERROR_COUNT	7:0	Provides a running total of errors detected on inbound AUX Channel requests. When an improperly formatted AUX request is made, the internal AUX controller will flag an error and increment this register by 1. The value of this register is cleared by writing a 0 to the REQUEST_COUNT_L register.

REQUEST_COUNT_L (0x7028)

BIT	7	6	5	4	3	2	1	0
Field	REQUEST_COUNT_L[7:0]							
Reset	0x00							
Access Type	Write 1 to Clear, Read							

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BITFIELD	BITS	DESCRIPTION
REQUEST_COUNT_L	7:0	AUX request count bits 7-0. Provides a running total of the number of AUX Request transactions received (native AUX and I²C-over-AUX). This register is updated after the request is received and before the reply is generated. The value of this register is cleared when a 0 is written to this register.

REQUEST_COUNT_H (0x7029)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	REQUEST_COUNT_H[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION
REQUEST_COUNT_H	1:0	AUX request count bits 9-8. Provides a running total of the number of AUX Request transactions received (native AUX and I²C-over-AUX). This register is updated after the request is received and before the reply is generated. The value of this register is cleared when a 0 is written to REQUEST_COUNT_L.

HPD_INTERRUPT (0x702C)

Instructs the receiver core to assert an interrupt to the transmitter using the HPD signal. An HPD pulse of 750µs is generated by this function. When the HDCP functionality is included in the core, this register can also be used to force a CP_IRQ event.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RSVD	HPD_IRQ
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–		Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ	0	Assert an interrupt to the transmitter using the hotplug detect (HPD) signal. The HPD output from the DPRX core is held low for approximately 750µs. This bit is self-clearing. See HPD_CTRL register for manual HPD conrol that may supercede this control.	0b0: Normal operation 0b1: HPD-IRQ asserted

HPD_INTERRUPT_MASK (0x702D)

Masks the specified interrupt sources from asserting the HPD_IRQ signal. When set to a 1, the specified interrupt source is masked. This register resets to all 0s at power up resulting in all interrupt sources being enabled.

BIT	7	6	5	4	3	2	1	0
Field	–	HPD_INTERRUPT_MASK[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

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BITFIELD	BITS	DESCRIPTION
HPD_INTERRUPT_MASK	6:0	Disables individual sources that can cause assertion of a hotplug detect interrupt event (HPD IRQ). Setting a bit to 1 masks (disables) the corresponding HPD IRQ source.

LANE_REMAP_B0 (0x7030)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		REMAP_LANE_1[1:0]		REMAP_LANE_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type					Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
REMAP_LANE_1	3:2	Specifies which physical lane number (0-3) will be mapped to the internal lane 1. The REMAP_ENABLE bit must be set for the mapping to be active.	0b00: Map physical lane 0 to logical lane 1 0b01: Map physical lane 1 to logical lane 1 0b10: Map physical lane 2 to logical lane 1 0b11: Map physical lane 3 to logical lane 1
REMAP_LANE_0	1:0	Specifies which physical lane number (0-3) will be mapped to the internal lane 0. The REMAP_ENABLE bit must be set for the mapping to be active.	0b00: Map physical lane 0 to logical lane 0 0b01: Map physical lane 1 to logical lane 0 0b10: Map physical lane 2 to logical lane 0 0b11: Map physical lane 3 to logical lane 0

LANE_REMAP_B1 (0x7031)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	REMAP_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REMAP_ENABLE	0	Remap enable. This bit must be set to enable the physical to logical lane remapping defined in the REMAP_LANE_0/1/2/3.	0b0: Lane remapping disabled 0b1: Lane remapping enabled

LANE_REMAP_B2 (0x7032)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	RSVD	INVERT_LANE_1	INVERT_LANE_0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
INVERT_LANE_1	1	Inverts the state of all bits received on lane 1.	0b0: Lane bits not inverted 0b1: Lane bits inverted
INVERT_LANE_0	0	Inverts the state of all bits received on lane 0.	0b0: Lane bits not inverted 0b1: Lane bits inverted

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VIDEO_INPUT_RESET (0x7054)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LINK_RESET	VIDEO_INPUT_RESET
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RESET	1	Resets the link clock domain logic. No internal control registers will be modified by this reset. This bit is self-clearing.	0b0: Normal operation 0b1: Link reset
VIDEO_INPUT_RESET	0	Resets the video capture clock domain logic. No internal control registers will be modified by this reset. This bit is self-clearing.	0b0: Normal operation 0b1: Video reset

EDP_IGNORE_MSA (0x7058)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	EDP_IGNORE_MSA
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EDP_IGNORE_MSA	0	When configured for eDP support, a 1 indicates that the Sink device does not require the video mode timing parameters to be transmitted through the MSA. This bit can only be set to a 1 when the receiver core display timing generator (DTG) is configured for DMA mode operation. The value of this bit is mirrored in the DPCD at offset 0x0007 bit 6.	0b0: MSA parameters required 0b1: MSA parameters not required (eDP support only)

MAX_LANE_COUNT (0x7070)

BIT	7	6	5	4	3	2	1	0
Field	MAX_LANE_COUNT[7:0]							
Reset	0x02							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
MAX_LANE_COUNT	7:0	The maximum number of lanes supported is specified through this register. This register should be set before the LINK_ENABLE register bit is set to a 1. The value of this register is reported to the DisplayPort source device through the DPCD register set at address 0x0002. Valid values are 1 and 2. All other values are reserved and must not be used.	0x01: 1 lane supported (lane 0) 0x02: 2 lanes supported (lane 0, 1) 0xXX: All other values reserved

MAX_LINK_RATE (0x7074)

BIT	7	6	5	4	3	2	1	0
Field	MAX_LINK_RATE[7:0]							
Reset	0x1E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_LINK_RATE	7:0	The maximum link rate supported is specified through this register. This register should be set before the LINK_ENABLE register bit is set to 1. The value of this register is reported to the DisplayPort source device through the DPCD register set at address 0x0001.	0x0A: 2.7Gbps 0x14: 5.4Gbps 0x1E: 8.1Gbps 0xXX: All other values reserved

LOCAL_EDID_VIDEO (0x7084)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOCAL_EDID_VIDEO
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOCAL_EDID_VIDEO	0	Enable local EDID support	0b0: no local EDID support 0b1: local EDID support

AUX_RD_INTERVAL (0x70A0)

BIT	7	6	5	4	3	2	1	0
Field	–	AUX_RD_INTERVAL[6:0]						
Reset	–	0x4						
Access Type	–	Write, Read						

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BITFIELD	BITS	DESCRIPTION	DECODE
AUX_RD_INTERVAL	6:0	Read interval during link training for link status and adjust requests. The value of this register is directly mapped from the values of the DPCD register at offset 0x000E. Only values listed below are valid.	0x00: 100µs for clock recovery, 400µs for channel equalization 0x01: 4ms 0x02: 8ms 0x03: 12ms 0x04: 16ms Other: Reserved

I2C_SPEED_CAPABILITY (0x70A4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	I2C_SPEED_CAPABILITY[5:0]					
Reset	–	–	0b111000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_SPEED_CAPABILITY	5:0	Configuration indicating the supported speed map on the external I^2C bus. Set the corresponding bit to a 1 to indicate support for an I^2C bus operating at that speed.	0b000001: 1Kbps 0b000010: 5Kbps 0b000100: 10Kbps 0b001000: 100Kbps 0b010000: 400Kbps 0b100000: 1Mbps

I2C_SCL_TO_SEL (0x70A5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	I2C_SCL_TO_SEL[3:0]			
Reset	–	–	–	–	0x8			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_SCL_TO_SEL	3:0	Selects the timeout for the I^2C SCL signal active (low) time during an I^2C-over-AUX transaction. Upon timeout the I^2C state machine is reset aborting the transaction, allowing SCL to be inactive (high).	0x0: Timeout disabled 0x1: 2ms 0x2: 4ms 0x3: 6ms 0x4: 8ms 0x5: 10ms 0x6: 12ms 0x7: 14ms 0x8: 16ms 0x9: 18ms 0x10: 20ms 0x11: 22ms 0x12: 24ms 0x13: 26ms 0x14: 28ms 0x15: 30ms

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DPCD_LINK_BW_SET (0x7400)

BIT	7	6	5	4	3	2	1	0
Field	DPCD_LINK_BW_SET[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_LINK_BW_SET	7:0	This is the DPCD (0x0100) value for the current link rate as set by the DP source device.	0x0A: 2.7Gbps 0x14: 5.4Gbps 0x1E: 8.1Gbps 0xXX: All other values reserved

DPCD_LANE_COUNT_SET (0x7404)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DPCD_LANE_COUNT_SET[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_LANE_COUNT_SET	4:0	This is the DPCD (0x0101) value for the number of lanes in use as set by the DP source device.	0x01: Lane 0 active 0x02: Lanes 0, 1 active 0xXX: All other values reserved

DPCD_ENHANCED_FRAME_EN (0x7408)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DPCD_ENHANCED_FRAME_EN
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_ENHANCED_FRAME_EN	0	This is the DPCD value for the current training pattern as set by the DP source. These are bits 2-0 of the DPCD register TRAINING_PATTERN_SET (0x0102).	0b0: Enhanced framing disabled 0b1: Enhanced framing enabled

DPCD_TRAINING_PATTERN_SET (0x740C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DPCD_TRAINING_PATTERN_SET[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Read Only		

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BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_TRAINING_PATTERN_SET	2:0	This is the DPCD value for the current training pattern as set by the DP source. These are bits 2-0 of the DPCD register TRAINING_PATTERN_SET (0x0102).	0b000: Training pattern disabled 0b001: Training pattern 1 (TPS1) 0b010: Training pattern 2 (TPS2) 0b011: Training pattern 3 (TPS3 - HBR2) 0b111: Training pattern 4 (TPS4 - HBR3) 0b100-110: Reserved

DPCD_LINK_QUAL_PAT_SET_B0 (0x7410)

BIT	7	6	5	4	3	2	1	0
Field	–	DPCD_LINK_QUAL_LANE1_SET[2:0]			–	DPCD_LINK_QUAL_LANE0_SET[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_LINK_QUAL_LANE1_SET	6:4	This is the DPCD value for the current link quality pattern for lane 1 as set by the DP source. These are bits 2-0 of the DPCD register LINK_QUAL_LANE0_SET (0x010C).	0b000: Link quality pattern disabled 0b001: D10.2 (TPS1) 0b010: Symbol Error Rate (SER) 0b011: PBRS7 0b100: 80-bit Custom 0b101: CP2520 Pattern 1 0b110: CP2520 Pattern 2 0b111: CP2520 Pattern 3 (TPS4)
DPCD_LINK_QUAL_LANE0_SET	2:0	This is the DPCD value for the current link quality pattern for lane 0 as set by the DP source. These are bits 2-0 of the DPCD register LINK_QUAL_LANE0_SET (0x010B).	0b000: Link quality pattern disabled 0b001: D10.2 (TPS1) 0b010: Symbol Error Rate (SER) 0b011: PBRS7 0b100: 80-bit Custom 0b101: CP2520 Pattern 1 0b110: CP2520 Pattern 2 0b111: CP2520 Pattern 3 (TPS4)

DPCD_SCRAMBLING_DISABLE (0x7418)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DPCD_SCRAMBLING_DISABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_SCRAMBLING_DISABLE	0	This is the DPCD value for scrambling disable control as set by the DP source. This is bit 5 of the DPCD register TRAINING_PATTERN_SET (0x0102).	0b0: Scrambling enabled 0b1: Scrambling disabled

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DPCD_SYMBOL_ERROR_COUNT_SELECT (0x741C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DPCD_SYMBOL_ERROR_COUNT_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_SYMBOL_ERROR_COUNT_SELECT	1:0	This is the DPCD value for the current symbol error count select as set by the DP source. These are bits 7-6 of the DPCD register TRAINING_PATTERN_SET (0x0102).	0b00: Disparity errors and illegal symbol errors 0b01: Disparity errors only 0b10: Illegal symbol errors only 0b11: Reserved

DPCD_TRAINING_LANE_0_SET (0x7420)

This register reflects the current values set by the transmitter for DPCD register TRAINING_LANE2_SET (0x105). Used by the transmitter during link training to configure the receiver PHY for lane 2.

BIT	7	6	5	4	3	2	1	0
Field	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
Reset	–	–	0b0	0b00		0b0	0b00	
Access Type	–	–	Read Only	Read Only		Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_PRE_EMPHASIS_REACHED	5	This is the DPCD value for the current max pre-emphasis reached as set by the DP source (training phase 1).	0b0: Max preemphasis not reached 0b1: Max preemphasis reached
PRE_EMPHASIS_SET	4:3	This is the DPCD value for the current preemphasis as set by the DP source (training phase 2).	0b00: Preemphasis level 0 (training phase 2) 0b01: Preemphasis level 1 (training phase 2) 0b10: Preemphasis level 2 (training phase 2) 0b11: Preemphasis level 3 (training phase 2)
MAX_SWING_REACHED	2	This is the DPCD value for the current max swing reached as set by the DP source (training phase 1).	0b0: Max swing not reached 0b1: Max swing reached
VOLTAGE_SWING_SET	1:0	This is the DPCD value for the current voltage swing as set by the DP source (training phase 1).	0b00: Voltage swing level 0 (training phase 1) 0b01: Voltage swing level 1 (training phase 1) 0b10: Voltage swing level 2 (training phase 1) 0b11: Voltage swing level 3 (training phase 1)

DPCD_TRAINING_LANE_1_SET (0x7424)

This register reflects the current values set by the transmitter for DPCD register TRAINING_LANE1_SET (0x104). Used by the transmitter during link training to configure the receiver PHY for lane 1.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
Reset	–	–	0b0	0b00		0b0	0b00	
Access Type	–	–	Read Only	Read Only		Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_PRE_EMPHASIS_REACHED	5	This is the DPCD value for the current max pre-emphasis reached as set by the DP source (training phase 1).	0b0: Max preemphasis not reached 0b1: Max preemphasis reached
PRE_EMPHASIS_SET	4:3	This is the DPCD value for the current preemphasis as set by the DP source (training phase 2).	0b00: Preemphasis level 0 (training phase 2) 0b01: Preemphasis level 1 (training phase 2) 0b10: Preemphasis level 2 (training phase 2) 0b11: Preemphasis level 3 (training phase 2)
MAX_SWING_REACHED	2	This is the DPCD value for the current max swing reached as set by the DP source (training phase 1).	0b0: Max swing not reached 0b1: Max swing reached
VOLTAGE_SWING_SET	1:0	This is the DPCD value for the current voltage swing as set by the DP source (training phase 1).	0b00: Voltage swing level 0 (training phase 1) 0b01: Voltage swing level 1 (training phase 1) 0b10: Voltage swing level 2 (training phase 1) 0b11: Voltage swing level 3 (training phase 1)

DPCD_DOWNSPREAD_CONTROL (0x7430)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DPCD_DOWNSPREAD_CONTROL
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
DPCD_DOWNSPREAD_CONTROL	0	Reflects the value of DPCD register MAX_DOWNSPREAD (0x0003).

DPCD_MAIN_LINK_CHANNEL_CODING_SET (0x7434)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DPCD_MAIN_LINK_CHANNEL_CODING_SET
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
DPCD_MAIN_LINK_CHANNEL_CODING_SET	0	This register reflects the value of DPCD register MAIN_LINK_CHANNEL_CODING (0x0006).

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DPCD_SET_POWER_STATE (0x7438)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DPCD_SET_POWER_STATE[2:0]		
Reset	–	–	–	–	–	0b010		
Access Type	–	–	–	–	–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_SET_POWER_STATE	2:0	This is the DPCD (0x0600) value for the current power state as set by the DP source device.	0b001: State D0, normal operation 0b010: State D3, power-down mode 0b101: Main link to state D3, AUX block fully powered Others: Reserved

DPCD_LANE01_STATUS_B0 (0x743C)

BIT	7	6	5	4	3	2	1	0
Field	–	LANE1_SYMBOL_LOCKED	LANE1_CHANNEL_EQ_DONE	LANE1_CLOCK_RECOVERY_DONE	–	LANE0_SYMBOL_LOCKED	LANE0_CHANNEL_EQ_DONE	LANE0_CLOCK_RECOVERY_DONE
Reset	–	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE1_SYMBOL_LOCKED	6	Lane 1 symbol locked.	0b0: Symbol lock not achieved 0b1: Symbol lock achieved
LANE1_CHANNEL_EQ_DONE	5	Lane 1 channel equalization done.	0b0: Channel equalization not done 0b1: Channel equalization done
LANE1_CLOCK_RECOVERY_DONE	4	Lane 1 clock recovery done.	0b0: Clock recovery not done 0b1: Clock recovery done
LANE0_SYMBOL_LOCKED	2	Lane 0 symbol locked.	0b0: Symbol lock not achieved 0b1: Symbol lock achieved
LANE0_CHANNEL_EQ_DONE	1	Lane 0 channel equalization done.	0b0: Symbol lock not achieved 0b1: Symbol lock achieved
LANE0_CLOCK_RECOVERY_DONE	0	Lane 0 clock recovery done.	0b0: Clock recovery not done 0b1: Clock recovery done

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DPCD_LANE01_STATUS_B1 (0x743D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LANE1_LANE_ALIGNED	LANE0_LANE_ALIGNED
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE1_LANE_ALIGNED	1	Lane 1 lane aligned.	0b0: Lane not aligned 0b1: Lane aligned
LANE0_LANE_ALIGNED	0	Lane 0 lane aligned.	0b0: Lane not aligned 0b1: Lane aligned

DPCD_LANE01_STATUS_B2 (0x743E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LANE1_TRAINING_LOST	LANE0_TRAINING_LOST
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE1_TRAINING_LOST	1	Lane 1 training lost	0b0: Training not lost 0b1: Training lost
LANE0_TRAINING_LOST	0	Lane 0 training lost.	0b0: Training not lost 0b1: Training lost

LANE0_TRAINING_LOST_CAUSE (0x7454)

When each lane of the main link loses training, the cause of the training loss is recorded in this register. Only the register for active lanes on the link are valid. The contents of this register for an unused lane are unpredictable.

BIT	7	6	5	4	3	2	1	0
Field	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RATE_CHANGE	7	Link bandwidth setting change.	0b0: No link bandwidth setting change 0b1: Link bandwidth setting change
TRAINING_PATTERN_3	6	Training pattern 3 active.	0b0: Training pattern 3 not active 0b1: Training pattern 3 active
TRAINING_PATTERN_2	5	Training pattern 2 active.	0b0: Training pattern 2 not active 0b1: Training pattern 2 active

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BITFIELD	BITS	DESCRIPTION	DECODE
TRAINING_PATTERN_1	4	Training pattern 1 active.	0b0: Training pattern 1 not active 0b1: Training pattern 1 active
CLOCK_RECOVERY_LOST	3	Clock recovery lost.	0b0: Clock recovery not lost 0b1: Clock recovery lost
SYMBOL_LOCK_LOST	2	Symbol lock lost	0b0: Symbol lock not lost 0b1: Symbol lock lost
ALIGNMENT_LOST	1	Interlane alignment lost.	0b0: Alignment not lost 0b1: Alignment lost
LANE_INACTIVE	0	Lane is inactive.	0b0: Lane not inactive 0b1: Lane inactive

LANE1_TRAINING_LOST_CAUSE (0x7455)

When each lane of the main link loses training, the cause of the training loss is recorded in this register. Only the register for active lanes on the link are valid. The contents of this register for an unused lane are unpredictable.

BIT	7	6	5	4	3	2	1	0
Field	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RATE_CHANGE	7	Link bandwidth setting change.	0b0: No link bandwidth setting change 0b1: Link bandwidth setting change
TRAINING_PATTERN_3	6	Training pattern 3 active.	0b0: Training pattern 3 not active 0b1: Training pattern 3 active
TRAINING_PATTERN_2	5	Training pattern 2 active.	0b0: Training pattern 2 not active 0b1: Training pattern 2 active
TRAINING_PATTERN_1	4	Training pattern 1 active.	0b0: Training pattern 1 not active 0b1: Training pattern 1 active
CLOCK_RECOVERY_LOST	3	Clock recovery lost.	0b0: Clock recovery not lost 0b1: Clock recovery lost
SYMBOL_LOCK_LOST	2	Symbol lock lost	0b0: Symbol lock not lost 0b1: Symbol lock lost
ALIGNMENT_LOST	1	Interlane alignment lost.	0b0: Alignment not lost 0b1: Alignment lost
LANE_INACTIVE	0	Lane is inactive.	0b0: Lane not inactive 0b1: Lane inactive

I2C_SPEED_CONTROL_SELECT (0x7478)

BIT	7	6	5	4	3	2	1	0
Field	–	–	I2C_SPEED_CAPABILITY[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

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BITFIELD	BITS	DESCRIPTION	DECODE
I2C_SPEED_CAPABILITY	5:0	This is the DPCD (0x0109) value for the current I^2C speed control mask as set by the DP source device. Each bit selects an I^2C speed available to the DP source. Multiple bits may be set.	0b000001: 1Kbps 0b000010: 5Kbps 0b000100: 10Kbps 0b001000: 100Kbps 0b010000: 400Kbps 0b100000: 1Mbps

MSA_TIMING_IGNORE (0x747C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSA_TIMING_IGNORE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_TIMING_IGNORE	0	This is the DPCD (0x0107, bit 7) value for the current MSA timing parameters ignore enable as set by the DP source device.	0b0: MSA parameters normal 0b1: MSA parameters are invalid

MST_MODE_CTRL (0x748C)

This is the DPCD (0x0111) value for the current MST mode control as set by the DP source device.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	UPSTREAM_IS_SRC	UP_REQ_EN	MST_EN
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
UPSTREAM_IS_SRC	2	This is the DPCD (0x0111) value for the current MST mode control as set by the DP source device.	0b0: Upstream device is pre DP v1.2 source or branch device 0b1: Upstream device is DP source
UP_REQ_EN	1	This is the DPCD (0x0111) value for the current MST mode control as set by the DP source device.	0b0: UP_REQ message disabled 0b1: UP_REQ message enabled
MST_EN	0	This is the DPCD (0x0111) value for the current MST mode control as set by the DP source device.	0b0: SST mode 0b1: MST mode

DPCD_SER_COUNT_LANE0_B0 (0x7490)

Symbol error count lane 0.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE0_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE0_B0	7:0	Valid symbol error count bits 7-0.

DPCD_SER_COUNT_LANE0_B1 (0x7491)

Symbol error count lane 0.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE0_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE0_B1	7:0	Valid symbol error count bits 15-8.

DPCD_SER_COUNT_LANE1_B0 (0x7494)

Symbol error count lane 1.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE1_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE1_B0	7:0	Valid symbol error count bits 7-0.

DPCD_SER_COUNT_LANE1_B1 (0x7495)

Symbol error count lane 1.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE1_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE1_B1	7:0	Valid symbol error count bits 15-8.

MSA_HRES_B0 (0x7500)

Horizontal resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HRES_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
MSA_HRES_B0	7:0	MSA horizontal resolution bits 7-0.

MSA_HRES_B1 (0x7501)

Horizontal resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HRES_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HRES_B1	7:0	MSA horizontal resolution bits 15-8.

MSA_HSPOL (0x7504)

Horizontal sync polarity detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSA_HSPOL
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_HSPOL	0	Main stream attribute horizontal sync polarity.	0b0: Active high (positive) 0b1: Active low (negative)

MSA_HSWIDTH_B0 (0x7508)

Horizontal sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HSWIDTH_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HSWIDTH_B0	7:0	MSA horizontal sync width bits 7-0.

MSA_HSWIDTH_B1 (0x7509)

Horizontal sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	–	MSA_HSWIDTH_B1[6:0]						
Reset	–	0b0000000						
Access Type	–	Read Only						

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BITFIELD	BITS	DESCRIPTION
MSA_HSWIDTH_B1	6:0	MSA horizontal sync width bits 14-8.

MSA_HSTART_B0 (0x750C)

Horizontal start detected in the Main Stream Attributes (MSA). Horizontal start is the number of pixels from the leading edge of HSYNC to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HSTART_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HSTART_B0	7:0	MSA horizontal start bits 7-0.

MSA_HSTART_B1 (0x750D)

Horizontal start detected in the Main Stream Attributes (MSA). Horizontal start is the number of pixels from the leading edge of HSYNC to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HSTART_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HSTART_B1	7:0	MSA horizontal start bits 15-8.

MSA_HTOTAL_B0 (0x7510)

Horizontal total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HTOTAL_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HTOTAL_B0	7:0	MSA horizontal total bits 7-0.

MSA_HTOTAL_B1 (0x7511)

Horizontal total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HTOTAL_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
MSA_HTOTAL_B1	7:0	MSA horizontal total bits 15-8.

MSA_VRES_B0 (0x7514)

Vertical resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VRES_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VRES_B0	7:0	MSA vertical resolution bits 7-0.

MSA_VRES_B1 (0x7515)

Vertical resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VRES_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VRES_B1	7:0	MSA vertical resolution bits 15-8.

MSA_VSPOL (0x7518)

Vertical sync polarity detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSA_VSPOL
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_VSPOL	0	Main stream attribute vertical sync polarity.	0b0: Active high (positive) 0b1: Active low (negative)

MSA_VSWIDTH_B0 (0x751C)

Vertical sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VSWIDTH_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
MSA_VSWIDTH_B0	7:0	MSA vertical sync width bits 7-0.

MSA_VSWIDTH_B1 (0x751D)

Vertical sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	–	MSA_VSWIDTH_B1[6:0]						
Reset	–	0b0000000						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
MSA_VSWIDTH_B1	6:0	MSA vertical sync width bits 14-8.

MSA_VSTART_B0 (0x7520)

Vertical start detected in the Main Stream Attributes (MSA). Vertical start is the number of lines from the leading edge of VSYNC to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VSTART_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VSTART_B0	7:0	MSA vertical start bits 7-0.

MSA_VSTART_B1 (0x7521)

Vertical start detected in the Main Stream Attributes (MSA). Vertical start is the number of lines from the leading edge of VSYNC to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VSTART_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VSTART_B1	7:0	MSA vertical start bits 15-8.

MSA_VTOTAL_B0 (0x7524)

Vertical total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VTOTAL_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
MSA_VTOTAL_B0	7:0	MSA vertical total bits 7-0.

MSA_VTOTAL_B1 (0x7525)

Vertical total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VTOTAL_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VTOTAL_B1	7:0	MSA vertical total bits 15-8.

MSA_MISC0 (0x7528)

Miscellaneous 0 attributes detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_COLOR_DEPTH[2:0]			MSA_YCBCR_COLOR	MSA_DYNAMIC_RANGE	MSA_COMP_FORMAT[1:0]		MSA_CLOCKING_MODE
Reset	0b000			0b0	0b0	0b00		0b0
Access Type	Read Only			Read Only	Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_COLOR_DEPTH	7:5	MSA MISC0 color depth.	0b000: 6bpc 0b001: 8bpc 0b010: 10bpc 0b011: 12bpc 0b100: 16bpc 0b101-111: Reserved
MSA_YCBCR_COLOR	4	MSA MISC0 YCbCr color.	0b0: BT601 0b1: BT709/special case RGB
MSA_DYNAMIC_RANGE	3	MSA MISC0 dynamic range.	0b0: VESA range 0b1: CEA range
MSA_COMP_FORMAT	2:1	MSA MISC0 component format.	0b00: RGB 0b01: YCbCr 4:2:2 0b10: YCbCr 4:4:4 0b11: RGB wide gamut
MSA_CLOCKING_MODE	0	MSA MISC0 clocking mode.	0b0: Synchronous mode 0b1: Asynchronous mode

MSA_MISC1 (0x752C)

Miscellaneous 1 attributes detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	MSA_Y_ONLY	–	–	–	–	MSA_STEREO_VIDEO[1:0]		MSA_INTERLACED_EVEN
Reset	0b0	–	–	–	–	0b00		0b0
Access Type	Read Only	–	–	–	–	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_Y_ONLY	7	MSA MISC1 Y-only control.	0b0: Full color 0b1: Y-only
MSA_STEREO_VIDEO	2:1	MSA MISC1 stereo video.	0b00: No inband 3D stereo 0b01: Next frame is RIGHT EYE (progressive video) 0b10: Reserved 0b11: Next frame is LEFT EYE (progressive video)
MSA_INTERLACED_EVEN	0	MSA MISC1 interlace.	0b0: Interlaced lines per frame is odd 0b1: Interlaced lines per frame is even

MSA_MVID_B0 (0x7530)

Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_MVID_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_MVID_B0	7:0	MSA Mvid bits 7-0.

MSA_MVID_B1 (0x7531)

Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_MVID_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_MVID_B1	7:0	MSA Mvid bits 15-8.

MSA_MVID_B2 (0x7532)

Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_MVID_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
MSA_MVID_B2	7:0	MSA Mvid bits 23-16.

MSA_NVID_B0 (0x7534)

Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_NVID_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_NVID_B0	7:0	MSA Nvid bits 7-0.

MSA_NVID_B1 (0x7535)

Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_NVID_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_NVID_B1	7:0	MSA Nvid bits 15-8.

MSA_NVID_B2 (0x7536)

Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_NVID_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_NVID_B2	7:0	MSA Nvid bits 23-16.

MSA_VBID (0x7538)

VB-ID value most recently received through main link.

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	MSA_VBID_NO_VIDEO	MSA_VBID_INTERLACED	MSA_VBID_FIELD_ID	MSA_VBID_VERT_BLANK
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–				Read Only	Read Only	Read Only	Read Only

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BITFIELD	BITS	DESCRIPTION	DECODE
MSA_VBID_NO_VIDEO	3	MSA VB-ID no video stream flag.	0b0: Video stream does not exist 0b1: Video stream exists
MSA_VBID_INTERLACED	2	MSA VB-ID interlaced flag.	0b0: Progressive video 0b1: Interlaced video
MSA_VBID_FIELD_ID	1	MSA VB-ID field ID flag.	0b0: Bottom field (interlaced video) or progressive video 0b1: Top field (interlaced video)
MSA_VBID_VERT_BLANK	0	MSA VB-ID vertical blanking flag.	0b0: Vertical blank not active 0b1: Vertical blank active

MSA_VIRTUAL_SINK_SELECT (0x7540)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MSA_VIRTUAL_SINK_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_VIRTUAL_SINK_SELECT	1:0	Selects the virtual sink device for MSA value reporting.	0b00: Virtual sink 0 0b01: Virtual sink 1 0b10: Virtual sink 2 0b11: Virtual sink 3

MST_SST_PORT_SELECT (0x7900)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MST_SST_PORT_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MST_SST_PORT_SELECT	1:0	Selects one of the four target user data output ports that will receive active symbols when configured for SST mode. This register is unused when configured for MST mode.	0b00: Video out port 0 0b01: Video out port 1 0b10: Video out port 2 0b11: Video out port 3

MST_PAYLOAD_ID_0 (0x7904)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_PAYLOAD_ID_0[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
MST_PAYLOAD_ID_0	6:0	Sets the MST payload ID of the video stream for video output port 0.

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MST_PAYLOAD_ID_1 (0x7908)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_PAYLOAD_ID_1[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
MST_PAYLOAD_ID_1	6:0	Sets the MST payload ID of the video stream for video output port 1.

MST_PAYLOAD_ID_2 (0x790C)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_PAYLOAD_ID_2[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
MST_PAYLOAD_ID_2	6:0	Sets the MST payload ID of the video stream for video output port 2.

MST_PAYLOAD_ID_3 (0x7910)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_PAYLOAD_ID_3[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
MST_PAYLOAD_ID_3	6:0	Sets the MST payload ID of the video stream for video output port 3.

MST_CLEAR_PAYLOAD_ID_TABLE (0x7934)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MST_CLEAR_PAYLOAD_ID_TABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
MST_CLEAR_PAYLOAD_ID_TABLE	0	Clears MST payload table. Normally the payload allocation table is managed by the DP source through the AUX channal. This bit is self-clearing.	0b0: Normal operation 0b1: Clear payload allocation table

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MST_VS0_ENABLE (0x7A00)

Enables the functionality for virtual sink 0. This sink device is associated with video output port 0. This is the only output sink/port in SST mode.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VS_ENABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VS_ENABLE	0	Enables the MST virtual sink device 0. This also enables the single sink device for SST mode. When disabled, video operations for this virtual sink remain in the idle state.	0b0: Virtual sink disabled 0b1: Virtual sink enabled

MST_VS0_SWAP_CBCR (0x7A08)

Controls swapping of color values for the associated video output port.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SWAP_CBCR
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SWAP_CBCR	0	Swap the Cb (blue) and Cr (red) values for pixels on the video output port when set for YCbCr color space.	0b0: No swap 0b1: Swap Cb and Cr

MST_VS0_VIDEO_FIFO_OVERFLOW (0x7A10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VIDEO_FIFO_OVERFLOW
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_FIFO_OVERFLOW	0	Indicates that the internal user data FIFO in the virtual sink device has detected an overflow condition. This status is sticky and is cleared by writing it to 1.	0b0: Normal operation 0b1: Video FIFO overflow

MST_VS0_DTG_ENABLE (0x7A14)

Controls video output for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DTG_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DTG_ENABLE	0	Enables the display timing generator (DTG) in the associated virtual sink device. The DTG should be disabled when the core detects the no video pattern on the link to prevent invalid data from being presented on the output video interface. The DTG should be enabled when a valid video mode has been detected.	0b0: DTG disabled 0b1: DTG enabled

MST_VS0_DMA_VSYNC_B0 (0x7A24)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_VSYNC_PULSE_WIDTH[7:0]							
Reset	0x3F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_PULSE_WIDTH	7:0	Sets the number of video clock cycles for the DMA mode vertical sync pulse width. The video VSYNC signal will be high for the specified number of clock cycles.

MST_VS0_DMA_VSYNC_B2 (0x7A26)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_VSYNC_FRONT_PORCH_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_FRONT_PORCH_L	7:0	DMA VSYNC front porch bits 7-0. Sets the number of video clock cycles after the last pixel of active frame data before asserting the DMA mode vertical sync pulse.

MST_VS0_DMA_VSYNC_B3 (0x7A27)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_VSYNC_FRONT_PORCH_H[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_FRONT_PORCH_H	3:0	DMA VSYNC front porch bits 11-8. Sets the number of video clock cycles after the last pixel of active frame data before asserting the DMA mode vertical sync pulse.

MST_VS0_DMA_HSYNC_B0 (0x7A28)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_HSYNC_PULSE_WIDTH_L[7:0]							
Reset	0x0F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_PULSE_WIDTH_L	7:0	DMA HSYNC width bits 7-0. Sets the number of video clock cycles for the DMA mode horizontal sync pulse width. The video HSYNC signal will be high for the specified number of clock cycles.

MST_VS0_DMA_HSYNC_B1 (0x7A29)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_HSYNC_PULSE_WIDTH_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_PULSE_WIDTH_H	3:0	DMA HSYNC width bits 11-8. Sets the number of video clock cycles for the DMA mode horizontal sync pulse width. The video HSYNC signal will be high for the specified number of clock cycles.

MST_VS0_DMA_HSYNC_B2 (0x7A2A)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_HSYNC_FRONT_PORCH_L[7:0]							
Reset	0x0F							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_FRONT_PORCH_L	7:0	DMA HSYNC front porch bits 7-0. Sets the number of video clock cycles after the last pixel of active line data before asserting the DMA mode horizontal sync pulse.

MST_VS0_DMA_HSYNC_B3 (0x7A2B)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_HSYNC_FRONT_PORCH_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_FRONT_PORCH_H	3:0	DMA HSYNC front porch bits 11-8. Sets the number of video clock cycles after the last pixel of active line data before asserting the DMA mode horizontal sync pulse.

MST_VS0_RED_CRC_B0 (0x7A38)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	RED_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RED_CRC_B0	7:0	Calculated eDP CRC for red color plane bits 7-0.

MST_VS0_RED_CRC_B1 (0x7A39)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	RED_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RED_CRC_B1	7:0	Calculated eDP CRC for red color plane bits 15-8.

MST_VS0_RED_CRC_B3 (0x7A3B)

Embedded DisplayPort calculated CRC for each color plane.

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BIT	7	6	5	4	3	2	1	0
Field	CRC_UPDATED	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Read Clears All	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_UPDATED	7	Calculated eDP CRC color plane values have been updated since last read of this register. This bit is cleared on read.	0b0: Calculated CRC not updated 0b1: Calculated CRC updated

MST_VS0_GRN_BLU_CRC_B0 (0x7A3C)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	BLU_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLU_CRC_B0	7:0	Calculated eDP CRC for blue color plane bits 7-0.

MST_VS0_GRN_BLU_CRC_B1 (0x7A3D)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	BLU_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLU_CRC_B1	7:0	Calculated eDP CRC for blue color plane bits 15-8.

MST_VS0_GRN_BLU_CRC_B2 (0x7A3E)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	GRN_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GRN_CRC_B0	7:0	Calculated eDP CRC for green color plane bits 7-0.

MST_VS0_GRN_BLU_CRC_B3 (0x7A3F)

Embedded DisplayPort calculated CRC for each color plane.

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BIT	7	6	5	4	3	2	1	0
Field	GRN_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GRN_CRC_B1	7:0	Calculated eDP CRC for green color plane bits 15-8.

MST_VS0_MSA_IGNORE_HRES_B0 (0x7A40)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_HRES_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSA_IGNORE_HRES_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS0_MSA_IGNORE_HRES_B1 (0x7A41)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_HRES_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSA_IGNORE_HRES_B1	7:0	MSA horizontal resolution override bits 15-8. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixel that defines a horizontal line.

MST_VS1_ENABLE (0x7B00)

Enables the functionality for virtual sink 1. This sink device is associated with video output port 1.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VS_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VS_ENABLE	0	Enables the MST virtual sink device 1. When disabled, video operations for this virtual sink remain in the idle state.	0b0: Virtual sink disabled 0b1: Virtual sink enabled

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MST_VS1_SWAP_CBCR (0x7B08)

Controls swapping of color values for the associated video output port.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SWAP_CBCR
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SWAP_CBCR	0	Swap the Cb (blue) and Cr (red) values for pixels on the video output port when set for YCbCr color space.	0b0: No swap 0b1: Swap Cb and Cr

MST_VS1_VIDEO_FIFO_OVERFLOW (0x7B10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VIDEO_FIFO_OVERFLOW
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_FIFO_OVERFLOW	0	Indicates that the internal user data FIFO in the virtual sink device has detected an overflow condition. This status is sticky and is cleared by writing it to 1.	0b0: Normal operation 0b1: Video FIFO overflow

MST_VS1_DTG_ENABLE (0x7B14)

Controls video output for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DTG_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DTG_ENABLE	0	Enables the display timing generator (DTG) in the associated virtual sink device. The DTG should be disabled when the core detects the no video pattern on the link to prevent invalid data from being presented on the output video interface. The DTG should be enabled when a valid video mode has been detected.	0b0: DTG disabled 0b1: DTG enabled

MST_VS1_DMA_VSYNC_B0 (0x7B24)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

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BIT	7	6	5	4	3	2	1	0
Field	DMA_VSYNC_PULSE_WIDTH[7:0]							
Reset	0x3F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_PULSE_WIDTH	7:0	Sets the number of video clock cycles for the DMA mode vertical sync pulse width. The video VSYNC signal will be high for the specified number of clock cycles.

MST_VS1_DMA_VSYNC_B2 (0x7B26)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_VSYNC_FRONT_PORCH_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_FRONT_PORCH_L	7:0	DMA VSYNC front porch bits 7-0. Sets the number of video clock cycles after the last pixel of active frame data before asserting the DMA mode vertical sync pulse.

MST_VS1_DMA_VSYNC_B3 (0x7B27)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_VSYNC_FRONT_PORCH_H[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_FRONT_PORCH_H	3:0	DMA VSYNC front porch bits 11-8. Sets the number of video clock cycles after the last pixel of active frame data before asserting the DMA mode vertical sync pulse.

MST_VS1_DMA_HSYNC_B0 (0x7B28)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_HSYNC_PULSE_WIDTH_L[7:0]							
Reset	0x0F							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_PULSE_WIDTH_L	7:0	DMA HSYNC width bits 7-0. Sets the number of video clock cycles for the DMA mode horizontal sync pulse width. The video HSYNC signal will be high for the specified number of clock cycles.

MST_VS1_DMA_HSYNC_B1 (0x7B29)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_HSYNC_PULSE_WIDTH_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_PULSE_WIDTH_H	3:0	DMA HSYNC width bits 11-8. Sets the number of video clock cycles for the DMA mode horizontal sync pulse width. The video HSYNC signal will be high for the specified number of clock cycles.

MST_VS1_DMA_HSYNC_B2 (0x7B2A)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_HSYNC_FRONT_PORCH_L[7:0]							
Reset	0x0F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_FRONT_PORCH_L	7:0	DMA HSYNC front porch bits 7-0. Sets the number of video clock cycles after the last pixel of active line data before asserting the DMA mode horizontal sync pulse.

MST_VS1_DMA_HSYNC_B3 (0x7B2B)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_HSYNC_FRONT_PORCH_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_FRONT_PORCH_H	3:0	DMA HSYNC front porch bits 11-8. Sets the number of video clock cycles after the last pixel of active line data before asserting the DMA mode horizontal sync pulse.

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MST_VS1_RED_CRC_B0 (0x7B38)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	RED_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RED_CRC_B0	7:0	Calculated eDP CRC for red color plane bits 7-0.

MST_VS1_RED_CRC_B1 (0x7B39)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	RED_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RED_CRC_B1	7:0	Calculated eDP CRC for red color plane bits 15-8.

MST_VS1_RED_CRC_B3 (0x7B3B)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	CRC_UPDATED	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Read Clears All	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_UPDATED	7	Calculated eDP CRC color plane values have been updated since last read of this register. This bit is cleared on read.	0b0: Calculated CRC not updated b01: Calculated CRC updated

MST_VS1_GRN_BLU_CRC_B0 (0x7B3C)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	BLU_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLU_CRC_B0	7:0	Calculated eDP CRC for blue color plane bits 7-0.

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MST_VS1_GRN_BLU_CRC_B1 (0x7B3D)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	BLU_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLU_CRC_B1	7:0	Calculated eDP CRC for blue color plane bits 15-8.

MST_VS1_GRN_BLU_CRC_B2 (0x7B3E)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	GRN_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GRN_CRC_B0	7:0	Calculated eDP CRC for green color plane bits 7-0.

MST_VS1_GRN_BLU_CRC_B3 (0x7B3F)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	GRN_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GRN_CRC_B1	7:0	Calculated eDP CRC for green color plane bits 15-8.

MST_VS1_MSA_IGNORE_HRES_B0 (0x7B40)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_HRES_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSA_IGNORE_HRES_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

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MST_VS1_MSA_IGNORE_HRES_B1 (0x7B41)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_HRES_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSA_IGNORE_HRES_B1	7:0	MSA horizontal resolution override bits 15-8. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixel that defines a horizontal line.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	04/22	Initial release	—

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