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ANALOG DEVICES

*Click **here** to ask an associate for production status of specific part numbers.*

MAX96749AC/749AP/767/769/855/857/859/861

GMSL3/2 Serializer with DP1.4/eDP1.4a Input, DSC Passthrough, HDCP, and Ethernet

General Description

The MAX96749AC/ MAX96767/ MAX96855/ MAX96859 convert DP1.4 and eDP1.4a to single or dual GMSL3/2 serial link. They also sends and receives control channel and peripheral control data, enabling transmission of video and bidirectional data over a single cable.

The MAX96749AP/ MAX96769/ MAX96857/ MAX96861 add HDCP1.4 and HDCP2.3 decryption over DP Link and encryption for each GMSL™ link, with on-chip secure key storage and a state machine for HDCP authentication and link monitoring.

Using the GMSL3/2 concurrent control channel, an ECU can program the serializer, all deserializers, and peripheral device registers at any time, independent of video timing. Four hardware programmable devices addresses are available. Two additional pass-through I^{2}C/UART channels and a passthrough SPI channel are provided for peripheral control as well as up to 26 programmable GPIO.

Operation is specified over the automotive temperature range of -40°C to +105°C and the device is AEC-Q100 qualified. The devices are available in compact 8x8mm 56-TQFN side-wettable package with exposed pad.

Data can be transmitted over low-cost 50Ω coax or 100Ω STP cables that meet the GMSL channel specification.

Table 1. Typical Maximum Cable Length

	3.2mm Ø 50Ω Coax, Foam Dielectric	2.7mm Ø 50Ω Coax, Solid Dielectric	100Ω Shielded Twisted Pair, AWG26
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, 105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at 105°C**		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m
12Gbps/187.5Mbps	14m	8m	7m

Applications

- Infotainment Display Applications
- Infotainment Display with Ethernet
- ADAS ECU to Infotainment ECU Applications

Benefits and Features

- DP1.4 and eDP1.4a Compatible Input Interface
  - Supports 1, 2, and 4 Lanes and 1.62, 2.7, 5.4, and 8.1Gbps Link Rates (RBR, HBR, HBR2, HBR3)
  - Supports SST and up to 2-Stream MST Modes
  - Supports 24-Bit Color Depth Uncompressed
  - Supports 24/30-Bit Color Depth Compressed
- Multiple GMSL Link Rates for System Flexibility
  - 12, 6, or 3Gbps Single Lane Forward Link Rates
  - 12Gbps Dual Link Rate (24Gbps in even/odd pixel splitter)
  - 187Mbps Reverse Link Rate
- Bandwidth Support
  - 6.5MHz to 215MHz PCLK Uncompressed 24bpp Video per GMSL2 Link
  - 6.5MHz to 410MHz PCLK Uncompressed 24bpp Video per GMSL3 Link
  - 6.5MHz to 430MHz PCLK Uncompressed 24bpp Video over Dual GMSL2 Links
  - Max PCLK of 820MHz Uncompressed Video in Even/Odd Pixel Splitter Mode (GMSL3)
  - Max PCLK of 1080MHz Compressed Video at 24bpp and 864MHz at 30bpp per GMSL3 link
- VESA® Compliant DSC v1.1 and v1.2 Compression Pass-Through Mode
- HDCP1.4/2.3 Decryption over DP Link and Encryption over Both GMSL Links (HDCP Repeater Device)
- DP SST Mode Audio and I^{2}S/TDM Forward and I^{2}S/TDM Reverse Audio Tunnels
- 100Mbps SGMII Ethernet Interface (4-, 6-, 8-Pin Modes) (select part numbers only)
- ASIL-Relevant Functional Safety Features
  - ASIL-B Compliant
  - Line-Fault Monitor Detects Serial I/O Shorted Together, to Ground, to Battery or Open
  - 16-Bit CRC Protection and Retransmission of Control Data (I^{2}C, UART, SPI, GPIO, Audio)
  - Optional 32-Bit CRC Protection of Video Line Data
  - I^{2}C/UART Control Channel End-to-End CRC
  - Full-frame and Region-Based CRC (4 Regions)
  - Forward Error Correction (FEC) on GMSL Links and DP Link
- Performance Tools Ensure High Link Margin
  - Continuous Adaptive Equalization on GMSL Links
  - Built-In Forward/Reverse PRBS
  - Continuous Monitoring of Pre- and Post- FEC Link BER

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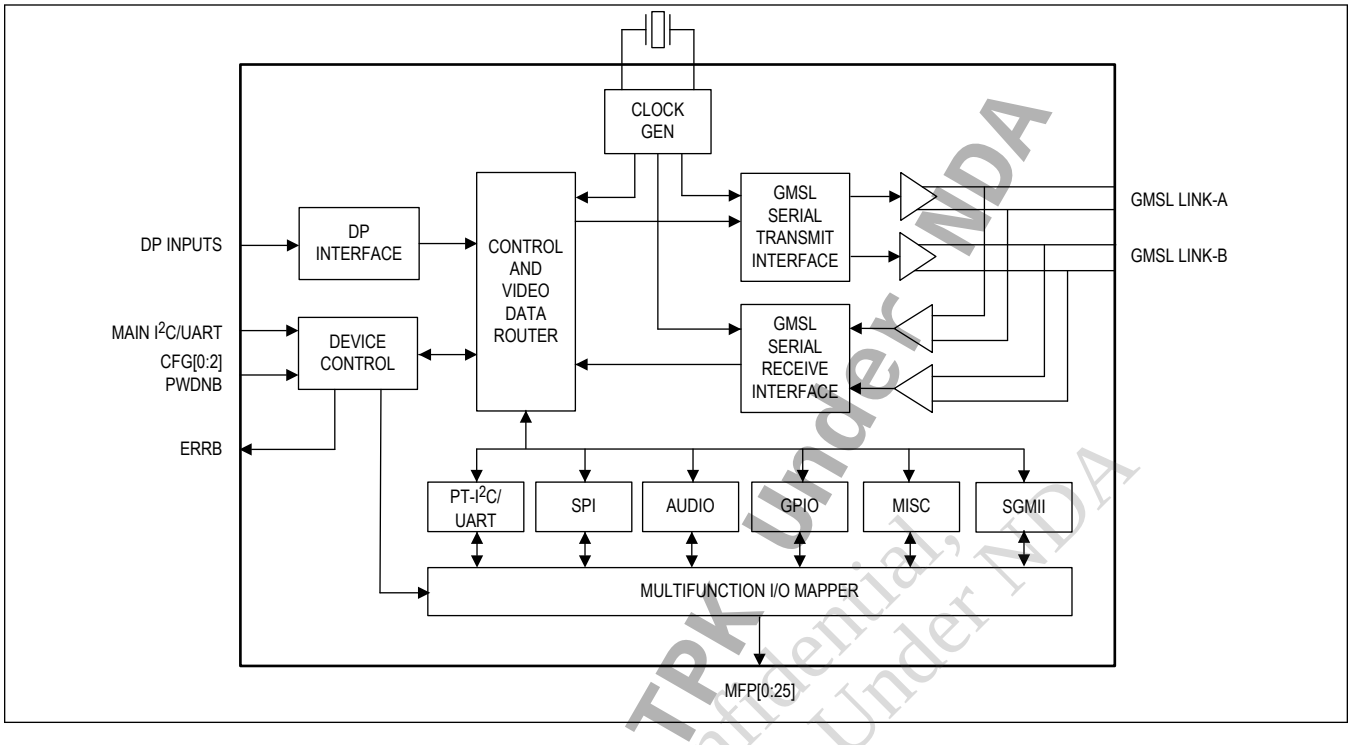
Simplified Block Diagram



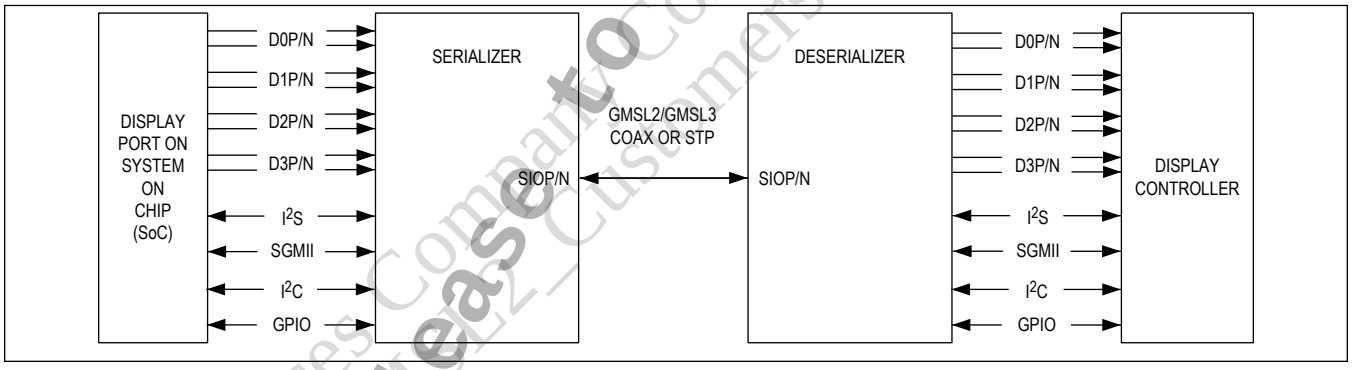


Figure 1. Typical Application Circuit

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Absolute Maximum Ratings

(All voltages with respect to ground.) .....
V_{DDIO} ..... −0.3V to +3.9V
V_{DD18} ..... −0.3V to +2.0V
V_{DD18_EDP} ..... −0.3V to +2.0V
V_{DD} ..... −0.3V to +1.1V
CAP_VDD ..... -0.3V to +1.2V
SIO_ pins (Active State) (*Note a*) ..... (V_{DD18} - 1.1V) to V_{DD18}
SIO_ pins (Inactive State) (*Note a*) ..... -0.3V to +1.1V
eRX_ ..... -0.3V to (V_{DD18} + 0.3V)
AUXP/N ..... -0.3V to (V_{DD18} + 0.3V)
XRES, X2, DIS_REM_CC ..... -0.3V to (V_{DD18} + 0.3V)
All Other Pins (*Note b*) ..... −0.3V to (V_{DDIO} + 0.3V)
Continuous Power Dissipation (T_A = +70ºC) for TQFN package (Multilayer board, θ_{JA} = 25°C/W) 2200mW
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note a: Active State means device is powered up and not in Sleep or Power-down modes. Inactive State means device is not powered up, or powered up in Sleep or Power-down mode.

Note b: Specified maximum voltage or 3.9V, whichever is lower.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56TQFN-EP

Package Code	T5688+6C
Outline Number	21-0135
Land Pattern Number	90-100041
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

SW-56TQFN-EP

Package Code	T5688Y+6C
Outline Number	21-100046
Land Pattern Number	90-100048
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board in still air. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

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Electrical Characteristics

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL FORWARD CHANNEL SERIAL OUTPUTS (SIO__)—SEE Figure 2							
Output Voltage Swing (Single-Ended)	$\|V_O\|$	R_L = 50Ω ±1%, (V_{OH} - V_{OL}) for both outputs	PAM4	400	500	600	mV
			NRZ	300	400	500	
Output Voltage Swing (Differential)	V_{OD}	R_L = 100Ω ±1%, peak-to-peak differential voltage	PAM4	800	1000	1200	mV_{PP}
			NRZ	600	800	1000	
Change in V_{OD} Between Complementary Output States	$\Delta\|V_{OD}\|$	R_L = 100Ω ±1%, $\|V_{OD(H)}-V_{OD(L)}\|$				25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state		0.4	0.5	0.6	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\|(V_{OS(H)} - V_{OS(L)})\|$				25	mV
Termination Resistance (Internal)	R_T	Incremental resistance around V_{OS}		43	50	57	Ω
DC ELECTRICAL CHARACTERISTICS / SGMII RX and TX LANES (All parameters are measured at R_{LOAD} = 100Ω ±1% Load)							
Output Differential Voltage	$\|V_{OD}\|$	For default TX signal swing settings. Programmable options exist for higher and lower swing levels		300	400	500	mV
Output Offset Voltage	V_{OS}	For default TX signal swing settings		400		600	mV
Output Ringing	V_{RING}	(Note 2)	For default TX signal swing settings			10	%
Output Impedance (Differential)	R_O			80		120	Ω
Mismatch in an Output Pair	ΔR_O					10	%
Change in V_{OD} Between Complementary States	$\Delta\|V_{OD}\|$					25	mV
Change in V_{OS} Between Complementary States	ΔV_{OS}					25	mV
Output Current on Short to Ground	I_{SA}, I_{SB}					40	mA
Output Current on Differential Short	I_{SAB}					12	mA
Input Common-Mode Voltage (AC Coupled)	V_{CM}				1.2		V
Differential Input Swing Voltage (Differential Peak)	V_{DIFF}			125		500	mV

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Differential Termination Resistance	R_{TERM}			80		120	Ω
DC ELECTRICAL CHARACTERISTICS / DP INPUTS (eRX__)							
Input Common-Mode Voltage	V_{CM_eRX}				0.5		V
Input Termination Resistance	R_I	Differential Measurement		90	100	110	Ω
DC ELECTRICAL CHARACTERISTICS / DP AUX CHANNEL							
Differential Peak-to-Peak Output Voltage	V_{OD}	V_{DD} = 1.0V, R_L = 100Ω ± 1%	Amplitude Setting 0		200		mV
			Amplitude Setting 1		400		
			Amplitude Setting 2		600		
			Amplitude Setting 3		800		
			Amplitude Setting 4		1000		
			Amplitude Setting 5		1200		
			Amplitude Setting 6		1380		
Input Peak-to-Peak Voltage	V_{ID}			140		1360	mV
Input Common-Mode Voltage	V_{CMI}				800		mV
Termination Resistance	R_I	Differential Measurement		90	110	125	Ω
DC ELECTRICAL CHARACTERISTICS / DP HPD							
HPD Driven Voltage	V_{OH_HPD}	Driven HPD Voltage, I_{OH_HPD} = -4mA		V_{DDIO} - 0.4			V
DC ELECTRICAL CHARACTERISTICS / I/O PINS							
High-Level Input Voltage	V_{IH}			0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA		V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA				0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled, V_{IN} = 0V to V_{DDIO}				1	µA
Input Capacitance	C_{IN}				3		pF
Internal Pullup/Pulldown Resistance	R_{IN}	40kΩ enabled			40		kΩ
		1MΩ enabled			1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS							
High-Level Input Voltage	V_{IH}			0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{DDIO}	V

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup Resistance	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Input Capacitance	C_{IN}			3		pF
Internal Pulldown Resistance	R_{PD}			1		MΩ
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held low to reset the chip		1		ms
DC ELECTRICAL CHARACTERISTICS / DIS_REM_CC INPUT						
High-Level Input Voltage	V_{IH}		1.6			V
Low-Level Input Voltage	V_{IL}				1.4	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DD18}			30	µA
Input Capacitance	C_{IN}			3		pF
Internal Pulldown Resistance	R_{PD}			100		kΩ
DC ELECTRICAL CHARACTERISTICS / LINE-FAULT DETECTION INPUTS (LMN0, LMN1, LMN2, LMN3)						
Open Pin Voltage	V_{O0}	LMN0 or LMN2		1.25		V
	V_{O1}	LMN1 or LMN3		0.75		
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1/OSC, X2) (*Note 2*)						
X1 Input Capacitance	C_{IN_X1}			3		pF
X2 Input Capacitance	C_{IN_X2}			1		pF
Internal X2 Limit Resistor	R_{LIM}			1.2		kΩ
Internal Feedback Resistor	R_{FB}			10		kΩ
Transconductance	g_M			28		mA/V

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED)							
High-Level Input Voltage	V_{IH}			0.9			V
Low-Level Input Voltage	V_{IL}					0.4	V
Input Impedance	R_{IN}				10		kΩ
X1 Input Capacitance	C_{IN_X1}				3		pF
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS (MST MODE, SINGLE 12GBPS GMSL LINK)							
Supply Current	I_{DD}	Maximum Power Consumption Use Case 4-Lane DP input, 8.1Gbps/Lane, 2-Stream MST Dual 12Gbps GMSL Links 2x 430MHz PCLK, RGB888	V_{DD18}		75	95	mA
			V_{DD}		520	1200	
			V_{DD18_eDP}		190	250	
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS (MST MODE, DUAL 6GBPS GMSL2 LINKS) (*Note 9*)							
Supply Current	I_{DD}	4-Lane DP input, 2.7Gbps/Lane, 2-Stream MST mode Dual 6Gbps GMSL2 Links 2x 1920x1080 (CTA VIC-16, 2200x1125 w/ blanking), 60Hz, Gradient Pattern, RGB888	V_{DD18}		75	95	mA
			V_{DD}		320	1000	
			V_{DD18_eDP}		180	240	
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS (SST MODE, SINGLE 6GBPS GMSL LINK)							
Supply Current	I_{DD}	1-Lane DP input, 5.4Gbps/Lane, SST mode Single 6Gbps GMSL Link 1280 x 720 (CTA VIC-4, 1650 x 750 w/blanking), 60Hz, Gradient Pattern, RGB888	V_{DD18}		50	70	mA
			V_{DD}		260	900	
			V_{DD18_eDP}		60	85	
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS (V_{DDIO} SUPPLY CURRENTS) (*Note 2*)							
Maximum V_{DDIO} Supply Current	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} at 1.9V		44		µA/MHz
			V_{DDIO} at 3.6V		81		

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Maximum Power-Down Current	I_{DD}	V_{DDIO} at 3.6V	T_A = +25ºC		6		µA
			T_A = +105ºC		7		
		V_{DD18} at 1.9V	T_A = +25ºC		1		
			T_A = +105ºC		7.5		
		V_{DD} at 1.05V	T_A = +25ºC		< 1		
			T_A = +105ºC		< 1		
		V_{DD_eDP} at 1.9V	T_A = +25ºC		1		
			T_A = +105ºC		7.5		
DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENT							
Maximum Sleep Current	I_{DD}	V_{DDIO} at 3.6V	T_A = +25ºC		7		µA
			T_A = +105ºC		8		
		V_{DD18} at 1.9V, both link-A and link-B sleep receivers active	T_A = +25ºC		28		
			T_A = +105ºC		38		
		V_{DD} at 1.05V	T_A = +25ºC		< 1		
			T_A = +105ºC		< 1		
		V_{DD_eDP} at 1.9V	T_A = +25ºC		1		
			T_A = +105ºC		7.5		
AC ELECTRICAL CHARACTERISTICS / GMSL FORWARD CHANNEL SERIAL OUTPUTS (SIO_)							
Serial Output Rise Time	t_R	NRZ	20% to 80%, V_O = 400mV, R_L = 100Ω ±1%		50		ps
Serial Output Fall Time	t_F	NRZ	80% to 20%, V_O = 400mV, R_L = 100Ω ±1%		50		ps
Total Serial Output Jitter	t_{TSOJ}	NRZ	PRBS7, single-ended or differential output		0.15		UI (P-P)
Deterministic Serial Output Jitter	t_{DSOJ}	NRZ	PRBS7, single-ended or differential output		0.10		UI (P-P)
Lock Time - Single Link	t_{LOCK}	See Figure 18			67	90	ms
Lock Time - Dual Link	t_{LOCK}	See Figure 18			90	120	ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from video applied to input to when the first video packet appears at GMSL outputs, assuming link is already established, FEC enabled (Figure 3)			5 x t_{FRAME} + 29900 x t_{PCLK} + 0.3ms		s
Maximum Video Latency	t_{SL}	Time from eRX_ input to SIO_ output in GMSL packet, FEC enabled (Figure 4)			2590 x t_{PCLK}		s

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / SGMII RX and TX LANES (All parameters are measured at R_{LOAD} = 100Ω ±1% Load) (*Note 2*)							
Clock Frequency Offset Between Devices	F_{SGMII_OFF}					±100	ppm
Clock Signal Duty Cycle	clock	Clock signal duty cycle at 625MHz		48		52	%
V^{OD} Rise/Fall Time	t_{rf}	20%-80%		100		200	ps
Skew Between Two Members of a Differential Pair	t_{SKEW}	Skew measured at 50% of the transition. T_{pHL} = propagation delay high to low transition, T_{pLH} = propagation delay low to high transition	$\lvert T_{pHLA}\rvert - \lvert T_{pLHB}\rvert$ or $\lvert T_{pLHA}\rvert - \lvert T_{pHLB}\rvert$			20	ps
Clock to Data Relationship from Either Edges of the Clock to Valid Data	$t_{clock2q}$	Skew measured at 0V differential.		250		550	ps
Setup Time when RXCLK is Used	t_{SETUP}	Measured at 50% of the transition		100			ps
Hold Time when RXCLK is Used	t_{HOLD}	Measured at 50% of the transition		100			ps
Total Output Jitter (BER = 1e-12)	Jit_{out}	When data is tracked with a CDR using 4MHz bandwidth				300	ps
Input Jitter Tolerence	Jit_{in}	For jitter frequency component higher than 637Khz		480			ps
AC ELECTRICAL CHARACTERISTICS / DP INPUTS (eRX__) (*Note 2*, *Note 4*)							
Supported Link Rates	f_{eDP}	Per Lane	HBR3		8.1		Gbps
			HBR2		5.4		
			HBR		2.7		
			RBR		1.62		
Unit Interval	UI_Rate	HBR3			123		ps
		HBR2			185.2		
	UI_Rate	HBR			370.4		
		RBR			617.3		
Unit Interval Tolerance	UI_TOL			-300		+300	ppm
CDR Tracking Bandwidth	$f_{CDR_Track_BW}$	HBR3			>15		MHz
		HBR2			>10		
		HBR			>10		
		RBR			>5.4		

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Jitter Tolerance	T_J	Jitter Frequency 5MHz	HBR3	0.77			UI
			HBR2	0.69			
			HBR	0.673			
			RBR	0.891			
SSC Downspread				0		0.5	%
SSC Modulation Rate				30		33	kHz
AC Coupling Capacitor	C_{AC}				150		nF
AC ELECTRICAL CHARACTERISTICS / DP AUX CHANNEL (*Note 2*)							
Unit Interval	UI			0.4		0.6	µs
Cycle-to-Cycle Jitter	t_{JCC}	UI Variation Within a Single Transaction				0.08	UI
		UI Variation Between Adjacent Bits				0.04	
AUX Slew Rate		Valid for default AUX channel swing amplitude.				375	mV/ns
AC ELECTRICAL CHARACTERISTICS / DP HPD							
HPD_IRQ Pulse Width				0.5		1	ms
HPD_IRQ Minimum Spacing				2			ms
AC ELECTRICAL CHARACTERISTICS / I²C / UART PORT TIMING							
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO} (*Note 2*)		20 x V_{DDIO}/5.5V		150	ns
I²C/UART Wake Time	t_{CC_WAKE}	From power-up or rising edge of PWDNB to local register access; for remote register access, I²C/UART wake time is the same as lock time (t_{LOCK}). See Figure 5			2.25	4	ms
AC ELECTRICAL CHARACTERISTICS / I²C TIMING—SEE Figure 6							
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I²C MST_BT = 010, I²C SLV_SH = 10)		9.6		100	kHz
		Mid f_{SCL} range: (I²C MST_BT = 101, I²C SLV_SH = 01)		100		400	
		High f_{SCL} range: (I²C MST_BT = 111, I²C SLV_SH = 00)		400		1000	
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low		4			µs
		f_{SCL} range, mid		0.6			
		f_{SCL} range, high		0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low		4.7			µs
		f_{SCL} range, mid		1.3			
		f_{SCL} range, high		0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low		4			µs
		f_{SCL} range, mid		0.6			
		f_{SCL} range, high		0.26			

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load On Each Bus Line	C_B	(*Note 2*)			100	pF
AC ELECTRICAL CHARACTERISTICS / SPI MASTER—SEE Figure 7 (*Note 2*, *Note 5*)						
Operating Frequency	f_{MCK}	(*Note 3*)	0.588		25	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	C_L = 5pF	$t_{MCK}/2$ - 3.4	$t_{MCK}/2$		ns
MOSI Data Output Delay	t_{MOD}	After SCLK falling edge, C_L = 5pF	-2.3		2.3	ns
MISO Input Setup Time	t_{MIS}	Before programmed sampling edge	13.5			ns
MISO Input Hold Time	t_{MIH}	After programmed sampling edge	-2			ns
AC ELECTRICAL CHARACTERISTICS / SPI SLAVE—SEE Figure 8 (*Note 2*, *Note 5*)						
Operating Frequency	f_{SCK}	(*Note 3*)			25	MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns
MISO Data Output Delay	t_{SOD}	After SCLK falling edge, C_L = 5pF	2.0		11.3	ns

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI Input Setup Time	t_{SIS}	Before SCLK rising edge	5			ns
MOSI Input Hold Time	t_{SIH}	After SCLK rising edge	3			ns
AC ELECTRICAL CHARACTERISTICS / I²S / TDM MASTER TIMING—SEE Figure 9 (Note 2, Note 6)						
WS Frequency	f_{WS}	C_L = 5pF	8		192	kHz
Sample Word Length	n_{WS}	C_L = 5pF	8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$, C_L = 5pF	0.512		49.152	MHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$, C_L = 5pF	0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$, C_L = 5pF	0.35 x t_{SCK}			ns
SD, WS Valid Time Before SCK	t_{MAVS}	$t_{SCK} = 1/f_{SCK}$, C_L = 5pF	0.2 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{MAVH}	$t_{SCK} = 1/f_{SCK}$, C_L = 5pF	0.2 x t_{SCK}	0.5 x t_{SCK}		ns
AC ELECTRICAL CHARACTERISTICS / I²S / TDM SLAVE TIMING—SEE Figure 10 (Note 2)						
WS Frequency	f_{WS}		8		192	kHz
Sample Word Length	n_{WS}		8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$	0.512		49.152	MHz
SD, WS Setup Time	t_{SAS}		4			ns
SD, WS Hold Time	t_{SAH}		4			ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1/OSC, X2) (Note 2)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}	(Note 8)			±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1/OSC, X2 UNCONNECTED) (Note 2)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}	(Note 8)			±200	ppm
Input Jitter		Sinusoidal jitter < 1MHz (rising edge), downstream deserializer using crystal reference			150	ps P-P
		12Gbps/187.5Mbps, sinusoidal jitter < 1MHz (rising edge), downstream deserializer using crystal reference			150	ps P-P
Input Duty Cycle	t_{DUTY}		40		60	%
Input Fall Time	t_F	80% to 20%			4	ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK OUTPUT (RCLKOUT)						
Frequency	f_{REF}	Crystal or reference clock input		25		MHz
Rise Time	t_R	20% to 80%, C_L = 10pF, 25MHz divided by 1, 2, or 4 (Note 2, Note 7)			4	ns

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Electrical Characteristics (continued)

(V_{DD18} = V_{DD18_eDP} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time	t_F	80% to 20%, CL = 10pF, 25MHz divided by 1, 2, or 4 (Note 2, Note 7)			4	ns
Jitter Generation	t_J			200		ps

Note 1: Min/Max limits are 100% tested at T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design.

Note 3: Production tested using ECS ECS-250-18-33Q-DS crystal.

Note 4: In compliance with DisplayPort v1.4a per PHY CTS excluding the RBR mode.

Note 5: Measured at 50MHz. For V_{DDIO} = 1.7V–2.24V, SPI_SPEED[1:0] = 00 and for V_{DDIO} = 2.25V–3.6V, SPI_SPEED[1:0] = 01.

Note 6: Measured at 50MHz. For V_{DDIO} = 1.7V–2.24V, I2S_SPEED[1:0] = 00 and for V_{DDIO} = 2.25V–3.6V, I2S_SPEED[1:0] = 01.

Note 7: MFP pin speed configured based on V_{DDIO}:
TTS = 01 for V_{DDIO} < 3V
TTS = 10 for V_{DDIO} ≥ 3V
See Table 16 for details regarding output speed programming.

Note 8: If SGMII feature is used, XTAL or Reference Clock ppm must be ±100 to ensure the SGMII clock complies with the SGMII specification.

Note 9: Does not apply to GMSL3 capable product variants.

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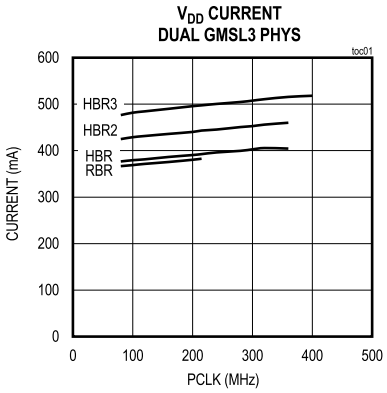
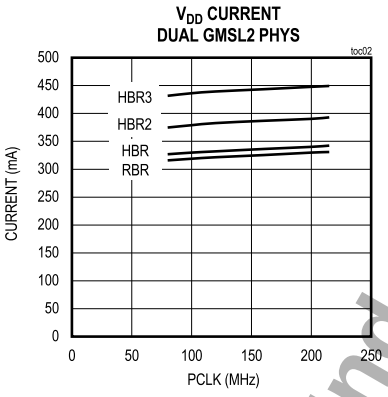
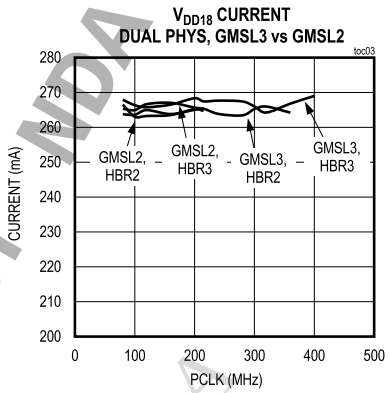
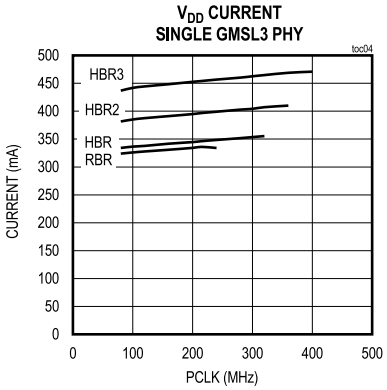
Typical Operating Characteristics

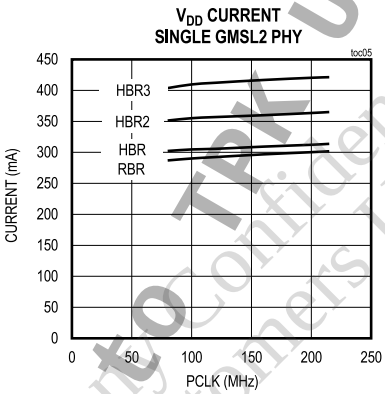
(V_{DD18} = V_{DD18_eDP} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.)

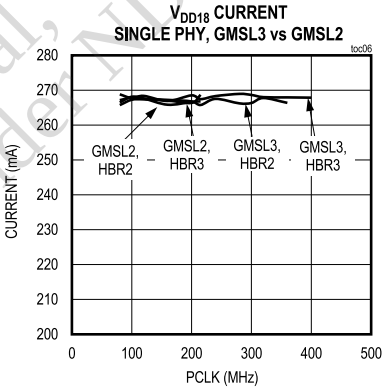


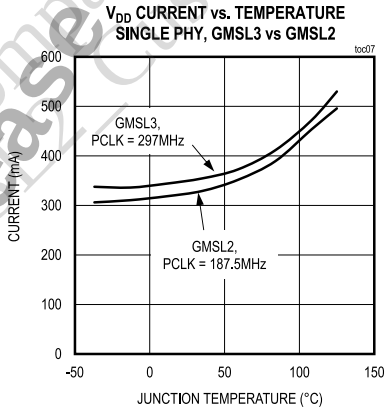












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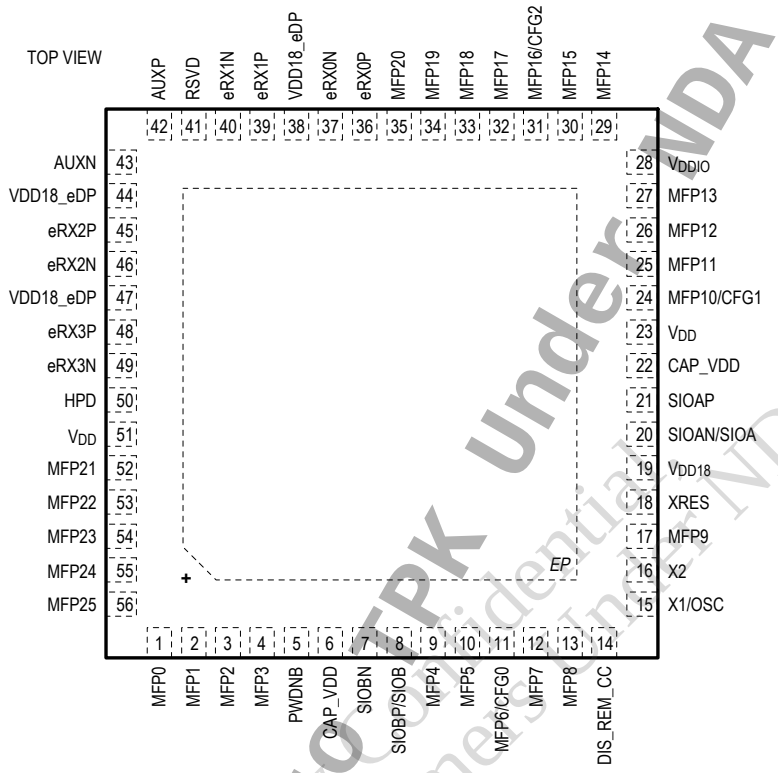
Pin Configuration



Pin Description

PIN	NAME	FUNCTION MODE	FUNCTION
GMSL SERIAL LINK (In single GMSL link applications, leave unused SIO link output pins unconnected)			
7	SIOBN	SIOBN	SIOBN: GMSL Link-B Inverted Twisted-Pair Serial-Data Input/Output. State of CFG2 on power-up determines configuration. SIOA: GMSL Link-A Coax Serial-Data Input/Output. State of CFG1 on power-up determines configuration.
8	SIOBP/SIOB	SIOBP SIOB	SIOBP: GMSL Link-B Noninverted Twisted-Pair Serial-Data Input/Output. State of CFG2 on power-up determines configuration. SIOB: GMSL Link-B Coax Serial-Data Input/Output. State of CFG1 on power-up determines configuration.
20	SIOAN/SIOA	SIOAN SIOA	SIOAN: GMSL Link-A Inverted Twisted-Pair Serial-Data Input/Output. State of CFG1 on power-up determines configuration. SIOA: GMSL Link-A Coax Serial-Data Input/Output. State of CFG1 on power-up determines configuration.
21	SIOAP	SIOAP	SIOAP: GMSL Link-A Noninverted Twisted-Pair Serial-Data Input/Output. State of CFG1 on power-up determines configuration. In COAX mode, terminate to ground via AC capacitor and 50ohm resistor.

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PIN	NAME	FUNCTION MODE	FUNCTION
DP INTERFACE (Leave pins unconnected when not used)			
36	eRX0P	eRX0P	eDP/DP Main Link Lane-0 Noninverted Input.
37	eRX0N	eRX0N	eDP/DP Main Link Lane-0 Inverted Input.
39	eRX1P	eRX1P	eDP/DP Main Link Lane-1 Noninverted Input.
40	eRX1N	eRX1N	eDP/DP Main Link Lane-1 Inverted Input.
42	AUXP	AUXP	eDP/DP AUX Channel Noninverted Input/Output.
43	AUXN	AUXN	eDP/DP AUX Channel Inverted Input/Output.
45	eRX2P	eRX2P	eDP/DP Main Link Lane-2 Noninverted Input.
46	eRX2N	eRX2N	eDP/DP Main Link Lane-2 Inverted Input.
48	eRX3P	eRX3P	eDP/DP Main Link Lane-3 Noninverted Input.
49	eRX3N	eRX3N	eDP/DP Main Link Lane-3 Inverted Input.
50	HPD	HPD	DP Hot Plug Detect Output. CMOS output. Default power-up is Logic-High. HPD is Logic Low when PWDNB is active Low with 1MΩ pulldown to GND.
MULTIFUNCTION PINS (*Denotes default state after power-up)			
1	MFP0	SGMII_RXCN RO(alt) SS2(alt) SCKOR2 SCLK RCLKOUT GPIO0*	SGMII_RXCN: SGMII RXC- LVDS Clock Input. Coupling capacitors may be required depending on the paired device. RO(alt): Alternate pin for RO. When Configured as Slave, SPI Mode-Select Input with Internal 1MΩ Pulldown to Ground. RO = high enables master read from MISO. RO = low enables master write to MOSI. SS2(alt): SPI Slave Select. When configured as master, slave 2 select push-pull output. SCKOR2: I^2S/TDM Serial-Clock Push-Pull Output. Supports reverse-path audio. SCLK: SPI Clock. When configured as master, push-pull clock output. When configured as slave, clock input with internal 1MΩ pulldown to ground. RCLKOUT: 25MHz Frequency Reference Push-Pull Output; Enabled or disabled by register write. GPIO0: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.

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PIN	NAME	FUNCTION MODE	FUNCTION
2	MFP1	SGMII_RXDP WSOR2 MOSI GPIO1*	SGMII_RXDP: SGMII RXD+ LVDS Data Input. Coupling capacitors may be required depending on the paired device. WSOR2: I^{2}S/TDM Word-Select Push-Pull Output. Outputs audio word select clock. Supports reverse-path audio. MOSI: SPI Master-Out Slave-In. When configured as master, push-pull output that drives data to external slave. When configured as slave, input with internal 1MΩ pulldown to ground that receives data from external master. GPIO1: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
3	MFP2	SGMII_RXDN SDOR2 MISO GPIO2*	SGMII_RXDN: SGMII RXD- LVDS Data Input. Coupling capacitors may be required depending on the paired device. SDOR2: I^{2}S/TDM Serial Data Push-Pull Output. Supports reverse-path audio. MISO: SPI Master In Slave Out. When configured as master, input with internal 1MΩ pulldown to ground that receives data from external slave. When configured as slave, push-pull output that drives data to an external master. GPIO2: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
4	MFP3	SDA* RX* SDAP(Alt 1) GPIO3*	SDA: I^{2}C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SDA or RX selected by CFG0 at power-up). RX: UART Input (SDA or RX selected by CFG0 at power-up). SDAP(Alternate 1): Peripheral I^{2}C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO3: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
9	MFP4	LMN0 GPIO4*	LMN0: Line-Fault Monitor Input. GPIO4: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.

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PIN	NAME	FUNCTION MODE	FUNCTION
10	MFP5	LMN1 GPIO5*	LMN1: Line-Fault Monitor Input. GPIO5: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
11	MFP6/CFG0	CFG0* HS_OUT GPO6	CFG0: Configuration Pin 0. Voltage at pin sets device mode, which is latched at power-up. Connect to a resistor divider between V_{DDIO} and ground. See Table 12. HS_OUT: Video Horizontal Sync Timing Signal Push-Pull Output. For debug use only. GPO6: Configurable General-Purpose Output.
12	MFP7	SCL* TX* SCLP(Alt 1) GPI7/ODO7	SCL: I^2C Clock Input/Open-Drain Output With Internal 40kΩ Pullup to V_{DDIO} (SCL or TX selected by CFG0 at power-up). TX: UART Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO} (SCL or TX selected by CFG0 at power-up). SCLP(Alternate 1): Peripheral I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPI7/ODO7: Configurable General Purpose Input and Open-Drain Output with Internal 40kΩ Pullup.
13	MFP8	LOCK* GPIO8	LOCK: Open-Drain Lock Indication Output with Internal 40kΩ Pullup to V_{DDIO}. LOCK = high indicates that GMSL link(s) has locked and is ready to send/receive data. See LOCK_CFG register description. LOCK is Hi-Z when PWDNB is low. GPIO8: Configurable General-Purpose Input/Output. Note: Leave pin unconnected when not used.
17	MFP9	ERRB* GPIO9	ERRB: Open-Drain Error Indication Output with Internal 40kΩ Pullup to V_{DDIO}. ERRB = low indicates that a data error, line fault, or interrupt has been detected. ERRB is Hi-Z when PWDNB is low. GPIO9: Configurable General-Purpose Input/Output. Note: Leave pin unconnected when not used.

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PIN	NAME	FUNCTION MODE	FUNCTION
24	MFP10/CFG1	CFG1* VS_OUT BNE SS1 RCLKOUT(Alt) GPO10	CFG1: Configuration Pin 1. Voltage at pin sets device modes, which are latched at power-up. Connect to a resistor divider between V_{DDIO} and ground. See Table 12. VS_OUT: Video Vertical Sync Timing Signal Push-Pull Output. For debug use only. BNE: SPI Buffer Not Empty. When configured as slave, SPI push-pull output. BNE = high indicates SPI data is available. SS1: SPI Slave Select. When configured as master, slave 1 select push-pull output. RCLKOUT(Alternate): 25MHz Frequency Reference Push-Pull Output; Enabled or disabled by register write. GPO10: Configurable General-Purpose Output.
25	MFP11	HS_IN SCKOR1(Alt) WS1 MS(Alt) GPIO11*	HS_IN: Video Horizontal Sync Timing Signal Push-Pull Input. For debug use only. SCKOR1(Alternate): I^2S/TDM Serial-Clock Push-Pull Output. Supports reverse-path audio. WS1: I^2S/TDM Word-Select Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. MS(Alternate): UART Mode Select with Internal 1MΩ Pulldown to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be overwritten by a register write. GPIO11: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
26	MFP12	MDIO VS_IN SDOR1(Alt) SD1 SDAP GPIO12*	MDIO: Ethernet Management Control Channel Data Input/Open-Drain Output with internal 40kΩ Pullup to V_{DDIO}. VS_IN: Video Vertical Sync Timing Signal Push-Pull Input. For debug use only. SDOR1(Alternate): I^2S/TDM Serial Data Push-Pull Output. Supports reverse-path audio. SD1: I^2S/TDM FWD Audio Channel Serial Data Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. SDAP: Peripheral I^2C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO12: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.

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PIN	NAME	FUNCTION MODE	FUNCTION
27	MFP13	MDC PCLK_IN WSOR1(Alt) SCK1 SCLP GPIO13*	MDC: Ethernet Management Control Channel Clock Input/Open-Drain Output with internal 40kΩ Pullup to V_{DDIO}. PCLK_IN: Video Pixel Clock Push-Pull Input. For debug use only WSOR1(Alternate): I^2S/TDM Word Select Push-Pull Output. Supports reverse-path audio. SCK1: I^2S/TDM FWD Audio Channel Clock Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. SCLP: Peripheral I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO13: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
29	MFP14	DE_IN MOSI(Alt) SCKOR1 SDA2/RX2 SDAP(Alt 2) GPIO14*	DE_IN: Video Data Enable Timing Signal Push-Pull Input. For debug use only MOSI(Alternate): SPI Master-Out Slave-In. When configured as master, push-pull output that drives data to external slave. When configured as slave, input with internal 1MΩ pulldown to ground that receives data from external master. SCKOR1: I^2S/TDM Serial-Clock Push-Pull Output. Supports reverse-path audio. SDA2: Pass-Through Port 2 I^2C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. RX2: Pass-Through Port 2 UART Input. SDAP(Alternate 2): Peripheral I^2C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO14: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.

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PIN	NAME	FUNCTION MODE	FUNCTION
30	MFP15	PCLK_OUT MISO(Alt) SDOR1 SCL2/TX2 SCLP(Alt 2) GPIO15*	PCLK_OUT: Video Pixel Clock Push-Pull Output. For debug use only. MISO(Alternate): SPI Master In Slave Out. When configured as master, input with internal 1MΩ pulldown to ground that receives data from external slave. When configured as slave, push-pull output that drives data to an external master. SDOR1: I^2S/TDM Serial Data Push-Pull Output. Supports reverse-path audio. SCL2: Pass-Through Port 2 I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. TX2: Pass-Through Port 2 UART Output with Internal 40kΩ Pullup to V_{DDIO}. SCLP(Alternate 2): Peripheral I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO15: Configurable General-Purpose Input/Output. Note: Leave pin unconnected when not used.
31	MFP16/CFG2	CFG2* DE_OUT WSOR1 GPO16	CFG2: Configuration Pin 2. Voltage at pin sets device modes, which are latched at power-up. Connect to a resistor divider between V_{DDIO} and ground. See Table 12. DE_OUT: Video Data Enable Timing Signal Push-Pull Output. For debug use only. WSOR1: I^2S/TDM Word Select Push-Pull Output. Supports reverse-path audio. GPO16: Configurable General-Purpose Output.
32	MFP17	SDA1* RX1 SDAP(Alt 3) GPIO17	SDA1: Pass-Through Port 1 I^2C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. Power-up default enables PT1 I^2C read access to serializer registers. Remote I^2C tunnel to deserializer disabled. RX1: Pass-Through Port 1 UART Input with Internal 40kΩ Pullup to V_{DDIO} . SDAP(Alternate 3): Peripheral I^2C Data Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO17: Configurable General-Purpose Input/Output. Note: Leave pin unconnected when not used.

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PIN	NAME	FUNCTION MODE	FUNCTION
33	MFP18	SCL1* TX1 SCLP(Alt 3) GPIO18	SCL1: Pass-Through Port 1 I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. Power-up default enables PT1 I^2C read access to serializer registers. Remote I^2C tunnel to deserializer disabled. TX1: Pass-Through Port 1 UART Output with Internal 40kΩ Pullup to V_{DDIO}. SCLP(Alternate 3): Peripheral I^2C Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. GPIO18: Configurable General-Purpose Input/Output. Note: Leave pin unconnected when not used.
34	MFP19	MDIO(Alt) LMN2 GPIO19*	MDIO(Alternate): Ethernet Management Control Channel Data Input/Open-Drain Output with internal 40kΩ Pullup to V_{DDIO}. LMN2: Line-Fault Monitor Input. GPIO19: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
35	MFP20	MDC(Alt) LMN3 GPIO20*	MDC(Alternate): Ethernet Management Control Channel Clock Input/Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}. LMN3: Line-Fault Monitor Input. GPIO20: Configurable General-Purpose Input/Output. Power-up default: GPI, CMOS input enabled, output disabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
52	MFP21	SGMII_TXDP GPI21*	SGMII_TXDP: SGMII TXD+ LVDS Data Output. Coupling capacitors may be required depending on the paired device. GPI21: Configurable General-Purpose Input. Power-up default: GPI, CMOS input enabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
53	MFP22	SGMII_TXDN SCK2 GPI22*	SGMII_TXDN: SGMII TXD- LVDS Data Output. Coupling capacitors may be required depending on the paired device. SCK2: I^2S/TDM Serial Clock Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. GPI22: Configurable General-Purpose Input. Power-up default: GPI, CMOS input enabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.

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PIN	NAME	FUNCTION MODE	FUNCTION
54	MFP23	SGMII_TXCP WS2 GPI23*	SGMII_TXCP: SGMII TXC+ LVDS Clock Output. Coupling capacitors may be required depending on the paired device. WS2: I^2S/TDM Serial-Word Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. GPI23: Configurable General-Purpose Input. Power-up default: GPI, CMOS input enabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
55	MFP24	SGMII_TXCN SD2 GPI24*	SGMII_TXCN: SGMII TXC- LVDS Clock Output. Coupling capacitors may be required depending on the paired device. SD2: I^2S/TDM Serial-Data Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. GPI24: Configurable General-Purpose Input. Power-up default: GPI, CMOS input enabled, GMSL GPIO tunnel disabled, local read enabled, 1MΩ pulldown. Note: Leave pin unconnected when not used.
56	MFP25	SGMII_RXCP SCLK(alt) RO SS2 MS GPI25/ODO25	SGMII_RXCP: SGMII RXC+ LVDS Clock Input. Coupling capacitors may be required depending on paired device. SCLK(alt): Alternate pin for I^2S/TDM FWD Audio Channel Clock Input with Internal 1MΩ Pulldown to Ground. Supports forward-path audio. RO: When Configured as Slave, SPI Mode-Select Input with Internal 1MΩ Pulldown to Ground. RO = high enables master read from MISO. RO = low enables master write to MOSI. SS2: SPI Slave Select. When configured as master, slave 2 select push-pull output. MS: UART Mode Select with Internal 1MΩ Pulldown to Ground. Set MS = low to select base mode. Set MS = high to select bypass mode. MS state may also be overwritten by a register write. GPI25/ODO25: Configurable General Purpose Input and Open-Drain Output with Internal 40kΩ Pullup.
MISCELLANEOUS—SEE Table 2			
5	PWDNB	PWDNB	Active-Low, Power-Down Input with Internal 1MΩ Pulldown to Ground. Apply logic low to place device in power-down mode. Connect to V_{DDIO}/logic high for normal operation.

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PIN	NAME	FUNCTION MODE	FUNCTION
14	DIS_REM_CC	DIS_REM_CC	Active-High Latch at Power-Up Input, with Internal 100kΩ Pulldown to Ground. Used to disable the remote control channel in multimaster configurations (local ECU control of serializer and deserializer). Connect to V_{DD18} to disable the remote control channel (sets DIS_REM_CC register bits to logic-1 for both links). Connect to ground or leave floating to enable the remote control channel function (sets DIS_REM_CC register bits to default logic-0 state). After power-up latch, register writes to DIS_REM_CC registers, one for each GMSL link, are required to change the state of the remote control channel. Note: Leave pin unconnected when not used.
15	X1/OSC	X1/OSC	X1/OSC: Crystal/Oscillator Input. Connect to either one terminal of a ±200ppm 25MHz crystal or a 25MHz external clock source. If crystal is used, connect a load capacitor from X1/OSC to ground (load capacitor value depends on crystal used).
16	X2	X2	X2: Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal. If crystal is used, connect a load capacitor from X2 to ground (load capacitor value depends on crystal used). If external oscillator is connected to X1/OSC, leave X2 floating.
18	XRES	XRES	Output Reference Resistor. Connect a 402Ω ±1% resistor between XRES and ground.
41	RSVD	RSVD	Reserved. Not internally connected. Leave open.
POWER SUPPLIES—SEE Table 2			
6, 22	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1V Core Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
19	V_{DD18}	V_{DD18}	1.7V to 1.9V Analog Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
23, 51	V_{DD}	V_{DD}	1.0V Core Supply. Connect a 0.95V to 1.05V supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
28	V_{DDIO}	V_{DDIO}	1.7V to 3.6V I/O Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
38, 44, 47	V_{DD18_eDP}	V_{DD18_eDP}	1.7V to 1.9V eDP/DP Analog Supply. Place decoupling capacitor connected to PCB ground plane as close to pin as possible.
EP	EP	EP	Exposed Pad. EP is internally connected to device ground. EP MUST be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

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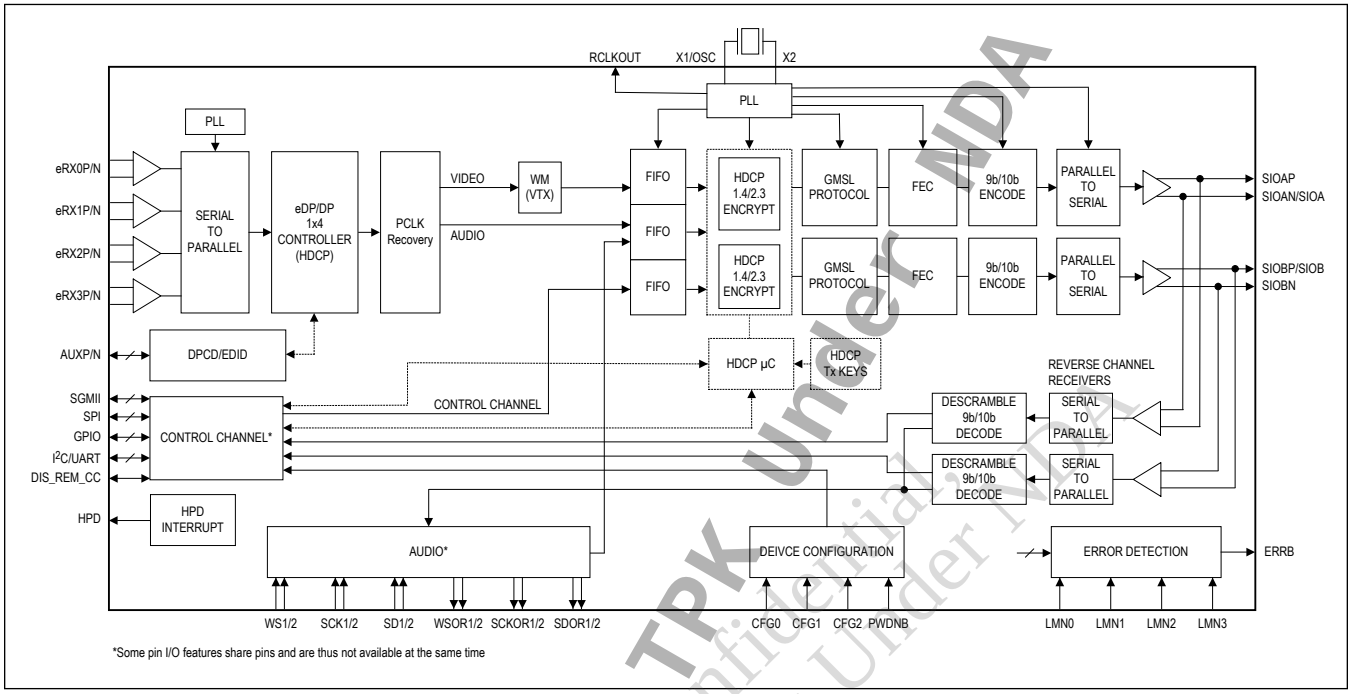
Functional Diagrams

Functional Block Diagram



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Detailed Description

External Component Requirements

See Figure 15 and Figure 16 for details on the minimum (application-specific) external component requirements. Also see *Typical Application Circuits* diagram.

Table 2. External Component Requirements

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
XRES	R_{XRES}		402 ±1%. Use a single resistor.	Ω
Line-Fault Pulldown Resistor	R_{PD}		49.9 ±1%	
Line-Fault Series Resistors - Coax Mode	R_{EXT1}	LMN0, LMN1, LMN2 or LMN3	48.7 ±1%	kΩ
	R_{EXT2}		DNI	
Line-Fault Series Resistor - STP Mode	R_{EXT1}	See *Line Fault* Section for STP Mode	48.7 ±1%	kΩ
	R_{EXT2}	See *Line Fault* Section for STP Mode	42.2 ±1%	
Link Isolation Capacitors	C_{LINK}	Place close to the SIO_ pins (7, 8, 20, and 21) used in the application.	0.1	µF
Coax Mode Termination Resistor	R_{TERM}	In coax mode, connect R_{TERM} between unused SIO_ pin and ground on each coax link.	49.9 ±1%	Ω
eRXxx Isolation Capacitors and trace impedance	C_eRX_N/P	DP trace, maintain 50Ω characteristic impedance, 0.1µF AC capacitor required.	0.1	µF
AUX Interface Isolation Capacitors	C_AUX	Place series 0.1µF DC blocking capacitors on AUXP and AUXN interfaces	0.1	µF
Crystal		Place as close as possible to pins 15 and 16.	25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values which compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible to pins 15 (X1/OSC) and pin 16 (X2).		
V_{DDIO} Decoupling Capacitors		Place a 0.01µF and a 0.1µF capacitor* as close as possible to pin 28.	0.01 + 0.1	µF
V_{DD18} Decoupling Capacitors		Place a 0.01µF and a 0.1µF capacitor* as close as possible to pin 19.	0.01 + 0.1	µF
V_{DD18_eDP} Decoupling Capacitors		Place a 0.01µF and a 0.1µF capacitor* as close as possible to pins 38, 44 and 47. Run separate traces from each pin to the capacitors.	0.01 + 0.1 on each V_{DD18_eDP} pin	µF

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Table 2. External Component Requirements (continued)

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
V_{DD} Decoupling Capacitors		Place 0.1µF and a 10µF capacitors* as close as possible to pins 23 and 51. Run separate traces from each pin to the capacitors.	0.1 + 10 on each V_{DD} pin	µF
CAP_VDD Decoupling Capacitors		Place 0.1µF capacitor as close as possible to pin 6. Place a 0.1µF and a 10µF capacitor as close as possible to pin 22.	0.1 (pin 6), 0.1 + 10 (pin 22)	µF
Open-Drain Pullup Resistors		Application-Specific. Quantity and values depend on multi-function GPIO pin configurations. Typically used for I^2C/UART pins.		
SGMII Isolation Capacitors	C_{SGMII}	Place between SGMII RX and TX devices to provide common mode voltage isolation. Place near driver output.	0.1	µF

* Power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

ESD Protection

Table 3. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIO__	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±8		kV
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, Coax Configuration		±6		
		ISO10605, R_D = 330Ω, CS = 150pF, Contact Discharge, STP Configuration		±6		
		ISO10605, R_D = 330Ω, C_S = 150pF, Air Discharge		±8		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews and register definitions. Designers must also have the following information to correctly design using this device:

- The **GMSL Channel Specification** contains physical layer requirements for the PCB traces, cables and connectors that constitute the GMSL link.
- The **GMSL Hardware Design and Validation Guide** contains recommendations for PCB design, applications circuits, selection of external components and guidelines for use of GMSL signal integrity tools.
- The **GMSL User Guide** contains detailed programming guidelines for GMSL device features.
- **Errata sheets** contain deviations from published device specifications, and are specific to part number and revision ID.

Contact factory to receive these documents, and for additional guidance on MAX96749AC/749AP/767/769/855/857/859/861 features.

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Feature List by Part Number

Table 4. Comparison of Part Numbers

	MAX96749AC	MAX96749AP	MAX96767	MAX96769	MAX96855	MAX96857	MAX96859	MAX96861
GMSL Generation(s)	GMSL2	GMSL2	GMSL2	GMSL2	GMSL3/2	GMSL3/2	GMSL3/2	GMSL3/2
GMSL Link Rates - Single Link	6/3Gbps	6/3Gbps	6/3Gbps	6/3Gbps	12/6/ 3Gbps	12/6/ 3Gbps	12/6/ 3Gbps	12/6/ 3Gbps
Max GMSL2 Dual Link Rate	12Gbps	12Gbps	12Gbps	12Gbps	12Gbps	12Gbps	12Gbps	12Gbps
Max Even/Odd Pixel Splitter Mode Link Rate	12Gbps	12Gbps	12Gbps	12Gbps	24Gbps	24Gbps	24Gbps	24Gbps
Max DP Lane Rate	8.1Gbps	8.1Gbps	8.1Gbps	8.1Gbps	8.1Gbps	8.1Gbps	8.1Gbps	8.1Gbps
VESA-Compliant DSC Compression Pass-Through	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
DP and GMSL Link HDCP (1.4 and 2.3)	No	**Yes**	No	**Yes**	No	**Yes**	No	**Yes**
SGMII (100Mbps)	No	No	**Yes**	**Yes**	No	No	**Yes**	**Yes**
Daisy Chain Support	No	No	No	No	No	No	**Yes**	**Yes**

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Functional Diagrams

LVDS Output Parameters

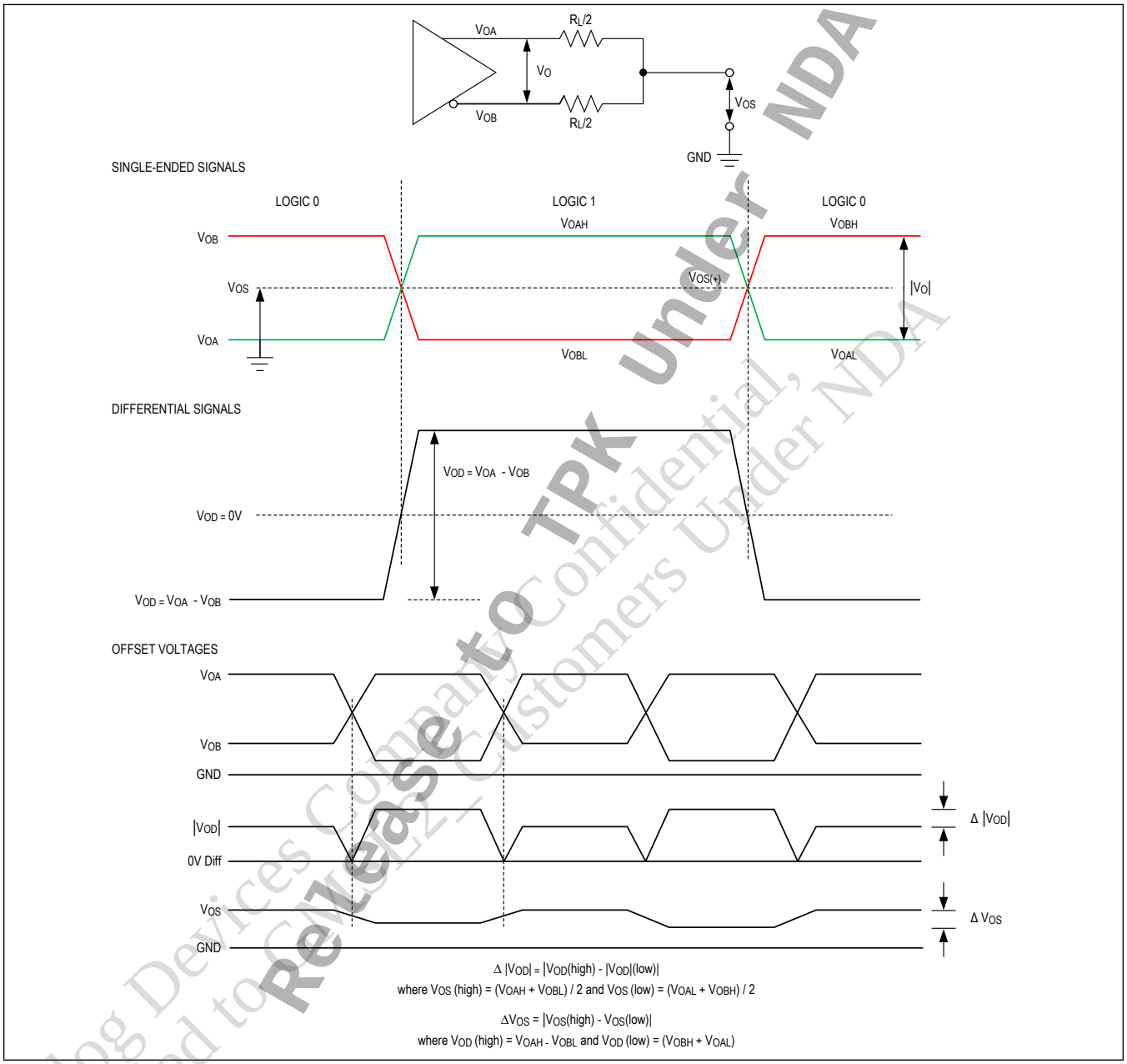

Figure 2. LVDS Output Parameters

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Serializer Video Initialization Time

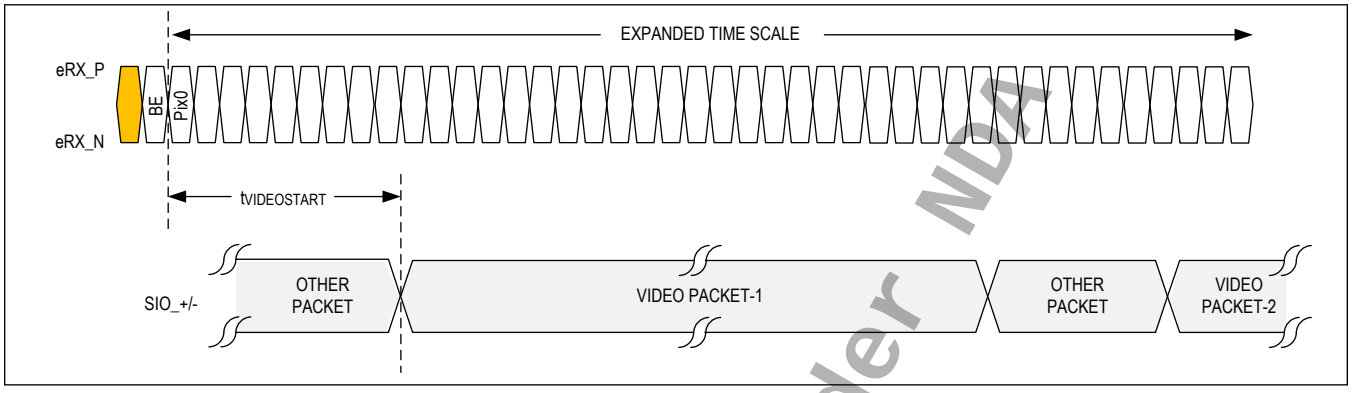

Figure 3. Serializer Video Initialization Time

Serializer Video Latency

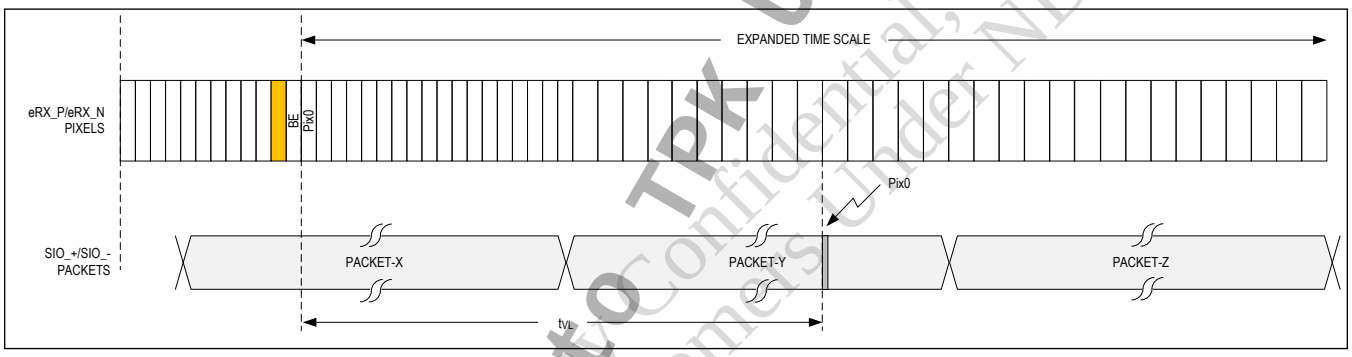

Figure 4. Serializer Video Latency

I²C/UART Wake Time

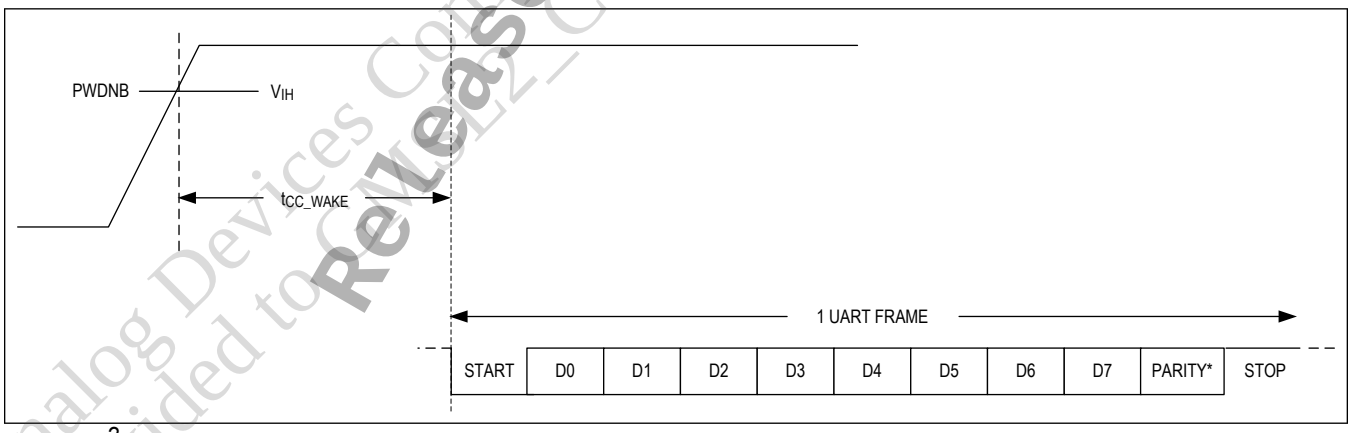

Figure 5. I²C/UART Wake Time

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I²C Timing Parameters

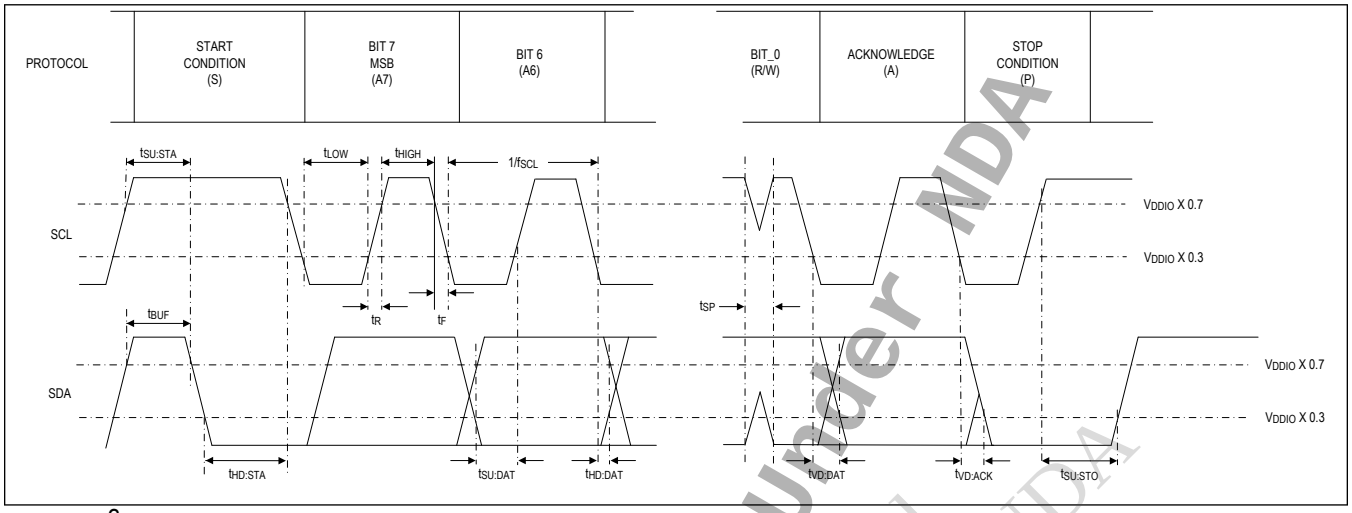

Figure 6. I²C Timing Parameters

SPI Master-Mode Timing Parameters

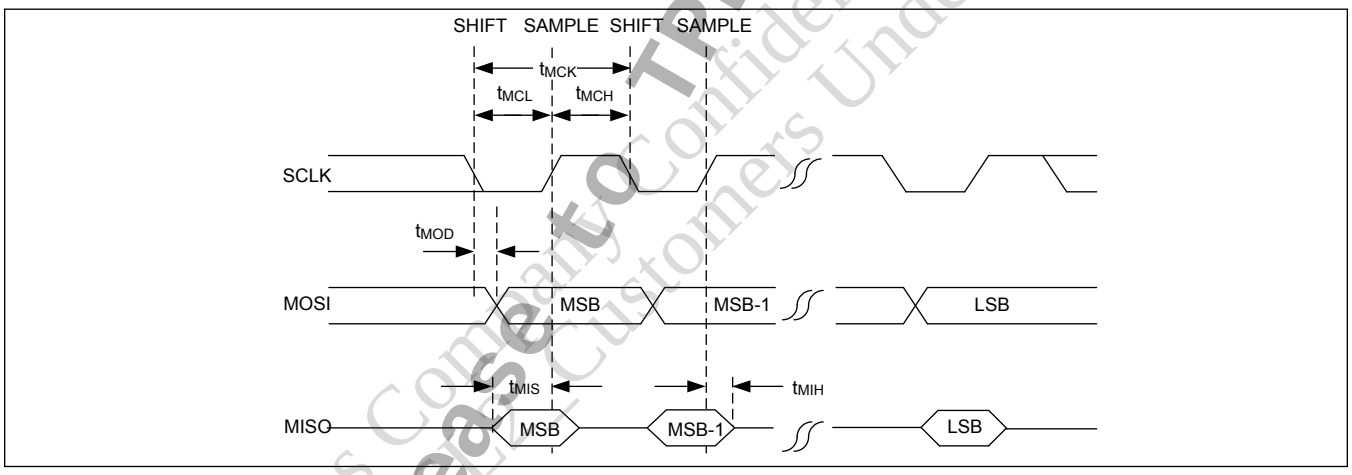

Figure 7. SPI Master-Mode Timing Parameters

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SPI Slave-Mode Timing Parameters

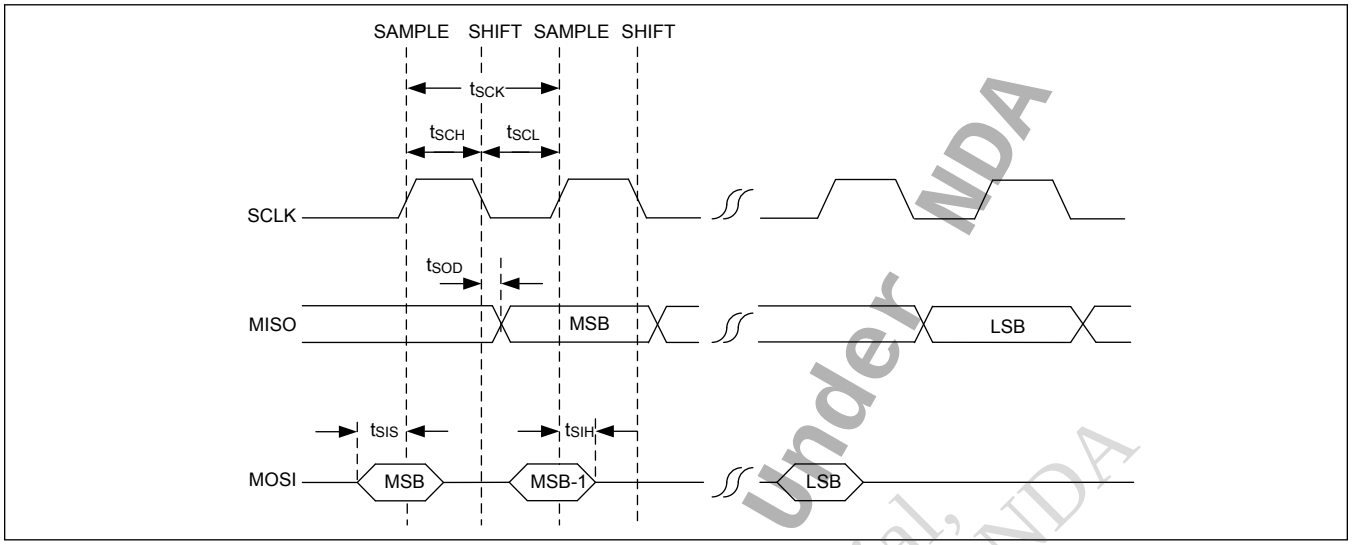

Figure 8. SPI Slave-Mode Timing Parameters

I²S Master-Mode Timing Parameters

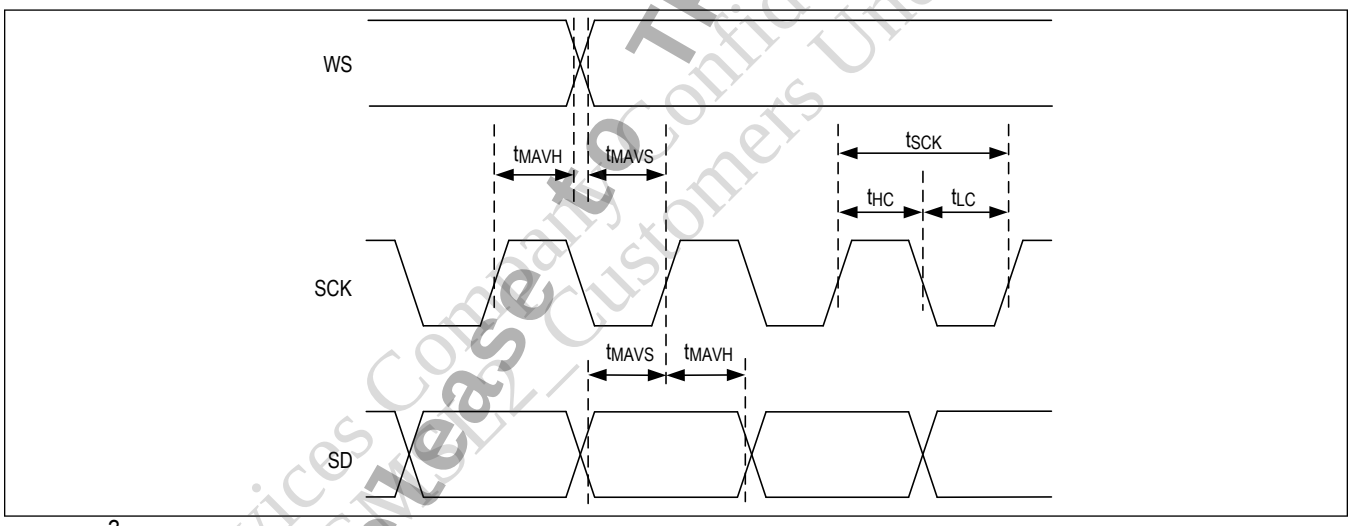

Figure 9. I²S Master-Mode Timing Parameters

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I²S Slave-Mode Timing Parameters

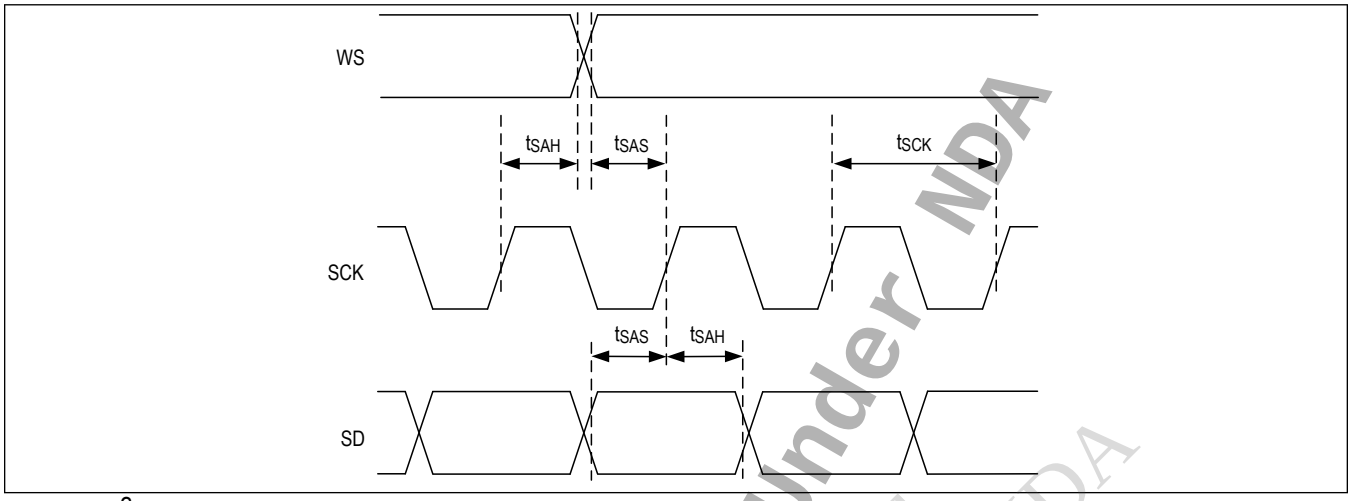

Figure 10. I²S Slave-Mode Timing Parameters

Detailed Description

Introduction

Gigabit Multimedia Serial Link™ serializers and deserializers provide high-speed, low bit-error-rate, serial-data transport supporting a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL3/2 provides fixed link rates of 12, 6 or 3Gbps forward, and 187.5Mbps reverse utilizing packetized data transmission.

The following sections provide a brief overview of the device features and functions. A more comprehensive GMSL user's guide, various application notes, and other collateral are available to assist in describing the features in more detail, with the associated implementation details. Contact the factory for this additional information and details on the configuration of each function and feature.

Product Overview

The MAX96749AC/749AP/767/769/855/857/859/861 convert a DP1.4 or eDP1.4a input interface to single or dual GMSL3/2 output. The DP interface supports PCLK rates from 6.5MHz to 820MHz uncompressed. The GMSL link, however, limits the achievable maximum PCLK rate per stream depending on individual use cases. See *Video Pipe Details*.

HDCP 1.4 and 2.3 encryption capability for each GMSL link is provided by the MAX96749AP/ MAX96769/ MAX96857/ MAX96861. After HDCP is configured, the authentication and key exchange are fully automated without requiring additional external ECU involvement.

DisplayPort

The MAX96749AC/749AP/767/769/855/857/859/861 serializers support DisplayPort 1.4 and embedded DisplayPort 1.4a input interfaces with lane rates of 1.62, 2.7, 5.4, and 8.1Gbps in 1-lane, 2-lane, and 4-lane configurations. They function as a DP sink device capable of supporting both Single-Stream Transport (SST) and Multi-Stream Transport (MST) modes (2-streams max). DP AUX and HPD interfaces are also supported.

These serializers also support VESA-compliant DSC compression passthrough, where the video source compresses the video stream and sends the compressed data to the serializer via the DP interface. The serializer receives the compressed stream and transports it over the GMSL link to the deserializer, which decompresses the stream and outputs on its video output interface.

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These serializers do not support the MST mode DP Topology Assistant and associated topology discovery, topology maintenance, EDID discovery, and messaging AUX client. Given the fixed nature of automotive infotainment platforms, the system topology, desired DP configuration, and Extended Display Identification Data (EDID) details of each display are known a priori. Thus, there is no need to support these functions. These features can be otherwise configured manually through appropriate register writes after initial device power-up.

The MAX96749AC/749AP/767/769/855/857/859/861 devices support legacy DP/eDP versions back to DP1.2 and eDP1.2.

GMSL3 12Gbps Link

The MAX96749AC/749AP/767/769 supports a GMSL2 link, which utilizes NRZ modulation at forward-link rates of 6Gbps and 3Gbps.

The MAX96855/857/859/861 devices additionally provide GMSL3 capability, which utilizes PAM4 modulation at a forward-link rate of 12Gbps. 12Gbps PAM4 modulation spectral content falls completely within that of the legacy GMSL2 mode with 6Gbps NRZ modulation. As a result, the same cables and connectors used in 6Gbps GMSL2 mode, provided they meet the GMSL3 channel specification, can be applied in GMSL3 applications.

Daisy Chaining

The MAX96859/861 support daisy-chained applications with up to four daisy-chained deserializers on each GMSL link.

Up to two video streams can be routed or replicated to either GMSL link, allowing the two streams to be routed downstream.

Daisy-chain deserializers select one of the two possible video streams to output locally. By default, the stream selected for the output of the daisy-chain repeater device is removed from the data to be forwarded to the next deserializer. Register programming can be used to change this behavior. The remaining video streams are repacked and forwarded downstream to additional deserializers in the chain.

Other Functions

The MAX96749AC/749AP/767/769/855/857/859/861 serializers have a main I^2C/UART control-channel interface that an Electronic Control Unit (ECU) uses to access serializer and deserializer registers, as well as peripheral devices, from either end of the link. Each device also has two pass-through I^2C/UART channels available for remote peripheral control. The pass-through I^2C/UART channels (PT1/PT2) do not have write access to serializer and deserializer registers. The PT1 control channel can however read serializer registers by default.

Two forward (serializer to deserializer) and two reverse (deserializer to serializer) audio channels are supported. The forward channel supports a single SST mode DP embedded audio channel or two I^2S/TDM audio streams from the local I^2S interfaces (Multifunction Pins (MFP)). Reverse I^2S/TDM audio channels are output to the local I^2S interfaces (MFP). The audio channels support I^2S stereo and up to 8 channels in the Time-Division Multiplexing (TDM) mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 bits to 32 bits.

Additionally, the MAX96749AC/749AP/767/769/855/857/859/861 include an SPI master/slave interface, including two slave-select pins, for peripheral control. The Serial Peripheral Interface (SPI) enables a host SPI master on one side of the GMSL link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link or can swap ends with reprogramming of the GMSL devices (a GMSL device can be configured as an SPI master or slave).

Up to 26 GPIOs are provided, depending on device feature utilization. GPIOs are typically used to tunnel low-speed (< 100kbps) signals over the GMSL link. A GPIO tunnel can be set up in the forward or reverse direction. It is also possible to locally read/write GPIOs instead of using the tunneling feature.

The devices include a video crossbar, which can be used to reorder the color and sync signals.

Watermark generation can used to detect frozen-frame failures. It inserts an invisible watermark in the video image, which is then checked by the deserializer.

The MAX96749AC/749AP/767/769/855/857/859/861 devices incorporate numerous link-margin optimization and monitoring functions to ensure high link margin. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging.

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DisplayPort Receiver

DP Sink Device

The MAX96749AC/749AP/767/769/855/857/859/861 function as DP sink devices supporting both Single-Stream Transport (SST) and Multi-Stream Transport (MST) modes (2-streams max).

They do not support the DP Topology Assistant and associated topology discovery, topology maintenance, Extended Display Identification Data (EDID) discovery, and messaging AUX client. Given the fixed nature of automotive infotainment platforms in the system topology, desired DP configuration and EDID details of each display are known a priori. Thus, there is no real need to support these functions.

DisplayPort Input Video Stream Formats

The MAX96749AC/749AP/767/769/855/857/859/861 DP inputs accept RGB666, RGB888, and RGB101010 (compressed only) data types in Single-Stream Transport (SST) and Multi-Stream Transport (MST) modes.

Pixel (column) interleaved streams can be split by the MAX96749AC/749AP/767/769/855/857/859/861. This is not done by the symmetric/asymmetric multiview engines, but by using the even/odd pixel splitter mode in the DP Receiver (DPRX).

The DP input also accepts VESA DSC compressed video (3:1 compression ratio for 24bpp and 3.75:1 compression ratio for 30bpp). There is a mechanism to pass the Picture Parameter Set (PPS) parameters from the DP source to deserializer devices, but not all deserializers support this mode. When not supported, the deserializer PPS must be loaded remotely through the serializer control channel or loaded locally at the deserializer through a local Electronic Control Unit (ECU), if so equipped. PPS through the AUX channel is not supported. As the serializers themselves do not support VESA DSC decompression and the messaging AUX client, additional measures must be taken to enable pass-through of the compressed data type to the appropriate deserializer with VESA DSC decompression features.

Configuring the MST Mode

Given the MAX96749AC/749AP/767/769/855/857/859/861 devices do not support the DP Topology Assistant and associated topology discovery, topology maintenance, EDID discovery, and messaging AUX client, modify the DP startup process as summarized in Table 5. The ECU should disable the topology manager.

Table 5. DisplayPort MST Setup

STEP	DESCRIPTION	INTERFACE	DIRECTION
1	Configure GMSL DP Serializer PHY setup. Configure DP (SST or MST mode, number of lanes, lane rates). Configure video pipe (configuration of various crossbars and feature sets within serializer video path) Configure video superframe splitting. Configure MST stream. Enable MST (asserting serializer MST enable bit).	I^2C	ECU → Serializer
2	Initiate DP link training.	AUX	ECU ⇔ Serializer
3	Clear and load DP serializer payload allocation table.	AUX	ECU → Serializer
4	Clear and load ECU payload allocation table.	–	ECU Only
5	Generate ACT trigger sequence.	DP Links	ECU → Serializer
6	Check for ACT trigger sequence recognition.	AUX	Serializer → ECU
7	Start MST video stream transmission.	DP Links	ECU → Serializer

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DP Link Training

MAX96749AC/749AP/767/769/855/857/859/861 link training is managed through AUX transactions from the DP source. Link training should be completed before the video is enabled. Link training recommendations are as follows:

- The MAX96749AC/749AP/767/769/855/857/859/861 devices are designed for use in embedded automotive applications where the link rate, lane count, and video resolutions are determined in advance (during system design), and strictly controlled by the DP source.
- Per the DP specification, if there are any link and/or signal integrity issues during the DP link training, the serializers properly signal to the DP source failures to obtain clock recovery, symbol lock, or lane alignment. The amplitude and/or pre-emphasis adjustment requests are issued if needed. If the link training fails after the amplitude/pre-emphasis adjustments, the serializer link training state machines stop and wait for further instructions from the DP source.
- Following a link training failure, consumer application DP sources proceed to reduce the lane count and/or link rate. The DP source program the reduced values into the sink and restart the training. As the link training is initiated and controlled by the DP source, the MAX96749AC/749AP/767/769/855/857/859/861 complies. While this is acceptable for consumer applications with flexible displays, in embedded applications with fixed displays/resolutions, DP sources should not perform the link rate and lane count reductions as it may cause insufficient link bandwidth for the video streams to be transported. In the embedded applications, the failure to complete the link training should be reported as a hard error signaling hardware issues and requiring engineering debug.
- Link training status can be checked through registers 0x6418 (link rate), 0x6419 (lane count), and 0x641A (training status). It can also be checked using DisplayPort Configuration Data (DPCD) registers located at 0x202, 0x203, 0x204, and 0x205.
- Contact the factory for additional information on DP link training constraints.

DisplayPort PHY

The MAX96749AC/749AP/767/769/855/857/859/861 support DP lane rates of 1.62, 2.7, 5.4, and 8.1Gbps in 1-lane, 2-lane, and 4-lane configurations. eDP/DP lanes can be remapped and/or phase inverted.

DP Main-Link Differential Input

The DP main link trace impedance must maintain a 50Ω characteristic impedance. 0.1µF DC blocking capacitors are also required.

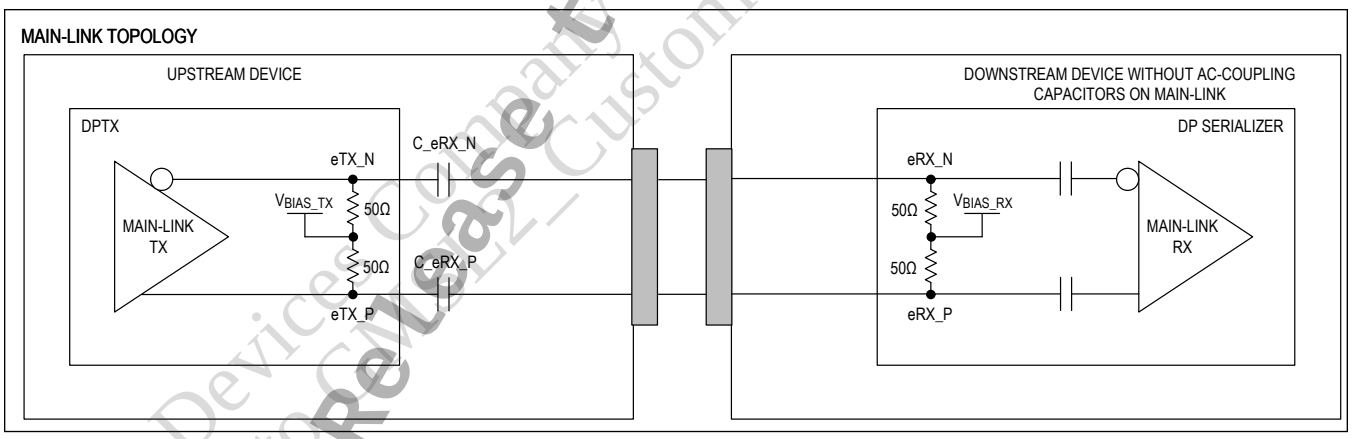

Figure 11. Main-Link Differential Pair

Spread Spectrum

Spread-spectrum modulation of the DP main link signal pairs is supported with a downspread of up to 0.5% at a modulation frequency of 30kHz to 33kHz. Spread spectrum is enabled by default during the link training sequence.

DP Content Protection

The MAX96749AC/749AP/767/769/855/857/859/861 support eDP Alternate Scrambler Seed Reset (ASSR) for display authentication and content protection.

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HDCP1.4 and 2.3 decryption is supported in the DP receiver. The serializer acts as a HDCP repeater devices, and the GMSL link provides encryption (HDCP 1.4 or 2.3) of individual video streams to the deserializer.. Each GMSL link (A or B) can have a maximum of two streams encrypted with HDCP. The same HDCP version (1.4 or 2.3) must be enabled for both streams on each link. Link-A and Link-B may use a different version of HDCP. The HDCP version must match between the DP link and GMSL link, it is not possible to mismatch versions between DP input and GMSL output.

AUX Channel

AUX channel read and write capabilities are supported in both native and I^{2}C over AUX modes.

DP Messaging AUX client functions are not supported.

AUX-Channel Differential Pair

The MAX96749AC/749AP/767/769/855/857/859/861 support both DP and eDP AUX channel interface configurations. However, they do not monitor the AUX_CH_P and AUX_CH_N common-mode voltage for source device hot plug/unplug and powered/unpowered detection. Therefore, ADI recommends only the use of the eDP AUX-Channel Differential Pair topology. Nevertheless, there may be special devices like test equipment, etc., that need the DP AUX channel configuration for one reason or another.

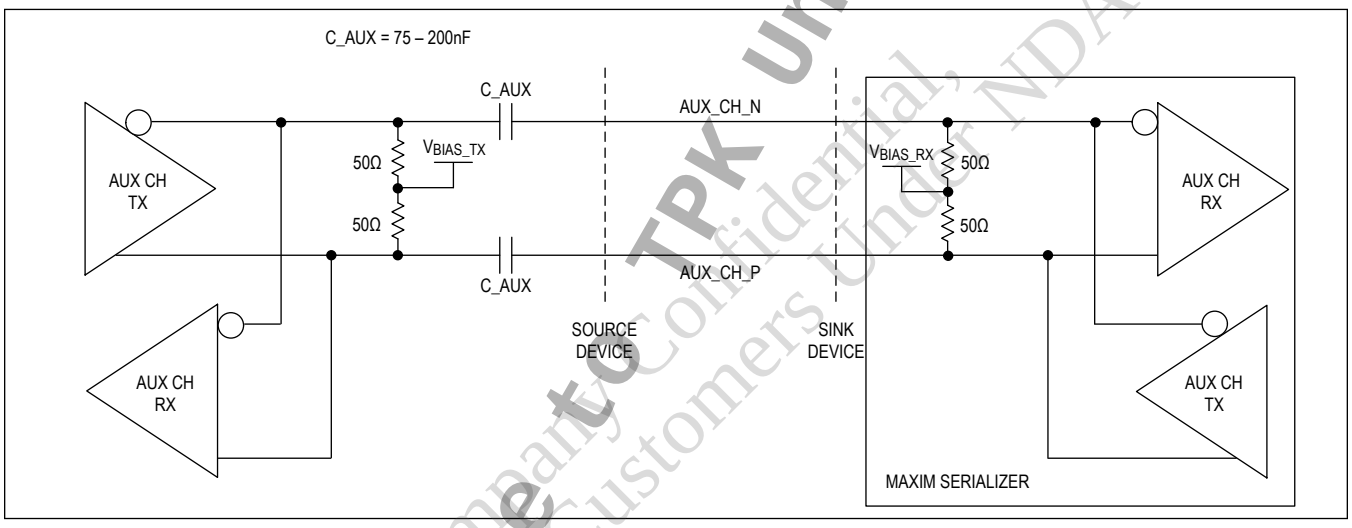

Figure 12. eDP AUX-Channel Differential Pair

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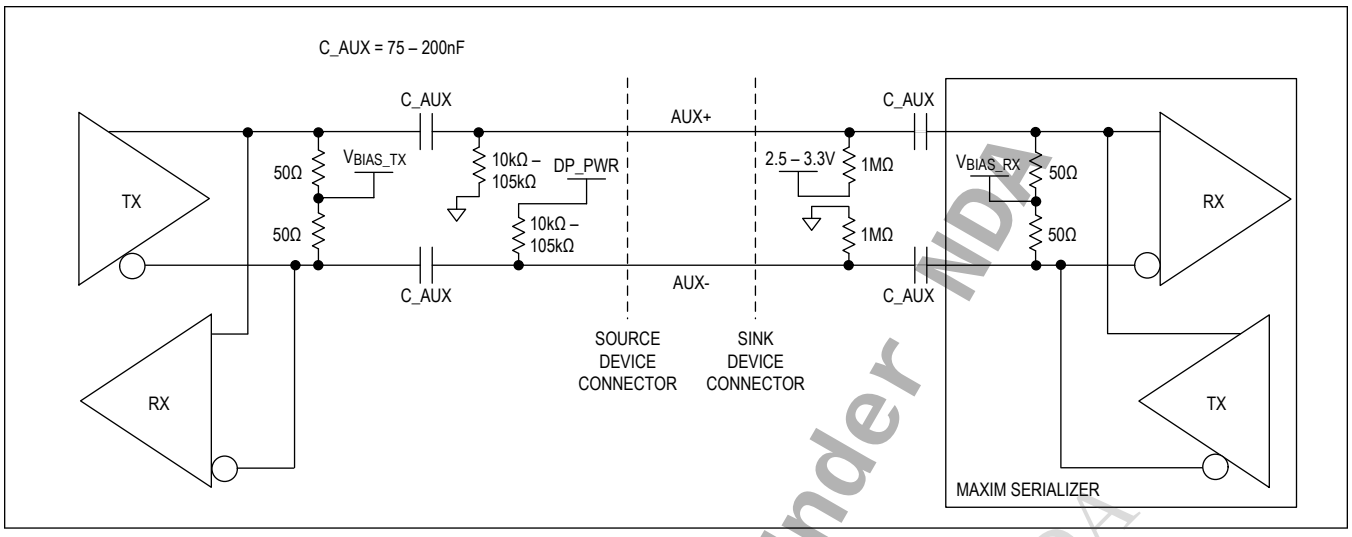

Figure 13. DP AUX-Channel Differential Pair

HPD Interface

The Hot-Plug Detection (HPD) pin supports both the hot plug detect and HPD IRQ functions. The HPD signal is asserted by the serializer whenever it is connected to its main power supply. During normal operation, the serializer may notify a link status change, for example, loss of synchronization, by toggling the HPD signal for interrupt request signaling.

Notes:

HPD pin output logic levels are referenced to V_{DDIO}. For the most robust operation, use the same supply voltage for the DP Source and the serializer V_{DDIO}. If different supply voltages are used, a level-shifting circuit may be required.

The MAX96749AC/749AP/767/769/855/857/859/861 IRQ_HPD pulse spacing can be less than 1µs. After receiving an IRQ_HPD pulse, the DP source must use a strategy to ignore subsequent pulses until it is ready to receive another one.

Audio-Related Secondary Data Packets

DisplayPort audio secondary data packets are supported for SST mode forward-channel audio. DP-embedded audio cannot be output locally at the serializer. The audio stream can be routed and/or replicated to both GMSL links, and all deserializers in a daisy-chain configuration can receive the DP embedded audio.

Extended Display Identification Data (EDID)

Extended Display Identification Data (EDID) is a standard communication method used by the DisplayPort to describe the video resolution and timings supported by a display. Without this data, the default resolution of 640 x 480 is all that can be supported. The MAX96749AC/749AP/767/769/855/857/859/861 devices contain two different EDID tables (read only and programmable) internal to the part. A user-supplied external source can provide the EDID table through one of the pass-through I²C ports. This is shown in Figure 14. The EDID feature is useful in SST mode applications when connecting to standard DP sources like laptops, in which the serializer appears like a standard DisplayPort display to the DP source. EDID is not needed for embedded automotive applications.

Three EDID sources can feed the I²C over the AUX channel.

1. Internal ROM with a preprogrammed EDID table containing timing information for 1920 x 1080 full HD with standard VESA timing.
2. Programmable RAM, with an address range 0x6500 to 0x65FF.
3. Pass-through control-channel pins (PT1 or PT2).

The EDP_VIDEO_CTRL2 (0x6422) register is used to select the EDID table to use and is also used in programming the RAM table. Assuming the RAM is programmed, to use the RAM, set bit 1, EDID_RAM_EN. To use the ROM (default), set bit 2, EDID_ROM_EN. If using an external EDID source, only set bit 0, EDID_READ_ONLY.

Contact the factory for details on programming the internal RAM EDID table.

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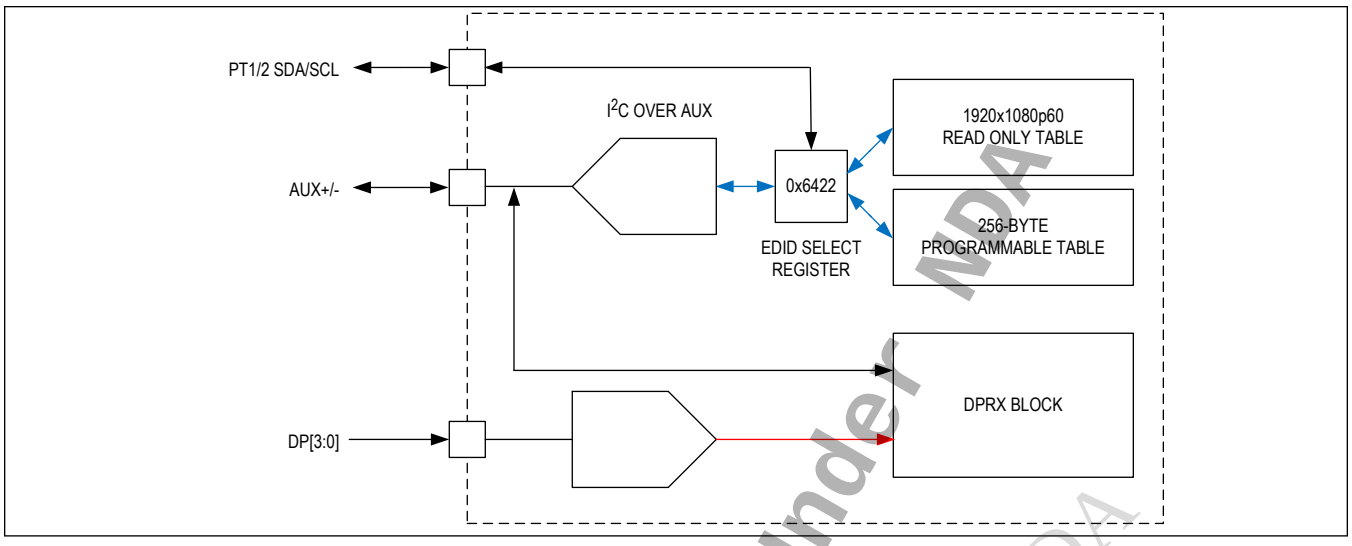

Figure 14. EDID Table Options

GMSL Protocol and Physical Layer

GMSL Protocol

GMSL3/2 is a fixed-rate transmission medium designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or external reference frequency. The link clock does not have any relation to the video pixel clock.

GMSL3/2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. The maximum packet size is limited to prevent a single channel from monopolizing the link bandwidth for an extended time and to ensure other channels are served. By design, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill the unused link bandwidth. The same data protocol is used on the forward and reverse channels, and for both video (forward path only) and bidirectional control channel data.

Legacy GMSL2 Device Backwards Compatibility

The MAX96749AC/749AP/767/769/855/857/859/861 are designed to pair with any legacy GMSL2 deserializer. All features of a given legacy GMSL2 deserializer may not be supported, however.

GMSL Physical Layer

Analog Devices' GMSL3/2 family of serial links has transmitter and receiver capability enabled simultaneously, allowing full-duplex operation on a single wire. A single cable between the serializer and deserializer delivers data being transmitted from each end of the link. Forward transmission is data being sent from the serializer to the deserializer. Reverse transmission is data being sent from the deserializer to the serializer.

Available forward-rate options for both Coax and STP links are fixed at 12, 6 or 3Gbps. The MAX96749AC/749AP/767/769/855/857/859/861 reverse-link rate is fixed at 187.5Mbps.

GMSL3 Mode

GMSL3 mode (MAX96855/857/859/861 only) utilizes PAM4 modulation at a forward-link rate of 12Gbps. When the configuration pins CFG[2:1] are used to set the channel mode, Forward Error Correction (FEC) is automatically enabled in the GMSL3 mode to provide robust communication. If GMSL3 is configured using register writes, FEC must be manually enabled. The system signal chain including PCB traces, connectors, and cables must meet the GMSL3 channel specification.

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GMSL2 Mode

GMSL2 mode utilizes NRZ modulation at forward-link rates of 6Gbps and 3Gbps. Forward Error Correction (FEC) is automatically disabled in GMSL2 mode, but can optionally be enabled. FEC should be enabled in compressed video pass-through applications. If sufficient bandwidth is available, enabling FEC in uncompressed applications increases link robustness. The system signal chain including PCB traces, connectors, and cables must meet the GMSL2 channel specification.

Cabling Options

GMSL3/2 devices support 50Ω Coax, 100Ω Shielded Twisted Pair (STP), or 100Ω Shielded Parallel Pair (SPP) cabling. Cable attenuation and return loss characteristics must stay within the requirements of the GMSL3/2 channel specification to achieve robust full-duplex link performance. These requirements vary with selected link rate. The available link rates and GMSL3/2 adaptive equalization enable support of a wide range of cabling options.

Coax or STP operation of the GMSL links is determined by the voltage at the CFG1 (Link-A) and CFG2 (Link-B) pins at power-up, and determine which cabling option applies. See Table 12. In the Coax mode, use only the SIOAN/SIOA or SIOBP/SIOB pin. AC-couple and terminate the unused SIOAP or SIOBN pin using the series connection of a 100nF capacitor and a 49.9Ω resistor. In the STP configuration, both the non-inverted (SIOAP and SIOBP/SIOB) and inverted (SIOAN/SIOA or SIOBN) pins are enabled by default.

Maximum cable length is limited by the frequency-dependent attenuation of the cable. Additionally, PCB and inline connectors degrade the return loss characteristic of the cable assembly. The GMSL3/2 channel specifications allow two inline connectors, and provide detailed requirements for cable attenuation and return loss, as well as insertion loss and return loss requirements for PCB traces. In general, any physical channel implementation compliant with the GMSL3/2 channel specification can be used with reliable results. Contact the factory for the GMSL3/2 channel specification document.

Short Channel Use Cases

GMSL3 mode SerDes use Feed Forward Equalization (FFE) to support a -18dB insertion loss channel at a 12Gbps rate. The FFE gain is based on the coax/STP configuration selected using the (CFG[2:0]) pins. Some applications use very short channels. For example, a short PCB track (< 3 inches) or a short cable (< 1m STP.) In these cases, the combination of the fixed FFE and receiver frequency response leads to an over-equalized operating point. The over-equalized condition leads to higher FEC input BER and a lower link margin solution than if FFE were disabled.

For these extremely short channels, i.e., insertion loss < 2dB, disable Feed-Forward Equalization (FFE) by writing register RLMSCE to 0x00 (0x14CE for Link-A and 0x15CE for Link-B).

GMSL Link Configurations

The MAX96749AC/749AP/767/769/855/857/859/861 devices have multiple and independent GMSL Link-A/-B configuration options. The CFG1 (Link-A) and CFG2 (Link-B) latch-on power-pin functions set both links independently at power-up. It is also possible to independently select link rate and cable type for Link-A and Link-B through post-power-up register writes.

Dual Link and Even/Odd Pixel Splitter Mode

The MAX96749AC/749AP/767/769/855/857/859/861 devices support 6Gbps dual lane mode to establish a 12Gbps virtual link to Maxim's GMSL2 deserializers with dual lane mode support.

In even/odd pixel splitter mode mode, the video core processes two pixels every clock cycle. The two pixels, even and odd, are routed to separate video pipes, even pixels in one video pipe and odd pixels in another. Each video pipe can be independently routed to each GMSL link. All video parameters (line length, line blanking, etc.) are divided by two, as well as the pixel clock.

Line Fault

The MAX96749AC/749AP/767/769/855/857/859/861 include a novel line-fault detection circuit. It detects and reports open-circuit, short-to-battery, short-to-ground, and line-to-line short. The line-fault monitor is disabled by default and enabled through bits PU_LF3:0 in register REG5. Registers LF0_LF1 and LF2_LF3 provide line fault status. If unmasked, a line-fault condition asserts ERRB. Line-fault detection cannot be used in applications with Power over Coax (PoC) or

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AC-coupled grounds.

The line-fault monitor pins offer flexible connection and programming in either Coax or STP applications. See Figure 15 and Figure 16. The monitor requires external resistors R_{EXT1} and R_{PD} in Coax mode, and R_{EXT1}, R_{EXT2}, and R_{PD} in STP mode connected to the LMNx pins. See Table 6 and Table 7.

The LMNx connections are provided as options on multifunction pins MFP4, MFP5, MFP19, and MFP20. See the *Pin Descriptions* table and Table 15.

Coax Mode

In Coax applications, any LMNx pin may be used. The MAX96749AC/749AP/767/769/855/857/859/861 source the line-fault monitor. The serializer board requires a single 48.7kΩ resistor (R_{EXT1}) connected directly from any of the LMNx pins to the serial link. R_{EXT2} is not used in Coax applications. The deserializer end of the serial link requires a 49.9kΩ resistor (R_{PD}) connected from the serial link to GND. Any of the line-monitor pins may be used in Coax applications.

Table 6. Coax Mode Line-Fault Configuration Options

SIGNAL	SIOAN/SIOA PIN	SIOBP/SIOB PIN
Line-Fault Pin	LMNx (Any LMN pin)	LMNx (Any LMN pin)
R_{EXT1}	48.7kΩ	48.7kΩ

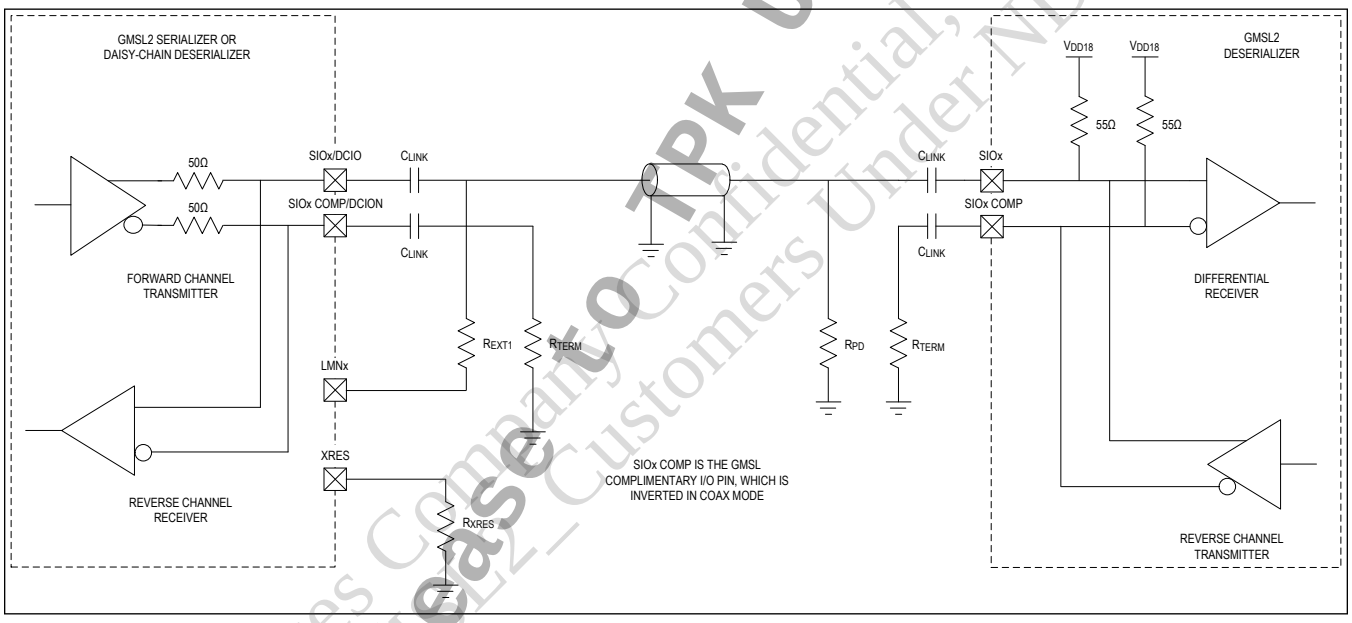

Figure 15. Typical GMSL Link Application Circuit for Coax Cable

STP Mode

If the serial link is operating in twisted-pair mode, connect one line to an even-numbered pin (LMN0/2) and the other line to an odd-numbered pin (LMN1/3) at the serializer. For reliable line-fault detection, the even-numbered pins (i.e., LMN0 and LMN2) must be connected to the line using a 42.2kΩ resistor (R_{EXT2}). The odd-numbered pins (i.e., LMN1 and LMN3) must use a 48.7kΩ resistor (R_{EXT1}) to connect to the line. On the deserializer end, both lines require a 49.9kΩ resistor (R_{PD}) connected to GND.

For full operation of line-fault detection in twisted-pair applications, ensure either LMN0/1 or LMN2/3 pairs are used. This pairing is required for proper operation of the line-to-line short detection; however, this pairing is not necessary for the detection of other fault conditions.

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Table 7. STP Mode Line-Fault Configuration Options

LINE-FAULT PAIR	OPTION	SIOAN/SIOA PIN	SIOAP PIN
LINE-FAULT PAIR #1: LMN0 AND LMN1	Option #1	LMN0: R_{EXT2} = 42.2kΩ to serial link	LMN1: R_{EXT1} = 48.7kΩ to serial link
	Option #2	LMN1: R_{EXT1} = 48.7kΩ to serial link	LMN0: R_{EXT2} = 42.2kΩ to serial link
LINE-FAULT PAIR #2: LMN2 AND LMN3	Option #1	LMN2: R_{EXT2} = 42.2kΩ to serial link	LMN3: R_{EXT1} = 48.7kΩ to serial link
	Option #2	LMN3: R_{EXT1} = 48.7kΩ to serial link	LMN2: R_{EXT2} = 42.2kΩ to serial link

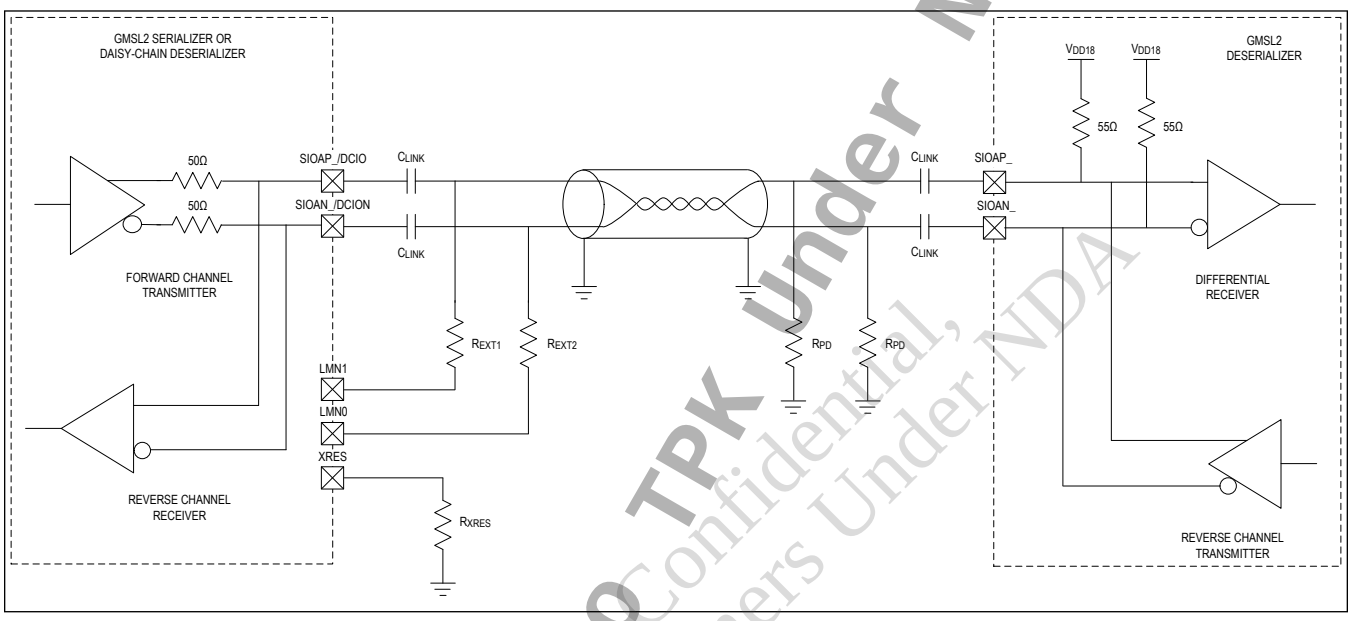

Figure 16. Typical GMSL Link Application Circuit for Twisted Pair

Line Fault in AC-Coupled Ground Applications

Use of the line-fault function is NOT recommended in applications with a floating cable shield. Contact the factory for details.

GMSL Link Polarity Inversion

In Shielded Twisted Pair (STP) applications, the device allows the SIOAP and SIOAN/SIOA pins, and the SIOBN and SIOBP/SIOB pins to be swapped for inverted polarity. This might be used to ease routing and achieve better signal integrity while designing PCBs. Contact the factory for configuration details.

It is, however, not possible to swap GMSL outputs in Coax use cases. Only the SIOAN/SIOA and SIOBP/SIOB pins may be used in the Coax mode. Incorrect connection of the Coax pin in the case of a design/layout mistake is acceptable for test purposes, but such mistakes must be corrected to be compliant with the GMSL2 channel specifications. Contact the factory for support.

GMSL Link Forward Error Correction (FEC)

Forward Error Correction (FEC) is increasingly required to handle errors in high-speed links. The primary need for FEC on the GMSL2 links is the pass-through of compressed video. Errors on a compressed video stream corrupt far more pixels than errors on an uncompressed stream. FEC has been implemented on devices that support GMSL2 mode and compressed data types to ensure that corrupted video will not be seen by the user on a link that passes the channel specification. FEC is also enabled on GMSL3 links by default to provide superior bit error rate performance.

Features:

- Burst-error correction capability equivalent to three FEC symbols (54 bits) per FEC block.

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- Debug capability to enable analyzing quality of received data.
  - Reports number of blocks processed, errors corrected and if it occurs, the number of uncorrectable errors.
  - Optional ERRB Interrupt output on deserializers when corrected or uncorrectable errors exceed 32-bit programmable threshold.

Notes:

- Correction is available for all data traffic in the GMSL lanes supporting FEC.
- Enabling FEC increases the required link bandwidth for video, and all forward control and side-channel data by a factor of 128/120 (approximately 6.7%).
- FEC adds approximately 4300 UI latency to the link.

Spread-Spectrum Clocking

Analog Devices' GMSL links provide exceptional EMI performance. Optional Spread-Spectrum Clocking (SSC) is available to mitigate electromagnetic interference emitted from devices and interconnections, and provide additional margin. SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to ±1250ppm from the center frequency. Contact the factory for more information.

AC-Coupled Cable Ground Applications

Twisted pair links for GMSL channels can experience static or dynamic ground voltage shifts between one Electronic Control Unit (ECU) or display and other ECUs in a vehicle system. Static differences in ground voltage causes current to flow in the cable shield if it is grounded at both ends. In the case of a failure, such as a ground disconnect, the shield may carry the current of both the ECU1 and ECU2. This can result in amperes of current in the shield. The concept is illustrated in Figure 17.

To avoid the impacts this can have on EMI, EMC, and signal integrity, Analog Devices has specific recommendations for AC-coupled cable ground applications including component selection and layout recommendations for a circuit that reduces the impedance between the shield and digital (ECU) ground. Doing this provides a return path for the offset current that best mitigates the negative impacts of the effect. Contact the factory for associated applications notes and technical support.

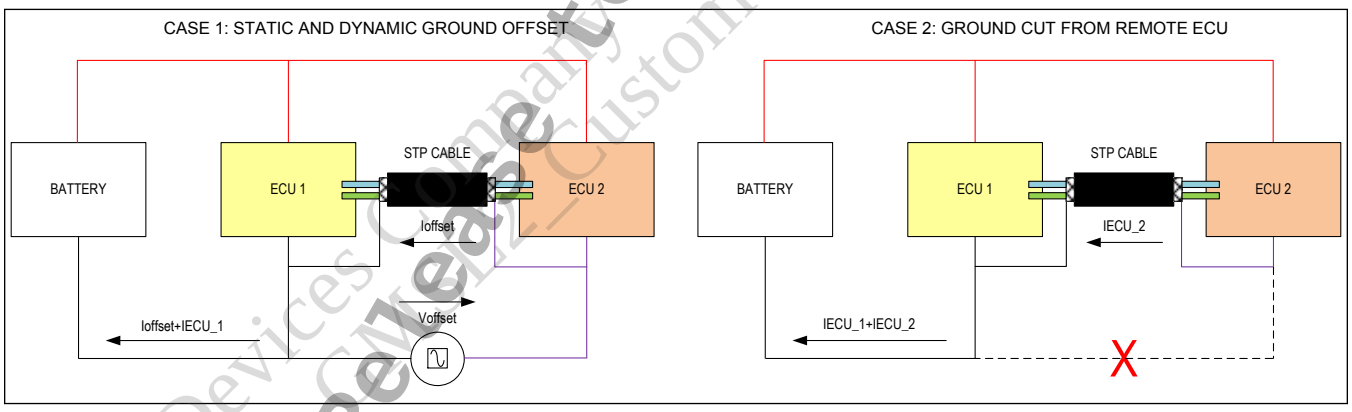

Figure 17. AC Ground Problem Description

GMSL Bandwidth Sharing

The GMSL forward bandwidth is shared among the video, main I²C/UART control channel, pass-through I²C/UARTs, I²S/TDM audio, SPI, SGMII, and GPIOs, plus various protocol-specific data exchanges (i.e., info frames, sync, and acknowledgements). The reverse-channel bandwidth is also shared with all of the above except video packets. The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth in either direction.

Link bandwidth is shared flexibly between the various communication channels requesting the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation: if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active

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communication channels to share. The packet-based protocol fulfills this sharing requirement.

The video and control-channel packets can be assigned one of four priority levels: low, normal, high, or urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with maximum latency requirements can be assigned an increased priority.

GMSL Bandwidth Calculations

Ensure the worst use cases do not exceed the available throughput of the forward and reverse links. The Evaluation Kit (EV kit) GUI includes a bandwidth (BW) calculator for initial bandwidth requirement estimates. Analog Devices also has other tools to calculate link bandwidth utilization. Consult the factory for high bandwidth use cases to ensure error-free performance.

Table 8 provides accurate estimates of the bandwidth utilization for each communication channel.

Table 8. Forward-Link and Reverse-Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Display Video (Forward Path Only)	**Without VESA DSC** PCLK * (bpp + 0.5 + packet_crc) * 10/9 * 2048/2047 * 128/120† (†only applies when GMSL FEC is enabled) With VESA DSC PCLK * 1/3 * (bpp + 0.5 + packet_crc) * 10/9 * 2048/2047 * 128/120 (GMSL FEC is required with VESA DSC com)
I^2C	(18 to 60) * I^2C clock rate, depending on available link bandwidth
UART	6 * (UART bit rate) with parity bit enabled 5 * (UART bit rate) with parity bit disabled
SPI	(1.7 to 3.1) * SPI rate
GPIO	60 * GPIO transition rate without delay compensation 80 * GPIO transition rate with delay compensation
I^2S/TDM	ws_freq * roundup ((bps * channel_cnt + 27)/18) * 20
100Mbps Ethernet	(132Mbps to 140Mbps) * utilization, depending on REQ hold off ratio

Note: Bandwidth utilization for all forward control channel and side channel communication increases by 6.7% when Forward Error Correction (FEC) is enabled.

Definitions:

PCLK = (total horizontal pixels) x (total vertical lines) x (frame rate). Total horizontal pixels and vertical lines include blanking.

bpp = Bits per pixel

packet_crc = 0.5 when video packet CRC is enabled; = 0 when video packet CRC is disabled (default).

ws_freq = Word select frequency

bps = Bits per sample, per audio channel (must be the same for all channels)

channel_cnt = Number of audio channels

utilization = percent of ethernet payload capability used. Equal to 1 for 100% ethernet channel loading.

REQ Hold off = Minimum number of extra bytes required in the ethernet transmit buffer prior to requesting transmission over the GMSL link. Register programmable.

Video Pipe Details

Bandwidth Support

The four-lane DP input running at HBR3 (8.1Gbps/lane) supports up to 1080 MHz total PCLK in 24-bit color and 864 MHz at 30-bit color. The MAX96749AC/749AP/767/769/855/857/859/861 have some constraints on how this bandwidth

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is used:

- 6.5MHz to 215MHz PCLK uncompressed 24bpp video over single GMSL2 link
- 6.5MHz to 410MHz PCLK uncompressed 24bpp video over single GMSL3 link
- 6.5MHz to 430MHz PCLK uncompressed 24bpp video over dual GMSL2 links
- Max PCLK of 820MHz uncompressed video in Even/Odd Pixel Splitter Mode (GMSL3)
- Max PCLK of 1080MHz compressed video at 24bpp and 864MHz at 30bpp (GMSL3)

Dynamic video routing:

- Individual streams from the DP can be routed to video pipes in the MAX96749AC/749AP/767/769/855/857/859/861 but not on a GMSL link. The displayed stream can thus be dynamically switched by changing the pipe(s) connected to the GMSL link(s).

Video-Line CRC

Video data integrity over the GMSL link is protected by Video-Line Cyclic Redundancy Check (CRC). A CRC32 polynomial is used to generate an optional 32-bit code at the end of each DE or HS pulse. This code is transferred to the deserializer using info frames. The deserializer CRC checker generates a code using the same polynomial, and checks if the generated and received CRC codes are the same. If not, it asserts an error. The CRC check is done at every falling edge of DE in the deserializer, even if the info frame is not received.

End-to-End Video Line CRC

The data path from the serializer DisplayPort input to the GMSL deserializer is CRC-protected for data integrity. For safety purposes and to meet a certain Automotive Safety Integrity Levels (ASIL), data is protected in three stages: 1) The DP receiver has an 8b/10b coding error detection mechanism for the received input. Errors can be reported to the interrupt (ERRB) output. 2) The signal path from DP receiver output to the GMSL link is covered by a CRC-protection mechanism. This starts from the output of the DP Receiver up to the input of video transmit block. It covers the large line memories. It is a video frame-based CRC. The CRC for each video frame is calculated at the output of the DP receiver and then recalculated before the video transmit block. The two CRC results are compared, and errors can be reported to the interrupt (ERRB) output. 3) Finally, the video data path over the GMSL link is covered by line-CRC and frame-CRC mechanisms that report errors detected by the deserializer. Interrupts from the deserializer can be communicated to the serializer using GPIO tunnels.

Video-Timing Generator

The Video-Timing Generator (VTG) is an auxiliary function that can substitute HS, VS, and DE signals with signals it generates as defined by the configuration registers. The VTG can generate almost any type of SYNC-signal set pattern in various modes to start the generated patterns. The VTG can generate a test pattern at any resolution with internally-generated clocks.

Video-Pattern Generator

The Video-Pattern Generator (VPG) is also an auxiliary function that can be used for various purposes. If desired, video from the peripheral can be replaced by the video pattern generated by the VPG. The VPG can be configured to generate various RGB888 patterns. It can generate a test pattern at any resolution with internally-generated clocks.

Video Color Crossbar

Data from the video input is captured and optionally multiplexed with the generated patterns from the VTG or VPG. Final data goes into a crossbar multiplexer that allows any input bit to be mapped to any output bit using the configuration registers. The crossbar can be used to reorder the color and sync signals.

Each video pipe has a separate video crossbar and each crossbar has its own configuration registers. If multiple crossbars exist, configuration register names have _X and _Y extensions indicating the video pipe to which they belong. CROSS[29:0] registers are used for video data crossbar settings. It is possible to have one crossbar input connected to multiple outputs.

Watermark Generator

Watermarking can only be applied to RGB888 data. This feature specifically detects frozen frames caused by the ECU

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in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector.

MAX96749AC/749AP/767/769/855/857/859/861 serializers provide a watermark generator for each video pipe and most GMSL2 deserializers provide a watermark detector. The watermark generator inserts into the video stream an invisible, time-varying watermark that is highly redundant and robust to image processing. The watermark detector looks for this time-varying watermark, and failure to detect all the generated watermarks indicates a frozen-frame failure between the generator and detector. Upon detection of this error condition, the watermark detector can generate an interrupt and/or blank the output video, returning the display to a safe state in less than 500ms.

PRBS

The MAX96749AC/749AP/767/769/855/857/859/861 include both Video and Audio Pseudorandom Binary Sequence (PRBS) generators to support link diagnostic functions.

Video PRBS

The video channel has a PRBS generator in the serializer and a PRBS checker in the deserializer to test the video channel operation. The video PRBS generator can work with the recovered PCLK received from a DP input. An external PCLK can also be provided to a designated GPIO pin to run the video PRBS generator. Note that all link bandwidth is not used by the video channel alone in the GMSL mode. So, it is possible to have a bit error on the link that does not cause a video PRBS error.

Audio PRBS

The audio channel includes a PRBS generator on the transmitter side and a checker at the receiver side to test the audio channel operation. The audio PRBS generator can operate using the incoming I^2S SCK and WS signals, or use an internally-generated reference clock. When audio PRBS generation is enabled, the channel is reset unless the WS and SCK are used from the I^2S inputs. The detected audio-channel bit errors are reported through a status register.

Video Authentication, Regional CRC, and Frame CRC

MAX96749AC/749AP/767/769/855/857/859/861 include a data path feature that can process video frames and generate various information such as the signature of a full-frame and dynamically changing or static partial frame regions. Contact the factory for application notes describing the region/frame CRC features and video authentication feature. These functions are supported by select GMSL deserializers.

Video Authentication

The control channel master of the MAX96749AC/749AP/767/769/855/857/859/861 can receive secure challenges from an authentication master in the vehicle. In turn, it can define dynamically changing rectangular region on an image frame. The serializer and deserializer can provide the signature for the programmed regions of the same video image on both ends of the video link. The authentication master can collect the signatures from the head unit and displays using the control channel masters, and compare them to determine if the head unit and the displays are authenticated for use within the vehicle.

Region-Based CRC

The video authentication module in the MAX96749AC/749AP/767/769/855/857/859/861 and deserializer can be repurposed to use static frame region definitions to provide a signature for a specific region on the image. The ECU can compare these signatures with the signature it generated to verify that critical images such as the telltale safety icons are present in the transmitted video stream. Up to four regions can be defined and compared within a frame. Contact the factory for more information.

Full-Frame CRC

The serializer and deserializer generate frame CRC signatures at the end of each video frame. The signatures can be read through registers. The MAX96749AC/749AP/767/769/855/857/859/861 also transmit CRC signatures to the deserializer using info frames. The deserializer continuously compares its CRC signature to the one received from the serializer and generates an interrupt if there is a mismatch.

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Minimum Blanking and Other Video Limits

The MAX96749AC/749AP/767/769/855/857/859/861 have minimum horizontal and vertical blanking requirements for video streams:

- Vertical blanking: Minimum six lines.

Consult the factory for guidance on blanking for specific resolutions.

For other video related features such as video-line CRC, video-frame CRC, and SHA256-related functions (video authentication), there are some additional minimum blanking constraints:

- Video: Minimum vertical blanking six lines.
- Line CRC: Minimum line length 256 pixels, minimum horizontal blanking 6 pixels.

For HDCP 1.4/AHDCP, minimum HSYNC pulse width 32 pixels.

Video Timing Signal Outputs

The MAX96749AC/749AP/767/769/855/857/859/861 can output video stream PCLK, HS, VS, and DE timing signals on the MFP23-MFP25 pins. Timing signal outputs are enabled by programming HVD_OUT_EN = 1. The specific video stream to be monitored and the tap point within the signal path are specified by the DEBUG_EXTRA register. Program the edge rates of the MFPs used for the timing outputs to their fastest settings (TTS = 00) when outputting the timing signals. See Table 16.

- DEBUG_EXTRA[3:2] selects the video pipe (X,Y).
- DEBUG_EXTRA[1:0] selects the stage where HS/VS/DE is tapped:
  - 0x = DPRX output
  - 10 = FIFO output
  - 11 = VTX output

HDCP

High-Bandwidth Digital Content Protection (HDCP) is an encryption scheme to protect digital audio and video content in various protocols. The supports HDCP 1.4 and 2.3 on the GMSL link and DP input link.

For power savings, the HDCP circuits are powered down by default. Once HDCP is enabled, the function powers up and authenticates, after which link integrity checks are periodically performed by the hardware through a dedicated control channel over the GMSL link. HDCP interrupts can be generated and status registers provide status of authentication progress indicating success and a ready state to the upstream video source.

Each HDCP device has a factory-programmed unique device ID called a Key Selection Vector (KSV) and associated private keys. They are licensed from DCP LLC.

HDCP capabilities differ among GMSL1 and GMSL2 devices. Contact the factory for information.

DisplayPort HDCP Repeater Support

An HDCP repeater receives and decrypts HDCP content, and then encrypts and transmits on one or more downstream links. The MAX96749AP/ MAX96769/ MAX96857/ MAX96861 supports HDCP repeater mode from the DP receiver to the GMSL transmitter.

Automatic HDCP Operation

The includes an automatic HDCP feature that fully automates the GMSL link HDCP 1.4/2.3 key-exchange authentication without requiring external µC involvement. Authentication and link-integrity checks are done by the hardware using a dedicated control channel over the GMSL link.

GMSL HDCP 1.4 has an optional fast mode to perform a link-integrity check every frame. This reduces the video out-of-encryption synchronization duration to as low as two frames.

HDCP and GMSL Link Configurations

The GMSL links support HDCP 1.4 and 2.3. Each GMSL link (A or B) can have a maximum of two streams encrypted with HDCP 1.4 or 2.3. The same HDCP version (1.4 or 2.3) must be enabled for both streams on each link. Link-A and Link-B may use different versions of HDCP. A summary of the HDCP and GMSL link rules follows:

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- Both GMSL links support HDCP 1.4 and 2.3 independently.
- Only a maximum of two streams can be HDCP enabled on each link.
- Each stream on a link can be HDCP enabled or not independently.
- If enabling two streams on a link, they must both be HDCP 1.4 or 2.3. There cannot be a mix of HDCP version on a link.
- HDCP versions can be different between GMSL Link-A and Link-B.

Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL serial link simultaneously with high-speed video data. GMSL2 devices support most or all of the following interfaces:

- Main I^{2}C/UART (internal access)
- Pass-Through I^{2}C/UART
- SPI
- GPIO
- I^{2}S/TDM Audio

Data from all these interfaces tunnel through the GMSL link. By default, the GMSL serializer and deserializer registers can only be accessed and configured through the main I^{2}C/UART interface.

The side channel, with its various interfaces, is accessed using multifunction GPIO pins (called MFPs on MAX96749AC/749AP/767/769/855/857/859/861). Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit on the number of pins available on a given device, not all interfaces can be simultaneously supported. See Table 15 and the *Pin Descriptions* section for default and alternate multifunction pin functions, as well as available combinations of interfaces.

Main I^{2}C/UART

The main I^{2}C/UART is located on the SDA_RX and SCL_TX pins of each GMSL device. The I^{2}C (SDA, SCL) or UART (Tx, Rx) interface is selected by the CFG configuration pin state at power-up (see Table 12). The selected interface provides master access to GMSL device registers, as well as peripheral device registers, from either end of the link.

The master ECU can be located on either end of the link (usually the serializer side for display applications and deserializer side for camera applications). Dual-master ECU controllers are supported, wherein DIS_REM_CC settings can disable the remote CC communications from each ECU being sent to both ends of the link. The status of the DIS_REM_CC pin is only checked at power-up and is applied to both links. After power-up, the state of DIS_REM_CC can be set individually for each link using bit field DIS_REM_CC in registers I2C_6. Optionally, software arbitration (such as token passing) can be used to prevent packet collisions.

The GMSL2 or GMSL3 serializer and deserializer must use the same control-channel interface (both I^{2}C or both UART), as do any peripheral devices connected to the main I^{2}C/UART. Unlike GMSL1 devices, there is no I^{2}C-to-UART conversion capability. I^{2}C/UART outputs are open-drain and require appropriately sized external pullup resistors for proper operation.

For detailed main-channel programming information, see the *Applications Information* section of this data sheet.

Multimaster I^{2}C Operation

When the MAX96749AC/749AP/767/769/855/857/859/861 are connected to more than one deserializer in , they can arbitrate and process I^{2}C packets from I^{2}C masters (µCs) connected to each deserializer. I^{2}C packets from each µC are processed in the order they are received, and the non-selected I^{2}C masters are put on hold using clock stretching by the respective deserializer.

Multimaster I^{2}C operation is available on the main I^{2}C channel and pass-through channels.

Main I^{2}C/UART Control-Channel CRC

For improved ASIL-B functional safety requirements at the system level, there must be a mechanism to prevent hardware faults or random errors from misconfiguring the device. The MAX96749AC/749AP/767/769/855/857/859/861 include CRC for I^{2}C and UART transactions, which operate in concert with compatible deserializers. The serializer I^{2}C/UART slave controller expects and validates a CRC-8 byte for all communication messages to maintain data integrity. This

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ensures the proper write data is received and the device is configured properly.

The serializer and deserializer(s) include a single counter incremented for both write and read transactions. Each device's counter increments only when the ECU transaction is for that particular device (when the I^{2}C device address matches that device). Therefore, the ECU needs to maintain separate transaction counters for the serializer and each deserializer, and send the appropriate counter value when writing to each device.

By default, the I^{2}C/UART CRC and Message Counter feature is disabled. Legacy I^{2}C/UART packet format is the default. When desired, these functions can be enabled by a register write by using the legacy packet format. All subsequent packets then use the I^{2}C/UART CRC feature.

Control Register CRC

Control Register CRC is a functional safety feature to ensure the MAX96749AC/749AP/767/769/855/857/859/861 are not placed into an undesired state through a fault.

Once the serializer is programmed, the Control and Status Register (CSR) bank is protected by a CRC calculation. After the serializer is set up through the CSR, the values should not change while the device is operating. Any change is considered a fault and ERRB is asserted if the OEN for Register CRC Flag is enabled. The serializer can report if the CSR values change due to faults (e.g., soft errors.). Alternately, the CRC value can be polled by the ECU to check for changes.

There are two modes: Basic CRC and User-Polling CRC.

Basic CRC Mode

The CRC is calculated iteratively on the CSR and a 16-bit CRC is written into registers REGCRC_MSB/REGCRC_LSB. Additionally, this value is logged internally. Periodically, the CRC is recomputed and compared with the stored value.

Procedure:

1. Functional registers are programmed.
2. Register CRC is set up:
   a. The I2C_WR_COMPUTE bit is written.
   b. The CRC_PERIOD register is written, which allows the period to be calculated with ~2ms to ~512ms.
   c. The PERIODIC_COMPUTE bit is written.
   d. The CHECK_CRC bit is written.
3. This causes a new CRC to be calculated and compared with the previously-computed CRC. Any mismatches result in ERRB being indicated.

User-Polling CRC Mode

This mode calculates an incrementally changing CRC. In this case, the same CRC as above is calculated, with the addition of computing the CRC using the value from a periodically incrementing 2-bit counter. The CRC value changes periodically, with the values repeating with a period of four. This mode guards against 'frozen' CRC calculation logic.

Procedure:

1. Functional registers are programmed.
2. Register CRC programming is done as above.
   a. Additionally, GEN_ROLLING_CRC is set.
3. The CRC calculation is deposited in the REGCRC_MSB/LSB registers, and the ECU can periodically poll this value to check the CRC calculation is advancing as predicted.
   a. The ECU sees the CRC values repeat and knows the registers are remaining unchanged.

Note that in this mode, ERRB is not indicated as the CRC value is changing periodically, and the usage mode is to have the user poll the CRC register.

Daisy-Chain Communication

All MAX96859/861 main control and side channels (video, I^{2}C, UART, I^{2}S/TDM, DP Audio, and GPIOs) can be directed to all the deserializers in a chain. The deserializers can only direct return channel data to the serializer. The deserializers cannot communicate directly with each other. It is, however, possible for the deserializers to communicate with a

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turnaround of the data within the serializer. A µC connected to a deserializer can access another deserializer's registers or peripherals if a loopback through the serializer is programmed. Various loopback, cross connections, and access to device register settings are available for the main control channel and pass-through control channels. Serializer turnaround is available by a register write on the main CC or PT1, PT2 channels. For example, deserializer-x may send a message through I^{2}C to deserializer-y by first sending the request on the return link to the serializer, wherein the serializer resends the message on the forward link to deserializer-y. Contact the factory for information.

Pass-Through I^{2}C/UART

Most GMSL2 devices have two pass-through I^{2}C/UART channels (PT1/PT2). These channels do not have write access to registers in the serializer or deserializer; they simply tunnel the I^{2}C or UART signal across the GMSL link. This can be useful to separate I^{2}C channels so that multimaster conflicts do not occur. The MAX96749AC/749AP/767/769/855/857/859/861 cannot arbitrate conflicts if multiple deserializers use the same pass-through channel. I^{2}C/UART outputs are open-drain and require appropriately-sized external pullup resistors for proper operation.

The MAX96749AC/749AP/767/769/855/857/859/861 and specific deserializers support access of the PT1 (SDA1_RX1 and SCL1_TX1) pass-through channel to local and remote register read access in support of ASIL applications. The PT2 channel does not have read access to internal registers.

SPI

The MAX96749AC/749AP/767/769/855/857/859/861 devices additionally include an SPI master/slave interface, including two slave-select pins, for peripheral control. The SPI interface enables a host SPI master on one side of the GMSL link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL devices (a GMSL device can be configured as an SPI master or slave). Normal SPI operation is a single device-to-device (point-to-point) tunnel (i.e., serializer to one deserializer and vice versa). In point-to-point applications, the SPI control channel is connected to either Link-A or Link-B deserializers, selected by the SPI_LINK_SEL register.

Additionally, using SPI_CC_RD, SPI_CC_WR, and SPI_CC_EN, it is also possible to control an SPI peripheral on the remote side of the link using the I^{2}C bus on the local side.

In daisy-chained applications, it is also possible to use the SPI slave to select addressing features to access multiple SPI slaves attached to each deserializer on a single daisy chain. On-the-fly programming is possible to reconfigure the SPI master to switch between the two GMSL link outputs.

The SPI control channel may also be used in the non-ACK (unidirectional) broadcast mode to any number of SPI slave devices on both links. Contact the factory for more information.

The SPI clock range is 600kHz to 25MHz. Ensure to meet setup and hold time requirements, especially for speeds higher than 20MHz. See Table 10.

I^{2}S/TDM Audio

GMSL devices for display applications support I^{2}S stereo and up to 8 channels of audio in the Time-Division Multiplexing (TDM) mode. The MAX96749AC/749AP/767/769/855/857/859/861 devices can support 2 forward and 2 reverse audio channels. Sample rates of 8kHz to 192kHz and sample depths of 8 bits to 32 bits are supported. The maximum SCK frequency is 49.152MHz. For system flexibility, GMSL devices can act as either the slave or master at either end of the link.

Audio Channel Configurations

The MAX96749AC/749AP/767/769/855/857/859/861 include two forward and two reverse audio channels. Additionally, the devices can source (forward direction from serializer to deserializer) audio from either of the device I^{2}S pin groups: DisplayPort secondary data channels (SST mode only), or a combination of the two. Reverse channel audio, from deserializer to serializer, can be output from the I^{2}S pin groups of the device. DisplayPort audio channels cannot be output locally at the serializer's I^{2}S pins.

General capabilities of the audio channels:

Forward Audio:

- Two forward audio channels, which can be sourced from the DP interface (SST mode only) or device I^{2}S pins. See

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Table 15.

- Two Audio Transmit blocks, suffixed X and Y. Each can be connected to GMSL Link-A or Link-B.
- Replication is possible by configuring the same I^2S input to drive both Audio Tx blocks.
- Replication is also possible on a daisy chain. If an audio stream is sent to Link-A, it can be received by all deserializers in the chain connected to Link-A.

HDCP encryption of Audio:

- When HDCP encryption is enabled, it must be associated with a video stream and then optionally an audio stream. Then, both the video and audio streams encrypted by the same HDCP cipher can only be decrypted by the same deserializer(i.e., the encrypted audio cannot be decrypted and output by a deserializer that is not decrypting the associated video).

I^2S and DisplayPort 8-Channel TDM Audio:

- If the display modules have I^2S sinks (Audio DACs) capable of selecting a pair of channels out of an 8-channel TDM, a single 8-channel TDM can be sent to all four deserializers in a daisy chain.
- DisplayPort supports multichannel audio and MAX96749AC/749AP/767/769/855/857/859/861 devices can convert them to TDM format and transmit over GMSL.

Reverse Audio

- For reverse audio, there are two Audio Receive blocks, each of which can be received from Link-A or Link-B, and output on MFPs. See Table 15.

The MAX96749AC/749AP/767/769/855/857/859/861 devices have two audio pipes, allowing the following combinations when using both pipes:

- Two FWD from device I^2S pins.
- One FWD from DP source (SST Mode).
- One FWD DP + one FWD I^2S pin.
- One FWD DP + one REV I^2S pin.
- One FWD I^2S pins + one REV I^2S pin.
- Two REV audio two I^2S pins.
- Two FWD and two REV audio to I^2S pins.

Singular stream configurations and combinations with respect to where audio is going or coming from (Link-A or Link-B, which deserializer in the chain, etc.) are also possible.

Speed Programming for SPI and I^2S

The SPI and I^2S interfaces may be used over a wide range of frequencies. The MAX96749AC/749AP/767/769/855/857/859/861 provide flexible programming of MFP rise and fall times (transition time) to maintain timing margins while minimizing radiated EMI.

Table 9 and Table 10 provide guidance on recommended transition time settings for various I^2S and SPI operating frequencies and V_{DDIO} supply voltages. See Table 16 for GPIO pin speed programming information.

At lower frequencies, SPI data is typically latched on the opposite clock edge than the edge on which it is shifted. See Figure 7 and Figure 8. At higher frequencies, however, the data must be latched on the same edge as the shift to meet setup and hold-time requirements. Table 10 provides guidance on programming the latching clock edge.

Table 9. Recommended I^2S Pin Programming

FREQUENCY	V_{DDIO}	RECOMMENDED SPEED SETTING (IO_EDGE_RATE)
< 25MHz	1.7V to 2.24V	01
	2.25V to 3.6V	10

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Table 10. Recommended SPI Pin Programming

FREQUENCY	V_{DDIO}	LATCHING EDGE	RECOMMENDED SPEED SETTING (IO_EDGE_RATE)
< 12.5MHz	1.7V to 2.24V	Opposite from Shift	01
	2.25V to 3.6V		10
12.5MHz to 25MHz	1.7V to 2.24V	Opposite from Shift	00
	2.25V to 3.6V		01

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Ethernet

The MAX96767/MAX96769/MAX96859/MAX96861 support bidirectional 100Mbps SGMII (AC coupled) data transport simultaneously with video and side-channel communication. This feature can be used with any GMSL3/2 deserializers that support RGMII/RMII or SGMII. Ethernet data shares the total link available bandwidth in the forward and reverse channels. See the *GMSL Bandwidth Calculations* section for more information.

A single 100Mbps interface is supported, which allows ethernet tunneling to a single deserializer, which can be connected to either SIOA or SIOB, and can be in any place in a daisy chain; however, ethernet cannot be tunneled to more than a single deserializer. Only 100Mbps rate is supported, 1Gbps and 10Mbps rates are not supported. In dual-link mode, similar to video and other side-channel data, RGMII/RMII data is split over the two links and recombined by the deserializer.

The LVDS receiver and transmitter is 1.25Gbps and the clocks are 625MHz. SGMII can operate in two main pin modes, one with an independent clock interface OR where the clock is recovered from the data lines. MDIO transactions are supported to configure external devices, but the serializer cannot be programmed via the MDIO interface (only the main control channel I^2C/UART interface can be used to access serializer registers).

CRC Error Detection and Correction

All GMSL serializers and deserializers provide 16-bit CRC protection of control-channel data (I^2C, UART, SPI, GPIOs, Audio) to enable error detection and correction for all control channel packets on the forward and reverse channels.

Control-Channel CRC

Every control-channel packet (excluding Idle and Acknowledge packets) can be protected by a 16-bit packet Cyclic Redundancy Check (CRC). Each packet type can be individually configured to enable or disable packet CRC. By default, all low-bandwidth channels have packet CRC.

Automatic Repeat Request (ARQ) / Automatic Retransmission

An automatic packet retransmission method, ARQ, is employed in GMSL serializers and deserializers for audio, SPI, IIC, UART, and GPIO channels. ARQ works in conjunction with 16-bit packet CRC to detect if packets are received without error or not.

The ARQ mechanism allows the transmit side to automatically retransmit packets when it does not get notification from the receiver that it is received error-free. Therefore, all corrupted and dropped packets are corrected by retransmitting them. This allows very high robustness of mission-critical control functions in the system.

Each control packet is tagged by a 4-bit sequence number that continuously increments and rolls over. The transmitter saves the last 16 packets transmitted on a certain type of communication channel. When the receiver receives a control packet, it checks that its CRC and sequence number are correct. When the correctness of both is validated, it sends back an acknowledge packet, which notifies the transmitter that the packet with a certain sequence number is correctly received.

When the transmitter does not get an acknowledge packet for a data packet with a certain sequence number, it automatically retransmits the data packet reading it from the internal packet memory. A 4-bit sequence number allows the transmitter to transmit up to 15 packets without getting any acknowledgment. This allows pipelined operation, which minimizes the effect of round-trip latency to get acknowledge packets, and increases the continuous available bandwidth. This retransmission process repeats until the packet is either acknowledged or maximum number of retransmissions is reached. Upon reaching the maximum, the packet is assumed as acknowledged, it is dropped from the transmission queue, and the send window moves forward to transmit subsequent packets.

A 3-bit register is allocated to set the maximum number of retransmissions. A packet can be retransmitted up to seven times depending on the register value set in the MAX_RT register for each communication channel.

Control Channel Latencies

Table 11. Typical Control Channel Latencies

FUNCTION	FORWARD	REVERSE	NOTES
I^2C	< 10µs	< 10µs	

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Table 11. Typical Control Channel Latencies (continued)

FUNCTION	FORWARD	REVERSE	NOTES
UART	< 10µs	< 10µs	
Audio	< 100µs	< 100µs	For typical use cases
SPI	< 10µs	< 10µs	Round trip

Power-Up and Link Start-Up

MAX96749AC/749AP/767/769/855/857/859/861 are in power-down mode when the PWDNB pin is low or when any of the power supplies are down. Registers and configurations are set to their default reset conditions.

The serializer and deserializer may power-up in any order. After PWDNB is released and all power supplies are up, each device starts its power-up sequence and performs the following actions in sequence:

The control channel (I^2C or UART) is functional on the local side. The device registers are writable and readable.

The link is established based on the following settings:

- LINK_EN_A, LINK_EN_B: Try establishing GMSL link on enabled PHY. By default, both links are enabled. LINK_EN bit of the unused link can be set to 0 to reduce power consumption.
- TX_RATE_A, TX_RATE_B: Selects the forward channel bit rate of 12, 6 or 3Gbps.
- Each enabled PHY performs link calibration, equalizer adaptation, and data-channel locking. Both devices set their LOCK pins high. By default (LOCK_CFG = 0), so SER asserts its lock pin when either Link-A or Link-B locks.
- The control channel is available to and from remote side.

After the devices are linked, they can be configured. This can be done locally or over the control channel, by a µC on either the serializer or deserializer side.

CFG[2:0] Pins

The CFG[2:0] pins are used to set initial register values and functional modes of the device at power-up. At power-up, the voltage levels at the CFG[2:0] input pins are latched. The decoded levels set initial register values and functional modes that may not be easily programmed through I^2C or UART after the device powers up. The configuration tables provide the exact details to choose resistor values for the CFG[2:0] pins.

The CFG[2:0] pins are shared with MFP pins. Before the pin levels are latched, the chip does not drive the pins. A precision resistor network must be connected to each CFG pin to set the desired configurations. Use these MFP pins, which double function as CFG pins, only as outputs after power-up.

See Table 12.

Table 12. CFG[2:0] Pin Configuration Table

CFG[2:0] INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (NOTES a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (NOTE c)		CFG0 MAPPED CONFIGURATION (NOTE d)		CFG1 MAPPED CONFIGURATION (NOTE d)			CFG2 MAPPED CONFIGURATION (NOTE d)		
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	I^2CSEL	DEVICE ADDRESS	GMSL MODE (LINK-A)	CXTP (LINK-A)	TX_RATE (LINK-A)	GMSL MODE (LINK-B)	CXTP (LINK-B)	TX_RATE (LINK-B)
0.0%	0.0%	11.7%	OPEN	10000	I^2C	0x80	GMSL3 (PAM4)	Twisted Pair	12G	GMSL3 (PAM4)	Twisted Pair	12G
16.9%	20.2%	23.6%	80600	20500		0x84			Reserved			Reserved
28.8%	32.1%	35.5%	68100	32400		0xC0		Coax	12G		Coax	12G
40.7%	44.0%	47.4%	56200	44200		0xC4			Reserved			Reserved

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Table 12. CFG[2:0] Pin Configuration Table (continued)

52.6%	56.0%	59.3%	44200	56200	UART	0xC4	GMSL2 (NRZ)	Coax	3G	GMSL2 (NRZ)	Coax	3G
64.5%	67.9%	71.2%	32400	68100		0xC0			6G			6G
76.4%	79.8%	83.1%	20500	80600		0x84		Twisted Pair	3G		Twisted Pair	3G
88.3%	100%	100%	10000	OPEN		0x80			6G			6G

Notes:

a) Resistor-divider tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG[2:0] input voltages to exceed the maximum or minimum voltage limits for each setting.

b) Other than the CFG[2:0] input resistor-divider, any load on CFG[2:0] must be ≥ 25 x (R1 + R2).

c) Each resistor in the voltage-divider must be ≤100kΩ.

d) CXTP: Shielded-Twisted-Pair or Coax mode serial link

GMSL_MODE: GMSL2(NRZ) or GMSL3(PAM4)

TX_RATE: Forward channel serial rate in bits-per-second

I2CSEL: I^2C or UART interface for SDA_RX and SCL_TX

DEVICE ADDRESS: Device address

Table 13. CFG[2:0] Pin Configuration Table

CFG[2:0] INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (NOTES a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (NOTE c)		CFG0 MAPPED CONFIGURATION (NOTE d)		CFG1 MAPPED CONFIGURATION (NOTE d)			CFG2 MAPPED CONFIGURATION (NOTE d)		
MIN	**TYP**	**MAX**	**R1 (Ω)**	**R2 (Ω)**	**I^2CSEL**	**DEVICE ADDRESS**	**GMSL MODE (LINK-A)**	**CXTP (LINK-A)**	**TX_RATE (LINK-A)**	**GMSL MODE (LINK-B)**	**CXTP (LINK-B)**	**TX_RATE (LINK-B)**
0.0%	0.0%	11.7%	OPEN	10000	I^2C	0x80	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
16.9%	20.2%	23.6%	80600	20500		0x84			Reserved			Reserved
28.8%	32.1%	35.5%	68100	32400		0xC0		Reserved	Reserved		Reserved	Reserved
40.7%	44.0%	47.4%	56200	44200		0xC4			Reserved			Reserved
52.6%	56.0%	59.3%	44200	56200	UART	0xC4	GMSL2	Coax	3G	GMSL2	Coax	3G
64.5%	67.9%	71.2%	32400	68100		0xC0			6G			6G
76.4%	79.8%	83.1%	20500	80600		0x84		Twisted Pair	3G		Twisted Pair	3G
88.3%	100%	100%	10000	OPEN		0x80			6G			6G

Notes:

a) Resistor divider tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG[2:0] input voltages to exceed the maximum or minimum voltage limits for each setting.

b) Other than the CFG[2:0] input resistor divider, any load on CFG[2:0] must be ≥ 25 x (R1 + R2).

c) Each resistor in the voltage divider must be ≤ 100kΩ.

d) CXTP: Shielded-Twisted-Pair or Coax mode serial link

GMSL_MODE: GMSL2 (NRZ)

TX_RATE: Forward channel serial rate in bits-per-second

I2CSEL: I^2C or UART interface for SDA_RX and SCL_TX

DEVICE ADDRESS: Device address

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GMSL2 Link Lock

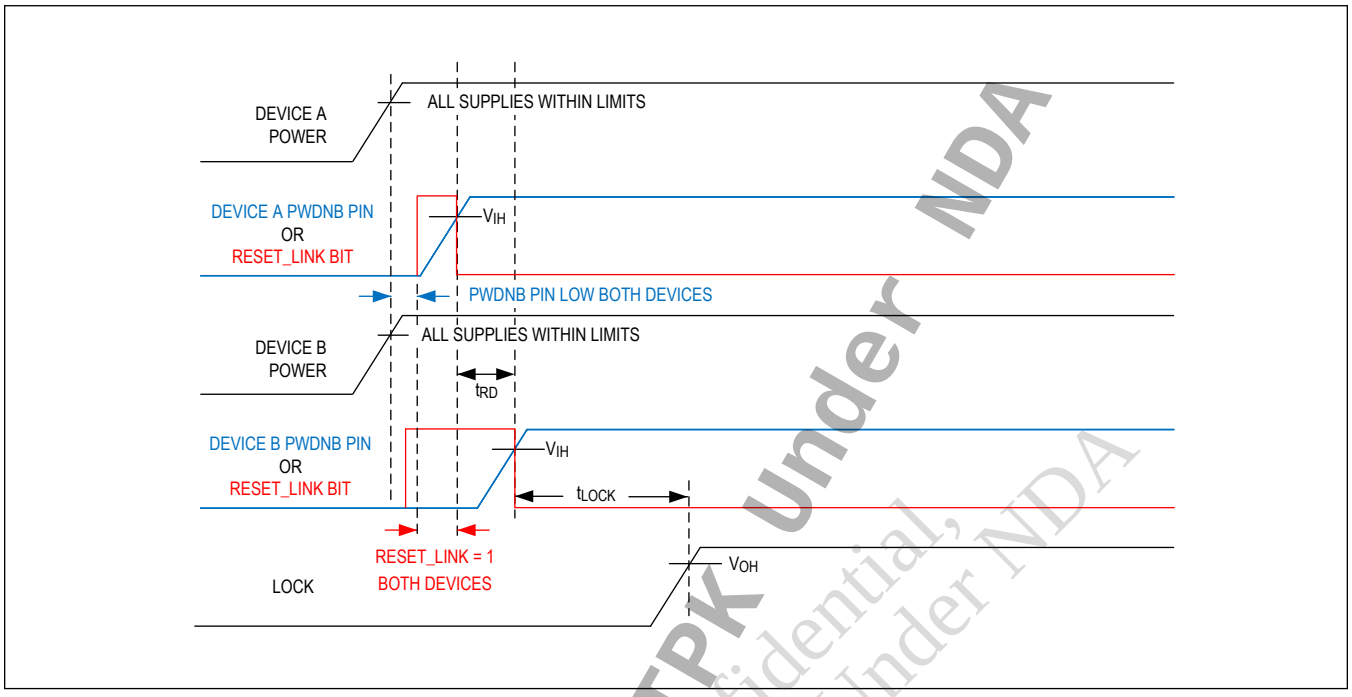

Figure 18. GMSL2 Lock Time

Figure 18 illustrates the sequence that is used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power-up or resume operation from a RESET_LINK state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I^2C/UART, SPI, GPIO, audio) can be used immediately after link lock is asserted.

The device will establish single link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in and the system is up and running. Lock is obtained with no interaction between the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

Dual-link and splitter configurations require additional user programming. For guidance on enabling these configurations and optimizing the lock time, contact the factory.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links, so a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. Lock time is measured from the later of PWDNB or RESET_LINK release in either the serializer or deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate lock, PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, RESET_LINK is assumed to be low after power-up (normal operation).
6. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices) must be less than the threshold specified in Note 6. Contact the factory for guidance if this timing cannot be

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guaranteed.

7. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and the deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permissible t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.
8. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This will minimize any disruptions caused by a transient loss in connectivity.

LOCK Reporting

MAX96749AC/749AP/767/769/855/857/859/861 devices can report the lock status of Link-A and/or Link-B at the LOCK pin, along with daisy-chain lock status. Lock pin behavior is configured by LOCK_CFG in REG5. Table 14 lists the available lock status reporting options. By default, the serializer asserts its lock pin when one or more deserializers have locked on Link-A or Link-B (value 0x0).

If daisy chaining is used on one or both links, DES_CNT (in LCTRL0, 0x28 for Link-A and 0x32 for Link-B) informs the serializer on the number of deserializer repeaters on each link.

Table 14. LOCK_CFG Register Decode Table

VALUE	DECODE
0x0	Link-A OR Link-B is locked.
0x1	Link-A AND Link-B are locked.
0x2	All deserializers on Chain-A OR Chain-B are locked.
0x3	All deserializers on Chain-A AND Chain-B are locked.

The number of deserializers locked on each daisy chain can be read from the DAISY_CHAIN_STATUS (in LCTRL2, 0x2A for Link-A and 0x34 for Link-B).

Device Reset

There are three general-reset options available through register writes:

- RESET_ALL (in CTRL0) resets all blocks, including all registers, digital blocks, and analog blocks. Register status is not saved or restored. This process is similar to driving the PWDNB pin low and then high.
- RESET_LINK(A/B) (in LCTRL1, 0x29 for Link-A and 0x33 for Link-B) resets all GMSL PHY-related digital logic of the respective link. After this bit is set, all control registers are still accessible through the local control channel. The settings of other registers are not affected. The link remains in RESET until RESET_LINK is cleared.
- RESET_ONESHOT(A/B) (in LCTRL1, 0x29 and 0x33) resets all GMSL PHY-related digital logic of the respective link, and then automatically clears itself. The settings of other registers are not affected. This is similar to setting and clearing RESET_LINK.

First set RESET_LINK(A/B) = 1 and then program registers that affect GMSL link operation (e.g., TX_RATE_A/B, CXTP_A/B), followed by RESET_LINK(A/B) = 0.

Multifunction Pin (MFP) Assignments

Side-channel functions, such as pass-through I^{2}C/UART, SPI, and audio, are enabled by programming multifunction pins (MFP). Each pin has several possible functions, but only one can be used at a time. Some functions require only a single pin, but most are implemented across a group of pins. For example, MS is a single pin, but SPI requires several pins. Users select pin functions to suit their use case by programming the appropriate registers. The *Pin Descriptions* table shows default and alternate functions for each MFP pin.

The transition time of each MFP can be changed from the default value by register programming. However, if the pass-through I^{2}C/UART function is selected, the transition time of these specific pins is fixed independent of the setting. The main channel I^{2}C/UART has a fixed speed.

Table 15 indicates how latch-on-power-up, I^{2}C/UART, audio, SPI, and other functions are mapped to the MFP pins.

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Transition times depend on the transition time setting and V_{DDIO} supply voltage. See Table 16 for typical transition times.

Table 15. GMSL MFP Pin Function Map

PIN	LATCH-ON POWER-UP	I²C/UART	AUDIO	SPI	OTHER FUNCTIONS	GPIO	BASELINE (DEFAULT FUNCTION, I/O TYPE AND STATUS)	TRANSITION TIME SETTING (TTS) DEFAULT
MFP0			SCK2	SCLK	VA_X_DONE	GPIO0 (dc)	GPI CMOS in, 1MΩ pulldown	10
MFP1			SD2	MOSI	VA_Y_DONE	GPIO1 (dc)	GPI CMOS in, 1MΩ pulldown	10
MFP2			WS2	MISO		GPIO2	GPI CMOS in, 1MΩ pulldown	10
MFP3/ SDA_RX		SDA, RX				GPIO3 (odo, slow)	SDA, RX ODO, 40kΩ pullup CMOS in	I²C
MFP4					LMN0	GPIO4 (slow)	GPI CMOS in, 1MΩ pulldown	11
MFP5					LMN1	GPIO5 (slow)	GPI CMOS in, 1MΩ pulldown	11
MFP6/ CFG0	CFG0					GPO6 (out, slow)	Disabled Hi-Z	11
MFP7/ SCL_TX		SCL, TX				GPIO7 (odo, slow)	SCL, TX ODO, 40kΩ pullup CMOS in	I²C
MFP8					LOCK	GPIO8 (slow)	LOCK ODO, 40kΩ pullup	11
MFP9					ERRB	GPIO9 (slow)	ERRB ODO, 40kΩ pullup	11
MFP10/ CFG1	CFG1					GPIO10 (out, slow)	Disabled Hi-Z	11
MFP11			WS1			GPIO11	GPI CMOS in, 1MΩ pulldown	10
MFP12			SD1			GPIO12	GPI CMOS in, 1MΩ pulldown	10
MFP13			SCK1			GPIO13	GPI CMOS in, 1MΩ pulldown	10
MFP14			SCKOR1			GPIO14	GPI CMOS in, 1MΩ pulldown	10
MFP15			SDOR1			GPO15	Disabled 1MΩ pulldown	10
MFP16	CFG2		WSOR1			GPO16 (out)	Disabled Hi-Z	10

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Table 15. GMSL MFP Pin Function Map (continued)

PIN	LATCH-ON POWER-UP	I²C/UART	AUDIO	SPI	OTHER FUNCTIONS	GPIO	BASELINE (DEFAULT FUNCTION, I/O TYPE AND STATUS)	TRANSITION TIME SETTING (TTS) DEFAULT
MFP17		Pass-Through SDA1, RX1				GPIO17	SDA1 ODO, 40kΩ pullup CMOS in	10
MFP18		Pass-Through SCL1, TX1				GPIO18	SCL1 ODO, 40kΩ pullup CMOS in	10
MFP19					LMN2	GPIO19 (slow)	GPI CMOS in, 1MΩ pulldown	11
MFP20					LMN3	GPIO20 (slow)	GPI CMOS in, 1MΩ pulldown	11
MFP21				BNE, SS1	VA_Z_DONE	GPIO21 (dc)	GPI CMOS in, 1MΩ pulldown	10
MFP22				RO, SS2	VA_U_DONE, PCLK_OUT	GPIO22 (dc)	GPI CMOS in, 1MΩ pulldown	10
MFP23		Pass-Through SDA2, RX2	WSOR2		DE_OUT	GPIO23 (dc)	GPI CMOS in, 1MΩ pulldown	10
MFP24			SDOR2	MS	RCLKOUT, HS_OUT	GPIO24 (dc)	GPI CMOS in, 1MΩ pulldown	10
MFP25		Pass-Through SCL2, TX2	SCKOR2		VS_OUT	GPIO25 (dc)	GPI CMOS in, 1MΩ pulldown	10

Notes:

- All MFP pins are Hi-Z in power-down state.
- All MFP IOs are latched in the sleep mode.
- Hi-Z: 1MΩ pullup/pulldown are disabled and input/output are disabled.
- Latched: Value of input before the sleep mode entered remains latched in the sleep mode and after return to the power-up mode.

Table 16. Control-Channel and Side-Channel Typical Rise and Fall Times

PIN OR GPIO TRANSITION TIME SETTING (TTS) (IO_EDGE_RATE)	RISE TIME*		FALL TIME**	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
HPD	2.1ns	1.1ns	2.0ns	1.1ns
00(HS)	1.0ns	0.6ns	0.8ns	0.5ns
01(MS)	2.1ns	1.1ns	2.0ns	1.1ns
10(LS)	4.0ns	2.3ns	4.3ns	2.3ns
11	9ns	5ns	10ns	5ns
I²C	***	***	40ns	30ns

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*20% to 80%, 10pF load.

**80% to 20%, 10pF load.

***Rise time for open-drain outputs depends on external pullup resistor value.

Table 17. GPIO Types

(TYPE)	DESCRIPTION
(slow)	Can only be used with slow transition time setting (IO_EDGE_RATE = 3).
(dc)	Can be used to combine multiple GPIOs received from separate deserializer in daisy chain.
(odo)	Open-drain output only
(out)	Output only

Notes:

- All GPIOs can combine reverse-path GPIOs received from Links A and B. See *Reverse GPIO Tunnels*.
- Up to four GPIOs can be used for delay-compensated reverse-path GPIO reception. (GPIO IDs = 8, 9, 10, 11)

General-Purpose Inputs and Outputs (GPIO)

GPIOs are typically used to pass low-speed (< 100kbps) signals over the GMSL link. A GPIO tunnel can be set up in the forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based: a GPIO packet is created and transmitted on the GMSL link when a rising- or falling-edge transition is detected at a GPI pin. The transition is regenerated at a GPO on the other end of the link.

The multifunction pins can be programmed as GPI (input), GPO (push-pull output or open-drain output), or GPIO (bidirectional input/output). Each GPIO can also be programmed for 1MΩ or 40kΩ pullup or pulldown (or none). Although an internal pullup is provided, high-speed, open-drain outputs require an appropriate-value external pullup resistor to V_{DDIO}. Inputs cannot be left unconnected. Always ensure that every pin configured as an input has a pullup or pulldown programmed, or is driven by another IC.

A GPI on one side of the serial link can be mapped to a single GPO or multiple GPOs on the other side of the link. Each GPI is assigned a pin ID with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0–GPIO0, GPIO1–GPIO1, GPIO2–GPIO2, etc. However, GPIO mapping can be arbitrarily changed through register settings.

GPIO Delay Compensation

GPI transitions can be transmitted in two modes: delay- and non-delay-compensated. When delay compensation is enabled (TX_COMP_EN for each GPIO), the GPI-to-GPO delay across the link is a precise, fixed value set by GPIO_FWD_CDLY (in 0x58 for Link-A and 0x68 for Link-B) and GPIO_REV_CDLY (in 0x59 for Link-A and 0x69 for Link-B). Latency increases, but jitter and skew decrease. It is critical that GPIO_FWD_CDLY and GPIO_REV_CDLY are set identically in both the serializer and deserializer.

Delay-compensated mode is not available beyond the first deserializer in daisy-chain configurations.

The state of each GPIO can be read or written by the register either locally or remotely over the GMSL link by a µC using the control channel I^2C/UART interface.

In the non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible based on priority and available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Non-delay-compensated mode should be used with signals tolerant to delay variation (e.g., µC interrupts).

Delay-compensated GPIO tunnels in reverse direction are limited to tunnels 8, 9, 10, and 11 in the MAX96749AC/749AP/767/769/855/857/859/861. All other reverse GPIO tunnels do not support delay compensation. There is no restriction in delay-compensated GPIOs in the forward direction (all tunnels support it). However, delay compensation is possible only between the serializer and first deserializer in the chain (both forward and reverse).

Typical GMSL device delays forward and reverse-link rates are shown in Table 18.

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Table 18. Typical GPIO Delays for Forward-Link and Reverse-Link Transmissions

DIRECTION SER --> DES0 >> DES1 >> DES2 >> DES3	DELAY COMPENSATION (TX_COM_EN)	DELAY DES0	DELAY DES1	DELAY DES2	DELAY DES3
GPIO forwarding from serializer to deserializer (12Gbps forward channel)	0	1.0µs	1.5µs	2.0µs	2.5µs
	1	3.5µs	Delay Compensation Not Supported in Daisy-Chain Configurations		
GPIO forwarding from serializer to deserializer (6Gbps forward channel)	0	710ns	860ns	1.0µs	1.2µs
	1	3.6µs	Delay Compensation Not Supported in Daisy-Chain Configurations		
GPIO forwarding from deserializer to serializer (187Mbps reverse channel)	0	5.8µs	8.3µs	10.8µs	13.3µs
	1	42µs	Delay Compensation Not Supported in Daisy-Chain Configurations		

Note: GPIO_FWD_CDLY and GPIO_REV_CDLY are set to default values.

Reserved GPIO Tunnel IDs

GPIO tunnel ID 29 (on forward and reverse) is used by the UART MS signal when the remote UART mode select function is enabled in that direction.

GPIO tunnel IDs 25, 26, 27, and 28 (on reverse) are used by HDCP 2.2/2.3 when enabled.

Do not use these reserved IDs for other purposes unless their reserved function is disabled (i.e., when UART is not used or when remote MS is disabled, use ID 29).

GPIO tunnel ID 31 is reserved for remote error.

GPIO tunnels can be mapped to any available GPO.

GPIO Tunnels in Daisy-Chain Applications

The MAX96749AC/749AP/767/769/855/857/859/861 support up to 25 GPIOs, dependent on device feature utilization. A GPIO tunnel can be set up in the forward or reverse direction. In daisy-chained applications, all GPIO packets on the forward channel are broadcast to all deserializers and each deserializer can choose if or not to receive them. On the reverse channel, each GPIO is sent directly to the serializer. Sending GPIO packets from deserializer to deserializer is not possible.

Forward GPIO Tunnels

When driving GPIO tunnels in the forward direction (from serializer MFPs to deserializer MFPs), each enabled MFP can be connected to a selected GPIO tunnel (with a specified ID) on each link. The forward GPIO tunnel ID must be programmed using GPIO_TX_ID for each MFP. The default GPIO tunnel IDs are the MFP index values, i.e., GPIO0 maps to tunnel 0, GPIO5 to tunnel 5, etc. A forward GPIO tunnel can be enabled independently for Link-A and Link-B by setting GPIO_TX_EN_A and GPIO_TX_EN_B for each MFP. All four combinations of these two bitfields are valid; enabling or disabling transmission is independent for the two links.

Reverse GPIO Tunnels

All deserializer MFP pins (except the ones shared with the CFG pins) can be connected to the serializer through reverse GPIO tunnels.

Most MAX96749AC/749AP/767/769/855/857/859/861 MFPs can connect to a single reverse GPIO tunnel on each link (single-tunnel GPIO). The tunnel ID they connect to must be programmed using GPIO_RX_ID for each MFP. The default GPIO tunnel IDs are the MFP index values. A reverse tunnel can be enabled independently for Link-A and Link-B by setting GPIO_RX_EN_A and GPIO_RX_EN_B for each MFP. All four combinations of these two bitfields are valid, i.e., enabling or disabling transmission is independent for the two links. When the serializer is connected to two links and a GPIO is connected to a reverse GPIO tunnel on both links (GPIO_RX_EN_A = 1 and GPIO_RX_EN_B = 1), the received GPIO values are combined by AND-ing or OR-ing them (selected by GPIO_OUT_LGC for the specific GPIO) and the combined signal is output to the serializer pin.

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When the serializer is driving several deserializers, there are too many MFPs on the deserializer side and all of them cannot be output separately at the serializer MFP outputs. The MAX96859/861 include an enhanced multitunnel GPIO connection feature. Certain serializer MFPs (multitunnel GPIO, indicated with 'dc' in Table 15) can connect to multiple reverse GPIO tunnels (up to four) on each link and output the combined GPIO value received from each tunnel. For these MFPs, the four GPIO tunnels the pin connects to are programmed using GPIO_RX_ID, GPIO_RX_ID2, GPIO_RX_ID3, and GPIO_RX_ID4.

The connection to each tunnel is enabled by setting GPIO_RX_EN_A, GPIO_RX_EN_B, GPIO_RX_EN2_A, GPIO_RX_EN2_B, GPIO_RX_EN3_A, GPIO_RX_EN3_B, GPIO_RX_EN4_A, and GPIO_RX_EN4_B. Each possible combination of these eight GPIO_RX_EN* is valid. The signals received through the connected tunnels are combined by AND-ing or OR-ing them (selected by GPIO_OUT_LGC) and the combined signal is output to the serializer pin. The same GPIO tunnel can be connected to multiple pins. Although this functionality is designed to support daisy-chain GPIOs, there is no restriction in which deserializer drives which GPIO tunnel. For example, two GPIO tunnels can be driven by two MFPs of the first deserializer in the chain and a third GPIO tunnel can be driven by the second deserializer in the chain. GPIO signals received from these three tunnels can then be combined and output to a single MFP pin of the serializer.

When the SOC detects an edge at a multitunnel GPIO of an MAX96749AC/749AP/767/769/855/857/859/861, it can read GPIO_RECVED_* to know the latest status of each received reverse GPIO signal. This allows the SOC to know which deserializer sent the GPIO transmission by reading a single register.

MFP Pin Equivalent Circuits

In general, MFP pins can all be classified as either programmable high-speed GPIO or programmable I²C/ODO (Open-Drain Output) GPIOs. Equivalent circuit representations are illustrated in Figure 19 and Figure 20.

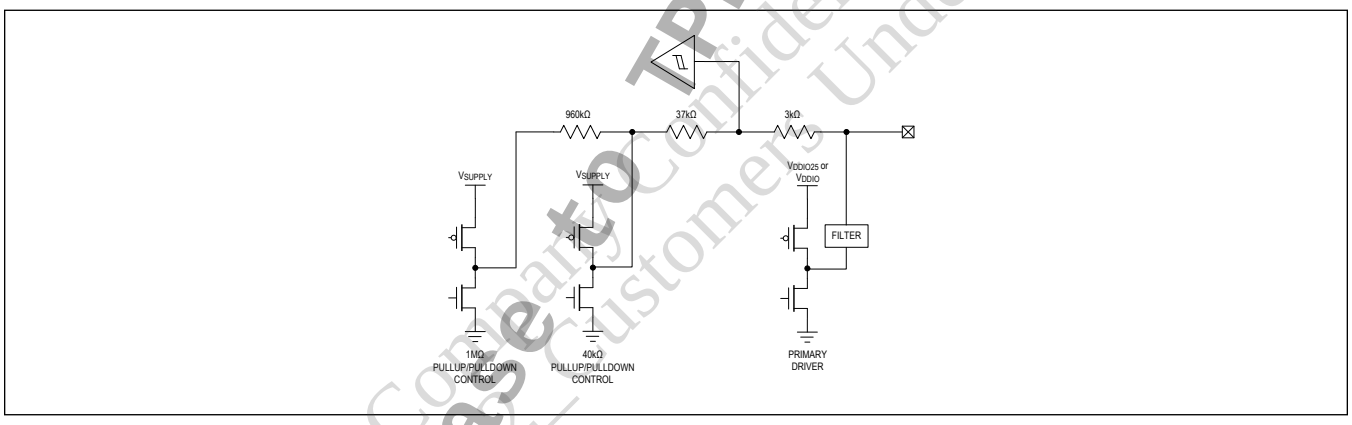

Figure 19. Standard High Speed GPIO

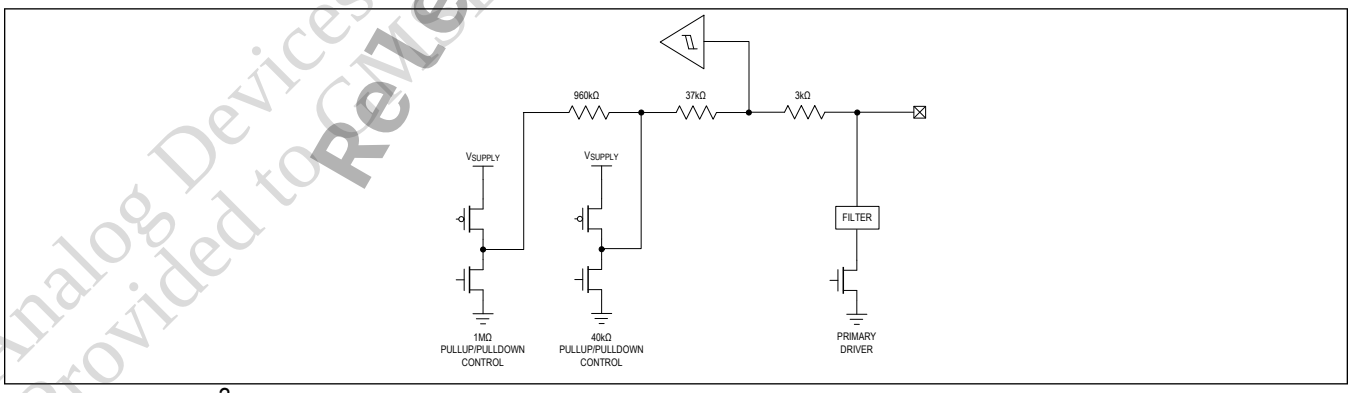

Figure 20. Standard I²C GPIO

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Clocking

GMSL Reference Clock

GMSL devices require a reference clock source to generate the link-rate clock and associated internal clocks. The serializer can be clocked using an external 25MHz crystal or an external low-jitter clock source. See the AC specifications in the Electrical Characteristics table.

Reference-Clock Generation

RCLKOUT can be used as a reference clock by a GMSL2 or GMSL1 serializer in close proximity. This arrangement eliminates the need for an additional external crystal or oscillator for the second serializer.

System Diagnostics

Error and Fault Condition Monitoring

All GMSL devices have an open-drain multipurpose error reporting and interrupt status output that can output detected error status and/or some events internal to the device (interrupts), which may be of interest to a host processor. The MAX96749AC/749AP/767/769/855/857/859/861 ERRB function is assigned to MFP9. The ERRB functionality of the MFP is enabled by default and it works in the open-drain output mode with 40K internal pullup. ERRB is an active-low signal, which indicates that an error or interrupt event occurred.

A variety of error and event sources can be programmed to drive the ERRB pin. Enabled sources assert ERRB immediately, with only a few gate delays. Each error and event that can drive ERRB pin also has a status flag in the registers. So, the reason for assertion of ERRB pin can be read from registers when several different events can drive the ERRB pin. Each ERRB source can be individually enabled and disabled.

The main functions/typical uses of this feature are the following:

- Routing of on-chip diagnostics to interrupt the controller.
- Routing of ASIL-related interrupts to interrupt the controller.
- Forwarding of single or daisy-chained deserializer diagnostic faults to the serializer ERRB signal.

ERRB Operation

There are many individual errors that can be output to the ERRB pin. Each error has a status register and an output enable (OEN) bit, which enables that error to be ORed into the ERRB output at the ERRB pin. The ERRB ORing concept is the same in every GMSL device. However, the possible errors that are available may differ.

During normal operation, monitor the ERRB pin of the GMSL devices to look for when an error occurs. When an error occurs, it is reported in the local register of that specific feature. If there is a counter for that type of error, it tracks the number of errors that occurred. Almost all errors/statuses can be routed to the ERRB pin. To find out if a specific error/status can be routed to the ERRB pin, consult the safety-related documents for the MAX96749AC/749AP/767/769/855/857/859/861.

For more information on error reporting, contact the factory.

Remote Error Reporting

GMSL devices can report the ERRB status of the remote device (the serializer or deserializer on the other end of the link) when the link is locked. Remote error status is transmitted over the internal GPIO tunnel using a programmable ID. The remote device transmits its ERRB status when ERR_TX_EN = 1, using the GPIO ID programmed in its ERR_TX_ID. Although the default value is acceptable in most cases, it may be necessary to change ERR_TX_ID to avoid sharing with other GPIO tunnels.

The local device receives the transmitted error status over the GPIO tunnel. Any MFP can be connected to the GPIO tunnel and output the received remote error status. To do this, for the MFP that outputs the remote error status, program GPIO_RX_EN = 1, GPIO_TX_EN = 0, GPIO_OUT_DIS = 0, GPIO_TX_ID = the programmed remote ERR_TX_ID value.

Remote error status can also be combined with local error status, and output at the ERRB pin similar to other local error and interrupt events.

To do this, set ERR_TX_EN and ERR_TX_ID as described above. Then, in the local device, set ERR_RX_ID = ”Remote

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ERR_TX_ID value", ERR_RX_EN = 1 and REM_ERR_OEN = 1. Whenever the remote ERRB status changes, it is transmitted to the local device and ORed with other errors to drive the ERRB pin of the local device. The host controller can read REM_ERR_FLAG to determine if the error is due to a remote or a local error/interrupt, and then act accordingly.

In devices where multiple remote devices can be connected (e.g., devices with two links and serializers that support daisy chaining), multiple remote ERRB status signals can be combined to the local ERRB pin. In daisy-chain capable serializers, multiple remote ERRB signals can be combined and output from a separate MFP, similar to combining multiple GPIO tunnel outputs.

Link Integrity Features

The GMSL Physical Layer (PHY) provides diagnostic tools to aid system bring-up and debug. These tools leverage parts of the adaptive equalizer implementation. These diagnostic tools are not laboratory instrumentation nor are they designed to demonstrate channel compliance.

These tools provide a high degree of visibility of the link and system performance. The GMSL diagnostic tool set provides a market leading level of visibility. These diagnostic tools include:

1. Eye mapping
2. Eye-opening monitor
3. Link (voltage) margining
4. FEC input and output BER rate (select devices)

These tools are a mixture of hardware and supporting software for data collection and processing. Remote (deserializer) control channel access must be enabled to use these functions. The Graphic User Interface (GUI) provides the required software and processing. Contact the factory for more information.

FEC Statistics Monitoring

Select deserializers include tools to monitor and log FEC statistics including the number of uncorrected errors, number of corrected errors, and total number of codeword blocks processed. The deserializer registers can be read and reset using the control channel.

Power Supplies and Thermal Management

Power Supplies

The MAX96749AC/749AP/767/769/855/857/859/861 provide flexible power supply configurations.

The 1.0V V_{DD} supply provides power to the digital core. Connect 1.0V ±5%.

The V_{DDIO} supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the part. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

V_{DD18} is the primary analog supply and is fixed at 1.8V. Connect 1.8V ±5%.

V_{DD18_eDP} is the supply for the DisplayPort interface and is fixed at 1.8V. Connect 1.8V ±5%.

Proper power-supply bypassing of all supplies is essential for high-frequency circuit stability. See Table 2. See Table 19 for power-supply tolerances and noise requirements. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

No specific power-supply ramp sequence is required.

Recommended Operating Conditions

Table 19. Recommended Operating Conditions

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V_{DD18}		1.7	1.8	1.9	V
	V_{DD18_eDP}		1.7	1.8	1.9	
	V_{DD}	1.0	0.95	1.0	1.05	
	V_{DDIO}	1.8	1.7	1.8	1.9	

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Table 19. Recommended Operating Conditions (continued)

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
		3.3	3.0	3.3	3.6	
Supply Noise	V_{DD18}			25		mV_{P-P}
	V_{DD18_eDP}			25		
	V_{DD}	1.0V		25		
	V_{DDIO}	1.8V		50		
		3.3V		100		
Operating Junction Temperature, T_J			-40		+125	ºC

Note: *Supply noise < 1MHz.*

Power Manager

The primary function of the power manager is to control the internal switched supply domains during the full sequence of power states, so the chip powers up smoothly. It serves as a guard before the chip powers up. Once the internal supplies meet their valid levels, the power manager relinquishes control to the digital core for normal operations. Another function of the power manager is to ensure the chip consumes minimum standby current during sleep mode and can quickly restore configurations to full operation after waking up. Finally, the power manager monitors the power supplies for Undervoltage (UV) and Overvoltage (OV) conditions.

UV/OV Detection

The MAX96749AC/749AP/767/769/855/857/859/861 devices include OV and UV detection logic. Register programming is required to enable these features.

In the event of an OV condition on V_{DD18}, V_{DDIO}, or V_{DD}, the ERRB pin is asserted, but no further action is taken. The device continues to remain powered with an OV condition and may suffer damage. V_{DD18_eDP} is not protected, but if connected to the same supply as V_{DD18}, it is by extension.

In a UV condition on V_{DD18}, the ERRB pin is asserted when V_{DD18} drops below an internal threshold level. The device continues to function unless V_{DD18} drops further to an internal reset level, in which case the device is reset. V_{DD18_eDP} is not protected, but if connected to the same supply as V_{DD18}, it is by extension.

In a UV condition on V_{DDIO}, the ERRB pin is asserted when V_{DDIO} drops below an internal threshold level. The device continues to function unless V_{DDIO} drops further to an internal reset level, in which case the device is reset.

In a UV condition on V_{DD}, the ERRB pin is asserted when V_{DD} drops below an internal threshold level and the device is reset.

Once the device is reset and the power supply voltage recovers, the device returns to its default power-up state with default register settings. The controller must then reinitiate device startup and reprogram all registers.

Power Modes

The MAX96749AC/749AP/767/769/855/857/859/861 devices support the following power modes:

- ACTIVE = All required circuits are powered up.
- SLEEP = All blocks, including the control channel, except local and remote wake-up circuitry, are disabled. Select register states are preserved.
- PWDNB = All blocks, including control channel, are inactive. Register states are set to power-up default.

There are two ways to go into low-power mode while all power supplies are active: assertion of the PWDNB pin (Power-Down mode) or invocation of the sleep state (Sleep mode). Both states provide very-low-power supply currents.

Power-Down (Standby) Mode

Asserting the PWDNB pin (active-low) places the device in standby power mode, and resets the digital registers and configurations to their default power-up condition. Any supply dropping below its internal threshold settings also places the device in power-down mode. If the power supply recovers, the device returns to the default power-up state with default register settings. Then, reinitiate device start-up and reprogram all the registers.

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Sleep Mode

The sleep state preserves a subset of register settings and configurations. The device can be put into the sleep state through an I^{2}C/UART command. Resuming to active state restores the device to its presleep condition without the need for additional register writes for retained registers. The register table includes an asterisk (*) for retained registers. Note that the state of registers 0x6424 (EDP_VID_CLK_CTRL0) and 0x6425 (EDP_VID_CLK_CTRL1) are not retained.

Resume is invoked by an I^{2}C command on the main I^{2}C inputs (SDA_RX/SCL_TX) or a low-frequency clock beacon transmitted from the master device over the GMSL link. If the main I^{2}C inputs is assigned to one of the pass-through I^{2}C input pins (SDA1/SCL1, SDA2/SCL2), the wake from sleep function can only be done through the main SDA_RX/SCL_TX pins, not the reassigned pass-through main I^{2}C pins.

Thermal Management

Power consumption of GMSL3/2 devices varies based on use case. Ensure to provide sufficient heat dissipation with proper board and cooling design techniques. The package exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below 125°C to avoid impacting device reliability.

Refer to Tutorial 4083 (*www.maximintegrated.com/thermal-tutorial*) for further guidance.

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Applications Information

Software Programming Model

Maxim automotive serializers and deserializers are designed to follow a general software programming model. Except for features that require in-operation control channel accesses such as the ASIL safety measures and interrupt handling, the following programming model should be followed:

1. Set the impacted functional blocks to disabled or reset mode. A general method to place the part in IDLE state is to stop all side channel and video traffic followed by a register write (RESET_LINK=1) to stop the GMSL link.
2. It is required that the settings for each feature are fully configured before it is enabled.
3. Establish the link by setting RESET_LINK=0 and wait for link to lock.
4. Start video and side channel traffic.

If changing the configuration of a feature is required during operation of other features, disable the feature that will be reconfigured, change its settings, and reenable it.

Conventional I²C/UART Control-Channel Programming

GMSL device registers can only be accessed and configured through the I²C/UART interface, in either I²C or UART modes, and via I²C-over-AUX on DisplayPort serializers. By default, the main I²C/UART control channel is also sent to the remote side device and any peripheral connections. This allows control of the GMSL devices from either end of the link. For multi-master configurations, with microcontrollers connected to both the serializer and deserializer, disabling the remote control channel by the DIS_REM_CC pin or through register settings is recommended to prevent bus contention.

SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, register address bytes, 1 or more data bytes, and finally a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address auto increments).

Device Address

Each device on the I²C/UART control channel must have a unique address. The GMSL device address is set to one of several 7-bit addresses according to the voltage level of the CFG0 pin at power-up. See Table 12. Note that the device address can be changed after power-up by writing to the DEV_ADDR and TX_SRC_ID registers.

I²C

Each device has an internal I²C slave for register access. The internal registers can be written and read according to the I²C protocol using the packet formats below.

Main I²C Host-to-GMSL Device Communication

The host I²C master has access to GMSL3/2 serializer and deserializer registers. The host can program GMSL3/2 device registers to configure the pass-through I²C/UART interfaces as either I²C or UART.

I²C Write-Packet Format

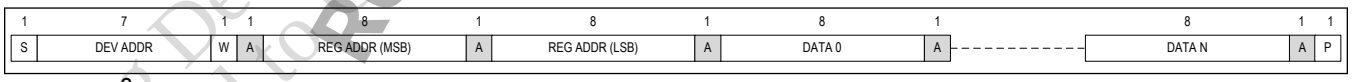

Figure 21. I²C Write-Packet Format

I²C Read-Packet Format

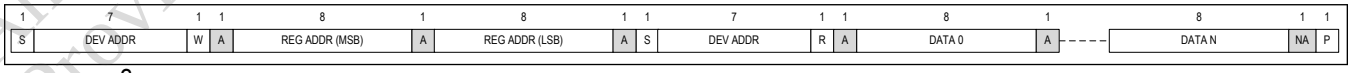

Figure 22. I²C Read-Packet Format

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Host-to-Peripheral Main I²C and Pass-Through I²C Communication

When communicating between a host and peripheral, main and pass-through I²C operation is the same. An I²C tunnel across the GMSL link connects the host's I²C master to the remote I²C slave. This logically connects separated I²C buses, enabling I²C transactions across the serial link to occur (with some delay) as if performed on the same physical I²C bus. The GMSL serializer and deserializer are intermediary devices: the host I²C master connects to a GMSL device I²C slave, and the peripheral I²C slave connects to a GMSL device I²C master.

For example, when the host I²C master transacts on one side of the link (local-side), data is forwarded to the other side (remote-side) by the I²C slave of the local-side GMSL device. Data is then received by the I²C master of the remote-side GMSL device, which in turn generates the same I²C transaction with the peripheral slave I²C. The remote-side GMSL device sends back any I²C data expected by the local-side.

The I²C interface uses clock stretching (holding SCL low) to account for timing differences between master and slave and to allow time for data to be forwarded and received across the serial link. All local-side I²C devices must support clock stretching by the GMSL device; remote-side I²C devices are not required to support clock stretching.

The host can program GMSL device registers to configure the pass-through I²C/UART interfaces as either I²C or UART.

UART

When the main I²C/UART interface is configured as UART, there are two operating modes: base and bypass.

UART Base Mode

Base mode is the means of ECU communication with the serializer and deserializer in which registers in these devices, as well as registers in peripheral devices, can be accessed. Base mode is enabled by default at power-up. In base mode, the ECU is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART packet protocol. The ECU can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer. In base mode, the ECU communicates with a UART peripheral in a way which is compatible with GMSL UART protocol. The device addresses of the serializer and deserializer in this mode are programmable.

In base mode, serializer, deserializer and peripheral registers can be written and read using the half-duplex GMSL UART protocol.

Figure 23 shows the UART protocol for writing and reading in base mode.

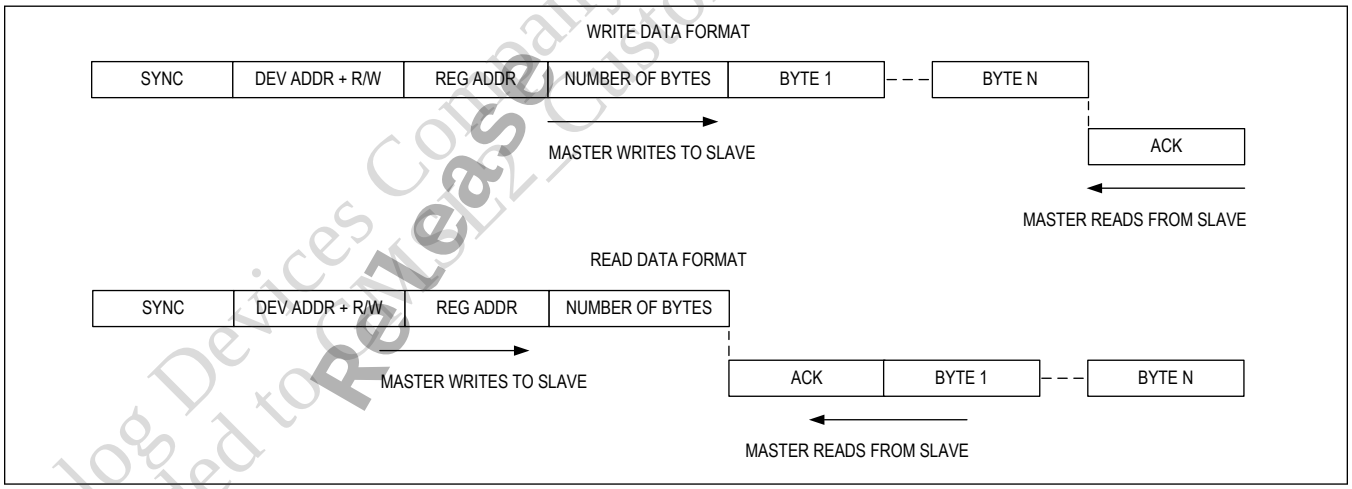

Figure 23. UART Protocol for Base Mode

UART Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the ECU, allowing the ECU to communicate only with peripheral devices. The ECU cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL link. Ignoring UART transactions prevents inadvertent miss-programming

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of serializer and deserializer registers. The device addresses of the serializer and deserializer in this mode are not programmable.

Switching Between UART Base and Bypass Modes

There are two ways to switch between base mode and bypass mode: programming the BYPASS_TO register and using the device MS pin.

When setting bypass mode via register writes the bypass mode can be temporary or permanent. When BYPASS_TO is programmed to have a timeout (2, 8 or 32ms), bypass mode is active only as long as there is UART activity. When there is no UART activity for the selected timeout, both devices exit bypass mode and the bit is automatically cleared. Only when

Permanent bypass mode is desired (BYPASS_TO = 11) the UART channel will remain in bypass mode until subsequent reprogramming or a device reset occurs.

When set by the MS pin, a high pin level puts the device into bypass mode, and a low level puts the device in base mode. MS is set on the fly and is not latched on power-up.

UART Frame Format

Regular UART frames with an even parity bit are used to carry 1 byte of data each. A frame consists of a low start bit followed by 8 data bits, a parity bit, and is finished with a high stop bit. The parity bit is high if the number of ones in the 8 bits of data is odd. Otherwise, the parity bit is low. There must be at least 1 high stop bit. If the next frame is in the same packet, there can be at most 4 high bits from the end of the stop bit to the beginning of the next start bit. Note that in the case of a parity bit error, the packet is discarded, starting from the frame with the error. The start of each frame is always a high-to-low transition (i.e., the stop bit is high and the start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer calibrates the length of 1 UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions, and the recipient of the data must perform error checking. The parity bit (which is enabled by default in bypass mode) can be disabled before entering bypass mode. Note that the bit rate in bypass mode must be the same bit rate last used in base mode.

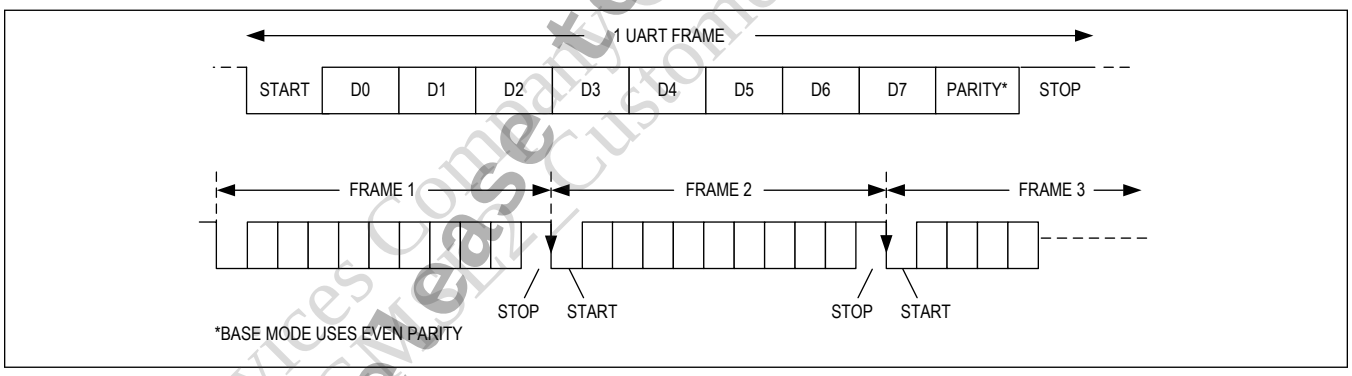

Figure 24. UART Data Format for Base Mode

Synchronization Frame

The serializer/deserializer must calibrate internal bit-length counters with the UART bit rate for proper recovery of UART frames. A sync frame (a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal 150MHz clock. Sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next sync frame.

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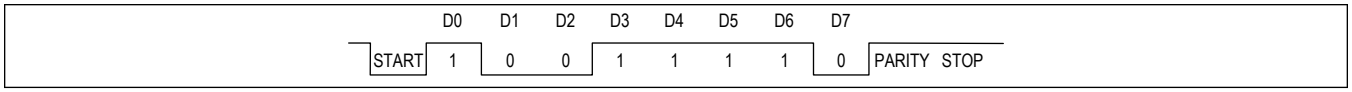

Figure 25. UART Synchronization Frame

Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors were detected in the transmitted packet, and it was recognized as valid. This is sent after the last bit of a successfully recognized packet has been received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

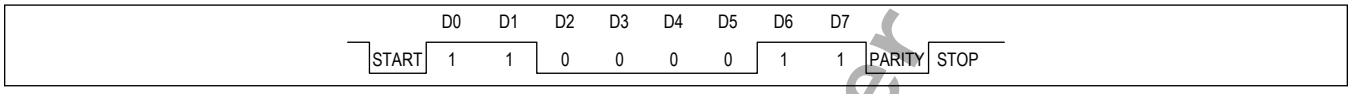

Figure 26. UART Acknowledge Frame

Write Packet

Write packets consist of a 5-byte packet header followed by one or more data bytes. A packet is recognized as a write packet when the LSB of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors were detected while receiving the write packet and the write packet is valid. Byte count indicates the number of data bytes to be written, and it cannot be 0.

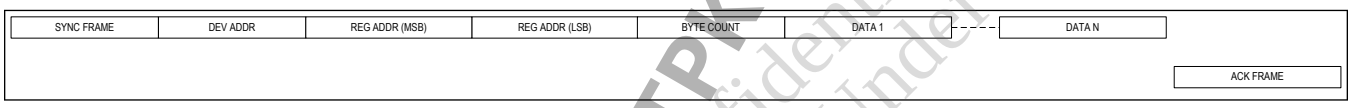

Figure 27. UART Write-Packet Format

Read Packet

Read packet consists of 5 bytes. The LSB of the device address frame is 1 for read packets. If no errors were detected while receiving the read packet and the packet is valid, the addressed device responds with an acknowledge frame followed by 1 or more data bytes. Byte count indicates the number of data bytes to be read, and it cannot be 0.

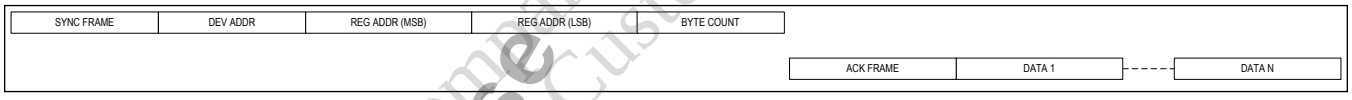

Figure 28. UART Read-Packet Format

I²C/UART Control-Channel Programming with CRC and Message Counter

By default, I²C/UART cyclic redundancy check (CRC) and Message Counter features are disabled in MAX96749AC/749AP/767/769/855/857/859/861. The conventional (legacy) I²C/UART packet format is the default. When desired, these functions will be enabled by a register write by using the legacy packet format and then all subsequent packets will use the new I²C/UART Control-Channel Programming with CRC and Message Counter (ASIL-protected format).

I²C

From ASIL-B functional safety requirements, there needs to be a mechanism to prevent hardware faults or random errors from misconfiguring the device. Therefore, CRC has been added to I²C and UART transactions. The MAX96749AC/749AP/767/769/855/857/859/861 I²C slave controller will expect and validate a CRC-8 byte (8-bit cyclic redundancy check) for all communication messages to maintain data integrity. This will ensure the proper write data is received and the device is configured properly.

When directly communicating with the MAX96749AC/749AP/767/769/855/857/859/861 via the I²C interface, the ECU must compute and send a CRC byte protecting the data sent to the device. The incoming CRC Byte is called a packet error checking (PEC) Byte. Likewise, for returned read packets (transactions), the ECU should store the received data, perform the CRC calculation, and compare the results to the received PEC Byte provided by the MAX96749AC/749AP/

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767/769/855/857/859/861 before accepting the data received as valid. To support PEC Byte computation and checking, the ECU must implement a CRC-8 encoding and decoding algorithm based on the following polynomial (0xA6):

$$P(x) = x8 + x6 + x3 + x2 + 1$$

This polynomial is capable of protecting a data stream of up to 247 bits with a Hamming Distance of 3, meaning any data stream 247 bits or less in length with any combination of 3 bits of error or less is guaranteed to be identified. If more than 3 bits of error is encountered, the CRC operation will very likely identify the problem, though this cannot be mathematically guaranteed.

A hardware implementation of the CRC calculation is shown in Figure 29. The CRC Engine shown is implemented internally within the MAX96749AC/749AP/767/769/855/857/859/861 I^{2}C interface. A similar implementation would be required in the ECU hardware or software to support direct I^{2}C communication, for purposes of generating the PEC Bytes sent to the MAX96749AC/749AP/767/769/855/857/859/861, or for checking PEC Bytes received from the MAX96749AC/749AP/767/769/855/857/859/861. The incoming I^{2}C data stream is fed into the CRC Engine MSB first. Once the data stream has been completely shifted into the engine, the CRC Remainder is known; this becomes the PEC Byte for both incoming write data and outgoing read data. Be sure to note the ordering of the bits within the Remainder. Note all I^{2}C transactions supply the command and data stream MSB first. Also, note that the PEC Byte itself is not included in the CRC calculation; it is only computed on the transaction header and data.

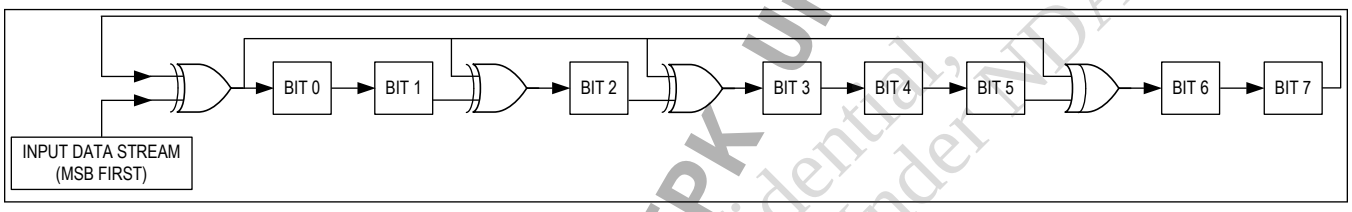

Figure 29. Hardware Implementation of CRC Calculation

I^{2}C Write Transaction

For incoming I^{2}C data streams, the MAX96749AC/749AP/767/769/855/857/859/861 will first clear the CRC Engine to 0 and then input the incoming data stream into the CRC Engine, MSB first. After the final bit of data is processed (in this case, the LSB of the incoming data stream is applied to the Engine), the Engine is stopped, and the computed CRC Remainder is known. The incoming PEC byte is calculated by the ECU using its copy of the CRC Engine then follows within the I^{2}C transaction (also MSB first) and is internally compared against the CRC Remainder as calculated by the MAX96749AC/749AP/767/769/855/857/859/861. If the PEC Byte received matches the CRC remainder calculated for the incoming data stream, the PEC operation is successful, and the transaction is accepted and executed by the MAX96749AC/749AP/767/769/855/857/859/861. If there is a mismatch, the MAX96749AC/749AP/767/769/855/857/859/861 will do the following:

- The write command will not be executed
- The slave controller will Nack the data packet
- The transaction will be retried
- Readback of the MAX96749AC/749AP/767/769/855/857/859/861 calculated PEC Byte will be possible (Ack/Nack could have errors)
- For critical writes, the ECU can also perform a readback of the written data to ensure success
- The CRC mismatch will trigger an error counter. The counter will increment for each CRC error. Once the counter reaches a programmable threshold, ERRB will be asserted.

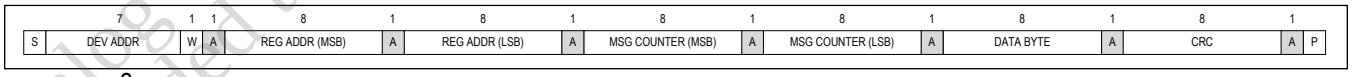

Figure 30. I^{2}C Single-Byte Write Transactions with CRC

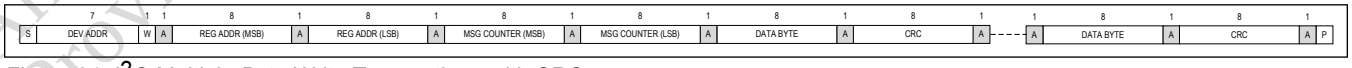

Figure 31. I^{2}C Multiple-Byte Write Transactions with CRC

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Figure 30 and Figure 31 show the I²C write transaction formatting with CRC PEC bytes added. The first CRC PEC Byte covers the data for the first 6 bytes: Device Address, Register Address MSB, Register Address LSB, Message Counter MSB, Message Counter LSB, and the first Data byte. If there are multiple Data bytes after the first, then a CRC PEC Byte is appended after each subsequent data byte. The CRC Engine is reset to 0 after each CRC calculation is completed, meaning a fresh CRC calculation is done each time. This is needed to prevent the number of data bits into the CRC Engine from exceeding the 247 bits allowed by the polynomial.

I²C Read Transactions

For outgoing I²C data streams, the MAX96749AC/749AP/767/769/855/857/859/861 will first clear the CRC Engine to 0 and then provide the outgoing data stream to the CRC Engine, MSB first. After the final bit of data is processed (in this case, the LSB of the outgoing data stream is applied to the Engine), the Engine is stopped and the CRC Remainder is known, and this becomes the outgoing PEC Byte. The outgoing PEC Byte, as calculated by the MAX96749AC/749AP/767/769/855/857/859/861 using its copy of the CRC Engine, then follows within the I²C transaction (also MSB first). As the ECU receives the data stream from the MAX96749AC/749AP/767/769/855/857/859/861, it should apply the data to its copy of the CRC Engine (MSB first, in the order it arrives in the I²C transaction, until the LSB of the data stream is applied to the Engine). At this point, there are two equivalent ways the ECU can complete the PEC operation to establish the validity of the received data:

Direct Comparison Method: the ECU stops the CRC Engine once the data stream MSB is applied and compares the resulting CRC Remainder to the PEC Byte supplied by the MAX96749AC/749AP/767/769/855/857/859/861 (again, MSB first). If the 2 bytes match, the data is accepted as valid, otherwise, it should be rejected. This is the method employed by the MAX96749AC/749AP/767/769/855/857/859/861 internally, as described above.

Zero Remainder Method: the ECU continues CRC Engine computations after the data LSB is applied by appending the received PEC Byte to the end of the data stream, MSB first (i.e. in the order received during the I²C transaction). Once the LSB of the PEC Byte arrives at the input of the CRC Engine, if the resulting CRC Remainder = 00h, the data is accepted as valid, otherwise it should be rejected.

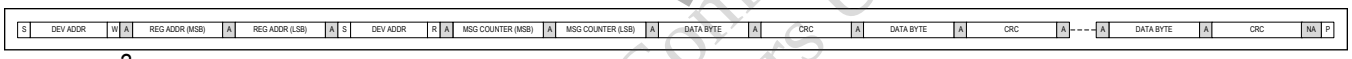

Figure 32. I²C Multiple-Byte Read Transactions with CRC

Figure 32 shows the I²C read transaction formatting with CRC PEC Bytes added. The first CRC PEC Byte covers the data for the first 7 bytes: Device Address, Register Address MSB, Register Address LSB, repeated Device Address, Message Counter MSB, Message Counter LSB, and the first read Data byte. If there are multiple read Data bytes after the first, then a CRC PEC Byte is appended after each subsequent read Data byte. The CRC Engine is reset to 0 after each CRC calculation is completed, meaning a fresh CRC calculation is done each time. This is needed to prevent the number of data bits into the CRC Engine from exceeding the 247 bits allowed by the polynomial.

I²C Message Counter

Another functional safety mechanism is a message counter that is part of each I²C transaction. The ECU and MAX96749AC/749AP/767/769/855/857/859/861 device will both keep a message counter. For each I²C write or read transaction, each side will increment their copy of the counter. For write transactions, the ECU will send the message counter to the MAX96749AC/749AP/767/769/855/857/859/861 as part of the I²C transaction. The MAX96749AC/749AP/767/769/855/857/859/861 will then compare the received message counter to its copy. If it is a match, then the write command is accepted and will be executed as normal, assuming the CRC value also matches. If the message counter is a mismatch, the MAX96749AC/749AP/767/769/855/857/859/861 will do the following: (same as if a CRC mismatch)

- The write command will not be executed
- The slave controller will Nack the data packet
- The transaction will be retried

Readback of the MAX96749AC/749AP/767/769/855/857/859/861 calculated PEC Byte will be possible (Ack/Nack could have errors).

For critical writes, the ECU can also perform a readback of the written data to ensure success.

The CRC mismatch will trigger an error counter. The counter will increment for each CRC error. Once the counter reaches a programmable threshold, ERRB will be asserted.

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For read transactions, the MAX96749AC/749AP/767/769/855/857/859/861 I^{2}C slave will send the message counter to the ECU, before the read Data and CRC bytes. The ECU must then ensure its copy of the message counter matches the received value from the MAX96749AC/749AP/767/769/855/857/859/861. Also, the read transaction has a repeated start condition and device address byte. The message counter will be incremented twice per read transaction, once when each device address byte matches. This is needed because a read could be initiated in two different ways. One is the way shown above, and the second is with only the second start condition and device address, immediately reading data from whatever was the last used register address. The MAX96749AC/749AP/767/769/855/857/859/861 will support both types, therefore incrementing the message counter twice with the first way, and once with the second.

For each serializer or deserializer device, there will be a single counter incremented for both write and read transactions. For a system with both a serializer and deserializer, each of the two devices will keep their own counter. The device's counter will increment only when the ECU transaction is for that particular device when the I^{2}C device address matches that device. Therefore, the ECU will need to maintain separate transaction counters for each of the serializer and deserializer, and send the appropriate counter value when writing to each device.

In addition, the serializer and deserializer will increment the message counter regardless of whether the message counter matches or not. It will also increment regardless of whether the CRC value matches or not. In other words, the message counter will increment for each I^{2}C write or read transaction, regardless of message counter or CRC errors. Additionally, the counter will increment once per transaction, regardless of the number of write or read data bytes in that transaction. The serializer and deserializer counter values will be readable by the ECU on demand.

Additional Information

The I^{2}C can also operate in bypass or tunneling mode. This passes transactions from the ECU to the SER, through the GMSL link to the DES, and then to a peripheral. These transactions will not have this CRC PEC Byte scheme, nor the message counter, and will just be passed through as-is. The ECU and peripheral are free to use some other CRC scheme if they like, but the CRC described here only applies to transactions to the SER or DES registers.

UART

From ASIL-B functional safety requirements, there needs to be a mechanism to prevent hardware faults or random errors from misconfiguring the device. Therefore, CRC will be added to I^{2}C and UART transactions. The MAX96749AC/749AP/767/769/855/857/859/861 UART slave controller will expect and validate a CRC-8 byte for all communication messages to maintain data integrity. This will ensure the proper write data is received and the device is configured properly.

When directly communicating with the MAX96749AC/749AP/767/769/855/857/859/861 via the UART interface, the ECU must compute and send a CRC Byte protecting the data sent to the device. The incoming CRC Byte is called a Packet Error Checking (PEC) byte. Likewise, for returned read packets, the ECU should store the received data, perform the CRC calculation, and compare the results to the received PEC Byte provided by the MAX96749AC/749AP/767/769/855/857/859/861 before accepting the data received as valid. To support PEC Byte computation and checking, the ECU must implement a CRC-8 (8-bit Cyclic Redundancy Check) encoding and decoding algorithm based on the following polynomial (0xA6):

P(x) = x8 + x6 + x3 + x2 + 1

This polynomial is capable of protecting a data stream of up to 247 bits with a Hamming Distance of 3, meaning any data stream 247 bits or less in length with any combination of 3 bits of error or less is guaranteed to be identified. If more than 3 bits of error is encountered, the CRC operation will very likely identify the problem, though this cannot be mathematically guaranteed. This Hamming Distance of 3 is in addition to the UART parity bit on each frame.

A hardware implementation of the CRC calculation is shown in the diagram below. The CRC Engine shown is implemented internally within the MAX96749AC/749AP/767/769/855/857/859/861 UART interface. A similar implementation would be required in the ECU hardware or software to support direct UART communication, for purposes of generating the PEC Bytes sent to the MAX96749AC/749AP/767/769/855/857/859/861, or for checking PEC Bytes received from the MAX96749AC/749AP/767/769/855/857/859/861. The incoming UART data stream is fed into the CRC Engine LSB first. Once the data stream has been completely shifted into the engine, the CRC Remainder is known; this becomes the PEC Byte for both incoming write data and outgoing read data. Be sure to note the ordering of the bits within the Remainder. Note all UART transactions supply the command and data stream LSB first. Also, note that the PEC Byte itself is not included in the CRC calculation; it is only computed on the packet header and data.

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UART Write Transactions

For incoming UART data streams, the MAX96749AC/749AP/767/769/855/857/859/861 will first clear the CRC Engine to 0 and then input the incoming data stream into the CRC Engine, LSB first. After the final bit of data is processed (in this case, the MSB of the incoming data stream is applied to the Engine), the Engine is stopped and the computed CRC Remainder is known. The incoming PEC Byte as calculated by the ECU using its copy of the CRC Engine then follows within the UART transaction (also LSB first) and is internally compared against the CRC Remainder as calculated by the MAX96749AC/749AP/767/769/855/857/859/861. If the PEC Byte received matches the CRC Remainder calculated for the incoming data stream, the PEC operation is successful, and the transaction is accepted and executed by the MAX96749AC/749AP/767/769/855/857/859/861. If there is a mismatch, the MAX96749AC/749AP/767/769/855/857/859/861 will do the following:

- The write command will not be executed
- The slave controller will Nack the data packet
- The transaction will be retried

Readback of the MAX96749AC/749AP/767/769/855/857/859/861 calculated PEC Byte will be possible (Ack/Nack could have errors)

For critical writes, the ECU can also perform a readback of the written data to ensure success

The CRC mismatch will trigger an error counter. The counter will increment for each CRC error. Once the counter reaches a programmable threshold, ERRB will be asserted.

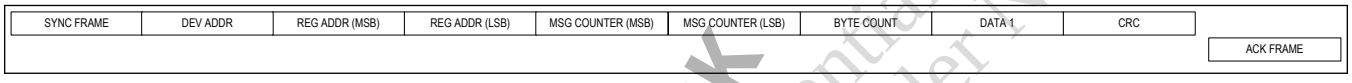

Figure 33. UART Single-Byte Write Packet with CRC

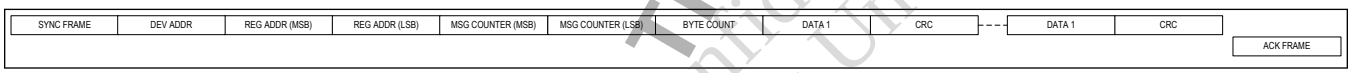

Figure 34. UART Multiple-Byte Write Packet with CRC

Figure 33 and Figure 34 show the UART write packet formatting with CRC PEC Bytes added. The first CRC PEC Byte covers the data for the first eight frames: Sync Frame, Dev Addr, Reg Addr MSB, Reg Addr LSB, Message Counter MSB, Message Counter LSB, Byte Count, and the first Data byte. If there are multiple Data bytes after the first, then a CRC PEC Byte is appended after each subsequent Data byte. The CRC Engine is reset to 0 after each CRC calculation is completed, meaning a fresh CRC calculation is done each time. This is needed to prevent the number of data bits into the CRC Engine from exceeding the 247 bits allowed by the polynomial.

UART Read Transactions

For outgoing UART data streams, the MAX96749AC/749AP/767/769/855/857/859/861 will first clear the CRC engine to 0 and then provide the outgoing data stream to the CRC Engine, LSB first. After the final bit of data is processed (in this case, the MSB of the outgoing data stream is applied to the Engine), the Engine is stopped and the CRC Remainder is known, and this becomes the outgoing PEC Byte. The outgoing PEC Byte, as calculated by the MAX96749AC/749AP/767/769/855/857/859/861 using its copy of the CRC Engine, then follows within the UART transaction (also LSB first). As the ECU receives the data stream from the MAX96749AC/749AP/767/769/855/857/859/861, it should apply the data to its copy of the CRC Engine (LSB first, in the order it arrives in the UART transaction, until the MSB of the data stream is applied to the engine). At this point, there are two equivalent ways the ECU can complete the PEC operation to establish the validity of the received data:

Direct Comparison Method: the ECU stops the CRC Engine once the data stream MSB is applied and compares the resulting CRC Remainder to the PEC Byte supplied by the MAX96749AC/749AP/767/769/855/857/859/861 (again, LSB first). If the 2 bytes match, the data is accepted as valid, otherwise, it should be rejected. This is the method employed by the MAX96749AC/749AP/767/769/855/857/859/861 internally, as described above.

Zero Remainder Method: the ECU continues CRC Engine computations after the data MSB is applied by appending the received PEC Byte to the end of the data stream, LSB first (i.e. in the order received during the UART transaction). Once the MSB of the PEC Byte arrives at the input of the CRC Engine, if the resulting CRC Remainder = 00h, the data is

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accepted as valid, otherwise it should be rejected.

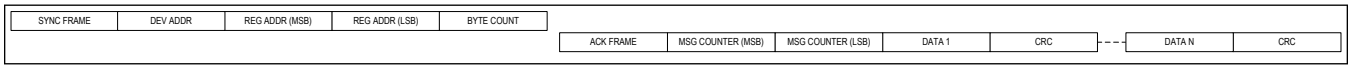

Figure 35. UART Multiple-Byte Read Packet with CRC

Figure 35 shows the UART read packet formatting with CRC PEC Bytes added. The first CRC PEC Byte covers the data for the first seven frames plus the first data byte: Sync Frame, Dev Addr, Reg Addr MSB, Reg Addr LSB, Message Counter MSB, Message Counter LSB, Byte Count, and the first Data byte. If there are multiple read Data bytes after the first, then a CRC PEC Byte is appended after each subsequent read Data byte. There is no CRC on the Ack Frame. This is because when the master waits for the Ack Frame, it waits for a specific value, 0xC3. If there is a bit error on the Ack Frame, the master would not detect the Ack, and it would be treated as a Nack, and the transaction would be retried. The CRC Engine is reset to 0 after each CRC calculation is completed, meaning a fresh CRC calculation is done each time. This is needed to prevent the number of data bits into the CRC Engine from exceeding the 247 bits allowed by the polynomial.

UART Message Counter

Another functional safety mechanism is a message counter that is part of each UART packet. The ECU and MAX96749AC/749AP/767/769/855/857/859/861 device will both keep a message counter. For each UART write or read packet, each side will increment their copy of the counter. For write packets, the ECU will send the message counter to the MAX96749AC/749AP/767/769/855/857/859/861 as part of the UART packet. The MAX96749AC/749AP/767/769/855/857/859/861 will then compare the received message counter to its copy. If it is a match, then the write command is accepted and will be executed as normal, assuming the CRC value also matches. If the message counter is a mismatch, the MAX96749AC/749AP/767/769/855/857/859/861 will do the following: (same as if a CRC mismatch)

- The write command will not be executed
- The slave controller will Nack the data packet
- The transaction will be retried

Readback of the MAX96749AC/749AP/767/769/855/857/859/861 calculated PEC Byte will be possible (Ack/Nack could have errors).

For critical writes, the ECU can also perform a readback of the written data to ensure success.

The CRC mismatch will trigger an error counter. The counter will increment for each CRC error. Once the counter reaches a programmable threshold, ERRB will be asserted.

For read packets, the MAX96749AC/749AP/767/769/855/857/859/861 UART slave will send the message counter to the ECU, before the read Data and CRC bytes. The ECU must then ensure its copy of the message counter matches the received value from the MAX96749AC/749AP/767/769/855/857/859/861.

For each serializer or deserializer device, there will be a single counter incremented for both write and read packets. For a system with both a serializer and deserializer, each of the two devices will keep their own counter. The device's counter will increment only when the ECU packet is for that particular device when the UART device address matches that device. Therefore, the ECU will need to maintain separate packet counters for each of the serializer and deserializer, and send the appropriate counter value when writing to each device.

In addition, the serializer and deserializer will increment the message counter regardless of whether the message counter matches or not. It will also increment regardless of whether the CRC value matches or not. In other words, the message counter will increment for each UART write or read packet, regardless of message counter or CRC errors.

Additionally, the counter will increment once per packet, regardless of the number of write or read data bytes in that packet. The serializer and deserializer counter values will be readable by the ECU on demand.

Additional Information

The UART can also operate in bypass or tunneling mode. This passes packets from the ECU to the SER, through the GMSL link to the DES, and then to a peripheral. These packets will not have this CRC PEC Byte scheme, nor the message counter, and will just be passed through as-is. The ECU and peripheral are free to use some other CRC scheme if they like, but the CRC described here only applies to packets to the SER or DES registers.

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Additional Control Channel Features

The MAX96749AC/749AP/767/769/855/857/859/861 device control channel configuration is detailed in Figure 36.

- The Main CC, PT#1, and PT#2 I²C/UART pins can be arbitrarily connected to the internal CC', PT#1', and PT#2' buses via bit fields in registers CC_10/11/12.
- PT#1 can independently be connected to read the serializer and deserializer control registers via bit PT1_READ_EN.
- PT#1' and PT#2' are tunneled across the link.
- The control channel connections for Link A and Link B are the same.
- CC' is connected to the serializer control channel and both deserializer control channels.
- CC' access to the deserializers control channel can be disabled using the DIS_REM_CC pin
  - Deserializer control and setup is then handled locally at the display
  - PT#1 read access to the deserializer registers remains active when the CC' channel is disabled with DIS_REM_CC

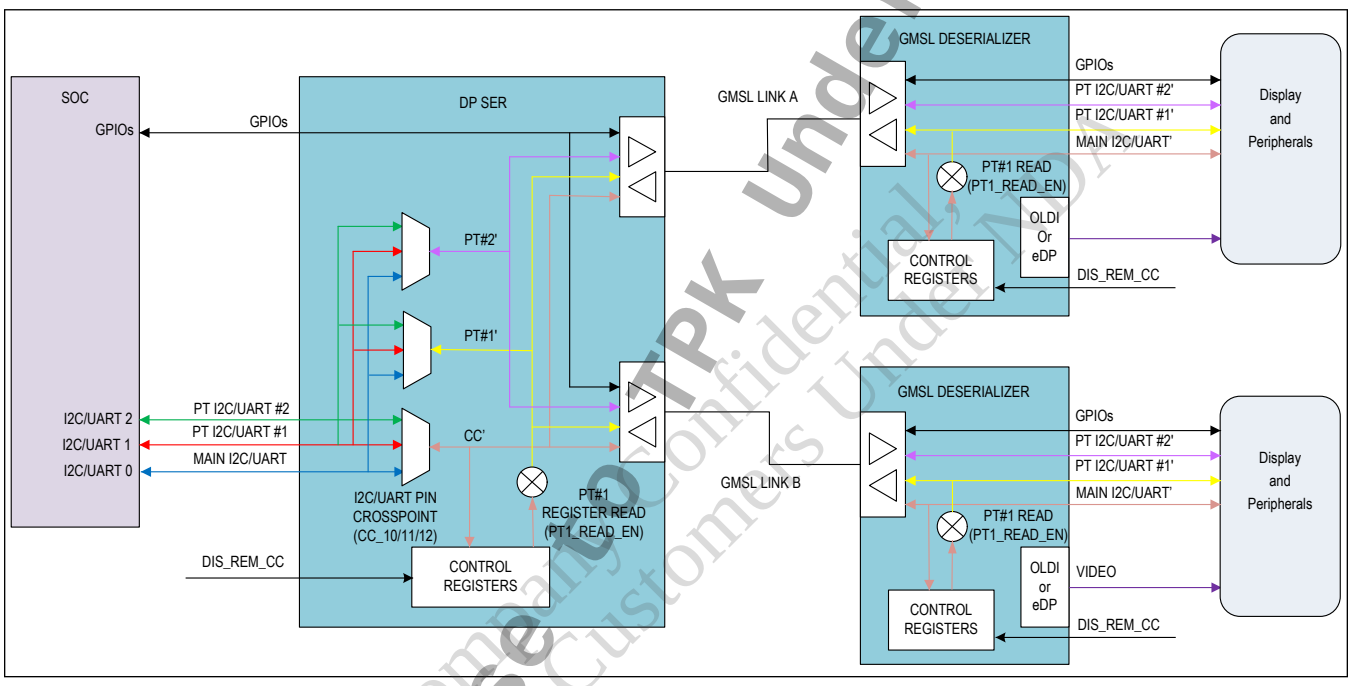

Figure 36. Main and PT Control Channel Configuration

Bussed I²C Pass-Through

In legacy GMSL2 PT designs, it was only possible to have a point-to-point I²C PT link, between one SER and one DES only where one µC may be connected to SER or DES. If PT was enabled in multiple DES, SER could not differentiate the packets coming from different DES.

In MAX96749AC/749AP/767/769/855/857/859/861 designs, bussed connection is supported: The same PT channel can be enabled in one SER and several DES. When the µC is connected to SER, it can communicate with peripherals connected to each DES by addressing them separately (each peripheral should have a unique I²C address). The SER PT channel in the MAX96749AC/749AP/767/769/855/857/859/861 SERs can differentiate packets coming from different DES.

I²C Arbitration

In applications where the main and PT I²C channels have multiple ECUs, one connected to each DES, arbitration allows multiple µCs to concurrently start an I²C packet on DES-side. This works like this: When the ECU on first DES starts a packet, SER selects the first DES and starts processing the packet it receives from the first DES. If the ECU on second DES starts a packet while the first DES is selected, the second DES starts doing clock stretch to the µC connected to itself. When SER finishes processing the packet from the first DES and switches to the second DES, the second DES

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releases clock stretch and allows its ECU to continue with the rest of the packet. This arbitration mechanism lifts the requirement of external synchronization between multiple ECUs. They can asynchronously start communication anytime.

To limit clock stretch time and allow more concurrency, ECUs should limit the length of I^{2}C packets (8 or 16 or 32 bytes for example depending on use case).

Note: This feature is only possible with newer GMSL3/2 deserializers. It does not work with legacy GMSL2 devices.

UART Wait Time in Splitter and Independent Link Modes

When one MAX96749AC/749AP/767/769/855/857/859/861 is driving two deserializers with UART as the main control channel, we require a wait time when switching accesses to DES_A and DES_B or vice versa. This is by default 256µs and set by UART_ARB_TO register.

So, after reading or writing DES_A and receiving the response, wait for at least 256us to start reading or writing DES_B.

Additionally, MAX96749AC/749AP/767/769/855/857/859/861 devices have another register ARB_TO_LEN. When there are more than one DES-side ECUs, we assume they don't usually know about each other's actions. ARB_TO_LEN and UART_ARB_TO allows one ECU to grab and hold the UART channel to itself.

For example, a typical scenario is like this:

1. ECU_A starts a UART packet and wins arbitration because UART channel has been idle for a while when the packet starts. (SER listens to packets from both DES and it will let the first one that starts a packet to win arbitration.)
2. ECU_A performs 1 or more reads/writes with delays between packets not exceeding ARB_TO_LEN/UART_ARB_TO. With the start of first packet, SER allows ECU_A to communicate and it starts blocking any packets from ECU_B. This may be useful because ECU_A may want to ensure that several registers are written without ECU_B interfering in-between those writes.
3. ECU_A ceases UART communication. UART line becomes idle for longer than ARB_TO_LEN/UART_ARB_TO.
4. ECU_B can start a UART packet and wins arbitration, then sequence repeats from Step 1 with ECU_A replaced with ECU_B. Or ECU_A again starts communication, go back to Step 1.

During steps 1, 2, 3, ECU_A has the UART link to itself, so if ECU_B starts a UART packet during those times, it will get no response. No response in UART means "NACK" and so ECU_B is forced to retry after waiting for some time.

Full I^{2}C Crossbar

Full crossbar between CC, PT1, PT2 pins and GMSL CC, PT1, PT2 channels: This allows any one set of CC, PT1, PT2 pins to connect to any channel. For example, main CC pins can be connected to PT1 channel instead of main CC. Or main CC pins can be connected to both CC and PT1 channels on GMSL. This feature allows more flexibility for some use cases and possibly solving interesting customer problems related to how CC, PT1, and PT2 channels are used. In DP Serializer applications, the I^{2}C-over-AUX is also included in crossbar, so it can be connected to one or more of Main CC, PT1, PT2 channels. There is also the option to connect I^{2}C-over-AUX to PT1 or PT2 pins only but not to PT1/PT2 channels. This allows an I^{2}C peripheral connected to the DP serializer's PT1 or PT2 pins to be accessed by ECU through I^{2}C-over-AUX.

PT1 Local/Remote Register Read

The pass-through I^{2}C1/UART1 channel (PT1) (not the PT2 channel) has an additional feature in support of ASIL system design.

The PT1 channel can be used to verify (read) the main local/remote registers to verify the main channel I^{2}C/UART registers have been correctly written. The remote (DES) register read remains available even in the event the remote control channel is disabled (DIS_REM_CC pin). The maximum transaction length allowed for both I^{2}C main and PT1 is 32 bytes when this mode is used. Prior to using PT1 register read access set SLV_TO = 110 (32ms) and SLV_TO_PT_1 = 110 (32ms).

When UART is used to read registers on PT1 the read response is delayed when another packet is active on Main control channel.

The allowed, collision-free, configurations are as follows:

- Main I^{2}C/UART read/write and local PT1 read
- Main I^{2}C/UART read/write and remote PT1 read

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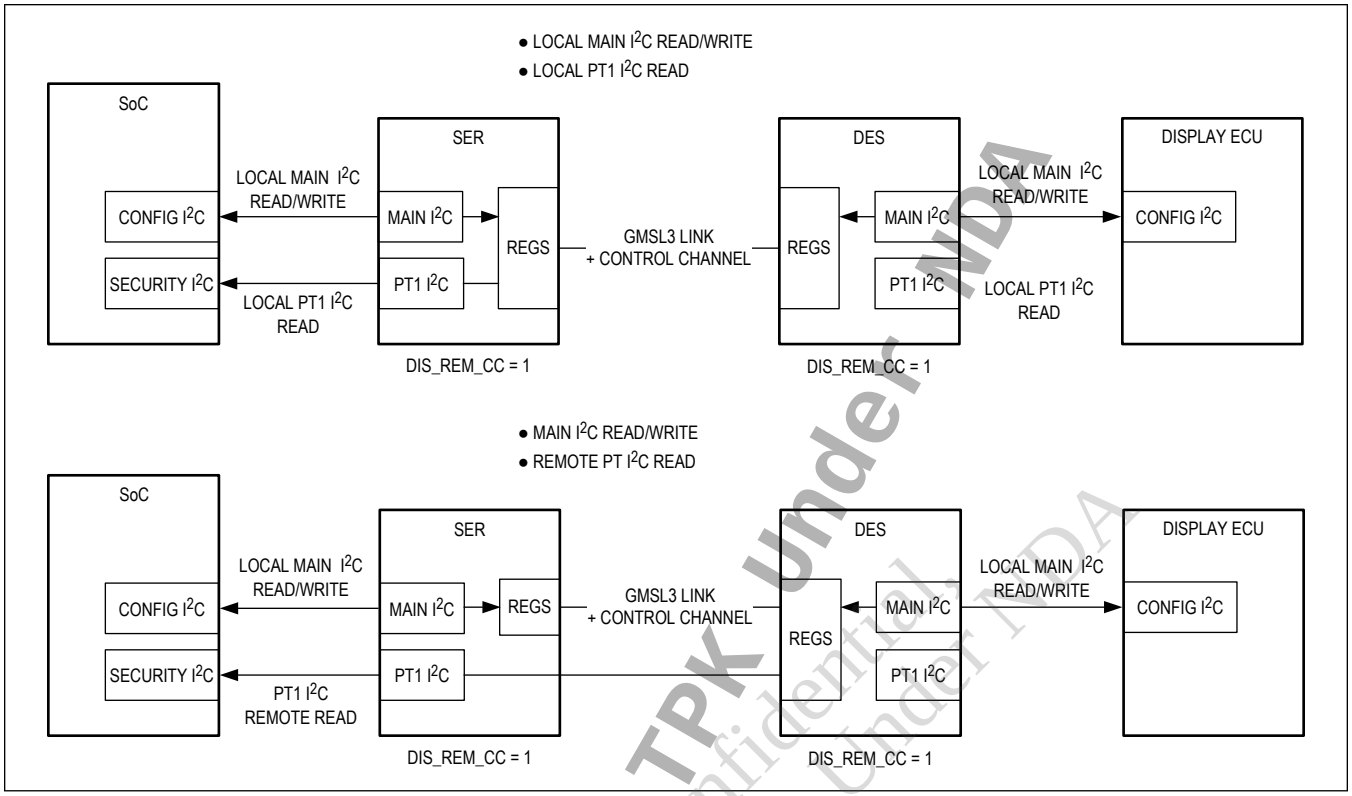

Figure 37. Allowed – No Collisions

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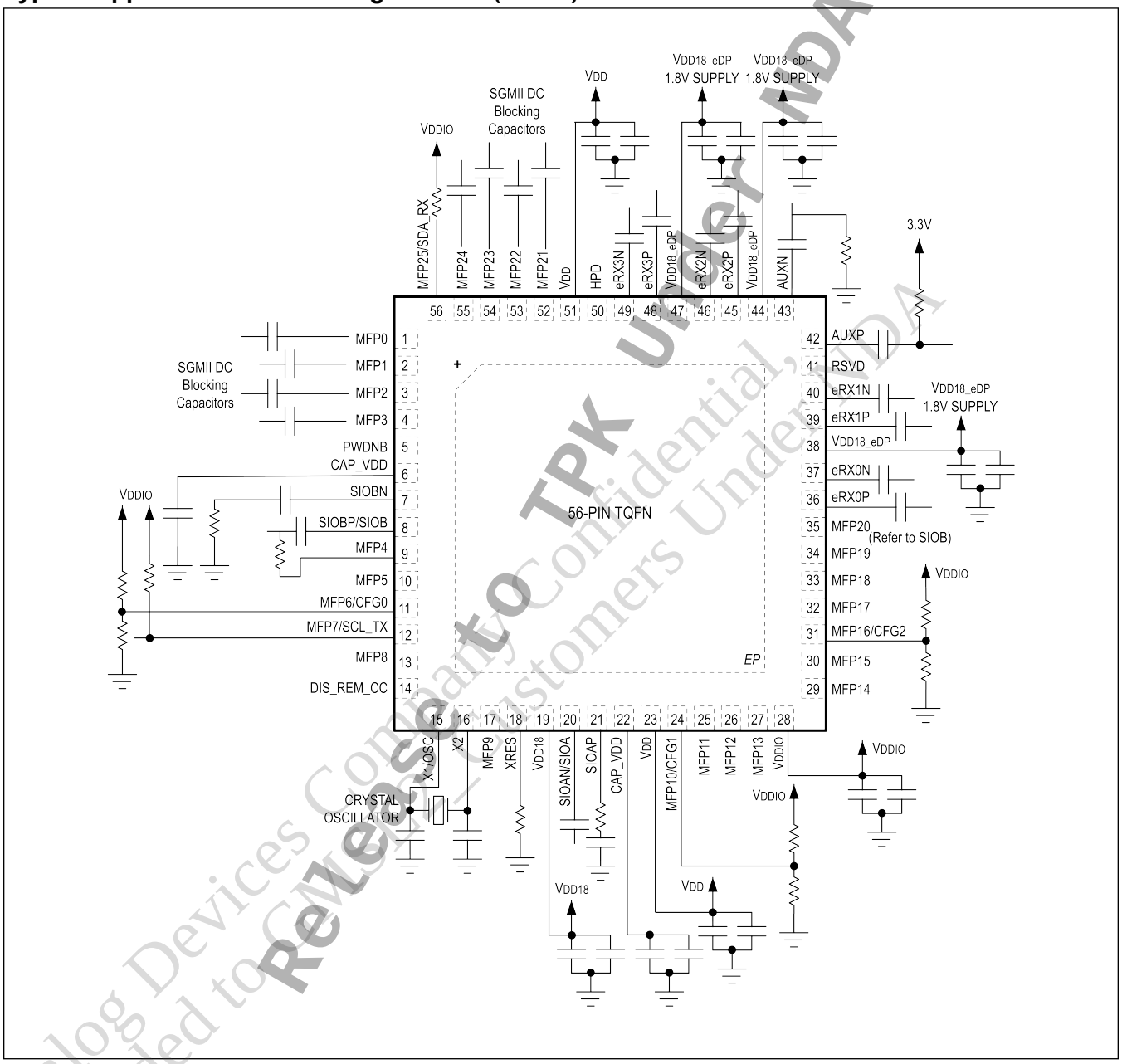
Typical Application Circuits

Typical Application Circuit - Single Ended (COAX)



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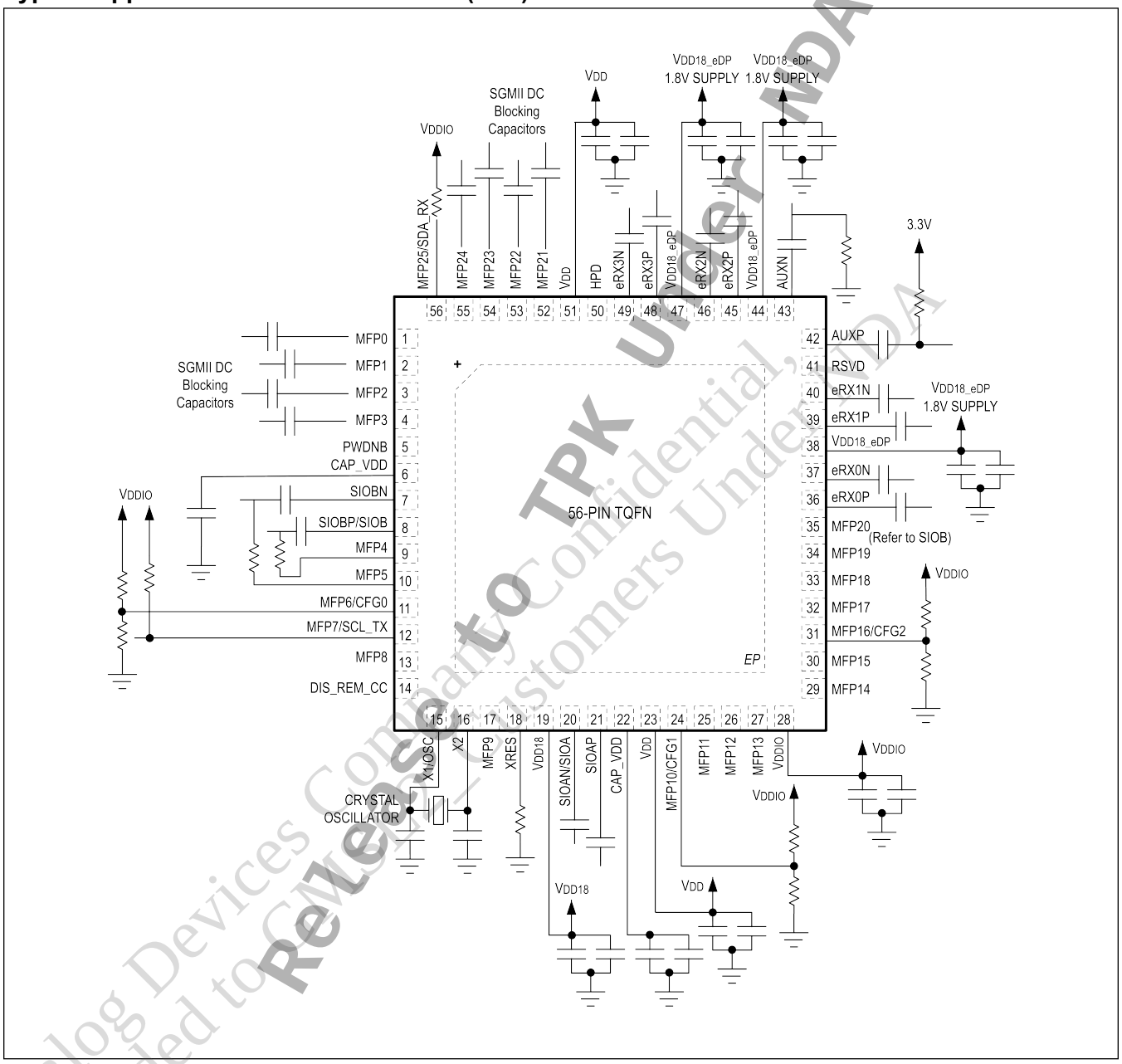
Typical Application Circuits (continued)

Typical Application Circuit - Differential (STP)



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Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	DP and GMSL HDCP
MAX96749ACGTN/V+	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	No
MAX96749ACGTN/V+T	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	No
MAX96749APGTN/V+	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	Yes**
MAX96749APGTN/V+T	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	Yes**
MAX96767GTN/V+*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	No
MAX96767GTN/V+T*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	No
MAX96769GTN/V+*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	Yes**
MAX96769GTN/V+T*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	Yes**
MAX96855GTN/V+*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	No
MAX96855GTN/V+T*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	No
MAX96857GTN/V+*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	Yes**
MAX96857GTN/V+T*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	Yes**
MAX96859GTN/V+*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	No
MAX96859GTN/V+T*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	No
MAX96861GTN/V+*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	Yes**
MAX96861GTN/V+T*	-40°C to +105°C	T5688+6C 56-lead TQFN-EP	Yes**
MAX96749ACGTN/VY+	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	No
MAX96749ACGTN/VY+T	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	No
MAX96749APGTN/VY+	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	Yes**
MAX96749APGTN/VY+T	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	Yes**
MAX96767GTN/VY+*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	No
MAX96767GTN/VY+T*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	No
MAX96769GTN/VY+*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	Yes**
MAX96769GTN/VY+T*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	Yes**
MAX96855GTN/VY+*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	No
MAX96855GTN/VY+T*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	No
MAX96857GTN/VY+*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	Yes**
MAX96857GTN/VY+T*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	Yes**
MAX96859GTN/VY+*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	No
MAX96859GTN/VY+T*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	No
MAX96861GTN/VY+*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	Yes**
MAX96861GTN/VY+T*	-40°C to +105°C	T5688Y+6C 56-lead SW TQFN-EP	Yes**

/V Denotes an automotive qualified part

+ Denotes a lead(Pb)-free/RoHS-compliant package

T Denotes tape and reel

Y Denotes Side-Wettable package

EP Denotes Exposed Pad

***HDCP parts require registration with Digital Content Protection, LLC*

**Future product—contact factory for availability.*

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Register Map

Reserved and Unused Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write). In this document default values are provided for read-only register bits. Read-only bit states are changed at powerup according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

HDCP (MAX96749AP/ MAX96769/ MAX96857/ MAX96861 Only)

The MAX96749AP/ MAX96769/ MAX96857/ MAX96861 has HDCP while the MAX96749AC/ MAX96767/ MAX96855/ MAX96859 does not. Register blocks (shown below), registers, and bitfields that refer to HDCP are reserved in the MAX96749AC/ MAX96767/ MAX96855/ MAX96859 and should not be changed from the default state.

Table 20. HDCP Register Blocks (MAX96749AP/ MAX96769/ MAX96857/ MAX96861 Only)

BLOCK NAME	REGISTER ADDRESS NAME
CFGL_AHDCP	0x00E0–0x00E7
HDCP_TX__HX	0x1600–0x16FF
HDCP_TX__HY	0x1700–0x17FF
HDCP_TX__HZ	0x1800–0x18FF
HDCP_TX__HU	0x1900–0x19FF

***Note**:* *Indicates that the register is stored when entering sleep mode and restored upon exit from sleep mode.

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x80	REG0[7:0]*	DEV_ADDR[6:0]							CFG_BLOCK
0x02	0x83	REG2[7:0]*	AUD_TX_Y_SRC	AUD_TX_X_SRC	AUD_TX_EN_Y	AUD_TX_EN_X	RSVD	RSVD	RSVD	RSVD
0x03	0x00	REG3[7:0]*	–	–	–	RSVD	RCLKEN	–	RCLKSEL[1:0]	
0x04	0x0D	REG4[7:0]*	GMSL3_B	GMSL3_A	HVD_OUT_EN	DIS_LOCAL_CC	RSVD	RSVD	RSVD	SW_INT
0x05	0xC0	REG5[7:0]*	LOCK_EN	ERRB_EN	LOCK_CFG[1:0]		PU_LF3	PU_LF2	PU_LF1	PU_LF0
0x07	0x07	REG7[7:0]*	–	–	CMP_STATUS_MASK[5:0]					
0x08	0x00	PWR0[7:0]	VDDBAD_STATUS[1:0]		CMP_STATUS[5:0]					
0x09	0x00	PWR1[7:0]	OVERTEMP	VDDBAD_STATUS_H	PORZ_STATUS[5:0]					
0x0C	0x35	PWR4[7:0]*	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			
0x0D	0xFF	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x01	REG14[7:0]	RSVD	RSVD	RSVD	RSVD	DEV_REV[3:0]			
TCTRL										
0x10	0x00	CTRL0[7:0]*	RESET_ALL	–	–	–	SLEEP	RSVD	–	–

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ADDRESS	RESET	NAME	MSB							LSB
0x11	0x0A	CTRL1[7:0]*	RSVD	RSVD	RSVD	–	RSVD	CXTP_B	RSVD	CXTP_A
0x13	0x00	CTRL3[7:0]	HPD_IN	–	–	–	LOCKED	ERROR	CMU_LOCKED	–
0x17	0x60	CTRL7[7:0]	RSVD	RSVD	RSVD	–	–	–	DIS_TEMP_WAKE_TO_SLEEP_B	DIS_TEMP_WAKE_TO_SLEEP_A
0x18	0x00	INTR0[7:0]*	–	–	–	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x19	0x00	INTR1[7:0]*	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x1A	0x0B	INTR2[7:0]*	RSVD	RSVD	REM_ERR_OEN_B	REM_ERR_OEN_A	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
0x1B	0x00	INTR3[7:0]	RSVD	RSVD	REM_ERR_FLAG_B	REM_ERR_FLAG_A	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x1C	0x08	INTR4[7:0]*	EOM_ERR_OEN_B	EOM_ERR_OEN_A	HDCP_INT_OEN_B	HDCP_INT_OEN_A	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	–
0x1D	0x00	INTR5[7:0]	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	HDCP_INT_FLAG_B	HDCP_INT_FLAG_A	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	–
0x1E	0xE6	INTR6[7:0]*	VDDCMP_INT_OEN	PORZ_INT_OEN	VDDBAD_INT_OEN	VDD_OV_OEN	DPRX_INT_OEN	APRBS_Y_ERR_OEN	APRBS_X_ERR_OEN	INT_ERR_OEN
0x1F	0x00	INTR7[7:0]	VDDCMP_INT_FLAG	PORZ_INT_FLAG	VDDBAD_INT_FLAG	VDD_OV_FLAG	DPRX_INT	APRBS_Y_ERR_FLAG	APRBS_X_ERR_FLAG	INT_ERR_FLAG
0x20	0x00	INTR8[7:0]*	SW_INT_OEN	VDDIO_OV_OEN	VDD1P8_OV_OEN	RSVD	LOCK_B_OEN	LOCK_A_OEN	LOCK_OEN	LOSS_OF_LOCK_OEN
0x21	0x00	INTR9[7:0]	SW_INT_FLAG	VDDIO_OV_FLAG	VDD1P8_OV_FLAG	RSVD	LOCK_B_FLAG	LOCK_A_FLAG	LOCK_FLAG	LOSS_OF_LOCK_FLAG
0x22	0x00	INTR10[7:0]*	LFLT_INT_OPEN_OEN	LFLT_INT_L2LS_OEN	LFLT_INT_BAT_S_OEN	LFLT_INT_GND_S_OEN	REG_CRC_ERR_OEN	I2C_UART_MSG CNTR_ERR_OEN	I2C_UART_CRC_ERR_OEN	HDCP2_INT_OEN
0x23	0x00	INTR11[7:0]	LFLT_INT_OPEN	LFLT_INT_L2LS	LFLT_INT_BAT_S	LFLT_INT_GND_S	REG_CRC_ERR_FLAG	I2C_UART_MSG CNTR_ERR_FLAG	I2C_UART_CRC_ERR_FLAG	HDCP2_INT_FLAG
0x24	0x51	DEV_ID16_LSB[7:0]*	DEV_ID16_LSB[7:0]							
0x25	0x00	DEV_ID16_MSB[7:0]*	DEV_ID16_MSB[7:0]							
0x26	0x22	LF0_LF1[7:0]	–	LF_1[2:0]			–	LF_0[2:0]		

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ADDRESS	RESET	NAME	MSB							LSB
0x27	0x22	LF2_LF3[7:0]	–	LF_3[2:0]			–	LF_2[2:0]		
LINK_CTRL A										
0x28	0x88	LCTRL0[7:0]*	RSVD	–	DES_CNT[1:0]		TX_RATE[1:0]		RSVD[1:0]	
0x29	0x00	LCTRL1[7:0]*	DIS_LOCK_TO	RSVD	RSVD	RSVD	–	–	RESET_ONESHOT	RESET_LINK
0x2A	0x00	LCTRL2[7:0]	DAISY_CHAIN_STATUS[1:0]		–	–	RSVD	RSVD	RSVD	LINK_LOCKED
0x2B	0x00	LCTRL3[7:0]	DEC_ERR[7:0]							
0x2C	0x00	LCTRL4[7:0]	IDLE_ERR[7:0]							
0x2D	0x00	LCTRL5[7:0]	PKT_CNT[7:0]							
0x2E	0x9F	LCTRL6[7:0]*	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x2F	0xDF	LCTRL7[7:0]*	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
LINK_CTRL B										
0x32	0x88	LCTRL0[7:0]*	RSVD	–	DES_CNT[1:0]		TX_RATE[1:0]		RSVD[1:0]	
0x33	0x00	LCTRL1[7:0]*	DIS_LOCK_TO	RSVD	RSVD	RSVD	–	–	RESET_ONESHOT	RESET_LINK
0x34	0x00	LCTRL2[7:0]	DAISY_CHAIN_STATUS[1:0]		–	–	RSVD	RSVD	RSVD	LINK_LOCKED
0x35	0x00	LCTRL3[7:0]	DEC_ERR[7:0]							
0x36	0x00	LCTRL4[7:0]	IDLE_ERR[7:0]							
0x37	0x00	LCTRL5[7:0]	PKT_CNT[7:0]							
0x38	0x9F	LCTRL6[7:0]*	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x39	0xDF	LCTRL7[7:0]*	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
TEST										
0x3C	0x04	TEST_0[7:0]	OTP_REV[7:0]							
0x3D	0x00	TEST_1[7:0]	DEBUG_EXTRA[7:0]							
TCTRL2										
0x40	0x00	REG0_INTR[7:0]*	FCRC_CHECK_ERR_OEN_Y	FCRC_CHECK_ERR_OEN_X	VOTE_ERR_FCRC_OEN_Y	VOTE_ERR_FCRC_OEN_X	VOTE_ERR_FCNT_OEN_Y	VOTE_ERR_FCNT_OEN_X	SGMII_INT_OEN	SGMII_DEC_ERR_OEN
0x41	0x88	REG1[7:0]*	ALT_DEV_ADDR_0[6:0]							–
0x42	0x8C	REG2[7:0]*	ALT_DEV_ADDR_1[6:0]							–
0x43	0xC8	REG3[7:0]*	ALT_DEV_ADDR_2[6:0]							–
0x44	0xCC	REG4[7:0]*	ALT_DEV_ADDR_3[6:0]							–
0x45	0x58	REG5[7:0]*	–	DP_AUX_MSG_INT_POLARITY	DP_AUX_MSG_INT_PIN_EN	DP_AUX_MSG_INT_PIN_SEL[1:0]		VID_DUP_X_Y	DUAL_LINK_MODE	USE_ALT_DEV_ADDR
0x46	0x00	REG6[7:0]*	–	–	–	–	–	CFG0_CONFIG_S[2:0]		

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ADDRESS	RESET	NAME	MSB							LSB
0x47	0x0C	REG7[7:0]*	CC_PIN_SEL_A[1:0]		CC_PIN_SEL_B[1:0]		RSVD[1:0]		RSVD	PCLKDETLOST_WO_PXRSTB
0x48	0x00	REG8_INTR[7:0]*	–	–	–	–	VTX_Y_PCLKDETLOST_OEN	VTX_X_PCLKDETLOST_OEN	SGMII_STOP_ERR_OEN	SGMII_PRBS_ERR_OEN
0x49	0x00	REG9[7:0]*	–	–	–	–	VTX_Y_PCLKDETLOST	VTX_X_PCLKDETLOST	–	–
0x4C	0xA5	REG12[7:0]*	PT2_PIN_SEL_A[1:0]		PT2_PIN_SEL_B[1:0]		PT1_PIN_SEL_A[1:0]		PT1_PIN_SEL_B[1:0]	
GMSL A										
0x50	0x66	TX0[7:0]*	RSVD[1:0]		RSVD	RSVD	–	RSVD	TX_FEC_EN	–
0x51	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x52	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x53	0x54	TX3[7:0]*	RSVD[1:0]		TX_FEC_ACTIVE	RSVD[1:0]		TIMEOUT[2:0]		
0x54	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
0x55	0x34	RX1[7:0]	RSVD	RSVD	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD
0x57	0x00	RX3[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0x58	0x41	GPIOA[7:0]*	GPIO_RX_FAST_BIDIR_EN	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
0x59	0x98	GPIOB[7:0]*	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
GMSL B										
0x60	0x66	TX0[7:0]*	RSVD[1:0]		RSVD	RSVD	–	RSVD	TX_FEC_EN	–
0x61	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x62	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x63	0x54	TX3[7:0]*	RSVD[1:0]		TX_FEC_ACTIVE	RSVD[1:0]		TIMEOUT[2:0]		
0x64	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
0x65	0x34	RX1[7:0]	RSVD	RSVD	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD
0x67	0x00	RX3[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0x68	0x41	GPIOA[7:0]*	GPIO_RX_FAST_BIDIR_EN	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
0x69	0x98	GPIOB[7:0]*	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					

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ADDRESS	RESET	NAME	MSB							LSB
CC A										
0x70	0x23	I2C_0[7:0]*	–	RSVD	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x71	0x52	I2C_1[7:0]*	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x72	0x00	I2C_2[7:0]*	SRC_A[6:0]							–
0x73	0x00	I2C_3[7:0]*	DST_A[6:0]							–
0x74	0x00	I2C_4[7:0]*	SRC_B[6:0]							–
0x75	0x00	I2C_5[7:0]*	DST_B[6:0]							–
0x76	0x18	I2C_6[7:0]*	DIS_REM_CC	–	–	MULTI_REM_MST_DIS	I2C_AUTO_CFG	–	I2C_SRC_CNT[1:0]	
0x78	0x60	UART_0[7:0]*	RSVD[1:0]		RSVD[1:0]		–	–	–	REM_MS_EN
0x79	0x00	PT_0[7:0]*	PT_I2C_SRC_CNT_2[1:0]		PT_I2C_SRC_CNT_1[1:0]		–	–	CC_2_EN	CC_1_EN
0x7B	0x00	PT_2[7:0]	PT_SRC_1[6:0]							–
0x7C	0x00	PT_3[7:0]	PT_DST_1[6:0]							–
0x7D	0x00	PT_4[7:0]	PT_SRC_2[6:0]							–
0x7E	0x00	PT_5[7:0]	PT_DST_2[6:0]							–
0x7F	0x00	I2C_8[7:0]*	–	–	MULTI_REM_MST_EN_2	MULTI_REM_MST_EN_1	DIS_REM_I2C_DES_3	DIS_REM_I2C_DES_2	DIS_REM_I2C_DES_1	DIS_REM_I2C_DES_0
CC B										
0x80	0x23	I2C_0[7:0]*	–	RSVD	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x81	0x52	I2C_1[7:0]*	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x82	0x00	I2C_2[7:0]*	SRC_A[6:0]							–
0x83	0x00	I2C_3[7:0]*	DST_A[6:0]							–
0x84	0x00	I2C_4[7:0]*	SRC_B[6:0]							–
0x85	0x00	I2C_5[7:0]*	DST_B[6:0]							–
0x86	0x18	I2C_6[7:0]*	DIS_REM_CC	–	–	MULTI_REM_MST_DIS	I2C_AUTO_CFG	–	I2C_SRC_CNT[1:0]	
0x88	0x60	UART_0[7:0]*	RSVD[1:0]		RSVD[1:0]		–	–	–	REM_MS_EN
0x89	0x00	PT_0[7:0]*	PT_I2C_SRC_CNT_2[1:0]		PT_I2C_SRC_CNT_1[1:0]		–	–	CC_2_EN	CC_1_EN
0x8B	0x00	PT_2[7:0]	PT_SRC_1[6:0]							–
0x8C	0x00	PT_3[7:0]	PT_DST_1[6:0]							–
0x8D	0x00	PT_4[7:0]	PT_SRC_2[6:0]							–
0x8E	0x00	PT_5[7:0]	PT_DST_2[6:0]							–
0x8F	0x00	I2C_8[7:0]*	–	–	MULTI_REM_MST_EN_2	MULTI_REM_MST_EN_1	DIS_REM_I2C_DES_3	DIS_REM_I2C_DES_2	DIS_REM_I2C_DES_1	DIS_REM_I2C_DES_0

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ADDRESS	RESET	NAME	MSB							LSB
CC_CMN										
0x90	0x42	CC_0[7:0]*	UART_ARB_TO[1:0]		EN_I2C_LOOPBACK	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
0x96	0x2B	CC_6[7:0]*	BITLEN_MAN_CFG_1	DIS_PAR_1	SLV_SH_PT_1[1:0]		I2CSEL_1	SLV_TO_PT_1[2:0]		
0x97	0x52	CC_7[7:0]*	RSVD	MST_BT_PT_1[2:0]			RSVD	MST_TO_PT_1[2:0]		
0x98	0x2B	CC_8[7:0]*	BITLEN_MAN_CFG_2	DIS_PAR_2	SLV_SH_PT_2[1:0]		I2CSEL_2	SLV_TO_PT_2[2:0]		
0x99	0x52	CC_9[7:0]*	RSVD	MST_BT_PT_2[2:0]			RSVD	MST_TO_PT_2[2:0]		
0x9A	0x01	CC_10[7:0]*	–	I2C_OVER_AUX_TO_CC_PINS_EN	–	–	I2C_OVER_AUX_TO_GMSL_CC_EN	PT2_PINS_TO_GMSL_CC_EN	PT1_PINS_TO_GMSL_CC_EN	CC_PINS_TO_GMSL_CC_EN
0x9B	0x02	CC_11[7:0]*	–	I2C_OVER_AUX_TO_PT1_PINS_EN	EN_PT1_LOOPBACK	PT1_LOOPBACK_TO_GMSL_CC_EN	I2C_OVER_AUX_TO_GMSL_PT1_EN	PT2_PINS_TO_GMSL_PT1_EN	PT1_PINS_TO_GMSL_PT1_EN	CC_PINS_TO_GMSL_PT1_EN
0x9C	0x04	CC_12[7:0]*	–	I2C_OVER_AUX_TO_PT2_PINS_EN	EN_PT2_LOOPBACK	PT2_LOOPBACK_TO_GMSL_CC_EN	I2C_OVER_AUX_TO_GMSL_PT2_EN	PT2_PINS_TO_GMSL_PT2_EN	PT1_PINS_TO_GMSL_PT2_EN	CC_PINS_TO_GMSL_PT2_EN
0x9D	0x88	CC_13[7:0]*	AHCC_AUTO_CFG_B	–	AHCC_SRC_CNT_B[1:0]		AHCC_AUTO_CFG_A	–	AHCC_SRC_CNT_A[1:0]	
0x9E	0x13	CC_14[7:0]*	–	–	–	PT1_READ_EN	–	–	PT_I2C_AUTO_CFG_2	PT_I2C_AUTO_CFG_1
0x9F	0x55	CC_15[7:0]*	PASS_KEY[7:0]							
CFGV VIDEO_X										
0xA0	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA1	0xB0	TX1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xA3	0x00	TX3[7:0]*	–	–	–	–	–	–	TX_STR_SEL[1:0]	
CFGV VIDEO_Y										
0xA4	0x30	TX0[7:0]*	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xA5	0xB0	TX1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xA7	0x01	TX3[7:0]*	–	–	–	–	–	–	TX_STR_SEL[1:0]	
CFGS AUDIO_X										
0xB0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xB1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xB2	0x00	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xB3	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xB4	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	DIS_DBL_ACK_RETX	–	ARQ_EN
0xB5	0x22	ARQ1[7:0]*	LINK_SEL	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xB6	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGS AUDIO_Y										
0xB8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xB9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xBA	0x01	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xBB	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							
0xBC	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	DIS_DBL_ACK_RETX	–	ARQ_EN
0xBD	0xA2	ARQ1[7:0]*	LINK_SEL	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xBE	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGI INFOFR										
0xC0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xC1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xC2	0x00	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xC3	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							
CFGS SPI										
0xC8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xC9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xCA	0x00	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xCB	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							
0xCC	0x91	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	DIS_DBL_ACK_RETX	–	ARQ_EN
0xCD	0x22	ARQ1[7:0]*	LINK_SEL	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xCE	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL CC										
0xD0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xD1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xD2	0x00	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xD3	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xD4	0x93	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	DIS_DBL_ACK_RETX_A	ARQ_EN_B	ARQ_EN_A
0xD5	0x22	ARQ1[7:0]*	–	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xD6	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
0xD7	0x00	ARQ3[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGL GPIO										
0xD8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xD9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xDA	0x00	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xDB	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							
0xDC	0x93	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	DIS_DBL_ACK_RETX_A	ARQ_EN_B	ARQ_EN_A
0xDD	0x22	ARQ1[7:0]*	–	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xDE	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
0xDF	0x00	ARQ3[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGL AHDCP										
0xE0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xE1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xE2	0x00	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xE3	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							
0xE4	0x93	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	DIS_DBL_ACK_RETX_A	ARQ_EN_B	ARQ_EN_A
0xE5	0x22	ARQ1[7:0]*	–	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xE6	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
0xE7	0x00	ARQ3[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGL IIC_X										
0xE8	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xE9	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xEA	0x00	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xEB	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xEC	0x93	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	DIS_DBL_ACK_RETX_A	ARQ_EN_B	ARQ_EN_A
0xED	0x22	ARQ1[7:0]*	–	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xEE	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
0xEF	0x00	ARQ3[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGL IIC_Y										
0xF0	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xF1	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xF2	0x00	TR2[7:0]*	–	–	–	–	–	TX_SRC_ID[2:0]		
0xF3	0xFF	TR3[7:0]*	RX_SRC_SEL[7:0]							
0xF4	0x93	ARQ0[7:0]*	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	DIS_DBL_ACK_RETX_A	ARQ_EN_B	ARQ_EN_A
0xF5	0x22	ARQ1[7:0]*	–	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xF6	0x00	ARQ2[7:0]	MAX_RT_ERR_A	RT_CNT_A[6:0]						
0xF7	0x00	ARQ3[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGH SGMII										
0xF8	0x30	TX0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0xF9	0xB0	TX1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0xFA	0x00	TX2[7:0]*	LINK_SEL	–	–	–	–	–	–	–
0xFB	0x00	TX3[7:0]*	–	–	–	–	–	–	–	–
VID_TX X										
0x100	0x61	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	VID_LINK_SEL[1:0]		VID_TX_EN
0x101	0x58	VIDEO_TX1[7:0]*	RSVD[1:0]		BPP[5:0]					
0x102	0x0A	VIDEO_TX2[7:0]*	PCLKDET_A	DRIFT_ERR_A	OVERFLOW_A	FIFO_WARN_A	RSVD	LIM_HEART	RSVD	RSVD
0x106	0x40	VIDEO_TX6[7:0]	RSVD	MASK_VIDEO_DE	RSVD[5:0]					
0x108	0x00	VIDEO_TX8[7:0]	PCLKDET_B	DRIFT_ERR_B	OVERFLOW_B	FIFO_WARN_B	–	–	–	RSVD
VID_TX Y										
0x110	0x61	VIDEO_TX0[7:0]*	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	VID_LINK_SEL[1:0]		VID_TX_EN

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ADDRESS	RESET	NAME	MSB							LSB
0x111	0x58	VIDEO_TX1[7:0]*	RSVD[1:0]		BPP[5:0]					
0x112	0x0A	VIDEO_TX2[7:0]*	PCLKDET_A	DRIFT_ERR_A	OVERFLOW_A	FIFO_WARN_A	RSVD	LIM_HEART	RSVD	RSVD
0x116	0x40	VIDEO_TX6[7:0]	RSVD	MASK_VIDEO_DE	RSVD[5:0]					
0x118	0x00	VIDEO_TX8[7:0]	PCLKDET_B	DRIFT_ERR_B	OVERFLOW_B	FIFO_WARN_B	–	–	–	RSVD
AUD_TX X										
0x140	0x00	AUDIO_TX0[7:0]*	–	–	–	–	INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
0x141	0x4C	AUDIO_TX1[7:0]*	RSVD[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	AUD_HDCP_SEL[1:0]	
0x145	0x00	AUDIO_TX5[7:0]	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
0x147	0x00	AUDIO_TX7[7:0]	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
0x148	0x40	AUDIO_TX8[7:0]	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
AUD_TX Y										
0x150	0x00	AUDIO_TX0[7:0]*	–	–	–	–	INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
0x151	0x5C	AUDIO_TX1[7:0]*	RSVD[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	AUD_HDCP_SEL[1:0]	
0x155	0x00	AUDIO_TX5[7:0]	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
0x157	0x00	AUDIO_TX7[7:0]	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
0x158	0x40	AUDIO_TX8[7:0]	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
AUD_RX X										
0x160	0x20	AUDIO_RX1[7:0]*	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
0x163	0x00	AUDIO_RX4[7:0]	APRBS_ERR[7:0]							
0x166	0x02	AUDIO_RX7[7:0]*	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
0x168	0x00	AUDIO_RX9[7:0]	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			

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ADDRESS	RESET	NAME	MSB							LSB
AUD_RX Y										
0x180	0x20	AUDIO_RX1[7:0]*	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
0x183	0x00	AUDIO_RX4[7:0]	APRBS_ERR[7:0]							
0x186	0x02	AUDIO_RX7[7:0]*	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
0x188	0x00	AUDIO_RX9[7:0]	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			
SPI										
0x1A0	0x08	SPI_0[7:0]*	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
0x1A1	0x1D	SPI_1[7:0]*	SPI_LOC_N[5:0]						RSVD[1:0]	
0x1A2	0x03	SPI_2[7:0]*	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
0x1A3	0x00	SPI_3[7:0]*	SPIM_SS_DLY_CLKS[7:0]							
0x1A4	0x00	SPI_4[7:0]*	SPIM_SCK_LO_CLKS[7:0]							
0x1A5	0x00	SPI_5[7:0]*	SPIM_SCK_HI_CLKS[7:0]							
0x1A6	0x03	SPI_6[7:0]*	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
0x1A7	0x00	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
0x1A8	0x00	SPI_8[7:0]*	REQ_HOLD_OFF_TO[7:0]							
0x1A9	0x00	SPI_9[7:0]	–	–	–	–	–	–	RSVD	SPIM_SCK_FB_MODE
SGMII_LINK										
0x1B0	0x10	SGMII_LINK_0[7:0]*	SG_TRGT_ID[1:0]		RSVD[1:0]		SG_HALF_DUPLEX	SG_CMD_RST_N	SG_EN	SG_T_IGNR_ID
0x1B1	0xE0	SGMII_LINK_1[7:0]*	SG_LOC_N[5:0]						SG_T_LOC_ID[1:0]	
0x1B2	0x01	SGMII_LINK_2[7:0]*	–	–	–	–	–	–	SG_BASE_PRIO[1:0]	
0x1B3	0x02	SGMII_LINK_3[7:0]*	SG_FRAME_DELAY_H	SG_FRAME_UF	SG_TX_OVRFLW	SG_RX_OVRFLW	SG_DYNAMIC_IFG	SG_EARLY_REQ_EN	SG_INTER_FRM_GAP[1:0]	
0x1B4	0x40	SGMII_LINK_4[7:0]*	SG_FRAME_DELAY_L[7:0]							
0x1B5	0x64	SGMII_LINK_5[7:0]*	MDIO_CLK_DIV[7:0]							
0x1B6	0x00	SGMII_LINK_6[7:0]*	MDIO_BUSY	MDIO_RD_VLD	RSVD	MDIO_PHY_ADRS[4:0]				
0x1B7	0x00	SGMII_LINK_7[7:0]*	MDIO_WRITE	MDIO_START	RMII_READD_PREAMBLE	MDIO_REG_ADRS[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x1B8	0x00	SGMII_LINK_8[7:0]	MDIO_WR_DATA_L[7:0]							
0x1B9	0x00	SGMII_LINK_9[7:0]	MDIO_WR_DATA_H[7:0]							
0x1BA	0x00	SGMII_LINK_10[7:0]	MDIO_RD_DATA_L[7:0]							
0x1BB	0x00	SGMII_LINK_11[7:0]	MDIO_RD_DATA_H[7:0]							
0x1BC	0x40	SGMII_LINK_12[7:0]*	–	MDIO_ALT_DRIVER	RSVD[1:0]		TEST_RMT_LOOPBACK	RSVD	ADD_RXC_DLY	RSVD
0x1BD	0x0E	SGMII_LINK_13[7:0]	–	–	REQ_HOLD_OFF_SGMII[5:0]					
WM										
0x1C0	0x80	WM_0[7:0]	WM_AUTO_SYNC_EN_X	WM_MODE_X[2:0]			–	–	–	WM_EN_X
0x1C2	0x80	WM_2[7:0]	WM_AUTO_SYNC_EN_Y	WM_MODE_Y[2:0]			–	–	–	WM_EN_Y
0x1DE	0x00	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x1DF	0x00	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
GPIOC 0										
0x200	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x201	0x80	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x202	0x40	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x203	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
0x204	0x00	GPIO_E[7:0]*	–	GPIO_RX_EN2_B	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x205	0x00	GPIO_F[7:0]*	–	GPIO_RX_EN3_B	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x206	0x00	GPIO_G[7:0]*	–	GPIO_RX_EN4_B	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 1										
0x208	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x209	0x81	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x20A	0x41	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x20B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
0x20C	0x00	GPIO_E[7:0]*	–	GPIO_RX_EN2_B	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x20D	0x00	GPIO_F[7:0]*	–	GPIO_RX_EN3_B	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x20E	0x00	GPIO_G[7:0]*	–	GPIO_RX_EN4_B	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIO 2										
0x210	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x211	0x82	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x212	0x42	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x213	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 3										
0x218	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x219	0x83	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		–	GPIO_TX_ID[4:0]				
0x21A	0x03	GPIO_C[7:0]*	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
0x21B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 4										
0x220	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x221	0x84	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x222	0x64	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x223	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 5										
0x228	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x229	0x85	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x22A	0x65	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x22B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A

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ADDRESS	RESET	NAME	MSB							LSB
GPIO 6										
0x230	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x231	0x26	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x232	0x66	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x233	0x00	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 7										
0x238	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x239	0x87	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		–	GPIO_TX_ID[4:0]				
0x23A	0x07	GPIO_C[7:0]*	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
0x23B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 8										
0x240	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x241	0x88	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x242	0x68	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x243	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 9										
0x248	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x249	0x89	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x24A	0x69	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x24B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 10										
0x250	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x251	0x2A	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x252	0x6A	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x253	0x00	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 11										
0x258	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS

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ADDRESS	RESET	NAME	MSB							LSB
0x259	0x8B	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x25A	0x4B	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x25B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 12										
0x260	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x261	0x8C	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x262	0x4C	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x263	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 13										
0x268	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x269	0x8D	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x26A	0x4D	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x26B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 14										
0x270	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x271	0x8E	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x272	0x4E	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x273	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 15										
0x278	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x279	0x8F	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x27A	0x4F	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x27B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 16										
0x280	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x281	0x30	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x282	0x50	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				

PRELIMINARY

Release to TPK under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x283	0x00	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 17										
0x288	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x289	0x91	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x28A	0x51	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x28B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 18										
0x290	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x291	0x92	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x292	0x52	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x293	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 19										
0x298	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x299	0x93	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x29A	0x73	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x29B	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIO 20										
0x2A0	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2A1	0x94	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2A2	0x74	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2A3	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
GPIOC 21										
0x2A8	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2A9	0x95	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2AA	0x55	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2AB	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A

PRELIMINARY

Release to TPI Under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x2AC	0x00	GPIO_E[7:0]*	–	GPIO_RX_EN2_B	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2AD	0x00	GPIO_F[7:0]*	–	GPIO_RX_EN3_B	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2AE	0x00	GPIO_G[7:0]*	–	GPIO_RX_EN4_B	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 22										
0x2B0	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2B1	0x96	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B2	0x56	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2B3	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
0x2B4	0x00	GPIO_E[7:0]*	–	GPIO_RX_EN2_B	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2B5	0x00	GPIO_F[7:0]*	–	GPIO_RX_EN3_B	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2B6	0x00	GPIO_G[7:0]*	–	GPIO_RX_EN4_B	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 23										
0x2B8	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2B9	0x97	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2BA	0x57	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2BB	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
0x2BC	0x00	GPIO_E[7:0]*	–	GPIO_RX_EN2_B	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2BD	0x00	GPIO_F[7:0]*	–	GPIO_RX_EN3_B	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2BE	0x00	GPIO_G[7:0]*	–	GPIO_RX_EN4_B	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 24										
0x2C0	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2C1	0x98	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				

PRELIMINARY

Released to TPK Under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x2C2	0x58	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2C3	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
0x2C4	0x00	GPIO_E[7:0]*	–	GPIO_RX_EN2_B	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2C5	0x00	GPIO_F[7:0]*	–	GPIO_RX_EN3_B	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2C6	0x00	GPIO_G[7:0]*	–	GPIO_RX_EN4_B	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIOC 25										
0x2C8	0x91	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
0x2C9	0x99	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CA	0x59	GPIO_C[7:0]*	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
0x2CB	0x20	GPIO_D[7:0]*	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
0x2CC	0x00	GPIO_E[7:0]*	–	GPIO_RX_EN2_B	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
0x2CD	0x00	GPIO_F[7:0]*	–	GPIO_RX_EN3_B	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
0x2CE	0x00	GPIO_G[7:0]*	–	GPIO_RX_EN4_B	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
GPIO_RECVED										
0x2F8	0xFF	GPIO_RX_0[7:0]*	GPIO_RECVED_A_7	GPIO_RECVED_A_6	GPIO_RECVED_A_5	GPIO_RECVED_A_4	GPIO_RECVED_A_3	GPIO_RECVED_A_2	GPIO_RECVED_A_1	GPIO_RECVED_A_0
0x2F9	0xFF	GPIO_RX_1[7:0]*	GPIO_RECVED_A_15	GPIO_RECVED_A_14	GPIO_RECVED_A_13	GPIO_RECVED_A_12	GPIO_RECVED_A_11	GPIO_RECVED_A_10	GPIO_RECVED_A_9	GPIO_RECVED_A_8
0x2FA	0xFF	GPIO_RX_2[7:0]*	GPIO_RECVED_A_23	GPIO_RECVED_A_22	GPIO_RECVED_A_21	GPIO_RECVED_A_20	GPIO_RECVED_A_19	GPIO_RECVED_A_18	GPIO_RECVED_A_17	GPIO_RECVED_A_16
0x2FB	0xDF	GPIO_RX_3[7:0]*	GPIO_RECVED_A_31	GPIO_RECVED_A_30	GPIO_RECVED_A_29	GPIO_RECVED_A_28	GPIO_RECVED_A_27	GPIO_RECVED_A_26	GPIO_RECVED_A_25	GPIO_RECVED_A_24
0x2FC	0xFF	GPIO_RX_4[7:0]*	GPIO_RECVED_B_7	GPIO_RECVED_B_6	GPIO_RECVED_B_5	GPIO_RECVED_B_4	GPIO_RECVED_B_3	GPIO_RECVED_B_2	GPIO_RECVED_B_1	GPIO_RECVED_B_0
0x2FD	0xFF	GPIO_RX_5[7:0]*	GPIO_RECVED_B_15	GPIO_RECVED_B_14	GPIO_RECVED_B_13	GPIO_RECVED_B_12	GPIO_RECVED_B_11	GPIO_RECVED_B_10	GPIO_RECVED_B_9	GPIO_RECVED_B_8

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Release to TPK Under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x2FE	0xFF	GPIO_RX_6[7:0]*	GPIO_RECVED_B_23	GPIO_RECVED_B_22	GPIO_RECVED_B_21	GPIO_RECVED_B_20	GPIO_RECVED_B_19	GPIO_RECVED_B_18	GPIO_RECVED_B_17	GPIO_RECVED_B_16
0x2FF	0xDF	GPIO_RX_7[7:0]*	GPIO_RECVED_B_31	GPIO_RECVED_B_30	GPIO_RECVED_B_29	GPIO_RECVED_B_28	GPIO_RECVED_B_27	GPIO_RECVED_B_26	GPIO_RECVED_B_25	GPIO_RECVED_B_24
MISC										
0x304	0xDC	UART_PT_0[7:0]*	RSVD[7:0]							
0x305	0x05	UART_PT_1[7:0]*	DIS_TEMP_WAKE_PERM_A	–	RSVD[5:0]					
0x306	0xDC	UART_PT_2[7:0]*	RSVD[7:0]							
0x307	0x05	UART_PT_3[7:0]*	DIS_TEMP_WAKE_PERM_B	–	RSVD[5:0]					
0x310	0x05	MISC_0[7:0]*	–	–	–	–	RSVD[1:0]		OV_LEVEL[1:0]	
0x311	0x55	MISC_1[7:0]*	RSVD[1:0]		OV1P8_LEVEL[1:0]		RSVD[1:0]		OVREG_LEVEL[1:0]	
0x312	0x00	MISC_2[7:0]	VDDIO_OV	VDD1P8_OV	RSVD	VDD_OV	RSVD[3:0]			
0x313	0x00	MISC_3[7:0]	–	–	–	–	–	–	–	LFLT_STKY_INT
0x320	0x00	CC_CRC[7:0]*	–	–	–	–	–	–	CC_MSGCNTR_EN	CC_CRC_EN
0x321	0x00	HDCP2_ID_0[7:0]*	–	–	–	HDCP2_INT_ID_OVERRIDE_X[4:0]				
0x322	0x00	HDCP2_ID_1[7:0]*	–	–	–	HDCP2_INT_ID_OVERRIDE_Y[4:0]				
0x327	0x50	MISC_8[7:0]*	RSVD[1:0]		OVDDIO_LEVEL[1:0]		–	–	–	–
0x328	0x00	MISC_9[7:0]*	–	–	–	–	–	–	RSVD	VDDOV_LOGIC
0x329	0x04	PIN_SEL[7:0]*	MS_PIN_SEL	RCLKOUT_PIN_SEL	SPI_PIN_SEL	MDIO_PIN_SEL	AUDIO_RX_PIN_SEL_Y[1:0]		AUDIO_RX_PIN_SEL_X[1:0]	
0x331	0x00	MISC_OTP2[7:0]	OTP_RELEASED	RSVD[6:0]						
CMU										
0x3E6	0x00	CMU6[7:0]	SET_TEMP1P0[1:0]		RSVD	RSVD[4:0]				
VTX X										
0x400	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x401	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x402	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x403	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x404	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x405	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x406	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x407	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x408	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x409	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x40A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x40B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x40C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x40D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x40E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x40F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x410	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x411	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x412	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x413	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x414	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x415	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x416	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x417	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x418	0x00	RSVD_0[7:0]	–	–	–	–	–	–	–	–
0x419	0x00	RSVD_1[7:0]	–	–	–	–	–	–	–	–
0x41A	0x00	RSVD_2[7:0]	–	–	–	–	–	–	–	–
0x41B	0x00	RSVD_3[7:0]	–	–	–	–	–	–	–	–
0x41C	0x00	RSVD_4[7:0]	–	–	–	–	–	–	–	–
0x41D	0x00	RSVD_5[7:0]	–	–	–	–	–	–	–	–

PRELIMINARY

Released to TDK Under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x41F	0x00	HS_VS[7:0]	–	DE_DET	VS_DET	HS_DET	–	–	VS_POL	HS_POL
0x420	0x07	VTX0[7:0]	GEN_VS	GEN_HS	GEN_DE	VID_ACTIVE	PCLKDET_VTX	VS_TRIG	VTG_MODE[1:0]	
0x421	0x00	VTX1[7:0]*	USE_DE_AS_HS	USE_HS_AS_DE	FORCE_VS_LOW	FORCE_HS_LOW	FORCE_DE_LOW	VS_INVERT	HS_INVERT	DE_INVERT
0x422	0x00	VTX2[7:0]	V_VS_DLY_2[7:0]							
0x423	0x00	VTX3[7:0]	V_VS_DLY_1[7:0]							
0x424	0x00	VTX4[7:0]	V_VS_DLY_0[7:0]							
0x425	0x00	VTX5[7:0]	V_VS_HIGH_2[7:0]							
0x426	0x00	VTX6[7:0]	V_VS_HIGH_1[7:0]							
0x427	0x00	VTX7[7:0]	V_VS_HIGH_0[7:0]							
0x428	0x00	VTX8[7:0]	V_VS_LOW_2[7:0]							
0x429	0x00	VTX9[7:0]	V_VS_LOW_1[7:0]							
0x42A	0x00	VTX10[7:0]	V_VS_LOW_0[7:0]							
0x42B	0x00	VTX11[7:0]	V2H_2[7:0]							
0x42C	0x00	VTX12[7:0]	V2H_1[7:0]							
0x42D	0x00	VTX13[7:0]	V2H_0[7:0]							
0x42E	0x00	VTX14[7:0]	V_HS_HIGH_1[7:0]							
0x42F	0x00	VTX15[7:0]	V_HS_HIGH_0[7:0]							
0x430	0x00	VTX16[7:0]	V_HS_LOW_1[7:0]							
0x431	0x00	VTX17[7:0]	V_HS_LOW_0[7:0]							
0x432	0x00	VTX18[7:0]	V_HS_CNT_1[7:0]							
0x433	0x00	VTX19[7:0]	V_HS_CNT_0[7:0]							
0x434	0x00	VTX20[7:0]	V2D_2[7:0]							
0x435	0x00	VTX21[7:0]	V2D_1[7:0]							
0x436	0x00	VTX22[7:0]	V2D_0[7:0]							
0x437	0x00	VTX23[7:0]	V_DE_HIGH_1[7:0]							
0x438	0x00	VTX24[7:0]	V_DE_HIGH_0[7:0]							
0x439	0x00	VTX25[7:0]	V_DE_LOW_1[7:0]							
0x43A	0x00	VTX26[7:0]	V_DE_LOW_0[7:0]							
0x43B	0x00	VTX27[7:0]	V_DE_CNT_1[7:0]							
0x43C	0x00	VTX28[7:0]	V_DE_CNT_0[7:0]							
0x43D	0x00	VTX29[7:0]	VID_PRBS_EN	–	–	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
0x43E	0x04	VTX30[7:0]	GRAD_INC[7:0]							
0x43F	0x00	VTX31[7:0]	CHKR_A_L[7:0]							
0x440	0x00	VTX32[7:0]	CHKR_A_M[7:0]							
0x441	0x00	VTX33[7:0]	CHKR_A_H[7:0]							
0x442	0x00	VTX34[7:0]	CHKR_B_L[7:0]							
0x443	0x00	VTX35[7:0]	CHKR_B_M[7:0]							
0x444	0x00	VTX36[7:0]	CHKR_B_H[7:0]							
0x445	0x00	VTX37[7:0]	CHKR_RPT_A[7:0]							
0x446	0x00	VTX38[7:0]	CHKR_RPT_B[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x447	0x00	VTX39[7:0]	CHKR_ALT[7:0]							
0x448	0x05	VTX40[7:0]*	DIS_COLOR_CROSSBAR	–	–	–	VA_BEFORE_WM	AUTO_COLOR_DEPTH	COLOR_DEPTH[1:0]	
0x449	0x09	VTX41[7:0]*	–	–	–	VID_ASIL_INJ_ERR	VID_ASIL_CRC_ERR_OEN	VID_ASIL_CRC_ERR	VID_ASIL_CRC_CHK_EARLY	VID_ASIL_CRC_CHK_EN
PXL_CAPT X										
0x450	0x00	RSVD_0[7:0]*	–	–	–	–	–	–	–	–
0x451	0x00	RSVD_1[7:0]*	–	–	–	–	–	–	–	–
0x452	0x00	RSVD_2[7:0]*	–	–	–	–	–	–	–	–
0x458	0x00	PXL_CAPT_0[7:0]	PIXEL_CAPT_H_HIGH[7:0]							
0x459	0x00	PXL_CAPT_1[7:0]	PIXEL_CAPT_H_LOW[7:0]							
0x45A	0x00	PXL_CAPT_2[7:0]	PIXEL_CAPT_V_HIGH[7:0]							
0x45B	0x00	PXL_CAPT_3[7:0]	PIXEL_CAPT_V_LOW[7:0]							
0x45C	0x00	PXL_CAPT_4[7:0]	PIXEL_CAPT_7_0[7:0]							
0x45D	0x00	PXL_CAPT_5[7:0]	PIXEL_CAPT_15_8[7:0]							
0x45E	0x00	PXL_CAPT_6[7:0]	PIXEL_CAPT_23_16[7:0]							
VIDEO_AUTH X										
0x460	0x05	AUTH0[7:0]	FRAME_CYCLE_MODULO_H[1:0]		LOCAL_CHALLENGE_MAX[1:0]		RSVD	AUTH_GLOBAL_PERIODIC	AUTH_GLOBAL_TRIG	AUTH_EN
0x461	0x04	AUTH1[7:0]	FRAME_CYCLE_MODULO_L[7:0]							
0x462	0x00	XMINL0a[7:0]	XMIN0a_LSB[7:0]							
0x463	0x00	XMINH0a[7:0]	–	–	XMIN0a_MSB[5:0]					
0x464	0x01	XMAXL0a[7:0]	XMAX0a_LSB[7:0]							
0x465	0x00	XMAXH0a[7:0]	–	–	XMAX0a_MSB[5:0]					
0x466	0x00	XMINL1a[7:0]	XMIN1a_LSB[7:0]							
0x467	0x00	XMINH1a[7:0]	–	–	XMIN1a_MSB[5:0]					
0x468	0x00	XMAXL1a[7:0]	XMAX1a_LSB[7:0]							
0x469	0x00	XMAXH1a[7:0]	–	–	XMAX1a_MSB[5:0]					
0x46A	0x00	XMINL2a[7:0]	XMIN2a_LSB[7:0]							
0x46B	0x00	XMINH2a[7:0]	–	–	XMIN2a_MSB[5:0]					
0x46C	0x00	XMAXL2a[7:0]	XMAX2a_LSB[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x46D	0x00	XMAXH2a[7:0]	–	–	XMAX2a_MSB[5:0]					
0x46E	0x00	XMINL3a[7:0]	XMIN3a_LSB[7:0]							
0x46F	0x00	XMINH3a[7:0]	–	–	XMIN3a_MSB[5:0]					
0x470	0x00	XMAXL3a[7:0]	XMAX3a_LSB[7:0]							
0x471	0x00	XMAXH3a[7:0]	–	–	XMAX3a_MSB[5:0]					
0x472	0x00	XMINL0b[7:0]	XMIN0b_LSB[7:0]							
0x473	0x00	XMINH0b[7:0]	–	–	XMIN0b_MSB[5:0]					
0x474	0x01	XMAXL0b[7:0]	XMAX0b_LSB[7:0]							
0x475	0x00	XMAXH0b[7:0]	–	–	XMAX0b_MSB[5:0]					
0x476	0x00	XMINL1b[7:0]	XMIN1b_LSB[7:0]							
0x477	0x00	XMINH1b[7:0]	–	–	XMIN1b_MSB[5:0]					
0x478	0x00	XMAXL1b[7:0]	XMAX1b_LSB[7:0]							
0x479	0x00	XMAXH1b[7:0]	–	–	XMAX1b_MSB[5:0]					
0x47A	0x00	XMINL2b[7:0]	XMIN2b_LSB[7:0]							
0x47B	0x00	XMINH2b[7:0]	–	–	XMIN2b_MSB[5:0]					
0x47C	0x00	XMAXL2b[7:0]	XMAX2b_LSB[7:0]							
0x47D	0x00	XMAXH2b[7:0]	–	–	XMAX2b_MSB[5:0]					
0x47E	0x00	XMINL3b[7:0]	XMIN3b_LSB[7:0]							
0x47F	0x00	XMINH3b[7:0]	–	–	XMIN3b_MSB[5:0]					
0x480	0x00	XMAXL3b[7:0]	XMAX3b_LSB[7:0]							
0x481	0x00	XMAXH3b[7:0]	–	–	XMAX3b_MSB[5:0]					
0x482	0x00	YMINL0a[7:0]	YMIN0a_LSB[7:0]							
0x483	0x00	YMINH0a[7:0]	–	–	YMIN0a_MSB[5:0]					
0x484	0x01	YMAXL0a[7:0]	YMAX0a_LSB[7:0]							
0x485	0x00	YMAXH0a[7:0]	FRAME0a_MSB[1:0]		YMAX0a_MSB[5:0]					
0x486	0x01	FRAME0a[7:0]	FRAME0a_LSB[7:0]							
0x487	0x00	YMINL1a[7:0]	YMIN1a_LSB[7:0]							
0x488	0x00	YMINH1a[7:0]	–	–	YMIN1a_MSB[5:0]					
0x489	0x00	YMAXL1a[7:0]	YMAX1a_LSB[7:0]							
0x48A	0x00	YMAXH1a[7:0]	FRAME1a_MSB[1:0]		YMAX1a_MSB[5:0]					

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ADDRESS	RESET	NAME	MSB							LSB
0x48B	0x00	FRAME1a[7:0]	FRAME1a_LSB[7:0]							
0x48C	0x00	YMINL2a[7:0]	YMIN2a_LSB[7:0]							
0x48D	0x00	YMINH2a[7:0]	–	–	YMIN2a_MSB[5:0]					
0x48E	0x00	YMAXL2a[7:0]	YMAX2a_LSB[7:0]							
0x48F	0x00	YMAXH2a[7:0]	FRAME2a_MSB[1:0]		YMAX2a_MSB[5:0]					
0x490	0x00	FRAME2a[7:0]	FRAME2a_LSB[7:0]							
0x491	0x00	YMINL3a[7:0]	YMIN3a_LSB[7:0]							
0x492	0x00	YMINH3a[7:0]	–	–	YMIN3a_MSB[5:0]					
0x493	0x00	YMAXL3a[7:0]	YMAX3a_LSB[7:0]							
0x494	0x00	YMAXH3a[7:0]	FRAME3a_MSB[1:0]		YMAX3a_MSB[5:0]					
0x495	0x00	FRAME3a[7:0]	FRAME3a_LSB[7:0]							
0x496	0x00	YMINL0b[7:0]	YMIN0b_LSB[7:0]							
0x497	0x00	YMINH0b[7:0]	–	–	YMIN0b_MSB[5:0]					
0x498	0x01	YMAXL0b[7:0]	YMAX0b_LSB[7:0]							
0x499	0x00	YMAXH0b[7:0]	FRAME0b_MSB[1:0]		YMAX0b_MSB[5:0]					
0x49A	0x01	FRAME0b[7:0]	FRAME0b_LSB[7:0]							
0x49B	0x00	YMINL1b[7:0]	YMIN1b_LSB[7:0]							
0x49C	0x00	YMINH1b[7:0]	–	–	YMIN1b_MSB[5:0]					
0x49D	0x00	YMAXL1b[7:0]	YMAX1b_LSB[7:0]							
0x49E	0x00	YMAXH1b[7:0]	FRAME1b_MSB[1:0]		YMAX1b_MSB[5:0]					
0x49F	0x00	FRAME1b[7:0]	FRAME1b_LSB[7:0]							
0x4A0	0x00	YMINL2b[7:0]	YMIN2b_LSB[7:0]							
0x4A1	0x00	YMINH2b[7:0]	–	–	YMIN2b_MSB[5:0]					
0x4A2	0x00	YMAXL2b[7:0]	YMAX2b_LSB[7:0]							
0x4A3	0x00	YMAXH2b[7:0]	FRAME2b_MSB[1:0]		YMAX2b_MSB[5:0]					
0x4A4	0x00	FRAME2b[7:0]	FRAME2b_LSB[7:0]							
0x4A5	0x00	YMINL3b[7:0]	YMIN3b_LSB[7:0]							
0x4A6	0x00	YMINH3b[7:0]	–	–	YMIN3b_MSB[5:0]					
0x4A7	0x00	YMAXL3b[7:0]	YMAX3b_LSB[7:0]							
0x4A8	0x00	YMAXH3b[7:0]	FRAME3b_MSB[1:0]		YMAX3b_MSB[5:0]					

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0x4A9	0x00	FRAME3b[7:0]	FRAME3b_LSB[7:0]							
0x4AA	0x00	out1[7:0]	FRAME_CNT_MSB	VA_SWAP_DIS	VA_DONE_FLAG	VA_DONE_OEN	–	A_OR_B	AUTH_DONE_B	AUTH_DONE_A
0x4AB	0x00	out1a[7:0]	FRAME_CNT_LSB[7:0]							
0x4AC	0x00	out2[7:0]	CRC_OUT_A_0[7:0]							
0x4AD	0x00	out3[7:0]	CRC_OUT_A_1[7:0]							
0x4AE	0x00	out4[7:0]	CRC_OUT_A_2[7:0]							
0x4AF	0x00	out5[7:0]	CRC_OUT_A_3[7:0]							
0x4B0	0x00	out6[7:0]	CRC_OUT_B_0[7:0]							
0x4B1	0x00	out7[7:0]	CRC_OUT_B_1[7:0]							
0x4B2	0x00	out8[7:0]	CRC_OUT_B_2[7:0]							
0x4B3	0x00	out9[7:0]	CRC_OUT_B_3[7:0]							
0x4B4	0x00	outa[7:0]	FULL_FRAME_CRC_0[7:0]							
0x4B5	0x00	outb[7:0]	FULL_FRAME_CRC_1[7:0]							
0x4B6	0x00	outc[7:0]	FULL_FRAME_CRC_2[7:0]							
0x4B7	0x00	outd[7:0]	FULL_FRAME_CRC_3[7:0]							
ASYM X										
0x4C0	0x00	ASYM0[7:0]	M_L[7:0]							
0x4C1	0x00	ASYM1[7:0]	M_M[7:0]							
0x4C2	0x00	ASYM2[7:0]	M_H[7:0]							
0x4C3	0x00	ASYM3[7:0]	N_L[7:0]							
0x4C4	0x00	ASYM4[7:0]	N_M[7:0]							
0x4C5	0x00	ASYM5[7:0]	N_H[7:0]							
0x4C6	0x00	ASYM6[7:0]	X_OFF_WR_L[7:0]							
0x4C7	0x00	ASYM7[7:0]	X_OFF_WR_H[7:0]							
0x4C8	0x00	ASYM8[7:0]	X_MAX_L[7:0]							
0x4C9	0x00	ASYM9[7:0]	X_MAX_H[7:0]							
0x4CA	0x00	ASYM10[7:0]	Y_MAX_L[7:0]							
0x4CB	0x00	ASYM11[7:0]	Y_MAX_H[7:0]							
0x4CC	0x80	ASYM12[7:0]	RSVD[7:0]							
0x4CD	0x14	ASYM13[7:0]*	LUT_TEMPLATE_SEL[3:0]				RSVD	RSVD	RSVD	RSVD
0x4CE	0x3F	ASYM14[7:0]*	RSVD	RSVD	RSVD	RSVD	ASYM_WR_B_MUX	RSVD	RSVD	RSVD
0x4D1	0xF0	ASYM17[7:0]*	RSVD[2:0]			RSVD	RSVD	RSVD	ASYM_UNDERFLOW	ASYM_OVERFLOW
0x4D8	0x00	AR0[7:0]	VS_DLY_0[7:0]							
0x4D9	0x00	AR1[7:0]	VS_DLY_1[7:0]							
0x4DA	0x00	AR2[7:0]	VS_DLY_2[7:0]							
0x4DB	0x00	AR3[7:0]	VS_HIGH_0[7:0]							
0x4DC	0x00	AR4[7:0]	VS_HIGH_1[7:0]							

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0x4DD	0x00	AR5[7:0]	VS_HIGH_2[7:0]							
0x4DE	0x00	AR6[7:0]	VS_LOW_0[7:0]							
0x4DF	0x00	AR7[7:0]	VS_LOW_1[7:0]							
0x4E0	0x00	AR8[7:0]	VS_LOW_2[7:0]							
0x4E1	0x00	AR9[7:0]	HS_DLY_0[7:0]							
0x4E2	0x00	AR10[7:0]	HS_DLY_1[7:0]							
0x4E3	0x00	AR11[7:0]	HS_DLY_2[7:0]							
0x4E4	0x00	AR12[7:0]	HS_HIGH_0[7:0]							
0x4E5	0x00	AR13[7:0]	HS_HIGH_1[7:0]							
0x4E6	0x00	AR14[7:0]	HS_LOW_0[7:0]							
0x4E7	0x00	AR15[7:0]	HS_LOW_1[7:0]							
0x4E8	0x00	AR16[7:0]	HS_CNT_0[7:0]							
0x4E9	0x00	AR17[7:0]	HS_CNT_1[7:0]							
0x4EA	0x00	AR18[7:0]	HS_LLOW_0[7:0]							
0x4EB	0x00	AR19[7:0]	HS_LLOW_1[7:0]							
0x4EC	0x00	AR20[7:0]	HS_LLOW_2[7:0]							
0x4ED	0x00	AR21[7:0]	DE_DLY_0[7:0]							
0x4EE	0x00	AR22[7:0]	DE_DLY_1[7:0]							
0x4EF	0x00	AR23[7:0]	DE_DLY_2[7:0]							
0x4F0	0x00	AR24[7:0]	DE_HIGH_0[7:0]							
0x4F1	0x00	AR25[7:0]	DE_HIGH_1[7:0]							
0x4F2	0x00	AR26[7:0]	DE_LOW_0[7:0]							
0x4F3	0x00	AR27[7:0]	DE_LOW_1[7:0]							
0x4F4	0x00	AR28[7:0]	DE_CNT_0[7:0]							
0x4F5	0x00	AR29[7:0]	DE_CNT_1[7:0]							
0x4F6	0x00	AR30[7:0]	DE_LLOW_0[7:0]							
0x4F7	0x00	AR31[7:0]	DE_LLOW_1[7:0]							
0x4F8	0x00	AR32[7:0]	DE_LLOW_2[7:0]							
0x4F9	0x00	AR33[7:0]	VS_INV	HS_INV	DE_INV	–	–	–	–	–
VTX Y										
0x500	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x501	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x502	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x503	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x504	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x505	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x506	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				

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0x507	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x508	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x509	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x50A	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x50B	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x50C	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x50D	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x50E	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x50F	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x510	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x511	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x512	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x513	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x514	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x515	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x516	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x517	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x518	0x00	RSVD_0[7:0]	–	–	–	–	–	–	–	–
0x519	0x00	RSVD_1[7:0]	–	–	–	–	–	–	–	–
0x51A	0x00	RSVD_2[7:0]	–	–	–	–	–	–	–	–
0x51B	0x00	RSVD_3[7:0]	–	–	–	–	–	–	–	–
0x51C	0x00	RSVD_4[7:0]	–	–	–	–	–	–	–	–
0x51D	0x00	RSVD_5[7:0]	–	–	–	–	–	–	–	–
0x51F	0x00	HS_VS[7:0]	–	DE_DET	VS_DET	HS_DET	–	–	VS_POL	HS_POL
0x520	0x07	VTX0[7:0]	GEN_VS	GEN_HS	GEN_DE	VID_ACTIVE	PCLKDET_VTX	VS_TRIG	VTG_MODE[1:0]	
0x521	0x00	VTX1[7:0]*	USE_DE_AS_HS	USE_HS_AS_DE	FORCE_VS_LOW	FORCE_HS_LOW	FORCE_DE_LOW	VS_INVERT	HS_INVERT	DE_INVERT
0x522	0x00	VTX2[7:0]	V_VS_DLY_2[7:0]							
0x523	0x00	VTX3[7:0]	V_VS_DLY_1[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x524	0x00	VTX4[7:0]	V_VS_DLY_0[7:0]							
0x525	0x00	VTX5[7:0]	V_VS_HIGH_2[7:0]							
0x526	0x00	VTX6[7:0]	V_VS_HIGH_1[7:0]							
0x527	0x00	VTX7[7:0]	V_VS_HIGH_0[7:0]							
0x528	0x00	VTX8[7:0]	V_VS_LOW_2[7:0]							
0x529	0x00	VTX9[7:0]	V_VS_LOW_1[7:0]							
0x52A	0x00	VTX10[7:0]	V_VS_LOW_0[7:0]							
0x52B	0x00	VTX11[7:0]	V2H_2[7:0]							
0x52C	0x00	VTX12[7:0]	V2H_1[7:0]							
0x52D	0x00	VTX13[7:0]	V2H_0[7:0]							
0x52E	0x00	VTX14[7:0]	V_HS_HIGH_1[7:0]							
0x52F	0x00	VTX15[7:0]	V_HS_HIGH_0[7:0]							
0x530	0x00	VTX16[7:0]	V_HS_LOW_1[7:0]							
0x531	0x00	VTX17[7:0]	V_HS_LOW_0[7:0]							
0x532	0x00	VTX18[7:0]	V_HS_CNT_1[7:0]							
0x533	0x00	VTX19[7:0]	V_HS_CNT_0[7:0]							
0x534	0x00	VTX20[7:0]	V2D_2[7:0]							
0x535	0x00	VTX21[7:0]	V2D_1[7:0]							
0x536	0x00	VTX22[7:0]	V2D_0[7:0]							
0x537	0x00	VTX23[7:0]	V_DE_HIGH_1[7:0]							
0x538	0x00	VTX24[7:0]	V_DE_HIGH_0[7:0]							
0x539	0x00	VTX25[7:0]	V_DE_LOW_1[7:0]							
0x53A	0x00	VTX26[7:0]	V_DE_LOW_0[7:0]							
0x53B	0x00	VTX27[7:0]	V_DE_CNT_1[7:0]							
0x53C	0x00	VTX28[7:0]	V_DE_CNT_0[7:0]							
0x53D	0x00	VTX29[7:0]	VID_PRBS_EN	–	–	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
0x53E	0x04	VTX30[7:0]	GRAD_INC[7:0]							
0x53F	0x00	VTX31[7:0]	CHKR_A_L[7:0]							
0x540	0x00	VTX32[7:0]	CHKR_A_M[7:0]							
0x541	0x00	VTX33[7:0]	CHKR_A_H[7:0]							
0x542	0x00	VTX34[7:0]	CHKR_B_L[7:0]							
0x543	0x00	VTX35[7:0]	CHKR_B_M[7:0]							
0x544	0x00	VTX36[7:0]	CHKR_B_H[7:0]							
0x545	0x00	VTX37[7:0]	CHKR_RPT_A[7:0]							
0x546	0x00	VTX38[7:0]	CHKR_RPT_B[7:0]							
0x547	0x00	VTX39[7:0]	CHKR_ALT[7:0]							
0x548	0x05	VTX40[7:0]*	DIS_COLOR_CROSSBAR	–	–	–	VA_BEFORE_WM	AUTO_COLOR_DEPTH	COLOR_DEPTH[1:0]	
0x549	0x09	VTX41[7:0]*	–	–	–	VID_ASIL_INJ_ERR	VID_ASIL_CRC_ERR_OEN	VID_ASIL_CRC_ERR	VID_ASIL_CRC_CHK_EARLY	VID_ASIL_CRC_CHK_EN

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ADDRESS	RESET	NAME	MSB							LSB
PXL_CAPT Y										
0x550	0x00	RSVD_0[7:0]*	–	–	–	–	–	–	–	–
0x551	0x00	RSVD_1[7:0]*	–	–	–	–	–	–	–	–
0x552	0x00	RSVD_2[7:0]*	–	–	–	–	–	–	–	–
0x558	0x00	PXL_CAPT_0[7:0]	PIXEL_CAPT_H_HIGH[7:0]							
0x559	0x00	PXL_CAPT_1[7:0]	PIXEL_CAPT_H_LOW[7:0]							
0x55A	0x00	PXL_CAPT_2[7:0]	PIXEL_CAPT_V_HIGH[7:0]							
0x55B	0x00	PXL_CAPT_3[7:0]	PIXEL_CAPT_V_LOW[7:0]							
0x55C	0x00	PXL_CAPT_4[7:0]	PIXEL_CAPT_7_0[7:0]							
0x55D	0x00	PXL_CAPT_5[7:0]	PIXEL_CAPT_15_8[7:0]							
0x55E	0x00	PXL_CAPT_6[7:0]	PIXEL_CAPT_23_16[7:0]							
VIDEO_AUTH Y										
0x560	0x05	AUTH0[7:0]	FRAME_CYCLE_MODULO_H[1:0]		LOCAL_CHALLENGE_MAX[1:0]		RSVD	AUTH_GLOBAL_PERIODIC	AUTH_GLOBAL_TRIG	AUTH_EN
0x561	0x04	AUTH1[7:0]	FRAME_CYCLE_MODULO_L[7:0]							
0x562	0x00	XMINL0a[7:0]	XMIN0a_LSB[7:0]							
0x563	0x00	XMINH0a[7:0]	–	–	XMIN0a_MSB[5:0]					
0x564	0x01	XMAXL0a[7:0]	XMAX0a_LSB[7:0]							
0x565	0x00	XMAXH0a[7:0]	–	–	XMAX0a_MSB[5:0]					
0x566	0x00	XMINL1a[7:0]	XMIN1a_LSB[7:0]							
0x567	0x00	XMINH1a[7:0]	–	–	XMIN1a_MSB[5:0]					
0x568	0x00	XMAXL1a[7:0]	XMAX1a_LSB[7:0]							
0x569	0x00	XMAXH1a[7:0]	–	–	XMAX1a_MSB[5:0]					
0x56A	0x00	XMINL2a[7:0]	XMIN2a_LSB[7:0]							
0x56B	0x00	XMINH2a[7:0]	–	–	XMIN2a_MSB[5:0]					
0x56C	0x00	XMAXL2a[7:0]	XMAX2a_LSB[7:0]							
0x56D	0x00	XMAXH2a[7:0]	–	–	XMAX2a_MSB[5:0]					
0x56E	0x00	XMINL3a[7:0]	XMIN3a_LSB[7:0]							
0x56F	0x00	XMINH3a[7:0]	–	–	XMIN3a_MSB[5:0]					
0x570	0x00	XMAXL3a[7:0]	XMAX3a_LSB[7:0]							
0x571	0x00	XMAXH3a[7:0]	–	–	XMAX3a_MSB[5:0]					

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ADDRESS	RESET	NAME	MSB							LSB
0x572	0x00	XMINL0b[7:0]	XMIN0b_LSB[7:0]							
0x573	0x00	XMINH0b[7:0]	–	–	XMIN0b_MSB[5:0]					
0x574	0x01	XMAXL0b[7:0]	XMAX0b_LSB[7:0]							
0x575	0x00	XMAXH0b[7:0]	–	–	XMAX0b_MSB[5:0]					
0x576	0x00	XMINL1b[7:0]	XMIN1b_LSB[7:0]							
0x577	0x00	XMINH1b[7:0]	–	–	XMIN1b_MSB[5:0]					
0x578	0x00	XMAXL1b[7:0]	XMAX1b_LSB[7:0]							
0x579	0x00	XMAXH1b[7:0]	–	–	XMAX1b_MSB[5:0]					
0x57A	0x00	XMINL2b[7:0]	XMIN2b_LSB[7:0]							
0x57B	0x00	XMINH2b[7:0]	–	–	XMIN2b_MSB[5:0]					
0x57C	0x00	XMAXL2b[7:0]	XMAX2b_LSB[7:0]							
0x57D	0x00	XMAXH2b[7:0]	–	–	XMAX2b_MSB[5:0]					
0x57E	0x00	XMINL3b[7:0]	XMIN3b_LSB[7:0]							
0x57F	0x00	XMINH3b[7:0]	–	–	XMIN3b_MSB[5:0]					
0x580	0x00	XMAXL3b[7:0]	XMAX3b_LSB[7:0]							
0x581	0x00	XMAXH3b[7:0]	–	–	XMAX3b_MSB[5:0]					
0x582	0x00	YMINL0a[7:0]	YMIN0a_LSB[7:0]							
0x583	0x00	YMINH0a[7:0]	–	–	YMIN0a_MSB[5:0]					
0x584	0x01	YMAXL0a[7:0]	YMAX0a_LSB[7:0]							
0x585	0x00	YMAXH0a[7:0]	FRAME0a_MSB[1:0]		YMAX0a_MSB[5:0]					
0x586	0x01	FRAME0a[7:0]	FRAME0a_LSB[7:0]							
0x587	0x00	YMINL1a[7:0]	YMIN1a_LSB[7:0]							
0x588	0x00	YMINH1a[7:0]	–	–	YMIN1a_MSB[5:0]					
0x589	0x00	YMAXL1a[7:0]	YMAX1a_LSB[7:0]							
0x58A	0x00	YMAXH1a[7:0]	FRAME1a_MSB[1:0]		YMAX1a_MSB[5:0]					
0x58B	0x00	FRAME1a[7:0]	FRAME1a_LSB[7:0]							
0x58C	0x00	YMINL2a[7:0]	YMIN2a_LSB[7:0]							
0x58D	0x00	YMINH2a[7:0]	–	–	YMIN2a_MSB[5:0]					
0x58E	0x00	YMAXL2a[7:0]	YMAX2a_LSB[7:0]							
0x58F	0x00	YMAXH2a[7:0]	FRAME2a_MSB[1:0]		YMAX2a_MSB[5:0]					

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ADDRESS	RESET	NAME	MSB							LSB
0x590	0x00	FRAME2a[7:0]	FRAME2a_LSB[7:0]							
0x591	0x00	YMINL3a[7:0]	YMIN3a_LSB[7:0]							
0x592	0x00	YMINH3a[7:0]	–	–	YMIN3a_MSB[5:0]					
0x593	0x00	YMAXL3a[7:0]	YMAX3a_LSB[7:0]							
0x594	0x00	YMAXH3a[7:0]	FRAME3a_MSB[1:0]		YMAX3a_MSB[5:0]					
0x595	0x00	FRAME3a[7:0]	FRAME3a_LSB[7:0]							
0x596	0x00	YMINL0b[7:0]	YMIN0b_LSB[7:0]							
0x597	0x00	YMINH0b[7:0]	–	–	YMIN0b_MSB[5:0]					
0x598	0x01	YMAXL0b[7:0]	YMAX0b_LSB[7:0]							
0x599	0x00	YMAXH0b[7:0]	FRAME0b_MSB[1:0]		YMAX0b_MSB[5:0]					
0x59A	0x01	FRAME0b[7:0]	FRAME0b_LSB[7:0]							
0x59B	0x00	YMINL1b[7:0]	YMIN1b_LSB[7:0]							
0x59C	0x00	YMINH1b[7:0]	–	–	YMIN1b_MSB[5:0]					
0x59D	0x00	YMAXL1b[7:0]	YMAX1b_LSB[7:0]							
0x59E	0x00	YMAXH1b[7:0]	FRAME1b_MSB[1:0]		YMAX1b_MSB[5:0]					
0x59F	0x00	FRAME1b[7:0]	FRAME1b_LSB[7:0]							
0x5A0	0x00	YMINL2b[7:0]	YMIN2b_LSB[7:0]							
0x5A1	0x00	YMINH2b[7:0]	–	–	YMIN2b_MSB[5:0]					
0x5A2	0x00	YMAXL2b[7:0]	YMAX2b_LSB[7:0]							
0x5A3	0x00	YMAXH2b[7:0]	FRAME2b_MSB[1:0]		YMAX2b_MSB[5:0]					
0x5A4	0x00	FRAME2b[7:0]	FRAME2b_LSB[7:0]							
0x5A5	0x00	YMINL3b[7:0]	YMIN3b_LSB[7:0]							
0x5A6	0x00	YMINH3b[7:0]	–	–	YMIN3b_MSB[5:0]					
0x5A7	0x00	YMAXL3b[7:0]	YMAX3b_LSB[7:0]							
0x5A8	0x00	YMAXH3b[7:0]	FRAME3b_MSB[1:0]		YMAX3b_MSB[5:0]					
0x5A9	0x00	FRAME3b[7:0]	FRAME3b_LSB[7:0]							
0x5AA	0x00	out1[7:0]	FRAME_CNT_MSB	VA_SWAP_DIS	VA_DONE_FLAG	VA_DONE_OEN	–	A_OR_B	AUTH_DONE_B	AUTH_DONE_A
0x5AB	0x00	out1a[7:0]	FRAME_CNT_LSB[7:0]							
0x5AC	0x00	out2[7:0]	CRC_OUT_A_0[7:0]							
0x5AD	0x00	out3[7:0]	CRC_OUT_A_1[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x5AE	0x00	out4[7:0]	CRC_OUT_A_2[7:0]							
0x5AF	0x00	out5[7:0]	CRC_OUT_A_3[7:0]							
0x5B0	0x00	out6[7:0]	CRC_OUT_B_0[7:0]							
0x5B1	0x00	out7[7:0]	CRC_OUT_B_1[7:0]							
0x5B2	0x00	out8[7:0]	CRC_OUT_B_2[7:0]							
0x5B3	0x00	out9[7:0]	CRC_OUT_B_3[7:0]							
0x5B4	0x00	outa[7:0]	FULL_FRAME_CRC_0[7:0]							
0x5B5	0x00	outb[7:0]	FULL_FRAME_CRC_1[7:0]							
0x5B6	0x00	outc[7:0]	FULL_FRAME_CRC_2[7:0]							
0x5B7	0x00	outd[7:0]	FULL_FRAME_CRC_3[7:0]							
ASYM Y										
0x5C0	0x00	ASYM0[7:0]	M_L[7:0]							
0x5C1	0x00	ASYM1[7:0]	M_M[7:0]							
0x5C2	0x00	ASYM2[7:0]	M_H[7:0]							
0x5C3	0x00	ASYM3[7:0]	N_L[7:0]							
0x5C4	0x00	ASYM4[7:0]	N_M[7:0]							
0x5C5	0x00	ASYM5[7:0]	N_H[7:0]							
0x5C6	0x00	ASYM6[7:0]	X_OFF_WR_L[7:0]							
0x5C7	0x00	ASYM7[7:0]	X_OFF_WR_H[7:0]							
0x5C8	0x00	ASYM8[7:0]	X_MAX_L[7:0]							
0x5C9	0x00	ASYM9[7:0]	X_MAX_H[7:0]							
0x5CA	0x00	ASYM10[7:0]	Y_MAX_L[7:0]							
0x5CB	0x00	ASYM11[7:0]	Y_MAX_H[7:0]							
0x5CC	0x80	ASYM12[7:0]	RSVD[7:0]							
0x5CD	0x14	ASYM13[7:0]*	LUT_TEMPLATE_SEL[3:0]				RSVD	RSVD	RSVD	RSVD
0x5CE	0x3F	ASYM14[7:0]*	RSVD	RSVD	RSVD	RSVD	ASYM_WR_B_MUX	RSVD	RSVD	RSVD
0x5D1	0xF0	ASYM17[7:0]*	RSVD[2:0]			RSVD	RSVD	RSVD	ASYM_UNDERFLOW	ASYM_OVERFLOW
0x5D8	0x00	AR0[7:0]	VS_DLY_0[7:0]							
0x5D9	0x00	AR1[7:0]	VS_DLY_1[7:0]							
0x5DA	0x00	AR2[7:0]	VS_DLY_2[7:0]							
0x5DB	0x00	AR3[7:0]	VS_HIGH_0[7:0]							
0x5DC	0x00	AR4[7:0]	VS_HIGH_1[7:0]							
0x5DD	0x00	AR5[7:0]	VS_HIGH_2[7:0]							
0x5DE	0x00	AR6[7:0]	VS_LOW_0[7:0]							
0x5DF	0x00	AR7[7:0]	VS_LOW_1[7:0]							
0x5E0	0x00	AR8[7:0]	VS_LOW_2[7:0]							
0x5E1	0x00	AR9[7:0]	HS_DLY_0[7:0]							
0x5E2	0x00	AR10[7:0]	HS_DLY_1[7:0]							
0x5E3	0x00	AR11[7:0]	HS_DLY_2[7:0]							
0x5E4	0x00	AR12[7:0]	HS_HIGH_0[7:0]							

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0x5E5	0x00	AR13[7:0]	HS_HIGH_1[7:0]							
0x5E6	0x00	AR14[7:0]	HS_LOW_0[7:0]							
0x5E7	0x00	AR15[7:0]	HS_LOW_1[7:0]							
0x5E8	0x00	AR16[7:0]	HS_CNT_0[7:0]							
0x5E9	0x00	AR17[7:0]	HS_CNT_1[7:0]							
0x5EA	0x00	AR18[7:0]	HS_LLOW_0[7:0]							
0x5EB	0x00	AR19[7:0]	HS_LLOW_1[7:0]							
0x5EC	0x00	AR20[7:0]	HS_LLOW_2[7:0]							
0x5ED	0x00	AR21[7:0]	DE_DLY_0[7:0]							
0x5EE	0x00	AR22[7:0]	DE_DLY_1[7:0]							
0x5EF	0x00	AR23[7:0]	DE_DLY_2[7:0]							
0x5F0	0x00	AR24[7:0]	DE_HIGH_0[7:0]							
0x5F1	0x00	AR25[7:0]	DE_HIGH_1[7:0]							
0x5F2	0x00	AR26[7:0]	DE_LOW_0[7:0]							
0x5F3	0x00	AR27[7:0]	DE_LOW_1[7:0]							
0x5F4	0x00	AR28[7:0]	DE_CNT_0[7:0]							
0x5F5	0x00	AR29[7:0]	DE_CNT_1[7:0]							
0x5F6	0x00	AR30[7:0]	DE_LLOW_0[7:0]							
0x5F7	0x00	AR31[7:0]	DE_LLOW_1[7:0]							
0x5F8	0x00	AR32[7:0]	DE_LLOW_2[7:0]							
0x5F9	0x00	AR33[7:0]	VS_INV	HS_INV	DE_INV	–	–	–	–	–
SHA256_A X										
0xE00	0x00	BR23[7:0]	SHA_A_1[7:0]							
0xE01	0x00	BR23H[7:0]	SHA_A_2[7:0]							
0xE02	0x00	BR24[7:0]	SHA_A_3[7:0]							
0xE03	0x00	BR24H[7:0]	SHA_A_4[7:0]							
0xE04	0x00	BR25[7:0]	SHA_A_5[7:0]							
0xE05	0x00	BR25H[7:0]	SHA_A_6[7:0]							
0xE06	0x00	BR26[7:0]	SHA_A_7[7:0]							
0xE07	0x00	BR26H[7:0]	SHA_A_8[7:0]							
0xE08	0x00	BR27[7:0]	SHA_A_9[7:0]							
0xE09	0x00	BR27H[7:0]	SHA_A_10[7:0]							
0xE0A	0x00	BR28[7:0]	SHA_A_11[7:0]							
0xE0B	0x00	BR28H[7:0]	SHA_A_12[7:0]							
0xE0C	0x00	BR29[7:0]	SHA_A_13[7:0]							
0xE0D	0x00	BR29H[7:0]	SHA_A_14[7:0]							
0xE0E	0x00	BR30[7:0]	SHA_A_15[7:0]							
0xE0F	0x00	BR30H[7:0]	SHA_A_16[7:0]							
0xE10	0x00	BR31[7:0]	SHA_A_17[7:0]							
0xE11	0x00	BR31H[7:0]	SHA_A_18[7:0]							
0xE12	0x00	BR32[7:0]	SHA_A_19[7:0]							
0xE13	0x00	BR32H[7:0]	SHA_A_20[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xE14	0x00	BR33[7:0]	SHA_A_21[7:0]							
0xE15	0x00	BR33H[7:0]	SHA_A_22[7:0]							
0xE16	0x00	BR34[7:0]	SHA_A_23[7:0]							
0xE17	0x00	BR34H[7:0]	SHA_A_24[7:0]							
0xE18	0x00	BR35[7:0]	SHA_A_25[7:0]							
0xE19	0x00	BR35H[7:0]	SHA_A_26[7:0]							
0xE1A	0x00	BR36[7:0]	SHA_A_27[7:0]							
0xE1B	0x00	BR36H[7:0]	SHA_A_28[7:0]							
0xE1C	0x00	BR37[7:0]	SHA_A_29[7:0]							
0xE1D	0x00	BR37H[7:0]	SHA_A_30[7:0]							
0xE1E	0x00	BR38[7:0]	SHA_A_31[7:0]							
0xE1F	0x00	BR38H[7:0]	SHA_A_32[7:0]							
SHA256_B X										
0xE20	0x00	BR23[7:0]	SHA_B_1[7:0]							
0xE21	0x00	BR23H[7:0]	SHA_B_2[7:0]							
0xE22	0x00	BR24[7:0]	SHA_B_3[7:0]							
0xE23	0x00	BR24H[7:0]	SHA_B_4[7:0]							
0xE24	0x00	BR25[7:0]	SHA_B_5[7:0]							
0xE25	0x00	BR25H[7:0]	SHA_B_6[7:0]							
0xE26	0x00	BR26[7:0]	SHA_B_7[7:0]							
0xE27	0x00	BR26H[7:0]	SHA_B_8[7:0]							
0xE28	0x00	BR27[7:0]	SHA_B_9[7:0]							
0xE29	0x00	BR27H[7:0]	SHA_B_10[7:0]							
0xE2A	0x00	BR28[7:0]	SHA_B_11[7:0]							
0xE2B	0x00	BR28H[7:0]	SHA_B_12[7:0]							
0xE2C	0x00	BR29[7:0]	SHA_B_13[7:0]							
0xE2D	0x00	BR29H[7:0]	SHA_B_14[7:0]							
0xE2E	0x00	BR30[7:0]	SHA_B_15[7:0]							
0xE2F	0x00	BR30H[7:0]	SHA_B_16[7:0]							
0xE30	0x00	BR31[7:0]	SHA_B_17[7:0]							
0xE31	0x00	BR31H[7:0]	SHA_B_18[7:0]							
0xE32	0x00	BR32[7:0]	SHA_B_19[7:0]							
0xE33	0x00	BR32H[7:0]	SHA_B_20[7:0]							
0xE34	0x00	BR33[7:0]	SHA_B_21[7:0]							
0xE35	0x00	BR33H[7:0]	SHA_B_22[7:0]							
0xE36	0x00	BR34[7:0]	SHA_B_23[7:0]							
0xE37	0x00	BR34H[7:0]	SHA_B_24[7:0]							
0xE38	0x00	BR35[7:0]	SHA_B_25[7:0]							
0xE39	0x00	BR35H[7:0]	SHA_B_26[7:0]							
0xE3A	0x00	BR36[7:0]	SHA_B_27[7:0]							
0xE3B	0x00	BR36H[7:0]	SHA_B_28[7:0]							
0xE3C	0x00	BR37[7:0]	SHA_B_29[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xE3D	0x00	BR37H[7:0]	SHA_B_30[7:0]							
0xE3E	0x00	BR38[7:0]	SHA_B_31[7:0]							
0xE3F	0x00	BR38H[7:0]	SHA_B_32[7:0]							
SHA256_A Y										
0xE40	0x00	BR23[7:0]	SHA_A_1[7:0]							
0xE41	0x00	BR23H[7:0]	SHA_A_2[7:0]							
0xE42	0x00	BR24[7:0]	SHA_A_3[7:0]							
0xE43	0x00	BR24H[7:0]	SHA_A_4[7:0]							
0xE44	0x00	BR25[7:0]	SHA_A_5[7:0]							
0xE45	0x00	BR25H[7:0]	SHA_A_6[7:0]							
0xE46	0x00	BR26[7:0]	SHA_A_7[7:0]							
0xE47	0x00	BR26H[7:0]	SHA_A_8[7:0]							
0xE48	0x00	BR27[7:0]	SHA_A_9[7:0]							
0xE49	0x00	BR27H[7:0]	SHA_A_10[7:0]							
0xE4A	0x00	BR28[7:0]	SHA_A_11[7:0]							
0xE4B	0x00	BR28H[7:0]	SHA_A_12[7:0]							
0xE4C	0x00	BR29[7:0]	SHA_A_13[7:0]							
0xE4D	0x00	BR29H[7:0]	SHA_A_14[7:0]							
0xE4E	0x00	BR30[7:0]	SHA_A_15[7:0]							
0xE4F	0x00	BR30H[7:0]	SHA_A_16[7:0]							
0xE50	0x00	BR31[7:0]	SHA_A_17[7:0]							
0xE51	0x00	BR31H[7:0]	SHA_A_18[7:0]							
0xE52	0x00	BR32[7:0]	SHA_A_19[7:0]							
0xE53	0x00	BR32H[7:0]	SHA_A_20[7:0]							
0xE54	0x00	BR33[7:0]	SHA_A_21[7:0]							
0xE55	0x00	BR33H[7:0]	SHA_A_22[7:0]							
0xE56	0x00	BR34[7:0]	SHA_A_23[7:0]							
0xE57	0x00	BR34H[7:0]	SHA_A_24[7:0]							
0xE58	0x00	BR35[7:0]	SHA_A_25[7:0]							
0xE59	0x00	BR35H[7:0]	SHA_A_26[7:0]							
0xE5A	0x00	BR36[7:0]	SHA_A_27[7:0]							
0xE5B	0x00	BR36H[7:0]	SHA_A_28[7:0]							
0xE5C	0x00	BR37[7:0]	SHA_A_29[7:0]							
0xE5D	0x00	BR37H[7:0]	SHA_A_30[7:0]							
0xE5E	0x00	BR38[7:0]	SHA_A_31[7:0]							
0xE5F	0x00	BR38H[7:0]	SHA_A_32[7:0]							
SHA256_B Y										
0xE60	0x00	BR23[7:0]	SHA_B_1[7:0]							
0xE61	0x00	BR23H[7:0]	SHA_B_2[7:0]							
0xE62	0x00	BR24[7:0]	SHA_B_3[7:0]							
0xE63	0x00	BR24H[7:0]	SHA_B_4[7:0]							
0xE64	0x00	BR25[7:0]	SHA_B_5[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0xE65	0x00	BR25H[7:0]	SHA_B_6[7:0]							
0xE66	0x00	BR26[7:0]	SHA_B_7[7:0]							
0xE67	0x00	BR26H[7:0]	SHA_B_8[7:0]							
0xE68	0x00	BR27[7:0]	SHA_B_9[7:0]							
0xE69	0x00	BR27H[7:0]	SHA_B_10[7:0]							
0xE6A	0x00	BR28[7:0]	SHA_B_11[7:0]							
0xE6B	0x00	BR28H[7:0]	SHA_B_12[7:0]							
0xE6C	0x00	BR29[7:0]	SHA_B_13[7:0]							
0xE6D	0x00	BR29H[7:0]	SHA_B_14[7:0]							
0xE6E	0x00	BR30[7:0]	SHA_B_15[7:0]							
0xE6F	0x00	BR30H[7:0]	SHA_B_16[7:0]							
0xE70	0x00	BR31[7:0]	SHA_B_17[7:0]							
0xE71	0x00	BR31H[7:0]	SHA_B_18[7:0]							
0xE72	0x00	BR32[7:0]	SHA_B_19[7:0]							
0xE73	0x00	BR32H[7:0]	SHA_B_20[7:0]							
0xE74	0x00	BR33[7:0]	SHA_B_21[7:0]							
0xE75	0x00	BR33H[7:0]	SHA_B_22[7:0]							
0xE76	0x00	BR34[7:0]	SHA_B_23[7:0]							
0xE77	0x00	BR34H[7:0]	SHA_B_24[7:0]							
0xE78	0x00	BR35[7:0]	SHA_B_25[7:0]							
0xE79	0x00	BR35H[7:0]	SHA_B_26[7:0]							
0xE7A	0x00	BR36[7:0]	SHA_B_27[7:0]							
0xE7B	0x00	BR36H[7:0]	SHA_B_28[7:0]							
0xE7C	0x00	BR37[7:0]	SHA_B_29[7:0]							
0xE7D	0x00	BR37H[7:0]	SHA_B_30[7:0]							
0xE7E	0x00	BR38[7:0]	SHA_B_31[7:0]							
0xE7F	0x00	BR38H[7:0]	SHA_B_32[7:0]							
SPI_CC_WR										
0x1300	0x00	SPI_CC_WR_[7:0]	–	–	–	–	–	–	–	–
SPI_CC_RD										
0x1380	0x00	SPI_CC_RD_[7:0]	–	–	–	–	–	–	–	–
RLMS_DCIO A										
0x1404	0x4B	RLMS4[7:0]*	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1405	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1406	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1407	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1464	0x90	RLMS64[7:0]*	RSVD[3:0]				–	RSVD	TxSSCMode[1:0]	

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ADDRESS	RESET	NAME	MSB							LSB
0x1470	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x1471	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1472	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x1473	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1474	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x1475	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x1476	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
RLMS_DCIO B										
0x1504	0x4B	RLMS4[7:0]*	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1505	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1506	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1507	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1564	0x90	RLMS64[7:0]*	RSVD[3:0]				–	RSVD	TxSSCMode[1:0]	
0x1570	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x1571	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1572	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x1573	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1574	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x1575	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x1576	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
HDCP_TX HX										
0x1676	0x80	HDCP_DES0[7:0]	AH_DES_REG_OFFSET_L[7:0]							
0x1677	0x16	HDCP_DES1[7:0]	AH_DES_REG_OFFSET_H[7:0]							
0x1678	0x00	HDCP_AS0[7:0]	ASEED_0[7:0]							
0x1679	0x00	HDCP_AS1[7:0]	ASEED_1[7:0]							
0x167A	0x00	HDCP_AS2[7:0]	ASEED_2[7:0]							
0x167B	0x00	HDCP_AS3[7:0]	ASEED_3[7:0]							
0x167C	0x00	HDCP_AS4[7:0]	ASEED_4[7:0]							
0x1680	0x00	HDCP_TX0[7:0]	GMSL_BKSV_0[7:0]							
0x1681	0x00	HDCP_TX1[7:0]	GMSL_BKSV_1[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x1682	0x00	HDCP_TX2[7:0]	GMSL_BKSV_2[7:0]							
0x1683	0x00	HDCP_TX3[7:0]	GMSL_BKSV_3[7:0]							
0x1684	0x00	HDCP_TX4[7:0]	GMSL_BKSV_4[7:0]							
0x1685	0xFF	HDCP_TX5[7:0]	RIP_0[7:0]							
0x1686	0xFF	HDCP_TX6[7:0]	RIP_1[7:0]							
0x1687	0xFF	HDCP_TX7[7:0]	PJP[7:0]							
0x1688	0x00	HDCP_TX8[7:0]	AN_0[7:0]							
0x1689	0x00	HDCP_TX9[7:0]	AN_1[7:0]							
0x168A	0x00	HDCP_TXA[7:0]	AN_2[7:0]							
0x168B	0x00	HDCP_TXB[7:0]	AN_3[7:0]							
0x168C	0x00	HDCP_TXC[7:0]	AN_4[7:0]							
0x168D	0x00	HDCP_TXD[7:0]	AN_5[7:0]							
0x168E	0x00	HDCP_TXE[7:0]	AN_6[7:0]							
0x168F	0x00	HDCP_TXF[7:0]	AN_7[7:0]							
0x1690	0x00	HDCP_TX10[7:0]	AKSV_0[7:0]							
0x1691	0x00	HDCP_TX11[7:0]	AKSV_1[7:0]							
0x1692	0x00	HDCP_TX12[7:0]	AKSV_2[7:0]							
0x1693	0x00	HDCP_TX13[7:0]	AKSV_3[7:0]							
0x1694	0x00	HDCP_TX14[7:0]	AKSV_4[7:0]							
0x1695	0x00	HDCP_TX15[7:0]	–	EN_INT_COMP	–	–	HDCP_RESET	START_AUTH	VSYNC_DET	ENC_EN
0x1696	0x01	HDCP_TX16[7:0]	–	–	–	PJF_MATCH	V_MATCHED	PJ_MATCHED	RI_MATCHED	INVALID_BKSV
0x1697	0x00	HDCP_TX17[7:0]	RSVD[6:0]							HDCP_REPEATER
0x1698	0x00	HDCP_TX18[7:0]	RSVD[7:0]							
0x1699	0x00	HDCP_TX19[7:0]	RSVD[1:0]		–	–	–	–	–	DIS_AUDIO_ENC

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ADDRESS	RESET	NAME	MSB							LSB
0x169A	0xFF	HDCP_TX1A[7:0]	PJFP_0[7:0]							
0x169B	0xFF	HDCP_TX1B[7:0]	PJFP_1[7:0]							
0x169C	0xFF	HDCP_TX1C[7:0]	PJFP_2[7:0]							
0x16A0	0x00	HDCP_TX20[7:0]	VH0_0[7:0]							
0x16A1	0x00	HDCP_TX21[7:0]	VH0_1[7:0]							
0x16A2	0x00	HDCP_TX22[7:0]	VH0_2[7:0]							
0x16A3	0x00	HDCP_TX23[7:0]	VH0_3[7:0]							
0x16A4	0x00	HDCP_TX24[7:0]	VH1_0[7:0]							
0x16A5	0x00	HDCP_TX25[7:0]	VH1_1[7:0]							
0x16A6	0x00	HDCP_TX26[7:0]	VH1_2[7:0]							
0x16A7	0x00	HDCP_TX27[7:0]	VH1_3[7:0]							
0x16A8	0x00	HDCP_TX28[7:0]	VH2_0[7:0]							
0x16A9	0x00	HDCP_TX29[7:0]	VH2_1[7:0]							
0x16AA	0x00	HDCP_TX2A[7:0]	VH2_2[7:0]							
0x16AB	0x00	HDCP_TX2B[7:0]	VH2_3[7:0]							
0x16AC	0x00	HDCP_TX2C[7:0]	VH3_0[7:0]							
0x16AD	0x00	HDCP_TX2D[7:0]	VH3_1[7:0]							
0x16AE	0x00	HDCP_TX2E[7:0]	VH3_2[7:0]							
0x16AF	0x00	HDCP_TX2F[7:0]	VH3_3[7:0]							
0x16B0	0x00	HDCP_TX30[7:0]	VH4_0[7:0]							
0x16B1	0x00	HDCP_TX31[7:0]	VH4_1[7:0]							
0x16B2	0x00	HDCP_TX32[7:0]	VH4_2[7:0]							
0x16B3	0x00	HDCP_TX33[7:0]	VH4_3[7:0]							
0x16B4	0x00	HDCP_TX34[7:0]	HDCP_MAX_DEV_EXCEEDED	HDCP_DEV_CNT[6:0]						

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ADDRESS	RESET	NAME	MSB							LSB
0x16B5	0x00	HDCP_TX35[7:0]	RSVD[3:0]				HDCP_MAX_CASCADE_EXCEEDED	HDCP_DEPTH[2:0]		
0x16B6	0x00	HDCP_TX36[7:0]	HDCP_GPMEM[7:0]							
0x16B7	0xC0	HDCP_TX37[7:0]*	HDCP_PD	FAST_PJ_EN	FORCE_AUDIO	FORCE_VIDEO	AH_MASK_ENCOFF	AH_MASK_NEWDEV	AH_MASK_KSVRDY	AH_MASK_FAIL
0x16B8	0x00	HDCP_TX38[7:0]	–	–	–	–	–	AH_RD_KSVL	AH_DISENC	AH_MODE
0x16B9	0x90	HDCP_TX39[7:0]*	AH_DES_ADDR[6:0]							–
0x16BA	0x00	HDCP_TX3A[7:0]	KSV_LIST_0[7:0]							
0x16BB	0x00	HDCP_TX3B[7:0]	KSV_LIST_1[7:0]							
0x16BC	0x00	HDCP_TX3C[7:0]	KSV_LIST_2[7:0]							
0x16BD	0x00	HDCP_TX3D[7:0]	KSV_LIST_3[7:0]							
0x16BE	0x00	HDCP_TX3E[7:0]	KSV_LIST_4[7:0]							
0x16BF	0x00	HDCP_TX3F[7:0]	KSV_LIST_5[7:0]							
0x16C0	0x00	HDCP_TX40[7:0]	KSV_LIST_6[7:0]							
0x16C1	0x00	HDCP_TX41[7:0]	KSV_LIST_7[7:0]							
0x16C2	0x00	HDCP_TX42[7:0]	KSV_LIST_8[7:0]							
0x16C3	0x00	HDCP_TX43[7:0]	KSV_LIST_9[7:0]							
0x16C4	0x00	HDCP_TX44[7:0]	KSV_LIST_10[7:0]							
0x16C5	0x00	HDCP_TX45[7:0]	KSV_LIST_11[7:0]							
0x16C6	0x00	HDCP_TX46[7:0]	KSV_LIST_12[7:0]							
0x16C7	0x00	HDCP_TX47[7:0]	KSV_LIST_13[7:0]							
0x16C8	0x00	HDCP_TX48[7:0]	KSV_LIST_14[7:0]							
0x16C9	0x00	HDCP_TX49[7:0]	KSV_LIST_15[7:0]							
0x16CA	0x00	HDCP_TX4A[7:0]	KSV_LIST_16[7:0]							
0x16CB	0x00	HDCP_TX4B[7:0]	KSV_LIST_17[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x16CC	0x00	HDCP_TX4C[7:0]	KSV_LIST_18[7:0]							
0x16CD	0x00	HDCP_TX4D[7:0]	KSV_LIST_19[7:0]							
0x16CE	0x00	HDCP_TX4E[7:0]	KSV_LIST_20[7:0]							
0x16CF	0x00	HDCP_TX4F[7:0]	KSV_LIST_21[7:0]							
0x16D0	0x00	HDCP_TX50[7:0]	KSV_LIST_22[7:0]							
0x16D1	0x00	HDCP_TX51[7:0]	KSV_LIST_23[7:0]							
0x16D2	0x00	HDCP_TX52[7:0]	KSV_LIST_24[7:0]							
0x16D3	0x00	HDCP_TX53[7:0]	KSV_LIST_25[7:0]							
0x16D4	0x00	HDCP_TX54[7:0]	KSV_LIST_26[7:0]							
0x16D5	0x00	HDCP_TX55[7:0]	KSV_LIST_27[7:0]							
0x16D6	0x00	HDCP_TX56[7:0]	KSV_LIST_28[7:0]							
0x16D7	0x00	HDCP_TX57[7:0]	KSV_LIST_29[7:0]							
0x16D8	0x00	HDCP_TX58[7:0]	KSV_LIST_30[7:0]							
0x16D9	0x00	HDCP_TX59[7:0]	KSV_LIST_31[7:0]							
0x16DA	0x00	HDCP_TX5A[7:0]	KSV_LIST_32[7:0]							
0x16DB	0x00	HDCP_TX5B[7:0]	KSV_LIST_33[7:0]							
0x16DC	0x00	HDCP_TX5C[7:0]	KSV_LIST_34[7:0]							
0x16DD	0x00	HDCP_TX5D[7:0]	KSV_LIST_35[7:0]							
0x16DE	0x00	HDCP_TX5E[7:0]	KSV_LIST_36[7:0]							
0x16DF	0x00	HDCP_TX5F[7:0]	KSV_LIST_37[7:0]							
0x16E0	0x00	HDCP_TX60[7:0]	KSV_LIST_38[7:0]							
0x16E1	0x00	HDCP_TX61[7:0]	KSV_LIST_39[7:0]							
0x16E2	0x00	HDCP_TX62[7:0]	KSV_LIST_40[7:0]							
0x16E3	0x00	HDCP_TX63[7:0]	KSV_LIST_41[7:0]							
0x16E4	0x00	HDCP_TX64[7:0]	KSV_LIST_42[7:0]							

PRELIMINARY

Release to TPK Under NDA

Analog Devices Company Confidential
Provided to Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x16E5	0x00	HDCP_TX65[7:0]	KSV_LIST_43[7:0]							
0x16E6	0x00	HDCP_TX66[7:0]	KSV_LIST_44[7:0]							
0x16E7	0x00	HDCP_TX67[7:0]	KSV_LIST_45[7:0]							
0x16E8	0x00	HDCP_TX68[7:0]	KSV_LIST_46[7:0]							
0x16E9	0x00	HDCP_TX69[7:0]	KSV_LIST_47[7:0]							
0x16EA	0x00	HDCP_TX6A[7:0]	KSV_LIST_48[7:0]							
0x16EB	0x00	HDCP_TX6B[7:0]	KSV_LIST_49[7:0]							
0x16EC	0x00	HDCP_TX6C[7:0]	KSV_LIST_50[7:0]							
0x16ED	0x00	HDCP_TX6D[7:0]	KSV_LIST_51[7:0]							
0x16EE	0x00	HDCP_TX6E[7:0]	KSV_LIST_52[7:0]							
0x16EF	0x00	HDCP_TX6F[7:0]	KSV_LIST_53[7:0]							
0x16F0	0x00	HDCP_TX70[7:0]	KSV_LIST_54[7:0]							
0x16F1	0x00	HDCP_TX71[7:0]	KSV_LIST_55[7:0]							
0x16F2	0x00	HDCP_TX72[7:0]	KSV_LIST_56[7:0]							
0x16F3	0x00	HDCP_TX73[7:0]	KSV_LIST_57[7:0]							
0x16F4	0x00	HDCP_TX74[7:0]	KSV_LIST_58[7:0]							
0x16F5	0x00	HDCP_TX75[7:0]	KSV_LIST_59[7:0]							
0x16F6	0x00	HDCP_TX76[7:0]	KSV_LIST_60[7:0]							
0x16F7	0x00	HDCP_TX77[7:0]	KSV_LIST_61[7:0]							
0x16F8	0x00	HDCP_TX78[7:0]	KSV_LIST_62[7:0]							
0x16F9	0x00	HDCP_TX79[7:0]	KSV_LIST_63[7:0]							
0x16FA	0x00	HDCP_TX7A[7:0]	KSV_LIST_64[7:0]							
0x16FB	0x00	HDCP_TX7B[7:0]	KSV_LIST_65[7:0]							
0x16FC	0x00	HDCP_TX7C[7:0]	KSV_LIST_66[7:0]							
0x16FD	0x00	HDCP_TX7D[7:0]	KSV_LIST_67[7:0]							

PRELIMINARY

Release to TPK under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x16FE	0x00	HDCP_TX7E[7:0]	KSV_LIST_68[7:0]							
0x16FF	0x00	HDCP_TX7F[7:0]	KSV_LIST_69[7:0]							
HDCP_TX HY										
0x1776	0x80	HDCP_DES0[7:0]	AH_DES_REG_OFFSET_L[7:0]							
0x1777	0x16	HDCP_DES1[7:0]	AH_DES_REG_OFFSET_H[7:0]							
0x1778	0x00	HDCP_AS0[7:0]	ASEED_0[7:0]							
0x1779	0x00	HDCP_AS1[7:0]	ASEED_1[7:0]							
0x177A	0x00	HDCP_AS2[7:0]	ASEED_2[7:0]							
0x177B	0x00	HDCP_AS3[7:0]	ASEED_3[7:0]							
0x177C	0x00	HDCP_AS4[7:0]	ASEED_4[7:0]							
0x1780	0x00	HDCP_TX0[7:0]	GMSL_BKSV_0[7:0]							
0x1781	0x00	HDCP_TX1[7:0]	GMSL_BKSV_1[7:0]							
0x1782	0x00	HDCP_TX2[7:0]	GMSL_BKSV_2[7:0]							
0x1783	0x00	HDCP_TX3[7:0]	GMSL_BKSV_3[7:0]							
0x1784	0x00	HDCP_TX4[7:0]	GMSL_BKSV_4[7:0]							
0x1785	0xFF	HDCP_TX5[7:0]	RIP_0[7:0]							
0x1786	0xFF	HDCP_TX6[7:0]	RIP_1[7:0]							
0x1787	0xFF	HDCP_TX7[7:0]	PJP[7:0]							
0x1788	0x00	HDCP_TX8[7:0]	AN_0[7:0]							
0x1789	0x00	HDCP_TX9[7:0]	AN_1[7:0]							
0x178A	0x00	HDCP_TXA[7:0]	AN_2[7:0]							
0x178B	0x00	HDCP_TXB[7:0]	AN_3[7:0]							
0x178C	0x00	HDCP_TXC[7:0]	AN_4[7:0]							
0x178D	0x00	HDCP_TXD[7:0]	AN_5[7:0]							
0x178E	0x00	HDCP_TXE[7:0]	AN_6[7:0]							

PRELIMINARY

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ADDRESS	RESET	NAME	MSB							LSB
0x178F	0x00	HDCP_TXF[7:0]	AN_7[7:0]							
0x1790	0x00	HDCP_TX10[7:0]	AKSV_0[7:0]							
0x1791	0x00	HDCP_TX11[7:0]	AKSV_1[7:0]							
0x1792	0x00	HDCP_TX12[7:0]	AKSV_2[7:0]							
0x1793	0x00	HDCP_TX13[7:0]	AKSV_3[7:0]							
0x1794	0x00	HDCP_TX14[7:0]	AKSV_4[7:0]							
0x1795	0x00	HDCP_TX15[7:0]	–	EN_INT_COMP	–	–	HDCP_RESET	START_AUTH	VSYNC_DET	ENC_EN
0x1796	0x01	HDCP_TX16[7:0]	–	–	–	PJF_MATCH	V_MATCHED	PJ_MATCHED	RI_MATCHED	INVALID_BKSV
0x1797	0x00	HDCP_TX17[7:0]	RSVD[6:0]							HDCP_REPEATER
0x1798	0x00	HDCP_TX18[7:0]	RSVD[7:0]							
0x1799	0x00	HDCP_TX19[7:0]	RSVD[1:0]		–	–	–	–	–	DIS_AUDIO_ENC
0x179A	0xFF	HDCP_TX1A[7:0]	PJFP_0[7:0]							
0x179B	0xFF	HDCP_TX1B[7:0]	PJFP_1[7:0]							
0x179C	0xFF	HDCP_TX1C[7:0]	PJFP_2[7:0]							
0x17A0	0x00	HDCP_TX20[7:0]	VH0_0[7:0]							
0x17A1	0x00	HDCP_TX21[7:0]	VH0_1[7:0]							
0x17A2	0x00	HDCP_TX22[7:0]	VH0_2[7:0]							
0x17A3	0x00	HDCP_TX23[7:0]	VH0_3[7:0]							
0x17A4	0x00	HDCP_TX24[7:0]	VH1_0[7:0]							
0x17A5	0x00	HDCP_TX25[7:0]	VH1_1[7:0]							
0x17A6	0x00	HDCP_TX26[7:0]	VH1_2[7:0]							
0x17A7	0x00	HDCP_TX27[7:0]	VH1_3[7:0]							
0x17A8	0x00	HDCP_TX28[7:0]	VH2_0[7:0]							
0x17A9	0x00	HDCP_TX29[7:0]	VH2_1[7:0]							

PRELIMINARY

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ADDRESS	RESET	NAME	MSB							LSB
0x17AA	0x00	HDCP_TX2A[7:0]	VH2_2[7:0]							
0x17AB	0x00	HDCP_TX2B[7:0]	VH2_3[7:0]							
0x17AC	0x00	HDCP_TX2C[7:0]	VH3_0[7:0]							
0x17AD	0x00	HDCP_TX2D[7:0]	VH3_1[7:0]							
0x17AE	0x00	HDCP_TX2E[7:0]	VH3_2[7:0]							
0x17AF	0x00	HDCP_TX2F[7:0]	VH3_3[7:0]							
0x17B0	0x00	HDCP_TX30[7:0]	VH4_0[7:0]							
0x17B1	0x00	HDCP_TX31[7:0]	VH4_1[7:0]							
0x17B2	0x00	HDCP_TX32[7:0]	VH4_2[7:0]							
0x17B3	0x00	HDCP_TX33[7:0]	VH4_3[7:0]							
0x17B4	0x00	HDCP_TX34[7:0]	HDCP_MAX_DEV_EXCEEDED	HDCP_DEV_CNT[6:0]						
0x17B5	0x00	HDCP_TX35[7:0]	RSVD[3:0]				HDCP_MAX_CASCADE_EXCEEDED	HDCP_DEPTH[2:0]		
0x17B6	0x00	HDCP_TX36[7:0]	HDCP_GPMEM[7:0]							
0x17B7	0xC0	HDCP_TX37[7:0]*	HDCP_PD	FAST_PJ_EN	FORCE_AUDIO	FORCE_VIDEO	AH_MASK_ENCOFF	AH_MASK_NEWDEV	AH_MASK_KSVRDY	AH_MASK_FAIL
0x17B8	0x00	HDCP_TX38[7:0]	–	–	–	–	–	AH_RD_KSVL	AH_DISENC	AH_MODE
0x17B9	0x90	HDCP_TX39[7:0]*	AH_DES_ADDR[6:0]							–
0x17BA	0x00	HDCP_TX3A[7:0]	KSV_LIST_0[7:0]							
0x17BB	0x00	HDCP_TX3B[7:0]	KSV_LIST_1[7:0]							
0x17BC	0x00	HDCP_TX3C[7:0]	KSV_LIST_2[7:0]							
0x17BD	0x00	HDCP_TX3D[7:0]	KSV_LIST_3[7:0]							
0x17BE	0x00	HDCP_TX3E[7:0]	KSV_LIST_4[7:0]							
0x17BF	0x00	HDCP_TX3F[7:0]	KSV_LIST_5[7:0]							

PRELIMINARY

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ADDRESS	RESET	NAME	MSB							LSB
0x17C0	0x00	HDCP_TX40[7:0]	KSV_LIST_6[7:0]							
0x17C1	0x00	HDCP_TX41[7:0]	KSV_LIST_7[7:0]							
0x17C2	0x00	HDCP_TX42[7:0]	KSV_LIST_8[7:0]							
0x17C3	0x00	HDCP_TX43[7:0]	KSV_LIST_9[7:0]							
0x17C4	0x00	HDCP_TX44[7:0]	KSV_LIST_10[7:0]							
0x17C5	0x00	HDCP_TX45[7:0]	KSV_LIST_11[7:0]							
0x17C6	0x00	HDCP_TX46[7:0]	KSV_LIST_12[7:0]							
0x17C7	0x00	HDCP_TX47[7:0]	KSV_LIST_13[7:0]							
0x17C8	0x00	HDCP_TX48[7:0]	KSV_LIST_14[7:0]							
0x17C9	0x00	HDCP_TX49[7:0]	KSV_LIST_15[7:0]							
0x17CA	0x00	HDCP_TX4A[7:0]	KSV_LIST_16[7:0]							
0x17CB	0x00	HDCP_TX4B[7:0]	KSV_LIST_17[7:0]							
0x17CC	0x00	HDCP_TX4C[7:0]	KSV_LIST_18[7:0]							
0x17CD	0x00	HDCP_TX4D[7:0]	KSV_LIST_19[7:0]							
0x17CE	0x00	HDCP_TX4E[7:0]	KSV_LIST_20[7:0]							
0x17CF	0x00	HDCP_TX4F[7:0]	KSV_LIST_21[7:0]							
0x17D0	0x00	HDCP_TX50[7:0]	KSV_LIST_22[7:0]							
0x17D1	0x00	HDCP_TX51[7:0]	KSV_LIST_23[7:0]							
0x17D2	0x00	HDCP_TX52[7:0]	KSV_LIST_24[7:0]							
0x17D3	0x00	HDCP_TX53[7:0]	KSV_LIST_25[7:0]							
0x17D4	0x00	HDCP_TX54[7:0]	KSV_LIST_26[7:0]							
0x17D5	0x00	HDCP_TX55[7:0]	KSV_LIST_27[7:0]							
0x17D6	0x00	HDCP_TX56[7:0]	KSV_LIST_28[7:0]							
0x17D7	0x00	HDCP_TX57[7:0]	KSV_LIST_29[7:0]							
0x17D8	0x00	HDCP_TX58[7:0]	KSV_LIST_30[7:0]							

PRELIMINARY

Release to TPK under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x17D9	0x00	HDCP_TX59[7:0]	KSV_LIST_31[7:0]							
0x17DA	0x00	HDCP_TX5A[7:0]	KSV_LIST_32[7:0]							
0x17DB	0x00	HDCP_TX5B[7:0]	KSV_LIST_33[7:0]							
0x17DC	0x00	HDCP_TX5C[7:0]	KSV_LIST_34[7:0]							
0x17DD	0x00	HDCP_TX5D[7:0]	KSV_LIST_35[7:0]							
0x17DE	0x00	HDCP_TX5E[7:0]	KSV_LIST_36[7:0]							
0x17DF	0x00	HDCP_TX5F[7:0]	KSV_LIST_37[7:0]							
0x17E0	0x00	HDCP_TX60[7:0]	KSV_LIST_38[7:0]							
0x17E1	0x00	HDCP_TX61[7:0]	KSV_LIST_39[7:0]							
0x17E2	0x00	HDCP_TX62[7:0]	KSV_LIST_40[7:0]							
0x17E3	0x00	HDCP_TX63[7:0]	KSV_LIST_41[7:0]							
0x17E4	0x00	HDCP_TX64[7:0]	KSV_LIST_42[7:0]							
0x17E5	0x00	HDCP_TX65[7:0]	KSV_LIST_43[7:0]							
0x17E6	0x00	HDCP_TX66[7:0]	KSV_LIST_44[7:0]							
0x17E7	0x00	HDCP_TX67[7:0]	KSV_LIST_45[7:0]							
0x17E8	0x00	HDCP_TX68[7:0]	KSV_LIST_46[7:0]							
0x17E9	0x00	HDCP_TX69[7:0]	KSV_LIST_47[7:0]							
0x17EA	0x00	HDCP_TX6A[7:0]	KSV_LIST_48[7:0]							
0x17EB	0x00	HDCP_TX6B[7:0]	KSV_LIST_49[7:0]							
0x17EC	0x00	HDCP_TX6C[7:0]	KSV_LIST_50[7:0]							
0x17ED	0x00	HDCP_TX6D[7:0]	KSV_LIST_51[7:0]							
0x17EE	0x00	HDCP_TX6E[7:0]	KSV_LIST_52[7:0]							
0x17EF	0x00	HDCP_TX6F[7:0]	KSV_LIST_53[7:0]							
0x17F0	0x00	HDCP_TX70[7:0]	KSV_LIST_54[7:0]							
0x17F1	0x00	HDCP_TX71[7:0]	KSV_LIST_55[7:0]							

PRELIMINARY

Release to TPK under NDA

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MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x17F2	0x00	HDCP_TX72[7:0]	KSV_LIST_56[7:0]							
0x17F3	0x00	HDCP_TX73[7:0]	KSV_LIST_57[7:0]							
0x17F4	0x00	HDCP_TX74[7:0]	KSV_LIST_58[7:0]							
0x17F5	0x00	HDCP_TX75[7:0]	KSV_LIST_59[7:0]							
0x17F6	0x00	HDCP_TX76[7:0]	KSV_LIST_60[7:0]							
0x17F7	0x00	HDCP_TX77[7:0]	KSV_LIST_61[7:0]							
0x17F8	0x00	HDCP_TX78[7:0]	KSV_LIST_62[7:0]							
0x17F9	0x00	HDCP_TX79[7:0]	KSV_LIST_63[7:0]							
0x17FA	0x00	HDCP_TX7A[7:0]	KSV_LIST_64[7:0]							
0x17FB	0x00	HDCP_TX7B[7:0]	KSV_LIST_65[7:0]							
0x17FC	0x00	HDCP_TX7C[7:0]	KSV_LIST_66[7:0]							
0x17FD	0x00	HDCP_TX7D[7:0]	KSV_LIST_67[7:0]							
0x17FE	0x00	HDCP_TX7E[7:0]	KSV_LIST_68[7:0]							
0x17FF	0x00	HDCP_TX7F[7:0]	KSV_LIST_69[7:0]							
FUNC_SAFE										
0x1D00	0x00	REGCRC0[7:0]*	–	–	RSVD	GEN_ROLLING_CRC	I2C_WR_COMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
0x1D01	0x00	REGCRC1[7:0]*	CRC_PERIOD[7:0]							
0x1D02	0x00	REGCRC2[7:0]	REGCRC_LSB[7:0]							
0x1D03	0x00	REGCRC3[7:0]	REGCRC_MSB[7:0]							
0x1D04	0x00	REGCRC4[7:0]*	MIN_RANGE_LSB[7:0]							
0x1D05	0x00	REGCRC5[7:0]*	MIN_RANGE_MSB[7:0]							
0x1D06	0xFF	REGCRC6[7:0]*	MAX_RANGE_LSB[7:0]							
0x1D07	0xFF	REGCRC7[7:0]*	MAX_RANGE_MSB[7:0]							
0x1D08	0xFF	REGCRC8[7:0]	SKIP0_LSB[7:0]							
0x1D09	0xFF	REGCRC9[7:0]	SKIP0_MSB[7:0]							

PRELIMINARY

Analog Devices Company Confidential
Provided to TPK Under NDA
Release to TPK Under NDA
Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x1D0A	0xFF	REGCRC10[7:0]	SKIP1_LSB[7:0]							
0x1D0B	0xFF	REGCRC11[7:0]	SKIP1_MSB[7:0]							
0x1D0C	0xFF	REGCRC12[7:0]	SKIP2_LSB[7:0]							
0x1D0D	0xFF	REGCRC13[7:0]	SKIP2_MSB[7:0]							
0x1D0E	0xFF	REGCRC14[7:0]	SKIP3_LSB[7:0]							
0x1D0F	0xFF	REGCRC15[7:0]	SKIP3_MSB[7:0]							
0x1D10	0xFF	REGCRC16[7:0]	SKIP4_LSB[7:0]							
0x1D11	0xFF	REGCRC17[7:0]	SKIP4_MSB[7:0]							
0x1D12	0xFF	REGCRC18[7:0]	SKIP5_LSB[7:0]							
0x1D13	0xFF	REGCRC19[7:0]	SKIP5_MSB[7:0]							
0x1D14	0xFF	REGCRC20[7:0]	SKIP6_LSB[7:0]							
0x1D15	0xFF	REGCRC21[7:0]	SKIP6_MSB[7:0]							
0x1D16	0xFF	REGCRC22[7:0]	SKIP7_LSB[7:0]							
0x1D17	0xFF	REGCRC23[7:0]	SKIP7_MSB[7:0]							
0x1D20	0x00	CC_CRC0[7:0]	CC_CRC_VAL[7:0]							
0x1D21	0x00	CC_CRC1[7:0]	MSGCNTR_LSB[7:0]							
0x1D22	0x00	CC_CRC2[7:0]	MSGCNTR_MSB[7:0]							
0x1D23	0x00	CC_CRC3[7:0]	CC_CRC_ERR_CNT[7:0]							
0x1D24	0x00	CC_CRC4[7:0]	MSGCNTR_ERR_CNT[7:0]							
0x1D25	0x00	CC_CRC5[7:0]	–	–	–	RESET_MSGCNTR	–	–	RESET_MSGCNTR_ERR_CNT	RESET_CC_CRC_ERR_CNT
0x1D26	0x20	CC_RTTN_ERR[7:0]	–	–	RTTN_CRC_INT_OEN	RTTN_CRC_ERR_FLAG	–	–	–	INJECT_RTTN_CRC_ERR
RBB_CRC_ERR A										
0x1D80	0x00	INTR_CRC_0[7:0]*	AUDIO_Y_CRC_ERR_OEN	AUDIO_X_CRC_ERR_OEN	AHDCP_CRC_ERR_OEN	GPIO_CRC_ERR_OEN	SPI_CRC_ERR_OEN	RBB_CC_CRC_ERR_OEN	PT2_CRC_ERR_OEN	PT1_CRC_ERR_OEN

PRELIMINARY

Release to TPK Under NDA

Analog Devices Company Confidential Provided to OEM Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x1D81	0x00	INTR_CRC_1[7:0]	AUDIO_Y_CRC_ERR_FLAG	AUDIO_X_CRC_ERR_FLAG	AHDCP_CRC_ERR_FLAG	GPIO_CRC_ERR_FLAG	SPI_CRC_ERR_FLAG	RBB_CC_CRC_ERR_FLAG	PT2_CRC_ERR_FLAG	PT1_CRC_ERR_FLAG
0x1D82	0x00	CNT0[7:0]	PT1_CRC_ERR[7:0]							
0x1D83	0x00	CNT1[7:0]	PT2_CRC_ERR[7:0]							
0x1D84	0x00	CNT2[7:0]	RBB_CC_CRC_ERR[7:0]							
0x1D85	0x00	CNT3[7:0]	SPI_CRC_ERR[7:0]							
0x1D86	0x00	CNT4[7:0]	GPIO_CRC_ERR[7:0]							
0x1D87	0x00	CNT5[7:0]	AHDCP_CRC_ERR[7:0]							
0x1D88	0x00	CNT6[7:0]	AUDIO_X_CRC_ERR[7:0]							
0x1D89	0x00	CNT7[7:0]	AUDIO_Y_CRC_ERR[7:0]							
0x1D8A	0x00	CNT8[7:0]	INFOFR_CRC_ERR[7:0]							
0x1D8B	0x00	INTR_CRC_2[7:0]*	–	–	–	–	–	–	–	INFOFR_CRC_ERR_OEN
0x1D8C	0x00	INTR_CRC_3[7:0]	–	–	–	–	–	–	–	INFOFR_CRC_ERR_FLAG
RBB_CRC_ERR B										
0x1D90	0x00	INTR_CRC_0[7:0]*	AUDIO_Y_CRC_ERR_OEN	AUDIO_X_CRC_ERR_OEN	AHDCP_CRC_ERR_OEN	GPIO_CRC_ERR_OEN	SPI_CRC_ERR_OEN	RBB_CC_CRC_ERR_OEN	PT2_CRC_ERR_OEN	PT1_CRC_ERR_OEN
0x1D91	0x00	INTR_CRC_1[7:0]	AUDIO_Y_CRC_ERR_FLAG	AUDIO_X_CRC_ERR_FLAG	AHDCP_CRC_ERR_FLAG	GPIO_CRC_ERR_FLAG	SPI_CRC_ERR_FLAG	RBB_CC_CRC_ERR_FLAG	PT2_CRC_ERR_FLAG	PT1_CRC_ERR_FLAG
0x1D92	0x00	CNT0[7:0]	PT1_CRC_ERR[7:0]							
0x1D93	0x00	CNT1[7:0]	PT2_CRC_ERR[7:0]							
0x1D94	0x00	CNT2[7:0]	RBB_CC_CRC_ERR[7:0]							
0x1D95	0x00	CNT3[7:0]	SPI_CRC_ERR[7:0]							
0x1D96	0x00	CNT4[7:0]	GPIO_CRC_ERR[7:0]							
0x1D97	0x00	CNT5[7:0]	AHDCP_CRC_ERR[7:0]							
0x1D98	0x00	CNT6[7:0]	AUDIO_X_CRC_ERR[7:0]							
0x1D99	0x00	CNT7[7:0]	AUDIO_Y_CRC_ERR[7:0]							
0x1D9A	0x00	CNT8[7:0]	INFOFR_CRC_ERR[7:0]							
0x1D9B	0x00	INTR_CRC_2[7:0]*	–	–	–	–	–	–	–	INFOFR_CRC_ERR_OEN
0x1D9C	0x00	INTR_CRC_3[7:0]	–	–	–	–	–	–	–	INFOFR_CRC_ERR_FLAG
PROG_CRC										
0x2000	0x00	COEFF_0_0[7:0]	COEFF_0_0[7:0]							

PRELIMINARY

Release 9 TPK Under NDA

Analog Devices Company Confidential, Provided to Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x2001	0x41	COEFF_0_1[7:0]	COEFF_0_1[7:0]							
0x2002	0x16	COEFF_0_2[7:0]	COEFF_0_2[7:0]							
0x2003	0x01	COEFF_0_3[7:0]	COEFF_0_3[7:0]							
0x2004	0x41	COEFF_0_4[7:0]	COEFF_0_4[7:0]							
0x2005	0x16	COEFF_0_5[7:0]	COEFF_0_5[7:0]							
0x2006	0x01	COEFF_0_6[7:0]	COEFF_0_6[7:0]							
0x2008	0x00	COEFF_1_0[7:0]	COEFF_1_0[7:0]							
0x2009	0xC3	COEFF_1_1[7:0]	COEFF_1_1[7:0]							
0x200A	0x3A	COEFF_1_2[7:0]	COEFF_1_2[7:0]							
0x200B	0x03	COEFF_1_3[7:0]	COEFF_1_3[7:0]							
0x200C	0xC3	COEFF_1_4[7:0]	COEFF_1_4[7:0]							
0x200D	0x3A	COEFF_1_5[7:0]	COEFF_1_5[7:0]							
0x200E	0x03	COEFF_1_6[7:0]	COEFF_1_6[7:0]							
0x2010	0x00	COEFF_2_0[7:0]	COEFF_2_0[7:0]							
0x2011	0xC7	COEFF_2_1[7:0]	COEFF_2_1[7:0]							
0x2012	0x63	COEFF_2_2[7:0]	COEFF_2_2[7:0]							
0x2013	0x07	COEFF_2_3[7:0]	COEFF_2_3[7:0]							
0x2014	0xC7	COEFF_2_4[7:0]	COEFF_2_4[7:0]							
0x2015	0x63	COEFF_2_5[7:0]	COEFF_2_5[7:0]							
0x2016	0x07	COEFF_2_6[7:0]	COEFF_2_6[7:0]							
0x2018	0x00	COEFF_3_0[7:0]	COEFF_3_0[7:0]							
0x2019	0x8E	COEFF_3_1[7:0]	COEFF_3_1[7:0]							
0x201A	0xC7	COEFF_3_2[7:0]	COEFF_3_2[7:0]							
0x201B	0x0E	COEFF_3_3[7:0]	COEFF_3_3[7:0]							
0x201C	0x8E	COEFF_3_4[7:0]	COEFF_3_4[7:0]							

PRELIMINARY

Analog Devices Company Confidential
Provided to TPK Under NDA
Release to TPK Under NDA
Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x201D	0xC7	COEFF_3_5[7:0]	COEFF_3_5[7:0]							
0x201E	0x0E	COEFF_3_6[7:0]	COEFF_3_6[7:0]							
0x2020	0x00	COEFF_4_0[7:0]	COEFF_4_0[7:0]							
0x2021	0x5D	COEFF_4_1[7:0]	COEFF_4_1[7:0]							
0x2022	0x99	COEFF_4_2[7:0]	COEFF_4_2[7:0]							
0x2023	0x1C	COEFF_4_3[7:0]	COEFF_4_3[7:0]							
0x2024	0x5D	COEFF_4_4[7:0]	COEFF_4_4[7:0]							
0x2025	0x99	COEFF_4_5[7:0]	COEFF_4_5[7:0]							
0x2026	0x1C	COEFF_4_6[7:0]	COEFF_4_6[7:0]							
0x2028	0x00	COEFF_5_0[7:0]	COEFF_5_0[7:0]							
0x2029	0xFB	COEFF_5_1[7:0]	COEFF_5_1[7:0]							
0x202A	0x24	COEFF_5_2[7:0]	COEFF_5_2[7:0]							
0x202B	0x38	COEFF_5_3[7:0]	COEFF_5_3[7:0]							
0x202C	0xFB	COEFF_5_4[7:0]	COEFF_5_4[7:0]							
0x202D	0x24	COEFF_5_5[7:0]	COEFF_5_5[7:0]							
0x202E	0x38	COEFF_5_6[7:0]	COEFF_5_6[7:0]							
0x2030	0x00	COEFF_6_0[7:0]	COEFF_6_0[7:0]							
0x2031	0xF6	COEFF_6_1[7:0]	COEFF_6_1[7:0]							
0x2032	0x49	COEFF_6_2[7:0]	COEFF_6_2[7:0]							
0x2033	0x70	COEFF_6_3[7:0]	COEFF_6_3[7:0]							
0x2034	0xF6	COEFF_6_4[7:0]	COEFF_6_4[7:0]							
0x2035	0x49	COEFF_6_5[7:0]	COEFF_6_5[7:0]							
0x2036	0x70	COEFF_6_6[7:0]	COEFF_6_6[7:0]							
0x2038	0x00	COEFF_7_0[7:0]	COEFF_7_0[7:0]							
0x2039	0xAD	COEFF_7_1[7:0]	COEFF_7_1[7:0]							

PRELIMINARY

Release to TPK Under NDA

Analog Devices Company Confidential
Provided to Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x203A	0x85	COEFF_7_2[7:0]	COEFF_7_2[7:0]							
0x203B	0xE1	COEFF_7_3[7:0]	COEFF_7_3[7:0]							
0x203C	0xAD	COEFF_7_4[7:0]	COEFF_7_4[7:0]							
0x203D	0x85	COEFF_7_5[7:0]	COEFF_7_5[7:0]							
0x203E	0xE1	COEFF_7_6[7:0]	COEFF_7_6[7:0]							
0x2040	0x00	COEFF_8_0[7:0]	COEFF_8_0[7:0]							
0x2041	0x1B	COEFF_8_1[7:0]	COEFF_8_1[7:0]							
0x2042	0x1D	COEFF_8_2[7:0]	COEFF_8_2[7:0]							
0x2043	0xC2	COEFF_8_3[7:0]	COEFF_8_3[7:0]							
0x2044	0x1B	COEFF_8_4[7:0]	COEFF_8_4[7:0]							
0x2045	0x1D	COEFF_8_5[7:0]	COEFF_8_5[7:0]							
0x2046	0xC2	COEFF_8_6[7:0]	COEFF_8_6[7:0]							
0x2048	0x00	COEFF_9_0[7:0]	COEFF_9_0[7:0]							
0x2049	0x36	COEFF_9_1[7:0]	COEFF_9_1[7:0]							
0x204A	0x3A	COEFF_9_2[7:0]	COEFF_9_2[7:0]							
0x204B	0x84	COEFF_9_3[7:0]	COEFF_9_3[7:0]							
0x204C	0x36	COEFF_9_4[7:0]	COEFF_9_4[7:0]							
0x204D	0x3A	COEFF_9_5[7:0]	COEFF_9_5[7:0]							
0x204E	0x84	COEFF_9_6[7:0]	COEFF_9_6[7:0]							
0x2050	0x00	COEFF_10_0[7:0]	COEFF_10_0[7:0]							
0x2051	0x2D	COEFF_10_1[7:0]	COEFF_10_1[7:0]							
0x2052	0x62	COEFF_10_2[7:0]	COEFF_10_2[7:0]							
0x2053	0x09	COEFF_10_3[7:0]	COEFF_10_3[7:0]							
0x2054	0x2D	COEFF_10_4[7:0]	COEFF_10_4[7:0]							
0x2055	0x62	COEFF_10_5[7:0]	COEFF_10_5[7:0]							

PRELIMINARY

Release to TPK Under NDA

Analog Devices Company Confidential
Provided to Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x2056	0x09	COEFF_10_6 [7:0]	COEFF_10_6[7:0]							
0x2058	0x00	COEFF_11_0 [7:0]	COEFF_11_0[7:0]							
0x2059	0x1B	COEFF_11_1 [7:0]	COEFF_11_1[7:0]							
0x205A	0xD2	COEFF_11_2 [7:0]	COEFF_11_2[7:0]							
0x205B	0x13	COEFF_11_3 [7:0]	COEFF_11_3[7:0]							
0x205C	0x1B	COEFF_11_4 [7:0]	COEFF_11_4[7:0]							
0x205D	0xD2	COEFF_11_5 [7:0]	COEFF_11_5[7:0]							
0x205E	0x13	COEFF_11_6 [7:0]	COEFF_11_6[7:0]							
0x2060	0x00	COEFF_12_0 [7:0]	COEFF_12_0[7:0]							
0x2061	0x77	COEFF_12_1 [7:0]	COEFF_12_1[7:0]							
0x2062	0xB2	COEFF_12_2 [7:0]	COEFF_12_2[7:0]							
0x2063	0x26	COEFF_12_3 [7:0]	COEFF_12_3[7:0]							
0x2064	0x77	COEFF_12_4 [7:0]	COEFF_12_4[7:0]							
0x2065	0xB2	COEFF_12_5 [7:0]	COEFF_12_5[7:0]							
0x2066	0x26	COEFF_12_6 [7:0]	COEFF_12_6[7:0]							
0x2068	0x00	COEFF_13_0 [7:0]	COEFF_13_0[7:0]							
0x2069	0xEE	COEFF_13_1 [7:0]	COEFF_13_1[7:0]							
0x206A	0x64	COEFF_13_2 [7:0]	COEFF_13_2[7:0]							
0x206B	0x4D	COEFF_13_3 [7:0]	COEFF_13_3[7:0]							
0x206C	0xEE	COEFF_13_4 [7:0]	COEFF_13_4[7:0]							
0x206D	0x64	COEFF_13_5 [7:0]	COEFF_13_5[7:0]							
0x206E	0x4D	COEFF_13_6 [7:0]	COEFF_13_6[7:0]							
0x2070	0x00	COEFF_14_0 [7:0]	COEFF_14_0[7:0]							
0x2071	0xDC	COEFF_14_1 [7:0]	COEFF_14_1[7:0]							
0x2072	0xC9	COEFF_14_2 [7:0]	COEFF_14_2[7:0]							

PRELIMINARY

Release to TPK under NDA

Analog Devices Company Confidential
Provided to Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x2073	0x9A	COEFF_14_3 [7:0]	COEFF_14_3[7:0]							
0x2074	0xDC	COEFF_14_4 [7:0]	COEFF_14_4[7:0]							
0x2075	0xC9	COEFF_14_5 [7:0]	COEFF_14_5[7:0]							
0x2076	0x9A	COEFF_14_6 [7:0]	COEFF_14_6[7:0]							
0x2078	0x00	COEFF_15_0 [7:0]	COEFF_15_0[7:0]							
0x2079	0xB8	COEFF_15_1 [7:0]	COEFF_15_1[7:0]							
0x207A	0x93	COEFF_15_2 [7:0]	COEFF_15_2[7:0]							
0x207B	0x35	COEFF_15_3 [7:0]	COEFF_15_3[7:0]							
0x207C	0xB8	COEFF_15_4 [7:0]	COEFF_15_4[7:0]							
0x207D	0x93	COEFF_15_5 [7:0]	COEFF_15_5[7:0]							
0x207E	0x35	COEFF_15_6 [7:0]	COEFF_15_6[7:0]							
0x2080	0x00	COEFF_16_0 [7:0]	COEFF_16_0[7:0]							
0x2081	0x31	COEFF_16_1 [7:0]	COEFF_16_1[7:0]							
0x2082	0x31	COEFF_16_2 [7:0]	COEFF_16_2[7:0]							
0x2083	0x6A	COEFF_16_3 [7:0]	COEFF_16_3[7:0]							
0x2084	0x31	COEFF_16_4 [7:0]	COEFF_16_4[7:0]							
0x2085	0x31	COEFF_16_5 [7:0]	COEFF_16_5[7:0]							
0x2086	0x6A	COEFF_16_6 [7:0]	COEFF_16_6[7:0]							
0x2088	0x00	COEFF_17_0 [7:0]	COEFF_17_0[7:0]							
0x2089	0x62	COEFF_17_1 [7:0]	COEFF_17_1[7:0]							
0x208A	0x62	COEFF_17_2 [7:0]	COEFF_17_2[7:0]							
0x208B	0xD4	COEFF_17_3 [7:0]	COEFF_17_3[7:0]							
0x208C	0x62	COEFF_17_4 [7:0]	COEFF_17_4[7:0]							
0x208D	0x62	COEFF_17_5 [7:0]	COEFF_17_5[7:0]							
0x208E	0xD4	COEFF_17_6 [7:0]	COEFF_17_6[7:0]							

PRELIMINARY

Release to TPK under NDA

Analog Devices Company Confidential
Provided to Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x2090	0x00	COEFF_18_0 [7:0]	COEFF_18_0[7:0]							
0x2091	0xC4	COEFF_18_1 [7:0]	COEFF_18_1[7:0]							
0x2092	0xC4	COEFF_18_2 [7:0]	COEFF_18_2[7:0]							
0x2093	0xA8	COEFF_18_3 [7:0]	COEFF_18_3[7:0]							
0x2094	0xC4	COEFF_18_4 [7:0]	COEFF_18_4[7:0]							
0x2095	0xC4	COEFF_18_5 [7:0]	COEFF_18_5[7:0]							
0x2096	0xA8	COEFF_18_6 [7:0]	COEFF_18_6[7:0]							
0x2098	0x00	COEFF_19_0 [7:0]	COEFF_19_0[7:0]							
0x2099	0x88	COEFF_19_1 [7:0]	COEFF_19_1[7:0]							
0x209A	0x89	COEFF_19_2 [7:0]	COEFF_19_2[7:0]							
0x209B	0x51	COEFF_19_3 [7:0]	COEFF_19_3[7:0]							
0x209C	0x88	COEFF_19_4 [7:0]	COEFF_19_4[7:0]							
0x209D	0x89	COEFF_19_5 [7:0]	COEFF_19_5[7:0]							
0x209E	0x51	COEFF_19_6 [7:0]	COEFF_19_6[7:0]							
0x20A0	0x00	COEFF_20_0 [7:0]	COEFF_20_0[7:0]							
0x20A1	0x10	COEFF_20_1 [7:0]	COEFF_20_1[7:0]							
0x20A2	0x13	COEFF_20_2 [7:0]	COEFF_20_2[7:0]							
0x20A3	0xA3	COEFF_20_3 [7:0]	COEFF_20_3[7:0]							
0x20A4	0x10	COEFF_20_4 [7:0]	COEFF_20_4[7:0]							
0x20A5	0x13	COEFF_20_5 [7:0]	COEFF_20_5[7:0]							
0x20A6	0xA3	COEFF_20_6 [7:0]	COEFF_20_6[7:0]							
0x20A8	0x00	COEFF_21_0 [7:0]	COEFF_21_0[7:0]							
0x20A9	0x20	COEFF_21_1 [7:0]	COEFF_21_1[7:0]							
0x20AA	0x26	COEFF_21_2 [7:0]	COEFF_21_2[7:0]							
0x20AB	0x46	COEFF_21_3 [7:0]	COEFF_21_3[7:0]							

PRELIMINARY

Analog Devices Company Confidential
Provided to TPK_Customers Under NDA
Release to TPK under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x20AC	0x20	COEFF_21_4 [7:0]	COEFF_21_4[7:0]							
0x20AD	0x26	COEFF_21_5 [7:0]	COEFF_21_5[7:0]							
0x20AE	0x46	COEFF_21_6 [7:0]	COEFF_21_6[7:0]							
0x20B0	0x00	COEFF_22_0 [7:0]	COEFF_22_0[7:0]							
0x20B1	0x01	COEFF_22_1 [7:0]	COEFF_22_1[7:0]							
0x20B2	0x5A	COEFF_22_2 [7:0]	COEFF_22_2[7:0]							
0x20B3	0x8D	COEFF_22_3 [7:0]	COEFF_22_3[7:0]							
0x20B4	0x01	COEFF_22_4 [7:0]	COEFF_22_4[7:0]							
0x20B5	0x5A	COEFF_22_5 [7:0]	COEFF_22_5[7:0]							
0x20B6	0x8D	COEFF_22_6 [7:0]	COEFF_22_6[7:0]							
0x20B8	0x00	COEFF_23_0 [7:0]	COEFF_23_0[7:0]							
0x20B9	0x43	COEFF_23_1 [7:0]	COEFF_23_1[7:0]							
0x20BA	0xA2	COEFF_23_2 [7:0]	COEFF_23_2[7:0]							
0x20BB	0x1B	COEFF_23_3 [7:0]	COEFF_23_3[7:0]							
0x20BC	0x43	COEFF_23_4 [7:0]	COEFF_23_4[7:0]							
0x20BD	0xA2	COEFF_23_5 [7:0]	COEFF_23_5[7:0]							
0x20BE	0x1B	COEFF_23_6 [7:0]	COEFF_23_6[7:0]							
0x20C0	0x01	COEFF_24_0 [7:0]	COEFF_24_0[7:0]							
0x20C1	0x86	COEFF_24_1 [7:0]	COEFF_24_1[7:0]							
0x20C2	0x44	COEFF_24_2 [7:0]	COEFF_24_2[7:0]							
0x20C3	0x37	COEFF_24_3 [7:0]	COEFF_24_3[7:0]							
0x20C4	0x86	COEFF_24_4 [7:0]	COEFF_24_4[7:0]							
0x20C5	0x44	COEFF_24_5 [7:0]	COEFF_24_5[7:0]							
0x20C6	0x37	COEFF_24_6 [7:0]	COEFF_24_6[7:0]							
0x20C8	0x02	COEFF_25_0 [7:0]	COEFF_25_0[7:0]							

PRELIMINARY

Release to TPK under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x20C9	0x0C	COEFF_25_1 [7:0]	COEFF_25_1[7:0]							
0x20CA	0x89	COEFF_25_2 [7:0]	COEFF_25_2[7:0]							
0x20CB	0x6E	COEFF_25_3 [7:0]	COEFF_25_3[7:0]							
0x20CC	0x0C	COEFF_25_4 [7:0]	COEFF_25_4[7:0]							
0x20CD	0x89	COEFF_25_5 [7:0]	COEFF_25_5[7:0]							
0x20CE	0x6E	COEFF_25_6 [7:0]	COEFF_25_6[7:0]							
0x20D0	0x04	COEFF_26_0 [7:0]	COEFF_26_0[7:0]							
0x20D1	0x59	COEFF_26_1 [7:0]	COEFF_26_1[7:0]							
0x20D2	0x04	COEFF_26_2 [7:0]	COEFF_26_2[7:0]							
0x20D3	0xDC	COEFF_26_3 [7:0]	COEFF_26_3[7:0]							
0x20D4	0x59	COEFF_26_4 [7:0]	COEFF_26_4[7:0]							
0x20D5	0x04	COEFF_26_5 [7:0]	COEFF_26_5[7:0]							
0x20D6	0xDC	COEFF_26_6 [7:0]	COEFF_26_6[7:0]							
0x20D8	0x08	COEFF_27_0 [7:0]	COEFF_27_0[7:0]							
0x20D9	0xB2	COEFF_27_1 [7:0]	COEFF_27_1[7:0]							
0x20DA	0x08	COEFF_27_2 [7:0]	COEFF_27_2[7:0]							
0x20DB	0xB8	COEFF_27_3 [7:0]	COEFF_27_3[7:0]							
0x20DC	0xB2	COEFF_27_4 [7:0]	COEFF_27_4[7:0]							
0x20DD	0x08	COEFF_27_5 [7:0]	COEFF_27_5[7:0]							
0x20DE	0xB8	COEFF_27_6 [7:0]	COEFF_27_6[7:0]							
0x20E0	0x10	COEFF_28_0 [7:0]	COEFF_28_0[7:0]							
0x20E1	0x64	COEFF_28_1 [7:0]	COEFF_28_1[7:0]							
0x20E2	0x11	COEFF_28_2 [7:0]	COEFF_28_2[7:0]							
0x20E3	0x70	COEFF_28_3 [7:0]	COEFF_28_3[7:0]							
0x20E4	0x64	COEFF_28_4 [7:0]	COEFF_28_4[7:0]							

PRELIMINARY

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ADDRESS	RESET	NAME	MSB							LSB
0x20E5	0x11	COEFF_28_5[7:0]	COEFF_28_5[7:0]							
0x20E6	0x70	COEFF_28_6[7:0]	COEFF_28_6[7:0]							
0x20E8	0x20	COEFF_29_0[7:0]	COEFF_29_0[7:0]							
0x20E9	0xC8	COEFF_29_1[7:0]	COEFF_29_1[7:0]							
0x20EA	0x22	COEFF_29_2[7:0]	COEFF_29_2[7:0]							
0x20EB	0xE0	COEFF_29_3[7:0]	COEFF_29_3[7:0]							
0x20EC	0xC8	COEFF_29_4[7:0]	COEFF_29_4[7:0]							
0x20ED	0x22	COEFF_29_5[7:0]	COEFF_29_5[7:0]							
0x20EE	0xE0	COEFF_29_6[7:0]	COEFF_29_6[7:0]							
0x20F0	0x40	COEFF_30_0[7:0]	COEFF_30_0[7:0]							
0x20F1	0x90	COEFF_30_1[7:0]	COEFF_30_1[7:0]							
0x20F2	0x45	COEFF_30_2[7:0]	COEFF_30_2[7:0]							
0x20F3	0xC0	COEFF_30_3[7:0]	COEFF_30_3[7:0]							
0x20F4	0x90	COEFF_30_4[7:0]	COEFF_30_4[7:0]							
0x20F5	0x45	COEFF_30_5[7:0]	COEFF_30_5[7:0]							
0x20F6	0xC0	COEFF_30_6[7:0]	COEFF_30_6[7:0]							
0x20F8	0x80	COEFF_31_0[7:0]	COEFF_31_0[7:0]							
0x20F9	0x20	COEFF_31_1[7:0]	COEFF_31_1[7:0]							
0x20FA	0x8B	COEFF_31_2[7:0]	COEFF_31_2[7:0]							
0x20FB	0x80	COEFF_31_3[7:0]	COEFF_31_3[7:0]							
0x20FC	0x20	COEFF_31_4[7:0]	COEFF_31_4[7:0]							
0x20FD	0x8B	COEFF_31_5[7:0]	COEFF_31_5[7:0]							
0x20FE	0x80	COEFF_31_6[7:0]	COEFF_31_6[7:0]							
0x20FF	0x00	PROG_CRC_1[7:0]	PROG_CRC_EN_Y	PROG_CRC_EN_X	–	–	–	–	–	–

PRELIMINARY

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Release to TPK Under NDA
Customers Under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x2100	0x00	PROG_CRC_2[7:0]	FRAME_CNT_Y[3:0]				FRAME_CNT_X[3:0]			
0x2101	0x00	PROG_CRC_3[7:0]	PROG_CRC_VAL_X0[7:0]							
0x2102	0x00	PROG_CRC_4[7:0]	PROG_CRC_VAL_X1[7:0]							
0x2103	0x00	PROG_CRC_5[7:0]	PROG_CRC_VAL_X2[7:0]							
0x2104	0x00	PROG_CRC_6[7:0]	PROG_CRC_VAL_X3[7:0]							
0x2105	0x00	PROG_CRC_7[7:0]	PROG_CRC_VAL_Y0[7:0]							
0x2106	0x00	PROG_CRC_8[7:0]	PROG_CRC_VAL_Y1[7:0]							
0x2107	0x00	PROG_CRC_9[7:0]	PROG_CRC_VAL_Y2[7:0]							
0x2108	0x00	PROG_CRC_10[7:0]	PROG_CRC_VAL_Y3[7:0]							
VCRC_CHK X										
0x2280	0x64	VCRC_CHK_REG1[7:0]*	FCRC_CHECK_EN	EN_VOTING_FOR_FCRC	EN_VOTING_FOR_FCNT	USE_FCRC_VALID	FCRC_CHECK_SEL	SPRS_LAST_DE	–	–
0x2281	0x00	VCRC_CHK_REG2[7:0]	FCRC_CHECK_ERR	VOTE_ERR_FCRC	VOTE_ERR_FCNT	–	–	–	–	–
0x2282	0x00	VCRC_CHK_REG3[7:0]	FCRC_CHECK_ERR_LAST	–	–	–	–	–	–	–
0x2283	0x00	VCRC_CHK_REG4[7:0]	FCRC_RCVD_0[7:0]							
0x2284	0x00	VCRC_CHK_REG5[7:0]	FCRC_RCVD_1[7:0]							
0x2285	0x00	VCRC_CHK_REG6[7:0]	FCRC_RCVD_2[7:0]							
0x2286	0x00	VCRC_CHK_REG7[7:0]	FCRC_RCVD_3[7:0]							
0x2287	0x00	VCRC_CHK_REG8[7:0]	FCNT_RCVD_0[7:0]							
0x2288	0x00	VCRC_CHK_REG9[7:0]	FCNT_RCVD_1[7:0]							
0x2289	0x00	VCRC_CHK_REG10[7:0]	FCNT_RCVD_2[7:0]							
0x228A	0x00	VCRC_CHK_REG11[7:0]	FCNT_RCVD_3[7:0]							
VCRC_CHK Y										
0x2290	0x64	VCRC_CHK_REG1[7:0]*	FCRC_CHECK_EN	EN_VOTING_FOR_FCRC	EN_VOTING_FOR_FCNT	USE_FCRC_VALID	FCRC_CHECK_SEL	SPRS_LAST_DE	–	–

PRELIMINARY

Release to TX under NDA

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Provided to Z_Customers Under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x2291	0x00	VCRC_CHK_REG2[7:0]	FCRC_CHECK_ERR	VOTE_ERR_FCRC	VOTE_ERR_FCNT	–	–	–	–	–
0x2292	0x00	VCRC_CHK_REG3[7:0]	FCRC_CHECK_ERR_LAST	–	–	–	–	–	–	–
0x2293	0x00	VCRC_CHK_REG4[7:0]	FCRC_RCVD_0[7:0]							
0x2294	0x00	VCRC_CHK_REG5[7:0]	FCRC_RCVD_1[7:0]							
0x2295	0x00	VCRC_CHK_REG6[7:0]	FCRC_RCVD_2[7:0]							
0x2296	0x00	VCRC_CHK_REG7[7:0]	FCRC_RCVD_3[7:0]							
0x2297	0x00	VCRC_CHK_REG8[7:0]	FCNT_RCVD_0[7:0]							
0x2298	0x00	VCRC_CHK_REG9[7:0]	FCNT_RCVD_1[7:0]							
0x2299	0x00	VCRC_CHK_REG10[7:0]	FCNT_RCVD_2[7:0]							
0x229A	0x00	VCRC_CHK_REG11[7:0]	FCNT_RCVD_3[7:0]							
CTRL_REGS_PICOMAX										
PROFILE										
DP_FCRC_INFO A										
DP_FCRC_INFO B										
HDCP2_TX X										
0x4100	0xA0	SYS_CNTL_B0[7:0]*	cmd_reset	clk_en	hdcp2_en	stream_en	sys_int_en[3:0]			
0x4101	0x00	SYS_CNTL_B1[7:0]	–	–	–	–	–	–	video_off	audio_off
0x4102	0x00	SYS_CNTL_B2[7:0]	cipher_fail	–	–	–	sys_int_stat[3:0]			
0x4103	0x00	SYS_CNTL_B3[7:0]	encryption_en	av_masked	tx_stat[5:0]					
0x4104	0x74	SYS_COMM_B0[7:0]*	i2c_slave_ID[6:0]							–
0x4105	0x0A	SYS_COMM_B1[7:0]	RSVD[2:0]			ahcc_slv_to[1:0]		i2c_speed[2:0]		
0x4106	0x08	SYS_COMM_B2[7:0]	–	–	–	hdcp_link_sel	RSVD[1:0]		i2c_slave_order[1:0]	
0x4107	0x00	SYS_COMM_B3[7:0]	–	–	–	–	–	–	–	–
0x4108	0x00	SYS_STAT_B0[7:0]	–	–	–	–	encryption_en_all[3:0]			
0x410A	0x00	RX_ID_0[7:0]	hdcp2_rxid_0[7:0]							
0x410B	0x00	RX_ID_1[7:0]	hdcp2_rxid_1[7:0]							
0x410D	0x00	RX_ID_2[7:0]	hdcp2_rxid_2[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x410E	0x00	RX_ID_3[7:0]	hdcp2_rxid_3[7:0]							
0x410F	0x00	RX_ID_4[7:0]	hdcp2_rxid_4[7:0]							
HDCP2_TX Y										
0x4110	0xA0	SYS_CNTL_B0[7:0]*	RSVD	RSVD	hdcp2_en	stream_en	sys_int_en[3:0]			
0x4111	0x00	SYS_CNTL_B1[7:0]	–	–	–	–	–	–	video_off	audio_off
0x4112	0x00	SYS_CNTL_B2[7:0]	cipher_fail	–	–	–	sys_int_stat[3:0]			
0x4113	0x00	SYS_CNTL_B3[7:0]	encryption_en	av_masked	tx_stat[5:0]					
0x4114	0x72	SYS_COMM_B0[7:0]*	i2c_slave_ID[6:0]							–
0x4115	0x02	SYS_COMM_B1[7:0]	–	–	–	–	–	RSVD[2:0]		
0x4116	0x10	SYS_COMM_B2[7:0]	–	–	–	hdcp_link_sel	–	–	i2c_slave_order[1:0]	
0x4117	0x00	SYS_COMM_B3[7:0]	–	–	–	–	–	–	–	–
0x411A	0x00	RX_ID_0[7:0]	hdcp2_rxid_0[7:0]							
0x411B	0x00	RX_ID_1[7:0]	hdcp2_rxid_1[7:0]							
0x411D	0x00	RX_ID_2[7:0]	hdcp2_rxid_2[7:0]							
0x411E	0x00	RX_ID_3[7:0]	hdcp2_rxid_3[7:0]							
0x411F	0x00	RX_ID_4[7:0]	hdcp2_rxid_4[7:0]							
HDCP2_PMX_SS										
0x41A0	0x00	SYS_IPC_OUTBOX_B0[7:0]	ipc_outbox[7:0]							
0x41A1	0x00	SYS_IPC_OUTBOX_B1[7:0]	ipc_outbox[7:0]							
0x41A2	0x00	SYS_IPC_OUTBOX_B2[7:0]	ipc_outbox[7:0]							
0x41A3	0x00	SYS_IPC_OUTBOX_B3[7:0]	ipc_outbox[7:0]							
0x41A4	0x00	SYS_IPC_INBOX_B0[7:0]	ipc_inbox[7:0]							
0x41A5	0x00	SYS_IPC_INBOX_B1[7:0]	ipc_inbox[7:0]							
0x41A6	0x00	SYS_IPC_INBOX_B2[7:0]	ipc_inbox[7:0]							
0x41A7	0x00	SYS_IPC_INBOX_B3[7:0]	ipc_inbox[7:0]							
0x41A8	0x00	SYS_IPC_IS_B0[7:0]	–	–	–	–	–	–	–	ipc_inbox_int_stat

PRELIMINARY

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ADDRESS	RESET	NAME	MSB							LSB
0x41AC	0x00	SYS_IPC_IE_B0[7:0]	–	–	–	–	–	–	–	ipc_inbox_int_en
SGMII_CTRL										
0x5000	0x10	SGMII_0[7:0]*	RESET_SGMII_IP	RSVD	SGMII_RX_PIN_SWAP	RSVD	SGMII_MDIO_EN	SGMII_TXCLK_EN	SGMII_EXT_RXCLK_EN	SGMII_EN
0x5005	0x00	SGMII_5[7:0]	RSVD	SGMII_STOP_ERR	DPLLLOCK_SNAP_ON_SGMII_STOP	WBLOCK_SNAP_ON_SGMII_STOP	–	–	–	–
0x5015	0x00	SGMII_21[7:0]	–	–	–	–	SGMII_PRBS_CHECK_STATUS	SGMII_DEC_ERR_FLAG	SGMII_PRBS_ERR_FLAG	SGMII_INT
0x5016	0x00	SGMII_22[7:0]	–	–	–	SGMII_XPCS_LINK_STATUS	RSVD	RSVD	ACT_DET_DATA	ACT_DET_CLK
0x5026	0x00	SGMII_32[7:0]	RSVD[7:0]							
0x5027	0x00	SGMII_33[7:0]	SGMII_DEC_ERR_CNT[7:0]							
SGMII										
EDPRX_CTRL										
0x6418	0x00	DPRX_TRN_STATUS0[7:0]	DPRX_LINK_RATE[7:0]							
0x6419	0x00	DPRX_TRN_STATUS1[7:0]	–	–	–	DPRX_LANE_CNT[4:0]				
0x641A	0x00	DPRX_TRN_STATUS2[7:0]	DPRX_TRAIN_STATE[3:0]				–	DPRX_TRAIN_PAT[2:0]		
0x641B	0x05	DPRX_TRN_STATUS3[7:0]	–	–	–	–	–	SYM_LOCK_COMB	LQP_TRN_NOCLR	TPS4_DESCRAM_ON
0x641C	0x00	DPRX_VID_STATUS0[7:0]	–	–	–	VBID_DSC_0	VBID_AUD_MUTE_0	VBID_NOVID_0	VBID_VBLANK_0	MODE_UPD_0
0x641D	0x00	DPRX_VID_STATUS1[7:0]	–	–	–	VBID_DSC_1	VBID_AUD_MUTE_1	VBID_NOVID_1	VBID_VBLANK_1	MODE_UPD_1
0x6420	0x00	EDP_VIDEO_CTRL0[7:0]*	RSVD	RSVD	RSVD	RSVD	–	–	VIDEO_OUT_EN[1:0]	
0x6421	0x03	EDP_VIDEO_CTRL1[7:0]*	–	DBL_PXL_EN_0	DUP_0	RSVD	–	–	FORCE_PXCLK_RUN[1:0]	
0x6422	0x75	EDP_VIDEO_CTRL2[7:0]*	RSVD[3:0]				RSVD	EDID_ROM_EN	EDID_RAM_EN	EDID_READ_ONLY
0x6423	0xA0	EDP_VIDEO_CTRL3[7:0]*	EDID_DEV_ADDR[6:0]							–

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Release to TPK Under NDA

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ADDRESS	RESET	NAME	MSB							LSB
0x6424	0xBB	EDP_VID_CLK_CTRL0[7:0]*	PCLK_RATE_MOD_1	–	PCLK_RATE_SEL_1[1:0]		PCLK_RATE_MOD_0	–	PCLK_RATE_SEL_0[1:0]	
0x6429	0x15	EDP_AUDIO_CTRL1[7:0]	DP_AUD_OUT_EN_0	–	–	RSVD[2:0]			RSVD[1:0]	
0x642D	0x15	EDP_AUDIO_CTRL5[7:0]	DP_AUD_OUT_EN_1	–	–	RSVD[2:0]			RSVD[1:0]	
0x6430	0x00	EDP_GEN_INT_ST0[7:0]	DP_RLMS3_INT	DP_RLMS2_INT	DP_RLMS1_INT	DP_RLMS0_INT	DPRX_INT	–	RSVD	RSVD
0x6433	0x00	EDP_GEN_INT_ST3[7:0]	RSVD	APB_ERR_M0_IST	–	–	–	–	–	–
0x6434	0x00	EDP_GEN_INT_EN0[7:0]	DP_RLMS3_IEN	DP_RLMS2_IEN	DP_RLMS1_IEN	DP_RLMS0_IEN	DPRX_IEN	–	RSVD	RSVD
0x6437	0x00	EDP_GEN_INT_EN3[7:0]	RSVD	APB_ERR_M0_IEN	–	–	–	–	–	–
0x6444	0x00	HPD_CTRL0[7:0]	–	–	–	–	HPD_IRQ_HO_DIS	HPD_IRQ	HPD_ST	HPD_MODE
0x6445	0xFF	HPD_CTRL1[7:0]	HPD_IRQ_TIME[7:0]							
0x6446	0x00	HPD_CTRL2[7:0]	–	–	–	–	–	HPD_IRQ_HO	HOT_PLUG_DET	DPRX_HPD
0x6447	0xDC	HPD_CTRL3[7:0]	HPD_IRQ_HO_TIME[7:0]							
0x64C0	0x01	APB_CTRL_M0_B0[7:0]	–	–	–	–	–	APB_TO_SEL_M0[2:0]		
0x64C2	0x00	APB_CTRL_M0_B2[7:0]	APB_ERR_IEN_M0[7:0]							
0x64C4	0x00	APB_STATUS_M0_B0[7:0]	APB_STATUS_M0[7:0]							
0x64C6	0x00	APB_STATUS_M0_B2[7:0]	APB_STATUS_ERR_M0[7:0]							
0x64C8	0x00	APB_ADRCTL_ERR_M0_B0[7:0]	APB_ADR_ERR_M0_L[7:0]							
0x64C9	0x00	APB_ADRCTL_ERR_M0_B1[7:0]	APB_ADR_ERR_M0_H[7:0]							
0x64CA	0x00	APB_ADRCTL_ERR_M0_B2[7:0]	–	–	–	APB_WR_ERR_M0	APB_STB_ERR_M0[3:0]			
0x64D0	0x01	DPCD_CTRL_M0_B0[7:0]	DPCD_ADDR_HI_M0_L[7:0]							
0x64D1	0x00	DPCD_CTRL_M0_B1[7:0]	–	–	–	–	DPCD_ADDR_HI_M0_H[3:0]			

PRELIMINARY

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ADDRESS	RESET	NAME	MSB							LSB
0x64D2	0x00	DPCD_CTRL_M0_B2[7:0]	–	–	–	–	–	–	DPCD_RDCLR_EN_M0	DPCD_APB_NOBLK_M0
EDID										
DPRX_HDCP_CRYPTO										
0x6800	0x02	HDCP1_CTRL[7:0]	–	–	–	–	–	HDCP1_RST	HDCP1_RPTR	HDCP1_EN
0x6801	0x00	HDCP1_STATUS[7:0]	HDCP1_AUTH_IN_PROGRESS	–	–	–	–	HDCP1_DS_CHG	HDCP1_DS_RDY	HDCP1_AUTH
0x6802	0x02	HDCP2_CTRL[7:0]	–	–	–	–	–	HDCP2_RST	HDCP2_RPTR	HDCP2_EN
0x6803	0x00	HDCP2_STATUS[7:0]	HDCP2_AUTH_IN_PROGRESS	–	–	HDCP2_STR_MGT_ERR	HDCP2_STR_MGT	HDCP2_DS_CHG	HDCP2_DS_RDY	HDCP2_AUTH
0x6804	0x03	HDCP_RPTR_DS_CFG_X[7:0]	–	–	–	–	–	RPTR_DS_ONE_RXID	RPTR_DS_HDCP2_EN	RPTR_DS_HDCP1_EN
0x6805	0x03	HDCP_RPTR_DS_CFG_Y[7:0]	–	–	–	–	–	–	RPTR_DS_HDCP2_EN	RPTR_DS_HDCP1_EN
0x6808	0x00	HDCP1_STATE[7:0]	HDCP1_STATE[7:0]							
0x6809	0x00	HDCP1_SUBSTATE[7:0]	HDCP1_SUBSTATE[7:0]							
0x680A	0x00	HDCP2_STATE[7:0]	HDCP2_STATE[7:0]							
0x680B	0x00	HDCP2_SUBSTATE[7:0]	HDCP2_SUBSTATE[7:0]							
DPRX_LINK										
0x7000	0x01	LINK_ENABLE[7:0]	–	–	–	–	–	–	–	LINK_ENABLE
0x7004	0x96	AUX_CLOCK_DIV_B0[7:0]	AUX_CLOCK_DIV_L[7:0]							
0x7005	0x00	AUX_CLOCK_DIV_B1[7:0]	–	–	–	–	–	–	AUX_CLOCK_DIV_H[1:0]	
0x7018	0x16	MISC_CONFIG_B0[7:0]	DISABLE_AUX_FILTER	ALPM_ENABLE	EDP_FUNCTION_ENABLE	MAX_DOWNSPREAD_CONFIG	BRANCH_SUPPORT_ENABLE	DISABLE_INACTIVE_COUNT	DEFER_LONG_I2C	MSA_DELAY_BYPASS
0x7019	0x01	MISC_CONFIG_B1[7:0]	–	–	–	–	PRESERVE_EVENT_INT	MSO_FUNCTION_EN	–	MST_FUNCTION_ENABLE
0x701C	0x14	DISPLAYPORT_VERSION[7:0]	DP_VERSION[7:0]							
0x7020	0x00	LINK_SERVICE_IRQ[7:0]	–	–	–	LINK_SERVICE_IRQ[4:0]				

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ADDRESS	RESET	NAME	MSB							LSB
0x7024	0x00	REQUEST_ERROR_COUNT[7:0]	REQUEST_ERROR_COUNT[7:0]							
0x7028	0x00	REQUEST_COUNT_L[7:0]	REQUEST_COUNT_L[7:0]							
0x7029	0x00	REQUEST_COUNT_H[7:0]	–	–	–	–	–	–	REQUEST_COUNT_H[1:0]	
0x702C	0x00	HPD_INTERRUPT[7:0]	–	–	–	–	–	–	RSVD	HPD_IRQ
0x702D	0x00	HPD_INTERRUPT_MASK[7:0]	–	HPD_INTERRUPT_MASK[6:0]						
0x7030	0x00	LANE_REMAP_B0[7:0]	REMAP_LANE_3[1:0]		REMAP_LANE_2[1:0]		REMAP_LANE_1[1:0]		REMAP_LANE_0[1:0]	
0x7031	0x00	LANE_REMAP_B1[7:0]	–	–	–	–	–	–	–	REMAP_ENABLE
0x7032	0x00	LANE_REMAP_B2[7:0]	–	–	–	–	INVERT_LANE_3	INVERT_LANE_2	INVERT_LANE_1	INVERT_LANE_0
0x7054	0x00	VIDEO_INPUT_RESET[7:0]	–	–	–	–	–	–	LINK_RESET	VIDEO_INPUT_RESET
0x7058	0x00	EDP_IGNORE_MSA[7:0]	–	–	–	–	–	–	–	EDP_IGNORE_MSA
0x7070	0x04	MAX_LANE_COUNT[7:0]	MAX_LANE_COUNT[7:0]							
0x7074	0x1E	MAX_LINK_RATE[7:0]	MAX_LINK_RATE[7:0]							
0x7075	0x00	MIN_LINK_RATE[7:0]	MIN_LINK_RATE[7:0]							
0x70A0	0x04	AUX_RD_INTERVAL[7:0]	–	AUX_RD_INTERVAL[6:0]						
0x70A4	0x38	I2C_SPEED_CAPABILITY[7:0]	–	–	I2C_SPEED_CAPABILITY[5:0]					
0x70A5	0x08	I2C_SCL_TIMEOUT_SEL[7:0]	–	–	–	–	I2C_SCL_TIMEOUT_SEL[3:0]			
0x7300	0x01	FEC_ENABLE[7:0]	–	–	–	–	–	–	FEC_BYPASS_ERROR_CORRECTION	FEC_SUPPORT
0x7301	0x00	FEC_CLEAR_ERROR[7:0]	–	–	–	–	–	–	FEC_BUFFER_RESET	FEC_CLR_ERROR_CNT
0x7302	0x00	FEC_PM_CLR[7:0]	–	–	–	–	–	–	MISSING_PM_ERRFL_CLR	UNEXP_PM_ERRFL_CLR

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0x7304	0x00	FEC_RUNNING[7:0]	–	–	–	–	–	–	–	FEC_RUNNING
0x7306	0x00	FEC_PM_ERRCTRL[7:0]	–	–	–	–	–	–	FEC_BADPMTRAN_EN	FEC_PMFIX_DIS
0x730C	0x00	FEC_FALSE_PM_ERR_CTRL[7:0]	–	–	–	FEC_PM_ERR_LANESEL	–	–	–	FEC_PM_ERR_IRQ_EN
0x730D	0x00	FEC_UNEXP_PM_ERR[7:0]	FEC_UNEXP_PM_ERR_FLG	–	–	–	FEC_UNEXP_PM_ERR_CNT[3:0]			
0x730E	0x00	FEC_MISSING_PM_ERR[7:0]	FEC_MISSING_PM_ERR_FLG	–	–	–	FEC_MISSING_PM_ERR_CNT[3:0]			
0x7400	0x00	DPCD_LINK_BW_SET[7:0]	DPCD_LINK_BW_SET[7:0]							
0x7404	0x00	DPCD_LANE_COUNT_SET[7:0]	–	–	–	DPCD_LANE_COUNT_SET[4:0]				
0x7408	0x01	DPCD_ENHANCED_FRAME_EN[7:0]	–	–	–	–	–	–	–	DPCD_ENHANCED_FRAME_EN
0x740C	0x00	DPCD_TRAINING_PATTERN_SET[7:0]	–	–	–	–	–	DPCD_TRAINING_PATTERN_SET[2:0]		
0x7410	0x00	DPCD_LINK_QUAL_PAT_SET_B0[7:0]	–	DPCD_LINK_QUAL_LANE1_SET[2:0]			–	DPCD_LINK_QUAL_LANE0_SET[2:0]		
0x7411	0x00	DPCD_LINK_QUAL_PAT_SET_B1[7:0]	–	DPCD_LINK_QUAL_LANE3_SET[2:0]			–	DPCD_LINK_QUAL_LANE2_SET[2:0]		
0x7418	0x01	DPCD_SCRAMBLING_DISABLE[7:0]	–	–	–	–	–	–	–	DPCD_SCRAMBLING_DISABLE
0x741C	0x00	DPCD_SYMBOL_ERROR_COUNT_SELECT[7:0]	–	–	–	–	–	–	DPCD_SYMBOL_ERROR_COUNT_SELECT[1:0]	
0x7420	0x00	DPCD_TRAINING_LANE_0_SET[7:0]	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
0x7424	0x00	DPCD_TRAINING_LANE_1_SET[7:0]	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	

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ADDRESS	RESET	NAME	MSB							LSB
0x7428	0x00	DPCD_TRAINING_LANE_2_SET[7:0]	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
0x742C	0x00	DPCD_TRAINING_LANE_3_SET[7:0]	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
0x7430	0x00	DPCD_DOWNSPREAD_CONTROL[7:0]	–	–	–	–	–	–	–	DPCD_DOWNSPREAD_CONTROL
0x7434	0x01	DPCD_MAIN_LINK_CHANNEL_CODING_SET[7:0]	–	–	–	–	–	–	–	DPCD_MAIN_LINK_CHANNEL_CODING_SET
0x7438	0x02	DPCD_SET_POWER_STATE[7:0]	–	–	–	–	–	DPCD_SET_POWER_STATE[2:0]		
0x743C	0x00	DPCD_LANE01_STATUS_B0[7:0]	–	LANE1_SYMBOL_LOCKED	LANE1_CHANNEL_EQ_DONE	LANE1_CLOCK_RECOVERY_DONE	–	LANE0_SYMBOL_LOCKED	LANE0_CHANNEL_EQ_DONE	LANE0_CLOCK_RECOVERY_DONE
0x743D	0x00	DPCD_LANE01_STATUS_B1[7:0]	–	–	–	–	–	–	LANE1_LANE_ALIGNED	LANE0_LANE_ALIGNED
0x743E	0x00	DPCD_LANE01_STATUS_B2[7:0]	–	–	–	–	–	–	LANE1_TRAINING_LOST	LANE0_TRAINING_LOST
0x7440	0x00	DPCD_LANE23_STATUS_B0[7:0]	–	LANE3_SYMBOL_LOCKED	LANE3_CHANNEL_EQ_DONE	LANE3_CLOCK_RECOVERY_DONE	–	LANE2_SYMBOL_LOCKED	LANE2_CHANNEL_EQ_DONE	LANE2_CLOCK_RECOVERY_DONE
0x7441	0x00	DPCD_LANE23_STATUS_B1[7:0]	–	–	–	–	–	–	LANE3_LANE_ALIGNED	LANE2_LANE_ALIGNED
0x7442	0x00	DPCD_LANE23_STATUS_B2[7:0]	–	–	–	–	–	–	LANE3_TRAINING_LOST	LANE2_TRAINING_LOST
0x7454	0x00	LANE0_TRAINING_LOST_CAUSE[7:0]	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
0x7455	0x00	LANE1_TRAINING_LOST_CAUSE[7:0]	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE

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ADDRESS	RESET	NAME	MSB							LSB
0x7456	0x00	LANE2_TRAINING_LOST_CAUSE[7:0]	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
0x7457	0x00	LANE3_TRAINING_LOST_CAUSE[7:0]	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
0x7478	0x00	I2C_SPEED_CONTROL_SELECT[7:0]	–	–	I2C_SPEED_CAPABILITY[5:0]					
0x747C	0x00	MSA_TIMING_IGNORE[7:0]	–	–	–	–	–	–	–	MSA_TIMING_IGNORE
0x7480	0x00	EDP_CONFIGURATION_SET[7:0]	RSVD	–	–	–	–	–	RSVD	ALT_SR_ENABLE
0x748C	0x00	MST_MODE_CTRL[7:0]	–	–	–	–	–	UPSTREAM_IS_SRC	UP_REQ_EN	MST_EN
0x7490	0x00	DPCD_SER_COUNT_LANE0_B0[7:0]	SER_COUNT_LANE0_B0[7:0]							
0x7491	0x00	DPCD_SER_COUNT_LANE0_B1[7:0]	SER_COUNT_LANE0_B1[7:0]							
0x7494	0x00	DPCD_SER_COUNT_LANE1_B0[7:0]	SER_COUNT_LANE1_B0[7:0]							
0x7495	0x00	DPCD_SER_COUNT_LANE1_B1[7:0]	SER_COUNT_LANE1_B1[7:0]							
0x7498	0x00	DPCD_SER_COUNT_LANE2_B0[7:0]	SER_COUNT_LANE2_B0[7:0]							
0x7499	0x00	DPCD_SER_COUNT_LANE2_B1[7:0]	SER_COUNT_LANE2_B1[7:0]							
0x749C	0x00	DPCD_SER_COUNT_LANE3_B0[7:0]	SER_COUNT_LANE3_B0[7:0]							
0x749D	0x00	DPCD_SER_COUNT_LANE3_B1[7:0]	SER_COUNT_LANE3_B1[7:0]							
0x7500	0x00	MSA_HRES_B0[7:0]	MSA_HRES_B0[7:0]							
0x7501	0x00	MSA_HRES_B1[7:0]	MSA_HRES_B1[7:0]							
0x7504	0x00	MSA_HSPOL[7:0]	–	–	–	–	–	–	–	MSA_HSPOL
0x7508	0x00	MSA_HSWIDTH_B0[7:0]	MSA_HSWIDTH_B0[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x7509	0x00	MSA_HSWIDTH_B1[7:0]	–	MSA_HSWIDTH_B1[6:0]						
0x750C	0x00	MSA_HSTART_B0[7:0]	MSA_HSTART_B0[7:0]							
0x750D	0x00	MSA_HSTART_B1[7:0]	MSA_HSTART_B1[7:0]							
0x7510	0x00	MSA_HTOTAL_B0[7:0]	MSA_HTOTAL_B0[7:0]							
0x7511	0x00	MSA_HTOTAL_B1[7:0]	MSA_HTOTAL_B1[7:0]							
0x7514	0x00	MSA_VRES_B0[7:0]	MSA_VRES_B0[7:0]							
0x7515	0x00	MSA_VRES_B1[7:0]	MSA_VRES_B1[7:0]							
0x7518	0x00	MSA_VSPOL[7:0]	–	–	–	–	–	–	–	MSA_VSPOL
0x751C	0x00	MSA_VSWIDTH_B0[7:0]	MSA_VSWIDTH_B0[7:0]							
0x751D	0x00	MSA_VSWIDTH_B1[7:0]	–	MSA_VSWIDTH_B1[6:0]						
0x7520	0x00	MSA_VSTART_B0[7:0]	MSA_VSTART_B0[7:0]							
0x7521	0x00	MSA_VSTART_B1[7:0]	MSA_VSTART_B1[7:0]							
0x7524	0x00	MSA_VTOTAL_B0[7:0]	MSA_VTOTAL_B0[7:0]							
0x7525	0x00	MSA_VTOTAL_B1[7:0]	MSA_VTOTAL_B1[7:0]							
0x7528	0x00	MSA_MISC0[7:0]	MSA_COLOR_DEPTH[2:0]			MSA_YCBCR_COLOR	MSA_DYNAMIC_RANGE	MSA_COMP_FORMAT[1:0]		MSA_CLOCKING_MODE
0x752C	0x00	MSA_MISC1[7:0]	MSA_Y_ONLY	–	–	–	–	MSA_STEREO_VIDEO[1:0]		MSA_INTERLACED_EVEN
0x7530	0x00	MSA_MVID_B0[7:0]	MSA_MVID_B0[7:0]							
0x7531	0x00	MSA_MVID_B1[7:0]	MSA_MVID_B1[7:0]							
0x7532	0x00	MSA_MVID_B2[7:0]	MSA_MVID_B2[7:0]							
0x7534	0x00	MSA_NVID_B0[7:0]	MSA_NVID_B0[7:0]							
0x7535	0x00	MSA_NVID_B1[7:0]	MSA_NVID_B1[7:0]							
0x7536	0x00	MSA_NVID_B2[7:0]	MSA_NVID_B2[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x7538	0x00	MSA_VBID[7:0]	–	MSA_VBID_COMPRESSED_STREAM	MSA_VBID_HDCP_SYNC_DET	MSA_VBID_AUDIO_MUTE	MSA_VBID_NO_VIDEO	MSA_VBID_INTERLACED	MSA_VBID_FIELD_ID	MSA_VBID_VERT_BLANK
0x7540	0x00	MSA_VIRTUAL_SINK_SELECT[7:0]	–	–	–	–	–	–	MSA_VIRTUAL_SINK_SELECT[1:0]	
0x7541	0x00	MSA_DSC_TS_SELECT[7:0]	–	–	–	–	–	–	–	MSA_DSC_TS_SELECT
0x7543	0x00	MSA_UPDATE[7:0]	–	–	–	–	–	–	VS1_MODE_UPDATE	VS0_MODE_UPDATE
0x7544	0x00	VS0_MSA_HTOTAL_B0[7:0]	VS0_MSA_HTOTAL_B0[7:0]							
0x7545	0x00	VS0_MSA_HTOTAL_B1[7:0]	VS0_MSA_HTOTAL_B1[7:0]							
0x7546	0x00	VS0_MSA_HRES_B0[7:0]	VS0_MSA_HRES_B0[7:0]							
0x7547	0x00	VS0_MSA_HRES_B1[7:0]	VS0_MSA_HRES_B1[7:0]							
0x7548	0x00	VS0_MSA_HSTART_B0[7:0]	VS0_MSA_HSTART_B0[7:0]							
0x7549	0x00	VS0_MSA_HSTART_B1[7:0]	VS0_MSA_HSTART_B1[7:0]							
0x754A	0x00	VS0_MSA_HSWIDTH_B0[7:0]	VS0_MSA_HSWIDTH_B0[7:0]							
0x754B	0x00	VS0_MSA_HSWIDTH_B1[7:0]	VS0_MSA_HSPOL	VS0_MSA_HSWIDTH_B1[6:0]						
0x754C	0x00	VS0_MSA_VTOTAL_B0[7:0]	VS0_MSA_VTOTAL_B0[7:0]							
0x754D	0x00	VS0_MSA_VTOTAL_B1[7:0]	VS0_MSA_VTOTAL_B1[7:0]							
0x754E	0x00	VS0_MSA_VRES_B0[7:0]	VS0_MSA_VRES_B0[7:0]							
0x754F	0x00	VS0_MSA_VRES_B1[7:0]	VS0_MSA_VRES_B1[7:0]							
0x7550	0x00	VS0_MSA_VSTART_B0[7:0]	VS0_MSA_VSTART_B0[7:0]							
0x7551	0x00	VS0_MSA_VSTART_B1[7:0]	VS0_MSA_VSTART_B1[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x7552	0x00	VS0_MSA_VSWIDTH_B0[7:0]	VS0_MSA_VSWIDTH_B0[7:0]							
0x7553	0x00	VS0_MSA_VSWIDTH_B1[7:0]	VS0_MSA_VSPOL	VS0_MSA_VSWIDTH_B1[6:0]						
0x7554	0x00	VS0_MSA_MISC0[7:0]	VS0_MSA_COLOR_DEPTH[2:0]			VS0_MSA_YCBCR_COLOR	VS0_MSA_DYNAMIC_RANGE	VS0_MSA_COMP_FORMAT[1:0]		VS0_MSA_CLOCKING_MODE
0x7555	0x00	VS0_MSA_MISC1[7:0]	VS0_MSA_Y_ONLY	–	–	–	–	VS0_MSA_STEREO_VIDEO[1:0]		VS0_MSA_INTERLACED_EVEN
0x7556	0x00	VS0_VBID[7:0]	–	VS0_VBID_COMPRESSED_STREAM	VS0_VBID_HDCP_SYNC_DET	VS0_VBID_AUDIO_MUTE	VS0_VBID_NO_VIDEO	VS0_VBID_INTERLACED	VS0_VBID_FIELD_ID	VS0_VBID_VERT_BLANK
0x7558	0x00	VS0_MSA_MVID_B0[7:0]	VS0_MSA_MVID_B0[7:0]							
0x7559	0x00	VS0_MSA_MVID_B1[7:0]	VS0_MSA_MVID_B1[7:0]							
0x755A	0x00	VS0_MSA_MVID_B2[7:0]	VS0_MSA_MVID_B2[7:0]							
0x755C	0x00	VS0_MSA_NVID_B0[7:0]	VS0_MSA_NVID_B0[7:0]							
0x755D	0x00	VS0_MSA_NVID_B1[7:0]	VS0_MSA_NVID_B1[7:0]							
0x755E	0x00	VS0_MSA_NVID_B2[7:0]	VS0_MSA_NVID_B2[7:0]							
0x7560	0x00	VS0_MSA_HRES_DSC_B0[7:0]	VS0_MSA_HRES_DSC_B0[7:0]							
0x7561	0x00	VS0_MSA_HRES_DSC_B1[7:0]	VS0_MSA_HRES_DSC_B1[7:0]							
0x7564	0x00	VS0_MSA_MVID_DSC_B0[7:0]	VS0_MSA_MVID_DSC_B0[7:0]							
0x7565	0x00	VS0_MSA_MVID_DSC_B1[7:0]	VS0_MSA_MVID_DSC_B1[7:0]							
0x7566	0x00	VS0_MSA_MVID_DSC_B2[7:0]	VS0_MSA_MVID_DSC_B2[7:0]							
0x7568	0x00	VS0_MSA_NVID_DSC_B0[7:0]	VS0_MSA_NVID_DSC_B0[7:0]							
0x7569	0x00	VS0_MSA_NVID_DSC_B1[7:0]	VS0_MSA_NVID_DSC_B1[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x756A	0x00	VS0_MSA_NVID_DSC_B2[7:0]	VS0_MSA_NVID_DSC_B2[7:0]							
0x7574	0x00	VS1_MSA_HTOTAL_B0[7:0]	VS1_MSA_HTOTAL_B0[7:0]							
0x7575	0x00	VS1_MSA_HTOTAL_B1[7:0]	VS1_MSA_HTOTAL_B1[7:0]							
0x7576	0x00	VS1_MSA_HRES_B0[7:0]	VS1_MSA_HRES_B0[7:0]							
0x7577	0x00	VS1_MSA_HRES_B1[7:0]	VS1_MSA_HRES_B1[7:0]							
0x7578	0x00	VS1_MSA_HSTART_B0[7:0]	VS1_MSA_HSTART_B0[7:0]							
0x7579	0x00	VS1_MSA_HSTART_B1[7:0]	VS1_MSA_HSTART_B1[7:0]							
0x757A	0x00	VS1_MSA_HSWIDTH_B0[7:0]	VS1_MSA_HSWIDTH_B0[7:0]							
0x757B	0x00	VS1_MSA_HSWIDTH_B1[7:0]	VS1_MSA_HSPOL	VS1_MSA_HSWIDTH_B1[6:0]						
0x757C	0x00	VS1_MSA_VTOTAL_B0[7:0]	VS1_MSA_VTOTAL_B0[7:0]							
0x757D	0x00	VS1_MSA_VTOTAL_B1[7:0]	VS1_MSA_VTOTAL_B1[7:0]							
0x757E	0x00	VS1_MSA_VRES_B0[7:0]	VS1_MSA_VRES_B0[7:0]							
0x757F	0x00	VS1_MSA_VRES_B1[7:0]	VS1_MSA_VRES_B1[7:0]							
0x7580	0x00	VS1_MSA_VSTART_B0[7:0]	VS1_MSA_VSTART_B0[7:0]							
0x7581	0x00	VS1_MSA_VSTART_B1[7:0]	VS1_MSA_VSTART_B1[7:0]							
0x7582	0x00	VS1_MSA_VSWIDTH_B0[7:0]	VS1_MSA_VSWIDTH_B0[7:0]							
0x7583	0x00	VS1_MSA_VSWIDTH_B1[7:0]	VS1_MSA_VSPOL	VS1_MSA_VSWIDTH_B1[6:0]						
0x7584	0x00	VS1_MSA_MISC0[7:0]	VS1_MSA_COLOR_DEPTH[2:0]			VS1_MSA_YCBCR_COLOR	VS1_MSA_DYNAMIC_RANGE	VS1_MSA_COMP_FORMAT[1:0]		VS1_MSA_CLOCKING_MODE

PRELIMINARY

Analog Devices Company Confidential, Provided to TPK_Customers Under NDA

Release to TPK under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x7585	0x00	VS1_MSA_MISC1[7:0]	VS1_MSA_Y_ONLY	–	–	–	–	VS1_MSA_STEREO_VIDEO[1:0]		VS1_MSA_INTERLACED_EVEN
0x7586	0x00	VS1_VBID[7:0]	–	VS1_VBID_COMPRESSED_STREAM	VS1_VBID_HDCP_SYNC_DET	VS1_VBID_AUDIO_MUTE	VS1_VBID_NO_VIDEO	VS1_VBID_INTERLACED	VS1_VBID_FIELD_ID	VS1_VBID_VERT_BLANK
0x7588	0x00	VS1_MSA_MVID_B0[7:0]	VS1_MSA_MVID_B0[7:0]							
0x7589	0x00	VS1_MSA_MVID_B1[7:0]	VS1_MSA_MVID_B1[7:0]							
0x758A	0x00	VS1_MSA_MVID_B2[7:0]	VS1_MSA_MVID_B2[7:0]							
0x758C	0x00	VS1_MSA_NVID_B0[7:0]	VS1_MSA_NVID_B0[7:0]							
0x758D	0x00	VS1_MSA_NVID_B1[7:0]	VS1_MSA_NVID_B1[7:0]							
0x758E	0x00	VS1_MSA_NVID_B2[7:0]	VS1_MSA_NVID_B2[7:0]							
0x7590	0x00	VS1_MSA_HRES_DSC_B0[7:0]	VS1_MSA_HRES_DSC_B0[7:0]							
0x7591	0x00	VS1_MSA_HRES_DSC_B1[7:0]	VS1_MSA_HRES_DSC_B1[7:0]							
0x7594	0x00	VS1_MSA_MVID_DSC_B0[7:0]	VS1_MSA_MVID_DSC_B0[7:0]							
0x7595	0x00	VS1_MSA_MVID_DSC_B1[7:0]	VS1_MSA_MVID_DSC_B1[7:0]							
0x7596	0x00	VS1_MSA_MVID_DSC_B2[7:0]	VS1_MSA_MVID_DSC_B2[7:0]							
0x7598	0x00	VS1_MSA_NVID_DSC_B0[7:0]	VS1_MSA_NVID_DSC_B0[7:0]							
0x7599	0x00	VS1_MSA_NVID_DSC_B1[7:0]	VS1_MSA_NVID_DSC_B1[7:0]							
0x759A	0x00	VS1_MSA_NVID_DSC_B2[7:0]	VS1_MSA_NVID_DSC_B2[7:0]							
0x7600	0x00	HCDP_ENABLE[7:0]	–	–	–	–	–	–	–	HDCP_ENABLE
0x7602	0x04	HCDP_AUTO_ENCRYPT[7:0]	–	–	–	–	–	HDCP_AUTO_ENCRYPT	–	–
0x7604	0x00	HCDP_MODE_SELECT[7:0]	–	–	–	–	–	–	HDCP_MODE_SELECT[1:0]	

PRELIMINARY

Analog Devices Company Confidential Provided to TPK under NDA Prerelease_2_Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x7654	0x00	HDCP_STREAM_CIPHER_ENABLE[7:0]	–	–	–	–	–	–	–	HDCP_STREAM_CIPHER_ENABLE
0x7690	0x00	HDCP_DECRYPT_STATUS[7:0]	–	–	–	–	–	–	HDCP_DECRYPT_READY	HDCP_DECRYPT_ACTIVE
0x7694	0x00	HDCP_LINK_INTEGRITY[7:0]	–	–	–	–	–	–	–	HDCP_LINK_INTEGRITY_FAIL
0x7900	0x00	MST_SST_PORT_SELECT[7:0]	–	–	–	–	–	–	MST_SST_PORT_SELECT[1:0]	
0x7901	0x00	DSC_DPCD_SELECT[7:0]	–	–	–	–	–	–	DSC_DPCD_SELECT[1:0]	
0x7902	0x00	CRC_DPCD_SELECT[7:0]	–	–	–	–	–	–	CRC_DPCD_SELECT[1:0]	
0x7904	0x00	MST_PAYLOAD_ID_0[7:0]	–	MST_PAYLOAD_ID_0[6:0]						
0x7908	0x00	MST_PAYLOAD_ID_1[7:0]	–	MST_PAYLOAD_ID_1[6:0]						
0x790C	0x00	MST_PAYLOAD_ID_2[7:0]	–	MST_PAYLOAD_ID_2[6:0]						
0x7910	0x00	MST_PAYLOAD_ID_3[7:0]	–	MST_PAYLOAD_ID_3[6:0]						
0x7934	0x00	MST_CLEAR_PAYLOAD_ID_TABLE[7:0]	–	–	–	–	–	–	–	MST_CLEAR_PAYLOAD_ID_TABLE
0x7A00	0x01	MST_VS0_ENABLE[7:0]	–	–	–	–	–	–	–	VS_ENABLE
0x7A04	0x01	MST_VS0_USER_PIXEL_WIDTH[7:0]	–	–	–	–	–	USER_PIXEL_WIDTH[2:0]		
0x7A08	0x00	MST_VS0_SWAP_CBCR[7:0]	–	–	–	–	CRC_MASK_SWAP	CRC_COMP_SWAP	PIX_MASK_SWAP	SWAP_CBCR
0x7A0C	0x02	MST_VS0_USER_FIFO_RESET[7:0]	DISABLE_VB_FAULT_RESET	VB_FRAME_RESET_PEND_SEL	BS_FRAME_RESET_SEL	DISABLE_FRAME_RESET	–	DISABLE_LINE_RESET_FIFO	DISABLE_HS_LINE_RESET	DISABLE_LINE_RESET
0x7A10	0x00	MST_VS0_VIDEO_FIFO_OVERFLOW[7:0]	–	–	–	–	–	–	–	VIDEO_FIFO_OVERFLOW
0x7A14	0x00	MST_VS0_DTG_ENABLE[7:0]	–	–	–	–	–	–	–	DTG_ENABLE

PRELIMINARY

Released to TPK Under NDA

Analog Devices Company Confidential, Provided to TPK Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x7A18	0x81	MST_VS0_DTG_MODE[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	–	RSVD	DMA_ENABLE
0x7A24	0x3F	MST_VS0_DMA_VSYNC_B0[7:0]	DMA_VSYNC_PULSE_WIDTH[7:0]							
0x7A26	0xFF	MST_VS0_DMA_VSYNC_B2[7:0]	DMA_VSYNC_FRONT_PORCH_L[7:0]							
0x7A27	0x01	MST_VS0_DMA_VSYNC_B3[7:0]	–	–	–	–	DMA_VSYNC_FRONT_PORCH_H[3:0]			
0x7A28	0x0F	MST_VS0_DMA_HSYNC_B0[7:0]	DMA_HSYNC_PULSE_WIDTH_L[7:0]							
0x7A29	0x00	MST_VS0_DMA_HSYNC_B1[7:0]	–	–	–	–	DMA_HSYNC_PULSE_WIDTH_H[3:0]			
0x7A2A	0x0F	MST_VS0_DMA_HSYNC_B2[7:0]	DMA_HSYNC_FRONT_PORCH_L[7:0]							
0x7A2B	0x00	MST_VS0_DMA_HSYNC_B3[7:0]	–	–	–	–	DMA_HSYNC_FRONT_PORCH_H[3:0]			
0x7A38	0x00	MST_VS0_RED_CRC_B0[7:0]	RED_CRC_B0[7:0]							
0x7A39	0x00	MST_VS0_RED_CRC_B1[7:0]	RED_CRC_B1[7:0]							
0x7A3B	0x00	MST_VS0_RED_CRC_B3[7:0]	CRC_UPDATED	–	–	–	–	–	–	–
0x7A3C	0x00	MST_VS0_GRN_BLU_CRC_B0[7:0]	BLU_CRC_B0[7:0]							
0x7A3D	0x00	MST_VS0_GRN_BLU_CRC_B1[7:0]	BLU_CRC_B1[7:0]							
0x7A3E	0x00	MST_VS0_GRN_BLU_CRC_B2[7:0]	GRN_CRC_B0[7:0]							
0x7A3F	0x00	MST_VS0_GRN_BLU_CRC_B3[7:0]	GRN_CRC_B1[7:0]							
0x7A40	0x00	MST_VS0_MSA_IGNORE_HRES_B0[7:0]	MSA_IGNORE_HRES_B0[7:0]							
0x7A41	0x00	MST_VS0_MSA_IGNORE_HRES_B1[7:0]	MSA_IGNORE_HRES_B1[7:0]							

PRELIMINARY

Released to TPK Under NDA

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MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x7A44	0x80	MST_VS0_MSA_IGNORE_COLOR[7:0]	MSA_IGNORE_COLOR_MODE_EN	–	–	MSA_IGNORE_COLOR_MODE[4:0]				
0x7A45	0x02	MST_VS0_DSC_MISC[7:0]	DSC_VBID_OVR	–	DSC_PIX_REM_OVR[1:0]		–	–	DSC_TS_AUTO_MDIV3	DSC_TS_USE_MDIV3
0x7A48	0x00	MST_VS0_PPS_CHUNK_SIZE_OVR_B0[7:0]	PPS_CHUNK_SIZE_OVR_B0[7:0]							
0x7A49	0x00	MST_VS0_PPS_CHUNK_SIZE_OVR_B1[7:0]	PPS_CHUNK_SIZE_OVR_B1[7:0]							
0x7A4A	0x00	MST_VS0_PPS_SLICE_WIDTH_OVR_B0[7:0]	PPS_SLICE_WIDTH_OVR_B0[7:0]							
0x7A4B	0x00	MST_VS0_PPS_SLICE_WIDTH_OVR_B1[7:0]	PPS_SLICE_WIDTH_OVR_B1[7:0]							
0x7A4C	0x00	MST_VS0_PPS_BITS_PER_PIX_OVR_B0[7:0]	PPS_BITS_PER_PIX_OVR_B0[7:0]							
0x7A4D	0x00	MST_VS0_PPS_BITS_PER_PIX_OVR_B1[7:0]	PPS_BITS_PER_PIX_OVR_B1[7:0]							
0x7A50	0x01	MST_VS0_DSC_SUPPORT[7:0]	–	–	–	–	–	–	–	DSC_SUPPORT
0x7A51	0x11	MST_VS0_DSC_VERSION[7:0]	DSC_VERSION[7:0]							
0x7A71	0x00	MST_VS0_DSC_STATUS_B1[7:0]	–	–	–	–	–	DSC_CHUNK_SIZE_ERROR	DSC_ACTIVE	DSC_ENABLE
0x7A73	0x00	MST_VS0_DSC_CRC_STATUS[7:0]	–	–	–	–	–	–	DSC_PIX_CRC_VAL	DSC_CRC_VAL
0x7A74	0x00	MST_VS0_DSC_CRC0_B0[7:0]	DSC_CRC0_B0[7:0]							
0x7A75	0x00	MST_VS0_DSC_CRC0_B1[7:0]	DSC_CRC0_B1[7:0]							
0x7A76	0x00	MST_VS0_DSC_CRC1_B0[7:0]	DSC_CRC1_B0[7:0]							

PRELIMINARY

Release to TPK under NDA

Analog Devices Company Confidential, Provided ONLY Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x7A77	0x00	MST_VS0_DSC_CRC1_B1[7:0]	DSC_CRC1_B1[7:0]							
0x7A78	0x00	MST_VS0_DSC_CRC2_B0[7:0]	DSC_CRC2_B0[7:0]							
0x7A79	0x00	MST_VS0_DSC_CRC2_B1[7:0]	DSC_CRC2_B1[7:0]							
0x7A7A	0x00	MST_VS0_DSC_PIX_CRC0_B0[7:0]	DSC_PIX_CRC0_B0[7:0]							
0x7A7B	0x00	MST_VS0_DSC_PIX_CRC0_B1[7:0]	DSC_PIX_CRC0_B1[7:0]							
0x7A7C	0x00	MST_VS0_DSC_PIX_CRC1_B0[7:0]	DSC_PIX_CRC1_B0[7:0]							
0x7A7D	0x00	MST_VS0_DSC_PIX_CRC1_B1[7:0]	DSC_PIX_CRC1_B1[7:0]							
0x7A7E	0x00	MST_VS0_DSC_PIX_CRC2_B0[7:0]	DSC_PIX_CRC2_B0[7:0]							
0x7A7F	0x00	MST_VS0_DSC_PIX_CRC2_B1[7:0]	DSC_PIX_CRC2_B1[7:0]							
0x7A80	0x01	MST_VS0_SECONDARY_ENABLE[7:0]	–	–	–	–	–	–	–	SECONDARY_ENABLE
0x7A84	0x01	MST_VS0_AUDIO_MUTE[7:0]	–	–	–	–	–	–	–	AUDIO_MUTE
0x7A8C	0x00	MST_VS0_AUDIO_SAMPLE_RES[7:0]	–	–	AUDIO_SAMPLE_RES[5:0]					
0x7A90	0x00	MST_VS0_AUDIO_CHANNEL_COUNT[7:0]	–	–	–	–	AUDIO_CHANNEL_COUNT[3:0]			
0x7A98	0x01	MST_VS0_AUDIO_OUTPUT_SELECT[7:0]	–	–	–	–	–	–	RSVD	RSVD
0x7A9C	0x00	MST_VS0_AUDIO_CHANNEL_MAP_B0[7:0]	–	CHANNEL_1_MAP[2:0]			–	CHANNEL_0_MAP[2:0]		
0x7A9D	0x00	MST_VS0_AUDIO_CHANNEL_MAP_B1[7:0]	–	CHANNEL_3_MAP[2:0]			–	CHANNEL_2_MAP[2:0]		

PRELIMINARY

Release to TPK under NDA

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MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB						LSB
0x7A9E	0x00	MST_VS0_AUDIO_CHANNEL_MAP_B2[7:0]	–	CHANNEL_5_MAP[2:0]			–	CHANNEL_4_MAP[2:0]	
0x7A9F	0x00	MST_VS0_AUDIO_CHANNEL_MAP_B3[7:0]	–	CHANNEL_7_MAP[2:0]			–	CHANNEL_6_MAP[2:0]	
0x7AA0	0x00	MST_VS0_MAUD_B0[7:0]	MAUD_B0[7:0]						
0x7AA1	0x00	MST_VS0_MAUD_B1[7:0]	MAUD_B1[7:0]						
0x7AA2	0x00	MST_VS0_MAUD_B2[7:0]	MAUD_B2[7:0]						
0x7AA4	0x00	MST_VS0_NAUD_B0[7:0]	NAUD_B0[7:0]						
0x7AA5	0x00	MST_VS0_NAUD_B1[7:0]	NAUD_B1[7:0]						
0x7AA6	0x00	MST_VS0_NAUD_B2[7:0]	NAUD_B2[7:0]						
0x7AB8	0x00	MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_0[7:0]	AUDIO_CHANNEL_STATUS_FIELD_0[7:0]						
0x7ABC	0x00	MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_1[7:0]	AUDIO_CHANNEL_STATUS_FIELD_1[7:0]						
0x7AC0	0x00	MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_2[7:0]	AUDIO_CHANNEL_STATUS_FIELD_2[7:0]						
0x7AC4	0x00	MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_3[7:0]	AUDIO_CHANNEL_STATUS_FIELD_3[7:0]						
0x7AC8	0x00	MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_4[7:0]	AUDIO_CHANNEL_STATUS_FIELD_4[7:0]						
0x7ACC	0x00	MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_5[7:0]	AUDIO_CHANNEL_STATUS_FIELD_5[7:0]						
0x7AD0	0x00	MST_VS0_AUDIO_CHANNEL_NUMBER_0_1[7:0]	CHANNEL_NUMBER_1[3:0]					CHANNEL_NUMBER_0[3:0]	

PRELIMINARY

Release to TPK under NDA

Analog Device Company Confidential, Provided to GL2_Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x7AD4	0x00	MST_VS0_AUDIO_CHANNEL_NUMBER_2_3[7:0]	CHANNEL_NUMBER_3[3:0]				CHANNEL_NUMBER_2[3:0]			
0x7AD8	0x00	MST_VS0_AUDIO_CHANNEL_NUMBER_4_5[7:0]	CHANNEL_NUMBER_5[3:0]				CHANNEL_NUMBER_4[3:0]			
0x7ADC	0x00	MST_VS0_AUDIO_CHANNEL_NUMBER_6_7[7:0]	CHANNEL_NUMBER_7[3:0]				CHANNEL_NUMBER_6[3:0]			
0x7AE4	0x00	MST_VS0_DSC_BUFFER_RDATA[7:0]	DSC_PPS_RDATA[7:0]							
0x7AE8	0x02	MST_VS0_AUDIO_PACKET_DEPTH[7:0]	–	–	–	–	–	–	AUDIO_PACKET_DEPTH[1:0]	
0x7B00	0x00	MST_VS1_ENABLE[7:0]	–	–	–	–	–	–	–	VS_ENABLE
0x7B04	0x01	MST_VS1_USER_PIXEL_WIDTH[7:0]	–	–	–	–	–	USER_PIXEL_WIDTH[2:0]		
0x7B08	0x00	MST_VS1_SWAP_CBCR[7:0]	–	–	–	–	CRC_MASK_SWAP	CRC_COMP_SWAP	PIX_MASK_SWAP	SWAP_CBCR
0x7B0C	0x02	MST_VS1_USER_FIFO_RESET[7:0]	DISABLE_VB_FAULT_RESET	VB_FRAME_RESET_PEND_SEL	BS_FRAME_RESET_SEL	DISABLE_FRAMEE_RESET	–	DISABLE_LINE_RESET_FIFO	DISABLE_HS_LINE_RESET	DISABLE_LINE_RESET
0x7B10	0x00	MST_VS1_VIDEO_FIFO_OVERFLOW[7:0]	–	–	–	–	–	–	–	VIDEO_FIFO_OVERFLOW
0x7B14	0x00	MST_VS1_DTG_ENABLE[7:0]	–	–	–	–	–	–	–	DTG_ENABLE
0x7B18	0x81	MST_VS1_DTG_MODE[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	DTG_DISABLE_MSA_RESET	RSVD	DMA_ENABLE
0x7B24	0x3F	MST_VS1_DMA_VSYNC_B0[7:0]	DMA_VSYNC_PULSE_WIDTH[7:0]							
0x7B26	0xFF	MST_VS1_DMA_VSYNC_B2[7:0]	DMA_VSYNC_FRONT_PORCH_L[7:0]							
0x7B27	0x01	MST_VS1_DMA_VSYNC_B3[7:0]	–	–	–	–	DMA_VSYNC_FRONT_PORCH_H[3:0]			

PRELIMINARY

Analog Devices Company Confidential, Provided TPK Under NDA Release 1.2 – Customers Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x7B28	0x0F	MST_VS1_DMA_HSYNC_B0[7:0]	DMA_HSYNC_PULSE_WIDTH_L[7:0]							
0x7B29	0x00	MST_VS1_DMA_HSYNC_B1[7:0]	–	–	–	–	DMA_HSYNC_PULSE_WIDTH_H[3:0]			
0x7B2A	0x0F	MST_VS1_DMA_HSYNC_B2[7:0]	DMA_HSYNC_FRONT_PORCH_L[7:0]							
0x7B2B	0x00	MST_VS1_DMA_HSYNC_B3[7:0]	–	–	–	–	DMA_HSYNC_FRONT_PORCH_H[3:0]			
0x7B38	0x00	MST_VS1_RED_CRC_B0[7:0]	RED_CRC_B0[7:0]							
0x7B39	0x00	MST_VS1_RED_CRC_B1[7:0]	RED_CRC_B1[7:0]							
0x7B3B	0x00	MST_VS1_RED_CRC_B3[7:0]	CRC_UPDATED	–	–	–	–	–	–	–
0x7B3C	0x00	MST_VS1_GRN_BLU_CRC_B0[7:0]	BLU_CRC_B0[7:0]							
0x7B3D	0x00	MST_VS1_GRN_BLU_CRC_B1[7:0]	BLU_CRC_B1[7:0]							
0x7B3E	0x00	MST_VS1_GRN_BLU_CRC_B2[7:0]	GRN_CRC_B0[7:0]							
0x7B3F	0x00	MST_VS1_GRN_BLU_CRC_B3[7:0]	GRN_CRC_B1[7:0]							
0x7B40	0x00	MST_VS1_MSA_IGNORE_HRES_B0[7:0]	MSA_IGNORE_HRES_B0[7:0]							
0x7B41	0x00	MST_VS1_MSA_IGNORE_HRES_B1[7:0]	MSA_IGNORE_HRES_B1[7:0]							
0x7B44	0x80	MST_VS1_MSA_IGNORE_COLOR[7:0]	MSA_IGNORE_COLOR_MODE_EN	–	–	MSA_IGNORE_COLOR_MODE[4:0]				
0x7B45	0x02	MST_VS1_DSC_MISC[7:0]	DSC_VBID_OVR	–	DSC_PIX_REM_OVR[1:0]		–	–	DSC_TS_AUTO_MDIV3	DSC_TS_USE_MDIV3
0x7B48	0x00	MST_VS1_PPS_CHUNK_SIZE_OVR_B0[7:0]	PPS_CHUNK_SIZE_OVR_B0[7:0]							

PRELIMINARY

Analog Devices Confidential, Provided to Customers Under NDA

Release to TPK Under NDA

MAXIM INTEGRATED CONFIDENTIAL/DISTRIBUTE ONLY UNDER NDA

ADDRESS	RESET	NAME	MSB							LSB
0x7B49	0x00	MST_VS1_PPS_CHUNK_SIZE_OVR_B1[7:0]	PPS_CHUNK_SIZE_OVR_B1[7:0]							
0x7B4A	0x00	MST_VS1_PPS_SLICE_WIDTH_OVR_B0[7:0]	PPS_SLICE_WIDTH_OVR_B0[7:0]							
0x7B4B	0x00	MST_VS1_PPS_SLICE_WIDTH_OVR_B1[7:0]	PPS_SLICE_WIDTH_OVR_B1[7:0]							
0x7B4C	0x00	MST_VS1_PPS_BITS_PER_PIX_OVR_B0[7:0]	PPS_BITS_PER_PIX_OVR_B0[7:0]							
0x7B4D	0x00	MST_VS1_PPS_BITS_PER_PIX_OVR_B1[7:0]	PPS_BITS_PER_PIX_OVR_B1[7:0]							
0x7B50	0x01	MST_VS1_DSC_SUPPORT[7:0]	–	–	–	–	–	–	–	DSC_SUPPORT
0x7B51	0x11	MST_VS1_DSC_VERSION[7:0]	DSC_VERSION[7:0]							
0x7B71	0x00	MST_VS1_DSC_STATUS_B1[7:0]	–	–	–	–	–	DSC_CHUNK_SIZE_ERROR	DSC_ACTIVE	DSC_ENABLE
0x7B73	0x00	MST_VS1_DSC_CRC_STATUS[7:0]	–	–	–	–	–	–	DSC_PIX_CRC_VAL	DSC_CRC_VAL
0x7B74	0x00	MST_VS1_DSC_CRC0_B0[7:0]	DSC_CRC0_B0[7:0]							
0x7B75	0x00	MST_VS1_DSC_CRC0_B1[7:0]	DSC_CRC0_B1[7:0]							
0x7B76	0x00	MST_VS1_DSC_CRC1_B0[7:0]	DSC_CRC1_B0[7:0]							
0x7B77	0x00	MST_V1_DSC_CRC1_B1[7:0]	DSC_CRC1_B1[7:0]							
0x7B78	0x00	MST_VS1_DSC_CRC2_B0[7:0]	DSC_CRC2_B0[7:0]							
0x7B79	0x00	MST_VS1_DSC_CRC2_B1[7:0]	DSC_CRC2_B1[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x7B7A	0x00	MST_VS1_DSC_PIX_CRC0_B0[7:0]	DSC_PIX_CRC0_B0[7:0]							
0x7B7B	0x00	MST_VS1_DSC_PIX_CRC0_B1[7:0]	DSC_PIX_CRC0_B1[7:0]							
0x7B7C	0x00	MST_VS1_DSC_PIX_CRC1_B0[7:0]	DSC_PIX_CRC1_B0[7:0]							
0x7B7D	0x00	MST_VS1_DSC_PIX_CRC1_B1[7:0]	DSC_PIX_CRC1_B1[7:0]							
0x7B7E	0x00	MST_VS1_DSC_PIX_CRC2_B0[7:0]	DSC_PIX_CRC2_B0[7:0]							
0x7B7F	0x00	MST_VS1_DSC_PIX_CRC2_B1[7:0]	DSC_PIX_CRC2_B1[7:0]							
0x7B80	0x01	MST_VS1_SECONDARY_ENABLE[7:0]	–	–	–	–	–	–	–	SECONDARY_ENABLE
0x7B84	0x01	MST_VS1_AUDIO_MUTE[7:0]	–	–	–	–	–	–	–	AUDIO_MUTE
0x7B8C	0x00	MST_VS1_AUDIO_SAMPLE_RES[7:0]	–	–	AUDIO_SAMPLE_RES[5:0]					
0x7B90	0x00	MST_VS1_AUDIO_CHANNEL_COUNT[7:0]	–	–	–	–	AUDIO_CHANNEL_COUNT[3:0]			
0x7B98	0x01	MST_VS1_AUDIO_OUTPUT_SELECT[7:0]	–	–	–	–	–	–	RSVD	RSVD
0x7B9C	0x00	MST_VS1_AUDIO_CHANNEL_MAP_B0[7:0]	–	CHANNEL_1_MAP[2:0]			–	CHANNEL_0_MAP[2:0]		
0x7B9D	0x00	MST_VS1_AUDIO_CHANNEL_MAP_B1[7:0]	–	CHANNEL_3_MAP[2:0]			–	CHANNEL_2_MAP[2:0]		
0x7B9E	0x00	MST_VS1_AUDIO_CHANNEL_MAP_B2[7:0]	–	CHANNEL_5_MAP[2:0]			–	CHANNEL_4_MAP[2:0]		
0x7B9F	0x00	MST_VS1_AUDIO_CHANNEL_MAP_B3[7:0]	–	CHANNEL_7_MAP[2:0]			–	CHANNEL_6_MAP[2:0]		
0x7BA0	0x00	MST_VS1_MAUD_B0[7:0]	MAUD_B0[7:0]							

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ADDRESS	RESET	NAME	MSB							LSB
0x7BA1	0x00	MST_VS1_MAUD_B1[7:0]	MAUD_B1[7:0]							
0x7BA2	0x00	MST_VS1_MAUD_B2[7:0]	MAUD_B2[7:0]							
0x7BA4	0x00	MST_VS1_NAUD_B0[7:0]	NAUD_B0[7:0]							
0x7BA5	0x00	MST_VS1_NAUD_B1[7:0]	NAUD_B1[7:0]							
0x7BA6	0x00	MST_VS1_NAUD_B2[7:0]	NAUD_B2[7:0]							
0x7BB8	0x00	MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_0[7:0]	AUDIO_CHANNEL_STATUS_FIELD_0[7:0]							
0x7BBC	0x00	MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_1[7:0]	AUDIO_CHANNEL_STATUS_FIELD_1[7:0]							
0x7BC0	0x00	MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_2[7:0]	AUDIO_CHANNEL_STATUS_FIELD_2[7:0]							
0x7BC4	0x00	MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_3[7:0]	AUDIO_CHANNEL_STATUS_FIELD_3[7:0]							
0x7BC8	0x00	MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_4[7:0]	AUDIO_CHANNEL_STATUS_FIELD_4[7:0]							
0x7BCC	0x00	MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_5[7:0]	AUDIO_CHANNEL_STATUS_FIELD_5[7:0]							
0x7BD0	0x00	MST_VS1_AUDIO_CHANNEL_NUMBER_0_1[7:0]	CHANNEL_NUMBER_1[3:0]				CHANNEL_NUMBER_0[3:0]			
0x7BD4	0x00	MST_VS1_AUDIO_CHANNEL_NUMBER_2_3[7:0]	CHANNEL_NUMBER_3[3:0]				CHANNEL_NUMBER_2[3:0]			
0x7BD8	0x00	MST_VS1_AUDIO_CHANNEL_NUMBER_4_5[7:0]	CHANNEL_NUMBER_5[3:0]				CHANNEL_NUMBER_4[3:0]			

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ADDRESS	RESET	NAME	MSB							LSB
0x7BDC	0x00	MST_VS1_AUDIO_CHANNEL_NUMBER_6_7[7:0]	CHANNEL_NUMBER_7[3:0]				CHANNEL_NUMBER_6[3:0]			
0x7BE4	0x00	MST_VS1_DSC_BUFFER_RDATA[7:0]	DSC_PPS_RDATA[7:0]							
0x7BE8	0x02	MST_VS1_AUDIO_PACKET_DEPTH[7:0]	–	–	–	–	–	–	AUDIO_PACKET_DEPTH[1:0]	
DPCD										

Register Details

REG0 (0x0)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	I²C/UART Device Address Default value is set according to the latched CFG pin value at power-up. See CFG pin decoding table in the data sheet.	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 .... 0b1000000: I²C write/read address is 0x80/0x81 0b1000010: I²C write/read address is 0x84/0x85 0b1000100: I²C write/read address is 0x88/0x89 0b1100000: I²C write/read address is 0xC0/0xC1 0b1100010: I²C write/read address is 0xC4/0xC5 0b1100100: I²C write/read address is 0xC8/0xC9 0b0100000: I²C write/read address is 0x40/0x41 0b0100010: I²C write/read address is 0x44/0x45 ... ... 0b1111111: I²C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.	0b0: Not Blocked 0b1: Blocked

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REG2 (0x2)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_TX_Y_SRC	AUD_TX_X_SRC	AUD_TX_EN_Y	AUD_TX_EN_X	RSVD	RSVD	RSVD	RSVD
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_TX_Y_SRC	7	Selects audio-input pins to use for forward audio engine Y	0x0: SCK1, SD1, WS1 0x1: SCK2, SD2, WS2
AUD_TX_X_SRC	6	Selects audio-input pins to use for forward audio engine X	0x0: SCK1, SD1, WS1 0x1: SCK2, SD2, WS2
AUD_TX_EN_Y	5	Audio Transmit Enable for Port Y	0b0: Audio transmit Channel Y disabled 0b1: Audio transmit Channel Y enabled
AUD_TX_EN_X	4	Audio Transmit Enable for Port X	0b0: Audio transmit Channel X disabled 0b1: Audio transmit Channel X enabled

REG3 (0x3)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RSVD	RCLKEN	–	RCLKSEL[1:0]	
Reset	–	–	–	0b0	0b0	–	0b00	
Access Type	–	–	–		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RCLKEN	3	Enables RCLK Output Bit is set by the RCLKEN pin at power-up.	0b0: RCLK output disabled 0b1: RCLK output enabled
RCLKSEL	1:0	RCLKOUT Clock Selection	0x0: XTAL/1 = 25MHz 0x1: XTAL/2 = 12.5MHz 0x2: XTAL/4 = 6.25MHz 0x3: Reserved

REG4 (0x4)*

BIT	7	6	5	4	3	2	1	0
Field	GMSL3_B	GMSL3_A	HVD_OUT_EN	DIS_LOCAL_CC	RSVD	RSVD	RSVD	SW_INT
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
GMSL3_B	7	GMSL2/GMSL3 selection for Link B Bit is set according to the latched CFG pin value at power-up. FEC is turned on by default when powering up in GMSL3 mode. When manually changing after power-up, make sure that FEC_TX_EN is also turned off or on according to user requirements.	0x0: Link B is GMSL2 0x1: Link B is GMSL3
GMSL3_A	6	GMSL2/GMSL3 selection for Link A Bit is set according to the latched CFG pin value at power-up. FEC is turned on by default when powering up in GMSL3 mode. When manually changing after power-up, make sure that FEC_TX_EN is also turned off or on according to user requirements.	0x0: Link A is GMSL2 0x1: Link A is GMSL3
HVD_OUT_EN	5	Enable HS,VS, DE, PCLK output from MFPs for system debug. By default, video pipe X signals are routed to MFPs. To route signals of other video pipes contact Maxim.	0b0: HS,VS,DE outputs disabled 0b1: HS,VS,DE outputs enabled
DIS_LOCAL_CC	4	Disables control-channel connection to RX/SDA and TX/SCL pins	0b0: RX/SDA and TX/SCL pins are connected to control channel 0b1: RX/SDA and TX/SCL pins are disconnected from control channel, registers can be programmed from remote side
SW_INT	0	Software interrupt to mark power-up Write 0 to clear after the part is configured.	0x0: Part is configured 0x1: Part is not configured

REG5 (0x5)*

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	LOCK_CFG[1:0]		PU_LF3	PU_LF2	PU_LF1	PU_LF0
Reset	0b1	0b1	0b00		0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enables LOCK output.	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enables ERRB output	0b0: ERRB output disabled 0b1: ERRB output enabled
LOCK_CFG	5:4	Configures what is reported at LOCK pin For settings 2 and 3, daisy chain repeater count should be programmed to DES_CNT bitfields in LINK_CTRL_A and LINK_CTRL_B register blocks.	0x0: Link A **OR** Link B is locked 0x1: Link A **AND** Link B is locked 0x2: All RPT/DES on Chain A is locked **OR** All RPT/DES on Chain B is locked 0x3: All RPT/DES on Chain A is locked **AND** All RPT/DES on Chain B is locked
PU_LF3	3	Powers Up Line-Fault Monitor 3	0b0: Line-fault monitor 3 disabled 0b1: Line-fault monitor 3 enabled
PU_LF2	2	Powers Up Line-Fault Monitor 2	0b0: Line-fault monitor 2 disabled 0b1: Line-fault monitor 2 enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
PU_LF1	1	Powers Up Line-Fault Monitor 1	0b0: Line-fault monitor 1 disabled 0b1: Line-fault monitor 1 enabled
PU_LF0	0	Powers Up Line-Fault Monitor 0	0b0: Line-fault monitor 0 disabled 0b1: Line-fault monitor 0 enabled

REG7 (0x7)*-

BIT	7	6	5	4	3	2	1	0
Field	–	–	CMP_STATUS_MASK[5:0]					
Reset	–	–	0b000111					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
CMP_STATUS_MASK	5:0	Select VDD comparator status bits to drive VDDCMP error flag and ERRB pin.

PWR0 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[1:0]		CMP_STATUS[5:0]					
Reset	0b00		0b000000					
Access Type	Read Only		Read Only					

BITFIELD	BITS	DESCRIPTION
VDDBAD_STATUS	7:6	Power manager switched 1V supply comparator status bits [1:0] 0: Latched high when VDD_sw < 0.806 V 1: Latched high when VDD_sw < 0.806 V
CMP_STATUS	5:0	Power manager comparator status bits 0: Latched low when VDD18 < 1.625 V 1: Latched low when switched VDDIO supply < 1.625 V 2: Latched low when VDD_sw < 0.806 V 3: VDD_sw < 1.041 V when equal to 0 (live) 4: VDD < 1.1092 V when equal to 0 (live)

PWR1 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	OVERTEMP	VDDBAD_STATUS_H	PORZ_STATUS[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Read Only	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OVERTEMP	7	Temperature monitor overtemp indicator. Trip temperature Ttrip set by SET_TEMP1P0[1:0] in CMU6.	0x0: T < Ttrip 0x1: T > Ttrip

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BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS_H	6	Power manager switched 1V supply comparator status bit [2] 2: LDO powered on when equal to 1 (live)	
PORZ_STATUS	5:0	Power-on-reset status bits 0: Latched low when either VDD18 < 1.516 V or VDDIO < 1.055 V 1: Reserved 2: Latched low when VDDIO < 1.055 V 3: Reserved 4: Latched low when VDD18 < 1.516 V 5: Reserved	

PWR4 (0xC)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			
Reset	0b0	0b0	0b1	0b1	0x5			
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable wake-up by local µC from SDA_RX Pin	0b0: Local wake-up enabled 0b1: Local wake-up disabled
WAKE_EN_B	5	Enable wake-up by remote chip connected to Link B	0b0: Link B remote wake-up disabled 0b1: Link B remote wake-up enabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to Link A	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	This register's value is FF. Read the 16-bit device ID at 0x0024 and 0x0025 (DEV_ID16_LSB and DEV_ID16_MSB)	0xFF: All GM13 devices

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	DEV_REV[3:0]			
Reset	0b0	0b0	0b0	0b0	0x1			
Access Type					Read Only			

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BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision	0xX: Device revision number

CTRL0 (0x10)*

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	–	–	–	SLEEP	RSVD	–	–
Reset	0b0	–	–	–	0b0	0b0	–	–
Access Type	Write, Read	–	–	–	Write, Read		–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Writing a 1 to this bit resets the device including all blocks, and registers are reset to defaults. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset
SLEEP	3	Activates Sleep Mode	0b0: Sleep mode disabled 0b1: Sleep mode enabled

CTRL1 (0x11)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	RSVD	CXTP_B	RSVD	CXTP_A
Reset	0b0	0b0	0b0	–	0b1	0b0	0b1	0b0
Access Type				–		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_B	2	Coax/twisted-pair cable select for Link B Bit is set according to the latched CFG pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/twisted-pair cable select for Link A Bit is set according to the latched CFG pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

CTRL3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	HPD_IN	–	–	–	LOCKED	ERROR	CMU_LOCKED	–
Reset	0b0	–	–	–	0b0	0b0	0b0	–
Access Type	Read Only	–	–	–	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IN	7	Reads back HPD pin level	0b0: Disabled 0b1: Enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED	3	GMSL link locked (bidirectional)	0b0: GMSL link not locked 0b1: GMSL link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock Multiplier Unit (CMU) Locked	0b0: CMU not locked 0b1: CMU locked

CTRL7 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	–	–	DIS_TEMP_WAKE_TO_SLEEP_B	DIS_TEMP_WAKE_TO_SLEEP_A
Reset	0b0	0b1	0b1	–	–	–	0b0	0b0
Access Type				–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_TEMP_WAKE_TO_SLEEP_B	1	Disables temporary wake-up signal while going into sleep.	0x0: Enabled 0x1: Disabled
DIS_TEMP_WAKE_TO_SLEEP_A	0	Disables temporary wake-up signal while going into sleep.	0x0: Enabled 0x1: Disabled

INTR0 (0x18)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	–	–	–	–	0b0	0b000		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A, DEC_ERR_B, IDLE_ERR_A, and IDLE_ERR_B bitfields after ERRB pin is asserted for 1µs.	0b0: Auto reset disabled 0b1: Auto reset enabled
DEC_ERR_THR	2:0	Decoding and idle error reporting threshold. DEC_ERR_FLAG_A is asserted when DEC_ERR_A ≥ DEC_ERR_THR. DEC_ERR_FLAG_B is asserted when DEC_ERR_B ≥ DEC_ERR_THR. IDLE_ERR_FLAG is asserted when IDLE_ERR_A ≥ DEC_ERR_THR or IDLE_ERR_B ≥ DEC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

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INTR1 (0x19)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0x0				0b0	0b000		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet Count Multiplier Exponent See the description of PKT_CNT bitfield (register LCTRL5).	0bXXX: PKT_CNT exponent
AUTO_CNT_RST_EN	3	Automatically resets PKT_CNT bitfield (register LCTRL5) after ERRB pin is asserted for 1µs.	0b0: Automatic reset disabled 0b1: Automatic reset enabled
PKT_CNT_THR	2:0	Packet count reporting threshold (see PKT_CNT description - register LCTRL5) PKT_CNT_FLAG is asserted when PKT_CNT_A ≥ PKT_CNT_THR or PKT_CNT_B ≥ PKT_CNT_THR.	0b000: 1 packet 0b001: 2 packets 0b010: 4 packets 0b011: 8 packets 0b100: 16 packets 0b101: 32 packets 0b110: 64 packets 0b111: 128 packets

INTR2 (0x1A)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_OEN_B	REM_ERR_OEN_A	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b1	0b1
Access Type			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_OEN_B	5	Enables reporting of remote error status (REM_ERR_B—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
REM_ERR_OEN_A	4	Enables reporting of remote error status (REM_ERR_A—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_OEN	3	Enables reporting of line-fault interrupt (LFLT_INT—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
IDLE_ERR_OEN	2	Enables reporting of idle word errors (IDLE_ERR_FLAG—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_B	1	Enables reporting of decoding errors (DEC_ERR_FLAG_B—0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enables reporting of decoding errors (DEC_ERR_FLAG_A— 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

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INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_FLAG_B	REM_ERR_FLAG_A	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type			Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_FLAG_B	5	Received remote side error status (inverse of remote side ERRB pin level on Link B)	0b0: No remote side error 0b1: Remote side error
REM_ERR_FLAG_A	4	Received remote side error status (inverse of remote side ERRB pin level on Link A)	0b0: No remote side error 0b1: Remote side error
LFLT_INT	3	Line-Fault Interrupt Asserted when any of line-fault monitors indicate a fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line-fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behavior.	0b0: No line fault 0b1: Line fault
IDLE_ERR_FLAG	2	Idle Word Error Flag Asserted when IDLE_ERR_A ≥ DEC_ERR_THR or when IDLE_ERR_B ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_B	1	Decoding Error Flag for Link B Asserted when DEC_ERR_B ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_A	0	Decoding Error for Link A Asserted when DEC_ERR_A ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted

INTR4 (0x1C)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_OEN_B	EOM_ERR_OEN_A	HDCP_INT_OEN_B	HDCP_INT_OEN_A	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	–
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b0	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_B	7	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_B—0x1D) for Link B at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
EOM_ERR_OEN_A	6	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_A—0x1D) for Link A at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_INT_OEN_B	5	Enables reporting of GMSL HDCP interrupt (HDCP_INT_B_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
HDCP_INT_OEN_A	4	Enables reporting of GMSL HDCP interrupt (HDCP_INT_A_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG—0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG—0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enables reporting of packet count flag (PKT_CNT_FLAG—0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	HDCP_INT_FLAG_B	HDCP_INT_FLAG_A	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_B	7	Eye-opening monitor is below configured threshold for Link B	0b0: No EOM error on Link B 0b1: EOM error on Link B
EOM_ERR_FLAG_A	6	Eye-opening monitor is below configured threshold for Link A	0b0: No EOM error on Link A 0b1: EOM error on Link A
HDCP_INT_FLAG_B	5	HDCP Interrupt Status Asserted when there is a GMSL HDCP interrupt.	0b0: No HDCP interrupt 0b1: HDCP interrupt
HDCP_INT_FLAG_A	4	HDCP Interrupt Status Asserted when there is a GMSL HDCP interrupt.	0b0: No HDCP interrupt 0b1: HDCP interrupt
MAX_RT_FLAG	3	Combined ARQ maximum retransmission limit error flag Asserted when any of the selected channels ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN (register ARQ1) bit.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG	2	Combined ARQ retransmission event flag Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN (0x1C) register bit.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet Count Flag Asserted when PKT_CNT_A ≥ PKT_CNT_THR (0x19) or PKT_CNT_B ≥ PKT_CNT_THR.	0b0: Flag not asserted 0b1: Flag asserted

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INTR6 (0x1E)*

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	PORZ_INT_OEN	VDDBAD_INT_OEN	VDD_OV_OEN	DPRX_INT_OEN	APRBS_Y_ERR_OEN	APRBS_X_ERR_OEN	INT_ERR_OEN
Reset	0b1	0b1	0b1	0b0	0b0	0b1	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	7	Enables reporting of combined V_{DD} comparator output (VDDCMP_INT_FLAG—0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PORZ_INT_OEN	6	Enables reporting of PORZ interrupt (PORZ_INT_FLAG—0x1F) at ERRB pin	0x0: Disable PORZ interrupt reporting 0x1: Enable PORZ interrupt reporting
VDDBAD_INT_OEN	5	Enable reporting of V_{DDBAD} interrupt (VDDBAD_INT_FLAG—0x1F) at ERRB pin	0x0: Disable VDDBAD interrupt reporting 0x1: Enable VDDBAD interrupt reporting
VDD_OV_OEN	4	Enables V_{DD} overvoltage status on ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DPRX_INT_OEN	3	Enables reporting of display port receiver interrupt (DPRX_INT—0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
APRBS_Y_ERR_OEN	2	Enables reporting of audio Rx Y Channel PRBS errors (APRBS_Y_ERR_FLAG—0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
APRBS_X_ERR_OEN	1	Enables reporting of audio Rx X Channel PRBS errors (APRBS_X_ERR_FLAG—0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
INT_ERR_OEN	0	Enable reporting internal error conditions (INT_ERR_FLAG—0x1F) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	PORZ_INT_FLAG	VDDBAD_INT_FLAG	VDD_OV_FLAG	DPRX_INT	APRBS_Y_ERR_FLAG	APRBS_X_ERR_FLAG	INT_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	7	Combined V_{DD} comparator output See CMP_STATUS_MASK register.	0b0: Flag not asserted 0b1: Flag asserted
PORZ_INT_FLAG	6	PORZ Interrupt Flag	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	5	Combined V_{DDBAD} Indicator	0b0: Flag not asserted 0b1: Flag asserted
VDD_OV_FLAG	4	V_{DD} Overvoltage Flag This bit stays high when asserted and must be cleared by the user. It is set when V_{DD} exceeds the overvoltage threshold. It is cleared when read.	0b0: V_{DD} overvoltage not detected 0b1: V_{DD} overvoltage detected

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BITFIELD	BITS	DESCRIPTION	DECODE
DPRX_INT	3	DPRX Interrupt	0b0: Flag not asserted 0b1: Flag asserted
APRBS_Y_ERR_FLAG	2	Audio Rx Y Channel PRBS Error Flag Asserted when AUD_RX_Y_APRBS_ERR > 0.	0b0: Flag not asserted 0b1: Flag asserted
APRBS_X_ERR_FLAG	1	Audio Rx X Channel PRBS Error Flag Asserted when AUD_RX_X_APRBS_ERR > 0.	0b0: Flag not asserted 0b1: Flag asserted
INT_ERR_FLAG	0	Combined Internal Error flag This flag is asserted when any one of these is asserted: OVERFLOW_A_X/Y/Z/U OVERFLOW_B_X/Y/Z/U DRIFT_ERR_A_X/Y/Z/U DRIFT_ERR_B_X/Y/Z/U ASYM_OVERFLOW_X/Y/Z/U ASYM_UNDERFLOW_X/Y/Z/U AUD_OVERFLOW_X/Y AUD_DRIFT_ERR_X/Y AUD_BLK_LEN_ERR_X/Y UART_TX_OVERFLOW_A/B UART_RX_OVERFLOW_A/B UART_TX_OVERFLOW_1_A/B UART_RX_OVERFLOW_1_A/B UART_TX_OVERFLOW_2_A/B UART_RX_OVERFLOW_2_A/B SPI_TX_OVRFLW SPI_RX_OVRFLW FAILLOCK_A/B	0b0: Flag not asserted 0b1: Flag asserted

INTR8 (0x20)*

BIT	7	6	5	4	3	2	1	0
Field	SW_INT_OEN	VDDIO_OV_OEN	VDD1P8_OV_OEN	RSVD	LOCK_B_OEN	LOCK_A_OEN	LOCK_OEN	LOSS_OF_LOCK_OEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SW_INT_OEN	7	Enables reporting of software interrupt on ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VDDIO_OV_OEN	6	Enables V_{DDIO} overvoltage status on ERRB.	0b0: Reporting disabled 0b1: Reporting enabled
VDD1P8_OV_OEN	5	Enables V_{DD1P8} overvoltage status on ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LOCK_B_OEN	3	Enables reporting of Link B lock status (LOCK_B_FLAG—0x21) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LOCK_A_OEN	2	Enables reporting of Link A lock status (LOCK_A_FLAG—0x21) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_OEN	1	Enables reporting of lock pin status (LOCK_FLAG—0x21) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LOSS_OF_LOCK_OEN	0	Enables reporting loss of lock at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR9 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	SW_INT_FLAG	VDDIO_OV_FLAG	VDD1P8_OV_FLAG	RSVD	LOCK_B_FLAG	LOCK_A_FLAG	LOCK_FLAG	LOSS_OF_LOCK_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Clears All	Read Clears All		Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SW_INT_FLAG	7	Software Interrupt Read-Only Value Follows the value of writable SW_INT (0x4) register bit.	0b0: Flag not asserted 0b1: Flag asserted
VDDIO_OV_FLAG	6	Sticky status value for V_{DDIO} overvoltage	0b0: Flag not asserted 0b1: Flag asserted
VDD1P8_OV_FLAG	5	Sticky status value for V_{DD1P8} overvoltage	0b0: Flag not asserted 0b1: Flag asserted
LOCK_B_FLAG	3	Link B Lock Status	0b0: Flag not asserted 0b1: Flag asserted
LOCK_A_FLAG	2	Link A Lock Status	0b0: Flag not asserted 0b1: Flag asserted
LOCK_FLAG	1	Lock pin status	0b0: Flag not asserted 0b1: Flag asserted
LOSS_OF_LOCK_FLAG	0	Loss of lock on GMSL link is detected (sticky)	0x0: Not detected 0x1: Detected

INTR10 (0x22)*

BIT	7	6	5	4	3	2	1	0
Field	LFLT_INT_OPEN_OEN	LFLT_INT_L2LS_OEN	LFLT_INT_BAT_S_OEN	LFLT_INT_GND_S_OEN	REG_CRC_ERR_OEN	I2C_UART_MSGCNTR_ERR_OEN	I2C_UART_CRC_ERR_OEN	HDCP2_INT_OEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_OPEN_OEN	7	Enables reporting of line fault open interrupt (LFLT_INT_OPEN—0x23) at ERRB pin	0x0: Reporting disabled 0x1: Reporting enabled
LFLT_INT_L2LS_OEN	6	Enables reporting of line-to-line short line-fault interrupt (LFLT_INT—0x1B) at ERRB pin	0x0: Reporting disabled 0x1: Reporting enabled
LFLT_INT_BAT_S_OEN	5	Enables reporting of short-to-battery line-fault interrupt (LFLT_INT—0x1B) at ERRB pin	0x0: Reporting disabled 0x1: Reporting enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_GND_S_OEN	4	Enables reporting of short-to-ground line-fault interrupt (LFLT_INT—0x1B) at ERRB pin.	0x0: Reporting disabled 0x1: Reporting enabled
REG_CRC_ERR_OEN	3	Enable reporting register CRC at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
I2C_UART_MSGCNTR_ERR_OEN	2	Enables reporting of I^2C/UART message count errors (I2C_UART_MSGCNTR_ERR_FLAG—0x23) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
I2C_UART_CRC_ERR_OEN	1	Enables reporting of I^2C/UART CRC errors (I2C_UART_CRC_ERR_FLAG—0x23) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
HDCP2_INT_OEN	0	Enables reporting of GMSL HDCP2 interrupt (HDCP2_INT_FLAG) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

INTR11 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	LFLT_INT_OPEN	LFLT_INT_L2LS	LFLT_INT_BAT_S	LFLT_INT_GND_S	REG_CRC_ERR_FLAG	I2C_UART_MSGCNTR_ERR_FLAG	I2C_UART_CRC_ERR_FLAG	HDCP2_INT_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_OPEN	7	Line Fault Interrupt Asserted when either one of line-fault monitors indicates an open-fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behavior.	0x0: No line fault 0x1: Line fault
LFLT_INT_L2LS	6	Line-Fault Interrupt Asserted when either one of line-fault monitors indicates a line-to-line short fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line-fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behavior.	0x0: No line fault 0x1: Line fault

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BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_BAT_S	5	Line-Fault Interrupt Asserted when either one of line-fault monitors indicates a short-to-battery fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line-fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behavior.	0x0: No line fault 0x1: Line fault
LFLT_INT_GND_S	4	Line-Fault Interrupt Asserted when either one of line-fault monitors indicates a short-to-ground fault status. See LF_0 and LF_1 bitfields (register LF0_LF1) for more information. Line-fault condition needs to be cleared to clear this flag. Use LFLT_SKTY_INT register to set interrupt behavior.	0x0: No line fault 0x1: Line fault
REG_CRC_ERR_FLAG	3	An error occurred on the register CRC calculation	0b0: Flag not asserted 0b1: Flag asserted
I2C_UART_MSGCNTR_ERR_FLAG	2	I^2C/UART Message Count Error Flag Asserted when MSGCNTR_ERR_CNx is nonzero.	0b0: Flag not asserted 0b1: Flag asserted
I2C_UART_CRC_ERR_FLAG	1	I^2C/UART CRC Error Flag Asserted when CC_CRC_ERR_CNT is nonzero.	0b0: Flag not asserted 0b1: Flag asserted
HDCP2_INT_FLAG	0	Asserted when there is a GMSL HDCP2 interrupt	0b0: No HDCP interrupt 0b1: HDCP interrupt

DEV_ID16_LSB (0x24)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID16_LSB[7:0]							
Reset	0x51							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID16_LSB	7:0	16-Bit Device Identifier	0x60: MAX96749AC 0x61: MAX96749AP 0x50: MAX96767 0x51: MAX96769 0x53: MAX96855 0x54: MAX96857 0x55: MAX96859 0x56: MAX96861

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DEV_ID16_MSB (0x25)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID16_MSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID16_MSB	7:0	16-Bit Device Identifier	0x60: MAX96749AC 0x61: MAX96749AP 0x50: MAX96767 0x51: MAX96769 0x53: MAX96855 0x54: MAX96857 0x55: MAX96859 0x56: MAX96861

LF0_LF1 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_1[2:0]			–	LF_0[2:0]		
Reset	–	0b010			–	0b010		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_1	6:4	Line-fault status of wire connected to LMN1 pin	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short
LF_0	2:0	Line-fault status of wire connected to LMN0 pin	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

LF2_LF3 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_3[2:0]			–	LF_2[2:0]		
Reset	–	0b010			–	0b010		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_3	6:4	Line-fault status of wire connected to LMN3 pin	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

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BITFIELD	BITS	DESCRIPTION	DECODE
LF_2	2:0	Line-fault status of wire connected to LMN2 pin	0b000: Short-to-battery 0b001: Short-to-GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

LCTRL0 (0x28, 0x32)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	DES_CNT[1:0]		TX_RATE[1:0]		RSVD[1:0]	
Reset	0b1	–	0b00		0b10		0b00	
Access Type	Write, Read	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Enables this GMSL link	0x0: Link is disabled 0x1: Link is enabled
DES_CNT	5:4	Set this to the number of repeater devices in the daisy chain connected to this link	0x0: No repeaters 0x1: One repeater 0x2: Two repeaters 0x3: Three repeaters
TX_RATE	3:2	Transmitter (forward channel) bit rate When changed, becomes active after the next link reset. Default value is set by the CFG pin at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: 12Gbps

LCTRL1 (0x29, 0x33)*

BIT	7	6	5	4	3	2	1	0
Field	DIS_LOCK_TO	RSVD	RSVD	RSVD	–	–	RESET_ONESHOT	RESET_LINK
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Write, Read				–	–	Write Clears All, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCK_TO	7	Disables Lock Timeout	0x0: PHY is reset if it cannot lock in 160ms 0x1: Timeout is disabled
RESET_ONESHOT	1	Reset entire data path in one-shot (keep register settings) Write 1 to activate reset. Bit automatically clears and releases reset.	0b0: No action 0b1: Reset data path
RESET_LINK	0	Resets whole data path for this link (keep register settings) Write a 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset

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LCTRL2 (0x2A, 0x34)

BIT	7	6	5	4	3	2	1	0
Field	DAISY_CHAIN_STATUS[1:0]		–	–	RSVD	RSVD	RSVD	LINK_LOCKED
Reset	0x0		–	–	0x0	0b0	0b0	0b0
Access Type	Read Only		–	–		Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DAISY_CHAIN_STATUS	7:6	Daisy-chain lock status for this link.	0x0: No repeaters locked 0x1: One repeater locked 0x2: Two repeaters locked 0x3: Three repeaters locked
RSVD	2	Rx data path is locked	0x0: Rx data path is not locked 0x1: Rx data path is locked
LINK_LOCKED	0	GMSL link locked (bidirectional)	0b0: GMSL link not locked 0b1: GMSL link locked

LCTRL3 (0x2B, 0x35)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR	7:0	Number of decoding (disparity) errors detected at this link Resets after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

LCTRL4 (0x2C, 0x36)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of idle word errors detected on this link Resets after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

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LCTRL5 (0x2D, 0x37)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of received packets of a selected type at this link Packet type is selected with PKT_CNT_SEL register. Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT x ($2^{PKT_CNT_EXP}$) and < (PKT_CNT + 1) x ($2^{PKT_CNT_EXP}$). When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

LCTRL6 (0x2E, 0x38)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0b1	–	–	0b11111				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmits local error status (inverse of ERRB pin level) to remote side through GPIO channel on this link	0b0: Transmit error status disabled 0b1: Transmit error status enabled
ERR_TX_ID	4:0	GPIO ID used for transmitting error status on this link	0bXXXXX: Value of GPIO ID for transmitting ERR_TX

LCTRL7 (0x2F, 0x39)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
Reset	0b1	0b1	–	0b11111				
Access Type	Write, Read	Read Only	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Receives remote error status (ERRB pin level) through GPIO channel on this link with ERR_RX_ID	0b0: Receive error status disabled 0b1: Receive error status enabled
RSVD	6	Received error status value from this link with ERR_RX_ID	0b0: Disabled 0b1: Enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_ID	4:0	First GPIO ID used for receiving error status on this link	0bXXXXX: Value of GPIO ID for receiving ERR_TX

TEST_0 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	OTP_REV[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OTP_REV	7:0	This register shows the revision of the data burned into the OTP. Every time a register default is changed thru OTP, this revision is incremented as a notification. Default value seen in the document may be overwritten by OTP.

TEST_1 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	DEBUG_EXTRA[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DEBUG_EXTRA	7:0	Extra debug control bits When HVD_OUT_EN=1 DEBUG_EXTRA[3:2] selects the pipeline (X,Y) DEBUG_EXTRA[1:0] selects the stage where HVD is tapped: 0x = DPRX output 10 = FIFO output 11 = VTX output

REG0_INTR (0x40)*

BIT	7	6	5	4	3	2	1	0
Field	FCRC_CHECK_ERR_OEN_Y	FCRC_CHECK_ERR_OEN_X	VOTE_ERR_FCRC_OEN_Y	VOTE_ERR_FCRC_OEN_X	VOTE_ERR_FCNT_OEN_Y	VOTE_ERR_FCNT_OEN_X	SGMII_INT_OEN	SGMII_DEC_ERR_OEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FCRC_CHECK_ERR_OEN_Y	7	Enables reporting of video frame CRC check error on ERRB pin for pipe Y.	0b0: Reporting disabled 0b1: Reporting enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
FCRC_CHECK_ERR_OEN_X	6	Enables reporting of video frame CRC check error on ERRB pin for pipe X.	0b0: Reporting disabled 0b1: Reporting enabled
VOTE_ERR_FCRC_OEN_Y	5	Enables reporting of video frame CRC voting error on ERRB pin for pipe Y (Frame CRC is sent in last line).	0b0: Reporting disabled 0b1: Reporting enabled
VOTE_ERR_FCRC_OEN_X	4	Enables reporting of video frame CRC voting error on ERRB pin for pipe X (Frame CRC is sent in last line).	0b0: Reporting disabled 0b1: Reporting enabled
VOTE_ERR_FCNT_OEN_Y	3	Enables reporting of video frame count voting error on ERRB pin for pipe Y (Frame CNT is sent in last line).	0b0: Reporting disabled 0b1: Reporting enabled
VOTE_ERR_FCNT_OEN_X	2	Enables reporting of video frame count voting error on ERRB pin for pipe X (Frame CNT is sent in last line).	0b0: Reporting disabled 0b1: Reporting enabled
SGMII_INT_OEN	1	Enables reporting of SGMII interrupt on ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
SGMII_DEC_ERR_OEN	0	Enables reporting of SGMII decoding error on ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

REG1 (0x41)*

BIT	7	6	5	4	3	2	1	0
Field	ALT_DEV_ADDR_0[6:0]							–
Reset	0b1000100							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_DEV_ADDR_0	7:1	I²C/UART Alternative Device Address 0 selected by CFG pin	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 . . 0b1000000: I²C write/read address is 0x80/0x81 0b1000010: I²C write/read address is 0x84/0x85 0b1000100: I²C write/read address is 0x88/0x89 0b1100000: I²C write/read address is 0xC0/0xC1 0b1100010: I²C write/read address is 0xC4/0xC5 0b1100100: I²C write/read address is 0xC8/0xC9 0b0100000: I²C write/read address is 0x40/0x41 0b0100010: I²C write/read address is 0x44/0x45 . . 0b1111111: I²C write/read address is 0xFE/0xFF

REG2 (0x42)*

BIT	7	6	5	4	3	2	1	0
Field	ALT_DEV_ADDR_1[6:0]							–
Reset	0b1000110							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
ALT_DEV_ADDR_1	7:1	I²C/UART Alternative Device Address 1 selected by CFG pin	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 . . 0b1000000: I²C write/read address is 0x80/0x81 0b1000010: I²C write/read address is 0x84/0x85 0b1000100: I²C write/read address is 0x88/0x89 0b1100000: I²C write/read address is 0xC0/0xC1 0b1100010: I²C write/read address is 0xC4/0xC5 0b1100100: I²C write/read address is 0xC8/0xC9 0b0100000: I²C write/read address is 0x40/0x41 0b0100010: I²C write/read address is 0x44/0x45 . . 0b1111111: I²C write/read address is 0xFE/0xFF

REG3 (0x43)*

BIT	7	6	5	4	3	2	1	0
Field	ALT_DEV_ADDR_2[6:0]							–
Reset	0b1100100							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_DEV_ADDR_2	7:1	I²C/UART Alternative Device Address 2 selected by CFG pin	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 . . 0b1000000: I²C write/read address is 0x80/0x81 0b1000010: I²C write/read address is 0x84/0x85 0b1000100: I²C write/read address is 0x88/0x89 0b1100000: I²C write/read address is 0xC0/0xC1 0b1100010: I²C write/read address is 0xC4/0xC5 0b1100100: I²C write/read address is 0xC8/0xC9 0b0100000: I²C write/read address is 0x40/0x41 0b0100010: I²C write/read address is 0x44/0x45 . . 0b1111111: I²C write/read address is 0xFE/0xFF

REG4 (0x44)*

BIT	7	6	5	4	3	2	1	0
Field	ALT_DEV_ADDR_3[6:0]							–
Reset	0b1100110							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
ALT_DEV_ADDR_3	7:1	I²C/UART Alternative Device Address 3 selected by CFG pin	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 . . 0b1000000: I²C write/read address is 0x80/0x81 0b1000010: I²C write/read address is 0x84/0x85 0b1000100: I²C write/read address is 0x88/0x89 0b1100000: I²C write/read address is 0xC0/0xC1 0b1100010: I²C write/read address is 0xC4/0xC5 0b1100100: I²C write/read address is 0xC8/0xC9 0b0100000: I²C write/read address is 0x40/0x41 0b0100010: I²C write/read address is 0x44/0x45 . . 0b1111111: I²C write/read address is 0xFE/0xFF

REG5 (0x45)*

BIT	7	6	5	4	3	2	1	0
Field	–	DP_AUX_MSG_INT_POLARITY	DP_AUX_MSG_INT_PIN_EN	DP_AUX_MSG_INT_PIN_SEL[1:0]		VID_DUP_X_Y	DUAL_LINK_MODE	USE_ALT_DEV_ADDR
Reset	–	0b1	0b0	0x3		0b0	0b0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DP_AUX_MSG_INT_POLARITY	6	DP AUX Message interrupt pin polarity.	0x0: Active low. 0x1: Active high.
DP_AUX_MSG_INT_PIN_EN	5	DP AUX Message interrupt pin enable.	0x0: DP AUX Message interrupt pin disabled 0x1: DP AUX Message interrupt pin enabled
DP_AUX_MSG_INT_PIN_SEL	4:3	DP AUX Message interrupt pin select.	0x0: Use ALT1 pin (MFP0) for DP_AUX_MSG_INT 0x1: Use ALT2 pins (MFP10) for DP_AUX_MSG_INT 0x2: Use ALT3 pins (MFP16) for DP_AUX_MSG_INT 0x3: Use (MFP25) for DP_AUX_MSG_INT
VID_DUP_X_Y	2	Duplicate video from Pipeline X to Pipeline Y at the output of FIFO	0x0: Duplication disabled 0x1: Duplication enabled
DUAL_LINK_MODE	1	Enables GMSL2 dual link mode Both links are reset momentarily when this bit's value is changed	0x0: Dual link mode disabled 0x1: Dual link mode enabled
USE_ALT_DEV_ADDR	0	Enables using alternative device addresses.	0x0: Alternative device addresses are not used 0x1: Alternative device addresses are used

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REG6 (0x46)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	CFG0_CONFIG_S[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CFG0_CONFIG_S	2:0	Saved value of config_pin_0[2:0] for alt_dev_addr selection. Note: Do not write to this register.

REG7 (0x47)*

BIT	7	6	5	4	3	2	1	0
Field	CC_PIN_SEL_A[1:0]		CC_PIN_SEL_B[1:0]		RSVD[1:0]		RSVD	PCLKDETLOST_WO_PXRSTB
Reset	0x0		0x0		0x3		0x0	0x0
Access Type	Write, Read		Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC_PIN_SEL_A	7:6	Selects pins connected to GMSL CC on this link	0b00: CC pins 0b01: PT1 pins 0b10: PT2 pins 0b11: Reserved
CC_PIN_SEL_B	5:4	Selects pins connected to GMSL CC on this link	0b00: CC pins 0b01: PT1 pins 0b10: PT2 pins 0b11: Reserved
PCLKDETLOST_WO_PXRSTB	0	When it is 1, *PCLKDET_LOST registers assert without checking if video is reset or not. When 0, they assert if pclkdet is gone and video is not reset.	0x0: Check if video is reset or not and do not assert if it is reset. 0x1: Do not check if video is reset or not and assert everytime if pclkdet is lost.

REG8_INTR (0x48)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VTX_Y_PCLKDETLOST_OEN	VTX_X_PCLKDETLOST_OEN	SGMII_STOP_ERR_OEN	SGMII_PRBS_ERR_OEN
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VTX_Y_PCLKDETLOST_OEN	3	Enables reporting of VTX_Y_PCLKDETLOST on ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VTX_X_PCLKDETLOST_OEN	2	Enables reporting of VTX_X_PCLKDETLOST on ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_STOP_ERR_OEN	1	Enables reporting of SGMII stop error on ERRB pin. Set SGMII_STOP_ERR=1 to clear.	0b0: Reporting disabled 0b1: Reporting enabled
SGMII_PRBS_ERR_OEN	0	Enables reporting of SGMII PRBB error on ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

REG9 (0x49)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VTX_Y_PCLKDETLOST	VTX_X_PCLKDETLOST	–	–
Reset	–	–	–	–	0b0	0b0	–	–
Access Type	–	–	–	–	Write 1 to Clear, Read	Write 1 to Clear, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VTX_Y_PCLKDETLOST	3	VTX_Y_PCLKDETLOST register. Modify PCLKDETLOST_WO_PXRSTB to change the behavior. Write 1 to clear.	0b0: Pclkdet is not lost 0b1: Pclkdet is lost
VTX_X_PCLKDETLOST	2	VTX_X_PCLKDETLOST register. Modify PCLKDETLOST_WO_PXRSTB to change the behavior. Write 1 to clear.	0b0: Pclkdet is not lost 0b1: Pclkdet is lost

REG12 (0x4C)*

BIT	7	6	5	4	3	2	1	0
Field	PT2_PIN_SEL_A[1:0]		PT2_PIN_SEL_B[1:0]		PT1_PIN_SEL_A[1:0]		PT1_PIN_SEL_B[1:0]	
Reset	0x2		0x2		0x1		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PT2_PIN_SEL_A	7:6	Selects pins connected to GMSL PT2 on this link	0b00: CC pins 0b01: PT1 pins 0b10: PT2 pins 0b11: Reserved
PT2_PIN_SEL_B	5:4	Selects pins connected to GMSL PT2 on this link	0b00: CC pins 0b01: PT1 pins 0b10: PT2 pins 0b11: Reserved
PT1_PIN_SEL_A	3:2	Selects pins connected to GMSL PT1 on this link	0b00: CC pins 0b01: PT1 pins 0b10: PT2 pins 0b11: Reserved
PT1_PIN_SEL_B	1:0	Selects pins connected to GMSL PT1 on this link	0b00: CC pins 0b01: PT1 pins 0b10: PT2 pins 0b11: Reserved

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TX0 (0x50, 0x60)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD	RSVD	–	RSVD	TX_FEC_EN	–
Reset	0b01		0b1	0b0	–	0b1	0b1	–
Access Type					–		Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
TX_FEC_EN	1	Enables forward error correction (FEC) in forward direction FEC is automatically enabled in GMSL3 mode according to the latched CFG pin value at power-up.	0x0: FEC is off 0x1: FEC is on

TX1 (0x51, 0x61)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
Reset	0b0	–	–	0b0	–	–	0b0	0b0
Access Type		–	–	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_EN	4	Error Generator Enable	0b0: Error generator disabled 0b1: Error generator enabled

TX2 (0x52, 0x62)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0b00		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error generator average bit-error rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits

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BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_BURST	3:1	Selects the error generator burst-error length in bits For example, if the bitfield value is 0b100, the burst-error length is 8 bits. Thus, each time an 8-bit error burst is generated, there is an error in the first and the last bit of the 8-bit window and the probability of an error in each of the remaining 6 bits is 50%.	0b000: 1 bit 0b001: 2 bits 0b010: 3 bits 0b011: 4 bits 0b100: 8 bits 0b101: 12 bits 0b110: 16 bits 0b111: 20 bits
ERRG_PER	0	Error generator error distribution selection	0b0: Pseudorandom 0b1: Periodic

TX3 (0x53, 0x63)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		TX_FEC_ACTIVE	RSVD[1:0]		TIMEOUT[2:0]		
Reset	0b01		0b0	0b10		0b100		
Access Type			Read Only			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_FEC_ACTIVE	5	Indicates FEC is active Communication with deserializer must be established for this bit to be set by hardware.	0x0: Not active 0x1: Actively generating FEC bits
TIMEOUT	2:0	ARQ timeout duration multiplier Multiplies a timeout base constant to set the ARQ timeout. (When daisy chain length is 3 or 4, this is internally incremented by 1)	0b000: 0.5 x timeout base 0b001: 1.0 x timeout base 0b010: 1.5 x timeout base 0b011: 2.0 x timeout base 0b100: 2.5 x timeout base 0b101: 3.0 x timeout base 0b110: 3.5 x timeout base 0b111: 4.0 x timeout base

RX0 (0x54, 0x64)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		RSVD	RSVD	PKT_CNT_SEL[3:0]			
Reset	0b00		0b0	0b0	0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Selects the sub-type of low-bandwidth (LBW) packets to count at PKT_CNT (register LCTRL5)	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_SEL	3:0	Selects the type of received packets to count at PKT_CNT (register LCTRL5).	0x0: None 0x1: Reserved 0x2: AUDIO 0x3: INFO Frame 0x4: SPI 0x5: I^2C 0x6: UART 0x7: GPIO 0x8: AHDCP 0x9: Reserved 0xA: I^2C/UART PT1 0xB: I^2C/UART PT2 0xC: Reserved 0xD: Reserved 0xE: All 0xF: Unknown and packets with error

RX1 (0x55, 0x65)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD
Reset	0b0	0b0	0b11		0b01		0b0	0b0
Access Type								

RX3 (0x57, 0x67)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type					Read Only			Read Clears All

BITFIELD	BITS	DESCRIPTION
RSVD	3	Link PRBS is synced to incoming data
RSVD	0	Failed word boundary lock (latched)

GPIOA (0x58, 0x68)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RX_FAST_BIDIR_EN	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0b1	0b000001					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_FAST_BIDIR_EN	7	GPIO fast-direction switch for bidirectional IO.	0b0: Fast-direction switch disabled 0b1: Fast-direction switch enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_CASC	6	Allows multiple pin transitions to be transmitted in the same packet.	0b0: Multiple pin transitions not allowed 0b1: Multiple pin transitions allowed
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward-compensation delay multiplier value

GPIOB (0x59, 0x69)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0b10		0b011000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet This allows grouping transitions of different GPIO inputs in a single packet and therefore increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This register needs to match on the serializer and the deserializer. This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse-compensation delay multiplier value

I2C_0 (0x70, 0x80)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	0b0	0b10		–	0b011		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I^2C-to-I^2C slave setup and hold-time setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I^2C slave. Set this according to the I^2C speed mode.	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C Standard-mode speed 0b11: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO	2:0	I^2C-to-I^2C slave timeout setting Internal GMSL I^2C slave times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x71, 0x81)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	0b0	0b101			–	0b010		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	I^2C-to-I^2C master bit-rate setting Configures the I^2C bit rate used by the internal I^2C master (in the device on the remote side from the external I^2C master). Set this according to the I^2C speed mode.	0b000: 9.92Kbps - Set for I^2C standard-mode speed 0b001: 33.2Kbps - Set for I^2C standard-mode speed 0b010: 99.2Kbps - Set for I^2C standard- or Fast-mode speed 0b011: 123Kbps - Set for I^2C Fast-mode speed 0b100: 203Kbps - Set for I^2C Fast-mode speed 0b101: 397Kbps - Set for I^2C Fast- or Fast-mode Plus speed 0b110: 625Kbps - Set for I^2C Fast-mode Plus speed 0b111: 980Kbps - Set for I^2C Fast-mode Plus speed
MST_TO	2:0	I^2C-to-I^2C master timeout setting Internal GMSL I^2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x72, 0x82)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I^2C address translator source A When I^2C device address matches I^2C SRC_A, internal I^2C master (on remote side) replaces the device address by I^2C DST_A.	0bXXXXXXX: Value of I^2C SRC_A

I2C_3 (0x73, 0x83)*

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I^2C address translator destination A See the description of I^2C SRC_A.	0bXXXXXXX: Value of I^2C DST_A

I2C_4 (0x74, 0x84)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I^2C address translator source B When I^2C device address matches I^2C SRC_B, internal I^2C master (on remote side) replaces the device address by I^2C DST_B.	0bXXXXXXX: Value of I^2C SRC_B

I2C_5 (0x75, 0x85)*

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I^2C address translator destination B. See the description of I^2C SRC_B.	0bXXXXXXX: Value of I^2C DST_B

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I2C_6 (0x76, 0x86)*

BIT	7	6	5	4	3	2	1	0
Field	DIS_REM_CC	–	–	MULTI_REM_MST_DIS	I2C_AUTO_CFG	–	I2C_SRC_CNT[1:0]	
Reset	0b0	–	–	0b1	0b1	–	0b00	
Access Type	Write, Read	–	–	Write, Read	Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_REM_CC	7	Disables remote control-channel link on this link	0b0: Remote control channel enabled 0b1: Remote control channel disabled
MULTI_REM_MST_DIS	4	Disable multi-master I2C operation in daisy chain for main control channel	0x0: Support multiple uCs on DES-side 0x1: Support single uC on DES-side, legacy behavior
I2C_AUTO_CFG	3	When this bit is set to 1, I^2C-to-I^2C number of links is determined based on daisy-chain lock status automatically. In daisy-chain mode, responses from all connected and locked I^2C channels are expected, otherwise, a response from a single I^2C channel is expected.	0b0: Number of I^2C-to-I^2C links is set by the I^2C SRC_CNT setting 0b1: Daisy-chain lock status automatically determines the number of I^2C-to-I^2C links
I2C_SRC_CNT	1:0	I^2C-to-I^2C number of links (valid when I2C_AUTO_CFG = 0) Set this to (N - 1) when expecting I^2C response from N remote I^2C transmitters. (usually the same as the number of remote devices connected to this device).	0b00: One deserializer connected 0b01: Two deserializers connected 0b10: Three deserializers connected 0b11: Four deserializers connected

UART_0 (0x78, 0x88)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		–	–	–	REM_MS_EN
Reset	0b01		0b10		–	–	–	0b0
Access Type					–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_MS_EN	0	Enables UART bypass-mode control by remote GPIO pin When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, the chip is in bypass mode, otherwise, the chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin

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PT_0 (0x79, 0x89)*

BIT	7	6	5	4	3	2	1	0
Field	PT_I2C_SRC_CNT_2[1:0]		PT_I2C_SRC_CNT_1[1:0]		–	–	CC_2_EN	CC_1_EN
Reset	0b00		0b00		–	–	0b0	0b0
Access Type	Write, Read		Write, Read		–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PT_I2C_SRC_CNT_2	7:6	I^2C-to-I^2C number of links (valid when PT_I2C_AUTO_CFG_2 = 0) Set this to (N - 1) when expecting I^2C response from N remote I^2C transmitters. (usually the same as the number of remote devices connected to this device)	0b00: One deserializer connected 0b01: Two deserializers connected 0b10: Three deserializers connected 0b11: Four deserializers connected
PT_I2C_SRC_CNT_1	5:4	I^2C-to-I^2C number of links (valid when PT_I2C_AUTO_CFG_1 = 0) Set this to (N - 1) when expecting I^2C response from N remote I^2C transmitters. (usually the same as the number of remote devices connected to this device)	0b00: One deserializer connected 0b01: Two deserializers connected 0b10: Three deserializers connected 0b11: Four deserializers connected
CC_2_EN	1	Enable pass-through control Channel 2 (SDA2/RX2, SCL2/TX2) on this link	0b0: Pass-through Channel 2 disabled 0b1: Pass-through Channel 2 enabled
CC_1_EN	0	Enable pass-through control Channel 1 (SDA1/RX1, SCL1/TX1) on this link	0b0: Pass-through Channel 1 disabled 0b1: Pass-through Channel 1 enabled

PT_2 (0x7B, 0x8B)

BIT	7	6	5	4	3	2	1	0
Field	PT_SRC_1[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
PT_SRC_1	7:1	I^2C address translator source for pass-through I^2C Channel 1 on this link When I^2C device address matches PT_SRC_1, internal I^2C master replaces the device address by PT_DST_1.	0bXXXXXXX: Value of I^2C PT_SRC_1

PT_3 (0x7C, 0x8C)

BIT	7	6	5	4	3	2	1	0
Field	PT_DST_1[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION	DECODE
PT_DST_1	7:1	I²C address translator destination for pass-through I²C Channel 1 on this link When I²C device address matches PT_SRC_1, internal I²C master replaces the device address by PT_DST_1.	0bXXXXXXX: Value of I²C PT_DST_1

PT_4 (0x7D, 0x8D)

BIT	7	6	5	4	3	2	1	0
Field	PT_SRC_2[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
PT_SRC_2	7:1	I²C address translator source for pass-through I²C Channel 2 on this link When I²C device address matches PT_SRC_2, internal I²C master replaces the device address by PT_DST_2.	0bXXXXXXX: Value of I²C PT_SRC_2

PT_5 (0x7E, 0x8E)

BIT	7	6	5	4	3	2	1	0
Field	PT_DST_2[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
PT_DST_2	7:1	I²C address translator destination for pass-through I²C Channel 2 on this link When I²C device address matches PT_SRC_2, internal I²C master replaces the device address by PT_DST_2.	0bXXXXXXX: Value of I²C PT_DST_2

I2C_8 (0x7F, 0x8F)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	MULTI_REM_MST_EN_2	MULTI_REM_MST_EN_1	DIS_REM_I2C_DES_3	DIS_REM_I2C_DES_2	DIS_REM_I2C_DES_1	DIS_REM_I2C_DES_0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MULTI_REM_MST_EN_2	5	Enable multi-master I2C operation in daisy chain for pass-through 2	0x0: Support single uC on DES-side, legacy behavior 0x1: Support multiple uCs on DES-side

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BITFIELD	BITS	DESCRIPTION	DECODE
MULTI_REM_MST_EN_1	4	Enable multi-master I2C operation in daisy chain for pass-through 1	0x0: Support single uC on DES-side, legacy behavior 0x1: Support multiple uCs on DES-side
DIS_REM_I2C_DES_3	3	When I2C control channel is used, set this to 1 if DIS_REM_CC=1 at the fourth DES on this link	0x0: DIS_REM_CC=0 at the fourth DES 0x1: DIS_REM_CC=1 at the fourth DES
DIS_REM_I2C_DES_2	2	When I2C control channel is used, set this to 1 if DIS_REM_CC=1 at the third DES on this link	0x0: DIS_REM_CC=0 at the third DES 0x1: DIS_REM_CC=1 at the third DES
DIS_REM_I2C_DES_1	1	When I2C control channel is used, set this to 1 if DIS_REM_CC=1 at the second DES on this link	0x0: DIS_REM_CC=0 at the second DES 0x1: DIS_REM_CC=1 at the second DES
DIS_REM_I2C_DES_0	0	When I2C control channel is used, set this to 1 if DIS_REM_CC=1 at the first DES on this link	0x0: DIS_REM_CC=0 at the first DES 0x1: DIS_REM_CC=1 at the first DES

CC_0 (0x90)*

BIT	7	6	5	4	3	2	1	0
Field	UART_ARB_TO[1:0]		EN_I2C_LOOPBACK	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	0b01		0b0	0b0	0b0	0b01		0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
UART_ARB_TO	7:6	UART link arbitration timeout configuration Only one link is selected as UART source for output data at any time. When no UART packets are received for the set duration, the next link as UART source is selected according to the next received UART frame.	0x0: 16µs 0x1: 64µs 0x2: 1ms 0x3: Reserved
EN_I2C_LOOPBACK	5	Enables I^2C loopback between links	0x0: I^2C loopback disabled 0x1: I^2C loopback enabled
LOC_MS_EN	4	Enables UART bypass mode control by local MFP pin Set to use MFP pin as MS pin (UART mode select). When MS is high, the chip is in bypass mode, otherwise, the chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR	3	Selects whether or not to receive and send parity bit in bypass mode	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO	2:1	UART soft-bypass timeout duration When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power-down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled

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BITFIELD	BITS	DESCRIPTION	DECODE
BYPASS_EN	0	Enables UART soft-bypass mode Bypass mode remains active as long as there is UART activity. When there is no UART activity for a selected duration (configured by BYPASS_TO bitfield), the device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

CC_6 (0x96)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_1	DIS_PAR_1	SLV_SH_PT_1[1:0]		I2CSEL_1	SLV_TO_PT_1[2:0]		
Reset	0b0	0b0	0b10		0b1	0b011		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_1	7	Use custom UART bit rate (BITLEN_PT_1 register) in pass-thru UART channel #1	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_1	6	Disables parity bit in pass-through UART Channel 1	0b0: Parity bit enabled 0b1: Parity bit disabled
SLV_SH_PT_1	5:4	Pass-through I^{2}C-to-I^{2}C slave setup and hold time setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I^{2}C slave. Set this according to the I^{2}C speed mode.	0b00: Set for I^{2}C Fast-mode Plus speed 0b01: Set for I^{2}C Fast-mode speed 0b10: Set for I^{2}C standard-mode speed 0b11: Reserved
I2CSEL_1	3	I^{2}C/UART mode selection for pass-through Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: UART mode 0b1: I^{2}C mode
SLV_TO_PT_1	2:0	Pass-through I^{2}C-to-I^{2}C slave timeout setting Internal GMSL I^{2}C slave times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

CC_7 (0x97)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_PT_1[2:0]			RSVD	MST_TO_PT_1[2:0]		
Reset	0b0	0b101			0b0	0b010		
Access Type		Write, Read				Write, Read		

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BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT_1	6:4	Pass-through I²C-to-I²C master bit rate setting, configures the I²C bit rate used by the internal I²C master (in the device on the remote side from the external I²C master). Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_PT_1	2:0	Pass-through I²C-to-I²C master timeout setting Internal GMSL I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

CC_8 (0x98)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	SLV_SH_PT_2[1:0]		I2CSEL_2	SLV_TO_PT_2[2:0]		
Reset	0b0	0b0	0b10		0b1	0b011		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Use custom UART bit rate (BITLEN_PT_2 register) in pass-thru UART channel #2	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_2	6	Disables parity bit in pass-through UART Channel 2	0b0: Parity bit enabled 0b1: Parity bit disabled
SLV_SH_PT_2	5:4	Pass-through I²C-to-I²C slave setup and hold time setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C slave. Set this according to the I²C speed mode.	0b00: Set for I²C Fast-mode Plus speed 0b01: Set for I²C Fast-mode speed 0b10: Set for I²C standard-mode speed 0b11: Reserved
I2CSEL_2	3	I²C/UART mode selection for pass-through Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: UART 0b1: I²C
SLV_TO_PT_2	2:0	Pass-through I²C-to-I²C slave timeout setting Internal GMSL I²C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

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CC_9 (0x99)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_PT_2[2:0]			RSVD	MST_TO_PT_2[2:0]		
Reset	0b0	0b101			0b0	0b010		
Access Type		Write, Read				Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT_2	6:4	Pass-through I²C-to-I²C master bit-rate setting, configures the I²C bit rate used by the internal I²C master (in the device on the remote side from the external I²C master). Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_PT_2	2:0	Pass-through I²C-to-I²C master timeout setting Internal GMSL I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

CC_10 (0x9A)*

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_OVER_AUX_TO_CC_PINS_EN	–	–	I2C_OVER_AUX_TO_GMSL_CC_EN	PT2_PINS_TO_GMSL_CC_EN	PT1_PINS_TO_GMSL_CC_EN	CC_PINS_TO_GMSL_CC_EN
Reset	–	0b0	–	–	0b0	0b0	0b0	0b1
Access Type	–	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_OVER_AUX_TO_CC_PINS_EN	6	Connects I²C-over-AUX channel to CC pins	0b0: I²C-over-AUX is not connected to CC pins 0b1: I²C-over-AUX is connected to CC pins
I2C_OVER_AUX_TO_GMSL_CC_EN	3	Connects I²C-over-AUX channel to GMSL CC channel	0b0: I²C-over-AUX is not connected to GMSL CC 0b1: I²C-over-AUX is connected to GMSL CC
PT2_PINS_TO_GMSL_CC_EN	2	Connects PT2 pins (SDA2_RX2, SCL2_TX2) to GMSL CC channel	0b0: PT2 pins are not connected to GMSL CC 0b1: PT2 pins are connected to GMSL CC

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BITFIELD	BITS	DESCRIPTION	DECODE
PT1_PINS_TO_GMSL_CC_EN	1	Connects PT1 pins (SDA1_RX1, SCL1_TX1) to GMSL CC channel	0b0: PT1 pins are not connected to GMSL CC 0b1: PT1 pins are connected to GMSL CC
CC_PINS_TO_GMSL_CC_EN	0	Connects main CC pins (SDA_RX, SCL_TX) to GMSL CC channel	0b0: CC pins are not connected to GMSL CC 0b1: CC pins are connected to GMSL CC

CC_11 (0x9B)*

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_OVER_AUX_TO_PT1_PINS_EN	EN_PT1_LOOPBACK	PT1_LOOPBACK_TO_GMSL_CC_EN	I2C_OVER_AUX_TO_GMSL_PT1_EN	PT2_PINS_TO_GMSL_PT1_EN	PT1_PINS_TO_GMSL_PT1_EN	CC_PINS_TO_GMSL_PT1_EN
Reset	–	0b0	0b0	0b0	0b0	0b0	0b1	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_OVER_AUX_TO_PT1_PINS_EN	6	Connects I^2C-over-AUX channel to PT1 pins	0b0: I^2C-over-AUX is not connected to PT1 pins 0b1: I^2C-over-AUX is connected to PT1 pins
EN_PT1_LOOPBACK	5	Enables I^2C loopback between links on PT1 channel	0x0: I^2C loopback disabled 0x1: I^2C loopback enabled
PT1_LOOPBACK_TO_GMSL_CC_EN	4	Loopbacks from PT1 channel to main CC channel	0x0: Loopback disabled 0x1: Loopback enabled
I2C_OVER_AUX_TO_GMSL_PT1_EN	3	Connects I^2C-over-AUX channel to GMSL PT1 channel	0b0: I^2C-over-AUX is not connected to GMSL PT1 channel 0b1: I^2C-over-AUX is connected to GMSL PT1 channel
PT2_PINS_TO_GMSL_PT1_EN	2	Connects PT2 pins (SDA2_RX2, SCL2_TX2) to GMSL PT1 channel	0b0: PT2 pins are not connected to GMSL PT1 channel 0b1: PT2 pins are connected to GMSL PT1 channel
PT1_PINS_TO_GMSL_PT1_EN	1	Connects PT1 pins (SDA1_RX1, SCL1_TX1) to GMSL PT1 channel	0b0: PT1 pins are not connected to GMSL PT1 channel 0b1: PT1 pins are connected to GMSL PT1 channel
CC_PINS_TO_GMSL_PT1_EN	0	Connects main CC pins (SDA_RX, SCL_TX) to GMSL PT1 channel	0b0: CC pins are not connected to GMSL PT1 channel 0b1: CC pins are connected to GMSL PT1 channel

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CC_12 (0x9C)*

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_OVER_AUX_TO_PT2_PINS_EN	EN_PT2_LOOPBACK	PT2_LOOPBACK_TO_GMSL_CC_EN	I2C_OVER_AUX_TO_GMSL_PT2_EN	PT2_PINS_TO_GMSL_PT2_EN	PT1_PINS_TO_GMSL_PT2_EN	CC_PINS_TO_GMSL_PT2_EN
Reset	–	0b0	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_OVER_AUX_TO_PT2_PINS_EN	6	Connects I^{2}C-over-AUX channel to PT2 pins	0b0: I^{2}C-over-AUX is not connected to PT2 pins 0b1: I^{2}C-over-AUX is connected to PT2 pins
EN_PT2_LOOPBACK	5	Enables I^{2}C loopback between links on PT2 channel	0x0: I^{2}C loopback disabled 0x1: I^{2}C loopback enabled
PT2_LOOPBACK_TO_GMSL_CC_EN	4	Loopbacks from PT2 channel to main CC channel	0x0: Loopback disabled 0x1: Loopback enabled
I2C_OVER_AUX_TO_GMSL_PT2_EN	3	Connects I^{2}C-over-AUX channel to GMSL PT2 channel.	0b0: I^{2}C-over-AUX is not connected to GMSL PT2 channel 0b1: I^{2}C-over-AUX is connected to GMSL PT2 channel
PT2_PINS_TO_GMSL_PT2_EN	2	Connects PT2 pins (SDA2_RX2, SCL2_TX2) to GMSL PT2 channel.	0b0: PT2 pins are not connected to GMSL PT2 channel 0b1: PT2 pins are connected to GMSL PT2 channel
PT1_PINS_TO_GMSL_PT2_EN	1	Connects PT1 pins (SDA1_RX1, SCL1_TX1) to GMSL PT2 channel.	0b0: PT1 pins are not connected to GMSL PT2 channel 0b1: PT1 pins are connected to GMSL PT2 channel
CC_PINS_TO_GMSL_PT2_EN	0	Connects main CC pins (SDA_RX, SCL_TX) to GMSL PT2 channel.	0b0: CC pins are not connected to GMSL PT2 channel 0b1: CC pins are connected to GMSL PT2 channel

CC_13 (0x9D)*

BIT	7	6	5	4	3	2	1	0
Field	AHCC_AUTO_CFG_B	–	AHCC_SRC_CNT_B[1:0]		AHCC_AUTO_CFG_A	–	AHCC_SRC_CNT_A[1:0]	
Reset	0b1	–	0b00		0b1	–	0b00	
Access Type	Write, Read	–	Write, Read		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
AHCC_AUTO_CFG_B	7	When this bit is set to 1, Auto-HDCP number of sinks on Link B is determined based on daisy-chain lock status automatically.	0b0: Number of I^{2}C-to-I^{2}C links is set by the I^{2}C SRC_CNT setting 0b1: Daisy-chain lock status automatically determines the number of I^{2}C-to-I^{2}C links

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BITFIELD	BITS	DESCRIPTION	DECODE
AHCC_SRC_CNT_B	5:4	Auto-HDCP number of sinks on link B (valid when AHCC_AUTO_CFG_B = 0) Set this to (N - 1) when expecting response from N remote Auto_HDCP transmitters.	0b00: One deserializer connected 0b01: Two deserializers connected 0b10: Three deserializers connected 0b11: Four deserializers connected
AHCC_AUTO_CFG_A	3	When this bit is set to 1, Auto-HDCP number of sinks on Link A is determined based on daisy-chain lock status automatically.	0b0: Number of I²C-to-I²C links is set by the I²C SRC_CNT setting 0b1: Daisy-chain lock status automatically determines the number of I²C-to-I²C links
AHCC_SRC_CNT_A	1:0	Auto-HDCP number of sinks on link A (valid when AHCC_AUTO_CFG_A = 0) Set this to (N - 1) when expecting response from N remote Auto_HDCP transmitters.	0b00: One deserializer connected 0b01: Two deserializers connected 0b10: Three deserializers connected 0b11: Four deserializers connected

CC_14 (0x9E)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PT1_READ_EN	–	–	PT_I2C_AUTO_CFG_2	PT_I2C_AUTO_CFG_1
Reset	–	–	–	0b1	–	–	0b1	0b1
Access Type	–	–	–	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PT1_READ_EN	4	Enable register read back with PT1 channel	
PT_I2C_AUTO_CFG_2	1	When set to 1, I²C-to-I²C number of links is determined based on daisy-chain lock status automatically. In daisy-chain mode, responses from all connected and locked I²C channels are expected, otherwise, a response from a single I²C channel is expected.	0b0: Number of PT2 I²C-to-I²C links is set by the PT_I2C_SRC_CNT_2 setting 0b1: Daisy-chain lock status automatically determines the number of I²C-to-I²C links
PT_I2C_AUTO_CFG_1	0	When set to 1, I²C-to-I²C number of links is determined based on daisy-chain lock status automatically. In daisy-chain mode, responses from all connected and locked I²C channels are expected, otherwise, a response from a single I²C channel is expected.	0b0: Number of PT1 I²C-to-I²C links is set by the PT_I2C_SRC_CNT_1 setting 0b1: Daisy-chain lock status automatically determines the number of I²C-to-I²C links

CC_15 (0x9F)*

BIT	7	6	5	4	3	2	1	0
Field	PASS_KEY[7:0]							
Reset	0x55							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
PASS_KEY	7:0	When the value of this field is 0x55, the registers are writable. Otherwise write transactions are blocked.	0x55: Registers are writable Others: Registers are not writable

TX0 (0xA0, 0xA4)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	–	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Access Type	Write, Read	–			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Transmits CRC Enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TX1 (0xA1, 0xA5)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TX3 (0xA3, 0xA7)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TX_STR_SEL[1:0]	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_STR_SEL	1:0	Stream ID used in packets transmitted from this channel	0bXX: Stream ID for packets from this channel

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TR0 (0xB0, 0xB8, 0xC8)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0xB1, 0xB9, 0xC9)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR2 (0xB2, 0xBA, 0xCA)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel Default value is set by CFG0 at power-up.	0bXXX: Source ID for packets from this channel

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TR3 (0xB3, 0xBB, 0xCB)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from the selected sources Each bit indicates if packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, packets with source ID equal to 0 and 3 are received.	0x00: Block all packets 0x01: Receive packets from source ID 0 0x02: Receive packets from source ID 1 0x03: Receive packets from source IDs 0 and 1 . . 0xFF: Receive packets from all source IDs

ARQ0 (0xB4, 0xBC, 0xCC)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	–	DIS_DBL_ACK_RETX	–	ARQ_EN
Access Type					–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX	2	Disables retransmission due to receiving same acknowledge twice	0b0: Enabled 0b1: Disabled
ARQ_EN	0	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0xB5, 0xBD, 0xCD)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_SEL	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_SEL	7	Selects the link adapter connects to	0x0: Connect to Link A 0x1: Connect to Link B
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

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ARQ2 (0xB6, 0xBE, 0xCE)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmitting limit (MAX_RT) for one packet in this channel on Link A	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel on Link A	0xXX: Count of retransmissions for this channel

TR0 (0xC0)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0xC1)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

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BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR2 (0xC2)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel Default value is set by CFG0 at power-up.	0bXXX: Source ID for packets from this channel

TR3 (0xC3)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from the selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: Block all packets 0x01: Receive packets from source ID 0 0x02: Receive packets from source ID 1 0x03: Receive packets from source IDs 0 and 1 . . 0xFF: Receive packets from all source IDs

TR0 (0xD0, 0xD8, 0xE0, 0xE8, 0xF0)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0xD1, 0xD9, 0xE1, 0xE9, 0xF1)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR2 (0xD2, 0xDA, 0xE2, 0xEA, 0xF2)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel Default value is set by CFG0 at power-up.	0bXXX: Source ID for packets from this channel

TR3 (0xD3, 0xDB, 0xE3, 0xEB, 0xF3)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from the selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: Block all packets 0x01: Receive packets from source ID 0 0x02: Receive packets from source ID 1 0x03: Receive packets from source IDs 0 and 1 . . 0xFF: Receive packets from all source IDs

ARQ0 (0xD4, 0xDC, 0xE4, 0xEC, 0xF4)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	DIS_DBL_ACK_RETX_B	DIS_DBL_ACK_RETX_A	ARQ_EN_B	ARQ_EN_A
Access Type					Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_DBL_ACK_RETX_B	3	Disables retransmission due to receiving same acknowledge twice	0b0: Enabled 0b1: Disabled
DIS_DBL_ACK_RETX_A	2	Disables retransmission due to receiving same acknowledge twice	0b0: Enabled 0b1: Disabled
ARQ_EN_B	1	Enables ARQ on Link B	0b0: ARQ disabled 0b1: ARQ enabled
ARQ_EN_A	0	Enables ARQ on Link A	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0xD5, 0xDD, 0xE5, 0xED, 0xF5)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
Access Type	–						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

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ARQ2 (0xD6, 0xDE, 0xE6, 0xEE, 0xF6)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_A	RT_CNT_A[6:0]						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_A	7	Reached maximum retransmitting limit (MAX_RT) for one packet in this channel on Link A	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_A	6:0	Total retransmission count in this channel on Link A	0xXX: Count of retransmissions for this channel

ARQ3 (0xD7, 0xDF, 0xE7, 0xEF, 0xF7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_B	RT_CNT_B[6:0]						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_B	7	Reached maximum retransmitting limit (MAX_RT) for one packet in this channel on Link B	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel on Link B	0xXX: Count of retransmissions for this channel

TX0 (0xF8)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

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TX1 (0xF9)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TX2 (0xFA)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_SEL	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_SEL	7	Selects the link adapter connects to	0x0: Connect to Link A 0x1: Connect to Link B

VIDEO_TX0 (0x100, 0x110)*

BIT	7	6	5	4	3	2	1	0
Field	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		–	VID_LINK_SEL[1:0]		VID_TX_EN
Access Type	Write, Read	Write, Read	Write, Read		–	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_SEL	7	Line-CRC checksum generation with DE or HS	0b0: Use DE for line CRC 0b1: Use HS for line CRC
LINE_CRC_EN	6	Line-CRC Enable Generates a CRC code for the video line and send it to the receiver side for comparison	0b0: Line CRC disabled 0b1: Line CRC enabled
ENC_MODE	5:4	HS, VS, and DE encoding mode	0b00: HS, VS, and DE encoding off 0b01: HS, VS, and DE encoding on, color bits always sent 0b10: HS, VS, and DE encoding on, color bits sent only when DE is high 0b11: HS, VS, and DE encoding on, color bits sent only when HS is high

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BITFIELD	BITS	DESCRIPTION	DECODE
VID_LINK_SEL	2:1	Selects the link that this video port connects to	0x0: Connect to Link A 0x1: Connect to Link B 0x2: Connect to Link A and Link B 0x3: Reserved
VID_TX_EN	0	Video transmit enable for this video port	0b0: Video transmit port disabled 0b1: Video transmit port enabled

VIDEO_TX1 (0x101, 0x111)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		BPP[5:0]					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BPP	5:0	Color bits per pixel (RGB888 = 24)	0bXXXXXX: Number of bits per pixel

VIDEO_TX2 (0x102, 0x112)*

BIT	7	6	5	4	3	2	1	0
Field	PCLKDET_A	DRIFT_ERR_A	OVERFLOW_A	FIFO_WARN_A	RSVD	LIM_HEART	RSVD	RSVD
Access Type	Read Only	Read Clears All	Read Clears All	Read Clears All		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PCLKDET_A	7	PCLK detected	0b0: Video transmit PCLK not detected 0b1: Video transmit PCLK detected
DRIFT_ERR_A	6	VID_TX PCLK drift error detected After the video pipeline starts, PCLK cannot drift more than a certain amount without restarting the subsystem.	0b0: Video transmit PCLK drift error not detected 0b1: Video transmit PCLK drift error detected
OVERFLOW_A	5	VID_TX FIFO has overflowed Video input throughput may be too high, bandwidth allocation on GMSL link for video may not be enough.	0b0: Video transmit FIFO has not overflowed 0b1: Video transmit FIFO has overflowed
FIFO_WARN_A	4	VID_TX FIFO is more than half full	0b0: Video transmit FIFO is less than or equal to half full 0b1: Video transmit FIFO is more than half full
LIM_HEART	2	Disables heartbeat during blanking Use together with SEQ_MISS_EN and DIS_PKT_DET registers in deserializer.	0b0: Heartbeat enabled during blanking 0b1: Hearbeat disabled during blanking

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VIDEO_TX6 (0x106, 0x116)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MASK_VIDEO_DE	RSVD[5:0]					
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION
MASK_VIDEO_DE	6	Mask video with DE

VIDEO_TX8 (0x108, 0x118)

BIT	7	6	5	4	3	2	1	0
Field	PCLKDET_B	DRIFT_ERR_B	OVERFLOW_B	FIFO_WARN_B	–	–	–	RSVD
Access Type	Read Only	Read Clears All	Read Clears All	Read Clears All	–	–	–	

BITFIELD	BITS	DESCRIPTION	DECODE
PCLKDET_B	7	PCLK detected	0b0: Video-transmit PCLK not detected 0b1: Video-transmit PCLK detected
DRIFT_ERR_B	6	VID_TX PCLK drift error detected. After the video pipeline starts, PCLK cannot drift more than a certain amount without restarting the subsystem.	0b0: Video-transmit PCLK drift error not detected 0b1: Video-transmit PCLK drift error detected
OVERFLOW_B	5	VID_TX FIFO has overflowed Video input throughput may be too high, bandwidth allocation on GMSL link for video may not be enough.	0b0: Video transmit FIFO has not overflowed 0b1: Video transmit FIFO has overflowed
FIFO_WARN_B	4	VID_TX FIFO is more than half full	0b0: Video transmit FIFO is less than or equal to half full 0b1: Video transmit FIFO is more than half full

AUDIO_TX0 (0x140, 0x150)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
INV_SCK	3	Invert SCK (when using local I^2S interface)	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS	2	Invert WS (when using local I^2S interface). This inverts the edge on which an audio sample frame is defined and captured.	0b0: Low/High WS pulse marks sample 0b1: High/Low WS pulse marks sample
FORCE_AUD	1	Forces audio data to zero	0b0: Normal audio data 0b1: Audio data forced to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
AUD_SINK_SRC	0	Sink-sourced mode enable for Audio Tx For use on the deserializer side when forward audio clock is the master.	0b0: Transmit audio in normal mode 0b1: Transmit audio in sink-sourced mode

AUDIO_TX1 (0x141, 0x151)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	AUD_HDCP_SEL[1:0]	
Access Type			Write, Read		Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_STR_TX	5:4	Audio stream ID	0b00: Use stream ID 0 0b01: Use stream ID 1 0b10: Use stream ID 2 0b11: Use stream ID 3
AUD_DRIFT_DET_EN	3	Enable audio clock drift detection Resets subsystem on SCK frequency drift and reports it.	0b0: Audio clock drift detection disabled 0b1: Audio clock drift detection enabled
AUD_INF_PER	2	Audio periodic info frame transmission enable	0b0: Audio periodic info frame transmission disabled 0b1: Audio periodic info frame transmission enabled
AUD_HDCP_SEL	1:0	Select the HDCP encryption engine that encrypts this audio channel	0x0: HDCP_X 0x1: HDCP_Y 0x2: HDCP_Z 0x3: HDCP_U

AUDIO_TX5 (0x145, 0x155)

BIT	7	6	5	4	3	2	1	0
Field	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_DRIFT_ERR	7	Audio clock frequency drift detected	0b0: Audio clock frequency drift not detected 0b1: Audio clock frequency drift detected
AUD_FIFO_WARN	6	Audio FIFO is more than half full	0b0: Audio FIFO is less than or equal to half full 0b1: Audio FIFO is more than half full
AUD_OVERFLOW	5	Audio buffer overflow detected	0b0: Audio buffer overflow not detected 0b1: Audio buffer overflow detected
ACLKDET	4	Audio clock detected	0b0: Audio clock not detected 0b1: Audio clock detected

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AUDIO_TX7 (0x147, 0x157)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_SEL	7	Audio PRBS clock selection, set to 0 in sink-sourced mode	0b0: SCK selected 0b1: Internal oscillator clock selected (150MHz)
PRBSEN_AUD	6	Audio PRBS enable	0b0: Audio PRBS disabled 0b1: Audio PRBS enabled

AUDIO_TX8 (0x148, 0x158)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_WS_LEN	7	Selects the length of the generated WS pulse	0b0: 256 data bits per WS cycle 0b1: 32 data bits per WS cycle
PRBS_WS_GEN	6	Audio PRBS WS generation enable	0b0: Audio PRBS WS generation disabled 0b1: Audio PRBS WS generation enabled

AUDIO_RX1 (0x160, 0x180)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
Access Type	Write, Read				Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_RX_SINK_SRC	7	Sink-sourced mode enable for Audio Rx For use on the serializer side.	0b0: Received audio in normal mode 0b1: Received audio in sink-sourced mode
INV_SCK_RX	3	Invert SCK at I^2S output	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS_RX	2	Invert WS at I^2S output	0b0: Do not invert WS 0b1: Invert WS
AUD_EN_RX	0	Audio receiver adapter enable	0b0: Audio receiver disabled 0b1: Audio receiver enabled

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AUDIO_RX4 (0x163, 0x183)

BIT	7	6	5	4	3	2	1	0
Field	APRBS_ERR[7:0]							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_ERR	7:0	Audio PRBS error counter, clears on read	0xXX: Number of audio PRBS errors

AUDIO_RX7 (0x166, 0x186)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
Access Type				Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_CHK_EN	4	Enables audio PRBS checker	0b0: Audio PRBS checker disabled 0b1: Audio PRBS checker enabled
AUD_STRM	3:2	Selected audio stream for reception	0b00: Receive stream ID 0 0b01: Receive stream ID 1 0b10: Receive stream ID 2 0b11: Receive stream ID 3

AUDIO_RX9 (0x168, 0x188)

BIT	7	6	5	4	3	2	1	0
Field	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			
Access Type	Read Clears All	Read Only	Read Only	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_BLK_LEN_ERR	7	Audio Rx block-length error detected	0b0: Received audio block-length error not detected 0b1: Received audio block-length error detected
AUD_LOCK	6	Audio pipeline frequency locked	0b0: Audio pipeline frequency is not locked 0b1: Audio pipeline frequency is locked
AUD_PKT_DET	5	Audio Rx: sufficient packet throughput detected	0b0: Valid audio stream not detected 0b1: Valid audio stream detected
APRBS_VALID	4	Audio PRBS is running	0b0: Audio PRBS is not running 0b1: Audio PRBS is running

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SPI_0 (0x1A0)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0b00		0b00		0b1	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Programs to local ID if filtering packets based on header ID	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_CC_TRG_ID	5:4	ID for GMSL header in SPI control-channel bridge mode	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_IGNR_ID	3	Selects whether SPI should use or ignore header ID to decide on packet acceptance	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_CC_EN	2	Enables control-channel SPI bridge function	0b0: SPI bridge disabled 0b1: SPI bridge enabled
MST_SLVN	1	Selects whether SPI is master or slave	0b0: SPI slave 0b1: SPI master
SPI_EN	0	Enable SPI channel	0b0: SPI channel disabled 0b1: SPI channel enabled

SPI_1 (0x1A1)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						RSVD[1:0]	
Reset	0b000111						0b01	
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Sets the packet size ((2N + 1) bytes) for GMSL SPI packet If this is programmed to a value greater than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes . . 0b111111: Packet size is 127 bytes

SPI_2 (0x1A2)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0b000			0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Hold off GMSL request until this number of extra bytes are received on SPI port.	0b00: No extra bytes 0b01: 1 extra byte 0b10: 2 extra bytes 0b11: 3 extra bytes
FULL_SCK_SETUP	4	Sample MISO after half or full SCK period	0b0: MISO sampled after half SCK period 0b1: MISO sampled after full SCK period
SPI_MOD3_F	3	Allows the suppression of an extra SCK prior to SS deassertion when SPI mode 3 is selected.	0b0: Extra SCK present prior to SS deassertion when in SPI mode 3 0b1: Extra SCK suppressed prior to SS deassertion when in SPI mode 3
SPI_MOD3	2	Selects SPI mode 0 or 3	0b0: SPI mode 0 0b1: SPI mode 3
SPIM_SS2_ACT_H	1	Sets the polarity for SS2 when the SPI is a master.	0b0: Slave select 2 is active low 0b1: Slave select 2 is active high
SPIM_SS1_ACT_H	0	Sets the polarity for SS1 when the SPI is a master	0b0: Slave select 1 is active low 0b1: Slave select 1 is active high

SPI_3 (0x1A3)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between: 1. Assertion of SS and start of SCK pulses 2. End of SCK pulses and deassertion of SS 3. Deassertion of SS and reassertion of SS (if necessary)	0xXX: Number of clock delays

SPI_4 (0x1A4)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time	0xXX: Number of clocks for SCK low time

SPI_5 (0x1A5)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time	0xXX: Number of clocks for SCK high time

SPI_6 (0x1A6)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0b0	0b0	0b0	0b0	0b1	0b1
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	Alternate GPU status register to use for BNE status if GPIO is not available	0b0: Buffer empty 0b1: Buffer not empty
SPIS_RWN	4	Alternate GPU control register to use for Read/Write control if GPIO is not available	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enable GPIO for use as Slave Select 2 output	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
SS_IO_EN_1	2	Enable GPIO for use as Slave Select 1 output	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
BNE_IO_EN	1	Enable GPIO for use as BNE output for SPI data available status	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function
RWN_IO_EN	0	Enable GPIO for use as RO input for control of SPI data movement	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function

SPI_7 (0x1A7)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
Reset	0b0	0b0	–	0b00000				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	SPI Rx buffer overflow flag	0b0: No SPI Rx buffer overflow 0b1: SPI Rx buffer overflow
SPI_TX_OVRFLW	6	SPI Tx buffer overflow flag	0b0: No SPI Tx buffer overflow 0b1: SPI Tx buffer overflow
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer	0bXXXXX: Number of bytes available

SPI_8 (0x1A8)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100ns increments) for GMSL request hold off. 0x00: Disabled	0xXX: Number of 100nS delay increments for GMSL request hold off

SPI_9 (0x1A9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RSVD	SPIM_SCK_FB_MODE
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_FB_MODE	0	Use delayed version of SCK (From MFP Rx) to improve SPI performance	0x0: SCK feedback mode disabled 0x1: SCK feedback mode enabled

SGMII_LINK_0 (0x1B0)*

BIT	7	6	5	4	3	2	1	0
Field	SG_TRGT_ID[1:0]		RSVD[1:0]		SG_HALF_DUPLEX	SG_CMD_RST_N	SG_EN	SG_T_IGNR_ID
Reset	0b00		0b01		0b0	0b0	0b0	0b0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SG_TRGT_ID	7:6	Header value for deserializer	0bXX: Header value for deserializer
SG_HALF_DUPLEX	3	Enable support for encoding half duplex SGMII encodings.	0b0: Full duplex 0b1: Half duplex
SG_CMD_RST_N	2	Software reset for SGMII function	0b0: SGMII is reset. 0b1: SGMII is not reset.
SG_EN	1	Enable SGMII RX/TX through GMSL	0b0: SGMII disabled 0b1: SGMII enabled
SG_T_IGNR_ID	0	Selects if SGMII should use or ignore header ID to decide on packet acceptance.	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets

SGMII_LINK_1 (0x1B1)*

BIT	7	6	5	4	3	2	1	0
Field	SG_LOC_N[5:0]						SG_T_LOC_ID[1:0]	
Reset	0b111000						0b00	
Access Type	Write, Read						Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
SG_LOC_N	7:2	Sets the packet size ((2N + 1) bytes) for GMSL2 SGMII packets. If this is programmed to a value of more than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes ... ... 0b111111: Packet size is 127 bytes
SG_T_LOC_ID	1:0	Program to local ID if this is a DES and device is filtering packets based on header ID.	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3

SGMII_LINK_2 (0x1B2)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SG_BASE_PRIO[1:0]	
Reset	–	–	–	–	–	–	0b01	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SG_BASE_PRIO	1:0	Starting GMSL2 request priority advances by one (if room) if Tx buffer is over half full.	0b00: Priority 1 (high) 0b01: Priority 2 0b10: Priority 3 0b11: Priority 4

SGMII_LINK_3 (0x1B3)*

BIT	7	6	5	4	3	2	1	0
Field	SG_FRAME_DELAY_H	SG_FRAME_UF	SG_TX_OVRFLW	SG_RX_OVRFLW	SG_DYNAMIC_IFG	SG_EARLY_REQ_EN	SG_INTER_FRM_GAP[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b10	
Access Type	Write, Read	Read Clears All	Read Clears All	Read Clears All	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SG_FRAME_DELAY_H	7	Most significant bit of the 9-bit parameter that selects the number of bytes required in Rx buffer prior to starting frame.	0bX: Most significant bit value
SG_FRAME_UF	6	Status flag indicating buffer underflow during SGMII frame	0b0: No buffer underflow 0b1: Buffer underflow
SG_TX_OVRFLW	5	Status flag indicating buffer overflow was detected on GMSL2 Tx buffer.	0b0: No GMSL2 Tx buffer overflow 0b1: GMSL2 Tx buffer overflow
SG_RX_OVRFLW	4	Status flag indicating buffer overflow was detected on GMSL2 Rx buffer.	0b0: No GMSL2 Rx buffer overflow 0b1: GMSL2 Rx buffer overflow
SG_DYNAMIC_IFG	3	When enabled, this bit reduces a minimum frame gap (as defined by interframe_gap) by one if number of bytes in Rx buffer exceeds (frame_delay + ((512 - frame_delay)/2)) at end of frame.	0x0: Do not reduce minimum frame gap by 1 0x1: Reduce minimum frame gap by 1
SG_EARLY_REQ_EN	2	Allow GMSL2 request during GMSL2 transmission, if enough new bytes are available	0x0: Do not allow GMSL2 requests 0x1: Allow GMSL2 requests

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BITFIELD	BITS	DESCRIPTION	DECODE
SG_INTER_FRM_GAP	1:0	Minimum number of interframe symbols	0b00: 4 0b01: 8 0b10: 12 0b11: 16

SGMII_LINK_4 (0x1B4)*

BIT	7	6	5	4	3	2	1	0
Field	SG_FRAME_DELAY_L[7:0]							
Reset	0x40							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SG_FRAME_DELAY_L	7:0	Least significant 8-bits of the 9-bit parameter that selects the number of bytes required in Rx buffer prior to starting frame.	0xXX: Least significant 8-bits value

SGMII_LINK_5 (0x1B5)*

BIT	7	6	5	4	3	2	1	0
Field	MDIO_CLK_DIV[7:0]							
Reset	0x64							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_CLK_DIV	7:0	Number of 150MHz clocks for MDC low/high time	0xXX: Number of SGMII clocks

SGMII_LINK_6 (0x1B6)*

BIT	7	6	5	4	3	2	1	0
Field	MDIO_BUSY	MDIO_RD_VLD	RSVD	MDIO_PHY_ADRS[4:0]				
Reset	0b0	0b0	0b0	0b00000				
Access Type	Read Only	Read Only		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_BUSY	7	Status bit indicating MDIO transaction is in progress.	0b0: MDIO not busy 0b1: MDIO busy
MDIO_RD_VLD	6	Valid flag for read data. Cleared on read	0b0: MDIO read data not valid 0b1: MDIO read data valid
MDIO_PHY_ADRS	4:0	Index selecting 1 of 32 potential PHYs on the MDIO bus	0bXXXXX: PHY index

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SGMII_LINK_7 (0x1B7)*

BIT	7	6	5	4	3	2	1	0
Field	MDIO_WRITE	MDIO_START	RMII_READD_PREAMBLE	MDIO_REG_ADRS[4:0]				
Reset	0b0	0b0	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_WRITE	7	Assert to indicate write operation	0b0: MDIO read 0b1: MDIO write
MDIO_START	6	Assert to start MDIO transaction. Must clear and set to start another transaction. Ignored if MDIO_BUSY status bit is asserted.	0b0: Clear 0b1: Start MDIO transaction
RMII_READD_PREAMBLE	5	Add 1B preamble to start of frame. Needed if other side of link is RMII	0x0: Do not add 1 byte preamble to start of frame 0x1: Add 1 byte preamble to start of frame
MDIO_REG_ADRS	4:0	Register address for targeted PHY	0bXXXXX: PHY address

SGMII_LINK_8 (0x1B8)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_WR_DATA_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_WR_DATA_L	7:0	Write data to use if performing a write operation	0xXX: LSB of MDIO write data

SGMII_LINK_9 (0x1B9)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_WR_DATA_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_WR_DATA_H	7:0	Write data to use if performing a write operation	0xXX: MSB of MDIO write data

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SGMII_LINK_10 (0x1BA)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_RD_DATA_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_RD_DATA_L	7:0	Resulting read data when performing a read operation.	0xXX: LSB of MDIO read data

SGMII_LINK_11 (0x1BB)

BIT	7	6	5	4	3	2	1	0
Field	MDIO_RD_DATA_H[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_RD_DATA_H	7:0	Resulting read data when performing a read operation.	0xXX: MSB of MDIO read data

SGMII_LINK_12 (0x1BC)*

BIT	7	6	5	4	3	2	1	0
Field	–	MDIO_ALT_DRIVER	RSVD[1:0]		TEST_RMT_LOOPBACK	RSVD	ADD_RXC_DLY	RSVD
Reset	–	0b1	0b00		0b0	0b0	0b0	0b0
Access Type	–	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MDIO_ALT_DRIVER	6	Enable alternative driver mode for MDIO pin	0x0: Open-drain driver 0x1: Push-pull with pullup
TEST_RMT_LOOPBACK	3	Loop GMSL2 Rx data back to GMSL2 Tx data. Rx data is not sent to SGMII Tx output.	0b0: Loopback disabled 0b1: Loopback enabled
ADD_RXC_DLY	1	Enable internal delay on RXC input per SGMII 2.0 Spec	0b0: RXC delay disabled 0b1: RXC delay enabled

SGMII_LINK_13 (0x1BD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	REQ_HOLD_OFF_SGMII[5:0]					
Reset	–	–	0b001110					
Access Type	–	–	Write, Read					

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BITFIELD	BITS	DESCRIPTION
REQ_HOLD_OFF_SGMII	5:0	Hold off GMSL2 Request until this number of extra bytes are received on SGMII port

WM_0 (0x1C0)

BIT	7	6	5	4	3	2	1	0
Field	WM_AUTO_SYNC_EN_X	WM_MODE_X[2:0]			–	–	–	WM_EN_X
Reset	0b1	0b000			–	–	–	0b0
Access Type	Write, Read	Write, Read			–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_AUTO_SYNC_EN_X	7	Auto-sync polarity detection (only effective for watermark block)	0b0: Disabled 0x1: Enabled
WM_MODE_X	6:4	Watermark Mode	0b000: Default generator mode − cycle through all four watermarks in video stream (default). 0b001: Error generator mode − cycle through only two watermarks to replicate a stuck frame. 0b01x: Reserved 0b1xx: Reserved
WM_EN_X	0	Watermark Enable	0b0: Watermarking disabled 0b1: Watermarking enabled

WM_2 (0x1C2)

BIT	7	6	5	4	3	2	1	0
Field	WM_AUTO_SYNC_EN_Y	WM_MODE_Y[2:0]			–	–	–	WM_EN_Y
Reset	0b1	0b000			–	–	–	0b0
Access Type	Write, Read	Write, Read			–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_AUTO_SYNC_EN_Y	7	Auto-sync polarity detection (only effective for watermark block)	0b0: Disabled 0x1: Enabled
WM_MODE_Y	6:4	Watermark Mode	0b000: Default generator mode − cycle through all four watermarks in video stream (default). 0b001: Error generator mode − cycle through only two watermarks to replicate a stuck frame. 0b01x: Reserved 0b1xx: Reserved
WM_EN_Y	0	Watermark Enable	0b0: Watermarking disabled 0b1: Watermarking enabled

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WM_WREN_0 (0x1DE)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_L	7:0	Writes 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.	0xBA: Enables writing to WM registers Others: WM registers remain read-only

WM_WREN_1 (0x1DF)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_H	7:0	Writes 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise, watermark registers are read-only.	0xDC: Enables writing to WM registers Others: WM registers remain read-only

GPIO_A (0x200, 0x208, 0x2A8, 0x2B0, 0x2B8, 0x2C0, 0x2C8)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
Access Type	Write, Read		Write, Read	Write, Read	Read Only	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drives value when GPIO_OUT_DIS = 0, GPIO_RX_EN_A = 0, and GPIO_RX_EN_B = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

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GPIO_B (0x201, 0x209, 0x2A9, 0x2B1, 0x2B9, 0x2C1, 0x2C9)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffers pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x202, 0x20A, 0x2AA, 0x2B2, 0x2BA, 0x2C2, 0x2CA)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when the pin is configured as non-GPIO. When cleared, the non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
IO_EDGE_RATE	6:5	Selects IO output edge rate	0x0: 1ns 0x1: 2ns 0x2: 4ns 0x3: 8ns
GPIO_RX_ID	4:0	First GPIO ID to receive and output at this pin Combined with other received GPIO IDs using GPIO_OUT_LGC.	0bXXXXX: GPIO ID to receive

GPIO_D (0x203, 0x20B, 0x2AB, 0x2B3, 0x2BB, 0x2C3, 0x2CB)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IO_RX_EN	5	Enables IO receiver	0x0: Disable 0x1: Enable
GPIO_OUT_LGC	4	When pin is used as GPIO, selects GPIO output drive logic function	0x0: AND the GPIO values received from both links 0x1: OR the GPIO values received from both links

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	3	Enable receiving first GPIO ID (GPIO_RX_ID) at this pin from link B	0b0: First GPIO ID disabled for reception 0b1: First GPIO ID enabled for reception
GPIO_TX_EN_B	2	Transmits GPIO to remote side on Link B	0b0: This GPIO source disabled for transmission 0b1: This GPIO source enabled for transmission
GPIO_RX_EN_A	1	Enable receiving first GPIO ID (GPIO_RX_ID) at this pin from Link A	0b0: First GPIO ID disabled for reception 0b1: First GPIO ID enabled for reception
GPIO_TX_EN_A	0	Transmits GPIO to remote side on Link A	0b0: This GPIO source disabled for transmission 0b1: This GPIO source enabled for transmission

GPIO_E (0x204, 0x20C, 0x2AC, 0x2B4, 0x2BC, 0x2C4, 0x2CC)*

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RX_EN2_B	GPIO_RX_EN2_A	GPIO_RX_ID2[4:0]				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN2_B	6	Enable receiving second GPIO ID (GPIO_RX_ID2) at this pin from Link B	0b0: Second GPIO ID disabled for reception 0b1: Second GPIO ID enabled for reception
GPIO_RX_EN2_A	5	Enable receiving second GPIO ID (GPIO_RX_ID2) at this pin from Link A	0b0: Second GPIO ID disabled for reception 0b1: Second GPIO ID enabled for reception
GPIO_RX_ID2	4:0	Second GPIO ID to receive and output at this pin Combined with other received GPIO IDs using GPIO_OUT_LGC.	0bXXXXX: GPIO ID to receive

GPIO_F (0x205, 0x20D, 0x2AD, 0x2B5, 0x2BD, 0x2C5, 0x2CD)*

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RX_EN3_B	GPIO_RX_EN3_A	GPIO_RX_ID3[4:0]				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN3_B	6	Enable receiving third GPIO ID (GPIO_RX_ID3) at this pin from Link B	0b0: Third GPIO ID disabled for reception 0b1: Third GPIO ID enabled for reception
GPIO_RX_EN3_A	5	Enable receiving third GPIO ID (GPIO_RX_ID3) at this pin from Link A	0b0: Third GPIO ID disabled for reception 0b1: Third GPIO ID enabled for reception
GPIO_RX_ID3	4:0	Third GPIO ID to receive and output at this pin Combined with other received GPIO IDs using GPIO_OUT_LGC.	0bXXXXX: GPIO ID to receive

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GPIO_G (0x206, 0x20E, 0x2AE, 0x2B6, 0x2BE, 0x2C6, 0x2CE)*

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RX_EN4_B	GPIO_RX_EN4_A	GPIO_RX_ID4[4:0]				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN4_B	6	Enable receiving fourth GPIO ID (GPIO_RX_ID4) at this pin from Link B	0b0: Fourth GPIO ID disabled for reception 0b1: Fourth GPIO ID enabled for reception
GPIO_RX_EN4_A	5	Enable receiving fourth GPIO ID (GPIO_RX_ID4) at this pin from Link A	0b0: Fourth GPIO ID disabled for reception 0b1: Fourth GPIO ID enabled for reception
GPIO_RX_ID4	4:0	Fourth GPIO ID to receive and output at this pin Combined with other received GPIO IDs using GPIO_OUT_LGC.	0bXXXXX: GPIO ID to receive

GPIO_A (0x210, 0x218, 0x220, 0x228, 0x230, 0x238, 0x240, 0x248, 0x250, 0x258, 0x260, 0x268, 0x270, 0x278, 0x280, 0x288, 0x290, 0x298, 0x2A0)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	–	–	GPIO_OUT_DIS
Access Type	Write, Read		Write, Read	Write, Read	Read Only	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drives value when GPIO_OUT_DIS = 0, GPIO_RX_EN_A = 0, and GPIO_RX_EN_B = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x211, 0x219, 0x221, 0x229, 0x231, 0x239, 0x241, 0x249, 0x251, 0x259, 0x261, 0x269, 0x271, 0x279, 0x281, 0x289, 0x291, 0x299, 0x2A1)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Access Type	Write, Read		Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffers pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x212, 0x21A, 0x222, 0x22A, 0x232, 0x23A, 0x242, 0x24A, 0x252, 0x25A, 0x262, 0x26A, 0x272, 0x27A, 0x282, 0x28A, 0x292, 0x29A, 0x2A2)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	IO_EDGE_RATE[1:0]		GPIO_RX_ID[4:0]				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting When set, RES_CFG and PULL_UPDN_SEL are effective when the pin is configured as non-GPIO. When cleared, the non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
IO_EDGE_RATE	6:5	Selects IO output edge rate	0x0: 1ns 0x1: 2ns 0x2: 4ns 0x3: 8ns
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_D (0x213, 0x21B, 0x223, 0x22B, 0x233, 0x23B, 0x243, 0x24B, 0x253, 0x25B, 0x263, 0x26B, 0x273, 0x27B, 0x283, 0x28B, 0x293, 0x29B, 0x2A3)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO_IO_RX_EN	GPIO_OUT_LGC	GPIO_RX_EN_B	GPIO_TX_EN_B	GPIO_RX_EN_A	GPIO_TX_EN_A
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IO_RX_EN	5	Enables IO receiver	0x0: Disable 0x1: Enable
GPIO_OUT_LGC	4	When pin is used as GPIO, selects GPIO output drive logic function.	0x0: AND the GPIO values received from both links 0x1: OR the GPIO values received from both links
GPIO_RX_EN_B	3	Receives GPIO from Link B	0b0: This GPIO source disabled for reception 0b1: This GPIO source enabled for reception
GPIO_TX_EN_B	2	Transmits GPIO to remote side on Link B	0b0: This GPIO source disabled for transmission 0b1: This GPIO source enabled for transmission
GPIO_RX_EN_A	1	Receives GPIO from Link A	0b0: This GPIO source disabled for reception 0b1: This GPIO source enabled for reception

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BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_EN_A	0	Transmits GPIO to remote side on Link A	0b0: This GPIO source disabled for transmission 0b1: This GPIO source enabled for transmission

GPIO_RX_0 (0x2F8)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_A_7	GPIO_RECVED_A_6	GPIO_RECVED_A_5	GPIO_RECVED_A_4	GPIO_RECVED_A_3	GPIO_RECVED_A_2	GPIO_RECVED_A_1	GPIO_RECVED_A_0
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_7	7	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_6	6	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_5	5	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_4	4	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_3	3	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_2	2	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_1	1	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_0	0	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

GPIO_RX_1 (0x2F9)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_A_15	GPIO_RECVED_A_14	GPIO_RECVED_A_13	GPIO_RECVED_A_12	GPIO_RECVED_A_11	GPIO_RECVED_A_10	GPIO_RECVED_A_9	GPIO_RECVED_A_8
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_15	7	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

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BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_14	6	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_13	5	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_12	4	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_11	3	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_10	2	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_9	1	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_8	0	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

GPIO_RX_2 (0x2FA)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_A_23	GPIO_RECVED_A_22	GPIO_RECVED_A_21	GPIO_RECVED_A_20	GPIO_RECVED_A_19	GPIO_RECVED_A_18	GPIO_RECVED_A_17	GPIO_RECVED_A_16
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_23	7	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_22	6	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_21	5	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_20	4	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_19	3	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_18	2	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

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BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_17	1	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_16	0	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

GPIO_RX_3 (0x2FB)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_A_31	GPIO_RECVED_A_30	GPIO_RECVED_A_29	GPIO_RECVED_A_28	GPIO_RECVED_A_27	GPIO_RECVED_A_26	GPIO_RECVED_A_25	GPIO_RECVED_A_24
Reset	0b1	0b1	0b0	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_A_31	7	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_30	6	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_29	5	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_28	4	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_27	3	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_26	2	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_25	1	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_A_24	0	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

GPIO_RX_4 (0x2FC)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_B_7	GPIO_RECVED_B_6	GPIO_RECVED_B_5	GPIO_RECVED_B_4	GPIO_RECVED_B_3	GPIO_RECVED_B_2	GPIO_RECVED_B_1	GPIO_RECVED_B_0
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_B_7	7	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_6	6	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_5	5	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_4	4	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_3	3	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_2	2	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_1	1	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_0	0	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

GPIO_RX_5 (0x2FD)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_B_15	GPIO_RECVED_B_14	GPIO_RECVED_B_13	GPIO_RECVED_B_12	GPIO_RECVED_B_11	GPIO_RECVED_B_10	GPIO_RECVED_B_9	GPIO_RECVED_B_8
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_B_15	7	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_14	6	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_13	5	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_12	4	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_11	3	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

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BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_B_10	2	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_9	1	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_8	0	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

GPIO_RX_6 (0x2FE)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_B_23	GPIO_RECVED_B_22	GPIO_RECVED_B_21	GPIO_RECVED_B_20	GPIO_RECVED_B_19	GPIO_RECVED_B_18	GPIO_RECVED_B_17	GPIO_RECVED_B_16
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_B_23	7	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_22	6	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_21	5	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_20	4	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_19	3	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_18	2	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_17	1	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_16	0	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

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GPIO_RX_7 (0x2FF)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RECVED_B_31	GPIO_RECVED_B_30	GPIO_RECVED_B_29	GPIO_RECVED_B_28	GPIO_RECVED_B_27	GPIO_RECVED_B_26	GPIO_RECVED_B_25	GPIO_RECVED_B_24
Reset	0b1	0b1	0b0	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
GPIO_RECVED_B_31	7	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_30	6	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_29	5	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_28	4	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_27	3	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_26	2	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_25	1	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel
GPIO_RECVED_B_24	0	Received GPIO value Write 0 or 1 to initialize the GPIO output before enabling the GPIO receive tunnel

UART_PT_0 (0x304)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0xDC							
Access Type								

UART_PT_1 (0x305)*

BIT	7	6	5	4	3	2	1	0
Field	DIS_TEMP_WAKE_PERM_A	–	RSVD[5:0]					
Reset	0b0	–	0b000101					
Access Type	Write, Read	–						

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BITFIELD	BITS	DESCRIPTION
DIS_TEMP_WAKE_PERM_A	7	Disables temporary wake-up force for link enable permanently

UART_PT_2 (0x306)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0xDC							
Access Type								

UART_PT_3 (0x307)*

BIT	7	6	5	4	3	2	1	0
Field	DIS_TEMP_WAKE_PERM_B	–	RSVD[5:0]					
Reset	0b0	–	0b000101					
Access Type	Write, Read	–						

BITFIELD	BITS	DESCRIPTION
DIS_TEMP_WAKE_PERM_B	7	Disables temporary wake-up force for link enable permanently

MISC_0 (0x310)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD[1:0]		OV_LEVEL[1:0]	
Reset	–	–	–	–	0b01		0b01	
Access Type	–	–	–	–			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
OV_LEVEL	1:0	V_{DD_SW} overvoltage comparator trip level	0x0: 1.10V 0x1: 1.12V 0x2: 1.15V 0x3: 1.18V

MISC_1 (0x311)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		OV1P8_LEVEL[1:0]		RSVD[1:0]		OVREG_LEVEL[1:0]	
Reset	0b01		0b01		0b01		0b01	
Access Type			Write, Read				Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
OV1P8_LEVEL	5:4	V_{DD18} overvoltage comparator trip level	0x0: 1.98V 0x1: 2.02V 0x2: 2.07V 0x3: 2.12V
OVREG_LEVEL	1:0	V_{REG} overvoltage comparator trip level	0x0: 1.32V 0x1: 1.35V 0x2: 1.38V 0x3: 1.41V

MISC_2 (0x312)

BIT	7	6	5	4	3	2	1	0
Field	VDDIO_OV	VDD1P8_OV	RSVD	VDD_OV	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Read Only	Read Only		Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDIO_OV	7	Live V_{DDIO} overvoltage status V_{TRIP_0V} level set by OVDDIO_LEVEL in register MISC_8.	0x0: Overvoltage not detected 0x1: Overvoltage detected
VDD1P8_OV	6	Live V_{DD18} overvoltage status V_{TRIP_ov} level set by OV1P8_LEVEL in register MISC_1.	0x0: Overvoltage not detected 0x1: Overvoltage detected
VDD_OV	4	Live V_{DD_sw} overvoltage status V_{TRIP_OV} set by OV_LEVEL in register MISC_0.	0x0: Overvoltage not detected 0x1: Overvoltage detected

MISC_3 (0x313)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LFLT_STKY_INT
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_STKY_INT	0	Selects if the line-fault interrupt should be sticky or live	0x0: Live 0x1: Sticky

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CC_CRC (0x320)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	CC_MSGCNTR_EN	CC_CRC_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC_MSGCNTR_EN	1	Enable I²C/UART message counter.	0x0: I²C/UART message counter disabled 0x1: I²C/UART message counter enabled
CC_CRC_EN	0	Enable I²C/UART CRC.	0x0: I²C/UART CRC disabled 0x1: I²C/UART CRC enabled

HDCP2_ID_0 (0x321)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	HDCP2_INT_ID_OVERRIDE_X[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP2_INT_ID_OVERRIDE_X	4:0	Override HDCP2 GPIO ID with this value for pipeline X	0x0: Internal HDCP2 interrupt GPIO ID is set according to the DES device address else: Use this value as HDCP2 interrupt GPIO ID

HDCP2_ID_1 (0x322)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	HDCP2_INT_ID_OVERRIDE_Y[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP2_INT_ID_OVERRIDE_Y	4:0	Override HDCP2 GPIO ID with this value for pipeline Y	0x0: Internal HDCP2 interrupt GPIO ID is set according to the DES device address else: Use this value as HDCP2 interrupt GPIO ID

MISC_8 (0x327)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		OVDDIO_LEVEL[1:0]		–	–	–	–
Reset	0b01		0b01		–	–	–	–
Access Type			Write, Read		–	–	–	–

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BITFIELD	BITS	DESCRIPTION	DECODE
OVDDIO_LEVEL	5:4	V_{DDIO} overvoltage comparator trip level	0x0: 3.64V 0x1: 3.75V 0x2: 3.85V 0x3: 3.96V

MISC_9 (0x328)*

RETENTION * This register needs to be in RETENTION *

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RSVD	VDDOV_LOGIC
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDOV_LOGIC	0	Selects whether VDD_OV and VDD1P8_OV function is gated by video detection	0x0: Over-voltage detection waits for active video 0x1: Over-voltage detection does not wait for active video

PIN_SEL (0x329)*

RETENTION * This register needs to be in RETENTION *

BIT	7	6	5	4	3	2	1	0
Field	MS_PIN_SEL	RCLKOUT_PIN_SEL	SPI_PIN_SEL	MDIO_PIN_SEL	AUDIO_RX_PIN_SEL_Y[1:0]		AUDIO_RX_PIN_SEL_X[1:0]	
Reset	0x0	0x0	0x0	0x0	0x1		0x0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MS_PIN_SEL	7	MS pin select	0x0: MFP25 0x1: MFP11
RCLKOUT_PIN_SEL	6	RCLKOUT pin select	0x0: MFP0 0x1: MFP10
SPI_PIN_SEL	5	SPI pin select	0x0: Use MFP0 for SCK, MFP1 for MOSI, MFP2 for MISO, MFP10 for BNE_SS1, and MFP25 for RO_SS2. 0x1: Use MFP25 for SCK, MFP14 for MOSI, MFP15 for MISO, MFP10 for BNE_SS1, and MFP0 for RO_SS2.
MDIO_PIN_SEL	4	MDIO-MDC pin select	0x0: Use MFP12 for MDIO and MFP13 for MDC 0x1: Use MFP19 for MDIO and MFP20 for MDC
AUDIO_RX_PIN_SEL_Y	3:2	Pin selection for Audio_RX_Y. Note: Set AUDIO_RX_PIN_SEL_X to a different value if AUDIO_RX_X is used.	0x0: Use MFP14,MFP15,MFP16. 0x1: Use MFP0, MFP1, MFP2. 0x2: Use MFP11,MFP12,MFP13. 0x3: RSVD
AUDIO_RX_PIN_SEL_X	1:0	Pin selection for Audio_RX_X. Note: Set AUDIO_RX_PIN_SEL_Y to a different value if AUDIO_RX_Y is used.	0x0: Use MFP14,MFP15,MFP16. 0x1: Use MFP0, MFP1, MFP2. 0x2: Use MFP11,MFP12,MFP13. 0x3: RSVD

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MISC_OTP2 (0x331)

BIT	7	6	5	4	3	2	1	0
Field	OTP_RELEASED	RSVD[6:0]						
Reset	0x0	0x00						
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OTP_RELEASED	7	Indicates whether OTP Program is a released version or a prototype version	0x0: Prototype 0x1: Released

CMU6 (0x3E6)

BIT	7	6	5	4	3	2	1	0
Field	SET_TEMP1P0[1:0]		RSVD	RSVD[4:0]				
Reset	0b00		0b0	0b00000				
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SET_TEMP1P0	7:6	TMON temperature trip point control.	0: Ttrip = 125C 1: Ttrip = 130C 2: Ttrip = 135C 3: Ttrip = 140C

CROSS_0 (0x400, 0x500)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0b0	0b0	0b00000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS0_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0.	0bXXXXX: Incoming bit position

CROSS_1 (0x401, 0x501)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0b0	0b0	0b00001				
Access Type	–	Write, Read	Write, Read	Write, Read				

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS1_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1.	0bXXXXX: Incoming bit position

CROSS_2 (0x402, 0x502)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0b0	0b0	0b00010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS2_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS2_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2.	0bXXXXX: Incoming bit position

CROSS_3 (0x403, 0x503)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0b0	0b0	0b00011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS3_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3.	0bXXXXX: Incoming bit position

CROSS_4 (0x404, 0x504)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0b0	0b0	0b00100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4.	0bXXXXX: Incoming bit position

CROSS_5 (0x405, 0x505)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0b0	0b0	0b00101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS5_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS5_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5.	0bXXXXX: Incoming bit position

CROSS_6 (0x406, 0x506)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0b0	0b0	0b00110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS6_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS6_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6.	0bXXXXX: Incoming bit position

CROSS_7 (0x407, 0x507)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0b0	0b0	0b00111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS7_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7.	0bXXXXX: Incoming bit position

CROSS_8 (0x408, 0x508)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0b0	0b0	0b01000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS8_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS8_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8.	0bXXXXX: Incoming bit position

CROSS_9 (0x409, 0x509)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0b0	0b0	0b01001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS9_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS9_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9.	0bXXXXX: Incoming bit position

CROSS_10 (0x40A, 0x50A)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0b0	0b0	0b01010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS10_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10.	0bXXXXX: Incoming bit position

CROSS_11 (0x40B, 0x50B)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0b0	0b0	0b01011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS11_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS11_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11.	0bXXXXX: Incoming bit position

CROSS_12 (0x40C, 0x50C)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0b0	0b0	0b01100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS12_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS12_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12.	0bXXXXX: Incoming bit position

CROSS_13 (0x40D, 0x50D)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0b0	0b0	0b01101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS13_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13.	0bXXXXX: Incoming bit position

CROSS_14 (0x40E, 0x50E)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0b0	0b0	0b01110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14.	0bXXXXX: Incoming bit position

CROSS_15 (0x40F, 0x50F)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0b0	0b0	0b01111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15.	0bXXXXX: Incoming bit position

CROSS_16 (0x410, 0x510)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0b0	0b0	0b10000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS16_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16.	0bXXXXX: Incoming bit position

CROSS_17 (0x411, 0x511)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0b0	0b0	0b10001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17.	0bXXXXX: Incoming bit position

CROSS_18 (0x412, 0x512)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0b0	0b0	0b10010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS18_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18.	0bXXXXX: Incoming bit position

CROSS_19 (0x413, 0x513)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0b0	0b0	0b10011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19.	0bXXXXX: Incoming bit position

CROSS_20 (0x414, 0x514)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0b0	0b0	0b10100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20.	0bXXXXX: Incoming bit position

CROSS_21 (0x415, 0x515)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0b0	0b0	0b10101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21.	0bXXXXX: Incoming bit position

CROSS_22 (0x416, 0x516)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0b0	0b0	0b10110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS22_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

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BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22.	0bXXXXX: Incoming bit position

CROSS_23 (0x417, 0x517)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0b0	0b0	0b10111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS23_I	6	Invert CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS23_F	5	Force CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23.	0bXXXXX: Incoming bit position

HS_VS (0x41F, 0x51F)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET	VS_DET	HS_DET	–	–	VS_POL	HS_POL
Reset	–	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET	6	DE activity is detected	0x0: DE is not detected 0x1: DE is detected
VS_DET	5	VS activity is detected	0x0: VS is not detected 0x1: VS is detected
HS_DET	4	HS activity is detected	0x0: HS is not detected 0x1: HS is detected
VS_POL	1	Detected VS polarity	0x0: VS is high when DE = 1 0x1: VS is low when DE = 1
HS_POL	0	Detected HS polarity	0x0: Active low 0x1: Active high

VTX0 (0x420, 0x520)

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VID_ACTIVE	PCLKDET_VTX	VS_TRIG	VTG_MODE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b1	0b11	
Access Type	Write, Read	Write, Read	Write, Read	Read Only	Read Only	Write, Read	Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
GEN_VS	7	Enable to generate VS output according to the timing definition	0b0: Do not generate VS 0b1: Generate VS
GEN_HS	6	Enable to generate HS output according to the timing definition	0b0: Do not generate HS 0b1: Generate HS
GEN_DE	5	Enable to generate DE output according to the timing definition	0b0: Do not generate DE 0b1: Generate DE
VID_ACTIVE	4	Video active indicator	0b0: Video input is in reset 0b1: Video input is active
PCLKDET_VTX	3	PCLK detected	0b0: PCLK not detected 0b1: PCLK detected
VS_TRIG	2	Selects VS trigger edge	0b0: Falling edge 0b1: Rising edge
VTG_MODE	1:0	Video timing generator mode	0b00: VS tracking mode 0b01: VS on trigger mode 0b10: Auto repeat mode 0b11: Free running mode

VTX1 (0x421, 0x521)*

BIT	7	6	5	4	3	2	1	0
Field	USE_DE_AS_HS	USE_HS_AS_DE	FORCE_VS_LOW	FORCE_HS_LOW	FORCE_DE_LOW	VS_INVERT	HS_INVERT	DE_INVERT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
USE_DE_AS_HS	7	Replace HS with DE	0x0: HS is unchanged 0x1: Use DE as HS
USE_HS_AS_DE	6	Replace DE with HS	0x0: DE is unchanged 0x1: Use HS as DE
FORCE_VS_LOW	5	Force VS Low (before optional inversion)	0x0: VS is not forced 0x1: VS is forced low
FORCE_HS_LOW	4	Force HS Low (before optional inversion)	0x0: HS is not forced 0x1: HS is forced low
FORCE_DE_LOW	3	Force DE Low (before optional inversion)	0x0: DE is not forced 0x1: DE is forced low
VS_INVERT	2	Invert VS after video timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INVERT	1	Invert HS after video timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INVERT	0	Invert DE after video timing generator	0b0: Do not invert DE 0b1: Invert DE

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VTX2 (0x422, 0x522)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_DLY_2	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DELAY cycles from the input VS. (bits [23:16])	0xXX: Most significant byte of VS delay

VTX3 (0x423, 0x523)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_DLY_1	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DELAY cycles from the input VS. (bits [15:8])	0xXX: Middle significant byte of VS delay

VTX4 (0x424, 0x524)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_DLY_0	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DELAY cycles from the input VS. (bits [7:0])	0xXX: Least significant byte of VS delay

VTX5 (0x425, 0x525)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_HIGH_2	7:0	VS high period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS high period

VTX6 (0x426, 0x526)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_HIGH_1	7:0	VS high period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS high period

VTX7 (0x427, 0x527)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_HIGH_0	7:0	VS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS high period

VTX8 (0x428, 0x528)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_LOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_LOW_2	7:0	VS low period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS low period

VTX9 (0x429, 0x529)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_LOW_1	7:0	VS low period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS low period

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VTX10 (0x42A, 0x52A)

BIT	7	6	5	4	3	2	1	0
Field	V_VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_VS_LOW_0	7:0	VS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS low period

VTX11 (0x42B, 0x52B)

BIT	7	6	5	4	3	2	1	0
Field	V2H_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_2	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first HS rising edge

VTX12 (0x42C, 0x52C)

BIT	7	6	5	4	3	2	1	0
Field	V2H_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_1	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first HS rising edge

VTX13 (0x42D, 0x52D)

BIT	7	6	5	4	3	2	1	0
Field	V2H_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_0	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS edge to first HS rising edge

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VTX14 (0x42E, 0x52E)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_HIGH_1	7:0	HS high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS high period

VTX15 (0x42F, 0x52F)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_HIGH_0	7:0	HS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS high period

VTX16 (0x430, 0x530)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_LOW_1	7:0	HS low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS low period

VTX17 (0x431, 0x531)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_LOW_0	7:0	HS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS low period

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VTX18 (0x432, 0x532)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_CNT_1	7:0	HS pulses per frame (bits [15:8])	0xXX: Most significant byte of HS pulses per frame

VTX19 (0x433, 0x533)

BIT	7	6	5	4	3	2	1	0
Field	V_HS_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_HS_CNT_0	7:0	HS pulses per frame (bits [7:0])	0xXX: Least significant byte of HS pulses per frame

VTX20 (0x434, 0x534)

BIT	7	6	5	4	3	2	1	0
Field	V2D_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_2	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first DE

VTX21 (0x435, 0x535)

BIT	7	6	5	4	3	2	1	0
Field	V2D_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_1	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first DE

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VTX22 (0x436, 0x536)

BIT	7	6	5	4	3	2	1	0
Field	V2D_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_0	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS edge to first DE

VTX23 (0x437, 0x537)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_HIGH_1	7:0	DE high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE high period

VTX24 (0x438, 0x538)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_HIGH_0	7:0	DE high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE high period

VTX25 (0x439, 0x539)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_LOW_1	7:0	DE low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE low period

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VTX26 (0x43A, 0x53A)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_LOW_0	7:0	DE low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE low period

VTX27 (0x43B, 0x53B)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_CNT_1	7:0	Active lines per frame (bits [15:8])	0xXX: Most significant byte of DE pulses per frame

VTX28 (0x43C, 0x53C)

BIT	7	6	5	4	3	2	1	0
Field	V_DE_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V_DE_CNT_0	7:0	Active lines per frame (bits [7:0])	0xXX: Least significant byte of DE pulses per frame

VTX29 (0x43D, 0x53D)

BIT	7	6	5	4	3	2	1	0
Field	VID_PRBS_EN	–	–	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
Reset	0b0	–	–	–	–	0b0	0b00	
Access Type	Write, Read	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PRBS_EN	7	Enables video PRBS generator	0b0: Video PRBS generator disabled 0b1: Video PRBS generator enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_MODE	2	Gradient pattern generator mode	0b0: Gradient mode increasing. Each gradient color starts from a value of 0x00 and increases to 0xFF 0b1: Gradient mode decreasing. Each gradient color starts from a value of 0xFF and decreases to 0x00
PATGEN_MODE	1:0	Pattern generator mode	0b00: Pattern generator disabled - use video from the serializer input 0b01: Generate checkerboard pattern 0b10: Generate gradient pattern 0b11: Reserved

VTX30 (0x43E, 0x53E)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_INC[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_INC	7:0	Gradient mode increment amount Increment amount is the register value divided by 4.	0xXX: Gradient increment base

VTX31 (0x43F, 0x53F)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_L	7:0	Checkerboard mode Color A lower byte	0xXX: Least significant byte of checkerboard mode Color A

VTX32 (0x440, 0x540)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_M	7:0	Checkerboard mode Color A middle byte	0xXX: Middle significant byte of checkerboard mode Color A

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VTX33 (0x441, 0x541)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_H	7:0	Checkerboard mode Color A high byte	0xXX: Most significant byte of checkerboard mode Color A

VTX34 (0x442, 0x542)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_L	7:0	Checkerboard mode Color B low byte	0xXX: Least significant byte of checkerboard mode Color B

VTX35 (0x443, 0x543)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_M	7:0	Checkerboard mode Color B middle byte	0xXX: Middle significant byte of checkerboard mode Color B

VTX36 (0x444, 0x544)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_H	7:0	Checkerboard mode Color B high byte	0xXX: Most significant byte of checkerboard mode Color B

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VTX37 (0x445, 0x545)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_A[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_A	7:0	Checkerboard mode Color A repeat count	0xXX: Repeat count of checkerboard mode Color A

VTX38 (0x446, 0x546)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_B	7:0	Checkerboard mode Color B repeat count	0xXX: Repeat count of checkerboard mode Color B

VTX39 (0x447, 0x547)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_ALT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_ALT	7:0	Checkerboard mode alternate line count	0xXX: Checkerboard mode alternate line count

VTX40 (0x448, 0x548)*

BIT	7	6	5	4	3	2	1	0
Field	DIS_COLOR_CROSSBAR	–	–	–	VA_BEFORE_WM	AUTO_COLOR_DEPTH	COLOR_DEPTH[1:0]	
Reset	0b0	–	–	–	0b0	0b1	0b01	
Access Type	Write, Read	–	–	–	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_COLOR_CROSSBAR	7	Disable color crossbar	0b0: Enable color crossbar 0b1: Disable color crossbar
VA_BEFORE_WM	3	For tell-tale safety applications, generate CRC before the watermark block	0x0: After watermark 0x1: Before watermark

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BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_COLOR_DEPTH	2	Auto bits per color When set to 1, BPP register in Video Tx register block determines bits per color.	0x0: Disabled 0x1: Enabled
COLOR_DEPTH	1:0	Bits per color (used when AUTO_COLOR_DEPTH—VTX40 register = 0)	0x0: 6-bits color 0x1: 8-bits color 0x2: 10-bits color 0x3: Reserved

VTX41 (0x449, 0x549)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VID_ASIL_INJ_ERR	VID_ASIL_CRC_ERR_OEN	VID_ASIL_CRC_ERR	VID_ASIL_CRC_CHK_EARLY	VID_ASIL_CRC_CHK_EN
Reset	–	–	–	0b0	0b1	0b0	0b0	0b1
Access Type	–	–	–	Write, Read	Write, Read	Read Clears All	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VID_ASIL_INJ_ERR	4	Inject error to verify video pipeline CRC functionality	0x0: Do not inject error 0x1: Inject error
VID_ASIL_CRC_ERR_OEN	3	Enable reporting video pipeline CRC error flag (VID_ASIL_CRC_ERR) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VID_ASIL_CRC_ERR	2	Latched video pipeline CRC error status for functional safety	0x0: Error not detected 0x1: Error detected
VID_ASIL_CRC_CHK_EARLY	1	Check video pipeline CRC before WM, FRC and Crossbar blocks This bit shall be set if any one of these blocks is enabled.	0x0: Video pipeline CRC is performed at the output of VTX 0x1: Video pipeline CRC is performed at the input of VTX
VID_ASIL_CRC_CHK_EN	0	Enable video pipeline CRC for functional safety 32-bit CRC is generated for each video frame when writing data to the video line FIFO memory and checked after data is read at the input or at the output of the VTX block.	0x0: Disabled 0x1: Enabled

PXL_CAPT_0 (0x458, 0x558)

BIT	7	6	5	4	3	2	1	0
Field	PIXEL_CAPT_H_HIGH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PIXEL_CAPT_H_HIGH	7:0	Horizontal(X) coordinate of the pixel to be captured

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PXL_CAPT_1 (0x459, 0x559)

BIT	7	6	5	4	3	2	1	0
Field	PIXEL_CAPT_H_LOW[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PIXEL_CAPT_H_LOW	7:0	Horizontal(X) coordinate of the pixel to be captured

PXL_CAPT_2 (0x45A, 0x55A)

BIT	7	6	5	4	3	2	1	0
Field	PIXEL_CAPT_V_HIGH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PIXEL_CAPT_V_HIGH	7:0	Vertical(Y) coordinate of the pixel to be captured

PXL_CAPT_3 (0x45B, 0x55B)

BIT	7	6	5	4	3	2	1	0
Field	PIXEL_CAPT_V_LOW[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PIXEL_CAPT_V_LOW	7:0	Vertical(Y) coordinate of the pixel to be captured

PXL_CAPT_4 (0x45C, 0x55C)

BIT	7	6	5	4	3	2	1	0
Field	PIXEL_CAPT_7_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PIXEL_CAPT_7_0	7:0	Captured pixel value

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PXL_CAPT_5 (0x45D, 0x55D)

BIT	7	6	5	4	3	2	1	0
Field	PIXEL_CAPT_15_8[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PIXEL_CAPT_15_8	7:0	Captured pixel value

PXL_CAPT_6 (0x45E, 0x55E)

BIT	7	6	5	4	3	2	1	0
Field	PIXEL_CAPT_23_16[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PIXEL_CAPT_23_16	7:0	Captured pixel value

AUTH0 (0x460, 0x560)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CYCLE_MODULO_H[1:0]		LOCAL_CHALLENGE_MAX[1:0]		RSVD	AUTH_GLOBAL_PERIODIC	AUTH_GLOBAL_TRIG	AUTH_EN
Reset	0b00		0b00		0b0	0b1	0b0	0b1
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CYCLE_MODULO_H	7:6	Modulo value for the frame-cycle counter	0bxx: MSB bits for frame cycle modulo value
LOCAL_CHALLENGE_MAX	5:4	Selects desired number of local challenges	0x0: One local challenge 0x1: Two local challenges 0x2: Three local challenges 0x3: Four local challenges
AUTH_GLOBAL_PERIODIC	2	Enable video authentication feature periodic global challenge mode	0x0: Disabled 0x1: Enabled
AUTH_GLOBAL_TRIG	1	Enable video authentication feature global challenge trigger. User needs to create a rising edge.	0x0: Disabled 0x1: Enabled
AUTH_EN	0	Enable video authentication feature	0x0: Disabled 0x1: Enabled

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AUTH1 (0x461, 0x561)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CYCLE_MODULO_L[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CYCLE_MODULO_L	7:0	Modulo value for the frame-cycle counter	0bxxxxxxxx: LSB bits for frame cycle modulo value

XMINL0a (0x462, 0x562)

BIT	7	6	5	4	3	2	1	0
Field	XMIN0a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN0a_LSB	7:0	Local Challenge X coordinate maximum value. Minimum allowed value is 2.

XMINH0a (0x463, 0x563)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN0a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN0a_MSB	5:0	Local Challenge X coordinate maximum value. Minimum allowed value is 2.

XMAXL0a (0x464, 0x564)

BIT	7	6	5	4	3	2	1	0
Field	XMAX0a_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX0a_LSB	7:0	Local Challenge X coordinate maximum value

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XMAXH0a (0x465, 0x565)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX0a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX0a_MSB	5:0	Local Challenge X coordinate maximum value

XMINL1a (0x466, 0x566)

BIT	7	6	5	4	3	2	1	0
Field	XMIN1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN1a_LSB	7:0	Local Challenge X coordinate maximum value.

XMINH1a (0x467, 0x567)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN1a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN1a_MSB	5:0	Local Challenge X coordinate maximum value

XMAXL1a (0x468, 0x568)

BIT	7	6	5	4	3	2	1	0
Field	XMAX1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX1a_LSB	7:0	Local Challenge X coordinate maximum value

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XMAXH1a (0x469, 0x569)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX1a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX1a_MSB	5:0	Local Challenge X coordinate maximum value

XMINL2a (0x46A, 0x56A)

BIT	7	6	5	4	3	2	1	0
Field	XMIN2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN2a_LSB	7:0	Local Challenge X coordinate maximum value.

XMINH2a (0x46B, 0x56B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN2a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN2a_MSB	5:0	Local Challenge X coordinate maximum value

XMAXL2a (0x46C, 0x56C)

BIT	7	6	5	4	3	2	1	0
Field	XMAX2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX2a_LSB	7:0	Local Challenge X coordinate maximum value

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XMAXH2a (0x46D, 0x56D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX2a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX2a_MSB	5:0	Local Challenge X coordinate maximum value

XMINL3a (0x46E, 0x56E)

BIT	7	6	5	4	3	2	1	0
Field	XMIN3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN3a_LSB	7:0	Local Challenge X coordinate maximum value.

XMINH3a (0x46F, 0x56F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN3a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN3a_MSB	5:0	Local Challenge X coordinate maximum value

XMAXL3a (0x470, 0x570)

BIT	7	6	5	4	3	2	1	0
Field	XMAX3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX3a_LSB	7:0	Local Challenge X coordinate maximum value

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XMAXH3a (0x471, 0x571)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX3a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX3a_MSB	5:0	Local Challenge X coordinate maximum value

XMINL0b (0x472, 0x572)

BIT	7	6	5	4	3	2	1	0
Field	XMIN0b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN0b_LSB	7:0	Local Challenge X coordinate maximum value. Minimum allowed value is 2.

XMINH0b (0x473, 0x573)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN0b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN0b_MSB	5:0	Local Challenge X coordinate maximum value. Minimum allowed value is 2.

XMAXL0b (0x474, 0x574)

BIT	7	6	5	4	3	2	1	0
Field	XMAX0b_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX0b_LSB	7:0	Local Challenge X coordinate maximum value

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XMAXH0b (0x475, 0x575)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX0b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX0b_MSB	5:0	Local Challenge X coordinate maximum value

XMINL1b (0x476, 0x576)

BIT	7	6	5	4	3	2	1	0
Field	XMIN1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN1b_LSB	7:0	Local Challenge X coordinate maximum value.

XMINH1b (0x477, 0x577)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN1b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN1b_MSB	5:0	Local Challenge X coordinate maximum value

XMAXL1b (0x478, 0x578)

BIT	7	6	5	4	3	2	1	0
Field	XMAX1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX1b_LSB	7:0	Local Challenge X coordinate maximum value

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XMAXH1b (0x479, 0x579)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX1b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX1b_MSB	5:0	Local Challenge X coordinate maximum value

XMINL2b (0x47A, 0x57A)

BIT	7	6	5	4	3	2	1	0
Field	XMIN2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN2b_LSB	7:0	Local Challenge X coordinate maximum value.

XMINH2b (0x47B, 0x57B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN2b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN2b_MSB	5:0	Local Challenge X coordinate maximum value

XMAXL2b (0x47C, 0x57C)

BIT	7	6	5	4	3	2	1	0
Field	XMAX2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX2b_LSB	7:0	Local Challenge X coordinate maximum value

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XMAXH2b (0x47D, 0x57D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX2b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX2b_MSB	5:0	Local Challenge X coordinate maximum value

XMINL3b (0x47E, 0x57E)

BIT	7	6	5	4	3	2	1	0
Field	XMIN3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMIN3b_LSB	7:0	Local Challenge X coordinate maximum value.

XMINH3b (0x47F, 0x57F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMIN3b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMIN3b_MSB	5:0	Local Challenge X coordinate maximum value

XMAXL3b (0x480, 0x580)

BIT	7	6	5	4	3	2	1	0
Field	XMAX3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
XMAX3b_LSB	7:0	Local Challenge X coordinate maximum value

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XMAXH3b (0x481, 0x581)

BIT	7	6	5	4	3	2	1	0
Field	–	–	XMAX3b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
XMAX3b_MSB	5:0	Local Challenge X coordinate maximum value

YMINL0a (0x482, 0x582)

BIT	7	6	5	4	3	2	1	0
Field	YMIN0a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN0a_LSB	7:0	Local Challenge Y coordinate maximum value

YMINH0a (0x483, 0x583)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN0a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN0a_MSB	5:0	Local Challenge Y coordinate maximum value

YMAXL0a (0x484, 0x584)

BIT	7	6	5	4	3	2	1	0
Field	YMAX0a_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX0a_LSB	7:0	Local Challenge Y coordinate maximum value

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YMAXH0a (0x485, 0x585)

BIT	7	6	5	4	3	2	1	0
Field	FRAME0a_MSB[1:0]		YMAX0a_MSB[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
FRAME0a_MSB	7:6	Local challenge frame number. Decimal 511 value is reserved.
YMAX0a_MSB	5:0	Local Challenge Y coordinate maximum value

FRAME0a (0x486, 0x586)

BIT	7	6	5	4	3	2	1	0
Field	FRAME0a_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME0a_LSB	7:0	Local challenge frame number. Decimal 511 value is reserved.

YMINL1a (0x487, 0x587)

BIT	7	6	5	4	3	2	1	0
Field	YMIN1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN1a_LSB	7:0	Local Challenge Y coordinate maximum value

YMINH1a (0x488, 0x588)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN1a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN1a_MSB	5:0	Local Challenge Y coordinate maximum value

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YMAXL1a (0x489, 0x589)

BIT	7	6	5	4	3	2	1	0
Field	YMAX1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX1a_LSB	7:0	Local Challenge Y coordinate maximum value

YMAXH1a (0x48A, 0x58A)

BIT	7	6	5	4	3	2	1	0
Field	FRAME1a_MSB[1:0]		YMAX1a_MSB[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
FRAME1a_MSB	7:6	Local challenge frame number. Decimal 511 value is reserved.
YMAX1a_MSB	5:0	Local Challenge Y coordinate maximum value

FRAME1a (0x48B, 0x58B)

BIT	7	6	5	4	3	2	1	0
Field	FRAME1a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME1a_LSB	7:0	Local challenge frame number. Decimal 511 value is reserved.

YMINL2a (0x48C, 0x58C)

BIT	7	6	5	4	3	2	1	0
Field	YMIN2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN2a_LSB	7:0	Local Challenge Y coordinate maximum value

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YMINH2a (0x48D, 0x58D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN2a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN2a_MSB	5:0	Local Challenge Y coordinate maximum value

YMAXL2a (0x48E, 0x58E)

BIT	7	6	5	4	3	2	1	0
Field	YMAX2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX2a_LSB	7:0	Local Challenge Y coordinate maximum value

YMAXH2a (0x48F, 0x58F)

BIT	7	6	5	4	3	2	1	0
Field	FRAME2a_MSB[1:0]		YMAX2a_MSB[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
FRAME2a_MSB	7:6	Local challenge frame number. Decimal 511 value is reserved.
YMAX2a_MSB	5:0	Local Challenge Y coordinate maximum value

FRAME2a (0x490, 0x590)

BIT	7	6	5	4	3	2	1	0
Field	FRAME2a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME2a_LSB	7:0	Local challenge frame number. Decimal 511 value is reserved.

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YMINL3a (0x491, 0x591)

BIT	7	6	5	4	3	2	1	0
Field	YMIN3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN3a_LSB	7:0	Local Challenge Y coordinate maximum value

YMINH3a (0x492, 0x592)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN3a_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN3a_MSB	5:0	Local Challenge Y coordinate maximum value

YMAXL3a (0x493, 0x593)

BIT	7	6	5	4	3	2	1	0
Field	YMAX3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX3a_LSB	7:0	Local Challenge Y coordinate maximum value

YMAXH3a (0x494, 0x594)

BIT	7	6	5	4	3	2	1	0
Field	FRAME3a_MSB[1:0]		YMAX3a_MSB[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
FRAME3a_MSB	7:6	Local challenge frame number. Decimal 511 value is reserved.
YMAX3a_MSB	5:0	Local Challenge Y coordinate maximum value

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FRAME3a (0x495, 0x595)

BIT	7	6	5	4	3	2	1	0
Field	FRAME3a_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME3a_LSB	7:0	Local challenge frame number. Decimal 511 value is reserved.

YMINL0b (0x496, 0x596)

BIT	7	6	5	4	3	2	1	0
Field	YMIN0b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN0b_LSB	7:0	Local Challenge Y coordinate maximum value

YMINH0b (0x497, 0x597)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN0b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN0b_MSB	5:0	Local Challenge Y coordinate maximum value

YMAXL0b (0x498, 0x598)

BIT	7	6	5	4	3	2	1	0
Field	YMAX0b_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX0b_LSB	7:0	Local Challenge Y coordinate maximum value

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YMAXH0b (0x499, 0x599)

BIT	7	6	5	4	3	2	1	0
Field	FRAME0b_MSB[1:0]		YMAX0b_MSB[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
FRAME0b_MSB	7:6	Local challenge frame number. Decimal 511 value is reserved.
YMAX0b_MSB	5:0	Local Challenge Y coordinate maximum value

FRAME0b (0x49A, 0x59A)

BIT	7	6	5	4	3	2	1	0
Field	FRAME0b_LSB[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME0b_LSB	7:0	Local challenge frame number. Decimal 511 value is reserved.

YMINL1b (0x49B, 0x59B)

BIT	7	6	5	4	3	2	1	0
Field	YMIN1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN1b_LSB	7:0	Local Challenge Y coordinate maximum value

YMINH1b (0x49C, 0x59C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN1b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN1b_MSB	5:0	Local Challenge Y coordinate maximum value

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YMAXL1b (0x49D, 0x59D)

BIT	7	6	5	4	3	2	1	0
Field	YMAX1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX1b_LSB	7:0	Local Challenge Y coordinate maximum value

YMAXH1b (0x49E, 0x59E)

BIT	7	6	5	4	3	2	1	0
Field	FRAME1b_MSB[1:0]		YMAX1b_MSB[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
FRAME1b_MSB	7:6	Local challenge frame number. Decimal 511 value is reserved.
YMAX1b_MSB	5:0	Local Challenge Y coordinate maximum value

FRAME1b (0x49F, 0x59F)

BIT	7	6	5	4	3	2	1	0
Field	FRAME1b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME1b_LSB	7:0	Local challenge frame number. Decimal 511 value is reserved.

YMINL2b (0x4A0, 0x5A0)

BIT	7	6	5	4	3	2	1	0
Field	YMIN2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN2b_LSB	7:0	Local Challenge Y coordinate maximum value

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YMINH2b (0x4A1, 0x5A1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN2b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN2b_MSB	5:0	Local Challenge Y coordinate maximum value

YMAXL2b (0x4A2, 0x5A2)

BIT	7	6	5	4	3	2	1	0
Field	YMAX2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX2b_LSB	7:0	Local Challenge Y coordinate maximum value

YMAXH2b (0x4A3, 0x5A3)

BIT	7	6	5	4	3	2	1	0
Field	FRAME2b_MSB[1:0]		YMAX2b_MSB[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
FRAME2b_MSB	7:6	Local challenge frame number. Decimal 511 value is reserved.
YMAX2b_MSB	5:0	Local Challenge Y coordinate maximum value

FRAME2b (0x4A4, 0x5A4)

BIT	7	6	5	4	3	2	1	0
Field	FRAME2b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME2b_LSB	7:0	Local challenge frame number. Decimal 511 value is reserved.

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YMINL3b (0x4A5, 0x5A5)

BIT	7	6	5	4	3	2	1	0
Field	YMIN3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMIN3b_LSB	7:0	Local Challenge Y coordinate maximum value

YMINH3b (0x4A6, 0x5A6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	YMIN3b_MSB[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
YMIN3b_MSB	5:0	Local Challenge Y coordinate maximum value

YMAXL3b (0x4A7, 0x5A7)

BIT	7	6	5	4	3	2	1	0
Field	YMAX3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YMAX3b_LSB	7:0	Local Challenge Y coordinate maximum value

YMAXH3b (0x4A8, 0x5A8)

BIT	7	6	5	4	3	2	1	0
Field	FRAME3b_MSB[1:0]		YMAX3b_MSB[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
FRAME3b_MSB	7:6	Local challenge frame number. Decimal 511 value is reserved.
YMAX3b_MSB	5:0	Local Challenge Y coordinate maximum value

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FRAME3b (0x4A9, 0x5A9)

BIT	7	6	5	4	3	2	1	0
Field	FRAME3b_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FRAME3b_LSB	7:0	Local challenge frame number. Decimal 511 value is reserved.

out1 (0x4AA, 0x5AA)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CNT_MSB	VA_SWAP_DIS	VA_DONE_FLAG	VA_DONE_OEN	–	A_OR_B	AUTH_DONE_B	AUTH_DONE_A
Reset	0b0	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	Read Only	Write, Read	Read Only	Write, Read	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CNT_MSB	7	Frame counter value of MSB	0xX: MSB bit of the counter value
VA_SWAP_DIS	6	disable auto A/B align between SERDES	
VA_DONE_FLAG	5	Video authentication done status flag.	0x0: Running 0x1: Challenge complete
VA_DONE_OEN	4	Enables video authentication done to be reflected to the ERRB pin.	0x0: disabled 0x1: enabled
A_OR_B	2	Shows which register bank is active.	0x0: A set 0x1: B set
AUTH_DONE_B	1	B Challenge is done	0x0: Challenge is running 0x1: Challenge is complete
AUTH_DONE_A	0	Challenge A is done	0x0: Challenge is running 0x1: Challenge is complete

out1a (0x4AB, 0x5AB)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CNT_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FRAME_CNT_LSB	7:0	Frame counter value LSB	0xX: LSB bit of the counter value

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out2 (0x4AC, 0x5AC)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_A_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_A_0	7:0	CRC result for Challenge A. Valid only at the rising edge of the completed signal.

out3 (0x4AD, 0x5AD)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_A_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_A_1	7:0	CRC result for challenge A. Valid only at the rising edge of the completed signal.

out4 (0x4AE, 0x5AE)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_A_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_A_2	7:0	CRC result for Challenge A. Valid only at the rising edge of the completed signal.

out5 (0x4AF, 0x5AF)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_A_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_A_3	7:0	CRC result for Challenge A. Valid only at the rising edge of the completed signal.

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out6 (0x4B0, 0x5B0)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_B_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_B_0	7:0	CRC result for Challenge B. Valid only at the rising edge of the completed signal.

out7 (0x4B1, 0x5B1)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_B_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_B_1	7:0	CRC result for Challenge B. Valid only at the rising edge of the completed signal.

out8 (0x4B2, 0x5B2)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_B_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_B_2	7:0	CRC result for Challenge B. Valid only at the rising edge of the completed signal.

out9 (0x4B3, 0x5B3)

BIT	7	6	5	4	3	2	1	0
Field	CRC_OUT_B_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CRC_OUT_B_3	7:0	CRC result for Challenge B. Valid only at the rising edge of the completed signal.

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outa (0x4B4, 0x5B4)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_0	7:0	Frames CRC result

outb (0x4B5, 0x5B5)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_1	7:0	Frames CRC result

outc (0x4B6, 0x5B6)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_2	7:0	Frames CRC result

outd (0x4B7, 0x5B7)

BIT	7	6	5	4	3	2	1	0
Field	FULL_FRAME_CRC_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FULL_FRAME_CRC_3	7:0	Frames CRC result

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ASYM0 (0x4C0, 0x5C0)

BIT	7	6	5	4	3	2	1	0
Field	M_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
M_L	7:0	Asymmetric dual-view total pixel count per frame in sub-image (low byte)

ASYM1 (0x4C1, 0x5C1)

BIT	7	6	5	4	3	2	1	0
Field	M_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
M_M	7:0	Asymmetric dual-view total pixel count per frame in sub-image (mid byte)

ASYM2 (0x4C2, 0x5C2)

BIT	7	6	5	4	3	2	1	0
Field	M_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
M_H	7:0	Asymmetric dual-view total pixel count per frame in sub-image (high byte)

ASYM3 (0x4C3, 0x5C3)

BIT	7	6	5	4	3	2	1	0
Field	N_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
N_L	7:0	Asymmetric dual-view total pixel count per frame for superframe (low byte)

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ASYM4 (0x4C4, 0x5C4)

BIT	7	6	5	4	3	2	1	0
Field	N_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
N_M	7:0	Asymmetric dual-view total pixel count per frame for superframe (mid byte)

ASYM5 (0x4C5, 0x5C5)

BIT	7	6	5	4	3	2	1	0
Field	N_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
N_H	7:0	Asymmetric dual-view total pixel count per frame for superframe (high byte)

ASYM6 (0x4C6, 0x5C6)

BIT	7	6	5	4	3	2	1	0
Field	X_OFF_WR_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
X_OFF_WR_L	7:0	Number of pixels to skip before writing when receiving a new line (low byte)

ASYM7 (0x4C7, 0x5C7)

BIT	7	6	5	4	3	2	1	0
Field	X_OFF_WR_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
X_OFF_WR_H	7:0	Number of pixels to skip before writing when receiving a new line (high byte)

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ASYM8 (0x4C8, 0x5C8)

BIT	7	6	5	4	3	2	1	0
Field	X_MAX_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
X_MAX_L	7:0	Index of the last pixel of sub-image in the superframe (low byte)

ASYM9 (0x4C9, 0x5C9)

BIT	7	6	5	4	3	2	1	0
Field	X_MAX_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
X_MAX_H	7:0	Index of the last pixel of sub-image in the superframe (high byte)

ASYM10 (0x4CA, 0x5CA)

BIT	7	6	5	4	3	2	1	0
Field	Y_MAX_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Y_MAX_L	7:0	Index of the last line of sub-image in the superframe (low byte)

ASYM11 (0x4CB, 0x5CB)

BIT	7	6	5	4	3	2	1	0
Field	Y_MAX_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Y_MAX_H	7:0	Index of the last line of sub-image in the superframe (high byte)

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ASYM12 (0x4CC, 0x5CC)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x80							
Access Type								

ASYM13 (0x4CD, 0x5CD)*

BIT	7	6	5	4	3	2	1	0
Field	LUT_TEMPLATE_SEL[3:0]				RSVD	RSVD	RSVD	RSVD
Reset	0x1				0b0	0b1	0b0	0b0
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
LUT_TEMPLATE_SEL	7:4	Select one of the predefined interfaces for asymmetric dual-view and line-skip method or the LUT-based method	0x0: Use LUT 0x1: 1:1 0x2: 2:1 0x3: 3:1 0x4: 4:1 0x5: 3:2 0x6: 4:3 0x7: 5:2 0x8: 5:3 0x9: 8:5 0xA: 2:1 inverted 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

ASYM14 (0x4CE, 0x5CE)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	ASYM_WR_B_MUX	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b1	0b1	0b1	0b1	0b1	0b1
Access Type					Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ASYM_WR_B_MUX	3	Set to 0 for asymmetric split	0x0: Video split enabled 0x1: Video split disabled

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ASYM17 (0x4D1, 0x5D1)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			RSVD	RSVD	RSVD	ASYM_UNDERFLOW	ASYM_OVERFLOW
Reset	0b111			0b1	0b0	0b0	0b0	0b0
Access Type							Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
ASYM_UNDERFLOW	1	Sticky underflow bit for FIFO	0x0: underflow not detected 0x1: underflow detected
ASYM_OVERFLOW	0	Sticky overflow bit for FIFO	0x0: overflow not detected 0x1: overflow detected

AR0 (0x4D8, 0x5D8)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_0	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DELAY cycles from the start. ([7:0])	0xXX: Least significant byte of VS delay

AR1 (0x4D9, 0x5D9)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_1	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the start. ([15:8])	0xXX: Middle significant byte of VS delay

AR2 (0x4DA, 0x5DA)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_2	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the start. ([23:16])	0xXX: Most significant byte of VS delay

AR3 (0x4DB, 0x5DB)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_0	7:0	VS high period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of VS high period

AR4 (0x4DC, 0x5DC)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_1	7:0	VS high period in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS high period

AR5 (0x4DD, 0x5DD)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_2	7:0	VS high period in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS high period

AR6 (0x4DE, 0x5DE)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_0	7:0	VS low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of VS low period

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AR7 (0x4DF, 0x5DF)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_1	7:0	VS low period in terms of PCLK cycles ([15:8])	0xXX: Middle significant byte of VS low period

AR8 (0x4E0, 0x5E0)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_2	7:0	VS low period in terms of PCLK cycles ([23:16])	0xXX: Most significant byte of VS low period

AR9 (0x4E1, 0x5E1)

BIT	7	6	5	4	3	2	1	0
Field	HS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_DLY_0	7:0	HS delay in terms of PCLK cycles The output HS is delayed by HS_DELAY cycles from the start. ([7:0])	0xXX: Least significant byte of VS delay

AR10 (0x4E2, 0x5E2)

BIT	7	6	5	4	3	2	1	0
Field	HS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_DLY_1	7:0	HS delay in terms of PCLK cycles The output HS is delayed by HS_DELAY cycles from the start. ([15:8])	0xXX: Least significant byte of VS delay

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AR11 (0x4E3, 0x5E3)

BIT	7	6	5	4	3	2	1	0
Field	HS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_DLY_2	7:0	HS delay in terms of PCLK cycles The output HS is delayed by HS_DELAY cycles from the start. ([23:16])	0xXX: Least significant byte of VS delay

AR12 (0x4E4, 0x5E4)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_0	7:0	HS high period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of HS high period

AR13 (0x4E5, 0x5E5)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_1	7:0	HS high period in terms of PCLK cycles ([15:8])	0xXX: Most significant byte of HS high period

AR14 (0x4E6, 0x5E6)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_0	7:0	HS low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of HS low period

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AR15 (0x4E7, 0x5E7)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_1	7:0	HS low period in terms of PCLK cycles ([15:8])	0xXX: Most significant byte of HS low period

AR16 (0x4E8, 0x5E8)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_0	7:0	HS pulses per frame ([7:0])	0xXX: Least significant byte of HS pulses per frame

AR17 (0x4E9, 0x5E9)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_1	7:0	HS pulses per frame ([15:8])	0xXX: Most significant byte of HS pulses per frame

AR18 (0x4EA, 0x5EA)

BIT	7	6	5	4	3	2	1	0
Field	HS_LLOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LLOW_0	7:0	HS long low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of HS low period

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AR19 (0x4EB, 0x5EB)

BIT	7	6	5	4	3	2	1	0
Field	HS_LLOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LLOW_1	7:0	HS long low period in terms of PCLK cycles ([15:8])	0xXX: Least significant byte of HS low period

AR20 (0x4EC, 0x5EC)

BIT	7	6	5	4	3	2	1	0
Field	HS_LLOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LLOW_2	7:0	HS long low period in terms of PCLK cycles ([23:16])	0xXX: Least significant byte of HS low period

AR21 (0x4ED, 0x5ED)

BIT	7	6	5	4	3	2	1	0
Field	DE_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DLY_0	7:0	DE delay in terms of PCLK cycles The output DE is delayed by DE_DELAY cycles from the start. ([7:0])	0xXX: Least significant byte of VS delay

AR22 (0x4EE, 0x5EE)

BIT	7	6	5	4	3	2	1	0
Field	DE_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DLY_1	7:0	DE delay in terms of PCLK cycles The output DE is delayed by DE_DELAY cycles from the start. ([15:8])	0xXX: Least significant byte of VS delay

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AR23 (0x4EF, 0x5EF)

BIT	7	6	5	4	3	2	1	0
Field	DE_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DLY_2	7:0	DE delay in terms of PCLK cycles The output DE is delayed by DE_DELAY cycles from the start. ([23:16])	0xXX: Least significant byte of VS delay

AR24 (0x4F0, 0x5F0)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_0	7:0	DE high period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of DE high period

AR25 (0x4F1, 0x5F1)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_1	7:0	DE high period in terms of PCLK cycles ([15:8])	0xXX: Most significant byte of DE high period

AR26 (0x4F2, 0x5F2)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_0	7:0	DE low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of DE low period

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AR27 (0x4F3, 0x5F3)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_1	7:0	DE low period in terms of PCLK cycles (15:8])	0xXX: Most significant byte of DE low period

AR28 (0x4F4, 0x5F4)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_0	7:0	Active lines per frame ([7:0])	0xXX: Least significant byte of DE pulses per frame

AR29 (0x4F5, 0x5F5)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_1	7:0	Active lines per frame ([15:8])	0xXX: Most significant byte of DE pulses per frame

AR30 (0x4F6, 0x5F6)

BIT	7	6	5	4	3	2	1	0
Field	DE_LLOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LLOW_0	7:0	DE long low period in terms of PCLK cycles ([7:0])	0xXX: Least significant byte of HS low period

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AR31 (0x4F7, 0x5F7)

BIT	7	6	5	4	3	2	1	0
Field	DE_LLOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LLOW_1	7:0	DE long low period in terms of PCLK cycles ([15:8])	0xXX: Least significant byte of HS low period

AR32 (0x4F8, 0x5F8)

BIT	7	6	5	4	3	2	1	0
Field	DE_LLOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LLOW_2	7:0	DE long low period in terms of PCLK cycles ([23:16])	0xXX: Least significant byte of HS low period

AR33 (0x4F9, 0x5F9)

BIT	7	6	5	4	3	2	1	0
Field	VS_INV	HS_INV	DE_INV	–	–	–	–	–
Reset	0b0	0b0	0b0	–	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_INV	7	Inverts VSYNC output of video timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INV	6	Inverts HSYNC output of video timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INV	5	Inverts DE output of video timing generator	0b0: Do not invert DE 0b1: Invert DE

BR23 (0xE00, 0xE40)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_1	7:0	SHA256 signature for video authentication byte Segment X. Bank A result.

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BR23H (0xE01, 0xE41)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_2	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR24 (0xE02, 0xE42)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_3	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR24H (0xE03, 0xE43)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_4	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR25 (0xE04, 0xE44)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_5[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_5	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

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BR25H (0xE05, 0xE45)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_6[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_6	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR26 (0xE06, 0xE46)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_7[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_7	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR26H (0xE07, 0xE47)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_8[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_8	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR27 (0xE08, 0xE48)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_9[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_9	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

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BR27H (0xE09, 0xE49)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_10[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_10	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR28 (0xE0A, 0xE4A)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_11[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_11	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR28H (0xE0B, 0xE4B)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_12[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_12	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR29 (0xE0C, 0xE4C)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_13[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_13	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

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BR29H (0xE0D, 0xE4D)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_14[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_14	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR30 (0xE0E, 0xE4E)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_15[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_15	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR30H (0xE0F, 0xE4F)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_16[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_16	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR31 (0xE10, 0xE50)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_17[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_17	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

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BR31H (0xE11, 0xE51)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_18[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_18	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR32 (0xE12, 0xE52)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_19[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_19	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR32H (0xE13, 0xE53)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_20[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_20	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR33 (0xE14, 0xE54)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_21[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_21	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

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BR33H (0xE15, 0xE55)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_22[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_22	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR34 (0xE16, 0xE56)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_23[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_23	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR34H (0xE17, 0xE57)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_24[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_24	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR35 (0xE18, 0xE58)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_25[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_25	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

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BR35H (0xE19, 0xE59)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_26[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_26	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR36 (0xE1A, 0xE5A)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_27[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_27	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR36H (0xE1B, 0xE5B)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_28[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_28	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR37 (0xE1C, 0xE5C)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_29[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_29	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

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BR37H (0xE1D, 0xE5D)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_30[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_30	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR38 (0xE1E, 0xE5E)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_31[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_31	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR38H (0xE1F, 0xE5F)

BIT	7	6	5	4	3	2	1	0
Field	SHA_A_32[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_A_32	7:0	SHA256 signature for video authentication byte segment X. Bank A result.

BR23 (0xE20, 0xE60)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_1	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

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BR23H (0xE21, 0xE61)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_2	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR24 (0xE22, 0xE62)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_3	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR24H (0xE23, 0xE63)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_4	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR25 (0xE24, 0xE64)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_5[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_5	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

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BR25H (0xE25, 0xE65)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_6[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_6	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR26 (0xE26, 0xE66)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_7[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_7	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR26H (0xE27, 0xE67)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_8[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_8	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR27 (0xE28, 0xE68)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_9[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_9	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

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BR27H (0xE29, 0xE69)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_10[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_10	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR28 (0xE2A, 0xE6A)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_11[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_11	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR28H (0xE2B, 0xE6B)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_12[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_12	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR29 (0xE2C, 0xE6C)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_13[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_13	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

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BR29H (0xE2D, 0xE6D)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_14[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_14	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR30 (0xE2E, 0xE6E)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_15[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_15	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR30H (0xE2F, 0xE6F)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_16[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_16	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR31 (0xE30, 0xE70)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_17[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_17	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

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BR31H (0xE31, 0xE71)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_18[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_18	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR32 (0xE32, 0xE72)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_19[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_19	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR32H (0xE33, 0xE73)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_20[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_20	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR33 (0xE34, 0xE74)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_21[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_21	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

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BR33H (0xE35, 0xE75)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_22[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_22	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR34 (0xE36, 0xE76)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_23[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_23	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR34H (0xE37, 0xE77)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_24[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_24	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR35 (0xE38, 0xE78)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_25[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_25	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

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BR35H (0xE39, 0xE79)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_26[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_26	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR36 (0xE3A, 0xE7A)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_27[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_27	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR36H (0xE3B, 0xE7B)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_28[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_28	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR37 (0xE3C, 0xE7C)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_29[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_29	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

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BR37H (0xE3D, 0xE7D)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_30[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_30	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR38 (0xE3E, 0xE7E)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_31[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_31	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

BR38H (0xE3F, 0xE7F)

BIT	7	6	5	4	3	2	1	0
Field	SHA_B_32[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SHA_B_32	7:0	SHA256 signature for video authentication byte segment X. Bank B result.

SPI_CC_WR_ (0x1300)

SPI/CC bridge write data: When the SPI/CC bridge mode is enabled, data written to the address is processed by the SPI bridge function as which is normally received by the internal SPI slave interface.

This behavior is also true for addresses 0x1301 to 0x137F. This is done to support burst writes on the CC interface.

SPI_CC_RD_ (0x1380)

SPI/CC bridge read data: When SPI/CC bridge mode is enabled, reads from this address return the output of the SPI Rx FIFO. If the FIFO is not empty (as indicated by BNE), the FIFO advances its read pointer in preparation for the next read from this space. Normally, the SPI slave transmits this data over the SPI interface.

This behavior is also true for addresses 0x1380 to 0x13FF. This is done to support burst reads on the CC interface. SPIS_BYTE_CNTcan be read to determine the proper burst length to read valid data from the FIFO.

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RLMS4 (0x1404, 0x1504)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x4				0b10		0b1	0b1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	A factor (N) used to select the order of number of observations in each eye-monitor window. N is used in the equation: Observations = 6.29 x $10^{(N + 2)}$	0xX: N factor
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits to allow in a measurement window.	0b00: Allow no errors 0b01: Allow one error 0b10: Allow two errors 0b11: Allow three errors
EOM_PER_MODE	1	Eye-opening monitor periodic mode enable.	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Eye-opening monitor enable.	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

RLMS5 (0x1405, 0x1505)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0b0	0b0010000						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye-opening monitor manual trigger. For use when periodic mode is disabled.	0b0: No action 0b1: EOM manual trigger request
EOM_MIN_THR	6:0	The EOM minimum threshold as defined by the equation: % eye-opening = EOM_MIN_THR/64 If the value is zero, the EOM is disabled.	0xXX: EOM minimum threshold factor

RLMS6 (0x1406, 0x1506)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	EOM_RST_THR[6:0]						
Reset	0b1	0b0000000						
Access Type	Write, Read	Write, Read						

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BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_MODE	7	Eye-opening is measured vertically or horizontally.	0b0: Vertical opening mode 0b1: Horizontal opening mode
EOM_RST_THR	6:0	The EOM refresh threshold as defined by the equation: % eye-opening = EOM_MIN_THR/64. Used only with periodic EOM mode. If the value is zero, the EOM is disabled.	0xXX: EOM refresh threshold factor

RLMS7 (0x1407, 0x1507)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-opening monitor measurement done	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Last completed EOM observation	0xXX: EOM measurement result

RLMS64 (0x1464, 0x1564)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				–	RSVD	TxSSCMode[1:0]	
Reset	0x9				–	0b0	0b00	
Access Type					–		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx Spread-Spectrum Mode	0b00: Manual Phase Mode 0b01: Reserved 0b10: Reserved 0b11: SSC enabled

RLMS70 (0x1470, 0x1570)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0b0000001						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx SSC Modulation Frequency Control	0x07: SSC 268ppm 0x06: SSC 580ppm 0x03: SSC 970ppm 0x01: SSC 1750ppm 0x01: SSC 2530ppm others: Reserved

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RLMS71 (0x1471, 0x1571)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0b000001						0b0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx SSC Center Spread Starting Phase	0x02: SSC 268ppm 0x02: SSC 580ppm 0x02: SSC 970ppm 0x02: SSC 1750ppm 0x02: SSC 2530ppm others: Reserved
TxSSCEn	0	Tx Spread-Spectrum Enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x1472, 0x1572)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx SSC Frequency Prescaler Low	0xC9: SSC 268ppm 0xAB: SSC 580ppm 0xAB: SSC 970ppm 0xF9: SSC 1750ppm 0xAB: SSC 2530ppm others: Reserved

RLMS73 (0x1473, 0x1573)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclH	2:0	Tx SSC Frequency Prescaler High	0x02: SSC 268ppm 0x00: SSC 580ppm 0x00: SSC 970ppm 0x00: SSC 1750ppm 0x00: SSC 2530ppm others: Reserved

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RLMS74 (0x1474, 0x1574)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx SSC Phase Accumulator Increment Low	0xF9: SSC 268ppm 0x63: SSC 580ppm 0x63: SSC 970ppm 0x2C: SSC 1750ppm 0x63: SSC 2530ppm others: Reserved

RLMS75 (0x1475, 0x1575)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx SSC Phase Accumulator Increment High	0x01: SSC 268ppm 0x07: SSC 580ppm 0x07: SSC 970ppm 0x05: SSC 1750ppm 0x07: SSC 2530ppm others: Reserved

RLMS76 (0x1476, 0x1576)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx SSC Phase Starting Phase Quadrant	0x00: SSC 268ppm 0x00: SSC 580ppm 0x00: SSC 970ppm 0x00: SSC 1750ppm 0x00: SSC 2530ppm others: Reserved

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HDCP_DES0 (0x1676, 0x1776)

BIT	7	6	5	4	3	2	1	0
Field	AH_DES_REG_OFFSET_L[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AH_DES_REG_OFFSET_L	7:0	Low byte of the register offset of the HDCP register block of the paired deserializer	0xXX: Low byte (LSB) of the register offset of deserializer's HDCP register block

HDCP_DES1 (0x1677, 0x1777)

BIT	7	6	5	4	3	2	1	0
Field	AH_DES_REG_OFFSET_H[7:0]							
Reset	0x16							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AH_DES_REG_OFFSET_H	7:0	High byte of the register offset of the HDCP register block of the paired deserializer	0xXX: High byte (MSB) of the register offset of deserializer's HDCP register block

HDCP_AS0 (0x1678, 0x1778)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_0	7:0	Optional seed for internal random number generator	0xXX: Byte 0 (LSB) of the internal random number generator seed

HDCP_AS1 (0x1679, 0x1779)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_1	7:0	Optional seed for internal random number generator	0xXX: Byte 1 of the internal random number generator seed

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HDCP_AS2 (0x167A, 0x177A)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_2	7:0	Optional seed for internal random number generator	0xXX: Byte 2 of the internal random number generator seed

HDCP_AS3 (0x167B, 0x177B)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_3	7:0	Optional seed for internal random number generator	0xXX: Byte 3 of the internal random number generator seed

HDCP_AS4 (0x167C, 0x177C)

BIT	7	6	5	4	3	2	1	0
Field	ASEED_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ASEED_4	7:0	Optional seed for internal random number generator	0xXX: Byte 4 (MSB) of the internal random number generator seed

HDCP_TX0 (0x1680, 0x1780)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_0	7:0	HDCP Receiver KSV	0xXX: Byte 0 (LSB) of the HDCP receiver KSV

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HDCP_TX1 (0x1681, 0x1781)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_1	7:0	HDCP Receiver KSV	0xXX: Byte 1 of the HDCP receiver KSV

HDCP_TX2 (0x1682, 0x1782)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_2	7:0	HDCP Receiver KSV	0xXX: Byte 2 of the HDCP receiver KSV

HDCP_TX3 (0x1683, 0x1783)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_3	7:0	HDCP Receiver KSV	0xXX: Byte 3 of the HDCP receiver KSV

HDCP_TX4 (0x1684, 0x1784)

BIT	7	6	5	4	3	2	1	0
Field	GMSL_BKSV_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL_BKSV_4	7:0	HDCP Receiver KSV	0xXX: Byte 4 (MSB) of the HDCP receiver KSV

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HDCP_TX5 (0x1685, 0x1785)

BIT	7	6	5	4	3	2	1	0
Field	RIP_0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RIP_0	7:0	Link verification response EN_INT_COMP = 0 → Ri of Tx (Read) EN_INT_COMP = 1 → Ri' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of Ri or Ri'

HDCP_TX6 (0x1686, 0x1786)

BIT	7	6	5	4	3	2	1	0
Field	RIP_1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RIP_1	7:0	Link verification response EN_INT_COMP = 0 → Ri of Tx (Read) EN_INT_COMP = 1 → Ri' of Rx (Write and Read)	0xXX: Byte 1 (MSB) of Ri or Ri'

HDCP_TX7 (0x1687, 0x1787)

BIT	7	6	5	4	3	2	1	0
Field	PJP[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PJP	7:0	Enhanced link verification response EN_INT_COMP = 0 → Pj of Tx (Read) EN_INT_COMP = 1 → Pj' of Rx (Write and Read)	0xXX: Value of Pj or Pj'

HDCP_TX8 (0x1688, 0x1788)

BIT	7	6	5	4	3	2	1	0
Field	AN_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_0	7:0	Session random number	0xXX: Byte 0 (LSB) of the session random number

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HDCP_TX9 (0x1689, 0x1789)

BIT	7	6	5	4	3	2	1	0
Field	AN_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_1	7:0	Session random number	0xXX: Byte 1 of the session random number

HDCP_TXA (0x168A, 0x178A)

BIT	7	6	5	4	3	2	1	0
Field	AN_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_2	7:0	Session random number	0xXX: Byte 2 of the session random number

HDCP_TXB (0x168B, 0x178B)

BIT	7	6	5	4	3	2	1	0
Field	AN_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_3	7:0	Session random number	0xXX: Byte 3 of the session random number

HDCP_TXC (0x168C, 0x178C)

BIT	7	6	5	4	3	2	1	0
Field	AN_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_4	7:0	Session random number	0xXX: Byte 4 of the session random number

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HDCP_TXD (0x168D, 0x178D)

BIT	7	6	5	4	3	2	1	0
Field	AN_5[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_5	7:0	Session random number	0xXX: Byte 5 of the session random number

HDCP_TXE (0x168E, 0x178E)

BIT	7	6	5	4	3	2	1	0
Field	AN_6[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_6	7:0	Session random number	0xXX: Byte 6 of the session random number

HDCP_TXF (0x168F, 0x178F)

BIT	7	6	5	4	3	2	1	0
Field	AN_7[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AN_7	7:0	Session random number	0xXX: Byte 7 (MSB) of the session random number

HDCP_TX10 (0x1690, 0x1790)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_0	7:0	HDCP transmitter KSV	0xXX: Byte 0 (LSB) of the HDCP transmitter KSV

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HDCP_TX11 (0x1691, 0x1791)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_1	7:0	HDCP transmitter KSV	0xXX: Byte 1 of the HDCP transmitter KSV

HDCP_TX12 (0x1692, 0x1792)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_2	7:0	HDCP transmitter KSV	0xXX: Byte 2 of the HDCP transmitter KSV

HDCP_TX13 (0x1693, 0x1793)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_3	7:0	HDCP transmitter KSV	0xXX: Byte 3 of the HDCP transmitter KSV

HDCP_TX14 (0x1694, 0x1794)

BIT	7	6	5	4	3	2	1	0
Field	AKSV_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AKSV_4	7:0	HDCP transmitter KSV	0xXX: Byte 4 (MSB) of the HDCP transmitter KSV

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HDCP_TX15 (0x1695, 0x1795)

BIT	7	6	5	4	3	2	1	0
Field	–	EN_INT_COMP	–	–	HDCP_RESET	START_AUTH	VSYNC_DET	ENC_EN
Reset	–	0b0	–	–	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	–	–	Write, Read	Write Clears All, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_INT_COMP	6	Enable internal comparison mode	0b0: µC comparison mode 0b1: Internal comparison mode
HDCP_RESET	3	Automatically resets to 0 ~ 1µs after it has written 1	0b0: Normal operation 0b1: Reset HDCP circuits
START_AUTH	2	Start HDCP authentication. Automatically resets to 0 after written.	0b0: Normal operation 0b1: Start authentication
VSYNC_DET	1	Automatically sets to 1 when VSYNC falling edge is detected	0b0: VSYNC falling edge not detected 0b1: VSYNC falling edge detected
ENC_EN	0	Enable HDCP encryption	0b0: HDCP encryption disabled 0b1: HDCP encryption enabled

HDCP_TX16 (0x1696, 0x1796)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PJF_MATCH	V_MATCHED	PJ_MATCHED	RI_MATCHED	INVALID_BKSV
Reset	–	–	–	0b0	0b0	0b0	0b0	0b1
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PJF_MATCH	4	At least one byte of Fast-Pj matches Fast-Pj'	0b0: Fast-Pj does not match Fast-Pj' 0b1: Fast-Pj matches Fast-Pj'
V_MATCHED	3	V matched V'	0b0: V does not match V' 0b1: V matches V'
PJ_MATCHED	2	Pj matched Pj'	0b0: Pj does not match Pj' 0b1: Pj matches Pj'
RI_MATCHED	1	Ri matched Ri'	0b0: Ri did not match Ri' 0b1: Ri matched Ri'
INVALID_BKSV	0	Invalid BKSV detected	0b0: BKSV is valid 0b1: BKSV is invalid

HDCP_TX17 (0x1697, 0x1797)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[6:0]							HDCP_REPEATER
Reset	0b0000000							0b0
Access Type								Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_REPEATER	0	HDCP repeater enable	0b0: HDCP repeater not enabled 0b1: HDCP repeater enabled

HDCP_TX18 (0x1698, 0x1798)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RSVD	7:0	Auto-HDCP status Read will automatically clear all bit [3:0]. [7:5] AH_STATE If AH_FAIL = 1 when read, 0b000: AHDCP reset state 0b001: AHDCP waiting for video link to setup 0b010: AHDCP in first part of authentication 0b011: AHDCP in second/third part of authentication 0b100: V' do not match 0b101: Max devices or cascade exceeded 0b110: R0 do not match 0b111: Bad BKSV [4] ENCRYPT_ON 0b1: HDCP encryption is running [3] AH_ENCOFF 0b1: Indicates that encryption is not enabled for more than 0.5 second or 1 second. Value 1 also sets INT if unmasked. Read to clear bit. [2] AH_NEW_DEV 0b1: New device is attached downstream. Value 1 also sets INT if unmasked. Read to clear bit. If DES is not a repeater, bit is always 0 after authentication and initial read. This bit mirrors DES BSTATUS NEW_DEV_CONN bit. DES NEW_DEV_CONN is cleared by AHDCP after setting this bit. [1] AH_KSV_READY 0b1: After BKSV or KSV_LIST are updated and checked (BKSV has 20 zero and 20 one. R0 and V' are matched). BKSV/KSV List are ready for upstream. Value 1 also sets INT if unmasked. Read to clear bit. If DES is not a repeater, bit is always 0 after authentication and initial read of 1. After reading DES BSTATUS, AHDCP controller clears DES BSTATUS register after V' matches. [0] AH_FAIL 0b1: AHDCP operation error. Value 1 also sets INT if unmasked. Read to clear bit. When AH_FAIL = 1, AHDCP controller stops. Reading this register automatically re-starts AHDCP

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HDCP_TX19 (0x1699, 0x1799)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	–	–	DIS_AUDIO_ENC
Reset	0b00		–	–	–	–	–	0b0
Access Type			–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_AUDIO_ENC	0	Disable encryption of audio	0b0: Audio encryption enabled 0b1: Audio encryption disabled

HDCP_TX1A (0x169A, 0x179A)

BIT	7	6	5	4	3	2	1	0
Field	PJFP_0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PJFP_0	7:0	Fast enhanced link verification response (low 8 bits) EN_INT_COMP = 0 → Pjf of Tx (Read) EN_INT_COMP = 1 → Pjf' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of Pjf or Pjf'

HDCP_TX1B (0x169B, 0x179B)

BIT	7	6	5	4	3	2	1	0
Field	PJFP_1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PJFP_1	7:0	Fast enhanced link verification response (middle 8 bits) EN_INT_COMP = 0 → Pjf of Tx (Read) EN_INT_COMP = 1 → Pjf' of Rx (Write and Read)	0xXX: Byte 1 of Pjf or Pjf'

HDCP_TX1C (0x169C, 0x179C)

BIT	7	6	5	4	3	2	1	0
Field	PJFP_2[7:0]							
Reset	0xFF							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
PJFP_2	7:0	Fast enhanced link verification response (high 8 bits) EN_INT_COMP = 0 → Pjf of Tx (Read) EN_INT_COMP = 1 → Pjf' of Rx (Write and Read)	0xXX: Byte 2 (MSB) of Pjf or Pjf'

HDCP_TX20 (0x16A0, 0x17A0)

BIT	7	6	5	4	3	2	1	0
Field	VH0_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH0_0	7:0	H0 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H0 or V'.H0

HDCP_TX21 (0x16A1, 0x17A1)

BIT	7	6	5	4	3	2	1	0
Field	VH0_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH0_1	7:0	H0 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H0 or V'.H0

HDCP_TX22 (0x16A2, 0x17A2)

BIT	7	6	5	4	3	2	1	0
Field	VH0_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH0_2	7:0	H0 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H0 or V'.H0

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HDCP_TX23 (0x16A3, 0x17A3)

BIT	7	6	5	4	3	2	1	0
Field	VH0_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH0_3	7:0	H0 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H0 or V'.H0

HDCP_TX24 (0x16A4, 0x17A4)

BIT	7	6	5	4	3	2	1	0
Field	VH1_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH1_0	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H1 or V'.H1

HDCP_TX25 (0x16A5, 0x17A5)

BIT	7	6	5	4	3	2	1	0
Field	VH1_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH1_1	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H1 or V'.H1

HDCP_TX26 (0x16A6, 0x17A6)

BIT	7	6	5	4	3	2	1	0
Field	VH1_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
VH1_2	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H1 or V'.H1

HDCP_TX27 (0x16A7, 0x17A7)

BIT	7	6	5	4	3	2	1	0
Field	VH1_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH1_3	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H1 or V'.H1

HDCP_TX28 (0x16A8, 0x17A8)

BIT	7	6	5	4	3	2	1	0
Field	VH2_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH2_0	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H2 or V'.H2

HDCP_TX29 (0x16A9, 0x17A9)

BIT	7	6	5	4	3	2	1	0
Field	VH2_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH2_1	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H2 or V'.H2

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HDCP_TX2A (0x16AA, 0x17AA)

BIT	7	6	5	4	3	2	1	0
Field	VH2_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH2_2	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H2 or V'.H2

HDCP_TX2B (0x16AB, 0x17AB)

BIT	7	6	5	4	3	2	1	0
Field	VH2_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH2_3	7:0	H1 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H2 or V'.H2

HDCP_TX2C (0x16AC, 0x17AC)

BIT	7	6	5	4	3	2	1	0
Field	VH3_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH3_0	7:0	H3 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H3 or V'.H3

HDCP_TX2D (0x16AD, 0x17AD)

BIT	7	6	5	4	3	2	1	0
Field	VH3_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
VH3_1	7:0	H3 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H3 or V'.H3

HDCP_TX2E (0x16AE, 0x17AE)

BIT	7	6	5	4	3	2	1	0
Field	VH3_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH3_2	7:0	H3 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H3 or V'.H3

HDCP_TX2F (0x16AF, 0x17AF)

BIT	7	6	5	4	3	2	1	0
Field	VH3_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH3_3	7:0	H3 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H3 or V'.H3

HDCP_TX30 (0x16B0, 0x17B0)

BIT	7	6	5	4	3	2	1	0
Field	VH4_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH4_0	7:0	H4 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 0 (LSB) of V.H4 or V'.H4

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HDCP_TX31 (0x16B1, 0x17B1)

BIT	7	6	5	4	3	2	1	0
Field	VH4_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH4_1	7:0	H4 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 1 of V.H4 or V'.H4

HDCP_TX32 (0x16B2, 0x17B2)

BIT	7	6	5	4	3	2	1	0
Field	VH4_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH4_2	7:0	H4 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 2 of V.H4 or V'.H4

HDCP_TX33 (0x16B3, 0x17B3)

BIT	7	6	5	4	3	2	1	0
Field	VH4_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VH4_3	7:0	H4 part of SHA-1 hash value EN_INT_COMP = 0 → V of Tx (Read) EN_INT_COMP = 1 → V' of Rx (Write and Read)	0xXX: Byte 3 (MSB) of V.H4 or V'.H4

HDCP_TX34 (0x16B4, 0x17B4)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_MAX_DEV_EXCEEDED	HDCP_DEV_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

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BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_MAX_DEV_EXCEEDED	7	Maximum device count exceeded in repeater mode	0b0: Maximum number of devices not exceeded (14 or less) 0b1: Maximum number of devices exceeded (more than 14)
HDCP_DEV_CNT	6:0	Repeater device count	0bXXXXXXX: Number of devices attached

HDCP_TX35 (0x16B5, 0x17B5)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				HDCP_MAX_CASCADE_EXCEEDED	HDCP_DEPTH[2:0]		
Reset	0x0				0b0	0b000		
Access Type					Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_MAX_CASCADE_EXCEEDED	3	HDCP repeater mode exceeded maximum depth	0b0: Maximum number of cascaded devices not exceeded (7 or less) 0b1: Maximum number of cascaded devices exceeded (more than 7)
HDCP_DEPTH	2:0	HDCP repeater depth	0bXXX: Depth of cascaded devices

HDCP_TX36 (0x16B6, 0x17B6)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_GPMEM[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_GPMEM	7:0	General purpose memory byte. This has no effect on the operation of the device, it can be used for handshaking between more than one microcontroller in the system.	0xXX: General purpose memory byte

HDCP_TX37 (0x16B7, 0x17B7)*

BIT	7	6	5	4	3	2	1	0
Field	HDCP_PD	FAST_PJ_EN	FORCE_AUDIO	FORCE_VIDEO	AH_MASK_ENCOFF	AH_MASK_NEWDEV	AH_MASK_KSVRDY	AH_MASK_FAIL
Reset	0b1	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_PD	7	Power down HDCP blocks	0b0: HDCP blocks powered up 0b1: Power down HDCP blocks
FAST_PJ_EN	6	Enable Fast-Pj mode (fast-enhanced link integrity check)	0b0: Normal Pj mode 0b1: Fast-Pj mode enabled
FORCE_AUDIO	5	Force to static audio	0b0: Normal operation 0b1: Force audio data to 0
FORCE_VIDEO	4	Force to static video	0b0: Normal operation 0b1: Force video to static video
AH_MASK_ENCOFF	3	Disable auto-HDCP encryption-off interrupt	0b0: Auto-HDCP encryption off interrupt enabled 0b1: Auto-HDCP encryption off interrupt masked
AH_MASK_NEWDEV	2	Disable auto-HDCP new-device interrupt	0b0: Auto-HDCP new device interrupt enabled 0b1: Auto-HDCP new device interrupt masked
AH_MASK_KSVRDY	1	Disable auto-HDCP new-device interrupt	0b0: Auto-HDCP KSV ready interrupt enabled 0b1: Auto-HDCP KSV ready interrupt masked
AH_MASK_FAIL	0	Disable auto-HDCP fail interrupt	0b0: Auto-HDCP fail interrupt enabled 0b1: Auto-HDCP fail interrupt masked

HDCP_TX38 (0x16B8, 0x17B8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	AH_RD_KSVL	AH_DISENC	AH_MODE
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write Clears All, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AH_RD_KSVL	2	Set this bit to 1 to begin Part 2 authentication for repeater DES. This bit is always read 0. In the DES repeater case, when the downstream KSV list is ready, the µC must set DES BSTATUS READY = 1 (and NEW_DEV_CONN = 1 if there is a new device attached), then write AH_RD_KSVLIS = 1 to trigger AHDCP to read the KSV list and check V's. If V' matches, AH_KSV_READY is set and DES BSTATUS is cleared.	0b0: Normal operation 0b1: Start Part 2 authentification for repeater deserializer
AH_DISENC	1	This bit is used to enable/disable cypher (encryption) in AHDCP mode without trigger reauthentication. 0: Enable cypher in next VS frame. 1: Disable cypher in next VS frame. Before changing AH_MODE from 1 to 0, make sure to set AH_DISENC = 1 and wait two VS frames to disable encyption for both SER and DES. Alternatively, set ENCRYPTION_ENABLE bit in both SER and DES to 0.	0b0: Enable encryption in next VS frame 0b1: Disable encryption in next VS frame
AH_MODE	0	Auto-HDCP enable. Before setting AH_MODE from 1 to 0, first set AH_DISENC from 0 to 1 and wait for about three VSYNC frame times so that encryption is turned off.	0b0: Manual HDCP or non-HDCP mode 0b1: Auto-HDCP mode

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HDCP_TX39 (0x16B9, 0x17B9)*

BIT	7	6	5	4	3	2	1	0
Field	AH_DES_ADDR[6:0]							–
Reset	0b1001000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
AH_DES_ADDR	7:1	Device address of the connected deserializer	0bXXXXXXX: Device address of the connected deserializer

HDCP_TX3A (0x16BA, 0x17BA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_0	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 0

HDCP_TX3B (0x16BB, 0x17BB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_1	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 1

HDCP_TX3C (0x16BC, 0x17BC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_2	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 2

HDCP_TX3D (0x16BD, 0x17BD)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_3	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 3

HDCP_TX3E (0x16BE, 0x17BE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_4	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 4

HDCP_TX3F (0x16BF, 0x17BF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_5	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 5

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HDCP_TX40 (0x16C0, 0x17C0)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_6	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 6

HDCP_TX41 (0x16C1, 0x17C1)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_7	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 7

HDCP_TX42 (0x16C2, 0x17C2)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_8	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 8

HDCP_TX43 (0x16C3, 0x17C3)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_9	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 9

HDCP_TX44 (0x16C4, 0x17C4)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_10	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 10

HDCP_TX45 (0x16C5, 0x17C5)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_11	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 11

HDCP_TX46 (0x16C6, 0x17C6)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_12	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 12

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HDCP_TX47 (0x16C7, 0x17C7)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_13	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 13

HDCP_TX48 (0x16C8, 0x17C8)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_14	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 14

HDCP_TX49 (0x16C9, 0x17C9)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_15	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 15

HDCP_TX4A (0x16CA, 0x17CA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_16[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_16	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 16

HDCP_TX4B (0x16CB, 0x17CB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_17[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_17	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 17

HDCP_TX4C (0x16CC, 0x17CC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_18[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_18	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 18

HDCP_TX4D (0x16CD, 0x17CD)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_19[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_19	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 19

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HDCP_TX4E (0x16CE, 0x17CE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_20[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_20	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 20

HDCP_TX4F (0x16CF, 0x17CF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_21[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_21	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 21

HDCP_TX50 (0x16D0, 0x17D0)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_22[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_22	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 22

HDCP_TX51 (0x16D1, 0x17D1)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_23[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_23	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 23

HDCP_TX52 (0x16D2, 0x17D2)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_24[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_24	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 24

HDCP_TX53 (0x16D3, 0x17D3)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_25[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_25	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 25

HDCP_TX54 (0x16D4, 0x17D4)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_26[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_26	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 26

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HDCP_TX55 (0x16D5, 0x17D5)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_27[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_27	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 27

HDCP_TX56 (0x16D6, 0x17D6)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_28[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_28	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 28

HDCP_TX57 (0x16D7, 0x17D7)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_29[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_29	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 29

HDCP_TX58 (0x16D8, 0x17D8)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_30[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_30	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 30

HDCP_TX59 (0x16D9, 0x17D9)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_31[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_31	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 31

HDCP_TX5A (0x16DA, 0x17DA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_32[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_32	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 32

HDCP_TX5B (0x16DB, 0x17DB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_33[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_33	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 33

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HDCP_TX5C (0x16DC, 0x17DC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_34[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_34	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 34

HDCP_TX5D (0x16DD, 0x17DD)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_35[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_35	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 35

HDCP_TX5E (0x16DE, 0x17DE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_36[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_36	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 36

HDCP_TX5F (0x16DF, 0x17DF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_37[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_37	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 37

HDCP_TX60 (0x16E0, 0x17E0)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_38[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_38	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 38

HDCP_TX61 (0x16E1, 0x17E1)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_39[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_39	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 39

HDCP_TX62 (0x16E2, 0x17E2)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_40[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_40	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 40

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HDCP_TX63 (0x16E3, 0x17E3)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_41[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_41	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 41

HDCP_TX64 (0x16E4, 0x17E4)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_42[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_42	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 42

HDCP_TX65 (0x16E5, 0x17E5)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_43[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_43	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 43

HDCP_TX66 (0x16E6, 0x17E6)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_44[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_44	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 44

HDCP_TX67 (0x16E7, 0x17E7)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_45[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_45	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 45

HDCP_TX68 (0x16E8, 0x17E8)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_46[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_46	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 46

HDCP_TX69 (0x16E9, 0x17E9)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_47[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_47	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 47

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HDCP_TX6A (0x16EA, 0x17EA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_48[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_48	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 48

HDCP_TX6B (0x16EB, 0x17EB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_49[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_49	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 49

HDCP_TX6C (0x16EC, 0x17EC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_50[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_50	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 50

HDCP_TX6D (0x16ED, 0x17ED)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_51[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_51	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 51

HDCP_TX6E (0x16EE, 0x17EE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_52[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_52	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 52

HDCP_TX6F (0x16EF, 0x17EF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_53[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_53	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 53

HDCP_TX70 (0x16F0, 0x17F0)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_54[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_54	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 54

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HDCP_TX71 (0x16F1, 0x17F1)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_55[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_55	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 55

HDCP_TX72 (0x16F2, 0x17F2)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_56[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_56	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 56

HDCP_TX73 (0x16F3, 0x17F3)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_57[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_57	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 57

HDCP_TX74 (0x16F4, 0x17F4)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_58[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_58	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 58

HDCP_TX75 (0x16F5, 0x17F5)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_59[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_59	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 59

HDCP_TX76 (0x16F6, 0x17F6)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_60[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_60	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 60

HDCP_TX77 (0x16F7, 0x17F7)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_61[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_61	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 61

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HDCP_TX78 (0x16F8, 0x17F8)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_62[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_62	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 62

HDCP_TX79 (0x16F9, 0x17F9)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_63[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_63	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 63

HDCP_TX7A (0x16FA, 0x17FA)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_64[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_64	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 64

HDCP_TX7B (0x16FB, 0x17FB)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_65[7:0]							
Reset	0x00							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_65	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 65

HDCP_TX7C (0x16FC, 0x17FC)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_66[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_66	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 66

HDCP_TX7D (0x16FD, 0x17FD)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_67[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_67	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 67

HDCP_TX7E (0x16FE, 0x17FE)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_68[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_68	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 68

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HDCP_TX7F (0x16FF, 0x17FF)

BIT	7	6	5	4	3	2	1	0
Field	KSV_LIST_69[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KSV_LIST_69	7:0	List of key selection vectors of all downstream repeaters and receivers (maximum of total 14 downstream repeaters and receivers are supported, 14 x 5 = 70)	0xXX: KSV list byte 69

REGCRC0 (0x1D00)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	GEN_ROLLING_CRC	I2C_WR_COMPUTE	PERIODIC_COMPUTE	CHECK_CRC	RESET_CRC
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–		Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_ROLLING_CRC	4	Calculate CRC using additional 4-bit counter, so CRC value cycles every 16 invocations	0x0: Disabled 0x1: Enabled
I2C_WR_COMPUTE	3	Do CRC compute after every I^2C register write	0x0: Disabled 0x1: Enabled
PERIODIC_COMPUTE	2	Do CRC checking on periodic basis, based on CRC_PERIOD value	0x0: Disabled 0x1: Enabled
CHECK_CRC	1	Upon calculation of CRC, compare with previous calculation, except on first time through. On miscompare, issue ERRB.	0x0: Do not check CRC 0x1: Check CRC
RESET_CRC	0	Reset CRC value to 16'FFFF	0x0: Do not reset CRC value 0x1: Reset CRC value

REGCRC1 (0x1D01)*

BIT	7	6	5	4	3	2	1	0
Field	CRC_PERIOD[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CRC_PERIOD	7:0	Period for CRC recomputation Period = (value+1)*2ms

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REGCRC2 (0x1D02)

BIT	7	6	5	4	3	2	1	0
Field	REGCRC_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGCRC_LSB	7:0	CRC result LSB

REGCRC3 (0x1D03)

BIT	7	6	5	4	3	2	1	0
Field	REGCRC_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REGCRC_MSB	7:0	CRC result MSB

REGCRC4 (0x1D04)*

BIT	7	6	5	4	3	2	1	0
Field	MIN_RANGE_LSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MIN_RANGE_LSB	7:0	Minimum Range LSB

REGCRC5 (0x1D05)*

BIT	7	6	5	4	3	2	1	0
Field	MIN_RANGE_MSB[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MIN_RANGE_MSB	7:0	Minimum Range LSB

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REGCRC6 (0x1D06)*

BIT	7	6	5	4	3	2	1	0
Field	MAX_RANGE_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MAX_RANGE_LSB	7:0	Maximum Range LSB

REGCRC7 (0x1D07)*

BIT	7	6	5	4	3	2	1	0
Field	MAX_RANGE_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MAX_RANGE_MSB	7:0	Maximum Range MSB

REGCRC8 (0x1D08)

BIT	7	6	5	4	3	2	1	0
Field	SKIP0_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP0_LSB	7:0	Address 0 to skip (LSB)

REGCRC9 (0x1D09)

BIT	7	6	5	4	3	2	1	0
Field	SKIP0_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP0_MSB	7:0	Address 0 to skip (MSB)

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REGCRC10 (0x1D0A)

BIT	7	6	5	4	3	2	1	0
Field	SKIP1_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP1_LSB	7:0	Address 1 to skip (LSB)

REGCRC11 (0x1D0B)

BIT	7	6	5	4	3	2	1	0
Field	SKIP1_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP1_MSB	7:0	Address 1 to skip (MSB)

REGCRC12 (0x1D0C)

BIT	7	6	5	4	3	2	1	0
Field	SKIP2_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP2_LSB	7:0	Address 2 to skip (LSB)

REGCRC13 (0x1D0D)

BIT	7	6	5	4	3	2	1	0
Field	SKIP2_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP2_MSB	7:0	Address 2 to skip (MSB)

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REGCRC14 (0x1D0E)

BIT	7	6	5	4	3	2	1	0
Field	SKIP3_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP3_LSB	7:0	Address 3 to skip (LSB)

REGCRC15 (0x1D0F)

BIT	7	6	5	4	3	2	1	0
Field	SKIP3_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP3_MSB	7:0	Address 3 to skip (MSB)

REGCRC16 (0x1D10)

BIT	7	6	5	4	3	2	1	0
Field	SKIP4_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP4_LSB	7:0	Address 4 to skip (LSB)

REGCRC17 (0x1D11)

BIT	7	6	5	4	3	2	1	0
Field	SKIP4_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP4_MSB	7:0	Address 4 to skip (MSB)

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REGCRC18 (0x1D12)

BIT	7	6	5	4	3	2	1	0
Field	SKIP5_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP5_LSB	7:0	Address 5 to skip (LSB)

REGCRC19 (0x1D13)

BIT	7	6	5	4	3	2	1	0
Field	SKIP5_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP5_MSB	7:0	Address 5 to skip (MSB)

REGCRC20 (0x1D14)

BIT	7	6	5	4	3	2	1	0
Field	SKIP6_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP6_LSB	7:0	Address 6 to skip (LSB)

REGCRC21 (0x1D15)

BIT	7	6	5	4	3	2	1	0
Field	SKIP6_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP6_MSB	7:0	Address 6 to skip (MSB)

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REGCRC22 (0x1D16)

BIT	7	6	5	4	3	2	1	0
Field	SKIP7_LSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP7_LSB	7:0	Address 7 to skip (LSB)

REGCRC23 (0x1D17)

BIT	7	6	5	4	3	2	1	0
Field	SKIP7_MSB[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SKIP7_MSB	7:0	Address 7 to skip (MSB)

CC_CRC0 (0x1D20)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_VAL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CC_CRC_VAL	7:0	Calculated CRC value for the last write transaction

CC_CRC1 (0x1D21)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_LSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_LSB	7:0	Bits 7:0 of current message counter value

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CC_CRC2 (0x1D22)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_MSB	7:0	Bits 15:8 of current message counter value

CC_CRC3 (0x1D23)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CC_CRC_ERR_CNT	7:0	Number of CC CRC errors detected

CC_CRC4 (0x1D24)

BIT	7	6	5	4	3	2	1	0
Field	MSGCNTR_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSGCNTR_ERR_CNT	7:0	Number of Message Counter errors detected

CC_CRC5 (0x1D25)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RESET_MSGCNTR	–	–	RESET_MSGCNTR_ERR_CNT	RESET_CC_CRC_ERR_CNT
Reset	–	–	–	0b0	–	–	0b0	0b0
Access Type	–	–	–	Write Clears All, Read	–	–	Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_MSGCNTR	4	Reset MSGCNTR_MSB and MSGCNTR_LSB to 0 (this bit automatically clears)	0x0: Do not reset 0x1: Reset
RESET_MSGCNTR_ERR_CNT	1	Reset MSGCNTR_ERR_CNT to 0 (this bit automatically clears)	0x0: Do not reset 0x1: Reset

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BITFIELD	BITS	DESCRIPTION	DECODE
RESET_CC_CRC_ERR_CNT	0	Reset CC_CRC_ERR_CNT to 0 (this bit automatically clears)	0x0: Do not reset 0x1: Reset

CC_RTTN_ERR (0x1D26)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RTTN_CRC_INT_OEN	RTTN_CRC_ERR_FLAG	–	–	–	INJECT_RTTN_CRC_ERR
Reset	–	–	0b1	0b0	–	–	–	0b0
Access Type	–	–	Write, Read	Read Clears All	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RTTN_CRC_INT_OEN	5	Retention memory CRC check error status reporting enable bit.	0b0: Reporting disabled 0b1: Reporting enabled
RTTN_CRC_ERR_FLAG	4	Sticky status value for retention memory CRC error.	0x0: Flag not asserted 0x1: Flag asserted
INJECT_RTTN_CRC_ERR	0	Set this bit before going into sleep mode to inject error to rttn crc value. Use for ASIL evaluation purposes. Do not add this register to RTTN map.	0x0: Do not inject errors 0x1: Inject errors

INTR_CRC_0 (0x1D80, 0x1D90)*

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_Y_CRC_ERR_OEN	AUDIO_X_CRC_ERR_OEN	AHDCP_CRC_ERR_OEN	GPIO_CRC_ERR_OEN	SPI_CRC_ERR_OEN	RBB_CC_CRC_ERR_OEN	PT2_CRC_ERR_OEN	PT1_CRC_ERR_OEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_Y_CRC_ERR_OEN	7	Enables reporting of AUDIO Y CRC errors (AUDIO_Y_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
AUDIO_X_CRC_ERR_OEN	6	Enables reporting of AUDIO X CRC errors (AUDIO_X_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
AHDCP_CRC_ERR_OEN	5	Enables reporting of AHDCP CRC errors (AHDCP_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
GPIO_CRC_ERR_OEN	4	Enables reporting of GPIO CRC errors (GPIO_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
SPI_CRC_ERR_OEN	3	Enables reporting of SPI CRC errors (SPI_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RBB_CC_CRC_ERR_OEN	2	Enables reporting of RBB CC CRC errors (RBB_CC_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

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BITFIELD	BITS	DESCRIPTION	DECODE
PT2_CRC_ERR_OEN	1	Enables reporting of PT2 CRC errors (PT2_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PT1_CRC_ERR_OEN	0	Enables reporting of PT1 CRC errors (PT1_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR_CRC_1 (0x1D81, 0x1D91)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_Y_CRC_ERR_FLAG	AUDIO_X_CRC_ERR_FLAG	AHDCP_CRC_ERR_FLAG	GPIO_CRC_ERR_FLAG	SPI_CRC_ERR_FLAG	RBB_CC_CRC_ERR_FLAG	PT2_CRC_ERR_FLAG	PT1_CRC_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_Y_CRC_ERR_FLAG	7	AUDIO Y CRC Error Flag Asserted when AUDIO Y CRC error count > 0. Read AUDIO_Y_CRC_ERR (register CNT7) to clear.	0b0: Flag not asserted 0b1: Flag asserted
AUDIO_X_CRC_ERR_FLAG	6	AUDIO X CRC Error Flag Asserted when AUDIO X CRC error count > 0. Read AUDIO_X_CRC_ERR (register CNT6) to clear.	0b0: Flag not asserted 0b1: Flag asserted
AHDCP_CRC_ERR_FLAG	5	AHDCP CRC Error Flag Asserted when AHDCP CRC error count > 0. Read AHDCP_CRC_ERR (register CNT5) to clear.	0b0: Flag not asserted 0b1: Flag asserted
GPIO_CRC_ERR_FLAG	4	GPIO CRC Error Flag Asserted when GPIO CRC error count > 0. Read GPIO_CRC_ERR (register CNT4) to clear.	0b0: Flag not asserted 0b1: Flag asserted
SPI_CRC_ERR_FLAG	3	SPI CRC Error Flag Asserted when SPI CRC error count > 0. Read SPI_CRC_ERR (register CNT3) to clear.	0b0: Flag not asserted 0b1: Flag asserted
RBB_CC_CRC_ERR_FLAG	2	RBB CC CRC Error Flag Asserted when RBB CC CRC error count > 0. Read RBB_CC_CRC_ERR (register CNT2) to clear.	0b0: Flag not asserted 0b1: Flag asserted
PT2_CRC_ERR_FLAG	1	PT2 CRC Error Flag Asserted when PT2 CRC error count > 0. Read PT2_CRC_ERR (register CNT1) to clear.	0b0: Flag not asserted 0b1: Flag asserted

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BITFIELD	BITS	DESCRIPTION	DECODE
PT1_CRC_ERR_FLAG	0	PT1 CRC Error flag Asserted when PT1 CRC error count > 0. Read PT1_CRC_ERR (register CNT0) to clear.	0b0: Flag not asserted 0b1: Flag asserted

CNT0 (0x1D82, 0x1D92)

BIT	7	6	5	4	3	2	1	0
Field	PT1_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
PT1_CRC_ERR	7:0	Number of PT1 CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

CNT1 (0x1D83, 0x1D93)

BIT	7	6	5	4	3	2	1	0
Field	PT2_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
PT2_CRC_ERR	7:0	Number of PT2 CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

CNT2 (0x1D84, 0x1D94)

BIT	7	6	5	4	3	2	1	0
Field	RBB_CC_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
RBB_CC_CRC_ERR	7:0	Number of RBB CC CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

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CNT3 (0x1D85, 0x1D95)

BIT	7	6	5	4	3	2	1	0
Field	SPI_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
SPI_CRC_ERR	7:0	Number of SPI CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

CNT4 (0x1D86, 0x1D96)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
GPIO_CRC_ERR	7:0	Number of GPIO CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

CNT5 (0x1D87, 0x1D97)

BIT	7	6	5	4	3	2	1	0
Field	AHDCP_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
AHDCP_CRC_ERR	7:0	Number of AHDCP CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

CNT6 (0x1D88, 0x1D98)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_X_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
AUDIO_X_CRC_ERR	7:0	Number of AUDIO X CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

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CNT7 (0x1D89, 0x1D99)

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_Y_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
AUDIO_Y_CRC_ERR	7:0	Number of AUDIO Y CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

CNT8 (0x1D8A, 0x1D9A)

BIT	7	6	5	4	3	2	1	0
Field	INFOFR_CRC_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
INFOFR_CRC_ERR	7:0	Number of InfoFrame CRC errors detected at link stream Reset after each read operation or with the rising edge of LOCK.

INTR_CRC_2 (0x1D8B, 0x1D9B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	INFOFR_CRC_ERR_OEN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
INFOFR_CRC_ERR_OEN	0	Enables reporting of InfoFrame CRC errors (INFOFR_CRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR_CRC_3 (0x1D8C, 0x1D9C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	INFOFR_CRC_ERR_FLAG
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

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BITFIELD	BITS	DESCRIPTION	DECODE
INFOFR_CRC_ERR_FLAG	0	InfoFrame CRC Error flag Asserted when INFOFR CRC error count > 0. Read INFOFR_CRC_ERR (register CNT8) to clear.	0b0: Flag not asserted 0b1: Flag asserted

COEFF_0_0 (0x2000)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_0_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_0_0	7:0	Programmable frame CRC coefficient.

COEFF_0_1 (0x2001)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_0_1[7:0]							
Reset	0x41							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_0_1	7:0	Programmable frame CRC coefficient.

COEFF_0_2 (0x2002)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_0_2[7:0]							
Reset	0x16							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_0_2	7:0	Programmable frame CRC coefficient.

COEFF_0_3 (0x2003)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_0_3[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_0_3	7:0	Programmable frame CRC coefficient.

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COEFF_0_4 (0x2004)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_0_4[7:0]							
Reset	0x41							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_0_4	7:0	Programmable frame CRC coefficient.

COEFF_0_5 (0x2005)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_0_5[7:0]							
Reset	0x16							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_0_5	7:0	Programmable frame CRC coefficient.

COEFF_0_6 (0x2006)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_0_6[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_0_6	7:0	Programmable frame CRC coefficient.

COEFF_1_0 (0x2008)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_1_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_1_0	7:0	Programmable frame CRC coefficient.

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COEFF_1_1 (0x2009)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_1_1[7:0]							
Reset	0xC3							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_1_1	7:0	Programmable frame CRC coefficient.

COEFF_1_2 (0x200A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_1_2[7:0]							
Reset	0x3A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_1_2	7:0	Programmable frame CRC coefficient.

COEFF_1_3 (0x200B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_1_3[7:0]							
Reset	0x03							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_1_3	7:0	Programmable frame CRC coefficient.

COEFF_1_4 (0x200C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_1_4[7:0]							
Reset	0xC3							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_1_4	7:0	Programmable frame CRC coefficient.

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COEFF_1_5 (0x200D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_1_5[7:0]							
Reset	0x3A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_1_5	7:0	Programmable frame CRC coefficient.

COEFF_1_6 (0x200E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_1_6[7:0]							
Reset	0x03							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_1_6	7:0	Programmable frame CRC coefficient.

COEFF_2_0 (0x2010)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_2_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_2_0	7:0	Programmable frame CRC coefficient.

COEFF_2_1 (0x2011)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_2_1[7:0]							
Reset	0xC7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_2_1	7:0	Programmable frame CRC coefficient.

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COEFF_2_2 (0x2012)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_2_2[7:0]							
Reset	0x63							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_2_2	7:0	Programmable frame CRC coefficient.

COEFF_2_3 (0x2013)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_2_3[7:0]							
Reset	0x07							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_2_3	7:0	Programmable frame CRC coefficient.

COEFF_2_4 (0x2014)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_2_4[7:0]							
Reset	0xC7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_2_4	7:0	Programmable frame CRC coefficient.

COEFF_2_5 (0x2015)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_2_5[7:0]							
Reset	0x63							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_2_5	7:0	Programmable frame CRC coefficient.

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COEFF_2_6 (0x2016)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_2_6[7:0]							
Reset	0x07							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_2_6	7:0	Programmable frame CRC coefficient.

COEFF_3_0 (0x2018)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_3_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_3_0	7:0	Programmable frame CRC coefficient.

COEFF_3_1 (0x2019)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_3_1[7:0]							
Reset	0x8E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_3_1	7:0	Programmable frame CRC coefficient.

COEFF_3_2 (0x201A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_3_2[7:0]							
Reset	0xC7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_3_2	7:0	Programmable frame CRC coefficient.

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COEFF_3_3 (0x201B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_3_3[7:0]							
Reset	0x0E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_3_3	7:0	Programmable frame CRC coefficient.

COEFF_3_4 (0x201C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_3_4[7:0]							
Reset	0x8E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_3_4	7:0	Programmable frame CRC coefficient.

COEFF_3_5 (0x201D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_3_5[7:0]							
Reset	0xC7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_3_5	7:0	Programmable frame CRC coefficient.

COEFF_3_6 (0x201E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_3_6[7:0]							
Reset	0x0E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_3_6	7:0	Programmable frame CRC coefficient.

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COEFF_4_0 (0x2020)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_4_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_4_0	7:0	Programmable frame CRC coefficient.

COEFF_4_1 (0x2021)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_4_1[7:0]							
Reset	0x5D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_4_1	7:0	Programmable frame CRC coefficient.

COEFF_4_2 (0x2022)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_4_2[7:0]							
Reset	0x99							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_4_2	7:0	Programmable frame CRC coefficient.

COEFF_4_3 (0x2023)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_4_3[7:0]							
Reset	0x1C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_4_3	7:0	Programmable frame CRC coefficient.

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COEFF_4_4 (0x2024)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_4_4[7:0]							
Reset	0x5D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_4_4	7:0	Programmable frame CRC coefficient.

COEFF_4_5 (0x2025)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_4_5[7:0]							
Reset	0x99							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_4_5	7:0	Programmable frame CRC coefficient.

COEFF_4_6 (0x2026)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_4_6[7:0]							
Reset	0x1C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_4_6	7:0	Programmable frame CRC coefficient.

COEFF_5_0 (0x2028)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_5_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_5_0	7:0	Programmable frame CRC coefficient.

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COEFF_5_1 (0x2029)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_5_1[7:0]							
Reset	0xFB							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_5_1	7:0	Programmable frame CRC coefficient.

COEFF_5_2 (0x202A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_5_2[7:0]							
Reset	0x24							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_5_2	7:0	Programmable frame CRC coefficient.

COEFF_5_3 (0x202B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_5_3[7:0]							
Reset	0x38							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_5_3	7:0	Programmable frame CRC coefficient.

COEFF_5_4 (0x202C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_5_4[7:0]							
Reset	0xFB							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_5_4	7:0	Programmable frame CRC coefficient.

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COEFF_5_5 (0x202D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_5_5[7:0]							
Reset	0x24							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_5_5	7:0	Programmable frame CRC coefficient.

COEFF_5_6 (0x202E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_5_6[7:0]							
Reset	0x38							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_5_6	7:0	Programmable frame CRC coefficient.

COEFF_6_0 (0x2030)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_6_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_6_0	7:0	Programmable frame CRC coefficient.

COEFF_6_1 (0x2031)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_6_1[7:0]							
Reset	0xF6							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_6_1	7:0	Programmable frame CRC coefficient.

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COEFF_6_2 (0x2032)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_6_2[7:0]							
Reset	0x49							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_6_2	7:0	Programmable frame CRC coefficient.

COEFF_6_3 (0x2033)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_6_3[7:0]							
Reset	0x70							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_6_3	7:0	Programmable frame CRC coefficient.

COEFF_6_4 (0x2034)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_6_4[7:0]							
Reset	0xF6							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_6_4	7:0	Programmable frame CRC coefficient.

COEFF_6_5 (0x2035)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_6_5[7:0]							
Reset	0x49							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_6_5	7:0	Programmable frame CRC coefficient.

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COEFF_6_6 (0x2036)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_6_6[7:0]							
Reset	0x70							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_6_6	7:0	Programmable frame CRC coefficient.

COEFF_7_0 (0x2038)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_7_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_7_0	7:0	Programmable frame CRC coefficient.

COEFF_7_1 (0x2039)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_7_1[7:0]							
Reset	0xAD							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_7_1	7:0	Programmable frame CRC coefficient.

COEFF_7_2 (0x203A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_7_2[7:0]							
Reset	0x85							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_7_2	7:0	Programmable frame CRC coefficient.

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COEFF_7_3 (0x203B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_7_3[7:0]							
Reset	0xE1							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_7_3	7:0	Programmable frame CRC coefficient.

COEFF_7_4 (0x203C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_7_4[7:0]							
Reset	0xAD							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_7_4	7:0	Programmable frame CRC coefficient.

COEFF_7_5 (0x203D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_7_5[7:0]							
Reset	0x85							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_7_5	7:0	Programmable frame CRC coefficient.

COEFF_7_6 (0x203E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_7_6[7:0]							
Reset	0xE1							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_7_6	7:0	Programmable frame CRC coefficient.

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COEFF_8_0 (0x2040)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_8_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_8_0	7:0	Programmable frame CRC coefficient.

COEFF_8_1 (0x2041)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_8_1[7:0]							
Reset	0x1B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_8_1	7:0	Programmable frame CRC coefficient.

COEFF_8_2 (0x2042)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_8_2[7:0]							
Reset	0x1D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_8_2	7:0	Programmable frame CRC coefficient.

COEFF_8_3 (0x2043)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_8_3[7:0]							
Reset	0xC2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_8_3	7:0	Programmable frame CRC coefficient.

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COEFF_8_4 (0x2044)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_8_4[7:0]							
Reset	0x1B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_8_4	7:0	Programmable frame CRC coefficient.

COEFF_8_5 (0x2045)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_8_5[7:0]							
Reset	0x1D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_8_5	7:0	Programmable frame CRC coefficient.

COEFF_8_6 (0x2046)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_8_6[7:0]							
Reset	0xC2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_8_6	7:0	Programmable frame CRC coefficient.

COEFF_9_0 (0x2048)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_9_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_9_0	7:0	Programmable frame CRC coefficient.

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COEFF_9_1 (0x2049)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_9_1[7:0]							
Reset	0x36							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_9_1	7:0	Programmable frame CRC coefficient.

COEFF_9_2 (0x204A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_9_2[7:0]							
Reset	0x3A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_9_2	7:0	Programmable frame CRC coefficient.

COEFF_9_3 (0x204B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_9_3[7:0]							
Reset	0x84							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_9_3	7:0	Programmable frame CRC coefficient.

COEFF_9_4 (0x204C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_9_4[7:0]							
Reset	0x36							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_9_4	7:0	Programmable frame CRC coefficient.

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COEFF_9_5 (0x204D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_9_5[7:0]							
Reset	0x3A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_9_5	7:0	Programmable frame CRC coefficient.

COEFF_9_6 (0x204E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_9_6[7:0]							
Reset	0x84							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_9_6	7:0	Programmable frame CRC coefficient.

COEFF_10_0 (0x2050)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_10_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_10_0	7:0	Programmable frame CRC coefficient.

COEFF_10_1 (0x2051)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_10_1[7:0]							
Reset	0x2D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_10_1	7:0	Programmable frame CRC coefficient.

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COEFF_10_2 (0x2052)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_10_2[7:0]							
Reset	0x62							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_10_2	7:0	Programmable frame CRC coefficient.

COEFF_10_3 (0x2053)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_10_3[7:0]							
Reset	0x09							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_10_3	7:0	Programmable frame CRC coefficient.

COEFF_10_4 (0x2054)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_10_4[7:0]							
Reset	0x2D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_10_4	7:0	Programmable frame CRC coefficient.

COEFF_10_5 (0x2055)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_10_5[7:0]							
Reset	0x62							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_10_5	7:0	Programmable frame CRC coefficient.

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COEFF_10_6 (0x2056)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_10_6[7:0]							
Reset	0x09							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_10_6	7:0	Programmable frame CRC coefficient.

COEFF_11_0 (0x2058)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_11_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_11_0	7:0	Programmable frame CRC coefficient.

COEFF_11_1 (0x2059)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_11_1[7:0]							
Reset	0x1B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_11_1	7:0	Programmable frame CRC coefficient.

COEFF_11_2 (0x205A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_11_2[7:0]							
Reset	0xD2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_11_2	7:0	Programmable frame CRC coefficient.

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COEFF_11_3 (0x205B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_11_3[7:0]							
Reset	0x13							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_11_3	7:0	Programmable frame CRC coefficient.

COEFF_11_4 (0x205C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_11_4[7:0]							
Reset	0x1B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_11_4	7:0	Programmable frame CRC coefficient.

COEFF_11_5 (0x205D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_11_5[7:0]							
Reset	0xD2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_11_5	7:0	Programmable frame CRC coefficient.

COEFF_11_6 (0x205E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_11_6[7:0]							
Reset	0x13							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_11_6	7:0	Programmable frame CRC coefficient.

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COEFF_12_0 (0x2060)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_12_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_12_0	7:0	Programmable frame CRC coefficient.

COEFF_12_1 (0x2061)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_12_1[7:0]							
Reset	0x77							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_12_1	7:0	Programmable frame CRC coefficient.

COEFF_12_2 (0x2062)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_12_2[7:0]							
Reset	0xB2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_12_2	7:0	Programmable frame CRC coefficient.

COEFF_12_3 (0x2063)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_12_3[7:0]							
Reset	0x26							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_12_3	7:0	Programmable frame CRC coefficient.

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COEFF_12_4 (0x2064)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_12_4[7:0]							
Reset	0x77							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_12_4	7:0	Programmable frame CRC coefficient.

COEFF_12_5 (0x2065)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_12_5[7:0]							
Reset	0xB2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_12_5	7:0	Programmable frame CRC coefficient.

COEFF_12_6 (0x2066)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_12_6[7:0]							
Reset	0x26							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_12_6	7:0	Programmable frame CRC coefficient.

COEFF_13_0 (0x2068)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_13_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_13_0	7:0	Programmable frame CRC coefficient.

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COEFF_13_1 (0x2069)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_13_1[7:0]							
Reset	0xEE							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_13_1	7:0	Programmable frame CRC coefficient.

COEFF_13_2 (0x206A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_13_2[7:0]							
Reset	0x64							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_13_2	7:0	Programmable frame CRC coefficient.

COEFF_13_3 (0x206B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_13_3[7:0]							
Reset	0x4D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_13_3	7:0	Programmable frame CRC coefficient.

COEFF_13_4 (0x206C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_13_4[7:0]							
Reset	0xEE							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_13_4	7:0	Programmable frame CRC coefficient.

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COEFF_13_5 (0x206D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_13_5[7:0]							
Reset	0x64							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_13_5	7:0	Programmable frame CRC coefficient.

COEFF_13_6 (0x206E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_13_6[7:0]							
Reset	0x4D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_13_6	7:0	Programmable frame CRC coefficient.

COEFF_14_0 (0x2070)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_14_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_14_0	7:0	Programmable frame CRC coefficient.

COEFF_14_1 (0x2071)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_14_1[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_14_1	7:0	Programmable frame CRC coefficient.

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COEFF_14_2 (0x2072)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_14_2[7:0]							
Reset	0xC9							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_14_2	7:0	Programmable frame CRC coefficient.

COEFF_14_3 (0x2073)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_14_3[7:0]							
Reset	0x9A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_14_3	7:0	Programmable frame CRC coefficient.

COEFF_14_4 (0x2074)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_14_4[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_14_4	7:0	Programmable frame CRC coefficient.

COEFF_14_5 (0x2075)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_14_5[7:0]							
Reset	0xC9							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_14_5	7:0	Programmable frame CRC coefficient.

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COEFF_14_6 (0x2076)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_14_6[7:0]							
Reset	0x9A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_14_6	7:0	Programmable frame CRC coefficient.

COEFF_15_0 (0x2078)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_15_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_15_0	7:0	Programmable frame CRC coefficient.

COEFF_15_1 (0x2079)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_15_1[7:0]							
Reset	0xB8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_15_1	7:0	Programmable frame CRC coefficient.

COEFF_15_2 (0x207A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_15_2[7:0]							
Reset	0x93							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_15_2	7:0	Programmable frame CRC coefficient.

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COEFF_15_3 (0x207B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_15_3[7:0]							
Reset	0x35							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_15_3	7:0	Programmable frame CRC coefficient.

COEFF_15_4 (0x207C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_15_4[7:0]							
Reset	0xB8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_15_4	7:0	Programmable frame CRC coefficient.

COEFF_15_5 (0x207D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_15_5[7:0]							
Reset	0x93							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_15_5	7:0	Programmable frame CRC coefficient.

COEFF_15_6 (0x207E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_15_6[7:0]							
Reset	0x35							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_15_6	7:0	Programmable frame CRC coefficient.

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COEFF_16_0 (0x2080)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_16_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_16_0	7:0	Programmable frame CRC coefficient.

COEFF_16_1 (0x2081)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_16_1[7:0]							
Reset	0x31							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_16_1	7:0	Programmable frame CRC coefficient.

COEFF_16_2 (0x2082)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_16_2[7:0]							
Reset	0x31							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_16_2	7:0	Programmable frame CRC coefficient.

COEFF_16_3 (0x2083)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_16_3[7:0]							
Reset	0x6A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_16_3	7:0	Programmable frame CRC coefficient.

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COEFF_16_4 (0x2084)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_16_4[7:0]							
Reset	0x31							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_16_4	7:0	Programmable frame CRC coefficient.

COEFF_16_5 (0x2085)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_16_5[7:0]							
Reset	0x31							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_16_5	7:0	Programmable frame CRC coefficient.

COEFF_16_6 (0x2086)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_16_6[7:0]							
Reset	0x6A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_16_6	7:0	Programmable frame CRC coefficient.

COEFF_17_0 (0x2088)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_17_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_17_0	7:0	Programmable frame CRC coefficient.

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COEFF_17_1 (0x2089)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_17_1[7:0]							
Reset	0x62							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_17_1	7:0	Programmable frame CRC coefficient.

COEFF_17_2 (0x208A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_17_2[7:0]							
Reset	0x62							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_17_2	7:0	Programmable frame CRC coefficient.

COEFF_17_3 (0x208B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_17_3[7:0]							
Reset	0xD4							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_17_3	7:0	Programmable frame CRC coefficient.

COEFF_17_4 (0x208C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_17_4[7:0]							
Reset	0x62							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_17_4	7:0	Programmable frame CRC coefficient.

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COEFF_17_5 (0x208D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_17_5[7:0]							
Reset	0x62							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_17_5	7:0	Programmable frame CRC coefficient.

COEFF_17_6 (0x208E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_17_6[7:0]							
Reset	0xD4							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_17_6	7:0	Programmable frame CRC coefficient.

COEFF_18_0 (0x2090)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_18_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_18_0	7:0	Programmable frame CRC coefficient.

COEFF_18_1 (0x2091)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_18_1[7:0]							
Reset	0xC4							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_18_1	7:0	Programmable frame CRC coefficient.

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COEFF_18_2 (0x2092)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_18_2[7:0]							
Reset	0xC4							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_18_2	7:0	Programmable frame CRC coefficient.

COEFF_18_3 (0x2093)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_18_3[7:0]							
Reset	0xA8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_18_3	7:0	Programmable frame CRC coefficient.

COEFF_18_4 (0x2094)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_18_4[7:0]							
Reset	0xC4							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_18_4	7:0	Programmable frame CRC coefficient.

COEFF_18_5 (0x2095)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_18_5[7:0]							
Reset	0xC4							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_18_5	7:0	Programmable frame CRC coefficient.

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COEFF_18_6 (0x2096)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_18_6[7:0]							
Reset	0xA8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_18_6	7:0	Programmable frame CRC coefficient.

COEFF_19_0 (0x2098)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_19_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_19_0	7:0	Programmable frame CRC coefficient.

COEFF_19_1 (0x2099)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_19_1[7:0]							
Reset	0x88							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_19_1	7:0	Programmable frame CRC coefficient.

COEFF_19_2 (0x209A)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_19_2[7:0]							
Reset	0x89							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_19_2	7:0	Programmable frame CRC coefficient.

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COEFF_19_3 (0x209B)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_19_3[7:0]							
Reset	0x51							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_19_3	7:0	Programmable frame CRC coefficient.

COEFF_19_4 (0x209C)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_19_4[7:0]							
Reset	0x88							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_19_4	7:0	Programmable frame CRC coefficient.

COEFF_19_5 (0x209D)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_19_5[7:0]							
Reset	0x89							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_19_5	7:0	Programmable frame CRC coefficient.

COEFF_19_6 (0x209E)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_19_6[7:0]							
Reset	0x51							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_19_6	7:0	Programmable frame CRC coefficient.

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COEFF_20_0 (0x20A0)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_20_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_20_0	7:0	Programmable frame CRC coefficient.

COEFF_20_1 (0x20A1)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_20_1[7:0]							
Reset	0x10							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_20_1	7:0	Programmable frame CRC coefficient.

COEFF_20_2 (0x20A2)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_20_2[7:0]							
Reset	0x13							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_20_2	7:0	Programmable frame CRC coefficient.

COEFF_20_3 (0x20A3)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_20_3[7:0]							
Reset	0xA3							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_20_3	7:0	Programmable frame CRC coefficient.

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COEFF_20_4 (0x20A4)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_20_4[7:0]							
Reset	0x10							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_20_4	7:0	Programmable frame CRC coefficient.

COEFF_20_5 (0x20A5)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_20_5[7:0]							
Reset	0x13							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_20_5	7:0	Programmable frame CRC coefficient.

COEFF_20_6 (0x20A6)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_20_6[7:0]							
Reset	0xA3							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_20_6	7:0	Programmable frame CRC coefficient.

COEFF_21_0 (0x20A8)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_21_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_21_0	7:0	Programmable frame CRC coefficient.

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COEFF_21_1 (0x20A9)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_21_1[7:0]							
Reset	0x20							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_21_1	7:0	Programmable frame CRC coefficient.

COEFF_21_2 (0x20AA)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_21_2[7:0]							
Reset	0x26							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_21_2	7:0	Programmable frame CRC coefficient.

COEFF_21_3 (0x20AB)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_21_3[7:0]							
Reset	0x46							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_21_3	7:0	Programmable frame CRC coefficient.

COEFF_21_4 (0x20AC)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_21_4[7:0]							
Reset	0x20							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_21_4	7:0	Programmable frame CRC coefficient.

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COEFF_21_5 (0x20AD)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_21_5[7:0]							
Reset	0x26							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_21_5	7:0	Programmable frame CRC coefficient.

COEFF_21_6 (0x20AE)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_21_6[7:0]							
Reset	0x46							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_21_6	7:0	Programmable frame CRC coefficient.

COEFF_22_0 (0x20B0)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_22_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_22_0	7:0	Programmable frame CRC coefficient.

COEFF_22_1 (0x20B1)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_22_1[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_22_1	7:0	Programmable frame CRC coefficient.

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COEFF_22_2 (0x20B2)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_22_2[7:0]							
Reset	0x5A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_22_2	7:0	Programmable frame CRC coefficient.

COEFF_22_3 (0x20B3)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_22_3[7:0]							
Reset	0x8D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_22_3	7:0	Programmable frame CRC coefficient.

COEFF_22_4 (0x20B4)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_22_4[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_22_4	7:0	Programmable frame CRC coefficient.

COEFF_22_5 (0x20B5)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_22_5[7:0]							
Reset	0x5A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_22_5	7:0	Programmable frame CRC coefficient.

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COEFF_22_6 (0x20B6)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_22_6[7:0]							
Reset	0x8D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_22_6	7:0	Programmable frame CRC coefficient.

COEFF_23_0 (0x20B8)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_23_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_23_0	7:0	Programmable frame CRC coefficient.

COEFF_23_1 (0x20B9)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_23_1[7:0]							
Reset	0x43							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_23_1	7:0	Programmable frame CRC coefficient.

COEFF_23_2 (0x20BA)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_23_2[7:0]							
Reset	0xA2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_23_2	7:0	Programmable frame CRC coefficient.

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COEFF_23_3 (0x20BB)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_23_3[7:0]							
Reset	0x1B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_23_3	7:0	Programmable frame CRC coefficient.

COEFF_23_4 (0x20BC)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_23_4[7:0]							
Reset	0x43							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_23_4	7:0	Programmable frame CRC coefficient.

COEFF_23_5 (0x20BD)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_23_5[7:0]							
Reset	0xA2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_23_5	7:0	Programmable frame CRC coefficient.

COEFF_23_6 (0x20BE)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_23_6[7:0]							
Reset	0x1B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_23_6	7:0	Programmable frame CRC coefficient.

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COEFF_24_0 (0x20C0)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_24_0[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_24_0	7:0	Programmable frame CRC coefficient.

COEFF_24_1 (0x20C1)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_24_1[7:0]							
Reset	0x86							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_24_1	7:0	Programmable frame CRC coefficient.

COEFF_24_2 (0x20C2)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_24_2[7:0]							
Reset	0x44							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_24_2	7:0	Programmable frame CRC coefficient.

COEFF_24_3 (0x20C3)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_24_3[7:0]							
Reset	0x37							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_24_3	7:0	Programmable frame CRC coefficient.

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COEFF_24_4 (0x20C4)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_24_4[7:0]							
Reset	0x86							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_24_4	7:0	Programmable frame CRC coefficient.

COEFF_24_5 (0x20C5)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_24_5[7:0]							
Reset	0x44							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_24_5	7:0	Programmable frame CRC coefficient.

COEFF_24_6 (0x20C6)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_24_6[7:0]							
Reset	0x37							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_24_6	7:0	Programmable frame CRC coefficient.

COEFF_25_0 (0x20C8)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_25_0[7:0]							
Reset	0x02							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_25_0	7:0	Programmable frame CRC coefficient.

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COEFF_25_1 (0x20C9)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_25_1[7:0]							
Reset	0x0C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_25_1	7:0	Programmable frame CRC coefficient.

COEFF_25_2 (0x20CA)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_25_2[7:0]							
Reset	0x89							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_25_2	7:0	Programmable frame CRC coefficient.

COEFF_25_3 (0x20CB)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_25_3[7:0]							
Reset	0x6E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_25_3	7:0	Programmable frame CRC coefficient.

COEFF_25_4 (0x20CC)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_25_4[7:0]							
Reset	0x0C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_25_4	7:0	Programmable frame CRC coefficient.

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COEFF_25_5 (0x20CD)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_25_5[7:0]							
Reset	0x89							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_25_5	7:0	Programmable frame CRC coefficient.

COEFF_25_6 (0x20CE)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_25_6[7:0]							
Reset	0x6E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_25_6	7:0	Programmable frame CRC coefficient.

COEFF_26_0 (0x20D0)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_26_0[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_26_0	7:0	Programmable frame CRC coefficient.

COEFF_26_1 (0x20D1)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_26_1[7:0]							
Reset	0x59							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_26_1	7:0	Programmable frame CRC coefficient.

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COEFF_26_2 (0x20D2)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_26_2[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_26_2	7:0	Programmable frame CRC coefficient.

COEFF_26_3 (0x20D3)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_26_3[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_26_3	7:0	Programmable frame CRC coefficient.

COEFF_26_4 (0x20D4)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_26_4[7:0]							
Reset	0x59							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_26_4	7:0	Programmable frame CRC coefficient.

COEFF_26_5 (0x20D5)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_26_5[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_26_5	7:0	Programmable frame CRC coefficient.

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COEFF_26_6 (0x20D6)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_26_6[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_26_6	7:0	Programmable frame CRC coefficient.

COEFF_27_0 (0x20D8)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_27_0[7:0]							
Reset	0x08							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_27_0	7:0	Programmable frame CRC coefficient.

COEFF_27_1 (0x20D9)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_27_1[7:0]							
Reset	0xB2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_27_1	7:0	Programmable frame CRC coefficient.

COEFF_27_2 (0x20DA)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_27_2[7:0]							
Reset	0x08							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_27_2	7:0	Programmable frame CRC coefficient.

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COEFF_27_3 (0x20DB)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_27_3[7:0]							
Reset	0xB8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_27_3	7:0	Programmable frame CRC coefficient.

COEFF_27_4 (0x20DC)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_27_4[7:0]							
Reset	0xB2							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_27_4	7:0	Programmable frame CRC coefficient.

COEFF_27_5 (0x20DD)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_27_5[7:0]							
Reset	0x08							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_27_5	7:0	Programmable frame CRC coefficient.

COEFF_27_6 (0x20DE)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_27_6[7:0]							
Reset	0xB8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_27_6	7:0	Programmable frame CRC coefficient.

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COEFF_28_0 (0x20E0)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_28_0[7:0]							
Reset	0x10							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_28_0	7:0	Programmable frame CRC coefficient.

COEFF_28_1 (0x20E1)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_28_1[7:0]							
Reset	0x64							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_28_1	7:0	Programmable frame CRC coefficient.

COEFF_28_2 (0x20E2)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_28_2[7:0]							
Reset	0x11							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_28_2	7:0	Programmable frame CRC coefficient.

COEFF_28_3 (0x20E3)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_28_3[7:0]							
Reset	0x70							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_28_3	7:0	Programmable frame CRC coefficient.

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COEFF_28_4 (0x20E4)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_28_4[7:0]							
Reset	0x64							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_28_4	7:0	Programmable frame CRC coefficient.

COEFF_28_5 (0x20E5)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_28_5[7:0]							
Reset	0x11							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_28_5	7:0	Programmable frame CRC coefficient.

COEFF_28_6 (0x20E6)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_28_6[7:0]							
Reset	0x70							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_28_6	7:0	Programmable frame CRC coefficient.

COEFF_29_0 (0x20E8)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_29_0[7:0]							
Reset	0x20							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_29_0	7:0	Programmable frame CRC coefficient.

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COEFF_29_1 (0x20E9)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_29_1[7:0]							
Reset	0xC8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_29_1	7:0	Programmable frame CRC coefficient.

COEFF_29_2 (0x20EA)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_29_2[7:0]							
Reset	0x22							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_29_2	7:0	Programmable frame CRC coefficient.

COEFF_29_3 (0x20EB)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_29_3[7:0]							
Reset	0xE0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_29_3	7:0	Programmable frame CRC coefficient.

COEFF_29_4 (0x20EC)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_29_4[7:0]							
Reset	0xC8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_29_4	7:0	Programmable frame CRC coefficient.

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COEFF_29_5 (0x20ED)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_29_5[7:0]							
Reset	0x22							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_29_5	7:0	Programmable frame CRC coefficient.

COEFF_29_6 (0x20EE)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_29_6[7:0]							
Reset	0xE0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_29_6	7:0	Programmable frame CRC coefficient.

COEFF_30_0 (0x20F0)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_30_0[7:0]							
Reset	0x40							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_30_0	7:0	Programmable frame CRC coefficient.

COEFF_30_1 (0x20F1)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_30_1[7:0]							
Reset	0x90							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_30_1	7:0	Programmable frame CRC coefficient.

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COEFF_30_2 (0x20F2)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_30_2[7:0]							
Reset	0x45							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_30_2	7:0	Programmable frame CRC coefficient.

COEFF_30_3 (0x20F3)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_30_3[7:0]							
Reset	0xC0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_30_3	7:0	Programmable frame CRC coefficient.

COEFF_30_4 (0x20F4)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_30_4[7:0]							
Reset	0x90							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_30_4	7:0	Programmable frame CRC coefficient.

COEFF_30_5 (0x20F5)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_30_5[7:0]							
Reset	0x45							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_30_5	7:0	Programmable frame CRC coefficient.

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COEFF_30_6 (0x20F6)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_30_6[7:0]							
Reset	0xC0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_30_6	7:0	Programmable frame CRC coefficient.

COEFF_31_0 (0x20F8)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_31_0[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_31_0	7:0	Programmable frame CRC coefficient.

COEFF_31_1 (0x20F9)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_31_1[7:0]							
Reset	0x20							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_31_1	7:0	Programmable frame CRC coefficient.

COEFF_31_2 (0x20FA)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_31_2[7:0]							
Reset	0x8B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_31_2	7:0	Programmable frame CRC coefficient.

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COEFF_31_3 (0x20FB)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_31_3[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_31_3	7:0	Programmable frame CRC coefficient.

COEFF_31_4 (0x20FC)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_31_4[7:0]							
Reset	0x20							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_31_4	7:0	Programmable frame CRC coefficient.

COEFF_31_5 (0x20FD)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_31_5[7:0]							
Reset	0x8B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_31_5	7:0	Programmable frame CRC coefficient.

COEFF_31_6 (0x20FE)

BIT	7	6	5	4	3	2	1	0
Field	COEFF_31_6[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COEFF_31_6	7:0	Programmable frame CRC coefficient.

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PROG_CRC_1 (0x20FF)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_EN_Y	PROG_CRC_EN_X	–	–	–	–	–	–
Reset	0x0	0x0	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PROG_CRC_EN_Y	7	Enables-disables programmable frame CRC of video Pipe Y.	0x0: Disable programmable frame CRC. 0x1: Enable programmable frame CRC.
PROG_CRC_EN_X	6	Enables-disables programmable frame CRC of video Pipe X.	0x0: Disable programmable frame CRC. 0x1: Enable programmable frame CRC.

PROG_CRC_2 (0x2100)

BIT	7	6	5	4	3	2	1	0
Field	FRAME_CNT_Y[3:0]				FRAME_CNT_X[3:0]			
Reset								
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
FRAME_CNT_Y	7:4	4 bit frame counter value which increments at every new frame
FRAME_CNT_X	3:0	4 bit frame counter value which increments at every new frame

PROG_CRC_3 (0x2101)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_VAL_X0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROG_CRC_VAL_X0	7:0	Frame CRC value [7:0] of programmable CRC

PROG_CRC_4 (0x2102)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_VAL_X1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROG_CRC_VAL_X1	7:0	Frame CRC value [15:8] of programmable CRC

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PROG_CRC_5 (0x2103)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_VAL_X2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROG_CRC_VAL_X2	7:0	Frame CRC value [23:16] of programmable CRC

PROG_CRC_6 (0x2104)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_VAL_X3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROG_CRC_VAL_X3	7:0	Frame CRC value [31:24] of programmable CRC

PROG_CRC_7 (0x2105)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_VAL_Y0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROG_CRC_VAL_Y0	7:0	Frame CRC value [7:0] of programmable CRC

PROG_CRC_8 (0x2106)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_VAL_Y1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROG_CRC_VAL_Y1	7:0	Frame CRC value [15:8] of programmable CRC

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PROG_CRC_9 (0x2107)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_VAL_Y2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROG_CRC_VAL_Y2	7:0	Frame CRC value [23:16] of programmable CRC

PROG_CRC_10 (0x2108)

BIT	7	6	5	4	3	2	1	0
Field	PROG_CRC_VAL_Y3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROG_CRC_VAL_Y3	7:0	Frame CRC value [31:24] of programmable CRC

VCRC_CHK_REG1 (0x2280, 0x2290)*

BIT	7	6	5	4	3	2	1	0
Field	FCRC_CHECK_EN	EN_VOTING_FOR_FCRC	EN_VOTING_FOR_FCNT	USE_FCRC_VALID	FCRC_CHECK_SEL	SPRS_LAST_DE	–	–
Reset	0x0	0x1	0x1	0x0	0x0	0x1	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
FCRC_CHECK_EN	7	Video Frame CRC check enable	0x0: Frame CRC check is disabled 0x1: Frame CRC check is enabled
EN_VOTING_FOR_FCRC	6	Enable voting for frame CRC	0x0: Voting for FCRC is disabled. 0x1: Voting for FCRC is enabled.
EN_VOTING_FOR_FCNT	5	Enable voting for frame count	0x0: Voting for FCNT is disabled. 0x1: Voting for FCNT is enabled.
USE_FCRC_VALID	4	Use frame crc valid bit in addional video line to enable/disable fcrc check for corresponding frame	
FCRC_CHECK_SEL	3	Frame CRC check select (programmable CRC / default CRC).	0x0: Use programmable CRC 0x1: Use default CRC
SPRS_LAST_DE	2	Suppress last video line when FCRC_CHECK_EN=1	0x0: Do not suppress last line when FCRC_CHECK_EN=1 0x1: Suppress last line when FCRC_CHECK_EN=1

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VCRC_CHK_REG2 (0x2281, 0x2291)

BIT	7	6	5	4	3	2	1	0
Field	FCRC_CHECK_ERR	VOTE_ERR_FCRC	VOTE_ERR_FCNT	–	–	–	–	–
Reset	0x0	0x0	0x0	–	–	–	–	–
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
FCRC_CHECK_ERR	7	FCRC check error status. Write 1 to clear.
VOTE_ERR_FCRC	6	It shows that voting error occurred in received FCRC, in which all 3 values are different. Write 1 to clear.
VOTE_ERR_FCNT	5	It shows that voting error occurred in received FCNT, in which all 3 values are different. Write 1 to clear.

VCRC_CHK_REG3 (0x2282, 0x2292)

BIT	7	6	5	4	3	2	1	0
Field	FCRC_CHECK_ERR_LAST	–	–	–	–	–	–	–
Reset	0x0	–	–	–	–	–	–	–
Access Type	Read Only	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
FCRC_CHECK_ERR_LAST	7	Error status of last frame CRC check	0x0: No error occurred in last frame CRC check 0x1: Error occurred in last frame CRC check

VCRC_CHK_REG4 (0x2283, 0x2293)

BIT	7	6	5	4	3	2	1	0
Field	FCRC_RCVD_0[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FCRC_RCVD_0	7:0	Received frame CRC [7:0] in last frame.

VCRC_CHK_REG5 (0x2284, 0x2294)

BIT	7	6	5	4	3	2	1	0
Field	FCRC_RCVD_1[7:0]							
Reset								
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
FCRC_RCVD_1	7:0	Received frame CRC [15:8] in last frame.

VCRC_CHK_REG6 (0x2285, 0x2295)

BIT	7	6	5	4	3	2	1	0
Field	FCRC_RCVD_2[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FCRC_RCVD_2	7:0	Received frame CRC [23:16] in last frame.

VCRC_CHK_REG7 (0x2286, 0x2296)

BIT	7	6	5	4	3	2	1	0
Field	FCRC_RCVD_3[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FCRC_RCVD_3	7:0	Received frame CRC [31:24] in last frame.

VCRC_CHK_REG8 (0x2287, 0x2297)

BIT	7	6	5	4	3	2	1	0
Field	FCNT_RCVD_0[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FCNT_RCVD_0	7:0	Received frame count [7:0] in last frame.

VCRC_CHK_REG9 (0x2288, 0x2298)

BIT	7	6	5	4	3	2	1	0
Field	FCNT_RCVD_1[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FCNT_RCVD_1	7:0	Received frame count [15:8] in last frame.

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VCRC_CHK_REG10 (0x2289, 0x2299)

BIT	7	6	5	4	3	2	1	0
Field	FCNT_RCVD_2[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FCNT_RCVD_2	7:0	Received frame count [23:16] in last frame.

VCRC_CHK_REG11 (0x228A, 0x229A)

BIT	7	6	5	4	3	2	1	0
Field	FCNT_RCVD_3[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FCNT_RCVD_3	7:0	Received frame count [31:24] in last frame.

SYS_CNTL_B0 (0x4100)*

BIT	7	6	5	4	3	2	1	0
Field	cmd_reset	clk_en	hdcp2_en	stream_en	sys_int_en[3:0]			
Reset	0b1	0b0	0b1	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_reset	7	Reset control for function when configured as a Source Device, otherwise ignored.	
clk_en	6	Clock gating control for function when configured as a Source Device, otherwise ignored.	
hdcp2_en	5	Enables HDCP2 Video Encryption when configured as a Source Device, otherwise ignored.	
stream_en	4	Enable video stream for HDCP2 operation	
sys_int_en	3:0	Interrupt Enable for ErrB interrupt generation	0bXXX1: Authentication Failed 0bXX1X: Topology Available 0bX1XX: Topology Changed 0b1XXX: Encryption Disabled

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SYS_CNTL_B1 (0x4101)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	video_off	audio_off
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
video_off	1	Disables Video when enabled.
audio_off	0	Disables Audio when enabled.

SYS_CNTL_B2 (0x4102)

BIT	7	6	5	4	3	2	1	0
Field	cipher_fail	–	–	–	sys_int_stat[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Read Only	–	–	–	Read Clears All			

BITFIELD	BITS	DESCRIPTION	DECODE
cipher_fail	7	Error in cipher generation seen	
sys_int_stat	3:0	Interrupt Status for ErrB interrupt generation	0bXXX1: Authentication Failed 0bXX1X: Topology Available 0bX1XX: Topology Changed 0b1XXX: Encryption Disabled

SYS_CNTL_B3 (0x4103)

BIT	7	6	5	4	3	2	1	0
Field	encryption_en	av_masked	tx_stat[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Read Only	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION
encryption_en	7	Audio/Video is being encrypted
av_masked	6	Audio/Video is being masked
tx_stat	5:0	HDCP 2.2 Tx Authentication Status

SYS_COMM_B0 (0x4104)*

BIT	7	6	5	4	3	2	1	0
Field	i2c_slave_ID[6:0]							–
Reset	0b0111010							–
Access Type	Write, Read							–

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BITFIELD	BITS	DESCRIPTION
i2c_slave_ID	7:1	Device address of HDCP2 Rx I2C Slave which receives and outputs video transmitted on pipe X

SYS_COMM_B1 (0x4105)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			ahcc_slv_to[1:0]		i2c_speed[2:0]		
Reset	0b000			0b01		0b010		
Access Type				Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ahcc_slv_to	4:3	AHCC time out setting	0x0: 128us/256us 0x1: 256us/512us 0x2: 512us/1ms 0x3: 1ms/2ms
i2c_speed	2:0	Speed of I2C bus	0x0: Reserved 0x1: 400K 0x2: 1M 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

SYS_COMM_B2 (0x4106)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	hdcp_link_sel	RSVD[1:0]		i2c_slave_order[1:0]	
Reset	–	–	–	0x0	0b10		0b00	
Access Type	–	–	–	Write, Read			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
hdcp_link_sel	4	Set to indicate this HDCP for which GMSL link	0x0: For GMSL Link A 0x1: For GMSL Link B
i2c_slave_order	1:0	Set to indicate DES order in the chain for this video stream	0x0: First 0x1: Second 0x2: Third 0x3: Fourth

SYS_STAT_B0 (0x4108)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	encryption_en_all[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
encryption_en_all	3:0	Encrypting video, each bit corresponds to one video stream

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RX_ID_0 (0x410A)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_0	7:0	HDCP2.3 Receiver's ID, byte 0

RX_ID_1 (0x410B)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_1	7:0	HDCP2.3 Receiver's ID, byte 1

RX_ID_2 (0x410D)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_2	7:0	HDCP2.3 Receiver's ID, byte 2

RX_ID_3 (0x410E)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_3	7:0	HDCP2.3 Receiver's ID, byte 3

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RX_ID_4 (0x410F)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_4	7:0	HDCP2.3 Receiver's ID, byte 4

SYS_CNTL_B0 (0x4110)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	hdcp2_en	stream_en	sys_int_en[3:0]			
Reset	0b1	0b0	0b1	0b0	0x0			
Access Type			Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
hdcp2_en	5	Enables HDCP2 Video Encryption when configured as a Source Device, otherwise ignored.	
stream_en	4	Enable video stream for HDCP2.2 operation	
sys_int_en	3:0	Interrupt Enable for ErrB interrupt generation	0bXXX1: Authentication Failed 0bXX1X: Topology Available 0bX1XX: Topology Changed 0b1XXX: Encryption Disabled

SYS_CNTL_B1 (0x4111)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	video_off	audio_off
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
video_off	1	Disables Video when enabled.
audio_off	0	Disables Audio when enabled.

SYS_CNTL_B2 (0x4112)

BIT	7	6	5	4	3	2	1	0
Field	cipher_fail	–	–	–	sys_int_stat[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Read Only	–	–	–	Read Clears All			

BITFIELD	BITS	DESCRIPTION	DECODE
cipher_fail	7	Error in cipher generation seen	

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BITFIELD	BITS	DESCRIPTION	DECODE
sys_int_stat	3:0	Interrupt Status for ErrB interrupt generation	0bXXX1: Authentication Failed 0bXX1X: Topology Available 0bX1XX: Topology Changed 0b1XXX: Encryption Disabled

SYS_CNTL_B3 (0x4113)

BIT	7	6	5	4	3	2	1	0
Field	encryption_en	av_masked	tx_stat[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Read Only	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION
encryption_en	7	Audio/Video is being encrypted
av_masked	6	Audio/Video is being masked
tx_stat	5:0	HDCP 2.2 Tx Authentication Status

SYS_COMM_B0 (0x4114)*

BIT	7	6	5	4	3	2	1	0
Field	i2c_slave_ID[6:0]							–
Reset	0b0111001							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
i2c_slave_ID	7:1	Device address of HDCP2.2 Rx I2C Slave which receives and outputs video transmitted on pipe Y

SYS_COMM_B1 (0x4115)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD[2:0]		
Reset	–	–	–	–	–	0b010		
Access Type	–	–	–	–	–			

SYS_COMM_B2 (0x4116)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	hdcp_link_sel	–	–	i2c_slave_order[1:0]	
Reset	–	–	–	0x1	–	–	0b00	
Access Type	–	–	–	Write, Read	–	–	Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
hdcp_link_sel	4	Set to indicate this HDCP for which GMSL link	0x0: For GMSL Link A 0x1: For GMSL Link B
i2c_slave_order	1:0	Set to indicate DES order in the chain for this video stream	0x0: First 0x1: Second 0x2: Third 0x3: Fourth

RX_ID_0 (0x411A)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_0	7:0	HDCP2.3 Receiver's ID, byte 0

RX_ID_1 (0x411B)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_1	7:0	HDCP2.3 Receiver's ID, byte 1

RX_ID_2 (0x411D)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_2	7:0	HDCP2.3 Receiver's ID, byte 2

RX_ID_3 (0x411E)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_3	7:0	HDCP2.3 Receiver's ID, byte 3

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RX_ID_4 (0x411F)

BIT	7	6	5	4	3	2	1	0
Field	hdcp2_rxid_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
hdcp2_rxid_4	7:0	HDCP2.3 Receiver's ID, byte 4

SYS_IPC_OUTBOX_B0 (0x41A0)

BIT	7	6	5	4	3	2	1	0
Field	ipc_outbox[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ipc_outbox	7:0	PicoMax Readable Mailbox. Interrupt issued to PicoMax when updated. Content format and interpretation is user-defined.

SYS_IPC_OUTBOX_B1 (0x41A1)

BIT	7	6	5	4	3	2	1	0
Field	ipc_outbox[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ipc_outbox	7:0	PicoMax Readable Mailbox. Interrupt issued to PicoMax when updated. Content format and interpretation is user-defined.

SYS_IPC_OUTBOX_B2 (0x41A2)

BIT	7	6	5	4	3	2	1	0
Field	ipc_outbox[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ipc_outbox	7:0	PicoMax Readable Mailbox. Interrupt issued to PicoMax when updated. Content format and interpretation is user-defined.

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SYS_IPC_OUTBOX_B3 (0x41A3)

BIT	7	6	5	4	3	2	1	0
Field	ipc_outbox[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ipc_outbox	7:0	PicoMax Readable Mailbox. Interrupt issued to PicoMax when updated. Content format and interpretation is user-defined.

SYS_IPC_INBOX_B0 (0x41A4)

BIT	7	6	5	4	3	2	1	0
Field	ipc_inbox[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ipc_inbox	7:0	PicoMax Mailbox that issues Host interrupt when updated. Content interpretation is user-defined.

SYS_IPC_INBOX_B1 (0x41A5)

BIT	7	6	5	4	3	2	1	0
Field	ipc_inbox[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ipc_inbox	7:0	PicoMax Mailbox that issues Host interrupt when updated. Content interpretation is user-defined.

SYS_IPC_INBOX_B2 (0x41A6)

BIT	7	6	5	4	3	2	1	0
Field	ipc_inbox[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ipc_inbox	7:0	PicoMax Mailbox that issues Host interrupt when updated. Content interpretation is user-defined.

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SYS_IPC_INBOX_B3 (0x41A7)

BIT	7	6	5	4	3	2	1	0
Field	ipc_inbox[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ipc_inbox	7:0	PicoMax Mailbox that issues Host interrupt when updated. Content interpretation is user-defined.

SYS_IPC_IS_B0 (0x41A8)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ipc_inbox_int_stat
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION
ipc_inbox_int_stat	0	Interrupt indicating IPC Inbox contents have changed.

SYS_IPC_IE_B0 (0x41AC)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ipc_inbox_int_en
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
ipc_inbox_int_en	0	Interrupt enable for associated status bit.

SGMII_0 (0x5000)*

BIT	7	6	5	4	3	2	1	0
Field	RESET_SGMII_IP	RSVD	SGMII_RX_PIN_SWAP	RSVD	SGMII_MDIO_EN	SGMII_TXCLK_EN	SGMII_EXT_RXCLK_EN	SGMII_EN
Reset	0x0	0x0	0x0	0x1	0x0	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_SGMII_IP	7	Used to reset SGMII IP. This is 0 by default, to be able to access IP registers.	0x0: SGMII IP is not reset 0x1: SGMII IP is reset
SGMII_RX_PIN_SWAP	5	SGMII RX pin swap	0x0: SGMII RX pins are not swapped 0x1: SGMII RX pins are swapped

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BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_MDIO_EN	3	SGMII MDIO enable	0x0: SGMII MDIO is disabled 0x1: SGMII MDIO is enabled
SGMII_TXCLK_EN	2	SGMII TX clock enable	0x0: SGMII TX clock is disabled 0x1: SGMII TX clock is enabled
SGMII_EXT_RXCLK_EN	1	SGMII external rx clock enable	0x0: External rx clock is disabled 0x1: External rx clock is enabled
SGMII_EN	0	SGMII enable	0x0: SGMII is disabled. 0x1: SGMII is enabled.

SGMII_5 (0x5005)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SGMII_STOP_ERR	DPLLLOCK_SNAP_ON_SGMII_STOP	WBLOCK_SNAP_ON_SGMII_STOP	–	–	–	–
Reset	0x0	0x0	0x0	0x0	–	–	–	–
Access Type		Write 1 to Clear, Read	Read Only	Read Only	–	–	–	–

BITFIELD	BITS	DESCRIPTION
SGMII_STOP_ERR	6	SGMII Stop error status. Drives ERRB pin when SGMII_STOP_ERR_OEN=1. It is cleared when 1 is written.
DPLLLOCK_SNAP_ON_SGMII_STOP	5	SGMII DPLL lock value when SGMII stops.
WBLOCK_SNAP_ON_SGMII_STOP	4	SGMII Wblock value when SGMII stops.

SGMII_21 (0x5015)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SGMII_PRBS_CHECK_STATUS	SGMII_DEC_ERR_FLAG	SGMII_PRBS_ERR_FLAG	SGMII_INT
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_PRBS_CHECK_STATUS	3	SGMII PRBS Checker synhronization status.	0x0: SGMII PRBS Checker is not synchronized. 0x1: SGMII PRBS Checker is synchronized.
SGMII_DEC_ERR_FLAG	2	SGMII Decoding error status. Drives ERRB pin when SGMII_DEC_ERR_OEN=1.	
SGMII_PRBS_ERR_FLAG	1	SGMII PRBS error status. Drives ERRB pin when SGMII_PRBS_ERR_OEN=1.	
SGMII_INT	0	Interrupt status of SGMII IP. Drives ERRB pin when SGMII_INT_OEN=1.	

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SGMII_22 (0x5016)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	SGMII_XPCS_LINK_STATUS	RSVD	RSVD	ACT_DET_DATA	ACT_DET_CLK
Reset	–	–	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	–	Read Only			Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SGMII_XPCS_LINK_STATUS	4	Link status register of SGMII IP.	0x0: Link Down 0x1: Link Up
ACT_DET_DATA	1	Status register for SGMII data activity detector.	0x0: Activity is not detected in SGMII rx data 0x1: Activity is detected in SGMII rx data
ACT_DET_CLK	0	Status register for SGMII clock activity detector.	0x0: Activity is not detected in SGMII rx clock 0x1: Activity is detected in SGMII rx clock

SGMII_32 (0x5026)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x0							
Access Type								

SGMII_33 (0x5027)

BIT	7	6	5	4	3	2	1	0
Field	SGMII_DEC_ERR_CNT[7:0]							
Reset	0x0							
Access Type	Write Clears All, Read							

BITFIELD	BITS	DESCRIPTION
SGMII_DEC_ERR_CNT	7:0	SGMII decoding error counter. Write to clear.

DPRX_TRN_STATUS0 (0x6418)

Provide status of DP Rx core link training operations.

BIT	7	6	5	4	3	2	1	0
Field	DPRX_LINK_RATE[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION	DECODE
DPRX_LINK_RATE	7:0	DP link rate that is set in the link bandwidth DPCD register (0x0100).	06: 1.62 Gbps 0A: 2.7 Gbps 14: 5.4 Gbps 1E: 8.1 Gbps XX: All other values reserved

DPRX_TRN_STATUS1 (0x6419)

Provide status of DP Rx core link training operations.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DPRX_LANE_CNT[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
DPRX_LANE_CNT	4:0	DP lane count that is set in the lane count DPCD register (0x0101).	01: Lane 0 active 02: Lanes 0, 1 active 04: Lanes 0,1,2,3 active XX: All other values reserved

DPRX_TRN_STATUS2 (0x641A)

Provide status of DP Rx core link training operations.

BIT	7	6	5	4	3	2	1	0
Field	DPRX_TRAIN_STATE[3:0]				–	DPRX_TRAIN_PAT[2:0]		
Reset	0x0				–	0b000		
Access Type	Read Only				–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
DPRX_TRAIN_STATE	7:4	DP Rx core training state. Each bit represents the competion of a training phase for all acitve lanes (active lane status ANDed together).	4: Clock recovery done 5: Channel equalization done 6: Symbol lock 7: Lane alignment
DPRX_TRAIN_PAT	2:0	DP training pattern that is set in the link training pattern DPCD register (0x102).	000: No training (normal data) 001: Training pattern 1 010: Training pattern 2 011: Training pattern 3 111: Training pattern 4 xxx: All other values reserved

DPRX_TRN_STATUS3 (0x641B)

Provide status of DP Rx core link training operations.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SYM_LOCK_COMB	LQP_TRN_NOCLR	TPS4_DESCRAM_ON
Reset	–	–	–	–	–	0b1	0b0	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
SYM_LOCK_COMB	2	Combines all active lanes for symbol lock detection (AND). This is normal operation. Individual (not combined) symbol lock detection is used for link quality compliance testing.	0: No combining of active lane symbol lock 1: Combined active lane symbol lock
LQP_TRN_NOCLR	1	Disables clearing of link quality error counters (SER count) when training status changes. Reading the error counters will continue to clear them.	0: Error counters cleared both by reading and training status change 1: Error counters only cleared by reading
TPS4_DESCRAM_ON	0	Automatically enables descrambling when training pattern 4 (TPS4) is set. Normally, descrambling is set independently of the training pattern setting.	0: Descrambling set independent of training pattern 1: Descrambling automatically set when TPS4 set

DPRX_VID_STATUS0 (0x641C)

Provide status of DP Rx core video streams.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VBID_DSC_0	VBID_AUD_MUTE_0	VBID_NOVID_0	VBID_VBLANK_0	MODE_UPD_0
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBID_DSC_0	4	DSC compressed stream flag (VBID bit 6) for stream 0. This indicates if the video stream is DSC compressed.	0: Video stream is not DSC compressed 1: Video stream is DSC compressed
VBID_AUD_MUTE_0	3	Audio mute flag (VBID bit 4) for stream 0. This indicates if the audio stream is active.	0: Audio stream is not muted (active) 1: Audio stream is muted
VBID_NOVID_0	2	No video stream flag (VBID bit 3) for stream 0. This indicates if the video stream exists.	0: Video stream does not exist 1: Video stream exists
VBID_VBLANK_0	1	Vertical blanking flag (VBID bit 0) for stream 0. This indicates if video blanking is active. This occurs during the vertical blank period of an active video stream or if there is no active video stream.	0: Vertical blank not active 1: Vertical blank active
MODE_UPD_0	0	Video mode update status for stream 0. This sticky status indicates that MSA parameters have been updated. Write 1 to clear the status allowing it to be set on the next update.	0: Awaiting MSA parameter update 1: MSA parameters updated

DPRX_VID_STATUS1 (0x641D)

Provide status of DP Rx core video streams.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VBID_DSC_1	VBID_AUD_MUTE_1	VBID_NOVID_1	VBID_VBLANK_1	MODE_UPD_1
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VBID_DSC_1	4	DSC compressed stream flag (VBID bit 6) for stream 1. This indicates if the video stream is DSC compressed.	0: Video stream is not DSC compressed 1: Video stream is DSC compressed
VBID_AUD_MUTE_1	3	Audio mute flag (VBID bit 4) for stream 1. This indicates if the audio stream is active.	0: Audio stream is not muted (active) 1: Audio stream is muted
VBID_NOVID_1	2	No video stream flag (VBID bit 3) for stream 1. This indicates if the video stream exists.	0: Video stream does not exist 1: Video stream exists
VBID_VBLANK_1	1	Vertical blanking flag (VBID bit 0) for stream 1. This indicates if video blanking is active. This occurs during the vertical blank period of an active video stream or if there is no active video stream.	0: Vertical blank not active 1: Vertical blank active
MODE_UPD_1	0	Video mode update status for stream 1. This sticky status indicates that MSA parameters have been updated. Write 1 to clear the status allowing it to be set on the next update.	0: Awaiting MSA parameter update 1: MSA parameters updated

EDP_VIDEO_CTRL0 (0x6420)*

Provides control of video out of EDP Rx.

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	–	–	VIDEO_OUT_EN[1:0]	
Reset	0b0	0b0	0b0	0b0	–	–	0x0	
Access Type					–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_OUT_EN	1:0	Enables video out for each of the four possible video streams. Each bit controls a corresponding video stream. Bit 0 → Pipe X Bit 1 → Pipe Y	0: Stream disabled 1: Stream enabled

EDP_VIDEO_CTRL1 (0x6421)*

BIT	7	6	5	4	3	2	1	0
Field	–	DBL_PXL_EN_0	DUP_0	RSVD	–	–	FORCE_PXCLK_RUN[1:0]	
Reset	–	0b0	0b0	0b0	–	–	0x3	
Access Type	–	Write, Read	Write, Read		–	–	Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
DBL_PXL_EN_0	6	Enable odd/even pixel split at DPRX output which allows processing video with pixel clock frequency up to 920MHz. Even pixels drive pipe X, odd pixels drive pipe Y	0x0: Do not split video 0x1: Split video to 2 video pipes
DUP_0	5	Duplicate video recevied on DPRX port 0 to port 1	0x0: Duplication disabled 0x1: Duplication enabled
FORCE_PXCLK_RUN	1:0	Keep pxclk running even when respective VIDEO_OUT_EN bit is 0	

EDP_VIDEO_CTRL2 (0x6422)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				RSVD	EDID_ROM_EN	EDID_RAM_EN	EDID_READ_ONLY
Reset	0x7				0b0	0b1	0b0	0b1
Access Type						Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EDID_ROM_EN	2	Connect EDID ROM to I2C-over-AUX	0x0: Disable EDID ROM See EDID_RAM_EN 0x1: EDID ROM is accessible through DisplayPort I2C-over-AUX using EDID_DEV_ADDR
EDID_RAM_EN	1	Connect EDID memory to I2C-over-AUX (automatically disconnected from I2C-over-AUX when EDID_ROM_EN=1)	0x0: Disable EDID RAM EDID RAM can be accessed through CC using CC EDID address 0x1: If EDID_ROM_EN=0, then EDID RAM memory is accessible through DisplayPort I2C-over-AUX using EDID_DEV_ADDR
EDID_READ_ONLY	0	Make EDID RAM read-only when it is connected to I2C-over-AUX	0x0: EDID is writable 0x1: EDID is read-only

EDP_VIDEO_CTRL3 (0x6423)*

BIT	7	6	5	4	3	2	1	0
Field	EDID_DEV_ADDR[6:0]							–
Reset	0b1010000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION
EDID_DEV_ADDR	7:1	EDID I^{2}C slave address

EDP_VID_CLK_CTRL0 (0x6424)*

BIT	7	6	5	4	3	2	1	0
Field	PCLK_RATE_MOD_1	–	PCLK_RATE_SEL_1[1:0]		PCLK_RATE_MOD_0	–	PCLK_RATE_SEL_0[1:0]	
Reset	0b1	–	0b11		0b1	–	0b11	
Access Type	Write, Read	–	Write, Read		Write, Read	–	Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
PCLK_RATE_MOD_1	7	DP video clock (pclk) rate select mode stream 1. This is a flag to inform the PMX to not set the DP video clock rate automatically. The rate must be set manually and will not be overridden by PMX.	0: Auto - PMX controls rate select 1: Manual - No PMX rate select control
PCLK_RATE_SEL_1	5:4	DP video clock (pclk) rate select stream 1. This sets the maximum pclk rate for the DP video stream. Lower rates reduce power and can improve clock stability.	00: 75 Mhz 01: 150 Mhz 10: 300 Mhz 11: 461 Mhz
PCLK_RATE_MOD_0	3	DP video clock (pclk) rate select mode stream 0. This is a flag to inform the PMX to not set the DP video clock rate automatically. The rate must be set manually and will not be overridden by PMX.	0: Auto - PMX controls rate select 1: Manual - No PMX rate select control
PCLK_RATE_SEL_0	1:0	DP video clock (pclk) rate select stream 0. This sets the maximum pclk rate for the DP video stream. Lower rates reduce power and can improve clock stability.	00: 75 Mhz 01: 150 Mhz 10: 300 Mhz 11: 461 Mhz

EDP_AUDIO_CTRL1 (0x6429)

BIT	7	6	5	4	3	2	1	0
Field	DP_AUD_OUT_EN_0	–	–	RSVD[2:0]			RSVD[1:0]	
Reset	0b0	–	–	0b101			0b01	
Access Type	Write, Read	–	–					

BITFIELD	BITS	DESCRIPTION
DP_AUD_OUT_EN_0	7	Enable DP audio output to GMSL

EDP_AUDIO_CTRL5 (0x642D)

BIT	7	6	5	4	3	2	1	0
Field	DP_AUD_OUT_EN_1	–	–	RSVD[2:0]			RSVD[1:0]	
Reset	0b0	–	–	0b101			0b01	
Access Type	Write, Read	–	–					

BITFIELD	BITS	DESCRIPTION
DP_AUD_OUT_EN_1	7	Enable DP audio output to GMSL

EDP_GEN_INT_ST0 (0x6430)

Interrupt status for general EDP operations. This register consolidates all the EDP Rx interrupt sources allowing easier identification of the interrupt source.

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BIT	7	6	5	4	3	2	1	0
Field	DP_RLMS3_INT	DP_RLMS2_INT	DP_RLMS1_INT	DP_RLMS0_INT	DPRX_INT	–	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	–	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	–		

BITFIELD	BITS	DESCRIPTION	DECODE
DP_RLMS3_INT	7	DP RLMS lane 3 interrupt status. This is a pass-through interrupt from the DP RLMS for lane 3.	0: DP RLMS3 interrupt inactive 1: DP RLMS3 interrupt active
DP_RLMS2_INT	6	DP RLMS lane 2 interrupt status. This is a pass-through interrupt from the DP RLMS for lane 2.	0: DP RLMS2 interrupt inactive 1: DP RLMS2 interrupt active
DP_RLMS1_INT	5	DP RLMS lane 1 interrupt status. This is a pass-through interrupt from the DP RLMS for lane 1.	0: DP RLMS1 interrupt inactive 1: DP RLMS1 interrupt active
DP_RLMS0_INT	4	DP RLMS lane 0 interrupt status. This is a pass-through interrupt from the DP RLMS for lane 0.	0: DP RLMS0 interrupt inactive 1: DP RLMS0 interrupt active
DPRX_INT	3	DPRx interrupt status. This is a pass-through interrupt from the DPRx core.	0: DPRX interrupt inactive 1: DPRX interrupt active

EDP_GEN_INT_ST3 (0x6433)

Interrupt status for general EDP operations. This register consolidates all the EDP Rx interrupt sources allowing easier identification of the interrupt source.

BIT	7	6	5	4	3	2	1	0
Field	RSVD	APB_ERR_M0_IST	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type		Write 1 to Clear, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
APB_ERR_M0_IST	6	APB master 0 error interrupt status. This sticky status indicates that an error occurred on an APB transaction for master 0 (it is actually a pass-through of APB_STATUS_ERR_M0—0x64C6, bit 0). To clear, write 1 to this bit or write 1 to APB_STATUS_ERR_M0 bit 0.

EDP_GEN_INT_EN0 (0x6434)

Interrupt enable for each interrupt status bit defined in the EDP General Interrupt Status registers (EDP_GEN_INT_STx). Each bit enables (ANDed with) the corresponding bit of the EDP General Interrupt Status with the results ORed to create the level-sensitive EDP Rx Interrupt signal.

BIT	7	6	5	4	3	2	1	0
Field	DP_RLMS3_IEN	DP_RLMS2_IEN	DP_RLMS1_IEN	DP_RLMS0_IEN	DPRX_IEN	–	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	–	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–		

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BITFIELD	BITS	DESCRIPTION	DECODE
DP_RLMS3_IEN	7	DP RLMS lane 3 interrupt enable. This enables a DP RLMS lane 3 interrupt event to assert the level-sensitive EDP Rx interrupt signal.	0: Interrupt not enabled 1: Interrupt enabled
DP_RLMS2_IEN	6	DP RLMS lane 2 interrupt enable. This enables a DP RLMS lane 2 interrupt event to assert the level-sensitive EDP Rx interrupt signal.	0: Interrupt not enabled 1: Interrupt enabled
DP_RLMS1_IEN	5	DP RLMS lane 1 interrupt enable. This enables a DP RLMS lane 1 interrupt event to assert the level-sensitive EDP Rx interrupt signal.	0: Interrupt not enabled 1: Interrupt enabled
DP_RLMS0_IEN	4	DP RLMS lane 0 interrupt enable. This enables a DP RLMS lane 0 interrupt event to assert the level-sensitive EDP Rx interrupt signal.	0: Interrupt not enabled 1: Interrupt enabled
DPRX_IEN	3	DPRx interrupt enable. This enables a DPRx interrupt event to assert the level-sensitive EDP Rx interrupt signal.	0: Interrupt not enabled 1: Interrupt enabled

EDP_GEN_INT_EN3 (0x6437)

Interrupt enable for each interrupt status bit defined in the EDP General Interrupt Status registers (EDP_GEN_INT_STx). Each bit enables (ANDed with) the corresponding bit of the EDP General Interrupt Status with the results ORed to create the level-sensitive EDP Rx Interrupt signal.

BIT	7	6	5	4	3	2	1	0
Field	RSVD	APB_ERR_M0_IEN	–	–	–	–	–	–
Reset	0b0	0b0	–	–	–	–	–	–
Access Type		Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
APB_ERR_M0_IEN	6	APB master 0 error interrupt enable. This enables a APB master 0 error event to assert the level-sensitive EDP Rx interrupt signal.	0: Interrupt not enabled 1: Interrupt enabled

HPD_CTRL0 (0x6444)

Provides control for the hotplug detect (HPD) output.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HPD_IRQ_HO_DIS	HPD_IRQ	HPD_ST	HPD_MODE
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ_HO_DIS	3	Disables the hold-off time that occurs after an HPD low-to-high event that does not allow (hold-off) another HPD low event until the hold-off time has expired.	0: HPD hold-off enabled 1: HPD hold-off disabled

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BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ	2	HPD-IRQ assertion (normal and manual mode). Setting this bit causes HPD to be deasserted (low) for the time set by HPD_IRQ_TIME (assuming HPD would otherwise be active). This bit is self-clearing after the HPD IRQ time expires.	0: HPD normal/manual setting 1: HPD inactive (low)
HPD_ST	1	Controls HPD output state when in manual operation. It has no effect when operating in normal mode.	0: HPD inactive (low) 1: HPD active (high)
HPD_MODE	0	HPD mode selects between normal and manual HPD operation In normal mode, HPD is controlled by the DPRx core or the HPD_IRQ control. In manual mode, HPD is controlled by HPD_ST or the HPD_IRQ control.	0: Normal operation 1: Manual operation

HPD_CTRL1 (0x6445)

Provides control for the hotplug detect (HPD) output.

BIT	7	6	5	4	3	2	1	0
Field	HPD_IRQ_TIME[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ_TIME	7:0	HPD IRQ time sets the HPD IRQ active (low) time in 10us (+1/-0) when activated by the HPD_IRQ control.	N: HPD low for N*10us (+1/-0) when HPD_IRQ asserted

HPD_CTRL2 (0x6446)

Provides control for the hotplug detect (HPD) output.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	HPD_IRQ_HO	HOT_PLUG_DET	DPRX_HPD
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ_HO	2	HPD IRQ hold-off active status.	0: HPD IRQ hold-off inactive 1: HPD IRQ hold-off active
HOT_PLUG_DET	1	Hotplug detect output. This is the result of the combination of all the hotplug detect (HPD) sources (DPRX_HPD, HPD_IRQ, HPD_ST). This signal is forced inactive when OSN calibration is active.	0: HPD output inactive (low) 1: HPD output active (high)
DPRX_HPD	0	HPD from DPRx core. This is the normal HPD control when not in manual mode (HPD_MODE) and HPD_IRQ inactive.	0: DPRx HPD inactive 1: DPRx HPD active

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HPD_CTRL3 (0x6447)

Provides control for the hotplug detect (HPD) output.

BIT	7	6	5	4	3	2	1	0
Field	HPD_IRQ_HO_TIME[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ_HO_TIME	7:0	HPD IRQ hold-off time sets the time that HPD is held high after an HPD low-to-high event. The time is in 10us (+1/-0) units.	N: HPD held high for N*10us (+1/-0) after HPD low-to-high event.

APB_CTRL_M0_B0 (0x64C0)

Provides control for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	APB_TO_SEL_M0[2:0]		
Reset	–	–	–	–	–	0b001		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
APB_TO_SEL_M0	2:0	Timeout selection for APB master 0 access. This is a watchdog timer that returns the APB to the idle state when a timeout occurs to prevent bus hangups.	0x0: No timeout 0x1: 5-6µs 0x2: 10-11µs 0x3: 100µs 0x4: 500µs 0x5: 1ms 0x6: 2ms 0x7: 4ms

APB_CTRL_M0_B2 (0x64C2)

Provides status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_ERR_IEN_M0[7:0]							
Reset	0x00							
Access Type	Write 1 to Clear, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
APB_ERR_IEN_M0	7:0	Interrupt enable for APB master 0 error interrupt APB_ERR_M0_IST (EDP_GEN_INT_ST3, bit 6). This register enables the individual APB error events (see APB_STATUS_ERR_M0) for generating the interrupt.	0: Slave error interrupt enable 1: Premature termination interrupt enable 2: Timeout interrupt enable 3: Decode error (no register at address) interrupt enable 4: Invalid access (non-byte write when byte only writes allowed) interrupt enable 5: Reserved for future use 6: Reserved for future use 7: Blocking (non-blocking mode) interrupt enable

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APB_STATUS_M0_B0 (0x64C4)

Provides status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_STATUS_M0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
APB_STATUS_M0	7:0	Bus cycle status for APB master 0. This register holds the status returned at the end of each bus cycle. Reading this register immediately after an APB master 0 cycle returns the status of the bus cycle. Bit zero indicates the normal APB slave error with bits [7:1] indicating the cause when an error occurs.	0: Slave error 1: Premature termination 2: Timeout 3: Decode error (no register at address) 4: Invalid access (non-byte write when byte only writes allowed) 5: Reserved for future use 6: Reserved for future use 7: Blocking (non-blocking mode)

APB_STATUS_M0_B2 (0x64C6)

Provides status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_STATUS_ERR_M0[7:0]							
Reset	0x00							
Access Type	Write 1 to Clear, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
APB_STATUS_ERR_M0	7:0	Captured (sticky) status for first errored APB master 0 cycle since last clear. Write 1 to each bit to clear. Bit 0 is used as interrupt status (APB_ERR_M0_IST) and is also cleared when that interrupt bit is written to 1 (cleared). Individual events are enabled for causing the interrupt by APB_ERR_IEN_M0.	0: Slave error 1: Premature termination 2: Timeout 3: Decode error (no register at address) 4: Invalid access (non-byte write when byte only writes allowed) 5: Reserved for future use 6: Reserved for future use 7: Blocking (non-blocking mode)

APB_ADRCTL_ERR_M0_B0 (0x64C8)

Provides address/control error status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_ADR_ERR_M0_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
APB_ADR_ERR_M0_L	7:0	Captured address low (bits [7:0]) for first errored APB master 0 bus cycle since last error status clear (see APB_STATUS_ERR_M0).

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APB_ADRCTL_ERR_M0_B1 (0x64C9)

Provides address/control error status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	APB_ADR_ERR_M0_H[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
APB_ADR_ERR_M0_H	7:0	Captured address high (bits [15:8]) for first errored APB master 0 bus cycle since last error status clear (see APB_STATUS_ERR_M0).

APB_ADRCTL_ERR_M0_B2 (0x64CA)

Provides address/control error status for APB master 0 bus cycles.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	APB_WR_ERR_M0	APB_STB_ERR_M0[3:0]			
Reset	–	–	–	0b0	0x0			
Access Type	–	–	–	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION
APB_WR_ERR_M0	4	Captured write cycle indicator for first errored APB master 0 bus cycle since last error status clear (see APB_STATUS_ERR_M0).
APB_STB_ERR_M0	3:0	Captured write strobes for first errored APB master 0 bus cycle since last error status clear (see APB_STATUS_ERR_M0).

DPCD_CTRL_M0_B0 (0x64D0)

Provides control for DPCD access via APB master 0.

BIT	7	6	5	4	3	2	1	0
Field	DPCD_ADDR_HI_M0_L[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DPCD_ADDR_HI_M0_L	7:0	Lower 8 bits [7:0] of the DPCD high address (bits [19:8]) used for DPCD register access via APB master 0. The DPCD registers exist within the DPRX_LINK block at the display port defined 20-bit address space. A defined 256-byte portal (DPCD) within the local address space provides the lower 8 bits of the DPCD address.

DPCD_CTRL_M0_B1 (0x64D1)

Provides control for DPCD access via APB master 0.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DPCD_ADDR_HI_M0_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DPCD_ADDR_HI_M0_H	3:0	Higher 4 bits [11:8] of the DPCD high address (bits [19:8]) used for DPCD register access via APB master 0. The DPCD registers exist within the DPRX_LINK block at the display port defined 20-bit address space. A defined 256-byte portal (DPCD) within the local address space provides the lower 8 bits of the DPCD address.

DPCD_CTRL_M0_B2 (0x64D2)

Provides control for DPCD access via APB master 0.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DPCD_RDCLR_EN_M0	DPCD_APB_NOBLK_M0
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_RDCLR_EN_M0	1	Enables clearing of DPCD register bits when reading registers via APB master 0 that are defined as read-to-clear. When read-clearing is disabled, read-to-clear DPCD registers read via APB master 0 will not be cleared.	0: Clearing on read is disabled 1: Clearing on read is enabled
DPCD_APB_NOBLK_M0	0	Enable APB non-blocking mode. This allows APB master 0 accesses to the DPCD registers to terminate the bus cycle immediately with blocked status if the access would be delayed due to a competing AUX cycles. Retrying the access is necessary if the bus status indicates the access was blocked.	0: APB blocking mode active 1: APB non-blocking mode active

HDCP1_CTRL (0x6800)

Provides control of DP HDCP-1 operations.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	HDCP1_RST	HDCP1_RPTR	HDCP1_EN
Reset	–	–	–	–	–	0b0	0b1	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
HDCP1_RST	2	Resets the DP HDCP-1 authentication process. If the process has reached the authentication state then a re-authentication request is sent to upstream (REAUTH_REQ in Bstatus with CP_IRQ). This bit is self-clearing.	0: HDCP1 normal operation 1: HDCP1 reset
HDCP1_RPTR	1	Enables DP HDCP-1 repeater mode. The state of this bit is also used to set the DPCD Bcaps REPEATER capability at DPCD 0x68028 bit 1.	0: HDCP1 repeater mode disabled 1: HDCP1 repeater mode enabled
HDCP1_EN	0	Enables DP HDCP-1 operation when set to 1. Disables DP HDCP-1 operations when set to 0 and the authentication process has not started or is reset. The state of this bit is also used to set the DPCD Bcaps HDCP_CAPABLE capability at DPCD 0x68028 bit 0.	0: HDPC-1 disabled 1: HDCP-1 enabled

HDCP1_STATUS (0x6801)

Provides status of DP HDCP-1 operations.

BIT	7	6	5	4	3	2	1	0
Field	HDCP1_AUTH_IN_PROGRESS	–	–	–	–	HDCP1_DS_CHG	HDCP1_DS_RDY	HDCP1_AUTH
Reset	0b0	–	–	–	–	0b0	0b0	0b0
Access Type	Read Only	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP1_AUTH_IN_PROGRESS	7	Indicates that the HDCP-1 repeater independent authentication process is in progress.	0: HDPC-1 authentication not in progress 1: HDCP-1 authentication in progress
HDCP1_DS_CHG	2	Indicates that the HDCP-1 repeater downstream status or KSV list changed. This bit is cleared with re-authentication or authentication reset.	0: HDCP1 no repeater downstream change 1: HDCP1 repeater downstream change
HDCP1_DS_RDY	1	Indicates that the HDCP-1 repeater downstream KSV list is ready for the repeater part of the protocol. This bit is cleared with re-authentication or authentication reset.	0: HDCP1 repeater downstream not ready 1: HDCP1 repeater downstream ready
HDCP1_AUTH	0	Indicates that the HDCP-1 authentication process has reached the authenticated state for the first part of the protocol that is independent of repeater operations. This bit is cleared with re-authentication or authentication reset.	0: HDPC-1 not authenticated, part 1 1: HDCP-1 authenticated, part 1

HDCP2_CTRL (0x6802)

Provides control of DP HDCP2 operations.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	HDCP2_RST	HDCP2_RPTR	HDCP2_EN
Reset	–	–	–	–	–	0b0	0b1	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP2_RST	2	Resets the DP HDCP-2 authentication process. If the process has reached the authentication state then a re-authentication request is sent to upstream (REAUTH_REQ in RxStatus with CP_IRQ). This bit is self-clearing.	0: HDCP2 normal operation 1: HDCP2 reset
HDCP2_RPTR	1	Enables DP HDCP2 repeater mode. The state of this bit is also used to set the DPCD RxCaps REPEATER capability for DPCD 0x6921D bit 0.	0: HDCP2 repeater mode disabled 1: HDCP2 repeater mode enabled
HDCP2_EN	0	Enables DP HDCP2 operation when set to 1. Disables DP HDCP2 operations when set to 0 and the authentication process has not started or is reset. The state of this bit is also used to set the DPCD RxCaps HDCP_CAPABLE capability for DPCD 0x6921D bit 1.	0: HDPC2 disabled 1: HDCP2 enabled

HDCP2_STATUS (0x6803)

Provides status of DP HDCP-2 operations.

BIT	7	6	5	4	3	2	1	0
Field	HDCP2_AUTH_IN_PROGRESS	–	–	HDCP2_STR_MGT_ERR	HDCP2_STR_MGT	HDCP2_DS_CHG	HDCP2_DS_RDY	HDCP2_AUTH
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP2_AUTH_IN_PROGRESS	7	Indicates that the HDCP-2 repeater independent authentication process is in progress.	0: HDPC-2 authentication not in progress 1: HDCP-2 authentication in progress
HDCP2_STR_MGT_ERR	4	Indicates that the HDCP-2 repeater has received a stream management message that would send Type 1 content on a video stream attached to HDCP-1 downstream. This bit is cleared with re-authentication or authentication reset.	0: HDCP2 no repeater stream management error 1: HDCP2 repeater stream management error
HDCP2_STR_MGT	3	Indicates that the HDCP-2 repeater has received a stream management message. This bit is cleared with re-authentication or authentication reset.	0: HDCP2 no repeater stream management message received 1: HDCP2 repeater stream management message received
HDCP2_DS_CHG	2	Indicates that the HDCP-2 repeater downstream status or Rx ID list changed. This bit is cleared with re-authentication or authentication reset.	0: HDCP2 no repeater downstream change 1: HDCP2 repeater downstream change

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BITFIELD	BITS	DESCRIPTION	DECODE
HDCP2_DS_RDY	1	Indicates that the HDCP-2 repeater downstream Rx ID list is ready state for the repeater part of the protocol.This bit is cleared with re-authentication or authentication reset.	0: HDCP2 repeater downstream not ready 1: HDCP2 repeater downstream ready
HDCP2_AUTH	0	Indicates that the HDCP-2 authentication process has reached the authenticated state for the first part of the protocol that is independent of repeater operations. This bit is cleared with re-authentication or authentication reset.	0: HDPC-2 not authenticated, part 1 1: HDCP-2 authenticated, part 1

HDCP_RPTR_DS_CFG_X (0x6804)

DPRX HDCP repeater downstream configuation for GMSL stream X.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RPTR_DS_ONE_RXID	RPTR_DS_HDCP2_EN	RPTR_DS_HDCP1_EN
Reset	–	–	–	–	–	0b0	0b1	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RPTR_DS_ONE_RXID	2	Enables repeater to use only 1 downstream Rx ID even though 2 are received. This is a special case where both downstream Rx IDs are the same due to split link operation.	0: Normal repeater Rx ID operation 1: Repeater uses only 1 received downstream Rx ID (special case)
RPTR_DS_HDCP2_EN	1	Enables HDCP-2 as downstream repeater for GMSL stream X.	0: HDCP2 downstream repeater disabled 1: HDCP2 downstream repeater enabled
RPTR_DS_HDCP1_EN	0	Enables HDCP-1 as downstream repeater for GMSL stream X.	0: HDCP1 downstream repeater disabled 1: HDCP1 downstream repeater enabled

HDCP_RPTR_DS_CFG_Y (0x6805)

DPRX HDCP repeater downstream configuation for GMSL stream Y.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RPTR_DS_HDCP2_EN	RPTR_DS_HDCP1_EN
Reset	–	–	–	–	–	–	0b1	0b1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RPTR_DS_HDCP2_EN	1	Enables HDCP-2 as downstream repeater for GMSL stream Y.	0: HDCP2 downstream repeater disabled 1: HDCP2 downstream repeater enabled
RPTR_DS_HDCP1_EN	0	Enables HDCP-1 as downstream repeater for GMSL stream Y.	0: HDCP1 downstream repeater disabled 1: HDCP1 downstream repeater enabled

HDCP1_STATE (0x6808)

DPRX HDCP-1 state.

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BIT	7	6	5	4	3	2	1	0
Field	HDCP1_STATE[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HDCP1_STATE	7:0	State of DP HDCP-1 operation.

HDCP1_SUBSTATE (0x6809)

DPRX HDCP-1 state.

BIT	7	6	5	4	3	2	1	0
Field	HDCP1_SUBSTATE[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HDCP1_SUBSTATE	7:0	Indicates the phase of operation within a given HDCP-1 state.

HDCP2_STATE (0x680A)

DPRX HDCP-2 state.

BIT	7	6	5	4	3	2	1	0
Field	HDCP2_STATE[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HDCP2_STATE	7:0	State of DP HDCP-1 operation.

HDCP2_SUBSTATE (0x680B)

DPRX HDCP-2 state.

BIT	7	6	5	4	3	2	1	0
Field	HDCP2_SUBSTATE[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HDCP2_SUBSTATE	7:0	Indicates the phase of operation within a given HDCP-2 state.

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LINK_ENABLE (0x7000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LINK_ENABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_ENABLE	0	Enables DP Rx for operation. When enabled, HPD is active (normally high, except when HPD IRQ is activated) and the DP Rx is operational. When disabled, HPD is held low and the DP Rx is disabled.	0: DP Rx disabled - HPD=0 1: DP Rx enabled - HPD active

AUX_CLOCK_DIV_B0 (0x7004)

BIT	7	6	5	4	3	2	1	0
Field	AUX_CLOCK_DIV_L[7:0]							
Reset	0x96							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
AUX_CLOCK_DIV_L	7:0	AUX clock divider bits 7-0. This integer value is the divisor used to generate the internal 1Mhz AUX clock from the APB interface clock.

AUX_CLOCK_DIV_B1 (0x7005)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AUX_CLOCK_DIV_H[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
AUX_CLOCK_DIV_H	1:0	AUX clock divider bits 9-8. This integer value is the divisor used to generate the internal 1Mhz AUX clock from the APB interface clock.

MISC_CONFIG_B0 (0x7018)

BIT	7	6	5	4	3	2	1	0
Field	DISABLE_AUX_FILTER	ALPM_ENABLE	EDP_FUNCTION_ENABLE	MAX_DOWNSPREAD_CONFIG	BRANCH_SUPPORT_ENABLE	DISABLE_INACTIVE_COUNT	DEFER_LONG_I2C	MSA_DELAY_BYPASS
Reset	0b0	0b0	0b0	0b1	0b0	0b1	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
DISABLE_AUX_FILTER	7	Disables the AUX data glitch filtering used to improve the robustness of the AUX channel.	0: Normal operation 1: AUX glitch filtering disabled
ALPM_ENABLE	6	Enables Embedded DisplayPort (eDP) power management functionality. This functionality may be set independently from EDP_FUNCTION_ENABLE.	0: eDP PM capabilities disabled 1: eDP PM capabilities enabled
EDP_FUNCTION_ENABLE	5	Enables Embedded DisplayPort (eDP) functionality and reports eDP capability in DPCD.	0: eDP capabilities disabled 1: eDP capabilities enabled
MAX_DOWNSPREAD_CONFIG	4	Enables downspread capability reported in DPCD. Must be enabled for compliance with DisplayPort 1.2a and above.	0: Downspread capability disabled 1: Downspread capability enabled
BRANCH_SUPPORT_ENABLE	3	Enables DisplayPort branch device capabilities.	0: Branch device capabilities disabled 1: Branch device capabilities enabled
DISABLE_INACTIVE_COUNT	2	Disables the inactive video counter (timer) that will assert HPD-IRQ if the counter expires without detecting video or the NO_VIDEO signal.	0: Inactive counter enabled 1: Inactive counter disabled
DEFER_LONG_I2C	1	Enables sending DEFER response to I2C-over-AUX transactions that will exceed the normal AUX timeout.	0: Respond with partial ACK 1: Respond with DEFER
MSA_DELAY_BYPASS	0	Disables validating Main Stream Attribute (MSA) values by checking for 2 consecutive matching values. Values are received each vertical blank period.	0: Normal MSA validation 1: MSA validation disabled

MISC_CONFIG_B1 (0x7019)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PRESERVE_EVENT_INT	MSO_FUNCTION_EN	–	MST_FUNCTION_ENABLE
Reset	–	–	–	–	0b0	0b0	–	0b1
Access Type	–	–	–	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PRESERVE_EVENT_INT	3	Disables clearing event interrupts.	0: Event interrupts not preserved 1: Event interrupts are preserved
MSO_FUNCTION_EN	2	Enables a special multi-stream functionality for single-stream transport (multi-SST operation - MSO) mode and reports MSO capability in DPCD.	0: MSO capablity disabled 1: MSO capability enabled
MST_FUNCTION_ENABLE	0	Enables multi-stream transport (MST) functionality and reports MST capability in DPCD.	0: MST capablity disabled 1: MST capability enabled

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DISPLAYPORT_VERSION (0x701C)

BIT	7	6	5	4	3	2	1	0
Field	DP_VERSION[7:0]							
Reset	0x14							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DP_VERSION	7:0	DisplayPort revision level reported through DPCD. This can be used to inform a DP source of the level of compatibility desired.	0x10: DP version 1.0 supported 0x11: DP version 1.1 supported 0x12: DP version 1.2 supported 0x13: DP version 1.3 supported 0x14: DP version 1.4 supported ----: Other values reserved

LINK_SERVICE_IRQ (0x7020)

Link Service IRQ Setting

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LINK_SERVICE_IRQ[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write Only				

BITFIELD	BITS	DESCRIPTION
LINK_SERVICE_IRQ	4:0	Sets the Link Service IRQ Vector accessed via DPCD 0x02005.These bits are self-clearing.

REQUEST_ERROR_COUNT (0x7024)

BIT	7	6	5	4	3	2	1	0
Field	REQUEST_ERROR_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REQUEST_ERROR_COUNT	7:0	Provides a running total of errors detected on inbound AUX Channel requests. When an improperly formatted AUX request is made, the internal AUX controller will flag an error and increment this register by 1. The value of this register is cleared by writing a 0 to the REQUEST_COUNT_L register.

REQUEST_COUNT_L (0x7028)

BIT	7	6	5	4	3	2	1	0
Field	REQUEST_COUNT_L[7:0]							
Reset	0x00							
Access Type	Write 1 to Clear, Read							

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BITFIELD	BITS	DESCRIPTION
REQUEST_COUNT_L	7:0	AUX request count bits 7-0. Provides a running total of the number of AUX Request transactions received (native AUX and I2C-over-AUX). This register is updated after the request is received and before the reply is generated. The value of this register is cleared when a 1 is written to bit 0 of this register.

REQUEST_COUNT_H (0x7029)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	REQUEST_COUNT_H[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION
REQUEST_COUNT_H	1:0	AUX request count bits 9-8. Provides a running total of the number of AUX Request transactions received (native AUX and I2C-over-AUX). This register is updated after the request is received and before the reply is generated. The value of this register is cleared when a 0 is written to REQUEST_COUNT_L.

HPD_INTERRUPT (0x702C)

Instructs the receiver core to assert an interrupt to the transmitter using the HPD signal. An HPD pulse of 750 usec is generated by this function. When the HDCP functionality is included in the core, this register can also be used to force a CP_IRQ event

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RSVD	HPD_IRQ
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–		Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_IRQ	0	Assert an interrupt to the transmitter using the hotplug detect (HPD) signal. The HPD output from the DPRx core is held low for approximately 750us. This bit is self-clearing. See HPD_CTRL register for manual HPD conrol that may supercede this control.	0: Normal operation 1: HPD-IRQ asserted

HPD_INTERRUPT_MASK (0x702D)

Masks the specified interrupt sources from asserting the HPD_IRQ signal. When set to a 1, the specified interrupt source is masked. This register resets to all 0s at power up resulting in all interrupt sources being enabled.

BIT	7	6	5	4	3	2	1	0
Field	–	HPD_INTERRUPT_MASK[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

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BITFIELD	BITS	DESCRIPTION
HPD_INTERRUPT_MASK	6:0	Disables individual sources that can cause assertion of a hotplug detect interrupt event (HPD IRQ). Setting a bit to 1 masks (disables) the corresponding HPD IRQ source.

LANE_REMAP_B0 (0x7030)

BIT	7	6	5	4	3	2	1	0
Field	REMAP_LANE_3[1:0]		REMAP_LANE_2[1:0]		REMAP_LANE_1[1:0]		REMAP_LANE_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
REMAP_LANE_3	7:6	Specifies which physical lane number (0-3) will be mapped to the internal lane 3. The REMAP_ENABLE bit must be set for the mapping to be active.	0: Map physical lane 0 to logical lane 3 1: Map physical lane 1 to logical lane 3 2: Map physical lane 2 to logical lane 3 3: Map physical lane 3 to logical lane 3
REMAP_LANE_2	5:4	Specifies which physical lane number (0-3) will be mapped to the internal lane 2. The REMAP_ENABLE bit must be set for the mapping to be active.	0: Map physical lane 0 to logical lane 2 1: Map physical lane 1 to logical lane 2 2: Map physical lane 2 to logical lane 2 3: Map physical lane 3 to logical lane 2
REMAP_LANE_1	3:2	Specifies which physical lane number (0-3) will be mapped to the internal lane 1. The REMAP_ENABLE bit must be set for the mapping to be active.	0: Map physical lane 0 to logical lane 1 1: Map physical lane 1 to logical lane 1 2: Map physical lane 2 to logical lane 1 3: Map physical lane 3 to logical lane 1
REMAP_LANE_0	1:0	Specifies which physical lane number (0-3) will be mapped to the internal lane 0. The REMAP_ENABLE bit must be set for the mapping to be active.	0: Map physical lane 0 to logical lane 0 1: Map physical lane 1 to logical lane 0 2: Map physical lane 2 to logical lane 0 3: Map physical lane 3 to logical lane 0

LANE_REMAP_B1 (0x7031)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	REMAP_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REMAP_ENABLE	0	Remap enable. This bit must be set to enable the physical to logical lane remapping defined in the REMAP_LANE_0/1/2/3.	0: Lane remapping disabled 1: Lane remapping enabled

LANE_REMAP_B2 (0x7032)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	INVERT_LANE_3	INVERT_LANE_2	INVERT_LANE_1	INVERT_LANE_0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
INVERT_LANE_3	3	Inverts the state of all bits received on lane 3.	0: Lane bits not inverted 1: Lane bits inverted
INVERT_LANE_2	2	Inverts the state of all bits received on lane 2.	0: Lane bits not inverted 1: Lane bits inverted
INVERT_LANE_1	1	Inverts the state of all bits received on lane 1.	0: Lane bits not inverted 1: Lane bits inverted
INVERT_LANE_0	0	Inverts the state of all bits received on lane 0.	0: Lane bits not inverted 1: Lane bits inverted

VIDEO_INPUT_RESET (0x7054)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LINK_RESET	VIDEO_INPUT_RESET
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RESET	1	Resets the link clock domain logic. No internal control registers will be modified by this reset. This bit is self-clearing.	0: Normal operation 1: Link reset
VIDEO_INPUT_RESET	0	Resets the video capture clock domain logic. No internal control registers will be modified by this reset. This bit is self-clearing.	0: Normal operation 1: Video reset

EDP_IGNORE_MSA (0x7058)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	EDP_IGNORE_MSA
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EDP_IGNORE_MSA	0	When configured for eDP support, a 1 indicates that the Sink device does not require the video mode timing parameters to be transmitted through the MSA. This bit can only be set to a 1 when the receiver core display timing generator (DTG) is configured for DMA mode operation. The value of this bit is mirrored in the DPCD at offset 0x0007 bit 6.	0: MSA parameters required 1: MSA parameters not required (eDP support only)

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MAX_LANE_COUNT (0x7070)

BIT	7	6	5	4	3	2	1	0
Field	MAX_LANE_COUNT[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_LANE_COUNT	7:0	The maximum number of lanes supported is specified through this register. This register should be set before the LINK_ENABLE register bit is set to a 1. The value of this register is reported to the DisplayPort source device through the DPCD register set at address 0x0002. Valid values are 1, 2, and 4. All other values are reserved and must not be used.	0x01: 1 lane supported (lane 0) 0x02: 2 lanes supported (lanes 0,1) 0x04: 4 lanes supported (lanes 0,1,2,3) XX: All other values reserved

MAX_LINK_RATE (0x7074)

BIT	7	6	5	4	3	2	1	0
Field	MAX_LINK_RATE[7:0]							
Reset	0x1E							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_LINK_RATE	7:0	The maximum link rate supported is specified through this register. This register should be set before the LINK_ENABLE register bit is set to 1. Link training will fail if the link bandwidth (rate) setting is above the value of this registers.The value of this register is reported to the DisplayPort source device through the DPCD register set at address 0x0001.	0x06: 1.62 Gbps 0x0A: 2.7 Gbps 0x14: 5.4 Gbps 0x1E: 8.1 Gbps XX: All other values reserved

MIN_LINK_RATE (0x7075)

BIT	7	6	5	4	3	2	1	0
Field	MIN_LINK_RATE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MIN_LINK_RATE	7:0	The minimum link rate supported is specified through this register. This register should be set before the LINK_ENABLE register bit is set to 1. Link training will fail if the link bandwidth (rate) setting is below the value of this registers.	0x00: No minimum rate 0x06: 1.62 Gbps 0x0A: 2.7 Gbps 0x14: 5.4 Gbps 0x1E: 8.1 Gbps XX: All other values reserved

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AUX_RD_INTERVAL (0x70A0)

BIT	7	6	5	4	3	2	1	0
Field	–	AUX_RD_INTERVAL[6:0]						
Reset	–	0b0000100						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
AUX_RD_INTERVAL	6:0	Read interval during link training for link status and adjust requests. The value of this register is directly mapped from the values of the DPCD register at offset 0x000E. Only values listed below are valid.	0x00: 100us for clock recovery, 400us for channel equalization 0x01: 4ms 0x02: 8ms 0x03: 12ms 0x04: 16ms Other: Reserved

I2C_SPEED_CAPABILITY (0x70A4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	I2C_SPEED_CAPABILITY[5:0]					
Reset	–	–	0b111000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_SPEED_CAPABILITY	5:0	Configuration indicating the supported speed map on the external I2C bus. Set the corresponding bit to a 1 to indicate support for an I2C bus operating at that speed.	000001: 1 Kbps 000010: 5 Kbps 000100: 10 Kbps 001000: 100 Kbps 010000: 400 Kbps 100000: 1 Mbps

I2C_SCL_TIMEOUT_SEL (0x70A5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	I2C_SCL_TIMEOUT_SEL[3:0]			
Reset	–	–	–	–	0x08			
Access Type	–	–	–	–	Write, Read			

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BITFIELD	BITS	DESCRIPTION	DECODE
I2C_SCL_TIMEOUT_SEL	3:0	Selects a maximum time (timeout) for the I2C-over-AUX SCL signal to be low (active) during a transaction. When the maximum low time is exceeded the transaction is immediately terminated.	0x00: Timeout disabled 0x01: 2 ms 0x02: 4 ms 0x03: 6 ms 0x04: 8 ms 0x05: 10 ms 0x06: 12 ms 0x07: 14 ms 0x08: 16 ms 0x09: 18 ms 0x0A: 20 ms 0x0B: 22 ms 0x0C: 24 ms 0x0D: 26 ms 0x0E: 28 ms 0x0F: 30 ms

FEC_ENABLE (0x7300)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	FEC_BYPASS_ERROR_CORRECTION	FEC_SUPPORT
Reset	–	–	–	–	–	–	0b0	0b1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BYPASS_ERROR_CORRECTION	1	Disables FEC internal error correction. Error detection is still active.	0: FEC error correction enabled 1: FEC error correction disabled
FEC_SUPPORT	0	FEC_SUPPORT allows FEC operation and indicates to the DP source via DPCD that FEC is supported	0: FEC support disabled. 1: FEC support enabled.

FEC_CLEAR_ERROR (0x7301)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	FEC_BUFFER_RESET	FEC_CLR_ERROR_CNT
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BUFFER_RESET	1		0: Normal operation 1: FEC buffer reset. This bit is self-clearing
FEC_CLR_ERROR_CNT	0		0: Normal operation 1: Clear error counters. This bit is self-clearing.

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FEC_PM_CLR (0x7302)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MISSING_PM_ERRFL_CLR	UNEXP_PM_ERRFL_CLR
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
MISSING_PM_ERRFL_CLR	1		0: Normal operation 1: Clear Missing Expected Parity Marker error flag and counter. This bit is self-clearing.
UNEXP_PM_ERRFL_CLR	0		0: Normal operation 1: Clear Unexpected Parity Marker error flag and counter. This bit is self-clearing.

FEC_RUNNING (0x7304)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	FEC_RUNNING
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_RUNNING	0		0: FEC is not running 1: FEC is running

FEC_PM_ERRCTRL (0x7306)

Please Note: Bit field settings in this register should not be modified without consulting the factory.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	FEC_BADPMTRAN_EN	FEC_PMFIX_DIS
Reset	–	–	–	–	–	–	0b0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_BADPMTRAN_EN	1	Enable the False Parity Marker conversion feature. Converts unexpected PM in data symbol. Please Note: This bit field should NOT be programmed without consulting the factory	0x0: Normal Operation (default) 0x1: Enable the False Parity Marker conversion feature
FEC_PMFIX_DIS	0	Disable Missing/Unexpected Parity Marker Correction feature. Please Note: This bit field should NOT be programmed without consulting the factory.	0x0: Normal Operation (default) 0x1: Disable Missing/Unexpected Parity Marker Correction feature

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FEC_FALSE_PM_ERR_CTRL (0x730C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FEC_PM_ERR_LANESEL	–	–	–	FEC_PM_ERR_IRQ_EN
Reset	–	–	–	0x0	–	–	–	0x0
Access Type	–	–	–	Write, Read	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_PM_ERR_LANESEL	4	Selects which Missing/Unexpected Parity Marker counters and flags are reported. Please see read only register fields FEC_UNEXP_PM_ERR_CNT, FEC_UNEXP_PM_ERR_FLG, FEC_MISSING_PM_ERR_CNT, and FEC_MISSING_PM_ERR_FLG. Default is to select counters and flags from Lane 0/1 decoder. Write a 1 to select counters and flags from Lane 2/3 decoder.	0x0: Select counters from Lane 0/1 FEC decoder 0x1: Select counters from Lane 2/3 FEC decoder
FEC_PM_ERR_IRQ_EN	0	Enable Missing/Unexpected FEC Parity Marker error interrupt request. This feature can be used by the host to enable interrupt requests when an unexpected or missing Parity Marker is detected. An unexpected Parity Marker can occur for several reasons; data corrupted into a PM by random bit errors, mistaken output by the DPTX. A missing expected PM can occur for several reasons; Parity Marker corrupted by a random bit error, mistaken output by the DPTX. It should be noted, that Parity Markers are not covered by FEC.	0x0: Disable (default) 0x1: Enable IRQ

FEC_UNEXP_PM_ERR (0x730D)

BIT	7	6	5	4	3	2	1	0
Field	FEC_UNEXP_PM_ERR_FLG	–	–	–	FEC_UNEXP_PM_ERR_CNT[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Read Only	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
FEC_UNEXP_PM_ERR_FLG	7	Unexpected Parity Marker Error Flag. This flag is asserted if more than 4 unexpected Parity Markers are received. When enabled, this error flag will trigger an interrupt. Please see register field FEC_PM_ERR_IRQ_EN This flag is cleared by writting a 1 to the UNEXP_PM_ERRFL_CLR register.

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BITFIELD	BITS	DESCRIPTION
FEC_UNEXP_PM_ERR_CNT	3:0	Reports the number of unexpected Parity Markers. This counter will limit and remain at 15 until cleared. This counter is cleared by writting a 1 to the UNEXP_PM_ERRFL_CLR register.

FEC_MISSING_PM_ERR (0x730E)

BIT	7	6	5	4	3	2	1	0
Field	FEC_MISSING_PM_ERR_FLG	–	–	–	FEC_MISSING_PM_ERR_CNT[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Read Only	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
FEC_MISSING_PM_ERR_FLG	7	Missing Expected Parity Marker Error Flag. This flag is asserted when 4 consecutive Parity Markers are detected as missing. When enabled, this error flag will trigger an interrupt. Please see register field FEC_PM_ERR_IRQ_EN. This flag is cleared by writing a 1 to the MISSING_PM_ERRFL_CLR register.
FEC_MISSING_PM_ERR_CNT	3:0	Counts Number of Missing expected Parity Markers. This is a running counter such that a missing Parity Marker causes the counter to increment, but when a correct Parity Marker is received the counter decrements. This count is cleared by writing a 1 to the MISSING_PM_ERRFL_CLR register.

DPCD_LINK_BW_SET (0x7400)

BIT	7	6	5	4	3	2	1	0
Field	DPCD_LINK_BW_SET[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_LINK_BW_SET	7:0	This is the DPCD (0x0100) value for the current link rate as set by the DP source device.	06: 1.62 Gbps (not supported) 0A: 2.7 Gbps 14: 5.4 Gbps 1E: 8.1 Gbps XX: All other values reserved

DPCD_LANE_COUNT_SET (0x7404)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DPCD_LANE_COUNT_SET[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Read Only				

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BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_LANE_COUNT_SET	4:0	This is the DPCD (0x0101) value for the number of lanes in use as set by the DP source device.	01: Lane 0 active 02: Lanes 0, 1 active 04: Lanes 0,1,2,3 active XX: All other values reserved

DPCD_ENHANCED_FRAME_EN (0x7408)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DPCD_ENHANCED_FRAME_EN
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_ENHANCED_FRAME_EN	0	This is the DPCD value for the current training pattern as set by the DP source. These are bits 2-0 of the DPCD register TRAINING_PATTERN_SET (0x0102).	0: Enhance framing disabled 1: Enhanced framing enabled

DPCD_TRAINING_PATTERN_SET (0x740C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DPCD_TRAINING_PATTERN_SET[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_TRAINING_PATTERN_SET	2:0	This is the DPCD value for the current training pattern as set by the DP source. These are bits 2-0 of the DPCD register TRAINING_PATTERN_SET (0x0102).	000: Training pattern disabled 001: Training pattern 1 (TPS1) 010: Training pattern 2 (TPS2) 011: Training pattern 3 (TPS3 - HBR2) 111: Training pattern 4 (TPS4 - HBR3) 100-110: Reserved

DPCD_LINK_QUAL_PAT_SET_B0 (0x7410)

BIT	7	6	5	4	3	2	1	0
Field	–	DPCD_LINK_QUAL_LANE1_SET[2:0]			–	DPCD_LINK_QUAL_LANE0_SET[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Read Only			–	Read Only		

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BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_LINK_QUAL_LANE1_SET	6:4	This is the DPCD value for the current link quality pattern for lane 1 as set by the DP source. These are bits 2-0 of the DPCD register LINK_QUAL_LANE0_SET (0x010C).	000: Link quality pattern disabled 001: D10.2 (TPS1) 010: Symbol Error Rate (SER) 011: PBRS7 100: 80-bit Custom 101: CP2520 Pattern 1 110: CP2520 Pattern 2 111: CP2520 Pattern 3 (TPS4)
DPCD_LINK_QUAL_LANE0_SET	2:0	This is the DPCD value for the current link quality pattern for lane 0 as set by the DP source. These are bits 2-0 of the DPCD register LINK_QUAL_LANE0_SET (0x010B).	000: Link quality pattern disabled 001: D10.2 (TPS1) 010: Symbol Error Rate (SER) 011: PBRS7 100: 80-bit Custom 101: CP2520 Pattern 1 110: CP2520 Pattern 2 111: CP2520 Pattern 3 (TPS4)

DPCD_LINK_QUAL_PAT_SET_B1 (0x7411)

BIT	7	6	5	4	3	2	1	0
Field	–	DPCD_LINK_QUAL_LANE3_SET[2:0]			–	DPCD_LINK_QUAL_LANE2_SET[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_LINK_QUAL_LANE3_SET	6:4	This is the DPCD value for the current link quality pattern for lane 3 as set by the DP source. These are bits 2-0 of the DPCD register LINK_QUAL_LANE0_SET (0x010E).	000: Link quality pattern disabled 001: D10.2 (TPS1) 010: Symbol Error Rate (SER) 011: PBRS7 100: 80-bit Custom 101: CP2520 Pattern 1 110: CP2520 Pattern 2 111: CP2520 Pattern 3 (TPS4)
DPCD_LINK_QUAL_LANE2_SET	2:0	This is the DPCD value for the current link quality pattern for lane 2 as set by the DP source. These are bits 2-0 of the DPCD register LINK_QUAL_LANE0_SET (0x010D).	000: Link quality pattern disabled 001: D10.2 (TPS1) 010: Symbol Error Rate (SER) 011: PBRS7 100: 80-bit Custom 101: CP2520 Pattern 1 110: CP2520 Pattern 2 111: CP2520 Pattern 3 (TPS4)

DPCD_SCRAMBLING_DISABLE (0x7418)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DPCD_SCRAMBLING_DISABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Read Only

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BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_SCRAMBLING_DISABLE	0	This is the DPCD value for scrambling disable control as set by the DP source. This is bit 5 of the DPCD register TRAINING_PATTERN_SET (0x0102).	0: Scrambling enabled 1: Scrambling disabled

DPCD_SYMBOL_ERROR_COUNT_SELECT (0x741C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DPCD_SYMBOL_ERROR_COUNT_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_SYMBOL_ERROR_COUNT_SELECT	1:0	This is the DPCD value for the current symbol error count select as set by the DP source. These are bits 7-6 of the DPCD register TRAINING_PATTERN_SET (0x0102).	00: Disparity errors and illegal symbol errors 01: Disparity errors only 10: Illegal symbol errors only 11: Reserved

DPCD_TRAINING_LANE_0_SET (0x7420)

This register reflects the current values set by the transmitter for DPCD register TRAINING_LANE2_SET (0x105). Used by the transmitter during link training to configure the receiver PHY for lane 2.

BIT	7	6	5	4	3	2	1	0
Field	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
Reset	–	–	0b0	0b00		0b0	0b00	
Access Type	–	–	Read Only	Read Only		Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_PRE_EMPHASIS_REACHED	5	This is the DPCD value for the current max pre-emphasis reached as set by the DP source (training phase 1).	0: Max preemphasis not reached 1: Max preemphasis reached
PRE_EMPHASIS_SET	4:3	This is the DPCD value for the current preemphasis as set by the DP source (training phase 2).	00: Preemphasis level 0 (training phase 2) 01: Preemphasis level 1 (training phase 2) 10: Preemphasis level 2 (training phase 2) 11: Preemphasis level 3 (training phase 2)
MAX_SWING_REACHED	2	This is the DPCD value for the current max swing reached as set by the DP source (training phase 1).	0: Max swing not reached 1: Max swing reached
VOLTAGE_SWING_SET	1:0	This is the DPCD value for the current voltage swing as set by the DP source (training phase 1).	00: Voltage swing level 0 (training phase 1) 01: Voltage swing level 1 (training phase 1) 10: Voltage swing level 2 (training phase 1) 11: Voltage swing level 3 (training phase 1)

DPCD_TRAINING_LANE_1_SET (0x7424)

This register reflects the current values set by the transmitter for DPCD register TRAINING_LANE1_SET (0x104). Used by the transmitter during link training to configure the receiver PHY for lane 1.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
Reset	–	–	0b0	0b00		0b0	0b00	
Access Type	–	–	Read Only	Read Only		Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_PRE_EMPHASIS_REACHED	5	This is the DPCD value for the current max pre-emphasis reached as set by the DP source (training phase 1).	0: Max preemphasis not reached 1: Max preemphasis reached
PRE_EMPHASIS_SET	4:3	This is the DPCD value for the current preemphasis as set by the DP source (training phase 2).	00: Preemphasis level 0 (training phase 2) 01: Preemphasis level 1 (training phase 2) 10: Preemphasis level 2 (training phase 2) 11: Preemphasis level 3 (training phase 2)
MAX_SWING_REACHED	2	This is the DPCD value for the current max swing reached as set by the DP source (training phase 1).	0: Max swing not reached 1: Max swing reached
VOLTAGE_SWING_SET	1:0	This is the DPCD value for the current voltage swing as set by the DP source (training phase 1).	00: Voltage swing level 0 (training phase 1) 01: Voltage swing level 1 (training phase 1) 10: Voltage swing level 2 (training phase 1) 11: Voltage swing level 3 (training phase 1)

DPCD_TRAINING_LANE_2_SET (0x7428)

This register reflects the current values set by the transmitter for DPCD register TRAINING_LANE2_SET (0x105). Used by the transmitter during link training to configure the receiver PHY for lane 2.

BIT	7	6	5	4	3	2	1	0
Field	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
Reset	–	–	0b0	0b00		0b0	0b00	
Access Type	–	–	Read Only	Read Only		Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_PRE_EMPHASIS_REACHED	5	This is the DPCD value for the current max pre-emphasis reached as set by the DP source (training phase 1).	0: Max preemphasis not reached 1: Max preemphasis reached
PRE_EMPHASIS_SET	4:3	This is the DPCD value for the current preemphasis as set by the DP source (training phase 2).	00: Preemphasis level 0 (training phase 2) 01: Preemphasis level 1 (training phase 2) 10: Preemphasis level 2 (training phase 2) 11: Preemphasis level 3 (training phase 2)
MAX_SWING_REACHED	2	This is the DPCD value for the current max swing reached as set by the DP source (training phase 1).	0: Max swing not reached 1: Max swing reached
VOLTAGE_SWING_SET	1:0	This is the DPCD value for the current voltage swing as set by the DP source (training phase 1).	00: Voltage swing level 0 (training phase 1) 01: Voltage swing level 1 (training phase 1) 10: Voltage swing level 2 (training phase 1) 11: Voltage swing level 3 (training phase 1)

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DPCD_TRAINING_LANE_3_SET (0x742C)

This register reflects the current values set by the transmitter for DPCD register TRAINING_LANE3_SET (0x106). Used by the transmitter during link training to configure the receiver PHY for lane 3.

BIT	7	6	5	4	3	2	1	0
Field	–	–	MAX_PRE_EMPHASIS_REACHED	PRE_EMPHASIS_SET[1:0]		MAX_SWING_REACHED	VOLTAGE_SWING_SET[1:0]	
Reset	–	–	0b0	0b00		0b0	0b00	
Access Type	–	–	Read Only	Read Only		Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_PRE_EMPHASIS_REACHED	5	This is the DPCD value for the current max pre-emphasis reached as set by the DP source (training phase 1).	0: Max preemphasis not reached 1: Max preemphasis reached
PRE_EMPHASIS_SET	4:3	This is the DPCD value for the current preemphasis as set by the DP source (training phase 2).	00: Preemphasis level 0 (training phase 2) 01: Preemphasis level 1 (training phase 2) 10: Preemphasis level 2 (training phase 2) 11: Preemphasis level 3 (training phase 2)
MAX_SWING_REACHED	2	This is the DPCD value for the current max swing reached as set by the DP source (training phase 1).	0: Max swing not reached 1: Max swing reached
VOLTAGE_SWING_SET	1:0	This is the DPCD value for the current voltage swing as set by the DP source (training phase 1).	00: Voltage swing level 0 (training phase 1) 01: Voltage swing level 1 (training phase 1) 10: Voltage swing level 2 (training phase 1) 11: Voltage swing level 3 (training phase 1)

DPCD_DOWNSPREAD_CONTROL (0x7430)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DPCD_DOWNSPREAD_CONTROL
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
DPCD_DOWNSPREAD_CONTROL	0	This register reflects the value of DPCD register MAX_DOWNSPREAD (0x0003).

DPCD_MAIN_LINK_CHANNEL_CODING_SET (0x7434)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DPCD_MAIN_LINK_CHANNEL_CODING_SET
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Read Only

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BITFIELD	BITS	DESCRIPTION
DPCD_MAIN_LINK_CHANNEL_CODING_SET	0	This register reflects the value of DPCD register MAIN_LINK_CHANNEL_CODING (0x0006).

DPCD_SET_POWER_STATE (0x7438)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DPCD_SET_POWER_STATE[2:0]		
Reset	–	–	–	–	–	0b010		
Access Type	–	–	–	–	–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
DPCD_SET_POWER_STATE	2:0	This is the DPCD (0x0600) value for the current power state as set by the DP source device.	001: State D0, normal operation 010: State D3, power down mode 101: Main link to state D3, AUX block fully powered Others: Reserved

DPCD_LANE01_STATUS_B0 (0x743C)

BIT	7	6	5	4	3	2	1	0
Field	–	LANE1_SYMBOL_LOCKED	LANE1_CHANNEL_EQ_DONE	LANE1_CLOCK_RECOVERY_DONE	–	LANE0_SYMBOL_LOCKED	LANE0_CHANNEL_EQ_DONE	LANE0_CLOCK_RECOVERY_DONE
Reset	–	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE1_SYMBOL_LOCKED	6	Lane 1 symbol locked.	0: Symbol lock not achieved 1: Symbol lock achieved
LANE1_CHANNEL_EQ_DONE	5	Lane 1 channel equalization done.	0: Channel equalization not done 1: Channel equalization done
LANE1_CLOCK_RECOVERY_DONE	4	Lane 1 clock recovery done.	0: Clock recovery not done 1: Clock recovery done
LANE0_SYMBOL_LOCKED	2	Lane 0 symbol locked.	0: Symbol lock not achieved 1: Symbol lock achieved
LANE0_CHANNEL_EQ_DONE	1	Lane 0 channel equalization done.	0: Channel equalization not done 1: Channel equalization done
LANE0_CLOCK_RECOVERY_DONE	0	Lane 0 clock recovery done.	0: Clock recovery not done 1: Clock recovery done

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DPCD_LANE01_STATUS_B1 (0x743D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LANE1_LANE_ALIGNED	LANE0_LANE_ALIGNED
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE1_LANE_ALIGNED	1	Lane 1 lane aligned.	0: Lane not aligned 1: Lane aligned
LANE0_LANE_ALIGNED	0	Lane 0 lane aligned.	0: Lane not aligned 1: Lane aligned

DPCD_LANE01_STATUS_B2 (0x743E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LANE1_TRAINING_LOST	LANE0_TRAINING_LOST
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE1_TRAINING_LOST	1	Lane 1 training lost	0: Training not lost 1: Training lost
LANE0_TRAINING_LOST	0	Lane 0 training lost.	0: Training not lost 1: Training lost

DPCD_LANE23_STATUS_B0 (0x7440)

BIT	7	6	5	4	3	2	1	0
Field	–	LANE3_SYMBOL_LOCKED	LANE3_CHANNEL_EQ_DONE	LANE3_CLOCK_RECOVERY_DONE	–	LANE2_SYMBOL_LOCKED	LANE2_CHANNEL_EQ_DONE	LANE2_CLOCK_RECOVERY_DONE
Reset	–	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE3_SYMBOL_LOCKED	6	Lane 3 symbol locked	0: Symbol lock not achieved 1: Symbol lock achieved
LANE3_CHANNEL_EQ_DONE	5	Lane 3 channel equalization done.	0: Channel equalization not done 1: Channel equalization done
LANE3_CLOCK_RECOVERY_DONE	4	Lane 3 clock recovery done.	0: Clock recovery not done 1: Clock recovery done

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BITFIELD	BITS	DESCRIPTION	DECODE
LANE2_SYMBOL_LOCKED	2	Lane 2 symbol locked.	0: Symbol lock not achieved 1: Symbol lock achieved
LANE2_CHANNEL_EQ_DONE	1	Lane 2 channel equalization done.	0: Channel equalization not done 1: Channel equalization done
LANE2_CLOCK_RECOVERY_DONE	0	Lane 2 clock recovery done.	0: Clock recovery not done 1: Clock recovery done

DPCD_LANE23_STATUS_B1 (0x7441)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LANE3_LANE_ALIGNED	LANE2_LANE_ALIGNED
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE3_LANE_ALIGNED	1	Lane 3 lane aligned.	0: Lane not aligned 1: Lane aligned
LANE2_LANE_ALIGNED	0	Lane 2 lane aligned.	0: Lane not aligned 1: Lane aligned

DPCD_LANE23_STATUS_B2 (0x7442)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LANE3_TRAINING_LOST	LANE2_TRAINING_LOST
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LANE3_TRAINING_LOST	1	Lane 3 training lost.	0: Training not lost 1: Training lost
LANE2_TRAINING_LOST	0	Lane 2 training lost.	0: Training not lost 1: Training lost

LANE0_TRAINING_LOST_CAUSE (0x7454)

When each lane of the main link loses training, the cause of the training loss is recorded in this register. Only the register for active lanes on the link are valid. The contents of this register for an unused lane are unpredictable.

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BIT	7	6	5	4	3	2	1	0
Field	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RATE_CHANGE	7	Link bandwidth setting change.	0: No link bandwidth setting change 1: Link bandwidth setting change
TRAINING_PATTERN_3	6	Training pattern 3 active.	0: Training pattern 3 not active 1: Training pattern 3 active
TRAINING_PATTERN_2	5	Training pattern 2 active.	0: Training pattern 2 not active 1: Training pattern 2 active
TRAINING_PATTERN_1	4	Training pattern 1 active.	0: Training pattern 1 not active 1: Training pattern 1 active
CLOCK_RECOVERY_LOST	3	Clock recovery lost.	0: Clock recovery not lost 1: Clock recovery lost
SYMBOL_LOCK_LOST	2	Symbol lock lost	0: Symbol lock not lost 1: Symbol lock lost
ALIGNMENT_LOST	1	Interlane alignment lost.	0: Alignment not lost 1: Alignment lost
LANE_INACTIVE	0	Lane is inactive.	0: Lane not inactive 1: Lane inactive

LANE1_TRAINING_LOST_CAUSE (0x7455)

When each lane of the main link loses training, the cause of the training loss is recorded in this register. Only the register for active lanes on the link are valid. The contents of this register for an unused lane are unpredictable.

BIT	7	6	5	4	3	2	1	0
Field	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RATE_CHANGE	7	Link bandwidth setting change.	0: No link bandwidth setting change 1: Link bandwidth setting change
TRAINING_PATTERN_3	6	Training pattern 3 active.	0: Training pattern 3 not active 1: Training pattern 3 active
TRAINING_PATTERN_2	5	Training pattern 2 active.	0: Training pattern 2 not active 1: Training pattern 2 active
TRAINING_PATTERN_1	4	Training pattern 1 active.	0: Training pattern 1 not active 1: Training pattern 1 active
CLOCK_RECOVERY_LOST	3	Clock recovery lost.	0: Clock recovery not lost 1: Clock recovery lost

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BITFIELD	BITS	DESCRIPTION	DECODE
SYMBOL_LOCK_LOST	2	Symbol lock lost	0: Symbol lock not lost 1: Symbol lock lost
ALIGNMENT_LOST	1	Interlane alignment lost.	0: Alignment not lost 1: Alignment lost
LANE_INACTIVE	0	Lane is inactive.	0: Lane not inactive 1: Lane inactive

LANE2_TRAINING_LOST_CAUSE (0x7456)

When each lane of the main link loses training, the cause of the training loss is recorded in this register. Only the register for active lanes on the link are valid. The contents of this register for an unused lane are unpredictable.

BIT	7	6	5	4	3	2	1	0
Field	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RATE_CHANGE	7	Link bandwidth setting change.	0: No link bandwidth setting change 1: Link bandwidth setting change
TRAINING_PATTERN_3	6	Training pattern 3 active.	0: Training pattern 3 not active 1: Training pattern 3 active
TRAINING_PATTERN_2	5	Training pattern 2 active.	0: Training pattern 2 not active 1: Training pattern 2 active
TRAINING_PATTERN_1	4	Training pattern 1 active.	0: Training pattern 1 not active 1: Training pattern 1 active
CLOCK_RECOVERY_LOST	3	Clock recovery lost.	0: Clock recovery not lost 1: Clock recovery lost
SYMBOL_LOCK_LOST	2	Symbol lock lost	0: Symbol lock not lost 1: Symbol lock lost
ALIGNMENT_LOST	1	Interlane alignment lost.	0: Alignment not lost 1: Alignment lost
LANE_INACTIVE	0	Lane is inactive.	0: Lane not inactive 1: Lane inactive

LANE3_TRAINING_LOST_CAUSE (0x7457)

When each lane of the main link loses training, the cause of the training loss is recorded in this register. Only the register for active lanes on the link are valid. The contents of this register for an unused lane are unpredictable.

BIT	7	6	5	4	3	2	1	0
Field	LINK_RATE_CHANGE	TRAINING_PATTERN_3	TRAINING_PATTERN_2	TRAINING_PATTERN_1	CLOCK_RECOVERY_LOST	SYMBOL_LOCK_LOST	ALIGNMENT_LOST	LANE_INACTIVE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

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BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RATE_CHANGE	7	Link bandwidth setting change.	0: No link bandwidth setting change 1: Link bandwidth setting change
TRAINING_PATTERN_3	6	Training pattern 3 active.	0: Training pattern 3 not active 1: Training pattern 3 active
TRAINING_PATTERN_2	5	Training pattern 2 active.	0: Training pattern 2 not active 1: Training pattern 2 active
TRAINING_PATTERN_1	4	Training pattern 1 active.	0: Training pattern 1 not active 1: Training pattern 1 active
CLOCK_RECOVERY_LOST	3	Clock recovery lost.	0: Clock recovery not lost 1: Clock recovery lost
SYMBOL_LOCK_LOST	2	Symbol lock lost	0: Symbol lock not lost 1: Symbol lock lost
ALIGNMENT_LOST	1	Interlane alignment lost.	0: Alignment not lost 1: Alignment lost
LANE_INACTIVE	0	Lane is inactive.	0: Lane not inactive 1: Lane inactive

I2C_SPEED_CONTROL_SELECT (0x7478)

BIT	7	6	5	4	3	2	1	0
Field	–	–	I2C_SPEED_CAPABILITY[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_SPEED_CAPABILITY	5:0	This is the DPCD (0x0109) value for the current I2C speed control mask as set by the DP source device. Each bit selects an I2C speed available to the DP source. Multiple bits may be set.	000001: 1 Kbps 000010: 5 Kbps 000100: 10 Kbps 001000: 100 Kbps 010000: 400 Kbps 100000: 1 Mbps

MSA_TIMING_IGNORE (0x747C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSA_TIMING_IGNORE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_TIMING_IGNORE	0	This is the DPCD (0x0107, bit7) value for the current MSA timing parameters ignore enable as set by the DP source device.	0: MSA parameters normal 1: MSA parameters are invalid

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EDP_CONFIGURATION_SET (0x7480)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	–	–	–	RSVD	ALT_SR_ENABLE
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type		–	–	–	–	–		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_SR_ENABLE	0	This is the DPCD (0x010A, bit 0) value for the current alternate scrambler reset enable.	0: Alternate scrambler reset (ASSR) disabled 1: Alternate scrambler reset (ASSR) enabled

MST_MODE_CTRL (0x748C)

This is the DPCD (0x0111) value for the current MST mode control as set by the DP source device.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	UPSTREAM_IS_SRC	UP_REQ_EN	MST_EN
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
UPSTREAM_IS_SRC	2	This is the DPCD (0x0111) value for the current MST mode control as set by the DP source device.	0: Upstream device is pre DP v1.2 source or branch device 1: Upstream device is DP source
UP_REQ_EN	1	This is the DPCD (0x0111) value for the current MST mode control as set by the DP source device.	0: UP_REQ message disabled 1: UP_REQ message enabled
MST_EN	0	This is the DPCD (0x0111) value for the current MST mode control as set by the DP source device.	0: SST mode 1: MST mode

DPCD_SER_COUNT_LANE0_B0 (0x7490)

Symbol error count lane 0.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE0_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE0_B0	7:0	Valid symbol error count bits 7-0.

DPCD_SER_COUNT_LANE0_B1 (0x7491)

Symbol error count lane 0.

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BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE0_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE0_B1	7:0	Valid symbol error count bits 15-8.

DPCD_SER_COUNT_LANE1_B0 (0x7494)

Symbol error count lane 1.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE1_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE1_B0	7:0	Valid symbol error count bits 7-0.

DPCD_SER_COUNT_LANE1_B1 (0x7495)

Symbol error count lane 1.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE1_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE1_B1	7:0	Valid symbol error count bits 15-8.

DPCD_SER_COUNT_LANE2_B0 (0x7498)

Symbol error count lane 2.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE2_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE2_B0	7:0	Valid symbol error count bits 7-0.

DPCD_SER_COUNT_LANE2_B1 (0x7499)

Symbol error count lane 2.

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BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE2_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE2_B1	7:0	Valid symbol error count bits 15-8.

DPCD_SER_COUNT_LANE3_B0 (0x749C)

Symbol error count lane 3.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE3_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE3_B0	7:0	Valid symbol error count bits 7-0.

DPCD_SER_COUNT_LANE3_B1 (0x749D)

Symbol error count lane 3.

BIT	7	6	5	4	3	2	1	0
Field	SER_COUNT_LANE3_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SER_COUNT_LANE3_B1	7:0	Valid symbol error count bits 15-8.

MSA_HRES_B0 (0x7500)

Horizontal resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HRES_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HRES_B0	7:0	MSA horizontal resolution bits 7-0.

MSA_HRES_B1 (0x7501)

Horizontal resolution detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	MSA_HRES_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HRES_B1	7:0	MSA horizontal resolution bits 15-8.

MSA_HSPOL (0x7504)

Horizontal sync polarity detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSA_HSPOL
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_HSPOL	0	Main stream attribute horizontal sync polarity.	0: Active high (positive) 1: Active low (negative)

MSA_HSWIDTH_B0 (0x7508)

Horizontal sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HSWIDTH_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HSWIDTH_B0	7:0	MSA horizontal sync width bits 7-0.

MSA_HSWIDTH_B1 (0x7509)

Horizontal sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	–	MSA_HSWIDTH_B1[6:0]						
Reset	–	0b0000000						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
MSA_HSWIDTH_B1	6:0	MSA horizontal sync width bits 14-8.

MSA_HSTART_B0 (0x750C)

Horizontal start detected in the Main Stream Attributes (MSA). Horizontal start is the number of pixels from the leading edge of hsync to start of active data (sync width plus back porch).

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BIT	7	6	5	4	3	2	1	0
Field	MSA_HSTART_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HSTART_B0	7:0	MSA horizontal start bits 7-0.

MSA_HSTART_B1 (0x750D)

Horizontal start detected in the Main Stream Attributes (MSA). Horizontal start is the number of pixels from the leading edge of hsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HSTART_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HSTART_B1	7:0	MSA horizontal start bits 15-8.

MSA_HTOTAL_B0 (0x7510)

Horizontal total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HTOTAL_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HTOTAL_B0	7:0	MSA horizontal total bits 7-0.

MSA_HTOTAL_B1 (0x7511)

Horizontal total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_HTOTAL_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_HTOTAL_B1	7:0	MSA horizontal total bits 15-8.

MSA_VRES_B0 (0x7514)

Vertical resolution detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	MSA_VRES_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VRES_B0	7:0	MSA vertical resolution bits 7-0.

MSA_VRES_B1 (0x7515)

Vertical resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VRES_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VRES_B1	7:0	MSA vertical resolution bits 15-8.

MSA_VSPOL (0x7518)

Vertical sync polarity detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSA_VSPOL
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_VSPOL	0	Main stream attribute vertical sync polarity.	0: Active high (positive) 1: Active low (negative)

MSA_VSWIDTH_B0 (0x751C)

Vertical sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VSWIDTH_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VSWIDTH_B0	7:0	MSA vertical sync width bits 7-0.

MSA_VSWIDTH_B1 (0x751D)

Vertical sync width detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	–	MSA_VSWIDTH_B1[6:0]						
Reset	–	0b0000000						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
MSA_VSWIDTH_B1	6:0	MSA vertical sync width bits 14-8.

MSA_VSTART_B0 (0x7520)

Vertical start detected in the Main Stream Attributes (MSA). Vertical start is the number of lines from the leading edge of vsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VSTART_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VSTART_B0	7:0	MSA vertical start bits 7-0.

MSA_VSTART_B1 (0x7521)

Vertical start detected in the Main Stream Attributes (MSA). Vertical start is the number of lines from the leading edge of vsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VSTART_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VSTART_B1	7:0	MSA vertical start bits 15-8.

MSA_VTOTAL_B0 (0x7524)

Vertical total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_VTOTAL_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VTOTAL_B0	7:0	MSA vertical total bits 7-0.

MSA_VTOTAL_B1 (0x7525)

Vertical total detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	MSA_VTOTAL_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_VTOTAL_B1	7:0	MSA vertical total bits 15-8.

MSA_MISC0 (0x7528)

Miscellaneous 0 attributes detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_COLOR_DEPTH[2:0]			MSA_YCBCR_COLOR	MSA_DYNAMIC_RANGE	MSA_COMP_FORMAT[1:0]		MSA_CLOCKING_MODE
Reset	0b000			0b0	0b0	0b00		0b0
Access Type	Read Only			Read Only	Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_COLOR_DEPTH	7:5	MSA MISC0 color depth.	000: 6 bpc 001: 8 bpc 010: 10 bpc 011: 12 bpc 100: 16 bpc 101-111: Reserved
MSA_YCBCR_COLOR	4	MSA MISC0 YCbCr color.	0: BT601 1: BT709 / special case RGB
MSA_DYNAMIC_RANGE	3	MSA MISC0 dynamic range.	0: VESA range 1: CEA range
MSA_COMP_FORMAT	2:1	MSA MISC0 component format.	00: RGB 01: YCbCr 4:2:2 10: YCbCr 4:4:4 11: RGB wide gamut
MSA_CLOCKING_MODE	0	MSA MISC0 clocking mode.	0: Synchronous mode 1: Asynchronous mode

MSA_MISC1 (0x752C)

Miscellaneous 1 attributes detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_Y_ONLY	–	–	–	–	MSA_STEREO_VIDEO[1:0]		MSA_INTERLACED_EVEN
Reset	0b0	–	–	–	–	0b00		0b0
Access Type	Read Only	–	–	–	–	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_Y_ONLY	7	MSA MISC1 Y-only control.	0: Full color 1: Y-only

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BITFIELD	BITS	DESCRIPTION	DECODE
MSA_STEREO_VIDEO	2:1	MSA MISC1 stereo video.	00: No inband 3D stereo 01: Next frame is RIGHT EYE (progressive video) 10: Reserved 11: Next frame is LEFT EYE (progressive video)
MSA_INTERLACED_EVEN	0	MSA MISC1 interlace.	0: Inerlaced lines per frame is odd 1: Interlaced lines per frame is even

MSA_MVID_B0 (0x7530)

Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_MVID_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_MVID_B0	7:0	MSA Mvid bits 7-0.

MSA_MVID_B1 (0x7531)

Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_MVID_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_MVID_B1	7:0	MSA Mvid bits 15-8.

MSA_MVID_B2 (0x7532)

Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_MVID_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_MVID_B2	7:0	MSA Mvid bits 23-16.

MSA_NVID_B0 (0x7534)

Nvid detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	MSA_NVID_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_NVID_B0	7:0	MSA Nvid bits 7-0.

MSA_NVID_B1 (0x7535)

Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_NVID_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_NVID_B1	7:0	MSA Nvid bits 15-8.

MSA_NVID_B2 (0x7536)

Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	MSA_NVID_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MSA_NVID_B2	7:0	MSA Nvid bits 23-16.

MSA_VBID (0x7538)

VB-ID value most recently received through main link.

BIT	7	6	5	4	3	2	1	0
Field	–	MSA_VBID_COMPRESSED_STREAM	MSA_VBID_HDCP_SYNC_DET	MSA_VBID_AUDIO_MUTE	MSA_VBID_NO_VIDEO	MSA_VBID_INTERLACED	MSA_VBID_FIELD_ID	MSA_VBID_VERT_BLANK
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_VBID_COMPRESSED_STREAM	6	MSA VB-ID compressed stream flag.	0: Video stream is not DSC compressed 1: Video stream is DSC compressed

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BITFIELD	BITS	DESCRIPTION	DECODE
MSA_VBID_HDCP_SYNC_DET	5	MSA VB-ID HDCP sync detect.	0: HDCP sync not detected 1: HDCP sync detected
MSA_VBID_AUDIO_MUTE	4	MSA VB-ID audio mute flag.	0: Audio stream is not muted (acitve) 1: Audio stream is muted
MSA_VBID_NO_VIDEO	3	MSA VB-ID no video stream flag.	0: Video stream does not exist 1: Video stream exists
MSA_VBID_INTERLACED	2	MSA VB-ID interlaced flag.	0: Progressive video 1: Interlaced video
MSA_VBID_FIELD_ID	1	MSA VB-ID field ID flag.	0: Bottom field (interlaced video) or progressive video 1: Top field (interlaced video)
MSA_VBID_VERT_BLANK	0	MSA VB-ID vertical blanking flag.	0: Vertical blank not active 1: Vertical blank active

MSA_VIRTUAL_SINK_SELECT (0x7540)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MSA_VIRTUAL_SINK_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_VIRTUAL_SINK_SELECT	1:0	Selects the virtual sink device for MSA value reporting.	00: Virtual sink 0 01: Virtual sink 1 10: Virtual sink 2 11: Virtual sink 3

MSA_DSC_TS_SELECT (0x7541)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSA_DSC_TS_SELECT
Reset	–	–	–	–	–	–	–	0b00
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_DSC_TS_SELECT	0	Selects the video timestamp (Mvid and Nvid) that is read from MSA_MVID and MSA_NVID registers when DSC is active. When DSC is not active there is no difference between the selections.	0: DSC modified timestamp 1: Original MSA timestamp

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MSA_UPDATE (0x7543)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VS1_MODE_UPDATE	VS0_MODE_UPDATE
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VS1_MODE_UPDATE	1	Video mode update status for stream 1. This sticky status indicates that MSA parameters have been updated. Write 1 to clear the status allowing it to be set on the next update.	0: Awaiting VS1 MSA parameter update 1: VS1 MSA parameters updated
VS0_MODE_UPDATE	0	Video mode update status for stream 0. This sticky status indicates that MSA parameters have been updated. Write 1 to clear the status allowing it to be set on the next update.	0: Awaiting VS0 MSA parameter update 1: VS0 MSA parameters updated

VS0_MSA_HTOTAL_B0 (0x7544)

Virtual sink 0 horizontal total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HTOTAL_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HTOTAL_B0	7:0	Virtual sink 0 MSA horizontal total bits 7-0.

VS0_MSA_HTOTAL_B1 (0x7545)

Virtual sink 0 horizontal total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HTOTAL_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HTOTAL_B1	7:0	Virtual sink 0 MSA horizontal total bits 15-8.

VS0_MSA_HRES_B0 (0x7546)

Virtual sink 0 horizontal resolution detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HRES_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HRES_B0	7:0	Virtual sink 0 MSA horizontal resolution bits 7-0.

VS0_MSA_HRES_B1 (0x7547)

Virtual sink 0 horizontal resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HRES_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HRES_B1	7:0	Virtual sink 0 MSA horizontal resolution bits 15-8.

VS0_MSA_HSTART_B0 (0x7548)

Virtual sink 0 horizontal start detected in the Main Stream Attributes (MSA). Horizontal start is the number of pixels from the leading edge of hsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HSTART_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HSTART_B0	7:0	Virtual sink 0 MSA horizontal start bits 7-0.

VS0_MSA_HSTART_B1 (0x7549)

Virtual sink 0 horizontal start detected in the Main Stream Attributes (MSA). Horizontal start is the number of pixels from the leading edge of hsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HSTART_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HSTART_B1	7:0	Virtual sink 0 MSA horizontal start bits 15-8.

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VS0_MSA_HSWIDTH_B0 (0x754A)

Virtual sink 0 horizontal sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HSWIDTH_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HSWIDTH_B0	7:0	Virtual sink 0 MSA horizontal sync width bits 7-0.

VS0_MSA_HSWIDTH_B1 (0x754B)

Virtual sink 0 horizontal sync width and sync polarity detected in the Main Stream Attributes (MSA),

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HSPOL	VS0_MSA_HSWIDTH_B1[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
VS0_MSA_HSPOL	7	Virtual sink 0 main stream attribute horizontal sync polarity.	0: Active high (positive) 1: Active low (negative)
VS0_MSA_HSWIDTH_B1	6:0	Virtual sink 0 MSA horizontal sync width bits 14-8.	

VS0_MSA_VTOTAL_B0 (0x754C)

Virtual sink 0 vertical total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_VTOTAL_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_VTOTAL_B0	7:0	Virtual sink 0 MSA vertical total bits 7-0.

VS0_MSA_VTOTAL_B1 (0x754D)

Virtual sink 0 vertical total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_VTOTAL_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
VS0_MSA_VTOTAL_B1	7:0	Virtual sink 0 MSA vertical total bits 15-8.

VS0_MSA_VRES_B0 (0x754E)

Virtual sink 0 vertical resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_VRES_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_VRES_B0	7:0	Virtual sink 0 MSA vertical resolution bits 7-0.

VS0_MSA_VRES_B1 (0x754F)

Virtual sink 0 vertical resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_VRES_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_VRES_B1	7:0	Virtual sink 0 MSA vertical resolution bits 15-8.

VS0_MSA_VSTART_B0 (0x7550)

Virtual sink 0 vertical start detected in the Main Stream Attributes (MSA). Vertical start is the number of lines from the leading edge of vsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_VSTART_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_VSTART_B0	7:0	Virtual sink 0 MSA vertical start bits 7-0.

VS0_MSA_VSTART_B1 (0x7551)

Virtual sink 0 vertical start detected in the Main Stream Attributes (MSA). Vertical start is the number of lines from the leading edge of vsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_VSTART_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
VS0_MSA_VSTART_B1	7:0	Virtual sink 0 MSA vertical start bits 15-8.

VS0_MSA_VSWIDTH_B0 (0x7552)

Virtual sink 0 vertical sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_VSWIDTH_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_VSWIDTH_B0	7:0	Virtual sink 0 MSA vertical sync width bits 7-0.

VS0_MSA_VSWIDTH_B1 (0x7553)

Virtual sink 0 vertical sync width and sync polarity detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_VSPOL	VS0_MSA_VSWIDTH_B1[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
VS0_MSA_VSPOL	7	Virtual sink 0 main stream attribute vertical sync polarity.	0: Active high (positive) 1: Active low (negative)
VS0_MSA_VSWIDTH_B1	6:0	Virtual sink 0 MSA vertical sync width bits 14-8.	

VS0_MSA_MISC0 (0x7554)

Virtual sink 0 miscellaneous 0 attributes detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_COLOR_DEPTH[2:0]			VS0_MSA_YCBCR_COLOR	VS0_MSA_DYNAMIC_RANGE	VS0_MSA_COMP_FORMAT[1:0]		VS0_MSA_CLOCKING_MODE
Reset	0b000			0b0	0b0	0b00		0b0
Access Type	Read Only			Read Only	Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS0_MSA_COLOR_DEPTH	7:5	Virtual sink 0 MSA MISC0 color depth.	000: 6 bpc 001: 8 bpc 010: 10 bpc 011: 12 bpc 100: 16 bpc 101-111: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
VS0_MSA_YCBCR_COLOR	4	Virtual sink 0 MSA MISC0 YCbCr color.	0: BT601 1: BT709 / special case RGB
VS0_MSA_DYNAMIC_RANGE	3	Virtual sink 0 MSA MISC0 dynamic range.	0: VESA range 1: CEA range
VS0_MSA_COMP_FORMAT	2:1	Virtual sink 0 MSA MISC0 component format.	00: RGB 01: YCbCr 4:2:2 10: YCbCr 4:4:4 11: RGB wide gamut
VS0_MSA_CLOCKING_MODE	0	Virtual sink 0 MSA MISC0 clocking mode.	0: Synchronous mode 1: Asynchronous mode

VS0_MSA_MISC1 (0x7555)

Virtual sink 0 miscellaneous 1 attributes detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_Y_ONLY	–	–	–	–	VS0_MSA_STEREO_VIDEO[1:0]		VS0_MSA_INTERLACED_EVEN
Reset	0b0	–	–	–	–	0b00		0b0
Access Type	Read Only	–	–	–	–	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS0_MSA_Y_ONLY	7	Virtual sink 0 MSA MISC1 Y-only control.	0: Full color 1: Y-only
VS0_MSA_STEREO_VIDEO	2:1	Virtual sink 0 MSA MISC1 stereo video.	00: No inband 3D stereo 01: Next frame is RIGHT EYE (progressive video) 10: Reserved 11: Next frame is LEFT EYE (progressive video)
VS0_MSA_INTERLACED_EVEN	0	Virtual sink 0 MSA MISC1 interlace.	0: Inerlaced lines per frame is odd 1: Interlaced lines per frame is even

VS0_VBID (0x7556)

Virtual sink 0 VB-ID value most recently received through main link.

BIT	7	6	5	4	3	2	1	0
Field	–	VS0_VBID_COMPRESSED_STREAM	VS0_VBID_HDCP_SYNC_DET	VS0_VBID_AUDIO_MUTE	VS0_VBID_NO_VIDEO	VS0_VBID_INTERLACED	VS0_VBID_FIELD_ID	VS0_VBID_VERT_BLANK
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS0_VBID_COMPRESSED_STREAM	6	Virtual sink 0 VB-ID compressed stream (DSC) flag.	0: Video stream is not DSC compressed 1: Video stream is DSC compressed

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BITFIELD	BITS	DESCRIPTION	DECODE
VS0_VBID_HDCP_SYNC_DET	5	Virtual sink 0 VB-ID HDCP sync detect.	0: HDCP sync not detected 1: HDCP sync detected
VS0_VBID_AUDIO_MUTE	4	Virtual sink 0 VB-ID audio mute flag.	0: Audio stream is not muted (acitve) 1: Audio stream is muted
VS0_VBID_NO_VIDEO	3	Virtual sink 0 VB-ID no video stream flag.	0: Video stream does not exist 1: Video stream exists
VS0_VBID_INTERLACED	2	Virtual sink 0 VB-ID interlaced flag.	0: Progressive video 1: Interlaced video
VS0_VBID_FIELD_ID	1	Virtual sink 0 VB-ID field ID flag.	0: Bottom field (interlaced video) or progressive video 1: Top field (interlaced video)
VS0_VBID_VERT_BLANK	0	Virtual sink 0 VB-ID vertical blanking flag.	0: Vertical blank not active 1: Vertical blank active

VS0_MSA_MVID_B0 (0x7558)

Virtual sink 0 Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_MVID_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_MVID_B0	7:0	Virtual sink 0 MSA Mvid bits 7-0.

VS0_MSA_MVID_B1 (0x7559)

Virtual sink 0 Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_MVID_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_MVID_B1	7:0	Virtual sink 0 MSA Mvid bits 15-8.

VS0_MSA_MVID_B2 (0x755A)

Virtual sink 0 Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_MVID_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_MVID_B2	7:0	Virtual sink 0 MSA Mvid bits 23-16.

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VS0_MSA_NVID_B0 (0x755C)

Virtual sink 0 Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_NVID_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_NVID_B0	7:0	Virtual sink 0 MSA Nvid bits 7-0.

VS0_MSA_NVID_B1 (0x755D)

Virtual sink 0 Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_NVID_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_NVID_B1	7:0	Virtual sink 0 MSA Nvid bits 15-8.

VS0_MSA_NVID_B2 (0x755E)

Virtual sink 0 Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_NVID_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_NVID_B2	7:0	Virtual sink 0 MSA Nvid bits 23-16.

VS0_MSA_HRES_DSC_B0 (0x7560)

Virtual sink 0 horizontal resolution modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HRES_DSC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HRES_DSC_B0	7:0	Virtual sink 0 MSA horizontal resolution modified for DSC GMSL formatting when DSC is active bits 7-0.

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VS0_MSA_HRES_DSC_B1 (0x7561)

Virtual sink 0 horizontal resolution modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_HRES_DSC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_HRES_DSC_B1	7:0	Virtual sink 0 MSA horizontal resolution modified for DSC GMSL formatting when DSC is active bits 15-8.

VS0_MSA_MVID_DSC_B0 (0x7564)

Virtual sink 0 Mvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_MVID_DSC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_MVID_DSC_B0	7:0	Virtual sink 0 MSA Mvid modified for DSC GMSL formatting when DSC is active bits 7-0.

VS0_MSA_MVID_DSC_B1 (0x7565)

Virtual sink 0 Mvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_MVID_DSC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_MVID_DSC_B1	7:0	Virtual sink 0 MSA Mvid modified for DSC GMSL formatting when DSC is active bits 15-8.

VS0_MSA_MVID_DSC_B2 (0x7566)

Virtual sink 0 Mvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_MVID_DSC_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
VS0_MSA_MVID_DSC_B2	7:0	Virtual sink 0 MSA Mvid modified for DSC GMSL formatting when DSC is active bits 23-16.

VS0_MSA_NVID_DSC_B0 (0x7568)

Virtual sink 0 Nvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_NVID_DSC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_NVID_DSC_B0	7:0	Virtual sink 0 MSA Nvid modified for DSC GMSL formatting when DSC is active bits 7-0.

VS0_MSA_NVID_DSC_B1 (0x7569)

Virtual sink 0 Nvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_NVID_DSC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_NVID_DSC_B1	7:0	Virtual sink 0 MSA Nvid modified for DSC GMSL formatting when DSC is active bits 15-8.

VS0_MSA_NVID_DSC_B2 (0x756A)

Virtual sink 0 Nvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS0_MSA_NVID_DSC_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS0_MSA_NVID_DSC_B2	7:0	Virtual sink 0 MSA Nvid modified for DSC GMSL formatting when DSC is active bits 23-16.

VS1_MSA_HTOTAL_B0 (0x7574)

Virtual sink 1 horizontal total detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HTOTAL_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HTOTAL_B0	7:0	Virtual sink 1 MSA horizontal total bits 7-0.

VS1_MSA_HTOTAL_B1 (0x7575)

Virtual sink 1 horizontal total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HTOTAL_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HTOTAL_B1	7:0	Virtual sink 1 MSA horizontal total bits 15-8.

VS1_MSA_HRES_B0 (0x7576)

Virtual sink 1 horizontal resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HRES_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HRES_B0	7:0	Virtual sink 1 MSA horizontal resolution bits 7-0.

VS1_MSA_HRES_B1 (0x7577)

Virtual sink 1 horizontal resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HRES_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HRES_B1	7:0	Virtual sink 1 MSA horizontal resolution bits 15-8.

VS1_MSA_HSTART_B0 (0x7578)

Virtual sink 1 horizontal start detected in the Main Stream Attributes (MSA). Horizontal start is the number of pixels from the leading edge of hsync to start of active data (sync width plus back porch).

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BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HSTART_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HSTART_B0	7:0	Virtual sink 1 MSA horizontal start bits 7-0.

VS1_MSA_HSTART_B1 (0x7579)

Virtual sink 1 horizontal start detected in the Main Stream Attributes (MSA). Horizontal start is the number of pixels from the leading edge of hsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HSTART_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HSTART_B1	7:0	Virtual sink 1 MSA horizontal start bits 15-8.

VS1_MSA_HSWIDTH_B0 (0x757A)

Virtual sink 1 horizontal sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HSWIDTH_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HSWIDTH_B0	7:0	Virtual sink 1 MSA horizontal sync width bits 7-0.

VS1_MSA_HSWIDTH_B1 (0x757B)

Virtual sink 1 horizontal sync width and sync polarity detected in the Main Stream Attributes (MSA),

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HSPOL	VS1_MSA_HSWIDTH_B1[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
VS1_MSA_HSPOL	7	Virtual sink 1 main stream attribute horizontal sync polarity.	0: Active high (positive) 1: Active low (negative)
VS1_MSA_HSWIDTH_B1	6:0	Virtual sink 1 MSA horizontal sync width bits 14-8.	

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VS1_MSA_VTOTAL_B0 (0x757C)

Virtual sink 1 vertical total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_VTOTAL_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_VTOTAL_B0	7:0	Virtual sink 1 MSA vertical total bits 7-0.

VS1_MSA_VTOTAL_B1 (0x757D)

Virtual sink 1 vertical total detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_VTOTAL_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_VTOTAL_B1	7:0	Virtual sink 1 MSA vertical total bits 15-8.

VS1_MSA_VRES_B0 (0x757E)

Virtual sink 1 vertical resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_VRES_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_VRES_B0	7:0	Virtual sink 1 MSA vertical resolution bits 7-0.

VS1_MSA_VRES_B1 (0x757F)

Virtual sink 1 vertical resolution detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_VRES_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_VRES_B1	7:0	Virtual sink 1 MSA vertical resolution bits 15-8.

VS1_MSA_VSTART_B0 (0x7580)

Virtual sink 1 vertical start detected in the Main Stream Attributes (MSA). Vertical start is the number of lines from the

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leading edge of vsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_VSTART_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_VSTART_B0	7:0	Virtual sink 1 MSA vertical start bits 7-0.

VS1_MSA_VSTART_B1 (0x7581)

Virtual sink 1 vertical start detected in the Main Stream Attributes (MSA). Vertical start is the number of lines from the leading edge of vsync to start of active data (sync width plus back porch).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_VSTART_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_VSTART_B1	7:0	Virtual sink 1 MSA vertical start bits 15-8.

VS1_MSA_VSWIDTH_B0 (0x7582)

Virtual sink 1 vertical sync width detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_VSWIDTH_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_VSWIDTH_B0	7:0	Virtual sink 1 MSA vertical sync width bits 7-0.

VS1_MSA_VSWIDTH_B1 (0x7583)

Virtual sink 1 vertical sync width and sync polarity detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_VSPOL	VS1_MSA_VSWIDTH_B1[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
VS1_MSA_VSPOL	7	Virtual sink 1 main stream attribute vertical sync polarity.	0: Active high (positive) 1: Active low (negative)

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BITFIELD	BITS	DESCRIPTION	DECODE
VS1_MSA_VSWIDTH_B1	6:0	Virtual sink 1 MSA vertical sync width bits 14-8.	

VS1_MSA_MISC0 (0x7584)

Virtual sink 1 miscellaneous 0 attributes detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_COLOR_DEPTH[2:0]			VS1_MSA_YCBCR_COLOR	VS1_MSA_DYNAMIC_RANGE	VS1_MSA_COMP_FORMAT[1:0]		VS1_MSA_CLOCKING_MODE
Reset	0b000			0b0	0b0	0b00		0b0
Access Type	Read Only			Read Only	Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS1_MSA_COLOR_DEPTH	7:5	Virtual sink 1 MSA MISC0 color depth.	000: 6 bpc 001: 8 bpc 010: 10 bpc 011: 12 bpc 100: 16 bpc 101-111: Reserved
VS1_MSA_YCBCR_COLOR	4	Virtual sink 1 MSA MISC0 YCbCr color.	0: BT601 1: BT709 / special case RGB
VS1_MSA_DYNAMIC_RANGE	3	Virtual sink 1 MSA MISC0 dynamic range.	0: VESA range 1: CEA range
VS1_MSA_COMP_FORMAT	2:1	Virtual sink 1 MSA MISC0 component format.	00: RGB 01: YCbCr 4:2:2 10: YCbCr 4:4:4 11: RGB wide gamut
VS1_MSA_CLOCKING_MODE	0	Virtual sink 1 MSA MISC0 clocking mode.	0: Synchronous mode 1: Asynchronous mode

VS1_MSA_MISC1 (0x7585)

Virtual sink 1 miscellaneous 1 attributes detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_Y_ONLY	–	–	–	–	VS1_MSA_STEREO_VIDEO[1:0]		VS1_MSA_INTERLACED_EVEN
Reset	0b0	–	–	–	–	0b00		0b0
Access Type	Read Only	–	–	–	–	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS1_MSA_Y_ONLY	7	Virtual sink 1 MSA MISC1 Y-only control.	0: Full color 1: Y-only

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BITFIELD	BITS	DESCRIPTION	DECODE
VS1_MSA_STEREO_VIDEO	2:1	Virtual sink 1 MSA MISC1 stereo video.	00: No inband 3D stereo 01: Next frame is RIGHT EYE (progressive video) 10: Reserved 11: Next frame is LEFT EYE (progressive video)
VS1_MSA_INTERLACED_EVEN	0	Virtual sink 1 MSA MISC1 interlace.	0: Inerlaced lines per frame is odd 1: Interlaced lines per frame is even

VS1_VBID (0x7586)

Virtual sink 1 VB-ID value most recently received through main link.

BIT	7	6	5	4	3	2	1	0
Field	–	VS1_VBID_COMPRESSED_STREAM	VS1_VBID_HDCP_SYNC_DET	VS1_VBID_AUDIO_MUTE	VS1_VBID_NO_VIDEO	VS1_VBID_INTERLACED	VS1_VBID_FIELD_ID	VS1_VBID_VERT_BLANK
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS1_VBID_COMPRESSED_STREAM	6	Virtual sink 1 VB-ID compressed stream (DSC) flag.	0: Video stream is not DSC compressed 1: Video stream is DSC compressed
VS1_VBID_HDCP_SYNC_DET	5	Virtual sink 1 VB-ID HDCP sync detect.	0: HDCP sync not detected 1: HDCP sync detected
VS1_VBID_AUDIO_MUTE	4	Virtual sink 1 VB-ID audio mute flag.	0: Audio stream is not muted (acitve) 1: Audio stream is muted
VS1_VBID_NO_VIDEO	3	Virtual sink 1 VB-ID no video stream flag.	0: Video stream does not exist 1: Video stream exists
VS1_VBID_INTERLACED	2	Virtual sink 1 VB-ID interlaced flag.	0: Progressive video 1: Interlaced video
VS1_VBID_FIELD_ID	1	Virtual sink 1 VB-ID field ID flag.	0: Bottom field (interlaced video) or progressive video 1: Top field (interlaced video)
VS1_VBID_VERT_BLANK	0	Virtual sink 1 VB-ID vertical blanking flag.	0: Vertical blank not active 1: Vertical blank active

VS1_MSA_MVID_B0 (0x7588)

Virtual sink 1 Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_MVID_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_MVID_B0	7:0	Virtual sink 1 MSA Mvid bits 7-0.

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VS1_MSA_MVID_B1 (0x7589)

Virtual sink 1 Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_MVID_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_MVID_B1	7:0	Virtual sink 1 MSA Mvid bits 15-8.

VS1_MSA_MVID_B2 (0x758A)

Virtual sink 1 Mvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_MVID_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_MVID_B2	7:0	Virtual sink 1 MSA Mvid bits 23-16.

VS1_MSA_NVID_B0 (0x758C)

Virtual sink 1 Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_NVID_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_NVID_B0	7:0	Virtual sink 1 MSA Nvid bits 7-0.

VS1_MSA_NVID_B1 (0x758D)

Virtual sink 1 Nvid detected in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_NVID_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_NVID_B1	7:0	Virtual sink 1 MSA Nvid bits 15-8.

VS1_MSA_NVID_B2 (0x758E)

Virtual sink 1 Nvid detected in the Main Stream Attributes (MSA).

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BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_NVID_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_NVID_B2	7:0	Virtual sink 1 MSA Nvid bits 23-16.

VS1_MSA_HRES_DSC_B0 (0x7590)

Virtual sink 1 horizontal resolution modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HRES_DSC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HRES_DSC_B0	7:0	Virtual sink 1 MSA horizontal resolution modified for DSC GMSL formatting when DSC is active bits 7-0.

VS1_MSA_HRES_DSC_B1 (0x7591)

Virtual sink 1 horizontal resolution modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_HRES_DSC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_HRES_DSC_B1	7:0	Virtual sink 1 MSA horizontal resolution modified for DSC GMSL formatting when DSC is active bits 15-8.

VS1_MSA_MVID_DSC_B0 (0x7594)

Virtual sink 1 Mvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_MVID_DSC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_MVID_DSC_B0	7:0	Virtual sink 1 MSA Mvid modified for DSC GMSL formatting when DSC is active bits 7-0.

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VS1_MSA_MVID_DSC_B1 (0x7595)

Virtual sink 1 Mvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_MVID_DSC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_MVID_DSC_B1	7:0	Virtual sink 1 MSA Mvid modified for DSC GMSL formatting when DSC is active bits 15-8.

VS1_MSA_MVID_DSC_B2 (0x7596)

Virtual sink 1 Mvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_MVID_DSC_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_MVID_DSC_B2	7:0	Virtual sink 1 MSA Mvid modified for DSC GMSL formatting when DSC is active bits 23-16.

VS1_MSA_NVID_DSC_B0 (0x7598)

Virtual sink 1 Nvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_NVID_DSC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_NVID_DSC_B0	7:0	Virtual sink 1 MSA Nvid modified for DSC GMSL formatting when DSC is active bits 7-0.

VS1_MSA_NVID_DSC_B1 (0x7599)

Virtual sink 1 Nvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_NVID_DSC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

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BITFIELD	BITS	DESCRIPTION
VS1_MSA_NVID_DSC_B1	7:0	Virtual sink 1 MSA Nvid modified for DSC GMSL formatting when DSC is active bits 15-8.

VS1_MSA_NVID_DSC_B2 (0x759A)

Virtual sink 1 Nvid detected modified for DSC GMSL formatting when DSC is active in the Main Stream Attributes (MSA).

BIT	7	6	5	4	3	2	1	0
Field	VS1_MSA_NVID_DSC_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VS1_MSA_NVID_DSC_B2	7:0	Virtual sink 1 MSA Nvid modified for DSC GMSL formatting when DSC is active bits 23-16.

HCDP_ENABLE (0x7600)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HDCP_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_ENABLE	0	HDCP hardware control status. This is automatically controlled by the authentication process.	0: HDCP control not enabled 1: HDCP control enabled

HCDP_AUTO_ENCRYPT (0x7602)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	HDCP_AUTO_ENCRYPT	–	–
Reset	–	–	–	–	–	0b1	–	–
Access Type	–	–	–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_AUTO_ENCRYPT	2	HDCP auto encryption allows the HDCP-1 stream encryption to be dynamically enabled and disabled.	0: HDCP auto encryption enable/disable is OFF 1: HDCP auto encryption enable/disable is OFF

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HCDP_MODE_SELECT (0x7604)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	HDCP_MODE_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_MODE_SELECT	1:0	HDCP mode select (HDCP-1 or HDCP-2). This is automatically controlled by the authentication process.	0: Invalid, mode not set 1: HDCP-1 2: HDCP-2

HDCP_STREAM_CIPHER_ENABLE (0x7654)

Stream cipher (decryption) control.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HDCP_STREAM_CIPHER_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_STREAM_CIPHER_ENABLE	0	Enables decryption of the main link stream. This is automatically controlled by the authentication process.	0: HDCP stream decryption disabled 1: HDCP stream decryption enabled

HDCP_DECRYPT_STATUS (0x7690)

Current decryption status.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	HDCP_DECRYPT_READY	HDCP_DECRYPT_ACTIVE
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_DECRYPT_READY	1	HDCP decryption ready status. This indicates that decryption is ready to be active.	0: Decryption not ready 1: Decryption ready
HDCP_DECRYPT_ACTIVE	0	HDCP decryption active status	0: Decryption not active 1: Decryption active

HDCP_LINK_INTEGRITY (0x7694)

Link integrity check status.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HDCP_LINK_INTEGRITY_FAIL
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_LINK_INTEGRITY_FAIL	0	HDCP link integrity check failure.	0: Link integrity check normal 1: Link integrity check failure

MST_SST_PORT_SELECT (0x7900)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MST_SST_PORT_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MST_SST_PORT_SELECT	1:0	Selects one of the user data output ports that will receive active symbols when configured for SST mode. This register is unused when configured for MST mode.	00: Video out port 0 01: Video out port 1 10: Video out port 2 (unused) 11: Video out port 3 (unused)

DSC_DPCD_SELECT (0x7901)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DSC_DPCD_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_DPCD_SELECT	1:0	Selects the sink that provides DSC configuration/control/status information for access through the default DPCD registers for DSC.	00: DSC sink 0 01: DSC sink 1 10: DSC sink 2 (unused) 11: DSC sink 3 (unused)

CRC_DPCD_SELECT (0x7902)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	CRC_DPCD_SELECT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

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BITFIELD	BITS	DESCRIPTION	DECODE
CRC_DPCD_SELECT	1:0	Selects the sink that provides CRC configuration/control/status information for access through the default DPCD registers for CRC.	00: Sink 0 01: Sink 1 10: Sink 2 (unused) 11: Sink 3 (unused)

MST_PAYLOAD_ID_0 (0x7904)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_PAYLOAD_ID_0[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
MST_PAYLOAD_ID_0	6:0	Sets the MST payload ID of the video stream for video output port 0.

MST_PAYLOAD_ID_1 (0x7908)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_PAYLOAD_ID_1[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
MST_PAYLOAD_ID_1	6:0	Sets the MST payload ID of the video stream for video output port 1.

MST_PAYLOAD_ID_2 (0x790C)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_PAYLOAD_ID_2[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
MST_PAYLOAD_ID_2	6:0	Sets the MST payload ID of the video stream for video output port 2.

MST_PAYLOAD_ID_3 (0x7910)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_PAYLOAD_ID_3[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
MST_PAYLOAD_ID_3	6:0	Sets the MST payload ID of the video stream for video output port 3.

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MST_CLEAR_PAYLOAD_ID_TABLE (0x7934)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MST_CLEAR_PAYLOAD_ID_TABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
MST_CLEAR_PAYLOAD_ID_TABLE	0	Clears MST payload table. Normally the payload allocation table is managed by the DP source through the AUX channal. This bit is self-clearing.	0: Normal operation 1: Clear payload allocation table

MST_VS0_ENABLE (0x7A00)

Enables the functionality for virtual sink 0. This sink device is associated with video output port 0. This is the only output sink/port in SST mode.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VS_ENABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VS_ENABLE	0	Enables the MST virtual sink device 0. This also enables the single sink device for SST mode. When disabled, video operations for this virtual sink remain in the idle state.	0: Virtual sink disabled 1: Virtual sink enabled

MST_VS0_USER_PIXEL_WIDTH (0x7A04)

Controls output data path width in pixels for the associated video output port.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	USER_PIXEL_WIDTH[2:0]		
Reset	–	–	–	–	–	0b001		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
USER_PIXEL_WIDTH	2:0	Sets the video output data path width in pixels per clock. Set to 1 for single pixel wide output and 2 for dual pixel wide output. All other values are reserved and should not be used. This should be set before any video is received.

MST_VS0_SWAP_CBCR (0x7A08)

Controls swapping of color values for the associated video output port.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CRC_MASK_SWAP	CRC_COMP_SWAP	PIX_MASK_SWAP	SWAP_CBCR
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_MASK_SWAP	3	Swap the pixel mask Cb (blue) and Cr (red) values for pixels used for CRC calculation.	0: No swap 1: Swap Cb and Cr
CRC_COMP_SWAP	2	Swap the pixel component Cb (blue) and Cr (red) values for pixels used for CRC calculation.	0: No swap 1: Swap Cb and Cr
PIX_MASK_SWAP	1	Swap the pixel mask Cb (blue) and Cr (red) values for pixels on the video output port for cases where the last pixel set contains extra pixels (user width > 1, DSC).	0: No swap 1: Swap Cb and Cr
SWAP_CBCR	0	Swap the Cb (blue) and Cr (red) values for pixels on the video output port when set for YCbCr color space.	0: No swap 1: Swap Cb and Cr

MST_VS0_USER_FIFO_RESET (0x7A0C)

BIT	7	6	5	4	3	2	1	0
Field	DISABLE_VB_FAULT_RESET	VB_FRAME_RESET_PEND_SEL	BS_FRAME_RESET_SEL	DISABLE_FRAME_RESET	–	DISABLE_LINE_RESET_FIFO	DISABLE_HS_LINE_RESET	DISABLE_LINE_RESET
Reset	0b0	0b0	0b0	0b0	–	0b0	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DISABLE_VB_FAULT_RESET	7	Disables the vertical blank fault detect reset. This reset occurs when the internal state indicates an active line while the incoming video indicates vertical blanking. This is for debug purposes only and should normally be set to 0.	0: Normal operation - vertical blank fault reset enabled 1: Vertical blank fault reset disabled
VB_FRAME_RESET_PEND_SEL	6	Selects vertical blank start to set reset pending for resetting of video FIFOs after each frame of received video data. This is for debug purposes only and should normally be set to 0.	0: Frame reset pending set by vsync 1: Frame reset pending set by vertical blank start
BS_FRAME_RESET_SEL	5	Selects BS symbol for resetting of video FIFOs after each frame of received video data. This is for debug purposes only and should normally be set to 0.	0: Frame reset at vsync 1: Frame reset at next BS after last line BS
DISABLE_FRAME_RESET	4	Disables normal resetting of video FIFOs after each frame of received video data. This is for debug purposes only and should normally be set to 0.	0: Normal operation - frame reset enabled 1: Frame reset disabled

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BITFIELD	BITS	DESCRIPTION	DECODE
DISABLE_LINE_RESET_FIFO	2	Disables normal resetting of video clock crossing FIFO after each line of received video data. This is for debug purposes only and should normally be set to 0.	0: Normal operation - line reset for clock crossing FIFO enabled 1: Line reset for clock crossing FIFO disabled
DISABLE_HS_LINE_RESET	1	Disables normal hsync resetting of video FIFOs after each line of received video data. This is for debug purposes only and should normally be set to 0.	0: Normal operation - line hsync reset enabled 1: Line hsync reset disabled
DISABLE_LINE_RESET	0	Disables normal resetting of video FIFOs after each line of received video data. This is for debug purposes only and should normally be set to 0.	0: Normal operation - line reset enabled 1: Line reset disabled

MST_VS0_VIDEO_FIFO_OVERFLOW (0x7A10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VIDEO_FIFO_OVERFLOW
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_FIFO_OVERFLOW	0	Indicates that the internal user data FIFO in the virtual sink device has detected an overflow condition. This status is sticky and is cleared by writing it to 1.	0: Normal operation 1: Video FIFO overflow

MST_VS0_DTG_ENABLE (0x7A14)

Controls video output for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DTG_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DTG_ENABLE	0	Enables the display timing generator (DTG) in the associated virtual sink device. The DTG should be disabled when the core detects the no video pattern on the link to prevent invalid data from being presented on the output video interface. The DTG should be enabled when a valid video mode has been detected.	0: DTG disabled 1: DTG enabled

MST_VS0_DTG_MODE (0x7A18)

Sets the operating mode for the Display Timing Generator (DTG) for the virtual sink device. Two primary modes, timing mode and DMA mode, are selected by bit 0 of this register. Timing mode is for applications requiring accurate video pixel timing recovery and DMA mode is for applications that do not require accurate video pixel timing recovery.

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BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	–	RSVD	DMA_ENABLE
Reset	0b1	0b0	0b0	0b0	0b0	–	0b0	0b1
Access Type						–		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DMA_ENABLE	0	DMA mode enable. In DMA mode, timing information is discarded and pixels are placed directly into memory. The sync pulses are used for data framing with the width of each pulse controlled by the DMA_SYNC_WIDTH register. The data enable for valid pixels may be discontinuous.	0: Timing mode (NOT SUPPORTED) 1: DMA mode

MST_VS0_DMA_VSYNC_B0 (0x7A24)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_VSYNC_PULSE_WIDTH[7:0]							
Reset	0x3F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_PULSE_WIDTH	7:0	Sets the number of video clock cycles for the DMA mode vertical sync pulse width. The video vsync signal will be high for the specified number of clock cycles.

MST_VS0_DMA_VSYNC_B2 (0x7A26)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_VSYNC_FRONT_PORCH_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_FRONT_PORCH_L	7:0	DMA vsync front porch bits 7-0. Sets the number of video clock cycles after the last pixel of active frame data before asserting the DMA mode vertical sync pulse.

MST_VS0_DMA_VSYNC_B3 (0x7A27)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_VSYNC_FRONT_PORCH_H[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_FRONT_PORCH_H	3:0	DMA vsync front porch bits 11-8. Sets the number of video clock cycles after the last pixel of active frame data before asserting the DMA mode vertical sync pulse.

MST_VS0_DMA_HSYNC_B0 (0x7A28)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_HSYNC_PULSE_WIDTH_L[7:0]							
Reset	0x0F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_PULSE_WIDTH_L	7:0	DMA hsync width bits 7-0. Sets the number of video clock cycles for the DMA mode horizontal sync pulse width. The video hsync signal will be high for the specified number of clock cycles.

MST_VS0_DMA_HSYNC_B1 (0x7A29)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_HSYNC_PULSE_WIDTH_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_PULSE_WIDTH_H	3:0	DMA hsync width bits 11-8. Sets the number of video clock cycles for the DMA mode horizontal sync pulse width. The video hsync signal will be high for the specified number of clock cycles.

MST_VS0_DMA_HSYNC_B2 (0x7A2A)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_HSYNC_FRONT_PORCH_L[7:0]							
Reset	0x0F							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_FRONT_PORCH_L	7:0	DMA hsync front porch bits 7-0. Sets the number of video clock cycles after the last pixel of active line data before asserting the DMA mode horizontal sync pulse.

MST_VS0_DMA_HSYNC_B3 (0x7A2B)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_HSYNC_FRONT_PORCH_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_FRONT_PORCH_H	3:0	DMA hsync front porch bits 11-8. Sets the number of video clock cycles after the last pixel of active line data before asserting the DMA mode horizontal sync pulse.

MST_VS0_RED_CRC_B0 (0x7A38)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	RED_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RED_CRC_B0	7:0	Calculated eDP CRC for red color plane bits 7-0.

MST_VS0_RED_CRC_B1 (0x7A39)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	RED_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RED_CRC_B1	7:0	Calculated eDP CRC for red color plane bits 15-8.

MST_VS0_RED_CRC_B3 (0x7A3B)

Embedded DisplayPort calculated CRC for each color plane.

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BIT	7	6	5	4	3	2	1	0
Field	CRC_UPDATED	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Read Clears All	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_UPDATED	7	Calculated eDP CRC color plane values have been updated since last read of this register. This bit is cleared on read.	0: Calculated CRC not updated 1: Calculated CRC updated

MST_VS0_GRN_BLU_CRC_B0 (0x7A3C)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	BLU_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLU_CRC_B0	7:0	Calculated eDP CRC for blue color plane bits 7-0.

MST_VS0_GRN_BLU_CRC_B1 (0x7A3D)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	BLU_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLU_CRC_B1	7:0	Calculated eDP CRC for blue color plane bits 15-8.

MST_VS0_GRN_BLU_CRC_B2 (0x7A3E)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	GRN_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GRN_CRC_B0	7:0	Calculated eDP CRC for green color plane bits 7-0.

MST_VS0_GRN_BLU_CRC_B3 (0x7A3F)

Embedded DisplayPort calculated CRC for each color plane.

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BIT	7	6	5	4	3	2	1	0
Field	GRN_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GRN_CRC_B1	7:0	Calculated eDP CRC for green color plane bits 15-8.

MST_VS0_MSA_IGNORE_HRES_B0 (0x7A40)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_HRES_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSA_IGNORE_HRES_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS0_MSA_IGNORE_HRES_B1 (0x7A41)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_HRES_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSA_IGNORE_HRES_B1	7:0	MSA horizontal resolution override bits 15-8. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixel that defines a horizontal line.

MST_VS0_MSA_IGNORE_COLOR (0x7A44)

Allows overriding the MSA defined color mode.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_COLOR_MODE_EN	–	–	MSA_IGNORE_COLOR_MODE[4:0]				
Reset	0b1	–	–	0x00				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_IGNORE_COLOR_MODE_EN	7	Enables the setting in bits 4-0 to control the color mode.	0: Normal MSA color mode 1: Use bits 4-0 for color mode

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BITFIELD	BITS	DESCRIPTION	DECODE
MSA_IGNORE_COLOR_MODE	4:0	MSA color mode override. When bit 7 is 1 this value is used in place of the normal MSA MISC0/MISC1 color mode setting that is used to unpack pixels from the data stream.	2-0: Replace MSA MISC0 bits 7-5 3: Replace MSA MISC0 bit 2=0, bit 1=1 4: Replace MSA MISC1 bit 7

MST_VS0_DSC_MISC (0x7A45)

Miscellaneous controls for DSC operation.

BIT	7	6	5	4	3	2	1	0
Field	DSC_VBID_OVR	–	DSC_PIX_REM_OVR[1:0]		–	–	DSC_TS_AUTO_MDIV3	DSC_TS_USE_MDIV3
Reset	0b0	–	0x0		–	–	0b1	0b0
Access Type	Write, Read	–	Write, Read		–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_VBID_OVR	7	Overrides the DSC video VBID to set DSC active.	0: No override - normal operation 1: Force DSC video active as if the DSC video VBID bit is set
DSC_PIX_REM_OVR	5:4	Overrides the calculated remainder for DSC horizontal resolution divide-by-3. This remainder determines the number of pixel bytes that are fillers in the last DSC "pixel" of a horizontal line.	0: No override - normal operation 1: Override as 1 filler byte 2: Override as 2 filler bytes 3: Override as 0 filler bytes
DSC_TS_AUTO_MDIV3	1	Enables automatic selection of dividing Mvid by 3 for DSC timestamp control. See bit 0.	0: Manual control of Mvid divide-by-3 1: Auto-select Mvid divide-by-3
DSC_TS_USE_MDIV3	0	Divide timestamp Mvid by 3 for DSC format conversion pixel clock generation. Normally Nvid is multiplied by 3 to produce the proper DSC format conversion pixel clock. Dividing Mvid by 3 is used for cases where multiplying Nvid by 3 results in the overflow the 24-bit Nvid value. Automatic selection of Mvid divide-by-3 (bit 1) is the default.	0: Normal Nvid multiplied-by-3 1: Mvid divide-by-3

MST_VS0_PPS_CHUNK_SIZE_OVR_B0 (0x7A48)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_CHUNK_SIZE_OVR_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_CHUNK_SIZE_OVR_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS0_PPS_CHUNK_SIZE_OVR_B1 (0x7A49)

Allows overriding the MSA defined horizontal resolution.

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BIT	7	6	5	4	3	2	1	0
Field	PPS_CHUNK_SIZE_OVR_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_CHUNK_SIZE_OVR_B1	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS0_PPS_SLICE_WIDTH_OVR_B0 (0x7A4A)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_SLICE_WIDTH_OVR_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_SLICE_WIDTH_OVR_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS0_PPS_SLICE_WIDTH_OVR_B1 (0x7A4B)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_SLICE_WIDTH_OVR_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_SLICE_WIDTH_OVR_B1	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS0_PPS_BITS_PER_PIX_OVR_B0 (0x7A4C)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_BITS_PER_PIX_OVR_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_BITS_PER_PIX_OVR_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

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MST_VS0_PPS_BITS_PER_PIX_OVR_B1 (0x7A4D)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_BITS_PER_PIX_OVR_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_BITS_PER_PIX_OVR_B1	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS0_DSC_SUPPORT (0x7A50)

Enables DSC support for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DSC_SUPPORT
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_SUPPORT	0	Enables support for DSC by providing the setting for the DPCD DSC support bit at 0x00060 when DSC_DPCD_SELECT=0.	0: DSC support disabled 1: DSC support enabled

MST_VS0_DSC_VERSION (0x7A51)

DSC version for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_VERSION[7:0]							
Reset	0x11							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_VERSION	7:0	Sets the supported DSC version by providing the setting for the DPCD DSC version value at 0x00061 when DSC_DPCD_SELECT=0. Bits 3-0 hold the major version number while bits 7-4 hold the minor version number.	3-0: DSC major version 7-4: DSC minor version

MST_VS0_DSC_STATUS_B1 (0x7A71)

DSC decoder status for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DSC_CHUNK_SIZE_ERROR	DSC_ACTIVE	DSC_ENABLE
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_CHUNK_SIZE_ERROR	2	DSC chunk size error detection.	0: No DSC chunk size error detected 1: DSC chunk size error detected
DSC_ACTIVE	1	DSC video stream active. This indicates that DSC operation is enabled and the DSC VB-ID bit is set indicating that DSC compressed video is flowing.	0: DSC video stream not active 1: DSC video stream active
DSC_ENABLE	0	DSC operation enable as set by DP source in DPCD 0x160 when DSC_DPCD_SELECT=0.	0: DSC operation not enabled 1: DSC operation enabled

MST_VS0_DSC_CRC_STATUS (0x7A73)

DSC CRC control/status for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DSC_PIX_CRC_VAL	DSC_CRC_VAL
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_PIX_CRC_VAL	1	DSC reconstructed pixel CRC valid.	0: DSC reconstructed pixel CRC not valid 1: DSC reconstructed pixel CRC valid
DSC_CRC_VAL	0	DSC compressed CRC valid.	0: DSC compressed CRC not valid 1: DSC compressed CRC valid

MST_VS0_DSC_CRC0_B0 (0x7A74)

DSC compressed CRC0 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC0_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC0_B0	7:0	DSC compressed CRC0 value bits 7-0.

MST_VS0_DSC_CRC0_B1 (0x7A75)

DSC compressed CRC0 for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC0_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC0_B1	7:0	DSC compressed CRC0 value bits 15-8.

MST_VS0_DSC_CRC1_B0 (0x7A76)

DSC compressed CRC1 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC1_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC1_B0	7:0	DSC compressed CRC1 value bits 7-0.

MST_VS0_DSC_CRC1_B1 (0x7A77)

DSC compressed CRC1 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC1_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC1_B1	7:0	DSC compressed CRC1 value bits 15-8.

MST_VS0_DSC_CRC2_B0 (0x7A78)

DSC compressed CRC2 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC2_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC2_B0	7:0	DSC compressed CRC2 value bits 7-0.

MST_VS0_DSC_CRC2_B1 (0x7A79)

DSC compressed CRC2 for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC2_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC2_B1	7:0	DSC compressed CRC2 value bits 15-8.

MST_VS0_DSC_PIX_CRC0_B0 (0x7A7A)

DSC reconstructed pixel CRC0 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC0_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC0_B0	7:0	DSC reconstructed pixel CRC0 value bits 7-0.

MST_VS0_DSC_PIX_CRC0_B1 (0x7A7B)

DSC reconstructed pixel CRC0 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC0_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC0_B1	7:0	DSC reconstructed pixel CRC0 value bits 15-8.

MST_VS0_DSC_PIX_CRC1_B0 (0x7A7C)

DSC reconstructed pixel CRC1 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC1_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC1_B0	7:0	DSC reconstructed pixel CRC1 value bits 7-0.

MST_VS0_DSC_PIX_CRC1_B1 (0x7A7D)

DSC reconstructed pixel CRC1 for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC1_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC1_B1	7:0	DSC reconstructed pixel CRC1 value bits 15-8.

MST_VS0_DSC_PIX_CRC2_B0 (0x7A7E)

DSC reconstructed pixel CRC2 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC2_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC2_B0	7:0	DSC reconstructed pixel CRC2 value bits 7-0.

MST_VS0_DSC_PIX_CRC2_B1 (0x7A7F)

DSC reconstructed pixel CRC2 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC2_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC2_B1	7:0	DSC reconstructed pixel CRC2 value bits 15-8.

MST_VS0_SECONDARY_ENABLE (0x7A80)

Enables the secondary channel functionality for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SECONDARY_ENABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SECONDARY_ENABLE	0	Enables processing of secondary channel data packets. This does not apply to the eDP function which continues to operate when this bit is 0.	0: Secondary channel disabled 1: Secondary channel enabled

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MST_VS0_AUDIO_MUTE (0x7A84)

Controls audio muting for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	AUDIO_MUTE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_MUTE	0	Forces audio output to zero (mute). If this occurs in the middle of a sample transaction the current sample will be completed before the mute operation is applied.	0: Audio not mute 1: Audio mute

MST_VS0_AUDIO_SAMPLE_RES (0x7A8C)

Controls the sample resolution of audio data output from the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	AUDIO_SAMPLE_RES[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
AUDIO_SAMPLE_RES	5:0	Number of bits per output audio sample. When set to a value less than the actual SDP sample resolution, samples will be truncated to the selected output bit length. When set to a value greater than the actual SDP sample resolution, the output value will be zero padded.

MST_VS0_AUDIO_CHANNEL_COUNT (0x7A90)

Channel count layout transmitted by audio source.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUDIO_CHANNEL_COUNT[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_COUNT	3:0	Number of audio sample channels in the selected audio stream. if two channels or less are used, set to 1. Otherwise, set this value to 8.

MST_VS0_AUDIO_OUTPUT_SELECT (0x7A98)

Controls mode of audio output from virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RSVD	RSVD
Reset	–	–	–	–	–	–	0b0	0b1
Access Type	–	–	–	–	–	–		

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MST_VS0_AUDIO_CHANNEL_MAP_B0 (0x7A9C)

Controls mapping of input audio channels to output audio channels.

BIT	7	6	5	4	3	2	1	0
Field	–	CHANNEL_1_MAP[2:0]			–	CHANNEL_0_MAP[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHANNEL_1_MAP	6:4	Selects the output audio channel that is mapped to input audio channel 1.
CHANNEL_0_MAP	2:0	Selects the output audio channel that is mapped to input audio channel 0.

MST_VS0_AUDIO_CHANNEL_MAP_B1 (0x7A9D)

Controls mapping of input audio channels to output audio channels.

BIT	7	6	5	4	3	2	1	0
Field	–	CHANNEL_3_MAP[2:0]			–	CHANNEL_2_MAP[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHANNEL_3_MAP	6:4	Selects the output audio channel that is mapped to input audio channel 3.
CHANNEL_2_MAP	2:0	Selects the output audio channel that is mapped to input audio channel 2.

MST_VS0_AUDIO_CHANNEL_MAP_B2 (0x7A9E)

Controls mapping of input audio channels to output audio channels.

BIT	7	6	5	4	3	2	1	0
Field	–	CHANNEL_5_MAP[2:0]			–	CHANNEL_4_MAP[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHANNEL_5_MAP	6:4	Selects the output audio channel that is mapped to input audio channel 5.
CHANNEL_4_MAP	2:0	Selects the output audio channel that is mapped to input audio channel 4.

MST_VS0_AUDIO_CHANNEL_MAP_B3 (0x7A9F)

Controls mapping of input audio channels to output audio channels.

BIT	7	6	5	4	3	2	1	0
Field	–	CHANNEL_7_MAP[2:0]			–	CHANNEL_6_MAP[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHANNEL_7_MAP	6:4	Selects the output audio channel that is mapped to input audio channel 7.

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BITFIELD	BITS	DESCRIPTION
CHANNEL_6_MAP	2:0	Selects the output audio channel that is mapped to input audio channel 6.

MST_VS0_MAUD_B0 (0x7AA0)

Maud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	MAUD_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MAUD_B0	7:0	Maud value detected in the most recent audio timestamp SDP bits 7-0.

MST_VS0_MAUD_B1 (0x7AA1)

Maud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	MAUD_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MAUD_B1	7:0	Maud value detected in the most recent audio timestamp SDP bits 15-8.

MST_VS0_MAUD_B2 (0x7AA2)

Maud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	MAUD_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MAUD_B2	7:0	Maud value detected in the most recent audio timestamp SDP bits 23-16.

MST_VS0_NAUD_B0 (0x7AA4)

Naud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	NAUD_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
NAUD_B0	7:0	Naud value detected in the most recent audio timestamp SDP bits 7-0.

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MST_VS0_NAUD_B1 (0x7AA5)

Naud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	NAUD_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
NAUD_B1	7:0	Naud value detected in the most recent audio timestamp SDP bits 15-8.

MST_VS0_NAUD_B2 (0x7AA6)

Naud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	NAUD_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
NAUD_B2	7:0	Naud value detected in the most recent audio timestamp SDP bits 23-16.

MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_0 (0x7AB8)

Channel status field byte 0 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_0	7:0	Channel status field byte 0 from audio SDP.

MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_1 (0x7ABC)

Channel status field byte 1 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_1	7:0	Channel status field byte 1 from audio SDP.

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MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_2 (0x7AC0)

Channel status field byte 2 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_2	7:0	Channel status field byte 2 from audio SDP.

MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_3 (0x7AC4)

Channel status field byte 3 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_3	7:0	Channel status field byte 3 from audio SDP.

MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_4 (0x7AC8)

Channel status field byte 4 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_4	7:0	Channel status field byte 4 from audio SDP.

MST_VS0_AUDIO_CHANNEL_STATUS_FIELD_5 (0x7ACC)

Channel status field byte 5 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_5[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_5	7:0	Channel status field byte 5 from audio SDP.

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MST_VS0_AUDIO_CHANNEL_NUMBER_0_1 (0x7AD0)

Audio channel number from audio SDP channel status.

BIT	7	6	5	4	3	2	1	0
Field	CHANNEL_NUMBER_1[3:0]				CHANNEL_NUMBER_0[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_1	7:4	Audo channel number 1 from audio SDP channel status.
CHANNEL_NUMBER_0	3:0	Audo channel number 0 from audio SDP channel status.

MST_VS0_AUDIO_CHANNEL_NUMBER_2_3 (0x7AD4)

Audio channel number from audio SDP channel status.

BIT	7	6	5	4	3	2	1	0
Field	CHANNEL_NUMBER_3[3:0]				CHANNEL_NUMBER_2[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_3	7:4	Audo channel number 3 from audio SDP channel status.
CHANNEL_NUMBER_2	3:0	Audo channel number 2 from audio SDP channel status.

MST_VS0_AUDIO_CHANNEL_NUMBER_4_5 (0x7AD8)

Audio channel number from audio SDP channel status.

BIT	7	6	5	4	3	2	1	0
Field	CHANNEL_NUMBER_5[3:0]				CHANNEL_NUMBER_4[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_5	7:4	Audo channel number 5 from audio SDP channel status.
CHANNEL_NUMBER_4	3:0	Audo channel number 4 from audio SDP channel status.

MST_VS0_AUDIO_CHANNEL_NUMBER_6_7 (0x7ADC)

Audio channel number from audio SDP channel status.

BIT	7	6	5	4	3	2	1	0
Field	CHANNEL_NUMBER_7[3:0]				CHANNEL_NUMBER_6[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_7	7:4	Audo channel number 7 from audio SDP channel status.

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BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_6	3:0	Audo channel number 6 from audio SDP channel status.

MST_VS0_DSC_BUFFER_RDATA (0x7AE4)

DSC PPS read data.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PPS_RDATA[7:0]							
Reset	00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PPS_RDATA	7:0	Writing sets the starting DSC PPS buffer read address (0-127). Reading provides the DSC PPS buffer data at the current read address. The read address is incremented for each read.

MST_VS0_AUDIO_PACKET_DEPTH (0x7AE8)

Audio packet depth

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AUDIO_PACKET_DEPTH[1:0]	
Reset	–	–	–	–	–	–	0b10	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
AUDIO_PACKET_DEPTH	1:0	Sets the number of audio packets to be queued before the audio stream output is started.

MST_VS1_ENABLE (0x7B00)

Enables the functionality for virtual sink 1. This sink device is associated with video output port 1.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VS_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VS_ENABLE	0	Enables the MST virtual sink device 1. When disabled, video operations for this virtual sink remain in the idle state.	0: Virtual sink disabled 1: Virtual sink enabled

MST_VS1_USER_PIXEL_WIDTH (0x7B04)

Controls output data path width in pixels for the associated video output port.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	USER_PIXEL_WIDTH[2:0]		
Reset	–	–	–	–	–	0b001		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
USER_PIXEL_WIDTH	2:0	Sets the video output data path width in pixels per clock. Set to 1 for single pixel wide output and 2 for dual pixel wide output. All other values are reserved and should not be used. This should be set before any video is received.

MST_VS1_SWAP_CBCR (0x7B08)

Controls swapping of color values for the associated video output port.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CRC_MASK_SWAP	CRC_COMP_SWAP	PIX_MASK_SWAP	SWAP_CBCR
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_MASK_SWAP	3	Swap the pixel mask Cb (blue) and Cr (red) values for pixels used for CRC calculation.	0: No swap 1: Swap Cb and Cr
CRC_COMP_SWAP	2	Swap the pixel component Cb (blue) and Cr (red) values for pixels used for CRC calculation.	0: No swap 1: Swap Cb and Cr
PIX_MASK_SWAP	1	Swap the pixel mask Cb (blue) and Cr (red) values for pixels on the video output port for cases where the last pixel set contains extra pixels (user width > 1, DSC).	0: No swap 1: Swap Cb and Cr
SWAP_CBCR	0	Swap the Cb (blue) and Cr (red) values for pixels on the video output port when set for YCbCr color space.	0: No swap 1: Swap Cb and Cr

MST_VS1_USER_FIFO_RESET (0x7B0C)

BIT	7	6	5	4	3	2	1	0
Field	DISABLE_VB_FAULT_RESET	VB_FRAME_RESET_PEND_SEL	BS_FRAME_RESET_SEL	DISABLE_FRAMEE_RESET	–	DISABLE_LINE_RESET_FIFO	DISABLE_HS_LINE_RESET	DISABLE_LINE_RESET
Reset	0b0	0b0	0b0	0b0	–	0b0	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DISABLE_VB_FAULT_RESET	7	Disables the vertical blank fault detect reset. This reset occurs when the internal state indicates an active line while the incoming video indicates vertical blanking. This is for debug purposes only and should normally be set to 0.	0: Normal operation - vertical blank fault reset enabled 1: Vertical blank fault reset disabled

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BITFIELD	BITS	DESCRIPTION	DECODE
VB_FRAME_RESET_PEND_SEL	6	Disables normal resetting of video FIFOs after each line of received video data. This is for debug purposes only and should normally be set to 0.	0: Frame reset pending set by vsync 1: Frame reset pending set by vertical blank start
BS_FRAME_RESET_SEL	5	Disables normal resetting of video FIFOs after each line of received video data. This is for debug purposes only and should normally be set to 0.	0: Frame reset at vsync 1: Frame reset at next BS after last line BS
DISABLE_FRAMEE_RESET	4	Disables normal resetting of video FIFOs after each frame of received video data. This is for debug purposes only and should normally be set to 0.	0: Normal operation - frame reset enabled 1: Frame reset disabled
DISABLE_LINE_RESET_FIFO	2	Disables normal resetting of video FIFOs after each line of received video data. This is for debug purposes only and should normally be set to 0.	0: Normal operation - line reset for FIFO enabled 1: Line reset for FIFO disabled
DISABLE_HS_LINE_RESET	1	Disables normal resetting of video FIFOs after each line of received video data. This is for debug purposes only and should normally be set to 0.	0: Normal operation - line hsync reset enabled 1: Line hsync reset disabled
DISABLE_LINE_RESET	0	Disables normal resetting of video FIFOs after each line of received video data. This is for debug purposes only and should normally be set to 0.	0: Normal operation - line reset enabled 1: Line reset disabled

MST_VS1_VIDEO_FIFO_OVERFLOW (0x7B10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VIDEO_FIFO_OVERFLOW
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_FIFO_OVERFLOW	0	Indicates that the internal user data FIFO in the virtual sink device has detected an overflow condition. This status is sticky and is cleared by writing it to 1.	0: Normal operation 1: Video FIFO overflow

MST_VS1_DTG_ENABLE (0x7B14)

Controls video output for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DTG_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

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BITFIELD	BITS	DESCRIPTION	DECODE
DTG_ENABLE	0	Enables the display timing generator (DTG) in the associated virtual sink device. The DTG should be disabled when the core detects the no video pattern on the link to prevent invalid data from being presented on the output video interface. The DTG should be enabled when a valid video mode has been detected.	0: DTG disabled 1: DTG enabled

MST_VS1_DTG_MODE (0x7B18)

Sets the operating mode for the Display Timing Generator (DTG) for the virtual sink device. Two primary modes, timing mode and DMA mode, are selected by bit 0 of this register. Timing mode is for applications requiring accurate video pixel timing recovery and DMA mode is for applications that do not require accurate video pixel timing recovery.

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	DTG_DISABLE_MSA_RESET	RSVD	DMA_ENABLE
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type					Write, Read			Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DTG_DISABLE_MSA_RESET	2	MSA video FIFO reset disable. This disables the reset of the user video data FIFOs when the MSA values are detected on the link. Normally, the FIFOs are reset when MSA values are received.	0: MSA video FIFO reset enabled 1: MSA video FIFO reset disabled
DMA_ENABLE	0	DMA mode enable. In DMA mode, timing information is discarded and pixels are placed directly into memory. The sync pulses are used for data framing with the width of each pulse controlled by the DMA_SYNC_WIDTH register. The data enable for valid pixels may be discontinuous.	0: Timing mode (NOT SUPPORTED) 1: DMA mode

MST_VS1_DMA_VSYNC_B0 (0x7B24)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_VSYNC_PULSE_WIDTH[7:0]							
Reset	0x3F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_PULSE_WIDTH	7:0	Sets the number of video clock cycles for the DMA mode vertical sync pulse width. The video vsync signal will be high for the specified number of clock cycles.

MST_VS1_DMA_VSYNC_B2 (0x7B26)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync.

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The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_VSYNC_FRONT_PORCH_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_FRONT_PORCH_L	7:0	DMA vsync front porch bits 7-0. Sets the number of video clock cycles after the last pixel of active frame data before asserting the DMA mode vertical sync pulse.

MST_VS1_DMA_VSYNC_B3 (0x7B27)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the vertical sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_VSYNC_FRONT_PORCH_H[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_VSYNC_FRONT_PORCH_H	3:0	DMA vsync front porch bits 11-8. Sets the number of video clock cycles after the last pixel of active frame data before asserting the DMA mode vertical sync pulse.

MST_VS1_DMA_HSYNC_B0 (0x7B28)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_HSYNC_PULSE_WIDTH_L[7:0]							
Reset	0x0F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_PULSE_WIDTH_L	7:0	DMA hsync width bits 7-0. Sets the number of video clock cycles for the DMA mode horizontal sync pulse width. The video hsync signal will be high for the specified number of clock cycles.

MST_VS1_DMA_HSYNC_B1 (0x7B29)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_HSYNC_PULSE_WIDTH_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

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BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_PULSE_WIDTH_H	3:0	DMA hsync width bits 11-8. Sets the number of video clock cycles for the DMA mode horizontal sync pulse width. The video hsync signal will be high for the specified number of clock cycles.

MST_VS1_DMA_HSYNC_B2 (0x7B2A)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	DMA_HSYNC_FRONT_PORCH_L[7:0]							
Reset	0x0F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_FRONT_PORCH_L	7:0	DMA hsync front porch bits 7-0. Sets the number of video clock cycles after the last pixel of active line data before asserting the DMA mode horizontal sync pulse.

MST_VS1_DMA_HSYNC_B3 (0x7B2B)

When the DTG is in DMA mode, the timing control logic outputs a fixed length, active high pulse for the horizontal sync. The timing of the pulse is controlled by the settings in this register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DMA_HSYNC_FRONT_PORCH_H[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DMA_HSYNC_FRONT_PORCH_H	3:0	DMA hsync front porch bits 11-8. Sets the number of video clock cycles after the last pixel of active line data before asserting the DMA mode horizontal sync pulse.

MST_VS1_RED_CRC_B0 (0x7B38)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	RED_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RED_CRC_B0	7:0	Calculated eDP CRC for red color plane bits 7-0.

MST_VS1_RED_CRC_B1 (0x7B39)

Embedded DisplayPort calculated CRC for each color plane.

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BIT	7	6	5	4	3	2	1	0
Field	RED_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RED_CRC_B1	7:0	Calculated eDP CRC for red color plane bits 15-8.

MST_VS1_RED_CRC_B3 (0x7B3B)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	CRC_UPDATED	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Read Clears All	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_UPDATED	7	Calculated eDP CRC color plane values have been updated since last read of this register. This bit is cleared on read.	0: Calculated CRC not updated 1: Calculated CRC updated

MST_VS1_GRN_BLU_CRC_B0 (0x7B3C)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	BLU_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLU_CRC_B0	7:0	Calculated eDP CRC for blue color plane bits 7-0.

MST_VS1_GRN_BLU_CRC_B1 (0x7B3D)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	BLU_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
BLU_CRC_B1	7:0	Calculated eDP CRC for blue color plane bits 15-8.

MST_VS1_GRN_BLU_CRC_B2 (0x7B3E)

Embedded DisplayPort calculated CRC for each color plane.

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BIT	7	6	5	4	3	2	1	0
Field	GRN_CRC_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GRN_CRC_B0	7:0	Calculated eDP CRC for green color plane bits 7-0.

MST_VS1_GRN_BLU_CRC_B3 (0x7B3F)

Embedded DisplayPort calculated CRC for each color plane.

BIT	7	6	5	4	3	2	1	0
Field	GRN_CRC_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
GRN_CRC_B1	7:0	Calculated eDP CRC for green color plane bits 15-8.

MST_VS1_MSA_IGNORE_HRES_B0 (0x7B40)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_HRES_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSA_IGNORE_HRES_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS1_MSA_IGNORE_HRES_B1 (0x7B41)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_HRES_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MSA_IGNORE_HRES_B1	7:0	MSA horizontal resolution override bits 15-8. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixel that defines a horizontal line.

MST_VS1_MSA_IGNORE_COLOR (0x7B44)

Allows overriding the MSA defined color mode.

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BIT	7	6	5	4	3	2	1	0
Field	MSA_IGNORE_COLOR_MODE_EN	–	–	MSA_IGNORE_COLOR_MODE[4:0]				
Reset	0b1	–	–	0x00				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
MSA_IGNORE_COLOR_MODE_EN	7	Enables the setting in bits 4-0 to control the color mode.	0: Normal MSA color mode 1: Use bits 4-0 for color mode
MSA_IGNORE_COLOR_MODE	4:0	MSA color mode override. When bit 7 is 1 this value is used in place of the normal MSA MISC0/MISC1 color mode setting that is used to unpack pixels from the data stream.	2-0: Replace MSA MISC0 bits 7-5 3: Replace MSA MISC0 bit 2=0, bit 1=1 4: Replace MSA MISC1 bit 7

MST_VS1_DSC_MISC (0x7B45)

Miscellaneous controls for DSC operation.

BIT	7	6	5	4	3	2	1	0
Field	DSC_VBID_OVR	–	DSC_PIX_REM_OVR[1:0]		–	–	DSC_TS_AUTO_MDIV3	DSC_TS_USE_MDIV3
Reset	0b0	–	0x0		–	–	0b1	0b0
Access Type	Write, Read	–	Write, Read		–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_VBID_OVR	7	Overrides the DSC video VBID to set DSC active.	0: No override - normal operation 1: Force DSC video active as if the DSC video VBID bit is set
DSC_PIX_REM_OVR	5:4	Overrides the calculated remainder for DSC horizontal resolution divide-by-3. This remainder determines the number of pixel bytes that are fillers in the last DSC "pixel" of a horizontal line.	0: No override - normal operation 1: Override as 1 filler byte 2: Override as 2 filler bytes 3: Override as 0 filler bytes
DSC_TS_AUTO_MDIV3	1	Enables automatic selection of dividing Mvid by 3 for DSC timestamp control. See bit 0.	0: Manual control of Mvid divide-by-3 1: Auto-select Mvid divide-by-3
DSC_TS_USE_MDIV3	0	Divide timestamp Mvid by 3 for DSC format conversion pixel clock generation. Normally Nvid is multiplied by 3 to produce the proper DSC format conversion pixel clock. Dividing Mvid by 3 is used for cases where multiplying Nvid by 3 results in the overflow the 24-bit Nvid value. Automatic selection of Mvid divide-by-3 (bit 1) is the default.	0: Normal Nvid multiplied-by-3 1: Mvid divide-by-3

MST_VS1_PPS_CHUNK_SIZE_OVR_B0 (0x7B48)

Allows overriding the MSA defined horizontal resolution.

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BIT	7	6	5	4	3	2	1	0
Field	PPS_CHUNK_SIZE_OVR_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_CHUNK_SIZE_OVR_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS1_PPS_CHUNK_SIZE_OVR_B1 (0x7B49)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_CHUNK_SIZE_OVR_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_CHUNK_SIZE_OVR_B1	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS1_PPS_SLICE_WIDTH_OVR_B0 (0x7B4A)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_SLICE_WIDTH_OVR_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_SLICE_WIDTH_OVR_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS1_PPS_SLICE_WIDTH_OVR_B1 (0x7B4B)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_SLICE_WIDTH_OVR_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_SLICE_WIDTH_OVR_B1	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

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MST_VS1_PPS_BITS_PER_PIX_OVR_B0 (0x7B4C)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_BITS_PER_PIX_OVR_B0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_BITS_PER_PIX_OVR_B0	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS1_PPS_BITS_PER_PIX_OVR_B1 (0x7B4D)

Allows overriding the MSA defined horizontal resolution.

BIT	7	6	5	4	3	2	1	0
Field	PPS_BITS_PER_PIX_OVR_B1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PPS_BITS_PER_PIX_OVR_B1	7:0	MSA horizontal resolution override bits 7-0. When this value (15-0) is non-zero it is used in place of the normal MSA horizontal resolution value for determining the number of pixels that defines a horizontal line.

MST_VS1_DSC_SUPPORT (0x7B50)

Enables DSC support for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DSC_SUPPORT
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_SUPPORT	0	Enables support for DSC by providing the setting for the DPCD DSC support bit at 0x00060 when DSC_DPCD_SELECT=1.	0: DSC support disabled 1: DSC support enabled

MST_VS1_DSC_VERSION (0x7B51)

DSC version for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_VERSION[7:0]							
Reset	0x11							
Access Type	Write, Read							

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BITFIELD	BITS	DESCRIPTION	DECODE
DSC_VERSION	7:0	Sets the supported DSC version by providing the setting for the DPCD DSC version value at 0x00061 when DSC_DPCD_SELECT=1. Bits 3-0 hold the major version number while bits 7-4 hold the minor version number.	3-0: DSC major version 7-4: DSC minor version

MST_VS1_DSC_STATUS_B1 (0x7B71)

DSC decoder status for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DSC_CHUNK_SIZE_ERROR	DSC_ACTIVE	DSC_ENABLE
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_CHUNK_SIZE_ERROR	2	DSC chunk size error detection.	0: No DSC chunk size error detected 1: DSC chunk size error detected
DSC_ACTIVE	1	DSC video stream active. This indicates that DSC operation is enabled and the DSC VB-ID bit is set indicating that DSC compressed video is flowing.	0: DSC video stream not active 1: DSC video stream active
DSC_ENABLE	0	DSC operation enable as set by DP source in the DSC DPCD 0x160 when DSC_DPCD_SELECT=1.	0: DSC operation not enabled 1: DSC operation enabled

MST_VS1_DSC_CRC_STATUS (0x7B73)

DSC CRC control/status for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	DSC_PIX_CRC_VAL	DSC_CRC_VAL
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DSC_PIX_CRC_VAL	1	DSC reconstructed pixel CRC valid.	0: DSC reconstructed pixel CRC not valid 1: DSC reconstructed pixel CRC valid
DSC_CRC_VAL	0	DSC compressed CRC valid.	0: DSC compressed CRC not valid 1: DSC compressed CRC valid

MST_VS1_DSC_CRC0_B0 (0x7B74)

DSC compressed CRC0 for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC0_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC0_B0	7:0	DSC compressed CRC0 value bits 7-0.

MST_VS1_DSC_CRC0_B1 (0x7B75)

DSC compressed CRC0 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC0_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC0_B1	7:0	DSC compressed CRC0 value bits 15-8.

MST_VS1_DSC_CRC1_B0 (0x7B76)

DSC compressed CRC1 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC1_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC1_B0	7:0	DSC compressed CRC1 value bits 7-0.

MST_V1_DSC_CRC1_B1 (0x7B77)

DSC compressed CRC1 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC1_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC1_B1	7:0	DSC compressed CRC1 value bits 15-8.

MST_VS1_DSC_CRC2_B0 (0x7B78)

DSC compressed CRC2 for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC2_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC2_B0	7:0	DSC compressed CRC2 value bits 7-0.

MST_VS1_DSC_CRC2_B1 (0x7B79)

DSC compressed CRC2 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_CRC2_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_CRC2_B1	7:0	DSC compressed CRC2 value bits 15-8.

MST_VS1_DSC_PIX_CRC0_B0 (0x7B7A)

DSC reconstructed pixel CRC0 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC0_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC0_B0	7:0	DSC reconstructed pixel CRC0 value bits 7-0.

MST_VS1_DSC_PIX_CRC0_B1 (0x7B7B)

DSC reconstructed pixel CRC0 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC0_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC0_B1	7:0	DSC reconstructed pixel CRC0 value bits 15-8.

MST_VS1_DSC_PIX_CRC1_B0 (0x7B7C)

DSC reconstructed pixel CRC1 for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC1_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC1_B0	7:0	DSC reconstructed pixel CRC1 value bits 7-0.

MST_VS1_DSC_PIX_CRC1_B1 (0x7B7D)

DSC reconstructed pixel CRC1 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC1_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC1_B1	7:0	DSC reconstructed pixel CRC1 value bits 15-8.

MST_VS1_DSC_PIX_CRC2_B0 (0x7B7E)

DSC reconstructed pixel CRC2 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC2_B0[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC2_B0	7:0	DSC reconstructed pixel CRC2 value bits 7-0.

MST_VS1_DSC_PIX_CRC2_B1 (0x7B7F)

DSC reconstructed pixel CRC2 for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PIX_CRC2_B1[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PIX_CRC2_B1	7:0	DSC reconstructed pixel CRC2 value bits 15-8.

MST_VS1_SECONDARY_ENABLE (0x7B80)

Enables the secondary channel functionality for the virtual sink.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SECONDARY_ENABLE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SECONDARY_ENABLE	0	Enables processing of secondary channel data packets. This does not apply to the eDP function which continues to operate when this bit is 0.	0: Secondary channel disabled 1: Secondary channel enabled

MST_VS1_AUDIO_MUTE (0x7B84)

Controls audio muting for the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	AUDIO_MUTE
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUDIO_MUTE	0	orces audio output to zero (mute). If this occurs in the middle of a sample transaction the current sample will be completed before the mute operation is applied.	0: Audio not mute 1: Audio mute

MST_VS1_AUDIO_SAMPLE_RES (0x7B8C)

Controls the sample resolution of audio data output from the virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	AUDIO_SAMPLE_RES[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
AUDIO_SAMPLE_RES	5:0	Number of bits per output audio sample. When set to a value less than the actual SDP sample resolution, samples will be truncated to the selected output bit length. When set to a value greater than the actual SDP sample resolution, the output value will be zero padded.

MST_VS1_AUDIO_CHANNEL_COUNT (0x7B90)

Channel count layout transmitted by audio source.

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BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUDIO_CHANNEL_COUNT[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_COUNT	3:0	Number of audio sample channels in the selected audio stream. if two channels or less are used, set to 1. Otherwise, set this value to 8.

MST_VS1_AUDIO_OUTPUT_SELECT (0x7B98)

Controls mode of audio output from virtual sink.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RSVD	RSVD
Reset	–	–	–	–	–	–	0b0	0b1
Access Type	–	–	–	–	–	–		

MST_VS1_AUDIO_CHANNEL_MAP_B0 (0x7B9C)

Selects the audio output port for active audio output.

BIT	7	6	5	4	3	2	1	0
Field	–	CHANNEL_1_MAP[2:0]			–	CHANNEL_0_MAP[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHANNEL_1_MAP	6:4	Selects the output audio channel that is mapped to input audio channel 1.
CHANNEL_0_MAP	2:0	Selects the output audio channel that is mapped to input audio channel 0.

MST_VS1_AUDIO_CHANNEL_MAP_B1 (0x7B9D)

Controls mapping of input audio channels to output audio channels.

BIT	7	6	5	4	3	2	1	0
Field	–	CHANNEL_3_MAP[2:0]			–	CHANNEL_2_MAP[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHANNEL_3_MAP	6:4	Selects the output audio channel that is mapped to input audio channel 3.
CHANNEL_2_MAP	2:0	Selects the output audio channel that is mapped to input audio channel 2.

MST_VS1_AUDIO_CHANNEL_MAP_B2 (0x7B9E)

Controls mapping of input audio channels to output audio channels.

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BIT	7	6	5	4	3	2	1	0
Field	–	CHANNEL_5_MAP[2:0]			–	CHANNEL_4_MAP[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHANNEL_5_MAP	6:4	Selects the output audio channel that is mapped to input audio channel 5.
CHANNEL_4_MAP	2:0	Selects the output audio channel that is mapped to input audio channel 4.

MST_VS1_AUDIO_CHANNEL_MAP_B3 (0x7B9F)

Controls mapping of input audio channels to output audio channels.

BIT	7	6	5	4	3	2	1	0
Field	–	CHANNEL_7_MAP[2:0]			–	CHANNEL_6_MAP[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
CHANNEL_7_MAP	6:4	Selects the output audio channel that is mapped to input audio channel 7.
CHANNEL_6_MAP	2:0	Selects the output audio channel that is mapped to input audio channel 6.

MST_VS1_MAUD_B0 (0x7BA0)

Maud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	MAUD_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MAUD_B0	7:0	Maud value detected in the most recent audio timestamp SDP bits 7-0.

MST_VS1_MAUD_B1 (0x7BA1)

Maud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	MAUD_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MAUD_B1	7:0	Maud value detected in the most recent audio timestamp SDP bits 15-8.

MST_VS1_MAUD_B2 (0x7BA2)

Maud value from audio SDP.

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BIT	7	6	5	4	3	2	1	0
Field	MAUD_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MAUD_B2	7:0	Maud value detected in the most recent audio timestamp SDP bits 23-16.

MST_VS1_NAUD_B0 (0x7BA4)

Naud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	NAUD_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
NAUD_B0	7:0	Naud value detected in the most recent audio timestamp SDP bits 7-0.

MST_VS1_NAUD_B1 (0x7BA5)

Naud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	NAUD_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
NAUD_B1	7:0	Naud value detected in the most recent audio timestamp SDP bits 15-8.

MST_VS1_NAUD_B2 (0x7BA6)

Naud value from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	NAUD_B2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
NAUD_B2	7:0	Naud value detected in the most recent audio timestamp SDP bits 23-16.

MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_0 (0x7BB8)

Channel status field byte 0 from audio SDP.

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BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_0	7:0	Channel status field byte 0 from audio SDP.

MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_1 (0x7BBC)

Channel status field byte 1 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_1	7:0	Channel status field byte 1 from audio SDP.

MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_2 (0x7BC0)

Channel status field byte 2 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_2	7:0	Channel status field byte 2 from audio SDP.

MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_3 (0x7BC4)

Channel status field byte 3 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_3	7:0	Channel status field byte 3 from audio SDP.

MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_4 (0x7BC8)

Channel status field byte 4 from audio SDP.

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BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_4	7:0	Channel status field byte 4 from audio SDP.

MST_VS1_AUDIO_CHANNEL_STATUS_FIELD_5 (0x7BCC)

Channel status field byte 5 from audio SDP.

BIT	7	6	5	4	3	2	1	0
Field	AUDIO_CHANNEL_STATUS_FIELD_5[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
AUDIO_CHANNEL_STATUS_FIELD_5	7:0	Channel status field byte 5 from audio SDP.

MST_VS1_AUDIO_CHANNEL_NUMBER_0_1 (0x7BD0)

Audio channel number from audio SDP channel status.

BIT	7	6	5	4	3	2	1	0
Field	CHANNEL_NUMBER_1[3:0]				CHANNEL_NUMBER_0[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_1	7:4	Audo channel number 1 from audio SDP channel status.
CHANNEL_NUMBER_0	3:0	Audo channel number 0 from audio SDP channel status.

MST_VS1_AUDIO_CHANNEL_NUMBER_2_3 (0x7BD4)

Audio channel number from audio SDP channel status.

BIT	7	6	5	4	3	2	1	0
Field	CHANNEL_NUMBER_3[3:0]				CHANNEL_NUMBER_2[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_3	7:4	Audo channel number 3 from audio SDP channel status.
CHANNEL_NUMBER_2	3:0	Audo channel number 2 from audio SDP channel status.

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MST_VS1_AUDIO_CHANNEL_NUMBER_4_5 (0x7BD8)

Audio channel number from audio SDP channel status.

BIT	7	6	5	4	3	2	1	0
Field	CHANNEL_NUMBER_5[3:0]				CHANNEL_NUMBER_4[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_5	7:4	Audo channel number 5 from audio SDP channel status.
CHANNEL_NUMBER_4	3:0	Audo channel number 4 from audio SDP channel status.

MST_VS1_AUDIO_CHANNEL_NUMBER_6_7 (0x7BDC)

Audio channel number from audio SDP channel status.

BIT	7	6	5	4	3	2	1	0
Field	CHANNEL_NUMBER_7[3:0]				CHANNEL_NUMBER_6[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHANNEL_NUMBER_7	7:4	Audo channel number 7 from audio SDP channel status.
CHANNEL_NUMBER_6	3:0	Audo channel number 5 from audio SDP channel status.

MST_VS1_DSC_BUFFER_RDATA (0x7BE4)

DSC PPS read data.

BIT	7	6	5	4	3	2	1	0
Field	DSC_PPS_RDATA[7:0]							
Reset	00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DSC_PPS_RDATA	7:0	Writing sets the starting DSC PPS buffer read address (0-127). Reading provides the DSC PPS buffer data at the current read address. The read address is incremented for each read.

MST_VS1_AUDIO_PACKET_DEPTH (0x7BE8)

Audio packet depth

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AUDIO_PACKET_DEPTH[1:0]	
Reset	–	–	–	–	–	–	0b10	
Access Type	–	–	–	–	–	–	Write, Read	

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BITFIELD	BITS	DESCRIPTION
AUDIO_PACKET_DEPTH	1:0	Sets the number of audio packets to be queued before the audio stream output is started.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/23	Initial release	—

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