

# DS90UH981-Q1 4K DS1 to FPD-Link IV Bridge Serializer With HDCP

## 1 Features

- Single or dual port MIPI DS1 receiver
  - Compliant to D-PHY v1.2 and DS1 v1.3.1
  - Packed 16/18/24/30-bit RGB and 16-bit YCbCr
  - Loosely packed 18-bit RGB and 20-bit 4:2:2
  - 1 clock lane and 1-4 configurable data lanes per D-PHY Port
  - Up to 2.5 Gbps/lane with skew calibration
  - Supports data lane swap and polarity inversion
  - Supports both burst and non-burst mode
  - SuperFrame Unpacking Capability
  - Suitable for 4K @ 60 Hz video resolution
- FPD-Link IV interface
  - Supports 10.8/6.75/3.375 Gbps per channel; Up to 21.6 Gbps over dual channels
  - Coax/STP interconnect support
  - Port Splitting to enable Y-cable interfaces
- Ultra-low latency control channel
  - Two I<sub>2</sub>C up to 1MHz (up to 3.4 MHz for local bus access)
  - High speed GPIOs
- Backwards compatible
  - Integrated HDCP v1.4 with on-chip keys
  - 720P 92x and 1080P/2K 94x product families
  - ADAS 936, 954, 960, 962, 9702, 9722 deserializers
- Security and diagnostics
  - Voltage and temperature monitoring
  - Line Fault Detection
  - BIST and pattern generation
  - CRC and error diagnostics
  - Unique ID for counterfeit protection
  - ECC on control bits
- Advanced link robustness and EMC control
  - Data scrambling
  - Spread spectrum clocking generation (SSCG)
- Low power operation
  - 1.8-V and 1.1-V dual power supply
- AEC-Q100 qualified for automotive applications
  - AEC-Q100 grade-level 2: -40°C to +105°C
  - 64 pin QFN Wettable flanks 9 mm x 9 mm
  - ISO 10605 and IEC 61000-4-2 ESD compliant

## 2 Applications

- Automotive displays:
  - Central Information Displays (CID)
  - Rear Seat Entertainment (RSE)
  - Digital instrument clusters
  - Head units and HMI modules
  - Head Up Display (HUD)
  - Rear view and side mirror displays

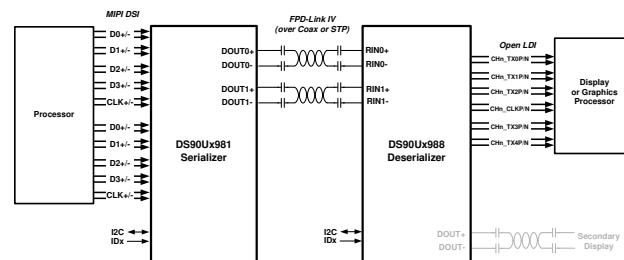
## 3 Description

DS90UH981-Q1 is a MIPI DS1 to FPD-Link III/IV bridge device. In conjunction with an FPD-Link IV deserializer, the chipset provides a high-speed serialized interface over low-cost 50Ω coax or STP cables. The DS90UH981-Q1 is a D-PHY v1.2 compliant device that serializes a MIPI DS1 input supporting video resolutions including 4K with 30-bit color depth. The FPD-Link IV interface supports video and audio data transmission and full duplex control, including I<sub>2</sub>C and GPIO data over a single channel or dual channels. Consolidation of video data and control over two FPD-Link IV lanes reduces the interconnect size and weight and simplifies system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, SSCG, and randomization. In backward compatible mode, the device supports up to 720p and 1080p resolutions with 24-bit color depth over a single/dual link as well as HDCP v1.4 support when paired with an HDCP-capable deserializer. In ADAS compatible mode, the device is interoperable with 936, 95x, 96x & 97x deserializers supporting resolutions up to 8MP+/40fps.

### Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
DS90UH981-Q1	VQFN (64)	9.00 mm × 9.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

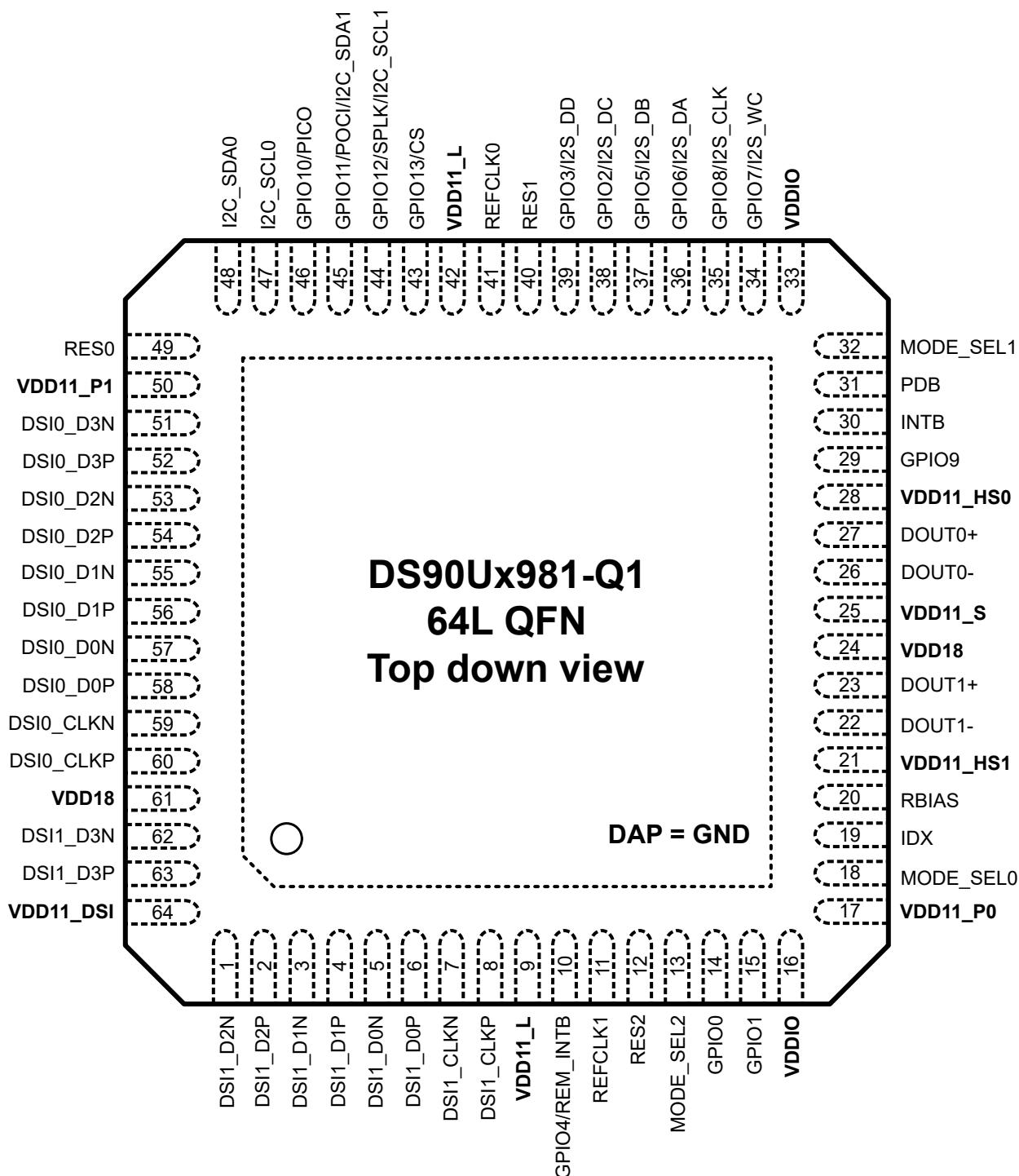
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (July 2022) to Revision B (October 2023)</b>	<b>Page</b>
• Added register address for polarity swapping function in DSI Receiver.....	41
• Added DSI Skew Calibration Section.....	44
• Added lower and upper thresholds for supply voltages table.....	67
• Added clarification that both TDM and I2S signals are received via the I2S pins, and clearly indicating the specific pins being referred to. ....	74
• Added additional register configuration description to Back Channel GPIO Configuration.....	83
• Added additional register configuration description to FPD-Link III Dual Link Operation.....	90
• FPD-Link III I2S Audio section now links to chip level Parallel I2S section.....	95
• Updated column numbers to start from 1 for IVI (MODE_SEL2=0) Configuration Select (MODE_SEL1) Table and ADAS (MODE_SEL2=1) Configuration Select (MODE_SEL1) Table.....	103
• Added information on I2C behavior in event of link disruption.....	108
• Corrected references to 0x70-0x77 to be called TARGET_ID_x as intended and updated daisy-chain example diagrams to be specific to DS90Ux981 device.....	108
• Description update for Remote Target Addressing.....	114
• Add Page_5: D-PHY Analog Port 0.....	219
• Add Page_7: D-PHY Analog Port 1.....	219

<b>Changes from Revision * (April 2021) to Revision A (July 2022)</b>	<b>Page</b>
• Clarified REFCLK1 pin connection when unused.....	4
• Added hyperlink for I2C Bus Pullup Resistor Calculation reference document.....	4
• Revised SPI references to use inclusive terminology.....	4
• Revised I2C references to use inclusive terminology.....	4
• Updated Return Loss of TX for Forward Channel maximum frequency of 5.4GHz .....	10
• SSCG section updated with constraints for backward compatible operation.....	50
• SSCG section updated to fix center spread diagram and revised equations.....	50
• Added a recommendation for minimum total horizontal blanking.....	56
• Added section for FPD-Link polarity swap.....	65

• Added reference to App Note for internal ADC.....	66
• Changed V_SF to CF for Pin_Voltage equation .....	67
• Updated lower and upper thresholds for supply voltages table.....	67
• Clarified REM_INTB functionality does not support multiple ports in independent FPD-Link mode.....	69
• Added new section description for ABUFF.....	72
• Added new section description for audio functionality.....	74
• Removed FPD-Link III I2S Audio section, and referenced to Parallel I2S.....	74
• Added support for higher FPD-Link III PCLK between 98x devices.....	88
• New section to include back channel optimizations for FPD Mode changes.....	91
• Removed FPD-Link III I2S Audio section, and referenced to new audio section.....	95
• Added clarification on switching to ADAS mode after startup in IVI .....	98
• Added more supported RGB input formats for DSI to CSI-2 conversion.....	98
• Removed comment (Port 0 Only) in IDx table; The IDX sets the VDDI2C for all I2C ports.....	105
• Added I2C considerations when hot plugging.....	108
• Unique ID section updated to reflect 12 byte registers instead of 10.....	116
• Description of register 0x0C[3] was corrected to provide proper register of CRC_ERROR_RESET.....	117
• Added figure for coax line fault circuit, removed ADC Threshold tables.....	444

## 5 Pin Configuration and Functions



**Figure 5-1. RTD Package  
64-Pin VQFN  
Top View**

**Table 5-1. Pin Functions**

PIN		I/O, TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
<b>MIPI DSI INPUT PINS</b>			
DSI0_D0P	58	I	DSI Channel 0 Input Data Lane 0 If unused, tie to Ground.
DSI0_D0N	57	I	
DSI0_D1P	56	I	DSI Channel 0 Input Data Lane 1 If unused, tie to Ground.
DSI0_D1N	55	I	
DSI0_D2P	54	I	DSI Channel 0 Input Data Lane 2 If unused, tie to Ground.
DSI0_D2N	53	I	
DSI0_D3P	52	I	DSI Channel 0 Input Data Lane 3 If unused, tie to Ground.
DSI0_D3N	51	I	
DSI0_CLKP	60	I	DSI Channel 0 Input Clock Lane If unused, tie to Ground.
DSI0_CLKN	59	I	
DSI1_D0P	6	I	DSI Channel 1 Input Data Lane 0 If unused, tie to Ground.
DSI1_D0N	5	I	
DSI1_D1P	4	I	DSI Channel 1 Input Data Lane 1 If unused, tie to Ground.
DSI1_D1N	3	I	
DSI1_D2P	2	I	DSI Channel 1 Input Data Lane 2 If unused, tie to Ground.
DSI1_D2N	1	I	
DSI1_D3P	63	I	DSI Channel 1 Input Data Lane 3 If unused, tie to Ground.
DSI1_D3N	62	I	
DSI1_CLKP	8	I	DSI Channel 1 Input Clock Lane If unused, tie to Ground.
DSI1_CLKN	7	I	
<b>FPD-Link IV INTERFACE PINS</b>			
DOUT0-	26	I/O	FPD-Link IV Input/Output 0 The pin must be AC-coupled with a 100 nF capacitor. PCB traces are recommended to maintain 100 Ω differential impedance. This can interface with a compatible FPD-Link III/IV deserializer RX through an STP or coaxial cable. In Coax configuration the AC-Coupling capacitor for DOUT+ must be 100 nF and DOUT- must be 47 nF. If port is unused, leave pins as No Connect. Reference <a href="#">Section 8.2</a>
DOUT0+	27		
DOUT1-	22	I/O	FPD-Link IV Input/Output 1 The pin must be AC-coupled with a 100 nF capacitor. PCB traces are recommended to maintain 100 Ω differential impedance. This can interface with a compatible FPD-Link III/IV deserializer RX through an STP or coaxial cable. In Coax configuration the AC-Coupling capacitor for DOUT+ must be 100 nF and DOUT- must be 47 nF. If port is unused, leave pins as No Connect. Reference <a href="#">Section 8.2</a>
DOUT1+	23		
<b>CLOCK REFERENCE PINS</b>			
REFCLK0	41	I	External Oscillator Input This pin is the primary clock reference input. This must be connected to an external CMOS-level 1.8V 27 MHz oscillator source (+/-100ppm). Reference <a href="#">Section 8.2.1</a>
REFCLK1	11	I	Reference Clock Input For Backward Compatibility. This clock is an optional reference clock that can be used when connecting to FPD-Link III devices requiring a specific PCLK frequency. The clock frequency is 16.5-33MHz (+/-100 ppm). This is optional if REFCLK0 is present. If unused leave as No Connect or tie to Ground.
<b>CONTROL PINS</b>			
I2C_SDA0	48	I/O, OD	I2C Data Input / Output Interface Open drain. Pull-up resistor to either 1.8V or 3.3V required for I2C functionality. Refer to "I2C Bus Pullup Resistor Calculation, <a href="#">SLVA689</a> " to determine the pull up resistor value. If unused leave as No Connect.

**Table 5-1. Pin Functions (continued)**

PIN		I/O, TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
I2C_SCL0	47	I/O, OD	I2C Clock Input / Output Interface Open drain. Pull-up resistor to either 1.8V or 3.3V required for I2C functionality. Refer to "I2C Bus Pullup Resistor Calculation, <a href="#">SLVA689</a> " to determine the pull up resistor value. If unused leave as No Connect.
GPIO11/POCI/ I2C_SDA1	45	I/O, PD	General Purpose Input/Output 11 Shared with Peripheral OUT Controller IN (POCI) and I2C_SDA1 When used as I2C_SDA1, pull-up resistor to 1.8V is required for I2C functionality. Refer to "I2C Bus Pullup Resistor Calculation, <a href="#">SLVA689</a> " to determine the pull up resistor value. Pin functionality defaults to I2C with an internal 25 kΩ pull down resistor disabled. If unused leave as No Connect.
GPIO12/SPLK/ I2C_SCL1	44	I/O, PD	General Purpose Input/Output 12 Shared with SPLK and I2C_SCL2 When used as I2C_SCL2, pull-up resistor to 1.8V is required for I2C functionality. Refer to "I2C Bus Pullup Resistor Calculation, <a href="#">SLVA689</a> " to determine the pull up resistor value. Pin functionality defaults to I2C with an internal 25 kΩ pull down resistor disabled. If unused leave as No Connect.
IDX	19	I, S	I2C Address Select See <a href="#">Table 7-51</a> . Connect to external Pull-up to VDD18 (pin 24) is required under all conditions. <b>DO NOT LEAVE OPEN OR NO CONNECT.</b> Connect to external pull-up and pull-down resistors to create a voltage divider.
MODE_SEL0	18	I, S	Mode Select 0 Input. See <a href="#">Table 7-47</a> . Connect to external Pull-up to VDD18 (pin 24) is required under all conditions. <b>DO NOT LEAVE OPEN OR NO CONNECT.</b> Connect to external pull-up and pull-down resistors to create a voltage divider.
MODE_SEL1	32	I, S	Mode Select 1 Input. See <a href="#">Table 7-48</a> . Connect to external Pull-up to VDD18 (pin 24) is required under all conditions. <b>DO NOT LEAVE OPEN OR NO CONNECT.</b> Connect to external pull-up and pull-down resistors to create a voltage divider.
MODE_SEL2	13	I, S	Mode Select 2 Input. See <a href="#">Table 7-46</a> MODE_SEL2 = 1, ADAS mode MODE_SEL2 = 0, IVI mode Internal 25 kΩ pull-down resistor. Connect to external Pull-up to VDD18 (pin 24) is required under all conditions. <b>DO NOT LEAVE OPEN OR NO CONNECT.</b> Connect to external pull-up and pull-down resistors to create a voltage divider.
PDB	31	I	Power-Down Mode Input Pin PDB = 1, device is enabled (normal operation) PDB = 0, device is powered down. Internal 25 kΩ pull-down resistor Reference <a href="#">Section 9.1</a>
INTB	30	O, OD	Interrupt output pin INTB = H, Normal Operation INTB = L, Interrupt Request Recommended pull-up: 4.7kΩ to VDDIO. <b>DO NOT LEAVE OPEN OR NO CONNECT.</b>
<b>I2S PINS</b>			
GPIO2/I2S_DC	38	I/O, PD	General Purpose Input/Output 2 Shared with I2S_DC Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO3/I2S_DD	39	I/O, PD	General Purpose Input/Output 3 Shared with I2S_DD Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO5/I2S_DB	37	I/O, PD	General Purpose Input/Output 5 Shared with I2S_DB Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO6/I2S_DA	36	I/O, PD	General Purpose Input/Output 6 Shared with I2S_DA Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.

**Table 5-1. Pin Functions (continued)**

PIN		I/O, TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
GPIO7/I2S_WC	34	I/O, PD	General Purpose Input/Output 7 Shared with I2S_WC Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO8/I2S_CLK	35	I/O, PD	General Purpose Input/Output 8 Shared with I2S_CLK Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
<b>SPI PINS</b>			
GPIO10/PICO	46	I/O, PD	General Purpose Input/Output 10 Shared with SPI Peripheral IN Controller OUT (PICO) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. When configured as an inputs, this pin can be used for sensing the input voltage of Line Fault Detection. For Line Fault Detection functionality, a 0.1μF decoupling capacitor is required as close to the device pin for filtering out any high frequency noise. If unused leave as No Connect.
GPIO11/POCI/I2C_SDA1	45	I/O, PD	General Purpose Input/Output 11 Shared with SPI Peripheral OUT Controller IN (POCI) and I2C_SDA1 When used as I2C_SDA1, pull-up resistor to 1.8V is required for I2C functionality. Refer to "I2C Bus Pullup Resistor Calculation, SLVA689" to determine the pull up resistor value. Pin functionality defaults to I2C with an internal 25 kΩ pull down resistor disabled. When configured as inputs, this pin can be used for sensing the input voltage of Line Fault Detection. For Line Fault Detection functionality, a 0.1μF decoupling capacitor is required as close to the device pin for filtering out any high frequency noise. If unused leave as No Connect.
GPIO12/SPLK/I2C_SCL1	44	I/O, PD	General Purpose Input/Output 12 Shared with SPLK and I2C_SCL2 When used as I2C_SCL2, pull-up resistor to 1.8V is required for I2C functionality. Refer to "I2C Bus Pullup Resistor Calculation, SLVA689" to determine the pull up resistor value. Pin functionality defaults to I2C with an internal 25 kΩ pull down resistor disabled. When configured as inputs, this pin can be used for sensing the input voltage of Line Fault Detection. A 0.1μF decoupling capacitor requires as close to the device pin for filtering out any high frequency noise. If unused leave as No Connect.
GPIO13/CS	43	I/O, PD	General Purpose Input/Output 13 Shared with Chip Select (CS) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. When configured as inputs, this pin can be used for sensing the input voltage of Line Fault Detection. A 0.1μF decoupling capacitor requires as close to the device pin for filtering any high frequency noise. If unused leave as No Connect.
<b>GPIO PINS</b>			
GPIO0	14	I/O, PD	General Purpose Input/Output 0 GPIO0 defaults to an input state. The pin has an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO1	15	I/O, PD	General Purpose Input/Output 1 GPIO1 defaults to an input state. The pin has an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO2/I2S_DC	38	I/O, PD	General Purpose Input/Output 2. GPIO2 defaults to an input state. Shared with I2S_DC Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO3/I2S_DD	39	I/O, PD	General Purpose Input/Output 3 GPIO3 defaults to an input state. Shared with I2S_DD Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.

**Table 5-1. Pin Functions (continued)**

PIN		I/O, TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
GPIO4/ REM_INTB	10	I/O, PD	General Purpose Input/Output (GPIO) or Remote Interrupt Pin. GPIO4 defaults to an input state. At device startup this pin must be left floating or pulled to GND. The remote interrupt function must be enabled manually after startup. When used as remote interrupt, REM_INTB directly mirrors the status of the INTB_IN signal from the remote device. No separate serializer register read is required to reset and change the status of this pin. If unused leave as No Connect.
GPIO5/I2S_DB	37	I/O, PD	General Purpose Input/Output 5 GPIO5 defaults to an input state. Shared with I2S_DB Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO6/I2S_DA	36	I/O, PD	General Purpose Input/Output 6 GPIO6 defaults to an input state. Shared with I2S_DA Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. This pin can be used for monitoring of external voltage source. If unused leave as No Connect.
GPIO7/I2S_WC	34	I/O, PD	General Purpose Input/Output 7 GPIO7 defaults to an input state. Shared with I2S_WC Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO8/I2S_CLK	35	I/O, PD	General Purpose Input/Output 8 GPIO8 defaults to an input state. Shared with I2S_CLK Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. This pin can be used for monitoring of external voltage source. If unused leave as No Connect.
GPIO9	29	I/O, PD	General Purpose Input/Output 9 GPIO9 defaults to an input state. GPIO9 has an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO10/PICO	46	I/O, PD	General Purpose Input/Output 10 GPIO10 defaults to an input state. Shared with Peripheral IN Controller OUT (PICO) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. If unused leave as No Connect.
GPIO11/POCI/ I2C_SDA1	45	I/O, PD	General Purpose Input/Output 11 Shared with Peripheral OUT Controller IN (POCI) and I2C_SDA1 When used as I2C_SDA1, typically pulled up by 2.2kΩ resistors to 1.8V Pin functionality defaults to I2C with an internal 25 kΩ pull down resistor disabled. If unused leave as No Connect.
GPIO12/SPLK/ I2C_SCL1	44	I/O, PD	General Purpose Input/Output 12 Shared with SPLK and I2C_SCL2 When used as I2C_SCL2, typically pulled up by 2.2kΩ resistors to 1.8V Pin functionality defaults to I2C with an internal 25 kΩ pull down resistor disabled. If unused leave as No Connect.
GPIO13/CS	43	I/O, PD	General Purpose Input/Output 13 GPIO13 defaults to an input state. Shared with Chip Select (CS) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor.
<b>POWER AND GROUND PINS</b>			
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the VQFN package. Connect to the ground plane (GND).
VDD18	24 61	P	1.8V (±5%) supply. Each pin must be decoupled with 0.01uF and bulk 1uF, 10uF to GND. See <a href="#">Figure 8-2</a> . Filters are required for this pin.

**Table 5-1. Pin Functions (continued)**

PIN		I/O, TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
VDD11_P1	50	P	1.15V ( $\pm 5\%$ ) supply. Each pin must be connected to 0.01uF and bulk 1uF to GND. See <a href="#">Figure 8-2</a> . Pins VDD11_P1, VDD11_DSI, VDD11_HS0, VDD11_HS1, VDD11_P0, VDD11_S are required to be filtered.
VDD11_DSI	64	P	
VDD11_HS0	28	P	
VDD11_HS1	21	P	
VDD11_L	9 42	P	
VDD11_P0	17	P	
VDD11_S	25	P	
VDDIO	16 33	P	1.8V ( $\pm 5\%$ ) LVCMOS I/O power. Pin must be decoupled with 1uF, and 0.1uF and 10uF capacitors to GND.
<b>OTHER PINS</b>			
RES0	49	—	Reserved. Must be left floating.
RES1	40	—	Reserved. Must be left floating.
RES2	12	—	Reserved. Recommended left as no connect, can be tied to VDD11 for layout compatibility with DS90Ux941AS-Q1
RBIAS	20	I	Resistor Bias Connect a 10 k $\Omega$ resistor (1% tol) to GND. This resistor is used for internal reference current calibration and must be a high accuracy resistor $\pm 1\%$ to provide proper operation.

(1) The definitions below define the functionality of the I/O cells for each pin. TYPE:

- I = Input
- O = Output
- I/O = Input/Output
- OD = Open Drain
- PD = Internal Pulldown
- P, G = Power supply, Ground
- S = Strap Input

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	VDD18 (VDD18)	-0.3	2.16	V
Supply voltage	VDD11 (VDD11_P0, VDD11_P1, VDD11_DSI, VDD11_L, VDD11_S, VDD11_HS0, VDD11_HS1)	-0.3	1.32	V
Supply voltage	VDDIO	-0.3	2.16	V
DSI input voltage	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-0.3	1.32	V
FPD-Link IV output voltage	DOUT0+, DOUT0-, DOUT1+, DOUT1-	-0.3	1.32	V
Analog voltage	RBIAS	-0.3	2.16	V
Reserved pin voltage	RES0, RES1, RES2	-0.3	1.32	V
LVCMS IO voltage	PDB, GPIO0, GPIO1, GPIO2 / I2S_DC, GPIO3 / I2S_DD, REM_INTB / GPIO4, GPIO5 / I2S_DB, GPIO6 / I2S_DA, GPIO7 / I2S_WC, GPIO8 / I2S_CLK, GPIO9, GPIO10 / MOSI, GPIO11 / MISO / I2C_SDA1, GPIO12 / SPLK / I2C_SCL1, GPIO13 / SS, INTB	-0.3	2.16	V
Reference Clock Voltage	REFCLK0, REFCLK1	-0.3	2.16	V
Configuration input voltage	MODE_SEL0, MODE_SEL1, MODE_SEL2, IDX	-0.3	2.16	V
Open-Drain voltage	GPIO11 / MISO / I2C_SDA1, GPIO12 / SPLK / I2C_SCL1, INTB I2C_SDA0, I2C_SCL0	-0.3	2.16	V
Junction temperature, T <sub>J</sub>		-0.3	3.96	
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

				VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	Pins DOUT0+, DOUT0-, DOUT1+, DOUT1-	±2	kV	
			All pins except DOUT0+, DOUT0-, DOUT1+, DOUT1-	±2		
		Charged device model (CDM), per AEC Q100-011				
		IEC 61000-4-2, R <sub>D</sub> = 330 Ω, C <sub>S</sub> = 150 pF	Contact Discharge (DOUT0+, DOUT0-, DOUT1+, DOUT1-)	±4		
		IEC 61000-4-2, R <sub>D</sub> = 330 Ω, C <sub>S</sub> = 150 pF	Air Discharge (DOUT0+, DOUT0-, DOUT1+, DOUT1-)	±8		
		ISO 10605 R <sub>D</sub> = 330 Ω, C <sub>S</sub> = 150 pF and 330 pF R <sub>D</sub> = 2 kΩ, C <sub>S</sub> = 150 pF and 330 pF		±4		
		Contact Discharge (DOUT0+, DOUT0-, DOUT1+, DOUT1-)		±8		
		Air Discharge (DOUT0+, DOUT0-, DOUT1+, DOUT1-)		±8		

## 6.3 Thermal Information

THERMAL METRIC		DS90UH981-Q1	UNIT
		RTD (VQFN)	
		64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	18.6	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	7.0	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	4.5	°C/W

## 6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
<b>RECOMMENDED OPERATING CONDITIONS</b>					
LVC MOS I/O supply voltage	VDDIO	1.71	1.8	1.89	V
I2C Supply Voltage	I2C_SDA0, I2C_SCL0, GPIO11 / MISO / I2C_SDA1, GPIO12 / SPLK / I2C_SCL1 = $V_{(I2C)}$ = 1.8 V	1.71	1.8	1.89	V
	I2C_SDA0, I2C_SCL0 = $V_{(I2C)}$ = 3.3 V <sup>(2)</sup>	3	3.3	3.6	V
Supply noise <sup>(1)</sup>	VDD11			25	mV <sub>PP</sub>
	VDD18			50	
	VDDIO = 1.8V			50	
	$V_{(I2C)}$ = 1.8V			50	
	$V_{(I2C)}$ = 3.3V			100	
Operating free air temperature, $T_A$	Operating free air temperature, $T_A$	-40	25	105	°C
MIPI data rate (per DSI lane)		150		2500	Mbps
MIPI DSI HS clock frequency			75	1250	MHz
Local I2C frequency, $f_{I2C}$	Local I2C frequency Standard Mode			0.1	MHz
	Local I2C frequency Fast Mode			0.4	
	Local I2C frequency Fast Plus Mode			1	
	Local I2C frequency High-Speed Mode			3.4	
Supply voltage	VDD18	1.71	1.8	1.89	V
Supply voltage	VDD11	1.09	1.15	1.21	V

(1) DC - 50 MHz

(2) Not supported for High-Speed Mode. Supported for Standard, Fast, and Fast-Plus I2C modes.

## 6.5 DC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>TOTAL POWER CONSUMPTION</b>						
$P_T$	Total power consumption	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>  2x DSI Input (4-lane, 630 Mbps/lane), 2x FPD-Link III output, 3.675 Gbps Backward compatible mode			1.106	W
$I_{DD-18T}$	1.8 V Total supply current				202	mA
$I_{DD-18}$	Supply current		VDD18		83	mA
$I_{DD-18}$	Supply current		VDDIO		119	mA
$I_{DD-11T}$	1.15 V Total supply current		VDD11 <sup>(2)</sup>		598	mA
$I_{DD-11}$	Supply current		VDD11_P1		1	mA
$I_{DD-11}$	Supply current		VDD11_DSI		1	mA
$I_{DD-11}$	Supply current		VDD11_L		497	mA
$I_{DD-11}$	Supply current		VDD11_P0		15	mA
$I_{DD-11}$	Supply current		VDD11_HS1		30	mA
$I_{DD-11}$	Supply current		VDD11_S		14	mA
$I_{DD-11}$	Supply current		VDD11_HS0		40	mA
$P_T$	Total power consumption	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>  1x DSI Input (4-lane, 1.26 Gbps/lane), 2x FPD-Link III output, 3.675 Gbps Backward compatible mode			0.984	W
$I_{DD-18T}$	1.8 V Total supply current		VDD18 and VDDIO <sup>(1)</sup>		165	mA
$I_{DD-18}$	Supply current		VDD18		46	mA
$I_{DD-18}$	Supply current		VDDIO		119	mA
$I_{DD-11T}$	1.15 V Total supply current		VDD11 <sup>(2)</sup>		555	mA
$I_{DD-11}$	Supply current		VDD11_P1		1	mA
$I_{DD-11}$	Supply current		VDD11_DSI		1	mA
$I_{DD-11}$	Supply current		VDD11_L		454	mA
$I_{DD-11}$	Supply current		VDD11_P0		15	mA
$I_{DD-11}$	Supply current		VDD11_HS1		30	mA
$I_{DD-11}$	Supply current		VDD11_S		14	mA
$I_{DD-11}$	Supply current		VDD11_HS0		40	mA
$P_T$	Total power consumption	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>  1x DSI Input (4-lane 630 Mbps/lane), 1x FPD-Link III output, 3.675 Gbps Backward compatible mode			0.775	W
$I_{DD-18T}$	1.8 V Total supply current		VDD18 and VDDIO <sup>(1)</sup>		104	mA
$I_{DD-18}$	Supply current		VDD18		46	mA
$I_{DD-18}$	Supply current		VDDIO		58	mA
$I_{DD-11T}$	1.15 V Total supply current		VDD11 <sup>(2)</sup>		478	mA
$I_{DD-11}$	Supply current		VDD11_P1		1	mA
$I_{DD-11}$	Supply current		VDD11_DSI		1	mA
$I_{DD-11}$	Supply current		VDD11_L		399	mA
$I_{DD-11}$	Supply current		VDD11_P0		12	mA
$I_{DD-11}$	Supply current		VDD11_HS1		24	mA
$I_{DD-11}$	Supply current		VDD11_S		11	mA
$I_{DD-11}$	Supply current		VDD11_HS0		30	mA

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$P_T$	Total power consumption  $I_{DD-18T}$ 1.8 V Total supply current  $I_{DD-18}$ Supply current  $I_{DD-18}$ Supply current  $I_{DD-11T}$ 1.15 V Total supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			0.781	W
$I_{DD-18T}$		VDD18 and VDDIO <sup>(1)</sup>			107	mA
$I_{DD-18}$		VDD18			46	mA
$I_{DD-18}$		VDDIO			61	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			478	mA
$I_{DD-11}$		VDD11_P1			1	mA
$I_{DD-11}$		VDD11_DSI			1	mA
$I_{DD-11}$		VDD11_L			395	mA
$I_{DD-11}$		VDD11_P0			12	mA
$I_{DD-11}$		VDD11_HS1			29	mA
$I_{DD-11}$		VDD11_S			11	mA
$I_{DD-11}$		VDD11_HS0			29	mA
$P_T$	Total power consumption  $I_{DD-18T}$ 1.8 V Total supply current  $I_{DD-18}$ Supply current  $I_{DD-18}$ Supply current  $I_{DD-11T}$ 1.15 V Total supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			1.108	W
$I_{DD-18T}$		VDD18 and VDDIO <sup>(1)</sup>			200	mA
$I_{DD-18}$		VDD18			83	mA
$I_{DD-18}$		VDDIO			117	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			603	mA
$I_{DD-11}$		VDD11_P1			1	mA
$I_{DD-11}$		VDD11_DSI			1	mA
$I_{DD-11}$		VDD11_L			494	mA
$I_{DD-11}$		VDD11_P0			15	mA
$I_{DD-11}$		VDD11_HS1			39	mA
$I_{DD-11}$		VDD11_S			14	mA
$I_{DD-11}$		VDD11_HS0			39	mA
$P_T$	Total power consumption  $I_{DD-18T}$ 1.8 V Total supply current  $I_{DD-18}$ Supply current  $I_{DD-18}$ Supply current  $I_{DD-11T}$ 1.15 V Total supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			0.826	W
$I_{DD-18T}$		VDD18 and VDDIO <sup>(1)</sup>			113	mA
$I_{DD-18}$		VDD18			51	mA
$I_{DD-18}$		VDDIO			61	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			506	mA
$I_{DD-11}$		VDD11_P1			1	mA
$I_{DD-11}$		VDD11_DSI			1	mA
$I_{DD-11}$		VDD11_L			410	mA
$I_{DD-11}$		VDD11_P0			12	mA
$I_{DD-11}$		VDD11_HS1			35	mA
$I_{DD-11}$		VDD11_S			12	mA
$I_{DD-11}$		VDD11_HS0			35	mA

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$P_T$	Total power consumption  1.8 V Total supply current  Supply current  Supply current  1.15 V Total supply current  Supply current  Supply current  Supply current  Supply current  Supply current  Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			1.202	W
$I_{DD-18T}$		VDD18 and VDDIO <sup>(1)</sup>			211	mA
$I_{DD-18}$		VDD18			94	mA
$I_{DD-18}$		VDDIO			117	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			663	mA
$I_{DD-11}$		VDD11_P1			2	mA
$I_{DD-11}$		VDD11_DSI			2	mA
$I_{DD-11}$		VDD11_L			526	mA
$I_{DD-11}$		VDD11_P0			16	mA
$I_{DD-11}$		VDD11_HS1			51	mA
$I_{DD-11}$		VDD11_S			15	mA
$I_{DD-11}$		VDD11_HS0			51	mA
$P_T$	Total power consumption  1.8 V Total supply current  Supply current  Supply current  1.15 V Total supply current  Supply current  Supply current  Supply current  Supply current  Supply current  Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			0.754	W
$I_{DD-18T}$		VDD18 and VDDIO <sup>(1)</sup>			99	mA
$I_{DD-18}$		VDD18			46	mA
$I_{DD-18}$		VDDIO			53	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			468	mA
$I_{DD-11}$		VDD11_P1			1	mA
$I_{DD-11}$		VDD11_DSI			1	mA
$I_{DD-11}$		VDD11_L			392	mA
$I_{DD-11}$		VDD11_P0			11	mA
$I_{DD-11}$		VDD11_HS1			23	mA
$I_{DD-11}$		VDD11_S			11	mA
$I_{DD-11}$		VDD11_HS0			29	mA
$P_T$	Total power consumption  1.8 V Total supply current  Supply current  Supply current  1.15 V Total supply current  Supply current  Supply current  Supply current  Supply current  Supply current  Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			0.847	W
$I_{DD-18T}$		VDD18 and VDDIO <sup>(1)</sup>			109	mA
$I_{DD-18}$		VDD18			51	mA
$I_{DD-18}$		VDDIO			57	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			529	mA
$I_{DD-11}$		VDD11_P1			1	mA
$I_{DD-11}$		VDD11_DSI			1	mA
$I_{DD-11}$		VDD11_L			433	mA
$I_{DD-11}$		VDD11_P0			13	mA
$I_{DD-11}$		VDD11_HS1			26	mA
$I_{DD-11}$		VDD11_S			13	mA
$I_{DD-11}$		VDD11_HS0			42	mA

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$P_T$	Total power consumption  $I_{DD-18T}$ 1.8 V Total supply current  $I_{DD-18}$ Supply current  $I_{DD-18}$ Supply current  $I_{DD-11T}$ 1.15 V Total supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			0.836	W
$I_{DD-18}$		VDD18 and VDDIO <sup>(1)</sup>			104	mA
$I_{DD-18}$		VDD18			51	mA
$I_{DD-18}$		VDDIO			53	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			528	mA
$I_{DD-11}$		VDD11_P1			1	mA
$I_{DD-11}$		VDD11_DSI			1	mA
$I_{DD-11}$		VDD11_L			432	mA
$I_{DD-11}$		VDD11_P0			13	mA
$I_{DD-11}$		VDD11_HS1			26	mA
$I_{DD-11}$		VDD11_S			12	mA
$I_{DD-11}$		VDD11_HS0			43	mA
$P_T$	Total power consumption  $I_{DD-18}$ 1.8 V Total supply current  $I_{DD-18}$ Supply current  $I_{DD-18}$ Supply current  $I_{DD-11T}$ 1.15 V Total supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			0.927	W
$I_{DD-18}$		VDD18 and VDDIO <sup>(1)</sup>			118	mA
$I_{DD-18}$		VDD18			59	mA
$I_{DD-18}$		VDDIO			59	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			581	mA
$I_{DD-11}$		VDD11_P1			2	mA
$I_{DD-11}$		VDD11_DSI			2	mA
$I_{DD-11}$		VDD11_L			457	mA
$I_{DD-11}$		VDD11_P0			12	mA
$I_{DD-11}$		VDD11_HS1			48	mA
$I_{DD-11}$		VDD11_S			12	mA
$I_{DD-11}$		VDD11_HS0			48	mA
$P_T$	Total power consumption  $I_{DD-18T}$ 1.8 V Total supply current  $I_{DD-18}$ Supply current  $I_{DD-18}$ Supply current  $I_{DD-11T}$ 1.15 V Total supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current  $I_{DD-11}$ Supply current	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			1.460	W
$I_{DD-18}$		VDD18 and VDDIO <sup>(1)</sup>			250	mA
$I_{DD-18}$		VDD18			120	mA
$I_{DD-18}$		VDDIO			130	mA
$I_{DD-11T}$		VDD11 <sup>(2)</sup>			815	mA
$I_{DD-11}$		VDD11_P1			3	mA
$I_{DD-11}$		VDD11_DSI			3	mA
$I_{DD-11}$		VDD11_L			626	mA
$I_{DD-11}$		VDD11_P0			16	mA
$I_{DD-11}$		VDD11_HS1			75	mA
$I_{DD-11}$		VDD11_S			16	mA
$I_{DD-11}$		VDD11_HS0			76	mA

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$P_Z$	PDB = LOW	VDD18 <sup>(1)</sup> , VDDIO <sup>(1)</sup> , VDD11 <sup>(2)</sup>			0.367	W
$I_{DD-18ZT}$		VDD18 and VDDIO <sup>(1)</sup>			2	mA
$I_{DD-18Z}$		VDD18			1	mA
$I_{DD-18Z}$		VDDIO			1	mA
$I_{DD-11ZT}$		VDD11 <sup>(2)</sup>			300	mA
$I_{DD-11Z}$		VDD11_P1			2	mA
$I_{DD-11Z}$		VDD11_DSI			2	mA
$I_{DD-11Z}$		VDD11_L			262	mA
$I_{DD-11Z}$		VDD11_P0			5	mA
$I_{DD-11Z}$		VDD11_HS1			12	mA
$I_{DD-11Z}$		VDD11_S			12	mA
$I_{DD-11Z}$		VDD11_HS0			5	mA

### 1.8-V LVCMOS I/O

$V_{OH}$	High-level output voltage	$I_{OH} = -4 \text{ mA}, \text{VDDIO} = 1.71 \text{ V to } 1.89 \text{ V}$	GPIO0, GPIO1, GPIO2 / I <sub>S_DC</sub> , GPIO3 / I <sub>S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>S_DB</sub> , GPIO6 / I <sub>S_DA</sub> , GPIO7 / I <sub>S_WC</sub> , GPIO8 / I <sub>S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, GPIO12 / I <sub>C_SDA1</sub> , GPIO11 / I <sub>C_SCL1</sub> , PDB, MODE_SEL2	VDDIO – 0.45	VDDIO	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4 \text{ mA}, \text{VDDIO} = 1.71 \text{ V to } 1.89 \text{ V}$	GPIO0, GPIO1, GPIO2 / I <sub>S_DC</sub> , GPIO3 / I <sub>S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>S_DB</sub> , GPIO6 / I <sub>S_DA</sub> , GPIO7 / I <sub>S_WC</sub> , GPIO8 / I <sub>S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, GPIO12 / I <sub>C_SDA1</sub> , GPIO11 / I <sub>C_SCL1</sub> , PDB, MODE_SEL2	GND	0.45	V
$V_{IH}$	High-level input voltage	$\text{VDDIO} = 1.71 \text{ V to } 1.89 \text{ V}$	GPIO0, GPIO1, GPIO2 / I <sub>S_DC</sub> , GPIO3 / I <sub>S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>S_DB</sub> , GPIO6 / I <sub>S_DA</sub> , GPIO7 / I <sub>S_WC</sub> , GPIO8 / I <sub>S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, GPIO12 / I <sub>C_SDA1</sub> , GPIO11 / I <sub>C_SCL1</sub> , PDB, MODE_SEL2	0.65 × VDDIO	VDDIO	V
$V_{IL}$	Low-level input voltage	$\text{VDDIO} = 1.71 \text{ V to } 1.89 \text{ V}$	GPIO0, GPIO1, GPIO2 / I <sub>S_DC</sub> , GPIO3 / I <sub>S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>S_DB</sub> , GPIO6 / I <sub>S_DA</sub> , GPIO7 / I <sub>S_WC</sub> , GPIO8 / I <sub>S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, GPIO12 / I <sub>C_SDA1</sub> , GPIO11 / I <sub>C_SCL1</sub> , PDB, MODE_SEL2	GND	0.35 × VDDIO	V
$I_{IH}$	Input high current	$V_{IN} = \text{VDDIO} = 1.71 \text{ V to } 1.89 \text{ V, Internal pulldown enabled}$	GPIO0, GPIO1, GPIO2 / I <sub>S_DC</sub> , GPIO3 / I <sub>S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>S_DB</sub> , GPIO6 / I <sub>S_DA</sub> , GPIO7 / I <sub>S_WC</sub> , GPIO8 / I <sub>S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, GPIO12 / I <sub>C_SDA1</sub> , GPIO11 / I <sub>C_SCL1</sub> , PDB, MODE_SEL2		100	$\mu\text{A}$
		$V_{IN} = \text{VDDIO} = 1.71 \text{ V to } 1.89 \text{ V, Internal pulldown disabled}$	GPIO0, GPIO1, GPIO2 / I <sub>S_DC</sub> , GPIO3 / I <sub>S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>S_DB</sub> , GPIO6 / I <sub>S_DA</sub> , GPIO7 / I <sub>S_WC</sub> , GPIO8 / I <sub>S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, GPIO12 / I <sub>C_SDA1</sub> , GPIO11 / I <sub>C_SCL1</sub> , PDB, MODE_SEL2		25	$\mu\text{A}$

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I <sub>IL</sub>	Input low current	V <sub>IN</sub> = 0 V	GPIO0, GPIO1, GPIO2 / I <sub>2S_DC</sub> , GPIO3 / I <sub>2S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>2S_DB</sub> , GPIO6 / I <sub>2S_DA</sub> , GPIO7 / I <sub>2S_WC</sub> , GPIO8 / I <sub>2S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, GPIO12 / I <sub>2C_SDA1</sub> , GPIO11 / I <sub>2C_SCL1</sub> , PDB, MODE_SEL2	-25		µA
I <sub>IN_STRAP</sub>	Strap pin input current	V <sub>IN</sub> = 0 V to VDD18	IDX, MODE_SEL0, MODE_SEL1	-2	2	µA
I <sub>OS</sub>	Output short circuit current	V <sub>OUT</sub> = 0 V	GPIO0, GPIO1, GPIO2 / I <sub>2S_DC</sub> , GPIO3 / I <sub>2S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>2S_DB</sub> , GPIO6 / I <sub>2S_DA</sub> , GPIO7 / I <sub>2S_WC</sub> , GPIO8 / I <sub>2S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, GPIO12 / I <sub>2C_SDA1</sub> , GPIO11 / I <sub>2C_SCL1</sub> , PDB, MODE_SEL2	-35		mA
I <sub>OZ</sub>	TRI-STATE output current	V <sub>OUT</sub> = 0 V or VDDIO, PDB = L	GPIO0, GPIO1, GPIO2 / I <sub>2S_DC</sub> , GPIO3 / I <sub>2S_DD</sub> , REM_INTB / GPIO4, GPIO5 / I <sub>2S_DB</sub> , GPIO6 / I <sub>2S_DA</sub> , GPIO7 / I <sub>2S_WC</sub> , GPIO8 / I <sub>2S_CLK</sub> , GPIO9, GPIO10 / MOSI, GPIO13 / SS, PDB, MODE_SEL2	-20	20	µA
			GPIO12 / I <sub>2C_SDA1</sub> , GPIO11 / I <sub>2C_SCL1</sub>	-40	40	µA

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>OPEN DRAIN OUTPUT</b>						
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA, V <sub>DIO</sub> = 1.71 V to 1.89 V	INTB	GND	0.45	V
I <sub>IN</sub>	Leakage current	V <sub>IN</sub> = V <sub>DIO</sub>		-65	65	μA
<b>SERIAL CONTROL BUS<sup>(3)</sup></b>						
V <sub>IL</sub>	Input low-level	Standard/Fast/Fast Plus Mode	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	GND	0.3 × V <sub>(I<sub>2C</sub>)</sub>	V
V <sub>IH</sub>	Input high-level	Standard/Fast/Fast Plus Mode		0.7 × V <sub>(I<sub>2C</sub>)</sub>	V <sub>(I<sub>2C</sub>)</sub>	V
V <sub>HYS</sub>	Input hysteresis	Standard/Fast/Fast Plus Mode		70		mV
V <sub>OL1</sub>	Output low-level	Standard-mode/Fast-mode, I <sub>OL</sub> = 3 mA, V <sub>(I<sub>2C</sub>)</sub> = 3.0 V to 3.6 V	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0	0	0.4	V
V <sub>OL1</sub>	Output low-level	Fast-mode Plus, I <sub>OL</sub> = 20 mA	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	0	0.4	V
V <sub>OL2</sub>	Output low-level	Standard-mode/Fast-mode I <sub>OL</sub> = 3 mA, V <sub>(I<sub>2C</sub>)</sub> = 1.71 V to 1.89 V	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	0	0.2 × V <sub>(I<sub>2C</sub>)</sub>	V
I <sub>IL</sub>	Input low current	V <sub>IN</sub> = 0V	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	-40		μA
I <sub>IH</sub>	Input high current	V <sub>IN</sub> = V <sub>(I<sub>2C</sub>)</sub>	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1		40	μA
I <sub>OL</sub>	Output low-level current	Standard/Fast Mode, V <sub>OL</sub> = 0.2 × V <sub>(I<sub>2C</sub>)</sub> , V <sub>(I<sub>2C</sub>)</sub> = 1.71 V to 1.89 V	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	3		mA
I <sub>OL</sub>	Output low-level current	Standard/Fast Mode, V <sub>OL</sub> = 0.4, V <sub>(I<sub>2C</sub>)</sub> = 3.0 V to 3.6 V	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	3		mA
I <sub>OL</sub>	Output low-level current	Fast Plus Mode	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	20		mA
C <sub>IN</sub>	Input capacitance		I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	5		pF
V <sub>nL</sub>	Noise margin at the LOW level	For each connected device (including hysteresis)	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	0.1 × V <sub>(I<sub>2C</sub>)</sub>		V
V <sub>nH</sub>	Noise margin at the HIGH level	For each connected device (including hysteresis)	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	0.2 × V <sub>(I<sub>2C</sub>)</sub>		V

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>SERIAL CONTROL BUS HIGH-SPEED MODE<sup>(3)</sup></b>						
V <sub>IL</sub>	Input low-level	High-Speed Mode	I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	GND	0.3 × V <sub>(I2C)</sub>	V
V <sub>IH</sub>	Input high-level	High-Speed Mode		0.7 × V <sub>(I2C)</sub>	V <sub>(I2C)</sub> + 0.5	V
V <sub>HYS</sub>	Input hysteresis	High-Speed Mode		70		mV
V <sub>OL</sub>	Output low-level	High-Speed Mode, I <sub>OL</sub> = 3 mA, V <sub>(I2C)</sub> = 1.71 V to 1.89 V		0	0.2 × V <sub>(I2C)</sub>	V
I <sub>IL</sub>	Input low current	V <sub>IN</sub> = 0V		-65	65	µA
I <sub>IH</sub>	Input high current	V <sub>IN</sub> = V <sub>(I2C)</sub>		-65	65	µA
C <sub>IN</sub>	Input capacitance		I <sub>2C</sub> _SDA0, I <sub>2C</sub> _SCL0, GPIO11 / MISO / I <sub>2C</sub> _SDA1, GPIO12 / SPLK / I <sub>2C</sub> _SCL1	5		pF
V <sub>nH</sub>	Noise margin at the HIGH level	For each connected device (including hysteresis)		0.2 × V <sub>(I2C)</sub>		V
V <sub>nL</sub>	Noise margin at the LOW level	For each connected device (including hysteresis)		0.1 × V <sub>(I2C)</sub>		V

### VOLTAGE AND TEMPERATURE SENSING

V <sub>ACC</sub>	Voltage sensor accuracy			-2.5	±1	+2.5	%
T <sub>ACC</sub>	Temperature sensor accuracy	-40 to 150 °C junction temperature		-5.5	±2.5	+5.5	°C

### FPD-LINK IV DC SPECIFICATIONS

V <sub>OUTl</sub>	Single-ended output amplitude		DOUT0+, DOUT0-, DOUT1+, DOUT1-	470	575	670	mV
V <sub>ODl</sub>	Differential output amplitude		DOUT0+, DOUT0-, DOUT1+, DOUT1-	940	1150	1340	mVpp
ΔV <sub>OD</sub>	Differential output voltage unbalance	R <sub>L</sub> =100Ω	DOUT0+, DOUT0-, DOUT1+, DOUT1-		1	50	mV
ΔV <sub>OS</sub>	Output offset voltage	R <sub>L</sub> =100Ω	DOUT0+, DOUT0-, DOUT1+, DOUT1-		VDD11/2		V
ΔV <sub>OS</sub>	Output offset voltage mismatch	R <sub>L</sub> =100Ω	DOUT0+, DOUT0-, DOUT1+, DOUT1-		1	50	mV
ΔV <sub>CM</sub>	Output common-mode noise		DOUT0+, DOUT0-, DOUT1+, DOUT1-			20	mV
V <sub>IN-BC</sub>	Single-ended back channel input amplitude	R <sub>L</sub> = 50 Ω Single-ended configuration. Back channel rate= 168.75 Mbps. (FPD-Link IV mode)	DOUT0+, DOUT0-, DOUT1+, DOUT1-	110			mV
V <sub>ID-BC</sub>	Differential back channel input amplitude	R <sub>L</sub> = 100 Ω. Differential configuration. Back channel rate = 168.75 Mbps. (FPD-Link IV mode)	DOUT0+, DOUT0-, DOUT1+, DOUT1-	220			mV
V <sub>IN-BC</sub>	Single-ended back channel input amplitude	R <sub>L</sub> = 50 Ω Single-ended configuration. Back channel rate = 5, 10, 20 Mbps (FPD-Link III and ADAS mode)	DOUT0+, DOUT0-, DOUT1+, DOUT1-	130			mV
V <sub>ID-BC</sub>	Differential back channel input amplitude	R <sub>L</sub> = 100 Ω. Differential configuration. Back channel rate = 5, 10, 20 Mbps (FPD-Link III and ADAS mode)	DOUT0+, DOUT0-, DOUT1+, DOUT1-	260			mV
R <sub>T</sub>	Internal termination resistor	Single-ended	DOUT0+, DOUT0-, DOUT1+, DOUT1-	40	50	60	Ω
		Differential	DOUT0+, DOUT0-, DOUT1+, DOUT1-	80	100	120	Ω

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>MIPI D-PHY HSRX RECEIVER</b>						
$V_{CMRX(DC)}$	Common-mode voltage, HS receive mode	Steady-state	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	70	330	mV
$V_{IDTH}$	Differential input high threshold	Data rates ≤ 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	70		mV
$V_{IDTH}$	Differential input high threshold	Data rate > 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		40	mV
$V_{IDTL}$	Differential input low threshold	Data rates ≤ 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-70		mV
$V_{IDTL}$	Differential input low threshold	Data rate > 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-40		mV

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$V_{IH-HS}$	Single-ended input high voltage	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		460		mV
$V_{IL-HS}$	Single-ended input low voltage	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-40			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		450		mV
$Z_{ID}$	Differential input impedance	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	80	100	125	$\Omega$
$Z_{ID\_Open}$	Differential input impedance in unterminated mode	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	10			k $\Omega$
<b>MIPI D-PHY LPRX RECEIVER</b>						

## 6.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$V_{IH-LP}$	LP logic 1 input voltage	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DSI0_CLKN,	740			mV
$V_{IL-LP}$	LP logic 0 input voltage, not in ULP state	DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		550		mV
$V_{HYST}$	Input hysteresis		25			mV

(1) VDD18 = 1.8 V and VDDIO = 1.8 V for typical, and 1.89 V for max

(2) VDD11 = 1.15 V for typical, and 1.2 V for max

(3) Multi-function pins in I2C mode. For GPIO11 / MISO / I2C\_SDA1 and GPIO12 / SPLK / I2C\_SCL1,  $V_{(I2C)}$  must be 1.8 V.

## 6.6 AC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>LVC MOS I/O</b>						
FC_GP IO_jit	Forward channel GPIO jitter 1 FC_GPIO	At maximum recommended GPIO rate over one 10.8 Gbps FC (1 des)			48.9	ns
FC_GP IO_jit	Forward channel GPIO jitter 1 FC_GPIO	At maximum recommended GPIO rate over two 10.8 Gbps FC (2 daisy-chained des), jitter at second des output			97.8	ns
FC_GP IO_jit	Forward channel GPIO jitter 1 FC_GPIO	At maximum recommended GPIO rate over three 10.8 Gbps FC (3 daisy-chained des), jitter at third des output			146.7	ns
FC_GP IO_jit	Forward channel GPIO jitter 1 FC_GPIO	At maximum recommended GPIO rate over four 10.8 Gbps FC (4 daisy-chained des), jitter at fourth des output			195.6	ns
FC_GP IO_jit	Forward channel GPIO jitter 2 FC_GPIO	At maximum recommended GPIO rate over one 10.8 Gbps FC (1 des)			97.8	ns
FC_GP IO_jit	Forward channel GPIO jitter 2 FC_GPIO	At maximum recommended GPIO rate over two 10.8 Gbps FC (2 daisy-chained des), jitter at second des output			195.6	ns
FC_GP IO_jit	Forward channel GPIO jitter 2 FC_GPIO	At maximum recommended GPIO rate over three 10.8 Gbps FC (3 daisy-chained des), jitter at third des output			293.3	ns
FC_GP IO_jit	Forward channel GPIO jitter 2 FC_GPIO	At maximum recommended GPIO rate over four 10.8 Gbps FC (4 daisy-chained des), jitter at fourth des output			391.1	ns
FC_GP IO_jit	Forward channel GPIO jitter 4 FC_GPIO	At maximum recommended GPIO rate over one 10.8 Gbps FC (1 des)			146.7	ns
FC_GP IO_jit	Forward channel GPIO jitter 4 FC_GPIO	At maximum recommended GPIO rate over two 10.8 Gbps FC (2 daisy-chained des), jitter at second des output			293.3	ns
FC_GP IO_jit	Forward channel GPIO jitter 4 FC_GPIO	At maximum recommended GPIO rate over three 10.8 Gbps FC (3 daisy-chained des), jitter at third des output			440	ns
FC_GP IO_jit	Forward channel GPIO jitter 4 FC_GPIO	At maximum recommended GPIO rate over four 10.8 Gbps FC (4 daisy-chained des), jitter at fourth des output			586.7	ns
FC_GP IO_Lat	Forward channel GPIO latency, 1 FC_GPIO	At maximum recommended GPIO rate over one 10.8 Gbps FC (1 des)			0.222	us
FC_GP IO_Lat	Forward channel GPIO latency, 1 FC_GPIO	At maximum recommended GPIO rate over two 10.8 Gbps FC (2 daisy-chained des), latency before second des output			0.444	us
FC_GP IO_Lat	Forward channel GPIO latency, 1 FC_GPIO	At maximum recommended GPIO rate over three 10.8 Gbps FC (3 daisy-chained des), latency before third des output			1.333	us

## 6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 1 FC_GPIO	At maximum recommended GPIO rate over four 10.8 Gbps FC (4 daisy-chained des), latency before fourth des output			5.333	us
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 2 FC_GPIO	At maximum recommended GPIO rate over one 10.8 Gbps FC (1 des)			0.444	us
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 2 FC_GPIO	At maximum recommended GPIO rate over two 10.8 Gbps FC (2 daisy-chained des), latency before second des output			0.889	us
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 2 FC_GPIO	At maximum recommended GPIO rate over three 10.8 Gbps FC (3 daisy-chained des), latency before third des output			2.667	us
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 2 FC_GPIO	At maximum recommended GPIO rate over four 10.8 Gbps FC (4 daisy-chained des), latency before fourth des output			10.667	us
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 4 FC_GPIO	At maximum recommended GPIO rate over one 10.8 Gbps FC (1 des)			1.778	us
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 4 FC_GPIO	At maximum recommended GPIO rate over two 10.8 Gbps FC (2 daisy-chained des), latency before second des output			3.556	us
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 4 FC_GPIO	At maximum recommended GPIO rate over three 10.8 Gbps FC (3 daisy-chained des), latency before third des output			10.667	us
FC_GP IO <sub>Lat</sub>	Forward channel GPIO latency, 4 FC_GPIO	At maximum recommended GPIO rate over four 10.8 Gbps FC (4 daisy-chained des), latency before fourth des output			42.667	us
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 1 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), jitter at serializer output			177.778	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, jitter at serializer output			213.333	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, jitter at serializer output			248.889	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, jitter at serializer output			284.444	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 4 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), jitter at serializer output			711.238	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, jitter at serializer output			853.485	ns

## 6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, jitter at serializer output			995.733	us
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, jitter at serializer output			1137.980	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 8 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), jitter at serializer output			1422.222	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, jitter at serializer output			1706.667	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, jitter at serializer output			1991.111	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, jitter at serializer output			2275.556	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 16 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), jitter at serializer output			2844.440	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, jitter at serializer output			3413.328	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, jitter at serializer output			3982.217	ns
BC_GP IO <sub>Jit</sub>	Back channel GPIO jitter, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, jitter at serializer output			4551.105	ns
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 1 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), latency at serializer output			1	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, latency at serializer output			2	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, latency at serializer output			3	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 1 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, latency at serializer output			4	us

## 6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 4 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), latency at serializer output				1	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, latency at serializer output				2	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, latency at serializer output				3	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 4 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, latency at serializer output				4	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 8 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), latency at serializer output				2	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, latency at serializer output				4	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, latency at serializer output				6	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 8 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, latency at serializer output				8	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 16 BC_GPIO	At maximum recommended GPIO rate over one 168.75 Mbps BC (1 des), latency at serializer output				3	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (2 daisy-chained des), input from second des, latency at serializer output				6	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (3 daisy-chained des), input from third des, latency at serializer output				9	us
BC_GP IO <sub>Lat</sub>	Back channel GPIO latency, 16 BC_GPIO	At maximum recommended GPIO rate over two 168.75 Mbps BC (4 daisy-chained des), input from fourth des, latency at serializer output				12	us
t <sub>CLH</sub>	LVCMOS low-to-high transition-time	V <sub>VDD18</sub> , C <sub>L</sub> = 8pF, Default Registers				2	ns
t <sub>CHL</sub>	LVCMOS high-to-low transition-time					2	ns
t <sub>PDB</sub>	PDB reset pulse width	Voltage supplies applied and stable	PDB	500			μs

## 6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{PDB\_D}$	Delay between PDB pulses	Minimum time between reset pulses		2		ms
$t_{PDB\_Glitch}$	PDB glitch filtering	Glitches less than the specified maximum will be ignored (device will not go into reset)		500		ns
<b>FPD-LINK IV TRANSCEIVER</b>						
$f_{FC}$	Forward channel data rate	FPD-Link IV	DOUT0+, DOUT0-, DOUT1+, DOUT1-	10.8	Gbps	
		FPD-Link III <sup>(3)</sup>		6.75		
		ADAS FPD-Link IV		3.375		
		97x ADAS FPD-Link IV		5.67		
		ADAS FPD-Link III		8.4		
				7.55		
				4.16		
$f_{BC}$	Back channel data rate <sup>(1)</sup>	FPD-Link IV FC rate = 10.8 Gbps, 6.75 Gbps or 3.375 Gbps	DOUT0+, DOUT0-, DOUT1+, DOUT1-	168.75	Mbps	
		FPD-Link III		20		
		ADAS FPD-Link IV and ADAS FPD-Link III FC = 8.4 Gbps, 7.55 Gbps, 4.16 Gbps		10		
				5		
				10		
$t_{JIT}$	Output Total Jitter - 10.8 Gbps FPD-Link IV	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	0.30	$UI_{FC}$	
$t_{JIT}$	Output Total Jitter - 6.75 Gbps FPD-Link IV	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	0.25	$UI_{FC}$	
$t_{JIT}$	Output Total Jitter - 5.67 Gbps FPD-Link III <sup>(3)</sup>	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	0.20	$UI_{FC}$	
$t_{JIT}$	Output Total Jitter - 3.375 Gbps FPD-Link IV	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	0.25	$UI_{FC}$	
$t_{JIT}$	Output Total Jitter - 4.16 Gbps ADAS FPD-Link III	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	0.25	$UI_{FC}$	
$t_{JIT}$	Output Total Jitter - 7.55 Gbps ADAS FPD-Link IV	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	0.25	$UI_{FC}$	
$t_{JIT}$	Output Total Jitter - 8.4 Gbps ADAS FPD-Link IV	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	0.25	$UI_{FC}$	
$t_{RF}$	Forward Channel Rise/Fall Time	20% to 80%,		30		ps
$E_{FCH}$	Output Eye Height - 10.8 Gbps NRZ FPD-Link IV	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	370		mVpp
$E_{FCH}$	Output Eye Height - 6.75 Gbps FPD-Link IV	$R_L = 100 \Omega$ . Measured with Type 2 CDR with JTF of 4 MHz, BER rate $10^{-12}$ , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	555		mVpp

## 6.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
E <sub>FCH</sub>	Output Eye Height - 5.67 Gbps FPD-Link III <sup>(3)</sup>	R <sub>L</sub> = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10 <sup>-12</sup> , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	585		mVpp
E <sub>FCH</sub>	Output Eye Height - 3.375 Gbps FPD-Link IV	R <sub>L</sub> = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10 <sup>-12</sup> , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	690		mVpp
E <sub>FCH</sub>	Output Eye Height - 3.675 Gbps FPD-Link III	R <sub>L</sub> = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10 <sup>-12</sup> , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	690		mVpp
E <sub>FCH</sub>	Output Eye Height - 8.4 Gbps ADAS FPD-Link IV	R <sub>L</sub> = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10 <sup>-12</sup> , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	665		mVpp
E <sub>FCH</sub>	Output Eye Height - 7.55 Gbps ADAS FPD-Link IV	R <sub>L</sub> = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10 <sup>-12</sup> , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	515		mVpp
E <sub>FCH</sub>	Output Eye Height - 4.16 Gbps ADAS FPD-Link III	R <sub>L</sub> = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10 <sup>-12</sup> , PRBS15. <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	660		mVpp
f <sub>DEV</sub>	Spread Spectrum Clocking Generation Deviation Frequency Magnitude	Center or Down Spread	DOUT0+, DOUT0-, DOUT1+, DOUT1-	0	0.5	%
f <sub>MOD</sub>	Spread Spectrum Clocking Generation Modulation Frequency		DOUT0+, DOUT0-, DOUT1+, DOUT1-	30	33	kHz
t <sub>TSD</sub>	Serializer Delay	Data in to Data out		245		ns
t <sub>PLL-LT</sub>	PLL Lock Time	PDB to valid FPD-Link output		0.5	2	ms
S <sub>11</sub>	Return Loss of TX	f <sub>FCMAX</sub> =5.4 GHz <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	-10		dB
S <sub>11</sub>	Return Loss of TX	f <sub>BCMIN</sub> = 84.375 MHz <sup>(2)</sup>	DOUT0+, DOUT0-, DOUT1+, DOUT1-	-28		dB

- (1) The backchannel data rate (Mbps) listed is for the encoded back channel data stream. For FPD-Link III, the internal reference frequency used to generate the encoded back channel data stream is two times the back channel datarate. For FPD-Link IV, the internal reference frequency used to generate the encoded back channel data stream is the same as the back channel datarate.
- (2) Measurement includes PCB and recommended external components
- (3) Refer to partner deserializer for maximum data rate. Certain deserializers support up to 105 MHz PCLK.

## 6.7 AC Electrical Characteristics DSI

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
<b>MIPI D-PHY HSRX RECEIVER AC SPECIFICATIONS</b>						
Δ V <sub>CMRX(HF)</sub>	Common-mode Interference HF	Data rate ≤ 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	100		mV

## 6.7 AC Electrical Characteristics DSI (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$\Delta V_{CMRX(HF)}$	Common-mode Interference HF	Data rate > 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		50	mV
$\Delta V_{CMRX(LF)}$	Common-mode Interference LF	Data rate $\leq$ 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-50	50	mV
$\Delta V_{CMRX(LF)}$	Common-mode Interference LF	Data rate > 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-25	25	mV

### MIPI D-PHY LPRX RECEIVER AC SPECIFICATIONS

$T_{MIN-RX}$	Minimum pulse width response	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	20		ns
$V_{INT}$	Peak interference amplitude	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		200	mV

## 6.7 AC Electrical Characteristics DSI (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$f_{INT}$	Interference frequency		DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	450			MHz
<b>MIPI D-PHY CLOCK TIMING SPECIFICATIONS</b>							
$UI_{INST}$	UI instantaneous	150 Mbps to 2.5 Gbps	DSI0_CLKP, DS0_CLKN, DSI1_CLKP, DSI1_CLKN	0.4	6.667	ns	
<b>MIPI D-PHY DATA-CLOCK TIMING SPECIFICATIONS</b>							
$t_{SETUP(RX)}$	Data-to-clock setup time	Data rate 150 Mbps to 1 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-0.15	0.15	UI <sub>HS</sub>	
		Data rate: 1 Gbps to 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-0.2	0.2	UI <sub>HS</sub>	

## 6.7 AC Electrical Characteristics DSI (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{HOLD(RX)}$	Data-to-clock hold time	Data rate < 1 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-0.15	0.15	UI <sub>HS</sub>
		Data rate: 1 Gbps to 1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-0.2	0.2	UI <sub>HS</sub>
$T_{SETUP[RX]} + T_{HOLD[RX]}$ dynamic	RX Data to clock total jitter tolerance	Data rate: 1.5 Gbps to 2.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	0.5		UI <sub>HS</sub>
$T_{SKEW[RX]_s}$ static	RX Static data to clock skew tolerance	Data rate: 1.5 Gbps to 2.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-0.2	0.2	UI <sub>HS</sub>

### MIPI D-PHY RECEIVER RETURN LOSS CHARACTERISTICS

## 6.7 AC Electrical Characteristics DSI (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
SDD <sub>RX</sub>	RX differential return loss	$f_{LPMAX}$	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-18	dB		
			DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN				
		$f_{MAX}$	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-3	dB		
SCC <sub>RX</sub>	RX common-mode return loss	1/4 $f_{INT, MIN}$	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN				
SCC <sub>RX</sub>	RX common-mode return loss	$f_{INT, MIN}, f_{MAX}$ Data Rate: <1.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	-6	dB		

## 6.7 AC Electrical Characteristics DSI (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
SCC <sub>RX</sub>	RX common-mode return loss	$f_{INT, MIN}, f_{MAX}$ Data Rate: 1.5 Gbps to 2.5 Gbps	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		-2.5		dB
SDC <sub>RX</sub>	RX mode conversion	>0 to $f_{MAX}$	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN		-26		dB

### MIPI D-PHY GLOBAL TIMING SPECIFICATIONS

t <sub>CLK-POST</sub> Tolerance	HS exit		DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	60 + 52 × UI		ns
t <sub>CLK-PRE</sub> Tolerance	Time HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode		DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	8		UI
t <sub>CLK-</sub> SETTLE	Time interval during which the HS receiver shall ignore any clock lane HS transitions		DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	95	300	ns

## 6.7 AC Electrical Characteristics DSI (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS termination	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	Time for Dn to reach $V_{TERM-EN}$	38	ns	
$t_{CLK-TRAIL Tolerance}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	60		ns	
$t_{CLK-PREPARE + t_{CLK-ZERO} Tolerance}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the clock	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	300		ns	
$t_{D-TERM-EN}$	Time for the data lane receiver to enable the HS line termination	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	Time for Dn to reach $V_{TERM-EN}$	35 + 4 $\times UI$	ns	
$t_{HS-PREPARE + t_{HS-ZERO} Tolerance}$	$t_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	145 + $10 \times UI$		ns	

## 6.7 AC Electrical Characteristics DSI (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{HS\text{-SETTLE}}$	Time interval during which the HS receiver shall ignore any data lane HS transitions, starting from the beginning of $t_{HS\text{-SETTLE}}$	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	85 + 6 $\times UI$	145 + $10 \times UI$	ns	
$t_{HS\text{-SKIP}}$	Time interval during which the HS-RX should ignore any transitions on the data lane, following a HS burst. The endpoint of the interval is defined as the beginning of the LP-11 state following the HS burst.	DSI0_D0P, DSI0_D0N, DSI0_D1P, DSI0_D1N, DSI0_D2P, DSI0_D2N, DSI0_D3P, DSI0_D3N, DSI0_CLKP, DS0_CLKN, DSI1_D0P, DSI1_D0N, DSI1_D1P, DSI1_D1N, DSI1_D2P, DSI1_D2N, DSI1_D3P, DSI1_D3N, DSI1_CLKP, DSI1_CLKN	40	55 + 4 $\times UI$	ns	

## 6.8 Recommended Timing for the Serial Control Bus

Over I<sup>2</sup>C supply and temperature ranges unless otherwise specified. <sup>(1)</sup>

			MIN	NOM	MAX	UNIT
<b>STANDARD FAST AND FAST-PLUS MODES</b>						
$f_{SCL}$	SCL Clock Frequency	Standard-mode	>0	100	kHz	
$f_{SCL}$	SCL Clock Frequency	Fast-mode	>0	400	kHz	
$f_{SCL}$	SCL Clock Frequency	Fast-mode Plus	>0	1	MHz	
$f_{SCLH}$	SCLH Clock Frequency	High-speed-mode	>0	3.4	MHz	
$t_{LOW}$	SCL Low Period	Standard-mode	4.7			μs
$t_{LOW}$	SCL Low Period	Fast-mode	1.3			μs
$t_{LOW}$	SCL Low Period	Fast-mode Plus	0.5			μs
$t_{LOW}$	SCL Low Period	High-speed-mode	0.16			μs
$t_{HIGH}$	SCL High Period	Standard-mode	4			μs
$t_{HIGH}$	SCL High Period	Fast-mode	0.6			μs
$t_{HIGH}$	SCL High Period	Fast-mode Plus	0.26			μs
$t_{HIGH}$	SCLH High Period	High-speed-mode	0.06			μs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard-mode	4			μs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Fast-mode	0.6			μs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Fast-mode Plus	0.26			μs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	High-speed-mode	0.16			μs
$t_{SU:STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			μs
$t_{SU:STA}$	Set up time for a start or a repeated start condition	Fast-mode	0.6			μs
$t_{SU:STA}$	Set up time for a start or a repeated start condition	Fast-mode Plus	0.26			μs

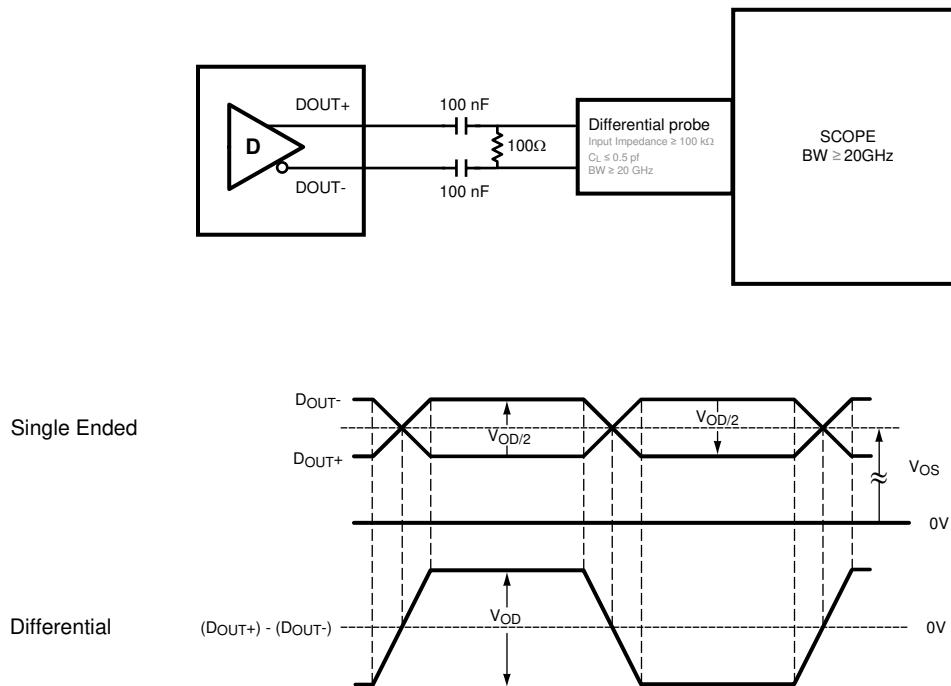
## 6.8 Recommended Timing for the Serial Control Bus (continued)

Over I<sub>2</sub>C supply and temperature ranges unless otherwise specified. (1)

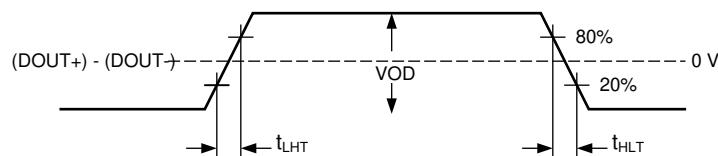
			MIN	NOM	MAX	UNIT
t <sub>SU:STA</sub>	Set up time for a start or a repeated start condition	High-speed-mode		0.16		μs
t <sub>HD:DAT</sub>	Data hold time	Standard-mode	0	3.45		μs
t <sub>HD:DAT</sub>	Data hold time	Fast-mode	0	0.9		μs
t <sub>HD:DAT</sub>	Data hold time	Fast-mode Plus	0	0.45		μs
t <sub>HD:DAT</sub>	Data hold time	High-speed-mode	0	0.07		μs
t <sub>SU:DAT</sub>	Data set up time	Standard-mode	250			ns
t <sub>SU:DAT</sub>	Data set up time	Fast-mode	100			ns
t <sub>SU:DAT</sub>	Data set up time	Fast-mode Plus	50			ns
t <sub>SU:DAT</sub>	Data set up time	High-speed-mode	10			ns
t <sub>SU:STO</sub>	Set up time for STOP condition	Standard-mode	4			μs
t <sub>SU:STO</sub>	Set up time for STOP condition	Fast-mode	0.6			μs
t <sub>SU:STO</sub>	Set up time for STOP condition	Fast-mode Plus	0.26			μs
t <sub>SU:STO</sub>	Set up time for STOP condition	High-speed-mode	0.16			μs
t <sub>BUF</sub>	Bus free time between STOP and START	Standard-mode	4.7			μs
t <sub>BUF</sub>	Bus free time between STOP and START	Fast-mode	1.3			μs
t <sub>BUF</sub>	Bus free time between STOP and START (FPD-Link IV, FPD-Link III with PCLK ≥ 50 MHz, ADAS compatibility mode)	Fast-mode Plus	0.5			μs
t <sub>BUF</sub>	Bus free time between STOP and START (FPD-Link III mode, PCLK < 50 MHz)	Fast-mode Plus	1			μs
t <sub>r</sub>	SCL and SDA rise time	Standard-mode		1000		ns
t <sub>r</sub>	SCL and SDA rise time	Fast-mode		300		ns
t <sub>r</sub>	SCL and SDA rise time	Fast-mode Plus		120		ns
t <sub>f</sub>	SCL and SDA fall time	Standard-mode		300		ns
t <sub>f</sub>	SCL and SDA fall time	Fast-mode		300		ns
t <sub>f</sub>	SCL and SDA fall time	Fast-mode Plus		120		ns
t <sub>f</sub>	SCL and SDA fall time	High-speed-mode	10	40		ns
C <sub>b</sub>	Capacitive load for each bus line	Standard-mode		400		pF
C <sub>b</sub>	Capacitive load for each bus line	Fast-mode		400		pF
C <sub>b</sub>	Capacitive load for each bus line	Fast-mode Plus		550		pF
C <sub>b</sub>	Capacitive load for each bus line	High-speed-mode		100		pF
t <sub>VD:DAT</sub>	Data valid time	Standard-mode		3.45		μs
t <sub>VD:DAT</sub>	Data valid time	Fast-mode		0.9		μs
t <sub>VD:DAT</sub>	Data valid time	Fast-mode Plus		0.45		μs
t <sub>VD:ACK</sub>	Data valid acknowledge time	Standard-mode		3.45		μs
t <sub>VD:ACK</sub>	Data valid acknowledge time	Fast-mode		0.9		μs
t <sub>VD:ACK</sub>	Data valid acknowledge time	Fast-mode Plus		0.45		μs
t <sub>SP</sub>	Input filter	Standard-mode		50		ns
t <sub>SP</sub>	Input filter	Fast-mode		50		ns
t <sub>SP</sub>	Input filter	Fast-mode Plus		50		ns
t <sub>SP</sub>	Input filter	High-speed-mode		10		ns

(1) Max C<sub>b</sub> = 100 pF for High-speed Mode (100 pF - 400 pF range is not supported)

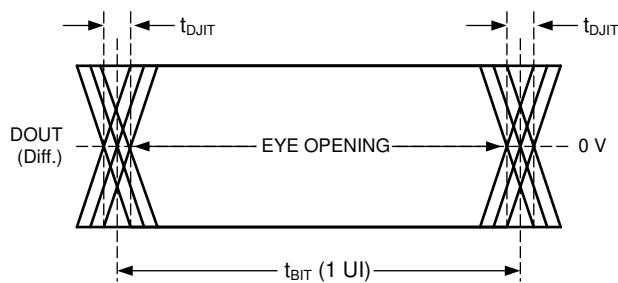
## 6.9 Timing Diagrams



**Figure 6-1. Serializer Output  $V_{OD}$   $V_{ID}$**



**Figure 6-2. Output Transition Times**



**Figure 6-3. Serializer Output Jitter**

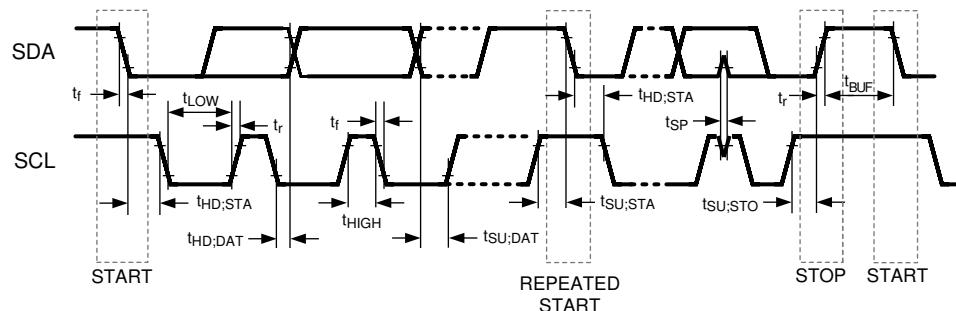


Figure 6-4. Serial Control Bus Timing Diagram

## 7 Detailed Description

### 7.1 Overview

The DS90UH981-Q1 converts MIPI Display Serial Interface (DSI) to an FPD-Link III/IV interface. The D-PHY receivers (up to 4 lanes + 1 clock) support up to 2.5 Gbps per lane, with a total bandwidth of 10 Gbps per port. This device transmits an FPD-Link IV output over a single coax/STP cable operating up to 10.8 Gbps line rate or Dual Coax/STP cable operating up to 21.6 Gbps line rate. The serial stream contains an embedded clock, video control signals, DSI video data, control information, and audio data. The payload is DC-balanced to enhance signal quality and is AC coupled. The DS90UH981-Q1 serializer is primarily intended for use with DS90Ux984-Q1, and DS90Ux988-Q1 deserializers, or the DS90Ux948-Q1, DS90Ux940-Q1, DS90Ux940N-Q1, DS90Ux926-Q1, DS90UB924-Q1, and DS90Ux928-Q1 deserializers in backwards compatible mode. In ADAS mode the DS90UH981-Q1 serializer can be paired with an ADAS deserializer such as the DS90UB936-Q1, DS90UB954-Q1, DS90UB960-Q1, DS90UB962-Q1, DS90UB9702-Q1 or DS90UB9722-Q1. In backward compatible mode, The DS90UH981-Q1 supports HDCP v1.4 with integrated on-chip keys when working with HDCP capable deserializers.

The DS90UH981-Q1 serializer and companion deserializer incorporate an I<sub>2</sub>C compatible interface. The I<sub>2</sub>C interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer and deserializer as well as remote I<sub>2</sub>C target devices. The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I<sub>2</sub>C transactions across the serial link from one I<sub>2</sub>C bus to another. The implementation allows for arbitration with other I<sub>2</sub>C compatible controllers at either side of the serial link.

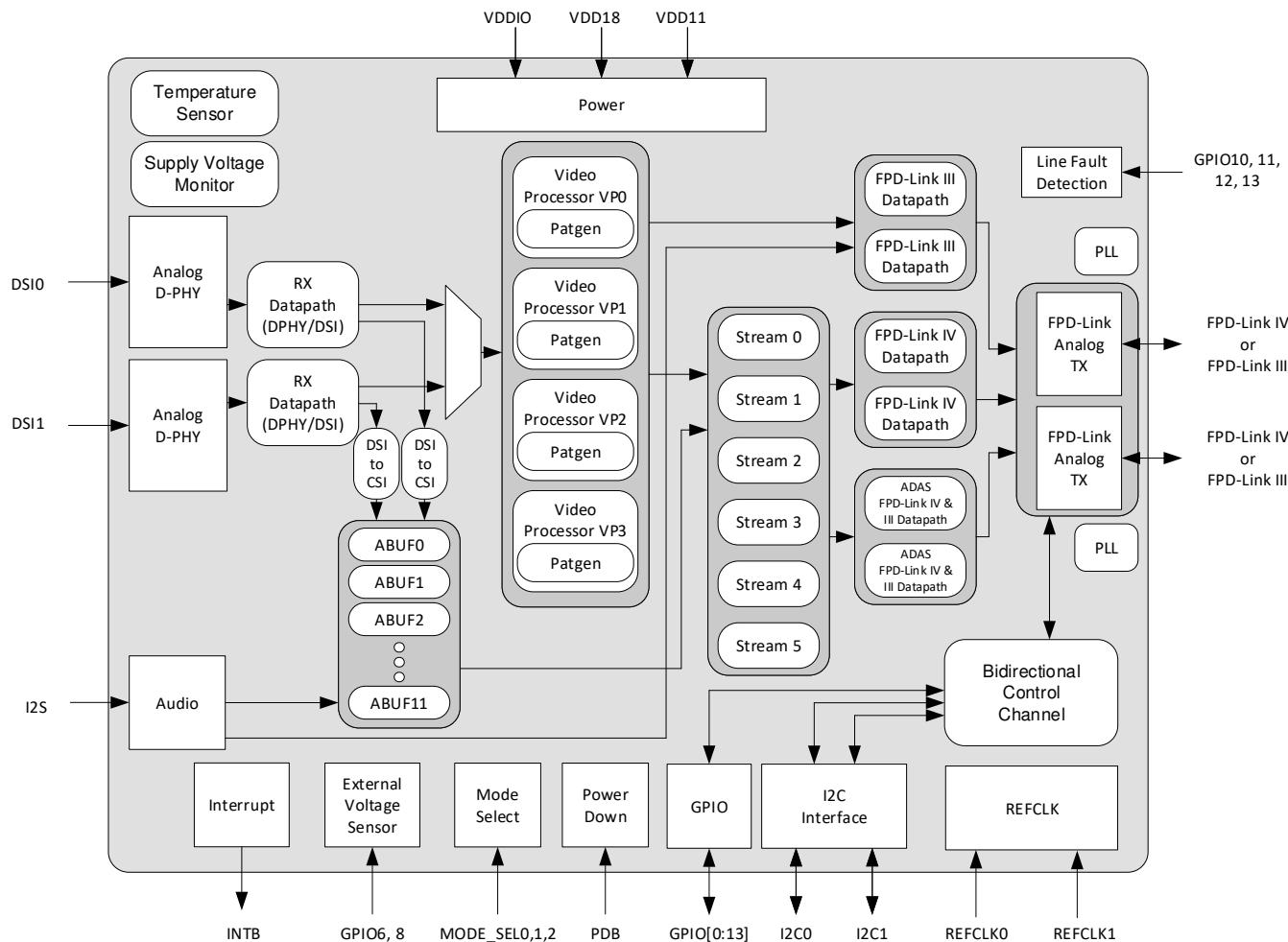
**Table 7-1. Features**

FUNCTION	DESCRIPTION
<b>DATA RATES</b>	
Forward Channel Line Rate	Up to 21.6 Gbps over STQ/Dual-coax or 10.8 Gbps per STP/Coax (including frame and coding overhead) Discrete rates of 10.8 Gbps, 6.75 Gbps and 3.375 Gbps available per FPD-Link IV lane Minimum 8 MHz PCLK for FPD-Link IV
Forward D-PHY Rate	10 Gbps per D-PHY port (2.5 Gbps per lane over 4 lanes), up to 20 Gbps over dual D-PHY port
Back Channel Rate	168.75 Mbps for FPD-Link IV
<b>INTERFACE</b>	
Cable	FPD-Link III/IV, NRZ signaling <ul style="list-style-type: none"> <li>• 50Ω coaxial single-ended cable</li> <li>• 100Ω differential STP</li> </ul>
System	D-PHY v1.2 <ul style="list-style-type: none"> <li>• Configurable 1, 2, 3, 4 lanes</li> <li>• 150 Mbps - 2.5 Gbps per lane</li> <li>• DSI v1.3.1</li> </ul>
Control	I <sub>2</sub> C, GPIO, and SPI <ul style="list-style-type: none"> <li>• 1MHz I<sub>2</sub>C (3.4 MHz local bus access)</li> <li>• High-Speed GPIO</li> <li>• Supports SPI and UART passthrough over GPIOs</li> </ul>
<b>NETWORKING TOPOLOGIES</b>	

**Table 7-1. Features (continued)**

FUNCTION	DESCRIPTION
Topologies	<ul style="list-style-type: none"> <li>Point-to-point topology</li> <li>Daisy-chain (when used with DS90Ux98x-Q1 deserializer)</li> <li>One –to –Many Y topology</li> <li>SuperFrame splitting</li> <li>Video aggregation</li> <li>Virtual Channel Support</li> </ul>
<b>DATA PROTECTION</b>	
Video	<ul style="list-style-type: none"> <li>Error detection on serializer input with error counter and alarm signal</li> </ul>
Control	<ul style="list-style-type: none"> <li>Errors are communicated back to serializer via I2C NACK and link alarm bit.</li> </ul>
<b>BACKWARD COMPATIBILITY</b>	
Forward Channel Line Rate	Backwards compatible rates of 875 Mbps to 5.67 Gbps available per FPD-Link III lane Backwards compatible mode supports a PCLK range of 25 MHz to 162 MHz single or 50 MHz to 324 MHz in dual mode (limited by deserializer capability)
Back Channel Rate	Backwards compatible rates of 5, 10, 20 Mbps for FPD-Link III
HDCP v1.4	HDCP v1.4 is supported in backward compatible mode when paired with HDCP-capable deserializers
<b>ADAS COMPATIBILITY</b>	
ADAS FPD-Link IV	Compatible with the DS90UB9702 and DS90UB9722 deserializers
ADAS FPD-Link III	<ul style="list-style-type: none"> <li>Compatible with the DS90UB960 and DS90UB962 deserializers</li> <li>Compatible with the DS90UB954 deserializer</li> <li>Compatible with the DS90UB936 deserializer</li> </ul>
<b>HEALTH MONITORING AND DIAGNOSTICS</b>	
Alarm	Alarm bit configurable to trigger on link status, bit errors, etc
Voltage & Temperature	<ul style="list-style-type: none"> <li>Measures up to 2 external voltages</li> <li>Measure internal die temperature</li> <li>8-bit resolution</li> </ul>
BIST	Pseudo-random bit sequence (PRBS) Built-in self test (BIST) function
Line Fault Detect	Serial link line fault monitor to detect power supply short, short to ground, or open.
ESD Event Counter	Detects and tracks number of ESD events trigger the devices ESD protection.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 DSI Receiver

The DS90UH981-Q1 features two separate MIPI D-PHY v1.2 compliant input ports that support DSI v1.3.1. Selection of DSI input port is made through the DSI\_PORT\_SEL bit in the BRIDGE\_CTL register. Each port allows 1-, 2-, 3-, or 4-lane operation. The number of lanes for both ports is controlled by the DSI\_LANES field in the BRIDGE\_CTL register and is set at power up through a strap option on the MODE\_SEL0 pin. Automatic lane detection is not supported. The DS90UH981-Q1 supports both continuous and non-continuous clocking modes on the DSI interface. The DSI lane ordering can be reversed internally and independently for each of the two D-PHY ports, using the DSI1\_LANE\_REVERSE or DSI0\_LANE\_REVERSE fields in the DSI\_DEVICE\_CFG register 0xB0:

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**Table 7-2. DSI0\_LANE\_REVERSE and DSI1\_LANE\_REVERSE Input Pins and Assignment**

DSI Input Pins	DSI Assignment
DSI_DEVICE_CFG:DSI0_LANE_REVERSE = 1	
DSI0_D3P/N	Port 0 Lane 0 P/N
DSI0_D2P/N	Port 0 Lane 1 P/N
DSI0_D1P/N	Port 0 Lane 2 P/N
DSI0_D0P/N	Port 0 Lane 3 P/N
DSI_DEVICE_CFG:DSI1_LANE_REVERSE = 1	
DSI1_D3P/N	Port 1 Lane 0 P/N
DSI1_D2P/N	Port 1 Lane 1 P/N
DSI1_D1P/N	Port 1 Lane 2 P/N
DSI1_D0P/N	Port 1 Lane 3 P/N

In addition, the DSI clock and data lane polarity can be inverted internally and independently for each of the two D-PHY ports using Page 5 0x16 (DSI Port 0) and Page 7 0x16 (DSI Port 1).

**Table 7-3. DSI0\_DATA\_PN\_SWAP Input Pins and Assignment**

DSI Input Pins	DSI Assignment
DSI_DEVICE_CFG:DSI0_DATA_PN_SWAP = 1	
DSI0_D3P	Port 0 Lane 3N
DSI0_D3N	Port 0 Lane 3P
DSI0_D2P	Port 0 Lane 2N
DSI0_D2N	Port 0 Lane 2P
DSI0_D1P	Port 0 Lane 1N
DSI0_D1N	Port 0 Lane 1P
DSI0_D0P	Port 0 Lane 0N
DSI0_D0N	Port 0 Lane 0P
DSI_DEVICE_CFG:DSI0_CLK_PN_SWAP = 1	
DSI0_CLKP	DSI0_CLKN
DSI0_CLKN	DSI0_CLKP

**Table 7-4. DSI1\_DATA\_PN\_SWAP Input Pins and Assignment**

DSI Input Pins	DSI Assignment
DSI_DEVICE_CFG:DSI1_DATA_PN_SWAP = 1	
DSI1_D3P	Port 1 Lane 3N
DSI1_D3N	Port 1 Lane 3P
DSI1_D2P	Port 1 Lane 2N
DSI1_D2N	Port 1 Lane 2P
DSI1_D1P	Port 1 Lane 1N
DSI1_D1N	Port 1 Lane 1P
DSI1_D0P	Port 1 Lane 0N
DSI1_D0N	Port 1 Lane 0P
DSI_DEVICE_CFG:DSI1_CLK_PN_SWAP = 1	
DSI1_CLKP	DSI1_CLKN
DSI1_CLKN	DSI1_CLKP

### 7.3.1.1 DSI Operating Mode

The D-PHY receiver can support High-Speed (HS) continuous and burst mode for fast data traffic and Low Power mode for control transactions. Low power data transmission and low power escape modes are not supported. During data transmission, data lane is in High-Speed mode. When data is not being sent, data lanes can either transition to low power mode or remain in HS mode and send null or blanking packets. There is a transition state to take the D-PHY from a Normal mode to the Low-Power state.

The sequence to enter High-Speed mode is: LP-11, LP-01, LP-00 at which point the Data Lane remains in High-Speed mode until a Stop state (LP-11) is received.

The D-PHY receiver supports the three different DSI video mode interface timing formats: non-burst with sync pulses, non-burst mode with sync events, or burst mode

- Non-burst with sync pulses: This mode allows the DSI RX to accurately reconstruct original video timing, including sync pulse widths. The DSI TX transmits both the start and end of sync pulses for accurate timing regeneration.
- Non-burst with sync events: This mode allows the DSI RX to accurately reconstruct original video timing, but accurate reconstruction of sync pulse widths is not required. The DSI TX transmits only the start of the sync pulse.
- Burst: This mode allows pixel data to be sent over a shorter duration using time-compressed burst format, and after HS data transmission the bus can enter Low Power Mode. This mode can reduce the power consumption.

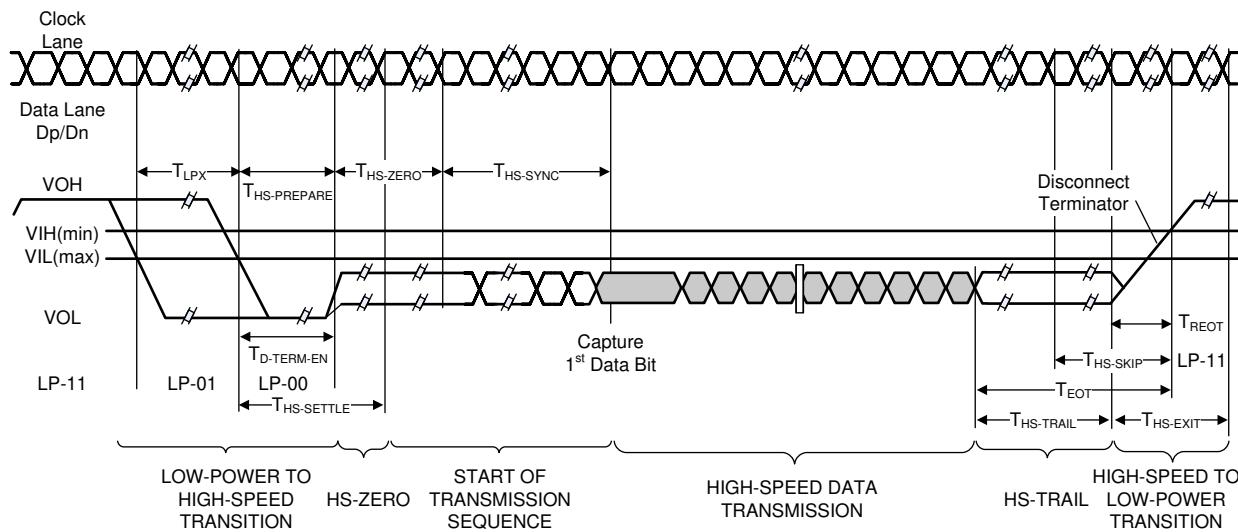
When using sync event mode, set 0x20[4] = 0 on Page\_4/Page\_6 for DSI port 0/1 respectively.

The DS90UH981-Q1's DSI receiver does not support bidirectional communication, therefore Bus Turn-around (BTA) is not supported.

According to the MIPI DSI v1.3.1 standard section 8.11.1, a DSI source must periodically end HS transmission and drive the data lanes to the LP-11 state at least once per frame to enable PHY synchronization. Make sure that the DSI source follows the MIPI DSI standard closely and enables LP-11 during at least one of the Blanking or Low Power periods of each video frame.

#### 7.3.1.1.1 High-Speed Mode

During high-speed data transmission, the digital D-PHY enables the termination signal to allow proper termination of the HS RX, and the LP RX must stay at LP-00 state. Both DSI data lane and clock lane operate in the same manner. The DS90UH981-Q1 supports DSI continuous clock lane mode where the clock LP RX stays at LP-00 state.



**Figure 7-1. Switching the Clock Lane Between Clock Transmission and Low-Power Mode**

### 7.3.1.1.2 Global Operation Timing Parameters

MIPI D-PHY v1.2 defines global operation timing for both D-PHY TX and RX. The DS90UH981-Q1 implements the following RX timing parameters:

- $t_{CLK-MISS}$
- $t_{CLK-SETTLE}$  (programmable)
- $t_{CLK-TERM-EN}$  (programmable)
- $t_{D-TERM-EN}$  (programmable)
- $t_{HS-SETTLE}$  (programmable)
- $t_{HS-SKIP}$  (programmable)
- $t_{INIT}$  target (programmable)
- $t_{EOT}$  parameter is not supported.

### 7.3.1.2 T-SKIP Programming

The D-PHY data lanes include the ability to ignore the final data bits during HS data transfer. The number of bits to be ignored is programmed into the D-PHY\_SKIP\_TIMING register on Page\_4 of the device Indirect Registers.

The TSKIP\_CNT field must be programmed based on the operating DSI clock frequency to meet the D-PHY THS-SKIP timing requirement. The TSKIP\_CNT value (dec) is defined in [Equation 1](#), where  $f_{DSI}$  is the DSI clock frequency in MHz. [Table 7-5](#) shows a couple of example TSKIP\_CNT values derived based on the given DSI clock frequency,  $f_{DSI}$ . TSKIP\_CNT value (in decimal) must be rounded to the closest even number; odd values are not valid.

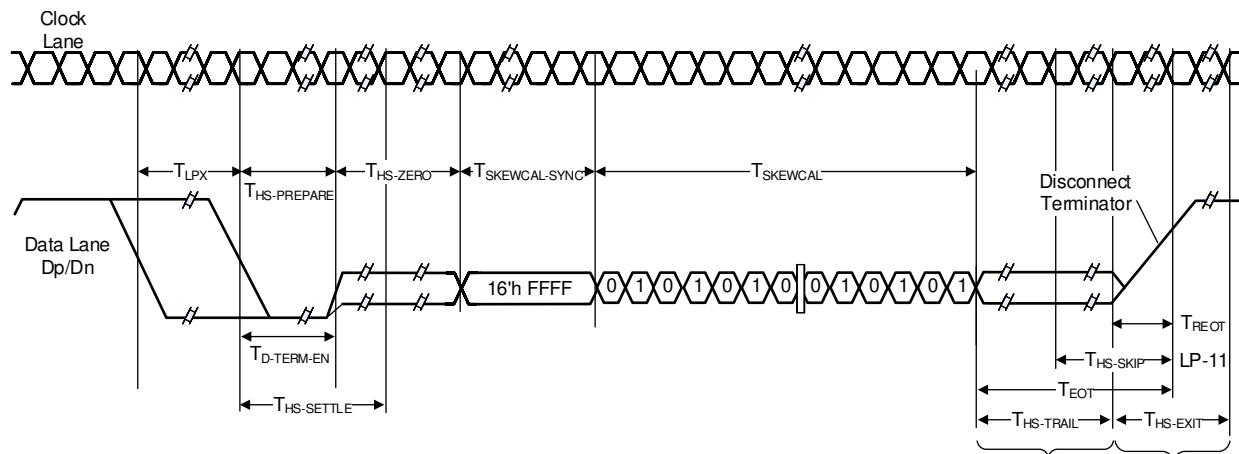
$$\text{TSKIP\_CNT} = \text{ROUND}((130 * f_{dsi}) / 4000 - 3) \quad (1)$$

**Table 7-5. TSKIP\_CNT Settings as a Function of  $f_{DSI}$  Examples**

$f_{DSI}$ [MHz]	TSKIP_CNT (dec)	DSI Indirect Register 0x05[6:1] (bin)	DSI Indirect Register 0x05 Setting (hex)
225	4	000100	0x08
315	6	000110	0x0c

### 7.3.1.3 DSI Skew Calibration

The D-PHY Receiver skew calibration shall be initiated by the D-PHY transmitter when the D-PHY is greater than 1.5 Gbps per lane. The DSI\_CAL\_EN should be set to a 1 to enable skew calibration. The D-PHY transmitter will send a deskew sequence before transmitting high speed data. This deskew sequence sent by the D-PHY transmitter will contain a 16 UI sync pattern of all 1's followed by a clock pattern(101010...) of at least 32768 UI and a maximum of 100us.



**Figure 7-2. DSI Skew Calibration Sequence**

### 7.3.1.3.1 DSI Skew Calibration Override

The setting of DSI\_CAL\_EN must be set to match the configuration of the DSI source. If Skew Calibration is enabled at the DSI source, then DSI\_CAL\_EN of the DS90UH981-Q1 should be set to 1. Skew Calibration can be enabled for each port using the port-specific script provided below.

```
## ****
## Enable Skew Calibration for PORT0
## ****
board.writeI2C(devAddr,0x40,0x14) #Writing to Page 5 D-PHY Analog P0
board.writeI2C(devAddr,0x41,0x21) #SKEW_CAL_CFG0_P0
board.writeI2C(devAddr,0x42,0xC0)
board.writeI2C(devAddr,0x41,0x2E) #SKEW_CAL_CFG1_P0
board.writeI2C(devAddr,0x42,0x40)
board.writeI2C(devAddr,0x41,0x31) #SKEW_CAL_CFG2_P0
board.writeI2C(devAddr,0x42,0x00)

## ****
## Enable Skew Calibration for PORT1
## ****
board.writeI2C(devAddr,0x40,0x1C) #Writing to Page 7 D-PHY Analog P1
board.writeI2C(devAddr,0x41,0x21) #SKEW_CAL_CFG0_P1
board.writeI2C(devAddr,0x42,0xC0)
board.writeI2C(devAddr,0x41,0x2E) #SKEW_CAL_CFG1_P1
board.writeI2C(devAddr,0x42,0x40)
board.writeI2C(devAddr,0x41,0x31) #SKEW_CAL_CFG2_P1
board.writeI2C(devAddr,0x42,0x00)
```

If Skew Calibration is disabled at the DSI source, then DSI\_CAL\_EN of the DS90UH981-Q1 should be set to 0. Skew Calibration can be disabled for each port using the port-specific script provided below.

```
## ****
## Disable Skew Calibration for PORT0
## ****
board.writeI2C(devAddr,0x40,0x14) #Writing to Page 5 D-PHY Analog P0
board.writeI2C(devAddr,0x41,0x21) #SKEW_CAL_CFG0_P0
board.writeI2C(devAddr,0x42,0xD0)
board.writeI2C(devAddr,0x41,0x2E) #SKEW_CAL_CFG1_P0
board.writeI2C(devAddr,0x42,0x00)
board.writeI2C(devAddr,0x41,0x31) #SKEW_CAL_CFG2_P0
board.writeI2C(devAddr,0x42,0x02)

## ****
## Disable Skew Calibration for PORT1
## ****
board.writeI2C(devAddr,0x40,0x1C) #Writing to Page 7 D-PHY Analog P1
board.writeI2C(devAddr,0x41,0x21) #SKEW_CAL_CFG0_P1
board.writeI2C(devAddr,0x42,0xD0)
board.writeI2C(devAddr,0x41,0x2E) #SKEW_CAL_CFG1_P1
board.writeI2C(devAddr,0x42,0x00)
board.writeI2C(devAddr,0x41,0x31) #SKEW_CAL_CFG2_P1
board.writeI2C(devAddr,0x42,0x02)
```

### 7.3.1.4 DSI Errors and Status

#### 7.3.1.4.1 DSI / D-PHY Error Detection and Reporting

The DS90UH981-Q1 detects and reports DSI errors for each lane via the DPHY\_DLАНEx\_ERR registers on indirect register Page\_4 for Port 0 and Page\_6 for Port 1:

- SoT Error
- SoT Sync Error
- EoT Sync Error

#### 7.3.1.4.2 DSI Protocol Error Detection

The DSI protocol error detection can be read from the DPHY\_DSI\_ERR\_RPT registers (0x2B and 0x2C) found on page\_4 and page\_6. The 12 different error detection statuses are:

- DSI\_NO\_EOTPKT : End of Transmit without EOT packet

- IS\_INV\_TYPE\_GLW\_ERR: Invalid Type on Generic Long Write packet
- IS\_INV\_WC\_GLW\_ERR: Invalid Word Count on Generic Long Write packet
- IS\_INV\_VC\_ERR: Invalid virtual channel errors
- IS\_INV\_DT\_ERR: Invalid data type errors
- IS\_CHECKSUM\_ERR: 16-bit CRC Checksum errors
- IS\_ECC\_MULTI\_ERR: Multi-bit ECC errors
- IS\_ECC\_SINGLE\_ERR: Single bit ECC errors
- HS RX TO ERROR: HS Receive timeout error
- EOT\_SYNC\_ERROR: EOT Sync error
- SOT SYNC ERROR: SOT Sync error
- SOT ERROR: SOT error

The error flags are cleared by writing INTR\_CTL\_DSI\_ERR (0x25) = 0x01 on Page\_4/Page\_6.

The DS90UH981-Q1 expects the DSI source to send EoTp, so if the source does not generate EoTp, then the DS90UH981-Q1 reports an error condition, if enabled.

#### 7.3.1.4.3 DSI Error Reporting

The main register page register 0xB1 DSI\_ERROR has two status bits related to DSI Errors. Bit 7 is the DSI\_ERROR status bit, which ORs all of the DSI error bits within the indirect registers. If dual DSI is enabled, the DSI0 and DSI1 error bits are OR'd together. However, if only one DSI port is enabled, then the status bit only shows the error bits within that DSI port. This bit does not clear on read. All of the error status bits must be cleared within the DSI indirect register Page\_4 and Page\_6. Bit 6 is the DPHY\_ERROR status bit, which ORs all of the DPHY error bits within the indirect registers. It works similarly to the DSI\_ERROR bit in that the DPHY\_ERROR bit only shows the errors of the D-PHY port enabled and is not cleared on read. All of the error status bits must be cleared within the D-PHY indirect register Page\_4 and Page\_6.

There are two registers that show all of the errors that could be causing the IS\_DPHY\_LANE\_ERROR (0x0E[0]) bit under INTR\_STS\_DPHY (0x0E) register (Page\_4 and Page\_6) to be set. This error report comes from the DSI logic and is spread over INTR\_STS\_DPHY\_ERR\_FIFO\_OVR (0x24) and INTR\_CTL\_DSI\_ERR (0x25) registers. The error report registers are cleared when reading registers. The optimal register read order for checking the DSI errors is to read the DSI\_ERROR register within the main registers, check the error report registers for an error, then read the INTR\_STS\_DPHY\_ERR\_FIFO\_OVR (0x24) and INTR\_CTL\_DSI\_ERR (0x25) registers on Page\_4 or Page\_6 for other errors and to clear the error report registers.

#### 7.3.1.4.4 DSI Error Counter

The DSI Error Counter increments on errors detected by the DSI Protocol logic. The DSI Error counter is located in the DSI\_DPHY\_ERR\_CNT register on Page\_4 and Page\_6 for DSI0 and DSI1, respectively. Each type of error can be enabled independently. If an error indication is enabled, the error counter increments if that condition is detected. Error conditions are enabled by setting the controls in the INTR\_STS\_DSI\_ERR and INTR\_STS\_DPHY\_ERR\_FIFO\_OVR registers on Page\_4 and Page\_6 Indirect Registers.

#### 7.3.1.5 Supported DSI Video Formats

The DS90UH981-Q1 supports five DSI RGB video formats:

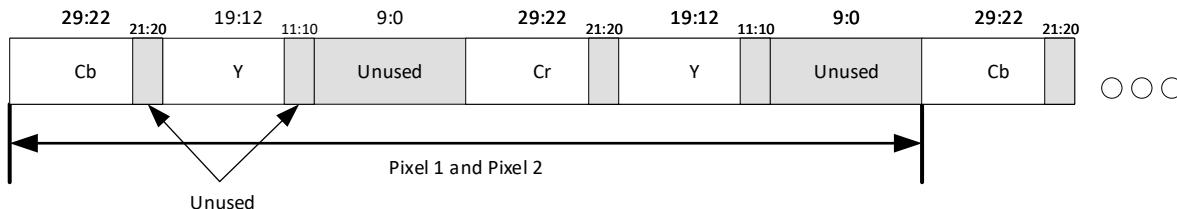
- RGB (Packed Pixel Stream, 30-bit Format, Data Type 0x0D)
- RGB888 (Packed Pixel Stream, 24-bit Format, Data Type 0x3E)
- RGB666 (Packed Pixel Stream, 18-bit Format, Data Type 0x1E)
- RGB565 (Packed Pixel Stream, 16-bit Format, Data Type 0x0E)
- RGB666 (Loosely Packed Pixel Stream, 18-bit format in Three Bytes, Data Type 0x2E)

The RGB video formats are automatically converted, if necessary, to 3-byte RGB888 for transmission over FPD-Link III.

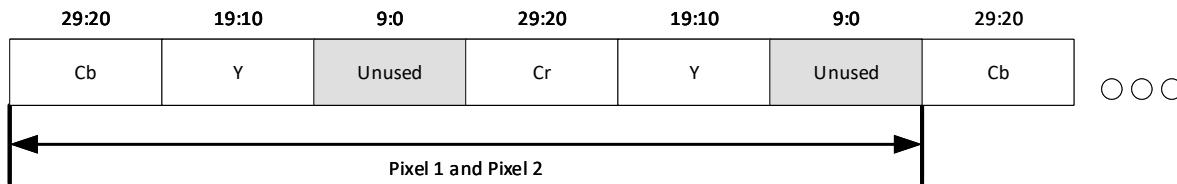
The DS90UH981-Q1 also supports pass-through of two DSI YCbCr video formats:

- Packed Pixel Stream, 16-bit YCbCr 4:2:2 Format, Data Type 0x2C
- Loosely Packed Pixel Stream, 20-bit YCbCr 4:2:2 Format, Data Type 0x0C

Each of the YCbCr formats is aligned to the 30-bit-per-pixel forward channel format shown below. When using YCbCr formats use 30 bpp to calculate FPD-Link bandwidth.



**Figure 7-3. FPD-Link 16-bit YCbCr 4:2:2 Format**



**Figure 7-4. FPD-Link 20-bit YCbCr 4:2:2 Format**

Refer to the deserializer datasheet for compatibility with the YCbCr format.

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#### Note

Typically, RGB pixel data is sent with one full horizontal video line of pixels in a single packet. The case of horizontal video line of active pixels divided into two or more packets is not supported.

### 7.3.2 FPD-Link IV High Speed Forward Channel Data Transfer

The High Speed Forward Channel transmits data according to the FPD-Link IV protocol. FPD-Link IV consists of 132-bit units of data transmission, referred to as frames. FPD-Link IV frames can transmit RGB data, sync signals, I<sup>2</sup>C, and GPIOs transmitted from serializer to deserializer. Each 132-bit frame can include up to 128 bits of RGB data. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. FPD-Link IV protocol allows for up to four distinct streams to be transferred over a single link. To manage the bandwidth allocation of the FPD-Link, each FPD-Link includes 65 different time slots which are divided up between the different FPD-Link streams.

The FPD-Link IV serial stream rate supports fixed-rates of 10.8 Gbps, 6.75 Gbps and 3.375 Gbps . When operating over both FPD-Link channels, a total data rate of 21.6 Gbps, 13.6 Gbps and 6.75 Gbps is supported, respectively.

#### 7.3.2.1 FPD-Link Streams

FPD-Link IV protocol supports transferring up to six distinct streams over a single link. FPD-Link streams can be used to transmit video or other data. Up to four streams can be used to send video data by mapping the outputs of the four video processors (VPs) to an FPD-Link stream. See [Section 7.3.2.5](#).

#### 7.3.2.2 FPD-Link Timeslots

There are 65 total timeslots in dual mode and 65 total slots per link layer in independent mode, which are used to divide the available FPD-Link bandwidth between different streams. Ensure that the video bandwidth does not exceed the FPD-Link IV bandwidth. The number of timeslots allocated to each stream are configured through the LINK0\_SLOT\_REQx and LINK1\_SLOT\_REQx in Page\_11 registers (0x06, 0x07, 0x08, 0x09, 0x16, 0x17, 0x18, and 0x19). Video streams can be assigned based on system needs (i.e. all four video streams can be assigned to Link Layer 0 or split across both Link Layer 0 and Link Layer 1). When assigning time slots, if fewer than 65 timeslots are requested, the additional timeslots are assigned to Stream 0. If greater than 65 timeslots are requested (an invalid configuration), priority is given to lower stream numbers. Timeslot assignments are updated only after the EN\_NEW\_TSLOTx bit is set. In Dual FPD-Link mode only the Link Layer 0 registers are

used. In general, timeslots can be assigned based on the proportion of the available bandwidth required by the individual stream. For example with a FPD-Link single link or independent with a data rate of 10.8 Gbps which supports up to 10.47 Gbps throughput (10.8 Gbps x 128/132), each timeslot accounts for a bandwidth of 161 Mbps (10.47 Gbps / 65). For a system configured to dual FPD-Link with 10.8 Gbps data rate per lane, the total bandwidth is 20.94 Gbps (2 x (10.8 Gbps x 128/132)). Each timeslot accounts for 322 Mbps (20.94 Gbps / 65). The time slot assignments are considered static and can not be modified during video transmission. It is recommended to adhere to the following procedure when modifying time slot assignments:

1. Disable the link layer (set LINK\_LAYER\_x\_EN = 0)
2. Disable all video processors used on the link (set VPx\_ENABLE= 0)
3. Configure time slots through LINK0\_SLOT\_REQx and LINK1\_SLOT\_REQx registers
4. Set EN\_NEW\_TSLOTx = 1
5. Enable the link layer (set LINK\_LAYER\_x\_EN = 1)
6. Enable all video processors used on the link (set VPx\_ENABLE= 1)

#### 7.3.2.2.1 Example Timeslot Assignment

1. Calculate the required bandwidth for each image by multiplying the PCLK by the number of bits per pixel.
  - EX: Stream 0: PCLK = 200 MHz with 30 bpp. Required bandwidth = 200 MHz \* 30 bpp = 6.0 Gbps
  - Stream 1: PCLK = 112 MHz with 24 bpp. Required bandwidth = 112 MHz \* 24 bpp = 2.688 Gbps
2. Calculate the proportion of the available bandwidth needed for each stream and the corresponding number of timeslots (Stream Bandwidth / Available Bandwidth \* Total Number of Timeslots rounded up).
  - EX: Stream 0: Proportion of Available Bandwidth = 6.0 Gbps / 10.47 Gbps = 0.57.
  - Number of Timeslots =  $65 \times 0.57 = 37.05 \approx 38$  Timeslots
  - Stream 1: Proportion of Available Bandwidth = 2.688 Gbps / 10.47 Gbps = 0.25.
  - Number of Timeslots =  $65 \times 0.25 = 16.25 \approx 17$  Timeslots
3. Verify the total number of timeslots is less than 65.
  - EX: 38 Timeslots for Stream 0 + 17 Timeslots for Stream 1 = 55
  - Timeslots is < 65 Timeslots so this configuration is valid.
4. (Optional) Assign extra timeslots evenly between streams. If this step is skipped, the remaining timeslots will be assigned to Stream 0.
  - EX: 65 - 55 = 10 remaining timeslots. Add 5 timeslots to Stream 0 and 5 timeslots to Stream 1. Stream 0 can be assigned 43 timeslots total (LINKx\_SLOT\_REQ0 = 43) and Stream 1 can be assigned 22 timeslots total (LINKx\_SLOT\_REQ1= 22).

#### 7.3.2.3 FPD-Link PLL

The FPD-Link forward channel is generated based on a phase locked loop (PLL) as shown in [Figure 7-5](#). In general, this PLL can select between REFCLK0 and REFCLK1 for the reference source. For FPD-Link IV, the 27 MHz connected to REFCLK0 must be used as the reference source. The PLL settings are automatically set at device start up according to the devices MODE\_SEL settings. This is the default setting and can be confirmed by checking the register CHx\_FPD3\_REFCLK1 = 0 (0x5[7] or 0x5[6]). In FPD-Link IV mode, the output of the PLL must be 5.4 GHz (10.8 Gbps/2 bits), 3.375 GHz (6.75 Gbps/2 bits or 3.375 Gbps/1 bit) as a result of FPD-Link mode set to full-rate mode in HALFRATE\_MODE\_CHx[7:6]. This output frequency is generated using the following settings, programmable via Page 2 of the indirect access registers. After modifying PLL values, reset the PLL using either PLL\_CH0\_RESET or PLL\_CH1\_RESET Field in RESET\_CTL register 0x01.

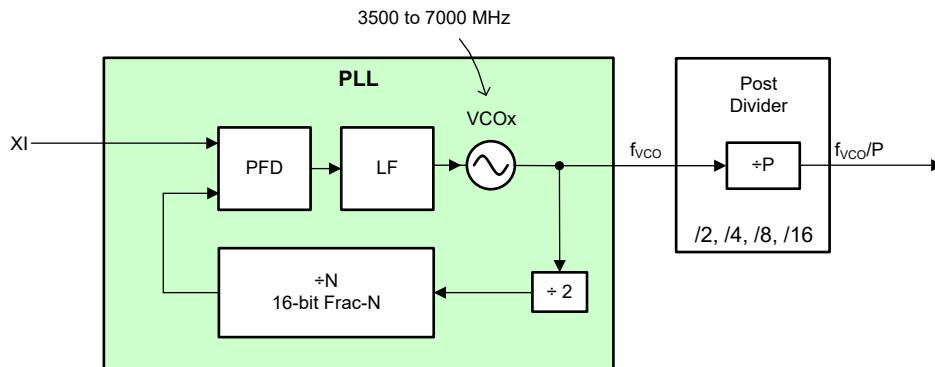
The following equation is used to calculate the VCO frequency:

- $f_{VCO}$  is the VCO frequency
- P is the post-divider value (1, 2, 4, 8, 16)

$$f_{VCO} = f_{REF} \times 2 \times \left[ N + \left( \frac{NUM}{DEN} \right) \right] \quad (2)$$

where

- $f_{REF}$  is the reference frequency, either from the REFCLK0 or REFCLK1
- N is the integer portion of the N-divider (0 to 65,535)
- NUM is the numerator portion of the N-divider fraction (0 to 16,777,206), NUM ≤ DEN
- DEN is the denominator portion of the N-divider fraction (1 to 16,777,206)

**Figure 7-5. FPD-Link IV PLL****Table 7-6. FPD-Link IV PLL Settings for 10.8 Gbps, 6.75 Gbps and 3.375 Gbps**

FPD-Link Data Rate	10.8 Gbps	6.75 Gbps	3.375 Gbps
FPD-Link Back Channel Rate		168.7 Mbp	
Reference Source		REFCLK0 (CHx_FPD3_REFCLK1 = 0 )	
N-Divider	100 (NDIV[7:0] = 0x64, NDIV[15:8] = 0x00)	125 (NDIV[7:0] = 0x7D, NDIV[15:8] = 0x00)	
Numerator	0 (NUM[7:0] = 0x00, NUM[15:8] = 0x00, NUM[23:16] = 0x00)		
Denominator		16,777,206 (DEN[7:0] = 0xF6, DEN[15:8] = 0xFF, DEN[23:16] = 0xFF)	
MASH Order		Integer (MASH_ORDER = 0x0)	
Post-Divider	1 (POST_DIV = 0x0)	2 (POST_DIV = 0x1)	2 (POST_DIV = 0x1)
FPD-Link PLL Frequency	5.4 GHz	3.375 GHz	3.375 GHz
Nyquist Frequency	5.4 GHz	3.375 GHz	1.6875 GHz
Back Channel Sampling Rate		1 (BC_DOWNSAMPLING_RATE = 0x0)	
Back Channel Configuration	6 (BC_CONFIG = 0x6)	0 (BC_CONFIG = 0x0)	0 (BC_CONFIG = 0x0)
Half Rate Mode	1 (HALFRATE_MODE_CHx = 0x1)	1 (HALFRATE_MODE_CHx = 0x1)	0 (HALFRATE_MODE_CHx = 0x0)

**Table 7-7. FPD-Link ADAS PLL Settings for 4.16 Gbps, 7.55 Gbps and 8.4 Gbps**

FPD-Link Data rate	4.16 Gbps	7.55 Gbps	8.4 Gbps
Reference Source		REFCLK0 (CHx_FPD3_REFCLK1 = 0 )	
N-Divider	77 (NDIV[7:0] = 0x4D, NDIV[15:8] = 0x00)	69 (NDIV[7:0] = 0x45, NDIV[15:8] = 0x00)	77 (NDIV[7:0] = 0x4D, NDIV[15:8] = 0x00)

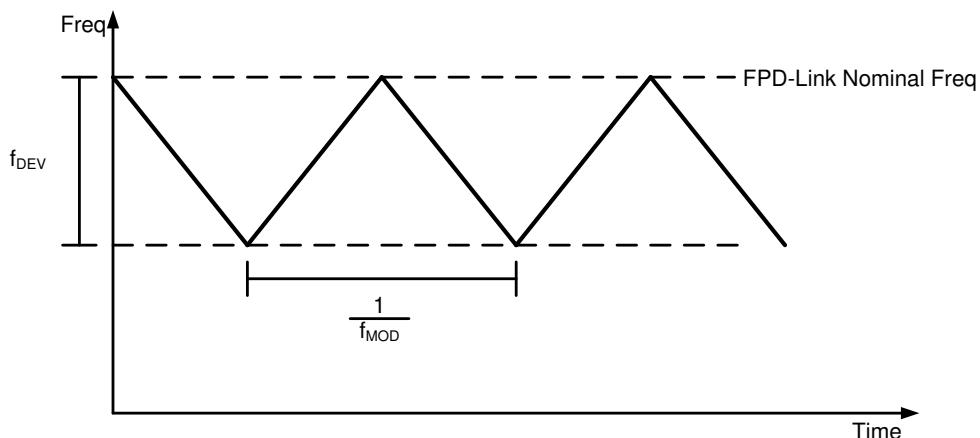
**Table 7-7. FPD-Link ADAS PLL Settings for 4.16 Gbps, 7.55 Gbps and 8.4 Gbps (continued)**

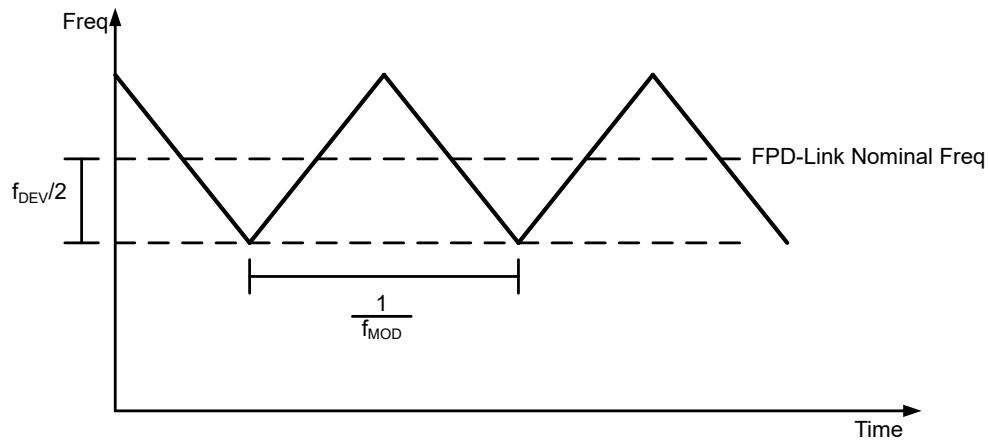
FPD-Link Data rate	4.16 Gbps	7.55 Gbps	8.4 Gbps
<b>Numerator</b>	621,378 (NUM[7:0] = 0x42, NUM[15:8] = 0x7B, NUM[23:16] = 0x09)	15,223,761 (NUM[7:0] = 0xD1, NUM[15:8] = 0x48, NUM[23:16] = 0xE8)	13,048,938 (NUM[7:0] = 0x6A, NUM[15:8] = 0x1C, NUM[23:16] = 0xC7)
<b>Denominator</b>	16,777,206 (DEN[7:0] = 0xF6, DEN[15:8] = 0xFF, DEN[23:16] = 0xFF)	16,777,206 (DEN[7:0] = 0xF6, DEN[15:8] = 0xFF, DEN[23:16] = 0xFF)	16,777,206 (DEN[7:0] = 0xF6, DEN[15:8] = 0xFF, DEN[23:16] = 0xFF)
<b>MASH Order</b>	Fractional (MASH_ORDER = 0x02)		
<b>Post-Divider</b>	2 (POST_DIV = 0x1)	1 (POST_DIV = 0x0)	1 (POST_DIV = 0x0)
<b>FPD-Link Frequency</b>	2.08 GHz	3.775 GHz	4.2 GHz
<b>Back Channel Sampling Rate</b>	2 (BC_DOWNSAMPLING_RATE = 0x1)	1 (BC_DOWNSAMPLING_RATE = 0x1)	2 (BC_DOWNSAMPLING_RATE = 0x1)
<b>Back Channel Configuration</b>	0 (BC_CONFIG = 0x0)	0 (BC_CONFIG = 0x0)	0 (BC_CONFIG = 0x0)
<b>Half Rate Mode</b>	1 (HALFRATE_MODE_CHx = 0x1)	1 (HALFRATE_MODE_CHx = 0x1)	1 (HALFRATE_MODE_CHx = 0x1)

### 7.3.2.4 Spread Spectrum Clock Generation (SSCG)

If desired, spread spectrum clocking can be enabled for the FPD-Link IV forward channel ranging between 30 kHz and 33 kHz modulation frequency. FPD-Link IV forward channel and back channel SSCG cannot exceed 0.5% frequency deviation. When paired in backward compatible mode with DS90Ux948-Q1 deserializers in FPD-Link III, the frequency deviation cannot exceed 0.3%. Both center-spread and down-spread ramps are supported. The deserializer spread spectrum capabilities must be checked to ensure proper spread spectrum compatibility. It is recommended to use center-spread SSC such that the average FPD-Link rate is maintained. If down-spread is desired, this will reduce the FPD-Link bandwidth and must be considered in bandwidth calculations. SSC configurations must be chosen such that the final display can tolerate the variation in the PCLK. In FPD-Link IV mode, the effects of SSC must be considered when choosing the appropriate M and N values.

The FPD PLL must be configured in fractional mode to enable SSCG. If the PLL was originally configured in integer mode (NUM[23:0] = 0), set NUM[23:0] equal to the value of DEN[23:0], and subtract one from the original NDIV[15:0] value. Additionally, set MASH\_ORDER to fractional mode (e.g. MASH\_ORDER[2:0] = 2). For instance, to enable SSCG using the default FPD-Link IV PLL settings set NDIV = 124 and NUM[23:0] = 16,777,206. To configure spread spectrum clock generation, the following equations can be used to calculate the RAMPX\_STOP and RAMPX\_INC.

**Figure 7-6. Down Spread SSCG**

**Figure 7-7. Center Spread SSCG**

$$\text{RAMPX\_STOP} = \frac{f_{\text{REF}}}{(4 \times f_{\text{MOD}})} \quad (3)$$

where

- $f_{\text{REF}}$  is the reference clock in kHz (27 MHz in FPD-Link IV Mode)
- $f_{\text{MOD}}$  is the modulation frequency in kHz

$$\text{RAMPX\_INC}_{\text{Initial}} = \frac{(VCO\_freq \times f_{\text{DEV}} \times \text{DEN}_{\text{Initial}})}{(\text{REFCLK} \times 2 \times 100 \times i_{\text{SPREAD}} \times \text{RAMPX\_STOP})} \quad (4)$$

- $\text{RAMPX\_INC}_{\text{Initial}}$  must be rounded to an integer number

where

- $f_{\text{DEV}}$  is the deviation frequency as a percentage of the forward channel frequency (Example: deviation frequency = 0.5% corresponds to  $f_{\text{DEV}} = 0.5$ )
- $i_{\text{SPREAD}} = 2$
- $\text{DEN}_{\text{Initial}}$  is the denominator of the N-divider in the FPD PLL (16,777,206 for FPD-Link IV Mode)
- $\text{REFCLK}$  is the reference clock frequency in MHz (27)
- $VCO\_freq$  is the VCO frequency in MHz

$$x = \begin{cases} \log_2 \frac{\text{RAMPX\_INC}_{\text{Initial}}}{32767}, & \text{RAMPX\_INC}_{\text{Initial}} > 32767 \\ 0, & \text{RAMPX\_INC}_{\text{Initial}} \leq 32767 \end{cases} \quad (5)$$

where

- $x$  must be rounded up to the nearest integer

$$\text{RAMPX\_INC}_{\text{Final}} = \frac{(VCO\_freq \times f_{\text{DEV}} \times \text{DEN}_{\text{Initial}})}{(\text{REFCLK} \times 2 \times 100 \times i_{\text{SPREAD}} \times \text{RAMPX\_STOP} \times 2^x)} \quad (6)$$

$$\text{DEN}_{\text{Final}} = \left( \frac{\text{DEN}_{\text{Initial}}}{2^x} \right) \quad (7)$$

$$\text{NUM}_{\text{Final}} = \left( \frac{\text{NUM}_{\text{Initial}}}{2^x} \right) \quad (8)$$

where

- Initial numerator and denominator are determined based on the FPD-Link rate. If the original PLL setting is integer mode (numerator = 0) then the first step of applying SSCG is to convert to fractional mode (subtract one from the integer part of the n divider and set both numerator and denominator to 16,777,206).

$$\text{VCO}_{\text{Freq,Final}} = f_{\text{REF}} \times 2 \left[ \text{Ndiv} + \left( \frac{\text{NUM}_{\text{Final}}}{\text{DEN}_{\text{Final}}} \right) \right] \quad (9)$$

$$f_{\text{DEV,Final}} = \left[ \frac{(\text{RAMPX\_INC}_{\text{Final}} \times \text{REFCLK} \times 2 \times 100 \times i_{\text{SPREAD}} \times \text{RAMPX\_STOP})}{(\text{VCO}_{\text{Freq,Final}} \times \text{DEN}_{\text{Final}})} \right] \quad (10)$$

For instance, to configure SSCG with  $f_{\text{MOD}} = 30 \text{ KHz}$  SSCG with down-spread  $f_{\text{DEV}} = 0.5\%$  frequency deviation and a reference clock of 27 MHz in FPD-Link IV Mode at a VCO frequency of 6.75 GHz.

$$\text{RAMPX\_STOP} = \frac{f_{\text{REF}}}{(4 \times f_{\text{MOD}})} \quad (11)$$

$$\text{RAMPX\_STOP} = \frac{27 \times 10^6}{(4 \times 30 \times 10^3)} = 225$$

$$\text{RAMPX\_INC}_{\text{Initial}} = \frac{(VCO\_freq \times f_{\text{DEV}} \times \text{DEN}_{\text{Initial}})}{(\text{REFCLK} \times 2 \times 100 \times i_{\text{SPREAD}} \times \text{RAMPX\_STOP})} \quad (12)$$

$$\text{RAMPX\_INC}_{\text{Initial}} = \frac{(6.75 \times 10^9 \times 0.5 \times 16,777,206)}{(27 \times 10^6 \times 2 \times 100 \times 2 \times 225)} = 23301.675 \approx 23302$$

$$x = \log_2 \left( \frac{23302}{32767} \right) = -0.49179 \approx 0$$

$$\text{RAMPX\_INC}_{\text{Final}} = \frac{(VCO\_freq \times f_{\text{DEV}} \times \text{DEN}_{\text{Initial}})}{(\text{REFCLK} \times 2 \times 100 \times i_{\text{SPREAD}} \times \text{RAMPX\_STOP} \times 2^x)} \quad (13)$$

$$\text{RAMPX\_INC}_{\text{Final}} = \frac{(6.75 \times 10^9 \times 0.5 \times 16,777,206)}{(27 \times 10^6 \times 2 \times 100 \times 2 \times 225 \times 2^0)} = 23301.675 \approx 23302$$

$$\text{DEN}_{\text{Final}} = \left( \frac{\text{DEN}_{\text{Initial}}}{2^x} \right) \quad (14)$$

$$\text{DEN}_{\text{Final}} = \left( \frac{16,777,206}{2^0} \right) = 16,777,206$$

$$\text{NUM}_{\text{Final}} = \left( \frac{\text{NUM}_{\text{Initial}}}{2^x} \right) \quad (15)$$

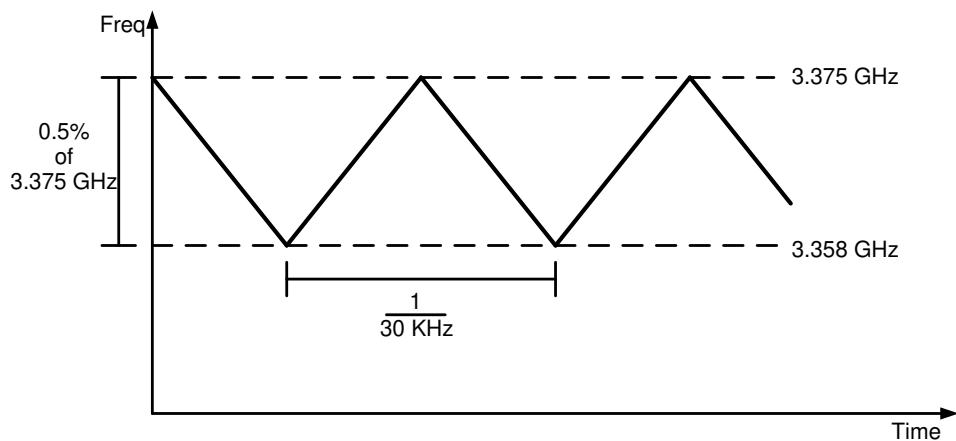
$$\text{NUM}_{\text{Final}} = \left( \frac{16,777,206}{2^0} \right) = 16,777,206$$

$$\text{VCO}_{\text{Freq,Final}} = f_{\text{REF}} \times 2 \left[ \text{Ndiv} + \left( \frac{\text{NUM}_{\text{Final}}}{\text{DEN}_{\text{Final}}} \right) \right] \quad (16)$$

$$\text{VCO}_{\text{Freq,Final}} = 27 \times 10^6 \times 2 \left[ 124 + \left( \frac{16,777,206}{16,777,206} \right) \right] = 27 \times 10^6 \times 250 = 6.75 \times 10^9$$

$$f_{\text{DEV,Final}} = \left[ \frac{(\text{RAMPX\_INC}_{\text{Final}} \times \text{REFCLK} \times 2 \times 100 \times i_{\text{SPREAD}} \times \text{RAMPX\_STOP})}{(\text{VCO}_{\text{Freq,Final}} \times \text{DEN}_{\text{Final}})} \right] \quad (17)$$

$$f_{\text{DEV,Final}} = \left[ \frac{(23302 \times 27 \times 10^6 \times 2 \times 100 \times 2 \times 225)}{(6.75 \times 10^9 \times 16,777,206)} \right] = 0.5$$



**Figure 7-8. Down Spread SSCG Example**

#### 7.3.2.5 FPD-Link IV Stream Configuration

Each FPD-Link channel can transmit data from up to four video processors (VP0 to VP3). To forward the video stream from the video processor, the video stream must first be enabled via the `LINK0_STREAM_EN` register for FPD-Link Port 0 or the `LINK1_STREAM_EN` register for FPD-Link Port 1 (Page\_11 indirect registers 0x01 and 0x11). The `LINKx_STREAM_EN` register is used to select which video streams are linked to each FPD-Link port. Once the video streams are linked to an FPD-Link port, the video streams must be mapped to the desired FPD-Link streams using the `LINK0_MAP_REGx` and `LINK1_MAP_REGx` registers (Page\_11 registers 0x02, 0x03, 0x12 and 0x13). In Dual FPD-Link Mode, only `LINK0_STREAM` registers is used. Video streams can be mapped to multiple video processors to create duplicate copies of one image. In the independent mode, there are six FPD-Link streams available per FPD-Link port. Mapping of VPs and ABUFF are similar to the single/dual mode of operation. For FPD-Link III video stream mapping, see [Section 7.3.21.1.1](#).

**Table 7-8. Video Stream Forwarding**

Video Processor	FPD-Link Port	Enable
VPx	FPD-Link Port 0	Enable: LINK0_STREAM_EN[x] = 1 Disable: LINK0_STREAM_EN[x] = 0
	FPD-Link Port 1	Enable: LINK1_STREAM_EN[x] = 1 Disable: LINK1_STREAM_EN[x] = 0

**Table 7-9. Video Stream Mapping**

Video Processor	FPD-Link Port	FPD-Link Stream
VPx	FPD-Link Port 0 <sup>(1)</sup>	Stream 0: LINK0_STREAM_MAP0 = x Stream 1: LINK0_STREAM_MAP1 = x Stream 2: LINK0_STREAM_MAP2 = x Stream 3: LINK0_STREAM_MAP3 = x Stream 4: LINK0_STREAM_MAP4 = x Stream 5: LINK0_STREAM_MAP5 = x
	FPD-Link Port 1 <sup>(1)</sup>	Stream 0: LINK1_STREAM_MAP0 = x Stream 1: LINK1_STREAM_MAP1 = x Stream 2: LINK1_STREAM_MAP2 = x Stream 3: LINK1_STREAM_MAP3 = x Stream 4: LINK1_STREAM_MAP4 = x Stream 5: LINK1_STREAM_MAP5 = x

- (1) Each of the four video processors can be mapped to only a single FPD-Link stream, meaning a maximum of four video streams can be transmitted by the FPD-Link IV serializer.

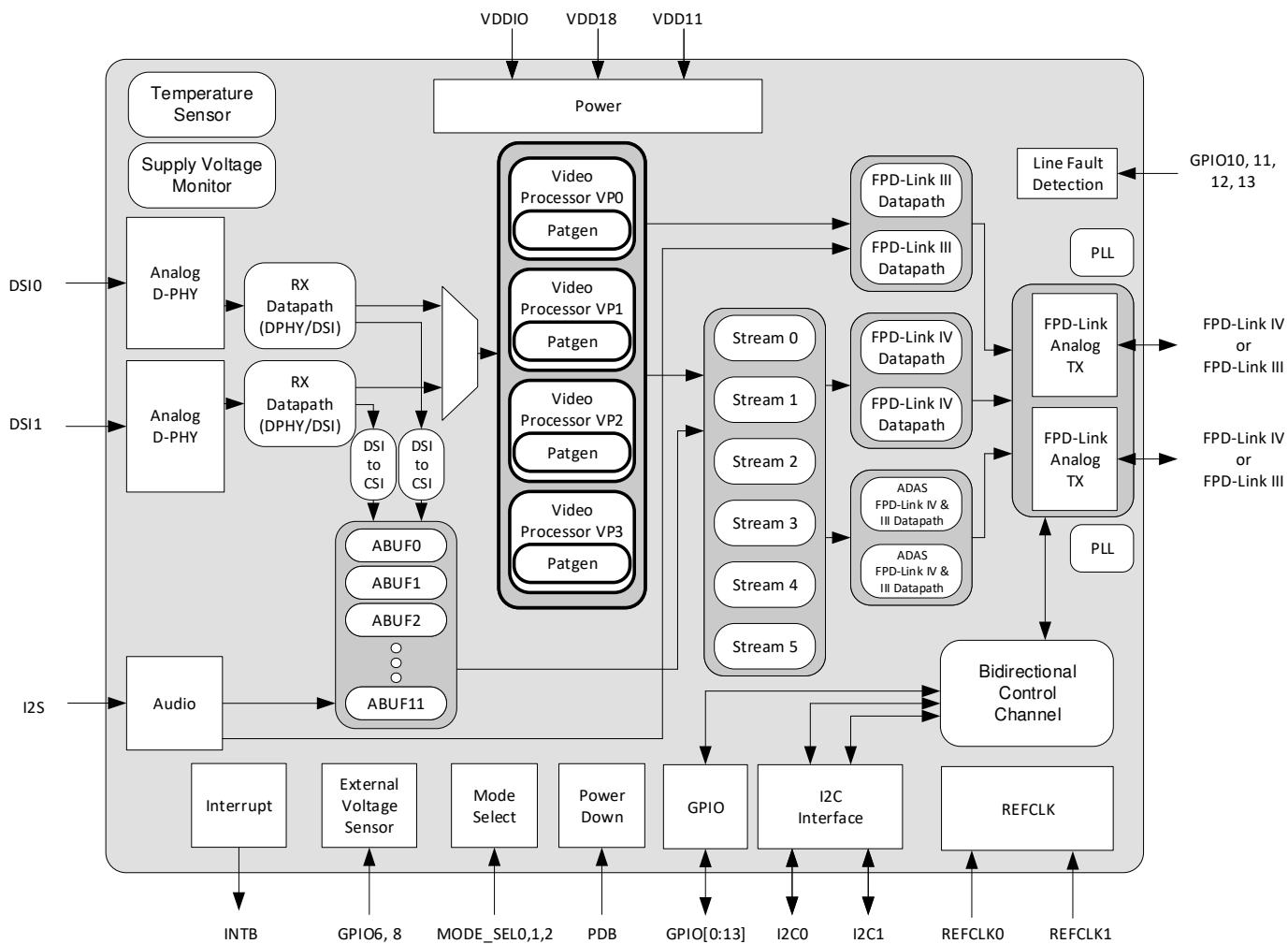
**Table 7-10. Stream Mapping Input**

Stream Map	Stream's Input
LINK0_STREAM_MAPx	0x0 = Video Processor 0
	0x1 = Video Processor 1
	0x2 = Video Processor 2
	0x3 = Video Processor 3

### 7.3.3 Back Channel Data Transfer

The back channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as BCC (Bidirectional Control Channel) frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high speed forward channel. The back channel frame consists of 30 bits which contain the I<sup>2</sup>C, CRC and four bits of standard GPIO information with a 168.75 Mbps line rate (when paired with an FPD-Link IV deserializer).

### 7.3.4 Video Processor



**Figure 7-9. Video Processor Block Diagram**

The DS90UH981-Q1 contains video processors (VP) to process the input video frames before sending the video across the link. There are four video processors allowing for four different video streams to be sent across the FPD-Link. Each of the video processors can modify and send out only one video stream each. The video processors need to store each active pixel of a single horizontal line of the video the video processor is sending out. The pixel storage for each video processor must be set in the NUM\_VID\_STREAMS (0x43[2:0]) register. The video processor regenerates the timing of the video being processed. The input videos to the video processors come from the DSI ports. Each video processors input can be selected independent of each other and more than one video processor can share inputs. The video processors can take in SuperFrames and convert the multi image frame into a single image to send across FPD-Link. The video processors can use the following tools to modify the video:

- Vertical Filtering
- Video Cropping
- Timing Generation
- Alternate Pixel Splitting
- Merge

The video processor is where the pattern generator is located. This allows for up to four patterns to be generated and sent out.

### 7.3.4.1 Input Configuration

The video processor must first be enabled via the VP\_ENABLE\_REG register 0x44 and then the video stream of interest is selected through registers VC\_SEL\_D-PHY01 (0xBD) and VC\_SEL\_D-PHY\_23 (0xBE). The pixel width must also be specified as 18-bit, 24-bit, or 30-bit. The LSB of video data is dropped if the input video data is higher bit per pixel than the selected pixel width.

**Table 7-11. Input Selection Parameters**

Enable Video Processor	Select D-PHY port and VC-ID	Set Pixel Width
Enable: VPx_ENABLE = 1 Disable: VPx_ENABLE = 0	Selects the output of D-PHY to be presented as the inputs to VPx  0 : Virtual Channel 0 input from D-PHY0 1 : Virtual Channel 1 input from D-PHY0 2 : Virtual Channel 2 input from D-PHY0 3 : Virtual Channel 3 input from D-PHY0 4 : Virtual Channel 0 input from D-PHY1 5 : Virtual Channel 1 input from D-PHY1 6 : Virtual Channel 2 input from D-PHY1 7 : Virtual Channel 3 input from D-PHY1	18-bit: VPx_WIDTH = 0 24-bit: VPx_WIDTH = 1 30-bit: VPx_WIDTH = 2

### 7.3.4.2 Timing Generation

To properly regenerate the video timing, the video processor must be programmed for the correct operating frequency and video parameters. The timing generator runs on a fixed frequency clock and typically inserts or removes pixels prior to the horizontal sync pulse if required. Timing is based on a quad-pixel clock, so pixels are inserted or removed as quad-pixels. The clock generator includes an adaption capability to allow operating slightly faster or slower to minimize the need for correction to blanking intervals. The following parameters must be set for proper timing generation for each video processor via registers on Page\_12: VID\_H\_ACTIVE, VID\_H\_BACK, VID\_H\_WIDTH, VID\_H\_TOTAL, VID\_V\_ACTIVE, VID\_V\_BACK, VID\_V\_WIDTH, and VID\_V\_FRONT. For HSYNC width, there is a minimum requirement for the video processor of 12 pixels and 8 pixels in FPD-Link IV and FPD-Link III respectively. The total horizontal blanking has a recommended minimum of 100 pixels. The processor computes the horizontal front porch timing from the other horizontal parameters. Video timing parameter requirements are listed in [Timing Generation Parameters](#). Vertical blanking parameters must match the vertical blanking of the SuperFrame after vertical filtering and cropping.

To allow video timing to stabilize, the timing generator can be programmed to drop initial video frames. By default, the timing generator discards the first frame (which can be a partial frame), and can discard up to three frames by programming the VP\_DROP\_FRAMES field. If the first video line of the subsequent frame is not available at the end of vertical blanking, the timing generator can be programmed either to wait for the video line (default) or to insert additional horizontal sync pulses until the next line arrives.

**Timing Generation Parameters**

Register Name	Timing Parameter Name	Description	Requirements	Equation
VID_H_ACTIVE	Horizontal Active	The total active horizontal period in number of pixels.		VID_H_ACTIVE = CROP_STOP_X - CROP_START_X + 1
H_ACTIVE_SHA_DOW	Horizontal Active	The total active horizontal period in number of pixels.		SOURCE_H_ACTIVE = VID_H_ACTIVE
VID_H_BACK	Horizontal Back Porch	The horizontal back porch in number of pixels.	Must be divisible by 4	VID_H_BACK = Desired Horizontal Back Porch

**Timing Generation Parameters (continued)**

Register Name	Timing Parameter Name	Description	Requirements	Equation
VID_H_WIDTH	Horizontal Sync	The width of the horizontal sync in number of pixels.	<ul style="list-style-type: none"> <li>Must be divisible by 4</li> <li>For FPD-Link IV must be at least 12 pixels</li> <li>For FPD-Link III must be at least 8 pixels</li> </ul>	VID_H_WIDTH = Desired Horizontal Sync
VID_H_TOTAL	Horizontal Total	The total horizontal width in number of pixels, including the active period, front porch, back porch, and horizontal sync.	Must be divisible by 4	VID_H_TOTAL = VID_H_ACTIVE + VID_H_BACK + VID_H_WIDTH + Desired Horizontal Front Porch
VID_V_ACTIVE	Vertical Active	The total active vertical period in number of lines.		VID_V_ACTIVE = CROP_STOP_Y - CROP_START_Y + 1
V_ACTIVE_SHA_DOW	Vertical Active	The total active vertical period in number of lines.		SOURCE_V_ACTIVE = VID_V_ACTIVE
VID_V_BACK	Vertical Back Porch	The vertical back porch in number of lines		VID_V_BACK = Original Image Vertical Back Porch x A/N + CROP_START_Y
VID_V_FRONT	Vertical Front Porch	The vertical front porch in number of lines.		VID_V_FRONT = Original Image Vertical Front Porch x A/N + Original Image Active Vertical - CROP_STOP_Y - 1
VID_V_WIDTH	Vertical Sync	The width of the vertical sync in number of lines.		VID_V_WIDTH = Original Image Vertical Sync x A/N

**7.3.4.2.1 Video Processor Frequency**

In FPD-Link IV mode the video processor operates based on a quad-pixel clock generated based on the forward channel rate divided by 40. An M/N divider is programmed to generate the desired quad-pixel clock. For example, when the FPD-Link IV forward channel is configured for 6.75 Gbps, the reference clock is 6.75 Gbps / 40 bits = 168.75 MHz. The video processor clock operates on a quad-pixel basis so that M/N divider must be programmed to 1/4 of the video stream's pixel clock frequency by setting PCLK\_GEN\_M and PCLK\_GEN\_N on Page 12, the video processor register page. PCLK\_GEN\_M is a 15-bit value, controlling the numerator, while the denominator N is equal to  $2^{\text{PCLK\_GEN\_N}}$ . PCLK\_GEN\_N value can range from 0 to 15, allowing a denominator of up to 32,768. Typically, N must be set to 32,768. For example, to create a 150 MHz pixel clock requires a quad-pixel clock of 37.5 MHz. If PCLK\_GEN\_N is set to the default of 15,  $\text{PCLK\_GEN\_M} = 37.5 * (2^{15}) / 270 = 4551.111$ . Choosing an M value of 4551, this produces an effective PCLK of 149.996 MHz, an offset of 31 ppm from the target PCLK.

$$\text{Video Processor Clock} = \text{Target PCLK} / 4 \quad (18)$$

$$\text{Video Processor Clock} = (\text{FC data rate} / 40) \times \text{PCLK\_GEN\_M} / (2^{\text{PCLK\_GEN\_N}}) \quad (19)$$

$$\text{PCLK\_GEN\_M} = \text{Video Processor Clock} \times (2^{\text{PCLK\_GEN\_N}}) / (\text{FC data rate} / 40) \quad (20)$$

If using down spread spectrum the bandwidth of the forward channel data rate is reduced and must be taken into account when calculating the PCLK\_GEN\_M and PCLK\_GEN\_N values.

**Table 7-12. Maximum PCLK for each video processor**

BPP	Max PCLK (MHz)
24	1080
18	1349
30	864

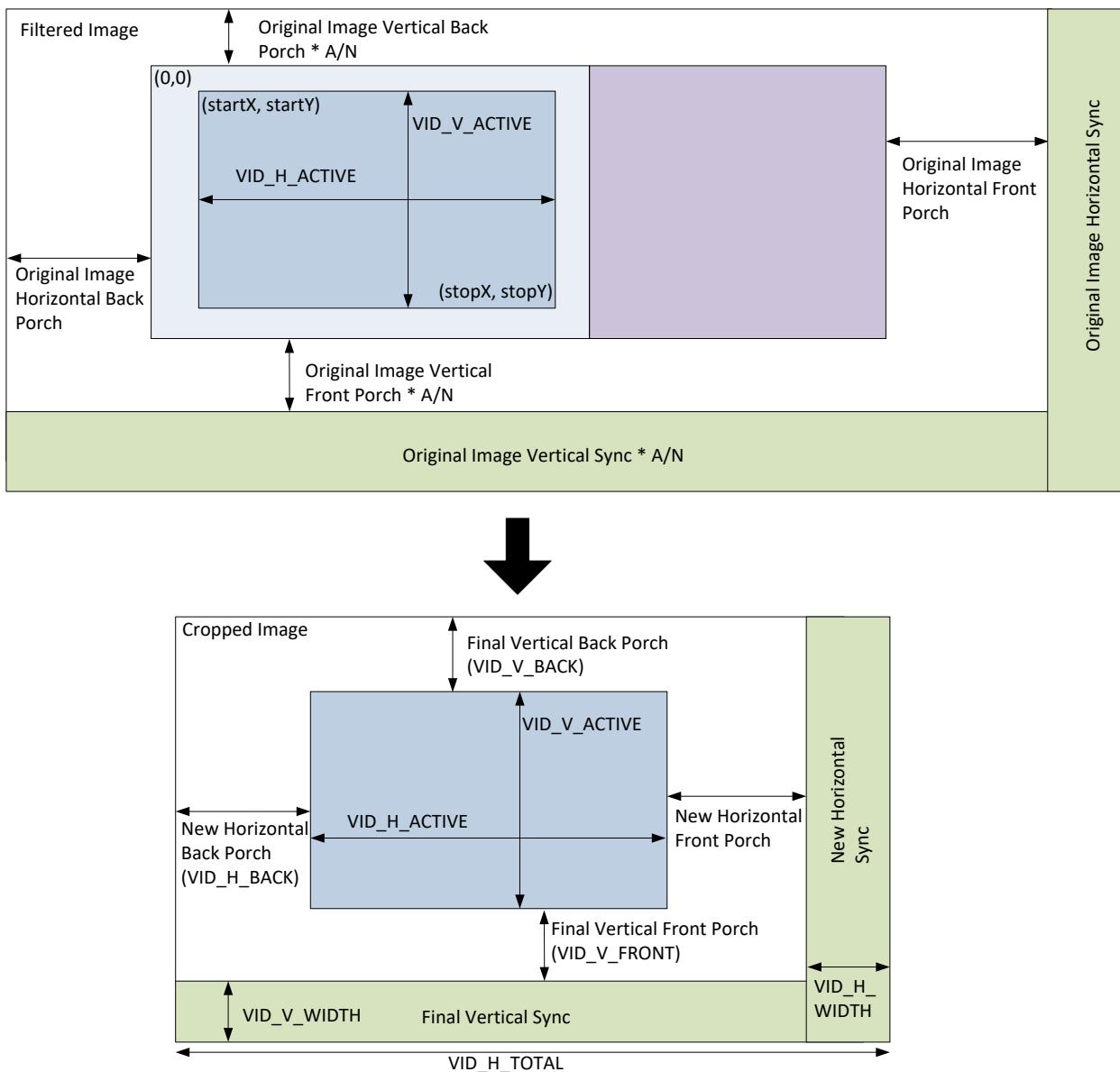
#### 7.3.4.2.2 Blanking Adjustments for Frequency Offset

Since the DS90UH981-Q1 generates timing from a local reference clock, there is the potential for a frequency offset between the actual video stream rate and the regenerated timing. The timing generator uses horizontal sync timing from the input to control regeneration and also uses this to check that the timing is correct. If the incoming horizontal timing is early relative to the generated timing, the generator drops pixels prior to generating the horizontal sync timing pulse.

If the incoming horizontal timing is late relative to the generated timing, the generator adds pixels prior to generating the horizontal sync timing pulse. Since the timing generator operates in four-pixel increments, four pixels are added or removed from the horizontal front porch to correct the offset as needed. This adds some jitter to the horizontal blanking.

Timing corrections are only made during active periods of video. During vertical blanking, an offset in timing can accumulate to the extent that larger compensation is required at the first active line. If there is accumulated error and the regenerated clock is fast (early), extra pixels are inserted to delay the start of the first active line. This delay is the total accumulated difference. A register control (RESYNC\_1ST\_LINE (0x01[7], 0x41[7], 0x81[7], and 0xC1[7]) on Page\_12) allows inserting a single four-pixel delay per video line until the difference is corrected.

If there is accumulated error and the regenerated clock is slow (late), blanking pixels are removed to delay the start of the first active line. Four pixels are removed prior to the first active line, and for each subsequent active line until the accumulated difference is corrected. During active video, the timing generator continues to monitor horizontal sync timing and make corrections of four pixels per line as needed to maintain accurate timing. Since the maximum correction is four pixels per line, the programmed frequency must be accurate within four pixels per line for the timing generator to maintain proper timing.



**Figure 7-10. Video Cropping and Video Parameters**

#### 7.3.4.3 SuperFrame (Multi-Image Frame) Capabilities

The DS90UH981-Q1 supports multi-image frames on each DSI video stream. The support for multi-image frames allows the pixels targeted at different displays to be combined into one frame. Up to four images are supported per frame. These multi-image frames are processed by four video processors, in which each video processor selects a single image (portion of the frame) to be forwarded and generates the timing for the selected image. As there are only four video processors, the total number of images included on the DSI inputs must be 4 or less. For example, if two DSI ports, DSI Port 0, DSI Port 1 are used and Port 0 carries 2 video streams, then Port 1 can carry a maximum of 2 video streams. As each video processor is independent, forwarded images can be identical or overlapping if desired. The video processors process the multi-image frame splitting in these steps:

1. Input Configuration: Enable video processor, map video stream input to the video processor and set the pixel width.

2. Vertical Filter: Select which lines of the images are forwarded
3. Video Cropping: Crop vertically filtered image to select desired portion of the image to forward
4. Timing Generation: Generate pixel clock and timing for the final image

The video processors process the multi-image frame aggregation in these steps:

1. Input Configuration: Enable video processor, map video stream to the video processor output and set the pixel width.
2. Vertical Filter: Select which lines of the images are forwarded
3. Timing Generation: Generate pixel clock and timing for the final image
4. Merge output of video processor to support aggregation of dual DSI input into an alternating pixel format or left/right format

#### 7.3.4.4 Vertical Filter

The vertical line selects which lines of a given video stream are forwarded. This is done based on the ratio A/N where A is the number of lines forwarded for every N lines of the multi-image frame. The vertical filter ratio values for A and N can be any number from 1 to 63. For proper operation, the number of lines in the multi-image frame must be a multiple of N. The images can be padded to the proper dimensions with additional vertical lines as these can be filtered out in the video cropping step. No horizontal adjustments are performed as part of the vertical filtering. The values for A and N are set via the VFILTER\_A and VFILTER\_N registers for each video processor on Page\_12. The vertical filter applies to both active lines and vertical blanking.

**Example:** For an A/N image where A=2 and N=3, the multi-image frame has 1.5 times as many lines as the resultant image. The video processor forwards the first two lines and drops the third. The video processor then forwards Lines 4 and 5 and drop the sixth. The vertical filter continues until the last line is reached.

The Vertical Active Input, Vertical Blanking Input and Vertical Total Input must each be divisible by N. The following Equations must be met for the Input parameters;

- Integer number = (Vertical Active Input) / N
- Integer number = (Vertical Blanking Input) / N
- Integer number = (Vertical Total Input) / N

The Vertical Back Porch, Vertical Front Porch, and Vertical Sync are recommended to each be divisible by N as well. In some cases, the Vertical Blanking Total can be too small to support each vertical blanking parameter being divisible by N. In these cases, the Vertical Blanking parameters must be selected using the following equations:

- Vertical Blanking Total Input/N = k where k must be an integer
- Round(VFP\_Input \* A/N) + Round(VBP\_Input \* A/N) + Round(VS\_Input \* A/N) = Vertical Blanking Total Input \* A/N
- Vertical Blanking Total Output = (Vertical Blanking Total Input + Number of Lines Cropped) \* A/N
- Vertical Blanking Total Output = VFP\_output + VBP\_output + VS\_output where VFP\_output, VBP\_output, and VS\_output can be selected as any integer value meeting this equation (e.g. the output value is not required to equal Round(Vertical Blanking parameter\*A/N)).

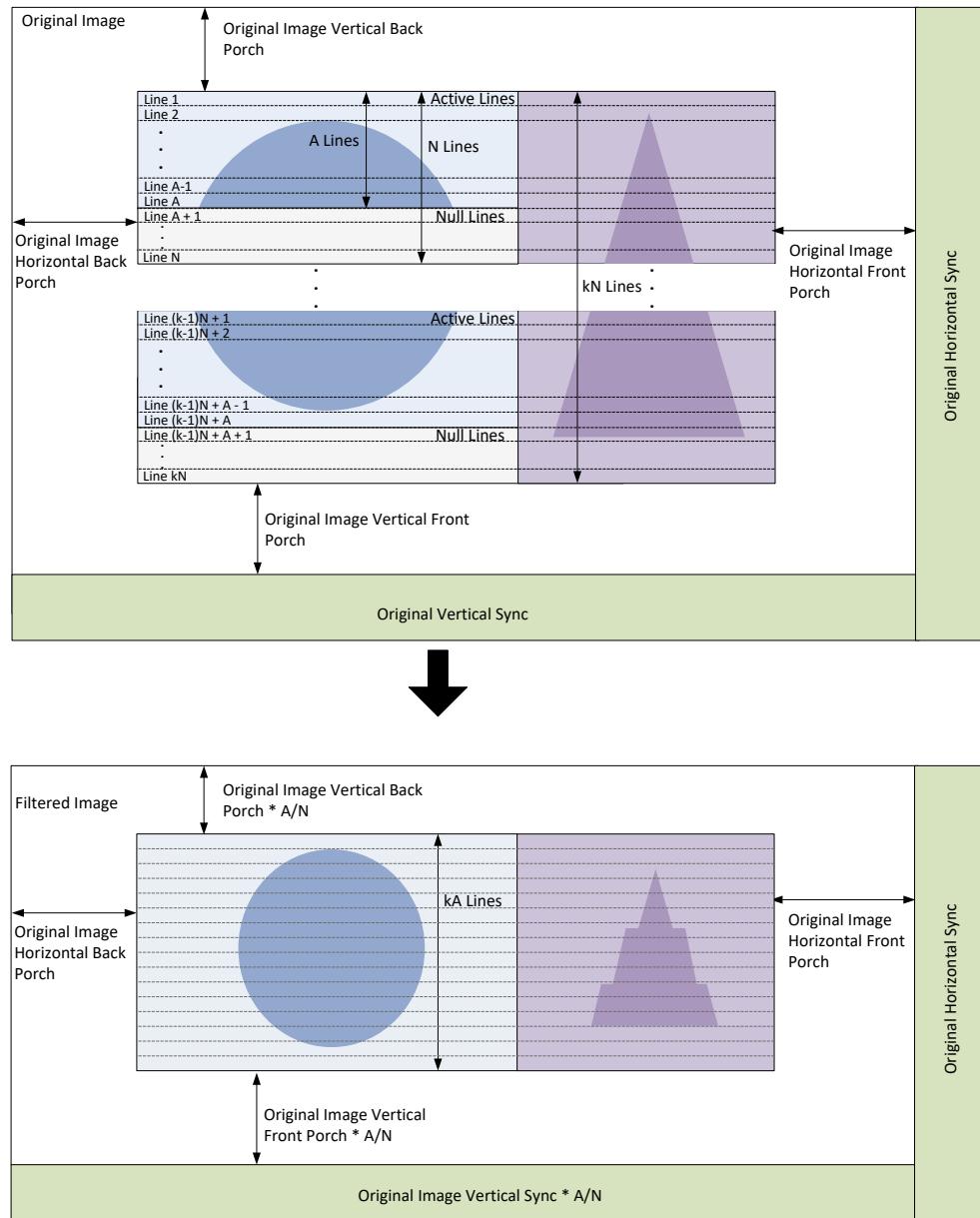
Example of correct blanking:

- A/N =5/6
- Vertical Blanking Total input = 6
- VFP\_Input = 1, VBP\_Input = 1, VS\_Input = 4
- Round(VFP\_Input \* A/N) + Round(VBP\_Input \* A/N) + Round(VS\_Input \* A/N) = Vertical Blanking Total Input \* A/N
- Round(1 \* 5/6) + Round(1 \* 5/6) + Round(4 \* 5/6) = 6 \* 5/6
- Round( 0.833 ) + Round( 0.833 ) + Round( 3.333 ) = 5
- 1 + 1 + 3 = 5
- VFP\_output = 1, VBP\_output = 1, VS\_output =3

Example of incorrect blanking:

- A/N =5/6

- Vertical Blanking Total input = 6
- VFP\_Input = 1, VBP\_Input = 2, VS\_Input = 3
- Round(VFP\_Input \* A/N) + Round(VBP\_Input \* A/N) + Round(VS\_Input \* A/N) = Vertical Blanking Total Input \* A/N
- Round(1 \* 5/6) + Round(2 \* 5/6) + Round(3 \* 5/6) = 6 \* 5/6
- Round( 0.833 ) + Round( 1.666 ) + Round( 2.5 ) = 5
- $1 + 2 + 3 \neq 5$



**Figure 7-11. Video Filtering**

To prevent overflow conditions the following requirements must be satisfied.

- Filtering Ratio =  $A - ((A-1)*A/N)$
- Filtering Ratio < 7
- VP Buffer Size > (Filtering Ratio \* Horizontal Active)

### 7.3.4.5 Video Cropping

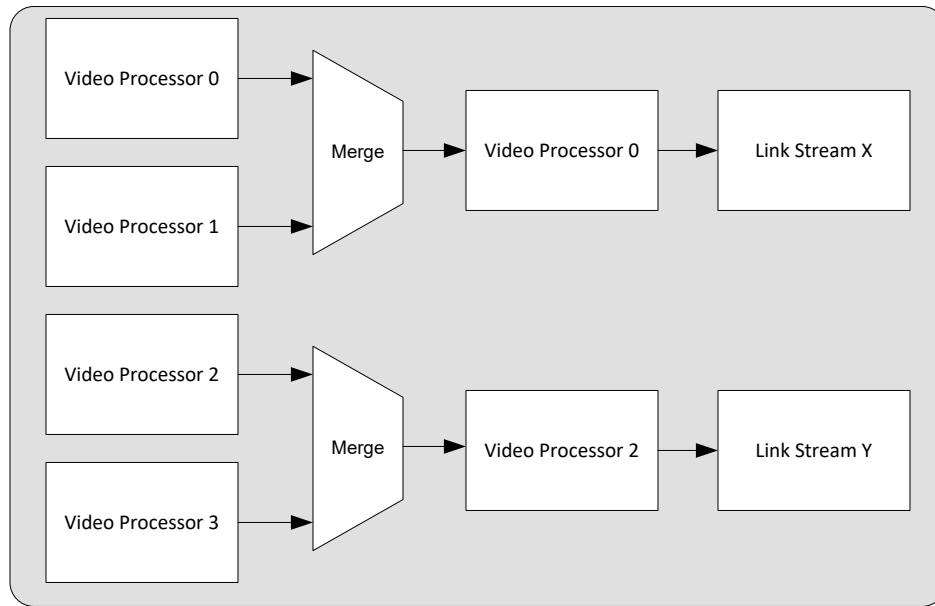
The video cropping step takes the vertically filtered image and crops image vertically and horizontally. The start and stop positions are measured in pixels based on the filtered image, not the original video frame. Valid positions are 0 to Line Length -1 for horizontal positions and from 0 to Number of Active Lines -1 for vertical positions. Pixels before the start position and after the stop position are not forwarded and replaced with blanking. Any vertical cropping results in additional vertical blanking in the final image. Cropping registers are set for each video processor on Page\_12. The horizontal start position is set via CROP\_START\_X0\_VP0 and CROP\_START\_X1\_VPx and the horizontal stop position is set via CROP\_STOP\_X0\_VPx and CROP\_STOP\_X1\_VPx. The vertical start position is set via CROP\_START\_Y0\_VPx and CROP\_START\_Y1\_VPx and the vertical stop position is set via CROP\_STOP\_Y0\_VPx and CROP\_STOP\_Y1\_VPx. When cropping the second image, the origin of the new image starts at (0,0), not at the CROP\_STOP values assigned to the first image.

**Table 7-13. Video Cropping Parameters**

Enable Cropping	Set X Start Position	Set Y Start Position	Set X Stop Position	Set Y Stop Position
VP_EN_CROP = 1	CROP_START_X[7:0]: 8 LSB of horizontal start position in pixels CROP_START_X[15:8]: 8 MSB of horizontal start position in pixels	CROP_START_Y[7:0]: 8 LSB of vertical start position using the line number CROP_START_Y15:8]: 8 MSB of vertical start position using the line number	CROP_STOP_X[7:0]: 8 LSB of horizontal stop position in pixels CROP_STOP_X[15:8]: 8 MSB of horizontal stop position in pixels	CROP_START_Y[7:0]: 8 LSB of vertical stop position using the line number CROP_START_Y15:8]: 8 MSB of vertical stop position using the line number

### 7.3.4.6 Video Processor Merge

Two video processors' output can be merged together to make a large image. The two videos that are being merged are required to be the same resolution and blanking. VP0 and VP1 can be combined, VP2 and VP3 can be combined. The video processors can merge images in 2 formats: "Odd/Even Merge" and "Left Right Merge." If VP0 and VP1 are merged, then select VP0 in the LINKx\_STREAM\_MAPx to output the merged image. If VP2 and VP3 are merged, then select VP2 in the LINKx\_STREAM\_MAPx to output the merged image. To properly merge the input videos the two input video streams must have a skew of less than 8 pixels.



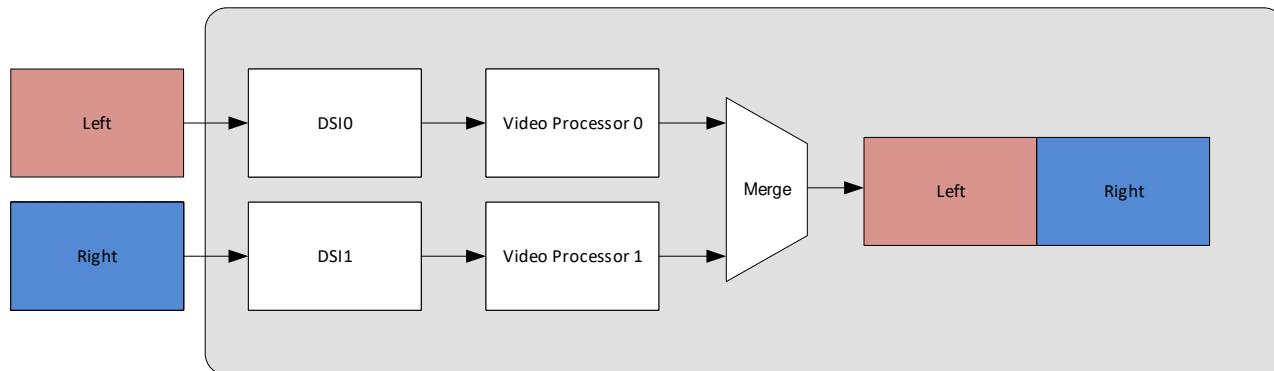
**Figure 7-12. Video Processor Merge Block**

### 7.3.4.6.1 Left Right Merge

Left right merge merges two input images using one of the input images as the left side of the final image and the other image as the right side of the final image. To set the video processors to use left right merge set the register VP\_DUAL\_MERGE\_LR\_EN to 1 in both of the video processors that are being merged. For the VP0 and VP1 merge, the left image is always in VP0, the right image is always in VP1. For the VP2 and VP3 merge, the left image is always in VP2, and the right image is always in VP3. The Left and Right input video timings must be the same for all video timing parameters. Use the following table to select the proper video timing for the input video and timing for the video processor.

**Table 7-14. Left Right Merge Timing Parameters**

	Input Video Source 0 and 1	VP0 or VP2 Timing	VP1 or VP3 Timing	Output Timing
<b>Total Horizontal</b>	(Target H Total)/2	Target H Total	Target H Total	Target H Total
<b>Vertical Total</b>	Target V Total	Target V Total	Target V Total	Target V Total
<b>Horizontal Active</b>	(Target H Active)/2	Target H Active	Target H Active	Target H Active
<b>Vertical Active</b>	Target V Active	Target V Active	Target V Active	Target V Active
<b>Horizontal Blanking</b>	(Target H Blanking)/2	Target H Blanking	Target H Blanking	Target H Blanking
<b>Vertical Blanking</b>	Target V Blanking	Target V Blanking	Target V Blanking	Target V Blanking
<b>PCLK</b>	(Target PCLK)/2	Target PCLK	Target PCLK	Target PCLK



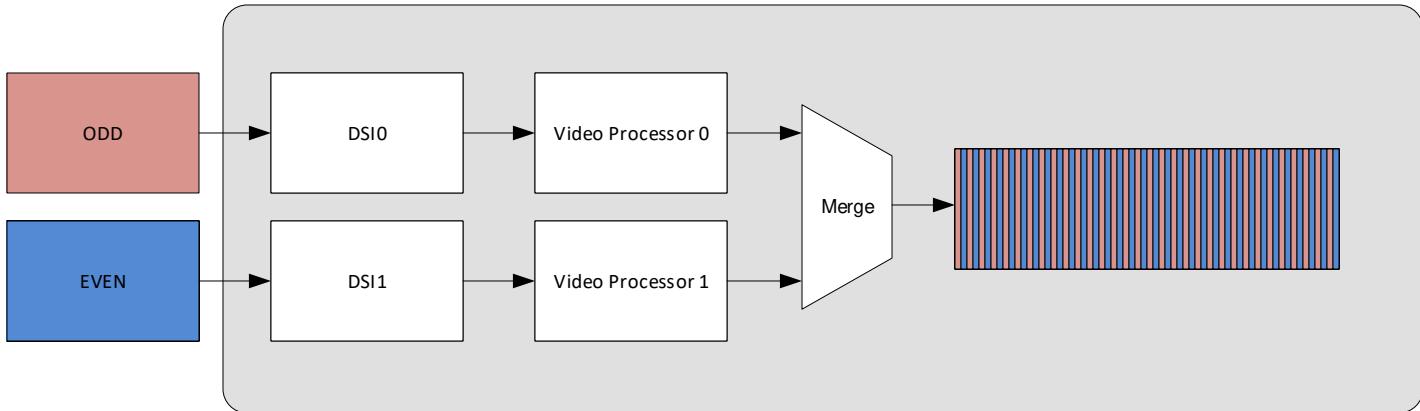
**Figure 7-13. Left Right Merge**

### 7.3.4.6.2 Alternating Pixel Merge

Alternating pixel merge merges two input images using one of the input images as the odd (first) horizontal pixels of the output and one image as the even (second) horizontal pixels of the output image. To set the video processors to use alternating pixel merge set the register VP\_DUAL\_MERGE\_ALT\_EN to 1 in both of the Video Processors that are being merged. For the VP0 and VP1 merge, the odd image is input to VP0; the even image is input to VP1. For the VP2 and VP3 merge, the odd image is input to VP2; the even image is input to VP3. The odd and even input video timings must be the same for all video timing parameters. Use the following table to select the proper video timing for the input video and timing for the video processor.

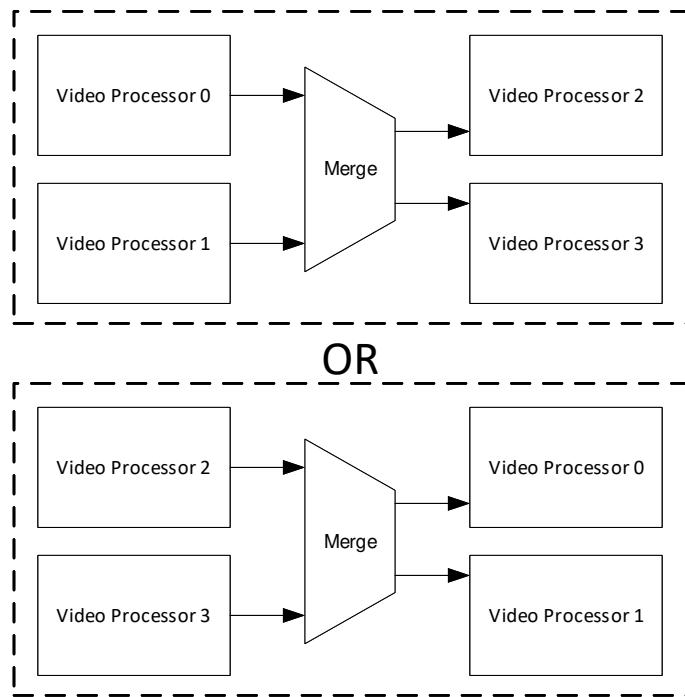
**Table 7-15. Alternating Pixel Merge Timing Parameters**

	Input Video Source 0 and 1	VP0 or VP2 Timing	VP1 or VP3 Timing	Output Timing
<b>Total Horizontal</b>	(Target H Total)/2	(Target H Total)/2	(Target H Total)/2	Target H Total
<b>Vertical Total</b>	Target V Total	Target V Total	Target V Total	Target V Total
<b>Horizontal Active</b>	(Target H Active)/2	(Target H Active)/2	(Target H Active)/2	Target H Active
<b>Vertical Active</b>	Target V Active	Target V Active	Target V Active	Target V Active
<b>Horizontal Blanking</b>	(Target H Blanking)/2	(Target H Blanking)/2	(Target H Blanking)/2	Target H Blanking
<b>Vertical Blanking</b>	Target V Blanking	Target V Blanking	Target V Blanking	Target V Blanking
<b>PCLK</b>	(Target PCLK)/2	Target PCLK	Target PCLK	Target PCLK

**Figure 7-14. Alternating Pixel Merge**

#### 7.3.4.6.3 Merged Image Processing

In addition to being mapped directly to an FPD-Link stream the merged stream can also be mapped to the input of the other two video processors. The merged stream can be set as the input to the other two video processors by setting the VP2VP\_EN register. This allows merged images to be cropped or filtered before being sent out on the FPD-Link.

**Figure 7-15. Merged Image Forwarding**

#### 7.3.5 FPD-Link Port Register Access

Since the DS90UH981-Q1 contains two downstream ports, some registers are duplicated to allow control and monitoring of the two ports. To facilitate this, the PORT\_SEL (0x2D) register controls access to the two sets of registers. Registers that are shared between ports (not duplicated) are available independent of the settings in the TX\_PORT\_SEL register.

Setting the TX\_READ\_PORT bit allows reading registers of the selected port. Writes occur to any port for which the TX\_WRITE\_PORT\_x select bit is set, allowing simultaneous writes to both ports if both write bits are set.

### 7.3.6 FPD-Link Port Polarity Swap

The DS90UH981-Q1 supports inverting the polarity of the positive and negative pins of the FPD-Link ports. The following script can be used to swap the polarity of the pins in FPD-Link IV mode:

```
## ****
## Invert P and N signal for PORT0 and PORT1 in FPD4
## ****
board.WriteI2C(devAddr,0x40,0x04); #Page 1
###Lane 0 TX###
#Invert FPD TX output
board.WriteI2C(devAddr,0x41,0x00)
board.writeI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x01)
board.WriteI2C(devAddr,0x42,0xFF)
board.writeI2C(devAddr,0x41,0x02)
board.WriteI2C(devAddr,0x42,0x03)
#Invert BCRX polarity
board.WriteI2C(devAddr,0x41,0x08)
reg_value0 = board.ReadI2C(devAddr,0x42)
board.writeI2C(devAddr,0x42,reg_value0 | 0x80)

###Lane 1 TX###
#Invert FPD TX output
board.WriteI2C(devAddr,0x41,0x20)
board.writeI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x21)
board.writeI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x22)
board.writeI2C(devAddr,0x42,0x03)
#Invert BCRX polarity
board.WriteI2C(devAddr,0x41,0x28)
reg_value1 = board.ReadI2C(devAddr,0x42)
board.writeI2C(devAddr,0x42,reg_value1 | 0x80)
```

The following script can be used to swap the polarity of the pins in FPD-Link III mode:

```
## ****
## Invert P and N signal for PORT0 and PORT1 in FPD3## ****
board.WriteI2C(devAddr,0x40,0x04); #Page 1
###Lane 0 TX###
#Invert FPD TX output
board.WriteI2C(devAddr,0x41,0x00)
board.writeI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x01)
board.WriteI2C(devAddr,0x42,0xFF)
board.writeI2C(devAddr,0x41,0x02)
board.WriteI2C(devAddr,0x42,0x03)
#Invert BCRX polarity
board.WriteI2C(devAddr,0x41,0x08)
reg_value0 = board.ReadI2C(devAddr,0x42)
board.writeI2C(devAddr,0x42,reg_value0 | 0x80)

###Lane 1 TX###
#Invert FPD TX output
board.WriteI2C(devAddr,0x41,0x20)
board.writeI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x21)
board.writeI2C(devAddr,0x42,0xFF)
board.WriteI2C(devAddr,0x41,0x22)
board.writeI2C(devAddr,0x42,0x03)
#Invert BCRX polarity
board.WriteI2C(devAddr,0x41,0x28)
reg_value1 = board.ReadI2C(devAddr,0x42)
board.writeI2C(devAddr,0x42,reg_value1 | 0x80)
```

### 7.3.7 Power Down (PDB)

The serializer has a PDB input pin to enable or power down the device. This pin can be controlled by an external device or through VDD18, where VDD18 = 1.71 V to 1.89 V. Make sure that this pin is not driven HIGH before all power supplies have reached final levels. When PDB is driven low, make sure that the pin is driven to 0 V for

at least 2 ms before releasing or driving high. In the case where PDB is pulled up to VDD18 directly, a 10-kΩ pull-up resistor and a >10 μF capacitor to ground are required (See [Section 9.1](#)).

Toggling PDB low powers down the device and resets all control registers to default. During this time, PDB must be held low for a minimum of 2 ms before going high again.

### 7.3.8 Internal ADC

The serializer device contains an 8-bit ADC that is used for various functions including line fault detection, temperature sensing, internal voltage sensing and external voltage monitoring. This ADC is configured using indirect register Page\_14 in the serializer devices. To enable the ADC set the ADC\_MODE (0x0D[7] = 0) on Page\_14). Refer to *Diagnostic Features of FPD-Link IV Devices* for more details implementation.

#### 7.3.8.1 ADC Timing Control

The ADC can read the voltage of up to 11 different sources. These sources can be enabled or disabled in register 0x07 or 0x08 on Page\_14. By default the ADC reads 5 voltage sources: the thermal sense element, and 4 internal supply voltages. The ADC samples a voltage source for a time period controlled by concatenating 4 bytes of 0x0F, 0x10, 0x11, and 0x11 register to represent the "ADC\_SRC\_CNT\_x[31:0]". To calculate the frequency at which the ADC updates each voltage source in their register, use the following formula:

$$VOL\_SRC\_FREQ = \frac{25MHz}{[ADC\_CLK\_VAL \times SRC\_CNT\_VAL \times (\#_VOL\_SRC\_EN)]} \quad (21)$$

For example, if "ADC\_CTRL\_CLK\_DIV (0x04[5:4])" is set to 2 and "SRC\_CNT\_VAL (0x0F,0x10,0x11,0x12)" is set to 13000 and there are 5 voltage sources enabled, then the ADC updates each voltage source at a frequency of 192.3 Hz.

$$192.3Hz = \frac{25MHz}{[2 \times 13000 \times (5)]} \quad (22)$$

#### 7.3.8.2 Temperature Sensing

The DS90UH981-Q1 uses the ADC and a thermal sense element to measure the junction temperature of the DS90UH981-Q1. The junction temperature is periodically read and stored in the TEMP\_FINAL (0x13) register on the ADC control register Page\_14. The formula to convert the TEMP\_FINAL to Celsius is below. The TEMP\_FINAL has a resolution of 2°C.

$$Temperature = (2 \times TEMP\_FINAL) - 273 \quad (23)$$

The DS90UH981-Q1 can also trigger an interrupt when the junction temperature exceeds the value of the TEMP\_HIGH (0x33) register or falls below the TEMP\_LOW (0x34) register on Page\_14. To enable this interrupts status to be displayed on the INTB pin, set bit 3 of the INTERRUPT\_CTL (0x51) register on the main page to 1. By default, this interrupt is triggered when internal junction temperatures exceed 140 °C or below -20 degrees C. These thresholds can be changed by writing to the TEMP\_HIGH or TEMP\_LOW register. The formula to convert between the temperature and the register value is the same as above [Equation 23](#). For more detailed registers setting refer to *Diagnostic Features of FPD-Link IV Devices*.

### 7.3.8.3 Internal Supply Monitoring

The serializer device uses the ADC to monitor the voltage levels of the 1.8V and 1.15V voltage supplies of the device. The ADC can read the voltages of four different pins of the device. Voltage Sensing below shows the register and pin locations for the four ADC voltage readings. The voltage sensors have a resolution of 2.5% for 1.15V and 1.8V.

For details information on registers setting refer to Page\_14 Registers

**Table 7-16. Voltage Sensing**

Voltage Pin being read	Nominal Voltage	Register name (Address)	Register address (on page_14)	CF (correction factor)
VDD18 pin	1.8V	IV0_FINAL	0x15	3.045
VDDIO pin	1.8V	IV1_FINAL	0x16	3.082
VDD11_P0 pin	1.15V	IV2_FINAL	0x17	1.844
VDD11_L pin	1.15V	IV3_FINAL	0x18	1.886

- Voltage equation for voltage sense

$$\text{Pin_Voltage} = \text{CF} * (1 / 255) * 1.207 * \text{IVx_FINAL} \quad (24)$$

The serializer device can also trigger an interrupt when the voltage supply goes above or below specific voltages. To display this interrupt's status on the INTB pin, set the INTERRUPT\_CTL[3] (0x51) register on the main page to 1. The voltage threshold values in [Table 7-17](#) below, are the recommended voltage values and they are +/- 5% of the Nominal Voltage. The upper or lower voltage thresholds can be changed by changing the values of the IVX\_HIGH and IVX\_LOW registers in the table below:

**Table 7-17. Upper Thresholds for Supply Voltages**

Supply Pin	Upper Threshold Voltage Register Name	Upper Threshold Voltage Register Offset Address (Page_14)	Upper Threshold Voltage +5% Nominal Voltage (V)
VDD18 pin	IV0_HIGH	0x39	1.8881
VDDIO	IV1_HIGH	0x3C	1.8822
VDD11_P0	IV2_HIGH	0x3F	1.2045
VDD11_L	IV3_HIGH	0x42	1.2048

**Table 7-18. Lower Thresholds for Supply Voltages**

Supply Pin	Lower Threshold Voltage Register Name	Lower Voltage Threshold Register Offset Address (Page_14)	Lower Threshold Voltage -5% Nominal Voltage (V)
VDD18 pin	IV0_LOW	0x3A	1.7007
VDDIO	IV1_LOW	0x3D	1.7071
VDD11_P0	IV2_LOW	0x40	1.0910
VDD11_L	IV3_LOW	0x43	1.0888

### 7.3.8.4 External Voltage Sensing

The ADC on the device can read and monitor the voltages of the GPIO6 and GPIO8 pins. The pins can read voltages from 0.4V to 1.207V. If a higher voltage is to be read, an external voltage divider is required. In order to read the voltage at the GPIO you must enable EXT\_VOL0 (0x08[0]) for GPIO6 and EXT\_VOL1 (0x08[1]) for GPIO8 on Page\_14. Disable the 25KΩ pull down on GPIO6 set REG\_GPIO\_EN\_PULL\_LOW\_1 (0xC9[6]) on Page\_9 to 0. Disable the 25KΩ pull down on GPIO8 set REG\_GPIO\_EN\_PULL\_LOW\_8 (0xCA[0]) on Page\_9 to 0. The ADC voltage can be read in EXT\_VOL0\_FINAL (0x1B) for GPIO6 and EXT\_VOL1\_FINAL (0x1C) for GPIO8. The formula to convert the ADC reading to the voltage is in the Equation below. Refer to registers information in Page\_14 Registers.

$$GPIOx\_Voltage = \left( \frac{1.207}{255} \right) \times EXT\_VOLx\_FINAL \quad (25)$$

The device can also trigger an interrupt when the voltages on GPIO6 and GPIO8 go above or below specific voltages. To display this interrupt's status on the INTB pin set the INTERRUPT\_CTL[3] in (0x51) register on the main page to 1. The registers to set the upper and lower voltages is in the Table Below. To calculate the values for the upper and lower threshold use the above formula to convert from voltage to register value.

**Table 7-19. Upper or Lower External Voltage Threshold**

Description	Register Name	Register Address (Page_14)
GPIO6 Upper Threshold	EXT_VOL0_HIGH	0x4C
GPIO6 Lower Threshold	EXT_VOL0_LOW	0x4D
GPIO8 Upper Threshold	EXT_VOL1_HIGH	0x4F
GPIO8 Lower Threshold	EXT_VOL1_LOW	0x50

### 7.3.9 Serial Link Fault Detect

As part of the diagnostics features for the DS90UH981-Q1, the line fault detection circuitry can be used to detect faults with the connection between the serializer and deserializer. This is done by monitoring and sensing the voltage on the cable between the SerDes and transmitting that voltage to a GPIO on either the serializer or deserializer. Refer to the [Line-Fault Detection Hardware Implementation](#) section and apps note *Diagnostic Features of FPD-Link IV Devices*, SNLA322 for more details of hardware implementation.

### 7.3.10 Interrupt Pin (INTB)

The INTB pin is an active low interrupt output pin that acts as an interrupt for various local and remote interrupt conditions. The global interrupt must be enabled, as well as the individual interrupts of interest, via the INTERRUPT\_CTL (0x51) register. The available interrupts are shown in [Table 7-20](#). Video processor interrupts are enabled via the INTR\_CTL\_VP\_VPx indirect access registers (Page\_12 0x33, 0x73, 0xB3, and 0xF3). FPD Transmitter Port interrupts are enabled via INTR\_CTL\_FPD4\_PORTx indirect access registers (Page\_9 0x8C, 0x9C), and Page\_0 of FPD3\_ICR (0xC6) and FPD3\_ISR (0xC7). Interrupt statuses are available regardless of whether an interrupt is included in the overall interrupt, including when the corresponding bit in INTERRUPT\_CTL is set to 0.

The general procedure for the FPD Transmitter interrupts to be monitored on the INTB pin configuration is as follows in FPD-Link III mode. If there is no active video on the SER input side, register 0x34[6] = 1 must be set on the FPD-Link III deserializer in order to establish LOCK.

1. FPD-Link IV SER - Enable REM\_INT as part of the FPD-Link III Transmitter interrupt by setting in Main Page Reg 0xC6[5] = 1, 0xC6[0] = 1
2. FPD-Link IV SER - Enable Global INTB and FPD\_TX Interrupts Main Page Reg 0x51[7] = 1, 0x51[1:0] = 0b11
3. Force FPD-Link III deserializer INTB\_IN = L
4. Observe FPD-Link IV SER INTB = L
5. Force FPD-Link III deserializer INTB\_IN = H
6. Observe FPD-Link IV SER INTB = L (INTB pin still low)
7. Read FPD-Link IV SER Main Page Register 0xC7 to clear interrupt
8. Observe FPD-Link IV SER INTB = H

**Table 7-20. Interrupt Statuses**

Status	Address	Description
Global Interrupt (GLOBAL_INT)	0x52[7]	Set when any of the enabled interrupts is set.
DPHY Port 1 Receiver Interrupt (IS_D-PHY_RX)	0x52[5]	Set when any of the enabled D-PHY Port 1 interrupts is set.

**Table 7-20. Interrupt Statuses (continued)**

Status	Address	Description
DPHY Port 0 Receiver Interrupt (IS_D-PHY_RX)	0x52[4]	Set when any of the enabled D-PHY Port 0 interrupts is set.
Device Interrupts (DEVICE_INT)	0x52[3]	Set when any of the Temperature, Voltage Monitor, Line Fault and ESD Interrupts is set.
Back channel GPIO Interrupt (BC_GPIO_INT)	0x52[2]	Set when any of the back channel GPIO interrupt is set on the deserializer.
FPD Transmitter port 1 Interrupt (IS_FPD_TX1)	0x52[1]	Set when any enabled FPD-Link Transmitter Port 1 interrupt is set.
FPD Transmitter port 0 Interrupt (IS_FPD_TX0)	0x52[0]	Set when any enabled FPD-Link Transmitter Port 0 interrupt is set.

### 7.3.11 Remote Interrupt Pin (GPIO4 / REM\_INTB)

GPIO4 / REM\_INTB is configured as a GPIO pin by default. The remote interrupt function must be enabled manually after startup if required. At device startup this pin must be left floating or pulled to GND. The REM\_INTB outputs the interrupt from the INTB\_IN deserializer. In Independent mode, REM\_INTB can be configured to mirror the INTB\_IN signal from either the partnering deserializer connected to Port 0 or Port 1 of the serializer.

The general procedure for configuring the (GPIO4 / REM\_INTB) interrupt in FPD-Link III or FPD-Link IV mode is shown in these steps.

1. FPD-Link IV SER - Enable REM\_INT as part of the FPD-Link Transmitter interrupt by setting in Main Page Reg 0xC6[5] = 1, 0xC6[0] = 1
2. FPD-Link IV SER - Configure GPIO4 Output<sup>1</sup> and forward REM\_INT by writing 0x1B = 0x88 for Port 0 or writing 0x1B = 0x98 for Port 1
3. FPD-Link IV SER - Enable Global INTB and FPD\_TX Interrupts Main Page Reg 0x51[7] = 1, 0x51[1:0] = 0b11
4. Force DES INTB\_IN = L
5. Observe FPD-Link IV SER REM\_INTB = L
6. Force DES INTB\_IN = H
7. Observe FPD-Link IV SER REM\_INTB = H

### 7.3.12 Video Processor Interrupt

Video processor interrupts are enabled via the INTR\_CTL\_VP\_VPx indirect access registers (Page\_12 0x33, 0x73, 0xB3, and 0xF3). Video processor interrupt statuses can be read in the INTR\_STS\_VP\_VPx indirect access registers (Page\_12 0x31, 0x71, 0xB1, and 0xF1). Video processor interrupt statuses can be polled periodically to detect video processor interrupts or a GPIO can be set to output the VP interrupt status to be monitored by a MCU to detect a VP interrupt.

**Table 7-21. Video Processor Interrupt Statuses**

Status	Address	Description
Video Crop Vertical Error (IS_CROP_VERT_ERR )	INTR_STS_VP_VPx[6]	Indicates that the video frame does not have enough lines for programmed vertical cropping.
Video Crop Horizontal Error (IS_CROP_HOR_ERR )	INTR_STS_VP_VPx[5]	Indicates that the video frame does not have enough pixels in a line for the programmed horizontal cropping.
Timing Generation Data Available Error (IS_TIMING_DATA_ERR)	INTR_STS_VP_VPx[4]	Indicates that the timing generator has detected a line length error or other error that results in no data being available to send from the video buffer during the active horizontal period.
Timing Generation Line Number Error (IS_TIMING_LINE_ERR)	INTR_STS_VP_VPx[3]	This error is reported if the timing generator detects a mismatch between the expected line number and the incoming line number. This can occur during video buffer errors or if the timing generator is not synchronized with the incoming video stream. When this error is reported, video lines are removed from the video buffers.

<sup>1</sup> For expanded functionality, REM\_INTB may be mapped to any GPIOx.

**Table 7-21. Video Processor Interrupt Statuses (continued)**

Status	Address	Description
Timing Generation Active Start Error (IS_TIMING_STRT_ERR)	INTR_STS_VP_VPx[2]	This error is reported if video data is not available when the timing generator indicates the start of the active video period.
Video Buffer Error (IS_VP_VBUF_ERR)	INTR_STS_VP_VPx[1]	Indicates the video buffer has detected an overflow error.
Video Processor Status Changed (IS_VP_STATUS_CHANGE)	INTR_STS_VP_VPx[0]	Indicates the video processor status has changed (any of the other interrupts in INTR_STS_VP_VPx is set or cleared).

### 7.3.13 FPD Transmitter Interrupt

FPD Transmitter Port interrupts are enabled via INTR\_CTL\_FPD4\_PORTx indirect access registers (Page\_9 0x8C and 0x9C) and FPD3\_ICR (Page\_0 0xC6). The status can be read in registers 0x8D and 0x9D on Page\_9, and 0xC7 on Main Page\_0.

**Table 7-22. FPD Transmitter Interrupt Statuses**

Status	Field Enable	Description
Receiver Lock Detected	INTR_STS_FPD4_PORTx[6], FPD3_ICR[6]	Set when the deserializer has indicated it is locked to the incoming data
Remote Interrupt	INTR_STS_FPD4_PORTx[5], FPD3_ICR[5]	Indicates the deserializer INTB_IN is LOW (interrupt detected)
Deserializer Interrupt	INTR_STS_FPD4_PORTx[4]	Indicates that the deserializer global interrupt is detected.

### 7.3.14 ESD Event Interrupt

The device can be configured to trigger an interrupt when the number of ESD events exceeds a given threshold. To enable this interrupt set the DEVICE\_INT\_EN (0x51[3]) register to 1 and ESD\_EVENT\_INT\_EN (0x61[6]) register to 1. The number of ESD events the device has detected is stored in the ESD\_EVENT\_COUNTER (0xBC[5:0]) register. The ESD event threshold count in the ESD\_EVENT\_COUNTER\_THRESHOLD (0x61[5:0]) register. To clear the interrupt, first clear the ESD\_EVENT\_COUNTER (0xBC[5:0]) register by writing a "0" and then a "1" to the ESD\_EVENT\_COUNTER\_ENABLE (0xBC[6]) register, then write a "1" to the ESD\_EVENT\_INT\_STS\_CLR (0x61[7]) register.

### 7.3.15 FPD-Link IV Built-In Self Test (BIST)

An optional at-speed Built-In Self Test (BIST) feature supports testing of the high speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

#### 7.3.15.1 BIST Configuration and Status

The BIST mode can be enabled at the deserializer via the BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors for errors. The deserializer stores errors over the forward channel in the registers. The serializer also tracks errors indicated by the CRC fields in each back channel frame. Enabling BIST mode does not cause loss of lock.

See [Figure 7-16](#) for the BIST mode flow diagram.

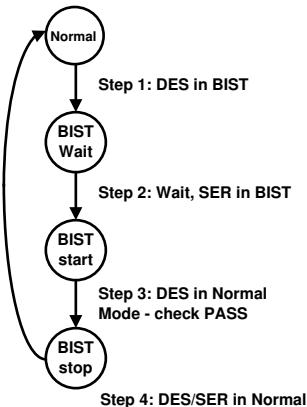
**Step 1:** The Serializer is paired with an FPD-Link IV Deserializer, BIST Mode is enabled via the register on the Deserializer. Right after BIST is enabled, part of the BIST sequence requires bit 0x02[5] be toggled locally on the Serializer (set 0x02[5]=1, then set 0x02[5]=0).

**Step 2:** An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link interface to the deserializer. Once the serializer and the deserializer are in BIST mode, the deserializer starts checking the data

stream. If an error is detected, it is indicated in the error registers of the deserializer. On the serializer, errors on the back channel are monitored and stored in the BIST\_BC\_ERROR register (0x0F).

**Step 3:** BIST is stopped via the deserializer register and the deserializer stops checking the data. The final test result is held in BIST\_BC\_ERROR and the BIST error register on the deserializer. The BIST duration is user controlled by the duration between enabling BIST mode and disabling BIST mode.

\*\*BIST can only be disabled from the deserializer. During BIST remote access to the deserializer from the serializer is disabled.



**Figure 7-16. BIST Mode Flow Diagram**

The BIST mode can also be enabled from the Serializer side with the configuration script provided below.

**Step 1:** The Serializer is paired with an FPD-Link IV Deserializer, BIST Mode is enabled via main page register 0x12[7]=1 (override DES capabilities) and 0x12[5]=1 (BIST enable) on the Serializer. Part of the BIST sequence requires allowing remote BIST to be enabled from the Deserializer via main page register 0x2D[3]=1 .

**Step 2:** Error injection scenarios are also checked in this script. FC errors are injected using the Serializer page\_9 register 0x8B. This Errors Injection section of the script could be used to validate the functionality of BIST mode. However, user can comment it out during system testing.

**Step 3:** BIST is stopped via Serializer main page register 0x12[7]=1 (override DES capabilities) and 0x12[5]=0 (BIST disable) and Deserializer main page register 0x2D[3]=0 (remote BIST mode). The BIST duration is user controlled by the duration between enabling BIST mode and disabling BIST mode.

```

## ****
## Enable BIST mode from the Serializer side
## ****
import time
serAddr = 0x18
desAddr0 = 0x58
desAlias0 = 0x58
board.writeI2C(serAddr,0x70,desAddr0)
board.writeI2C(serAddr,0x78,desAlias0)
board.writeI2C(serAddr,0x88,0x0)
InjectErrors = 3 # Max 127
Dwell = 1 # Seconds
## ****
## Enable I2C Passthrough
## ****
I2C_PASS_THROUGH = board.ReadI2C(serAddr,0x7,1)
I2C_PASS_THROUGH_MASK = 0x08
I2C_PASS_THROUGH_REG = I2C_PASS_THROUGH | I2C_PASS_THROUGH_MASK
board.writeI2C(serAddr,0x07,I2C_PASS_THROUGH_REG) #Enable I2C Passthrough
## ****
## Enable BIST mode
## ****
board.writeI2C(desAlias0,0x2D,0x08) # Allow remote BIST enable
board.writeI2C(serAddr,0x12,0xA0) # Enable BIST from SER side
  
```

```

print "BIST Enabled"
print "Dwell", Dwell, "Seconds"
time.sleep(Dwell)
## ****
## Inject Errors
## ****
board.writeI2C(serAddr,0x40,0x24)
board.writeI2C(serAddr,0x41,0x8B)
board.writeI2C(serAddr,0x42,InjectErrors | 0x80)
print "Inject", InjectErrors, "FC Errors"
## ****
## Check Results
## ****
board.writeI2C(serAddr,0x12,0x80) # Disable_BIST from SER side
board.writeI2C(desAlias0,0x2D,0x00) # Disable remote BIST
print "BIST Disabled"
print "Detected FC Errors:", board.ReadI2C(desAlias0,0xB8,1)

```

### 7.3.15.2 Forward Channel and Back Channel Error Checking

While in BIST mode, the serializer stops sending video data and switches over to an internal all zeroes pattern. The internal all-zeroes pattern goes through scrambler, DC-balancing, etc. and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers.

The back channel data is checked for CRC errors once the serializer locks onto the back channel serial stream, as indicated by link detect status (register bit 0x0C[0]). Back channel errors are stored in the BIST\_BC\_ERROR register, which is cleared when the serializer enters BIST mode. The BIST mode CRC error register is active in BIST mode only and keeps a record of the last BIST run until cleared or the serializer enters BIST mode again.

### 7.3.16 Auxiliary Buffers and Secondary-Data Packets (SDP)

The Auxiliary Buffer (ABUFF) architecture includes a non-video data path over FPD-Link IV forward channel only. The Auxiliary Buffers are meant to store audio data. Each buffer can receive data packets from the auxiliary sources, which can then be mapped to one of the 6 streams on each of the two link layers . On the deserializer, more than one ABUFF can be mapped to a stream on the FPD-Link daisy-chain output.

If an ABUFF is mapped to a stream shared with one of the video buffers (VBUFF), the Link layer (LINK0/1) fetches the data from ABUFF after the video data has been sent. The data in the ABUFF is sent over the FPD-Link IV link only during the horizontal blanking period of the video stream. Alternatively, an ABUFF can be mapped to a stream that is not mapped to any of the VBUFF. In this case, the auxiliary data is transmitted over the FPD-Link IV along with the video stream but using separate, dedicated timeslots.

There are multiple sources for the ABUFF on the serializer side. The ABUFF destination for the serializers are the 6 streams inside each link layer. An ABUFF to Link Layer mapping muxes/demuxes nodes to/from Link 0 and Link 1 streams based on a per ABUFF register select bit (as part of serializer ABUFF register map). The deserializer has 6 stream destinations for daisy-chain transmitting and for the DS90Ux984-Q1 deserializer, two SDP DP/eDP ports. The deserializer's I2S controller copies the audio auxiliary data from stream 0 or stream 1 if SDP\_TYPE\_IN (serializer register 0x81 plus offset) is 0 (audio packets). Refer to Application Note SNLA407 *FPD-Link IV Audio* for more details on configuration.

ABUFF sources and destinations for the DS90Ux98x family devices are as follows:

**Table 7-23. DS90Ux98x ABUFF Sources and Destinations**

Device	ABUFF Sources	ABUFF Destinations
DS90Ux681	Audio, CSI	Link layer 0 or 1 streams
DS90Ux981	Audio, CSI	Link layer 0 or 1 streams
DS90Ux943A	Audio, DP	Link layer 0 or 1 streams
DS90Ux983	Audio, DP	Link layer 0 or 1 streams
DS90Ux984	FPD-Link IV RX	Daisy-chain link layer 0 or 1 streams, DP/eDP ports 0 and 1

**Table 7-23. DS90Ux98x ABUFF Sources and Destinations (continued)**

Device	ABUFF Sources	ABUFF Destinations
DS90Ux988	FPD-Link IV RX	Daisy-chain link layer 0 or 1 streams

The auxiliary data with respect to blanking time has the following constraint:

1. Highest number of bits to transmit in that time is 567 bits
2. Total horizontal blanking time is minimum of 100 pixels
3. Total vertical blanking lines is minimum of 1 line
4. Any data that needs to be sent at the rate of once per frame can be sent during vertical blanking lines

### 7.3.16.1 ABUFF Serializer Configuration and Registers

The serializer Auxiliary Buffer registers are on Page\_11 registers 0x80 through 0xDF. Each of the 12 ABUFFs have 8 registers assigned containing fields for configuration, mapping, and interrupts; as shown in [Table 7-24](#). For additional information on debug and interrupt configuration, refer to the serializer register map.

**Table 7-24. Serializer ABUFF0 Registers**

Register	Bits	Field	Description
Page_11 0x80	7	SDP_OFFSET_CRCNTN_BYP	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUFF packet 1: Offset correction feature is bypassed"
Page_11 0x80	1	ABUFF_TO_PORT_SEL	ABUFF0 Port Select This bit works in conjunction with ABUFF_TO_DEST_SEL. 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer
Page_11 0x80	0	ABUFF_ENABLE	0: ABUFF disabled 1: ABUFF enabled
Page_11 0x82	7:5	ABUFF_TO_DEST_SEL	ABUFF0 Destination Select ABUFF_TO_PORT_SEL to selects the desired port 000: ABUFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 111: Reserved
Page_11 0x82	4:0	SRC_TO_ABUFF_SEL	Maps ABUFF to ABUFF SRCx

### 7.3.16.2 ABUFF Deserializer Configuration and Registers

The deserializer auxiliary buffer registers are on Page\_17 registers 0x80 through 0xDF. Each of the 12 ABUFFs have 3 registers (ABUFFx\_CTL0 through ABUFFx\_CTL8) assigned containing fields for configuration, mapping, and interrupts. [Table 7-25](#) shows the primary registers for enabling and mapping ABUFF0. For additional debug and interrupt configuration, refer to the register map.

**Table 7-25. Deserializer ABUFF0 Registers**

Register	Bits	Field	Description
Page_17 0x80	1	ABUFF_TO_PORT_SEL	ABUFF0 Port Select This bit works in conjunction with ABUFF_TO_DEST_SEL. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer

**Table 7-25. Deserializer ABUFF0 Registers (continued)**

Register	Bits	Field	Description
Page_17 0x80	0	ABUFFx_ENABLE	0: ABUFFx disabled 1: ABUFFx enabled
Page_17 0x82	7:5	ABUFF_TO_DEST_SEL	ABUFF0 Destination Select ABUFF_TO_PORT_SEL to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 111: Reserved

### 7.3.17 Audio

The serializer I2S pins can be sent audio over to the deserializer. For audio pass-through, the audio streams support 32 to 192 kHz sampling rate (32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz), 2 to 8-channels, and 16 to 32 bit word size (all even intervals, e.g. 16, 18, 20, 22, 24, 26, 28, 30, 32). I2S audio is supported from serializer to deserializer but the reverse direction (deserializer to serializer) is not supported.

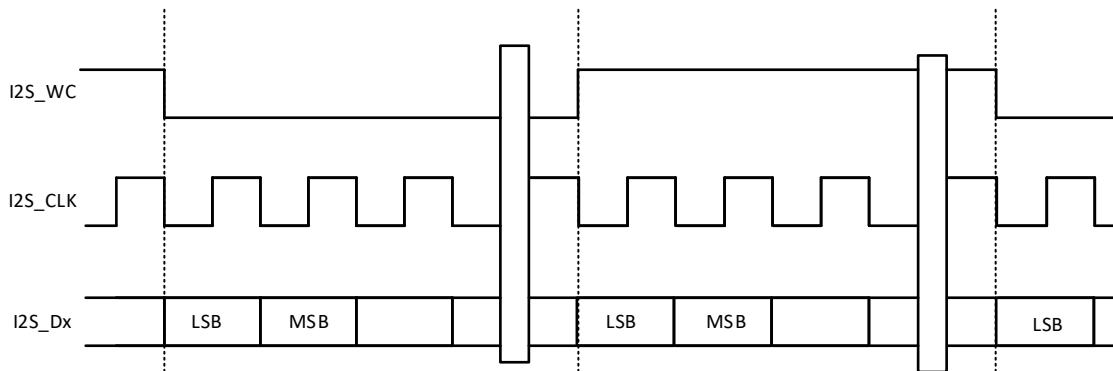
Many of the serializer and deserializer audio registers are configured in the serializer and sent over the FPD-Link to the deserializer. For DS90UH981-Q1, both TDM and I2S audio are received from I2S pins (I2S\_CLK, I2S\_WC, and I2S\_Dx). Downstream deserializers cannot convert between I2S and TDM. Therefore, converting audio modes must be performed by the serializer.

Refer to Application Note SNLA407 *FPD-Link IV Audio* for more details on implementation.

#### 7.3.17.1 Audio Formats

##### 7.3.17.1.1 Parallel I2S

I2S audio is supported externally through I2S pins (I2S\_CLK, I2S\_WC, and I2S\_Dx) which are shared with GPIO pins. The bit clock (I2S\_CLK) supports frequencies between 1 MHz to 12.288 MHz. Four I2S data inputs transport two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2S\_WC) input. Using the I2S\_2\_TDM feature, up to 8 channels of I2S can be multiplexed together to output a TDM signal. The I2S interface supports a range of I2S sample rates as shown in the table below:

**Figure 7-17. I2S Frame Timing Diagram****Table 7-26. I2S Audio Sample Rates Example**

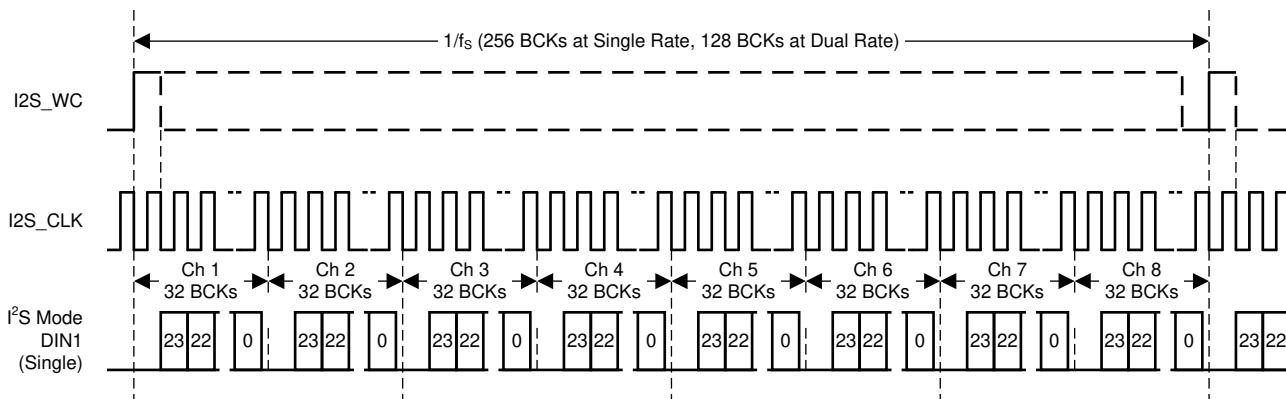
Sample Rate (kHz)	I2S Data Word Size (bits)	I2S CLK (MHz)
32	16	1.024

**Table 7-26. I2S Audio Sample Rates Example (continued)**

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S CLK (MHz)
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

### 7.3.17.1.2 TDM Audio Interface

In addition to the I2S audio interface, the serializer also supports TDM format. A number of specifications for TDM format are in common use, and the DS90Ux98x offers flexible support for word length, bit clock, number of channels that can be multiplexed. For example, assume that word clock signal (I2S\_WC) period =  $256 \times$  bit clock (I2S\_CLK) time period. In this case, the DS90Ux98x can multiplex 8 channels with maximum word length of 32 bits each. Using the TDM\_2\_I2S feature, a TDM input is deconstructed into 8 I2S channels. [Figure 7-18](#) shows the 8 channel TDM with 32-bit word length with 24-bits of data, in a format similar to I2S.

**Figure 7-18. TDM Format**

### 7.3.17.1.3 Audio Inputs and Conversion

The serializer audio input can be in parallel I2S format or TDM format. If I2S\_2\_TDM or TDM\_2\_I2S is set, audio input is converted and sent to deserializer via FPD-Link III or FPD-Link IV datapath and audio transport configuration per [Transport Modes, Splitting, and Forwarding](#). Available registers for TDM configuration and serializer audio format conversion are shown in [Table 7-27](#).

**Table 7-27. FPD-Link IV Serializer Registers: Audio Formatting and Conversion**

Address	Register Name	Field	Description
0x53[7]	AUDIO_CFG	TDM_2_I2S	Enable TDM to parallel I2S audio conversion: When this bit is set, the TDM to parallel I2S conversion is enabled. TDM audio data on the I2S_DA pin splits onto four I2S data signals. In this mode, the input has to be 8 channel with 32-bit word length.
0x53[6]	AUDIO_CFG	I2S_2_TDM	Enable Parallel I2S to TDM Audio conversion: Setting this bit to a 1 enables TDM audio conversion for the I2S audio. Parallel I2S data on the I2S pins is serialized onto a single I2S_DA signal for sending over the serial link. In this mode, the input has to be 16-bit or 32-bit word length and up to 8 channels. Note: the output is 8 channel TDM but if not all 8 channels are used, the unused channels are blanked in the output.
0x53[5]	AUDIO_CFG	AUDIO_MODE	Audio Mode: Selects source for audio to be sent over the FPD-Link III downstream link. 0: Reserved 1: I2S audio from I2S pins
0x53[3]	AUDIO_CFG	TDM_FS_MODE	TDM Frame Sync Mode: Sets active level for the Frame Sync for the TDM audio generator. The Frame Sync signal provides an active pulse to indicate the first sample data on the TDM data signal. 0x0 = Active high Frame Sync. 0x1 = Active low Frame Sync This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
0x53[2]	AUDIO_CFG	TDM_DELAY	TDM Data Delay: Controls data delay for TDM audio samples from the active Frame Sync edge. 0x0 = Data is not delayed from Frame Sync (data is left justified). 0x1 = Data is delayed 1 bit from Frame Sync This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
0x53[1:0]	AUDIO_CFG	TDM_FS_WIDTH	TDM Frame Sync Width: Indicates width of TDM Frame Sync pulse for I2S to TDM conversion 00 = FS is 50/50 duty cycle 01 = FS is one slot/channel wide 1x = FS is 1 clock pulse wide

### 7.3.17.2 Transport Modes, Splitting, and Forwarding

The serializer or deserializer daisy-chain can send Audio to downstream deserializers via Audio over GPIO and Data Island transport modes. Audio over GPIO and Data Island transport modes can be used in FPD-Link III and FPD-Link IV modes, depending on the capability of the serializer and deserializer. The user must pay attention to the FPD mode, transport mode, and port enabling when configuring Audio registers since some registers only apply to certain transport and FPD-Link modes or ports.

Audio over GPIO transport mode utilizes the in-band forward channel GPIO bit stream to send the I2S clock, word clock, and 4 channels of Audio data to the deserializer. In Audio over GPIO mode, the four GPIO signals are assigned as follows:

- FC\_GPIO0 : I2S\_CLK
- FC\_GPIO1 : I2S\_WC
- FC\_GPIO2 : I2S\_DA
- FC\_GPIO3 : I2S\_DB

When Audio via GPIO is enabled, the Audio data is not encrypted via HDCP. Audio via GPIO only supports 2 or 4-channel audio.

Audio Data Island transport mode utilizes Audio packet data in the video stream channel. This method allows 2, 4, or 8 channels of Audio to be sent. Since the Audio is sent over the video channel, the Audio is encrypted if HDCP content protection is enabled for the Audio/Video connection.

Refer to Application Note SNLA407 *FPD-Link IV Audio* for more details on implementation.

#### 7.3.17.2.1 FPD-Link IV Audio Transport Modes

In FPD-Link IV mode, the serializer or local deserializer daisy-chain Audio registers in FPD4\_DATAPATH\_CTL and FPD3\_DATAPATH\_CTL are configured based on desired transport mode, number of Audio channels, and port configuration. Both I2S\_TRANSPORT\_SEL and FPD4\_I2S\_TRANSPORT need to be configured to the same transport mode. I2S\_MODE and FPD4\_I2SB\_FC\_EN are set based on the number of Audio channels. I2S\_TRANSPORT\_SEL, FPD4\_I2S\_TRANSPORT, and FPD4\_I2SB\_FC\_EN are port specific registers and are used in combination with the PORT\_SEL register (0x0E for deserializer daisy-chain and 0x2D for serializer) to select which FPD-Link IV port is configured. I2S transport on FPD-Link Port 0 is enabled by setting main page register 0x02[1] to 1. I2S transport on FPD-Link Port 1 is enabled by setting main page register 0x02[2] to 1. When enabled, transport mode for each port is set based on the I2S\_TRANSPORT\_SEL and FPD4\_I2S\_TRANSPORT.

When transporting Audio via Data Island transport mode with video present, there is a minimum horizontal blanking constraint based the amount of Audio bits accumulated during active video portion of the frame.

$$\text{AUDIO_FPD_FRAME_CNT} * \text{FPD_FRAME_PERIOD} < \text{HBLANK_PERIOD} \quad (26)$$

Where

$$\text{AUDIO_FPD_FRAME_CNT} = (\text{AUDIO_BITS_PER_LINE} / 128) + 2$$

$$\text{AUDIO_BITS_PER_LINE} = (\text{HTOTAL} / \text{PCLK}) * (\text{I2S_CLK} * 4)$$

$$\text{FPD_FRAME_PERIOD} \text{ (in ns)} = 132 / \text{FPD RATE} \text{ (in Mbps)}$$

PCLK = Pixel Clock in MHz

$$\text{HBLANK_PERIOD} \text{ (in ns)} = (\text{HTOTAL} - \text{HACTIVE}) / \text{PCLK} \text{ (in MHz)}$$

Where

If I2S: I2S\_CLK=SAMPLE\_RATE\*WORD\_SIZE\*2

If TDM: I2S\_CLK=SAMPLE\_RATE\*WORD\_SIZE\*NUMBER\_CHANNELS

When operating in Data Island transport mode, the Audio data is transmitted through the auxiliary buffers described in [Auxiliary Buffers and Secondary-Data Packets \(SDP\)](#). By default, ABUFF0 and ABUFF1 are configured for packetized Audio transport. For general use cases, ABUFF0 must be enabled and mapped to Link Layer 0 when Link Layer 0 Audio is desired and ABUFF1 must be enabled and mapped to Link Layer 1 when Link Layer 1 Audio is desired. Audio data can be transmitted without video through any desired stream by mapping ABUFFx to that stream. To extract Audio output from a terminating deserializer, Stream 0 must be enabled and used for ABUFF with audio.

**Table 7-28. FPD-Link IV Transmit Audio Configuration**

Serializer Configuration Field	Field Name	Description
Main_Page 0x5A[3]	I2S_TRANSPORT_SEL	Enable I2S data as Forward Channel Data Island 0x0 = Enable I2S Data Island Transport 0x1 = Enable I2S Data Forward Channel Frame Transport

**Table 7-28. FPD-Link IV Transmit Audio Configuration (continued)**

Serializer Configuration Field	Field Name	Description
Main_Page 0x5A[1:0]	I2S_MODE	I2S Channel Mode 0x0 = 2-channel I2S audio 0x1 = 4-channel I2S audio 0x2 = 5.1- or 7.1-channel surround audio is enabled 0x3 = Reserved Note that I2S Data Island Transport is the only option for surround audio.
Main_Page 0x0D[6]	FPD4_I2SB_FC_EN_Px	If FPD4 Audio uses forward channel GPIO, this bit enables 4-channel audio using FC_GPIO[3]. This is per port register.
Main_Page 0x0D[5]	FPD4_I2S_TRANSPORT_Px	In FPD4, this indicates if 0x0 = I2S data over FC_GPIO if bit [4] is set. This bit for port 1 is default set to 0 This is per port register.
Main_Page 0x0D[4]	FPD4_FC_SD_P_STREAM_Px	In FPD4, if bit[5] is 0: 0x0 = I2S audio for FPD4 is disabled (default) 0x1 = I2S audio over FC_GPIO enabled. This is a per port register. If bit[5] is 1: 0x0 = I2S over data island through SDP0 stream 0x1 = I2S over data island through SDP1 stream
Main_Page 0x02[2:1]	I2S_EN	Enable I2S input and transport 0x1 = Enabled I2S transport through FPD-Link Port 0 0x2 = Enables I2S transport through FPD-Link Port 1
Main_Page 0x05[1:0]	I2S_AUDIO_SPLIT	Split audio for FPD4 Port 0 and Port 1; If I2S is enabled, and audio over GPIO is selected, select I2S_DA and I2S_DB or I2S_DC and I2S_DD.

### 7.3.17.2.2 FPD-Link III Audio Transport Modes

By default, audio transport in FPD-Link III mode is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames can be disabled from control registers if Audio over GPIO is desired. In this mode, I2S\_DA and I2S\_DB are transmitted to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer. If connected to a DS90UB926Q-Q1 deserializer, only I2S\_DA is transmitted. Surround Sound Mode, which transmits all four I2S data inputs (I2S\_D[A..D]), can only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer.

To disable Data Island Transport mode and use Audio over GPIO mode instead, set I2S\_TRANSPORT\_SEL to 1. Set the number of I2S channels in the I2S\_MODE (0x5A[1:0]) register.

Table 7-29 shows I2S\_MODE and I2S\_TRANSPORT\_SEL settings for the possible channel count and transport mode combinations for FPD-Link III audio transmitting from serializer or deserializer daisy-chain output. Table 7-30 shows the specific registers used for FPD-Link III audio transport configuration in either Audio over GPIO or Data Island transport modes.

**Table 7-29. FPD-Link III TX Audio Example Configurations**

I2S Pins	Number of Audio Channels	Transport Mode	I2S_MODE (Main_Page 0x5A[1:0])	I2S_TRANSPORT_SEL (Main_Page 0x5A[3])
1	2	Data Island	0b00	0
1	2	Audio over GPIO	0b00	1
2	4	Data Island	0b01	0
2	4	Audio over GPIO	0b01	1

**Table 7-29. FPD-Link III TX Audio Example Configurations (continued)**

I2S Pins	Number of Audio Channels	Transport Mode	I2S_MODE (Main_Page 0x5A[1:0])	I2S_TRANSPORT_SEL (Main_Page 0x5A[3])
4	8 <sup>(1)</sup>	Data Island	0b10	0

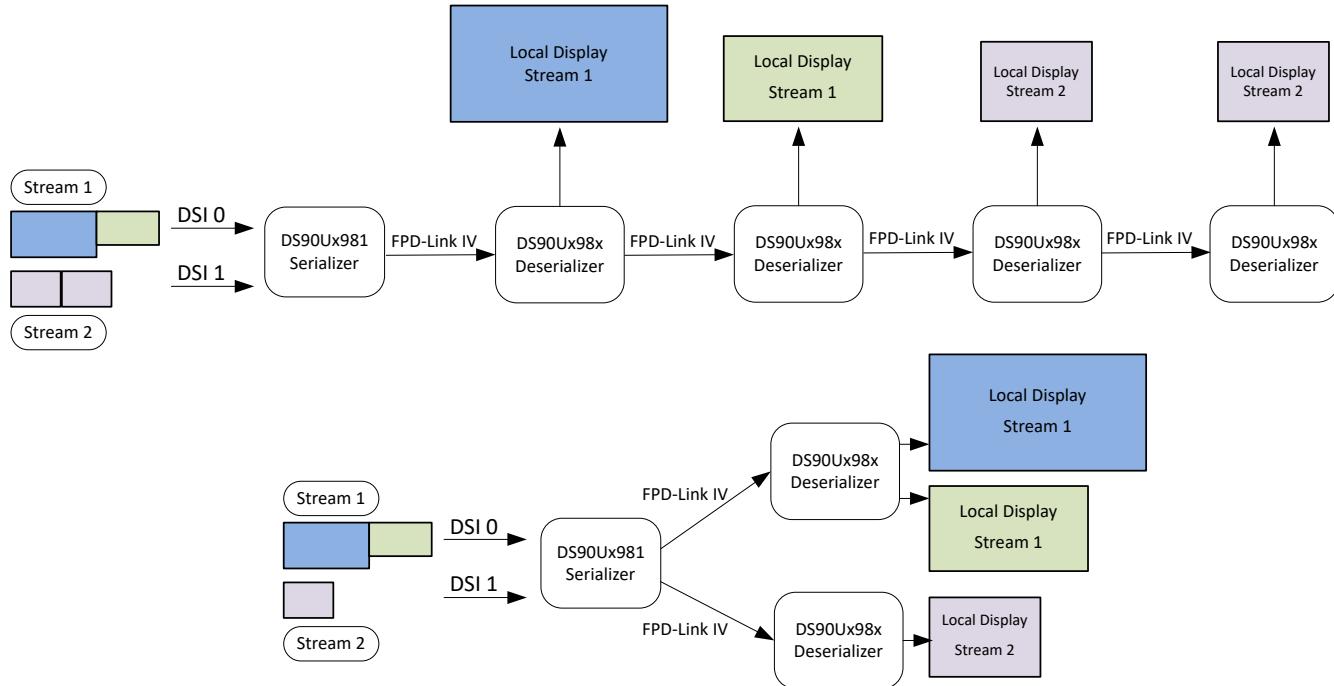
(1) If only use 6 channels, serializer treats Data Island like an I2S input with blanked data. Two unused channels can be blanked.

**Table 7-30. FPD-Link III Transmit Audio Configuration**

Serializer Configuration Field	Field Name	Description
Main_Page 0x5A[3]	I2S_TRANSPORT_SEL	Enable I2S data as Forward Channel Data Island 0x0 = Enable I2S Data Island Transport 0x1 = Enable I2S Data Forward Channel Frame Transport
Main_Page 0x5A[1:0]	I2S_MODE	I2S Channel Mode 0x0 = 2-channel I2S audio 0x1 = 4-channel I2S audio 0x2 = 5.1- or 7.1-channel surround audio is enabled 0x3 = Reserved Note that I2S Data Island Transport is the only option for surround audio.
Main_Page 0x0D[6]	FPD4_I2SB_FC_EN_Px	Audio uses forward channel GPIO, this bit enables 4-channel audio using FC_GPIO[3]. This is per port register.
Main_Page 0x0D[5]	FPD4_I2S_TRANSPORT_Px	This bit indicates if 0x0 = I2S data over FC_GPIO if bit [4] is set. This bit for port 1 is default set to 0 This is per port register.
Main_Page 0x0D[4]	FPD4_FC_SD_PX	If bit[5] is 0: 0x0 = I2S audio for FPD4 is disabled. - Default 0x1 = I2S audio over FC_GPIO enabled. This is per port register. If bit[5] is 1: 0 = I2S over data island through SDP0 stream 1 = I2S over data island through SDP1 stream
Main_Page 0x02[2:1]	I2S_EN	Enable I2S input and transport 0x1 = Enabled I2S transport through FPD-Link Port 0 0x2 = Enables I2S transport through FPD-Link Port 1

### 7.3.18 FPD-Link IV Daisy-Chaining

When the DS90UH981-Q1 is paired with FPD-Link IV deserializers, daisy-chain functionality supported for both FPD-Link IV or FPD-Link III modes drivers. Daisy-chaining allows the user to system to drive multiple displays from one source stream. The FPD-Link IV deserializers can extract 1 or more video stream(s) for export to a local display with remaining video streams forwarded to any downstream deserializers. With four video processors on the DS90UH981-Q1, up to four display streams can be supported (the last deserializer can be either an FPD-Link IV deserializer or FPD-Link III deserializer). Possible use cases can be seen in the [Figure 7-19](#), showing the deserializer configured for 1 video stream output and 2 video stream outputs. More info on daisy-chaining can be found in FPD-Link IV deserializer data sheets.


**Figure 7-19. Daisy-Chaining Application Examples**

### 7.3.19 General-Purpose I/O

#### 7.3.19.1 GPIO[0:13] Configuration

In normal operation, GPIO[0:13] can be used as general purpose inputs or outputs. GPIO modes are configured in the GPIOx\_PIN\_CTL registers (0x17 - 0x24). GPIO[10:13] share pins with the SPI interface in FPD-Link III backward compatibility mode. When using the SPI interface, the SPI configuration will override standard GPIO register configuration. GPIO[2:3] and GPIO[5:8] share pins with the I2S audio interface. When using the I2S interface, I2S configuration settings will override standard GPIO register configuration. GPIO[11:12] shares pins with I2C\_SDA1 and I2C\_SCL1 and can be used for I<sup>2</sup>C communication if the GPIO[11:12] input is enabled. When using I<sup>2</sup>C1 interface in use, the pull-up resistor requires on GPIO[11:12] pin.

If a GPIO is set to "VP Combined INTERRUPT Status" when a VP interrupt occurs then the GPIO will pulse high for about 40 ns or if set to "Inverted VP Combined INTERRUPT Status" low for about 40 ns. This can be used to detect and count VP interrupts as they occur. The interrupt status can also be read from a register.

**Table 7-31. GPIO Configuration**

GPIO Output Function	Source	GPIO Output Enable GPIOx_PIN_CTL[7]	GPIOX Output Source Select GPIOx_PIN_CTL[6:4]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[3:0]
GPIOx Output Disabled	X	0	X	X
GPIOx linked to BC_GPIO0	Received from FPD Port 0	1	000	0000
GPIOx linked to BC_GPIO1		1	000	0001
GPIOx linked to BC_GPIO2		1	000	0010
GPIOx linked to BC_GPIO3		1	000	0011
GPIOx linked to BC_GPIO4		1	000	0100
GPIOx linked to BC_GPIO5		1	000	0101
GPIOx linked to BC_GPIO6		1	000	0110
GPIOx linked to BC_GPIO7		1	000	0111
PORT0 REM_INTB		1	000	1000
PORT0 RX_LOCK_DET		1	000	1001
PORT0 FPD3_TX_INTN		1	000	1010
PORT0 FPD3_TX_INT		1	000	1011
PORT0 RX_LOCK_DET ANDed with PORT1 RX_LOCK_DET		1	000	1100
Reserved	Reserved	1	000	1101-1111
GPIOx linked to BC_GPIO8	Received from FPD Port 0	1	100	0000
GPIOx linked to BC_GPIO9		1	100	0001
GPIOx linked to BC_GPIO10		1	100	0010
GPIOx linked to BC_GPIO11		1	100	0011
GPIOx linked to BC_GPIO12		1	100	0100
GPIOx linked to BC_GPIO13		1	100	0101
GPIOx linked to BC_GPIO14		1	100	0110
GPIOx linked to BC_GPIO15		1	100	0111
PORT0 REM_INTB		1	100	1000
PORT0 RX_LOCK_DET		1	100	1001
PORT0 FPD3_TX_INTN		1	100	1010
PORT0 FPD3_TX_INT		1	100	1011
Reserved	Reserved	1	100	1100-1111

**Table 7-31. GPIO Configuration (continued)**

GPIO Output Function	Source	GPIO Output Enable GPIOx_PIN_CTL[7]	GPIOX Output Source Select GPIOx_PIN_CTL[6:4]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[3:0]
GPIOx linked to BC_GPIO0	Received from FPD Port 1	1	001	0000
GPIOx linked to BC_GPIO1		1	001	0001
GPIOx linked to BC_GPIO2		1	001	0010
GPIOx linked to BC_GPIO3		1	001	0011
GPIOx linked to BC_GPIO4		1	001	0100
GPIOx linked to BC_GPIO5		1	001	0101
GPIOx linked to BC_GPIO6		1	001	0110
GPIOx linked to BC_GPIO7		1	001	0111
PORT1 REM_INTB		1	001	1000
RX_LOCK_DET		1	001	1001
FPD3_TX_INTN		1	001	1010
FPD3_TX_INT		1	001	1011
Reserved		1	001	1100-1111
GPIOx linked to BC_GPIO8	Received from FPD Port 1	1	101	0000
GPIOx linked to BC_GPIO9		1	101	0001
GPIOx linked to BC_GPIO10		1	101	0010
GPIOx linked to BC_GPIO11		1	101	0011
GPIOx linked to BC_GPIO12		1	101	0100
GPIOx linked to BC_GPIO13		1	101	0101
GPIOx linked to BC_GPIO14		1	101	0110
GPIOx linked to BC_GPIO15		1	101	0111
REM_INTB		1	101	1000
RX_LOCK_DET		1	101	1001
FPD3_TX_INTN		1	101	1010
FPD3_TX_INT		1	101	1011
Reserved	Reserved	1	101	1100-1111

**Table 7-31. GPIO Configuration (continued)**

GPIO Output Function	Source	GPIO Output Enable GPIOx_PIN_CTL[7]	GPIOX Output Source Select GPIOx_PIN_CTL[6:4]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[3:0]
Fixed output value of 0	NA	1	x10	0000
Fixed output value of 1		1	x10	0001
Inverted INTERRUPT STATUS		1	x10	0010
INTERRUPT STATUS		1	x10	0011
Inverted VP Combined INTERRUPT Status		1	x10	0100
VP Combined INTERRUPT Status		1	x10	0101
Reserved		1	x10	0110-1111

**Table 7-32. GPIO Output Functions**

GPIO OUTPUT FUNCTION	FUNCTION DESCRIPTION
REM_INTB	INTB_IN signal for the deserializer
RX_LOCK_DET	FPD-LinkLock status from the deserializer see "FPD-Link Lock" section
FPD3_TX_INT	FPD-Link III interrupt
FPD3_TX_INTN	Inverted FPD-Link III interrupt
INTERRUPT STATUS	Global Interrupt signal (Inverse of the Interrupt Pin)
Inverted INTERRUPT STATUS	Global Interrupt signal Inverted (mirrors the Interrupt Pin)
VP Combined INTERRUPT Status	The GPIO will be high for about 40ns when a interrupt in the video processor is triggered
Inverted VP Combined INTERRUPT Status	The GPIO will be low for about 40ns when a interrupt in the video processor is triggered

### 7.3.19.2 Back Channel GPIO Configuration

For Back Channel GPIO operation, 1, 4, 8, or 16 GPIOs can be sent over the back channel frame where the number of Back Channel GPIOs is programmed via GPIO\_BC\_EN register. When GPIO[0:13] pins are configured to output back channel GPIOs, the effective GPIO frequency depends on the back channel frequency and configuration, configured by the partner deserializer. Consult the appropriate deserializer data sheet for details on how to configure the back channel frequency. As well, the selected deserializer GPIOs must be configured to be sent on the back channel using the deserializer registers. GPIO0 has the option to enable High-Speed GPIO mode through GPIO\_BC\_EN register on the serializer and BC\_FRAMES is programmed on the paired FPD-Link IV deserializer.

When configuring back channel GPIOs, set main page register ENH\_BC\_CHK (0x6C[5]) field ENH\_BC\_CHK\_EN to 1 and 0x6C[3:2] field LNK\_DET\_CNT to 0x3. Note that register 0x6C is a port specific register and is used in combination with the PORT\_SEL register (0x0E) to select each FPD-Link port.

The procedure below is an example configuring the GPIOx information carried from backward compatible DS90Ux94x, and DS90Ux92x deserializer to the DS90UH981-Q1 serializer. Note that the D\_GPIO[3:0] of the backward compatible device, such as a DS90Ux94x or DS90Ux92x deserializer requires dual link mode operation. For normal GPIO operation, setting dual link port is not required.

Setting backward compatible for FPD-Link III mode GPIOs:

- Establish a link between the serializer and deserializer.
- Configure the deserializer device to dual port mode operation in register 0x34[1:0] = 0x3.
- Select the desired D\_GPIO pin for example D\_GPIO3 in register 0x1F[3:0]= 0x3.
- Apply VDDIO to the D\_GPIO3 for the deserializer.
- Configure the serializer DS90UH981-Q1 device for dual port mode in register 0x2D = 0x12.
- Disable the GPIOx input GPIO\_IN\_EN\_HIGH[5:0] in register 0x3E and GPIO\_IN\_EN\_LOW[7:0] in register 0x3F.

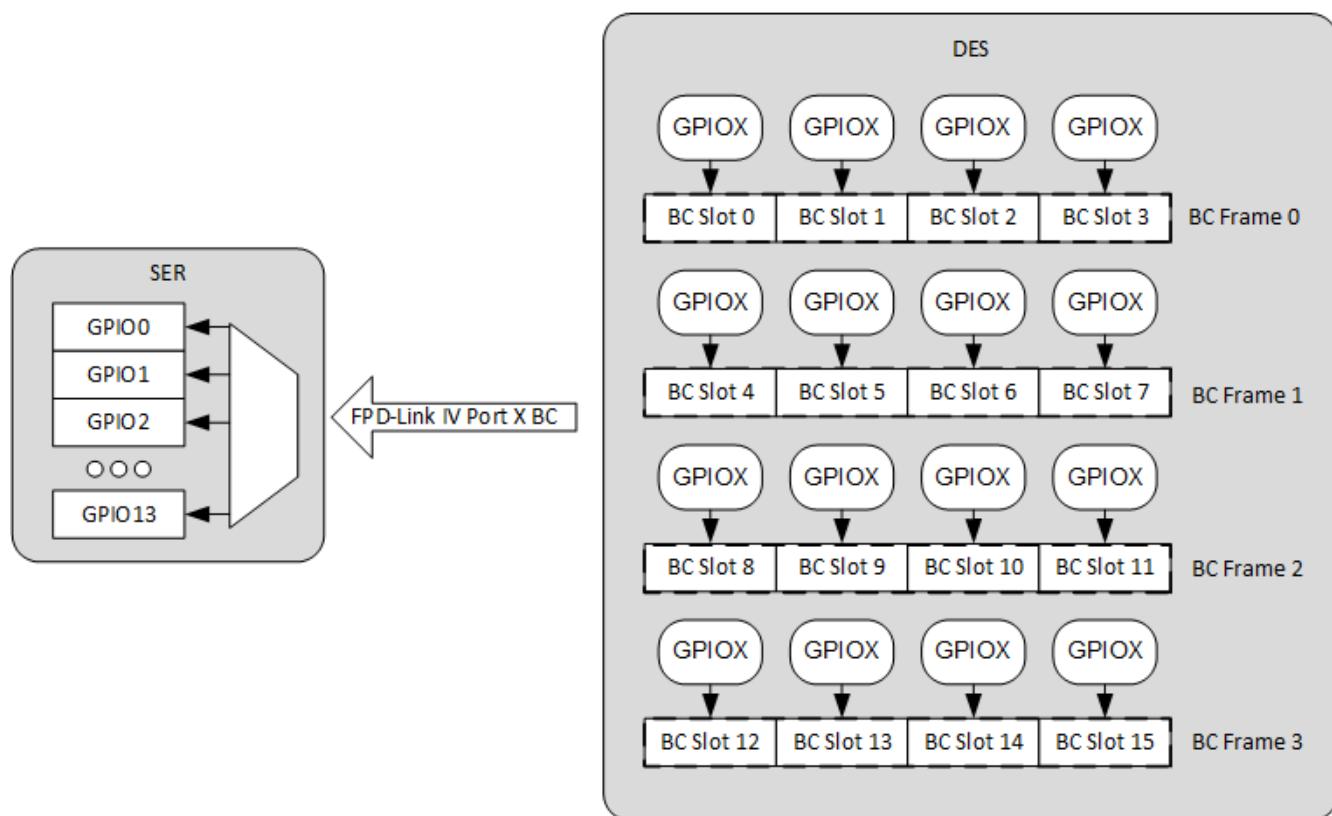
- Enable GPIO output GPIOx\_PIN\_CTL[3:0] in register 0x17 - 0x24. (DGPIOS are always received on port1, if so, port1 needs to be selected from GPIOx\_PIN\_CTL[6:4])
- Set GPIO output enable GPIOx\_PIN\_CTL[7] in register 0x17 - 0x24.

Setting back channel for FPD-Link IV mode GPIOs:

- Refer to deserializer 98x devices for register configuration.
- Select the desired GPIOx in the register GPIOx\_PIN\_CTL[6:4] and GPIOx\_PIN\_CTL[3:0]

**Table 7-33. Back Channel GPIO Configuration**

DESCRIPTION	OUTPUT SIGNAL
GPIO_BC_EN	0x0: Four GPIO slots from the Back Channel mapped on local GPIO[3:0] slots 0x1:Eight GPIO slots from the Back Channel mapped on local GPIO[7:0] slots 0x10: Sixteen GPIO slots from the Back Channel mapped on local [GPIO15:0] slots (Only up to fourteen GPIOs mapped is a valid configuration due to the limited number of GPIOs) 0x11: One HS-GPIO0



**Figure 7-20. Back Channel GPIO**

### 7.3.19.3 Forward Channel GPIO Configuration

The DS90UH981-Q1 can send input data from the GPIO pins across the forward channel to a remote deserializer. In order to do this, the GPIO pin must be programmed for input mode using the GPIOx\_PIN\_CTL registers. There are four forward channel GPIO signals (FC\_GPIOx) per FPD port that can be used to send data from any of the fourteen GPIO pins. All FC\_GPIOx signals are sent as part of every other forward channel frame. The same GPIO pin can be connected to multiple forward channel GPIO signals. In addition to sending input data from GPIO pins, fixed values can also be sent on the forward channel GPIO signals. For each port, the following GPIO controls are available through the FC\_GPIO\_CTL0 (0x15), FC\_GPIO\_CTL1 (0x16), and FPD4\_DATAPATH\_CTL (0x0D) registers :

The procedure below is an example configuring the GPIOx information carried from DS90UH981-Q1 serializer to the backward compatible DS90Ux94x, and DS90Ux92x deserializer. Note that the D\_GPIO[3:0] of the backward

compatible device such as DS90Ux94x, and DS90Ux92x deserializer requires to set dual link mode operation. For normal GPIO operation, setting dual link is not required.

Setting forward channel FPD-Link III mode GPIOs:

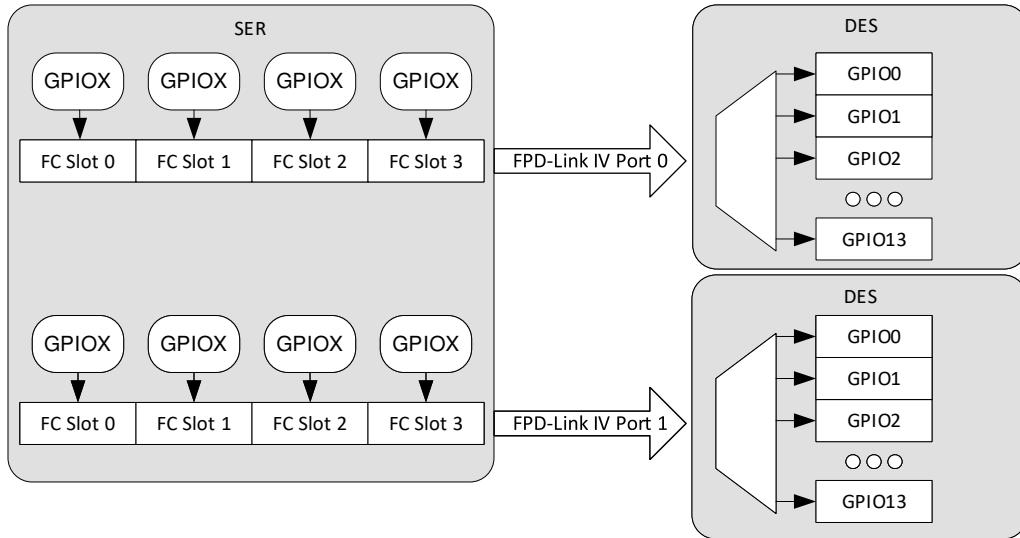
- Establish a link between the serializer DS90UH981-Q1 and deserializer 92x and 94x.
- Configure the deserializer device to dual port mode operation in register 0x34[1:0] = 0x3.
- Select the desired D\_GPIOx pin, for example D\_GPIO3 in register 0x1F[3:0]= 0x5.
- Configure the serializer DS90UH981-Q1 device in dual port mode in register 0x59 = 0x3.
- There are a total of 4 GPIO slots for GPIO mapping. These slots are corresponded to the GPIOx in the deserializer. For example, FC\_GPIO slot 3 is programmed to use GPIO3 pin as the source. Enabling the desired GPIOx slot in register FPD4\_DATAPATH\_CTL[1:0] = 0x3. This will enable four GPIO[3:0] for the deserializer.
- Assign the desired GPIOx for the DS90UH981-Q1 device by configuring the register 0x15 and 0x16. For this example set FC\_GPIO\_CTL1[7:0] = 0x0 to assign GPIO0 for DS90UH981-Q1.
- Apply 1.8V to GPIO0 of the DS90UH981-Q1 device
- Enable the GPIOx input GPIO\_IN\_EN\_HIGH[5:0] in register 0x3E and GPIO\_IN\_EN\_LOW[7:0] in register 0x3F.
- Disable GPIO output GPIOx\_PIN\_CTL[7] in register 0x17 - 0x24.

Setting forward channel FPD-Link IV mode GPIOs:

- Establish a link between the serializer DS90UH981-Q1 and deserializer 98x.
- Configure the serializer DS90UH981-Q1 device in dual port mode in register 0x05 FPD4\_CFG[5:2].
- Assign the desired GPIOx for the DS90UH981-Q1 device by configuring the register 0x15 and 0x16. For this example set FC\_GPIO\_CTL1[7:0] = 0x0 to assign GPIO0 for DS90UH981-Q1.
- Apply 1.8V to GPIO0 of the DS90UH981-Q1 device
- Enable the GPIOx input GPIO\_IN\_EN\_HIGH[5:0] in register 0x3E and GPIO\_IN\_EN\_LOW[7:0] in register 0x3F.
- Disable GPIO output GPIOx\_PIN\_CTL[7] in register 0x17 - 0x24.

**Table 7-34. Forward Channel GPIO Configuration**

DESCRIPTION	OUTPUT SIGNAL
GPIOEN_FC	GPIOs disabled: GPIOEN_FC = 0x00 One GPIO: GPIOEN_FC = 0x01 Two GPIOs: GPIOEN_FC = 0x02 Four GPIOs: GPIOEN_FC = 0x03
FC_GPIOx	GPIO0: FC_GPIOx_SEL = 0000 GPIO1: FC_GPIOx_SEL = 0001 GPIO2: FC_GPIOx_SEL = 0010 ... GPIO13: FC_GPIOx_SEL = 1101 Constant value of 0: FC_GPIOx_SEL = 1110 Constant value of 1: FC_GPIOx_SEL = 1111

**Figure 7-21. Forward Channel GPIO**

### 7.3.20 Internal Pattern Generation

The DS90UH981-Q1 serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no input is applied. For FPD-Link IV operation, there is one pattern generator per video processor.

#### 7.3.20.1 Pattern Options

The DS90UH981-Q1 serializer pattern generator is capable of generating 20 default patterns for use in basic testing and debugging of panels. Each can be inverted using PGCTL register and the FPD4\_PGCTL\_VPx registers on Page\_12, shown below:

1. Checkerboard (White/Black)
2. White
3. Black
4. Red
5. Green
6. Blue
7. Horizontally Scaled Black to White
8. Horizontally Scaled Black to Red
9. Horizontally Scaled Black to Green
10. Horizontally Scaled Black to Blue
11. Vertically Scaled Black to White
12. Vertically Scaled Black to Red
13. Vertically Scaled Black to Green
14. Vertically Scaled Black to Blue
15. Custom color (or the inversion) configured in PGRS, PGGS, PGBS registers
16. VCOM (Yellow, Cyan, Yellow, Red)
17. Alternate VCOM (Blue, Cyan, Yellow, Red)
18. Custom Color Checkerboard (Custom/Black)
19. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black)
20. UNH-IOL MIPI D-PHY Compliance Test Pattern

Due to the quad pixel clock architecture of the FPD-Link IV serializer devices, patterns #6-9 (horizontally scaled patterns) and #19 (color bars) must only be used when the active line length meets a minimum number of pixels

based on the configured bits per color. If the minimum horizontal pixel count is not met, then the pattern does not correctly scale to the screen size (ex. less than 8 color bars shown). If the screen size does not meet the minimum number of horizontal pixels, then it is suggested to use one of the other available patterns instead.

**Table 7-35. Minimum Pixels Per Line for PATGEN Horizontally Scaled or Color Bar Patterns**

PATGEN Bits Per Pixel	Minimum Active Horizontal Pixels
30bpp	4096
24bpp	1024
18bpp	256

### 7.3.20.2 Color Modes

By default, the Pattern Generator operates in 24-bit color mode, where 8 most significant bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode and 30-bit color mode can be activated from the configuration registers. In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled; the 2 least significant bits will be 0. In 30-bit mode, 10 most significant bits of the Red, Green, and Blue outputs are enabled.

### 7.3.20.3 Video Timing

The Pattern Generator uses the video timing settings of the video processor being used to generate the pattern. Set the PATGEN\_TSEL field (Page\_12 registers 0x29, 0x69, 0xA9, 0xE9) to 0 to use the video processor timing when the video processor timing is used to generate the pattern. The PATGEN\_FREERUN field Page\_12 registers 0x28, 0x68, 0xA8, 0xE8) must be set to 1 to operate independently from the incoming video.

### 7.3.20.4 Pattern Inversion

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

### 7.3.20.5 Auto Scrolling

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns can be defined in the registers. The patterns can appear in any order in the sequence and can also appear more than once. The pattern sequence can be configured through PGTS0x register found in [PATGEN Registers](#).

### 7.3.20.6 Additional Features

Additional pattern generator features can be accessed through the Pattern Generator Indirect Register Map. There is one copy of this register map per each video processor. It can be accessed through the Pattern Generator Indirect Address (PGIA) (0x66 Main Page and 0x2A, 0x6A, 0xAA, and 0xEA on Page\_12) and the Pattern Generator Indirect Data (PGID) registers (0x67 Main Page and 0x2B, 0x6B, 0xAB, and 0xEB on Page\_12). See [Application Note AN-2198](#).

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**7.3.21 Backward Compatibility**

The DS90UH981-Q1 serializer is backward compatible to DS90Ux94x and DS90Ux92x deserializers. To enable backward capability, set the desired channel to FPD-Link III mode via FPD3\_TX\_MODE (0x59[2:0]). The FPD-Link III data path can be connected to any of the four video streams from the video processor modules FPD3\_STREAM\_SEL(0x57) register.

**Table 7-36. Backward Compatibility**

MODE	DESERIALIZER	PCLK	Forward Channel Rate	Back Channel Rate	Output Format	Typical Resolution Supported
Single Link	DS90UB924	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	10 Mbps	oLDI	900p/720p
	DS90Ux926	25 MHz ≤ PCLK ≤ 85 MHz	875 Mbps to 2.975 Gbps	10 Mbps	RGB	720p
	DS90Ux928	25 MHz ≤ PCLK ≤ 85 MHz	875 Mbps to 2.975 Gbps	10 Mbps	oLDI	720p
	DS90Ux940	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	900p / 720p
	DS90Ux940N	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	900p / 720p
	DS90Ux948	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	900p / 720p
	DS90Ux984 in FPD-Link III Mode	25 MHz ≤ PCLK ≤ 162 MHz	875 Mbps to 5.67 Gbps	5 Mbps 10 Mbps 20 Mbps	DP	1080p
	DS90Ux988 in FPD-Link III Mode	25 MHz ≤ PCLK ≤ 162 MHz	875 Mbps to 5.67 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	1080p
Dual Link	DS90Ux948	50 MHz ≤ PCLK ≤ 192 MHz	1.75 Gbps to 6.72 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	2K (2048x1080) / FHD (1920x1080)
	DS90Ux940	50 MHz ≤ PCLK ≤ 170 MHz	1.75 Gbps to 5.95 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	WUXGA (1920×1200) / FHD (1920x1080)
	DS90Ux940N	50 MHz ≤ PCLK ≤ 170 MHz	1.75 Gbps to 5.95 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	WUXGA (1920×1200) / FHD (1920x1080)
	DS90Ux984 in FPD-Link III Mode	50 MHz ≤ PCLK ≤ 324 MHz	1.75 Gbps to 11.34 Gbps	5 Mbps 10 Mbps 20 Mbps	DP	2K/3K
	DS90Ux988 in FPD-Link III Mode	50 MHz ≤ PCLK ≤ 324 MHz	1.75 Gbps to 11.34 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	2K/3K

The DS90Ux94x deserializer linerates are automatically set based on the PCLK frequency. In the FPD-Link III mode, the PLL must be programmed to generate the correct line rate (dividers, Reference REFCLK select, etc.) and the ENABLE\_FPD3\_FIFO (0x5B[3]) register must be set to 1.

**7.3.21.1 Video Processor Configuration in FPD-Link III Mode**

Video filtering, video cropping, and video timing parameters must be configured in the same manner as in FPD-Link IV Mode. However, the PCLK used in FPD-Link III mode is sourced directly from the reference source, not from the forward channel rate so the video processor frequency is set differently. As well, the FPD-Link port configuration is different in FPD-Link III mode vs FPD-Link IV mode. In FPD-Link III mode, only one video stream is assigned to each FPD-Link Port, meaning that a maximum of two video processors can be enabled.

### 7.3.21.1.1 FPD-Link III Port Configuration

Each FPD-Link III Port can transmit data from one of the four video processors (VP0 to VP3). The FPD3\_STREAM\_SEL (0x57) register is used to select which video processor the FPD-Link Port transmits. In Independent or Single FPD-Link III modes select the FPD-Link port using PORT\_SEL (0x2D) then set the FPD3\_STREAM\_SEL register to select the video processor for the FPD-Link port. In Dual FPD-Link III the register is not port specific and the setting applies to both ports.

**Table 7-37. Video Stream Forwarding**

Video Processor	FPD-Link Port
VPx	VP0: FPD3_STREAM_SEL[1:0] = 0x0 VP1: FPD3_STREAM_SEL[1:0] = 0x1 VP2: FPD3_STREAM_SEL[1:0] = 0x2 VP3: FPD3_STREAM_SEL[1:0] = 0x3

### 7.3.21.1.2 Video Processor Frequency

The video processor clock is a quad-pixel clock generated automatically to be 1/4 of the PCLK corresponding to the selected FPD-Link III line rate. The video processor clock is generated using a phase-locked loop (PLL) with the selected reference clock as the input, as shown in the FPD-Link III PLL section. The reference clock source is selected using either the CH0\_FPD3\_REFCLK1 or CH1\_FPD3\_REFCLK1 bits (0x5[6] or 0x5[7]). The VCO's (voltage controlled oscillators) range is 3500 MHz to 7000 MHz. Configuring the PLL requires selecting the input source, setting the N-divider, numerator, denominator, MASH order (either integer or fractional), and the post-divider. After configuring these settings, the PLL must be reset using either the PLL\_CH0\_RESET or PLL\_CH1\_RESET bits (0x1[5] or 0x1[4]). The video processor clock is governed by the following equations:

$$VP\_CLK = \frac{\text{Target\_PCLK}}{4} \quad (27)$$

$$\text{FPD3\_Line\_Rate(MHz)} = \text{Target\_PCLK} \times 35 \quad (28)$$

$$f_{VCO}(\text{MHz}) = \left( \frac{\text{FPD3\_Line\_Rate}}{2} \right) \times P \quad (29)$$

where

- $f_{VCO}$  is the VCO frequency
- P is the post-divider value (2, 4, 8, or 16)

$$f_{VCO} = f_{\text{REF}} \times 2 \times \left[ N + \left( \frac{\text{NUM}}{\text{DEN}} \right) \right] \quad (30)$$

where

- $f_{\text{Ref}}$  is the reference frequency, either from the REFCLK0 or REFCLK1
- N is the integer portion of the N-divider (0 to 65,535)
- NUM is the numerator portion of the N-divider fraction (0 to 16,777,206),  $\text{NUM} \leq \text{DEN}$
- DEN is the denominator portion of the N-divider fraction (1 to 16,777,206)

### 7.3.21.1.3 Example FPD-Link III PLL Calculation

1. Start with the desired PCLK frequency and calculate the corresponding FPD-Link III Line Rate (PCLK  $\times$  35).
  - EX: PCLK = 95.75 MHz, so FPD-Link III Line Rate = 3351.25 MHz
2. Then consider all potential VCO frequencies (FPD-Link III Line Rate / 2  $\times$  P) and find the valid VCO frequencies which fall in the VCO range of 3500-7000MHz
  - EX: Potential VCO frequencies are:  $3351.25 / 2 \times 2 = 3351.25$  MHz,  $3351.25 / 2 \times 4 = 6702.5$  MHz,  $3351.25 / 2 \times 8 = 13,405$  MHz, and  $3351.25 / 2 \times 16 = 26,810$  MHz. Only 6702.5 MHz is a valid VCO frequency. This means that POST\_DIV must be programmed to 0x6 (selects a post-divider of 4).
3. Determine the integer portion of the N-divider (integer portion of  $f_{VCO} / (2 \times f_{\text{Ref}})$ ).

- EX:  $6702.5 / (2 \times f_{\text{Ref}}) = 6702.5 / (2 \times 27) = 124.12$  so the integer portion is 124. This means that NDIV[7:0] must be programmed to 0x7C and NDIV[15:8] must be programmed to 0x00.
4. Determine the numerator and denominator of the N-divider (fractional portion of  $f_{\text{VCO}} / (2 \times f_{\text{Ref}})$ ).
- EX:  $6702.5 / (2 \times 27) - 124 = 0.12 \overline{037}$ . A fractional approximation of this is 13/108. Larger denominators are preferred when possible. To find the form of this fraction with the largest possible denominator, find the closest multiple of the denominator to the maximum denominator (16,777,206). Divide the maximum denominator (16,777,206) by the current denominator (108) and round down:  $16,777,206 / 108 = 155,344.5$  so use the 155,344th multiple of the original fraction. Multiplying our numerator and denominator by this factor gives us our final fraction:  $2,019,472 / 16,777,152^2$

**Table 7-38. FPD-Link III Clock Register Configuration**

Reference Select	REFCLK0: CHx_FPD3_REFCLK1 = 0 REFCLK1: CHx_FPD3_REFCLK1 = 1
N-Divider	NDIV[15:0] = Integer portion of N divider
Numerator	NUM[23:0] = Numerator portion of N divider
Denominator	DEN[23:0] = Denominator portion of N divider
MASH Order	Integer: MASH_ORDER = 0x0 Fractional: MASH_ORDER = 0x2
Post-Divider	2: POST_DIV = 0x5 4: POST_DIV = 0x6 8: POST_DIV = 0x7 16: POST_DIV = 0x4

### 7.3.21.2 FPD-Link III Modes of Operation

The FPD-Link III transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered. The following modes are supported:

#### 7.3.21.2.1 FPD-Link III Single Link Operation

Single Link mode transmits the video over a single FPD-Link III to a single receiver. Single link mode supports frequencies up to 96 MHz for 24-bit video when paired with the DS90Ux940, DS90Ux940N, DS90Ux948, or DS90UB924. This mode is compatible with the DS90Ux926 or DS90Ux928 when operating below 85 MHz. When paired with another FPD-Link IV capable device, single link mode supports frequencies up to 162 MHz. If the downstream device is capable, the secondary FPD-Link III link can be used for high-speed control.

In Forced Single mode (set via FPD3\_MODE\_CTL1 register), the secondary TX Phy and back channel is disabled.

#### 7.3.21.2.2 FPD-Link III Dual Link Operation

In Dual Link mode, the FPD-Link III TX splits a single video stream and sends alternating pixels on two downstream links. If HDCP is enabled, a single HDCP connection is created for the video that is sent on the two links. The receiver must be capable of receiving the dual-stream video. Dual link mode is capable of supporting an pixel clock frequency of up to 324 MHz (limited by deserializer capability), with each FPD-Link III TX port running at one-half the frequency. This allows support for full 2K video. The secondary FPD-Link III link can be used for high-speed control.

Dual Link mode can be enabled using the FPD3\_MODE\_CTL register, as long as both FPD-Link Ports are configured for FPD-Link III mode in FPD4\_TX\_MODE register. In dual FPD-Link III mode, FPD3\_MODE\_CTL Register 0x59[6:5], bits DUAL\_ALIGN\_DE & DISABLE\_DUAL\_SWAP must be set to 1.

#### 7.3.21.2.3 FPD-Link III Independent Operation

In this mode, the two FPD-Link channels operate as independent single link channels. When switching from independent to dual mode or vice-versa, a soft reset is required to establish the link.

<sup>2</sup> Various methods can be used to find the fractional representation. Free tools to find a fractional representation of a decimal such as [this one](#) can simplify this process.

#### 7.3.21.2.4 FPD-Link III Replicate Mode

In this mode, the FPD-Link III TX operates as a 1:2 HDCP Repeater. A second HDCP core is implemented to support HDCP authentication and encryption to independent HDCP-capable receivers. To use replicate mode, set the FPD-Link III mode to independent and configure two video processors identically with each video processor mapped to a single FPD-Link III channel.

#### 7.3.21.2.5 Setting FPD-Link III Modes

The DS90UH981-Q1 automatically detects the capabilities of downstream links and can resolve whether a single device, dual-capable device, or multiple single link devices are connected.

Modes can be set using the FPD3\_MODE\_CTL register, as long as the FPD-Link Port is configured for FPD-Link III mode in the FPD4\_TX\_MODE register.

#### 7.3.21.3 FPD-Link Back Channel Optimizations

When switching to a FPD-Link mode different from the MODE\_SEL2 strap setting, the following scripts can be run to optimize the back channel receiver for the intended mode.

The following script contains the optimizations for serializers strapped in FPD-Link III or ADAS mode during start up and later switched to FPD-Link IV :

```
## ****
## Optimized back channel settings for FPD3 to FPD4 Mode
## ****
board.WriteI2C(DEV_ADDR,0x40,0x04) #Select Page 1 FPD Port Indirect Page
board.writeI2C(DEV_ADDR,0x41,0x05) #Setting BC Setting 0 for Port 0
board.writeI2C(DEV_ADDR,0x42,0x00)
board.writeI2C(DEV_ADDR,0x41,0x06) #Setting BC Setting 1 for Port 0
board.writeI2C(DEV_ADDR,0x42,0x00)
board.writeI2C(DEV_ADDR,0x41,0x0D) #Setting BC Setting 2 for Port 0
board.writeI2C(DEV_ADDR,0x42,0x34)
board.writeI2C(DEV_ADDR,0x41,0x0E) #Setting BC Setting 3 for Port 0
board.writeI2C(DEV_ADDR,0x42,0x53)
board.writeI2C(DEV_ADDR,0x41,0x25) #Setting BC Setting 0 for Port 1
board.writeI2C(DEV_ADDR,0x42,0x00)
board.writeI2C(DEV_ADDR,0x41,0x26) #Setting BC Setting 1 for Port 1
board.writeI2C(DEV_ADDR,0x42,0x00)
board.writeI2C(DEV_ADDR,0x41,0x2D) #Setting BC Setting 2 for Port 1
board.writeI2C(DEV_ADDR,0x42,0x34)
board.writeI2C(DEV_ADDR,0x41,0x2E) #Setting BC Setting 3 for Port 1
board.writeI2C(DEV_ADDR,0x42,0x53)
```

The following script contains the optimizations for serializers strapped in FPD-Link IV mode during start up and later switched to FPD-Link III or ADAS mode :

```
## ****
## Optimized back channel settings for FPD4 to FPD3 Mode
## ****
board.WriteI2C(DEV_ADDR,0x40,0x04) #Select Page 1 FPD Port Indirect Page
board.writeI2C(DEV_ADDR,0x41,0x05) #Setting BC Setting 0 for Port 0
board.writeI2C(DEV_ADDR,0x42,0x00)
board.writeI2C(DEV_ADDR,0x41,0x06) #Setting BC Setting 1 for Port 0
board.writeI2C(DEV_ADDR,0x42,0xFF)
board.writeI2C(DEV_ADDR,0x41,0x0D) #Setting BC Setting 2 for Port 0
board.writeI2C(DEV_ADDR,0x42,0x70)
board.writeI2C(DEV_ADDR,0x41,0x0E) #Setting BC Setting 3 for Port 0
board.writeI2C(DEV_ADDR,0x42,0x70)
board.writeI2C(DEV_ADDR,0x41,0x25) #Setting BC Setting 0 for Port 1
board.writeI2C(DEV_ADDR,0x42,0x00)
board.writeI2C(DEV_ADDR,0x41,0x26) #Setting BC Setting 1 for Port 1
board.writeI2C(DEV_ADDR,0x42,0xFF)
board.writeI2C(DEV_ADDR,0x41,0x2D) #Setting BC Setting 2 for Port 1
board.writeI2C(DEV_ADDR,0x42,0x70)
board.writeI2C(DEV_ADDR,0x41,0x2E) #Setting BC Setting 3 for Port 1
board.writeI2C(DEV_ADDR,0x42,0x70)
```

### 7.3.21.4 SPI Communication (Pass-Through Mode)

In backward compatible mode, the SPI Control Channel utilizes the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available, Forward Channel and Reverse Channel modes. In Forward Channel mode, the SPI Controller is located at the Serializer, such that the direction of sending SPI data is in the same direction as the video data. In Reverse Channel mode, the SPI Controller is located at the Deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI Control Channel can operate in a high speed mode when writing data, but must operate at lower frequencies when reading data. During SPI reads, data is clocked from the peripheral to the controller on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round trip data latency. On the other hand, for SPI writes, data can be sent at much higher frequencies as the POCI pin can be ignored by the controller.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

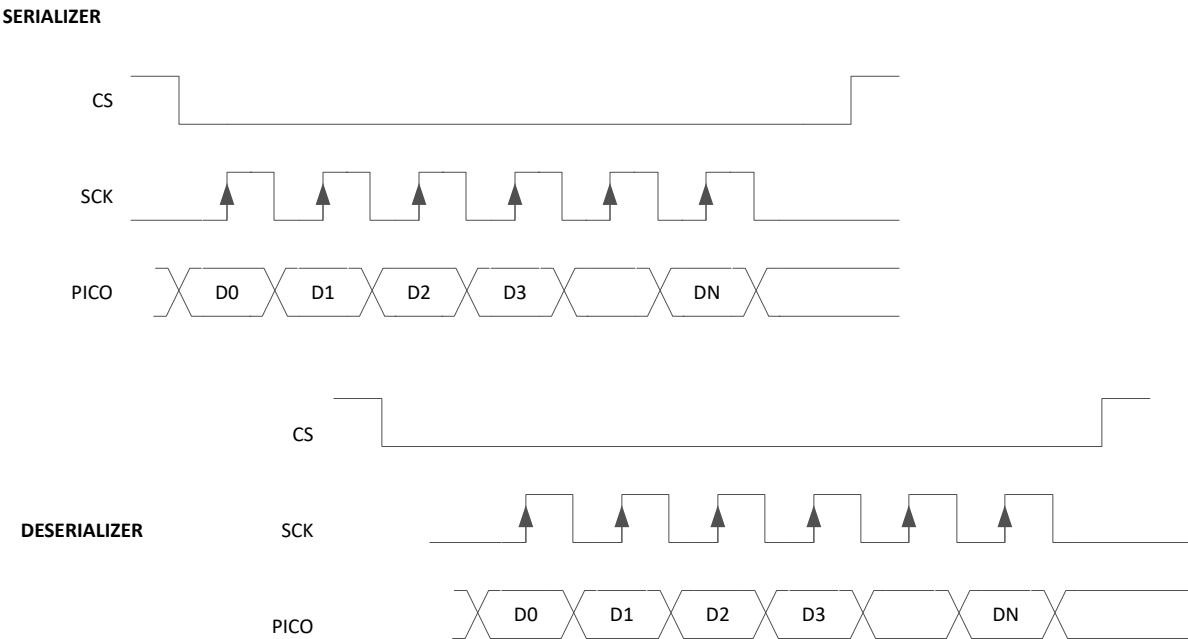
**Note:** SPI cannot be used to access Serializer / Deserializer registers.

#### 7.3.21.4.1 SPI Mode Configuration

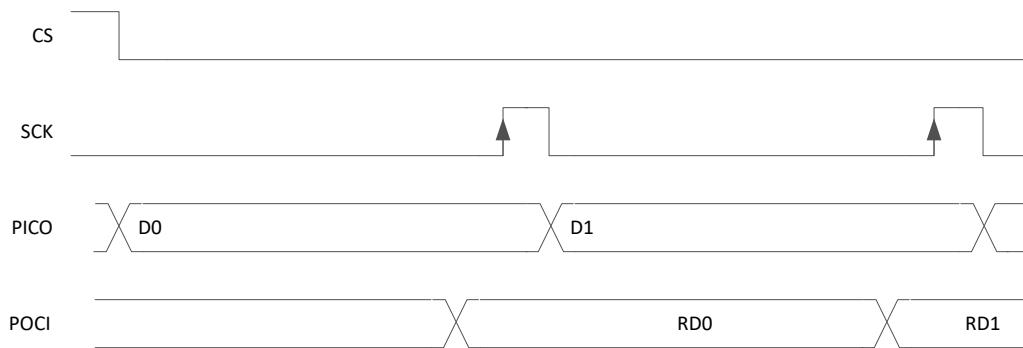
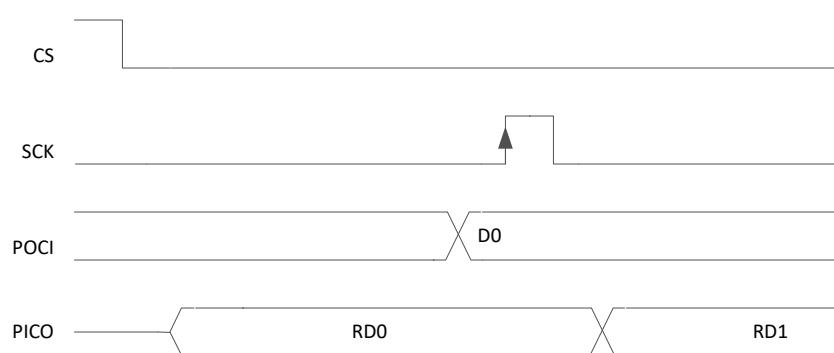
SPI is configured over I<sup>2</sup>C using the High-Speed Control Channel Configuration Mode (HSCC\_MODE) field found in register 0x10 and 0x11. The bits must be configured for either High-Speed, Forward Channel SPI mode (110) or High-Speed, Reverse Channel SPI mode (111).

#### 7.3.21.4.2 Forward Channel SPI Operation

In Forward Channel SPI operation, the SPI controller located on the Serializer generates the SPI Clock (SCK), Peripheral IN Controller OUT data (PICO), and active low Chip Select (CS). The serializer oversamples the SPI signals directly using the video pixel clock. The three sampled values for SCK, PICO, and CS are each sent on data bits in the forward channel frame. At the Deserializer, the SPI signals are regenerated using the pixel clock. In order to preserve setup and hold time, the Deserializer will hold PICO data while the SCK signal is high. In addition, it delays SCK by one pixel clock relative to the PICO data, increasing setup by one pixel clock.

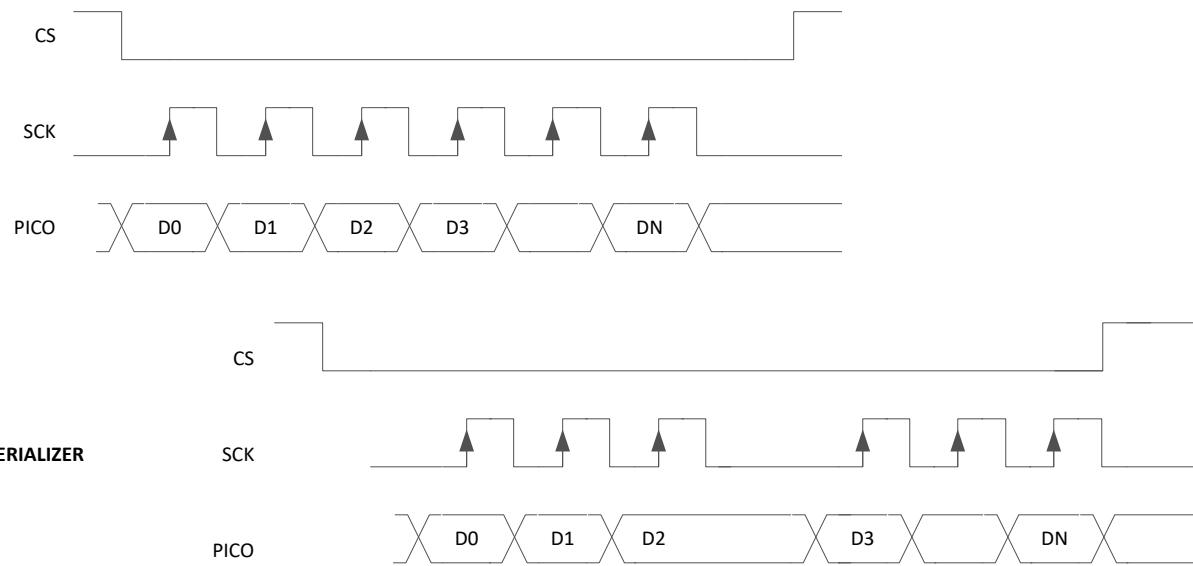


**Figure 7-22. Forward Channel SPI Write**

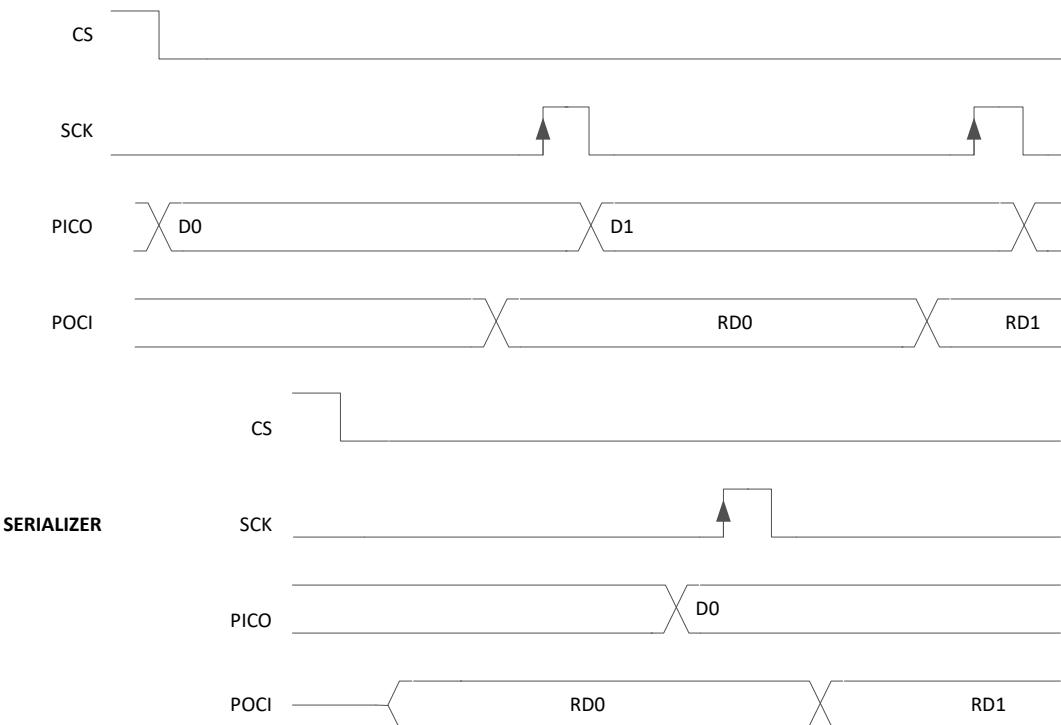
**SERIALIZER****DESERIALIZER****Figure 7-23. Forward Channel SPI Read****7.3.21.4.3 Reverse Channel SPI Operation**

In Reverse Channel SPI operation, the deserializer samples the Chip Select (CS), SPI clock (SCK) into the internal oscillator clock domain. In addition, upon detection of the active SPI clock edge, the deserializer samples the SPI data (POCI). The SPI data samples are stored in a buffer to be passed to the Serializer over the back channel. The deserializer sends SPI information in a back channel frame to the Serializer. In each back channel frame, the deserializer sends an indication of the Chip Select value. The Chip Select must be inactive (high) for at least one back-channel frame period to ensure propagation to the Serializer.

Because data is delivered in separate back channel frames and buffered, the data can be regenerated in bursts. The following figure shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the CS active indication, the second frame delivered the first three data bits, and the third frame delivers the additional data bits.

**DESERIALIZER****Figure 7-24. Reverse Channel SPI Write**

For Reverse Channel SPI reads, the SPI controller must wait for a round-trip response before generating the sampling edge of the SPI clock. This is similar to operation in Forward channel mode. Note that at most one data/clock sample will be sent per back channel frame.

**DESERIALIZER****Figure 7-25. Reverse Channel SPI Read**

For both Reverse Channel SPI writes and reads, the CS signal must be deasserted for at least one back channel frame period.

**Table 7-39. SPI CS Deassertion Requirement**

BACK CHANNEL FREQUENCY	DEASSERTION REQUIREMENT
5 Mbps	7.5 $\mu$ s
10 Mbps	3.75 $\mu$ s
20 Mbps	1.875 $\mu$ s

### 7.3.21.5 FPD-Link III I2S Audio

Refer to [Parallel I2S](#) in audio section for detail information.

### 7.3.21.6 FPD-Link III I2S Transport Modes

By default, audio is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames can be disabled from control registers if Forward Channel Frame Transport of I2S data is desired. In this mode, only I2S\_DA is transmitted to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer. If connected to a DS90UB926Q-Q1 deserializer, I2S\_DA and I2S\_DB are transmitted. Surround Sound Mode, which transmits all four I2S data inputs (I2S\_D[A..D]), can only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer.

### 7.3.21.7 FPD-Link III Pattern Generation

In backwards compatible mode the pattern generator is set in the video processor pattern generation registers like in FPD-Link IV. Depending upon the FPD-Link III mode there are some additional constraints:

1. Single Lane Mode: Only a single video processor is enabled and mapped to the appropriate FPD-Link port. Video output only on single lane.
2. Independent Mode: Two video processors are enabled and each of these video processors is mapped to a single FPD-Link port.
3. Dual Lane Mode: One video processor is enabled and mapped to FPD-Link Port 0. The video output is on both FPD-Link lanes.

#### 7.3.21.7.1 Video Processor Pattern Generation

This method of pattern generation is the same as that used with FPD-Link IV pattern generation, in which the pattern generation configuration is done via the pattern generation registers on the Video Processor Register Page (Page\_12) and the indirect access pattern generator registers.

#### 7.3.21.7.2 FPD-Link Port Pattern Generation

This is the method of pattern generation used by previous FPD-Link III devices such as DS90Ux94x devices. In this method, the indirect access pattern generator registers will be used as well as registers 0x64-0x65 on the main page. This mode can use external timing and for proper operation PATGEN\_TSEL must be programmed to 0. For detailed information on how to configure the patterns, refer to [Application Note SNLA132](#).

### 7.3.21.8 FPD-Link III Built-In Self Test (BIST)

An optional at-speed FPD-Link III Built-In Self Test (BIST) feature supports testing of the high speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

#### 7.3.21.8.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test can select the internal Oscillator clock (OSC) frequency. The user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK is valid throughout the entire duration of BIST.

See [Figure 7-26](#) for the BIST mode flow diagram.

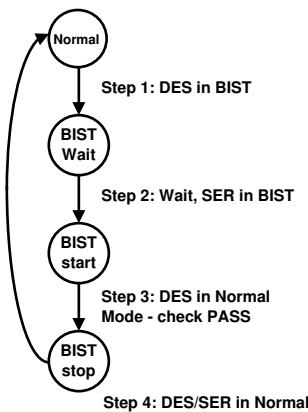
**Step 1:** The Serializer is paired with an FPD-Link III Deserializer, BIST Mode is enabled via the BISTEN pin or through register on the Deserializer. Right after BIST is enabled, part of the BIST sequence requires bit 0x02[5] be toggled locally on the Serializer (set 0x02[5]=1, then set 0x02[5]=0). The desired clock source is selected through the deserializer BISTC pin, or through register on the Deserializer.

**Step 2:** An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

**Step 3:** To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. The BIST duration is user controlled by the duration of the BISTEN signal.

**Step 4:** The link returns to normal operation after the deserializer BISTEN pin is low. [Figure 7-27](#) shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they can be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

\*\*BIST can only be disabled from the deserializer. During BIST remote access to the deserializer from the serializer is disabled.

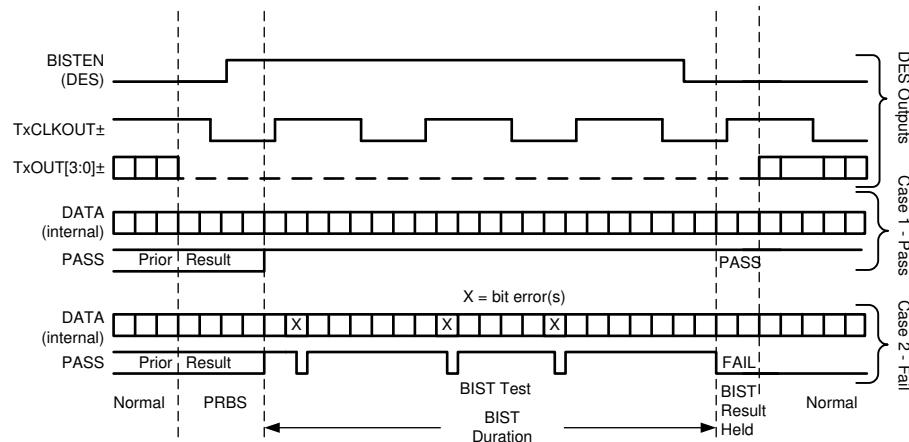


**Figure 7-26. BIST Mode Flow Diagram**

#### 7.3.21.8.2 Forward Channel and Back Channel Error Checking

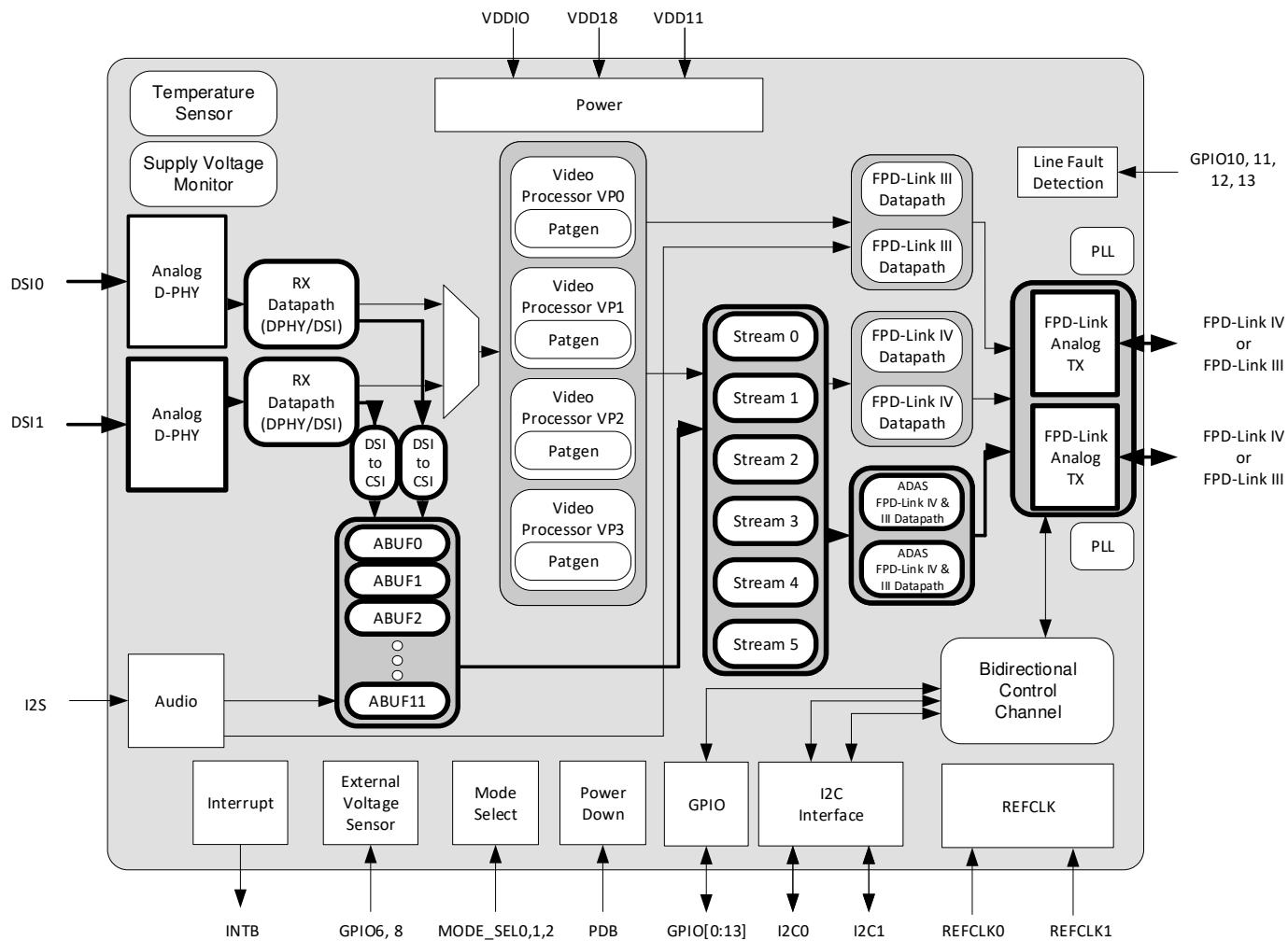
While in BIST mode, the serializer stops sampling the FPD-Link input pins and switches over to an internal all zeroes pattern. The internal all-zeroes pattern goes through scrambler, DC-balancing, etc. and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer.

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0]). CRC errors are recorded in an 8-bit register in the deserializer. The register is cleared when the serializer enters BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps a record of the last BIST run until cleared or the serializer enters BIST mode again.



**Figure 7-27. BIST Waveforms with OLDI Deserializer**

### 7.3.22 ADAS Compatibility



**Figure 7-28. ADAS Block Diagram**

The DS90UH981-Q1 is compatible with the deserializers in the 97x family, 95x family, the 960 family and DS90UB936 deserializers. To enable operation with these deserializers, the DS90UH981-Q1 converts the DSI input to CSI-2 packets before transmitting across the FPD-Link. To set the DS90UH981-Q1 in ADAS mode please refer to the [Section 7.4](#) section to configure the MODE\_SEL pins. Make sure that the DS90UH981-Q1 is configured to an FPD-Link rate supported by the partner deserializer. ADAS compatibility mode includes two operating modes: single and independent mode. When in single mode the DS90UH981-Q1 outputs FPD-Link on Port 0 and disable Port 1. The registers that control the DSI to CSI-2 conversion are on Page\_4 (DPHY Port 0) and Page\_6 (DPHY Port 1). Each DSI port supports up to four virtual channels. In ADAS mode, up to eight virtual channels total can be used across the two DSI ports. [Table 7-40](#) details the available data type conversions from DSI to CSI-2 when operating in ADAS mode.

If the DS90UH981-Q1 is set to IVI mode via the MODE\_SEL pins during start-up, Page\_9 registers ENCODER\_MODE\_PORT0 (0x84[2:0]), ENCODER\_MODE\_PORT1(0x94[2:0]) and Main Page register GENERAL\_CFG(0x7[1:0]) needs to be set to switch the device to be ADAScompatible. Optimization scripts from [FPD-Link Back Channel Optimizations](#) also need to be applied when switching inbetween IVI and ADAS modes.

**Table 7-40. DSI to CSI-2 Input Type Requirement**

DSI Input Data Type	CSI-2 Output Data Type	CSI-2 Data Type [5:0]	Description
RGB888 (0x3E)	RGB888	0x24	RGB888 image data R[7:0], G[7:0], B[7:0]
	RGB666	0x23	RGB666 image data R[7:2], G[7:2], B[7:2]
	RGB565	0x22	RGB565 image data R[7:3], G[7:2], B[7:3]
	YUV-422 (8-bit)	0x1E	YUV4:2:2 image data
	YUV-420 legacy (8-bit)	0x1A	YUV4:2:0 image data, Legacy YUV420 8-bit
RGB666 Loosely Packed (0x2E) Or RGB666 Packed (0x1E)	RGB666	0x23	RGB666 image data
	RGB565	0x22	RGB565 image data R[5:1], G[5:0], B[5:1]
	YUV-422 (8-bit)	0x1E	YUV4:2:2 image data
	YUV-420 legacy (8-bit)	0x1A	YUV4:2:0 image data, Legacy YUV420 8-bit
RGB565 (0x0E)	RGB565	0x22	RGB565 image data
	YUV-422 (8-bit)	0x1E	YUV4:2:2 image data
	YUV-420 legacy (8-bit)	0x1A	YUV4:2:0 image data, Legacy YUV420 8-bit
RGB101010 (0x0D)	RGB888	0x24	RGB888 image data R[7:0], G[7:0], B[7:0]
	RGB666	0x23	RGB666 image data R[7:2], G[7:2], B[7:2]
	RGB565	0x22	RGB565 image data R[7:3], G[7:2], B[7:3]
	YUV-422 (8-bit)	0x1E	YUV4:2:2 image data
	YUV-420 legacy (8-bit)	0x1A	YUV4:2:0 image data, Legacy YUV420 8-bit
YCbCr16(0x2C)	YUV-422 (8-bit)	0x1E	YUV4:2:2 image data
	YUV-420 legacy (8-bit)	0x1A	YUV4:2:0 image data, Legacy YUV420 8-bit

The DSI input type and CSI-2 output data type must be programmed into register CSI\_CFG0\_VC registers on Page\_4 or Page\_6. [Table 7-41](#) shows the registers that control the virtual channels on each of the DSI ports.

**Table 7-41. DSI to CSI-2 VC Registers**

Port	Indirect Register Page	Virtual Channel	Registers
Port 0	Page_4 (DPHY Port 0)	VC0	0x80 - 0x82
		VC1	0x88 - 0x8A
		VC2	0x90 - 0x92
		VC3	0x98 - 0x9A
Port 1	Page_6 (DPHY Port 1)	VC0	0x80 - 0x82
		VC1	0x88 - 0x8A
		VC2	0x90 - 0x92
		VC3	0x98 - 0x9A

The input DSI data type and output CSI-2 data type must be programmed into the registers corresponding to the correct DSI port and virtual channel. The CSI-2 line length must also be programmed for each port and virtual channel: refer to [Table 7-42](#)

**Table 7-42. DSI to CSI-2 Registers**

Register	Bit	Name	Description
CSI_CFG0_VCx (0x80, 0x88, 0x90, 0x98)	5:2	OFMT	Output data format: 0000b = RGB888 0001b = RGB666 0010b = RGB565 0011b = YUV-420 0101b = YUV-422 (8-bit)
	1:0	IFMT	Input data format: 00b = RGB 01b = YCbCr16
CSI_LINE_LEN_LSB _VCx (0x81, 0x89, 0x91, 0x99)	7:0	CSI LINE LEN LSB	CSI-2 line length's 8 least significant bits
CSI_LINE_LEN_MSB _VCx (0x82, 0x8A, 0x92, 0x9A)	7:0	CSI LINE LEN MSB	CSI-2 line length's 8 most significant bits

After the DSI to CSI-2 registers have been programmed, the link layer must be programmed to send out the correct data to the correct FPD-Link port. The FPD-Link link layer includes 12 Auxiliary Buffers that are used in ADAS mode to hold CSI-2 data before transmitting on the FPD-Link. These Auxiliary Buffers are controlled by registers in indirect register Page\_11 in the registers in [Table 7-43](#). Each virtual channel must be assigned to an Auxiliary Buffer to be sent correctly across FPD-Link.

**Table 7-43. ADAS FPD-Link Link Layer Auxiliary Buffers**

Buffer	Register Addresses
0	0x80 - 0x87
1	0x88 - 0x8F
2	0x90 - 0x97
3	0x98 - 0x9F
4	0xA0 - 0xA7
5	0xA8 - 0xAF
6	0xB0 - 0xB7
7	0xB8 - 0xBF
8	0xC0 - 0xC7
9	0xC8 - 0xCF
10	0xD0 - 0xD7
11	0xD8 - 0xDF

**Table 7-44. ADAS Link Layer Register Settings**

Register address	Bit	Name	Description
ABUFFX_CTL0 (0x80, 0x88, 0x90, 0x98, 0xA0 0xA8, 0xB0, 0xB8, 0xC0, 0xC8 0xD0, 0xD8)	1	Port Selection	FPD-Link output port 0 = FPD-Link Port 0 1 = FPD-Link Port 1
	0	Slot Enable	0 = Buffer disabled 1 = Buffer enabled

**Table 7-44. ADAS Link Layer Register Settings (continued)**

Register address	Bit	Name	Description
ABUFFX_CTL1 (0x81, 0x89, 0x91, 0x99, 0xA1 0xA9, 0xB1, 0xB9, 0xC1, 0xC9 0xD1, 0xD9)	3:0	Data Type input	0x07 = CSI-2 data
ABUFFX_CTL2 (0x82, 0x8A, 0x92, 0x9A, 0xA2 0xAA, 0xB2, 0xBA, 0xC2, 0xCA 0xD2, 0xDA)	4:0	Source for Buffer	Please refer to the <a href="#">Table 7-45</a> to select the correct DSI port and virtual channel for the source of the slot.

**Table 7-45. ADAS Link Layer Source Select**

SRC_TO_ABUFF_SEL	DSI Port	Virtual Channel
20 (0x14)	0	0
21 (0x15)	0	1
22 (0x16)	0	2
23 (0x17)	0	3
24 (0x18)	1	0
25 (0x19)	1	1
26 (0x1A)	1	2
27 (0x1B)	1	3

To make sure that the DSI input data does not exceed the buffer size, the DSI clock input must be limited to below the output FPD-Link bandwidth. To calculate the max DSI clock use the following equations:

$$\frac{FPD - \text{Link\_data\_rate} \times \text{encoding}}{2 \times (\# \text{ of DSI lanes})} \geq \text{DSI Clock Freq} \quad (31)$$

Here is an example of using the equations to find the max DSI clock frequency for a system that is using 4.2 Gbps data rate with 4 DSI input lanes:

$$\frac{4.2\text{Gbps} \times \left(\frac{32\text{b}}{40\text{b}}\right)}{2 \times (\# \text{ of DSI lanes})} \geq \text{DSI Clock Freq} \quad (32)$$

### 7.3.22.1 ADAS Pattern Generator

Since the ADAS mode does not use the video processor, the ADAS pattern generator is different than the video processor pattern generator. For the ADAS pattern generator two types of patterns are supported: Reference color bar patterns and fixed color patterns accessed by the ADAS pattern generator in the indirect register page 8.

### 7.3.22.2 ADAS Reference Color Bar Pattern

The reference color bar patterns are based on the pattern defined in Appendix D of the mipi\_CTS\_for\_DPHY\_v1-1\_r03 specification. The pattern is an 8-color bar pattern designed to provide high, low, and medium frequency outputs on the CSI-2 transmit data lanes.

The CSI-2 reference pattern provides 8 color bars by default with the following byte data for the color bars: X bytes of 0xAA (high-frequency pattern, inverted), X bytes of 0x33 (mid-frequency pattern), X bytes of 0xF0 (low-frequency pattern, inverted), X bytes of 0x7F (lone 0 pattern), X bytes of 0x55 (high-frequency pattern), X bytes of 0xCC (mid-frequency pattern, inverted), X bytes of 0x0F (low-frequency pattern), and Y bytes of 0x80 (long 1 pattern). In most cases, Y is the same as X. For certain data types, the last color bar needs to be larger than the others to properly fill the video line dimensions.

The pattern generator is programmable with the following options:

- Number of color bars (1, 2, 4, or 8)
- Number of bytes per line
- Number of bytes per color bar
- CSI-2 datatype field and VC-ID
- Number of active video lines per frame
- Number of total lines per frame (active plus blanking)
- Line period (possibly program in units of 10 ns)
- Vertical front porch – number of blank lines prior to the FrameEnd packet
- Vertical back porch – number of blank lines following the FrameStart packet

The pattern generator relies on proper programming by software to make sure the color bar widths are set to multiples of the block (or word) size required for the specified datatype. For example, for RGB888, the block size is 3 bytes which also matches the pixel size. In this case, the number of bytes per color bar must be a multiple of 3.

### 7.3.22.3 ADAS Fixed Color Patterns

When programmed for fixed color pattern mode, the pattern generator can generate a video image with a programmable fixed data pattern. The basic programming fields for image dimensions are the same as used with the color bar patterns. When sending fixed color patterns, the color bar controls allow the user to alternate between the fixed pattern data and the bit-wise inverse of the fixed pattern data.

The fixed color patterns assume a fixed block size for the byte pattern. The block size is programmable through a register and is designed to support most 8-bit, 10-bit, and 12-bit pixel formats. The block size must be set based on the pixel size converted to blocks that are an integer multiple of bytes. For example, an RGB888 pattern can consist of 3-byte pixels and can therefore require a 3-byte block size. A 2x12-bit pixel image can also require 3-byte block size, while a 3x12-bit pixel image can require 9 bytes (2 pixels) to send an integer number of bytes.

The fixed color patterns support block sizes up to 16 bytes in length, allowing additional options for patterns in some conditions. For example, an RGB888 image can alternate between four different pixels by using a twelve-byte block size. An alternating black and white RGB888 image can be sent with a block size of 6-bytes by setting the first three bytes to 0xFF and the next three bytes to 0x00.

To support up to 16-byte block sizes, a set of sixteen registers are implemented to allow programming the value for each data byte.

### 7.3.22.4 ADAS Packet Generator Programming

The information in this section provides details on how to program the pattern generator to provide a specific color bar pattern, based on datatype, frame size, and line size.

Most basic configuration information is determined directly from the expected video frame parameters. The requirements include the datatype, frame rate (frames per second), number of active lines per frame, number of total lines per frame (active plus blanking), and number of pixels per line.

- PGEN\_ACT\_LPF – Number of active lines per frame
- PGEN\_TOT\_LPF – Number of total lines per frame
- CSI-2 Data Type field and VC-ID.
- Optional: PGEN\_VBP – Vertical back porch. This is the number of lines of vertical blanking following Frame Valid.
- Optional: PGEN\_VFP – Vertical front porch. This is the number of lines of vertical blanking preceding Frame Valid.
- PGEN\_LINE\_PD – Line period in 10-ns units. Compute based on Frame Rate and total lines per frame.
- PGEN\_BAR\_SIZE – Color bar size in bytes. Compute based on datatype and line length in bytes (see details below).

### 7.3.22.5 ADAS Determining Color Bar Size

The color bar pattern must be programmed in units of a block or word size dependent on the datatype of the video being sent. The sizes are defined in the MIPI CSI-2 specification. For example, RGB888 requires a 3-byte block size which is the same as the pixel size.

When programming the Pattern Generator, software must compute the required bar size in bytes based on the line size and the number of bars. For the standard 8-color bar pattern, that requires the following algorithm:

- Select the desired datatype, and a valid length for that datatype (in pixels).
- Convert pixels/line to blocks/line (by dividing by the number of pixels/block, as defined in the datatype specification).
- Divide the blocks/line result by the number of color bars (8), giving blocks/bar.
- Round result down to the nearest integer.
- Convert blocks/bar to bytes/bar and program that value into the PGEN\_BAR\_SIZE register.

As an alternative, the blocks/line can be computed by converting pixels/line to bytes/line and dividing by bytes/block.

## 7.4 Device Functional Modes

### 7.4.1 Mode Select Configuration Settings (MODE\_SEL[2:0])

Configuration of the device can be done via the MODE\_SEL[2:0] input pins, or via the configuration register bits. A pull-up resistor and a pull-down resistor of suggested values can be used to set the voltage ratio of the MODE\_SEL[2:0] inputs. The 3-bit MODE\_SEL strapped values can be read from TX\_MODE\_STS register at address 0x27. MODE\_SEL2 configures the device to be in ADAS or IVI mode. If MODE\_SEL2 = 0 the device is in IVI mode. See [Table 7-47](#) and [Table 7-48](#). If MODE\_SEL2 = 1 the device is in ADAS mode. See [Table 7-49](#) and [Table 7-50](#).

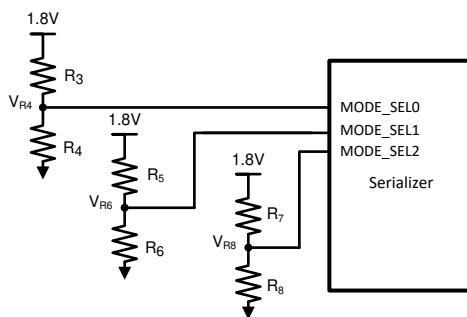


Figure 7-29. MODE\_SEL[2:0] Connection Diagram

Table 7-46. Configuration Select (MODE\_SEL2)

#	RATIO MIN	RATIO TYPICAL	RATIO MAX	SUGGESTED RESISTOR PULL-UP R7 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R8 kΩ (1% tol)	IVI or ADAS
0	0	0	0.35	OPEN	40.2	IVI
1	0.65	1	1	0	OPEN	ADAS

Table 7-47. IVI (MODE\_SEL2=0) Configuration Select (MODE\_SEL0)

#	RATIO MIN	RATIO TYPICAL	RATIO MAX	VR4 (V); VDD = 1.8	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	FPD-Link Rate (Gbps)	FPD-Link III or FPD-Link IV	DUAL/ INDEPENDENT
1	0	0	0.115	0	OPEN	40.2	10.8	FPD-Link IV	Dual
2	0.172	0.211	0.244	0.380	95.3	25.5	10.8	FPD-Link IV	Independent
3	Reserved								

**Table 7-47. IVI (MODE\_SEL2=0) Configuration Select (MODE\_SEL0) (continued)**

#	RATIO MIN	RATIO TYPICAL	RATIO MAX	VR4 (V); VDD = 1.8	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	FPD-Link Rate (Gbps)	FPD-Link III or FPD-Link IV	DUAL/INDEPENDENT
4	Reserved								
5	0.528	0.556	0.575	1.001	15.0	18.7	6.75	FPD-Link IV	Dual
6	0.640	0.673	0.684	1.211	14.3	29.4	6.75	FPD-Link IV	Independent
7	0.761	0.79	0.813	1.422	21.5	80.6	3.375	FPD-Link IV	Independent
8	0.874	0.926	1	1.667	10.0	97.6	2.975	FPD-Link III	Independent

**Table 7-48. IVI (MODE\_SEL2=0) Configuration Select (MODE\_SEL1)**

#	RATIO MIN	RATIO TYPICAL	RATIO MAX	VR6 (V); VDD = 1.8	SUGGESTED RESISTOR PULL-UP R5 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R6 kΩ (1% tol)	DSI LANES	DSI_CAL_EN	DISABLE DSI
1	0	0	0.115	0	OPEN	40.2	2	0	0
2	0.172	0.211	0.244	0.380	95.3	25.5	2	0	1
3	0.291	0.325	0.362	0.585	22.1	10.7	4	0	0
4	0.408	0.441	0.464	0.794	28.0	22.1	4	0	1
5	0.528	0.556	0.575	1.001	15.0	18.7	2	1	0
6	0.640	0.673	0.684	1.211	14.3	29.4	2	1	1
7	0.761	0.79	0.813	1.422	21.5	80.6	4	1	0
8	0.874	0.926	1	1.667	10.0	97.6	4	1	1

**Table 7-49. ADAS (MODE\_SEL2=1) Configuration Select (MODE\_SEL0)**

#	RATIO MIN	RATIO TYPICAL	RATIO MAX	VR4 (V); VDD = 1.8	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	FPD-Link Rate	FPD-Link TX Mode
1	0	0	0.115	0	OPEN	40.2	4.16 Gbps	Independent
2	Reserved							
3	Reserved							
4	0.408	0.441	0.464	0.794	28.0	22.1	8.4 Gbps	Independent
5	Reserved							
6	0.643	0.673	0.684	1.211	14.3	29.4	8.4 Gbps	Single
7	Reserved							
8	Reserved							

**Table 7-50. ADAS (MODE\_SEL2=1) Configuration Select (MODE\_SEL1)**

#	RATIO MIN	RATIO TYPICAL	RATIO MAX	VR6 (V); VDD = 1.8	SUGGESTED RESISTOR PULL-UP R5 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R6 kΩ (1% tol)	DSI_CAL_EN
0	0.408	0.441	0.464	0.794	28.0	22.1	0
1	0.874	0.926	1.000	1.667	10.0	97.6	1

- MODE\_SEL1 is used to configure the DSI interface.
- Only 2 or 4 lanes can be selected from strapping. 1 or 3 lanes can be set in the register 0x4F
- DSI\_CAL\_EN = 1 enables DSI skew calibration. DSI\_CAL\_EN = 0 does not run DSI skew calibration
- DISABLE DSI = 1 disables DSI RX and DSI DISABLE = 0 enables DSI RX.

## 7.4.2 FPD-Link IV Modes of Operation

The FPD-Link IV transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered. The FPD-Link Port mode is set via the FPD4\_TX\_MODE register. After the FPD-Link mode is set the device must be reset using the DIGITAL\_RESET\_NOREGS (0x02[0]) register. The following modes are supported:

- Single Link Operation
- Dual Link Operation
- Independent Link Operation

### 7.4.2.1 Single Link Operation

Single Link mode transmits the video over a single FPD-Link port to a single receiver. To configure for Single Link mode, set FPD4\_TX\_MODE( 0x5[5:2] ) equal to 0xB or 0xE for FPD-Link port 0 and FPD-Link Port 1 respectively. Additionally set the field to operate in independent mode and set LINK\_LAYER\_CTL[3] =0 to disable link layer 1.

### 7.4.2.2 Dual Link Operation

In Dual Link mode, the FPD-Link IV TX splits a single video stream and sends alternating pixels on two downstream links. The receiver must be capable of receiving the dual-stream video. Dual link mode is supports a total line rate of 21.6 Gbps, with each FPD-Link IV TX port running at one-half the rate, 10.8 Gbps.

### 7.4.2.3 Independent Link Operation

In this mode, the two FPD-Link channels operate as independent single link channels.

## 7.5 Programming

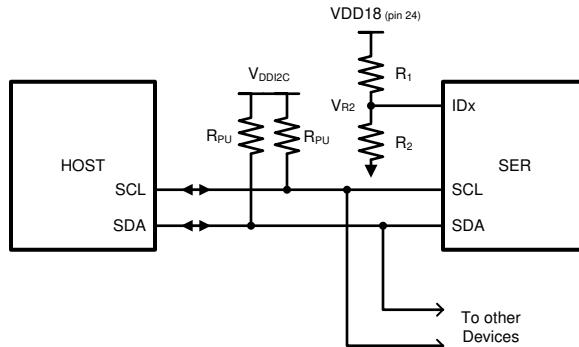
### 7.5.1 I<sup>2</sup>C Serial Control Bus

#### 7.5.1.1 I<sup>2</sup>C Device Address

The DS90UH981-Q1 implements two I<sup>2</sup>C-compatible serial control buses. The I<sup>2</sup>C is for local device configuration and incorporates a Bidirectional Control Channel (BCC) that allows communication across the FPD-Link cable with remote deserializers as well as remote I<sup>2</sup>C target devices. The DS90UH981-Q1 implements two I<sup>2</sup>C compatible targets and two I<sup>2</sup>C controller (sends I<sup>2</sup>C commands on all two I<sup>2</sup>C ports) capable of operation with Standard, Fast, Fast-plus and High Speed. This allows for remote I<sup>2</sup>C operation up to 1 MHz and local I<sup>2</sup>C operation up to 3.4 MHz. The 3.4 MHz communication is not supported when all three I<sup>2</sup>C ports operate I<sup>2</sup>C transaction simultaneously. In high-speed mode accessing to the local registers can only support up to two ports.

For accesses to local registers, the I<sup>2</sup>C targets operate without stretching the clock. Accesses to remote devices over the Bidirectional Control Channel results in clock stretching to allow for response time across the link. The DS90UH981-Q1 can also act as I<sup>2</sup>C Controller for regenerating Bidirectional Control Channel accesses originating from the remote devices across FPD-Link.

The primary device address is set via a resistor divider (R1 and R2 — see [Figure 7-30](#) below) connected to the ID<sub>x</sub> pin. Each of the two I<sup>2</sup>C ports has a dedicated target address. By default, the target address of I<sup>2</sup>C target 0 is set to the primary I<sup>2</sup>C address corresponding to the ID<sub>x</sub> pin. I<sup>2</sup>C target 0 is the primary I<sup>2</sup>C address (7-bit form), and I<sup>2</sup>C target 1 is the primary I<sup>2</sup>C address (7-bit form) plus two. For instance, if the primary I<sup>2</sup>C address is set to 0x18, I<sup>2</sup>C target 0 has a target address of 0x18, and I<sup>2</sup>C target 1 has a target address of 0x1A. These addresses can be overwritten using the DEV\_ID register, which has two copies, one for each I<sup>2</sup>C target.

**Figure 7-30. I<sup>2</sup>C Connection**

The IDx pin configures the control interface to one of four possible device addresses. A pull-up resistor and a pull-down resistor can be used to set the appropriate voltage on the IDx input pin. See below.

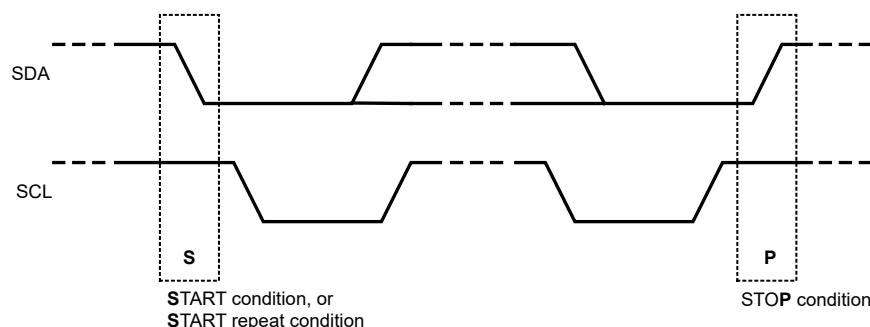
**Table 7-51. Serial Control Bus Addresses For IDX**

MODE #	RATIO TYPICAL	VR2 (V); VDD = 1.8	I <sup>2</sup> C Voltage Level	SUGGESTED RESISTOR PULL-UP R1 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R2 kΩ (1% tol)	7-BIT ADDRESS I <sup>2</sup> C Target 0	8-BIT ADDRESS I <sup>2</sup> C Target 0	8-BIT ADDRESS I <sup>2</sup> C Target 1	8-BIT ADDRESS I <sup>2</sup> C Target 2
1	0	0	1.8	OPEN	10.0	0x0C	0x18	0x1A	0x1C
2	0.213	0.384	1.8	42.2	11.5	0x10	0x20	0x22	0x24
3	0.327	0.589	1.8	29.4	14.3	0x14	0x28	0x2A	0x2C
4	0.441	0.793	1.8	28.7	22.6	0x18	0x30	0x32	0x34
5	0.551	0.999	3.3	15	18.7	0x0C	0x18	0x1A	0x1C
6	0.671	1.208	3.3	13.7	28	0x10	0x20	0x22	0x24
7	0.787	1.417	3.3	16.2	60.4	0x14	0x28	0x2A	0x2C
8	1	1.8	3.3	10.0	OPEN	0x18	0x30	0x32	0x34

### 7.5.1.2 I<sup>2</sup>C Bus Operation

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V<sub>DD18</sub> or V<sub>DD33</sub> (only I<sup>2</sup>C Bus 0 can handle 3.3V). The pull-up resistor value can be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low. Refer to "I<sup>2</sup>C Bus Pullup Resistor Calculation, SLVA689" to determine the pull-up resistor value for the SCL and SDA rise time.

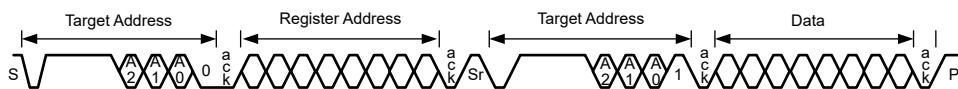
The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions Low while SCL is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 7-31

**Figure 7-31. Start And Stop Conditions**

To communicate with an I<sup>2</sup>C target, the host controller sends the target address and listens for a response from the target. This response is referred to as an acknowledge bit (ACK). If a target on the bus is addressed correctly, the controller Acknowledges (ACKs) by driving the SDA bus low. If the address doesn't match a device's target address, the controller Not-acknowledges (NACKs) by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the controller is writing data, the target ACKs after every data byte is successfully received. When the controller is reading data, the controller ACKs after every data byte is received to let the target know the controller wants to receive another data byte. When the controller wants to stop reading, the controller NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition.



**Figure 7-32. Serial Control Bus — Write**



**Figure 7-33. Serial Control Bus — Read**

The I<sup>2</sup>C controller located at the serializer must support I<sup>2</sup>C clock stretching. For more information on I<sup>2</sup>C interface requirements and throughput considerations, please refer to TI Application Note [SNLA131](#).

The serializer includes several different mechanisms to prevent I<sup>2</sup>C bus hangs:

- I<sup>2</sup>C Bus Arbitrator
- I<sup>2</sup>C Bus Timeout
- BCC Watchdog Timer

The I<sup>2</sup>C bus arbitrator function is designed to prevent one I<sup>2</sup>C target device of the SER holding the other I<sup>2</sup>C targets from accessing the BCC. An example of this timeout is when an I<sup>2</sup>C target's CLK is held by the controller during a transfer between Device address and Offset address phase or between Offset address phase and a repeated start phase for a long period of time. The timer starts after the SER I<sup>2</sup>C target receives a START command, and expires after the timeout period set by ARB\_TIMEOUT (register 0x3[6:5]) if the SER I<sup>2</sup>C target does not receive a STOP command. When the ARB\_TIMEOUT occurs, a STOP signal is internally generated by the SER and sent to the DES through the BCC. The arbiter to access BCC is now free to be used by the other I<sup>2</sup>C targets of the SER. The STOP signal is passed on the remote DES I<sup>2</sup>C bus. The I<sup>2</sup>C bus arbitrator can be disabled by setting ARB\_TIMEOUT\_DISABLE = 1 in register 0x3[7]. The I<sup>2</sup>C bus arbitrator can be safely disabled without consequence if the system implementation does not utilize more than one I<sup>2</sup>C bus on the SER device or if the system has provisions put in place to make sure that I<sup>2</sup>C transactions from multiple controllers on the SER side do not attempt to simultaneously communicate using multiple I<sup>2</sup>C target devices of the SER.

The I<sup>2</sup>C bus timeout function is designed to make sure that the local I<sup>2</sup>C bus is free in the case where the SER is configured to act as a proxy I<sup>2</sup>C controller on the bus (if an I<sup>2</sup>C controller on the remote DES side initiates a command to access a device attached to the local SER I<sup>2</sup>C bus through the BCC). The I<sup>2</sup>C bus timer starts when the SER proxy I<sup>2</sup>C controller has started a command, and expires after either 1 second or 50us (based on the setting of I2C\_BUS\_TIMER\_SPEEDUP in register 0x3[1]) if no toggling of SDA is detected while SCL is HIGH. When the timeout occurs, the SER internally generates a NACK signal and sends to the remote DES through the BCC to free the DES I<sup>2</sup>C bus. The I<sup>2</sup>C bus timeout feature can be disabled by setting I2C\_BUS\_TIMER\_DISABLE = 1 in register 0x3[0]. The I<sup>2</sup>C bus timer must not be disabled if the system implementation is configured to use the proxy I<sup>2</sup>C controller functionality of the SER (when a remote controller device attached to the DES I<sup>2</sup>C bus needs to access a target I<sup>2</sup>C device on the SER I<sup>2</sup>C bus through the BCC). The I2C\_BUS\_TIMER\_SPEEDUP function can be used to reduce the timeout period of the I<sup>2</sup>C controller on the

DES side if that controller needs to access a remote target on the SER side more quickly after initial power up of the FPD-Link.

The BCC watchdog timer is designed to prevent the local SER I<sup>2</sup>C bus from stretching the I<sup>2</sup>C CLK beyond an acceptable time period. This timeout can potentially happen when trying to access a remote DES or remote I<sup>2</sup>C target attached to the remote DES. The timer starts after the SER receives a START command from the local I<sup>2</sup>C target. The timer expires after the timeout period set by BCC\_WATCHDOG\_TIMER (register 0x29[7:1]) if the SER does not receive a response from the remote deserializer through the BCC. When the timeout happens, a NACK is sent to the local I<sup>2</sup>C controller attached to the SER. The BCC watchdog timeout can be disabled by setting BCC\_WDOG\_DIS = 1 in register 0x29[0], however disabling the BCC watchdog timer under any typical system configuration is not recommended, as the lack of a timeout can lock the I<sup>2</sup>C bus if any transaction is issued over the BCC when the FPD-Link is not yet LOCKed, or if there is an error in the BCC I<sup>2</sup>C transaction.

### 7.5.2 Bidirectional Control

The Bidirectional Control Channel (BCC) is compatible with I<sup>2</sup>C devices, allowing local I<sup>2</sup>C target access to device registers as well as bidirectional I<sup>2</sup>C operation across the link to the deserializer and attached devices. I<sup>2</sup>C access must not be attempted across the link when TX Port Lock status is Low.

### 7.5.3 I<sup>2</sup>C Target Operation

The DS90UH981-Q1 implements two I<sup>2</sup>C-compatible targets capable of operation compliant to the Standard, Fast, and Fast-plus modes of operation allowing I<sup>2</sup>C operation at up to 1 MHz clock frequencies (up to 3.4 MHz for local bus access). Local I<sup>2</sup>C transactions to access DS90UH981-Q1 registers can be conducted 2 ms after power supplies are stable and PDB is brought high. For accesses to local registers, the I<sup>2</sup>C target operates without stretching the clock (except when multiple I<sup>2</sup>C targets are being used to access the DS90UH981-Q1 registers simultaneously). Make sure that control registers for indirect access registers (e.g. 0x40-0x42) are not being accessed simultaneously by multiple I<sup>2</sup>C controllers. In cases where multiple I<sup>2</sup>C controllers attempt to access the same DS90UH981-Q1 register at the same time, priority is given to I<sup>2</sup>C Port 0, followed by Port 1, and lastly I<sup>2</sup>C commands sent over the back channel.

A spurious one-byte I<sup>2</sup>C read or write transaction with a random address can be observed on the local bus when a downstream deserializer is reset, powered-on/off, hot-plugged, or connected/disconnected. On the serializer or deserializer, remote downstream I<sup>2</sup>C transactions can be disabled to prohibit the potential I<sup>2</sup>C transactions from being acknowledged. On the serializer, set main page register I<sup>2</sup>C\_CTRL\_CHAIN\_CTL2 (0x3A) to 0x88 to disable I<sup>2</sup>C transactions from a remote controller. In Daisy-Chain configuration on the Deserializer, set main page register TX\_I<sup>2</sup>C\_CONTROLLER\_DISABLE (0x08[5]) to 0x1 to disable I<sup>2</sup>C transactions originating from a downstream controller.

### 7.5.4 Remote Target Operation

The Bidirectional Control Channel provides a mechanism to read or write I<sup>2</sup>C registers in remote devices over the FPD-Link interface. The I<sup>2</sup>C Controller located at the deserializer must support I<sup>2</sup>C clock stretching. Accesses to serializers or remote target devices over the Bidirectional Control Channel results in clock stretching to allow for response time across the link. The DS90UH981-Q1 acts as an I<sup>2</sup>C target on the local bus, forwards read and write requests to the remote device, and returns the response from the remote device to the local I<sup>2</sup>C bus. To allow for the propagation and regeneration of the I<sup>2</sup>C transaction at the remote device, the DS90UH981-Q1 stretches the I<sup>2</sup>C clock while waiting for the remote response.

To communicate with a remote target device, a routing mechanism is used to send BCC commands from a source to destination based on system topology. The serializer or deserializer that is connected to the host controller must control the BCC routing. If the DS90UH981-Q1 is not connected to the host controller, consult the appropriate serializer or deserializer data sheet for details on how to configure bidirectional channel communication routing. To enable remote target operation, register 0x07 [3] must be set to enable I<sup>2</sup>C pass through mode for each I<sup>2</sup>C Bus. For example, to configure I<sup>2</sup>C Port 0 to communicate with remote devices, I<sup>2</sup>C Port 0, register 0x07[3] must be set by an I<sup>2</sup>C controller attached to Port 0 and to configure I<sup>2</sup>C Port 1 to communicate with remote devices, I<sup>2</sup>C Port 1, register 0x07[3] must be set by an I<sup>2</sup>C controller attached to Port 1. If the DS90UH981-Q1 is connected to host controller, registers TARGET\_ID\_x(0x70 -

0x77), TARGET\_ALIAS\_x(0x78 - 0x7F), and TARGET\_DEST\_x(0x88 - 0x8F) are grouped together to control the direction, routing port, source and destination of bidirectional communication. Each I<sup>2</sup>C port has a copy of TARGET\_ID\_x(0x70 - 0x77), TARGET\_ALIAS\_x(0x78 - 0x7F), and TARGET\_DEST\_x(0x88 - 0x8F) registers. A description of these registers are listed in [Table 7-52](#).

**Table 7-52. Bidirectional Channel Communication Over Daisy-Chain Registers**

Register Name	Bits	Bits Name	Description
TARGET_ID_x	7:1	TARGET_IDx	7-bit Remote target Device ID x Configures the physical I <sup>2</sup> C address of the remote I <sup>2</sup> C target device attached to the remote deserializer. If an I <sup>2</sup> C transaction is addressed to the target Alias ID x, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the deserializer.
	0	RESERVED	Reserved
TARGET_ALIAS_x	7:1	TARGET_ALIAS_IDx	7-bit Remote target Device Alias ID x Configures the decoder for detecting transactions designated for an I <sup>2</sup> C target device attached to the remote deserializer. The transaction is remapped to the address specified in the target ID x register. A value of 0 in this field disables access to the remote I <sup>2</sup> C target.
	0	LCL_PORTSEL_IDX	In a remote I <sup>2</sup> C transaction, this bit directs the transaction to either take Port 0 or Port 1 of the local FPD-Link to hop to the next device.
TARGET_DEST_x	7:5	DEST_ADDR	Destination port selection See <a href="#">Table 7-53</a>
	4	FIRST_DC_PSEL	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
	3	MID_DC_PSEL	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
	2	FINAL_DC_PSEL	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
	1:0	REMAINING_DEPTH	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth

TARGET\_ID\_x controls the BCC message routing directions. When this bit is set to 0, BCC messages are routed to downstream devices. Set to one has no effect.

TARGET\_ALIAS\_x controls the BCC message routing ports. When this bit is set to 1, BCC messages are routed through either RX port 1 or daisy-chain TX port 1 depending on TARGET\_ID\_x[0] settings. When this bit is set to 0, BCC messages are routed through either RX port 0 or daisy-chain TX port 0 depending on TARGET\_ID\_x[0] settings.

TARGET\_DEST\_x controls the destination port selections (bit 2:0), depth 1 port selection (bit 3), depth 2 port selection (bit 4), depth 3 port selection (bit 5), and remaining depth (bit 7:6). Available destination port selections are listed in [Table 7-53](#).

**Table 7-53. Destination Port Selections**

TARGET_DEST_x[7:5]	DS90UH981-Q1 Serializer	DS90Ux98x Deserializer <sup>(1)</sup>
000	I <sup>2</sup> C Port 0	I <sup>2</sup> C Port 0
001	I <sup>2</sup> C Port 1	I <sup>2</sup> C Port 1

**DS90UH981-Q1**

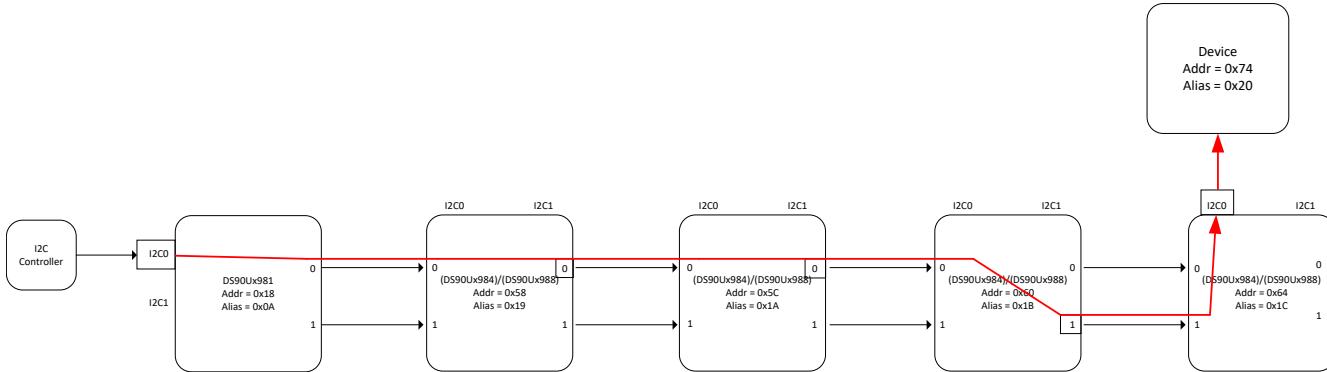
SNLS644B – APRIL 2021 – REVISED OCTOBER 2023

**Table 7-53. Destination Port Selections (continued)**

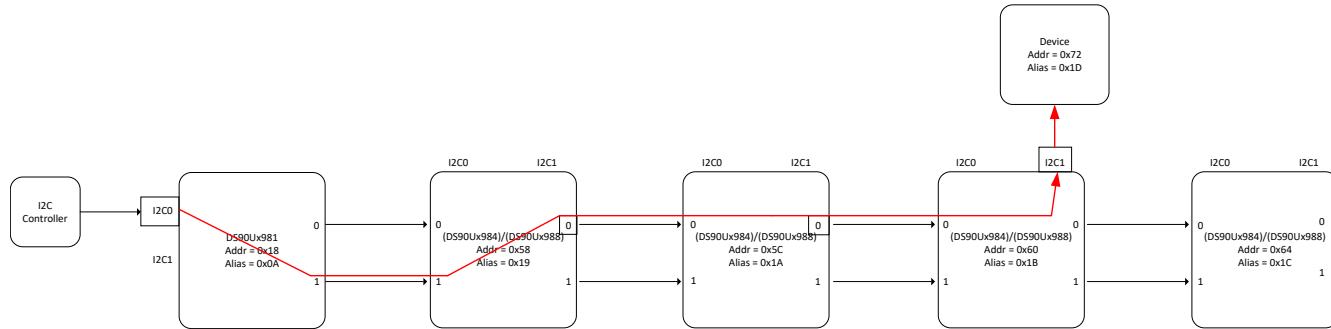
TARGET_DEST_x[7:5]	DS90UH981-Q1 Serializer	DS90Ux98x Deserializer <sup>(1)</sup>
010	Reserved	Reserved
011-111	Reserved	Reserved

(1) Refer to corresponding DS90Ux98x data sheet.

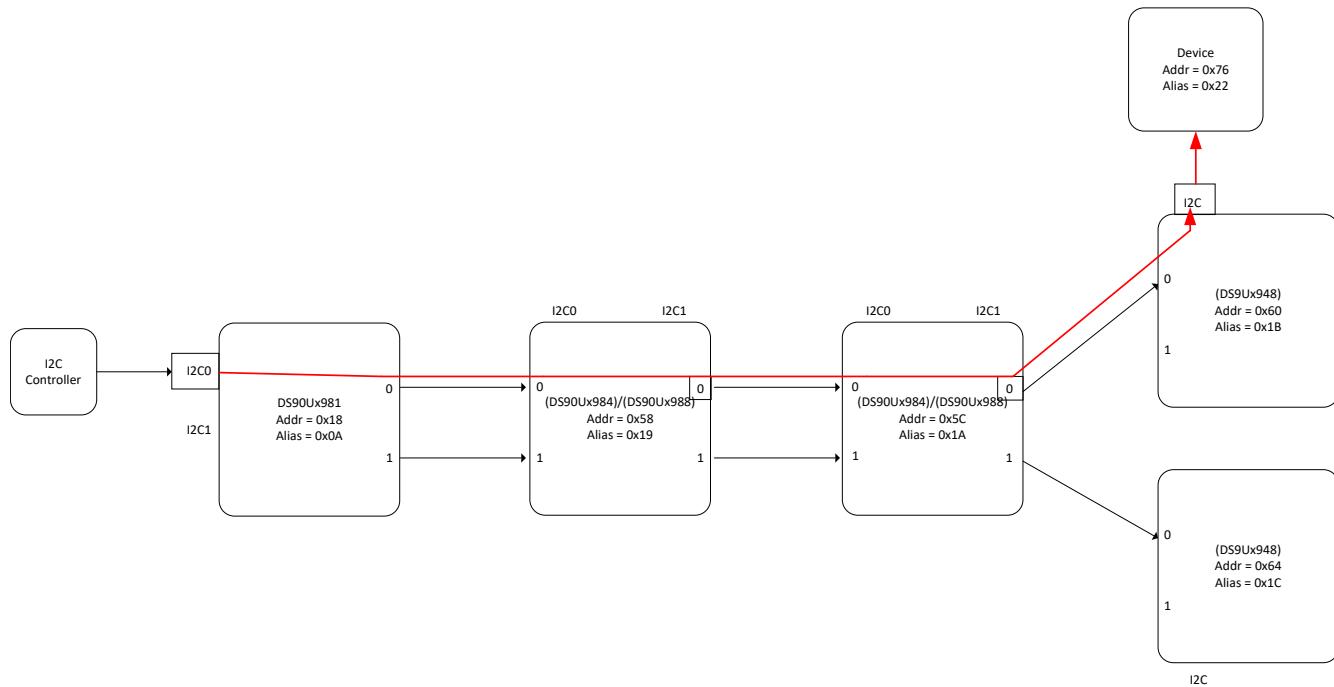
Daisy-chain operation supports a maximum of three daisy-chain devices. Depths 1, 2, and 3 port selection bit controls the forwarding port selection of the corresponding daisy-chain device.

**Figure 7-34. Daisy-Chain Communication Example #1****Table 7-54. Daisy-Chain Communication Example #1**

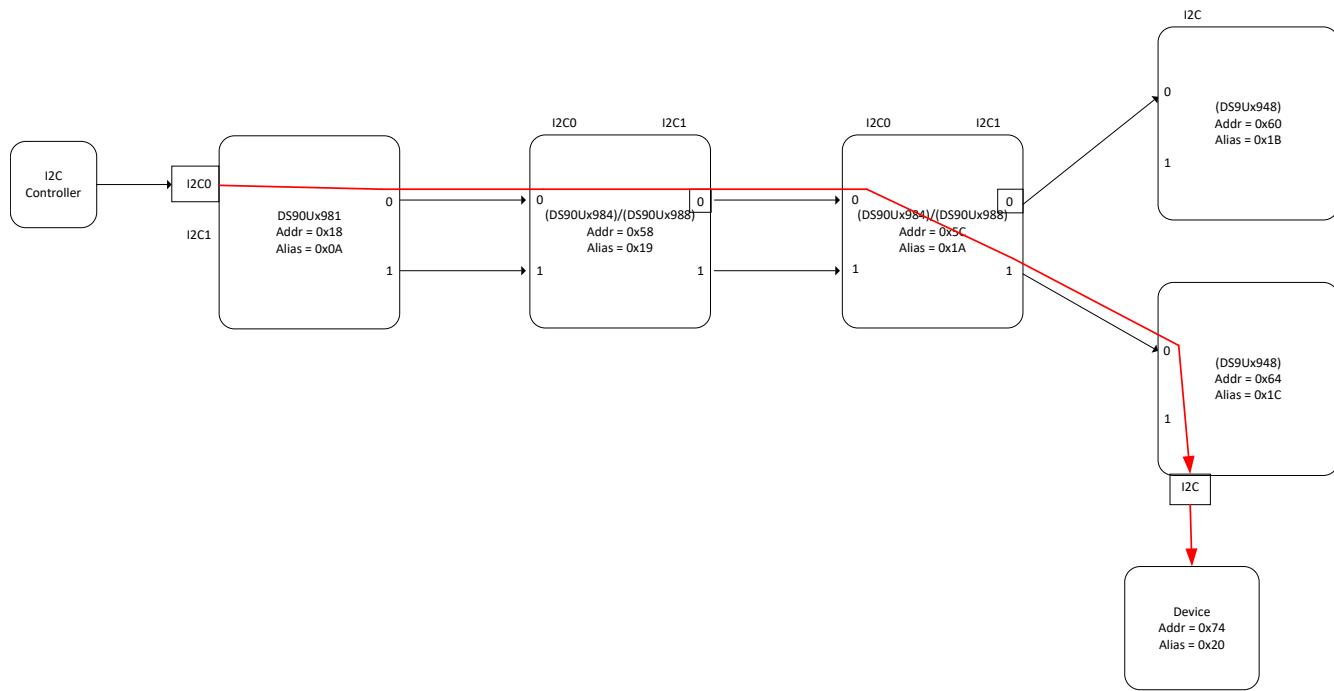
Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0111010	0x74
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0010000	0x20
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	000	0x07
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	1	
	1:0	REMAINING_DEPTH[1:0]	11	

**Figure 7-35. Daisy-Chain Communication Example #2****Table 7-55. Daisy-Chain Communication Example #2**

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0111 001	0x72
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0001110	0x1D
	0	LCL_PORTSEL_ID0	1	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	001	0x22
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	10	

**Figure 7-36. Daisy-Chain Communication Example #3****Table 7-56. Daisy-Chain Communication Example #3**

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0111 011	0x76
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0010001	0x22
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	000	0x02
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	10	

**Figure 7-37. Daisy-Chain Communication Example #4****Table 7-57. Daisy-Chain Communication Example #2**

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0111 010	0x74
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0010000	0x20
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	000	0x06
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	1	
	1:0	REMAINING_DEPTH[1:0]	10	

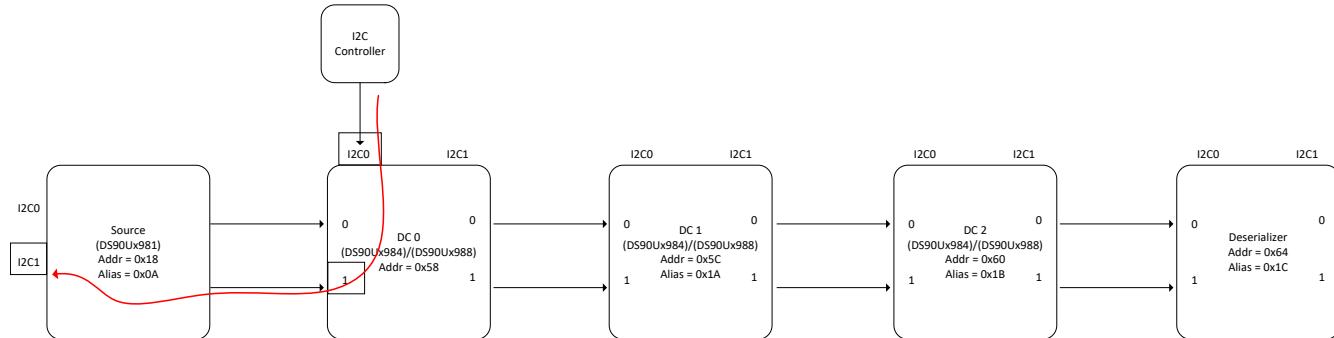


Figure 7-38. BCC Communication Upstream Example

Table 7-58. BCC Communication Upstream Example

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID0	0001 1000	0x18
	0	RESERVED	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0000101	0x0B
	0	LCL_PORTSEL_ID0	1	
TARGET_DEST_0	7:5	DEST_ADDR[2:0]	001	0x20
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	0	

Daisy-chain operation supports a maximum of three daisy-chain devices plus one additional deserializer. Depths 1, 2, and 3 port selection bit controls the forwarding port selection of the corresponding daisy-chain device.

#### 7.5.4.1 Remote Target Addressing

Various system use cases require multiple devices with the same fixed I<sup>2</sup>C target address to be remotely accessible from the same I<sup>2</sup>C bus at the serializer. The DS90UH981-Q1 provides target ID virtual addressing to differentiate target addresses when connecting two or more remote devices. Eight pairs of Target Alias and Target ID registers are allocated for each I<sup>2</sup>C target in registers 0x70 through 0x7F. The alias registers allow programming virtual addresses which the host controller uses to access remote devices. The Target ID register provides the actual target address for the device on the remote I<sup>2</sup>C bus. The DS90Ux981 has two I<sup>2</sup>C Ports (I2C0 and I2C1). Each I<sup>2</sup>C Port has 8 different Target Alias registers associated to it. Hence, there are a total of 16 Target Alias registers across both I<sup>2</sup>C Ports, and multiple devices can be directly accessible remotely without the need for reprogramming. Multiple aliases can be assigned to the same Target ID as well.

#### 7.5.5 Multi-Controller Arbitration Support

The Bidirectional Control Channel implements I<sup>2</sup>C compatible bus arbitration in the proxy I<sup>2</sup>C controller implementation. When sending a data bit, each I<sup>2</sup>C controller senses the value on the SDA line. If the controller is sending a logic 1 but senses a logic 0, the controller has lost arbitration. The controller stops driving SDA, retrying the transaction when the bus becomes idle. Thus, multiple I<sup>2</sup>C controllers can be implemented in the system.

If the system does require controller-target operation in both directions across the BCC, some method of communication must be used to make sure only one direction of operation occurs at any time. The communication method can include using available read/write registers in one of the devices to allow controllers to communicate with each other to pass control between the two controllers.

### 7.5.6 I<sup>2</sup>C Restrictions on Multi-Controller Operation

The I<sup>2</sup>C specification does not provide for arbitration between controllers under certain conditions. The system must make sure the following conditions cannot occur to prevent undefined conditions on the I<sup>2</sup>C bus:

- One controller generates a repeated Start while another controller is sending a data bit.
- One controller generates a Stop while another controller is sending a data bit.
- One controller generates a repeated Start while another controller sends a Stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I<sup>2</sup>C target.

### 7.5.7 Multi-Controller Access to Device Registers

When using the latest generation of FPD-Link devices, main page registers can be accessed simultaneously from both local and remote I<sup>2</sup>C controllers. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I<sup>2</sup>C targets is still allowed in only one direction at a time.

### 7.5.8 Indirect Register Page Access Through Alternative Device Address

Alternatively to using the indirect register access registers (0x40, 0x41, 0x42) the indirect register pages can be accessed and modified by using an alternative I<sup>2</sup>C address. To set the I<sup>2</sup>C address set register IND\_REG\_I2C\_IDX (0xF9, 0xFB, 0xFD, 0xFF), to set the indirect register page set IND\_REG\_I2C\_CTLx (0xF8, 0xFA, 0xFC, 0xFE). All of these I<sup>2</sup>C addresses can then be accessed from local I<sup>2</sup>C controllers attached to the device. For remote I<sup>2</sup>C access using the direct access option, only IND\_REG\_ID0 can be mapped one page at a time.

An I<sup>2</sup>C controller on the deserializer can only use the I<sup>2</sup>C address IND\_REG\_I2C\_ID0 (0xF9) to access the corresponding indirect register page that is set in register IND\_REG\_I2C\_CTL0(0xF8).

### 7.5.9 Unique ID

Each device is programmed with a Unique ID that is burnt into devices at Wafer level. Unique ID with a 12 bytes customer readable value indicating wafer lot and position of each IC inside a wafer. Combination of UniqueIDs can be read and maintained by customer in a database or in a Hash table. Each system can be identified by the UniqueID programmed into the devices. Authenticity of the overall system can be established at the powerup/initialization or periodically by checking the UniqueID.

A Unique ID is programmed into each device and can be read using I<sup>2</sup>C reads. To read the Unique ID, set the APB\_SELECT (0x48[7:3]) register to DIE ID (00011) then set registers APB\_ADRx (0x49 and 0x4A) to the Unique ID register being read, then read the APB\_DATA0 register. There are 12 Unique ID registers, each of the registers contain 8 bits of the total unique ID. The table below lists the Unique ID APB registers addresses.

**Table 7-59. Unique ID Registers**

APB register	APB address (APB_ADR0 = APB address[0:7], APB_ADR1 = APB address[8:15])
UNIQUE_ID_0	0x0000
UNIQUE_ID_1	0x0001
UNIQUE_ID_2	0x0002
UNIQUE_ID_3	0x0003
UNIQUE_ID_4	0x0004
UNIQUE_ID_5	0x0005
UNIQUE_ID_6	0x0006
UNIQUE_ID_7	0x0007
UNIQUE_ID_8	0x0008
UNIQUE_ID_9	0x0009
UNIQUE_ID_10	0x000A
UNIQUE_ID_11	0x000B

### 7.5.10 FPD-Link Lock

The deserializer's PLL locks onto the FPD-Link signal sent out of the DS90UH981-Q1 and constantly send the lock status to the DS90UH981-Q1 across the back channel. The DS90UH981-Q1 displays this lock status in the RX\_LOCK\_DET (0x0C[6]) register. If the forward channel signal or back channel signal are disrupted then the DS90UH981-Q1 indicates a loss of lock. If the deserializer is locked onto the forward channel signal and the back channel signal is disrupted then the DS90UH981-Q1 indicates a loss of lock.

### 7.5.11 ESD Event Counter

The ESD event counter tracks the number of ESD events experienced by the device. These ESD events are counted when the integrated ESD structure is activated. The ESD event counter is enabled by default and must be cleared to 0 on power up by writing a 0 and then a 1 to the ESD\_EVENT\_COUNTER\_ENABLE (0xBC[6]) as power supply transients can cause the ESD event counter to increment. The number of ESD events can be read in the ESD\_EVENT\_COUNTER (0xBC[5:0]) register. There is no ESD dead-time built into the counter, which means that even with a single pulse event more than one ESD event can be logged. The ESD event counter can not count ESD events on the FPD-Link lines themselves because the external CMC's and ESD protection can prevent the device's ESD structure from triggering. The ESD\_EVENT\_COUNTER (0xBC[5:0]) register does not clear when the device is reset through registers or through the PDB pin. To clear the ESD\_EVENT\_COUNTER (0xBC[5:0]) register to 0 set the ESD\_EVENT\_COUNTER\_ENABLE (0xBC[6]) register to 0 then 1.

## 7.6 Register Map

The DS90UH981-Q1 implements the following register blocks, accessible via I2C including over the bi-directional control channel:

- Shared Registers
- FPD-Link TX Port Registers (separate register block for each of the TX ports)
- I2C Port Registers (separate register block for each of the I2C ports)

TargetID/TargetAlias/TargetDest/I2C\_Pass\_Through (0x07[3]) can be written and read only from their corresponding local I2C port. FPD-Link TX Port Registers can be read and written by setting the TX\_PORT\_SEL register to appropriate setting (0x01 for Port 0 and 0x12 for Port 1).

**Table 7-60. Main Register Map Descriptions**

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP	
0x00	I2C Port Registers	I2C Target 0	I2C Target 1
0x01-0x06	Digital Shared Registers	Shared	
0x07-0x08	I2C Port Registers	I2C Target 0	I2C Target 1
0x09-0x16	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1
0x17-0x2C	Digital Shared Registers	Shared	
0x2D	I2C Port Registers	I2C Target 0	I2C Target 1
0x2E-0x56	Digital Shared Registers	Shared	
0x57-0x6F	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1
0x70-0x7F	I2C Port Registers	I2C Target 0	I2C Target 1
0x80-0x87	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1
0x88-0x8F	I2C Port Registers	I2C Target 0	I2C Target 1
0x90-0xA3	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1
0xA4-0xBF	Digital Shared Registers	Shared	
0xC0-0xFF	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1

### 7.6.1 Main\_Page Registers

**Table 7-61** lists the memory-mapped registers for the Main\_Page registers. All register offset addresses not listed in **Table 7-61** should be considered as reserved locations and the register contents should not be modified.

**Table 7-61. MAIN\_PAGE Registers**

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID	I2C_DEVICE_ID	Go
0x1	RESET_CTL	RESET_CTL	Go
0x2	GENERAL_CFG2	GENERAL_CFG2	Go
0x3	I2C_CONTROLLER_CFG	I2C_CONTROLLER_CFG	Go
0x4	SDA_SETUP	SDA_SETUP	Go
0x5	FPD4_CFG	FPD4_CFG	Go
0x6	GENERAL_STS2	GENERAL_STS2	Go
0x7	GENERAL_CFG	GENERAL_CFG	Go
0x8	DES_ID	DES_ID	Go
0x9	BC_DUTY_CYC	BC_DUTY_CYC	Go
0xA	CRC_ERROR0	CRC_ERROR0	Go
0xB	CRC_ERROR1	CRC_ERROR1	Go
0xC	GENERAL_STS	GENERAL_STS	Go
0xD	FPD4_DATAPATH_CTL	FPD4_DATAPATH_CTL	Go
0xE	FPD4_DATAPATH_CTL2	FPD4_DATAPATH_CTL2	Go

**Table 7-61. MAIN\_PAGE Registers (continued)**

Address	Acronym	Register Name	Section
0xF	BIST_BC_ERRORS	BIST_BC_ERRORS	<a href="#">Go</a>
0x10	FPD3_DES_CAP1	FPD3_DES_CAP1	<a href="#">Go</a>
0x11	FPD3_DES_CAP2	FPD3_DES_CAP2	<a href="#">Go</a>
0x12	FPD4_REMOTE_PAR_CAP1	FPD4_REMOTE_PAR_CAP1	<a href="#">Go</a>
0x13	FPD4_REMOTE_PAR_CAP2	FPD4_REMOTE_PAR_CAP2	<a href="#">Go</a>
0x14	TX_BIST_CTL	TX_BIST_CTL	<a href="#">Go</a>
0x15	FC_GPIO_CTL0	FC_GPIO_CTL0	<a href="#">Go</a>
0x16	FC_GPIO_CTL1	FC_GPIO_CTL1	<a href="#">Go</a>
0x17	GPIO0_PIN_CTL	GPIO0_PIN_CTL	<a href="#">Go</a>
0x18	GPIO1_PIN_CTL	GPIO1_PIN_CTL	<a href="#">Go</a>
0x19	GPIO2_PIN_CTL	GPIO2_PIN_CTL	<a href="#">Go</a>
0x1A	GPIO3_PIN_CTL	GPIO3_PIN_CTL	<a href="#">Go</a>
0x1B	GPIO4_PIN_CTL	GPIO4_PIN_CTL	<a href="#">Go</a>
0x1C	GPIO5_PIN_CTL	GPIO5_PIN_CTL	<a href="#">Go</a>
0x1D	GPIO6_PIN_CTL	GPIO6_PIN_CTL	<a href="#">Go</a>
0x1E	GPIO7_PIN_CTL	GPIO7_PIN_CTL	<a href="#">Go</a>
0x1F	GPIO8_PIN_CTL	GPIO8_PIN_CTL	<a href="#">Go</a>
0x20	GPIO9_PIN_CTL	GPIO9_PIN_CTL	<a href="#">Go</a>
0x21	GPIO10_PIN_CTL	GPIO10_PIN_CTL	<a href="#">Go</a>
0x22	GPIO11_PIN_CTL	GPIO11_PIN_CTL	<a href="#">Go</a>
0x23	GPIO12_PIN_CTL	GPIO12_PIN_CTL	<a href="#">Go</a>
0x24	GPIO13_PIN_CTL	GPIO13_PIN_CTL	<a href="#">Go</a>
0x25	GPI_PIN_STS1	GPI_PIN_STS1	<a href="#">Go</a>
0x26	GPI_PIN_STS2	GPI_PIN_STS2	<a href="#">Go</a>
0x27	TX_MODE_STS	TX_MODE_STS	<a href="#">Go</a>
0x28	GPIO_EN_BC	GPIO_EN_BC	<a href="#">Go</a>
0x29	BCC_WDOG_CTL	BCC_WDOG_CTL	<a href="#">Go</a>
0x2A	I2C_CONTROL	I2C_CONTROL	<a href="#">Go</a>
0x2B	SCL_HIGH_TIME	SCL_HIGH_TIME	<a href="#">Go</a>
0x2C	SCL_LOW_TIME	SCL_LOW_TIME	<a href="#">Go</a>
0x2D	PORT_SEL	PORT_SEL	<a href="#">Go</a>
0x2E	LINK_DET_CTL	LINK_DET_CTL	<a href="#">Go</a>
0x2F	IO_CTL	IO_CTL	<a href="#">Go</a>
0x30	REV_ID	REV_ID	<a href="#">Go</a>
0x31	PLL_REFCLK_FREQ	PLL_REFCLK_FREQ	<a href="#">Go</a>
0x32	REFCLK0_FREQ	REFCLK0_FREQ	<a href="#">Go</a>
0x38	I2C_CTRL_CHAIN_CTL1	I2C_CTRL_CHAIN_CTL1	<a href="#">Go</a>
0x39	I2C_CTRL_CHAIN_CTL2	I2C_CTRL_CHAIN_CTL2	<a href="#">Go</a>
0x3A	I2C_CTRL_CHAIN_CTL3	I2C_CTRL_CHAIN_CTL3	<a href="#">Go</a>
0x3B	CUSTOM_REGISTER_SETTING	CUSTOM_REGISTER_SETTING	<a href="#">Go</a>
0x3C	MAILBOX_3C	MAILBOX_3C	<a href="#">Go</a>
0x3D	MAILBOX_3D	MAILBOX_3D	<a href="#">Go</a>
0x3E	GPIO_IN_EN_HIGH	GPIO_IN_EN_HIGH	<a href="#">Go</a>
0x3F	GPIO_IN_EN_LOW	GPIO_IN_EN_LOW	<a href="#">Go</a>
0x40	IND_ACC_CTL	IND_ACC_CTL	<a href="#">Go</a>

**Table 7-61. MAIN\_PAGE Registers (continued)**

Address	Acronym	Register Name	Section
0x41	IND_ACC_ADDR	IND_ACC_ADDR	<a href="#">Go</a>
0x42	IND_ACC_DATA	IND_ACC_DATA	<a href="#">Go</a>
0x43	VP_CONFIG_REG	VP_CONFIG_REG	<a href="#">Go</a>
0x44	VP_ENABLE_REG	VP_ENABLE_REG	<a href="#">Go</a>
0x45	VP_GLOBAL_STS	VP_GLOBAL_STS	<a href="#">Go</a>
0x47	BCC_CONFIG	BCC_CONFIG	<a href="#">Go</a>
0x48	APB_CTL	APB_CTL	<a href="#">Go</a>
0x49	APB_ADR0	APB_ADR0	<a href="#">Go</a>
0x4A	APB_ADR1	APB_ADR1	<a href="#">Go</a>
0x4B	APB_DATA0	APB_DATA0	<a href="#">Go</a>
0x4C	APB_DATA1	APB_DATA1	<a href="#">Go</a>
0x4D	APB_DATA2	APB_DATA2	<a href="#">Go</a>
0x4E	APB_DATA3	APB_DATA3	<a href="#">Go</a>
0x4F	BRIDGE_CTL	BRIDGE_CTL	<a href="#">Go</a>
0x50	BRIDGE_STS	BRIDGE_STS	<a href="#">Go</a>
0x51	INTERRUPT_CTL	INTERRUPT_CTL	<a href="#">Go</a>
0x52	INTERRUPT_STS	INTERRUPT_STS	<a href="#">Go</a>
0x53	AUDIO_CFG	AUDIO_CFG	<a href="#">Go</a>
0x54	SPI_TIMING1	SPI_TIMING1	<a href="#">Go</a>
0x55	SPI_TIMING2	SPI_TIMING2	<a href="#">Go</a>
0x56	SPI_CONFIG	SPI_CONFIG	<a href="#">Go</a>
0x57	FPD3_STREAM_SEL	FPD3_STREAM_SEL	<a href="#">Go</a>
0x58	FPD3_DUAL_STS	FPD3_DUAL_STS	<a href="#">Go</a>
0x59	FPD3_MODE_CTL	FPD3_MODE_CTL	<a href="#">Go</a>
0x5A	FPD3_DATAPATH_CTL	FPD3_DATAPATH_CTL	<a href="#">Go</a>
0x5B	FPD3_FIFO_CFG	FPD3_FIFO_CFG	<a href="#">Go</a>
0x5C	FPD3_FIFO_STS	FPD3_FIFO_STS	<a href="#">Go</a>
0x62	FC_POWERDOWN_CTL	FC_POWERDOWN_CTL	<a href="#">Go</a>
0x63	BC_POWERDOWN_CTL	BC_POWERDOWN_CTL	<a href="#">Go</a>
0x64	PGCTL	PGCTL	<a href="#">Go</a>
0x65	PGCFG	PGCFG	<a href="#">Go</a>
0x66	PGIA	PGIA	<a href="#">Go</a>
0x67	PGID	PGID	<a href="#">Go</a>
0x69	PGTSTDAT	PGTSTDAT	<a href="#">Go</a>
0x6A	BC_PROCESSING_CFG	BC_PROCESSING_CFG	<a href="#">Go</a>
0x6B	ENH_BC_STS	ENH_BC_STS	<a href="#">Go</a>
0x6C	ENH_BC_CHK	ENH_BC_CHK	<a href="#">Go</a>
0x6D	BCC_STATUS	BCC_STATUS	<a href="#">Go</a>
0x6E	DATAPATH_BC_FC	DATAPATH_BC_FC	<a href="#">Go</a>
0x6F	FC_BCC_TEST	FC_BCC_TEST	<a href="#">Go</a>
0x70	TARGET_ID_0	TARGET_ID_0	<a href="#">Go</a>
0x71	TARGET_ID_1	TARGET_ID_1	<a href="#">Go</a>
0x72	TARGET_ID_2	TARGET_ID_2	<a href="#">Go</a>
0x73	TARGET_ID_3	TARGET_ID_3	<a href="#">Go</a>
0x74	TARGET_ID_4	TARGET_ID_4	<a href="#">Go</a>

**Table 7-61. MAIN\_PAGE Registers (continued)**

Address	Acronym	Register Name	Section
0x75	TARGET_ID_5	TARGET_ID_5	<a href="#">Go</a>
0x76	TARGET_ID_6	TARGET_ID_6	<a href="#">Go</a>
0x77	TARGET_ID_7	TARGET_ID_7	<a href="#">Go</a>
0x78	TARGET_ALIAS_0	TARGET_ALIAS_0	<a href="#">Go</a>
0x79	TARGET_ALIAS_1	TARGET_ALIAS_1	<a href="#">Go</a>
0x7A	TARGET_ALIAS_2	TARGET_ALIAS_2	<a href="#">Go</a>
0x7B	TARGET_ALIAS_3	TARGET_ALIAS_3	<a href="#">Go</a>
0x7C	TARGET_ALIAS_4	TARGET_ALIAS_4	<a href="#">Go</a>
0x7D	TARGET_ALIAS_5	TARGET_ALIAS_5	<a href="#">Go</a>
0x7E	TARGET_ALIAS_6	TARGET_ALIAS_6	<a href="#">Go</a>
0x7F	TARGET_ALIAS_7	TARGET_ALIAS_7	<a href="#">Go</a>
0x80	RX_BKSV0	RX_BKSV0	<a href="#">Go</a>
0x81	RX_BKSV1	RX_BKSV1	<a href="#">Go</a>
0x82	RX_BKSV2	RX_BKSV2	<a href="#">Go</a>
0x83	RX_BKSV3	RX_BKSV3	<a href="#">Go</a>
0x84	RX_BKSV4	RX_BKSV4	<a href="#">Go</a>
0x87	LOCAL_INT_STS	LOCAL_INT_STS	<a href="#">Go</a>
0x88	TARGET_DEST_0	TARGET_DEST_0	<a href="#">Go</a>
0x89	TARGET_DEST_1	TARGET_DEST_1	<a href="#">Go</a>
0x8A	TARGET_DEST_2	TARGET_DEST_2	<a href="#">Go</a>
0x8B	TARGET_DEST_3	TARGET_DEST_3	<a href="#">Go</a>
0x8C	TARGET_DEST_4	TARGET_DEST_4	<a href="#">Go</a>
0x8D	TARGET_DEST_5	TARGET_DEST_5	<a href="#">Go</a>
0x8E	TARGET_DEST_6	TARGET_DEST_6	<a href="#">Go</a>
0x8F	TARGET_DEST_7	TARGET_DEST_7	<a href="#">Go</a>
0x90	TX_KSV0	TX_KSV0	<a href="#">Go</a>
0x91	TX_KSV1	TX_KSV1	<a href="#">Go</a>
0x92	TX_KSV2	TX_KSV2	<a href="#">Go</a>
0x93	TX_KSV3	TX_KSV3	<a href="#">Go</a>
0x94	TX_KSV4	TX_KSV4	<a href="#">Go</a>
0x98	TX_AN0	TX_AN0	<a href="#">Go</a>
0x99	TX_AN1	TX_AN1	<a href="#">Go</a>
0x9A	TX_AN2	TX_AN2	<a href="#">Go</a>
0x9B	TX_AN3	TX_AN3	<a href="#">Go</a>
0x9C	TX_AN4	TX_AN4	<a href="#">Go</a>
0x9D	TX_AN5	TX_AN5	<a href="#">Go</a>
0x9E	TX_AN6	TX_AN6	<a href="#">Go</a>
0x9F	TX_AN7	TX_AN7	<a href="#">Go</a>
0xA0	RX_BCAPS	RX_BCAPS	<a href="#">Go</a>
0xA1	RX_BSTATUS0	RX_BSTATUS0	<a href="#">Go</a>
0xA2	RX_BSTATUS1	RX_BSTATUS1	<a href="#">Go</a>
0xA3	KSV_FIFO	KSV_FIFO	<a href="#">Go</a>
0xA4	GPIO_INT_CTL0	GPIO_INT_CTL0	<a href="#">Go</a>
0xA5	GPIO_INT_CTL1	GPIO_INT_CTL1	<a href="#">Go</a>
0xA6	GPIO_INT_STS0	GPIO_INT_STS0	<a href="#">Go</a>

**Table 7-61. MAIN\_PAGE Registers (continued)**

Address	Acronym	Register Name	Section
0xA7	GPIO_INT_STS1	GPIO_INT_STS1	<a href="#">Go</a>
0xB0	DSI_DEVICE_CFG	DSI_DEVICE_CFG	<a href="#">Go</a>
0xB1	DSI_ERROR	DSI_ERROR	<a href="#">Go</a>
0xB9	REG_I2C_FLTR_DEPTH_HS	REG_I2C_FLTR_DEPTH_HS	<a href="#">Go</a>
0xBC	FPD_TX_ESD_EVENT_CNTR	FPD_TX_ESD_EVENT_CNTR	<a href="#">Go</a>
0xBD	VP_DPHY_SEL0	VP_DPHY_SEL0	<a href="#">Go</a>
0xBE	VP_DPHY_SEL1	VP_DPHY_SEL1	<a href="#">Go</a>
0xBF	DUAL_VIDSYNC	DUAL_VIDSYNC	<a href="#">Go</a>
0xC0	HDCP_DBG	HDCP_DBG	<a href="#">Go</a>
0xC1	HDCP_DBG2	HDCP_DBG2	<a href="#">Go</a>
0xC2	HDCP_CFG	HDCP_CFG	<a href="#">Go</a>
0xC3	HDCP_CTL	HDCP_CTL	<a href="#">Go</a>
0xC4	HDCP_STS	HDCP_STS	<a href="#">Go</a>
0xC6	FPD3_ICR	FPD3_ICR	<a href="#">Go</a>
0xC7	FPD3_ISR	FPD3_ISR	<a href="#">Go</a>
0xC8	NVM_CTL	NVM_CTL	<a href="#">Go</a>
0xCD	HDCP_CFG2	HDCP_CFG2	<a href="#">Go</a>
0xCE	BLUE_SCREEN	BLUE_SCREEN	<a href="#">Go</a>
0xD0	IND_STS	IND_STS	<a href="#">Go</a>
0xD1	IND_SAR	IND_SAR	<a href="#">Go</a>
0xD2	IND_OAR	IND_OAR	<a href="#">Go</a>
0xD3	IND_DATA	IND_DATA	<a href="#">Go</a>
0xE2	LINK_CFG_ALIAS	LINK_CFG_ALIAS	<a href="#">Go</a>
0xE3	HDCP_CTL_ALIAS	HDCP_CTL_ALIAS	<a href="#">Go</a>
0xE4	FPD3_STS_ALIAS	FPD3_STS_ALIAS	<a href="#">Go</a>
0xE5	HDCP_TEST_ALIAS	HDCP_TEST_ALIAS	<a href="#">Go</a>
0xE6	FPD3_ICR_ALIAS	FPD3_ICR_ALIAS	<a href="#">Go</a>
0xE7	FPD3_ISR_ALIAS	FPD3_ISR_ALIAS	<a href="#">Go</a>
0xE9	HDCP_CFG2_ALIAS	HDCP_CFG2_ALIAS	<a href="#">Go</a>
0xF0	TX_ID0	TX_ID0	<a href="#">Go</a>
0xF1	TX_ID1	TX_ID1	<a href="#">Go</a>
0xF2	TX_ID2	TX_ID2	<a href="#">Go</a>
0xF3	TX_ID3	TX_ID3	<a href="#">Go</a>
0xF4	TX_ID4	TX_ID4	<a href="#">Go</a>
0xF5	TX_ID5	TX_ID5	<a href="#">Go</a>
0xF6	HDCP_TX_ID6	HDCP_TX_ID6	<a href="#">Go</a>
0xF8	IND_REG_I2C_CTL0	IND_REG_I2C_CTL0	<a href="#">Go</a>
0xF9	IND_REG_I2C_ID0	IND_REG_I2C_ID0	<a href="#">Go</a>
0xFA	IND_REG_I2C_CTL1	IND_REG_I2C_CTL1	<a href="#">Go</a>
0xFB	IND_REG_I2C_ID1	IND_REG_I2C_ID1	<a href="#">Go</a>
0xFC	IND_REG_I2C_CTL2	IND_REG_I2C_CTL2	<a href="#">Go</a>
0xFD	IND_REG_I2C_ID2	IND_REG_I2C_ID2	<a href="#">Go</a>
0xFE	IND_REG_I2C_CTL3	IND_REG_I2C_CTL3	<a href="#">Go</a>
0xFF	IND_REG_I2C_ID3	IND_REG_I2C_ID3	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. [Table 7-62](#) shows the codes that are used for access types in this section.

**Table 7-62. Main\_Page Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
RW	R W	Read Write
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WC	W C	Write to Clear
WStrap	W Strap	Write Default value loaded from bootstrap pin after reset.
Reset or Default Value		
-n		Value after reset or the default value

#### 7.6.1.1 I2C\_DEVICE\_ID Register (Address = 0x0) [Default = 0x00]

I2C\_DEVICE\_ID is shown in [Table 7-63](#).

Return to the [Summary Table](#).

**Table 7-63. I2C\_DEVICE\_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	DEVICE_ID	R/W	0x0	7-bit I2C address of Serializer for the primary I2C port. Defaults to address configured by the IDx strap pin. Each I2C target derives its DEVICE_ID from the value written to this register. I2C target 0: DEVICE_ID (primary I2C address) I2C target 1: DEVICE_ID + 1 To change the device ID, set I2C_DEVICE_ID[0] to 1 and then write to this register at the I2C device address you want to change.
0	SER_ID	R/W	0x0	0x0= Device ID is based on the value strapped from the IDx pin 0x1= Register I2C Device ID overrides value strapped from the IDx pin

#### 7.6.1.2 RESET\_CTL Register (Address = 0x1) [Default = 0x00]

RESET\_CTL is shown in [Table 7-64](#).

Return to the [Summary Table](#).

**Table 7-64. RESET\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	DSI_RESET	RH/W1S	0x0	Used as DSI reset
5	PLL0_RESET	RH/W1S	0x0	PLL 0 reset
4	PLL1_RESET	RH/W1S	0x0	PLL 1 reset
3	RESERVED	R/W	0x0	Reserved

**Table 7-64. RESET\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2	RESERVED	R	0x0	Reserved
1	DIGITAL_RESET_ALL	RH/W1S	0x0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 0x0= Normal operation 0x1= Reset
0	DIGITAL_RESET_NOREGS	RH/W1S	0x0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 0x0= Normal operation 0x1= Reset

**7.6.1.3 GENERAL\_CFG2 Register (Address = 0x2) [Default = 0xD0]**GENERAL\_CFG2 is shown in [Table 7-65](#).Return to the [Summary Table](#).**Table 7-65. GENERAL\_CFG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	HALFRATE_MODE_CH1	R	0x1	FPD half/full rate mode for FPD3/4 lane 0 By default, this register is Read-Only status indicating the current rate setting, based on the FPD mode of operation as follows: 0: Full-rate, if device configured to 3.375Gbps through mode strap in FPD-Link IV mode. 1: Half-rate, if device is configured for FPD3 mode, or FPD-Link IV mode If the FPD_RATE_OVERRIDE bit in the register is set to 1, this register becomes Read-Write and will control the half-rate mode setting for digital logic.
6	HALFRATE_MODE_CH0	R	0x1	FPD half/full rate mode for FPD3/4 lane 1 By default, this register is Read-Only status indicating the current rate setting, based on the FPD mode of operation as follows: 0: Full-rate, if device configured to 3.375Gbps through mode strap in FPD-Link IV mode. 1: Half-rate, if device is configured for FPD3 mode, or FPD-Link IV mode If the FPD_RATE_OVERRIDE bit in the register is set to 1, this register becomes Read-Write and will control the half-rate mode setting for digital logic.
5	CRC_ERROR_RESET	R/W	0x0	Clear CRC Error Counters. This bit is NOT self-clearing. 0x0= Normal operation 0x1= Clear counters
4	RESERVED	R/W	0x1	Reserved
3	DSI_DISABLE	R/W	0x0	DSI Disable Resets the analog DSI and digital DSI. This bit is NOT self-clearing. It is a strap option on the MODE_SEL1 pin. 1: Reset 0: Normal operation
2:1	I2S_EN	R/W	0x0	Enable I2S for FPD4 through GPIO or data island method depending upon per port REG 0x5A[3] selection.
0	FPD_RATE_OVERRIDE	R/W	0x0	FPD Rate Override Control 0: FPD Half-rate/Full-rate setting is based on configured operational mode 1: FPD Half-rate/Full-rate setting is based on override controls For digital logic, rate override controls are the HALFRATE_MODE_CHx controls in this register. For analog logic, rate override controls are the sel_fulrate controls on Page 1, register 0x09 and 0x29.

**7.6.1.4 I2C\_CONTROLLER\_CFG Register (Address = 0x3) [Default = 0x60]**I2C\_CONTROLLER\_CFG is shown in [Table 7-66](#).Return to the [Summary Table](#).**Table 7-66. I2C\_CONTROLLER\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	ARB_TIMEOUT_DISABLE	R/W	0x0	By default, ARB_TIMEOUT values are effective. This bit provides an override to disable timeout in case it is needed.
6:5	ARB_TIMEOUT	R/W	0x3	This is for I2S Daisy Chain Arbiter timeout. Default is set to highest timeout= 2'b11.
4:3	SDA_OUT_DELAY	R/W	0x0	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 0x0= 200ns 0x1= 240ns 0x2= 280ns 0x3= 320ns Actual delays may be larger dependent on system capacitances and signal rise/fall times.
2	LOCAL_WRITE_DIS	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C controller attached to the Deserializer. Setting this bit does not affect remote access to I2C targets at the Serializer.
1	I2C_BUS_TIMER_SPEED_UP	R/W	0x0	Speed up I2C Bus Watchdog Timer 0x0= Watchdog Timer expires after approximately 1 second. 0x1= Watchdog Timer expires after approximately 50 microseconds
0	I2C_BUS_TIMER_DISABLE	R/W	0x0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus will be assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL.

**7.6.1.5 SDA\_SETUP Register (Address = 0x4) [Default = 0x01]**SDA\_SETUP is shown in [Table 7-67](#).Return to the [Summary Table](#).**Table 7-67. SDA\_SETUP Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	RESERVED
3:0	RESERVED	R/W	0x1	Reserved

**7.6.1.6 FPD4\_CFG Register (Address = 0x5) [Default = 0x28]**FPD4\_CFG is shown in [Table 7-68](#).Return to the [Summary Table](#).**Table 7-68. FPD4\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CH1_FPD3_REFCLK1	R/W	0x0	Using REFCLK1 (25 - 50 MHz) for CH1 FPD-Link III instead of REFCLK0 (27 MHz)

**Table 7-68. FPD4\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	CH0_FPD3_REFCLK1	R/W	0x0	Using REFCLK1 (25 - 50 MHz) for CH0 FPD-Link III instead of REFCLK0 (27 MHz)
5:2	FPD4_TX_MODE	R/W	0xA	FPD4 TX Mode: This register controls the operating mode of the FPD4 Transmit function. 0x0= FPD3 Port 0, FPD3 Port 1 (FPD3 mode selected by 0x59) 0x3= FPD4 Port 0, FPD3 Port 1 (set 0x59 to forced single Port 1) 0xA= FPD4 Dual 0xB= Forced Single FPD4 Port0 (Port 1 disabled) 0xC= FPD3 Port 0, FPD4 Port 1 (set 0x59 to forced single Port 0) 0xE= Forced Single FPD4 Port1 (Port 0 disabled) 0xF= FPD4 Independent
1	I2S_AUDIO_SPLIT_P1	R/W	0x0	Split audio for FPD4 Port0; If I2S is enabled, and audio over GPIO is selected, select I2S_DA and I2S_DB or I2S_DC and I2S_DD.
0	I2S_AUDIO_SPLIT_P0	R/W	0x0	Split audio for FPD4 Port1; If I2S is enabled, and audio over GPIO is selected, select I2S_DA and I2S_DB or I2S_DC and I2S_DD.

**7.6.1.7 GENERAL\_STS2 Register (Address = 0x6) [Default = 0x00]**GENERAL\_STS2 is shown in [Table 7-69](#).Return to the [Summary Table](#).**Table 7-69. GENERAL\_STS2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DEV	R	0x0	0x0= DS90UH981 0x1= DS90UB981
4	REFCLK0_VALID	R	0x0	REFCLK0 REFCLK valid
3	PLL_REFCLK_VALID	R	0x0	PLL REFCLK valid
2:0	RESERVED	R	0x0	Reserved

**7.6.1.8 GENERAL\_CFG Register (Address = 0x7) [Default = 0x80]**GENERAL\_CFG is shown in [Table 7-70](#).Return to the [Summary Table](#).**Table 7-70. GENERAL\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RX_CRC_CHECKER_ENABLE	R/W	0x1	CRC Checker Enable 0x0= Disable 0x1= Enable The PORT_SEL register controls which FPD port is selected for this register bit.
6	RESERVED	R	0x0	Reserved
5	TX_AUTO_ACK	R/W	0x0	Automatically Acknowledge I2C Remote Write When enabled, I2C writes to the Deserializer (or any remote I2C Target, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus. Each I2C target maintains its own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel. 0x0= Disable 0x1= Enable

**Table 7-70. GENERAL\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	I2C_PASS_ALL	R/W	0x0	Each I2C target maintains its own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel. 0x0= Enable Forward Control Channel pass-through only of I2C accesses to I2C Target IDs matching either the remote Deserializer Target ID or the remote Target ID. Each I2C target maintains its own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel. 0x1= Enable Forward Control Channel pass-through of all I2C accesses to I2C Target IDs that do not match the Serializer I2C Target ID.
3	I2C_PASS_THROUGH	R/W	0x0	I2C Pass-Through Mode Each I2C target maintains its own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel. 0x0= Pass-Through Disabled 0x1:= Pass-Through Enabled
2	RESERVED	R/W	0x0	Reserved
1:0	ADAS_IVI_MODE	R/W	0x0	ADAS or IVI mode. This register is set by MODE_SEL2 and MODE_SEL0 0x3 - Enable ADAS mode 0x0 - Enable IVI mode

**7.6.1.9 DES\_ID Register (Address = 0x8) [Default = 0x00]**DES\_ID is shown in [Table 7-71](#).Return to the [Summary Table](#).**Table 7-71. DES\_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	DES_DEV_ID	R/W	0x0	7-bit Deserializer Device ID Configures the I2C Target ID of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent loading by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates the Deserializer Device ID for the Deserializer attached to Port 1
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Deserializer Device ID Prevent auto-loading of the Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written. If PORT1_SEL is set, this bit controls DES_DEV_ID_P1.

**7.6.1.10 BC\_DUTY\_CYC Register (Address = 0x9) [Default = 0x80]**BC\_DUTY\_CYC is shown in [Table 7-72](#).Return to the [Summary Table](#).

If PORT1\_SEL is set, this register indicates Port1 Back Channel Duty Cycle

**Table 7-72. BC\_DUTY\_CYC Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	BC_DUTY_CYCLE_	R	0x80	Back Channel Duty Cycle measurement (per port): This register provides a measurement of the back channel duty cycle for the selected FPD3 port. The measurement is between 0 and 255 where 0x80 indicates a 50% duty cycle signal. To determine % duty cycle from the measurement, use the following equation: Duty Cycle (%) = BC_DUTY_CYCLE * 100 / 256

**7.6.1.11 CRC\_ERROR0 Register (Address = 0xA) [Default = 0x00]**CRC\_ERROR0 is shown in [Table 7-73](#).Return to the [Summary Table](#).

If PORT1\_SEL is set, this register indicates Port1 Status

**Table 7-73. CRC\_ERROR0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_7_0	R	0x0	Number of Back Channel CRC errors – 8 least significant bits. This register is cleared using the CRC ERROR RESET in register 0x02[5].

**7.6.1.12 CRC\_ERROR1 Register (Address = 0xB) [Default = 0x00]**CRC\_ERROR1 is shown in [Table 7-74](#).Return to the [Summary Table](#).

If PORT1\_SEL is set, this register indicates Port1 Status

**Table 7-74. CRC\_ERROR1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_15_8	R	0x0	Number of Back Channel CRC errors – 8 most significant bits. This register is cleared using the CRC ERROR RESET in register 0x02[5].

**7.6.1.13 GENERAL\_STS Register (Address = 0xC) [Default = 0x00]**GENERAL\_STS is shown in [Table 7-75](#).Return to the [Summary Table](#).

If PORT1\_SEL is set, this register indicates Port1 Status

**Table 7-75. GENERAL\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved.
6	RX_LOCK_DET	R	0x0	RX Lock detect for selected port: This bit indicates current Receiver Lock Detect status for the selected port. This value is returned as part of the back channel information from the Deserializer.
5	RESERVED	R	0x0	Reserved
4	LINK_LOST	R	0x0	Link Lost Flag for selected port: This bit indicates that loss of link has been detected. This register bit will stay high until cleared using the CRC ERROR RESET in register 0x04.

**Table 7-75. GENERAL\_STS Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3	BIST_CRC_ERROR	R	0x0	CRC error during BIST communication with Deserializer. This bit is cleared upon restart of BIST or assertion of CRC ERROR RESET in register 0x02[5].
2	RESERVED	R	0x0	Reserved
1	BC_CRC_ERROR	R	0x0	Back channel error detect for selected port: Back channel CRC error during communication with Deserializer. This bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x02[5].
0	LINK_DETECT	R	0x0	Link Detect status for selected port: 0x0= Cable link not detected 0x1= Cable link detected

**7.6.1.14 FPD4\_DATAPATH\_CTL Register (Address = 0xD) [Default = 0xE4]**FPD4\_DATAPATH\_CTL is shown in [Table 7-76](#).Return to the [Summary Table](#).

Datapath Control Register 1 The Datapath Control values are sent as part of the DCA sequence to the deserializer. The fields indicate capabilities and operational modes of the forward channel.

**Table 7-76. FPD4\_DATAPATH\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x1	Reserved
6	FPD4_I2SB_FC_EN_P0	R/W	0x1	If FPD4 Audio uses forward channel GPIO, this bit enables 4-channel audio using FC_GPIO[3]. This is per port register.
5	FPD4_I2S_TRANSPORT_P0	R/W	0x1	In FPD4, this indicates if 0= I2S data over FC_GPIO if bit [4] is set. This bit for port1 is always set to 0
4	FPD4_FC_SD_P_STREAM_P0	R/W	0x0	In FPD4, if bit[5] is 0; 0= I2S audio for FPD4 is disabled. - Default 1= I2S audio over FC_GPIO enabled. This is per port register. If bit[5] is 1; 0= I2S over data island through SDP0 stream 1= I2S over data island through SDP1 stream
3	FPD4_VIDEO_DISABLE	R/W	0x0	If this bit is set, it disables video on paired De-serializer
2	FPD4_DUAL_EN	R/W	0x1	This bit indicates FPD4 is configured as FPD4 dual link. When on Deserializer, REG0x31[4:2]==000, This configuration takes place. If REG0x31[4:2] != 000, FPD4_dual_en is ignored.
1:0	GPIOEN_FC	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs for the selected port 0x0= GPIOs disabled 0x1= One GPIO 0x2= Two GPIOs 0x3= Four GPIOs

**7.6.1.15 FPD4\_DATAPATH\_CTL2 Register (Address = 0xE) [Default = 0x00]**FPD4\_DATAPATH\_CTL2 is shown in [Table 7-77](#).Return to the [Summary Table](#).

Datapath Control Register 2 The Datapath Control values are sent as part of the DCA sequence to the deserializer. The fields indicate capabilities and operational modes of the forward channel.

**Table 7-77. FPD4\_DATAPATH\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	RESERVED
3	FC_ECC_BCC_ONLY_P0	R/W	0x0	Forward Channel ECC on I2C only If ECC operation is enabled, this bit indicates if ECC is enabled for the I2C bit only.
2	FC_ECC_GPIO_P0_	R/W	0x0	Forward Channel ECC on GPIO bit If ECC operation is enabled, this bit indicates if ECC is included for the GPIO bit which is encoded as part of CSI[0].
1:0	FC_ECC_P0_	R/W	0x0	Forward Channel ECC Operation 0x0= No ECC present 0x1= 6-bit ECC 0x2= 7-bit ECC 0x3= 8-bit ECC

**7.6.1.16 BIST\_BC\_ERRORS Register (Address = 0xF) [Default = 0x00]**BIST\_BC\_ERRORS is shown in [Table 7-78](#).Return to the [Summary Table](#).**Table 7-78. BIST\_BC\_ERRORS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	BIST_BC_ERROR_COUNT	R	0x0	BIST Back Channel CRC Error Counter This register is cleared upon loss of link, restart of BIST, or assertion of CRC ERROR RESET in register 0x04. If PORT1_SEL is set, this register indicates port 1 status

**7.6.1.17 FPD3\_DES\_CAP1 Register (Address = 0x10) [Default = 0x00]**FPD3\_DES\_CAP1 is shown in [Table 7-79](#).Return to the [Summary Table](#).

FPD3 Deserializer Capabilities Register 1 This register contains the lower bits of the Deserializer Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the Deserializer. If bit 7 is set, the bits become read/write rather than read-only.

**Table 7-79. FPD3\_DES\_CAP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	FREEZE_FPD3_DES_CAP	R/W	0x0	Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Back Channel. The Capabilities will be frozen at the values written in registers 0x10 and 0x11.
6	HSCC_MODE_0	R/W	0x0	High-Speed Control Channel bit 0 Lowest bit of the 3-bit HSCC indication. The other 2 bits are contained in register HSCC_MODE_2_1. This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	DUAL_LINK_CAP	R/W	0x0	Dual link Capabilities Indicates if the Deserializer is capable of dual link operation. This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.

**Table 7-79. FPD3\_DES\_CAP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2	DUAL_CHANNEL	R/W	0x0	Dual Channel 0/1 Indication In a dual-link capable device, indicates if this is the primary or secondary channel. 0x0= Primary channel (channel 0) 0x1= Secondary channel (channel 1) This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
1	VID_24B_HD_AUD	R/W	0x0	Deserializer supports 24-bit video concurrently with HD audio This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
0	DES_CAP_FC_GPIO	R/W	0x0	Deserializer supports GPIO in the Forward Channel Frame This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.

**7.6.1.18 FPD3\_DES\_CAP2 Register (Address = 0x11) [Default = 0x00]**FPD3\_DES\_CAP2 is shown in [Table 7-80](#).Return to the [Summary Table](#).

FPD3 Deserializer Capabilities Register 2 This register contains the upper bits of the Deserializer Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the Deserializer. If bit 7 is set, the bits become read/write rather than read-only.

**Table 7-80. FPD3\_DES\_CAP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	FC_BCC_CRC6	R/W	0x0	Enable Forward Channel CRC6 for BCC frames Enable enhanced CRC and start sequence for forward channel signaling of the Bidirectional Control Channel
2	RGB_CHKSUM_ERR	R	0x0	RGB Checksum Error Detected: If RGB Checksum is enabled through the HDCP Transmitter HDCP_DBG register, this bit will indicate if a checksum error is detected.
1:0	HSCC_MODE_2_1	R/W	0x0	High-Speed Control Channel bit 0 Upper bits of the 3-bit HSCC indication. The lowest bit is contained in register HSCC_MODE_0. 0x0= Normal back channel frame, GPIO mode 0x1= High Speed GPIO mode, 1 GPIO 0x2= High Speed GPIO mode, 2 GPIOs 0x3= High Speed GPIO mode: 4 GPIOs 0x4= Reserved 0x5= Reserved 0x6= High Speed, Forward Channel SPI mode 0x7= High Speed, Reverse Channel SPI mode In Single Link devices, only Normal back channel frame modes (0x0) are supported.

**7.6.1.19 FPD4\_REMOTE\_PAR\_CAP1 Register (Address = 0x12) [Default = 0x00]**FPD4\_REMOTE\_PAR\_CAP1 is shown in [Table 7-81](#).

Return to the [Summary Table](#).

FPD4 Partner Capabilities Register 1 This register contains the lower bits of the Partner Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the Deserializer. If bit 7 is set, the bits become read/write rather than read-only.

**Table 7-81. FPD4\_REMOTE\_PAR\_CAP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	FREEZE_FPD4_DES_CAP	R/W	0x0	Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Back Channel. The Capabilities will be frozen at the values written in registers 0x12 and 0x13.
6	RESERVED	R	0x0	Reserved
5	BIST_EN	R/W	0x0	Link BIST Enable This bit is used in conjunction with capable de-serializers to enable link BIST.
4	RESERVED	R	0x0	Reserved
3:0	RESERVED	R	0x0	Reserved

#### 7.6.1.20 FPD4\_REMOTE\_PAR\_CAP2 Register (Address = 0x13) [Default = 0x00]

FPD4\_REMOTE\_PAR\_CAP2 is shown in [Table 7-82](#).

Return to the [Summary Table](#).

**Table 7-82. FPD4\_REMOTE\_PAR\_CAP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	FPD4_REMOTE_PAR_CAP2	R/W	0x0	FPD4 Deserializer Capabilities Register 2 This register contains the upper bits of the Deserializer Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the Deserializer. If bit 7 is set, the bits become read/write rather than read-only.

#### 7.6.1.21 TX\_BIST\_CTL Register (Address = 0x14) [Default = 0x00]

TX\_BIST\_CTL is shown in [Table 7-83](#).

Return to the [Summary Table](#).

BIST and DOPL mode control register

**Table 7-83. TX\_BIST\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	BISTEN_NO_RESET	R/W	0x0	Enable BIST mode with FPD PLL reset
2:1	RESERVED	R	0x0	Reserved
0	BIST_EN	R/W	0x0	BIST Control 0x0= Disabled 0x1= Enabled This bit is used in conjunction with capable serializers to enable link BIST.

#### 7.6.1.22 FC\_GPIO\_CTL0 Register (Address = 0x15) [Default = 0x00]

FC\_GPIO\_CTL0 is shown in [Table 7-84](#).

[Return to the Summary Table.](#)

Forward channel GPIO Control Register 0

**Table 7-84. FC\_GPIO\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	FC_GPIO1_SEL	R/W	0x0	Forward channel GPIO1 Select: Determines the data sent on GPIO1 for the selected port forward channel. 0x0 - 0xD= Pin GPIOx 0xE= Constant value of 0 0xF= Constant value of 1 TX Port 0 Default= 0x1 TX Port 1 Default= 0xB
3:0	FC_GPIO0_SEL	R/W	0x0	Forward channel GPIO0 Select: Determines the data sent on GPIO0 for the selected port forward channel. 0x0 - 0xD= Pin GPIOx 0xE= Constant value of 0 0xF= Constant value of 1 TX Port 0 Default= 0x0 TX Port 1 Default= 0xA

**7.6.1.23 FC\_GPIO\_CTL1 Register (Address = 0x16) [Default = 0x00]**

FC\_GPIO\_CTL1 is shown in [Table 7-85](#).

[Return to the Summary Table.](#)

Forward channel GPIO Control Register 1

**Table 7-85. FC\_GPIO\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	FC_GPIO3_SEL	R/W	0x0	Forward channel GPIO3 Select: Determines the data sent on GPIO3 for the selected port forward channel. 0x0 - 0xD= Pin GPIOx 0xE= Constant value of 0 0xF= Constant value of 1 TX Port 0 Default= 0x3 TX Port 1 Default= 0xD
3:0	FC_GPIO2_SEL	R/W	0x0	Forward channel GPIO2 Select: Determines the data sent on GPIO2 for the selected port forward channel. 0x0 - 0xD= Pin GPIOx 0xE= Constant value of 0 0xF= Constant value of 1 TX Port 0 Default= 0x2 TX Port 1 Default= 0xC

**7.6.1.24 GPIO0\_PIN\_CTL Register (Address = 0x17) [Default = 0x00]**

GPIO0\_PIN\_CTL is shown in [Table 7-86](#).

[Return to the Summary Table.](#)

**Table 7-86. GPIO0\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO0_OUTPUT_EN	R/W	0x0	GPIO0 Output Enable 0x0= Disabled 0x1= Enabled

**Table 7-86. GPIO0\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:4	GPIO0_OUT_SRC	R/W	0x0	GPIO0 Output Source Select: Refer to GPIO0_OUT_SEL

**Table 7-86. GPIO0\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO0_OUT_SEL	R/W	0x0	<p>GPIO0 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO0_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO0_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO0_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO0_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO0_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-86. GPIO0\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.25 GPIO1\_PIN\_CTL Register (Address = 0x18) [Default = 0x00]**GPIO1\_PIN\_CTL is shown in [Table 7-87](#).Return to the [Summary Table](#).**Table 7-87. GPIO1\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO1_OUTPUT_EN	R/W	0x0	GPIO1 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO1_OUT_SRC	R/W	0x0	GPIO1 Output Source Select: Refer to GPIO1_OUT_SEL

**Table 7-87. GPIO1\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO1_OUT_SEL	R/W	0x0	<p>GPIO1 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO1_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO1_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO1_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO1_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO1_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-87. GPIO1\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.26 GPIO2\_PIN\_CTL Register (Address = 0x19) [Default = 0x00]**GPIO2\_PIN\_CTL is shown in [Table 7-88](#).Return to the [Summary Table](#).**Table 7-88. GPIO2\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO2_OUTPUT_EN	R/W	0x0	GPIO2 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO2_OUT_SRC	R/W	0x0	GPIO2 Output Source Select Selects output source for GPIO2 data: 000b= FPD Port 0 [15:0] data; 100b= FPD port 0 [31:16] data 001b= FPD Port 1 [15:0] data; 101b= FPD port 1 [31:16] data x10b= Device Status x11b= Reserved

**Table 7-88. GPIO2\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO2_OUT_SEL	R/W	0x0	<p>GPIO2 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO2_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO2_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO2_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO2_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO2_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-88. GPIO2\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.27 GPIO3\_PIN\_CTL Register (Address = 0x1A) [Default = 0x00]**GPIO3\_PIN\_CTL is shown in [Table 7-89](#).Return to the [Summary Table](#).**Table 7-89. GPIO3\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO3_OUTPUT_EN	R/W	0x0	GPIO3 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO3_OUT_SRC	R/W	0x0	GPIO3 Output Source Select: Refer to GPIO3_OUT_SEL

**Table 7-89. GPIO3\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO3_OUT_SEL	R/W	0x0	<p>GPIO3 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO3_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO3_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO3_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO3_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO3_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-89. GPIO3\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.28 GPIO4\_PIN\_CTL Register (Address = 0x1B) [Default = 0x08]**GPIO4\_PIN\_CTL is shown in [Table 7-90](#).Return to the [Summary Table](#).**Table 7-90. GPIO4\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO4_OUTPUT_EN	R/W	0x0	GPIO4 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO4_OUT_SRC	R/W	0x0	GPIO4 Output Source Select: Refer to GPIO4_OUT_SEL

**Table 7-90. GPIO4\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO4_OUT_SEL	R/W	0x8	<p>GPIO4 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO4_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO4_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO4_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO4_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO4_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-90. GPIO4\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.29 GPIO5\_PIN\_CTL Register (Address = 0x1C) [Default = 0x00]**GPIO5\_PIN\_CTL is shown in [Table 7-91](#).Return to the [Summary Table](#).**Table 7-91. GPIO5\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO5_OUTPUT_EN	R/W	0x0	GPIO5 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO5_OUT_SRC	R/W	0x0	GPIO5 Output Source Select: Refer to GPIO5_OUT_SEL

**Table 7-91. GPIO5\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO5_OUT_SEL	R/W	0x0	<p>GPIO5 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO5_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO5_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO5_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO5_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO5_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-91. GPIO5\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.30 GPIO6\_PIN\_CTL Register (Address = 0x1D) [Default = 0x00]**GPIO6\_PIN\_CTL is shown in [Table 7-92](#).Return to the [Summary Table](#).**Table 7-92. GPIO6\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO6_OUTPUT_EN	R/W	0x0	GPIO6 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO6_OUT_SRC	R/W	0x0	GPIO6 Output Source Select: Refer to GPIO6_OUT_SEL

**Table 7-92. GPIO6\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO6_OUT_SEL	R/W	0x0	<p>GPIO6 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO6_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO6_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO6_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO6_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO6_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-92. GPIO6\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.31 GPIO7\_PIN\_CTL Register (Address = 0x1E) [Default = 0x00]**GPIO7\_PIN\_CTL is shown in [Table 7-93](#).Return to the [Summary Table](#).**Table 7-93. GPIO7\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO7_OUTPUT_EN	R/W	0x0	GPIO7 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO7_OUT_SRC	R/W	0x0	GPIO7 Output Source Select: Refer to GPIO7_OUT_SEL

**Table 7-93. GPIO7\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO7_OUT_SEL	R/W	0x0	<p>GPIO7 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO7_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO7_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO7_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO7_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO7_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-93. GPIO7\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.32 GPIO8\_PIN\_CTL Register (Address = 0x1F) [Default = 0x00]**GPIO8\_PIN\_CTL is shown in [Table 7-94](#).Return to the [Summary Table](#).**Table 7-94. GPIO8\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO8_OUTPUT_EN	R/W	0x0	GPIO8 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO8_OUT_SRC	R/W	0x0	GPIO8 Output Source Select: Refer to GPIO8_OUT_SEL

**Table 7-94. GPIO8\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO8_OUT_SEL	R/W	0x0	<p>GPIO8 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO8_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO8_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO8_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO8_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO8_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-94. GPIO8\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.33 GPIO9\_PIN\_CTL Register (Address = 0x20) [Default = 0x00]**GPIO9\_PIN\_CTL is shown in [Table 7-95](#).Return to the [Summary Table](#).**Table 7-95. GPIO9\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO9_OUTPUT_EN	R/W	0x0	GPIO9 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO9_OUT_SRC	R/W	0x0	GPIO9 Output Source Select: Refer to GPIO9_OUT_SEL

**Table 7-95. GPIO9\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO9_OUT_SEL	R/W	0x0	<p>GPIO9 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO9_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO9_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO9_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO9_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO9_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-95. GPIO9\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.34 GPIO10\_PIN\_CTL Register (Address = 0x21) [Default = 0x00]**GPIO10\_PIN\_CTL is shown in [Table 7-96](#).Return to the [Summary Table](#).**Table 7-96. GPIO10\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO10_OUTPUT_EN	R/W	0x0	GPIO10 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO10_OUT_SRC	R/W	0x0	GPIO10 Output Source Select: Refer to GPIO10_OUT_SEL

**Table 7-96. GPIO10\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO10_OUT_SEL	R/W	0x0	<p>GPIO10 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO10_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO10_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO10_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO10_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO10_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-96. GPIO10\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.35 GPIO11\_PIN\_CTL Register (Address = 0x22) [Default = 0x00]**GPIO11\_PIN\_CTL is shown in [Table 7-97](#).Return to the [Summary Table](#).**Table 7-97. GPIO11\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO11_OUTPUT_EN	R/W	0x0	GPIO11 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO11_OUT_SRC	R/W	0x0	GPIO11 Output Source Select: Refer to GPIO11_OUT_SEL

**Table 7-97. GPIO11\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO11_OUT_SEL	R/W	0x0	<p>GPIO11 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO11_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO11_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO11_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO11_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO11_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-97. GPIO11\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.36 GPIO12\_PIN\_CTL Register (Address = 0x23) [Default = 0x00]**GPIO12\_PIN\_CTL is shown in [Table 7-98](#).Return to the [Summary Table](#).**Table 7-98. GPIO12\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO12_OUTPUT_EN	R/W	0x0	GPIO12 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO12_OUT_SRC	R/W	0x0	GPIO12 Output Source Select: Refer to GPIO12_OUT_SEL

**Table 7-98. GPIO12\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO12_OUT_SEL	R/W	0x0	<p>GPIO12 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO12_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO12_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO12_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO12_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO12_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-98. GPIO12\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.37 GPIO13\_PIN\_CTL Register (Address = 0x24) [Default = 0x00]**GPIO13\_PIN\_CTL is shown in [Table 7-99](#).Return to the [Summary Table](#).**Table 7-99. GPIO13\_PIN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO13_OUTPUT_EN	R/W	0x0	GPIO13 Output Enable 0x0= Disabled 0x1= Enabled
6:4	GPIO13_OUT_SRC	R/W	0x0	GPIO13 Output Source Select: Refer to GPIO13_OUT_SEL

**Table 7-99. GPIO13\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	GPIO13_OUT_SEL	R/W	0x0	<p>GPIO13 Output Select</p> <p>Determines the output data for the selected source.</p> <p>If GPIO13_OUT_SRC is set to 000b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO0</li> <li>0001b= Received PORT0 BC_GPIO1</li> <li>0010b= Received PORT0 BC_GPIO2</li> <li>0011b= Received PORT0 BC_GPIO3</li> <li>0100b= Received PORT0 BC_GPIO4</li> <li>0101b= Received PORT0 BC_GPIO5</li> <li>0110b= Received PORT0 BC_GPIO6</li> <li>0111b= Received PORT0 BC_GPIO7</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100b= AND(PORT0 RX_LOCK_DET,PORT1 RX_LOCK_DET)</li> <li>1101 - 1111b= Reserved</li> </ul> <p>If GPIO13_OUT_SRC is set to 100b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT0 BC_GPIO8</li> <li>0001b= Received PORT0 BC_GPIO9</li> <li>0010b= Received PORT0 BC_GPIO10</li> <li>0011b= Received PORT0 BC_GPIO11</li> <li>0100b= Received PORT0 BC_GPIO12</li> <li>0101b= Received PORT0 BC_GPIO13</li> <li>0110b= Received PORT0 BC_GPIO14</li> <li>0111b= Received PORT0 BC_GPIO15</li> <li>1000b= PORT0 RX_INTN</li> <li>1001b= PORT0 RX_LOCK_DET</li> <li>1010b= PORT0 FPD3_TX_INTN</li> <li>1011b= PORT0 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO13_OUT_SRC is set to 001b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO0</li> <li>0001b= Received PORT1 BC_GPIO1</li> <li>0010b= Received PORT1 BC_GPIO2</li> <li>0011b= Received PORT1 BC_GPIO3</li> <li>0100b= Received PORT1 BC_GPIO4</li> <li>0101b= Received PORT1 BC_GPIO5</li> <li>0110b= Received PORT1 BC_GPIO6</li> <li>0111b= Received PORT1 BC_GPIO7</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO13_OUT_SRC is set to 101b, the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Received PORT1 BC_GPIO8</li> <li>0001b= Received PORT1 BC_GPIO9</li> <li>0010b= Received PORT1 BC_GPIO10</li> <li>0011b= Received PORT1 BC_GPIO11</li> <li>0100b= Received PORT1 BC_GPIO12</li> <li>0101b= Received PORT1 BC_GPIO13</li> <li>0110b= Received PORT1 BC_GPIO14</li> <li>0111b= Received PORT1 BC_GPIO15</li> <li>1000b= PORT1 RX_INTN</li> <li>1001b= PORT1 RX_LOCK_DET</li> <li>1010b= PORT1 FPD3_TX_INTN</li> <li>1011b= PORT1 FPD3_TX_INT</li> <li>1100 - 1111b= Reserved</li> </ul> <p>If GPIO13_OUT_SRC is set to x10b (Device Status), the following selections apply:</p> <ul style="list-style-type: none"> <li>0000b= Fixed output value of 0</li> <li>0001b= Fixed output value of 1</li> <li>0010b= Inverted INTERRUPT STATUS</li> <li>0011b= INTERRUPT STATUS</li> </ul>

**Table 7-99. GPIO13\_PIN\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
				0100b= Inverted VP Combined INTERRUPT Status 0101b= VP Combined INTERRUPT Status 0110 - 1111b= Reserved

**7.6.1.38 GPI\_PIN\_STS1 Register (Address = 0x25) [Default = 0x00]**GPI\_PIN\_STS1 is shown in [Table 7-100](#).Return to the [Summary Table](#).**Table 7-100. GPI\_PIN\_STS1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	GPIO_PIN_STS_7_0	R	0x0	Read status value set on the GPIO pins 7:0

**7.6.1.39 GPI\_PIN\_STS2 Register (Address = 0x26) [Default = 0x00]**GPI\_PIN\_STS2 is shown in [Table 7-101](#).Return to the [Summary Table](#).**Table 7-101. GPI\_PIN\_STS2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	GPIO_PIN_STS_13_8	R	0x0	Read status value set on the GPIO pins 13:8

**7.6.1.40 TX\_MODE\_STS Register (Address = 0x27) [Default = 0x88]**TX\_MODE\_STS is shown in [Table 7-102](#).Return to the [Summary Table](#).**Table 7-102. TX\_MODE\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MODE_SEL1_DONE	R	0x1	Indicates MODE_SEL1 value has stabilized and been latched
6:4	MODE_SEL1_DECODE	R	0x0	Returns the 3-bit decode of the MODE_SEL1 pin
3	MODE_SEL0_DONE	R	0x1	Indicates MODE_SEL0 value has stabilized and been latched
2:0	MODE_SEL0_DECODE	R	0x0	Returns the 3-bit decode of the MODE_SEL0 pin

**7.6.1.41 GPIO\_EN\_BC Register (Address = 0x28) [Default = 0x02]**GPIO\_EN\_BC is shown in [Table 7-103](#).Return to the [Summary Table](#).**Table 7-103. GPIO\_EN\_BC Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved

**Table 7-103. GPIO\_EN\_BC Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	GPIO_BC_EN	R/W	0x2	Indicates how many GPIOs are carried through FPD4 back-channel. When 0x0= four GPIOs mapped on local GPIO[3:0], where every back-channel frames always provides 4 GPIOs. When 0x1= Eight GPIOs mapped on local GPIOs. Where Idle frame with K28.5 and K28.3 carries GPIO[3:0] and K28.1 and K28.2 provides GPIO[7:4]. i.e. every alternate back-channel frames provide GPIO[3:0] and GPIO[7:4] When 0x2= 16 GPIOs mapped on local GPIOs, (with Max valid GPIOs are only 13), where Idle frame with K28.5=GPIO[3:0], K28.1=GPIO[7:4], K28.3=GPIO[11:8] and K28.2=GPIO[15:12]. i.e. every fourth frame updates given GPIO frame status. When 0x3, back channel receives one HS GPIO. Each back channel frame contains four samples for single GPIO. HS GPIO is always on GPIO[0] from back-channel module, one for each FPD4 port

**7.6.1.42 BCC\_WDOG\_CTL Register (Address = 0x29) [Default = 0xFE]**BCC\_WDOG\_CTL is shown in [Table 7-104](#).Return to the [Summary Table](#).**Table 7-104. BCC\_WDOG\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	BCC_WATCHDOG_TIMER	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
0	BCC_WDOG_DIS	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 0x0= Enables BCC Watchdog Timer operation 0x1= Disables BCC Watchdog Timer operation

**7.6.1.43 I2C\_CONTROL Register (Address = 0x2A) [Default = 0x1E]**I2C\_CONTROL is shown in [Table 7-105](#).Return to the [Summary Table](#).**Table 7-105. I2C\_CONTROL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	SDA_HOLD_TIME	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xE	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

**7.6.1.44 SCL\_HIGH\_TIME Register (Address = 0x2B) [Default = 0x7F]**SCL\_HIGH\_TIME is shown in [Table 7-106](#).Return to the [Summary Table](#).

**Table 7-106. SCL\_HIGH\_TIME Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_SCL_HIGH	R/W	0x7F	I2C Controller SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional oscillator clock periods. Min_delay= 38.0952ns * (TX_SCL_HIGH + 5)

**7.6.1.45 SCL\_LOW\_TIME Register (Address = 0x2C) [Default = 0x7F]**SCL\_LOW\_TIME is shown in [Table 7-107](#).Return to the [Summary Table](#).**Table 7-107. SCL\_LOW\_TIME Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_SCL_LOW	R/W	0x7F	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional clock periods. Min_delay= 38.0952ns * (TX_SCL_LOW + 5)

**7.6.1.46 PORT\_SEL Register (Address = 0x2D) [Default = 0x01]**PORT\_SEL is shown in [Table 7-108](#).Return to the [Summary Table](#).

FPD TX Port page Select TX port register page for reading and writing port specific registers. The register provides separate controls for read selection and for write selection. The 2-bit TX\_READ\_PORT field provides for reading values from a single port. The 4-bit TX\_WRITE\_PORT field provides individual enables for each port, allowing simultaneous writes to any of the four FPD3 Receive port register blocks. A separate copy of the PORT\_SEL register is maintained for each possible function that may access the registers, preventing conflict between the possible sources of register access.

**Table 7-108. PORT\_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	PHYS_PORT_NUM	R	0x0	Physical port number. This field provides the physical port connection when reading from a remote device via the Bidirectional Control Channel or through local I2C interface. When accessed via local I2C interfaces, the value returned is the I2C port connection. When accessed via Bidirectional Control Channel, the value returned is the port number of the received port connection. Main Page=00 Target0/controller0=00 Target1/Controller1=01

**Table 7-108. PORT\_SEL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
5:4	TX_READ_PORT	R/W	0x0	Select TX port for register read. This field selects one of the two TX port register blocks for readback. This applies to all paged FPD3/FPD4 Transmitter port registers. 00= Port 0 registers 01= Port 1 registers When access via local I2C interfaces, the default settings depends upon the interface as shown in the default value column. Since there are only 2 physical FPD TX ports, values of 2 and 3 do not provide access to FPD TX port registers. Settings of 2 and 3 will return values for DEVICE_ID (0x00), BCC_STATUS registers (register 0x6D) and TargetID/TargetAlias/TargetDest registers (0x70-0x7F, and 0x80-0x8F) as those registers are implemented specifically for each target or controller rather than per FPD port. Main Page=00 Target0/controller0=00 Target1/controller1=01
3	RESERVED	R/W	0x0	Reserved
2	TX_WRITE_PORT_2	R/W	0x0	Write enable for Target2/Controller2 registers. Setting this bit will allow writing DEVICE_ID (0x00), BCC_STATUS registers (register 0x6D) and TargetID/TargetAlias/TargetDest registers (0x70-0x7F, and 0x80-0x8F) as those registers are implemented specifically for each target or controller rather than per FPD port. DEVICE_ID (0x00), BCC_STATUS registers (register 0x6D) and TargetID/TargetAlias/TargetDest registers (0x70-0x7F, and 0x80-0x8F) as those registers are implemented specifically for each target or controller rather than per FPD port. Main page=0 Target0/controller0=0 Target1/controller1=0
1	TX_WRITE_PORT_1	R/W	0x0	Write enable for TX port 1 registers. This bit enables writes to TX port 1 registers. Any combination of TX port registers can be written simultaneously. This applies to all paged FPD3/FPD4 transmitter port registers. 0= write disables 1= write enables. Main page=0 Target0/controller0=0 Target1/controller1=1
0	TX_WRITE_PORT_0	R/W	0x1	Write enable for TX port 0 registers. This bit enables writes to TX port 0 registers. Any combination of TX port registers can be written simultaneously. This applies to all paged FPD3/FPD4 transmitter port registers. 0= write disables 1= write enables. Main page=0 Target0/controller0=1 Target1/controller1=0

**7.6.1.47 LINK\_DET\_CTL Register (Address = 0x2E) [Default = 0x00]**LINK\_DET\_CTL is shown in [Table 7-109](#).Return to the [Summary Table](#).

**Table 7-109. LINK\_DET\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2:0	LINK_DETECT_TIMER	R/W	0x0	Bidirectional Control Channel Link Detect Timer This field configures the link detection timeout period. If the timer expires without valid communication over the reverse channel, link detect will be deasserted. 0x0= 162 us 0x1= 325 us 0x2= 650 us 0x3= 1.3 ms 0x4= 10.25us 0x5= 20.5us 0x6= 41us 0x7= 82us

**7.6.1.48 IO\_CTL Register (Address = 0x2F) [Default = 0x09]**IO\_CTL is shown in [Table 7-110](#).Return to the [Summary Table](#).**Table 7-110. IO\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	I2C_SEL3P3V	R/W	0x0	I2C select 0x0= 1.8V 0x1= 3.3V Strapped from the ID <sub>x</sub> pin during power-up
6	RESERVED	R/W	0x0	Reserved
5:4	RESERVED	R/W	0x0	Reserved
3:0	RESERVED	R/W	0x9	Reserved

**7.6.1.49 REV\_ID Register (Address = 0x30) [Default = 0x00]**REV\_ID is shown in [Table 7-111](#).Return to the [Summary Table](#).**Table 7-111. REV\_ID Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	REV_ID	R	0x0	Rev ID 0b0010= Production Device
3:0	RESERVED	R	0x0	Reserved

**7.6.1.50 PLL\_REFCLK\_FREQ Register (Address = 0x31) [Default = 0x00]**PLL\_REFCLK\_FREQ is shown in [Table 7-112](#).Return to the [Summary Table](#).**Table 7-112. PLL\_REFCLK\_FREQ Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PLL_REFCLK_FREQ	R	0x0	PLL refclk detection frequency

**7.6.1.51 REFCLK0\_FREQ Register (Address = 0x32) [Default = 0x00]**REFCLK0\_FREQ is shown in [Table 7-113](#).Return to the [Summary Table](#).**Table 7-113. REFCLK0\_FREQ Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	REFCLK0_FREQ	R	0x0	REFCLK0 detection frequency

**7.6.1.52 I2C\_CTRL\_CHAIN\_CTL1 Register (Address = 0x38) [Default = 0x21]**I2C\_CTRL\_CHAIN\_CTL1 is shown in [Table 7-114](#).Return to the [Summary Table](#).**Table 7-114. I2C\_CTRL\_CHAIN\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	I2C_TARGET1_CONN	R/W	0x2	I2C Target 1 Connection Controls which I2C port is connected to I2C Target 1 Allowed values: 0x0= No connection 0x1= Connect primary I2C port (I2C_SDA0/I2C_SCL0) 0x2= Connect second I2C port (I2C_SDA1/I2C_SCL1)
3	RESERVED	R	0x0	Reserved
2:0	I2C_TARGET0_CONN	R/W	0x1	I2C Target 0 Connection Controls which I2C port is connected to I2C Target 0 Allowed values: 0x0= No connection 0x1= Connect primary I2C port (I2C_SDA0/I2C_SCL0) 0x2= Connect second I2C port (I2C_SDA1/I2C_SCL1)

**7.6.1.53 I2C\_CTRL\_CHAIN\_CTL2 Register (Address = 0x39) [Default = 0x04]**I2C\_CTRL\_CHAIN\_CTL2 is shown in [Table 7-115](#).Return to the [Summary Table](#).**Table 7-115. I2C\_CTRL\_CHAIN\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2:0	I2C_TARGET2_CONN	R/W	0x4	I2C Target 2 Connection Controls which I2C port is connected to I2C Target 2 Allowed values: 0x0= No connection 0x1= Connect primary I2C port (SDA/SCL) 0x2= Connect second I2C port (SDA2/SCL2) 0x4= Connect third I2C port (SDA3/SCL3)

**7.6.1.54 I2C\_CTRL\_CHAIN\_CTL3 Register (Address = 0x3A) [Default = 0x00]**I2C\_CTRL\_CHAIN\_CTL3 is shown in [Table 7-116](#).Return to the [Summary Table](#).**Table 7-116. I2C\_CTRL\_CHAIN\_CTL3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DIS_CONTROLLER1	R/W	0x0	Disable remote controller from FPD link port 1

**Table 7-116. I2C\_CTRL\_CHAIN\_CTL3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:4	RESERVED	R	0x0	Reserved
3	DIS_CONTROLLER0	R/W	0x0	Disable remote controller from FPD link port 0
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

**7.6.1.55 CUSTOM\_REGISTER\_SETTING Register (Address = 0x3B) [Default = 0x00]**CUSTOM\_REGISTER\_SETTING is shown in [Table 7-117](#).Return to the [Summary Table](#).**Table 7-117. CUSTOM\_REGISTER\_SETTING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	LOAD_CUSTOM_SETTING	RH/W1S	0x0	Self clearing bit, enables the user to load a custom configuration
6:5	RESERVED	R	0x0	Reserved
4:0	CUSTOM_SETTING_VALUE	R/W	0x0	Used to load any custom settings

**7.6.1.56 MAILBOX\_3C Register (Address = 0x3C) [Default = 0x00]**MAILBOX\_3C is shown in [Table 7-118](#).Return to the [Summary Table](#).**Table 7-118. MAILBOX\_3C Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MAILBOX_3C	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

**7.6.1.57 MAILBOX\_3D Register (Address = 0x3D) [Default = 0x00]**MAILBOX\_3D is shown in [Table 7-119](#).Return to the [Summary Table](#).**Table 7-119. MAILBOX\_3D Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MAILBOX_3D	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

**7.6.1.58 GPIO\_IN\_EN\_HIGH Register (Address = 0x3E) [Default = 0xFF]**GPIO\_IN\_EN\_HIGH is shown in [Table 7-120](#).Return to the [Summary Table](#).

**Table 7-120. GPIO\_IN\_EN\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x1	Reserved
6	RESERVED	R	0x1	Reserved
5	GPIO13_INPUT_EN	R/W	0x1	GPIO13 Input Enable 0x0= Disabled 0x1= Enabled
4	GPIO12_INPUT_EN	R/W	0x1	GPIO12 Input Enable 0x0= Disabled 0x1= Enabled
3	GPIO11_INPUT_EN	R/W	0x1	GPIO11 Input Enable 0x0= Disabled 0x1= Enabled
2	GPIO10_INPUT_EN	R/W	0x1	GPIO10 Input Enable 0x0= Disabled 0x1= Enabled
1	GPIO9_INPUT_EN	R/W	0x1	GPIO9 Input Enable 0x0= Disabled 0x1= Enabled
0	GPIO8_INPUT_EN	R/W	0x1	GPIO8 Input Enable 0x0= Disabled 0x1= Enabled

**7.6.1.59 GPIO\_IN\_EN\_LOW Register (Address = 0x3F) [Default = 0xFF]**GPIO\_IN\_EN\_LOW is shown in [Table 7-121](#).Return to the [Summary Table](#).**Table 7-121. GPIO\_IN\_EN\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GPIO7_INPUT_EN	R/W	0x1	GPIO7 Input Enable 0x0= Disabled 0x1= Enabled
6	GPIO6_INPUT_EN	R/W	0x1	GPIO6 Input Enable 0x0= Disabled 0x1= Enabled
5	GPIO5_INPUT_EN	R/W	0x1	GPIO5 Input Enable 0x0= Disabled 0x1= Enabled
4	GPIO4_INPUT_EN	R/W	0x1	GPIO4 Input Enable 0x0= Disabled 0x1= Enabled
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable 0x0= Disabled 0x1= Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable 0x0= Disabled 0x1= Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable 0x0= Disabled 0x1= Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable 0x0= Disabled 0x1= Enabled

**7.6.1.60 IND\_ACC\_CTL Register (Address = 0x40) [Default = 0x00]**IND\_ACC\_CTL is shown in [Table 7-122](#).Return to the [Summary Table](#).**Table 7-122. IND\_ACC\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:2	IND_ACC_SEL	R/W	0x0	Indirect Access Register Select: Selects target page for register access 0000: Disabled 0001: FPD Ports 0-1 registers 0010: FPD PLL 0-1 registers 0011: Reserved 0100: DPHY P0 Digital Registers 0101: Reserved 0110: DPHY P1 Digital Registers 0111: Reserved 1000: ADAS compatibility Registers 1001: DFT Registers 1010: Reserved 1011: Link Layer Registers 1100: Video Processor 0/1/2/3 Registers 1101: Reserved 1110: ADC Control Registers 1111: Reserved
1	IND_ACC_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1. For auto-increment on reads, the IND_ACC_READ bit should also be set.
0	IND_ACC_READ	R/W	0x0	Indirect Access Register Read: Typically, this bit should be set to 1 when reading indirect access registers. It should be set to 0 when writing to indirect access registers. For access to page 1 registers, setting this bit allows Clear-on-read of status registers. If this bit is set to 0, the status registers may be read, but will not be cleared on read. For access to analog registers that require prefetch, setting this allows generation of a read strobe to the analog block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register.

**7.6.1.61 IND\_ACC\_ADDR Register (Address = 0x41) [Default = 0x00]**IND\_ACC\_ADDR is shown in [Table 7-123](#).Return to the [Summary Table](#).**Table 7-123. IND\_ACC\_ADDR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IND_ACC_ADDR	R/W	0x0	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

**7.6.1.62 IND\_ACC\_DATA Register (Address = 0x42) [Default = 0x00]**IND\_ACC\_DATA is shown in [Table 7-124](#).Return to the [Summary Table](#).

**Table 7-124. IND\_ACC\_DATA Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IND_ACC_DATA	R/W	0x0	Indirect Access Register Data: Writing this register will cause an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register

**7.6.1.63 VP\_CONFIG\_REG Register (Address = 0x43) [Default = 0x01]**VP\_CONFIG\_REG is shown in [Table 7-125](#).Return to the [Summary Table](#).

Video Processor Global Configuration Register

**Table 7-125. VP\_CONFIG\_REG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:4	VP2VP_EN	R/W	0x0	Video Processor to Video Processor Forwarding 0x0= VP input set by VP_DPHY_SELx (0xBD, 0xBE) If the merge functionality is disabled: 0x1= The VP2 output is forwarded to the input of VP0 and VP1 0x2= The VP0 output is forwarded to the input of VP2 and VP3 If the merge functionality is enabled: 0x1= The merged stream from VP0 and VP1 is mapped to the input of VP2 and VP3 0x2= The merged stream from VP2 and VP3 is mapped to the input of VP0 and VP1
3	RESERVED	R	0x0	Reserved
2:0	NUM_VID_STREAMS	R/W	0x1	Number of Video Processors meant to be used. This field controls the memory allocation, in pixels, to the VPs (VP0:VP1:VP2:VP3) 0x0= 16K:0:0:0 0x1= 16K:16K:0:0 0x2= 16K:8K:8K:0 0x3= 8K:8K:8K:8K

**7.6.1.64 VP\_ENABLE\_REG Register (Address = 0x44) [Default = 0x00]**VP\_ENABLE\_REG is shown in [Table 7-126](#).Return to the [Summary Table](#).

Video Processor Enable Register

**Table 7-126. VP\_ENABLE\_REG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	VP3_ENABLE	R/W	0x0	Enable Video Processor 3 Additional control and status for VP3 are starting at register 0xC0 of Indirect Register page 12
2	VP2_ENABLE	R/W	0x0	Enable Video Processor 2 Additional control and status for VP2 are starting at register 0x80 of Indirect Register page 12

**Table 7-126. VP\_ENABLE\_REG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	VP1_ENABLE	R/W	0x0	Enable Video Processor 1 Additional control and status for VP1 are starting at register 0x40 of Indirect Register page 12
0	VP0_ENABLE	R/W	0x0	Enable Video Processor 0 Additional control and status for VP0 are starting at register 0x00 of Indirect Register page 12

**7.6.1.65 VP\_GLOBAL\_STS Register (Address = 0x45) [Default = 0x00]**VP\_GLOBAL\_STS is shown in [Table 7-127](#).Return to the [Summary Table](#).

Video Processor Global Status Register Summary of status from all video processors

**Table 7-127. VP\_GLOBAL\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	VP3_TIMING_GEN_STS	R	0x0	Timing Generator Status for Video Processor 3 This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.
2	VP2_TIMING_GEN_STS	R	0x0	Timing Generator Status for Video Processor 2 This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.
1	VP1_TIMING_GEN_STS	R	0x0	Timing Generator Status for Video Processor 1 This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.
0	VP0_TIMING_GEN_STS	R	0x0	Timing Generator Status for Video Processor 0 This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

**7.6.1.66 BCC\_CONFIG Register (Address = 0x47) [Default = 0x01]**BCC\_CONFIG is shown in [Table 7-128](#).Return to the [Summary Table](#).**Table 7-128. BCC\_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	I2C_CONTROLLER_DISABLE	R/W	0x0	This bit will disable the remote reads and writes from the I2C controller. I2C controller writes and reads to the local registers will still work, but no remote writes and reads 0x0= I2C controller remote read/write is enabled 0x1= I2C controller remote read/writes is disabled

**Table 7-128. BCC\_CONFIG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	BCC_TERM_ON_ERR	R/W	0x0	Terminate Control Channel transactions on CRC Error detection During control channel operations, if a CRC Error occurs, it is unlikely to affect control channel operation. Setting this bit will allow more conservative operation that terminates any active Control Channel operation if an error is detected in the back channel. 0x0= Don't terminate BCC transactions on CRC Errors 0x1= Terminate BCC transactions on CRC Errors This bit will have no effect if Enhanced Error checking is disabled (BCC_EN_ENH_ERROR set to 0).
3	RESERVED	R	0x0	Reserved
2	BCC_ACK_REMOTE_READ	R/W	0x0	Enable Control Channel to acknowledge start of remote read. When operating with a link partner that supports Enhanced Error Checking for the Bidirectional Control Channel, setting this bit allows the Serializer to generate an internal acknowledge to the beginning of a remote I2C target read. This allows additional error detection at the Deserializer. This bit should not be set when operating with Deserializers that do not support Enhanced Error Checking. 0x0= Disable 0x1= Enable
1	BCC_EN_DATA_CHK	R/W	0x0	Enable checking of returned data Enhanced Error checking can check for errors on returned data during an acknowledge cycle for data sent to remote devices over the Bidirectional Control Channel. In addition, If an error is detected, this register control will allow changing a remote Ack to a Nack to indicate the data error on the local I2C interface. This bit should not be set when operating with Deserializers that do not support Enhanced Error checking as they will not always return the correct data during an Ack. 0x0= Disable returned data error detection 0x1= Enable returned data error detection
0	BCC_EN_ENH_ERROR	R/W	0x1	Enable Enhanced Error checking in Bidirectional Control Channel The Bidirectional Control Channel can detect certain error conditions and terminate transactions if an error is detected. This capability can be disabled by setting this bit to 0. 0x0= Disable Enhanced Error checking 0x1= Enable Enhanced Error checking

#### 7.6.1.67 APB\_CTL Register (Address = 0x48) [Default = 0x00]

APB\_CTL is shown in [Table 7-129](#).

Return to the [Summary Table](#).

**Table 7-129. APB\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	APB_SELECT	R/W	0x0	APB Select: Selects target for register access: 00000 - 00010: Reserved 00011: Unique ID (read only) 00100 - 11111: Reserved
2	APB_AUTO_INC	R/W	0x0	APB Auto Increment: Enables auto-increment mode. Upon completion of an APB read or write, the APB address will automatically be incremented by 0x1
1	APB_READ	R/W	0x0	Start APB Read: Setting this bit to a 1 will begin an APB read. Read data will be available in the APB_DATA0 register. The APB_ADR0 register should be programmed prior to setting this bit. This bit will be cleared when the read is complete.

**Table 7-129. APB\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	APB_ENABLE	R/W	0x0	APB Interface Enable: Set to a 1 to enable the APB interface. The APB_SELECT bits indicate what device is selected.

**7.6.1.68 APB\_ADR0 Register (Address = 0x49) [Default = 0x00]**APB\_ADR0 is shown in [Table 7-130](#).Return to the [Summary Table](#).

APB Address Register 0

**Table 7-130. APB\_ADR0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	APB_ADR0	R/W	0x0	APB Address byte 0 (LSB)

**7.6.1.69 APB\_ADR1 Register (Address = 0x4A) [Default = 0x00]**APB\_ADR1 is shown in [Table 7-131](#).Return to the [Summary Table](#).

APB Address Register 1

**Table 7-131. APB\_ADR1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	APB_ADR1	R/W	0x0	APB Address byte 1 (MSB)

**7.6.1.70 APB\_DATA0 Register (Address = 0x4B) [Default = 0x00]**APB\_DATA0 is shown in [Table 7-132](#).Return to the [Summary Table](#).

APB Data Register 0

**Table 7-132. APB\_DATA0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	APB_DATA0	R/W	0x0	Byte 0 (LSB) of the APB Interface Data

**7.6.1.71 APB\_DATA1 Register (Address = 0x4C) [Default = 0x00]**APB\_DATA1 is shown in [Table 7-133](#).Return to the [Summary Table](#).

APB Data Register 1

**Table 7-133. APB\_DATA1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	APB_DATA1	R/W	0x0	Byte 1 of the APB Interface Data

**7.6.1.72 APB\_DATA2 Register (Address = 0x4D) [Default = 0x00]**APB\_DATA2 is shown in [Table 7-134](#).Return to the [Summary Table](#).

APB Data Register 2

**Table 7-134. APB\_DATA2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	APB_DATA2	R/W	0x0	Byte 2 of the APB Interface Data

**7.6.1.73 APB\_DATA3 Register (Address = 0x4E) [Default = 0x00]**APB\_DATA3 is shown in [Table 7-135](#).Return to the [Summary Table](#).

APB Data Register 3

**Table 7-135. APB\_DATA3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	APB_DATA3	R/W	0x0	Byte 3 (MSB) of the APB Interface Data

**7.6.1.74 BRIDGE\_CTL Register (Address = 0x4F) [Default = 0x01]**BRIDGE\_CTL is shown in [Table 7-136](#).Return to the [Summary Table](#).**Table 7-136. BRIDGE\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_CONTINUOUS_CLK	R/W	0x0	DSI Continuous Clock Mode This bit controls handling of the DSI Clock lane. If in continuous clock mode, the DSI logic will assume the clock input is always in HS Mode and will bypass initialization requirements for the clock lane. PORT_SEL(0x2D) selects which DSI port this setting modifies. 1: Continuous Clock 0: Non-Continuous Clock
6	RESERVED	R	0x0	Reserved
5	DSI_PORT_SEL	R/W	0x0	DSI Receive input select In Single DSI mode, this control selects the active input DSI Port. 0: Select DSI Input port 0 1: Select DSI Input port 1 In Independent DSI to FPD3 mode, setting this bit to 1 will swap the DSI ports such that DSI port 0 will map to FPD3 port 1 and DSI port 1 will map to FPD3 port 0. If DUAL_DSI_EN is set to 1, DSI_PORT_SEL should be set to 0.
4	RESERVED	R	0x0	Reserved
3:2	DSI_LANES	R/W	0x0	DSI Lane Selection Indicates number of DSI Lanes that are active. 00: 1 Lane (DSI Lane 0) 01: 2 Lanes 10: 3 Lanes 11: 4 Lanes DSI_LANES is initially loaded from the MODE_SEL1 pin strap options. To avoid video errors, the DSI_LANES field should only be changed when the DSI input is inactive. PORT_SEL(0x2D) selects which DSI port this setting modifies.
1	RESERVED	R/W	0x0	Reserved

**Table 7-136. BRIDGE\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	DSI_TO_VP_FWD_EN	R/W	0x1	DSI to VP Forwarding Enable Enables data path between the DSI block and the VP/DSI to CSI converter. Recommended value of 1 1- Forwarding enable 0- Forwarding disabled

**7.6.1.75 BRIDGE\_STS Register (Address = 0x50) [Default = 0x02]**BRIDGE\_STS is shown in [Table 7-137](#).Return to the [Summary Table](#).**Table 7-137. BRIDGE\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	CFG_CKSUM	R	0x1	Configuration checksum status: Indicates result of Configuration checksum during initialization. The device verifies the 2's complement checksum in the last 128 bytes of the efuse-ROM. A value of 1 indicates the checksum passed.
0	RESERVED	R	0x0	Reserved

**7.6.1.76 INTERRUPT\_CTL Register (Address = 0x51) [Default = 0x00]**INTERRUPT\_CTL is shown in [Table 7-138](#).Return to the [Summary Table](#).**Table 7-138. INTERRUPT\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	INTB_PIN_EN	R/W	0x0	Global Interrupt Enable
6	IE_VIDEO_PROC	R/W	0x0	Video Processor Interrupt Enable interrupt from the Video Processors.
5	RESERVED	R/W	0x0	Reserved
4	IE_DPHY_RX0	R/W	0x0	DPHY Interrupt Enable interrupt
3	DEVICE_INT_EN	R/W	0x0	Enable local interrupts. ESD event counter, TEMP sensor, Voltage sensor, line fault. Check status reg 0x87
2	REMOTE_INT_EN	R/W	0x0	Enable remote interrupts. Remote interrupts are captured in REG 0xA6 and 0xA7.
1	IE_FPD_TX1	R/W	0x0	FPD TX Port 1 Interrupt Enable interrupt from FPD TX Port 1
0	IE_FPD_TX0	R/W	0x0	FPD TX Port 0 Interrupt Enable interrupt from FPD TX Port 0

**7.6.1.77 INTERRUPT\_STS Register (Address = 0x52) [Default = 0x00]**INTERRUPT\_STS is shown in [Table 7-139](#).

Return to the [Summary Table](#).

**Table 7-139. INTERRUPT\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	GLOBAL_INT	R	0x0	Global Interrupt Enable. Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INTB_PIN_EN bit in the INTERRUPT_CTL register. Basically OR's the STS bits in this register only if corresponding IE* bit is set in INTERRUPT_CTL register
6	RESERVED	R	0x0	RESERVED
5	IS_DPHY_RX1	R	0x0	DPHY Port 1 Receiver Interrupt An interrupt has occurred for the DPHY Port 1.
4	IS_DPHY_RX0	R	0x0	DPHY Port 1 Receiver Interrupt An interrupt has occurred for the DPHY Port 0.
3	DEVICE_INT	R	0x0	Local device interrupts. REG 0x87
2	REMOTE_INT	R	0x0	remote GPIO interrupts. REG 0xA6; REG 0xA7 for status.
1	IS_FPD_TX1	R	0x0	FPD3 TX Port 1 Interrupt An interrupt has occurred for FPD TX Port 1 either in FPD3 or FPD4 datapath. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are FPD3_PORT_STS1, FPD4_PORT_STS1
0	IS_FPD_TX0	R	0x0	FPD3 TX Port 0 Interrupt An interrupt has occurred for FPD TX Port 0 either in FPD3 or FPD4 datapath. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are FPD3_PORT_STS0, FPD4_PORT_STS0

#### 7.6.1.78 AUDIO\_CFG Register (Address = 0x53) [Default = 0x22]

AUDIO\_CFG is shown in [Table 7-140](#).

Return to the [Summary Table](#).

**Table 7-140. AUDIO\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	TDM_2_I2S	R/W	0x0	Enable TDM to parallel I2S audio conversion: When this bit is set, the TDM to parallel I2S conversion is enabled. TDM audio data on the I2S_DA pin will be split onto four I2S data signals.
6	I2S_2_TDM	R/W	0x0	Enable Parallel I2S to TDM Audio conversion: Setting this bit to a 1 will enable TDM audio conversion for the I2S audio. Parallel I2S data on the I2S pins will be serialized onto a single I2S_DA signal for sending over the serial link.
5	AUDIO_MODE	R/W	0x1	Audio Mode: Selects source for audio to be sent over the FPD-Link III downstream link. 0x0= Reserved 0x1= I2S audio from I2S pins
4	RESERVED	R/W	0x0	Reserved
3	TDM_FS_MODE	R/W	0x0	TDM Frame Sync Mode: Sets active level for the Frame Sync for the TDM audio generator. The Frame Sync signal provides an active pulse to indicate the first sample data on the TDM data signal. 0x0= Active high Frame Sync 0x1= Active low Frame Sync (similar to I2S word select) This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.

**Table 7-140. AUDIO\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2	TDM_DELAY	R/W	0x0	TDM Data Delay: Controls data delay for TDM audio samples from the active Frame Sync edge. 0x0= Data is not delayed from Frame Sync (data is left justified) 0x1= Data is delayed 1 bit from Frame Sync This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
1:0	TDM_FS_WIDTH	R/W	0x2	TDM Frame Sync Width: Indicates width of TDM Frame Sync pulse for I2S to TDM conversion 00b= FS is 50/50 duty cycle 01b= FS is one slot/channel wide 1xb= FS is 1 clock pulse wide

**7.6.1.79 SPI\_TIMING1 Register (Address = 0x54) [Default = 0x22]**SPI\_TIMING1 is shown in [Table 7-141](#).Return to the [Summary Table](#).**Table 7-141. SPI\_TIMING1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	SPI_HOLD	R/W	0x2	SPI Data Hold from SPI clock: FPD-Link III only These bits set the minimum hold time for SPI data following the SPI clock sampling edge. In addition, this also sets the minimum active pulse width for the SPI output clock. Hold= (SPI_HOLD + 1) * 40ns For example, default setting of 2 will result in 120ns data hold time.
3:0	SPI_SETUP	R/W	0x2	SPI Data Setup to SPI Clock: FPD-Link III only These bits set the minimum setup time for SPI data to the SPI clock active edge. In addition, this also sets the minimum inactive width for the SPI output clock. Hold= (SPI_SETUP + 1) * 40ns For example, default setting of 2 will result in 120ns data setup time.

**7.6.1.80 SPI\_TIMING2 Register (Address = 0x55) [Default = 0x02]**SPI\_TIMING2 is shown in [Table 7-142](#).Return to the [Summary Table](#).**Table 7-142. SPI\_TIMING2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SPI_SS_SETUP	R/W	0x2	SPI Target Select Setup: FPD-Link III only This field controls the delay from assertion of the Target Select low to initial data timing. Delays are in units of 40ns. Delay= (SPI_SS_SETUP + 1) * 40ns

**7.6.1.81 SPI\_CONFIG Register (Address = 0x56) [Default = 0x00]**SPI\_CONFIG is shown in [Table 7-143](#).Return to the [Summary Table](#).

**Table 7-143. SPI\_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	SPI_CTRL_OVER	R	0x0	SPI Controller Overflow Detection: FPD-Link III only This flag is set if the SPI Controller detects an overflow condition. This occurs if the SPI Controller is unable to regenerate the remote SPI data at a fast enough rate to keep up with data arriving from the remote Deserializer. If this condition occurs, it suggests the SPI_SETUP and SPI_HOLD times should be set to smaller values. This flag is cleared by setting the SPI_CLR_OVER bit in this register.
6:3	RESERVED	R	0x0	Reserved
2	SPI_CLR_OVER	R/W	0x0	Clear SPI Controller Overflow Flag: FPD-Link III only Setting this bit to 1 will clear the SPI Controller Overflow Detection flag (SPI_CTRL_OVER). This bit is not self-clearing and must be set back to 0.
1	SPI_CPHA	R	0x0	SPI Clock Phase setting: FPD-Link III only Determines which phase of the SPI clock is used for sampling data. 0x0= Data sampled on leading (first) clock edge 0x1= Data sampled on trailing (second) clock edge This bit is read-only, with a value of 0. The DS90UH949 does not support CPHA of 1.
0	SPI_CPOL	R/W	0x0	SPI Clock Polarity setting: FPD-Link III only Determines the base (inactive) value of the SPI clock. 0x0= base value of the clock is 0 0x1= base value of the clock is 1 This bit affects both capture and propagation of SPI signals.

**7.6.1.82 FPD3\_STREAM\_SEL Register (Address = 0x57) [Default = 0x00]**FPD3\_STREAM\_SEL is shown in [Table 7-144](#).Return to the [Summary Table](#).

FPD-LINK III Video Stream Select

**Table 7-144. FPD3\_STREAM\_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1:0	FPD3_STREAM	R/W	0x0	FPD-Link III Stream Default: Port 0= 0x0 Port 1= 0x1 Selects the video processor stream to connect to the selected FPD3 transmitter. If device is in Independent or single FPD-Link III mode then PORT_SEL register determines which FPD-Link port this register modifies. In dual mode this register is not port specific. 0x0= Video Processor 0 0x1= Video Processor 1 0x2= Video Processor 2 0x3= Video Processor 3

**7.6.1.83 FPD3\_DUAL\_STS Register (Address = 0x58) [Default = 0x00]**FPD3\_DUAL\_STS is shown in [Table 7-145](#).Return to the [Summary Table](#).

FPD-LINK III Status. This register shows status for the selected FPD3 link. In Independent Mode,

**Table 7-145. FPD3\_DUAL\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	FPD3_LINK_RDY	R	0x0	FPD3 Link ready: This bit indicates that the FPD3 link has detected a valid downstream connection and determined capabilities for the downstream link.
6	FPD3_TX_STS	R	0x0	FPD3 Transmit status: This bit indicates that the FPD3 Transmitter is active and the receiver is locked to the transmit clock. It is only asserted once a valid input has been detected, and the FPD3 Transmit connection has entered the correct mode (i.e. Single vs Dual mode).
5:4	FPD3_PORT_STS	R	0x0	FPD3 Port Status: If FPD3_TX_STS is set to a 1, this field indicates the port mode status as follows: 0x0= Dual FPD-Link III Transmitter mode 0x1= Single FPD-Link III Transmit on port 0 0x2= Single FPD-Link III Transmit on port 1 0x3= FPD-Link III Transmit on both ports (Replicate or Splitter mode)
3:0	RESERVED	R	0x0	Reserved

**7.6.1.84 FPD3\_MODE\_CTL Register (Address = 0x59) [Default = 0x01]**FPD3\_MODE\_CTL is shown in [Table 7-146](#).Return to the [Summary Table](#).

FPD-LINK III Mode Control.

**Table 7-146. FPD3\_MODE\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	DUAL_ALIGN_DE	R/W	0x0	Dual Align on DE: In dual-link mode, if this bit is set to a 1, the odd/even data will be sent on the primary/secondary links respectively, based on the assertion of DE. If this bit is set to a 0, data will be sent on alternating links without regard to odd/even pixel position.
5	DISABLE_DUAL_SWAP	R/W	0x0	Disable Dual Swap: Prevents automatic correction of swapped Dual link connection. Setting this bit allows writes to the DUAL_SWAP control in the DUAL_CTL1 register
4	DUAL_SWAP	R/W	0x0	Dual Swap Control: Indicates current status of the Dual Swap control. If automatic correction of Dual Swap is disabled via the DISABLE_DUAL_SWAP control, this bit may be modified by software.
3	FORCE_LINK_RDY	R/W	0x0	Force Link Ready: Forces link ready indication, bypassing back channel link detection. To enable desired operation, it may be necessary to force the Deserializer capabilities registers (DES_CAP1 and DES_CAP2) for each port.

**Table 7-146. FPD3\_MODE\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2:0	FPD3_TX_MODE	R/W	0x1	FPD3 TX Mode: 'Strap 0x1= Single 0x3= Dual This register controls the operating mode of the FPD3 Transmit function. 0x0= Reserved 0x1= Forced Single Port 0 FPD-Link III Transmitter mode 0x2= Forced Single Port 1 FPD-Link III Transmitter mode 0x3= Forced Dual FPD-Link III Transmitter mode 0x4= Reserved 0x5= Forced Independent FPD3 mode 0x6= Reserved 0x7= Forced Splitter Mode (half of video stream on each port) Default value is set by the MODE_SEL0 pin

**7.6.1.85 FPD3\_DATAPATH\_CTL Register (Address = 0x5A) [Default = 0x02]**FPD3\_DATAPATH\_CTL is shown in [Table 7-147](#).Return to the [Summary Table](#).

FPD-LINK III Datapath Control. This configures the selected FPD3 link

**Table 7-147. FPD3\_DATAPATH\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	PASS_RGB	R/W	0x0	FPD-Link III only Setting this bit causes RGB data to be sent independent of DE in DS90UH981, which can be used to allow DS90UH981 to interoperate with DS90UB926, DS90UB928, DS90UB940, and DS90UB948. However, setting this bit prevents HDCP operation and blocks packetized audio. 1: Pass RGB data independent of DE 0: Block RGB data when DE is deasserted
5	DE_POLARITY	R/W	0x0	FPD-Link III only This bit indicates the polarity of the DE (Data Enable) signal. 0x0= DE is positive (active high, idle low) 0x1= DE is inverted (active low, idle high)
4	RESERVED	R/W	0x0	Reserved
3	I2S_TRANSPORT_SEL	R/W	0x0	FPD-Link III only 0x0= Enable I2S Data Island Transport 0x1= Enable I2S Data Forward Channel Frame Transport
2	VIDEO_18B_EN	R/W	0x0	FPD-Link III only 18-bit Video Select 0x0= Select 24-bit video mode 0x1= Select 18-bit video mode
1:0	I2S_MODE	R/W	0x2	FPD-Link III only I2S Channel Mode 0x0= 2-channel I2S audio 0x1= 4-channel I2S audio 0x2= 5.1- or 7.1-channel surround audio is enabled 0x3= Reserved Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

**7.6.1.86 FPD3\_FIFO\_CFG Register (Address = 0x5B) [Default = 0x23]**FPD3\_FIFO\_CFG is shown in [Table 7-148](#).Return to the [Summary Table](#).**Table 7-148. FPD3\_FIFO\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	FPD3_ALIGN_ERR THR	R/W	0x2	FPDLink-III Channel Alignment Error Threshold This field configures the threshold for flagging an error in FPDLink-III channel alignment. If the FPDLink-III Channel Alignment (FPD3_CHAN_ALIGN) magnitude is greater than this value, an error will be flagged in FPD3_CHAN_ALIGN_ERR.
3	ENABLE_FPD3_FIFO	R/W	0x0	Enable 35- to 40-bit FIFO This bit enables the 35- to 40-bit FIFOs.
2:0	FPD3_FIFO_DRAIN	R/W	0x3	Drain threshold for 35- to 40-bit FIFOs in 40-bit words This field configures the number of 40-bit words available in the 35-bit to 40-bit FIFO at which to start draining the FIFO. Valid values are 0-3; values above 3 will likely cause FIFO overruns. A value of 7 is invalid.

**7.6.1.87 FPD3\_FIFO\_STS Register (Address = 0x5C) [Default = 0x00]**FPD3\_FIFO\_STS is shown in [Table 7-149](#).Return to the [Summary Table](#).**Table 7-149. FPD3\_FIFO\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	FPD3_CHAN_ALIGN_ER	R/WC	0x0	FPD-Link III Channel Alignment Error This bit indicates an error in alignment between the two FPDLink-III channels.
3:0	RESERVED	R	0x0	Reserved

**7.6.1.88 FC\_POWERDOWN\_CTL Register (Address = 0x62) [Default = 0x00]**FC\_POWERDOWN\_CTL is shown in [Table 7-150](#).Return to the [Summary Table](#).**Table 7-150. FC\_POWERDOWN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	PD_FCTX	R/W	0x0	Override Value for powering down the FC transmitter
2	PD_FCTX_OV	R/W	0x0	Override enable for powering down the FC transmitter
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

**7.6.1.89 BC\_POWERDOWN\_CTL Register (Address = 0x63) [Default = 0x00]**BC\_POWERDOWN\_CTL is shown in [Table 7-151](#).Return to the [Summary Table](#).

**Table 7-151. BC\_POWERDOWN\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PD_BCRX	R/W	0x0	Override Value for powering down the BC receiver
4	RESERVED	R/W	0x0	Reserved
3	RSTB_BC	R/W	0x0	Override Value for resetting the BC
2	RESERVED	R/W	0x0	Reserved
1	RSTB_BC_EARLY	R/W	0x0	Override Value for resetting the BC early signal
0	RESERVED	R/W	0x0	Reserved

**7.6.1.90 PGCTL Register (Address = 0x64) [Default = 0x08]**PGCTL is shown in [Table 7-152](#).Return to the [Summary Table](#).**Table 7-152. PGCTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 0x0: Checkerboard (White/Black) 0x1: White 0x2: Black 0x3: Red 0x4: Green 0x5: Blue 0x6: Horizontally Scaled Black to White 0x7: Horizontally Scaled Black to Red 0x8: Horizontally Scaled Black to Green 0x9: Horizontally Scaled Black to Blue 0xA: Vertically Scaled Black to White 0xB: Vertically Scaled Black to Red 0xC: Vertically Scaled Black to Green 0xD: Vertically Scaled Black to Blue 0xE: Custom color configured in PGRS, PGGS, PGBS registers 0xF: VCOM (Yellow, Cyan, Blue, Red) 0x10: Alternate VCOM (Blue, Cyan, Yellow, Red) 0x11: Custom Color Checkerboard (Custom/Black) 0x12: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 0x13: UNH-IOL MIPI D-PHY compliance test pattern 0x1A - 0x1F: Reserved
2	RESERVED	R/W	0x0	Reserved

**Table 7-152. PGCTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	<p>When PATGEN_LEGACY_ENB= 0,            Pattern generator, pattern checker and            forwarding enable encoding:            0x0= Disable pattern generator and pattern checker            0x1= Enable pattern generator            0x2= Enable pattern checker, do not forward patterns on to the RX            datapath            0x3= Enable pattern checker, forward patterns on to the RX datapath            When PAT_ENC_EN= 0x2 or PAT_ENC_EN= 0x3, the local pattern            generator is still enabled internally for comparison with incoming            video stream            When PAT_ENC_EN= 0x3, the local pattern generator 's patterns are            forwarded, not the incoming video stream            When PATGEN_LEGACY_ENB= 1,            PAT_ENC_EN[1]:            0x0= Disable pattern checker            0x1= Enable pattern checker            PAT_ENC_EN[0]:            0x0= Disable pattern generator            0x1= Enable pattern generator            Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]</p>

**7.6.1.91 PGCFG Register (Address = 0x65) [Default = 0x08]**PGCFG is shown in [Table 7-153](#).Return to the [Summary Table](#).**Table 7-153. PGCFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHK	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 0x0= Normal operation (each square is 1x1 pixel) 0x1= Scale checkered patterns by 4 (each square is 4x4 pixels) 0x2= Scale checkered patterns by 8 (each square is 8x8 pixels) 0x3= Scale checkered patterns by 16 (each square is 16x16 pixels)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 0x0= Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0x1= Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 0x2= Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 0x3= Reserved
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 0x0= The Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. 0x1= The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 0x0= Do not invert the color output. 0x1= Invert the color output.

**Table 7-153. PGCFG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 0x0= The Pattern Generator retains the current pattern. 0x1= The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register.

**7.6.1.92 PGIA Register (Address = 0x66) [Default = 0x00]**PGIA is shown in [Table 7-154](#).Return to the [Summary Table](#).**Table 7-154. PGIA Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

**7.6.1.93 PGID Register (Address = 0x67) [Default = 0x00]**PGID is shown in [Table 7-155](#).Return to the [Summary Table](#).**Table 7-155. PGID Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

**7.6.1.94 PGTSTDAT Register (Address = 0x69) [Default = 0x00]**PGTSTDAT is shown in [Table 7-156](#).Return to the [Summary Table](#).**Table 7-156. PGTSTDAT Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGBE register.
6	RESERVED	R	0x0	Reserved
5:0	PATGEN_TST_DATA	R	0x0	Test Data: This field contains the Debug Monitor output. See the Debug Monitor section of the Pattern Generator DDS for details.

**7.6.1.95 BC\_PROCESSING\_CFG Register (Address = 0x6A) [Default = 0x0A]**BC\_PROCESSING\_CFG is shown in [Table 7-157](#).Return to the [Summary Table](#).**Table 7-157. BC\_PROCESSING\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	BC_DOWNSAMPLING RATE	R/WStrap	0x0	Back channel down sampling rate 2'b00: downsampling rate 1 (10.8Gbps I/VI Strap) 2'b01: downsampling rate 2 (Default + All 40bit ADAS Strap + 6.75Gbps/3.375 I/VI Strap) 2'b10: downsampling rate 4 2'b11: downsampling rate 8
5	RESERVED	R/W	0x0	Reserved
4:0	RESERVED	R/W	0xA	Reserved

**7.6.1.96 ENH\_BC\_STS Register (Address = 0x6B) [Default = 0x00]**ENH\_BC\_STS is shown in [Table 7-158](#).Return to the [Summary Table](#).

BCC Status Register This register provides error status for the Bidirectional Control Channel.

**Table 7-158. ENH\_BC\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	ALIGN_ERR	R	0x0	Align Error Flag When ENH_BC_CHK_EN is set in ENH_BC_CHK register, then this bit will show the status the alignment error flag, This occurs if a valid K 28.5 code occurs in a different byte than expected,
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	VALID_K_CODE_ERR	R	0x0	Valid K Code Error Flag When ENH_BC_CHK_EN is set in ENH_BC_CHK register, then this bit will show the status of valid K code errors. This occurs when the K code is valid but not the K28.5 code that is expected.

**7.6.1.97 ENH\_BC\_CHK Register (Address = 0x6C) [Default = 0x00]**ENH\_BC\_CHK is shown in [Table 7-159](#).Return to the [Summary Table](#).

BCC Status Register This register provides error status for the Bidirectional Control Channel.

**Table 7-159. ENH\_BC\_CHK Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	ENH_BC_CHK_EN	R/W	0x0	Enables for enhanced back channel checks valid k code error and alignment error, see 0x6B[0] and 0x6B[3]
4	RESERVED	R/W	0x0	Reserved
3:2	LNK_DET_CNT	R/W	0x0	Link Detect Frame Count These bits chooses the number of frames needed before a valid link detect signal is sent

**Table 7-159. ENH\_BC\_CHK Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

**7.6.1.98 BCC\_STATUS Register (Address = 0x6D) [Default = 0x00]**BCC\_STATUS is shown in [Table 7-160](#).Return to the [Summary Table](#).**Table 7-160. BCC\_STATUS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	
5	RESERVED	R/WC	0x0	Reserved
4	BCC_CONTROLLER_ER_R_P3	R/WC	0x0	BCC Controller Error This flag indicates a back channel CRC error or loss of back channel Lock occurred while waiting for a response from the Deserializer while the BCC I2C Controller is active. This flag is cleared on read of this register.
3	BCC_CONTROLLER_TO_P3	R/WC	0x0	BCC Target Timeout Error This bit will be set if the BCC Watchdog Timer expires while waiting for a response from the Deserializer while the BCC I2C Controller is active. This flag is cleared on read of this register.
2	BCC_TARGET_ERR_P3	R/WC	0x0	BCC Target Error This flag indicates a back channel CRC error or loss of back channel Lock occurred while waiting for a response from the Deserializer while the BCC I2C Target is active. This flag is cleared on read of this register.
1	BCC_TARGET_TO_P3	R/WC	0x0	BCC Target Timeout Error This bit will be set if the BCC Watchdog Timer expires while waiting for a response from the Deserializer while the BCC I2C Target is active. This flag is cleared on read of this register.
0	BCC_RESP_ERR_P3	R/WC	0x0	This flag indicates an error has been detected in response to a command on the Bidirectional Control Channel. When the Serializer sends a control channel frame, the Deserializer should return the 8-bit data field in the subsequent response. The Serializer checks the returned data for errors, and will set this flag if an error is detected. This flag is cleared on read of this register.

**7.6.1.99 DATAPATH\_BC\_FC Register (Address = 0x6E) [Default = 0x80]**DATAPATH\_BC\_FC is shown in [Table 7-161](#).Return to the [Summary Table](#).**Table 7-161. DATAPATH\_BC\_FC Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved

**Table 7-161. DATAPATH\_BC\_FC Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2:0	BC_CONFIG_0	R/W	0x0	Back Channel Configuration 2'b00: 0 (Default, 6.75/3.375Gbps IBI Strap, ALL ADAS) 2'b01: 1 2'b10: 2 (10.8Gbps IBI Strap) 2'b11: 3

**7.6.1.100 FC\_BCC\_TEST Register (Address = 0x6F) [Default = 0x00]**FC\_BCC\_TEST is shown in [Table 7-162](#).Return to the [Summary Table](#).

Forward Channel BCC Test Register This register allows forcing error conditions on the Forward Channel BCC interface. This allows system testing of error handling.

**Table 7-162. FC\_BCC\_TEST Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FORCE_BCC_ERROR_P3	RH/W1S	0x0	Force an error on forward channel BCC frame Setting the FORCE_BCC_ERROR bit will cause an error to be forced on a forward channel BCC frame. The BCC_ERROR_SEL and BCC_FRAME_SEL fields in this register determine the type of error to be forced and which frame will include the error. This bit is self-clearing and will always return 0.
5:3	BCC_ERROR_SEL_P3	R/W	0x0	BCC Error Select The BCC Error Select determines which type of error is forced on a forward channel BCC frame. 0x0= No error 0x1= Force CRC Error 0x2= Force Sequence Error (skips one sequence number) 0x3= Drop BCC Frame (results in sequence error at Deserializer) 0x4= Force error on Data field (random bit 1 through 7) 0x5= Force error on Data field, bit 0 (RW bit if during Start command) 0x6 - 0x7= Reserved
2:0	BCC_FRAME_SEL_P3	R/W	0x0	BCC Frame Select The BCC Frame Select allows selection of the forward channel BCC frame which will include the error condition selected in the force control bits of this register. BCC transfers are sent in bytes for each block transferred. This value may be set in range of 0 to 7 to force an error on any of the first 8 bytes sent on the BCC forward channel.

**7.6.1.101 TARGET\_ID\_0 Register (Address = 0x70) [Default = 0x00]**TARGET\_ID\_0 is shown in [Table 7-163](#).Return to the [Summary Table](#).

Remote Target ID register 0 Each I2C target maintains its own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-163. TARGET\_ID\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ID0	R/W	0x0	7-bit Remote Target Device ID 0 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.

**Table 7-163. TARGET\_ID\_0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	RESERVED	R/W	0x0	Reserved

**7.6.1.102 TARGET\_ID\_1 Register (Address = 0x71) [Default = 0x00]**TARGET\_ID\_1 is shown in [Table 7-164](#).Return to the [Summary Table](#).

Remote Target ID register 1 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-164. TARGET\_ID\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ID1	R/W	0x0	7-bit Remote Target Device ID 1 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID1	R/W	0x0	Reserved

**7.6.1.103 TARGET\_ID\_2 Register (Address = 0x72) [Default = 0x00]**TARGET\_ID\_2 is shown in [Table 7-165](#).Return to the [Summary Table](#).

Remote Target ID register 2 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-165. TARGET\_ID\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ID2	R/W	0x0	7-bit Remote Target Device ID 2 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID2	R/W	0x0	Reserved

**7.6.1.104 TARGET\_ID\_3 Register (Address = 0x73) [Default = 0x00]**TARGET\_ID\_3 is shown in [Table 7-166](#).Return to the [Summary Table](#).

Remote Target ID register 3 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-166. TARGET\_ID\_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ID3	R/W	0x0	7-bit Remote Target Device ID 3 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.

**Table 7-166. TARGET\_ID\_3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	DEST_PKT_RXDIR_ID3	R/W	0x0	Reserved

**7.6.1.105 TARGET\_ID\_4 Register (Address = 0x74) [Default = 0x00]**TARGET\_ID\_4 is shown in [Table 7-167](#).Return to the [Summary Table](#).

Remote Target ID register 4 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-167. TARGET\_ID\_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ID4	R/W	0x0	7-bit Remote Target Device ID 4 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID4	R/W	0x0	Reserved

**7.6.1.106 TARGET\_ID\_5 Register (Address = 0x75) [Default = 0x00]**TARGET\_ID\_5 is shown in [Table 7-168](#).Return to the [Summary Table](#).

Remote Target ID register 5 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-168. TARGET\_ID\_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ID5	R/W	0x0	7-bit Remote Target Device ID 5 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID5	R/W	0x0	Reserved

**7.6.1.107 TARGET\_ID\_6 Register (Address = 0x76) [Default = 0x00]**TARGET\_ID\_6 is shown in [Table 7-169](#).Return to the [Summary Table](#).

Remote Target ID register 6 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-169. TARGET\_ID\_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ID6	R/W	0x0	7-bit Remote Target Device ID 6 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.

**Table 7-169. TARGET\_ID\_6 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	DEST_PKT_RXDIR_ID6	R/W	0x0	Reserved

**7.6.1.108 TARGET\_ID\_7 Register (Address = 0x77) [Default = 0x00]**TARGET\_ID\_7 is shown in [Table 7-170](#).Return to the [Summary Table](#).

Remote Target ID register 7 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-170. TARGET\_ID\_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ID7	R/W	0x0	7-bit Remote Target Device ID 7 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID7	R/W	0x0	Reserved

**7.6.1.109 TARGET\_ALIAS\_0 Register (Address = 0x78) [Default = 0x00]**TARGET\_ALIAS\_0 is shown in [Table 7-171](#).Return to the [Summary Table](#).

Remote Target Alias register 0 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-171. TARGET\_ALIAS\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID0	R/W	0x0	7-bit Remote Target Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID0	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer). This bit is grouped with ID0.

**7.6.1.110 TARGET\_ALIAS\_1 Register (Address = 0x79) [Default = 0x00]**TARGET\_ALIAS\_1 is shown in [Table 7-172](#).Return to the [Summary Table](#).

Remote Target Alias register 1 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-172. TARGET\_ALIAS\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID1	R/W	0x0	7-bit Remote Target Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID1 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID1	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer). This bit is grouped with ID1.

**7.6.1.111 TARGET\_ALIAS\_2 Register (Address = 0x7A) [Default = 0x00]**TARGET\_ALIAS\_2 is shown in [Table 7-173](#).Return to the [Summary Table](#).

Remote Target Alias register 2 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-173. TARGET\_ALIAS\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID2	R/W	0x0	7-bit Remote Target Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID2 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID2	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer). This bit is grouped with ID2

**7.6.1.112 TARGET\_ALIAS\_3 Register (Address = 0x7B) [Default = 0x00]**TARGET\_ALIAS\_3 is shown in [Table 7-174](#).Return to the [Summary Table](#).

Remote Target Alias register 3 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-174. TARGET\_ALIAS\_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID3	R/W	0x0	7-bit Remote Target Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID3 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID3	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer). This bit is grouped with ID3.

**7.6.1.113 TARGET\_ALIAS\_4 Register (Address = 0x7C) [Default = 0x00]**TARGET\_ALIAS\_4 is shown in [Table 7-175](#).Return to the [Summary Table](#).

Remote Target Alias register 4 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-175. TARGET\_ALIAS\_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID4	R/W	0x0	7-bit Remote Target Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID4 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID4	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID4.

**7.6.1.114 TARGET\_ALIAS\_5 Register (Address = 0x7D) [Default = 0x00]**

TARGET\_ALIAS\_5 is shown in [Table 7-176](#).

Return to the [Summary Table](#).

Remote Target Alias register 5 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-176. TARGET\_ALIAS\_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID5	R/W	0x0	7-bit Remote Target Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID5 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID5	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID5.

**7.6.1.115 TARGET\_ALIAS\_6 Register (Address = 0x7E) [Default = 0x00]**

TARGET\_ALIAS\_6 is shown in [Table 7-177](#).

Return to the [Summary Table](#).

Remote Target Alias register 6 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-177. TARGET\_ALIAS\_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID6	R/W	0x0	7-bit Remote Target Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID6 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID6	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID6.

**7.6.1.116 TARGET\_ALIAS\_7 Register (Address = 0x7F) [Default = 0x00]**

TARGET\_ALIAS\_7 is shown in [Table 7-178](#).

Return to the [Summary Table](#).

Remote Target Alias register 7 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-178. TARGET\_ALIAS\_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID7	R/W	0x0	7-bit Remote Target Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID7 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID7	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer). This bit is grouped with ID7.

**7.6.1.117 RX\_BKSV0 Register (Address = 0x80) [Default = 0x00]**

RX\_BKSV0 is shown in [Table 7-179](#).

Return to the [Summary Table](#).

**Table 7-179. RX\_BKSV0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	BKSV0	R	0x0	BKSV0: Value of byte0 of the Receiver KSV.

**7.6.1.118 RX\_BKSV1 Register (Address = 0x81) [Default = 0x00]**

RX\_BKSV1 is shown in [Table 7-180](#).

Return to the [Summary Table](#).

**Table 7-180. RX\_BKSV1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	BKSV1	R	0x0	BKSV1: Value of byte1 of the Receiver KSV.

**7.6.1.119 RX\_BKSV2 Register (Address = 0x82) [Default = 0x00]**

RX\_BKSV2 is shown in [Table 7-181](#).

Return to the [Summary Table](#).

**Table 7-181. RX\_BKSV2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	BKSV2	R	0x0	BKSV2: Value of byte2 of the Receiver KSV.

**7.6.1.120 RX\_BKSV3 Register (Address = 0x83) [Default = 0x00]**

RX\_BKSV3 is shown in [Table 7-182](#).

Return to the [Summary Table](#).

**Table 7-182. RX\_BKSV3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	BKSV3	R	0x0	BKSV3: Value of byte3 of the Receiver KSV.

**7.6.1.121 RX\_BKSV4 Register (Address = 0x84) [Default = 0x00]**RX\_BKSV4 is shown in [Table 7-183](#).Return to the [Summary Table](#).**Table 7-183. RX\_BKSV4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	BKSV4	R	0x0	BKSV4: Value of byte4 of the Receiver KSV.

**7.6.1.122 LOCAL\_INT\_STS Register (Address = 0x87) [Default = 0x00]**LOCAL\_INT\_STS is shown in [Table 7-184](#).Return to the [Summary Table](#).**Table 7-184. LOCAL\_INT\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	INTERRUPT_TEMP	R	0x0	interrupt status for temperature sensor
2	INTERRUPT_VOLT	R	0x0	interrupt status for voltage monitor
1	INTERRUPT_LINE_FAULT	R	0x0	interrupt status for line fault
0	INTERRUPT_ESD_EVEN	R	0x0	interrupt status for ESD event

**7.6.1.123 TARGET\_DEST\_0 Register (Address = 0x88) [Default = 0x00]**TARGET\_DEST\_0 is shown in [Table 7-185](#).Return to the [Summary Table](#).

Remote Target Destination register 0 Each I2C target maintains its own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-185. TARGET\_DEST\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination port selection
4	FIRST_DC_PSEL	R/W	0x0	First daisy-chain port routing selection. Used for daisy-chain to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chain length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1

**Table 7-185. TARGET\_DEST\_0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth

**7.6.1.124 TARGET\_DEST\_1 Register (Address = 0x89) [Default = 0x00]**TARGET\_DEST\_1 is shown in [Table 7-186](#).Return to the [Summary Table](#).

Remote Target Destination register 1 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-186. TARGET\_DEST\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination port selection
4	FIRST_DC_PSEL	R/W	0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11:3 remaining depth

**7.6.1.125 TARGET\_DEST\_2 Register (Address = 0x8A) [Default = 0x00]**TARGET\_DEST\_2 is shown in [Table 7-187](#).Return to the [Summary Table](#).

Remote Target Destination register 2 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-187. TARGET\_DEST\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination port selection
4	FIRST_DC_PSEL	R/W	0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1

**Table 7-187. TARGET\_DEST\_2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3	MID_DC_PSEL	R/W	0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11:3 remaining depth

**7.6.1.126 TARGET\_DEST\_3 Register (Address = 0x8B) [Default = 0x00]**TARGET\_DEST\_3 is shown in [Table 7-188](#).Return to the [Summary Table](#).

Remote Target Destination register 3 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-188. TARGET\_DEST\_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination port selection
4	FIRST_DC_PSEL	R/W	0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11:3 remaining depth

**7.6.1.127 TARGET\_DEST\_4 Register (Address = 0x8C) [Default = 0x00]**TARGET\_DEST\_4 is shown in [Table 7-189](#).Return to the [Summary Table](#).

Remote Target Destination register 4 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-189. TARGET\_DEST\_4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination port selection
4	FIRST_DC_PSEL	R/W	0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11:3 remaining depth

**7.6.1.128 TARGET\_DEST\_5 Register (Address = 0x8D) [Default = 0x00]**TARGET\_DEST\_5 is shown in [Table 7-190](#).Return to the [Summary Table](#).

Remote Target Destination register 5 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-190. TARGET\_DEST\_5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination port selection
4	FIRST_DC_PSEL	R/W	0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11:3 remaining depth

### 7.6.1.129 TARGET\_DEST\_6 Register (Address = 0x8E) [Default = 0x00]

TARGET\_DEST\_6 is shown in [Table 7-191](#).

Return to the [Summary Table](#).

Remote Target Destination register 6 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-191. TARGET\_DEST\_6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination port selection
4	FIRST_DC_PSEL	R/W	0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11:3 remaining depth

### 7.6.1.130 TARGET\_DEST\_7 Register (Address = 0x8F) [Default = 0x00]

TARGET\_DEST\_7 is shown in [Table 7-192](#).

Return to the [Summary Table](#).

Remote Target Destination register 7 Each I2C target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

**Table 7-192. TARGET\_DEST\_7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination port selection
4	FIRST_DC_PSEL	R/W	0x0	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1

**Table 7-192. TARGET\_DEST\_7 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	REMAINING_DEPTH	R/W	0x0	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11:3 remaining depth

**7.6.1.131 TX\_KSV0 Register (Address = 0x90) [Default = 0x00]**TX\_KSV0 is shown in [Table 7-193](#).Return to the [Summary Table](#).**Table 7-193. TX\_KSV0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_KSV0	R	0x0	TX_KSV0: Value of byte0 of the Transmitter KSV.

**7.6.1.132 TX\_KSV1 Register (Address = 0x91) [Default = 0x00]**TX\_KSV1 is shown in [Table 7-194](#).Return to the [Summary Table](#).**Table 7-194. TX\_KSV1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_KSV1	R	0x0	TX_KSV1: Value of byte1 of the Transmitter KSV.

**7.6.1.133 TX\_KSV2 Register (Address = 0x92) [Default = 0x00]**TX\_KSV2 is shown in [Table 7-195](#).Return to the [Summary Table](#).**Table 7-195. TX\_KSV2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_KSV2	R	0x0	TX_KSV2: Value of byte2 of the Transmitter KSV.

**7.6.1.134 TX\_KSV3 Register (Address = 0x93) [Default = 0x00]**TX\_KSV3 is shown in [Table 7-196](#).Return to the [Summary Table](#).**Table 7-196. TX\_KSV3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_KSV3	R	0x0	TX_KSV3: Value of byte3 of the Transmitter KSV.

**7.6.1.135 TX\_KSV4 Register (Address = 0x94) [Default = 0x00]**TX\_KSV4 is shown in [Table 7-197](#).Return to the [Summary Table](#).

**Table 7-197. TX\_KSV4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_KSV4	R	0x0	TX_KSV4: Value of byte4 of the Transmitter KSV.

**7.6.1.136 TX\_AN0 Register (Address = 0x98) [Default = 0x00]**TX\_AN0 is shown in [Table 7-198](#).Return to the [Summary Table](#).**Table 7-198. TX\_AN0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_AN0	R	0x0	TX_AN0: Value of byte0 of the Transmitter An value.

**7.6.1.137 TX\_AN1 Register (Address = 0x99) [Default = 0x00]**TX\_AN1 is shown in [Table 7-199](#).Return to the [Summary Table](#).**Table 7-199. TX\_AN1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_AN1	R	0x0	TX_AN1: Value of byte1 of the Transmitter An value.

**7.6.1.138 TX\_AN2 Register (Address = 0x9A) [Default = 0x00]**TX\_AN2 is shown in [Table 7-200](#).Return to the [Summary Table](#).**Table 7-200. TX\_AN2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_AN2	R	0x0	TX_AN2: Value of byte2 of the Transmitter An value.

**7.6.1.139 TX\_AN3 Register (Address = 0x9B) [Default = 0x00]**TX\_AN3 is shown in [Table 7-201](#).Return to the [Summary Table](#).**Table 7-201. TX\_AN3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_AN3	R	0x0	TX_AN3: Value of byte3 of the Transmitter An value.

**7.6.1.140 TX\_AN4 Register (Address = 0x9C) [Default = 0x00]**TX\_AN4 is shown in [Table 7-202](#).Return to the [Summary Table](#).**Table 7-202. TX\_AN4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_AN4	R	0x0	TX_AN4: Value of byte4 of the Transmitter An value.

**7.6.1.141 TX\_AN5 Register (Address = 0x9D) [Default = 0x00]**TX\_AN5 is shown in [Table 7-203](#).Return to the [Summary Table](#).**Table 7-203. TX\_AN5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_AN5	R	0x0	TX_AN5: Value of byte5 of the Transmitter An value.

**7.6.1.142 TX\_AN6 Register (Address = 0x9E) [Default = 0x00]**TX\_AN6 is shown in [Table 7-204](#).Return to the [Summary Table](#).**Table 7-204. TX\_AN6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_AN6	R	0x0	TX_AN6: Value of byte6 of the Transmitter An value.

**7.6.1.143 TX\_AN7 Register (Address = 0x9F) [Default = 0x00]**TX\_AN7 is shown in [Table 7-205](#).Return to the [Summary Table](#).**Table 7-205. TX\_AN7 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_AN7	R	0x0	TX_AN7: Value of byte7 of the Transmitter An value.

**7.6.1.144 RX\_BCAPS Register (Address = 0xA0) [Default = 0x13]**RX\_BCAPS is shown in [Table 7-206](#).Return to the [Summary Table](#).**Table 7-206. RX\_BCAPS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	REPEATER	R	0x0	Repeater: Indicates if the attached Receiver supports downstream connections. This bit is valid once the Bksv is ready as indicated by the BKSV_RDY bit in the HDCP
5	KSV_FIFO_RDY	R	0x0	KSV FIFO Ready: Indicates the receiver has built the list of attached KSVs and computed the verification value V'.
4	FAST_I2C	R	0x1	Fast I2C: The HDCP Receiver supports fast I2C. Since the I2C is embedded in the serial data, this bit is not relevant.
3:2	RESERVED	R	0x0	Reserved
1	FEATURES_1_1	R	0x1	1.1_Features: The HDCP Receiver supports the Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options.
0	FAST_REAUTH	R	0x1	Fast Reauthentication: The HDCP Receiver is capable of receiving (unencrypted) video signal during the session re-authentication.

### 7.6.1.145 RX\_BSTATUS0 Register (Address = 0xA1) [Default = 0x00]

RX\_BSTATUS0 is shown in [Table 7-207](#).

Return to the [Summary Table](#).

**Table 7-207. RX\_BSTATUS0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	MAX_DEVS_EXCEEDED	R	0x0	Maximum Devices Exceeded: Indicates a topology error was detected. Indicates the number of downstream devices has exceeded the depth of the Repeater's KSV FIFO.
6:0	DEVICE_COUNT	R	0x0	Device Count: Total number of attached downstream device. For a Repeater, this will indicate the number of downstream devices, not including the Repeater. For an HDCP Receiver that is not also a Repeater, this field will be 0.

### 7.6.1.146 RX\_BSTATUS1 Register (Address = 0xA2) [Default = 0x00]

RX\_BSTATUS1 is shown in [Table 7-208](#).

Return to the [Summary Table](#).

**Table 7-208. RX\_BSTATUS1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved: Write as 0, read as 0
3	MAX_CASC_EXCEEDED	R	0x0	Maximum Cascade Exceeded: Indicates a topology error was detected. Indicates that more than seven levels of repeaters have been cascaded together.
2:0	CASC_DEPTH	R	0x0	Cascade Depth: Indicates the number of attached levels of devices for the Repeater.

### 7.6.1.147 KSV\_FIFO Register (Address = 0xA3) [Default = 0x00]

KSV\_FIFO is shown in [Table 7-209](#).

Return to the [Summary Table](#).

**Table 7-209. KSV\_FIFO Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	RESERVED	R	0x0	KSV FIFO: Each read of the KSV FIFO returns one byte of the KSV FIFO list composed by the downstream Receiver.

### 7.6.1.148 GPIO\_INT\_CTL0 Register (Address = 0xA4) [Default = 0x00]

GPIO\_INT\_CTL0 is shown in [Table 7-210](#).

Return to the [Summary Table](#).

**Table 7-210. GPIO\_INT\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	GPIO_INT_CTL0	R/W	0x0	Enable Interrupt from GPIO [7:0]

**7.6.1.149 GPIO\_INT\_CTL1 Register (Address = 0xA5) [Default = 0x00]**GPIO\_INT\_CTL1 is shown in [Table 7-211](#).Return to the [Summary Table](#).**Table 7-211. GPIO\_INT\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5:0	GPIO_INT_CTL1	R/W	0x0	Enable Interrupt from GPIO [15:8] (GPIO[15:14] are reserved.)

**7.6.1.150 GPIO\_INT\_STS0 Register (Address = 0xA6) [Default = 0x00]**GPIO\_INT\_STS0 is shown in [Table 7-212](#).Return to the [Summary Table](#).**Table 7-212. GPIO\_INT\_STS0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	GPIO_INT_STS0	RW/WC	0x0	Interrupt Status from GPIO [7:0] Interrupt bit is asserted by rising edge of GPIO bit and Clear-on-Read.

**7.6.1.151 GPIO\_INT\_STS1 Register (Address = 0xA7) [Default = 0x00]**GPIO\_INT\_STS1 is shown in [Table 7-213](#).Return to the [Summary Table](#).**Table 7-213. GPIO\_INT\_STS1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	RW/WC	0x0	Reserved
5:0	GPIO_INT_STS1	RW/WC	0x0	Interrupt Status from GPIO [15:8] Interrupt bit is asserted by rising edge of GPIO bit and Clear-on-Read. (GPIO[15:14] are reserved)

**7.6.1.152 DSI\_DEVICE\_CFG Register (Address = 0xB0) [Default = 0x00]**DSI\_DEVICE\_CFG is shown in [Table 7-214](#).Return to the [Summary Table](#).**Table 7-214. DSI\_DEVICE\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved: Write as 0, read as 0
4	DSI1_LANE_REVERSE	R/W	0x0	Reverse lane order for DSI Port 1: 0: DSI Port 1 Lanes 3,2,1,0 inputs are mapped to Lanes 3,2,1,0 1: DSI Port 1 Lanes 3,2,1,0 inputs are mapped to Lanes 0,1,2,3
3:1	RESERVED	R	0x0	Reserved: Write as 0, read as 0
0	DSI0_LANE_REVERSE	R/W	0x0	Reverse lane order for DSI Port 0: 0: DSI Port 0 Lanes 3,2,1,0 inputs are mapped to Lanes 3,2,1,0 1: DSI Port 0 Lanes 3,2,1,0 inputs are mapped to Lanes 0,1,2,3

**7.6.1.153 DSI\_ERROR Register (Address = 0xB1) [Default = 0x00]**DSI\_ERROR is shown in [Table 7-215](#).Return to the [Summary Table](#).**Table 7-215. DSI\_ERROR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_ERROR	R	0x0	ORs all of the DSI error bits within the indirect registers. Will not clear on read. All of the error status bits must be cleared within the DSI indirect register Page_4 and Page_6. In Dual DSI or Independent DSI mode, this bit will indicate an error was detected on either DSI input. The optimal register read order for checking the DSI errors is to read this DSI_ERROR register first then check the error report registers for an error, then read the INTR_STS_DPHY_ERR_FIFO_OVR (0x24) and INTR_CTL_DSI_ERR (0x25) registers on Page_4 or Page_6 for other errors and to clear the error report registers.
6	DPHY_ERROR	R	0x0	OR of LANE_SYNC_ERROR and DPHY_LANE_ERROR from DSI indirect registers. Will not clear on read. In Dual DSI or Independent DSI mode, this bit will indicate an error was detected on either DPHY input.
5:0	RESERVED	R	0x0	Reserved

**7.6.1.154 REG\_I2C\_FLTR\_DEPTH\_HS Register (Address = 0xB9) [Default = 0x03]**REG\_I2C\_FLTR\_DEPTH\_HS is shown in [Table 7-216](#).Return to the [Summary Table](#).**Table 7-216. REG\_I2C\_FLTR\_DEPTH\_HS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REG_I2C_FLTR_DEPTH_HS	R/W	0x3	The filter depth for HS I2C Glitch Filter Depth. This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

**7.6.1.155 FPD\_TX\_ESD\_EVENT\_CNTR Register (Address = 0xBC) [Default = 0x40]**FPD\_TX\_ESD\_EVENT\_CNTR is shown in [Table 7-217](#).Return to the [Summary Table](#).**Table 7-217. FPD\_TX\_ESD\_EVENT\_CNTR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	ESD_EVENT_COUNTER_ENABLE	R/W	0x1	ESD Event Counter Enable At power up this register should be disabled and re-enabled to clear the effects of power supply transients Writing a 0 to this register will clear the ESD_EVENT_COUNTER register to 0.
5:0	ESD_EVENT_COUNTER	R	0x0	ESD Event Counter Displays the number of ESD events that have occurred

**7.6.1.156 VP\_DPHY\_SEL0 Register (Address = 0xBD) [Default = 0x00]**VP\_DPHY\_SEL0 is shown in [Table 7-218](#).Return to the [Summary Table](#).

**Table 7-218. VP\_DPHY\_SEL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:3	VP1_DPHY_SEL	R/W	0x0	Selects the output of DPHY to be presented as the outputs to VP1 0: Virtual Channel 0 input from DPHY0 1: Virtual Channel 1 input from DPHY0 2: Virtual Channel 2 input from DPHY0 3: Virtual Channel 3 input from DPHY0 4: Virtual Channel 0 input from DPHY1 5: Virtual Channel 1 input from DPHY1 6: Virtual Channel 2 input from DPHY1 7: Virtual Channel 3 input from DPHY1
2:0	VP0_DPHY_SEL	R/W	0x0	Selects the output of DPHY to be presented as the outputs to VP0 0: Virtual Channel 0 input from DPHY0 1: Virtual Channel 1 input from DPHY0 2: Virtual Channel 2 input from DPHY0 3: Virtual Channel 3 input from DPHY0 4: Virtual Channel 0 input from DPHY1 5: Virtual Channel 1 input from DPHY1 6: Virtual Channel 2 input from DPHY1 7: Virtual Channel 3 input from DPHY1

**7.6.1.157 VP\_DPHY\_SEL1 Register (Address = 0xBE) [Default = 0x00]**VP\_DPHY\_SEL1 is shown in [Table 7-219](#).Return to the [Summary Table](#).**Table 7-219. VP\_DPHY\_SEL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:3	VP3_DPHY_SEL	R/W	0x0	Selects the output of DPHY to be presented as the outputs to VP3 0: Virtual Channel 0 input from DPHY0 1: Virtual Channel 1 input from DPHY0 2: Virtual Channel 2 input from DPHY0 3: Virtual Channel 3 input from DPHY0 4: Virtual Channel 0 input from DPHY1 5: Virtual Channel 1 input from DPHY1 6: Virtual Channel 2 input from DPHY1 7: Virtual Channel 3 input from DPHY1
2:0	VP2_DPHY_SEL	R/W	0x0	Selects the output of DPHY to be presented as the outputs to VP2 0: Virtual Channel 0 input from DPHY0 1: Virtual Channel 1 input from DPHY0 2: Virtual Channel 2 input from DPHY0 3: Virtual Channel 3 input from DPHY0 4: Virtual Channel 0 input from DPHY1 5: Virtual Channel 1 input from DPHY1 6: Virtual Channel 2 input from DPHY1 7: Virtual Channel 3 input from DPHY1
7:0	RESERVED	R	0x0	Reserved

**7.6.1.158 DUAL\_VIDSYNC Register (Address = 0xBF) [Default = 0x00]**DUAL\_VIDSYNC is shown in [Table 7-220](#).Return to the [Summary Table](#).**Table 7-220. DUAL\_VIDSYNC Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved

**Table 7-220. DUAL\_VIDSYNC Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	DUAL_VIDSYNC_SLV	R/W	0x0	This device is a target in dual video sync mode: 1-target, 0-controller
0	DUAL_VIDSYNC_MODE	R/W	0x0	Video sync mode between dual SER/dual channels: 1- enabled, 0-disabled

**7.6.1.159 HDCP\_DBG Register (Address = 0xC0) [Default = 0x00]**HDCP\_DBG is shown in [Table 7-221](#).Return to the [Summary Table](#).**Table 7-221. HDCP\_DBG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	HDCP_I2C_TO_SPEED	R/W	0x0	HDCP I2C Timer Speedup: For diagnostic purposes allow speedup of the HDCP I2C Controller 1 second idle timer to 50us. Texas Instruments use only, should be marked as Reserved in datasheet.
6	HDCP_I2C_TO_DIS	R/W	0x0	HDCP I2C Timeout Disable: Setting this bit to a 1 will disable the bus timeout function in the HDCP I2C controller. When enabled, the bus timeout function allows the I2C controller to assume the bus is free if no signaling occurs for more than 1 second.
5	FORCE_RI_ERR	RH/W1S	0x0	Force RI Synchronization Error: Forces an Ri synchronization error by causing the HDCP Transmitter to not count a frame. Allows checking of the Ri synchronization process. This bit is self-clearing.
4	DIS_RI_SYNC	R/W	0x0	Disable RI Synchronization check: Ri is normally checked both before and after the start of frame 128. The check at frame 127 ensures synchronization between the two. Setting this bit to a 1 will disable the check at frame 127.
3	RGB_CHKSUM_EN	R/W	0x0	Enable RGB video line checksum: Enables sending of ones-complement checksum for each 8-bit RGB data channel following end of each video data line. When in FPD3 Mode, this bit must be enabled for correct CRC error accumulation.
2	FC_TESTMODE	R/W	0x0	Frame Counter Testmode: Speeds up frame counter used for Pj and Ri verification. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames.
1	TMR_SPEEDUP	R/W	0x0	Timer Speedup: Speed up HDCP authentication timers.
0	HDCP_I2C_FAST	R/W	0x0	HDCP I2C Fast Mode Enable Setting this bit to a 1 will enable the HDCP I2C Controller in the HDCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Controller will operate with Standard mode timing. This bit is mirrored in the IND_STS register

**7.6.1.160 HDCP\_DBG2 Register (Address = 0xC1) [Default = 0x00]**HDCP\_DBG2 is shown in [Table 7-222](#).Return to the [Summary Table](#).

**Table 7-222. HDCP\_DBG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	DBG_SEL	R/W	0x0	Test Mux select: Selects signals to be brought out on test output bus. Signals may be brought to external pins as well as the HDCP_TEST register. See the Test Interface section of the HDCP Transmit DDS for details.
3	DBG_FREERUN	R/W	0x0	Test Mux Freerun: Enables continuous output of test mux data. If set to 0, data will be sampled and held following setting of the DBG_SAMPLE register bit. Freerun operation is most useful for viewing on external pins. Sample/Hold is most useful for reading through the HDCP_TEST register.
2	DBG_SAMPLE	RH/W1S	0x0	Test Mux Sample/Hold: Enables sampling of the test mux data within its source clock domain. Guarantees valid data readback through the HDCP_TEST register. This bit is self-clearing.
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

**7.6.1.161 HDCP\_CFG Register (Address = 0xC2) [Default = 0x82]**HDCP\_CFG is shown in [Table 7-223](#).Return to the [Summary Table](#).**Table 7-223. HDCP\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	ENH_LV	R/W	0x1	Enable Enhanced Link Verification: Enables enhanced link verification. Allows checking of the encryption Pj value on every 16th frame. 0x0= Enhanced Link Verification disabled 0x1= Enhanced Link Verification enabled
6	HDCP_EESS	R/W	0x0	Enable Enhanced Encryption Status Signaling: Enables Enhanced Encryption Status Signaling (EESS) instead of the Original Encryption Status Signaling (OESS). 0x0= OESS mode enabled 0x1= EESS mode enabled
5	TX_RPTR	R/W	0x0	Transmit Repeater Enable: Enables the transmitter to act as a repeater. In this mode, the HDCP Transmitter incorporates the additional authentication steps required of an HDCP Repeater. 0x0= Transmit Repeater mode disabled 0x1= Transmit Repeater mode enabled
4:3	ENC_MODE	R/W	0x0	Encryption Control Mode: Determines mode for controlling whether encryption is required for video frames. 0x0= Enc_Authenticated 0x1= Enc_Reg_Control 0x2= Enc_Always 0x3= Enc_InBand_Control (per frame)
2	WAIT_100MS	R/W	0x0	Enable 100ms Wait: The HDCP 1.3 specification allows for a 100ms wait to allow the HDCP Receiver to compute the initial encryption values. The FPD-LinkIII implementation guarantees that the Receiver will complete the computations before the HDCP Transmitter. Thus the timer is unnecessary. To enable the 100ms timer, set this bit to a 1.
1	RX_DET_SEL	R/W	0x1	RX Detect Select: Controls assertion of the Receiver Detect Interrupt. If set to 0, the Receiver Detect Interrupt will be asserted on detection of an FPD-Link III Receiver. If set to 1, the Receiver Detect Interrupt will also require a receive lock indication from the receiver.

**Table 7-223. HDCP\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	HDCP_AVMUTE	R/W	0x0	Enable AVMUTE: Setting this bit to a 1 will initiate AVMUTE operation. The transmitter will ignore encryption status controls while in this state. If this bit is set to a 0, normal operation will resume. This bit may only be set if the HDCP_EESS bit is also set.

**7.6.1.162 HDCP\_CTL Register (Address = 0xC3) [Default = 0x00]**HDCP\_CTL is shown in [Table 7-224](#).Return to the [Summary Table](#).**Table 7-224. HDCP\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	HDCP_RST	RH/W1S	0x0	HDCP Reset: Setting this bit will reset the HDCP transmitter and disable HDCP authentication. This bit is self-clearing.
6	RESERVED	R	0x0	Reserved: Write as 0, read as 0.
5	KSV_LIST_VALID	RH/W1S	0x0	KSV List Valid: The controller sets this bit after validating the Repeater's KSV List against the Key revocation list. This allows completion of the Authentication process. This bit is self-clearing.
4	KSV_VALID	R/W	0x0	KSV Valid: The controller sets this bit after validating the Receiver's KSV against the Key revocation list. This allows continuation of the Authentication process. This bit will be cleared upon assertion of the KSV_RDY flag in the HDCP_STS register. Setting this bit to a 0 will have no effect.
3	HDCP_ENC_DIS	RH/W1S	0x0	HDCP Encrypt Disable: Disables HDCP encryption. Setting this bit to a 1 will cause video data to be sent without encryption. Authentication status will be maintained. This bit is self-clearing.
2	HDCP_ENC_EN	R/W	0x0	HDCP Encrypt Enable: Enables HDCP encryption. When set, if the device is authenticated, encrypted data will be sent. If device is not authenticated, a blue screen will be sent. Encryption should always be enabled when video data requiring content protection is being supplied to the transmitter. When this bit is not set, video data will be sent without encryption. Note that when CFG_ENC_MODE is set to Enc_Always, this bit will be read only with a value of 1.
1	HDCP_DIS	RH/W1S	0x0	HDCP Disable: Disables HDCP authentication. Setting this bit to a 1 will disable the HDCP authentication. This bit is self-clearing.
0	HDCP_EN	R/W	0x0	HDCP Enable/Restart: Enables HDCP authentication. If HDCP is already enabled, setting this bit to a 1 will restart authentication. Setting this bit to a 0 will have no effect. A register read will return the current HDCP enabled status.

**7.6.1.163 HDCP\_STS Register (Address = 0xC4) [Default = 0x00]**HDCP\_STS is shown in [Table 7-225](#).Return to the [Summary Table](#).

**Table 7-225. HDCP\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	I2C_ERR_DET	R/WC	0x0	HDCP I2C Error Detected: This bit indicates an error was detected on the embedded communications channel with the HDCP Receiver. Setting of this bit might indicate that a problem exists on the link between the HDCP Transmitter and HDCP Receiver. This bit will be cleared on read.
6	RX_INT	R	0x0	RX Interrupt: Status of the RX Interrupt signal. The signal is received from the attached HDCP Receiver and is the status on the INTB_IN pin of the HDCP Receiver. The signal is active low, so a 0 indicates an interrupt condition.
5	RX_LOCK_DET	R	0x0	Receiver Lock Detect: This bit indicates that the downstream Receiver has indicated Receive Lock to incoming serial data.
4	DOWN_HPD	R/WC	0x0	Downstream Hot Plug Detect: This bit indicates a downstream repeater has reported a Hot Plug event, indicating addition of a new receiver. This bit will be cleared on read.
3	RX_DETECT	R	0x0	Receiver Detect: This bit indicates that a downstream Receiver has been detected.
2	KSV_LIST_RDY	R	0x0	HDCP Repeater KSV List Ready: This bit indicates that the Receiver KSV list has been read and is available in the KSV_FIFO registers. The device will wait for the controller to set the KSV_LIST_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_LIST_VALID bit.
1	KSV_RDY	R	0x0	HDCP Receiver KSV Ready: This bit indicates that the Receiver KSV has been read and is available in the HDCP_BKSV registers. If the device is not a Repeater, it will wait for the controller to set the KSV_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_VALID bit.
0	AUTHED	R	0x0	HDCP Authenticated: Indicates the HDCP authentication has completed successfully. The controller may now send video data requiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authentication.

**7.6.1.164 FPD3\_ICR Register (Address = 0xC6) [Default = 0x00]**FPD3\_ICR is shown in [Table 7-226](#).Return to the [Summary Table](#).**Table 7-226. FPD3\_ICR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	IE_RXDET_INT	R/W	0x0	Interrupt on Receiver Detect: Enables interrupt on detection of a downstream Receiver. If LINK_CFG[3] (RX_DET_SEL) is set to a 1, the interrupt will wait for Receiver Lock Detect.
5	IE_RX_Rem_INT	R/W	0x0	Interrupt on Receiver interrupt: Enables interrupt on indication from the downstream receiver. Allows propagation of interrupts from downstream devices.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved

**Table 7-226. FPD3\_ICR Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	INT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.

**7.6.1.165 FPD3\_ISR Register (Address = 0xC7) [Default = 0x00]**FPD3\_ISR is shown in [Table 7-227](#).Return to the [Summary Table](#).**Table 7-227. FPD3\_ISR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_RXDET_INT	R	0x0	Interrupt on Receiver Detect interrupt: A downstream receiver has been detected. If if LINK_CFG[3] (RX_DET_SEL) is set to a 1, the interrupt will wait for Receiver Lock Detect.
5	IS_RXREM_INT	R	0x0	Interrupt on Receiver interrupt: Receiver has indicated an interrupt request from downstream device.
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	INT	R	0x0	Global Interrupt: Set if any enabled interrupt is indicated.

**7.6.1.166 NVM\_CTL Register (Address = 0xC8) [Default = 0x00]**NVM\_CTL is shown in [Table 7-228](#).Return to the [Summary Table](#).**Table 7-228. NVM\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7	NVM_PASS	R	0x0	NVM Verify pass: This bit indicates the completion status of the NVM verification process. This bit is valid only when NVM_DONE is asserted. 0x0= NVM Verify failed 0x1= NVM Verify passed
6	NVM_DONE	R	0x0	NVM Verify done: This bit indicates that the NVM Verification has completed.
5	RESERVED	R/W	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2	NVM_VFY	R/W	0x0	NVM Verify: Setting this bit will enable a verification of the NVM contents. This is done by reading all NVM keys, computing a SHA-1 hash value, and verifying against the SHA-1 hash stored in NVM. This bit will be cleared upon completion of the NVM Verification.
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

**7.6.1.167 HDCP\_CFG2 Register (Address = 0xCD) [Default = 0x02]**HDCP\_CFG2 is shown in [Table 7-229](#).

Return to the [Summary Table](#).

**Table 7-229. HDCP\_CFG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	RPULSE_EN	R/W	0x1	Enable Rising Edge Pulse Enable for Receiver Detect Interrupt: Enables an interrupt pulse for the Receiver Detect Interrupt on the rising edge of the signal. This affects both the rx lock detect and rx link detect select options for the receiver detect interrupt. Both RPULSE_EN and FPULSE_EN can be enabled at the same time to generate an interrupt on both edges 0x0= rising edge pulse disabled 0x1= rising edge pulse enabled
0	FPULSE_EN	R/W	0x0	Enable Falling Edge Pulse Enable for Receiver Detect Interrupt: Enables an interrupt pulse for the Receiver Detect Interrupt on the falling edge of the signal. This affects both the rx lock detect and rx link detect select options for the receiver detect interrupt. Both RPULSE_EN and FPULSE_EN can be enabled at the same time to generate an interrupt on both edges 0x0= falling edge pulse disabled 0x1= falling edge pulse enabled

**7.6.1.168 BLUE\_SCREEN Register (Address = 0xCE) [Default = 0xFF]**

BLUE\_SCREEN is shown in [Table 7-230](#).

Return to the [Summary Table](#).

**Table 7-230. BLUE\_SCREEN Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	BLUE_SCREEN_VAL	R/W	0xFF	Blue Screen Data Value: Provides the 8-bit data value sent on the Blue channel when the HDCP Transmitter is sending a blue screen.

**7.6.1.169 IND\_STS Register (Address = 0xD0) [Default = 0x00]**

IND\_STS is shown in [Table 7-231](#).

Return to the [Summary Table](#).

**Table 7-231. IND\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IA_RST	R/W	0x0	Indirect Access Reset: Setting this bit to a 1 will reset the I2C Controller in the HDCP Receiver. As this may leave the I2C bus in an indeterminate state, it should only be done if the Indirect Access mechanism is not able to complete due to an error on the destination I2C bus.
6	RESERVED	R/W	0x0	Reserved
5	I2C_TO_DIS	R/W	0x0	I2C Timeout Disable: Setting this bit to a 1 will disable the bus timeout function in the I2C controller. When enabled, the bus timeout function allows the I2C controller to assume the bus is free if no signaling occurs for more than 1 second.
4	I2C_FAST	R/W	0x0	I2C Fast mode Enable: Setting this bit to a 1 will enable the I2C Controller in the HDCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Controller will operate with Standard mode timing.
3	RESERVED	R	0x0	
2	RESERVED	R	0x0	Reserved

**Table 7-231. IND\_STS Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	IA_ACK	R	0x0	Indirect Access Acknowledge: The acknowledge bit indicates that a valid acknowledge was received upon completion of the indirect read or write to the target. A value of 0 indicates the read/write did not complete successfully.
0	IA_DONE	R	0x0	Indirect Access Done: Set to a 1 to indicate completion of Indirect Register Access. This bit will be cleared or read or by start of a new Indirect Register Access.

**7.6.1.170 IND\_SAR Register (Address = 0xD1) [Default = 0x00]**IND\_SAR is shown in [Table 7-232](#).Return to the [Summary Table](#).**Table 7-232. IND\_SAR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	IA_SADDR	R/W	0x0	Indirect Access Target Address: (HDCP Receiver Only) This field should be programmed with the target address for the I2C target to be accessed.
0	IA_RW	R/W	0x0	Indirect Access Read/Write: (HDCP Receiver Only) 0x0= Write 0x1= Read

**7.6.1.171 IND\_OAR Register (Address = 0xD2) [Default = 0x00]**IND\_OAR is shown in [Table 7-233](#).Return to the [Summary Table](#).**Table 7-233. IND\_OAR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IA_OFFSET	R/W	0x0	Indirect Access Offset: (HDCP Receiver Only) This field should be programmed with the register address for the I2C indirect access.

**7.6.1.172 IND\_DATA Register (Address = 0xD3) [Default = 0x00]**IND\_DATA is shown in [Table 7-234](#).Return to the [Summary Table](#).**Table 7-234. IND\_DATA Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IA_DATA	R/W	0x0	Indirect Access Data: (HDCP Receiver Only) For an indirect write, this field should be written with the write data. For an indirect read, this field will contain the result of a successful read.

**7.6.1.173 LINK\_CFG\_ALIAS Register (Address = 0xE2) [Default = 0x00]**LINK\_CFG\_ALIAS is shown in [Table 7-235](#).Return to the [Summary Table](#).

**Table 7-235. LINK\_CFG\_ALIAS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LINK_CFG	R	0x0	Read-only alias of LINK_CFG register

**7.6.1.174 HDCP\_CTL\_ALIAS Register (Address = 0xE3) [Default = 0x00]**HDCP\_CTL\_ALIAS is shown in [Table 7-236](#).Return to the [Summary Table](#).**Table 7-236. HDCP\_CTL\_ALIAS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	HDCP_CTL	R	0x0	Read-only alias of HDCP_CTL register

**7.6.1.175 FPD3\_STS\_ALIAS Register (Address = 0xE4) [Default = 0x00]**FPD3\_STS\_ALIAS is shown in [Table 7-237](#).Return to the [Summary Table](#).**Table 7-237. FPD3\_STS\_ALIAS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	FPD3_STS	R	0x0	Read-only alias of FPD3_STS register

**7.6.1.176 HDCP\_TEST\_ALIAS Register (Address = 0xE5) [Default = 0x00]**HDCP\_TEST\_ALIAS is shown in [Table 7-238](#).Return to the [Summary Table](#).**Table 7-238. HDCP\_TEST\_ALIAS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	HDCP_TEST	R	0x0	Read-only alias of HDCP_TEST register

**7.6.1.177 FPD3\_ICR\_ALIAS Register (Address = 0xE6) [Default = 0x00]**FPD3\_ICR\_ALIAS is shown in [Table 7-239](#).Return to the [Summary Table](#).**Table 7-239. FPD3\_ICR\_ALIAS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	FPD3_ICR	R	0x0	Read-only alias of FPD3_ICR register

**7.6.1.178 FPD3\_ISR\_ALIAS Register (Address = 0xE7) [Default = 0x00]**FPD3\_ISR\_ALIAS is shown in [Table 7-240](#).Return to the [Summary Table](#).**Table 7-240. FPD3\_ISR\_ALIAS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	FPD3_ISR	R	0x0	Read-only alias of FPD3_ISR register

**7.6.1.179 HDCP\_CFG2\_ALIAS Register (Address = 0xE9) [Default = 0x00]**HDCP\_CFG2\_ALIAS is shown in [Table 7-241](#).Return to the [Summary Table](#).**Table 7-241. HDCP\_CFG2\_ALIAS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	HDCP_CFG2	R	0x0	Read-only alias of HDCP_CFG2 register

**7.6.1.180 TX\_ID0 Register (Address = 0xF0) [Default = 0x5F]**TX\_ID0 is shown in [Table 7-242](#).Return to the [Summary Table](#).**Table 7-242. TX\_ID0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_ID0	R	0x5F	TX_ID0: First byte ID code, '_'

**7.6.1.181 TX\_ID1 Register (Address = 0xF1) [Default = 0x55]**TX\_ID1 is shown in [Table 7-243](#).Return to the [Summary Table](#).**Table 7-243. TX\_ID1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_ID1	R	0x55	TX_ID1: 2nd byte of ID code, 'U'

**7.6.1.182 TX\_ID2 Register (Address = 0xF2) [Default = 0x48]**TX\_ID2 is shown in [Table 7-244](#).Return to the [Summary Table](#).**Table 7-244. TX\_ID2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_ID2	R	0x48	TX_ID2: 3rd byte of ID code. Value will be either 'B' or 'H'. 'H' indicates an HDCP capable device. UB= 0x42 UH= 0x48

**7.6.1.183 TX\_ID3 Register (Address = 0xF3) [Default = 0x39]**TX\_ID3 is shown in [Table 7-245](#).Return to the [Summary Table](#).**Table 7-245. TX\_ID3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_ID3	R	0x39	TX_ID3: 4th byte of ID code, '9'

**7.6.1.184 TX\_ID4 Register (Address = 0xF4) [Default = 0x38]**TX\_ID4 is shown in [Table 7-246](#).

Return to the [Summary Table](#).

**Table 7-246. TX\_ID4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_ID4	R	0x38	TX_ID4: 5th byte of ID code, '8'

**7.6.1.185 TX\_ID5 Register (Address = 0xF5) [Default = 0x33]**

TX\_ID5 is shown in [Table 7-247](#).

Return to the [Summary Table](#).

**Table 7-247. TX\_ID5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TX_ID5	R	0x33	TX_ID5: 6th byte of ID code, '1'

**7.6.1.186 HDCP\_TX\_ID6 Register (Address = 0xF6) [Default = 0x30]**

HDCP\_TX\_ID6 is shown in [Table 7-248](#).

Return to the [Summary Table](#).

**Table 7-248. HDCP\_TX\_ID6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	HDCP_TX_ID6	R	0x30	HDCP_TX_ID5: 6th byte of ID code, '0'

**7.6.1.187 IND\_REG\_I2C\_CTL0 Register (Address = 0xF8) [Default = 0x00]**

IND\_REG\_I2C\_CTL0 is shown in [Table 7-249](#).

Return to the [Summary Table](#).

**Table 7-249. IND\_REG\_I2C\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	IND_ACC_SEL0	R/W	0x0	<p>Indirect Access Register Select:  Selects target page for register access  0000: Disabled  0001: FPD Ports 0-1 registers  0010: FPD PLL 0-1 registers  0011: Reserved  0100: DPHY P0 Digital Registers  0101: Reserved  0110: DPHY P1 Digital Registers  0111: Reserved  1000: ADAS compatibility Registers  1001: DFT Registers  1010: Reserved  1011: Link Layer Registers  1100: Video Processor 0/1/2/3 Registers  1101: Reserved  1110: ADC Control Registers  1111: Reserved</p> <p>NOTE: This register acts the same way as the PORT_SEL, where there is separate register for each target and each controller, in order to stop one target/controller from affecting the access of another target/controller.</p>

**7.6.1.188 IND\_REG\_I2C\_ID0 Register (Address = 0xF9) [Default = 0x00]**IND\_REG\_I2C\_ID0 is shown in [Table 7-250](#).Return to the [Summary Table](#).**Table 7-250. IND\_REG\_I2C\_ID0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	IND_I2C_ID0	R/W	0x0	7-bit address for use to directly access the indirect register page listed in IND_REG_I2C_CTL0; The address of 7'h00 is considered disabled and will not be recognised. This address cannot be the DEVICE_ID as in I2C_DEVICE_ID, or any of the other IND_I2C_IDX addresses.
0	RESERVED	R	0x0	Reserved

**7.6.1.189 IND\_REG\_I2C\_CTL1 Register (Address = 0xFA) [Default = 0x00]**IND\_REG\_I2C\_CTL1 is shown in [Table 7-251](#).Return to the [Summary Table](#).**Table 7-251. IND\_REG\_I2C\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	IND_ACC_SEL1	R/W	0x0	Indirect Access Register Select: Selects target page for register access 0000: Disabled 0001: FPD Ports 0-1 registers 0010: FPD PLL 0-1 registers 0011: Reserved 0100: DPHY P0 Digital Registers 0101: Reserved 0110: DPHY P1 Digital Registers 0111: Reserved 1000: ADAS compatibility Registers 1001: Registers 1010: Reserved 1011: Link Layer Registers 1100: Video Processor 0/1/2/3 Registers 1101: Reserved 1110: ADC Control Registers 1111: Reserved NOTE: This register acts the same way as the PORT_SEL, where there is separate register for each target and each controller, in order to stop one target/controller from affecting the access of another target/controller.

**7.6.1.190 IND\_REG\_I2C\_ID1 Register (Address = 0xFB) [Default = 0x00]**IND\_REG\_I2C\_ID1 is shown in [Table 7-252](#).Return to the [Summary Table](#).**Table 7-252. IND\_REG\_I2C\_ID1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	IND_I2C_ID1	R/W	0x0	7-bit address for use to directly access the indirect register page listed in IND_REG_I2C_CTL1; The address of 7'h00 is considered disabled and will not be recognised. This address cannot be the DEVICE_ID as in I2C_DEVICE_ID, or any of the other IND_I2C_IDX addresses.
0	RESERVED	R	0x0	Reserved

**7.6.1.191 IND\_REG\_I2C\_CTL2 Register (Address = 0xFC) [Default = 0x00]**IND\_REG\_I2C\_CTL2 is shown in [Table 7-253](#).Return to the [Summary Table](#).**Table 7-253. IND\_REG\_I2C\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	IND_ACC_SEL2	R/W	0x0	<p>Indirect Access Register Select:  Selects target page for register access  0000: Disabled  0001: FPD Ports 0-1 registers  0010: FPD PLL 0-1 registers  0011: Reserved  0100: DPHY P0 Digital Registers  0101: Reserved  0110: DPHY P1 Digital Registers  0111: Reserved  1000: ADAS compatibility Registers  1001: DFT Registers  1010: Reserved  1011: Link Layer Registers  1100: Video Processor 0/1/2/3 Registers  1101: Reserved  1110: ADC Control Registers  1111: Reserved</p> <p>NOTE: This register acts the same way as the PORT_SEL, where there is separate register for each target and each controller, in order to stop one target/controller from affecting the access of another target/controller.</p>

**7.6.1.192 IND\_REG\_I2C\_ID2 Register (Address = 0xFD) [Default = 0x00]**IND\_REG\_I2C\_ID2 is shown in [Table 7-254](#).Return to the [Summary Table](#).**Table 7-254. IND\_REG\_I2C\_ID2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	IND_I2C_ID2	R/W	0x0	7-bit address for use to directly access the indirect register page listed in IND_REG_I2C_CTL2; The address of 7'h00 is considered disabled and will not be recognised. This address cannot be the DEVICE_ID as in I2C_DEVICE_ID, or any of the other IND_I2C_IDX addresses.
0	RESERVED	R	0x0	Reserved

**7.6.1.193 IND\_REG\_I2C\_CTL3 Register (Address = 0xFE) [Default = 0x00]**IND\_REG\_I2C\_CTL3 is shown in [Table 7-255](#).Return to the [Summary Table](#).**Table 7-255. IND\_REG\_I2C\_CTL3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved

**Table 7-255. IND\_REG\_I2C\_CTL3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4:0	IND_ACC_SEL3	R/W	0x0	<p>Indirect Access Register Select:  Selects target page for register access  0000: Disabled  0001: FPD Ports 0-1 registers  0010: FPD PLL 0-1 registers  0011: Reserved  0100: DPHY P0 Digital Registers  0101: Reserved  0110: DPHY P1 Digital Registers  0111: Reserved  1000: ADAS compatibility Registers  1001: DFT Registers  1010: Reserved  1011: Link Layer Registers  1100: Video Processor 0/1/2/3 Registers  1101: Reserved  1110: ADC Control Registers  1111: Reserved</p> <p>NOTE: This register acts the same way as the PORT_SEL, where there is separate register for each target and each controller, in order to stop one target/controller from affecting the access of another target/controller.</p>

**7.6.1.194 IND\_REG\_I2C\_ID3 Register (Address = 0xFF) [Default = 0x00]**IND\_REG\_I2C\_ID3 is shown in [Table 7-256](#).Return to the [Summary Table](#).**Table 7-256. IND\_REG\_I2C\_ID3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	IND_I2C_ID3	R/W	0x0	<p>7-bit address for use to directly access the indirect register page listed in IND_REG_I2C_CTL3;  The address of 7'h00 is considered disabled and will not be recognised. This address cannot be the DEVICE_ID as in I2C_DEVICE_ID, or any of the other IND_I2C_IDX addresses.</p>
0	RESERVED	R	0x0	Reserved

## 7.6.2 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map ([Table 7-257](#)). Register access is provided via an indirect access mechanism through the Indirect Access registers (IND\_ACC\_CTL, IND\_ACC\_ADDR, and IND\_ACC\_DATA). These registers are located at offsets 0x40-0x42 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the IND\_ACC\_CTL register to select the desired register block
2. Write to the IND\_ACC\_ADDR register to set the register offset
3. Write the data value to the IND\_ACC\_DATA register

If auto-increment is set in the IND\_ACC\_CTL register, repeating Step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the IND\_ACC\_CTL register to select the desired register block
2. Write to the IND\_ACC\_ADDR register to set the register offset
3. Read from the IND\_ACC\_DATA register

If auto-increment is set in the IND\_ACC\_CTL register, repeating Step 3 will read additional data bytes from subsequent register offset locations.

**Table 7-257. Indirect Register Map Description**

IA SELECT 0x40[5:2]	PAGE/BLOCK	INDIRECT REGISTERS	DESCRIPTION
0000	0	Reserved	Reserved
0001	1	Page_1: FPD Port	FPD Port Registers
0010	2	Page_2: FPD PLL	PLL Control Registers
0011	3	Reserved	Reserved
0100	4	Page_4: D-PHY Digital Port 0	DSI 0 Control Registers
0101	5	Page_5: D-PHY Analog Port 0	D-PHY Analog Port 0
0110	6	Page_6: D-PHY Digital Port 1	DSI 1 Control Registers
0111	7	Page_7: D-PHY Analog Port 1	D-PHY Analog Port 1
1000	8	Page_8: ADAS Compatability	ADAS Compatability Registers
1001	9	Page_9: DFT Registers	Reserved
1010	10	Reserved	Reserved
1011	11	Page_11: Link Layer Registers	Video Stream Registers
1100	12	Page_12: Video Processor Registers	Video Processor 0/1/2/3 Registers
1101	13	Reserved	Reserved
1110	14	Page_14: ADC Control	ADC control Registers

### 7.6.2.1 Page\_1\_FPD\_Port Registers

[Table 7-258](#) lists the memory-mapped registers for the Page\_1\_FPD\_Port registers. All register offset addresses not listed in [Table 7-258](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-258. PAGE\_1\_FPD\_PORT Registers**

Address	Acronym	Register Name	Section
0x0	INVERT_POLARITY_PORT0_SE	INVERT_POLARITY_PORT0_SEGO G0	Go

**Table 7-258. PAGE\_1\_FPD\_PORT Registers (continued)**

Address	Acronym	Register Name	Section
0x1	INVERT_POLARITY_PORT0_SE G1	INVERT_POLARITY_PORT0_SEG1	Go
0x2	INVERT_POLARITY_PORT0_SE G2	INVERT_POLARITY_PORT0_SEG2	Go
0x6	CH0_BC_SETTING_1	CH0_BC_SETTING_1	Go
0xD	CH0_BC_SETTING_2	CH0_BC_SETTING_2	Go
0xE	CH0_BC_SETTING_3	CH0_BC_SETTING_3	Go
0x20	INVERT_POLARITY_PORT1_SE G0	INVERT_POLARITY_PORT1_SEG0	Go
0x21	INVERT_POLARITY_PORT1_SE G1	INVERT_POLARITY_PORT1_SEG1	Go
0x22	INVERT_POLARITY_PORT1_SE G2	INVERT_POLARITY_PORT1_SEG2	Go
0x26	CH1_BC_SETTING_1	CH1_BC_SETTING_1	Go
0x2D	CH1_BC_SETTING_2	CH1_BC_SETTING_2	Go
0x2E	CH1_BC_SETTING_3	CH1_BC_SETTING_3	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-259](#) shows the codes that are used for access types in this section.

**Table 7-259. Page\_1\_FPD\_Port Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

#### 7.6.2.1.1 INVERT\_POLARITY\_PORT0\_SEG0 Register (Address = 0x0) [Default = 0x00]

INVERT\_POLARITY\_PORT0\_SEG0 is shown in [Table 7-260](#).

Return to the [Summary Table](#).

**Table 7-260. INVERT\_POLARITY\_PORT0\_SEG0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	INVERT_POLARITY_PORT0_SEG0	R/W	0x0	Invert polarity PORT0 for segment 0 0x0= Normal operation 0x1= Inverted polarity

#### 7.6.2.1.2 INVERT\_POLARITY\_PORT0\_SEG1 Register (Address = 0x1) [Default = 0x00]

INVERT\_POLARITY\_PORT0\_SEG1 is shown in [Table 7-261](#).

Return to the [Summary Table](#).

**Table 7-261. INVERT\_POLARITY\_PORT0\_SEG1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	INVERT_POLARTIY POR T0_SEG1	R/W	0x0	Invert polarity PORT0 for segment 1 0x0= Normal operation 0x1= Inverted polarity

**7.6.2.1.3 INVERT\_POLARITY\_PORT0\_SEG2 Register (Address = 0x2) [Default = 0x00]**INVERT\_POLARITY\_PORT0\_SEG2 is shown in [Table 7-262](#).Return to the [Summary Table](#).**Table 7-262. INVERT\_POLARITY\_PORT0\_SEG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R/W	0x0	Reserved
1:0	INVERT_POLARTIY POR T0_SEG2	R/W	0x0	Invert polarity PORT0 for segment 2 0x0= Normal operation 0x1= Inverted polarity

**7.6.2.1.4 CH0\_BC\_SETTING\_1 Register (Address = 0x6) [Default = X]**CH0\_BC\_SETTING\_1 is shown in [Table 7-263](#).Return to the [Summary Table](#).**Table 7-263. CH0\_BC\_SETTING\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CH0_BC_SETTING_1	R/W	X	Channel 0 back channel optimization setting 1 When strapped to FPD-Link III the default value is 0xFF When strapped to FPD-Link IV the default value is 0x00 Note: This value needs to be changed to the appropriate default value when switching to FPD mode different from strap

**7.6.2.1.5 CH0\_BC\_SETTING\_2 Register (Address = 0xD) [Default = X]**CH0\_BC\_SETTING\_2 is shown in [Table 7-264](#).Return to the [Summary Table](#).**Table 7-264. CH0\_BC\_SETTING\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CH0_BC_SETTING_2	R/W	X	Channel 0 back channel optimization setting 2 When strapped to FPD-Link III the default value is 0x70 When strapped to FPD-Link IV the default value is 0x34 Note: This value needs to be changed to the appropriate default value when switching to FPD mode different from strap

**7.6.2.1.6 CH0\_BC\_SETTING\_3 Register (Address = 0xE) [Default = X]**CH0\_BC\_SETTING\_3 is shown in [Table 7-265](#).Return to the [Summary Table](#).

**Table 7-265. CH0\_BC\_SETTING\_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CH0_BC_SETTING_3	R/W	X	Channel 0 back channel optimization setting 3 When strapped to FPD-Link III the default value is 0x37 When strapped to FPD-Link IV the default value is 0x53 Note: This value needs to be changed to the appropriate default value when switching to FPD mode different from strap

**7.6.2.1.7 INVERT\_POLARITY\_PORT1\_SEG0 Register (Address = 0x20) [Default = 0x00]**INVERT\_POLARITY\_PORT1\_SEG0 is shown in [Table 7-266](#).Return to the [Summary Table](#).**Table 7-266. INVERT\_POLARITY\_PORT1\_SEG0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	INVERT_POLARTIY_PORT1_SEG0	R/W	0x0	Invert polarity PORT1 for segment 0 0x0= Normal operation 0x1= Inverted polarity

**7.6.2.1.8 INVERT\_POLARITY\_PORT1\_SEG1 Register (Address = 0x21) [Default = 0x00]**INVERT\_POLARITY\_PORT1\_SEG1 is shown in [Table 7-267](#).Return to the [Summary Table](#).**Table 7-267. INVERT\_POLARITY\_PORT1\_SEG1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	INVERT_POLARTIY_PORT1_SEG1	R/W	0x0	Invert polarity PORT1 for segment 1 0x0= Normal operation 0x1= Inverted polarity

**7.6.2.1.9 INVERT\_POLARITY\_PORT1\_SEG2 Register (Address = 0x22) [Default = 0x00]**INVERT\_POLARITY\_PORT1\_SEG2 is shown in [Table 7-268](#).Return to the [Summary Table](#).**Table 7-268. INVERT\_POLARITY\_PORT1\_SEG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R/W	0x0	Reserved
1:0	INVERT_POLARTIY_PORT1_SEG2	R/W	0x0	Invert polarity PORT1 for segment 1 0x0= Normal operation 0x1= Inverted polarity

**7.6.2.1.10 CH1\_BC\_SETTING\_1 Register (Address = 0x26) [Default = X]**CH1\_BC\_SETTING\_1 is shown in [Table 7-269](#).Return to the [Summary Table](#).

**Table 7-269. CH1\_BC\_SETTING\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CH1_BC_SETTING_1	R/W	X	Channel 0 back channel optimization setting 1 When strapped to FPD-Link III the default value is 0x00 When strapped to FPD-Link IV the default value is 0xFF Note: This value needs to be changed to the appropriate default value when switching to FPD mode different from strap

**7.6.2.1.11 CH1\_BC\_SETTING\_2 Register (Address = 0x2D) [Default = X]**CH1\_BC\_SETTING\_2 is shown in [Table 7-270](#).Return to the [Summary Table](#).**Table 7-270. CH1\_BC\_SETTING\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CH1_GAIN_SETTING_2	R/W	X	Channel 1 back channel optimization setting 2 When strapped to FPD-Link III the default value is 0x34 When strapped to FPD-Link IV the default value is 0x70 Note: This value needs to be changed to the appropriate default value when switching to FPD mode different from strap

**7.6.2.1.12 CH1\_BC\_SETTING\_3 Register (Address = 0x2E) [Default = X]**CH1\_BC\_SETTING\_3 is shown in [Table 7-271](#).Return to the [Summary Table](#).**Table 7-271. CH1\_BC\_SETTING\_3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CH1_GAIN_SETTING_3	R/W	X	Channel 1 back channel optimization setting 3 When strapped to FPD-Link III the default value is 0x53 When strapped to FPD-Link IV the default value is 0x37 Note: This value needs to be changed to the appropriate default value when switching to FPD mode different from strap

### 7.6.2.2 Page\_2\_FPD\_PLL Registers

Table 7-272 lists the memory-mapped registers for the Page\_2\_FPD\_PLL registers. All register offset addresses not listed in Table 7-272 should be considered as reserved locations and the register contents should not be modified.

**Table 7-272. PAGE\_2\_FPD\_PLL Registers**

Address	Acronym	Register Name	Section
0x0	PLL_LOST_STATUS_CH0	PLL_LOST_STATUS_CH0	Go
0x4	MASH_ORDER_CH0	MASH_ORDER_CH0	Go
0x5	NDIV_7:0_CH0	NDIV_7:0_CH0	Go
0x6	NDIV_15:8_CH0	NDIV_15:8_CH0	Go
0x13	PDIV_CH0	PDIV_CH0	Go
0x14	SSCG_CTRL1_CH0	SSCG_CTRL1_CH0	Go
0x15	SSCG_CTRL2_CH0	SSCG_CTRL2_CH0	Go
0x16	SSCG_CTRL3_CH0	SSCG_CTRL3_CH0	Go
0x17	SSCG_CTRL4_CH0	SSCG_CTRL4_CH0	Go
0x18	DEN_7:0_CH0	DEN_7:0_CH0	Go
0x19	DEN_15:8_CH0	DEN_15:8_CH0	Go
0x1A	DEN_23:16_CH0	DEN_23:16_CH0	Go
0x1E	NUM_7:0_CH0	NUM_7:0_CH0	Go
0x1F	NUM_15:8_CH0	NUM_15:8_CH0	Go
0x20	NUM_23:16_CH0	NUM_23:16_CH0	Go
0x40	PLL_LOST_STATUS_CH1	PLL_LOST_STATUS_CH1	Go
0x44	MASH_ORDER_CH1	MASH_ORDER_CH1	Go
0x45	NDIV_7:0_CH1	NDIV_7:0_CH1	Go
0x46	NDIV_15:8_CH1	NDIV_15:8_CH1	Go
0x47	PLL_LOCK_STATUS_CH1	PLL_LOCK_STATUS_CH1	Go
0x4E	VCO_CH1	VCO_CH1	Go
0x53	PDIV_CH1	PDIV_CH1	Go
0x54	SSCG_CTRL1_CH1	SSCG_CTRL1_CH1	Go
0x55	SSCG_CTRL2_CH1	SSCG_CTRL2_CH1	Go
0x56	SSCG_CTRL3_CH1	SSCG_CTRL3_CH1	Go
0x57	SSCG_CTRL4_CH1	SSCG_CTRL4_CH1	Go
0x58	DEN_7:0_CH1	DEN_7:0_CH1	Go
0x59	DEN_15:8_CH1	DEN_15:8_CH1	Go
0x5A	DEN_23:16_CH1	DEN_23:16_CH1	Go
0x5E	NUM_7:0_CH1	NUM_7:0_CH1	Go
0x5F	NUM_15:8_CH1	NUM_15:8_CH1	Go
0x60	NUM_23:16_CH1	NUM_23:16_CH1	Go

Complex bit access types are encoded to fit into small table cells. Table 7-273 shows the codes that are used for access types in this section.

**Table 7-273. Page\_2\_FPD\_PLL Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear

**Table 7-273. Page\_2\_FPD\_PLL Access Type Codes  
(continued)**

Access Type	Code	Description
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

#### 7.6.2.2.1 PLL\_LOST\_STATUS\_CH0 Register (Address = 0x0) [Default = 0x01]

PLL\_LOST\_STATUS\_CH0 is shown in [Table 7-274](#).

Return to the [Summary Table](#).

**Table 7-274. PLL\_LOST\_STATUS\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	pll_lock_lost	RC	0x0	checks to see if pll_lock has been lost, clears after read
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

#### 7.6.2.2.2 MASH\_ORDER\_CH0 Register (Address = 0x4) [Default = X]

MASH\_ORDER\_CH0 is shown in [Table 7-275](#).

Return to the [Summary Table](#).

**Table 7-275. MASH\_ORDER\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:2	mash_order	R/W	X	Sets MASH order 0x0= Integer 0x2= Fractional Default value is set by the MODE_SEL0 pin For FPD3 modes, defaults to fractional (010) For FPD4 modes, defaults to integer (000)
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

#### 7.6.2.2.3 NDIV\_7:0\_CH0 Register (Address = 0x5) [Default = X]

NDIV\_7:0\_CH0 is shown in [Table 7-276](#).

Return to the [Summary Table](#).

DEFAULT\_05

**Table 7-276. NDIV\_7:0\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	NDIV[7:0]	R/W	X	N Divider 8-LSB for FPD-Link Port 0. 0x0= NDIV= 1 Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x6E (NDIV= 110) For FPD4 modes, default= 0x7D (NDIV= 125)

**7.6.2.2.4 NDIV\_15:8\_CH0 Register (Address = 0x6) [Default = X]**NDIV\_15:8\_CH0 is shown in [Table 7-277](#).Return to the [Summary Table](#).

DEFAULT\_06

**Table 7-277. NDIV\_15:8\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	NDIV[15:8]	R/W	X	N Divider 8-MSB for FPD-Link Port 0. Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x00 (NDIV= 110) For FPD4 modes, default= 0x00 (NDIV= 125)

**7.6.2.2.5 PDIV\_CH0 Register (Address = 0x13) [Default = X]**PDIV\_CH0 is shown in [Table 7-278](#).Return to the [Summary Table](#).**Table 7-278. PDIV\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	auto_vco_sel_en	R/W	0x1	VCO auto selection, instead of programming which vco manually
6:4	vco_post_div_sel	R/W	X	VCO post divider 0x0= /1 (FPD-Link IV only) 0x1= /2 (FPD-Link IV only) 0x2= /4 (FPD-Link IV only) 0x3= /8 (FPD-Link IV only) 0x4= /16 (FPD-Link III only) 0x5= /2 (FPD-Link III only) 0x6= /4 (FPD-Link III only) 0x7= /8 (FPD-Link III only) Default value is set by the MODE_SEL0 pin FPD-Link III default= 110 (/4) FPD-Link IV default= 000 (/1)
3:0	RESERVED	R/W	0x0	Reserved

**7.6.2.2.6 SSCG\_CTRL1\_CH0 Register (Address = 0x14) [Default = 0x80]**SSCG\_CTRL1\_CH0 is shown in [Table 7-279](#).Return to the [Summary Table](#).**Table 7-279. SSCG\_CTRL1\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	sscg_cntr_spread	R/W	0x1	SSCG mode spread selection 0x0= down-spread ramp 0x1= center-spread ramp
6:0	rampx_inc[6:0]	R/W	0x0	Increment per step that will be added to the ramp [6:0] for SSCG

**7.6.2.2.7 SSCG\_CTRL2\_CH0 Register (Address = 0x15) [Default = 0x00]**SSCG\_CTRL2\_CH0 is shown in [Table 7-280](#).Return to the [Summary Table](#).**Table 7-280. SSCG\_CTRL2\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	rampx_inc[14:7]	R/W	0x0	Increment per step that will be added to the ramp [14:7] for SSCG

**7.6.2.2.8 SSCG\_CTRL3\_CH0 Register (Address = 0x16) [Default = 0x00]**SSCG\_CTRL3\_CH0 is shown in [Table 7-281](#).Return to the [Summary Table](#).**Table 7-281. SSCG\_CTRL3\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	rampx_stop[7:0]	R/W	0x0	number of PFD cycles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

**7.6.2.2.9 SSCG\_CTRL4\_CH0 Register (Address = 0x17) [Default = 0x00]**SSCG\_CTRL4\_CH0 is shown in [Table 7-282](#).Return to the [Summary Table](#).**Table 7-282. SSCG\_CTRL4\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	sscg_en	R/W	0x0	enable spread spectrum clock generation
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	rampx_stop[9:8]	R/W	0x0	number of PFD cycles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

**7.6.2.2.10 DEN\_7:0\_CH0 Register (Address = 0x18) [Default = 0xF6]**DEN\_7:0\_CH0 is shown in [Table 7-283](#).Return to the [Summary Table](#).**Table 7-283. DEN\_7:0\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	den_mash[7:0]	R/W	0xF6	Bits 7:0 of denominator of fractional N-divider for FPD-Link Port 0.

**7.6.2.2.11 DEN\_15:8\_CH0 Register (Address = 0x19) [Default = 0xFF]**DEN\_15:8\_CH0 is shown in [Table 7-284](#).Return to the [Summary Table](#).

**Table 7-284. DEN\_15:8\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	den_mash[15:8]	R/W	0xFF	Bits 15:8 of denominator of fractional N-divider for FPD-Link Port 0.

**7.6.2.2.12 DEN\_23:16\_CH0 Register (Address = 0x1A) [Default = 0xFF]**DEN\_23:16\_CH0 is shown in [Table 7-285](#).Return to the [Summary Table](#).**Table 7-285. DEN\_23:16\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	den_mash_23_16	R/W	0xFF	Bits 23:16 of denominator of fractional N-divider for FPD-Link Port 0.

**7.6.2.2.13 NUM\_7:0\_CH0 Register (Address = 0x1E) [Default = X]**NUM\_7:0\_CH0 is shown in [Table 7-286](#).Return to the [Summary Table](#).**Table 7-286. NUM\_7:0\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	num_mash[7:0]	R/W	X	Bits 7:0 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x4A (NUM= 3106890) For FPD4 modes, default= 0

**7.6.2.2.14 NUM\_15:8\_CH0 Register (Address = 0x1F) [Default = X]**NUM\_15:8\_CH0 is shown in [Table 7-287](#).Return to the [Summary Table](#).**Table 7-287. NUM\_15:8\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	num_mash[15:8]	R/W	X	Bits 15:8 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x68 (NUM= 3106890) For FPD4 modes, default= 0

**7.6.2.2.15 NUM\_23:16\_CH0 Register (Address = 0x20) [Default = X]**NUM\_23:16\_CH0 is shown in [Table 7-288](#).Return to the [Summary Table](#).**Table 7-288. NUM\_23:16\_CH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	num_mash[23:16]	R/W	X	Bits 23:16 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x2F (NUM= 3106890) For FPD4 modes, default= 0

**7.6.2.2.16 PLL\_LOST\_STATUS\_CH1 Register (Address = 0x40) [Default = 0x01]**PLL\_LOST\_STATUS\_CH1 is shown in [Table 7-289](#).

Return to the [Summary Table](#).

**Table 7-289. PLL\_LOST\_STATUS\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	pll_lock_lost	RC	0x0	checks to see if pll_lock has been lost, clears after read
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

**7.6.2.2.17 MASH\_ORDER\_CH1 Register (Address = 0x44) [Default = 0x01]**

MASH\_ORDER\_CH1 is shown in [Table 7-290](#).

Return to the [Summary Table](#).

**Table 7-290. MASH\_ORDER\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:2	mash_order		0x0	bits to program MASH order Mode values 3'h7: adas_mode ? 3'h2:3'h2 Default: adas_mode ? 3'h2:3'h0
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

**7.6.2.2.18 NDIV\_7:0\_CH1 Register (Address = 0x45) [Default = X]**

NDIV\_7:0\_CH1 is shown in [Table 7-291](#).

Return to the [Summary Table](#).

DEFAULT\_05

**Table 7-291. NDIV\_7:0\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ncount[7:0]	R/W	X	Ncount's Divider values Default value is set by the MODE_SEL0 pin For FPD3 modes, default NCOUNT= 110 For FPD4 modes, default NCOUNT= 125

**7.6.2.2.19 NDIV\_15:8\_CH1 Register (Address = 0x46) [Default = X]**

NDIV\_15:8\_CH1 is shown in [Table 7-292](#).

Return to the [Summary Table](#).

DEFAULT\_06

**Table 7-292. NDIV\_15:8\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ncount[15:8]	R/W	X	Ncount's Divider values Default value is set by the MODE_SEL0 pin For FPD3 modes, default NCOUNT= 124 For FPD4 modes, default NCOUNT= 125

**7.6.2.2.20 PLL\_LOCK\_STATUS\_CH1 Register (Address = 0x47) [Default = 0x00]**PLL\_LOCK\_STATUS\_CH1 is shown in [Table 7-293](#).Return to the [Summary Table](#).**Table 7-293. PLL\_LOCK\_STATUS\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	pll_lock	R	0x0	pll_lock status

**7.6.2.2.21 VCO\_CH1 Register (Address = 0x4E) [Default = X]**VCO\_CH1 is shown in [Table 7-294](#).Return to the [Summary Table](#).**Table 7-294. VCO\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6:4	RESERVED	R/W	0x1	Reserved
3:2	vcoN_active_1_0	R/W	X	Lock VCO selection 0x0= VCO1 0x1= VCO2 0x2= VCO3 0x3= VCO4 Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x0 (VCO1) For FPD4 modes, default= 0x1 (VCO2)
1:0	RESERVED	R/W	0x3	Reserved

**7.6.2.2.22 PDIV\_CH1 Register (Address = 0x53) [Default = X]**PDIV\_CH1 is shown in [Table 7-295](#).Return to the [Summary Table](#).**Table 7-295. PDIV\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	auto_vco_sel_en	R/W	0x1	vco auto selection, instead of programming which vco manually

**Table 7-295. PDIV\_CH1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:4	vco_post_div_sel	R/W	X	VCO post divider 0x0= /1 (FPD-Link IV only) 0x1= /2 (FPD-Link IV only) 0x2= /4 (FPD-Link IV only) 0x3= /8 (FPD-Link IV only) 0x4= /16 (FPD-Link III only) 0x5= /2 (FPD-Link III only) 0x6= /4 (FPD-Link III only) 0x7= /8 (FPD-Link III only) Default value is set by the MODE_SEL0 pin FPD-Link III default= 110 (/4) FPD-Link IV default= 000 (/1)
3:0	RESERVED	R/W	0x0	Reserved

**7.6.2.2.23 SSCG\_CTL1\_CH1 Register (Address = 0x54) [Default = 0x80]**SSCG\_CTL1\_CH1 is shown in [Table 7-296](#).Return to the [Summary Table](#).**Table 7-296. SSCG\_CTL1\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	sscg_cntr_sprd	R/W	0x1	SSCG mode spread selection 0x0= down-spread ramp 0x1= center-spread ramp
6:0	rampx_inc[6:0]	R/W	0x0	Increment per step that will be added to the ramp [6:0] for SSCG

**7.6.2.2.24 SSCG\_CTL2\_CH1 Register (Address = 0x55) [Default = 0x00]**SSCG\_CTL2\_CH1 is shown in [Table 7-297](#).Return to the [Summary Table](#).**Table 7-297. SSCG\_CTL2\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	rampx_inc[14:7]	R/W	0x0	Increment per step that will be added to the ramp [14:7] for SSCG

**7.6.2.2.25 SSCG\_CTL3\_CH1 Register (Address = 0x56) [Default = 0x00]**SSCG\_CTL3\_CH1 is shown in [Table 7-298](#).Return to the [Summary Table](#).**Table 7-298. SSCG\_CTL3\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	rampx_stop[7:0]	R/W	0x0	number of PFD cycles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

**7.6.2.2.26 SSCG\_CTL4\_CH1 Register (Address = 0x57) [Default = 0x00]**SSCG\_CTL4\_CH1 is shown in [Table 7-299](#).Return to the [Summary Table](#).

**Table 7-299. SSCG\_CTL4\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	sscg_en	R/W	0x0	enable spread spectrum clock generation
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	rampx_stop[9:8]	R/W	0x0	number of PFD cycles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

**7.6.2.2.27 DEN\_7:0\_CH1 Register (Address = 0x58) [Default = 0xF6]**DEN\_7:0\_CH1 is shown in [Table 7-300](#).Return to the [Summary Table](#).

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**Table 7-300. DEN\_7:0\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	den_mash[7:0]	R/W	0xF6	Bits 7:0 of denominator of fractional N-divider for FPD-Link Port 0.

**7.6.2.2.28 DEN\_15:8\_CH1 Register (Address = 0x59) [Default = 0xFF]**DEN\_15:8\_CH1 is shown in [Table 7-301](#).Return to the [Summary Table](#).**Table 7-301. DEN\_15:8\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	den_mash[15:8]	R/W	0xFF	Bits 15:8 of denominator of fractional N-divider for FPD-Link Port 0.

**7.6.2.2.29 DEN\_23:16\_CH1 Register (Address = 0x5A) [Default = 0xFF]**DEN\_23:16\_CH1 is shown in [Table 7-302](#).Return to the [Summary Table](#).**Table 7-302. DEN\_23:16\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	den_mash[23:16]	R/W	0xFF	Bits 23:16 of denominator of fractional N-divider for FPD-Link Port 0.

**7.6.2.2.30 NUM\_7:0\_CH1 Register (Address = 0x5E) [Default = X]**NUM\_7:0\_CH1 is shown in [Table 7-303](#).Return to the [Summary Table](#).**Table 7-303. NUM\_7:0\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	num_mash[7:0]	R/W	X	Bits 7:0 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x4A (NUM= 3106890) For FPD4 modes, default= 0

**7.6.2.2.31 NUM\_15:8\_CH1 Register (Address = 0x5F) [Default = X]**NUM\_15:8\_CH1 is shown in [Table 7-304](#).Return to the [Summary Table](#).**Table 7-304. NUM\_15:8\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	num_mash[15:8]	R/W	X	Bits 15:8 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x4A (NUM= 3106890) For FPD4 modes, default= 0

**7.6.2.2.32 NUM\_23:16\_CH1 Register (Address = 0x60) [Default = X]**NUM\_23:16\_CH1 is shown in [Table 7-305](#).Return to the [Summary Table](#).**Table 7-305. NUM\_23:16\_CH1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	num_mash[23:16]	R/W	X	Bits 23:16 of numerator of fractional N-divider for FPD-Link Port 0 Default value is set by the MODE_SEL0 pin For FPD3 modes, default= 0x4A (NUM= 3106890) For FPD4 modes, default= 0

### 7.6.2.3 Page\_4\_D-PHY\_Digital\_Port\_0 Registers

Table 7-306 lists the memory-mapped registers for the Page\_4\_D-PHY\_Digital\_Port\_0 registers. All register offset addresses not listed in Table 7-306 should be considered as reserved locations and the register contents should not be modified.

**Table 7-306. PAGE\_4\_D-PHY\_DIGITAL\_PORT\_0 Registers**

Address	Acronym	Register Name	Section
0x1	DPHY_TINIT_TIMING	DPHY_TINIT_TIMING	Go
0x2	DPHY_TERM_TIMING	DPHY_TERM_TIMING	Go
0x3	DPHY_CLK_SETTLE_TIMING	DPHY_CLK_SETTLE_TIMING	Go
0x4	DPHY_HS_SETTLE_TIMING	DPHY_HS_SETTLE_TIMING	Go
0x5	DPHY_SKIP_TIMING	DPHY_SKIP_TIMING	Go
0x7	DPHY_BYPASS	DPHY_BYPASS	Go
0x8	HSRX_TO_CNT	HSRX_TO_CNT	Go
0x9	DPHY_CLK_PRP_ZERO_TIMING_G	DPHY_CLK_PRP_ZERO_TIMING	Go
0xD	INTR_CTL_DPHY	INTR_CTL_DPHY	Go
0xE	INTR_STS_DPHY	INTR_STS_DPHY	Go
0xF	DPHY_STATUS	DPHY_STATUS	Go
0x10	DPHY_DLANE0_ERR	DPHY_DLANE0_ERR	Go
0x11	DPHY_DLANE1_ERR	DPHY_DLANE1_ERR	Go
0x12	DPHY_DLANE2_ERR	DPHY_DLANE2_ERR	Go
0x13	DPHY_DLANE3_ERR	DPHY_DLANE3_ERR	Go
0x14	DPHY_ERR_CLK_LANE	DPHY_ERR_CLK_LANE	Go
0x15	DPHY_SYNC_STS	DPHY_SYNC_STS	Go
0x16	DPHY_FIFO_ERR	DPHY_FIFO_ERR	Go
0x17	DPHY_CLANE_DBG2	DPHY_CLANE_DBG2	Go
0x18	DPHY_CLANE_DBG	DPHY_CLANE_DBG	Go
0x19	DPHY_DLANE_DBG1	DPHY_DLANE_DBG1	Go
0x1A	DPHY_DLANE_DBG2	DPHY_DLANE_DBG2	Go
0x1B	DPHY_DLANE_DBG3	DPHY_DLANE_DBG3	Go
0x20	DPHY_DSI_CONFIG_0	DPHY_DSI_CONFIG_0	Go
0x21	DPHY_DSI_CONFIG_1	DPHY_DSI_CONFIG_1	Go
0x23	INTR_STS_DSI_ERR	INTR_STS_DSI_ERR	Go
0x24	INTR_STS_DPHY_ERR_FIFO_O_VR	INTR_STS_DPHY_ERR_FIFO_OVR	Go
0x25	INTR_CTL_DSI_ERR	INTR_CTL_DSI_ERR	Go
0x26	INTR_CTL_DPHY_ERR_FIFO_O_VR	INTR_CTL_DPHY_ERR_FIFO_OVR	Go
0x27	CFG_DSI_ERR_EN	CFG_DSI_ERR_EN	Go
0x28	CFG_DPHY_ERR_FIFO_OVR_E_N	CFG_DPHY_ERR_FIFO_OVR_EN	Go
0x29	DSI_DPHY_ERR_CNTR	DSI_DPHY_ERR_CNTR	Go
0x2A	DPHY_DSI_VC_DTYPE	DPHY_DSI_VC_DTYPE	Go
0x2E	DSI_VCID_STAT	DSI_VCID_STAT	Go
0x30	DSI_DATA_TYPE0	DSI_DATA_TYPE0	Go
0x31	DSI_DATA_TYPE1	DSI_DATA_TYPE1	Go
0x32	DSI_DATA_TYPE2	DSI_DATA_TYPE2	Go
0x33	DSI_DATA_TYPE3	DSI_DATA_TYPE3	Go

**Table 7-306. PAGE\_4\_D-PHY\_DIGITAL\_PORT\_0 Registers (continued)**

Address	Acronym	Register Name	Section
0x36	DPHY_DSI_EN_HSRX	DPHY_DSI_EN_HSRX	Go
0x37	DPHY_DSI_EN_LPRX	DPHY_DSI_EN_LPRX	Go
0x38	DPHY_DSI_EN_RXTERM_0	DPHY_DSI_EN_RXTERM_0	Go
0x39	DPHY_DSI_EN_RXTERM_1	DPHY_DSI_EN_RXTERM_1	Go
0x55	BRIDGE_CFG	BRIDGE_CFG	Go
0x57	TDM_CONFIG	TDM_CONFIG	Go
0x58	PRBS_CTRL_STATUS_DLANE0	PRBS_CTRL_STATUS_DLANE0	Go
0x59	PRBS_ERROR_COUNT_DLANE 0	PRBS_ERROR_COUNT_DLANE0	Go
0x5A	PRBS_STATUS_DLANE1	PRBS_STATUS_DLANE1	Go
0x5B	PRBS_ERROR_COUNT_DLANE 1	PRBS_ERROR_COUNT_DLANE1	Go
0x5C	PRBS_STATUS_DLANE2	PRBS_STATUS_DLANE2	Go
0x5D	PRBS_ERROR_COUNT_DLANE 2	PRBS_ERROR_COUNT_DLANE2	Go
0x5E	PRBS_STATUS_DLANE3	PRBS_STATUS_DLANE3	Go
0x5F	PRBS_ERROR_COUNT_DLANE 3	PRBS_ERROR_COUNT_DLANE3	Go
0x80	CSI_CFG0_VC0	CSI_CFG0_VC0	Go
0x81	CSI_LINE_LEN_LSB_VC0	CSI_LINE_LEN_LSB_VC0	Go
0x82	CSI_LINE_LEN_MSB_VC0	CSI_LINE_LEN_MSB_VC0	Go
0x88	CSI_CFG0_VC1	CSI_CFG0_VC1	Go
0x89	CSI_LINE_LEN_LSB_VC1	CSI_LINE_LEN_LSB_VC1	Go
0x8A	CSI_LINE_LEN_MSB_VC1	CSI_LINE_LEN_MSB_VC1	Go
0x90	CSI_CFG0_VC2	CSI_CFG0_VC2	Go
0x91	CSI_LINE_LEN_LSB_VC2	CSI_LINE_LEN_LSB_VC2	Go
0x92	CSI_LINE_LEN_MSB_VC2	CSI_LINE_LEN_MSB_VC2	Go
0x98	CSI_CFG0_VC3	CSI_CFG0_VC3	Go
0x99	CSI_LINE_LEN_LSB_VC3	CSI_LINE_LEN_LSB_VC3	Go
0x9A	CSI_LINE_LEN_MSB_VC3	CSI_LINE_LEN_MSB_VC3	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-307](#) shows the codes that are used for access types in this section.

**Table 7-307. Page\_4\_D-PHY\_Digital\_Port\_0 Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
<b>Write Type</b>		
W	W	Write
W1S	W 1S	Write 1 to set
<b>Reset or Default Value</b>		

**Table 7-307. Page\_4\_D-PHY\_Digital\_Port\_0 Access Type Codes (continued)**

Access Type	Code	Description
-n		Value after reset or the default value

#### 7.6.2.3.1 DPHY\_TINIT\_TIMING Register (Address = 0x1) [Default = 0x00]

DPHY\_TINIT\_TIMING is shown in [Table 7-308](#).

Return to the [Summary Table](#).

**Table 7-308. DPHY\_TINIT\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	
2:0	TINIT_TIME	R/W	0x0	D-PHY Initialization Time after power up in 100us units Initialization time= (TINIT_TIME + 1) * 100us

#### 7.6.2.3.2 DPHY\_TERM\_TIMING Register (Address = 0x2) [Default = 0x00]

DPHY\_TERM\_TIMING is shown in [Table 7-309](#).

Return to the [Summary Table](#).

**Table 7-309. DPHY\_TERM\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	DPHY_TERM_CLK_TIMING	R/W	0x0	Tclk TermEn terminal Count
3	RESERVED	R	0x0	Reserved
2:0	DPHY_TERM_DATA_TIMING	R/W	0x0	TD TermEn terminal Count

#### 7.6.2.3.3 DPHY\_CLK\_SETTLE\_TIMING Register (Address = 0x3) [Default = 0x1D]

DPHY\_CLK\_SETTLE\_TIMING is shown in [Table 7-310](#).

Return to the [Summary Table](#).

**Table 7-310. DPHY\_CLK\_SETTLE\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	TCLK_SETTLE_CNT	R/W	0x1D	TCLK-SETTLE Tclk Settle terminal Count in units of 10ns

#### 7.6.2.3.4 DPHY\_HS\_SETTLE\_TIMING Register (Address = 0x4) [Default = 0x14]

DPHY\_HS\_SETTLE\_TIMING is shown in [Table 7-311](#).

Return to the [Summary Table](#).

**Table 7-311. DPHY\_HS\_SETTLE\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

**Table 7-311. DPHY\_HS\_SETTLE\_TIMING Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:0	THS_SETTLE_CNT	R/W	0x14	THS-SETTLE Settle terminal Count in units of 10ns.

**7.6.2.3.5 DPHY\_SKIP\_TIMING Register (Address = 0x5) [Default = 0x3A]**DPHY\_SKIP\_TIMING is shown in [Table 7-312](#).Return to the [Summary Table](#).**Table 7-312. DPHY\_SKIP\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:1	TSKIP_CNT	R/W	0x1D	Tskip Count This register controls the amount of data that will be ignored at the end of transmission detection. This value is in units of the DDR clock (i.e. two UI intervals). Setting of this register will be dependent on the D-PHY lane frequency.
0	RESERVED	R	0x0	Reserved

**7.6.2.3.6 DPHY\_BYPASS Register (Address = 0x7) [Default = 0x00]**DPHY\_BYPASS is shown in [Table 7-313](#).Return to the [Summary Table](#).**Table 7-313. DPHY\_BYPASS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	BYPASS_TINIT	R/W	0x0	Bypass Tinit wait time
6	BYPASS_TCK_MISS	R/W	0x0	Bypass Tck Miss time
5	BYPASS_ULPS_CK0	R/W	0x0	Bypass ULPS for CLK0
4:0	BYPASS_LP	RH/W1S	0x0	Bypass Lp on clk and data lanes 3,2,1,0

**7.6.2.3.7 HSRX\_TO\_CNT Register (Address = 0x8) [Default = 0x00]**HSRX\_TO\_CNT is shown in [Table 7-314](#).Return to the [Summary Table](#).

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**Table 7-314. HSRX\_TO\_CNT Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	HSRX_TO_CNT	R/W	0x0	Timeout counter in ms. The timer will have a 1 ms range; example: if HSRX_TO_CNT= 1, then the timeout will occur between 0-1ms and if HSRX_TO_CNT= 255, then the timeout will occur between 254-255ms. If the register value is 0, then the timeout will be off.

**7.6.2.3.8 DPHY\_CLK\_PRP\_ZERO\_TIMING Register (Address = 0x9) [Default = 0x1D]**DPHY\_CLK\_PRP\_ZERO\_TIMING is shown in [Table 7-315](#).Return to the [Summary Table](#).

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**Table 7-315. DPHY\_CLK\_PRP\_ZERO\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	TCLK_PRP_ZERO_CNT	R/W	0x1D	TCLK-SETTLE TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock. ( in units of 10ns)

**7.6.2.3.9 INTR\_CTL\_DPHY Register (Address = 0xD) [Default = 0x00]**INTR\_CTL\_DPHY is shown in [Table 7-316](#).Return to the [Summary Table](#).**Table 7-316. INTR\_CTL\_DPHY Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	IE_DPHY_LANE_SYNC_ERROR	R/W	0x0	Enables interrupt for lane sync error
0	IE_DPHY_LANE_ERROR	R/W	0x0	Enables interrupt for lane error

**7.6.2.3.10 INTR\_STS\_DPHY Register (Address = 0xE) [Default = 0x00]**INTR\_STS\_DPHY is shown in [Table 7-317](#).Return to the [Summary Table](#).**Table 7-317. INTR\_STS\_DPHY Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	IS_DPHY_LANE_SYNC_ERROR	RC	0x0	Interrupt status for D-PHY Lane Sync Error This flag indicates the proper synchronization was not detected on all data lanes at the same time. Each enabled lane is expected to detect the sync sequence at the same time. If this does not occur correctly, this flag will be set. In addition, the DPHY_SYNC_STS register may be read to determine the synchronization status at the most recent error condition.
0	IS_DPHY_LANE_ERROR	RC	0x0	Interrupt status for D-PHY Lane Error Detected If this bit is set, one or more of the clock or data lanes has detected an error. To determine the error, read the DPHY_DLANEEx_ERR and DPHY_CLANE_ERR registers. This flag will be cleared when the Lane Error registers have been read.

**7.6.2.3.11 DPHY\_STATUS Register (Address = 0xF) [Default = 0x00]**DPHY\_STATUS is shown in [Table 7-318](#).Return to the [Summary Table](#).**Table 7-318. DPHY\_STATUS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	C_LANE_ACTIVE	R	0x0	Clock Lane Active 0: Clock Lane not active 1: Clock Lane active Once the TINIT_TIME expires and the dphy calibration is done for all the lanes, this bit remains set to 1.

**Table 7-318. DPHY\_STATUS Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	D_LANE_ACTIVE	R	0x0	Data Lanes Active For each data lane, this register reports if the lane is detected as active. There are no timers associated with it for inactive lane detection. 0: Data Lane is not active 1: Data Lane is active Once the TINIT_TIME expires and the dphy calibration is done for all the lanes, this bit reflects the number of DPHY lanes selected in the BRIDGE_CTL reg of Main page.

**7.6.2.3.12 DPHY\_DLANE0\_ERR Register (Address = 0x10) [Default = 0x00]**DPHY\_DLANE0\_ERR is shown in [Table 7-319](#).Return to the [Summary Table](#).**Table 7-319. DPHY\_DLANE0\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	EOT_SYNC_ERROR_0	RC	0x0	End of transmission sync error - Uncorrectable
3	SOT ERROR_0	RC	0x0	Bit Error in SYNC Sequence - Correctable
2	SOT SYNC ERROR_0	RC	0x0	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_0	RC	0x0	Control Error in HS Request Mode This error happens in a DPHY data lane when lprx of the corresponding data lane doesn't transition from 2'b01 to 2'b00 during LP to HS transition.
0	HS RX TO ERROR_0	RC	0x0	HS Transmission timeout error During the HS mode of data, if the hsrx_to_cnt (in ms) is reached, HS RX TO ERROR_0 bit is set. The counter will be reset upon entering LP.

**7.6.2.3.13 DPHY\_DLANE1\_ERR Register (Address = 0x11) [Default = 0x00]**DPHY\_DLANE1\_ERR is shown in [Table 7-320](#).Return to the [Summary Table](#).**Table 7-320. DPHY\_DLANE1\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	EOT_SYNC_ERROR_1	RC	0x0	End of transmission sync error - Uncorrectable
3	SOT ERROR_1	RC	0x0	Bit Error in SYNC Sequence - Correctable
2	SOT SYNC ERROR_1	RC	0x0	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_1	RC	0x0	Control Error in HS Request Mode This error happens in a DPHY data lane when lprx of the corresponding data lane doesn't transition from 2'b01 to 2'b00 during LP to HS transition.
0	HS RX TO ERROR_1	RC	0x0	HS Transmission timeout error During the HS mode of data, if the hsrx_to_cnt (in ms) is reached, HS RX TO ERROR_0 bit is set. The counter will be reset upon entering LP.

**7.6.2.3.14 DPHY\_DLANE2\_ERR Register (Address = 0x12) [Default = 0x00]**DPHY\_DLANE2\_ERR is shown in [Table 7-321](#).Return to the [Summary Table](#).**Table 7-321. DPHY\_DLANE2\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	EOT_SYNC_ERROR_2	RC	0x0	End of transmission sync error - Uncorrectable
3	SOT ERROR_2	RC	0x0	Bit Error in SYNC Sequence - Correctable
2	SOT SYNC ERROR_2	RC	0x0	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_2	RC	0x0	Control Error in HS Request Mode
0	HS RX TO ERROR_2	RC	0x0	HS Transmission timeout error

**7.6.2.3.15 DPHY\_DLANE3\_ERR Register (Address = 0x13) [Default = 0x00]**DPHY\_DLANE3\_ERR is shown in [Table 7-322](#).Return to the [Summary Table](#).

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**Table 7-322. DPHY\_DLANE3\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	EOT_SYNC_ERROR_3	RC	0x0	End of transmission sync error - Uncorrectable
3	SOT ERROR_3	RC	0x0	Bit Error in SYNC Sequence - Correctable
2	SOT SYNC ERROR_3	RC	0x0	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_3	RC	0x0	Control Error in HS Request Mode
0	HS RX TO ERROR_3	RC	0x0	HS Transmission timeout error

**7.6.2.3.16 DPHY\_ERR\_CLK\_LANE Register (Address = 0x14) [Default = 0x00]**DPHY\_ERR\_CLK\_LANE is shown in [Table 7-323](#).Return to the [Summary Table](#).

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**Table 7-323. DPHY\_ERR\_CLK\_LANE Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	CNTRL_ERR_HSRQST_CLK	RC	0x0	Control Error in HS Request Mode This error happens in a DPHY clock lane when lpx of the clock data lane doesn't transition from 2'b01 to 2'b00 during LP to HS transition.
1	RESERVED	R	0x0	Reserved
0	HS RX TO ERROR_CLK	RC	0x0	HS Transmission timeout error During the HS mode of clock, if the hsrx_to_cnt (in ms) is reached, HS RX TO ERROR_0 bit is set. The counter will be reset upon entering LP.

**7.6.2.3.17 DPHY\_SYNC\_STS Register (Address = 0x15) [Default = 0x00]**DPHY\_SYNC\_STS is shown in [Table 7-324](#).Return to the [Summary Table](#).**Table 7-324. DPHY\_SYNC\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	DLANE3_SYNC_STS	R	0x0	Sync Status for DLANE 3 Reports synchronization status for Data Lane 3 during most recent Synchronization error When only some of DPHY data lanes have received SoT byte (0xB8) while the others haven't, these bits reflect the sync received status of the DPHY data lanes.
2	DLANE2_SYNC_STS	R	0x0	Sync Status for DLANE 2 Reports synchronization status for Data Lane 3 during most recent Synchronization error
1	DLANE1_SYNC_STS	R	0x0	Sync Status for DLANE 1 Reports synchronization status for Data Lane 3 during most recent Synchronization error
0	DLANE0_SYNC_STS	R	0x0	Sync Status for DLANE 0 Reports synchronization status for Data Lane 3 during most recent Synchronization error

**7.6.2.3.18 DPHY\_FIFO\_ERR Register (Address = 0x16) [Default = 0x00]**DPHY\_FIFO\_ERR is shown in [Table 7-325](#).Return to the [Summary Table](#).**Table 7-325. DPHY\_FIFO\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	DLANE3_FIFO_OVERFLOW	RC	0x0	FIFO Overflow Error for DLANE3 Data from the DLANE FIFOs are read only when each of the enabled lanes has received data. If one or more of the enabled data lanes did not receive SoT byte, the FIFOs of the other DLANES will overflow. These register bits reflect the status of the DLANE FIFOs that overflowed.
2	DLANE2_FIFO_OVERFLOW	RC	0x0	FIFO Overflow Error for DLANE2
1	DLANE1_FIFO_OVERFLOW	RC	0x0	FIFO Overflow Error for DLANE1
0	DLANE0_FIFO_OVERFLOW	RC	0x0	FIFO Overflow Error for DLANE0

**7.6.2.3.19 DPHY\_CLANE\_DBG2 Register (Address = 0x17) [Default = 0x00]**DPHY\_CLANE\_DBG2 is shown in [Table 7-326](#).Return to the [Summary Table](#).**Table 7-326. DPHY\_CLANE\_DBG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	RESERVED	R	0x0	
0	BYPASS_TPRP_ZERO_C_NTR_CLANE_OV	R/W	0x0	If CLANE_OVERRIDE is set, a value of 1 on this bit will force clk_prp_zero_flag

**7.6.2.3.20 DPHY\_CLANE\_DBG Register (Address = 0x18) [Default = 0x00]**DPHY\_CLANE\_DBG is shown in [Table 7-327](#).Return to the [Summary Table](#).**Table 7-327. DPHY\_CLANE\_DBG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CLANE_OVERRIDE	R/W	0x0	Override Clock Lane State The Clock Lane State Machine is forced to the state specified by the value in CLANE_STATE field
6	CLANE_HSRX_TO_DISABLE	R/W	0x0	Disables the HS RX Timeout option only within the clock lane. This is to help when running in continuous clock mode. The Data lanes can still check for the timeout, but the clock lane will not cause an error
5	BYPASS_TSETTLE_CNT_R_CLANE_OV	R/W	0x0	If CLANE_OVERRIDE is set, a value of 1 on this bit will force clk_settle_flag
4	BYPASS_TERMEN_CNT_R_CLANE_OV	R/W	0x0	If CLANE_OVERRIDE is set, a value of 1 on this bit will force lineterm_flag
3:0	CLANE_STATE	R/W	0x0	If CLANE_OVERRIDE is set, this value is used for forcing the Clock Lane State Machine

**7.6.2.3.21 DPHY\_DLANE\_DBG1 Register (Address = 0x19) [Default = 0x04]**DPHY\_DLANE\_DBG1 is shown in [Table 7-328](#).Return to the [Summary Table](#).**Table 7-328. DPHY\_DLANE\_DBG1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	BYPASS_SYNC_SEQ_DETECT	R/W	0x0	Force sync_detect for all active Data Lanes
5	BYPASS_TSETTLE_CNT_R_HSSYNC	R/W	0x0	Force hssync_en_flag for all active Data Lanes
4	BYPASS_TERMEN_CNT_R_HSSYNC	R/W	0x0	Force lineterm_flag for all active Data Lanes
3	BYPASS_VALID_SYNC_DETECT	R/W	0x0	Bypass Valid Sync Detect This bit controls whether a LANE_SYNC_ERROR will prevent DPHY video reception. By default, all data lanes are expected to detect synchronization almost at the same time. If they do not, video reception is normally disabled. 0: Require synchronization across all enabled lanes 1: Forward video if synchronization check fails
2	LEADER_SEQ_MODE	R/W	0x1	Leader Sequence Detect Mode This bit controls detection of the Leader Sequence for synchronization on the DPHY data lanes. 0: Less Restrictive detection (allow single bit errors within an 8-bit window) 1: More Restrictive detection (allow single bit error within the first 6-bits following the HS_ZERO data)
1:0	RESERVED	R	0x0	

**7.6.2.3.22 DPHY\_DLANE\_DBG2 Register (Address = 0x1A) [Default = 0x00]**DPHY\_DLANE\_DBG2 is shown in [Table 7-329](#).Return to the [Summary Table](#).

**Table 7-329. DPHY\_DLANE\_DBG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DLANE_STATE_OVERRIDE	R/W	0x0	Override Data Lane State Vector
6:5	RESERVED	R	0x0	
4:0	DLANE_STATE_VAL	R/W	0x0	If DLANE_STATE_OVERRIDE is set, this value is used for forcing the Data Lane State Machine for all active Data Lanes

**7.6.2.3.23 DPHY\_DLANE\_DBG3 Register (Address = 0x1B) [Default = 0x00]**DPHY\_DLANE\_DBG3 is shown in [Table 7-330](#).Return to the [Summary Table](#).**Table 7-330. DPHY\_DLANE\_DBG3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_PROT_STATE_OVERRIDE	R/W	0x0	Override DSI Protocol State Vector
6:4	RESERVED	R	0x0	
3:0	DSI_PROT_STATE_VAL	R/W	0x0	If DSI_PROT_STATE_OVERRIDE is set, this value is used for forcing the DSI_PROT_STATE_OVERRIDE State Machine

**7.6.2.3.24 DPHY\_DSI\_CONFIG\_0 Register (Address = 0x20) [Default = 0x4F]**DPHY\_DSI\_CONFIG\_0 is shown in [Table 7-331](#).Return to the [Summary Table](#).**Table 7-331. DPHY\_DSI\_CONFIG\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	DSI_TRY_RECOVERY	R/W	0x1	DSI Attempt Recovery When set to a 1, the DSI Protocol module will attempt to recover from error conditions.
5	RESERVED	R	0x0	Reserved
4	DSI_SYNC_PULSE_MODE	R/W	0x0	Controls generation of Sync Pulses 0: Event mode (Hsync end and Vsync end packets are ignored); Used in burst mode 1: Pulse mode
3:0	DSI_VC_ENABLE	R/W	0xF	Enable VC-IDs Each bit in this four bit field enables one of the four Virtual Channel IDs. If a packet was received without an expected VC-ID, an error will be reported. For the error to be reported in the DSI_ERR_DET bit, the DSI_INV_VC_ERR_EN bit must also be set. These controls do not filter out packets with invalid VC-IDs.

**7.6.2.3.25 DPHY\_DSI\_CONFIG\_1 Register (Address = 0x21) [Default = 0x00]**DPHY\_DSI\_CONFIG\_1 is shown in [Table 7-332](#).Return to the [Summary Table](#).

**Table 7-332. DPHY\_DSI\_CONFIG\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_NO_GRAYSCALE	R/W	0x0	Disable Grayscale Interpolation For DSI RGB data types less than 24 bits, the conversion to RGB888 replicates the most significant subpixel bits on the otherwise-unused least significant subpixel bits in order to achieve a higher grayscale range. 0: Enable Grayscale Interpolation 1: Disable Grayscale Interpolation
3	DSI_NULL_CRC_DIS	R/W	0x0	Error reporting for NULL and BLANK long packets; when set CRC errors in DSI/CSI packets are ignored
6:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DSI_NO_EOTPkt	R/W	0x0	No EOT Packet mode If set to 0, the device will indicate an error if an End of Transmission occurs without an EOT Packet. If set to 0, no error will be indicated. The error is indicated in the DPHY_ERR_FIFO_OVR status register.

**7.6.2.3.26 INTR\_STS\_DSI\_ERR Register (Address = 0x23) [Default = 0x00]**INTR\_STS\_DSI\_ERR is shown in [Table 7-333](#).Return to the [Summary Table](#).**Table 7-333. INTR\_STS\_DSI\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IS_INV_TYPE_GLW_ERR	RC	0x0	Received Invalid Type on Generic Long Write packet
6	IS_INV_WC_GLW_ERR	RC	0x0	Received Invalid Word Count on Generic Long Write packet
5	IS_INV_LEN_ERR	RC	0x0	Received HS to LP prior to consuming the number of bytes as indicated by the Word Count in the recent DSI/CSI packet.
4	IS_INV_VC_ERR	RC	0x0	Received DSI/CSI packet with a VC that has been disabled
3	IS_INV_DT_ERR	RC	0x0	Received V/H_SYNC END in the pulse mode configuration OR any other unsupported Data Type
2	IS_CHECKSUM_ERR	RC	0x0	CHECKSUM error status for a received DSI/CSI packet
1	IS_ECC_MULTI_ERR	RC	0x0	Multi bit of ECC error received on a DSI/CSI packet header (not correctable by the hardware)
0	IS_ECC_SINGLE_ERR	RC	0x0	Single bit of ECC error received on a DSI/CSI packet header (corrected by the hardware)

**7.6.2.3.27 INTR\_STS\_DPHY\_ERR\_FIFO\_OVR Register (Address = 0x24) [Default = 0x00]**INTR\_STS\_DPHY\_ERR\_FIFO\_OVR is shown in [Table 7-334](#).Return to the [Summary Table](#).**Table 7-334. INTR\_STS\_DPHY\_ERR\_FIFO\_OVR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IS_DATA_TYPE_OVR	RC	0x0	DSI DATA TYPE register overflow status. When set, indicates that all the DSI_DATA_TYPE registers are valid and a new data_type has been received on DSI/CSI long packet, effectively having no space to save the data_type.
6	IS_I2C_WR_OVR	RC	0x0	I2C Write FIFO overflow status
5	IS_SDP_WR_OVR	RC	0x0	SD Write FIFO overflow status
4	IS_DPHY_FIFO_OVR	RC	0x0	One of the DPHY's DLANE FIFO overflow status
3	IS_EOT_WITHOUT_EOT_P	RC	0x0	Received EoT without EoTP

**Table 7-334. INTR\_STS\_DPHY\_ERR\_FIFO\_OVR Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2	IS_EOT_SYNC_ERR	RC	0x0	EOT_SYNC_ERR status
1	IS_SOT_SYNC_ERR	RC	0x0	SOT_SYNC_ERR status
0	IS_SOT_ERR	RC	0x0	SOT_ERR status

**7.6.2.3.28 INTR\_CTL\_DSI\_ERR Register (Address = 0x25) [Default = 0x00]**INTR\_CTL\_DSI\_ERR is shown in [Table 7-335](#).Return to the [Summary Table](#).**Table 7-335. INTR\_CTL\_DSI\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IE_INV_TYPE_GLW_ERR	R/W	0x0	Enables interrupt for INV_TYPE_GLW_ERR
6	IE_INV_WC_GLW_ERR	R/W	0x0	Enables interrupt for INV_WC_GLW_ERR
5	IE_INV_LEN_ERR	R/W	0x0	Enables interrupt for INV_LEN_ERR
4	IE_INV_VC_ERR	R/W	0x0	Enables interrupt for INV_VC_ERR
3	IE_INV_DT_ERR	R/W	0x0	Enables interrupt for INV_DT_ERR
2	IE_CHECKSUM_ERR	R/W	0x0	Enables interrupt for IE_CHECKSUM_ERR
1	IE_ECC_MULTI_ERR	R/W	0x0	Enables interrupt for IE_ECC_MULTI_ERR
0	IE_ECC_SINGLE_ERR	R/W	0x0	Enables interrupt for ECC_SINGLE_ERR

**7.6.2.3.29 INTR\_CTL\_DPHY\_ERR\_FIFO\_OVR Register (Address = 0x26) [Default = 0x00]**INTR\_CTL\_DPHY\_ERR\_FIFO\_OVR is shown in [Table 7-336](#).Return to the [Summary Table](#).**Table 7-336. INTR\_CTL\_DPHY\_ERR\_FIFO\_OVR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IE_DATA_TYPE_OVR	R/W	0x0	Enables interrupt for DATA_TYPE_OVR
6	IE_I2C_WR_OVR	R/W	0x0	Enables interrupt for I2C_WR_OVR
5	IE_SDP_WR_OVR	R/W	0x0	Enables interrupt for SDP_WR_OVR
4	IE_DPHY_FIFO_OVR	R/W	0x0	Enables interrupt for DPHY_FIFO_OVR
3	IE_EOT_WITHOUT_EOTP	R/W	0x0	Enables interrupt for EOT_WITHOUT_EOTP
2	IE_EOT_SYNC_ERR	R/W	0x0	Enables interrupt for EOT_SYNC_ERR
1	IE_SOT_SYNC_ERR	R/W	0x0	Enables interrupt for SOT_SYNC_ERR
0	IE_SOT_ERR	R/W	0x0	Enables interrupt for SOT_ERR

**7.6.2.3.30 CFG\_DSI\_ERR\_EN Register (Address = 0x27) [Default = 0x00]**CFG\_DSI\_ERR\_EN is shown in [Table 7-337](#).Return to the [Summary Table](#).**Table 7-337. CFG\_DSI\_ERR\_EN Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CFG_EN_INV_TYPE_GLW_ERR	R/W	0x0	Enables INV_TYPE_GLW_ERR to be included in INTR_STS_DSI_ERR
6	CFG_EN_INV_WC_GLW_ERR	R/W	0x0	Enables INV_WC_GLW_ERR to be included in INTR_STS_DSI_ERR

**Table 7-337. CFG\_DSI\_ERR\_EN Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
5	CFG_EN_INV_LEN_ERR	R/W	0x0	Enables INV_LEN_ERR to be included in INTR_STS_DSI_ERR
4	CFG_EN_INV_VC_ERR	R/W	0x0	Enables INV_VC_ERR to be included in INTR_STS_DSI_ERR
3	CFG_EN_INV_DT_ERR	R/W	0x0	Enables INV_DT_ERR to be included in INTR_STS_DSI_ERR
2	CFG_EN_CHECKSUM_E RR	R/W	0x0	Enables IE_CHECKSUM_ERR to be included in INTR_STS_DSI_ERR
1	CFG_EN_ECC_MULTI_E RR	R/W	0x0	Enables IE_ECC_MULTI_ERR to be included in INTR_STS_DSI_ERR
0	CFG_EN_ECC_SINGLE_ ERR	R/W	0x0	Enables ECC_SINGLE_ERR to be included in INTR_STS_DSI_ERR

**7.6.2.3.31 CFG\_DPHY\_ERR\_FIFO\_OVR\_EN Register (Address = 0x28) [Default = 0x00]**CFG\_DPHY\_ERR\_FIFO\_OVR\_EN is shown in [Table 7-338](#).Return to the [Summary Table](#).**Table 7-338. CFG\_DPHY\_ERR\_FIFO\_OVR\_EN Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CFG_EN_DATA_TYPE_O VR	R/W	0x0	Enables IE_DATA_TYPE_OVR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
6	CFG_EN_I2C_WR_OVR	R/W	0x0	Enables IE_I2C_WR_OVR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
5	CFG_EN_SDP_WR_OVR	R/W	0x0	Enables IE_SDP_WR_OVR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
4	CFG_EN_DPHY_FIFO_O VR	R/W	0x0	Enables IE_DPHY_FIFO_OVR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
3	CFG_EN_EOT_WITHOUT _EOTP	R/W	0x0	Enables IE_EOT_WITHOUT_EOTP to be included in INTR_STS_DPHY_ERR_FIFO_OVR
2	CFG_EN_EOT_SYNC_E RR	R/W	0x0	Enables IE_EOT_SYNC_ERR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
1	CFG_EN_SOT_SYNC_E RR	R/W	0x0	Enables IE_SOT_SYNC_ERR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
0	CFG_EN_SOT_ERR	R/W	0x0	Enables IE_SOT_ERR to be included in INTR_STS_DPHY_ERR_FIFO_OVR

**7.6.2.3.32 DSI\_DPHY\_ERR\_CNTR Register (Address = 0x29) [Default = 0x00]**DSI\_DPHY\_ERR\_CNTR is shown in [Table 7-339](#).Return to the [Summary Table](#).**Table 7-339. DSI\_DPHY\_ERR\_CNTR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	DSI_DPHY_ERROR_CO UNT	RC	0x0	DSI Error Count This register reports the number of errors that have been detected on any of the status bits of INTR_STS_DSI_ERR or INTR_STS_DPHY_ERR_FIFO_OVR status registers. This value will be cleared on read.

**7.6.2.3.33 DPHY\_DSI\_VC\_DTYPE Register (Address = 0x2A) [Default = 0x00]**DPHY\_DSI\_VC\_DTYPE is shown in [Table 7-340](#).

Return to the [Summary Table](#).

**Table 7-340. DPHY\_DSI\_VC\_DTYPE Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	DSI_VC	R	0x0	DSI Virtual Channel ID This field returns the Virtual Channel ID for the most recently received pixel stream packet. This field is updated by the DSI Protocol logic whenever a packet header is detected with the lower 4 bits of the DTYPE in the range of 0xB to 0xE.
5:0	DSI_DTYPE	R	0x0	DSI Data Type This field returns the Data Type for the most recently received pixel stream packet. This field is updated by the DSI Protocol logic whenever a packet header is detected with the lower 4 bits of the DTYPE in the range of 0xB to 0xE.

**7.6.2.3.34 DSI\_VCID\_STAT Register (Address = 0x2E) [Default = 0x00]**

DSI\_VCID\_STAT is shown in [Table 7-341](#).

Return to the [Summary Table](#).

**Table 7-341. DSI\_VCID\_STAT Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_VCID_STAT_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 7 of this register. Clearing of individual bits of DSI_VCID_STAT is not supported.
6:4	RESERVED	R	0x0	Reserved
3:0	DSI_VCID_STAT	R	0x0	Each bit of this field corresponds to a VC. When a DSI/CSI short/long packet is received, the VCID is captured in the corresponding bit in this register.

**7.6.2.3.35 DSI\_DATA\_TYPE0 Register (Address = 0x30) [Default = 0x00]**

DSI\_DATA\_TYPE0 is shown in [Table 7-342](#).

Return to the [Summary Table](#).

**Table 7-342. DSI\_DATA\_TYPE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_DATA_TYPE0_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 0 of this register.
6	DSI_DATA_TYPE0_VLD	R	0x0	When set, this bit validates bits 5:0 of this register.
5:0	DSI_DATA_TYPE0	R	0x0	A unique DSI DATA TYPE captured on a DSI/CSI long packet. This field can be cleared by writing a 1 into bit 7 of this register.

**7.6.2.3.36 DSI\_DATA\_TYPE1 Register (Address = 0x31) [Default = 0x00]**

DSI\_DATA\_TYPE1 is shown in [Table 7-343](#).

Return to the [Summary Table](#).

**Table 7-343. DSI\_DATA\_TYPE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_DATA_TYPE1_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 0 of this register.
6	DSI_DATA_TYPE1_VLD	R	0x0	When set, this bit validates bits 5:0 of this register.
5:0	DSI_DATA_TYPE1	R	0x0	A unique DSI DATA TYPE captured on a DSI/CSI long packet. This field can be cleared by writing a 1 into bit 7 of this register.

**7.6.2.3.37 DSI\_DATA\_TYPE2 Register (Address = 0x32) [Default = 0x00]**DSI\_DATA\_TYPE2 is shown in [Table 7-344](#).Return to the [Summary Table](#).**Table 7-344. DSI\_DATA\_TYPE2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_DATA_TYPE2_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 0 of this register.
6	DSI_DATA_TYPE2_VLD	R	0x0	When set, this bit validates bits 5:0 of this register.
5:0	DSI_DATA_TYPE2	R	0x0	A unique DSI DATA TYPE captured on a DSI/CSI long packet. This field can be cleared by writing a 1 into bit 7 of this register.

**7.6.2.3.38 DSI\_DATA\_TYPE3 Register (Address = 0x33) [Default = 0x00]**DSI\_DATA\_TYPE3 is shown in [Table 7-345](#).Return to the [Summary Table](#).**Table 7-345. DSI\_DATA\_TYPE3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_DATA_TYPE3_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 0 of this register.
6	DSI_DATA_TYPE3_VLD	R	0x0	When set, this bit validates bits 5:0 of this register.
5:0	DSI_DATA_TYPE3	R	0x0	A unique DSI DATA TYPE captured on a DSI/CSI long packet. This field can be cleared by writing a 1 into bit 7 of this register.

**7.6.2.3.39 DPHY\_DSI\_EN\_HSRX Register (Address = 0x36) [Default = 0x00]**DPHY\_DSI\_EN\_HSRX is shown in [Table 7-346](#).Return to the [Summary Table](#).**Table 7-346. DPHY\_DSI\_EN\_HSRX Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	EN_HSRX_OV	R/W	0x0	Overwrite to enable CSI RX HS receiver
5	RESERVED	R	0x0	Reserved
4	EN_HSRX_CLK0	R/W	0x0	Enable HSRX CLK0
3	EN_HSRX_D3	R/W	0x0	Enable HSRX D3
2	EN_HSRX_D2	R/W	0x0	Enable HSRX D2
1	EN_HSRX_D1	R/W	0x0	Enable HSRX D1
0	EN_HSRX_D0	R/W	0x0	Enable HSRX D0

**7.6.2.3.40 DPHY\_DSI\_EN\_LPRX Register (Address = 0x37) [Default = 0x00]**DPHY\_DSI\_EN\_LPRX is shown in [Table 7-347](#).Return to the [Summary Table](#).

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**Table 7-347. DPHY\_DSI\_EN\_LPRX Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	EN_LPRX_OV	R/W	0x0	Overwrite CSI LP Receiver

**Table 7-347. DPHY\_DSI\_EN\_LPRX Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
5	RESERVED	R	0x0	Reserved
4	EN_LPRX_CLK0	R/W	0x0	Enable LP Receiver for CLK0
3	EN_LPRX_D3	R/W	0x0	Enable LP Receiver for D3
2	EN_LPRX_D2	R/W	0x0	Enable LP Receiver for D2
1	EN_LPRX_D1	R/W	0x0	Enable LP Receiver for D1
0	EN_LPRX_D0	R/W	0x0	Enable LP Receiver for D0

**7.6.2.3.41 DPHY\_DSI\_EN\_RXTERM\_0 Register (Address = 0x38) [Default = 0x00]**DPHY\_DSI\_EN\_RXTERM\_0 is shown in [Table 7-348](#).Return to the [Summary Table](#).

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**Table 7-348. DPHY\_DSI\_EN\_RXTERM\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	EN_RXTERM_OV	R/W	0x0	Overwrite CSI RX HS Termination
5	RESERVED	R	0x0	Reserved
4	EN_RXTERM_CLK0	R/W	0x0	Enable RX Termination for CSI CLK0
3	EN_RXTERM_D3	R/W	0x0	Enable RX Termination for CSI D3
2	EN_RXTERM_D2	R/W	0x0	Enable RX Termination for CSI D2
1	EN_RXTERM_D1	R/W	0x0	Enable RX Termination for CSI D1
0	EN_RXTERM_D0	R/W	0x0	Enable RX Termination for CSI D0

**7.6.2.3.42 DPHY\_DSI\_EN\_RXTERM\_1 Register (Address = 0x39) [Default = 0x00]**DPHY\_DSI\_EN\_RXTERM\_1 is shown in [Table 7-349](#).Return to the [Summary Table](#).**Table 7-349. DPHY\_DSI\_EN\_RXTERM\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	DPHY_CLRZ_OV	R/W	0x0	Overwrite DPHY_CLRZ
5:4	RESERVED	R	0x0	Reserved
3	DPHY_CLRZ_D3	R/W	0x0	Set DPHY_CLRZ for CSI D3
2	DPHY_CLRZ_D2	R/W	0x0	Set DPHY_CLRZ for CSI D2
1	DPHY_CLRZ_D1	R/W	0x0	Set DPHY_CLRZ for CSI D1
0	DPHY_CLRZ_D0	R/W	0x0	Set DPHY_CLRZ for CSI D0

**7.6.2.3.43 BRIDGE\_CFG Register (Address = 0x55) [Default = 0x00]**BRIDGE\_CFG is shown in [Table 7-350](#).Return to the [Summary Table](#).

**Table 7-350. BRIDGE\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:4	DSI_BYTES_PER_PIXEL	R/W	0x0	<p>Number of DSI Bytes Per Pixel:  For Continuous Clock Mode, selects the number of DSI bytes per pixel for the desired DSI Data Type</p> <p>00: 3 bytes/pixel (RGB888, RGB666 loosely packed, 20b YCbCr 4:2:2, 24b YCbCr 4:2:2, 12b YCbCr 4:2:0, Compressed)</p> <p>01: 2.25 bytes/pixel (RGB666 packed)</p> <p>10: 2 bytes/pixel (RGB565, 16b YCbCr 4:2:2)</p> <p>11: Reserved</p> <p>Notes: All RGB formats are converted to RGB888. YCbCr and Compressed formats are passed through unconverted</p> <p>In Independent DSI to FPD3 mode, this controls affects the selected port.</p>
3:0	RESERVED	R	0x0	Reserved

**7.6.2.3.44 TDM\_CONFIG Register (Address = 0x57) [Default = 0x02]**TDM\_CONFIG is shown in [Table 7-351](#).Return to the [Summary Table](#).**Table 7-351. TDM\_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	
3	TDM_FS_MODE	R/W	0x0	<p>TDM Frame Sync Mode:  Sets active level for the Frame Sync for the TDM audio. The Frame Sync signal provides an active pulse to indicate the first sample data on the TDM data signal.</p> <p>0: Active high Frame Sync  1: Active low Frame Sync (similar to I2S word select)  This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.</p>
2	TDM_DELAY	R/W	0x0	<p>TDM Data Delay:  Controls data delay for TDM audio samples from the active Frame Sync edge.</p> <p>0: Data is not delayed from Frame Sync (data is left justified)  1: Data is delayed 1 bit from Frame Sync  This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.</p>
1:0	TDM_FS_WIDTH	R/W	0x2	<p>TDM Frame Sync Width:  Indicates width of TDM Frame Sync pulse for I2S to TDM conversion</p> <p>00: FS is 50/50 duty cycle  01: FS is one slot/channel wide  1x: FS is 1 clock pulse wide</p>

**7.6.2.3.45 PRBS\_CTRL\_STATUS\_DLANE0 Register (Address = 0x58) [Default = 0x00]**PRBS\_CTRL\_STATUS\_DLANE0 is shown in [Table 7-352](#).Return to the [Summary Table](#).**Table 7-352. PRBS\_CTRL\_STATUS\_DLANE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PRBS_CHK_EN_D0	R/W	0x0	Set this bit to enable PRBS check on HSRX[3:0] on DPHY Data Lane0
4	PRBS_FAIL_STKY_FLG_D0	R	0x0	Fail status of the PRBS (sticky); Once failed, set to 1

**Table 7-352. PRBS\_CTRL\_STATUS\_DLANE0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3	PRBS_FAIL_LIVE_FLG_D0	R	0x0	Fail status of the PRBS (live); latest fail status
2	PRBS_STATUS_D0	R	0x0	When set, bits 4 and 3 of this register are valid
1:0	RESERVED	R	0x0	Reserved

**7.6.2.3.46 PRBS\_ERROR\_COUNT\_DLANE0 Register (Address = 0x59) [Default = 0x00]**PRBS\_ERROR\_COUNT\_DLANE0 is shown in [Table 7-353](#).Return to the [Summary Table](#).**Table 7-353. PRBS\_ERROR\_COUNT\_DLANE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PRBS_ERR_CNT_D0	R	0x0	Number of bits errored during PRBS checking of DPHY Data Lane0

**7.6.2.3.47 PRBS\_STATUS\_DLANE1 Register (Address = 0x5A) [Default = 0x00]**PRBS\_STATUS\_DLANE1 is shown in [Table 7-354](#).Return to the [Summary Table](#).**Table 7-354. PRBS\_STATUS\_DLANE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PRBS_CHK_EN_D1	R/W	0x0	Set this bit to enable PRBS check on HSRX[3:0] on DPHY Data Lane1
4	PRBS_FAIL_STKY_FLG_D1	R	0x0	Fail status of the PRBS (sticky); Once failed, set to 1
3	PRBS_FAIL_LIVE_FLG_D1	R	0x0	Fail status of the PRBS (live); latest fail status
2	PRBS_STATUS_D1	R	0x0	When set, bits 4 and 3 of this register are valid
1:0	RESERVED	R	0x0	Reserved

**7.6.2.3.48 PRBS\_ERROR\_COUNT\_DLANE1 Register (Address = 0x5B) [Default = 0x00]**PRBS\_ERROR\_COUNT\_DLANE1 is shown in [Table 7-355](#).Return to the [Summary Table](#).

DSI Error Configuration Register 0

**Table 7-355. PRBS\_ERROR\_COUNT\_DLANE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PRBS_ERR_CNT_D1	R	0x0	Number of bits errored during PRBS checking of DPHY Data Lane1

**7.6.2.3.49 PRBS\_STATUS\_DLANE2 Register (Address = 0x5C) [Default = 0x00]**PRBS\_STATUS\_DLANE2 is shown in [Table 7-356](#).Return to the [Summary Table](#).

DSI VC and DTYPEn Register

**Table 7-356. PRBS\_STATUS\_DLANE2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PRBS_CHK_EN_D2	R/W	0x0	Set this bit to enable PRBS check on HSRX[3:0] on DPHY Data Lane2
4	PRBS_FAIL_STKY_FLG_D2	R	0x0	Fail status of the PRBS (sticky); Once failed, set to 1
3	PRBS_FAIL_LIVE_FLG_D2	R	0x0	Fail status of the PRBS (live); latest fail status
2	PRBS_STATUS_D2	R	0x0	When set, bits 4 and 3 of this register are valid
1:0	RESERVED	R	0x0	Reserved

**7.6.2.3.50 PRBS\_ERROR\_COUNT\_DLANGE2 Register (Address = 0x5D) [Default = 0x00]**PRBS\_ERROR\_COUNT\_DLANGE2 is shown in [Table 7-357](#).Return to the [Summary Table](#).

Pattern Generator Control Register

**Table 7-357. PRBS\_ERROR\_COUNT\_DLANGE2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PRBS_ERR_CNT_D2	R	0x0	Number of bits errored during PRBS checking of DPHY Data Lane2

**7.6.2.3.51 PRBS\_STATUS\_DLANGE3 Register (Address = 0x5E) [Default = 0x00]**PRBS\_STATUS\_DLANGE3 is shown in [Table 7-358](#).Return to the [Summary Table](#).

Pattern Generator Configuration Register

**Table 7-358. PRBS\_STATUS\_DLANGE3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PRBS_CHK_EN_D3	R/W	0x0	Set this bit to enable PRBS check on HSRX[3:0] on DPHY Data Lane3
4	PRBS_FAIL_STKY_FLG_D3	R	0x0	Fail status of the PRBS (sticky); Once failed, set to 1
3	PRBS_FAIL_LIVE_FLG_D3	R	0x0	Fail status of the PRBS (live); latest fail status
2	PRBS_STATUS_D3	R	0x0	When set, bits 4 and 3 of this register are valid
1:0	RESERVED	R	0x0	Reserved

**7.6.2.3.52 PRBS\_ERROR\_COUNT\_DLANGE3 Register (Address = 0x5F) [Default = 0x00]**PRBS\_ERROR\_COUNT\_DLANGE3 is shown in [Table 7-359](#).Return to the [Summary Table](#).

Pattern Generator CSI DI Register

**Table 7-359. PRBS\_ERROR\_COUNT\_DLANGE3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PRBS_ERR_CNT_D3	R	0x0	Number of bits errored during PRBS checking of DPHY Data Lane3

**7.6.2.3.53 CSI\_CFG0\_VC0 Register (Address = 0x80) [Default = 0x00]**CSI\_CFG0\_VC0 is shown in [Table 7-360](#).Return to the [Summary Table](#).

Pattern Generator Line Size Register 1

**Table 7-360. CSI\_CFG0\_VC0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R/W	0x0	reserved
5:2	OFMT	R/W	0x0	Output data format: 0000b= RGB888 0001b= RGB666 0010b= RGB565 0011b= YUV-420 0101b= YUV-422 (8-bit)
1:0	IFMT	R/W	0x0	Input data format: 00b= RGB 01b= YCbCr16

**7.6.2.3.54 CSI\_LINE\_LEN\_LSB\_VC0 Register (Address = 0x81) [Default = 0x00]**CSI\_LINE\_LEN\_LSB\_VC0 is shown in [Table 7-361](#).Return to the [Summary Table](#).

Pattern Generator Line Size Register 0

**Table 7-361. CSI\_LINE\_LEN\_LSB\_VC0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_LSB_VC0	R/W	0x0	CSI line length's 8 least significant bits

**7.6.2.3.55 CSI\_LINE\_LEN\_MSB\_VC0 Register (Address = 0x82) [Default = 0x00]**CSI\_LINE\_LEN\_MSB\_VC0 is shown in [Table 7-362](#).Return to the [Summary Table](#).

Pattern Generator Bar Size Register 1

**Table 7-362. CSI\_LINE\_LEN\_MSB\_VC0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_MSB_VC0	R/W	0x0	CSI line length's 8 most significant bits

**7.6.2.3.56 CSI\_CFG0\_VC1 Register (Address = 0x88) [Default = 0x00]**CSI\_CFG0\_VC1 is shown in [Table 7-363](#).Return to the [Summary Table](#).

Pattern Generator Bar Size Register 0

**Table 7-363. CSI\_CFG0\_VC1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R/W	0x0	reserved

**Table 7-363. CSI\_CFG0\_VC1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
5:2	OFMT	R/W	0x0	Output data format: 0000b= RGB888 0001b= RGB666 0010b= RGB565 0011b= YUV-420 0101b= YUV-422 (8-bit)
1:0	IFMT	R/W	0x0	Input data format: 00b= RGB 01b= YCbCr16

**7.6.2.3.57 CSI\_LINE\_LEN\_LSB\_VC1 Register (Address = 0x89) [Default = 0x00]**CSI\_LINE\_LEN\_LSB\_VC1 is shown in [Table 7-364](#).Return to the [Summary Table](#).

Pattern Generator Active LPF Register 1

**Table 7-364. CSI\_LINE\_LEN\_LSB\_VC1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_LSB_VC1	R/W	0x0	CSI line length's 8 least significant bits

**7.6.2.3.58 CSI\_LINE\_LEN\_MSB\_VC1 Register (Address = 0x8A) [Default = 0x00]**CSI\_LINE\_LEN\_MSB\_VC1 is shown in [Table 7-365](#).Return to the [Summary Table](#).

Pattern Generator Active LPF Register 0

**Table 7-365. CSI\_LINE\_LEN\_MSB\_VC1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_MSB_VC1	R/W	0x0	CSI line length's 8 most significant bits

**7.6.2.3.59 CSI\_CFG0\_VC2 Register (Address = 0x90) [Default = 0x00]**CSI\_CFG0\_VC2 is shown in [Table 7-366](#).Return to the [Summary Table](#).

Pattern Generator Total LPF Register 1

**Table 7-366. CSI\_CFG0\_VC2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R/W	0x0	reserved
5:2	OFMT	R/W	0x0	Output data format: 0000b= RGB888 0001b= RGB666 0010b= RGB565 0011b= YUV-420 0101b= YUV-422 (8-bit)
1:0	IFMT	R/W	0x0	Input data format: 00b= RGB 01b= YCbCr16

**7.6.2.3.60 CSI\_LINE\_LEN\_LSB\_VC2 Register (Address = 0x91) [Default = 0x00]**CSI\_LINE\_LEN\_LSB\_VC2 is shown in [Table 7-367](#).Return to the [Summary Table](#).

Pattern Generator Total LPF Register 0

**Table 7-367. CSI\_LINE\_LEN\_LSB\_VC2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_LSB_VC2	R/W	0x0	CSI line length's 8 least significant bits

**7.6.2.3.61 CSI\_LINE\_LEN\_MSB\_VC2 Register (Address = 0x92) [Default = 0x00]**CSI\_LINE\_LEN\_MSB\_VC2 is shown in [Table 7-368](#).Return to the [Summary Table](#).

Pattern Generator Line Period Register 1

**Table 7-368. CSI\_LINE\_LEN\_MSB\_VC2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_MSB_VC2	R/W	0x0	CSI line length's 8 most significant bits

**7.6.2.3.62 CSI\_CFG0\_VC3 Register (Address = 0x98) [Default = 0x00]**CSI\_CFG0\_VC3 is shown in [Table 7-369](#).Return to the [Summary Table](#).

Pattern Generator Line Period Register 0

**Table 7-369. CSI\_CFG0\_VC3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R/W	0x0	reserved
5:2	OFMT	R/W	0x0	Output data format: 0000b= RGB888 0001b= RGB666 0010b= RGB565 0011b= YUV-420 0101b= YUV-422 (8-bit)
1:0	IFMT	R/W	0x0	Input data format: 00b= RGB 01b= YCbCr16

**7.6.2.3.63 CSI\_LINE\_LEN\_LSB\_VC3 Register (Address = 0x99) [Default = 0x00]**CSI\_LINE\_LEN\_LSB\_VC3 is shown in [Table 7-370](#).Return to the [Summary Table](#).

Pattern Generator VBP Register

**Table 7-370. CSI\_LINE\_LEN\_LSB\_VC3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_LSB_VC3	R/W	0x0	CSI line length's 8 least significant bits

### 7.6.2.3.64 CSI\_LINE\_LEN\_MSB\_VC3 Register (Address = 0x9A) [Default = 0x00]

CSI\_LINE\_LEN\_MSB\_VC3 is shown in [Table 7-371](#).

Return to the [Summary Table](#).

Pattern Generator VFP Register

**Table 7-371. CSI\_LINE\_LEN\_MSB\_VC3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_MSB_VC3	R/W	0x0	CSI line length's 8 most significant bits

### 7.6.2.4 Page\_5:\_D-PHY\_Analog\_Port\_0 Registers

[Table 7-372](#) lists the memory-mapped registers for the Page\_5:\_D-PHY\_Analog\_Port\_0 registers. All register offset addresses not listed in [Table 7-372](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-372. PAGE\_5:\_D-PHY\_ANALOG\_PORT\_0 Registers**

Address	Acronym	Register Name	Section
0x16	DSI_POLARITY_SWAP_PORT_0	DSI_POLARITY_SWAP_PORT_0	<a href="#">Go</a>
0x21	SKEW_CAL_CFG0_P0	SKEW_CAL_CFG0_P0	<a href="#">Go</a>
0x2E	SKEW_CAL_CFG1_P0	SKEW_CAL_CFG1_P0	<a href="#">Go</a>
0x31	SKEW_CAL_CFG2_P0	SKEW_CAL_CFG2_P0	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. [Table 7-373](#) shows the codes that are used for access types in this section.

**Table 7-373. Page\_5:\_D-PHY\_Analog\_Port\_0 Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 7.6.2.4.1 DSI\_POLARITY\_SWAP\_PORT\_0 Register (Address = 0x16) [Default = 0x00]

DSI\_POLARITY\_SWAP\_PORT\_0 is shown in [Table 7-374](#).

Return to the [Summary Table](#).

**Table 7-374. DSI\_POLARITY\_SWAP\_PORT\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	DSI0_CLK_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI0 clock
3	DSI0_DATA3_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI0 lane 3
2	DSI0_DATA2_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI0 lane 2
1	DSI0_DATA1_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI0 lane 1
0	DSI0_DATA0_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI0 lane 0

**7.6.2.4.2 SKEW\_CAL\_CFG0\_P0 Register (Address = 0x21) [Default = 0xD0]**SKEW\_CAL\_CFG0\_P0 is shown in [Table 7-375](#).Return to the [Summary Table](#).**Table 7-375. SKEW\_CAL\_CFG0\_P0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x1	Reserved
6	RESERVED	R	0x1	Reserved
5	RESERVED	R	0x0	Reserved
4	SKEW_CAL_CFG0_P0	R/W	0x1	This register controls DSI skew calibration and its initial value is controlled by MODE_SEL1. 1: DSI skew calibration disabled (DSI_CAL_EN= 0) 0: DSI skew calibration enabled (DSI_CAL_EN= 1)
3:0	RESERVED	R	0x0	Reserved

**7.6.2.4.3 SKEW\_CAL\_CFG1\_P0 Register (Address = 0x2E) [Default = 0x00]**SKEW\_CAL\_CFG1\_P0 is shown in [Table 7-376](#).Return to the [Summary Table](#).**Table 7-376. SKEW\_CAL\_CFG1\_P0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	SKEW_CAL_CFG1_P0	R/W	0x0	This register controls DSI skew calibration and its initial value is controlled by MODE_SEL1. 0: DSI skew calibration disabled (DSI_CAL_EN= 0) 1: DSI skew calibration enabled (DSI_CAL_EN= 1)
5:0	RESERVED	R	0x0	Reserved

**7.6.2.4.4 SKEW\_CAL\_CFG2\_P0 Register (Address = 0x31) [Default = 0x02]**SKEW\_CAL\_CFG2\_P0 is shown in [Table 7-377](#).Return to the [Summary Table](#).**Table 7-377. SKEW\_CAL\_CFG2\_P0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	SKEW_CAL_CFG2_P0	R/W	0x1	This register controls DSI skew calibration and its initial value is controlled by MODE_SEL1. 1: DSI skew calibration disabled (DSI_CAL_EN= 0) 0: DSI skew calibration enabled (DSI_CAL_EN= 1)
0	RESERVED	R/W	0x0	Reserved

### 7.6.2.5 Page\_6\_D-PHY\_Digital\_Port\_1 Registers

Table 7-378 lists the memory-mapped registers for the Page\_6\_D-PHY\_Digital\_Port\_1 registers. All register offset addresses not listed in Table 7-378 should be considered as reserved locations and the register contents should not be modified.

**Table 7-378. PAGE\_6\_D-PHY\_DIGITAL\_PORT\_1 Registers**

Address	Acronym	Register Name	Section
0x1	DPHY_TINIT_TIMING	DPHY_TINIT_TIMING	Go
0x2	DPHY_TERM_TIMING	DPHY_TERM_TIMING	Go
0x3	DPHY_CLK_SETTLE_TIMING	DPHY_CLK_SETTLE_TIMING	Go
0x4	DPHY_HS_SETTLE_TIMING	DPHY_HS_SETTLE_TIMING	Go
0x5	DPHY_SKIP_TIMING	DPHY_SKIP_TIMING	Go
0x7	DPHY_BYPASS	DPHY_BYPASS	Go
0x8	HSRX_TO_CNT	HSRX_TO_CNT	Go
0x9	DPHY_CLK_PRP_ZERO_TIMING_G	DPHY_CLK_PRP_ZERO_TIMING	Go
0xD	INTR_CTL_DPHY	INTR_CTL_DPHY	Go
0xE	INTR_STS_DPHY	INTR_STS_DPHY	Go
0xF	DPHY_STATUS	DPHY_STATUS	Go
0x10	DPHY_DLANE0_ERR	DPHY_DLANE0_ERR	Go
0x11	DPHY_DLANE1_ERR	DPHY_DLANE1_ERR	Go
0x12	DPHY_DLANE2_ERR	DPHY_DLANE2_ERR	Go
0x13	DPHY_DLANE3_ERR	DPHY_DLANE3_ERR	Go
0x14	DPHY_ERR_CLK_LANE	DPHY_ERR_CLK_LANE	Go
0x15	DPHY_SYNC_STS	DPHY_SYNC_STS	Go
0x16	DPHY_FIFO_ERR	DPHY_FIFO_ERR	Go
0x17	DPHY_CLANE_DBG2	DPHY_CLANE_DBG2	Go
0x18	DPHY_CLANE_DBG	DPHY_CLANE_DBG	Go
0x19	DPHY_DLANE_DBG1	DPHY_DLANE_DBG1	Go
0x1A	DPHY_DLANE_DBG2	DPHY_DLANE_DBG2	Go
0x1B	DPHY_DLANE_DBG3	DPHY_DLANE_DBG3	Go
0x20	DPHY_DSI_CONFIG_0	DPHY_DSI_CONFIG_0	Go
0x21	DPHY_DSI_CONFIG_1	DPHY_DSI_CONFIG_1	Go
0x23	INTR_STS_DSI_ERR	INTR_STS_DSI_ERR	Go
0x24	INTR_STS_DPHY_ERR_FIFO_O_VR	INTR_STS_DPHY_ERR_FIFO_OVR	Go
0x25	INTR_CTL_DSI_ERR	INTR_CTL_DSI_ERR	Go
0x26	INTR_CTL_DPHY_ERR_FIFO_O_VR	INTR_CTL_DPHY_ERR_FIFO_OVR	Go
0x27	CFG_DSI_ERR_EN	CFG_DSI_ERR_EN	Go
0x28	CFG_DPHY_ERR_FIFO_OVR_E_N	CFG_DPHY_ERR_FIFO_OVR_EN	Go
0x29	DSI_DPHY_ERR_CNTR	DSI_DPHY_ERR_CNTR	Go
0x2A	DPHY_DSI_VC_DTYPE	DPHY_DSI_VC_DTYPE	Go
0x2E	DSI_VCID_STAT	DSI_VCID_STAT	Go
0x30	DSI_DATA_TYPE0	DSI_DATA_TYPE0	Go
0x31	DSI_DATA_TYPE1	DSI_DATA_TYPE1	Go
0x32	DSI_DATA_TYPE2	DSI_DATA_TYPE2	Go
0x33	DSI_DATA_TYPE3	DSI_DATA_TYPE3	Go

**Table 7-378. PAGE\_6\_D-PHY\_DIGITAL\_PORT\_1 Registers (continued)**

Address	Acronym	Register Name	Section
0x36	DPHY_DSI_EN_HSRX	DPHY_DSI_EN_HSRX	Go
0x37	DPHY_DSI_EN_LPRX	DPHY_DSI_EN_LPRX	Go
0x38	DPHY_DSI_EN_RXTERM_0	DPHY_DSI_EN_RXTERM_0	Go
0x39	DPHY_DSI_EN_RXTERM_1	DPHY_DSI_EN_RXTERM_1	Go
0x55	BRIDGE_CFG	BRIDGE_CFG	Go
0x57	TDM_CONFIG	TDM_CONFIG	Go
0x58	PRBS_CTRL_STATUS_DLANE0	PRBS_CTRL_STATUS_DLANE0	Go
0x59	PRBS_ERROR_COUNT_DLANE 0	PRBS_ERROR_COUNT_DLANE0	Go
0x5A	PRBS_STATUS_DLANE1	PRBS_STATUS_DLANE1	Go
0x5B	PRBS_ERROR_COUNT_DLANE 1	PRBS_ERROR_COUNT_DLANE1	Go
0x5C	PRBS_STATUS_DLANE2	PRBS_STATUS_DLANE2	Go
0x5D	PRBS_ERROR_COUNT_DLANE 2	PRBS_ERROR_COUNT_DLANE2	Go
0x5E	PRBS_STATUS_DLANE3	PRBS_STATUS_DLANE3	Go
0x5F	PRBS_ERROR_COUNT_DLANE 3	PRBS_ERROR_COUNT_DLANE3	Go
0x80	CSI_CFG0_VC0	CSI_CFG0_VC0	Go
0x81	CSI_LINE_LEN_LSB_VC0	CSI_LINE_LEN_LSB_VC0	Go
0x82	CSI_LINE_LEN_MSB_VC0	CSI_LINE_LEN_MSB_VC0	Go
0x88	CSI_CFG0_VC1	CSI_CFG0_VC1	Go
0x89	CSI_LINE_LEN_LSB_VC1	CSI_LINE_LEN_LSB_VC1	Go
0x8A	CSI_LINE_LEN_MSB_VC1	CSI_LINE_LEN_MSB_VC1	Go
0x90	CSI_CFG0_VC2	CSI_CFG0_VC2	Go
0x91	CSI_LINE_LEN_LSB_VC2	CSI_LINE_LEN_LSB_VC2	Go
0x92	CSI_LINE_LEN_MSB_VC2	CSI_LINE_LEN_MSB_VC2	Go
0x98	CSI_CFG0_VC3	CSI_CFG0_VC3	Go
0x99	CSI_LINE_LEN_LSB_VC3	CSI_LINE_LEN_LSB_VC3	Go
0x9A	CSI_LINE_LEN_MSB_VC3	CSI_LINE_LEN_MSB_VC3	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-379](#) shows the codes that are used for access types in this section.

**Table 7-379. Page\_6\_D-PHY\_Digital\_Port\_1 Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
<b>Write Type</b>		
W	W	Write
W1S	W 1S	Write 1 to set
<b>Reset or Default Value</b>		

**Table 7-379. Page\_6\_D-PHY\_Digital\_Port\_1 Access Type Codes (continued)**

Access Type	Code	Description
-n		Value after reset or the default value

#### 7.6.2.5.1 DPHY\_TINIT\_TIMING Register (Address = 0x1) [Default = 0x00]

DPHY\_TINIT\_TIMING is shown in [Table 7-380](#).

Return to the [Summary Table](#).

Pattern Generator Color 0 Register

**Table 7-380. DPHY\_TINIT\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	
2:0	TINIT_TIME	R/W	0x0	D-PHY Initialization Time after power up in 100us units Initialization time= (TINIT_TIME + 1) * 100us

#### 7.6.2.5.2 DPHY\_TERM\_TIMING Register (Address = 0x2) [Default = 0x00]

DPHY\_TERM\_TIMING is shown in [Table 7-381](#).

Return to the [Summary Table](#).

Pattern Generator Color 1 Register

**Table 7-381. DPHY\_TERM\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	DPHY_TERM_CLK_TIMING	R/W	0x0	Tclk TermEn terminal Count
3	RESERVED	R	0x0	Reserved
2:0	DPHY_TERM_DATA_TIMING	R/W	0x0	TD TermEn terminal Count

#### 7.6.2.5.3 DPHY\_CLK\_SETTLE\_TIMING Register (Address = 0x3) [Default = 0x1D]

DPHY\_CLK\_SETTLE\_TIMING is shown in [Table 7-382](#).

Return to the [Summary Table](#).

Pattern Generator Color 2 Register

**Table 7-382. DPHY\_CLK\_SETTLE\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	TCLK_SETTLE_CNT	R/W	0x1D	TCLK-SETTLE Tclk Settle terminal Count in units of 10ns

#### 7.6.2.5.4 DPHY\_HS\_SETTLE\_TIMING Register (Address = 0x4) [Default = 0x14]

DPHY\_HS\_SETTLE\_TIMING is shown in [Table 7-383](#).

Return to the [Summary Table](#).

Pattern Generator Color 3 Register

**Table 7-383. DPHY\_HS\_SETTLE\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	THS_SETTLE_CNT	R/W	0x14	THS-SETTLE Settle terminal Count in units of 10ns.

#### 7.6.2.5.5 DPHY\_SKIP\_TIMING Register (Address = 0x5) [Default = 0x3A]

DPHY\_SKIP\_TIMING is shown in [Table 7-384](#).

Return to the [Summary Table](#).

Pattern Generator Color 4 Register

**Table 7-384. DPHY\_SKIP\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:1	TSKIP_CNT	R/W	0x1D	Tskip Count This register controls the amount of data that will be ignored at the end of transmission detection. This value is in units of the DDR clock (i.e. two UI intervals). Setting of this register will be dependent on the D-PHY lane frequency.
0	RESERVED	R	0x0	Reserved

#### 7.6.2.5.6 DPHY\_BYPASS Register (Address = 0x7) [Default = 0x00]

DPHY\_BYPASS is shown in [Table 7-385](#).

Return to the [Summary Table](#).

Pattern Generator Color 5 Register

**Table 7-385. DPHY\_BYPASS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	BYPASS_TINIT	R/W	0x0	Bypass Tinit wait time
6	BYPASS_TCK_MISS	R/W	0x0	Bypass Tck Miss time
5	BYPASS_ULPS_CK0	R/W	0x0	Bypass ULPS for CLK0
4:0	BYPASS_LP	RH/W1S	0x0	Bypass Lp on clk and data lanes 3,2,1,0

#### 7.6.2.5.7 HSRX\_TO\_CNT Register (Address = 0x8) [Default = 0x00]

HSRX\_TO\_CNT is shown in [Table 7-386](#).

Return to the [Summary Table](#).

Pattern Generator Color 6 Register

**Table 7-386. HSRX\_TO\_CNT Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	HSRX_TO_CNT	R/W	0x0	Timeout counter in ms. The timer will have a 1 ms range; example: if HSRX_TO_CNT= 1, then the timeout will occur between 0-1ms and if HSRX_TO_CNT= 255, then the timeout will occur between 254-255ms. If the register value is 0, then the timeout will be off.

**7.6.2.5.8 DPHY\_CLK\_PRP\_ZERO\_TIMING Register (Address = 0x9) [Default = 0x1D]**DPHY\_CLK\_PRP\_ZERO\_TIMING is shown in [Table 7-387](#).Return to the [Summary Table](#).

Pattern Generator Color 7 Register

**Table 7-387. DPHY\_CLK\_PRP\_ZERO\_TIMING Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	TCLK_PRP_ZERO_CNT	R/W	0x1D	TCLK-SETTLE TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock. ( in units of 10ns)

**7.6.2.5.9 INTR\_CTL\_DPHY Register (Address = 0xD) [Default = 0x00]**INTR\_CTL\_DPHY is shown in [Table 7-388](#).Return to the [Summary Table](#).

Pattern Generator Color 8 Register

**Table 7-388. INTR\_CTL\_DPHY Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	IE_DPHY_LANE_SYNC_ERROR	R/W	0x0	Enables interrupt for lane sync error
0	IE_DPHY_LANE_ERROR	R/W	0x0	Enables interrupt for lane error

**7.6.2.5.10 INTR\_STS\_DPHY Register (Address = 0xE) [Default = 0x00]**INTR\_STS\_DPHY is shown in [Table 7-389](#).Return to the [Summary Table](#).

Pattern Generator Color 9 Register

**Table 7-389. INTR\_STS\_DPHY Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	IS_DPHY_LANE_SYNC_ERROR	RC	0x0	Interrupt status for D-PHY Lane Sync Error This flag indicates the proper synchronization was not detected on all data lanes at the same time. Each enabled lane is expected to detect the sync sequence at the same time. If this does not occur correctly, this flag will be set. In addition, the DPHY_SYNC_STS register may be read to determine the synchronization status at the most recent error condition.
0	IS_DPHY_LANE_ERROR	RC	0x0	Interrupt status for D-PHY Lane Error Detected If this bit is set, one or more of the clock or data lanes has detected an error. To determine the error, read the DPHY_DLАНEx_ERR and DPHY_CLANE_ERR registers. This flag will be cleared when the Lane Error registers have been read.

**7.6.2.5.11 DPHY\_STATUS Register (Address = 0xF) [Default = 0x00]**DPHY\_STATUS is shown in [Table 7-390](#).Return to the [Summary Table](#).

Pattern Generator Color 10 Register

**Table 7-390. DPHY\_STATUS Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	C_LANE_ACTIVE	R	0x0	Clock Lane Active 0: Clock Lane not active 1: Clock Lane active Once the TINIT_TIME expires and the dphy calibration is done for all the lanes, this bit remains set to 1.
3:0	D_LANE_ACTIVE	R	0x0	Data Lanes Active For each data lane, this register reports if the lane is detected as active. There are no timers associated with it for inactive lane detection. 0: Data Lane is not active 1: Data Lane is active Once the TINIT_TIME expires and the dphy calibration is done for all the lanes, this bit reflects the number of DPHY lanes selected in the BRIDGE_CTL reg of Main page.

**7.6.2.5.12 DPHY\_DLANE0\_ERR Register (Address = 0x10) [Default = 0x00]**DPHY\_DLANE0\_ERR is shown in [Table 7-391](#).Return to the [Summary Table](#).

Pattern Generator Color 11 Register

**Table 7-391. DPHY\_DLANE0\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	EOT_SYNC_ERROR_0	RC	0x0	End of transmission sync error - Uncorrectable
3	SOT ERROR_0	RC	0x0	Bit Error in SYNC Sequence - Correctable
2	SOT SYNC ERROR_0	RC	0x0	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_0	RC	0x0	Control Error in HS Request Mode This error happens in a DPHY data lane when lpx of the corresponding data lane doesn't transition from 2'b01 to 2'b00 during LP to HS transition.
0	HS RX TO ERROR_0	RC	0x0	HS Transmission timeout error During the HS mode of data, if the hsrx_to_cnt (in ms) is reached, HS RX TO ERROR_0 bit is set. The counter will be reset upon entering LP.

**7.6.2.5.13 DPHY\_DLANE1\_ERR Register (Address = 0x11) [Default = 0x00]**DPHY\_DLANE1\_ERR is shown in [Table 7-392](#).Return to the [Summary Table](#).

Pattern Generator Color 12 Register

**Table 7-392. DPHY\_DLANE1\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	EOT_SYNC_ERROR_1	RC	0x0	End of transmission sync error - Uncorrectable
3	SOT ERROR_1	RC	0x0	Bit Error in SYNC Sequence - Correctable

**Table 7-392. DPHY\_DLANE1\_ERR Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2	SOT SYNC ERROR_1	RC	0x0	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_1	RC	0x0	Control Error in HS Request Mode This error happens in a DPHY data lane when lpx of the corresponding data lane doesn't transition from 2'b01 to 2'b00 during LP to HS transition.
0	HS RX TO ERROR_1	RC	0x0	HS Transmission timeout error During the HS mode of data, if the hsrx_to_cnt (in ms) is reached, HS RX TO ERROR_0 bit is set. The counter will be reset upon entering LP.

**7.6.2.5.14 DPHY\_DLANE2\_ERR Register (Address = 0x12) [Default = 0x00]**DPHY\_DLANE2\_ERR is shown in [Table 7-393](#).Return to the [Summary Table](#).

Pattern Generator Color 13 Register

**Table 7-393. DPHY\_DLANE2\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	EOT_SYNC_ERROR_2	RC	0x0	End of transmission sync error - Uncorrectable
3	SOT ERROR_2	RC	0x0	Bit Error in SYNC Sequence - Correctable
2	SOT SYNC ERROR_2	RC	0x0	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_2	RC	0x0	Control Error in HS Request Mode
0	HS RX TO ERROR_2	RC	0x0	HS Transmission timeout error

**7.6.2.5.15 DPHY\_DLANE3\_ERR Register (Address = 0x13) [Default = 0x00]**DPHY\_DLANE3\_ERR is shown in [Table 7-394](#).Return to the [Summary Table](#).

Pattern Generator Color 14 Register

**Table 7-394. DPHY\_DLANE3\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	EOT_SYNC_ERROR_3	RC	0x0	End of transmission sync error - Uncorrectable
3	SOT ERROR_3	RC	0x0	Bit Error in SYNC Sequence - Correctable
2	SOT SYNC ERROR_3	RC	0x0	SYNC Sequence Error - Uncorrectable
1	CNTRL_ERR_HSRQST_3	RC	0x0	Control Error in HS Request Mode
0	HS RX TO ERROR_3	RC	0x0	HS Transmission timeout error

**7.6.2.5.16 DPHY\_ERR\_CLK\_LANE Register (Address = 0x14) [Default = 0x00]**DPHY\_ERR\_CLK\_LANE is shown in [Table 7-395](#).Return to the [Summary Table](#).

Pattern Generator Color 15 Register

**Table 7-395. DPHY\_ERR\_CLK\_LANE Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	CNTRL_ERR_HSRQST_CLK	RC	0x0	Control Error in HS Request Mode This error happens in a DPHY clock lane when lpx of the clock data lane doesn't transition from 2'b01 to 2'b00 during LP to HS transition.
1	RESERVED	R	0x0	Reserved
0	HS RX TO ERROR_CLK	RC	0x0	HS Transmission timeout error During the HS mode of clock, if the hsrx_to_cnt (in ms) is reached, HS RX TO ERROR_0 bit is set. The counter will be reset upon entering LP.

**7.6.2.5.17 DPHY\_SYNC\_STS Register (Address = 0x15) [Default = 0x00]**DPHY\_SYNC\_STS is shown in [Table 7-396](#).Return to the [Summary Table](#).**Table 7-396. DPHY\_SYNC\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	DLANE3_SYNC_STS	R	0x0	Sync Status for DLANE 3 Reports synchronization status for Data Lane 3 during most recent Synchronization error When only some of DPHY data lanes have received SoT byte (0xB8) while the others haven't, these bits reflect the sync received status of the DPHY data lanes.
2	DLANE2_SYNC_STS	R	0x0	Sync Status for DLANE 2 Reports synchronization status for Data Lane 3 during most recent Synchronization error
1	DLANE1_SYNC_STS	R	0x0	Sync Status for DLANE 1 Reports synchronization status for Data Lane 3 during most recent Synchronization error
0	DLANE0_SYNC_STS	R	0x0	Sync Status for DLANE 0 Reports synchronization status for Data Lane 3 during most recent Synchronization error

**7.6.2.5.18 DPHY\_FIFO\_ERR Register (Address = 0x16) [Default = 0x00]**DPHY\_FIFO\_ERR is shown in [Table 7-397](#).Return to the [Summary Table](#).

Pattern Generator Control Register

**Table 7-397. DPHY\_FIFO\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	DLANE3_FIFO_OVERFL OW	RC	0x0	FIFO Overflow Error for DLANE3 Data from the DLANE FIFOs are read only when each of the enabled lanes has received data. If one or more of the enabled data lanes did not receive SoT byte, the FIFOs of the other DLANES will overflow. These register bits reflect the status of the DLANE FIFOs that overflowed.
2	DLANE2_FIFO_OVERFL OW	RC	0x0	FIFO Overflow Error for DLANE2

**Table 7-397. DPHY\_FIFO\_ERR Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	DLANE1_FIFO_OVERFL OW	RC	0x0	FIFO Overflow Error for DLANE1
0	DLANE0_FIFO_OVERFL OW	RC	0x0	FIFO Overflow Error for DLANE0

**7.6.2.5.19 DPHY\_CLANE\_DBG2 Register (Address = 0x17) [Default = 0x00]**DPHY\_CLANE\_DBG2 is shown in [Table 7-398](#).[Return to the Summary Table.](#)

Pattern Generator Configuration Register

**Table 7-398. DPHY\_CLANE\_DBG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	RESERVED	R	0x0	
0	BYPASS_TPRP_ZERO_C NTR_CLANE_OV	R/W	0x0	If CLANE_OVERRIDE is set, a value of 1 on this bit will force clk_prp_zero_flag

**7.6.2.5.20 DPHY\_CLANE\_DBG Register (Address = 0x18) [Default = 0x00]**DPHY\_CLANE\_DBG is shown in [Table 7-399](#).[Return to the Summary Table.](#)

Pattern Generator CSI DI Register

**Table 7-399. DPHY\_CLANE\_DBG Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CLANE_OVERRIDE	R/W	0x0	Override Clock Lane State The Clock Lane State Machine is forced to the state specified by the value in CLANE_STATE field
6	CLANE_HSRX_TO_DISABLE	R/W	0x0	Disables the HS RX Timeout option only within the clock lane. This is to help when running in continuous clock mode. The Data lanes can still check for the timeout, but the clock lane will not cause an error
5	BYPASS_TSETTLE_CNT R_CLANE_OV	R/W	0x0	If CLANE_OVERRIDE is set, a value of 1 on this bit will force clk_settle_flag
4	BYPASS_TERMEN_CNT R_CLANE_OV	R/W	0x0	If CLANE_OVERRIDE is set, a value of 1 on this bit will force lineterm_flag
3:0	CLANE_STATE	R/W	0x0	If CLANE_OVERRIDE is set, this value is used for forcing the Clock Lane State Machine

**7.6.2.5.21 DPHY\_DLANE\_DBG1 Register (Address = 0x19) [Default = 0x04]**DPHY\_DLANE\_DBG1 is shown in [Table 7-400](#).[Return to the Summary Table.](#)

Pattern Generator Line Size Register 1

**Table 7-400. DPHY\_DLANE\_DBG1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	BYPASS_SYNC_SEQ_DE TECT	R/W	0x0	Force sync_detect for all active Data Lanes

**Table 7-400. DPHY\_DLANE\_DBG1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
5	BYPASS_TSETTLE_CNT_R_HSSYNC	R/W	0x0	Force hssync_en_flag for all active Data Lanes
4	BYPASS_TERMEN_CNT_R_HSSYNC	R/W	0x0	Force lineterm_flag for all active Data Lanes
3	BYPASS_VALID_SYNC_DETECT	R/W	0x0	Bypass Valid Sync Detect This bit controls whether a LANE_SYNC_ERROR will prevent DPHY video reception. By default, all data lanes are expected to detect synchronization almost at the same time. If they do not, video reception is normally disabled. 0: Require synchronization across all enabled lanes 1: Forward video if synchronization check fails
2	LEADER_SEQ_MODE	R/W	0x1	Leader Sequence Detect Mode This bit controls detection of the Leader Sequence for synchronization on the DPHY data lanes. 0: Less Restrictive detection (allow single bit errors within an 8-bit window) 1: More Restrictive detection (allow single bit error within the first 6-bits following the HS_ZERO data)
1:0	RESERVED	R	0x0	

**7.6.2.5.22 DPHY\_DLANE\_DBG2 Register (Address = 0x1A) [Default = 0x00]**DPHY\_DLANE\_DBG2 is shown in [Table 7-401](#).Return to the [Summary Table](#).

Pattern Generator Line Size Register 0

**Table 7-401. DPHY\_DLANE\_DBG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DLANE_STATE_OVERRIDE	R/W	0x0	Override Data Lane State Vector
6:5	RESERVED	R	0x0	
4:0	DLANE_STATE_VAL	R/W	0x0	If DLANE_STATE_OVERRIDE is set, this value is used for forcing the Data Lane State Machine for all active Data Lanes

**7.6.2.5.23 DPHY\_DLANE\_DBG3 Register (Address = 0x1B) [Default = 0x00]**DPHY\_DLANE\_DBG3 is shown in [Table 7-402](#).Return to the [Summary Table](#).

Pattern Generator Bar Size Register 1

**Table 7-402. DPHY\_DLANE\_DBG3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_PROT_STATE_OVERRIDE	R/W	0x0	Override DSI Protocol State Vector
6:4	RESERVED	R	0x0	
3:0	DSI_PROT_STATE_VAL	R/W	0x0	If DSI_PROT_STATE_OVERRIDE is set, this value is used for forcing the DSI_PROT_STATE_OVERRIDE State Machine

**7.6.2.5.24 DPHY\_DSI\_CONFIG\_0 Register (Address = 0x20) [Default = 0x4F]**DPHY\_DSI\_CONFIG\_0 is shown in [Table 7-403](#).

Return to the [Summary Table](#).

Pattern Generator Bar Size Register 0

**Table 7-403. DPHY\_DSI\_CONFIG\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	DSI_TRY_RECOVERY	R/W	0x1	DSI Attempt Recovery When set to a 1, the DSI Protocol module will attempt to recover from error conditions.
5	RESERVED	R	0x0	Reserved
4	DSI_SYNC_PULSE_MODE	R/W	0x0	Controls generation of Sync Pulses 0: Event mode (Hsync end and Vsync end packets are ignored); Used in burst mode 1: Pulse mode
3:0	DSI_VC_ENABLE	R/W	0xF	Enable VC-IDs Each bit in this four bit field enables one of the four Virtual Channel IDs. If a packet was received without an expected VC-ID, an error will be reported. For the error to be reported in the DSI_ERR_DET bit, the DSI_INV_VC_ERR_EN bit must also be set. These controls do not filter out packets with invalid VC-IDs.

#### 7.6.2.5.25 DPHY\_DSI\_CONFIG\_1 Register (Address = 0x21) [Default = 0x00]

DPHY\_DSI\_CONFIG\_1 is shown in [Table 7-404](#).

Return to the [Summary Table](#).

Pattern Generator Active LPF Register 1

**Table 7-404. DPHY\_DSI\_CONFIG\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_NO_GRAYSCALE	R/W	0x0	Disable Grayscale Interpolation For DSI RGB data types less than 24 bits, the conversion to RGB888 replicates the most significant subpixel bits on the otherwise-unused least significant subpixel bits in order to achieve a higher grayscale range. 0: Enable Grayscale Interpolation 1: Disable Grayscale Interpolation
6:3	RESERVED	R	0x0	Reserved
3	DSI_NULL_CRC_DIS	R/W	0x0	Error reporting for NULL and BLANK long packets; when set CRC errors in DSI/CSI packets are ignored
2:1	RESERVED	R	0x0	Reserved
0	DSI_NO_EOTPKT	R/W	0x0	No EOT Packet mode If set to 0, the device will indicate an error if an End of Transmission occurs without an EOT Packet. If set to 0, no error will be indicated. The error is indicated in the DPHY_ERR_FIFO_OVR status register.

#### 7.6.2.5.26 INTR\_STS\_DSI\_ERR Register (Address = 0x23) [Default = 0x00]

INTR\_STS\_DSI\_ERR is shown in [Table 7-405](#).

Return to the [Summary Table](#).

Pattern Generator Active LPF Register 0

**Table 7-405. INTR\_STS\_DSI\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IS_INV_TYPE_GLW_ERR	RC	0x0	Received Invalid Type on Generic Long Write packet

**Table 7-405. INTR\_STS\_DSI\_ERR Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	IS_INV_WC_GLW_ERR	RC	0x0	Received Invalid Word Count on Generic Long Write packet
5	IS_INV_LEN_ERR	RC	0x0	Received HS to LP prior to consuming the number of bytes as indicated by the Word Count in the recent DSI/CSI packet.
4	IS_INV_VC_ERR	RC	0x0	Received DSI/CSI packet with a VC that has been disabled
3	IS_INV_DT_ERR	RC	0x0	Received V/H_SYNC END in the pulse mode configuration OR any other unsupported Data Type
2	IS_CHECKSUM_ERR	RC	0x0	CHECKSUM error status for a received DSI/CSI packet
1	IS_ECC_MULTI_ERR	RC	0x0	Multi bit of ECC error received on a DSI/CSI packet header (not correctable by the hardware)
0	IS_ECC_SINGLE_ERR	RC	0x0	Single bit of ECC error received on a DSI/CSI packet header (corrected by the hardware)

**7.6.2.5.27 INTR\_STS\_DPHY\_ERR\_FIFO\_OVR Register (Address = 0x24) [Default = 0x00]**INTR\_STS\_DPHY\_ERR\_FIFO\_OVR is shown in [Table 7-406](#).Return to the [Summary Table](#).

Pattern Generator Total LPF Register 1

**Table 7-406. INTR\_STS\_DPHY\_ERR\_FIFO\_OVR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IS_DATA_TYPE_OVR	RC	0x0	DSI DATA TYPE register overflow status. When set, indicates that all the DSI_DATA_TYPE registers are valid and a new data_type has been received on DSI/CSI long packet, effectively having no space to save the data_type.
6	IS_I2C_WR_OVR	RC	0x0	I2C Write FIFO overflow status
5	IS_SDP_WR_OVR	RC	0x0	SD Write FIFO overflow status
4	IS_DPHY_FIFO_OVR	RC	0x0	One of the DPHY's DLANE FIFO overflow status
3	IS_EOT_WITHOUT_EOT_P	RC	0x0	Received EoT without EoTP
2	IS_EOT_SYNC_ERR	RC	0x0	EOT_SYNC_ERR status within dsi_core_prot
1	IS_SOT_SYNC_ERR	RC	0x0	SOT_SYNC_ERR status within dsi_core_prot
0	IS_SOT_ERR	RC	0x0	SOT_ERR status within dsi_core_prot

**7.6.2.5.28 INTR\_CTL\_DSI\_ERR Register (Address = 0x25) [Default = 0x00]**INTR\_CTL\_DSI\_ERR is shown in [Table 7-407](#).Return to the [Summary Table](#).

Pattern Generator Total LPF Register 0

**Table 7-407. INTR\_CTL\_DSI\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IE_INV_TYPE_GLW_ERR	R/W	0x0	Enables INV_TYPE_GLW_ERR
6	IE_INV_WC_GLW_ERR	R/W	0x0	Enables INV_WC_GLW_ERR
5	IE_INV_LEN_ERR	R/W	0x0	Enables INV_LEN_ERR
4	IE_INV_VC_ERR	R/W	0x0	Enables INV_VC_ERR
3	IE_INV_DT_ERR	R/W	0x0	Enables INV_DT_ERR
2	IE_CHECKSUM_ERR	R/W	0x0	Enables CHECKSUM_ERR
1	IE_ECC_MULTI_ERR	R/W	0x0	Enables ECC_MULTI_ERR

**Table 7-407. INTR\_CTL\_DSI\_ERR Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	IE_ECC_SINGLE_ERR	R/W	0x0	Enables ECC_SINGLE_ERR

**7.6.2.5.29 INTR\_CTL\_DPHY\_ERR\_FIFO\_OVR Register (Address = 0x26) [Default = 0x00]**INTR\_CTL\_DPHY\_ERR\_FIFO\_OVR is shown in [Table 7-408](#).Return to the [Summary Table](#).

Pattern Generator Line Period Register 1

**Table 7-408. INTR\_CTL\_DPHY\_ERR\_FIFO\_OVR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	IE_DATA_TYPE_OVR	R/W	0x0	Enables DATA_TYPE_OVR
6	IE_I2C_WR_OVR	R/W	0x0	Enables I2C_WR_OVR
5	IE_SDP_WR_OVR	R/W	0x0	Enables SDP_WR_OVR
4	IE_DPHY_FIFO_OVR	R/W	0x0	Enables DPHY_FIFO_OVR
3	IE_EOT_WITHOUT_EOTP	R/W	0x0	Enables EOT_WITHOUT_EOTP
2	IE_EOT_SYNC_ERR	R/W	0x0	Enables EOT_SYNC_ERR
1	IE_SOT_SYNC_ERR	R/W	0x0	Enables SOT_SYNC_ERR
0	IE_SOT_ERR	R/W	0x0	Enables SOT_ERR

**7.6.2.5.30 CFG\_DSI\_ERR\_EN Register (Address = 0x27) [Default = 0x00]**CFG\_DSI\_ERR\_EN is shown in [Table 7-409](#).Return to the [Summary Table](#).

Pattern Generator Line Period Register 0

**Table 7-409. CFG\_DSI\_ERR\_EN Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CFG_EN_INV_TYPE_GLW_ERR	R/W	0x0	Enables INV_TYPE_GLW_ERR to be included in INTR_STS_DSI_ERR
6	CFG_EN_INV_WC_GLW_ERR	R/W	0x0	Enables INV_WC_GLW_ERR to be included in INTR_STS_DSI_ERR
5	CFG_EN_INV_LEN_ERR	R/W	0x0	Enables INV_LEN_ERR to be included in INTR_STS_DSI_ERR
4	CFG_EN_INV_VC_ERR	R/W	0x0	Enables INV_VC_ERR to be included in INTR_STS_DSI_ERR
3	CFG_EN_INV_DT_ERR	R/W	0x0	Enables INV_DT_ERR to be included in INTR_STS_DSI_ERR
2	CFG_EN_CHECKSUM_ERR	R/W	0x0	Enables IE_CHECKSUM_ERR to be included in INTR_STS_DSI_ERR
1	CFG_EN_ECC_MULTI_ERR	R/W	0x0	Enables IE_ECC_MULTI_ERR to be included in INTR_STS_DSI_ERR
0	CFG_EN_ECC_SINGLE_ERR	R/W	0x0	Enables ECC_SINGLE_ERR to be included in INTR_STS_DSI_ERR

**7.6.2.5.31 CFG\_DPHY\_ERR\_FIFO\_OVR\_EN Register (Address = 0x28) [Default = 0x00]**CFG\_DPHY\_ERR\_FIFO\_OVR\_EN is shown in [Table 7-410](#).Return to the [Summary Table](#).

Pattern Generator VBP Register

**Table 7-410. CFG\_DPHY\_ERR\_FIFO\_OVR\_EN Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CFG_EN_DATA_TYPE_OVR	R/W	0x0	Enables IE_DATA_TYPE_OVR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
6	CFG_EN_I2C_WR_OVR	R/W	0x0	Enables IE_I2C_WR_OVR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
5	CFG_EN_SDP_WR_OVR	R/W	0x0	Enables IE_SDP_WR_OVR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
4	CFG_EN_DPHY_FIFO_OVR	R/W	0x0	Enables IE_DPHY_FIFO_OVR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
3	CFG_EN_EOT_WITHOUT_EOTP	R/W	0x0	Enables IE_EOT_WITHOUT_EOTP to be included in INTR_STS_DPHY_ERR_FIFO_OVR
2	CFG_EN_EOT_SYNC_ERR	R/W	0x0	Enables IE_EOT_SYNC_ERR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
1	CFG_EN_SOT_SYNC_ERR	R/W	0x0	Enables IE_SOT_SYNC_ERR to be included in INTR_STS_DPHY_ERR_FIFO_OVR
0	CFG_EN_SOT_ERR	R/W	0x0	Enables IE_SOT_ERR to be included in INTR_STS_DPHY_ERR_FIFO_OVR

**7.6.2.5.32 DSI\_DPHY\_ERR\_CNTR Register (Address = 0x29) [Default = 0x00]**DSI\_DPHY\_ERR\_CNTR is shown in [Table 7-411](#).Return to the [Summary Table](#).

Pattern Generator VFP Register

**Table 7-411. DSI\_DPHY\_ERR\_CNTR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	DSI_DPHY_ERROR_COUNT	RC	0x0	DSI Error Count This register reports the number of errors that have been detected on any of the status bits of INTR_STS_DSI_ERR or INTR_STS_DPHY_ERR_FIFO_OVR status registers. This value will be cleared on read.

**7.6.2.5.33 DPHY\_DSI\_VC\_DTYPE Register (Address = 0x2A) [Default = 0x00]**DPHY\_DSI\_VC\_DTYPE is shown in [Table 7-412](#).Return to the [Summary Table](#).

Pattern Generator Color 0 Register

**Table 7-412. DPHY\_DSI\_VC\_DTYPE Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	DSI_VC	R	0x0	DSI Virtual Channel ID This field returns the Virtual Channel ID for the most recently received pixel stream packet. This field is updated by the DSI Protocol logic whenever a packet header is detected with the lower 4 bits of the DTYPE in the range of 0xB to 0xE.
5:0	DSI_DTYPE	R	0x0	DSI Data Type This field returns the Data Type for the most recently received pixel stream packet. This field is updated by the DSI Protocol logic whenever a packet header is detected with the lower 4 bits of the DTYPE in the range of 0xB to 0xE.

### 7.6.2.5.34 DSI\_VCID\_STAT Register (Address = 0x2E) [Default = 0x00]

DSI\_VCID\_STAT is shown in [Table 7-413](#).

Return to the [Summary Table](#).

Pattern Generator Color 1 Register

**Table 7-413. DSI\_VCID\_STAT Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_VCID_STAT_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 7 of this register. Clearing of individual bits of DSI_VCID_STAT is not supported.
6:4	RESERVED	R	0x0	Reserved
3:0	DSI_VCID_STAT	R	0x0	Each bit of this field corresponds to a VC. When a DSI/CSI short/long packet is received, the VCID is captured in the corresponding bit in this register.

### 7.6.2.5.35 DSI\_DATA\_TYPE0 Register (Address = 0x30) [Default = 0x00]

DSI\_DATA\_TYPE0 is shown in [Table 7-414](#).

Return to the [Summary Table](#).

Pattern Generator Color 2 Register

**Table 7-414. DSI\_DATA\_TYPE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_DATA_TYPE0_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 0 of this register.
6	DSI_DATA_TYPE0_VLD	R	0x0	When set, this bit validates bits 5:0 of this register.
5:0	DSI_DATA_TYPE0	R	0x0	A unique DSI DATA TYPE captured on a DSI/CSI long packet. This field can be cleared by writing a 1 into bit 7 of this register.

### 7.6.2.5.36 DSI\_DATA\_TYPE1 Register (Address = 0x31) [Default = 0x00]

DSI\_DATA\_TYPE1 is shown in [Table 7-415](#).

Return to the [Summary Table](#).

Pattern Generator Color 3 Register

**Table 7-415. DSI\_DATA\_TYPE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_DATA_TYPE1_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 0 of this register.
6	DSI_DATA_TYPE1_VLD	R	0x0	When set, this bit validates bits 5:0 of this register.
5:0	DSI_DATA_TYPE1	R	0x0	A unique DSI DATA TYPE captured on a DSI/CSI long packet. This field can be cleared by writing a 1 into bit 7 of this register.

### 7.6.2.5.37 DSI\_DATA\_TYPE2 Register (Address = 0x32) [Default = 0x00]

DSI\_DATA\_TYPE2 is shown in [Table 7-416](#).

Return to the [Summary Table](#).

Pattern Generator Color 4 Register

**Table 7-416. DSI\_DATA\_TYPE2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_DATA_TYPE2_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 0 of this register.

**Table 7-416. DSI\_DATA\_TYPE2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	DSI_DATA_TYPE2_VLD	R	0x0	When set, this bit validates bits 5:0 of this register.
5:0	DSI_DATA_TYPE2	R	0x0	A unique DSI DATA TYPE captured on a DSI/CSI long packet. This field can be cleared by writing a 1 into bit 7 of this register.

**7.6.2.5.38 DSI\_DATA\_TYPE3 Register (Address = 0x33) [Default = 0x00]**DSI\_DATA\_TYPE3 is shown in [Table 7-417](#).Return to the [Summary Table](#).

Pattern Generator Color 5 Register

**Table 7-417. DSI\_DATA\_TYPE3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	DSI_DATA_TYPE3_CLR	RH/W1S	0x0	This register can be cleared by writing a 1 into bit 0 of this register.
6	DSI_DATA_TYPE3_VLD	R	0x0	When set, this bit validates bits 5:0 of this register.
5:0	DSI_DATA_TYPE3	R	0x0	A unique DSI DATA TYPE captured on a DSI/CSI long packet. This field can be cleared by writing a 1 into bit 7 of this register.

**7.6.2.5.39 DPHY\_DSI\_EN\_HSRX Register (Address = 0x36) [Default = 0x00]**DPHY\_DSI\_EN\_HSRX is shown in [Table 7-418](#).Return to the [Summary Table](#).

Pattern Generator Color 6 Register

**Table 7-418. DPHY\_DSI\_EN\_HSRX Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	EN_HSRX_OV	R/W	0x0	Overwrite to enable CSI RX HS receiver
5	RESERVED	R	0x0	Reserved
4	EN_HSRX_CLK0	R/W	0x0	Enable HSRX CLK0
3	EN_HSRX_D3	R/W	0x0	Enable HSRX D3
2	EN_HSRX_D2	R/W	0x0	Enable HSRX D2
1	EN_HSRX_D1	R/W	0x0	Enable HSRX D1
0	EN_HSRX_D0	R/W	0x0	Enable HSRX D0

**7.6.2.5.40 DPHY\_DSI\_EN\_LPRX Register (Address = 0x37) [Default = 0x00]**DPHY\_DSI\_EN\_LPRX is shown in [Table 7-419](#).Return to the [Summary Table](#).

Pattern Generator Color 7 Register

**Table 7-419. DPHY\_DSI\_EN\_LPRX Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	EN_LPRX_OV	R/W	0x0	Overwrite CSI LP Receiver
5	RESERVED	R	0x0	Reserved
4	EN_LPRX_CLK0	R/W	0x0	Enable LP Receiver for CLK0
3	EN_LPRX_D3	R/W	0x0	Enable LP Receiver for D3

**Table 7-419. DPHY\_DSI\_EN\_LPRX Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2	EN_LPRX_D2	R/W	0x0	Enable LP Receiver for D2
1	EN_LPRX_D1	R/W	0x0	Enable LP Receiver for D1
0	EN_LPRX_D0	R/W	0x0	Enable LP Receiver for D0

**7.6.2.5.41 DPHY\_DSI\_EN\_RXTERM\_0 Register (Address = 0x38) [Default = 0x00]**DPHY\_DSI\_EN\_RXTERM\_0 is shown in [Table 7-420](#).Return to the [Summary Table](#).

Pattern Generator Color 8 Register

**Table 7-420. DPHY\_DSI\_EN\_RXTERM\_0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	EN_RXTERM_OV	R/W	0x0	Overwrite CSI RX HS Termination
5	RESERVED	R	0x0	Reserved
4	EN_RXTERM_CLK0	R/W	0x0	Enable RX Termination for CSI CLK0
3	EN_RXTERM_D3	R/W	0x0	Enable RX Termination for CSI D3
2	EN_RXTERM_D2	R/W	0x0	Enable RX Termination for CSI D2
1	EN_RXTERM_D1	R/W	0x0	Enable RX Termination for CSI D1
0	EN_RXTERM_D0	R/W	0x0	Enable RX Termination for CSI D0

**7.6.2.5.42 DPHY\_DSI\_EN\_RXTERM\_1 Register (Address = 0x39) [Default = 0x00]**DPHY\_DSI\_EN\_RXTERM\_1 is shown in [Table 7-421](#).Return to the [Summary Table](#).

Pattern Generator Color 9 Register

**Table 7-421. DPHY\_DSI\_EN\_RXTERM\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	DPHY_CLRZ_OV	R/W	0x0	Overwrite DPHY_CLRZ
5:4	RESERVED	R	0x0	Reserved
3	DPHY_CLRZ_D3	R/W	0x0	Set DPHY_CLRZ for CSI D3
2	DPHY_CLRZ_D2	R/W	0x0	Set DPHY_CLRZ for CSI D2
1	DPHY_CLRZ_D1	R/W	0x0	Set DPHY_CLRZ for CSI D1
0	DPHY_CLRZ_D0	R/W	0x0	Set DPHY_CLRZ for CSI D0

**7.6.2.5.43 BRIDGE\_CFG Register (Address = 0x55) [Default = 0x00]**BRIDGE\_CFG is shown in [Table 7-422](#).Return to the [Summary Table](#).

Pattern Generator Color 10 Register

**Table 7-422. BRIDGE\_CFG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

**Table 7-422. BRIDGE\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
5:4	DSI_BYTES_PER_PIXEL	R/W	0x0	Number of DSI Bytes Per Pixel: For Continuous Clock Mode, selects the number of DSI bytes per pixel for the desired DSI Data Type 00: 3 bytes/pixel (RGB888, RGB666 loosely packed, 20b YCbCr 4:2:2, 24b YCbCr 4:2:2, 12b YCbCr 4:2:0, Compressed) 01: 2.25 bytes/pixel (RGB666 packed) 10: 2 bytes/pixel (RGB565, 16b YCbCr 4:2:2) 11: Reserved Notes: All RGB formats are converted to RGB888. YCbCr and Compressed formats are passed through unconverted In Independent DSI to FPD3 mode, this controls affects the selected port.
3:0	RESERVED	R	0x0	Reserved

**7.6.2.5.44 TDM\_CONFIG Register (Address = 0x57) [Default = 0x02]**TDM\_CONFIG is shown in [Table 7-423](#).Return to the [Summary Table](#).

Pattern Generator Color 11 Register

**Table 7-423. TDM\_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	
3	TDM_FS_MODE	R/W	0x0	TDM Frame Sync Mode: Sets active level for the Frame Sync for the TDM audio. The Frame Sync signal provides an active pulse to indicate the first sample data on the TDM data signal. 0: Active high Frame Sync 1: Active low Frame Sync (similar to I2S word select) This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
2	TDM_DELAY	R/W	0x0	TDM Data Delay: Controls data delay for TDM audio samples from the active Frame Sync edge. 0: Data is not delayed from Frame Sync (data is left justified) 1: Data is delayed 1 bit from Frame Sync This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
1:0	TDM_FS_WIDTH	R/W	0x2	TDM Frame Sync Width: Indicates width of TDM Frame Sync pulse for I2S to TDM conversion 00: FS is 50/50 duty cycle 01: FS is one slot/channel wide 1x: FS is 1 clock pulse wide

**7.6.2.5.45 PRBS\_CTRL\_STATUS\_DLANE0 Register (Address = 0x58) [Default = 0x00]**PRBS\_CTRL\_STATUS\_DLANE0 is shown in [Table 7-424](#).Return to the [Summary Table](#).

Pattern Generator Color 12 Register

**Table 7-424. PRBS\_CTRL\_STATUS\_DLANE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PRBS_CHK_EN_D0	R/W	0x0	Set this bit to enable PRBS check on HSRX[3:0] on DPHY Data Lane0

**Table 7-424. PRBS\_CTRL\_STATUS\_DLANE0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	PRBS_FAIL_STKY_FLG_D0	R	0x0	Fail status of the PRBS (sticky); Once failed, set to 1
3	PRBS_FAIL_LIVE_FLG_D0	R	0x0	Fail status of the PRBS (live); latest fail status
2	PRBS_STATUS_D0	R	0x0	When set, bits 4 and 3 of this register are valid
1:0	RESERVED	R	0x0	Reserved

**7.6.2.5.46 PRBS\_ERROR\_COUNT\_DLANGE0 Register (Address = 0x59) [Default = 0x00]**PRBS\_ERROR\_COUNT\_DLANGE0 is shown in [Table 7-425](#).Return to the [Summary Table](#).

Pattern Generator Color 13 Register

**Table 7-425. PRBS\_ERROR\_COUNT\_DLANGE0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PRBS_ERR_CNT_D0	R	0x0	Number of bits errored during PRBS checking of DPHY Data Lane0

**7.6.2.5.47 PRBS\_STATUS\_DLANGE1 Register (Address = 0x5A) [Default = 0x00]**PRBS\_STATUS\_DLANGE1 is shown in [Table 7-426](#).Return to the [Summary Table](#).

Pattern Generator Color 14 Register

**Table 7-426. PRBS\_STATUS\_DLANGE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PRBS_CHK_EN_D1	R/W	0x0	Set this bit to enable PRBS check on HSRX[3:0] on DPHY Data Lane1
4	PRBS_FAIL_STKY_FLG_D1	R	0x0	Fail status of the PRBS (sticky); Once failed, set to 1
3	PRBS_FAIL_LIVE_FLG_D1	R	0x0	Fail status of the PRBS (live); latest fail status
2	PRBS_STATUS_D1	R	0x0	When set, bits 4 and 3 of this register are valid
1:0	RESERVED	R	0x0	Reserved

**7.6.2.5.48 PRBS\_ERROR\_COUNT\_DLANGE1 Register (Address = 0x5B) [Default = 0x00]**PRBS\_ERROR\_COUNT\_DLANGE1 is shown in [Table 7-427](#).Return to the [Summary Table](#).

Pattern Generator Color 15 Register

**Table 7-427. PRBS\_ERROR\_COUNT\_DLANGE1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PRBS_ERR_CNT_D1	R	0x0	Number of bits errored during PRBS checking of DPHY Data Lane1

**7.6.2.5.49 PRBS\_STATUS\_DLANE2 Register (Address = 0x5C) [Default = 0x00]**

PRBS\_STATUS\_DLANE2 is shown in [Table 7-428](#).

Return to the [Summary Table](#).

**Table 7-428. PRBS\_STATUS\_DLANE2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PRBS_CHK_EN_D2	R/W	0x0	Set this bit to enable PRBS check on HSRX[3:0] on DPHY Data Lane2
4	PRBS_FAIL_STKY_FLG_D2	R	0x0	Fail status of the PRBS (sticky); Once failed, set to 1
3	PRBS_FAIL_LIVE_FLG_D2	R	0x0	Fail status of the PRBS (live); latest fail status
2	PRBS_STATUS_D2	R	0x0	When set, bits 4 and 3 of this register are valid
1:0	RESERVED	R	0x0	Reserved

**7.6.2.5.50 PRBS\_ERROR\_COUNT\_DLANE2 Register (Address = 0x5D) [Default = 0x00]**

PRBS\_ERROR\_COUNT\_DLANE2 is shown in [Table 7-429](#).

Return to the [Summary Table](#).

**Table 7-429. PRBS\_ERROR\_COUNT\_DLANE2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PRBS_ERR_CNT_D2	R	0x0	Number of bits errored during PRBS checking of DPHY Data Lane2

**7.6.2.5.51 PRBS\_STATUS\_DLANE3 Register (Address = 0x5E) [Default = 0x00]**

PRBS\_STATUS\_DLANE3 is shown in [Table 7-430](#).

Return to the [Summary Table](#).

**Table 7-430. PRBS\_STATUS\_DLANE3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PRBS_CHK_EN_D3	R/W	0x0	Set this bit to enable PRBS check on HSRX[3:0] on DPHY Data Lane3
4	PRBS_FAIL_STKY_FLG_D3	R	0x0	Fail status of the PRBS (sticky); Once failed, set to 1
3	PRBS_FAIL_LIVE_FLG_D3	R	0x0	Fail status of the PRBS (live); latest fail status
2	PRBS_STATUS_D3	R	0x0	When set, bits 4 and 3 of this register are valid
1:0	RESERVED	R	0x0	Reserved

**7.6.2.5.52 PRBS\_ERROR\_COUNT\_DLANE3 Register (Address = 0x5F) [Default = 0x00]**

PRBS\_ERROR\_COUNT\_DLANE3 is shown in [Table 7-431](#).

Return to the [Summary Table](#).

**Table 7-431. PRBS\_ERROR\_COUNT\_DLANE3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PRBS_ERR_CNT_D3	R	0x0	Number of bits errored during PRBS checking of DPHY Data Lane3

**7.6.2.5.53 CSI\_CFG0\_VC0 Register (Address = 0x80) [Default = 0x00]**CSI\_CFG0\_VC0 is shown in [Table 7-432](#).Return to the [Summary Table](#).**Table 7-432. CSI\_CFG0\_VC0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R/W	0x0	reserved
5:2	OFMT	R/W	0x0	Output data format: 0000b= RGB888 0001b= RGB666 0010b= RGB565 0011b= YUV-420 0101b= YUV-422 (8-bit)
1:0	IFMT	R/W	0x0	Input data format: 00b= RGB 01b= YCbCr16

**7.6.2.5.54 CSI\_LINE\_LEN\_LSB\_VC0 Register (Address = 0x81) [Default = 0x00]**CSI\_LINE\_LEN\_LSB\_VC0 is shown in [Table 7-433](#).Return to the [Summary Table](#).**Table 7-433. CSI\_LINE\_LEN\_LSB\_VC0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_LSB_VC0	R/W	0x0	CSI line length's 8 least significant bits

**7.6.2.5.55 CSI\_LINE\_LEN\_MSB\_VC0 Register (Address = 0x82) [Default = 0x00]**CSI\_LINE\_LEN\_MSB\_VC0 is shown in [Table 7-434](#).Return to the [Summary Table](#).**Table 7-434. CSI\_LINE\_LEN\_MSB\_VC0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_MSB_VC_0	R/W	0x0	CSI line length's 8 most significant bits

**7.6.2.5.56 CSI\_CFG0\_VC1 Register (Address = 0x88) [Default = 0x00]**CSI\_CFG0\_VC1 is shown in [Table 7-435](#).Return to the [Summary Table](#).**Table 7-435. CSI\_CFG0\_VC1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R/W	0x0	reserved
5:2	OFMT	R/W	0x0	Output data format: 0000b= RGB888 0001b= RGB666 0010b= RGB565 0011b= YUV-420 0101b= YUV-422 (8-bit)

**Table 7-435. CSI\_CFG0\_VC1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	IFMT	R/W	0x0	Input data format: 00b= RGB 01b= YCbCr16

**7.6.2.5.57 CSI\_LINE\_LEN\_LSB\_VC1 Register (Address = 0x89) [Default = 0x00]**CSI\_LINE\_LEN\_LSB\_VC1 is shown in [Table 7-436](#).Return to the [Summary Table](#).**Table 7-436. CSI\_LINE\_LEN\_LSB\_VC1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_LSB_VC1	R/W	0x0	CSI line length's 8 least significant bits

**7.6.2.5.58 CSI\_LINE\_LEN\_MSB\_VC1 Register (Address = 0x8A) [Default = 0x00]**CSI\_LINE\_LEN\_MSB\_VC1 is shown in [Table 7-437](#).Return to the [Summary Table](#).**Table 7-437. CSI\_LINE\_LEN\_MSB\_VC1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_MSB_VC1	R/W	0x0	CSI line length's 8 most significant bits

**7.6.2.5.59 CSI\_CFG0\_VC2 Register (Address = 0x90) [Default = 0x00]**CSI\_CFG0\_VC2 is shown in [Table 7-438](#).Return to the [Summary Table](#).**Table 7-438. CSI\_CFG0\_VC2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R/W	0x0	reserved
5:2	OFMT	R/W	0x0	Output data format: 0000b= RGB888 0001b= RGB666 0010b= RGB565 0011b= YUV-420 0101b= YUV-422 (8-bit)
1:0	IFMT	R/W	0x0	Input data format: 00b= RGB 01b= YCbCr16

**7.6.2.5.60 CSI\_LINE\_LEN\_LSB\_VC2 Register (Address = 0x91) [Default = 0x00]**CSI\_LINE\_LEN\_LSB\_VC2 is shown in [Table 7-439](#).Return to the [Summary Table](#).**Table 7-439. CSI\_LINE\_LEN\_LSB\_VC2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_LSB_VC2	R/W	0x0	CSI line length's 8 least significant bits

**7.6.2.5.61 CSI\_LINE\_LEN\_MSB\_VC2 Register (Address = 0x92) [Default = 0x00]**CSI\_LINE\_LEN\_MSB\_VC2 is shown in [Table 7-440](#).Return to the [Summary Table](#).**Table 7-440. CSI\_LINE\_LEN\_MSB\_VC2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_MSB_VC2	R/W	0x0	CSI line length's 8 most significant bits

**7.6.2.5.62 CSI\_CFG0\_VC3 Register (Address = 0x98) [Default = 0x00]**CSI\_CFG0\_VC3 is shown in [Table 7-441](#).Return to the [Summary Table](#).**Table 7-441. CSI\_CFG0\_VC3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R/W	0x0	reserved
5:2	OFMT	R/W	0x0	Output data format: 0000b= RGB888 0001b= RGB666 0010b= RGB565 0011b= YUV-420 0101b= YUV-422 (8-bit)
1:0	IFMT	R/W	0x0	Input data format: 00b= RGB 01b= YCbCr16

**7.6.2.5.63 CSI\_LINE\_LEN\_LSB\_VC3 Register (Address = 0x99) [Default = 0x00]**CSI\_LINE\_LEN\_LSB\_VC3 is shown in [Table 7-442](#).Return to the [Summary Table](#).**Table 7-442. CSI\_LINE\_LEN\_LSB\_VC3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_LSB_VC3	R/W	0x0	CSI line length's 8 least significant bits

**7.6.2.5.64 CSI\_LINE\_LEN\_MSB\_VC3 Register (Address = 0x9A) [Default = 0x00]**CSI\_LINE\_LEN\_MSB\_VC3 is shown in [Table 7-443](#).Return to the [Summary Table](#).**Table 7-443. CSI\_LINE\_LEN\_MSB\_VC3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CSI_LINE_LEN_MSB_VC3	R/W	0x0	CSI line length's 8 most significant bits

**7.6.2.6 Page\_7:\_D-PHY\_Analog\_Port\_1 Registers**

[Table 7-444](#) lists the memory-mapped registers for the Page\_7:\_D-PHY\_Analog\_Port\_1 registers. All register offset addresses not listed in [Table 7-444](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-444. PAGE\_7:\_D-PHY\_ANALOG\_PORT\_1 Registers**

Address	Acronym	Register Name	Section
0x16	DSI_POLARITY_SWAP_PORT_1	DSI_POLARITY_SWAP_PORT_1	<a href="#">Go</a>
0x21	SKEW_CAL_CFG0_P1	SKEW_CAL_CFG0_P1	<a href="#">Go</a>
0x2E	SKEW_CAL_CFG1_P1	SKEW_CAL_CFG1_P1	<a href="#">Go</a>
0x31	SKEW_CAL_CFG2_P1	SKEW_CAL_CFG2_P1	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. [Table 7-445](#) shows the codes that are used for access types in this section.

**Table 7-445. Page\_7:\_D-PHY\_Analog\_Port\_1 Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

#### 7.6.2.6.1 DSI\_POLARITY\_SWAP\_PORT\_1 Register (Address = 0x16) [Default = 0x00]

DSI\_POLARITY\_SWAP\_PORT\_1 is shown in [Table 7-446](#).

Return to the [Summary Table](#).

**Table 7-446. DSI\_POLARITY\_SWAP\_PORT\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	DSI1_CLK_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI1 clock
3	DSI1_DATA3_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI1 lane 3
2	DSI1_DATA2_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI1 lane 2
1	DSI1_DATA1_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI1 lane 1
0	DSI1_DATA0_PN_SWAP	R/W	0x0	Invert P/N polarity for DSI1 lane 0

#### 7.6.2.6.2 SKEW\_CAL\_CFG0\_P1 Register (Address = 0x21) [Default = 0xD0]

SKEW\_CAL\_CFG0\_P1 is shown in [Table 7-447](#).

Return to the [Summary Table](#).

**Table 7-447. SKEW\_CAL\_CFG0\_P1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x1	Reserved
6	RESERVED	R	0x1	Reserved
5	RESERVED	R	0x0	Reserved
4	SKEW_CAL_CFG0_P1	R/W	0x1	This register controls DSI skew calibration and its initial value is controlled by MODE_SEL1. 1: DSI skew calibration disabled (DSI_CAL_EN= 0) 0: DSI skew calibration enabled (DSI_CAL_EN= 1)
3:0	RESERVED	R	0x0	Reserved

**7.6.2.6.3 SKEW\_CAL\_CFG1\_P1 Register (Address = 0x2E) [Default = 0x00]**SKEW\_CAL\_CFG1\_P1 is shown in [Table 7-448](#).Return to the [Summary Table](#).**Table 7-448. SKEW\_CAL\_CFG1\_P1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	SKEW_CAL_CFG1_P1	R/W	0x0	This register controls DSI skew calibration and its initial value is controlled by MODE_SEL1. 0: DSI skew calibration disabled (DSI_CAL_EN= 0) 1: DSI skew calibration enabled (DSI_CAL_EN= 1)
5:0	RESERVED	R	0x0	Reserved

**7.6.2.6.4 SKEW\_CAL\_CFG2\_P1 Register (Address = 0x31) [Default = 0x02]**SKEW\_CAL\_CFG2\_P1 is shown in [Table 7-449](#).Return to the [Summary Table](#).**Table 7-449. SKEW\_CAL\_CFG2\_P1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	SKEW_CAL_CFG2_P1	R/W	0x1	This register controls DSI skew calibration and its initial value is controlled by MODE_SEL1. 1: DSI skew calibration disabled (DSI_CAL_EN= 0) 0: DSI skew calibration enabled (DSI_CAL_EN= 1)
0	RESERVED	R/W	0x0	Reserved

### 7.6.2.7 Page\_8\_ADAS\_Compatability Registers

Table 7-450 lists the memory-mapped registers for the Page\_8\_ADAS\_Compatability registers. All register offset addresses not listed in Table 7-450 should be considered as reserved locations and the register contents should not be modified.

**Table 7-450. PAGE\_8\_ADAS\_COMPATABILITY Registers**

Address	Acronym	Register Name	Section
0x81	PGEN_CTL_PORT0	PGEN_CTL_PORT0	Go
0x82	PGEN_CFG_PORT0	PGEN_CFG_PORT0	Go
0x83	PGEN_CSI_DI_PORT0	PGEN_CSI_DI_PORT0	Go
0x84	PGEN_LINE_SIZE1_PORT0	PGEN_LINE_SIZE1_PORT0	Go
0x85	PGEN_LINE_SIZE0_PORT0	PGEN_LINE_SIZE0_PORT0	Go
0x86	PGEN_BAR_SIZE1_PORT0	PGEN_BAR_SIZE1_PORT0	Go
0x87	PGEN_BAR_SIZE0_PORT0	PGEN_BAR_SIZE0_PORT0	Go
0x88	PGEN_ACT_LPF1_PORT0	PGEN_ACT_LPF1_PORT0	Go
0x89	PGEN_ACT_LPF0_PORT0	PGEN_ACT_LPF0_PORT0	Go
0x8A	PGEN_TOT_LPF1_PORT0	PGEN_TOT_LPF1_PORT0	Go
0x8B	PGEN_TOT_LPF0_PORT0	PGEN_TOT_LPF0_PORT0	Go
0x8C	PGEN_LINE_PD1_PORT0	PGEN_LINE_PD1_PORT0	Go
0x8D	PGEN_LINE_PD0_PORT0	PGEN_LINE_PD0_PORT0	Go
0x8E	PGEN_VBP_PORT0	PGEN_VBP_PORT0	Go
0x8F	PGEN_VFP_PORT0	PGEN_VFP_PORT0	Go
0x90	PGEN_COLOR0_PORT0	PGEN_COLOR0_PORT0	Go
0x91	PGEN_COLOR1_PORT0	PGEN_COLOR1_PORT0	Go
0x92	PGEN_COLOR2_PORT0	PGEN_COLOR2_PORT0	Go
0x93	PGEN_COLOR3_PORT0	PGEN_COLOR3_PORT0	Go
0x94	PGEN_COLOR4_PORT0	PGEN_COLOR4_PORT0	Go
0x95	PGEN_COLOR5_PORT0	PGEN_COLOR5_PORT0	Go
0x96	PGEN_COLOR6_PORT0	PGEN_COLOR6_PORT0	Go
0x97	PGEN_COLOR7_PORT0	PGEN_COLOR7_PORT0	Go
0x98	PGEN_COLOR8_PORT0	PGEN_COLOR8_PORT0	Go
0x99	PGEN_COLOR9_PORT0	PGEN_COLOR9_PORT0	Go
0x9A	PGEN_COLOR10_PORT0	PGEN_COLOR10_PORT0	Go
0x9B	PGEN_COLOR11_PORT0	PGEN_COLOR11_PORT0	Go
0x9C	PGEN_COLOR12_PORT0	PGEN_COLOR12_PORT0	Go
0x9D	PGEN_COLOR13_PORT0	PGEN_COLOR13_PORT0	Go
0x9E	PGEN_COLOR14_PORT0	PGEN_COLOR14_PORT0	Go
0x9F	PGEN_COLOR15_PORT0	PGEN_COLOR15_PORT0	Go
0xA0	CRC_CHK_CTL_PORT0	CRC_CHK_CTL_PORT0	Go
0xA1	CRC_CHK_STS_PORT0		Go
0xA2	LONG_PKT_CNT_B0_PORT0		Go
0xA3	LONG_PKT_CNT_B1_PORT0		Go
0xA4	SHORT_PKT_CNT_B0_PORT0		Go
0xA5	SHORT_PKT_CNT_B1_PORT0		Go
0xA6	CRC_ERR_CNT_B0_PORT0		Go
0xA7	CRC_ERR_CNT_B1_PORT0		Go
0xA8	ECC_ERR_CNT_B0_PORT0		Go
0xA9	ECC_ERR_CNT_B1_PORT0		Go

**Table 7-450. PAGE\_8\_ADAS\_COMPATABILITY Registers (continued)**

Address	Acronym	Register Name	Section
0xAA	ECC_COR_CNT_B0_PORT0		Go
0xAB	ECC_COR_CNT_B1_PORT0		Go
0xAC	LEN_ERR_CNT_B0_PORT0		Go
0xAD	LEN_ERR_CNT_B1_PORT0		Go
0xC1	PGEN_CTL_PORT1	PGEN_CTL_PORT1	Go
0xC2	PGEN_CFG_PORT1	PGEN_CFG_PORT1	Go
0xC3	PGEN_CSI_DI_PORT1	PGEN_CSI_DI_PORT1	Go
0xC4	PGEN_LINE_SIZE1_PORT1	PGEN_LINE_SIZE1_PORT1	Go
0xC5	PGEN_LINE_SIZE0_PORT1	PGEN_LINE_SIZE0_PORT1	Go
0xC6	PGEN_BAR_SIZE1_PORT1	PGEN_BAR_SIZE1_PORT1	Go
0xC7	PGEN_BAR_SIZE0_PORT1	PGEN_BAR_SIZE0_PORT1	Go
0xC8	PGEN_ACT_LPF1_PORT1	PGEN_ACT_LPF1_PORT1	Go
0xC9	PGEN_ACT_LPF0_PORT1	PGEN_ACT_LPF0_PORT1	Go
0xCA	PGEN_TOT_LPF1_PORT1	PGEN_TOT_LPF1_PORT1	Go
0xCB	PGEN_TOT_LPF0_PORT1	PGEN_TOT_LPF0_PORT1	Go
0xCC	PGEN_LINE_PD1_PORT1	PGEN_LINE_PD1_PORT1	Go
0xCD	PGEN_LINE_PD0_PORT1	PGEN_LINE_PD0_PORT1	Go
0xCE	PGEN_VBP_PORT1	PGEN_VBP_PORT1	Go
0xCF	PGEN_VFP_PORT1	PGEN_VFP_PORT1	Go
0xD0	PGEN_COLOR0_PORT1	PGEN_COLOR0_PORT1	Go
0xD1	PGEN_COLOR1_PORT1	PGEN_COLOR1_PORT1	Go
0xD2	PGEN_COLOR2_PORT1	PGEN_COLOR2_PORT1	Go
0xD3	PGEN_COLOR3_PORT1	PGEN_COLOR3_PORT1	Go
0xD4	PGEN_COLOR4_PORT1	PGEN_COLOR4_PORT1	Go
0xD5	PGEN_COLOR5_PORT1	PGEN_COLOR5_PORT1	Go
0xD6	PGEN_COLOR6_PORT1	PGEN_COLOR6_PORT1	Go
0xD7	PGEN_COLOR7_PORT1	PGEN_COLOR7_PORT1	Go
0xD8	PGEN_COLOR8_PORT1	PGEN_COLOR8_PORT1	Go
0xD9	PGEN_COLOR9_PORT1	PGEN_COLOR9_PORT1	Go
0xDA	PGEN_COLOR10_PORT1	PGEN_COLOR10_PORT1	Go
0xDB	PGEN_COLOR11_PORT1	PGEN_COLOR11_PORT1	Go
0xDC	PGEN_COLOR12_PORT1	PGEN_COLOR12_PORT1	Go
0xDD	PGEN_COLOR13_PORT1	PGEN_COLOR13_PORT1	Go
0xDE	PGEN_COLOR14_PORT1	PGEN_COLOR14_PORT1	Go
0xDF	PGEN_COLOR15_PORT1	PGEN_COLOR15_PORT1	Go
0xE0	CRC_CHK_CTL_PORT1	CRC_CHK_CTL_PORT1	Go
0xE1	CRC_CHK_STS_PORT1		Go
0xE2	LONG_PKT_CNT_B0_PORT1	LONG_PKT_CNT_B0_PORT1	Go
0xE3	LONG_PKT_CNT_B1_PORT1	LONG_PKT_CNT_B1_PORT1	Go
0xE4	SHORT_PKT_CNT_B0_PORT1	SHORT_PKT_CNT_B0_PORT1	Go
0xE5	SHORT_PKT_CNT_B1_PORT1	SHORT_PKT_CNT_B1_PORT1	Go
0xE6	CRC_ERR_CNT_B0_PORT1	CRC_ERR_CNT_B0_PORT1	Go
0xE7	CRC_ERR_CNT_B1_PORT1	CRC_ERR_CNT_B1_PORT1	Go
0xE8	ECC_ERR_CNT_B0_PORT1	ECC_ERR_CNT_B0_PORT1	Go
0xE9	ECC_ERR_CNT_B1_PORT1	ECC_ERR_CNT_B1_PORT1	Go

**Table 7-450. PAGE\_8\_ADAS\_COMPATABILITY Registers (continued)**

Address	Acronym	Register Name	Section
0xEA	ECC_COR_CNT_B0_PORT1	ECC_COR_CNT_B0_PORT1	Go
0xEB	ECC_COR_CNT_B1_PORT1	ECC_COR_CNT_B1_PORT1	Go
0xEC	LEN_ERR_CNT_B0_PORT1	LEN_ERR_CNT_B0_PORT1	Go
0xED	LEN_ERR_CNT_B1_PORT1	LEN_ERR_CNT_B1_PORT1	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-451](#) shows the codes that are used for access types in this section.

**Table 7-451. Page\_8\_ADAS\_Compatability Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

#### 7.6.2.7.1 PGEN\_CTL\_PORT0 Register (Address = 0x81) [Default = 0x00]

PGEN\_CTL\_PORT0 is shown in [Table 7-452](#).

Return to the [Summary Table](#).

**Table 7-452. PGEN\_CTL\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	SPARE	R/W	0x0	Reserved
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

#### 7.6.2.7.2 PGEN\_CFG\_PORT0 Register (Address = 0x82) [Default = 0x33]

PGEN\_CFG\_PORT0 is shown in [Table 7-453](#).

Return to the [Summary Table](#).

**Table 7-453. PGEN\_CFG\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	SPARE	R/W	0x0	Reserved
5:4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars

**Table 7-453. PGEN\_CFG\_PORT0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 12.

**7.6.2.7.3 PGEN\_CSI\_DI\_PORT0 Register (Address = 0x83) [Default = 0x24]**PGEN\_CSI\_DI\_PORT0 is shown in [Table 7-454](#).Return to the [Summary Table](#).**Table 7-454. PGEN\_CSI\_DI\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5:0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

**7.6.2.7.4 PGEN\_LINE\_SIZE1\_PORT0 Register (Address = 0x84) [Default = 0x07]**PGEN\_LINE\_SIZE1\_PORT0 is shown in [Table 7-455](#).Return to the [Summary Table](#).**Table 7-455. PGEN\_LINE\_SIZE1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

**7.6.2.7.5 PGEN\_LINE\_SIZE0\_PORT0 Register (Address = 0x85) [Default = 0x80]**PGEN\_LINE\_SIZE0\_PORT0 is shown in [Table 7-456](#).Return to the [Summary Table](#).**Table 7-456. PGEN\_LINE\_SIZE0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

**7.6.2.7.6 PGEN\_BAR\_SIZE1\_PORT0 Register (Address = 0x86) [Default = 0x00]**PGEN\_BAR\_SIZE1\_PORT0 is shown in [Table 7-457](#).Return to the [Summary Table](#).**Table 7-457. PGEN\_BAR\_SIZE1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

**7.6.2.7.7 PGEN\_BAR\_SIZE0\_PORT0 Register (Address = 0x87) [Default = 0xF0]**

PGEN\_BAR\_SIZE0\_PORT0 is shown in [Table 7-458](#).

Return to the [Summary Table](#).

**Table 7-458. PGEN\_BAR\_SIZE0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

**7.6.2.7.8 PGEN\_ACT\_LPF1\_PORT0 Register (Address = 0x88) [Default = 0x01]**

PGEN\_ACT\_LPF1\_PORT0 is shown in [Table 7-459](#).

Return to the [Summary Table](#).

**Table 7-459. PGEN\_ACT\_LPF1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

**7.6.2.7.9 PGEN\_ACT\_LPF0\_PORT0 Register (Address = 0x89) [Default = 0xE0]**

PGEN\_ACT\_LPF0\_PORT0 is shown in [Table 7-460](#).

Return to the [Summary Table](#).

**Table 7-460. PGEN\_ACT\_LPF0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

**7.6.2.7.10 PGEN\_TOT\_LPF1\_PORT0 Register (Address = 0x8A) [Default = 0x02]**

PGEN\_TOT\_LPF1\_PORT0 is shown in [Table 7-461](#).

Return to the [Summary Table](#).

**Table 7-461. PGEN\_TOT\_LPF1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

**7.6.2.7.11 PGEN\_TOT\_LPF0\_PORT0 Register (Address = 0x8B) [Default = 0x0D]**

PGEN\_TOT\_LPF0\_PORT0 is shown in [Table 7-462](#).

Return to the [Summary Table](#).

**Table 7-462. PGEN\_TOT\_LPF0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

**7.6.2.7.12 PGEN\_LINE\_PD1\_PORT0 Register (Address = 0x8C) [Default = 0x0C]**PGEN\_LINE\_PD1\_PORT0 is shown in [Table 7-463](#).Return to the [Summary Table](#).**Table 7-463. PGEN\_LINE\_PD1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[15:8]	R/W	0xC	Line Period Most significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds. (981: This register needs to be scaled up by the ratio of clk_div40 MHz/100 MHz)

**7.6.2.7.13 PGEN\_LINE\_PD0\_PORT0 Register (Address = 0x8D) [Default = 0x67]**PGEN\_LINE\_PD0\_PORT0 is shown in [Table 7-464](#).Return to the [Summary Table](#).**Table 7-464. PGEN\_LINE\_PD0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds. (981: This register needs to be scaled up by the ratio of clk_div40 MHz/100 MHz)

**7.6.2.7.14 PGEN\_VBP\_PORT0 Register (Address = 0x8E) [Default = 0x21]**PGEN\_VBP\_PORT0 is shown in [Table 7-465](#).Return to the [Summary Table](#).**Table 7-465. PGEN\_VBP\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

**7.6.2.7.15 PGEN\_VFP\_PORT0 Register (Address = 0x8F) [Default = 0x0A]**PGEN\_VFP\_PORT0 is shown in [Table 7-466](#).Return to the [Summary Table](#).

**Table 7-466. PGEN\_VFP\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_VFP	R/W	0xA	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

**7.6.2.7.16 PGEN\_COLOR0\_PORT0 Register (Address = 0x90) [Default = 0xAA]**PGEN\_COLOR0\_PORT0 is shown in [Table 7-467](#).Return to the [Summary Table](#).**Table 7-467. PGEN\_COLOR0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

**7.6.2.7.17 PGEN\_COLOR1\_PORT0 Register (Address = 0x91) [Default = 0x33]**PGEN\_COLOR1\_PORT0 is shown in [Table 7-468](#).Return to the [Summary Table](#).**Table 7-468. PGEN\_COLOR1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

**7.6.2.7.18 PGEN\_COLOR2\_PORT0 Register (Address = 0x92) [Default = 0xF0]**PGEN\_COLOR2\_PORT0 is shown in [Table 7-469](#).Return to the [Summary Table](#).**Table 7-469. PGEN\_COLOR2\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

**7.6.2.7.19 PGEN\_COLOR3\_PORT0 Register (Address = 0x93) [Default = 0x7F]**PGEN\_COLOR3\_PORT0 is shown in [Table 7-470](#).Return to the [Summary Table](#).

**Table 7-470. PGEN\_COLOR3\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

**7.6.2.7.20 PGEN\_COLOR4\_PORT0 Register (Address = 0x94) [Default = 0x55]**PGEN\_COLOR4\_PORT0 is shown in [Table 7-471](#).Return to the [Summary Table](#).**Table 7-471. PGEN\_COLOR4\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

**7.6.2.7.21 PGEN\_COLOR5\_PORT0 Register (Address = 0x95) [Default = 0xCC]**PGEN\_COLOR5\_PORT0 is shown in [Table 7-472](#).Return to the [Summary Table](#).**Table 7-472. PGEN\_COLOR5\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

**7.6.2.7.22 PGEN\_COLOR6\_PORT0 Register (Address = 0x96) [Default = 0x0F]**PGEN\_COLOR6\_PORT0 is shown in [Table 7-473](#).Return to the [Summary Table](#).**Table 7-473. PGEN\_COLOR6\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

**7.6.2.7.23 PGEN\_COLOR7\_PORT0 Register (Address = 0x97) [Default = 0x80]**PGEN\_COLOR7\_PORT0 is shown in [Table 7-474](#).Return to the [Summary Table](#).

**Table 7-474. PGEN\_COLOR7\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

**7.6.2.7.24 PGEN\_COLOR8\_PORT0 Register (Address = 0x98) [Default = 0x00]**PGEN\_COLOR8\_PORT0 is shown in [Table 7-475](#).Return to the [Summary Table](#).

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**Table 7-475. PGEN\_COLOR8\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

**7.6.2.7.25 PGEN\_COLOR9\_PORT0 Register (Address = 0x99) [Default = 0x00]**PGEN\_COLOR9\_PORT0 is shown in [Table 7-476](#).Return to the [Summary Table](#).**Table 7-476. PGEN\_COLOR9\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

**7.6.2.7.26 PGEN\_COLOR10\_PORT0 Register (Address = 0x9A) [Default = 0x00]**PGEN\_COLOR10\_PORT0 is shown in [Table 7-477](#).Return to the [Summary Table](#).**Table 7-477. PGEN\_COLOR10\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

**7.6.2.7.27 PGEN\_COLOR11\_PORT0 Register (Address = 0x9B) [Default = 0x00]**PGEN\_COLOR11\_PORT0 is shown in [Table 7-478](#).Return to the [Summary Table](#).**Table 7-478. PGEN\_COLOR11\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

**7.6.2.7.28 PGEN\_COLOR12\_PORT0 Register (Address = 0x9C) [Default = 0x00]**PGEN\_COLOR12\_PORT0 is shown in [Table 7-479](#).Return to the [Summary Table](#).**Table 7-479. PGEN\_COLOR12\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

**7.6.2.7.29 PGEN\_COLOR13\_PORT0 Register (Address = 0x9D) [Default = 0x00]**PGEN\_COLOR13\_PORT0 is shown in [Table 7-480](#).Return to the [Summary Table](#).**Table 7-480. PGEN\_COLOR13\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

**7.6.2.7.30 PGEN\_COLOR14\_PORT0 Register (Address = 0x9E) [Default = 0x00]**PGEN\_COLOR14\_PORT0 is shown in [Table 7-481](#).Return to the [Summary Table](#).**Table 7-481. PGEN\_COLOR14\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

**7.6.2.7.31 PGEN\_COLOR15\_PORT0 Register (Address = 0x9F) [Default = 0x00]**PGEN\_COLOR15\_PORT0 is shown in [Table 7-482](#).Return to the [Summary Table](#).

Video Processor Status Register

**Table 7-482. PGEN\_COLOR15\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR15	R/W	0x0	Pattern Generator Color 15 For Fixed Color Patterns, this register controls the sixteenth byte of the fixed color pattern.

**7.6.2.7.32 CRC\_CHK\_CTL\_PORT0 Register (Address = 0xA0) [Default = 0x00]**CRC\_CHK\_CTL\_PORT0 is shown in [Table 7-483](#).Return to the [Summary Table](#).

Video Interrupt Status Register

The bits in this register will be set on occurrence of the associated event. If the corresponding interrupt mask register is set, an Interrupt will be generated for the event. The interrupt status bits will be cleared on a read of this register.

**Table 7-483. CRC\_CHK\_CTL\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	CLR_CRC_CNT	R/W	0x0	1: Clears CRC checker counters
0	CRC_ENABLE	R/W	0x0	1: Enables CRC checker

**7.6.2.7.33 CRC\_CHK\_STS\_PORT0 Register (Address = 0xA1) [Default = 0x00]**

CRC\_CHK\_STS\_PORT0 is shown in [Table 7-484](#).

Return to the [Summary Table](#).

**Table 7-484. CRC\_CHK\_STS\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	SHORT_PKT_DET	R	0x0	Short Packet (FS) Detected; Cleared by CLR_CRC_CNT
4	LONG_PKT_DET	R	0x0	Long Packet Detected; Cleared by CLR_CRC_CNT
3	ECC_ERR	R	0x0	ECC Error detected; Cleared by CLR_CRC_CNT
2	ECC_COR	R	0x0	ECC Correction detected; Cleared by CLR_CRC_CNT
1	LENGTH_ERR	R	0x0	Line Length Error detected; Cleared by CLR_CRC_CNT
0	CRC_ERR	R	0x0	CRC Error detected; Cleared by CLR_CRC_CNT

**7.6.2.7.34 LONG\_PKT\_CNT\_B0\_PORT0 Register (Address = 0xA2) [Default = 0x00]**

LONG\_PKT\_CNT\_B0\_PORT0 is shown in [Table 7-485](#).

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**Table 7-485. LONG\_PKT\_CNT\_B0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LONG_PKT_CNT_B0	R	0x0	Long Packet Count [7:0]; Cleared by CLR_CRC_CNT

**7.6.2.7.35 LONG\_PKT\_CNT\_B1\_PORT0 Register (Address = 0xA3) [Default = 0x00]**

LONG\_PKT\_CNT\_B1\_PORT0 is shown in [Table 7-486](#).

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**Table 7-486. LONG\_PKT\_CNT\_B1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LONG_PKT_CNT_B1	R	0x0	Long Packet Count [15:8]; Cleared by CLR_CRC_CNT

**7.6.2.7.36 SHORT\_PKT\_CNT\_B0\_PORT0 Register (Address = 0xA4) [Default = 0x00]**

SHORT\_PKT\_CNT\_B0\_PORT0 is shown in [Table 7-487](#).

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**Table 7-487. SHORT\_PKT\_CNT\_B0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	SHORT_PKT_CNT_B0	R	0x0	Short Packet (FS) Count [7:0]; Cleared by CLR_CRC_CNT

**7.6.2.7.37 SHORT\_PKT\_CNT\_B1\_PORT0 Register (Address = 0xA5) [Default = 0x00]**SHORT\_PKT\_CNT\_B1\_PORT0 is shown in [Table 7-488](#).Return to the [Summary Table](#).**Table 7-488. SHORT\_PKT\_CNT\_B1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	SHORT_PKT_CNT_B1	R	0x0	Short Packet (FS) Count [15:8]; Cleared by CLR_CRC_CNT

**7.6.2.7.38 CRC\_ERR\_CNT\_B0\_PORT0 Register (Address = 0xA6) [Default = 0x00]**CRC\_ERR\_CNT\_B0\_PORT0 is shown in [Table 7-489](#).Return to the [Summary Table](#).**Table 7-489. CRC\_ERR\_CNT\_B0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CRC_ERR_CNT_B0	R	0x0	CRC Error Count [7:0] Cleared by CLR_CRC_CNT

**7.6.2.7.39 CRC\_ERR\_CNT\_B1\_PORT0 Register (Address = 0xA7) [Default = 0x00]**CRC\_ERR\_CNT\_B1\_PORT0 is shown in [Table 7-490](#).Return to the [Summary Table](#).**Table 7-490. CRC\_ERR\_CNT\_B1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CRC_ERR_CNT_B1	R	0x0	CRC Error Count [15:8] Cleared by CLR_CRC_CNT

**7.6.2.7.40 ECC\_ERR\_CNT\_B0\_PORT0 Register (Address = 0xA8) [Default = 0x00]**ECC\_ERR\_CNT\_B0\_PORT0 is shown in [Table 7-491](#).Return to the [Summary Table](#).**Table 7-491. ECC\_ERR\_CNT\_B0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ECC_ERR_CNT_B0	R	0x0	ECC Error Count [7:0] Cleared by CLR_CRC_CNT

**7.6.2.7.41 ECC\_ERR\_CNT\_B1\_PORT0 Register (Address = 0xA9) [Default = 0x00]**ECC\_ERR\_CNT\_B1\_PORT0 is shown in [Table 7-492](#).Return to the [Summary Table](#).**Table 7-492. ECC\_ERR\_CNT\_B1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ECC_ERR_CNT_B1	R	0x0	ECC Error Count [15:8] Cleared by CLR_CRC_CNT

**7.6.2.7.42 ECC\_COR\_CNT\_B0\_PORT0 Register (Address = 0xAA) [Default = 0x00]**

ECC\_COR\_CNT\_B0\_PORT0 is shown in [Table 7-493](#).

Return to the [Summary Table](#).

**Table 7-493. ECC\_COR\_CNT\_B0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ECC_COR_CNT_B0	R	0x0	ECC Correction Count [7:0] Cleared by CLR_CRC_CNT

**7.6.2.7.43 ECC\_COR\_CNT\_B1\_PORT0 Register (Address = 0xAB) [Default = 0x00]**

ECC\_COR\_CNT\_B1\_PORT0 is shown in [Table 7-494](#).

Return to the [Summary Table](#).

**Table 7-494. ECC\_COR\_CNT\_B1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ECC_COR_CNT_B1	R	0x0	ECC Correction Count [15:8] Cleared by CLR_CRC_CNT

**7.6.2.7.44 LEN\_ERR\_CNT\_B0\_PORT0 Register (Address = 0xAC) [Default = 0x00]**

LEN\_ERR\_CNT\_B0\_PORT0 is shown in [Table 7-495](#).

Return to the [Summary Table](#).

**Table 7-495. LEN\_ERR\_CNT\_B0\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LEN_ERR_CNT_B0	R	0x0	Line Length Error Count [7:0] Cleared by CLR_CRC_CNT

**7.6.2.7.45 LEN\_ERR\_CNT\_B1\_PORT0 Register (Address = 0xAD) [Default = 0x00]**

LEN\_ERR\_CNT\_B1\_PORT0 is shown in [Table 7-496](#).

Return to the [Summary Table](#).

**Table 7-496. LEN\_ERR\_CNT\_B1\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LEN_ERR_CNT_B1	R	0x0	Line Length Error Count [15:8] Cleared by CLR_CRC_CNT

**7.6.2.7.46 PGEN\_CTL\_PORT1 Register (Address = 0xC1) [Default = 0x00]**

PGEN\_CTL\_PORT1 is shown in [Table 7-497](#).

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Video Interrupt Control Register

The bits in this register enable interrupts for the associated bits in the Interrupt Status register.

**Table 7-497. PGEN\_CTL\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	SPARE	R/W	0x0	Reserved
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

**7.6.2.7.47 PGEN\_CFG\_PORT1 Register (Address = 0xC2) [Default = 0x33]**

PGEN\_CFG\_PORT1 is shown in [Table 7-498](#).

Return to the [Summary Table](#).

Video Processor total horizontal period measure

**Table 7-498. PGEN\_CFG\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	SPARE	R/W	0x0	Reserved
5:4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars
3:0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 12.

**7.6.2.7.48 PGEN\_CSI\_DI\_PORT1 Register (Address = 0xC3) [Default = 0x24]**

PGEN\_CSI\_DI\_PORT1 is shown in [Table 7-499](#).

Return to the [Summary Table](#).

Video Processor total horizontal period measure

**Table 7-499. PGEN\_CSI\_DI\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5:0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

**7.6.2.7.49 PGEN\_LINE\_SIZE1\_PORT1 Register (Address = 0xC4) [Default = 0x07]**

PGEN\_LINE\_SIZE1\_PORT1 is shown in [Table 7-500](#).

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Video Processor Control Register

**Table 7-500. PGEN\_LINE\_SIZE1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

**7.6.2.7.50 PGEN\_LINE\_SIZE0\_PORT1 Register (Address = 0xC5) [Default = 0x80]**

PGEN\_LINE\_SIZE0\_PORT1 is shown in [Table 7-501](#).

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## Video Processor Configuration Register

**Table 7-501. PGEN\_LINE\_SIZE0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

**7.6.2.7.51 PGEN\_BAR\_SIZE1\_PORT1 Register (Address = 0xC6) [Default = 0x00]**PGEN\_BAR\_SIZE1\_PORT1 is shown in [Table 7-502](#).Return to the [Summary Table](#).**Table 7-502. PGEN\_BAR\_SIZE1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

**7.6.2.7.52 PGEN\_BAR\_SIZE0\_PORT1 Register (Address = 0xC7) [Default = 0xF0]**PGEN\_BAR\_SIZE0\_PORT1 is shown in [Table 7-503](#).Return to the [Summary Table](#).**Table 7-503. PGEN\_BAR\_SIZE0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

**7.6.2.7.53 PGEN\_ACT\_LPF1\_PORT1 Register (Address = 0xC8) [Default = 0x01]**PGEN\_ACT\_LPF1\_PORT1 is shown in [Table 7-504](#).Return to the [Summary Table](#).**Table 7-504. PGEN\_ACT\_LPF1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

**7.6.2.7.54 PGEN\_ACT\_LPF0\_PORT1 Register (Address = 0xC9) [Default = 0xE0]**PGEN\_ACT\_LPF0\_PORT1 is shown in [Table 7-505](#).Return to the [Summary Table](#).**Table 7-505. PGEN\_ACT\_LPF0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

**7.6.2.7.55 PGEN\_TOT\_LPF1\_PORT1 Register (Address = 0xCA) [Default = 0x02]**PGEN\_TOT\_LPF1\_PORT1 is shown in [Table 7-506](#).Return to the [Summary Table](#).

Vertical Filter A Register

**Table 7-506. PGEN\_TOT\_LPF1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

**7.6.2.7.56 PGEN\_TOT\_LPF0\_PORT1 Register (Address = 0xCB) [Default = 0x0D]**PGEN\_TOT\_LPF0\_PORT1 is shown in [Table 7-507](#).Return to the [Summary Table](#).

Vertical Filter B Register

**Table 7-507. PGEN\_TOT\_LPF0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

**7.6.2.7.57 PGEN\_LINE\_PD1\_PORT1 Register (Address = 0xCC) [Default = 0x0C]**PGEN\_LINE\_PD1\_PORT1 is shown in [Table 7-508](#).Return to the [Summary Table](#).

Crop Start X1 Register

**Table 7-508. PGEN\_LINE\_PD1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[15:8]	R/W	0xC	Line Period Most significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds. (981: This register needs to be scaled up by the ratio of clk_div40 MHz/100 MHz)

**7.6.2.7.58 PGEN\_LINE\_PD0\_PORT1 Register (Address = 0xCD) [Default = 0x67]**PGEN\_LINE\_PD0\_PORT1 is shown in [Table 7-509](#).Return to the [Summary Table](#).

Crop Start X1 Register

**Table 7-509. PGEN\_LINE\_PD0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds. (981: This register needs to be scaled up by the ratio of clk_div40 MHz/100 MHz)

**7.6.2.7.59 PGEN\_VBP\_PORT1 Register (Address = 0xCE) [Default = 0x21]**PGEN\_VBP\_PORT1 is shown in [Table 7-510](#).Return to the [Summary Table](#).

Crop Start Y0 Register

**Table 7-510. PGEN\_VBP\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

**7.6.2.7.60 PGEN\_VFP\_PORT1 Register (Address = 0xCF) [Default = 0x0A]**PGEN\_VFP\_PORT1 is shown in [Table 7-511](#).Return to the [Summary Table](#).

Crop Start Y1 Register

**Table 7-511. PGEN\_VFP\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_VFP	R/W	0xA	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

**7.6.2.7.61 PGEN\_COLOR0\_PORT1 Register (Address = 0xD0) [Default = 0xAA]**PGEN\_COLOR0\_PORT1 is shown in [Table 7-512](#).Return to the [Summary Table](#).

Crop Stop X0 Register

**Table 7-512. PGEN\_COLOR0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

**7.6.2.7.62 PGEN\_COLOR1\_PORT1 Register (Address = 0xD1) [Default = 0x33]**PGEN\_COLOR1\_PORT1 is shown in [Table 7-513](#).

[Return to the Summary Table.](#)

Crop Stop X1 Register

**Table 7-513. PGEN\_COLOR1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

**7.6.2.7.63 PGEN\_COLOR2\_PORT1 Register (Address = 0xD2) [Default = 0xF0]**

PGEN\_COLOR2\_PORT1 is shown in [Table 7-514](#).

[Return to the Summary Table.](#)

Crop Stop Y0 Register

**Table 7-514. PGEN\_COLOR2\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

**7.6.2.7.64 PGEN\_COLOR3\_PORT1 Register (Address = 0xD3) [Default = 0x7F]**

PGEN\_COLOR3\_PORT1 is shown in [Table 7-515](#).

[Return to the Summary Table.](#)

Crop Stop Y1 Register

**Table 7-515. PGEN\_COLOR3\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

**7.6.2.7.65 PGEN\_COLOR4\_PORT1 Register (Address = 0xD4) [Default = 0x55]**

PGEN\_COLOR4\_PORT1 is shown in [Table 7-516](#).

[Return to the Summary Table.](#)

**Table 7-516. PGEN\_COLOR4\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

**7.6.2.7.66 PGEN\_COLOR5\_PORT1 Register (Address = 0xD5) [Default = 0xCC]**PGEN\_COLOR5\_PORT1 is shown in [Table 7-517](#).Return to the [Summary Table](#).**Table 7-517. PGEN\_COLOR5\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

**7.6.2.7.67 PGEN\_COLOR6\_PORT1 Register (Address = 0xD6) [Default = 0x0F]**PGEN\_COLOR6\_PORT1 is shown in [Table 7-518](#).Return to the [Summary Table](#).**Table 7-518. PGEN\_COLOR6\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

**7.6.2.7.68 PGEN\_COLOR7\_PORT1 Register (Address = 0xD7) [Default = 0x80]**PGEN\_COLOR7\_PORT1 is shown in [Table 7-519](#).Return to the [Summary Table](#).**Table 7-519. PGEN\_COLOR7\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

**7.6.2.7.69 PGEN\_COLOR8\_PORT1 Register (Address = 0xD8) [Default = 0x00]**PGEN\_COLOR8\_PORT1 is shown in [Table 7-520](#).Return to the [Summary Table](#).**Table 7-520. PGEN\_COLOR8\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

**7.6.2.7.70 PGEN\_COLOR9\_PORT1 Register (Address = 0xD9) [Default = 0x00]**PGEN\_COLOR9\_PORT1 is shown in [Table 7-521](#).Return to the [Summary Table](#).

**Table 7-521. PGEN\_COLOR9\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

**7.6.2.7.71 PGEN\_COLOR10\_PORT1 Register (Address = 0xDA) [Default = 0x00]**PGEN\_COLOR10\_PORT1 is shown in [Table 7-522](#).Return to the [Summary Table](#).**Table 7-522. PGEN\_COLOR10\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

**7.6.2.7.72 PGEN\_COLOR11\_PORT1 Register (Address = 0xDB) [Default = 0x00]**PGEN\_COLOR11\_PORT1 is shown in [Table 7-523](#).Return to the [Summary Table](#).**Table 7-523. PGEN\_COLOR11\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

**7.6.2.7.73 PGEN\_COLOR12\_PORT1 Register (Address = 0xDC) [Default = 0x00]**PGEN\_COLOR12\_PORT1 is shown in [Table 7-524](#).Return to the [Summary Table](#).**Table 7-524. PGEN\_COLOR12\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

**7.6.2.7.74 PGEN\_COLOR13\_PORT1 Register (Address = 0xDD) [Default = 0x00]**PGEN\_COLOR13\_PORT1 is shown in [Table 7-525](#).Return to the [Summary Table](#).**Table 7-525. PGEN\_COLOR13\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

**7.6.2.7.75 PGEN\_COLOR14\_PORT1 Register (Address = 0xDE) [Default = 0x00]**PGEN\_COLOR14\_PORT1 is shown in [Table 7-526](#).Return to the [Summary Table](#).**Table 7-526. PGEN\_COLOR14\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

**7.6.2.7.76 PGEN\_COLOR15\_PORT1 Register (Address = 0xDF) [Default = 0x00]**PGEN\_COLOR15\_PORT1 is shown in [Table 7-527](#).Return to the [Summary Table](#).**Table 7-527. PGEN\_COLOR15\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR15	R/W	0x0	Pattern Generator Color 15 For Fixed Color Patterns, this register controls the sixteenth byte of the fixed color pattern.

**7.6.2.7.77 CRC\_CHK\_CTL\_PORT1 Register (Address = 0xE0) [Default = 0x00]**CRC\_CHK\_CTL\_PORT1 is shown in [Table 7-528](#).Return to the [Summary Table](#).**Table 7-528. CRC\_CHK\_CTL\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	CLR_CRC_CNT	R/W	0x0	1: Clears CRC checker counters
0	CRC_ENABLE	R/W	0x0	1: Enables CRC checker

**7.6.2.7.78 CRC\_CHK\_STS\_PORT1 Register (Address = 0xE1) [Default = 0x00]**CRC\_CHK\_STS\_PORT1 is shown in [Table 7-529](#).Return to the [Summary Table](#).**Table 7-529. CRC\_CHK\_STS\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	SHORT_PKT_DET	R	0x0	Short Packet (FS) Detected; Cleared by CLR_CRC_CNT
4	LONG_PKT_DET	R	0x0	Long Packet Detected; Cleared by CLR_CRC_CNT
3	ECC_ERR	R	0x0	ECC Error detected; Cleared by CLR_CRC_CNT
2	ECC_COR	R	0x0	ECC Correction detected; Cleared by CLR_CRC_CNT
1	LENGTH_ERR	R	0x0	Line Length Error detected; Cleared by CLR_CRC_CNT
0	CRC_ERR	R	0x0	CRC Error detected; Cleared by CLR_CRC_CNT

**7.6.2.7.79 LONG\_PKT\_CNT\_B0\_PORT1 Register (Address = 0xE2) [Default = 0x00]**LONG\_PKT\_CNT\_B0\_PORT1 is shown in [Table 7-530](#).

Return to the [Summary Table](#).

**Table 7-530. LONG\_PKT\_CNT\_B0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LONG_PKT_CNT_B0	R	0x0	Long Packet Count [7:0]; Cleared by CLR_CRC_CNT

**7.6.2.7.80 LONG\_PKT\_CNT\_B1\_PORT1 Register (Address = 0xE3) [Default = 0x00]**

LONG\_PKT\_CNT\_B1\_PORT1 is shown in [Table 7-531](#).

Return to the [Summary Table](#).

**Table 7-531. LONG\_PKT\_CNT\_B1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LONG_PKT_CNT_B1	R	0x0	Long Packet Count [15:8]; Cleared by CLR_CRC_CNT

**7.6.2.7.81 SHORT\_PKT\_CNT\_B0\_PORT1 Register (Address = 0xE4) [Default = 0x00]**

SHORT\_PKT\_CNT\_B0\_PORT1 is shown in [Table 7-532](#).

Return to the [Summary Table](#).

**Table 7-532. SHORT\_PKT\_CNT\_B0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	SHORT_PKT_CNT_B0	R	0x0	Short Packet (FS) Count [7:0]; Cleared by CLR_CRC_CNT

**7.6.2.7.82 SHORT\_PKT\_CNT\_B1\_PORT1 Register (Address = 0xE5) [Default = 0x00]**

SHORT\_PKT\_CNT\_B1\_PORT1 is shown in [Table 7-533](#).

Return to the [Summary Table](#).

**Table 7-533. SHORT\_PKT\_CNT\_B1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	SHORT_PKT_CNT_B1	R	0x0	Short Packet (FS) Count [15:8]; Cleared by CLR_CRC_CNT

**7.6.2.7.83 CRC\_ERR\_CNT\_B0\_PORT1 Register (Address = 0xE6) [Default = 0x00]**

CRC\_ERR\_CNT\_B0\_PORT1 is shown in [Table 7-534](#).

Return to the [Summary Table](#).

**Table 7-534. CRC\_ERR\_CNT\_B0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CRC_ERR_CNT_B0	R	0x0	CRC Error Count [7:0] Cleared by CLR_CRC_CNT

**7.6.2.7.84 CRC\_ERR\_CNT\_B1\_PORT1 Register (Address = 0xE7) [Default = 0x00]**

CRC\_ERR\_CNT\_B1\_PORT1 is shown in [Table 7-535](#).

Return to the [Summary Table](#).

**Table 7-535. CRC\_ERR\_CNT\_B1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CRC_ERR_CNT_B1	R	0x0	CRC Error Count [15:8] Cleared by CLR_CRC_CNT

**7.6.2.7.85 ECC\_ERR\_CNT\_B0\_PORT1 Register (Address = 0xE8) [Default = 0x00]**ECC\_ERR\_CNT\_B0\_PORT1 is shown in [Table 7-536](#).Return to the [Summary Table](#).**Table 7-536. ECC\_ERR\_CNT\_B0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ECC_ERR_CNT_B0	R	0x0	ECC Error Count [7:0] Cleared by CLR_CRC_CNT

**7.6.2.7.86 ECC\_ERR\_CNT\_B1\_PORT1 Register (Address = 0xE9) [Default = 0x00]**ECC\_ERR\_CNT\_B1\_PORT1 is shown in [Table 7-537](#).Return to the [Summary Table](#).**Table 7-537. ECC\_ERR\_CNT\_B1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ECC_ERR_CNT_B1	R	0x0	ECC Error Count [15:8] Cleared by CLR_CRC_CNT

**7.6.2.7.87 ECC\_COR\_CNT\_B0\_PORT1 Register (Address = 0xEA) [Default = 0x00]**ECC\_COR\_CNT\_B0\_PORT1 is shown in [Table 7-538](#).Return to the [Summary Table](#).**Table 7-538. ECC\_COR\_CNT\_B0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ECC_COR_CNT_B0	R	0x0	ECC Correction Count [7:0] Cleared by CLR_CRC_CNT

**7.6.2.7.88 ECC\_COR\_CNT\_B1\_PORT1 Register (Address = 0xEB) [Default = 0x00]**ECC\_COR\_CNT\_B1\_PORT1 is shown in [Table 7-539](#).Return to the [Summary Table](#).**Table 7-539. ECC\_COR\_CNT\_B1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	ECC_COR_CNT_B1	R	0x0	ECC Correction Count [15:8] Cleared by CLR_CRC_CNT

**7.6.2.7.89 LEN\_ERR\_CNT\_B0\_PORT1 Register (Address = 0xEC) [Default = 0x00]**LEN\_ERR\_CNT\_B0\_PORT1 is shown in [Table 7-540](#).Return to the [Summary Table](#).

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**Table 7-540. LEN\_ERR\_CNT\_B0\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LEN_ERR_CNT_B0	R	0x0	Line Length Error Count [7:0] Cleared by CLR_CRC_CNT

### 7.6.2.7.90 LEN\_ERR\_CNT\_B1\_PORT1 Register (Address = 0xED) [Default = 0x00]

LEN\_ERR\_CNT\_B1\_PORT1 is shown in [Table 7-541](#).

Return to the [Summary Table](#).

**Table 7-541. LEN\_ERR\_CNT\_B1\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LEN_ERR_CNT_B1	R	0x0	Line Length Error Count [15:8] Cleared by CLR_CRC_CNT

### 7.6.2.8 Page\_9\_DFT Registers

[Table 7-542](#) lists the memory-mapped registers for the Page\_9\_DFT registers. All register offset addresses not listed in [Table 7-542](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-542. PAGE\_9\_DFT Registers**

Address	Acronym	Register Name	Section
0x84	ENCODER_MODE_PORT0	ENCODER_MODE_PORT0	Go
0x88	ALARM_BC_EN_PORT0	ALARM_BC_EN_PORT0	Go
0x8B	FORCE_BIST_ERR	FORCE_BIST_ERR	Go
0x8C	INTR_CTL_FPD4_PORT0	INTR_CTL_FPD4_PORT0	Go
0x8D	INTR_STS_FPD4_PORT0	INTR_STS_FPD4_PORT0	Go
0x94	ENCODER_MODE_PORT1	ENCODER_MODE_PORT1	Go
0x98	ALARM_BC_EN_PORT1	ALARM_BC_EN_PORT1	Go
0x9C	INTR_CTL_FPD4_PORT1	INTR_CTL_FPD4_PORT1	Go
0x9D	INTR_STS_FPD4_PORT1	INTR_STS_FPD4_PORT1	Go
0xC9	REG_GPIO_EN_PULL_LOW_1	REG_GPIO_EN_PULL_LOW_1	Go
0xCA	REG_GPIO_EN_PULL_LOW_2	REG_GPIO_EN_PULL_LOW_2	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-543](#) shows the codes that are used for access types in this section.

**Table 7-543. Page\_9\_DFT Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

### 7.6.2.8.1 ENCODER\_MODE\_PORT0 Register (Address = 0x84) [Default = 0x0X]

ENCODER\_MODE\_PORT0 is shown in [Table 7-544](#).

Return to the [Summary Table](#).

**Table 7-544. ENCODER\_MODE\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2:0	FPD_ENCODER_MODE_0	R/W	X	Default value is set by the MODE_SEL2 and MODE_SEL0 pin at power-up This contains the strap Mode values 000: ADAS 40-bit Encode Mode 001: I2I 132-bit Encode Mode Note: when switching modes after power-up, this register must be checked and set to the appropriate encoding mode

**7.6.2.8.2 ALARM\_BC\_EN\_PORT0 Register (Address = 0x88) [Default = 0x00]**ALARM\_BC\_EN\_PORT0 is shown in [Table 7-545](#).Return to the [Summary Table](#).**Table 7-545. ALARM\_BC\_EN\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	BCC_TARGET_TO_ERR_OR_EN	R/W	0x0	Enable BCC_TARGET_TO_ERROR alarm
5	BCC_TARGET_ERROR_EN	R/W	0x0	Enable BCC_TARGET_ERROR alarm
4	BCC_CONTROLLER_TO_ERROR_EN	R/W	0x0	Enable BC BCC_CONTROLLER_TO_ERR alarm
3	BCC_CONTROLLER_ERROR_EN	R/W	0x0	Enable BCC_CONTROLLER_ERROR alarm
2	BCC_DATA_ERROR_EN	R/W	0x0	Enable BCC_DATA_ERROR alarm
1	CRC_ERR_EN	R/W	0x0	Enable CRC_ERR alarm
0	LINK_DETECT_EN	R/W	0x0	Enable LINK_DETECT alarm

**7.6.2.8.3 FORCE\_BIST\_ERR Register (Address = 0x8B) [Default = 0x00]**FORCE\_BIST\_ERR is shown in [Table 7-546](#).Return to the [Summary Table](#).**Table 7-546. FORCE\_BIST\_ERR Register Field Descriptions**

Bit	Field	Type	Default	Description
7	FORCE_FC_ERR	RH/W1S	0x0	Set to force FC error based on the FORCE_ERR_CNT. Self clearing register bit 0: Force Disabled 1: Force Enabled
6:0	FORCE_ERR_CNT	R/W	0x0	Force error count.

**7.6.2.8.4 INTR\_CTL\_FPD4\_PORT0 Register (Address = 0x8C) [Default = 0x00]**INTR\_CTL\_FPD4\_PORT0 is shown in [Table 7-547](#).Return to the [Summary Table](#).**Table 7-547. INTR\_CTL\_FPD4\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

**Table 7-547. INTR\_CTL\_FPD4\_PORT0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	IE_RX_LOCK_DET_INT	R/W	0x0	Enables Interrupt on Receiver Lock Detect
5	IE_RX_Rem_INT	R/W	0x0	Enables Interrupt on Remote Receiver interrupt
4	IE_DES_INT	R/W	0x0	FPD4 Deserializer Interrupt Set to 1 if the Deserializer has sent an interrupt to the Serializer. This is controlled by the Interrupt registers in the Deserializer.
3	IE_RX_LOCK_LOST_DET_INT	R/W	0x0	Enables Interrupt on Receiver Lock Lost Detect
2:0	RESERVED	R	0x0	Reserved

**7.6.2.8.5 INTR\_STS\_FPD4\_PORT0 Register (Address = 0x8D) [Default = 0x00]**INTR\_STS\_FPD4\_PORT0 is shown in [Table 7-548](#).Return to the [Summary Table](#).**Table 7-548. INTR\_STS\_FPD4\_PORT0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_RX_LOCK_DET_INT	RC	0x0	Interrupt on Receiver Lock Detect
5	IS_RX_Rem_INT	RC	0x0	Interrupt on Remote Receiver interrupt
4	IS_DES_INT	RC	0x0	FPD4 Deserializer Interrupt Set to 1 if the Deserializer has sent an interrupt to the Serializer. This is controlled by the Interrupt registers in the Deserializer.
3	IS_RX_LOCK_LOST_DET_INT	RC	0x0	Interrupt on Receiver Lock Lost Detect
2:0	RESERVED	R	0x0	Reserved

**7.6.2.8.6 ENCODER\_MODE\_PORT1 Register (Address = 0x94) [Default = 0x0X]**ENCODER\_MODE\_PORT1 is shown in [Table 7-549](#).Return to the [Summary Table](#).**Table 7-549. ENCODER\_MODE\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2:0	FPD_ENCODER_MODE_1	R/W	X	Default value is set by the MODE_SEL2 and MODE_SEL0 pin at power-up This contains the strap Mode values 000: ADAS 40-bit Encode Mode 001: IVI 132-bit Encode Mode Note: when switching modes after power-up, this register must be checked and set to the appropriate encoding mode

**7.6.2.8.7 ALARM\_BC\_EN\_PORT1 Register (Address = 0x98) [Default = 0x00]**ALARM\_BC\_EN\_PORT1 is shown in [Table 7-550](#).Return to the [Summary Table](#).**Table 7-550. ALARM\_BC\_EN\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

**Table 7-550. ALARM\_BC\_EN\_PORT1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	BCC_TARGET_TO_ERR_OR_EN	R/W	0x0	Enable BCC_TARGET_TO_ERROR alarm
5	BCC_TARGET_ERROR_EN	R/W	0x0	Enable BCC_TARGET_ERROR alarm
4	BCC_CONTROLLER_TO_ERROR_EN	R/W	0x0	Enable BC BCC_CONTROLLER_TO_ERR alarm
3	BCC_CONTROLLER_ERROR_EN	R/W	0x0	Enable BCC_CONTROLLER_ERROR alarm
2	BCC_DATA_ERROR_EN	R/W	0x0	Enable BCC_DATA_ERROR alarm
1	CRC_ERR_EN	R/W	0x0	Enable CRC_ERR alarm
0	LINK_DETECT_EN	R/W	0x0	Enable LINK_DETECT alarm

**7.6.2.8.8 INTR\_CTL\_FPD4\_PORT1 Register (Address = 0x9C) [Default = 0x00]**INTR\_CTL\_FPD4\_PORT1 is shown in [Table 7-551](#).Return to the [Summary Table](#).**Table 7-551. INTR\_CTL\_FPD4\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_RX_LOCK_DET_INT	R/W	0x0	Enables Interrupt on Receiver Lock Detect
5	IE_RX_Rem_INT	R/W	0x0	Enables Interrupt on Remote Receiver interrupt
4	IE_DES_INT	R/W	0x0	FPD4 Deserializer Interrupt Set to 1 if the Deserializer has sent an interrupt to the Serializer. This is controlled by the Interrupt registers in the Deserializer.
3	IE_RX_LOCK_LOST_DET_INT	R/W	0x0	Enables Interrupt on Receiver Lock Lost Detect
2:0	RESERVED	R	0x0	Reserved

**7.6.2.8.9 INTR\_STS\_FPD4\_PORT1 Register (Address = 0x9D) [Default = 0x00]**INTR\_STS\_FPD4\_PORT1 is shown in [Table 7-552](#).Return to the [Summary Table](#).**Table 7-552. INTR\_STS\_FPD4\_PORT1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_RX_LOCK_DET_INT	RC	0x0	Interrupt on Receiver Lock Detect
5	IS_RX_Rem_INT	RC	0x0	Interrupt on Remote Receiver interrupt
4	IS_DES_INT	RC	0x0	FPD4 Deserializer Interrupt Set to 1 if the Deserializer has sent an interrupt to the Serializer. This is controlled by the Interrupt registers in the Deserializer.
3	IS_RX_LOCK_LOST_DET_INT	RC	0x0	Interrupt on Receiver Lock Lost Detect
2:0	RESERVED	R	0x0	Reserved

**7.6.2.8.10 REG\_GPIO\_EN\_PULL\_LOW\_1 Register (Address = 0xC9) [Default = 0xFF]**REG\_GPIO\_EN\_PULL\_LOW\_1 is shown in [Table 7-553](#).

Return to the [Summary Table](#).

**Table 7-553. REG\_GPIO\_EN\_PULL\_LOW\_1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	GPIO_EN_PULL_LOW_7_0	R/W	0xFF	GPIO Enable internal pull down resistors for GPIO 0-7 1= Pull down enabled 0= Pull down disabled

**7.6.2.8.11 REG\_GPIO\_EN\_PULL\_LOW\_2 Register (Address = 0xCA) [Default = 0x27]**

REG\_GPIO\_EN\_PULL\_LOW\_2 is shown in [Table 7-554](#).

Return to the [Summary Table](#).

**Table 7-554. REG\_GPIO\_EN\_PULL\_LOW\_2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	GPIO_EN_PULL_LOW_1_3_8	R/W	0x27	GPIO Enable internal pull down resistors for GPIO 8-13 1= Pull down enabled 0= Pull down disabled

**7.6.2.9 Page\_11\_Link\_Layer Registers**

[Table 7-555](#) lists the memory-mapped registers for the Page\_11\_Link\_Layer registers. All register offset addresses not listed in [Table 7-555](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-555. PAGE\_11\_LINK\_LAYER Registers**

Address	Acronym	Register Name	Section
0x0	LINK_LAYER_CTL	LINK_LAYER_CTL	Go
0x1	LINK0_STREAM_EN	LINK0_STREAM_EN	Go
0x2	LINK0_MAP_REG0	LINK0_MAP_REG0	Go
0x3	LINK0_MAP_REG1	LINK0_MAP_REG1	Go
0x4	LINK0_MAP_REG2	LINK0_MAP_REG2	Go
0x6	LINK0_SLOT_REQ0	LINK0_SLOT_REQ0	Go
0x7	LINK0_SLOT_REQ1	LINK0_SLOT_REQ1	Go
0x8	LINK0_SLOT_REQ2	LINK0_SLOT_REQ2	Go
0x9	LINK0_SLOT_REQ3	LINK0_SLOT_REQ3	Go
0xA	LINK0_SLOT_REQ4	LINK0_SLOT_REQ4	Go
0xB	LINK0_SLOT_REQ5	LINK0_SLOT_REQ5	Go
0xE	LINK0_CONFIG	LINK0_CONFIG	Go
0x11	LINK1_STREAM_EN	LINK1_STREAM_EN	Go
0x12	LINK1_MAP_REG0	LINK1_MAP_REG0	Go
0x13	LINK1_MAP_REG1	LINK1_MAP_REG1	Go
0x14	LINK1_MAP_REG2	LINK1_MAP_REG2	Go
0x16	LINK1_SLOT_REQ0	LINK1_SLOT_REQ0	Go
0x17	LINK1_SLOT_REQ1	LINK1_SLOT_REQ1	Go
0x18	LINK1_SLOT_REQ2	LINK1_SLOT_REQ2	Go
0x19	LINK1_SLOT_REQ3	LINK1_SLOT_REQ3	Go
0x1A	LINK1_SLOT_REQ4	LINK1_SLOT_REQ4	Go
0x1B	LINK1_SLOT_REQ5	LINK1_SLOT_REQ5	Go
0x1E	LINK1_CONFIG	LINK1_CONFIG	Go

**Table 7-555. PAGE\_11\_LINK\_LAYER Registers (continued)**

Address	Acronym	Register Name	Section
0x20	VP_WIDTH0	VP_WIDTH0	Go
0x22	PKT_FIFO_OVRFLW_STS	PKT_FIFO_OVRFLW_STS	Go
0x23	PKT_FIFO_OVRFLW_CLR	PKT_FIFO_OVRFLW_CLR	Go
0x24	CORRUPT_PKT_CRC	CORRUPT_PKT_CRC	Go
0x25	LINK_ECC_TEST0	LINK_ECC_TEST0	Go
0x26	LINK_ECC_TEST1	LINK_ECC_TEST1	Go
0x27	LINK_ECC_TEST2	LINK_ECC_TEST2	Go
0x31	VP_VPOL_CTL	VP_VPOL_CTL	Go
0x32	VP_OVERRIDE_CTL	VP_OVERRIDE_CTL	Go
0x80	ABUFF0_CTL0	ABUFF0_CTL0	Go
0x81	ABUFF0_CTL1	ABUFF0_CTL1	Go
0x82	ABUFF0_CTL2	ABUFF0_CTL2	Go
0x86	ABUFF0_CTL6	ABUFF0_CTL6	Go
0x88	ABUFF1_CTL0	ABUFF1_CTL0	Go
0x89	ABUFF1_CTL1	ABUFF1_CTL1	Go
0x8A	ABUFF1_CTL2	ABUFF1_CTL2	Go
0x8E	ABUFF1_CTL6	ABUFF1_CTL6	Go
0x90	ABUFF2_CTL0	ABUFF2_CTL0	Go
0x91	ABUFF2_CTL1	ABUFF2_CTL1	Go
0x92	ABUFF2_CTL2	ABUFF2_CTL2	Go
0x96	ABUFF2_CTL6	ABUFF2_CTL6	Go
0x98	ABUFF3_CTL0	ABUFF3_CTL0	Go
0x99	ABUFF3_CTL1	ABUFF3_CTL1	Go
0x9A	ABUFF3_CTL2	ABUFF3_CTL2	Go
0x9E	ABUFF3_CTL6	ABUFF3_CTL6	Go
0xA0	ABUFF4_CTL0	ABUFF4_CTL0	Go
0xA1	ABUFF4_CTL1	ABUFF4_CTL1	Go
0xA2	ABUFF4_CTL2	ABUFF4_CTL2	Go
0xA6	ABUFF4_CTL6	ABUFF4_CTL6	Go
0xA8	ABUFF5_CTL0	ABUFF5_CTL0	Go
0xA9	ABUFF5_CTL1	ABUFF5_CTL1	Go
0xAA	ABUFF5_CTL2	ABUFF5_CTL2	Go
0xAE	ABUFF5_CTL6	ABUFF5_CTL6	Go
0xB0	ABUFF6_CTL0	ABUFF6_CTL0	Go
0xB1	ABUFF6_CTL1	ABUFF6_CTL1	Go
0xB2	ABUFF6_CTL2	ABUFF6_CTL2	Go
0xB6	ABUFF6_CTL6	ABUFF6_CTL6	Go
0xB8	ABUFF7_CTL0	ABUFF7_CTL0	Go
0xB9	ABUFF7_CTL1	ABUFF7_CTL1	Go
0xBA	ABUFF7_CTL2	ABUFF7_CTL2	Go
0xBE	ABUFF7_CTL6	ABUFF7_CTL6	Go
0xC0	ABUFF8_CTL0	ABUFF8_CTL0	Go
0xC1	ABUFF8_CTL1	ABUFF8_CTL1	Go
0xC2	ABUFF8_CTL2	ABUFF8_CTL2	Go
0xC6	ABUFF8_CTL6	ABUFF8_CTL6	Go

**Table 7-555. PAGE\_11\_LINK\_LAYER Registers (continued)**

Address	Acronym	Register Name	Section
0xC8	ABUFF9_CTL0	ABUFF9_CTL0	Go
0xC9	ABUFF9_CTL1	ABUFF9_CTL1	Go
0xCA	ABUFF9_CTL2	ABUFF9_CTL2	Go
0xCE	ABUFF9_CTL6	ABUFF9_CTL6	Go
0xD0	ABUFF10_CTL0	ABUFF10_CTL0	Go
0xD1	ABUFF10_CTL1	ABUFF10_CTL1	Go
0xD2	ABUFF10_CTL2	ABUFF10_CTL2	Go
0xD6	ABUFF10_CTL6	ABUFF10_CTL6	Go
0xD8	ABUFF11_CTL0	ABUFF11_CTL0	Go
0xD9	ABUFF11_CTL1	ABUFF11_CTL1	Go
0xDA	ABUFF11_CTL2	ABUFF11_CTL2	Go
0xDE	ABUFF11_CTL6	ABUFF11_CTL6	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-556](#) shows the codes that are used for access types in this section.

**Table 7-556. Page\_11\_Link\_Layer Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
<b>Write Type</b>		
W	W	Write
W1SS	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

#### 7.6.2.9.1 LINK\_LAYER\_CTL Register (Address = 0x0) [Default = 0x00]

LINK\_LAYER\_CTL is shown in [Table 7-557](#).

Return to the [Summary Table](#).

**Table 7-557. LINK\_LAYER\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	EN_NEW_TSLOT1	RH/W1SS	0x0	Enable New Time-slot assignments for Link Layer 1 Setting this bit to a 1 will enable the device to begin using the new time-slot information programmed into the LINK1_SLOT_REQ registers. This register bit will be cleared once the new time-slot information has been enabled
2	LINK_LAYER_1_EN	R/W	0x0	Link Layer enable for Link Layer 1 0x0= all Link Layer 1 video streams disabled 0x1= Video Streams with LINK1_STREAM_EN bits set will be enabled

**Table 7-557. LINK\_LAYER\_CTL Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	EN_NEW_TSLOT0	RH/W1SS	0x0	Enable New Time-slot assignments for Link Layer 0 Setting this bit to a 1 will enable the device to begin using the new time-slot information programmed into the LINKx_SLOT_REQ registers. This register bit will be cleared once the new time-slot information has been enabled
0	LINK_LAYER_0_EN	R/W	0x0	Link Layer enable for Link Layer 0 0x0= all Link Layer 0 video streams disabled 0x1= Video Streams with LINK0_STREAM_EN bits set will be enabled

**7.6.2.9.2 LINK0\_STREAM\_EN Register (Address = 0x1) [Default = 0x00]**LINK0\_STREAM\_EN is shown in [Table 7-558](#).Return to the [Summary Table](#).**Table 7-558. LINK0\_STREAM\_EN Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	LINK0_STREAM_EN3	R/W	0x0	Link Layer 0 Stream Enable 3 Setting this bit will enable the Link Layer processing for the associated Video Stream.
2	LINK0_STREAM_EN2	R/W	0x0	Link Layer 0 Stream Enable 2 Setting this bit will enable the Link Layer processing for the associated Video Stream.
1	LINK0_STREAM_EN1	R/W	0x0	Link Layer 0 Stream Enable 1 Setting this bit will enable the Link Layer processing for the associated Video Stream.
0	LINK0_STREAM_EN0	R/W	0x0	Link Layer 0 Stream Enable 0 Setting this bit will enable the Link Layer processing for the associated Video Stream.

**7.6.2.9.3 LINK0\_MAP\_REG0 Register (Address = 0x2) [Default = 0x10]**LINK0\_MAP\_REG0 is shown in [Table 7-559](#).Return to the [Summary Table](#).**Table 7-559. LINK0\_MAP\_REG0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK0_STREAM_MAP1	R/W	0x1	Link Layer Stream 1 Map Selects the Video Processor for assignment to Video Stream 1. Value may be in the range of 0-5. If the LINK0_STREAM_EN[1] is set to 0, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK0_STREAM_MAP0	R/W	0x0	Link Layer Stream 0 Map Selects the Video Processor for assignment to Video Stream 0. Value may be in the range of 0-5. If the LINK0_STREAM_EN[0] is set to 0, this value will be ignored.

**7.6.2.9.4 LINK0\_MAP\_REG1 Register (Address = 0x3) [Default = 0x32]**LINK0\_MAP\_REG1 is shown in [Table 7-560](#).Return to the [Summary Table](#).**Table 7-560. LINK0\_MAP\_REG1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK0_STREAM_MAP3	R/W	0x3	Link Layer Stream 3 Map Selects the Video Processor for assignment to Video Stream 3. Value may be in the range of 0-5. If the LINK0_STREAM_EN[3] is set to 0, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK0_STREAM_MAP2	R/W	0x2	Link Layer Stream 2 Map Selects the Video Processor for assignment to Video Stream 2. Value may be in the range of 0-5. If the LINK0_STREAM_EN[2] is set to 0, this value will be ignored.

**7.6.2.9.5 LINK0\_MAP\_REG2 Register (Address = 0x4) [Default = 0x00]**LINK0\_MAP\_REG2 is shown in [Table 7-561](#).Return to the [Summary Table](#).**Table 7-561. LINK0\_MAP\_REG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK0_STREAM_MAP5	R/W	0x0	Link Layer Stream 5 Map Selects the Video Processor for assignment to Video Stream 5. Value may be in the range of 0-5. If the LINK0_STREAM_EN[3] is set to 5, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK0_STREAM_MAP4	R/W	0x0	Link Layer Stream 4 Map Selects the Video Processor for assignment to Video Stream 4. Value may be in the range of 0-5. If the LINK0_STREAM_EN[2] is set to 4, this value will be ignored.

**7.6.2.9.6 LINK0\_SLOT\_REQ0 Register (Address = 0x6) [Default = 0x00]**LINK0\_SLOT\_REQ0 is shown in [Table 7-562](#).Return to the [Summary Table](#).**Table 7-562. LINK0\_SLOT\_REQ0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ0	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 0. The total number of LINK0 slots should add up to 65. If less than 65 are assigned, the extra slots will be assigned to stream 0.

**7.6.2.9.7 LINK0\_SLOT\_REQ1 Register (Address = 0x7) [Default = 0x00]**LINK0\_SLOT\_REQ1 is shown in [Table 7-563](#).Return to the [Summary Table](#).

**Table 7-563. LINK0\_SLOT\_REQ1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ1	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 1.

**7.6.2.9.8 LINK0\_SLOT\_REQ2 Register (Address = 0x8) [Default = 0x00]**LINK0\_SLOT\_REQ2 is shown in [Table 7-564](#).Return to the [Summary Table](#).**Table 7-564. LINK0\_SLOT\_REQ2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ2	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 2.

**7.6.2.9.9 LINK0\_SLOT\_REQ3 Register (Address = 0x9) [Default = 0x00]**LINK0\_SLOT\_REQ3 is shown in [Table 7-565](#).Return to the [Summary Table](#).**Table 7-565. LINK0\_SLOT\_REQ3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK0_SLOT_REQ3	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 3.

**7.6.2.9.10 LINK0\_SLOT\_REQ4 Register (Address = 0xA) [Default = 0x00]**LINK0\_SLOT\_REQ4 is shown in [Table 7-566](#).Return to the [Summary Table](#).**Table 7-566. LINK0\_SLOT\_REQ4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:0	LINK0_SLOT_REQ4	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 4.

**7.6.2.9.11 LINK0\_SLOT\_REQ5 Register (Address = 0xB) [Default = 0x00]**LINK0\_SLOT\_REQ5 is shown in [Table 7-567](#).Return to the [Summary Table](#).**Table 7-567. LINK0\_SLOT\_REQ5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:0	LINK0_SLOT_REQ5	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 5.

**7.6.2.9.12 LINK0\_CONFIG Register (Address = 0xE) [Default = 0x00]**LINK0\_CONFIG is shown in [Table 7-568](#).Return to the [Summary Table](#).**Table 7-568. LINK0\_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	LINK0_POL_OV	R/W	0x0	
0	LINK0_EVENT_MODE_EN	R/W	0x0	Link Layer 0 Event Mode enable This bit controls how the link layer sends HSync/VSync information. 0: Send HSync/VSync pulses with active period matching incoming video 1: Send a single cycle event to indicate HSync and VSync

**7.6.2.9.13 LINK1\_STREAM\_EN Register (Address = 0x11) [Default = 0x00]**LINK1\_STREAM\_EN is shown in [Table 7-569](#).Return to the [Summary Table](#).**Table 7-569. LINK1\_STREAM\_EN Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	LINK1_STREAM_EN5	R/W	0x0	Link Layer 1 Stream Enable 5 Setting this bit will enable the Link Layer processing for the associated Video Stream.
4	LINK1_STREAM_EN4	R/W	0x0	Link Layer 1 Stream Enable 4 Setting this bit will enable the Link Layer processing for the associated Video Stream.
3	LINK1_STREAM_EN3	R/W	0x0	Link Layer 1 Stream Enable 3 Setting this bit will enable the Link Layer processing for the associated Video Stream.
2	LINK1_STREAM_EN2	R/W	0x0	Link Layer 1 Stream Enable 2 Setting this bit will enable the Link Layer processing for the associated Video Stream.
1	LINK1_STREAM_EN1	R/W	0x0	Link Layer 1 Stream Enable 1 Setting this bit will enable the Link Layer processing for the associated Video Stream.
0	LINK1_STREAM_EN0	R/W	0x0	Link Layer 1 Stream Enable 0 Setting this bit will enable the Link Layer processing for the associated Video Stream.

**7.6.2.9.14 LINK1\_MAP\_REG0 Register (Address = 0x12) [Default = 0x00]**LINK1\_MAP\_REG0 is shown in [Table 7-570](#).Return to the [Summary Table](#).**Table 7-570. LINK1\_MAP\_REG0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK1_STREAM_MAP1	R/W	0x0	Link Layer Stream 1 Map Selects the Video Processor for assignment to Video Stream 1. Value may be in the range of 0-5. If the LINK1_STREAM_EN[1] is set to 0, this value will be ignored.
3	RESERVED	R	0x0	Reserved

**Table 7-570. LINK1\_MAP\_REG0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
2:0	LINK1_STREAM_MAP0	R/W	0x0	Link Layer Stream 0 Map Selects the Video Processor for assignment to Video Stream 0. Value may be in the range of 0-5. If the LINK1_STREAM_EN[0] is set to 0, this value will be ignored.

**7.6.2.9.15 LINK1\_MAP\_REG1 Register (Address = 0x13) [Default = 0x00]**LINK1\_MAP\_REG1 is shown in [Table 7-571](#).Return to the [Summary Table](#).**Table 7-571. LINK1\_MAP\_REG1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK1_STREAM_MAP3	R/W	0x0	Link Layer Stream 3 Map Selects the Video Processor for assignment to Video Stream 3. Value may be in the range of 0-5. If the LINK1_STREAM_EN[3] is set to 0, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK1_STREAM_MAP2	R/W	0x0	Link Layer Stream 2 Map Selects the Video Processor for assignment to Video Stream 2. Value may be in the range of 0-5. If the LINK1_STREAM_EN[2] is set to 0, this value will be ignored.

**7.6.2.9.16 LINK1\_MAP\_REG2 Register (Address = 0x14) [Default = 0x00]**LINK1\_MAP\_REG2 is shown in [Table 7-572](#).Return to the [Summary Table](#).**Table 7-572. LINK1\_MAP\_REG2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK1_STREAM_MAP5	R/W	0x0	Link Layer Stream 5 Map Selects the Video Processor for assignment to Video Stream 5. Value may be in the range of 0-5. If the LINK1_STREAM_EN[3] is set to 5, this value will be ignored.
3	RESERVED	R	0x0	Reserved
2:0	LINK1_STREAM_MAP4	R/W	0x0	Link Layer Stream 4 Map Selects the Video Processor for assignment to Video Stream 4. Value may be in the range of 0-5. If the LINK1_STREAM_EN[2] is set to 4, this value will be ignored.

**7.6.2.9.17 LINK1\_SLOT\_REQ0 Register (Address = 0x16) [Default = 0x00]**LINK1\_SLOT\_REQ0 is shown in [Table 7-573](#).Return to the [Summary Table](#).**Table 7-573. LINK1\_SLOT\_REQ0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

**Table 7-573. LINK1\_SLOT\_REQ0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:0	LINK1_SLOT_REQ0	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 0. The total number of LINK1 slots should add up to 65. If less than 65 are assigned, the extra slots will be assigned to stream 0.

**7.6.2.9.18 LINK1\_SLOT\_REQ1 Register (Address = 0x17) [Default = 0x00]**LINK1\_SLOT\_REQ1 is shown in [Table 7-574](#).Return to the [Summary Table](#).**Table 7-574. LINK1\_SLOT\_REQ1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ1	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 1.

**7.6.2.9.19 LINK1\_SLOT\_REQ2 Register (Address = 0x18) [Default = 0x00]**LINK1\_SLOT\_REQ2 is shown in [Table 7-575](#).Return to the [Summary Table](#).**Table 7-575. LINK1\_SLOT\_REQ2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ2	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 2.

**7.6.2.9.20 LINK1\_SLOT\_REQ3 Register (Address = 0x19) [Default = 0x00]**LINK1\_SLOT\_REQ3 is shown in [Table 7-576](#).Return to the [Summary Table](#).**Table 7-576. LINK1\_SLOT\_REQ3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ3	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 3.

**7.6.2.9.21 LINK1\_SLOT\_REQ4 Register (Address = 0x1A) [Default = 0x00]**LINK1\_SLOT\_REQ4 is shown in [Table 7-577](#).Return to the [Summary Table](#).**Table 7-577. LINK1\_SLOT\_REQ4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ4	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 4.

**7.6.2.9.22 LINK1\_SLOT\_REQ5 Register (Address = 0x1B) [Default = 0x00]**LINK1\_SLOT\_REQ5 is shown in [Table 7-578](#).Return to the [Summary Table](#).**Table 7-578. LINK1\_SLOT\_REQ5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ5	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending Video Stream 5.

**7.6.2.9.23 LINK1\_CONFIG Register (Address = 0x1E) [Default = 0x00]**LINK1\_CONFIG is shown in [Table 7-579](#).Return to the [Summary Table](#).**Table 7-579. LINK1\_CONFIG Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	LINK1_POL_OV	R/W	0x0	Link polarity override for PORT1
0	LINK1_EVENT_MODE_EN	R/W	0x0	Link Layer 1 Event Mode enable This bit controls how the link layer sends HSync/VSync information. 0: Send HSync/VSync pulses with active period matching incoming video 1: Send a single cycle event to indicate HSync and VSync

**7.6.2.9.24 VP\_WIDTH0 Register (Address = 0x20) [Default = 0x55]**VP\_WIDTH0 is shown in [Table 7-580](#).Return to the [Summary Table](#).**Table 7-580. VP\_WIDTH0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	VP3_WIDTH	R/W	0x1	Pixel Width for Video Processor 3 This field controls the pixel width for video data from the video processor. 0: 18-bit 1: 24-bit 2: 30-bit 3: Reserved
5:4	VP2_WIDTH	R/W	0x1	Pixel Width for Video Processor 2 This field controls the pixel width for video data from the video processor. 0: 18-bit 1: 24-bit 2: 30-bit 3: Reserved
3:2	VP1_WIDTH	R/W	0x1	Pixel Width for Video Processor 1 This field controls the pixel width for video data from the video processor. 0: 18-bit 1: 24-bit 2: 30-bit 3: Reserved

**Table 7-580. VP\_WIDTH0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	VP0_WIDTH	R/W	0x1	Pixel Width for Video Processor 0 This field controls the pixel width for video data from the video processor. 0: 18-bit 1: 24-bit 2: 30-bit 3: Reserved

**7.6.2.9.25 PKT\_FIFO\_OVRFLW\_STS Register (Address = 0x22) [Default = 0x00]**PKT\_FIFO\_OVRFLW\_STS is shown in [Table 7-581](#).Return to the [Summary Table](#).**Table 7-581. PKT\_FIFO\_OVRFLW\_STS Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	RESERVED
5:0	PKT_FIFO_OVRFLW_STS	R	0x0	Packet FIFO overflow status for each video processor. Bits [3:0] are valid. A buffer can overflow if the fill rate (VPx quad pclk) is much faster than the drain rate (link layer slot assignment BW for the stream assigned to VPx).

**7.6.2.9.26 PKT\_FIFO\_OVRFLW\_CLR Register (Address = 0x23) [Default = 0x00]**PKT\_FIFO\_OVRFLW\_CLR is shown in [Table 7-582](#).Return to the [Summary Table](#).**Table 7-582. PKT\_FIFO\_OVRFLW\_CLR Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	RESERVED
5:0	PKT_FIFO_OVRFLW_CLR	R/W	0x0	Clear packet FIFO overflow status for each

**7.6.2.9.27 CORRUPT\_PKT\_CRC Register (Address = 0x24) [Default = 0x00]**CORRUPT\_PKT\_CRC is shown in [Table 7-583](#).Return to the [Summary Table](#).**Table 7-583. CORRUPT\_PKT\_CRC Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	RESERVED
5:0	CORRUPT_PKT_CRC	R/W	0x0	Corrupt Stream CRC Set bit to 1 to corrupt the CRC for each video stream data packet. CRC will be corrupted on each packet until this register is cleared.

**7.6.2.9.28 LINK\_ECC\_TEST0 Register (Address = 0x25) [Default = 0x00]**LINK\_ECC\_TEST0 is shown in [Table 7-584](#).Return to the [Summary Table](#).

**Table 7-584. LINK\_ECC\_TEST0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6	FORCE_ECC_STREAM_EN	R/W	0x0	Enable Stream filter matching for forcing errors If this bit is set to 0, the FORCE_ECC_STREAM control will be ignored and errors will be forced on all active video streams If this bit is set to 1, the FORCE_ECC_STREAM field will be used to only force errors on the selected stream.
5	FORCE_ECC_TYPE_EN	R/W	0x0	Enable Type Field matching for forcing errors If this bit is set to 0, the type field will be ignored and errors will be forced on any Control frame If this bit is set to 1, the FORCE_ECC_TYPE field will be used to only force errors on control frames that match that type field.
4	FORCE_ECC_2BIT_SEL	R/W	0x0	Force Errors Number of bits control Indicates the number of bits which will have errors forced in the control field 0: 1-bit error 1: 2-bit error
3:2	FORCE_ECC_ERR_FIELD_SEL	R/W	0x0	Force Errors field select Control frames include 3 or 4 copies of the control information. This control allows forcing errors on 1 to all 4 control frame fields: 0: Force error on 1 field only 1: Force error on 2 fields 2: Force error on 3 fields 3: Force error on all control fields
1	FORCE_1_CTL_ECC_ERROR	R/W	0x0	Force Errors on a single ECC Control Frame Set bit to 1 to force an error on a single Forward Channel control frame which match requirements in the LINK_ECC_TEST register settings.
0	FORCE_CTL_ECC_ERR	R/W	0x0	Force Continuous Errors on ECC Control Frames Set bit to 1 to force errors on Forward Channel control frames which match requirements in the LINK_ECC_TEST register settings.

**7.6.2.9.29 LINK\_ECC\_TEST1 Register (Address = 0x26) [Default = 0x08]**LINK\_ECC\_TEST1 is shown in [Table 7-585](#).Return to the [Summary Table](#).**Table 7-585. LINK\_ECC\_TEST1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	RESERVED
4	FORCE_ECC_LINK1_SELECT	R/W	0x0	Select Link Layer 1 Set bit to 1 to force errors on Link 1
3	FORCE_ECC_LINK0_SELECT	R/W	0x1	Select Link Layer 0 Set bit to 1 to force errors on Link 0
2:0	FORCE_ECC_STREAM	R/W	0x0	Force ECC Stream control If FORCE_ECC_STREAM_EN is set, errors will be forced only on the selected stream.

**7.6.2.9.30 LINK\_ECC\_TEST2 Register (Address = 0x27) [Default = 0x00]**LINK\_ECC\_TEST2 is shown in [Table 7-586](#).Return to the [Summary Table](#).

**Table 7-586. LINK\_ECC\_TEST2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	FORCE_ECC_TYPE	R/W	0x0	Force ECC Type field If FORCE_ECC_TYPE_EN is set, errors will be force on control frames with a Type field that matches this programmed value.

**7.6.2.9.31 VP\_VPOL\_CTL Register (Address = 0x31) [Default = 0x00]**VP\_VPOL\_CTL is shown in [Table 7-587](#).Return to the [Summary Table](#).**Table 7-587. VP\_VPOL\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	RESERVED
5	VS_POL_OV5	R/W	0x0	VSync Polarity override value for input video Stream 5 If VP_POL_OVERRIDE is set to 1, this bit controls the VSync polarity 0: Active high polarity 1: Active low polarity This bit is ignored if VP_POL_OVERRIDE is 0.
4	VS_POL_OV4	R/W	0x0	VSync Polarity override value for input video Stream 4 If VP_POL_OVERRIDE is set to 1, this bit controls the VSync polarity 0: Active high polarity 1: Active low polarity This bit is ignored if VP_POL_OVERRIDE is 0.
3	VS_POL_OV3	R/W	0x0	VSync Polarity override value for input video Stream 3 If VP_POL_OVERRIDE is set to 1, this bit controls the VSync polarity 0: Active high polarity 1: Active low polarity This bit is ignored if VP_POL_OVERRIDE is 0.
2	VS_POL_OV2	R/W	0x0	VSync Polarity override value for input video Stream 2 If VP_POL_OVERRIDE is set to 1, this bit controls the VSync polarity 0: Active high polarity 1: Active low polarity This bit is ignored if VP_POL_OVERRIDE is 0.
1	VS_POL_OV1	R/W	0x0	VSync Polarity override value for input video Stream 1 If VP_POL_OVERRIDE is set to 1, this bit controls the VSync polarity 0: Active high polarity 1: Active low polarity This bit is ignored if VP_POL_OVERRIDE is 0.
0	VS_POL_OV0	R/W	0x0	VSync Polarity override value for input video Stream 0 If VP_POL_OVERRIDE is set to 1, this bit controls the VSync polarity 0: Active high polarity 1: Active low polarity This bit is ignored if VP_POL_OVERRIDE is 0.

**7.6.2.9.32 VP\_OVERRIDE\_CTL Register (Address = 0x32) [Default = 0x00]**VP\_OVERRIDE\_CTL is shown in [Table 7-588](#).Return to the [Summary Table](#).

**Table 7-588. VP\_OVERRIDE\_CTL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:1	RESERVED	R	0x0	RESERVED
0	VP_POL_OVERRIDE	R/W	0x0	Video Stream polarity override enable Setting this bit to 1 overrides the HSync and VSync polarity controls using the polarity override values in the VP_HPOL_CTL and VP_VPOL_CTL registers.

**7.6.2.9.33 ABUFF0\_CTL0 Register (Address = 0x80) [Default = 0x01]**ABUFF0\_CTL0 is shown in [Table 7-589](#).Return to the [Summary Table](#).**Table 7-589. ABUFF0\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x1	1 Activates the ABUFF block

**7.6.2.9.34 ABUFF0\_CTL1 Register (Address = 0x81) [Default = 0x00]**ABUFF0\_CTL1 is shown in [Table 7-590](#).Return to the [Summary Table](#).**Table 7-590. ABUFF0\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DSI GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.35 ABUFF0\_CTL2 Register (Address = 0x82) [Default = 0x00]**ABUFF0\_CTL2 is shown in [Table 7-591](#).Return to the [Summary Table](#).**Table 7-591. ABUFF0\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5

**Table 7-591. ABUFF0\_CTL2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4:0	SRC_TO_ABUFF_SEL	R/W	0x0	Source of ABUFF data: 0x14= DS1 Port 0; Virtual Channel 0 0x15= DS1 Port 0; Virtual Channel 1 0x16= DS1 Port 0; Virtual Channel 2 0x17= DS1 Port 0; Virtual Channel 3 0x18= DS1 Port 1; Virtual Channel 0 0x19= DS1 Port 1; Virtual Channel 1 0x1A= DS1 Port 1; Virtual Channel 2 0x1B= DS1 Port 1; Virtual Channel 3

**7.6.2.9.36 ABUFF0\_CTL6 Register (Address = 0x86) [Default = 0x00]**ABUFF0\_CTL6 is shown in [Table 7-592](#).Return to the [Summary Table](#).**Table 7-592. ABUFF0\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.37 ABUFF1\_CTL0 Register (Address = 0x88) [Default = 0x01]**ABUFF1\_CTL0 is shown in [Table 7-593](#).Return to the [Summary Table](#).**Table 7-593. ABUFF1\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x1	1 Activates the ABUFF block

**7.6.2.9.38 ABUFF1\_CTL1 Register (Address = 0x89) [Default = 0x00]**ABUFF1\_CTL1 is shown in [Table 7-594](#).Return to the [Summary Table](#).**Table 7-594. ABUFF1\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

**Table 7-594. ABUFF1\_CTL1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DS1 GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.39 ABUFF1\_CTL2 Register (Address = 0x8A) [Default = 0x01]**ABUFF1\_CTL2 is shown in [Table 7-595](#).Return to the [Summary Table](#).**Table 7-595. ABUFF1\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x1	Source of ABUFF data: 0x14= DS1 Port 0; Virtual Channel 0 0x15= DS1 Port 0; Virtual Channel 1 0x16= DS1 Port 0; Virtual Channel 2 0x17= DS1 Port 0; Virtual Channel 3 0x18= DS1 Port 1; Virtual Channel 0 0x19= DS1 Port 1; Virtual Channel 1 0x1A= DS1 Port 1; Virtual Channel 2 0x1B= DS1 Port 1; Virtual Channel 3

**7.6.2.9.40 ABUFF1\_CTL6 Register (Address = 0x8E) [Default = 0x00]**ABUFF1\_CTL6 is shown in [Table 7-596](#).Return to the [Summary Table](#).**Table 7-596. ABUFF1\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.41 ABUFF2\_CTL0 Register (Address = 0x90) [Default = 0x00]**ABUFF2\_CTL0 is shown in [Table 7-597](#).Return to the [Summary Table](#).**Table 7-597. ABUFF2\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved

**Table 7-597. ABUFF2\_CTL0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.42 ABUFF2\_CTL1 Register (Address = 0x91) [Default = 0x00]**ABUFF2\_CTL1 is shown in [Table 7-598](#).Return to the [Summary Table](#).**Table 7-598. ABUFF2\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DSI GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.43 ABUFF2\_CTL2 Register (Address = 0x92) [Default = 0x02]**ABUFF2\_CTL2 is shown in [Table 7-599](#).Return to the [Summary Table](#).**Table 7-599. ABUFF2\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x2	Source of ABUFF data: 0x14= DSI Port 0; Virtual Channel 0 0x15= DSI Port 0; Virtual Channel 1 0x16= DSI Port 0; Virtual Channel 2 0x17= DSI Port 0; Virtual Channel 3 0x18= DSI Port 1; Virtual Channel 0 0x19= DSI Port 1; Virtual Channel 1 0x1A= DSI Port 1; Virtual Channel 2 0x1B= DSI Port 1; Virtual Channel 3

**7.6.2.9.44 ABUFF2\_CTL6 Register (Address = 0x96) [Default = 0x00]**ABUFF2\_CTL6 is shown in [Table 7-600](#).Return to the [Summary Table](#).

**Table 7-600. ABUFF2\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.45 ABUFF3\_CTL0 Register (Address = 0x98) [Default = 0x00]**ABUFF3\_CTL0 is shown in [Table 7-601](#).Return to the [Summary Table](#).**Table 7-601. ABUFF3\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.46 ABUFF3\_CTL1 Register (Address = 0x99) [Default = 0x00]**ABUFF3\_CTL1 is shown in [Table 7-602](#).Return to the [Summary Table](#).**Table 7-602. ABUFF3\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DSI GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.47 ABUFF3\_CTL2 Register (Address = 0x9A) [Default = 0x03]**ABUFF3\_CTL2 is shown in [Table 7-603](#).Return to the [Summary Table](#).**Table 7-603. ABUFF3\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5

**Table 7-603. ABUFF3\_CTL2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4:0	SRC_TO_ABUFF_SEL	R/W	0x3	Source of ABUFF data: 0x14= DS1 Port 0; Virtual Channel 0 0x15= DS1 Port 0; Virtual Channel 1 0x16= DS1 Port 0; Virtual Channel 2 0x17= DS1 Port 0; Virtual Channel 3 0x18= DS1 Port 1; Virtual Channel 0 0x19= DS1 Port 1; Virtual Channel 1 0x1A= DS1 Port 1; Virtual Channel 2 0x1B= DS1 Port 1; Virtual Channel 3

**7.6.2.9.48 ABUFF3\_CTL6 Register (Address = 0x9E) [Default = 0x00]**ABUFF3\_CTL6 is shown in [Table 7-604](#).Return to the [Summary Table](#).**Table 7-604. ABUFF3\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.49 ABUFF4\_CTL0 Register (Address = 0xA0) [Default = 0x00]**ABUFF4\_CTL0 is shown in [Table 7-605](#).Return to the [Summary Table](#).**Table 7-605. ABUFF4\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.50 ABUFF4\_CTL1 Register (Address = 0xA1) [Default = 0x00]**ABUFF4\_CTL1 is shown in [Table 7-606](#).Return to the [Summary Table](#).**Table 7-606. ABUFF4\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

**Table 7-606. ABUFF4\_CTL1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DS1 GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.51 ABUFF4\_CTL2 Register (Address = 0xA2) [Default = 0x04]**ABUFF4\_CTL2 is shown in [Table 7-607](#).Return to the [Summary Table](#).**Table 7-607. ABUFF4\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x4	Source of ABUFF data: 0x14= DS1 Port 0; Virtual Channel 0 0x15= DS1 Port 0; Virtual Channel 1 0x16= DS1 Port 0; Virtual Channel 2 0x17= DS1 Port 0; Virtual Channel 3 0x18= DS1 Port 1; Virtual Channel 0 0x19= DS1 Port 1; Virtual Channel 1 0x1A= DS1 Port 1; Virtual Channel 2 0x1B= DS1 Port 1; Virtual Channel 3

**7.6.2.9.52 ABUFF4\_CTL6 Register (Address = 0xA6) [Default = 0x00]**ABUFF4\_CTL6 is shown in [Table 7-608](#).Return to the [Summary Table](#).**Table 7-608. ABUFF4\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.53 ABUFF5\_CTL0 Register (Address = 0xA8) [Default = 0x00]**ABUFF5\_CTL0 is shown in [Table 7-609](#).Return to the [Summary Table](#).**Table 7-609. ABUFF5\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved

**Table 7-609. ABUFF5\_CTL0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.54 ABUFF5\_CTL1 Register (Address = 0xA9) [Default = 0x00]**ABUFF5\_CTL1 is shown in [Table 7-610](#).Return to the [Summary Table](#).**Table 7-610. ABUFF5\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DSI GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.55 ABUFF5\_CTL2 Register (Address = 0xAA) [Default = 0x05]**ABUFF5\_CTL2 is shown in [Table 7-611](#).Return to the [Summary Table](#).**Table 7-611. ABUFF5\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x5	Source of ABUFF data: 0x14= DSI Port 0; Virtual Channel 0 0x15= DSI Port 0; Virtual Channel 1 0x16= DSI Port 0; Virtual Channel 2 0x17= DSI Port 0; Virtual Channel 3 0x18= DSI Port 1; Virtual Channel 0 0x19= DSI Port 1; Virtual Channel 1 0x1A= DSI Port 1; Virtual Channel 2 0x1B= DSI Port 1; Virtual Channel 3

**7.6.2.9.56 ABUFF5\_CTL6 Register (Address = 0xAE) [Default = 0x00]**ABUFF5\_CTL6 is shown in [Table 7-612](#).Return to the [Summary Table](#).

**Table 7-612. ABUFF5\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.57 ABUFF6\_CTL0 Register (Address = 0xB0) [Default = 0x00]**ABUFF6\_CTL0 is shown in [Table 7-613](#).Return to the [Summary Table](#).**Table 7-613. ABUFF6\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.58 ABUFF6\_CTL1 Register (Address = 0xB1) [Default = 0x00]**ABUFF6\_CTL1 is shown in [Table 7-614](#).Return to the [Summary Table](#).**Table 7-614. ABUFF6\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DSI GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.59 ABUFF6\_CTL2 Register (Address = 0xB2) [Default = 0x06]**ABUFF6\_CTL2 is shown in [Table 7-615](#).Return to the [Summary Table](#).**Table 7-615. ABUFF6\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5

**Table 7-615. ABUFF6\_CTL2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4:0	SRC_TO_ABUFF_SEL	R/W	0x6	Source of ABUFF data: 0x14= DS1 Port 0; Virtual Channel 0 0x15= DS1 Port 0; Virtual Channel 1 0x16= DS1 Port 0; Virtual Channel 2 0x17= DS1 Port 0; Virtual Channel 3 0x18= DS1 Port 1; Virtual Channel 0 0x19= DS1 Port 1; Virtual Channel 1 0x1A= DS1 Port 1; Virtual Channel 2 0x1B= DS1 Port 1; Virtual Channel 3

**7.6.2.9.60 ABUFF6\_CTL6 Register (Address = 0xB6) [Default = 0x00]**ABUFF6\_CTL6 is shown in [Table 7-616](#).Return to the [Summary Table](#).**Table 7-616. ABUFF6\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.61 ABUFF7\_CTL0 Register (Address = 0xB8) [Default = 0x00]**ABUFF7\_CTL0 is shown in [Table 7-617](#).Return to the [Summary Table](#).**Table 7-617. ABUFF7\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.62 ABUFF7\_CTL1 Register (Address = 0xB9) [Default = 0x00]**ABUFF7\_CTL1 is shown in [Table 7-618](#).Return to the [Summary Table](#).**Table 7-618. ABUFF7\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

**Table 7-618. ABUFF7\_CTL1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DS1 GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.63 ABUFF7\_CTL2 Register (Address = 0xBA) [Default = 0x07]**ABUFF7\_CTL2 is shown in [Table 7-619](#).Return to the [Summary Table](#).**Table 7-619. ABUFF7\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x7	Source of ABUFF data: 0x14= DS1 Port 0; Virtual Channel 0 0x15= DS1 Port 0; Virtual Channel 1 0x16= DS1 Port 0; Virtual Channel 2 0x17= DS1 Port 0; Virtual Channel 3 0x18= DS1 Port 1; Virtual Channel 0 0x19= DS1 Port 1; Virtual Channel 1 0x1A= DS1 Port 1; Virtual Channel 2 0x1B= DS1 Port 1; Virtual Channel 3

**7.6.2.9.64 ABUFF7\_CTL6 Register (Address = 0xBE) [Default = 0x00]**ABUFF7\_CTL6 is shown in [Table 7-620](#).Return to the [Summary Table](#).**Table 7-620. ABUFF7\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.65 ABUFF8\_CTL0 Register (Address = 0xC0) [Default = 0x00]**ABUFF8\_CTL0 is shown in [Table 7-621](#).Return to the [Summary Table](#).**Table 7-621. ABUFF8\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved

**Table 7-621. ABUFF8\_CTL0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.66 ABUFF8\_CTL1 Register (Address = 0xC1) [Default = 0x00]**ABUFF8\_CTL1 is shown in [Table 7-622](#).Return to the [Summary Table](#).**Table 7-622. ABUFF8\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DSI GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.67 ABUFF8\_CTL2 Register (Address = 0xC2) [Default = 0x08]**ABUFF8\_CTL2 is shown in [Table 7-623](#).Return to the [Summary Table](#).**Table 7-623. ABUFF8\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0x8	Source of ABUFF data: 0x14= DSI Port 0; Virtual Channel 0 0x15= DSI Port 0; Virtual Channel 1 0x16= DSI Port 0; Virtual Channel 2 0x17= DSI Port 0; Virtual Channel 3 0x18= DSI Port 1; Virtual Channel 0 0x19= DSI Port 1; Virtual Channel 1 0x1A= DSI Port 1; Virtual Channel 2 0x1B= DSI Port 1; Virtual Channel 3

**7.6.2.9.68 ABUFF8\_CTL6 Register (Address = 0xC6) [Default = 0x00]**ABUFF8\_CTL6 is shown in [Table 7-624](#).Return to the [Summary Table](#).

**Table 7-624. ABUFF8\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.69 ABUFF9\_CTL0 Register (Address = 0xC8) [Default = 0x00]**ABUFF9\_CTL0 is shown in [Table 7-625](#).Return to the [Summary Table](#).**Table 7-625. ABUFF9\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.70 ABUFF9\_CTL1 Register (Address = 0xC9) [Default = 0x00]**ABUFF9\_CTL1 is shown in [Table 7-626](#).Return to the [Summary Table](#).**Table 7-626. ABUFF9\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DSI GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.71 ABUFF9\_CTL2 Register (Address = 0xCA) [Default = 0x09]**ABUFF9\_CTL2 is shown in [Table 7-627](#).Return to the [Summary Table](#).**Table 7-627. ABUFF9\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5

**Table 7-627. ABUFF9\_CTL2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4:0	SRC_TO_ABUFF_SEL	R/W	0x9	Source of ABUFF data: 0x14= DS1 Port 0; Virtual Channel 0 0x15= DS1 Port 0; Virtual Channel 1 0x16= DS1 Port 0; Virtual Channel 2 0x17= DS1 Port 0; Virtual Channel 3 0x18= DS1 Port 1; Virtual Channel 0 0x19= DS1 Port 1; Virtual Channel 1 0x1A= DS1 Port 1; Virtual Channel 2 0x1B= DS1 Port 1; Virtual Channel 3

**7.6.2.9.72 ABUFF9\_CTL6 Register (Address = 0xCE) [Default = 0x00]**ABUFF9\_CTL6 is shown in [Table 7-628](#).Return to the [Summary Table](#).**Table 7-628. ABUFF9\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.73 ABUFF10\_CTL0 Register (Address = 0xD0) [Default = 0x00]**ABUFF10\_CTL0 is shown in [Table 7-629](#).Return to the [Summary Table](#).**Table 7-629. ABUFF10\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.74 ABUFF10\_CTL1 Register (Address = 0xD1) [Default = 0x00]**ABUFF10\_CTL1 is shown in [Table 7-630](#).Return to the [Summary Table](#).**Table 7-630. ABUFF10\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

**Table 7-630. ABUFF10\_CTL1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DS1 GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.75 ABUFF10\_CTL2 Register (Address = 0xD2) [Default = 0x0A]**ABUFF10\_CTL2 is shown in [Table 7-631](#).Return to the [Summary Table](#).**Table 7-631. ABUFF10\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0xA	Source of ABUFF data: 0x14= DS1 Port 0; Virtual Channel 0 0x15= DS1 Port 0; Virtual Channel 1 0x16= DS1 Port 0; Virtual Channel 2 0x17= DS1 Port 0; Virtual Channel 3 0x18= DS1 Port 1; Virtual Channel 0 0x19= DS1 Port 1; Virtual Channel 1 0x1A= DS1 Port 1; Virtual Channel 2 0x1B= DS1 Port 1; Virtual Channel 3

**7.6.2.9.76 ABUFF10\_CTL6 Register (Address = 0xD6) [Default = 0x00]**ABUFF10\_CTL6 is shown in [Table 7-632](#).Return to the [Summary Table](#).**Table 7-632. ABUFF10\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

**7.6.2.9.77 ABUFF11\_CTL0 Register (Address = 0xD8) [Default = 0x00]**ABUFF11\_CTL0 is shown in [Table 7-633](#).Return to the [Summary Table](#).**Table 7-633. ABUFF11\_CTL0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved

**Table 7-633. ABUFF11\_CTL0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	0 Maps to Link Layer of Port 0, 1 Maps to Link Layer of Port 1
0	ABUFF_ENABLE	R/W	0x0	1 Activates the ABUFF block

**7.6.2.9.78 ABUFF11\_CTL1 Register (Address = 0xD9) [Default = 0x00]**ABUFF11\_CTL1 is shown in [Table 7-634](#).Return to the [Summary Table](#).**Table 7-634. ABUFF11\_CTL1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SDP_TYPE_IN	R/W	0x0	type of SDP: 0x0= audio 0x1= DSI GLW 0x2= Audio Info Frame 0x3= means Non Audio Info Frame 0x4= MISC 0x5= Reserved 0x6= Reserved 0x7= PASSTHROUGH Mode

**7.6.2.9.79 ABUFF11\_CTL2 Register (Address = 0xDA) [Default = 0x0B]**ABUFF11\_CTL2 is shown in [Table 7-635](#).Return to the [Summary Table](#).**Table 7-635. ABUFF11\_CTL2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	Select the Stream to map the ABUFF to 0x0= Stream 0 0x1= Stream 1 0x2= Stream 2 0x3= Stream 3 0x4= Stream 4 0x5= Stream 5
4:0	SRC_TO_ABUFF_SEL	R/W	0xB	Source of ABUFF data: 0x14= DSI Port 0; Virtual Channel 0 0x15= DSI Port 0; Virtual Channel 1 0x16= DSI Port 0; Virtual Channel 2 0x17= DSI Port 0; Virtual Channel 3 0x18= DSI Port 1; Virtual Channel 0 0x19= DSI Port 1; Virtual Channel 1 0x1A= DSI Port 1; Virtual Channel 2 0x1B= DSI Port 1; Virtual Channel 3

**7.6.2.9.80 ABUFF11\_CTL6 Register (Address = 0xDE) [Default = 0x00]**ABUFF11\_CTL6 is shown in [Table 7-636](#).Return to the [Summary Table](#).

**Table 7-636. ABUFF11\_CTL6 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	1 indicates ABUFF FIFO Overflow
0	STS_FIFO_PKT_DROPPED	RC	0x0	1 indicates ABUFF packets were dropped (because of offset correction feature)

### 7.6.2.10 Page\_12\_Video\_Processor Registers

Table 7-637 lists the memory-mapped registers for the Page\_12\_Video\_Processor registers. All register offset addresses not listed in Table 7-637 should be considered as reserved locations and the register contents should not be modified.

**Table 7-637. PAGE\_12\_VIDEO\_PROCESSOR Registers**

Address	Acronym	Register Name	Section
0x0	VID_PROC_CTL_VP0	VID_PROC_CTL_VP0	Go
0x1	VID_PROC_CFG_VP0	VID_PROC_CFG_VP0	Go
0x2	H_ACTIVE0_SHADOW_VP0	H_ACTIVE0_SHADOW_VP0	Go
0x3	H_ACTIVE1_SHADOW_VP0	H_ACTIVE1_SHADOW_VP0	Go
0x4	V_ACTIVE0_SHADOW_VP0	V_ACTIVE0_SHADOW_VP0	Go
0x5	V_ACTIVE1_SHADOW_VP0	V_ACTIVE1_SHADOW_VP0	Go
0x6	VFILTER_A_VP0	VFILTER_A_VP0	Go
0x7	VFILTER_N_VP0	VFILTER_N_VP0	Go
0x8	CROP_START_X0_VP0	CROP_START_X0_VP0	Go
0x9	CROP_START_X1_VP0	CROP_START_X1_VP0	Go
0xA	CROP_START_Y0_VP0	CROP_START_Y0_VP0	Go
0xB	CROP_START_Y1_VP0	CROP_START_Y1_VP0	Go
0xC	CROP_STOP_X0_VP0	CROP_STOP_X0_VP0	Go
0xD	CROP_STOP_X1_VP0	CROP_STOP_X1_VP0	Go
0xE	CROP_STOP_Y0_VP0	CROP_STOP_Y0_VP0	Go
0xF	CROP_STOP_Y1_VP0	CROP_STOP_Y1_VP0	Go
0x10	VID_H_ACTIVE0_VP0	VID_H_ACTIVE0_VP0	Go
0x11	VID_H_ACTIVE1_VP0	VID_H_ACTIVE1_VP0	Go
0x12	VID_H_BACK0_VP0	VID_H_BACK0_VP0	Go
0x13	VID_H_BACK1_VP0	VID_H_BACK1_VP0	Go
0x14	VID_H_WIDTH0_VP0	VID_H_WIDTH0_VP0	Go
0x15	VID_H_WIDTH1_VP0	VID_H_WIDTH1_VP0	Go
0x16	VID_H_TOTAL0_VP0	VID_H_TOTAL0_VP0	Go
0x17	VID_H_TOTAL1_VP0	VID_H_TOTAL1_VP0	Go
0x18	VID_V_ACTIVE0_VP0	VID_V_ACTIVE0_VP0	Go
0x19	VID_V_ACTIVE1_VP0	VID_V_ACTIVE1_VP0	Go
0x1A	VID_V_BACK0_VP0	VID_V_BACK0_VP0	Go
0x1B	VID_V_BACK1_VP0	VID_V_BACK1_VP0	Go
0x1C	VID_V_WIDTH0_VP0	VID_V_WIDTH0_VP0	Go
0x1D	VID_V_WIDTH1_VP0	VID_V_WIDTH1_VP0	Go
0x1E	VID_V_FRONT0_VP0	VID_V_FRONT0_VP0	Go
0x1F	VID_V_FRONT1_VP0	VID_V_FRONT1_VP0	Go
0x20	GEN_LATE_THRESH_VP0	GEN_LATE_THRESH_VP0	Go
0x21	GEN_EARLY_THRESH_VP0	GEN_EARLY_THRESH_VP0	Go
0x22	GEN_START_DELAY_VP0	GEN_START_DELAY_VP0	Go
0x23	PCLK_GEN_M_0_VP0	PCLK_GEN_M_0_VP0	Go
0x24	PCLK_GEN_M_1_VP0	PCLK_GEN_M_1_VP0	Go
0x25	PCLK_GEN_N_VP0	PCLK_GEN_N_VP0	Go
0x26	MAX_M_ADJUST_VP0	MAX_M_ADJUST_VP0	Go
0x27	VID_PROC_CFG2_VP0	VID_PROC_CFG2_VP0	Go
0x28	FPD4_PGCTL_VP0	FPD4_PGCTL_VP0	Go

**Table 7-637. PAGE\_12\_VIDEO\_PROCESSOR Registers (continued)**

Address	Acronym	Register Name	Section
0x29	FPD4_PGCFG_VP0	FPD4_PGCFG_VP0	Go
0x2A	FPD4_PGIA_VP0	FPD4_PGIA_VP0	Go
0x2B	FPD4_PGID_VP0	FPD4_PGID_VP0	Go
0x2C	FPD4_PGDBG_VP0	FPD4_PGDBG_VP0	Go
0x2D	FPD4_PGTSTDAT_VP0	FPD4_PGTSTDAT_VP0	Go
0x30	VP_STS_VP0	VP_STS_VP0	Go
0x31	INTR_STS_VP_VP0	INTR_STS_VP_VP0	Go
0x33	INTR_CTL_VP_VP0	INTR_CTL_VP_VP0	Go
0x35	MEAS_H_TOTAL0_VP0	MEAS_H_TOTAL0_VP0	Go
0x36	MEAS_H_TOTAL1_VP0	MEAS_H_TOTAL1_VP0	Go
0x40	VID_PROC_CTL_VP1	VID_PROC_CTL_VP1	Go
0x41	VID_PROC_CFG_VP1	VID_PROC_CFG_VP1	Go
0x42	H_ACTIVE0_SHADOW_VP1	H_ACTIVE0_SHADOW_VP1	Go
0x43	H_ACTIVE1_SHADOW_VP1	H_ACTIVE1_SHADOW_VP1	Go
0x44	V_ACTIVE0_SHADOW_VP1	V_ACTIVE0_SHADOW_VP1	Go
0x45	V_ACTIVE1_SHADOW_VP1	V_ACTIVE1_SHADOW_VP1	Go
0x46	VFILTER_A_VP1	VFILTER_A_VP1	Go
0x47	VFILTER_N_VP1	VFILTER_N_VP1	Go
0x48	CROP_START_X0_VP1	CROP_START_X0_VP1	Go
0x49	CROP_START_X1_VP1	CROP_START_X1_VP1	Go
0x4A	CROP_START_Y0_VP1	CROP_START_Y0_VP1	Go
0x4B	CROP_START_Y1_VP1	CROP_START_Y1_VP1	Go
0x4C	CROP_STOP_X0_VP1	CROP_STOP_X0_VP1	Go
0x4D	CROP_STOP_X1_VP1	CROP_STOP_X1_VP1	Go
0x4E	CROP_STOP_Y0_VP1	CROP_STOP_Y0_VP1	Go
0x4F	CROP_STOP_Y1_VP1	CROP_STOP_Y1_VP1	Go
0x50	VID_H_ACTIVE0_VP1	VID_H_ACTIVE0_VP1	Go
0x51	VID_H_ACTIVE1_VP1	VID_H_ACTIVE1_VP1	Go
0x52	VID_H_BACK0_VP1	VID_H_BACK0_VP1	Go
0x53	VID_H_BACK1_VP1	VID_H_BACK1_VP1	Go
0x54	VID_H_WIDTH0_VP1	VID_H_WIDTH0_VP1	Go
0x55	VID_H_WIDTH1_VP1	VID_H_WIDTH1_VP1	Go
0x56	VID_H_TOTAL0_VP1	VID_H_TOTAL0_VP1	Go
0x57	VID_H_TOTAL1_VP1	VID_H_TOTAL1_VP1	Go
0x58	VID_V_ACTIVE0_VP1	VID_V_ACTIVE0_VP1	Go
0x59	VID_V_ACTIVE1_VP1	VID_V_ACTIVE1_VP1	Go
0x5A	VID_V_BACK0_VP1	VID_V_BACK0_VP1	Go
0x5B	VID_V_BACK1_VP1	VID_V_BACK1_VP1	Go
0x5C	VID_V_WIDTH0_VP1	VID_V_WIDTH0_VP1	Go
0x5D	VID_V_WIDTH1_VP1	VID_V_WIDTH1_VP1	Go
0x5E	VID_V_FRONT0_VP1	VID_V_FRONT0_VP1	Go
0x5F	VID_V_FRONT1_VP1	VID_V_FRONT1_VP1	Go
0x60	GEN_LATE_THRESH_VP1	GEN_LATE_THRESH_VP1	Go
0x61	GEN_EARLY_THRESH_VP1	GEN_EARLY_THRESH_VP1	Go
0x62	GEN_START_DELAY_VP1	GEN_START_DELAY_VP1	Go

**Table 7-637. PAGE\_12\_VIDEO\_PROCESSOR Registers (continued)**

Address	Acronym	Register Name	Section
0x63	PCLK_GEN_M_0_VP1	PCLK_GEN_M_0_VP1	Go
0x64	PCLK_GEN_M_1_VP1	PCLK_GEN_M_1_VP1	Go
0x65	PCLK_GEN_N_VP1	PCLK_GEN_N_VP1	Go
0x66	MAX_M_ADJUST_VP1	MAX_M_ADJUST_VP1	Go
0x67	VID_PROC_CFG2_VP1	VID_PROC_CFG2_VP1	Go
0x68	FPD4_PGCTL_VP1	FPD4_PGCTL_VP1	Go
0x69	FPD4_PGCFG_VP1	FPD4_PGCFG_VP1	Go
0x6A	FPD4_PGIA_VP1	FPD4_PGIA_VP1	Go
0x6B	FPD4_Pgid_VP1	FPD4_Pgid_VP1	Go
0x6C	FPD4_PGDBG_VP1	FPD4_PGDBG_VP1	Go
0x6D	FPD4_PGTSTDAT_VP1	FPD4_PGTSTDAT_VP1	Go
0x70	VP_STS_VP1	VP_STS_VP1	Go
0x71	INTR_STS_VP_VP1	INTR_STS_VP_VP1	Go
0x73	INTR_CTL_VP_VP1	INTR_CTL_VP_VP1	Go
0x75	MEAS_H_TOTAL0_VP1	MEAS_H_TOTAL0_VP1	Go
0x76	MEAS_H_TOTAL1_VP1	MEAS_H_TOTAL1_VP1	Go
0x80	VID_PROC_CTL_VP2	VID_PROC_CTL_VP2	Go
0x81	VID_PROC_CFG_VP2	VID_PROC_CFG_VP2	Go
0x82	H_ACTIVE0_SHADOW_VP2	H_ACTIVE0_SHADOW_VP2	Go
0x83	H_ACTIVE1_SHADOW_VP2	H_ACTIVE1_SHADOW_VP2	Go
0x84	V_ACTIVE0_SHADOW_VP2	V_ACTIVE0_SHADOW_VP2	Go
0x85	V_ACTIVE1_SHADOW_VP2	V_ACTIVE1_SHADOW_VP2	Go
0x86	VFILTER_A_VP2	VFILTER_A_VP2	Go
0x87	VFILTER_N_VP2	VFILTER_N_VP2	Go
0x88	CROP_START_X0_VP2	CROP_START_X0_VP2	Go
0x89	CROP_START_X1_VP2	CROP_START_X1_VP2	Go
0x8A	CROP_START_Y0_VP2	CROP_START_Y0_VP2	Go
0x8B	CROP_START_Y1_VP2	CROP_START_Y1_VP2	Go
0x8C	CROP_STOP_X0_VP2	CROP_STOP_X0_VP2	Go
0x8D	CROP_STOP_X1_VP2	CROP_STOP_X1_VP2	Go
0x8E	CROP_STOP_Y0_VP2	CROP_STOP_Y0_VP2	Go
0x8F	CROP_STOP_Y1_VP2	CROP_STOP_Y1_VP2	Go
0x90	VID_H_ACTIVE0_VP2	VID_H_ACTIVE0_VP2	Go
0x91	VID_H_ACTIVE1_VP2	VID_H_ACTIVE1_VP2	Go
0x92	VID_H_BACK0_VP2	VID_H_BACK0_VP2	Go
0x93	VID_H_BACK1_VP2	VID_H_BACK1_VP2	Go
0x94	VID_H_WIDTH0_VP2	VID_H_WIDTH0_VP2	Go
0x95	VID_H_WIDTH1_VP2	VID_H_WIDTH1_VP2	Go
0x96	VID_H_TOTAL0_VP2	VID_H_TOTAL0_VP2	Go
0x97	VID_H_TOTAL1_VP2	VID_H_TOTAL1_VP2	Go
0x98	VID_V_ACTIVE0_VP2	VID_V_ACTIVE0_VP2	Go
0x99	VID_V_ACTIVE1_VP2	VID_V_ACTIVE1_VP2	Go
0x9A	VID_V_BACK0_VP2	VID_V_BACK0_VP2	Go
0x9B	VID_V_BACK1_VP2	VID_V_BACK1_VP2	Go
0x9C	VID_V_WIDTH0_VP2	VID_V_WIDTH0_VP2	Go

**Table 7-637. PAGE\_12\_VIDEO\_PROCESSOR Registers (continued)**

Address	Acronym	Register Name	Section
0x9D	VID_V_WIDTH1_VP2	VID_V_WIDTH1_VP2	Go
0x9E	VID_V_FRONT0_VP2	VID_V_FRONT0_VP2	Go
0x9F	VID_V_FRONT1_VP2	VID_V_FRONT1_VP2	Go
0xA0	GEN_LATE_THRESH_VP2	GEN_LATE_THRESH_VP2	Go
0xA1	GEN_EARLY_THRESH_VP2	GEN_EARLY_THRESH_VP2	Go
0xA2	GEN_START_DELAY_VP2	GEN_START_DELAY_VP2	Go
0xA3	PCLK_GEN_M_0_VP2	PCLK_GEN_M_0_VP2	Go
0xA4	PCLK_GEN_M_1_VP2	PCLK_GEN_M_1_VP2	Go
0xA5	PCLK_GEN_N_VP2	PCLK_GEN_N_VP2	Go
0xA6	MAX_M_ADJUST_VP2	MAX_M_ADJUST_VP2	Go
0xA7	VID_PROC_CFG2_VP2	VID_PROC_CFG2_VP2	Go
0xA8	FPD4_PGCTL_VP2	FPD4_PGCTL_VP2	Go
0xA9	FPD4_PGCFG_VP2	FPD4_PGCFG_VP2	Go
0xAA	FPD4_PGIA_VP2	FPD4_PGIA_VP2	Go
0xAB	FPD4_PGID_VP2	FPD4_PGID_VP2	Go
0xAC	FPD4_PGDBG_VP2	FPD4_PGDBG_VP2	Go
0xAD	FPD4_PGTSTDAT_VP2	FPD4_PGTSTDAT_VP2	Go
0xB0	VP_STS_VP2	VP_STS_VP2	Go
0xB1	INTR_STS_VP_VP2	INTR_STS_VP_VP2	Go
0xB3	INTR_CTL_VP_VP2	INTR_CTL_VP_VP2	Go
0xB5	MEAS_H_TOTAL0_VP2	MEAS_H_TOTAL0_VP2	Go
0xB6	MEAS_H_TOTAL1_VP2	MEAS_H_TOTAL1_VP2	Go
0xC0	VID_PROC_CTL_VP3	VID_PROC_CTL_VP3	Go
0xC1	VID_PROC_CFG_VP3	VID_PROC_CFG_VP3	Go
0xC2	H_ACTIVE0_SHADOW_VP3	H_ACTIVE0_SHADOW_VP3	Go
0xC3	H_ACTIVE1_SHADOW_VP3	H_ACTIVE1_SHADOW_VP3	Go
0xC4	V_ACTIVE0_SHADOW_VP3	V_ACTIVE0_SHADOW_VP3	Go
0xC5	V_ACTIVE1_SHADOW_VP3	V_ACTIVE1_SHADOW_VP3	Go
0xC6	VFILTER_A_VP3	VFILTER_A_VP3	Go
0xC7	VFILTER_N_VP3	VFILTER_N_VP3	Go
0xC8	CROP_START_X0_VP3	CROP_START_X0_VP3	Go
0xC9	CROP_START_X1_VP3	CROP_START_X1_VP3	Go
0xCA	CROP_START_Y0_VP3	CROP_START_Y0_VP3	Go
0xCB	CROP_START_Y1_VP3	CROP_START_Y1_VP3	Go
0xCC	CROP_STOP_X0_VP3	CROP_STOP_X0_VP3	Go
0xCD	CROP_STOP_X1_VP3	CROP_STOP_X1_VP3	Go
0xCE	CROP_STOP_Y0_VP3	CROP_STOP_Y0_VP3	Go
0xCF	CROP_STOP_Y1_VP3	CROP_STOP_Y1_VP3	Go
0xD0	VID_H_ACTIVE0_VP3	VID_H_ACTIVE0_VP3	Go
0xD1	VID_H_ACTIVE1_VP3	VID_H_ACTIVE1_VP3	Go
0xD2	VID_H_BACK0_VP3	VID_H_BACK0_VP3	Go
0xD3	VID_H_BACK1_VP3	VID_H_BACK1_VP3	Go
0xD4	VID_H_WIDTH0_VP3	VID_H_WIDTH0_VP3	Go
0xD5	VID_H_WIDTH1_VP3	VID_H_WIDTH1_VP3	Go
0xD6	VID_H_TOTAL0_VP3	VID_H_TOTAL0_VP3	Go

**Table 7-637. PAGE\_12\_VIDEO\_PROCESSOR Registers (continued)**

Address	Acronym	Register Name	Section
0xD7	VID_H_TOTAL1_VP3	VID_H_TOTAL1_VP3	Go
0xD8	VID_V_ACTIVE0_VP3	VID_V_ACTIVE0_VP3	Go
0xD9	VID_V_ACTIVE1_VP3	VID_V_ACTIVE1_VP3	Go
0xDA	VID_V_BACK0_VP3	VID_V_BACK0_VP3	Go
0xDB	VID_V_BACK1_VP3	VID_V_BACK1_VP3	Go
0xDC	VID_V_WIDTH0_VP3	VID_V_WIDTH0_VP3	Go
0xDD	VID_V_WIDTH1_VP3	VID_V_WIDTH1_VP3	Go
0xDE	VID_V_FRONT0_VP3	VID_V_FRONT0_VP3	Go
0xDF	VID_V_FRONT1_VP3	VID_V_FRONT1_VP3	Go
0xE0	GEN_LATE_THRESH_VP3	GEN_LATE_THRESH_VP3	Go
0xE1	GEN_EARLY_THRESH_VP3	GEN_EARLY_THRESH_VP3	Go
0xE2	GEN_START_DELAY_VP3	GEN_START_DELAY_VP3	Go
0xE3	PCLK_GEN_M_0_VP3	PCLK_GEN_M_0_VP3	Go
0xE4	PCLK_GEN_M_1_VP3	PCLK_GEN_M_1_VP3	Go
0xE5	PCLK_GEN_N_VP3	PCLK_GEN_N_VP3	Go
0xE6	MAX_M_ADJUST_VP3	MAX_M_ADJUST_VP3	Go
0xE7	VID_PROC_CFG2_VP3	VID_PROC_CFG2_VP3	Go
0xE8	FPD4_PGCTL_VP3	FPD4_PGCTL_VP3	Go
0xE9	FPD4_PGCFG_VP3	FPD4_PGCFG_VP3	Go
0xEA	FPD4_PGIA_VP3	FPD4_PGIA_VP3	Go
0xEB	FPD4_Pgid_VP3	FPD4_Pgid_VP3	Go
0xEC	FPD4_PGDBG_VP3	FPD4_PGDBG_VP3	Go
0xED	FPD4_PGTSTDAT_VP3	FPD4_PGTSTDAT_VP3	Go
0xF0	VP_STS_VP3	VP_STS_VP3	Go
0xF1	INTR_STS_VP_VP3	INTR_STS_VP_VP3	Go
0xF3	INTR_CTL_VP_VP3	INTR_CTL_VP_VP3	Go
0xF5	MEAS_H_TOTAL0_VP3	MEAS_H_TOTAL0_VP3	Go
0xF6	MEAS_H_TOTAL1_VP3	MEAS_H_TOTAL1_VP3	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-638](#) shows the codes that are used for access types in this section.

**Table 7-638. Page\_12\_Video\_Processor Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
<b>Write Type</b>		
W	W	Write
W1S	W 1S	Write 1 to set
<b>Reset or Default Value</b>		

**Table 7-638. Page\_12\_Video\_Processor Access  
Type Codes (continued)**

Access Type	Code	Description
-n		Value after reset or the default value

#### 7.6.2.10.1 VID\_PROC\_CTL\_VP0 Register (Address = 0x0) [Default = 0x00]

VID\_PROC\_CTL\_VP0 is shown in [Table 7-639](#).

Return to the [Summary Table](#).

**Table 7-639. VID\_PROC\_CTL\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	VP_DUAL_MERGE_LR_EN	R/W	0x0	Enable Merge of Dual Images for Concatenated LR Output This bit enables merging of dual image, one from each Video Processor into a single image with concatenated left right image. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The line from VP0 (VP2) is output first. This generated the left line followed by the right line assuming VP0(VP2) receives the left image and VP1(VP3) receives the right image.
3	VP_DUAL_MERGE_ALT_EN	R/W	0x0	Enable Merge of Dual Images for Alternate Pixel Output This bit enables merging of dual image, one from each Video Processor into a single image with alternating pixels. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The pixel from VP0 (VP2) is output first.
2	VP_EN_CROP	R/W	0x0	Enable Video Cropping This bit enables video cropping. Video cropping controls should be configured prior to setting this bit. In addition, video cropping controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
1	VP_EN_VFILT	R/W	0x0	Enable Vertical Filter processing This bit enables vertical line filter for multi-image processing. Vertical Filter controls should be configured prior to setting this bit. In addition, Vertical Filter controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
0	VP_ENABLE	R	0x0	Enable Video Processor This is a read-only copy of the Video Processor enable in the main register page VP_ENABLE_REG.

#### 7.6.2.10.2 VID\_PROC\_CFG\_VP0 Register (Address = 0x1) [Default = 0xA8]

VID\_PROC\_CFG\_VP0 is shown in [Table 7-640](#).

Return to the [Summary Table](#).

**Table 7-640. VID\_PROC\_CFG\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESYNC_1ST_LINE	R/W	0x1	Video Processor Re-sync first Line When this bit is set, the video processor will wait for the full GEN_START_DELAY before sending the first line of active video. When this bit is set to a 0, the video processor will send the first active line as soon as it is available following expiration of the horizontal blanking timer. A setting of 0 allows reduced stretching of horizontal blanking if the video generator clock is faster than incoming data, but may be less tolerant to large frequency difference between the clocks.

**Table 7-640. VID\_PROC\_CFG\_VP0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	IGNORE_LINE_NUM	R/W	0x0	Video Processor Timing Generator Ignore Line Number This register bit controls allows the video timing generator to ignore the line number for starting active video and detecting error conditions. 1= Ignore Line Number 0= Require proper line number for starting active video
5	VP_WAIT4LINE	R/W	0x1	Video Processor wait for Video Line This register bit controls how the timing generator handles a condition where first video line is not available at the end of the Vertical Back Porch Timing 1: Wait for first video line, adding delay in the horizontal back porch period 0: Generate extra vertical lines of blanking while waiting This register is for debug purpose only
4:3	VP_DROP_FRAMES	R/W	0x1	Video Process Drop Frames control Controls the number of video frames to drop at start of video reception. By default, the first frame (typically a partial frame) will be dropped.
2	VP_GEN_CORRECT_LATE	R/W	0x0	Enable Horizontal Front Porch correction for late condition in video timing generation
1:0	VP_SRC_SELECT	R/W	0x0	Video Processor Source Select Selects between 4 input video streams Default setting of this register will match the port number for the video processor.

**7.6.2.10.3 H\_ACTIVE0\_SHADOW\_VP0 Register (Address = 0x2) [Default = 0x00]**H\_ACTIVE0\_SHADOW\_VP0 is shown in [Table 7-641](#).Return to the [Summary Table](#).**Table 7-641. H\_ACTIVE0\_SHADOW\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	H_ACTIVE_SHADOW_7_0	R/W	0x0	Horizontal Active period This value should be programmed to match the VID_H_ACTIVE parameter in pixels

**7.6.2.10.4 H\_ACTIVE1\_SHADOW\_VP0 Register (Address = 0x3) [Default = 0x00]**H\_ACTIVE1\_SHADOW\_VP0 is shown in [Table 7-642](#).Return to the [Summary Table](#).**Table 7-642. H\_ACTIVE1\_SHADOW\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	H_ACTIVE_SHADOW_15_8	R/W	0x0	Horizontal Active period This value should be programmed to match the VID_H_ACTIVE parameter in pixels

**7.6.2.10.5 V\_ACTIVE0\_SHADOW\_VP0 Register (Address = 0x4) [Default = 0x00]**V\_ACTIVE0\_SHADOW\_VP0 is shown in [Table 7-643](#).Return to the [Summary Table](#).

**Table 7-643. V\_ACTIVE0\_SHADOW\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	V_ACTIVE_SHADOW_7_0	R/W	0x0	Vertical Active period This value should be programmed to match the VID_V_ACTIVE parameter in pixels

**7.6.2.10.6 V\_ACTIVE1\_SHADOW\_VP0 Register (Address = 0x5) [Default = 0x00]**V\_ACTIVE1\_SHADOW\_VP0 is shown in [Table 7-644](#).Return to the [Summary Table](#).**Table 7-644. V\_ACTIVE1\_SHADOW\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	V_ACTIVE_SHADOW_15_8	R/W	0x0	Vertical Active period This value should be programmed to match the VID_V_ACTIVE parameter in pixels

**7.6.2.10.7 VFILTER\_A\_VP0 Register (Address = 0x6) [Default = 0x01]**VFILTER\_A\_VP0 is shown in [Table 7-645](#).Return to the [Summary Table](#).**Table 7-645. VFILTER\_A\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	VFILTER_ALT_LINE	R/W	0x0	Select for alternate line images. This bit applies for the special case when the VFILTER_A= 1 and VFILTER_N=2 0- extract lines (0, 2, 4 ...) 1- extract lines (1, 3, 5 ...)
6	RESERVED	R	0x0	Reserved
5:0	VFILTER_A	R/W	0x1	Vertical Filter A parameter Controls the number of lines (A) of each block of N lines that will be forwarded if Vertical Filter is enabled

**7.6.2.10.8 VFILTER\_N\_VP0 Register (Address = 0x7) [Default = 0x01]**VFILTER\_N\_VP0 is shown in [Table 7-646](#).Return to the [Summary Table](#).**Table 7-646. VFILTER\_N\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	VFILTER_N	R/W	0x1	Vertical Filter N parameter Controls the block size (N) for vertical filter operation.

**7.6.2.10.9 CROP\_START\_X0\_VP0 Register (Address = 0x8) [Default = 0x00]**CROP\_START\_X0\_VP0 is shown in [Table 7-647](#).Return to the [Summary Table](#).

**Table 7-647. CROP\_START\_X0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_X[7:0]	R/W	0x0	Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.10 CROP\_START\_X1\_VP0 Register (Address = 0x9) [Default = 0x00]**CROP\_START\_X1\_VP0 is shown in [Table 7-648](#).Return to the [Summary Table](#).**Table 7-648. CROP\_START\_X1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_X[15:8]	R/W	0x0	Image Cropping Start X position (bits 15:8) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.11 CROP\_START\_Y0\_VP0 Register (Address = 0xA) [Default = 0x00]**CROP\_START\_Y0\_VP0 is shown in [Table 7-649](#).Return to the [Summary Table](#).

Video Processor Configuration Register 2

**Table 7-649. CROP\_START\_Y0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[7:0]	R/W	0x0	Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.12 CROP\_START\_Y1\_VP0 Register (Address = 0xB) [Default = 0x00]**CROP\_START\_Y1\_VP0 is shown in [Table 7-650](#).Return to the [Summary Table](#).**Table 7-650. CROP\_START\_Y1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[15:8]	R/W	0x0	Image Cropping Start Y position (bits 15:8) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.13 CROP\_STOP\_X0\_VP0 Register (Address = 0xC) [Default = 0x00]**

CROP\_STOP\_X0\_VP0 is shown in [Table 7-651](#).

Return to the [Summary Table](#).

**Table 7-651. CROP\_STOP\_X0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[7:0]	R/W	0x0	Image Cropping Stop X position (bits 7:0) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.14 CROP\_STOP\_X1\_VP0 Register (Address = 0xD) [Default = 0x00]**

CROP\_STOP\_X1\_VP0 is shown in [Table 7-652](#).

Return to the [Summary Table](#).

**Table 7-652. CROP\_STOP\_X1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[15:8]	R/W	0x0	Image Cropping Stop X position (bits 15:8) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.15 CROP\_STOP\_Y0\_VP0 Register (Address = 0xE) [Default = 0x00]**

CROP\_STOP\_Y0\_VP0 is shown in [Table 7-653](#).

Return to the [Summary Table](#).

**Table 7-653. CROP\_STOP\_Y0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[7:0]	R/W	0x0	Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.16 CROP\_STOP\_Y1\_VP0 Register (Address = 0xF) [Default = 0x00]**

CROP\_STOP\_Y1\_VP0 is shown in [Table 7-654](#).

Return to the [Summary Table](#).

**Table 7-654. CROP\_STOP\_Y1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[15:8]	R/W	0x0	Image Cropping Stop Y position (bits 15:8) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.17 VID\_H\_ACTIVE0\_VP0 Register (Address = 0x10) [Default = 0x00]**

VID\_H\_ACTIVE0\_VP0 is shown in [Table 7-655](#).

Return to the [Summary Table](#).

**Table 7-655. VID\_H\_ACTIVE0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

**7.6.2.10.18 VID\_H\_ACTIVE1\_VP0 Register (Address = 0x11) [Default = 0x00]**

VID\_H\_ACTIVE1\_VP0 is shown in [Table 7-656](#).

Return to the [Summary Table](#).

Video Processor Status Register

**Table 7-656. VID\_H\_ACTIVE1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

**7.6.2.10.19 VID\_H\_BACK0\_VP0 Register (Address = 0x12) [Default = 0x00]**

VID\_H\_BACK0\_VP0 is shown in [Table 7-657](#).

Return to the [Summary Table](#).

Video Interrupt Status Register

The bits in this register will be set on occurrence of the associated event. If the corresponding interrupt mask register is set, an Interrupt will be generated for the event. The interrupt status bits will be cleared on a read of this register.

**Table 7-657. VID\_H\_BACK0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[7:0]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

**7.6.2.10.20 VID\_H\_BACK1\_VP0 Register (Address = 0x13) [Default = 0x00]**

VID\_H\_BACK1\_VP0 is shown in [Table 7-658](#).

Return to the [Summary Table](#).

Video Interrupt Control Register

The bits in this register enable interrupts for the associated bits in the Interrupt Status register.

**Table 7-658. VID\_H\_BACK1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[15:8]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

**7.6.2.10.21 VID\_H\_WIDTH0\_VP0 Register (Address = 0x14) [Default = 0x00]**

VID\_H\_WIDTH0\_VP0 is shown in [Table 7-659](#).

Return to the [Summary Table](#).

Video Processor total horizontal period measure

**Table 7-659. VID\_H\_WIDTH0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[7:0]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

**7.6.2.10.22 VID\_H\_WIDTH1\_VP0 Register (Address = 0x15) [Default = 0x00]**

VID\_H\_WIDTH1\_VP0 is shown in [Table 7-660](#).

Return to the [Summary Table](#).

Video Processor total horizontal period measure

**Table 7-660. VID\_H\_WIDTH1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[15:8]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

**7.6.2.10.23 VID\_H\_TOTAL0\_VP0 Register (Address = 0x16) [Default = 0x00]**

VID\_H\_TOTAL0\_VP0 is shown in [Table 7-661](#).

Return to the [Summary Table](#).

ADC Moving Average Filter and Input Clock Frequency Divider Selection

**Table 7-661. VID\_H\_TOTAL0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[7:0]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead. *H total must be divisible by 4

**7.6.2.10.24 VID\_H\_TOTAL1\_VP0 Register (Address = 0x17) [Default = 0x00]**

VID\_H\_TOTAL1\_VP0 is shown in [Table 7-662](#).

Return to the [Summary Table](#).

**Table 7-662. VID\_H\_TOTAL1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[15:8]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead. *H total must be divisible by 4

**7.6.2.10.25 VID\_V\_ACTIVE0\_VP0 Register (Address = 0x18) [Default = 0x00]**

VID\_V\_ACTIVE0\_VP0 is shown in [Table 7-663](#).

Return to the [Summary Table](#).

**Table 7-663. VID\_V\_ACTIVE0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

**7.6.2.10.26 VID\_V\_ACTIVE1\_VP0 Register (Address = 0x19) [Default = 0x00]**

VID\_V\_ACTIVE1\_VP0 is shown in [Table 7-664](#).

Return to the [Summary Table](#).

**Table 7-664. VID\_V\_ACTIVE1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

**7.6.2.10.27 VID\_V\_BACK0\_VP0 Register (Address = 0x1A) [Default = 0x00]**

VID\_V\_BACK0\_VP0 is shown in [Table 7-665](#).

Return to the [Summary Table](#).

**Table 7-665. VID\_V\_BACK0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[7:0]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

**7.6.2.10.28 VID\_V\_BACK1\_VP0 Register (Address = 0x1B) [Default = 0x00]**

VID\_V\_BACK1\_VP0 is shown in [Table 7-666](#).

Return to the [Summary Table](#).

**Table 7-666. VID\_V\_BACK1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[15:8]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

**7.6.2.10.29 VID\_V\_WIDTH0\_VP0 Register (Address = 0x1C) [Default = 0x00]**

VID\_V\_WIDTH0\_VP0 is shown in [Table 7-667](#).

Return to the [Summary Table](#).

**Table 7-667. VID\_V\_WIDTH0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[7:0]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

**7.6.2.10.30 VID\_V\_WIDTH1\_VP0 Register (Address = 0x1D) [Default = 0x00]**VID\_V\_WIDTH1\_VP0 is shown in [Table 7-668](#).Return to the [Summary Table](#).**Table 7-668. VID\_V\_WIDTH1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[15:8]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

**7.6.2.10.31 VID\_V\_FRONT0\_VP0 Register (Address = 0x1E) [Default = 0x00]**VID\_V\_FRONT0\_VP0 is shown in [Table 7-669](#).Return to the [Summary Table](#).**Table 7-669. VID\_V\_FRONT0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[7:0]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

**7.6.2.10.32 VID\_V\_FRONT1\_VP0 Register (Address = 0x1F) [Default = 0x00]**VID\_V\_FRONT1\_VP0 is shown in [Table 7-670](#).Return to the [Summary Table](#).**Table 7-670. VID\_V\_FRONT1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[15:8]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

**7.6.2.10.33 GEN\_LATE\_THRESH\_VP0 Register (Address = 0x20) [Default = 0x00]**GEN\_LATE\_THRESH\_VP0 is shown in [Table 7-671](#).Return to the [Summary Table](#).**Table 7-671. GEN\_LATE\_THRESH\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LATE_THRESH	R/W	0x0	Video Timing Late Threshold This value controls the threshold for sending a late pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is late by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

**7.6.2.10.34 GEN\_EARLY\_THRESH\_VP0 Register (Address = 0x21) [Default = 0x00]**GEN\_EARLY\_THRESH\_VP0 is shown in [Table 7-672](#).Return to the [Summary Table](#).**Table 7-672. GEN\_EARLY\_THRESH\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EARLY_THRESH	R/W	0x0	Video Timing Early Threshold This value controls the threshold for sending an early pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is early by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

**7.6.2.10.35 GEN\_START\_DELAY\_VP0 Register (Address = 0x22) [Default = 0x10]**GEN\_START\_DELAY\_VP0 is shown in [Table 7-673](#).Return to the [Summary Table](#).**Table 7-673. GEN\_START\_DELAY\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	GEN_STRT_DLY[7:0]	R/W	0x10	Video Timing Start Delay Provides a delay from HSync pulse to regenerating horizontal image timing. Setting is in units of 16 pixel clocks.

**7.6.2.10.36 PCLK\_GEN\_M\_0\_VP0 Register (Address = 0x23) [Default = 0x00]**PCLK\_GEN\_M\_0\_VP0 is shown in [Table 7-674](#).Return to the [Summary Table](#).**Table 7-674. PCLK\_GEN\_M\_0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PCLK_GEN_M[7:0]	R/W	0x0	PCLK Generator M value (bits 7:0) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

**7.6.2.10.37 PCLK\_GEN\_M\_1\_VP0 Register (Address = 0x24) [Default = 0x10]**PCLK\_GEN\_M\_1\_VP0 is shown in [Table 7-675](#).Return to the [Summary Table](#).**Table 7-675. PCLK\_GEN\_M\_1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	PCLK_GEN_M[14:8]	R/W	0x10	PCLK Generator M value (bits 14:8) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

**7.6.2.10.38 PCLK\_GEN\_N\_VP0 Register (Address = 0x25) [Default = 0x0F]**PCLK\_GEN\_N\_VP0 is shown in [Table 7-676](#).

Return to the [Summary Table](#).

**Table 7-676. PCLK\_GEN\_N\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PCLK_GEN_N	R/W	0xF	PCLK Generator N value Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the control of the N value. Actual value is $2^{PCLK\_GEN\_M}$ . The default setting for this register chooses an N value of $2^{15}$ or 32,768.

**7.6.2.10.39 MAX\_M\_ADJUST\_VP0 Register (Address = 0x26) [Default = 0x08]**

MAX\_M\_ADJUST\_VP0 is shown in [Table 7-677](#).

Return to the [Summary Table](#).

**Table 7-677. MAX\_M\_ADJUST\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MAX_M_ADJUST	R/W	0x8	Pixel Clock Generator Max Adjustment Video Timing generation will attempt to match pixel clock generation to the incoming video stream. This register sets a limit on the maximum +/- adjustment to the PCLK_GEN_M value.

**7.6.2.10.40 VID\_PROC\_CFG2\_VP0 Register (Address = 0x27) [Default = 0x00]**

VID\_PROC\_CFG2\_VP0 is shown in [Table 7-678](#).

Return to the [Summary Table](#).

**Table 7-678. VID\_PROC\_CFG2\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DUAL_MERGE_ALT_DLY	R/W	0x0	Dual Merge Alt mode path delay control (measured in input pixel clocks) 00- no delay 01- one clock delay 10- two clock delay 11- three clock delay
4	CROP_ALT_PIX_RIGHT	R/W	0x0	Alternate pixel cropping right enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is selected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , right pixels selected
3	CROP_ALT_PIX_LEFT	R/W	0x0	Alternate pixel cropping left enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is selected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , left pixels selected
2	GEN_VS_POL	R/W	0x0	Vertical Sync Polarity: Controls polarity of the vertical sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated

**Table 7-678. VID\_PROC\_CFG2\_VP0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	GEN_HS_POL	R/W	0x0	Horizontal Sync Polarity: Controls polarity of the horizontal sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
0	VP_AUTO_DETECT	R/W	0x0	Video Processor Auto-detect timing Setting this bit to a 1 allows the video processor timing generator to auto-detect the Horizontal period. It will use the auto-detected value (MEAS_H_TOTAL registers) instead of the value in the VID_H_TOTAL registers.

**7.6.2.10.41 FPD4\_PGCTL\_VP0 Register (Address = 0x28) [Default = 0x08]**FPD4\_PGCTL\_VP0 is shown in [Table 7-679](#).Return to the [Summary Table](#).**Table 7-679. FPD4\_PGCTL\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: Checkerboard (White/Black) 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom/Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 1: Enable Pattern Generator asynchronous to video input 0: Enable Pattern Generator synchronous to video input

**Table 7-679. FPD4\_PGCTL\_VP0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	<p>When PATGEN_LEGACY_ENB= 0,          Pattern generator, pattern checker and          forwarding enable encoding:          00: Disable pattern generator and pattern checker          01: Enable pattern generator          10: Enable pattern checker, do not forward patterns on to the RX          datapath          11: Enable pattern checker, forward patterns on to the RX datapath          When PAT_ENC_EN= 2 'b10 or PAT_ENC_EN= 2 'b11, the local          pattern generator is still enabled internally for comparison with          incoming video stream          When PAT_ENC_EN= 2 'b11, the local pattern generator's patterns          are forwarded, not the incoming video stream          When PATGEN_LEGACY_ENB= 1,          PAT_ENC_EN[1]:          1: Enable pattern checker          0: Disable pattern checker          PAT_ENC_EN[0]:          1: Enable pattern generator          0: Disable pattern generator          Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]</p>

**7.6.2.10.42 FPD4\_PGCFG\_VP0 Register (Address = 0x29) [Default = 0x08]**FPD4\_PGCFG\_VP0 is shown in [Table 7-680](#).Return to the [Summary Table](#).**Table 7-680. FPD4\_PGCFG\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHK	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 11: Scale checkered patterns by 16 (each square is 16x16 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 00: Normal operation (each square is 1x1 pixel)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 10: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 11: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.

**Table 7-680. FPD4\_PGCFG\_VP0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

**7.6.2.10.43 FPD4\_PGIA\_VP0 Register (Address = 0x2A) [Default = 0x00]**FPD4\_PGIA\_VP0 is shown in [Table 7-681](#).Return to the [Summary Table](#).**Table 7-681. FPD4\_PGIA\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

**7.6.2.10.44 FPD4\_Pgid\_VP0 Register (Address = 0x2B) [Default = 0x00]**FPD4\_Pgid\_VP0 is shown in [Table 7-682](#).Return to the [Summary Table](#).**Table 7-682. FPD4\_Pgid\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

**7.6.2.10.45 FPD4\_PGDBG\_VP0 Register (Address = 0x2C) [Default = 0x00]**FPD4\_PGDBG\_VP0 is shown in [Table 7-683](#).Return to the [Summary Table](#).**Table 7-683. FPD4\_PGDBG\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	PATGEN_DBG_SEL	R/W	0x0	Test Mux Select: This field selects the signals to be brought out on the test output bus as well as read in the PGTSTDAT register. See the Debug Monitor section of the Pattern Generator DDS for details.
3	PATGEN_ERR_INJ	R/W	0x0	Error Injection Select: 0: Disable error injection 1: Enable error injection
2	PATGEN_RAND	R/W	0x0	Random Pattern Generation Select: 1: Output a pseudo-random pattern, overriding all other pattern selection. 0: Output a pattern as configured in Fixed or Auto-Scrolling Pattern Modes.

**Table 7-683. FPD4\_PGDDBG\_VP0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	PATGEN_DBG_FREERUN	R/W	0x0	Test Mux Freerun: Enables continuous output of test mux data. If set to 0, data will be sampled and held following setting of the PATGEN_DBG_SAMPLE register bit. Freerun operation is most useful for viewing on external pins. Sample/Hold is most useful for reading through the PGTSTDAT register.
0	PATGEN_DBG_SAMPLE	RH/W1S	0x0	Test Mux Sample/Hold: Enables sampling of the test mux data within its source clock domain. Guarantees valid data readback through the PGTSTDAT register. This bit is self-clearing.

**7.6.2.10.46 FPD4\_PGTSTDAT\_VP0 Register (Address = 0x2D) [Default = 0x00]**FPD4\_PGTSTDAT\_VP0 is shown in [Table 7-684](#).Return to the [Summary Table](#).**Table 7-684. FPD4\_PGTSTDAT\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGCE register.
6	RESERVED	R	0x0	Reserved
5:0	PATGEN_TST_DATA	R	0x0	Test Data: This field contains the Debug Monitor output. See the Debug Monitor section of the Pattern Generator DDS for details.

**7.6.2.10.47 VP\_STS\_VP0 Register (Address = 0x30) [Default = 0x00]**VP\_STS\_VP0 is shown in [Table 7-685](#).Return to the [Summary Table](#).**Table 7-685. VP\_STS\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved: Reads return 0, writes are ignored.
2	VP_INTERRUPT	R	0x0	Video Processor Interrupt Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP_STATUS_CHANGE	RC	0x0	Video Processor Status Changed This bit will be set if the Tming Generator status has changed. It is a read-only copy of the IS_VP_STATUS_CHANGE bit in the VP_ISR_0 register. It will be cleared when The VP_ISR_0 Register is read.
0	TIMING_GEN_STS	R	0x0	Timing Generator Status This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

**7.6.2.10.48 INTR\_STS\_VP\_VP0 Register (Address = 0x31) [Default = 0x00]**INTR\_STS\_VP\_VP0 is shown in [Table 7-686](#).Return to the [Summary Table](#).

**Table 7-686. INTR\_STS\_VP\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_CROP_VERT_ERR	RC	0x0	Video Crop Vertical error This error is reported if the Video Cropping module detects that the video frame is too short for proper cropping.
5	IS_CROP_HOR_ERR	RC	0x0	Video Crop Horizontal error This error is reported if the Video Cropping module detects that the video line is too short for proper cropping.
4	IS_TIMING_DATA_ERR	RC	0x0	Timing Gen Data Available error This error is reported if the timing generator detects a line length error or other error that results in no data available to send from the video buffer during active horizontal period.
3	IS_TIMING_LINE_ERR	RC	0x0	Timing Gen Line Number error This error is reported if the timing generator detects a mismatch with the incoming line number. This may occur on video buffer errors or if timing is not synchronized between incoming stream and timing generator. When this event occurs, video lines will be flushed from the video buffers.
2	IS_TIMING_STRT_ERR	RC	0x0	Timing Gen Active Start error At start of active video period, this error will be set if video data is not available
1	IS_VP_VBUF_ERR	RC	0x0	Video Buffer error This field Indicates the video buffer logic detected a buffer overflow error.
0	IS_VP_STATUS_CHANGE	RC	0x0	Video Processor Status Changed This bit will be set if Video Processor status has changed.

**7.6.2.10.49 INTR\_CTL\_VP\_VP0 Register (Address = 0x33) [Default = 0x00]**INTR\_CTL\_VP\_VP0 is shown in [Table 7-687](#).Return to the [Summary Table](#).**Table 7-687. INTR\_CTL\_VP\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_CROP_VERT_ERR	R/W	0x0	Enable Video Crop Vertical error interrupt
5	IE_CROP_HOR_ERR	R/W	0x0	Enable Video Crop Horizontal error interrupt
4	IE_TIMING_DATA_ERR	R/W	0x0	Enable Timing Gen Data Available error interrupt
3	IE_TIMING_LINE_ERR	R/W	0x0	Enable Timing Gen Line Number error interrupt
2	IE_TIMING_STRT_ERR	R/W	0x0	Enable Timing Gen Active Start error interrupt
1	IE_VP_VBUF_ERR	R/W	0x0	Enable Video Buffer error interrupt
0	IE_VP_STATUS_CHANGE	R/W	0x0	Enable Video Processor Status Changed

**7.6.2.10.50 MEAS\_H\_TOTAL0\_VP0 Register (Address = 0x35) [Default = 0x00]**MEAS\_H\_TOTAL0\_VP0 is shown in [Table 7-688](#).Return to the [Summary Table](#).

**Table 7-688. MEAS\_H\_TOTAL0\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[7:0]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

**7.6.2.10.51 MEAS\_H\_TOTAL1\_VP0 Register (Address = 0x36) [Default = 0x00]**MEAS\_H\_TOTAL1\_VP0 is shown in [Table 7-689](#).Return to the [Summary Table](#).**Table 7-689. MEAS\_H\_TOTAL1\_VP0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[15:8]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

**7.6.2.10.52 VID\_PROC\_CTL\_VP1 Register (Address = 0x40) [Default = 0x00]**VID\_PROC\_CTL\_VP1 is shown in [Table 7-690](#).Return to the [Summary Table](#).**Table 7-690. VID\_PROC\_CTL\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	VP_DUAL_MERGE_LR_EN	R/W	0x0	Enable Merge of Dual Images for Concatenated LR Output This bit enables merging of dual image, one from each Video Processor into a single image with concatenated left right image. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The line from VP0 (VP2) is output first. This generated the left line followed by the right line assuming VP0(VP2) receives the left image and VP1(VP3) receives the right image.
3	VP_DUAL_MERGE_ALT_EN	R/W	0x0	Enable Merge of Dual Images for Alternate Pixel Output This bit enables merging of dual image, one from each Video Processor into a single image with alternating pixels. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The pixel from VP0 (VP2) is output first.
2	VP_EN_CROP	R/W	0x0	Enable Video Cropping This bit enables video cropping. Video cropping controls should be configured prior to setting this bit. In addition, video cropping controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
1	VP_EN_VFILT	R/W	0x0	Enable Vertical Filter processing This bit enables vertical line filter for multi-image processing. Vertical Filter controls should be configured prior to setting this bit. In addition, Vertical Filter controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.

**Table 7-690. VID\_PROC\_CTL\_VP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	VP_ENABLE	R	0x0	Enable Video Processor This is a read-only copy of the Video Processor enable in the main register page VP_ENABLE_REG.

**7.6.2.10.53 VID\_PROC\_CFG\_VP1 Register (Address = 0x41) [Default = 0xA9]**VID\_PROC\_CFG\_VP1 is shown in [Table 7-691](#).Return to the [Summary Table](#).**Table 7-691. VID\_PROC\_CFG\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESYNC_1ST_LINE	R/W	0x1	Video Processor Re-sync first Line When this bit is set, the video processor will wait for the full GEN_START_DELAY before sending the first line of active video. When this bit is set to a 0, the video processor will send the first active line as soon as it is available following expiration of the horizontal blanking timer. A setting of 0 allows reduced stretching of horizontal blanking if the video generator clock is faster than incoming data, but may be less tolerant to large frequency difference between the clocks.
6	IGNORE_LINE_NUM	R/W	0x0	Video Processor Timing Generator Ignore Line Number This register bit controls allows the video timing generator to ignore the line number for starting active video and detecting error conditions. 1: Ignore Line Number 0: Require proper line number for starting active video
5	VP_WAIT4LINE	R/W	0x1	Video Processor wait for Video Line This register bit controls how the timing generator handles a condition where first video line is not available at the end of the Vertical Back Porch Timing 1: Wait for first video line, adding delay in the horizontal back porch period 0: Generate extra vertical lines of blanking while waiting This register is for debug purpose only
4:3	VP_DROP_FRAMES	R/W	0x1	Video Process Drop Frames control Controls the number of video frames to drop at start of video reception. By default, the first frame (typically a partial frame) will be dropped.
2	VP_GEN_CORRECT_LATE	R/W	0x0	Enable Horizontal Front Porch correction for late condition in video timing generation
1:0	VP_SRC_SELECT	R/W	0x1	Video Processor Source Select Selects between 4 input video streams Default setting of this register will match the port number for the video processor.

**7.6.2.10.54 H\_ACTIVE0\_SHADOW\_VP1 Register (Address = 0x42) [Default = 0x00]**H\_ACTIVE0\_SHADOW\_VP1 is shown in [Table 7-692](#).Return to the [Summary Table](#).**Table 7-692. H\_ACTIVE0\_SHADOW\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	H_ACTIVE_SHADOW_7_0	R/W	0x0	Horizontal Active period This value should be programmed to match the VID_H_ACTIVE parameter in pixels

**7.6.2.10.55 H\_ACTIVE1\_SHADOW\_VP1 Register (Address = 0x43) [Default = 0x00]**H\_ACTIVE1\_SHADOW\_VP1 is shown in [Table 7-693](#).Return to the [Summary Table](#).**Table 7-693. H\_ACTIVE1\_SHADOW\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	H_ACTIVE_SHADOW_15 _8	R/W	0x0	Horizontal Active period This value should be programmed to match the VID_H_ACTIVE parameter in pixels

**7.6.2.10.56 V\_ACTIVE0\_SHADOW\_VP1 Register (Address = 0x44) [Default = 0x00]**V\_ACTIVE0\_SHADOW\_VP1 is shown in [Table 7-694](#).Return to the [Summary Table](#).**Table 7-694. V\_ACTIVE0\_SHADOW\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	V_ACTIVE_SHADOW_7_0	R/W	0x0	Vertical Active period This value should be programmed to match the VID_V_ACTIVE parameter in pixels

**7.6.2.10.57 V\_ACTIVE1\_SHADOW\_VP1 Register (Address = 0x45) [Default = 0x00]**V\_ACTIVE1\_SHADOW\_VP1 is shown in [Table 7-695](#).Return to the [Summary Table](#).**Table 7-695. V\_ACTIVE1\_SHADOW\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	V_ACTIVE_SHADOW_15_8	R/W	0x0	Vertical Active period This value should be programmed to match the VID_V_ACTIVE parameter in pixels

**7.6.2.10.58 VFILTER\_A\_VP1 Register (Address = 0x46) [Default = 0x01]**VFILTER\_A\_VP1 is shown in [Table 7-696](#).Return to the [Summary Table](#).**Table 7-696. VFILTER\_A\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	VFILTER_ALT_LINE	R/W	0x0	Select for alternate line images. This bit applies for the special case when the VFILTER_A= 1 and VFILTER_N=2 0- extract lines (0, 2, 4 ...) 1- extract lines (1, 3, 5 ...)
6	RESERVED	R	0x0	Reserved
5:0	VFILTER_A	R/W	0x1	Vertical Filter A parameter Controls the number of lines (A) of each block of N lines that will be forwarded if Vertical Filter is enabled

**7.6.2.10.59 VFILTER\_N\_VP1 Register (Address = 0x47) [Default = 0x01]**VFILTER\_N\_VP1 is shown in [Table 7-697](#).Return to the [Summary Table](#).

**Table 7-697. VFILTER\_N\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	VFILTER_N	R/W	0x1	Vertical Filter N parameter Controls the block size (N) for vertical filter operation.

**7.6.2.10.60 CROP\_START\_X0\_VP1 Register (Address = 0x48) [Default = 0x00]**CROP\_START\_X0\_VP1 is shown in [Table 7-698](#).Return to the [Summary Table](#).**Table 7-698. CROP\_START\_X0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_X[7:0]	R/W	0x0	Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.61 CROP\_START\_X1\_VP1 Register (Address = 0x49) [Default = 0x00]**CROP\_START\_X1\_VP1 is shown in [Table 7-699](#).Return to the [Summary Table](#).**Table 7-699. CROP\_START\_X1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_X[15:8]	R/W	0x0	Image Cropping Start X position (bits 15:8) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.62 CROP\_START\_Y0\_VP1 Register (Address = 0x4A) [Default = 0x00]**CROP\_START\_Y0\_VP1 is shown in [Table 7-700](#).Return to the [Summary Table](#).**Table 7-700. CROP\_START\_Y0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[7:0]	R/W	0x0	Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.63 CROP\_START\_Y1\_VP1 Register (Address = 0x4B) [Default = 0x00]**CROP\_START\_Y1\_VP1 is shown in [Table 7-701](#).Return to the [Summary Table](#).

**Table 7-701. CROP\_START\_Y1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[15:8]	R/W	0x0	Image Cropping Start Y position (bits 15:8) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.64 CROP\_STOP\_X0\_VP1 Register (Address = 0x4C) [Default = 0x00]**CROP\_STOP\_X0\_VP1 is shown in [Table 7-702](#).Return to the [Summary Table](#).**Table 7-702. CROP\_STOP\_X0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[7:0]	R/W	0x0	Image Cropping Stop X position (bits 7:0) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.65 CROP\_STOP\_X1\_VP1 Register (Address = 0x4D) [Default = 0x00]**CROP\_STOP\_X1\_VP1 is shown in [Table 7-703](#).Return to the [Summary Table](#).**Table 7-703. CROP\_STOP\_X1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[15:8]	R/W	0x0	Image Cropping Stop X position (bits 15:8) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.66 CROP\_STOP\_Y0\_VP1 Register (Address = 0x4E) [Default = 0x00]**CROP\_STOP\_Y0\_VP1 is shown in [Table 7-704](#).Return to the [Summary Table](#).**Table 7-704. CROP\_STOP\_Y0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[7:0]	R/W	0x0	Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.67 CROP\_STOP\_Y1\_VP1 Register (Address = 0x4F) [Default = 0x00]**CROP\_STOP\_Y1\_VP1 is shown in [Table 7-705](#).

[Return to the Summary Table.](#)

Mask Interrupts for the following thresholds

**Table 7-705. CROP\_STOP\_Y1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[15:8]	R/W	0x0	Image Cropping Stop Y position (bits 15:8) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.68 VID\_H\_ACTIVE0\_VP1 Register (Address = 0x50) [Default = 0x00]**

VID\_H\_ACTIVE0\_VP1 is shown in [Table 7-706](#).

[Return to the Summary Table.](#)

**Table 7-706. VID\_H\_ACTIVE0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

**7.6.2.10.69 VID\_H\_ACTIVE1\_VP1 Register (Address = 0x51) [Default = 0x00]**

VID\_H\_ACTIVE1\_VP1 is shown in [Table 7-707](#).

[Return to the Summary Table.](#)

**Table 7-707. VID\_H\_ACTIVE1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

**7.6.2.10.70 VID\_H\_BACK0\_VP1 Register (Address = 0x52) [Default = 0x00]**

VID\_H\_BACK0\_VP1 is shown in [Table 7-708](#).

[Return to the Summary Table.](#)

**Table 7-708. VID\_H\_BACK0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[7:0]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

**7.6.2.10.71 VID\_H\_BACK1\_VP1 Register (Address = 0x53) [Default = 0x00]**

VID\_H\_BACK1\_VP1 is shown in [Table 7-709](#).

[Return to the Summary Table.](#)

**Table 7-709. VID\_H\_BACK1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[15:8]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

**7.6.2.10.72 VID\_H\_WIDTH0\_VP1 Register (Address = 0x54) [Default = 0x00]**VID\_H\_WIDTH0\_VP1 is shown in [Table 7-710](#).Return to the [Summary Table](#).**Table 7-710. VID\_H\_WIDTH0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[7:0]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

**7.6.2.10.73 VID\_H\_WIDTH1\_VP1 Register (Address = 0x55) [Default = 0x00]**VID\_H\_WIDTH1\_VP1 is shown in [Table 7-711](#).Return to the [Summary Table](#).**Table 7-711. VID\_H\_WIDTH1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[15:8]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

**7.6.2.10.74 VID\_H\_TOTAL0\_VP1 Register (Address = 0x56) [Default = 0x00]**VID\_H\_TOTAL0\_VP1 is shown in [Table 7-712](#).Return to the [Summary Table](#).

Mark Interrupts for following thresholds

**Table 7-712. VID\_H\_TOTAL0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[7:0]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead. *H total must be divisible by 4

**7.6.2.10.75 VID\_H\_TOTAL1\_VP1 Register (Address = 0x57) [Default = 0x00]**VID\_H\_TOTAL1\_VP1 is shown in [Table 7-713](#).Return to the [Summary Table](#).

**Table 7-713. VID\_H\_TOTAL1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[15:8]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead. *H total must be divisible by 4

**7.6.2.10.76 VID\_V\_ACTIVE0\_VP1 Register (Address = 0x58) [Default = 0x00]**VID\_V\_ACTIVE0\_VP1 is shown in [Table 7-714](#).Return to the [Summary Table](#).**Table 7-714. VID\_V\_ACTIVE0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

**7.6.2.10.77 VID\_V\_ACTIVE1\_VP1 Register (Address = 0x59) [Default = 0x00]**VID\_V\_ACTIVE1\_VP1 is shown in [Table 7-715](#).Return to the [Summary Table](#).**Table 7-715. VID\_V\_ACTIVE1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

**7.6.2.10.78 VID\_V\_BACK0\_VP1 Register (Address = 0x5A) [Default = 0x00]**VID\_V\_BACK0\_VP1 is shown in [Table 7-716](#).Return to the [Summary Table](#).**Table 7-716. VID\_V\_BACK0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[7:0]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

**7.6.2.10.79 VID\_V\_BACK1\_VP1 Register (Address = 0x5B) [Default = 0x00]**VID\_V\_BACK1\_VP1 is shown in [Table 7-717](#).Return to the [Summary Table](#).**Table 7-717. VID\_V\_BACK1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[15:8]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

**7.6.2.10.80 VID\_V\_WIDTH0\_VP1 Register (Address = 0x5C) [Default = 0x00]**

VID\_V\_WIDTH0\_VP1 is shown in [Table 7-718](#).

Return to the [Summary Table](#).

**Table 7-718. VID\_V\_WIDTH0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[7:0]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

**7.6.2.10.81 VID\_V\_WIDTH1\_VP1 Register (Address = 0x5D) [Default = 0x00]**

VID\_V\_WIDTH1\_VP1 is shown in [Table 7-719](#).

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**Table 7-719. VID\_V\_WIDTH1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[15:8]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

**7.6.2.10.82 VID\_V\_FRONT0\_VP1 Register (Address = 0x5E) [Default = 0x00]**

VID\_V\_FRONT0\_VP1 is shown in [Table 7-720](#).

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**Table 7-720. VID\_V\_FRONT0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[7:0]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

**7.6.2.10.83 VID\_V\_FRONT1\_VP1 Register (Address = 0x5F) [Default = 0x00]**

VID\_V\_FRONT1\_VP1 is shown in [Table 7-721](#).

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**Table 7-721. VID\_V\_FRONT1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[15:8]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

**7.6.2.10.84 GEN\_LATE\_THRESH\_VP1 Register (Address = 0x60) [Default = 0x00]**

GEN\_LATE\_THRESH\_VP1 is shown in [Table 7-722](#).

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**Table 7-722. GEN\_LATE\_THRESH\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LATE_THRESH	R/W	0x0	Video Timing Late Threshold This value controls the threshold for sending a late pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is late by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

**7.6.2.10.85 GEN\_EARLY\_THRESH\_VP1 Register (Address = 0x61) [Default = 0x00]**GEN\_EARLY\_THRESH\_VP1 is shown in [Table 7-723](#).Return to the [Summary Table](#).**Table 7-723. GEN\_EARLY\_THRESH\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EARLY_THRESH	R/W	0x0	Video Timing Early Threshold This value controls the threshold for sending an early pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is early by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

**7.6.2.10.86 GEN\_START\_DELAY\_VP1 Register (Address = 0x62) [Default = 0x10]**GEN\_START\_DELAY\_VP1 is shown in [Table 7-724](#).Return to the [Summary Table](#).**Table 7-724. GEN\_START\_DELAY\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	GEN_STRT_DLY[7:0]	R/W	0x10	Video Timing Start Delay Provides a delay from HSync pulse to regenerating horizontal image timing. Setting is in units of 16 pixel clocks.

**7.6.2.10.87 PCLK\_GEN\_M\_0\_VP1 Register (Address = 0x63) [Default = 0x00]**PCLK\_GEN\_M\_0\_VP1 is shown in [Table 7-725](#).Return to the [Summary Table](#).**Table 7-725. PCLK\_GEN\_M\_0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PCLK_GEN_M[7:0]	R/W	0x0	PCLK Generator M value (bits 7:0) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

**7.6.2.10.88 PCLK\_GEN\_M\_1\_VP1 Register (Address = 0x64) [Default = 0x10]**PCLK\_GEN\_M\_1\_VP1 is shown in [Table 7-726](#).Return to the [Summary Table](#).**Table 7-726. PCLK\_GEN\_M\_1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

**Table 7-726. PCLK\_GEN\_M\_1\_VP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6:0	PCLK_GEN_M[14:8]	R/W	0x10	PCLK Generator M value (bits 14:8) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

**7.6.2.10.89 PCLK\_GEN\_N\_VP1 Register (Address = 0x65) [Default = 0x0F]**PCLK\_GEN\_N\_VP1 is shown in [Table 7-727](#).Return to the [Summary Table](#).**Table 7-727. PCLK\_GEN\_N\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PCLK_GEN_N	R/W	0xF	PCLK Generator N value Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the control of the N value. Actual value is $2^{PCLK\_GEN\_M}$ . The default setting for this register chooses an N value of $2^{15}$ or 32,768.

**7.6.2.10.90 MAX\_M\_ADJUST\_VP1 Register (Address = 0x66) [Default = 0x08]**MAX\_M\_ADJUST\_VP1 is shown in [Table 7-728](#).Return to the [Summary Table](#).**Table 7-728. MAX\_M\_ADJUST\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MAX_M_ADJUST	R/W	0x8	Pixel Clock Generator Max Adjustment Video Timing generation will attempt to match pixel clock generation to the incoming video stream. This register sets a limit on the maximum +/- adjustment to the PCLK_GEN_M value.

**7.6.2.10.91 VID\_PROC\_CFG2\_VP1 Register (Address = 0x67) [Default = 0x00]**VID\_PROC\_CFG2\_VP1 is shown in [Table 7-729](#).Return to the [Summary Table](#).**Table 7-729. VID\_PROC\_CFG2\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DUAL_MERGE_ALT_DLY	R/W	0x0	Dual Merge Alt mode path delay control (measured in input pixel clocks) 00- no delay 01- one clock delay 10- two clock delay 11- three clock delay
4	CROP_ALT_PIX_RIGHT	R/W	0x0	Alternate pixel cropping right enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is selected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , right pixels selected

**Table 7-729. VID\_PROC\_CFG2\_VP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3	CROP_ALT_PIX_LEFT	R/W	0x0	Alternate pixel cropping left enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is selected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , left pixels selected
2	GEN_VS_POL	R/W	0x0	Vertical Sync Polarity: Controls polarity of the vertical sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
1	GEN_HS_POL	R/W	0x0	Horizontal Sync Polarity: Controls polarity of the horizontal sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
0	VP_AUTO_DETECT	R/W	0x0	Video Processor Auto-detect timing Setting this bit to a 1 allows the video processor timing generator to auto-detect the Horizontal period. It will use the auto-detected value (MEAS_H_TOTAL registers) instead of the value in the VID_H_TOTAL registers.

#### 7.6.2.10.92 FPD4\_PGCTL\_VP1 Register (Address = 0x68) [Default = 0x08]

FPD4\_PGCTL\_VP1 is shown in [Table 7-730](#).

Return to the [Summary Table](#).

**Table 7-730. FPD4\_PGCTL\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG.PATGEN_INV is set to 1. 00000: Checkerboard (White/Black) 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom/Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 1: Enable Pattern Generator asynchronous to video input 0: Enable Pattern Generator synchronous to video input

**Table 7-730. FPD4\_PGCTL\_VP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	<p>When PATGEN_LEGACY_ENB= 0,          Pattern generator, pattern checker and          forwarding enable encoding:          00: Disable pattern generator and pattern checker          01: Enable pattern generator          10: Enable pattern checker, do not forward patterns on to the RX          datapath          11: Enable pattern checker, forward patterns on to the RX datapath          When PAT_ENC_EN= 2 'b10 or PAT_ENC_EN= 2 'b11, the local          pattern generator is still enabled internally for comparison with          incoming video stream          When PAT_ENC_EN= 2 'b11, the local pattern generator's patterns          are forwarded, not the incoming video stream          When PATGEN_LEGACY_ENB= 1,          PAT_ENC_EN[1]:          1: Enable pattern checker          0: Disable pattern checker          PAT_ENC_EN[0]:          1: Enable pattern generator          0: Disable pattern generator          Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]</p>

**7.6.2.10.93 FPD4\_PGCFG\_VP1 Register (Address = 0x69) [Default = 0x08]**FPD4\_PGCFG\_VP1 is shown in [Table 7-731](#).Return to the [Summary Table](#).**Table 7-731. FPD4\_PGCFG\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHK	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 11: Scale checkered patterns by 16 (each square is 16x16 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 00: Normal operation (each square is 1x1 pixel)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 10: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 11: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.

**Table 7-731. FPD4\_PGCFG\_VP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

**7.6.2.10.94 FPD4\_PGIA\_VP1 Register (Address = 0x6A) [Default = 0x00]**FPD4\_PGIA\_VP1 is shown in [Table 7-732](#).Return to the [Summary Table](#).**Table 7-732. FPD4\_PGIA\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

**7.6.2.10.95 FPD4\_Pgid\_VP1 Register (Address = 0x6B) [Default = 0x00]**FPD4\_Pgid\_VP1 is shown in [Table 7-733](#).Return to the [Summary Table](#).**Table 7-733. FPD4\_Pgid\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

**7.6.2.10.96 FPD4\_PGDBG\_VP1 Register (Address = 0x6C) [Default = 0x00]**FPD4\_PGDBG\_VP1 is shown in [Table 7-734](#).Return to the [Summary Table](#).**Table 7-734. FPD4\_PGDBG\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	PATGEN_ERR_INJ	R/W	0x0	Error Injection Select: 0: Disable error injection 1: Enable error injection
2	PATGEN_RAND	R/W	0x0	Random Pattern Generation Select: 1: Output a pseudo-random pattern, overriding all other pattern selection. 0: Output a pattern as configured in Fixed or Auto-Scrolling Pattern Modes.
1	RESERVED	R/W	0x0	Reserved

**Table 7-734. FPD4\_PGDDBG\_VP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	RESERVED	RH/W1S	0x0	Reserved

**7.6.2.10.97 FPD4\_PGTSTDAT\_VP1 Register (Address = 0x6D) [Default = 0x00]**FPD4\_PGTSTDAT\_VP1 is shown in [Table 7-735](#).Return to the [Summary Table](#).**Table 7-735. FPD4\_PGTSTDAT\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGCE register.
6	RESERVED	R	0x0	Reserved
5:0	RESERVED	R	0x0	Reserved

**7.6.2.10.98 VP\_STS\_VP1 Register (Address = 0x70) [Default = 0x00]**VP\_STS\_VP1 is shown in [Table 7-736](#).Return to the [Summary Table](#).**Table 7-736. VP\_STS\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	VP_INTERRUPT	R	0x0	Video Processor Interrupt Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP_STATUS_CHANGE	RC	0x0	Video Processor Status Changed This bit will be set if the Tming Generator status has changed. It is a read-only copy of the IS_VP_STATUS_CHANGE bit in the VP_ISR_0 register. It will be cleared when The VP_ISR_0 Register is read.
0	TIMING_GEN_STS	R	0x0	Timing Generator Status This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

**7.6.2.10.99 INTR\_STS\_VP\_VP1 Register (Address = 0x71) [Default = 0x00]**INTR\_STS\_VP\_VP1 is shown in [Table 7-737](#).Return to the [Summary Table](#).**Table 7-737. INTR\_STS\_VP\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_CROP_VERT_ERR	RC	0x0	Video Crop Vertical error This error is reported if the Video Cropping module detects that the video frame is too short for proper cropping.
5	IS_CROP_HOR_ERR	RC	0x0	Video Crop Horizontal error This error is reported if the Video Cropping module detects that the video line is too short for proper cropping.

**Table 7-737. INTR\_STS\_VP\_VP1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	IS_TIMING_DATA_ERR	RC	0x0	Timing Gen Data Available error This error is reported if the timing generator detects a line length error or other error that results in no data available to send from the video buffer during active horizontal period.
3	IS_TIMING_LINE_ERR	RC	0x0	Timing Gen Line Number error This error is reported if the timing generator detects a mismatch with the incoming line number. This may occur on video buffer errors or if timing is not synchronized between incoming stream and timing generator. When this event occurs, video lines will be flushed from the video buffers.
2	IS_TIMING_STRT_ERR	RC	0x0	Timing Gen Active Start error At start of active video period, this error will be set if video data is not available
1	IS_VP_VBUF_ERR	RC	0x0	Video Buffer error This field Indicates the video buffer logic detected a buffer overflow error.
0	IS_VP_STATUS_CHANGE	RC	0x0	Video Processor Status Changed This bit will be set if Video Processor status has changed.

**7.6.2.10.100 INTR\_CTL\_VP\_VP1 Register (Address = 0x73) [Default = 0x00]**INTR\_CTL\_VP\_VP1 is shown in [Table 7-738](#).Return to the [Summary Table](#).**Table 7-738. INTR\_CTL\_VP\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_CROP_VERT_ERR	R/W	0x0	Enable Video Crop Vertical error interrupt
5	IE_CROP_HOR_ERR	R/W	0x0	Enable Video Crop Horizontal error interrupt
4	IE_TIMING_DATA_ERR	R/W	0x0	Enable Timing Gen Data Available error interrupt
3	IE_TIMING_LINE_ERR	R/W	0x0	Enable Timing Gen Line Number error interrupt
2	IE_TIMING_STRT_ERR	R/W	0x0	Enable Timing Gen Active Start error interrupt
1	IE_VP_VBUF_ERR	R/W	0x0	Enable Video Buffer error interrupt
0	IE_VP_STATUS_CHANGE	R/W	0x0	Enable Video Processor Status Changed

**7.6.2.10.101 MEAS\_H\_TOTAL0\_VP1 Register (Address = 0x75) [Default = 0x00]**MEAS\_H\_TOTAL0\_VP1 is shown in [Table 7-739](#).Return to the [Summary Table](#).**Table 7-739. MEAS\_H\_TOTAL0\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[7:0]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

**7.6.2.10.102 MEAS\_H\_TOTAL1\_VP1 Register (Address = 0x76) [Default = 0x00]**

MEAS\_H\_TOTAL1\_VP1 is shown in [Table 7-740](#).

Return to the [Summary Table](#).

**Table 7-740. MEAS\_H\_TOTAL1\_VP1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[15:8]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

**7.6.2.10.103 VID\_PROC\_CTL\_VP2 Register (Address = 0x80) [Default = 0x00]**

VID\_PROC\_CTL\_VP2 is shown in [Table 7-741](#).

Return to the [Summary Table](#).

**Table 7-741. VID\_PROC\_CTL\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	VP_DUAL_MERGE_LR_EN	R/W	0x0	Enable Merge of Dual Images for Concatenated LR Output This bit enables merging of dual image, one from each Video Processor into a single image with concatenated left right image. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The line from VP0 (VP2) is output first. This generated the left line followed by the right line assuming VP0(VP2) receives the left image and VP1(VP3) receives the right image.
3	VP_DUAL_MERGE_ALT_EN	R/W	0x0	Enable Merge of Dual Images for Alternate Pixel Output This bit enables merging of dual image, one from each Video Processor into a single image with alternating pixels. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The pixel from VP0 (VP2) is output first.
2	VP_EN_CROP	R/W	0x0	Enable Video Cropping This bit enables video cropping. Video cropping controls should be configured prior to setting this bit. In addition, video cropping controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
1	VP_EN_VFILT	R/W	0x0	Enable Vertical Filter processing This bit enables vertical line filter for multi-image processing. Vertical Filter controls should be configured prior to setting this bit. In addition, Vertical Filter controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
0	VP_ENABLE	R	0x0	Enable Video Processor This is a read-only copy of the Video Processor enable in the main register page VP_ENABLE_REG.

**7.6.2.10.104 VID\_PROC\_CFG\_VP2 Register (Address = 0x81) [Default = 0xAA]**

VID\_PROC\_CFG\_VP2 is shown in [Table 7-742](#).

Return to the [Summary Table](#).

**Table 7-742. VID\_PROC\_CFG\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESYNC_1ST_LINE	R/W	0x1	Video Processor Re-sync first Line When this bit is set, the video processor will wait for the full GEN_START_DELAY before sending the first line of active video. When this bit is set to a 0, the video processor will send the first active line as soon as it is available following expiration of the horizontal blanking timer. A setting of 0 allows reduced stretching of horizontal blanking if the video generator clock is faster than incoming data, but may be less tolerant to large frequency difference between the clocks.
6	IGNORE_LINE_NUM	R/W	0x0	Video Processor Timing Generator Ignore Line Number This register bit controls allows the video timing generator to ignore the line number for starting active video and detecting error conditions. 1: Ignore Line Number 0: Require proper line number for starting active video
5	VP_WAIT4LINE	R/W	0x1	Video Processor wait for Video Line This register bit controls how the timing generator handles a condition where first video line is not available at the end of the Vertical Back Porch Timing 1: Wait for first video line, adding delay in the horizontal back porch period 0: Generate extra vertical lines of blanking while waiting This register is for debug purpose only
4:3	VP_DROP_FRAMES	R/W	0x1	Video Process Drop Frames control Controls the number of video frames to drop at start of video reception. By default, the first frame (typically a partial frame) will be dropped.
2	VP_GEN_CORRECT_LATE	R/W	0x0	Enable Horizontal Front Porch correction for late condition in video timing generation
1:0	VP_SRC_SELECT	R/W	0x2	Video Processor Source Select Selects between 4 input video streams Default setting of this register will match the port number for the video processor.

**7.6.2.10.105 H\_ACTIVE0\_SHADOW\_VP2 Register (Address = 0x82) [Default = 0x00]**H\_ACTIVE0\_SHADOW\_VP2 is shown in [Table 7-743](#).Return to the [Summary Table](#).**Table 7-743. H\_ACTIVE0\_SHADOW\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	H_ACTIVE_SHADOW_7_0	R/W	0x0	Horizontal Active period This value should be programmed to match the VID_H_ACTIVE parameter in pixels

**7.6.2.10.106 H\_ACTIVE1\_SHADOW\_VP2 Register (Address = 0x83) [Default = 0x00]**H\_ACTIVE1\_SHADOW\_VP2 is shown in [Table 7-744](#).Return to the [Summary Table](#).**Table 7-744. H\_ACTIVE1\_SHADOW\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	H_ACTIVE_SHADOW_15_8	R/W	0x0	Horizontal Active period This value should be programmed to match the VID_H_ACTIVE parameter in pixels

**7.6.2.10.107 V\_ACTIVE0\_SHADOW\_VP2 Register (Address = 0x84) [Default = 0x00]**V\_ACTIVE0\_SHADOW\_VP2 is shown in [Table 7-745](#).Return to the [Summary Table](#).**Table 7-745. V\_ACTIVE0\_SHADOW\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	V_ACTIVE_SHADOW_7_0	R/W	0x0	Vertical Active period This value should be programmed to match the VID_V_ACTIVE parameter in pixels

**7.6.2.10.108 V\_ACTIVE1\_SHADOW\_VP2 Register (Address = 0x85) [Default = 0x00]**V\_ACTIVE1\_SHADOW\_VP2 is shown in [Table 7-746](#).Return to the [Summary Table](#).**Table 7-746. V\_ACTIVE1\_SHADOW\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	V_ACTIVE_SHADOW_15_-8	R/W	0x0	Vertical Active period This value should be programmed to match the VID_V_ACTIVE parameter in pixels

**7.6.2.10.109 VFILTER\_A\_VP2 Register (Address = 0x86) [Default = 0x01]**VFILTER\_A\_VP2 is shown in [Table 7-747](#).Return to the [Summary Table](#).**Table 7-747. VFILTER\_A\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	VFILTER_ALT_LINE	R/W	0x0	Select for alternate line images. This bit applies for the special case when the VFILTER_A=1 and VFILTER_N=2 0- extract lines (0, 2, 4 ...) 1- extract lines (1, 3, 5 ...)
6	RESERVED	R	0x0	Reserved
5:0	VFILTER_A	R/W	0x1	Vertical Filter A parameter Controls the number of lines (A) of each block of N lines that will be forwarded if Vertical Filter is enabled

**7.6.2.10.110 VFILTER\_N\_VP2 Register (Address = 0x87) [Default = 0x01]**VFILTER\_N\_VP2 is shown in [Table 7-748](#).Return to the [Summary Table](#).**Table 7-748. VFILTER\_N\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	VFILTER_N	R/W	0x1	Vertical Filter N parameter Controls the block size (N) for vertical filter operation.

**7.6.2.10.111 CROP\_START\_X0\_VP2 Register (Address = 0x88) [Default = 0x00]**CROP\_START\_X0\_VP2 is shown in [Table 7-749](#).

Return to the [Summary Table](#).

**Table 7-749. CROP\_START\_X0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_X[7:0]	R/W	0x0	Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.112 CROP\_START\_X1\_VP2 Register (Address = 0x89) [Default = 0x00]**

CROP\_START\_X1\_VP2 is shown in [Table 7-750](#).

Return to the [Summary Table](#).

**Table 7-750. CROP\_START\_X1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_X[15:8]	R/W	0x0	Image Cropping Start X position (bits 15:8) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.113 CROP\_START\_Y0\_VP2 Register (Address = 0x8A) [Default = 0x00]**

CROP\_START\_Y0\_VP2 is shown in [Table 7-751](#).

Return to the [Summary Table](#).

**Table 7-751. CROP\_START\_Y0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[7:0]	R/W	0x0	Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.114 CROP\_START\_Y1\_VP2 Register (Address = 0x8B) [Default = 0x00]**

CROP\_START\_Y1\_VP2 is shown in [Table 7-752](#).

Return to the [Summary Table](#).

**Table 7-752. CROP\_START\_Y1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[15:8]	R/W	0x0	Image Cropping Start Y position (bits 15:8) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.115 CROP\_STOP\_X0\_VP2 Register (Address = 0x8C) [Default = 0x00]**CROP\_STOP\_X0\_VP2 is shown in [Table 7-753](#).Return to the [Summary Table](#).**Table 7-753. CROP\_STOP\_X0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[7:0]	R/W	0x0	Image Cropping Stop X position (bits 7:0) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.116 CROP\_STOP\_X1\_VP2 Register (Address = 0x8D) [Default = 0x00]**CROP\_STOP\_X1\_VP2 is shown in [Table 7-754](#).Return to the [Summary Table](#).**Table 7-754. CROP\_STOP\_X1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[15:8]	R/W	0x0	Image Cropping Stop X position (bits 15:8) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.117 CROP\_STOP\_Y0\_VP2 Register (Address = 0x8E) [Default = 0x00]**CROP\_STOP\_Y0\_VP2 is shown in [Table 7-755](#).Return to the [Summary Table](#).**Table 7-755. CROP\_STOP\_Y0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[7:0]	R/W	0x0	Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.118 CROP\_STOP\_Y1\_VP2 Register (Address = 0x8F) [Default = 0x00]**CROP\_STOP\_Y1\_VP2 is shown in [Table 7-756](#).Return to the [Summary Table](#).**Table 7-756. CROP\_STOP\_Y1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[15:8]	R/W	0x0	Image Cropping Stop Y position (bits 15:8) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.119 VID\_H\_ACTIVE0\_VP2 Register (Address = 0x90) [Default = 0x00]**

VID\_H\_ACTIVE0\_VP2 is shown in [Table 7-757](#).

Return to the [Summary Table](#).

**Table 7-757. VID\_H\_ACTIVE0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

**7.6.2.10.120 VID\_H\_ACTIVE1\_VP2 Register (Address = 0x91) [Default = 0x00]**

VID\_H\_ACTIVE1\_VP2 is shown in [Table 7-758](#).

Return to the [Summary Table](#).

**Table 7-758. VID\_H\_ACTIVE1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

**7.6.2.10.121 VID\_H\_BACK0\_VP2 Register (Address = 0x92) [Default = 0x00]**

VID\_H\_BACK0\_VP2 is shown in [Table 7-759](#).

Return to the [Summary Table](#).

**Table 7-759. VID\_H\_BACK0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[7:0]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

**7.6.2.10.122 VID\_H\_BACK1\_VP2 Register (Address = 0x93) [Default = 0x00]**

VID\_H\_BACK1\_VP2 is shown in [Table 7-760](#).

Return to the [Summary Table](#).

**Table 7-760. VID\_H\_BACK1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[15:8]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

**7.6.2.10.123 VID\_H\_WIDTH0\_VP2 Register (Address = 0x94) [Default = 0x00]**

VID\_H\_WIDTH0\_VP2 is shown in [Table 7-761](#).

Return to the [Summary Table](#).

**Table 7-761. VID\_H\_WIDTH0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[7:0]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

**7.6.2.10.124 VID\_H\_WIDTH1\_VP2 Register (Address = 0x95) [Default = 0x00]**VID\_H\_WIDTH1\_VP2 is shown in [Table 7-762](#).Return to the [Summary Table](#).**Table 7-762. VID\_H\_WIDTH1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[15:8]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

**7.6.2.10.125 VID\_H\_TOTAL0\_VP2 Register (Address = 0x96) [Default = 0x00]**VID\_H\_TOTAL0\_VP2 is shown in [Table 7-763](#).Return to the [Summary Table](#).**Table 7-763. VID\_H\_TOTAL0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[7:0]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead. *H total must be divisible by 4

**7.6.2.10.126 VID\_H\_TOTAL1\_VP2 Register (Address = 0x97) [Default = 0x00]**VID\_H\_TOTAL1\_VP2 is shown in [Table 7-764](#).Return to the [Summary Table](#).**Table 7-764. VID\_H\_TOTAL1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[15:8]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead. *H total must be divisible by 4

**7.6.2.10.127 VID\_V\_ACTIVE0\_VP2 Register (Address = 0x98) [Default = 0x00]**VID\_V\_ACTIVE0\_VP2 is shown in [Table 7-765](#).Return to the [Summary Table](#).**Table 7-765. VID\_V\_ACTIVE0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

**7.6.2.10.128 VID\_V\_ACTIVE1\_VP2 Register (Address = 0x99) [Default = 0x00]**

VID\_V\_ACTIVE1\_VP2 is shown in [Table 7-766](#).

Return to the [Summary Table](#).

**Table 7-766. VID\_V\_ACTIVE1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

**7.6.2.10.129 VID\_V\_BACK0\_VP2 Register (Address = 0x9A) [Default = 0x00]**

VID\_V\_BACK0\_VP2 is shown in [Table 7-767](#).

Return to the [Summary Table](#).

**Table 7-767. VID\_V\_BACK0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[7:0]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

**7.6.2.10.130 VID\_V\_BACK1\_VP2 Register (Address = 0x9B) [Default = 0x00]**

VID\_V\_BACK1\_VP2 is shown in [Table 7-768](#).

Return to the [Summary Table](#).

**Table 7-768. VID\_V\_BACK1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[15:8]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

**7.6.2.10.131 VID\_V\_WIDTH0\_VP2 Register (Address = 0x9C) [Default = 0x00]**

VID\_V\_WIDTH0\_VP2 is shown in [Table 7-769](#).

Return to the [Summary Table](#).

**Table 7-769. VID\_V\_WIDTH0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[7:0]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

**7.6.2.10.132 VID\_V\_WIDTH1\_VP2 Register (Address = 0x9D) [Default = 0x00]**

VID\_V\_WIDTH1\_VP2 is shown in [Table 7-770](#).

Return to the [Summary Table](#).

**Table 7-770. VID\_V\_WIDTH1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[15:8]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

**7.6.2.10.133 VID\_V\_FRONT0\_VP2 Register (Address = 0x9E) [Default = 0x00]**VID\_V\_FRONT0\_VP2 is shown in [Table 7-771](#).Return to the [Summary Table](#).**Table 7-771. VID\_V\_FRONT0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[7:0]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

**7.6.2.10.134 VID\_V\_FRONT1\_VP2 Register (Address = 0x9F) [Default = 0x00]**VID\_V\_FRONT1\_VP2 is shown in [Table 7-772](#).Return to the [Summary Table](#).**Table 7-772. VID\_V\_FRONT1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[15:8]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

**7.6.2.10.135 GEN\_LATE\_THRESH\_VP2 Register (Address = 0xA0) [Default = 0x00]**GEN\_LATE\_THRESH\_VP2 is shown in [Table 7-773](#).Return to the [Summary Table](#).**Table 7-773. GEN\_LATE\_THRESH\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LATE_THRESH	R/W	0x0	Video Timing Late Threshold This value controls the threshold for sending a late pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is late by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

**7.6.2.10.136 GEN\_EARLY\_THRESH\_VP2 Register (Address = 0xA1) [Default = 0x00]**GEN\_EARLY\_THRESH\_VP2 is shown in [Table 7-774](#).Return to the [Summary Table](#).

**Table 7-774. GEN\_EARLY\_THRESH\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EARLY_THRESH	R/W	0x0	Video Timing Early Threshold This value controls the threshold for sending an early pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is early by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

**7.6.2.10.137 GEN\_START\_DELAY\_VP2 Register (Address = 0xA2) [Default = 0x10]**GEN\_START\_DELAY\_VP2 is shown in [Table 7-775](#).Return to the [Summary Table](#).**Table 7-775. GEN\_START\_DELAY\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	GEN_STRT_DLY[7:0]	R/W	0x10	Video Timing Start Delay Provides a delay from HSync pulse to regenerating horizontal image timing. Setting is in units of 16 pixel clocks.

**7.6.2.10.138 PCLK\_GEN\_M\_0\_VP2 Register (Address = 0xA3) [Default = 0x00]**PCLK\_GEN\_M\_0\_VP2 is shown in [Table 7-776](#).Return to the [Summary Table](#).**Table 7-776. PCLK\_GEN\_M\_0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PCLK_GEN_M[7:0]	R/W	0x0	PCLK Generator M value (bits 7:0) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

**7.6.2.10.139 PCLK\_GEN\_M\_1\_VP2 Register (Address = 0xA4) [Default = 0x10]**PCLK\_GEN\_M\_1\_VP2 is shown in [Table 7-777](#).Return to the [Summary Table](#).**Table 7-777. PCLK\_GEN\_M\_1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	PCLK_GEN_M[14:8]	R/W	0x10	PCLK Generator M value (bits 14:8) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

**7.6.2.10.140 PCLK\_GEN\_N\_VP2 Register (Address = 0xA5) [Default = 0x0F]**PCLK\_GEN\_N\_VP2 is shown in [Table 7-778](#).Return to the [Summary Table](#).**Table 7-778. PCLK\_GEN\_N\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

**Table 7-778. PCLK\_GEN\_N\_VP2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	PCLK_GEN_N	R/W	0xF	PCLK Generator N value Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the control of the N value. Actual value is $2^{\text{PCLK\_GEN\_M}}$ . The default setting for this register chooses an N value of $2^{15}$ or 32,768.

**7.6.2.10.141 MAX\_M\_ADJUST\_VP2 Register (Address = 0xA6) [Default = 0x08]**MAX\_M\_ADJUST\_VP2 is shown in [Table 7-779](#).Return to the [Summary Table](#).**Table 7-779. MAX\_M\_ADJUST\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MAX_M_ADJUST	R/W	0x8	Pixel Clock Generator Max Adjustment Video Timing generation will attempt to match pixel clock generation to the incoming video stream. This register sets a limit on the maximum +/- adjustment to the PCLK_GEN_M value.

**7.6.2.10.142 VID\_PROC\_CFG2\_VP2 Register (Address = 0xA7) [Default = 0x00]**VID\_PROC\_CFG2\_VP2 is shown in [Table 7-780](#).Return to the [Summary Table](#).**Table 7-780. VID\_PROC\_CFG2\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DUAL_MERGE_ALT_DLY	R/W	0x0	Dual Merge Alt mode path delay control (measured in input pixel clocks) 00- no delay 01- one clock delay 10- two clock delay 11- three clock delay
4	CROP_ALT_PIX_RIGHT	R/W	0x0	Alternate pixel cropping right enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is selected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , right pixels selected
3	CROP_ALT_PIX_LEFT	R/W	0x0	Alternate pixel cropping left enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is selected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , left pixels selected
2	GEN_VS_POL	R/W	0x0	Vertical Sync Polarity: Controls polarity of the vertical sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
1	GEN_HS_POL	R/W	0x0	Horizontal Sync Polarity: Controls polarity of the horizontal sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated

**Table 7-780. VID\_PROC\_CFG2\_VP2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	VP_AUTO_DETECT	R/W	0x0	Video Processor Auto-detect timing Setting this bit to a 1 allows the video processor timing generator to auto-detect the Horizontal period. It will use the auto-detected value (MEAS_H_TOTAL registers) instead of the value in the VID_H_TOTAL registers.

**7.6.2.10.143 FPD4\_PGCTL\_VP2 Register (Address = 0xA8) [Default = 0x08]**FPD4\_PGCTL\_VP2 is shown in [Table 7-781](#).Return to the [Summary Table](#).**Table 7-781. FPD4\_PGCTL\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	<p>Fixed Pattern Select:  This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PGEN_INV is set to 1.</p> <ul style="list-style-type: none"> <li>00000: Checkerboard (White/Black)</li> <li>00001: White</li> <li>00010: Black</li> <li>00011: Red</li> <li>00100: Green</li> <li>00101: Blue</li> <li>00110: Horizontally Scaled Black to White</li> <li>00111: Horizontally Scaled Black to Red</li> <li>01000: Horizontally Scaled Black to Green</li> <li>01001: Horizontally Scaled Black to Blue</li> <li>01010: Vertically Scaled Black to White</li> <li>01011: Vertically Scaled Black to Red</li> <li>01100: Vertically Scaled Black to Green</li> <li>01101: Vertically Scaled Black to Blue</li> <li>01110: Custom color configured in PGRS, PGGS, PGBS registers</li> <li>01111: VCOM (Yellow, Cyan, Blue, Red)</li> <li>10000: Alternate VCOM (Blue, Cyan, Yellow, Red)</li> <li>10001: Custom Color Checkerboard (Custom/Black)</li> <li>10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black)</li> <li>10011: UNH-IOL MIPI D-PHY compliance test pattern</li> <li>11010-11111: Reserved</li> </ul>
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 1: Enable Pattern Generator asynchronous to video input 0: Enable Pattern Generator synchronous to video input

**Table 7-781. FPD4\_PGCTL\_VP2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	<p>When PATGEN_LEGACY_ENB= 0,  Pattern generator, pattern checker and  forwarding enable encoding:  00: Disable pattern generator and pattern checker  01: Enable pattern generator  10: Enable pattern checker, do not forward patterns on to the RX  datapath  11: Enable pattern checker, forward patterns on to the RX datapath  When PAT_ENC_EN= 2 'b10 or PAT_ENC_EN= 2 'b11, the local  pattern generator is still enabled internally for comparison with  incoming video stream  When PAT_ENC_EN= 2 'b11, the local pattern generator's patterns  are forwarded, not the incoming video stream  When PATGEN_LEGACY_ENB= 1,  PAT_ENC_EN[1]:  1: Enable pattern checker  0: Disable pattern checker  PAT_ENC_EN[0]:  1: Enable pattern generator  0: Disable pattern generator  Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]</p>

#### 7.6.2.10.144 FPD4\_PGCFG\_VP2 Register (Address = 0xA9) [Default = 0x08]

FPD4\_PGCFG\_VP2 is shown in [Table 7-782](#).

Return to the [Summary Table](#).

**Table 7-782. FPD4\_PGCFG\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHK	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 11: Scale checkered patterns by 16 (each square is 16x16 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 00: Normal operation (each square is 1x1 pixel)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 10: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 11: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.

**Table 7-782. FPD4\_PGCfg\_VP2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

**7.6.2.10.145 FPD4\_PGIA\_VP2 Register (Address = 0xAA) [Default = 0x00]**FPD4\_PGIA\_VP2 is shown in [Table 7-783](#).Return to the [Summary Table](#).**Table 7-783. FPD4\_PGIA\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

**7.6.2.10.146 FPD4\_Pgid\_VP2 Register (Address = 0xAB) [Default = 0x00]**FPD4\_Pgid\_VP2 is shown in [Table 7-784](#).Return to the [Summary Table](#).**Table 7-784. FPD4\_Pgid\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

**7.6.2.10.147 FPD4\_Pgdbg\_VP2 Register (Address = 0xAC) [Default = 0x00]**FPD4\_Pgdbg\_VP2 is shown in [Table 7-785](#).Return to the [Summary Table](#).**Table 7-785. FPD4\_Pgdbg\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	PATGEN_ERR_INJ	R/W	0x0	Error Injection Select: 0: Disable error injection 1: Enable error injection
2	PATGEN RAND	R/W	0x0	Random Pattern Generation Select: 1: Output a pseudo-random pattern, overriding all other pattern selection. 0: Output a pattern as configured in Fixed or Auto-Scrolling Pattern Modes.
1	RESERVED	R/W	0x0	Reserved

**Table 7-785. FPD4\_PGDBG\_VP2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	RESERVED	RH/W1S	0x0	Reserved

**7.6.2.10.148 FPD4\_PGTSTDAT\_VP2 Register (Address = 0xAD) [Default = 0x00]**FPD4\_PGTSTDAT\_VP2 is shown in [Table 7-786](#).Return to the [Summary Table](#).**Table 7-786. FPD4\_PGTSTDAT\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGCE register.
6	RESERVED	R	0x0	Reserved
5:0	PATGEN_TST_DATA	R	0x0	Test Data: This field contains the Debug Monitor output. See the Debug Monitor section of the Pattern Generator DDS for details.

**7.6.2.10.149 VP\_STS\_VP2 Register (Address = 0xB0) [Default = 0x00]**VP\_STS\_VP2 is shown in [Table 7-787](#).Return to the [Summary Table](#).**Table 7-787. VP\_STS\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	VP_INTERRUPT	R	0x0	Video Processor Interrupt Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP_STATUS_CHANGE	RC	0x0	Video Processor Status Changed This bit will be set if the Tming Generator status has changed. It is a read-only copy of the IS_VP_STATUS_CHANGE bit in the VP_ISR_0 register. It will be cleared when The VP_ISR_0 Register is read.
0	TIMING_GEN_STS	R	0x0	Timing Generator Status This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

**7.6.2.10.150 INTR\_STS\_VP\_VP2 Register (Address = 0xB1) [Default = 0x00]**INTR\_STS\_VP\_VP2 is shown in [Table 7-788](#).Return to the [Summary Table](#).**Table 7-788. INTR\_STS\_VP\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_CROP_VERT_ERR	RC	0x0	Video Crop Vertical error This error is reported if the Video Cropping module detects that the video frame is too short for proper cropping.
5	IS_CROP_HOR_ERR	RC	0x0	Video Crop Horizontal error This error is reported if the Video Cropping module detects that the video line is too short for proper cropping.

**Table 7-788. INTR\_STS\_VP\_VP2 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	IS_TIMING_DATA_ERR	RC	0x0	Timing Gen Data Available error This error is reported if the timing generator detects a line length error or other error that results in no data available to send from the video buffer during active horizontal period.
3	IS_TIMING_LINE_ERR	RC	0x0	Timing Gen Line Number error This error is reported if the timing generator detects a mismatch with the incoming line number. This may occur on video buffer errors or if timing is not synchronized between incoming stream and timing generator. When this event occurs, video lines will be flushed from the video buffers.
2	IS_TIMING_STRT_ERR	RC	0x0	Timing Gen Active Start error At start of active video period, this error will be set if video data is not available
1	IS_VP_VBUF_ERR	RC	0x0	Video Buffer error This field Indicates the video buffer logic detected a buffer overflow error.
0	IS_VP_STATUS_CHANGE	RC	0x0	Video Processor Status Changed This bit will be set if Video Processor status has changed.

**7.6.2.10.151 INTR\_CTL\_VP\_VP2 Register (Address = 0xB3) [Default = 0x00]**INTR\_CTL\_VP\_VP2 is shown in [Table 7-789](#).Return to the [Summary Table](#).**Table 7-789. INTR\_CTL\_VP\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_CROP_VERT_ERR	R/W	0x0	Enable Video Crop Vertical error interrupt
5	IE_CROP_HOR_ERR	R/W	0x0	Enable Video Crop Horizontal error interrupt
4	IE_TIMING_DATA_ERR	R/W	0x0	Enable Timing Gen Data Available error interrupt
3	IE_TIMING_LINE_ERR	R/W	0x0	Enable Timing Gen Line Number error interrupt
2	IE_TIMING_STRT_ERR	R/W	0x0	Enable Timing Gen Active Start error interrupt
1	IE_VP_VBUF_ERR	R/W	0x0	Enable Video Buffer error interrupt
0	IE_VP_STATUS_CHANGE	R/W	0x0	Enable Video Processor Status Changed

**7.6.2.10.152 MEAS\_H\_TOTAL0\_VP2 Register (Address = 0xB5) [Default = 0x00]**MEAS\_H\_TOTAL0\_VP2 is shown in [Table 7-790](#).Return to the [Summary Table](#).**Table 7-790. MEAS\_H\_TOTAL0\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[7:0]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

**7.6.2.10.153 MEAS\_H\_TOTAL1\_VP2 Register (Address = 0xB6) [Default = 0x00]**

MEAS\_H\_TOTAL1\_VP2 is shown in [Table 7-791](#).

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**Table 7-791. MEAS\_H\_TOTAL1\_VP2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[15:8]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

**7.6.2.10.154 VID\_PROC\_CTL\_VP3 Register (Address = 0xC0) [Default = 0x00]**

VID\_PROC\_CTL\_VP3 is shown in [Table 7-792](#).

Return to the [Summary Table](#).

**Table 7-792. VID\_PROC\_CTL\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	VP_DUAL_MERGE_LR_EN	R/W	0x0	Enable Merge of Dual Images for Concatenated LR Output This bit enables merging of dual image, one from each Video Processor into a single image with concatenated left right image. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The line from VP0 (VP2) is output first. This generated the left line followed by the right line assuming VP0(VP2) receives the left image and VP1(VP3) receives the right image.
3	VP_DUAL_MERGE_ALT_EN	R/W	0x0	Enable Merge of Dual Images for Alternate Pixel Output This bit enables merging of dual image, one from each Video Processor into a single image with alternating pixels. The Video Processor can only be paired as VP0/VP1 or VP2/VP3. The pixel from VP0 (VP2) is output first.
2	VP_EN_CROP	R/W	0x0	Enable Video Cropping This bit enables video cropping. Video cropping controls should be configured prior to setting this bit. In addition, video cropping controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
1	VP_EN_VFILT	R/W	0x0	Enable Vertical Filter processing This bit enables vertical line filter for multi-image processing. Vertical Filter controls should be configured prior to setting this bit. In addition, Vertical Filter controls should be configured prior to setting the Video Processor Enable control in the main register page VP_ENABLE_REG.
0	VP_ENABLE	R	0x0	Enable Video Processor This is a read-only copy of the Video Processor enable in the main register page VP_ENABLE_REG.

**7.6.2.10.155 VID\_PROC\_CFG\_VP3 Register (Address = 0xC1) [Default = 0xAB]**

VID\_PROC\_CFG\_VP3 is shown in [Table 7-793](#).

Return to the [Summary Table](#).

**Table 7-793. VID\_PROC\_CFG\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESYNC_1ST_LINE	R/W	0x1	Video Processor Re-sync first Line When this bit is set, the video processor will wait for the full GEN_START_DELAY before sending the first line of active video. When this bit is set to a 0, the video processor will send the first active line as soon as it is available following expiration of the horizontal blanking timer. A setting of 0 allows reduced stretching of horizontal blanking if the video generator clock is faster than incoming data, but may be less tolerant to large frequency difference between the clocks.
6	IGNORE_LINE_NUM	R/W	0x0	Video Processor Timing Generator Ignore Line Number This register bit controls allows the video timing generator to ignore the line number for starting active video and detecting error conditions. 1: Ignore Line Number 0: Require proper line number for starting active video
5	VP_WAIT4LINE	R/W	0x1	Video Processor wait for Video Line This register bit controls how the timing generator handles a condition where first video line is not available at the end of the Vertical Back Porch Timing 1: Wait for first video line, adding delay in the horizontal back porch period 0: Generate extra vertical lines of blanking while waiting This register is for debug purpose only
4:3	VP_DROP_FRAMES	R/W	0x1	Video Process Drop Frames control Controls the number of video frames to drop at start of video reception. By default, the first frame (typically a partial frame) will be dropped.
2	VP_GEN_CORRECT_LATE	R/W	0x0	Enable Horizontal Front Porch correction for late condition in video timing generation
1:0	VP_SRC_SELECT	R/W	0x3	Video Processor Source Select Selects between 4 input video streams Default setting of this register will match the port number for the video processor.

**7.6.2.10.156 H\_ACTIVE0\_SHADOW\_VP3 Register (Address = 0xC2) [Default = 0x00]**H\_ACTIVE0\_SHADOW\_VP3 is shown in [Table 7-794](#).Return to the [Summary Table](#).**Table 7-794. H\_ACTIVE0\_SHADOW\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	H_ACTIVE_SHADOW_7_0	R/W	0x0	Horizontal Active period This value should be programmed to match the VID_H_ACTIVE parameter in pixels

**7.6.2.10.157 H\_ACTIVE1\_SHADOW\_VP3 Register (Address = 0xC3) [Default = 0x00]**H\_ACTIVE1\_SHADOW\_VP3 is shown in [Table 7-795](#).Return to the [Summary Table](#).**Table 7-795. H\_ACTIVE1\_SHADOW\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	H_ACTIVE_SHADOW_15_8	R/W	0x0	Horizontal Active period This value should be programmed to match the VID_H_ACTIVE parameter in pixels

**7.6.2.10.158 V\_ACTIVE0\_SHADOW\_VP3 Register (Address = 0xC4) [Default = 0x00]**V\_ACTIVE0\_SHADOW\_VP3 is shown in [Table 7-796](#).Return to the [Summary Table](#).**Table 7-796. V\_ACTIVE0\_SHADOW\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	V_ACTIVE_SHADOW_7_0	R/W	0x0	Vertical Active period This value should be programmed to match the VID_V_ACTIVE parameter in pixels

**7.6.2.10.159 V\_ACTIVE1\_SHADOW\_VP3 Register (Address = 0xC5) [Default = 0x00]**V\_ACTIVE1\_SHADOW\_VP3 is shown in [Table 7-797](#).Return to the [Summary Table](#).**Table 7-797. V\_ACTIVE1\_SHADOW\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	V_ACTIVE_SHADOW_15_-8	R/W	0x0	Vertical Active period This value should be programmed to match the VID_V_ACTIVE parameter in pixels

**7.6.2.10.160 VFILTER\_A\_VP3 Register (Address = 0xC6) [Default = 0x01]**VFILTER\_A\_VP3 is shown in [Table 7-798](#).Return to the [Summary Table](#).**Table 7-798. VFILTER\_A\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	VFILTER_ALT_LINE	R/W	0x0	Select for alternate line images. This bit applies for the special case when the VFILTER_A=1 and VFILTER_N=2 0- extract lines (0, 2, 4 ...) 1- extract lines (1, 3, 5 ...)
6	RESERVED	R	0x0	Reserved
5:0	VFILTER_A	R/W	0x1	Vertical Filter A parameter Controls the number of lines (A) of each block of N lines that will be forwarded if Vertical Filter is enabled

**7.6.2.10.161 VFILTER\_N\_VP3 Register (Address = 0xC7) [Default = 0x01]**VFILTER\_N\_VP3 is shown in [Table 7-799](#).Return to the [Summary Table](#).**Table 7-799. VFILTER\_N\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	VFILTER_N	R/W	0x1	Vertical Filter N parameter Controls the block size (N) for vertical filter operation.

**7.6.2.10.162 CROP\_START\_X0\_VP3 Register (Address = 0xC8) [Default = 0x00]**CROP\_START\_X0\_VP3 is shown in [Table 7-800](#).

Return to the [Summary Table](#).

**Table 7-800. CROP\_START\_X0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_X[7:0]	R/W	0x0	Image Cropping Start X position (bits 7:0) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.163 CROP\_START\_X1\_VP3 Register (Address = 0xC9) [Default = 0x00]**

CROP\_START\_X1\_VP3 is shown in [Table 7-801](#).

Return to the [Summary Table](#).

**Table 7-801. CROP\_START\_X1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_X[15:8]	R/W	0x0	Image Cropping Start X position (bits 15:8) The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.164 CROP\_START\_Y0\_VP3 Register (Address = 0xCA) [Default = 0x00]**

CROP\_START\_Y0\_VP3 is shown in [Table 7-802](#).

Return to the [Summary Table](#).

**Table 7-802. CROP\_START\_Y0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[7:0]	R/W	0x0	Image Cropping Start Y position (bits 7:0) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.165 CROP\_START\_Y1\_VP3 Register (Address = 0xCB) [Default = 0x00]**

CROP\_START\_Y1\_VP3 is shown in [Table 7-803](#).

Return to the [Summary Table](#).

**Table 7-803. CROP\_START\_Y1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_START_Y[15:8]	R/W	0x0	Image Cropping Start Y position (bits 15:8) The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.166 CROP\_STOP\_X0\_VP3 Register (Address = 0xCC) [Default = 0x00]**CROP\_STOP\_X0\_VP3 is shown in [Table 7-804](#).Return to the [Summary Table](#).**Table 7-804. CROP\_STOP\_X0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[7:0]	R/W	0x0	Image Cropping Stop X position (bits 7:0) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.167 CROP\_STOP\_X1\_VP3 Register (Address = 0xCD) [Default = 0x00]**CROP\_STOP\_X1\_VP3 is shown in [Table 7-805](#).Return to the [Summary Table](#).**Table 7-805. CROP\_STOP\_X1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_X[15:8]	R/W	0x0	Image Cropping Stop X position (bits 15:8) The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position will not be forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

**7.6.2.10.168 CROP\_STOP\_Y0\_VP3 Register (Address = 0xCE) [Default = 0x00]**CROP\_STOP\_Y0\_VP3 is shown in [Table 7-806](#).Return to the [Summary Table](#).**Table 7-806. CROP\_STOP\_Y0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[7:0]	R/W	0x0	Image Cropping Stop Y position (bits 7:0) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.169 CROP\_STOP\_Y1\_VP3 Register (Address = 0xCF) [Default = 0x00]**CROP\_STOP\_Y1\_VP3 is shown in [Table 7-807](#).Return to the [Summary Table](#).**Table 7-807. CROP\_STOP\_Y1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	CROP_STOP_Y[15:8]	R/W	0x0	Image Cropping Stop Y position (bits 15:8) The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position will not be forwarded, replaced with blank lines (DE will be deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

**7.6.2.10.170 VID\_H\_ACTIVE0\_VP3 Register (Address = 0xD0) [Default = 0x00]**

VID\_H\_ACTIVE0\_VP3 is shown in [Table 7-808](#).

Return to the [Summary Table](#).

**Table 7-808. VID\_H\_ACTIVE0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

**7.6.2.10.171 VID\_H\_ACTIVE1\_VP3 Register (Address = 0xD1) [Default = 0x00]**

VID\_H\_ACTIVE1\_VP3 is shown in [Table 7-809](#).

Return to the [Summary Table](#).

**Table 7-809. VID\_H\_ACTIVE1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Horizontal Active period This value controls the horizontal active period for Video Timing generation.

**7.6.2.10.172 VID\_H\_BACK0\_VP3 Register (Address = 0xD2) [Default = 0x00]**

VID\_H\_BACK0\_VP3 is shown in [Table 7-810](#).

Return to the [Summary Table](#).

**Table 7-810. VID\_H\_BACK0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[7:0]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

**7.6.2.10.173 VID\_H\_BACK1\_VP3 Register (Address = 0xD3) [Default = 0x00]**

VID\_H\_BACK1\_VP3 is shown in [Table 7-811](#).

Return to the [Summary Table](#).

**Table 7-811. VID\_H\_BACK1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_BACK[15:8]	R/W	0x0	Video Timing Generator Horizontal Back Porch period This value controls the horizontal back porch period for Video Timing generation.

**7.6.2.10.174 VID\_H\_WIDTH0\_VP3 Register (Address = 0xD4) [Default = 0x00]**

VID\_H\_WIDTH0\_VP3 is shown in [Table 7-812](#).

Return to the [Summary Table](#).

**Table 7-812. VID\_H\_WIDTH0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[7:0]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

**7.6.2.10.175 VID\_H\_WIDTH1\_VP3 Register (Address = 0xD5) [Default = 0x00]**VID\_H\_WIDTH1\_VP3 is shown in [Table 7-813](#).Return to the [Summary Table](#).**Table 7-813. VID\_H\_WIDTH1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_WIDTH[15:8]	R/W	0x0	Video Timing Generator Horizontal Sync width This value controls the horizontal Sync pulse width for Video Timing generation.

**7.6.2.10.176 VID\_H\_TOTAL0\_VP3 Register (Address = 0xD6) [Default = 0x00]**VID\_H\_TOTAL0\_VP3 is shown in [Table 7-814](#).Return to the [Summary Table](#).**Table 7-814. VID\_H\_TOTAL0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[7:0]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead. *H total must be divisible by 4

**7.6.2.10.177 VID\_H\_TOTAL1\_VP3 Register (Address = 0xD7) [Default = 0x00]**VID\_H\_TOTAL1\_VP3 is shown in [Table 7-815](#).Return to the [Summary Table](#).**Table 7-815. VID\_H\_TOTAL1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_H_TOTAL[15:8]	R/W	0x0	Video Timing Generator Horizontal period This value controls the total horizontal period for Video Timing generation. If VP_AUTO_DETECT is set to 1, this value is ignored and the measured horizontal period is used instead. *H total must be divisible by 4

**7.6.2.10.178 VID\_V\_ACTIVE0\_VP3 Register (Address = 0xD8) [Default = 0x00]**VID\_V\_ACTIVE0\_VP3 is shown in [Table 7-816](#).Return to the [Summary Table](#).**Table 7-816. VID\_V\_ACTIVE0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[7:0]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

**7.6.2.10.179 VID\_V\_ACTIVE1\_VP3 Register (Address = 0xD9) [Default = 0x00]**

VID\_V\_ACTIVE1\_VP3 is shown in [Table 7-817](#).

Return to the [Summary Table](#).

**Table 7-817. VID\_V\_ACTIVE1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_ACTIVE[15:8]	R/W	0x0	Video Timing Generator Vertical Active period This value controls the vertical active period for Video Timing generation.

**7.6.2.10.180 VID\_V\_BACK0\_VP3 Register (Address = 0xDA) [Default = 0x00]**

VID\_V\_BACK0\_VP3 is shown in [Table 7-818](#).

Return to the [Summary Table](#).

**Table 7-818. VID\_V\_BACK0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[7:0]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

**7.6.2.10.181 VID\_V\_BACK1\_VP3 Register (Address = 0xDB) [Default = 0x00]**

VID\_V\_BACK1\_VP3 is shown in [Table 7-819](#).

Return to the [Summary Table](#).

**Table 7-819. VID\_V\_BACK1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_BACK[15:8]	R/W	0x0	Video Timing Generator Vertical Back Porch period This value controls the vertical back porch period for Video Timing generation.

**7.6.2.10.182 VID\_V\_WIDTH0\_VP3 Register (Address = 0xDC) [Default = 0x00]**

VID\_V\_WIDTH0\_VP3 is shown in [Table 7-820](#).

Return to the [Summary Table](#).

**Table 7-820. VID\_V\_WIDTH0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[7:0]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

**7.6.2.10.183 VID\_V\_WIDTH1\_VP3 Register (Address = 0xDD) [Default = 0x00]**

VID\_V\_WIDTH1\_VP3 is shown in [Table 7-821](#).

Return to the [Summary Table](#).

**Table 7-821. VID\_V\_WIDTH1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_WIDTH[15:8]	R/W	0x0	Video Timing Generator Vertical Sync width This value controls the vertical Sync pulse width for Video Timing generation.

**7.6.2.10.184 VID\_V\_FRONT0\_VP3 Register (Address = 0xDE) [Default = 0x00]**VID\_V\_FRONT0\_VP3 is shown in [Table 7-822](#).Return to the [Summary Table](#).**Table 7-822. VID\_V\_FRONT0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[7:0]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

**7.6.2.10.185 VID\_V\_FRONT1\_VP3 Register (Address = 0xDF) [Default = 0x00]**VID\_V\_FRONT1\_VP3 is shown in [Table 7-823](#).Return to the [Summary Table](#).**Table 7-823. VID\_V\_FRONT1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	VID_V_FRONT[15:8]	R/W	0x0	Video Timing Generator Vertical Front Porch period This value controls the vertical front porch period for Video Timing generation

**7.6.2.10.186 GEN\_LATE\_THRESH\_VP3 Register (Address = 0xE0) [Default = 0x00]**GEN\_LATE\_THRESH\_VP3 is shown in [Table 7-824](#).Return to the [Summary Table](#).**Table 7-824. GEN\_LATE\_THRESH\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LATE_THRESH	R/W	0x0	Video Timing Late Threshold This value controls the threshold for sending a late pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is late by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

**7.6.2.10.187 GEN\_EARLY\_THRESH\_VP3 Register (Address = 0xE1) [Default = 0x00]**GEN\_EARLY\_THRESH\_VP3 is shown in [Table 7-825](#).Return to the [Summary Table](#).

**Table 7-825. GEN\_EARLY\_THRESH\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EARLY_THRESH	R/W	0x0	Video Timing Early Threshold This value controls the threshold for sending an early pulse to the pixel clock generation for the video timing generator. For each video line, if the timing regeneration detects the pixel clock is early by greater than the LATE_THRESH (in pixels), a pulse will be sent to the clock generator to increment the pixel clock generation M value.

**7.6.2.10.188 GEN\_START\_DELAY\_VP3 Register (Address = 0xE2) [Default = 0x10]**GEN\_START\_DELAY\_VP3 is shown in [Table 7-826](#).Return to the [Summary Table](#).**Table 7-826. GEN\_START\_DELAY\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	GEN_STRT_DLY[7:0]	R/W	0x10	Video Timing Start Delay Provides a delay from HSync pulse to regenerating horizontal image timing. Setting is in units of 16 pixel clocks.

**7.6.2.10.189 PCLK\_GEN\_M\_0\_VP3 Register (Address = 0xE3) [Default = 0x00]**PCLK\_GEN\_M\_0\_VP3 is shown in [Table 7-827](#).Return to the [Summary Table](#).**Table 7-827. PCLK\_GEN\_M\_0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PCLK_GEN_M[7:0]	R/W	0x0	PCLK Generator M value (bits 7:0) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

**7.6.2.10.190 PCLK\_GEN\_M\_1\_VP3 Register (Address = 0xE4) [Default = 0x10]**PCLK\_GEN\_M\_1\_VP3 is shown in [Table 7-828](#).Return to the [Summary Table](#).**Table 7-828. PCLK\_GEN\_M\_1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	PCLK_GEN_M[14:8]	R/W	0x10	PCLK Generator M value (bits 14:8) Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the M value for the divider ratio.

**7.6.2.10.191 PCLK\_GEN\_N\_VP3 Register (Address = 0xE5) [Default = 0x0F]**PCLK\_GEN\_N\_VP3 is shown in [Table 7-829](#).Return to the [Summary Table](#).**Table 7-829. PCLK\_GEN\_N\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

**Table 7-829. PCLK\_GEN\_N\_VP3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
3:0	PCLK_GEN_N	R/W	0xF	PCLK Generator N value Pixel clock generation requires setting an M/N ratio to generate the pixel clock from the FPD4 clock. This register provides the control of the N value. Actual value is $2^{\text{PCLK\_GEN\_M}}$ . The default setting for this register chooses an N value of $2^{15}$ or 32,768.

**7.6.2.10.192 MAX\_M\_ADJUST\_VP3 Register (Address = 0xE6) [Default = 0x08]**MAX\_M\_ADJUST\_VP3 is shown in [Table 7-830](#).Return to the [Summary Table](#).**Table 7-830. MAX\_M\_ADJUST\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MAX_M_ADJUST	R/W	0x8	Pixel Clock Generator Max Adjustment Video Timing generation will attempt to match pixel clock generation to the incoming video stream. This register sets a limit on the maximum +/- adjustment to the PCLK_GEN_M value.

**7.6.2.10.193 VID\_PROC\_CFG2\_VP3 Register (Address = 0xE7) [Default = 0x00]**VID\_PROC\_CFG2\_VP3 is shown in [Table 7-831](#).Return to the [Summary Table](#).**Table 7-831. VID\_PROC\_CFG2\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:5	DUAL_MERGE_ALT_DLY	R/W	0x0	Dual Merge Alt mode path delay control (measured in input pixel clocks) 00- no delay 01- one clock delay 10- two clock delay 11- three clock delay
4	CROP_ALT_PIX_RIGHT	R/W	0x0	Alternate pixel cropping right enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is selected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , right pixels selected
3	CROP_ALT_PIX_LEFT	R/W	0x0	Alternate pixel cropping left enabled. The CROP_ALT_PIX_RIGHT and CROP_ALT_PIX_LEFT work as a pair. If neither is selected then no alternate pixel processing. 0: alternate pixel cropping disabled 1: alternate pixel cropping enabled , left pixels selected
2	GEN_VS_POL	R/W	0x0	Vertical Sync Polarity: Controls polarity of the vertical sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated
1	GEN_HS_POL	R/W	0x0	Horizontal Sync Polarity: Controls polarity of the horizontal sync pulse generated by the Timing Generator 0: Active high pulse generated 1: Active low pulse generated

**Table 7-831. VID\_PROC\_CFG2\_VP3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	VP_AUTO_DETECT	R/W	0x0	Video Processor Auto-detect timing Setting this bit to a 1 allows the video processor timing generator to auto-detect the Horizontal period. It will use the auto-detected value (MEAS_H_TOTAL registers) instead of the value in the VID_H_TOTAL registers.

**7.6.2.10.194 FPD4\_PGCTL\_VP3 Register (Address = 0xE8) [Default = 0x08]**FPD4\_PGCTL\_VP3 is shown in [Table 7-832](#).Return to the [Summary Table](#).**Table 7-832. FPD4\_PGCTL\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	<p>Fixed Pattern Select:  This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PGEN_INV is set to 1.</p> <p>00000: Checkerboard (White/Black)  00001: White  00010: Black  00011: Red  00100: Green  00101: Blue  00110: Horizontally Scaled Black to White  00111: Horizontally Scaled Black to Red  01000: Horizontally Scaled Black to Green  01001: Horizontally Scaled Black to Blue  01010: Vertically Scaled Black to White  01011: Vertically Scaled Black to Red  01100: Vertically Scaled Black to Green  01101: Vertically Scaled Black to Blue  01110: Custom color configured in PGRS, PGGS, PGBS registers  01111: VCOM (Yellow, Cyan, Blue, Red)  10000: Alternate VCOM (Blue, Cyan, Yellow, Red)  10001: Custom Color Checkerboard (Custom/Black)  10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black)  10011: UNH-IOL MIPI D-PHY compliance test pattern  11010-11111: Reserved </p>
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 1: Enable Pattern Generator asynchronous to video input 0: Enable Pattern Generator synchronous to video input

**Table 7-832. FPD4\_PGCTL\_VP3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1:0	PAT_ENC_EN	R/W	0x0	<p>When PATGEN_LEGACY_ENB= 0,          Pattern generator, pattern checker and          forwarding enable encoding:          00: Disable pattern generator and pattern checker          01: Enable pattern generator          10: Enable pattern checker, do not forward patterns on to the RX          datapath          11: Enable pattern checker, forward patterns on to the RX datapath          When PAT_ENC_EN= 2 'b10 or PAT_ENC_EN= 2 'b11, the local          pattern generator is still enabled internally for comparison with          incoming video stream          When PAT_ENC_EN= 2 'b11, the local pattern generator's patterns          are forwarded, not the incoming video stream          When PATGEN_LEGACY_ENB= 1,          PAT_ENC_EN[1]:          1: Enable pattern checker          0: Disable pattern checker          PAT_ENC_EN[0]:          1: Enable pattern generator          0: Disable pattern generator          Setting PAT_ENC_EN[1] will also set PAT_ENC_EN[0]</p>

**7.6.2.10.195 FPD4\_PGCFG\_VP3 Register (Address = 0xE9) [Default = 0x08]**FPD4\_PGCFG\_VP3 is shown in [Table 7-833](#).Return to the [Summary Table](#).**Table 7-833. FPD4\_PGCFG\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHK	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 11: Scale checkered patterns by 16 (each square is 16x16 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 00: Normal operation (each square is 1x1 pixel)
5	PATGEN_LEGACY_ENB	R/W	0x0	Legacy pattern generator and pattern checker enable: See PGCTL[1:0] (PAT_ENC_EN)
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 10: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 11: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.

**Table 7-833. FPD4\_PGCFG\_VP3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

**7.6.2.10.196 FPD4\_PGIA\_VP3 Register (Address = 0xEA) [Default = 0x00]**FPD4\_PGIA\_VP3 is shown in [Table 7-834](#).Return to the [Summary Table](#).**Table 7-834. FPD4\_PGIA\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment: When 1, this bit causes reads or writes to the PGID register to automatically increment PATGEN_IA and thereby increase throughput by eliminating unnecessary writes to PGIA.
6:0	PATGEN_IA	R/W	0x0	Indirect Address: This 7-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-incrementing is enabled and the next address is the desired address.

**7.6.2.10.197 FPD4\_PGID\_VP3 Register (Address = 0xEB) [Default = 0x00]**FPD4\_PGID\_VP3 is shown in [Table 7-835](#).Return to the [Summary Table](#).**Table 7-835. FPD4\_PGID\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value.

**7.6.2.10.198 FPD4\_PGDBG\_VP3 Register (Address = 0xEC) [Default = 0x00]**FPD4\_PGDBG\_VP3 is shown in [Table 7-836](#).Return to the [Summary Table](#).**Table 7-836. FPD4\_PGDBG\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	PATGEN_DBG_SEL	R/W	0x0	Test Mux Select: This field selects the signals to be brought out on the test output bus as well as read in the PGTSTDAT register. See the Debug Monitor section of the Pattern Generator DDS for details.
3	PATGEN_ERR_INJ	R/W	0x0	Error Injection Select: 0: Disable error injection 1: Enable error injection
2	PATGEN RAND	R/W	0x0	Random Pattern Generation Select: 1: Output a pseudo-random pattern, overriding all other pattern selection. 0: Output a pattern as configured in Fixed or Auto-Scrolling Pattern Modes.

**Table 7-836. FPD4\_PGDBG\_VP3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	RH/W1S	0x0	Reserved

**7.6.2.10.199 FPD4\_PGTSTDAT\_VP3 Register (Address = 0xED) [Default = 0x00]**FPD4\_PGTSTDAT\_VP3 is shown in [Table 7-837](#).Return to the [Summary Table](#).**Table 7-837. FPD4\_PGTSTDAT\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag: This bit is 1 if any errors have been seen during pattern checking. It is cleared by a read to the PGCE register.
6	RESERVED	R	0x0	Reserved
5:0	RESERVED	R	0x0	Reserved

**7.6.2.10.200 VP\_STS\_VP3 Register (Address = 0xF0) [Default = 0x00]**VP\_STS\_VP3 is shown in [Table 7-838](#).Return to the [Summary Table](#).**Table 7-838. VP\_STS\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	VP_INTERRUPT	R	0x0	Video Processor Interrupt Indicates if any of the bits in the VP_ISR_0 register are set to 1 and the associated mask bit in the VP_IMR register is also set.
1	VP_STATUS_CHANGE	RC	0x0	Video Processor Status Changed This bit will be set if the Tming Generator status has changed. It is a read-only copy of the IS_VP_STATUS_CHANGE bit in the VP_ISR_0 register. It will be cleared when The VP_ISR_0 Register is read.
0	TIMING_GEN_STS	R	0x0	Timing Generator Status This field Indicates if the timing generator is properly synchronized to incoming video. It will be set following the first video frame forwarded, and remain set until timing fails.

**7.6.2.10.201 INTR\_STS\_VP\_VP3 Register (Address = 0xF1) [Default = 0x00]**INTR\_STS\_VP\_VP3 is shown in [Table 7-839](#).Return to the [Summary Table](#).**Table 7-839. INTR\_STS\_VP\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_CROP_VERT_ERR	RC	0x0	Video Crop Vertical error This error is reported if the Video Cropping module detects that the video frame is too short for proper cropping.
5	IS_CROP_HOR_ERR	RC	0x0	Video Crop Horizontal error This error is reported if the Video Cropping module detects that the video line is too short for proper cropping.

**Table 7-839. INTR\_STS\_VP\_VP3 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	IS_TIMING_DATA_ERR	RC	0x0	Timing Gen Data Available error This error is reported if the timing generator detects a line length error or other error that results in no data available to send from the video buffer during active horizontal period.
3	IS_TIMING_LINE_ERR	RC	0x0	Timing Gen Line Number error This error is reported if the timing generator detects a mismatch with the incoming line number. This may occur on video buffer errors or if timing is not synchronized between incoming stream and timing generator. When this event occurs, video lines will be flushed from the video buffers.
2	IS_TIMING_STRT_ERR	RC	0x0	Timing Gen Active Start error At start of active video period, this error will be set if video data is not available
1	IS_VP_VBUF_ERR	RC	0x0	Video Buffer error This field Indicates the video buffer logic detected a buffer overflow error.
0	IS_VP_STATUS_CHANGE	RC	0x0	Video Processor Status Changed This bit will be set if Video Processor status has changed.

**7.6.2.10.202 INTR\_CTL\_VP\_VP3 Register (Address = 0xF3) [Default = 0x00]**INTR\_CTL\_VP\_VP3 is shown in [Table 7-840](#).Return to the [Summary Table](#).**Table 7-840. INTR\_CTL\_VP\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_CROP_VERT_ERR	R/W	0x0	Enable Video Crop Vertical error interrupt
5	IE_CROP_HOR_ERR	R/W	0x0	Enable Video Crop Horizontal error interrupt
4	IE_TIMING_DATA_ERR	R/W	0x0	Enable Timing Gen Data Available error interrupt
3	IE_TIMING_LINE_ERR	R/W	0x0	Enable Timing Gen Line Number error interrupt
2	IE_TIMING_STRT_ERR	R/W	0x0	Enable Timing Gen Active Start error interrupt
1	IE_VP_VBUF_ERR	R/W	0x0	Enable Video Buffer error interrupt
0	IE_VP_STATUS_CHANGE	R/W	0x0	Enable Video Processor Status Changed

**7.6.2.10.203 MEAS\_H\_TOTAL0\_VP3 Register (Address = 0xF5) [Default = 0x00]**MEAS\_H\_TOTAL0\_VP3 is shown in [Table 7-841](#).Return to the [Summary Table](#).**Table 7-841. MEAS\_H\_TOTAL0\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[7:0]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

### 7.6.2.10.204 MEAS\_H\_TOTAL1\_VP3 Register (Address = 0xF6) [Default = 0x00]

MEAS\_H\_TOTAL1\_VP3 is shown in [Table 7-842](#).

Return to the [Summary Table](#).

**Table 7-842. MEAS\_H\_TOTAL1\_VP3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	MEAS_H_TOTAL[15:8]	R	0x0	Video Timing Measured Horizontal period The Video Timing generator monitors the incoming horizontal period using the video timing quad-pixel clock. The measured total is in pixel clocks and is generated by measuring 4 consecutive lines, providing an averaging of 4 video lines. If the VP_AUTO_DETECT bit is set in the VP_CONFIG_REG2, this value is used as the horizontal total period. Note, this period is updated every 4 lines, so may not be a constant value.

### 7.6.2.11 Page\_14\_ADC\_Control Registers

Table 7-843 lists the memory-mapped registers for the Page\_14\_ADC\_Control registers. All register offset addresses not listed in Table 7-843 should be considered as reserved locations and the register contents should not be modified.

**Table 7-843. PAGE\_14\_ADC\_CONTROL Registers**

Address	Acronym	Register Name	Section
0x4	ADC_CLK_DIV_SEL	ADC_CLK_DIV_SEL	Go
0x7	ADC_INPUT_EN_LSB	ADC_INPUT_EN_LSB	Go
0x8	SAR_ADC_INPUT_EN_MSB	SAR_ADC_INPUT_EN_MSB	Go
0xD	ADC_MODE	ADC_MODE	Go
0x13	TEMP_FINAL	TEMP_FINAL	Go
0x15	IV0_FINAL	IV0_FINAL	Go
0x16	IV1_FINAL	IV1_FINAL	Go
0x17	IV2_FINAL	IV2_FINAL	Go
0x18	IV3_FINAL	IV3_FINAL	Go
0x1B	EXT_VOL0_FINAL	EXT_VOL0_FINAL	Go
0x1C	EXT_VOL1_FINAL	EXT_VOL1_FINAL	Go
0x1D	LINE_FAULT0_FINAL	LINE_FAULT0_FINAL	Go
0x1E	LINE_FAULT1_FINAL	LINE_FAULT1_FINAL	Go
0x1F	LINE_FAULT2_FINAL	LINE_FAULT2_FINAL	Go
0x20	LINE_FAULT3_FINAL	LINE_FAULT3_FINAL	Go
0x23	INT_STATUS_LSB_LOW	INT_STATUS_LSB_LOW	Go
0x24	INT_STATUS_MSB_LOW	INT_STATUS_MSB_LOW	Go
0x25	INT_STATUS_LSB_HIGH	INT_STATUS_LSB_HIGH	Go
0x26	INT_STATUS_MSB_HIGH	INT_STATUS_MSB_HIGH	Go
0x27	INT_LINE_FAULT0_M0	INT_LINE_FAULT0_M0	Go
0x28	INT_LINE_FAULT1_M0	INT_LINE_FAULT1_M0	Go
0x29	INT_LINE_FAULT2_M0	INT_LINE_FAULT2_M0	Go
0x2A	INT_LINE_FAULT3_M0	INT_LINE_FAULT3_M0	Go
0x2B	INT_LINE_FAULT0_M1	INT_LINE_FAULT0_M1	Go
0x2C	INT_LINE_FAULT1_M1	INT_LINE_FAULT1_M1	Go
0x2D	INT_LINE_FAULT2_M1	INT_LINE_FAULT2_M1	Go
0x2E	INT_LINE_FAULT3_M1	INT_LINE_FAULT3_M1	Go
0x2F	INT_LINE_FAULT_UNDEF	INT_LINE_FAULT_UNDEF	Go
0x30	INT_LINE_FAULT_SATURATE	INT_LINE_FAULT_SATURATE	Go
0x33	TEMP_HIGH	TEMP_HIGH	Go
0x34	TEMP_LOW	TEMP_LOW	Go
0x35	TEMP_ADC_OFFSET	TEMP_ADC_OFFSET	Go
0x39	IV0_HIGH	IV0_HIGH	Go
0x3A	IV0_LOW	IV0_LOW	Go
0x3B	IV0_ADC_OFFSET	IV0_ADC_OFFSET	Go
0x3C	IV1_HIGH	IV1_HIGH	Go
0x3D	IV1_LOW	IV1_LOW	Go
0x3E	IV1_ADC_OFFSET	IV1_ADC_OFFSET	Go
0x3F	IV2_HIGH	IV2_HIGH	Go
0x40	IV2_LOW	IV2_LOW	Go
0x41	IV2_ADC_OFFSET	IV2_ADC_OFFSET	Go

**Table 7-843. PAGE\_14\_ADC\_CONTROL Registers (continued)**

Address	Acronym	Register Name	Section
0x42	IV3_HIGH	IV3_HIGH	Go
0x43	IV3_LOW	IV3_LOW	Go
0x44	IV3_ADC_OFFSET	IV3_ADC_OFFSET	Go
0x4B	TEMP_IV_MASK	TEMP_IV_MASK	Go
0x4C	EXT_VOL0_HIGH	EXT_VOL0_HIGH	Go
0x4D	EXT_VOL0_LOW	EXT_VOL0_LOW	Go
0x4E	EXT_VOL0_ADC_OFFSET	EXT_VOL0_ADC_OFFSET	Go
0x4F	EXT_VOL1_HIGH	EXT_VOL1_HIGH	Go
0x50	EXT_VOL1_LOW	EXT_VOL1_LOW	Go
0x51	EXT_VOL1_ADC_OFFSET	EXT_VOL1_ADC_OFFSET	Go
0x52	EXT_VOL_MASK	EXT_VOL_MASK	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-844](#) shows the codes that are used for access types in this section.

**Table 7-844. Page\_14\_ADC\_Control Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

#### 7.6.2.11.1 ADC\_CLK\_DIV\_SEL Register (Address = 0x4) [Default = 0xD0]

ADC\_CLK\_DIV\_SEL is shown in [Table 7-845](#).

Return to the [Summary Table](#).

**Table 7-845. ADC\_CLK\_DIV\_SEL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:6	ADC_AVG_SEL	R/W	0x3	Moving Average Filter Selection 0x0= No avg 0x1= 2 samples 0x2= 4 samples 0x3= 8 samples (default)
5:4	ADC_CTRL_CLK_DIV	R/W	0x1	Clock Divider Selection 0x0= 25Mhz 0x1= 12.5 Mhz (default) 0x2= 8.33 Mhz 0x3= 6.25 Mhz
3:0	RESERVED	R	0x0	Reserved

#### 7.6.2.11.2 ADC\_INPUT\_EN\_LSB Register (Address = 0x7) [Default = 0x3D]

ADC\_INPUT\_EN\_LSB is shown in [Table 7-846](#).

Return to the [Summary Table](#).

**Table 7-846. ADC\_INPUT\_EN\_LSB Register Field Descriptions**

Bit	Field	Type	Default	Description
7	ADC_INPUT_EN_IV6	R/W	0x0	Enables for ADC reading IV6
6	ADC_INPUT_EN_IV5	R/W	0x0	Enables for ADC reading IV5
5	ADC_INPUT_EN_IV4	R/W	0x1	Enables for ADC reading IV4
4	ADC_INPUT_EN_IV3	R/W	0x1	Enables for ADC reading IV3
3	ADC_INPUT_EN_IV2	R/W	0x1	Enables for ADC reading IV2
2	ADC_INPUT_EN_IV1	R/W	0x1	Enables for ADC reading IV1
1	RESERVED	R/W	0x0	Reserved
0	ADC_INPUT_EN_TEMP	R/W	0x1	Enables for ADC reading temp sensor

**7.6.2.11.3 SAR\_ADC\_INPUT\_EN\_MSB Register (Address = 0x8) [Default = 0x00]**

SAR\_ADC\_INPUT\_EN\_MSB is shown in [Table 7-847](#).

Return to the [Summary Table](#).

**Table 7-847. SAR\_ADC\_INPUT\_EN\_MSB Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	ADC_INPUT_EN_LINE_FAULT3	R/W	0x0	Enables for ADC reading line fault 3
4	ADC_INPUT_EN_LINE_FAULT2	R/W	0x0	Enables for ADC reading line fault 2
3	ADC_INPUT_EN_LINE_FAULT1	R/W	0x0	Enables for ADC reading line fault 1
2	ADC_INPUT_EN_LINE_FAULT0	R/W	0x0	Enables for ADC reading line fault 0
1	ADC_INPUT_EN_EXT_V_OLO0	R/W	0x0	Enables for ADC reading external voltage 0
0	ADC_INPUT_EN_EXT_V_OLO1	R/W	0x0	Enables for ADC reading external voltage 1

**7.6.2.11.4 ADC\_MODE Register (Address = 0xD) [Default = 0x80]**

ADC\_MODE is shown in [Table 7-848](#).

Return to the [Summary Table](#).

**Table 7-848. ADC\_MODE Register Field Descriptions**

Bit	Field	Type	Default	Description
7	ADC_MODE	R/W	0x1	ADC Mode 0= Enabled 1= Disabled
6	RESERVED	R/W	0x0	Reserved
5:3	RESERVED	R/W	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

**7.6.2.11.5 TEMP\_FINAL Register (Address = 0x13) [Default = 0x00]**

TEMP\_FINAL is shown in [Table 7-849](#).

Return to the [Summary Table](#).

**Table 7-849. TEMP\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TEMP_FINAL	R	0x0	holds adc value for temp_final

**7.6.2.11.6 IV0\_FINAL Register (Address = 0x15) [Default = 0x00]**

IV0\_FINAL is shown in [Table 7-850](#).

Return to the [Summary Table](#).

**Table 7-850. IV0\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV0_FINAL	R	0x0	holds adc value for iv1_final (Refer to internal supply voltage sensing ) for debug purposes

**7.6.2.11.7 IV1\_FINAL Register (Address = 0x16) [Default = 0x00]**

IV1\_FINAL is shown in [Table 7-851](#).

Return to the [Summary Table](#).

**Table 7-851. IV1\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV1_FINAL	R	0x0	holds adc value for iv2_final (Refer to internal supply voltage sensing ) for debug purposes

**7.6.2.11.8 IV2\_FINAL Register (Address = 0x17) [Default = 0x00]**

IV2\_FINAL is shown in [Table 7-852](#).

Return to the [Summary Table](#).

**Table 7-852. IV2\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV2_FINAL	R	0x0	holds adc value for iv3_final (Refer to internal supply voltage sensing ) for debug purposes

**7.6.2.11.9 IV3\_FINAL Register (Address = 0x18) [Default = 0x00]**

IV3\_FINAL is shown in [Table 7-853](#).

Return to the [Summary Table](#).

**Table 7-853. IV3\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV3_FINAL	R	0x0	holds adc value for iv4_final (Refer to internal supply voltage sensing ) for debug purposes

**7.6.2.11.10 EXT\_VOL0\_FINAL Register (Address = 0x1B) [Default = 0x00]**

EXT\_VOL0\_FINAL is shown in [Table 7-854](#).

Return to the [Summary Table](#).

**Table 7-854. EXT\_VOL0\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_FINAL	R	0x0	holds adc value for ext_vol0_final (Refer to External Voltage Sensing) for debug purposes

**7.6.2.11.11 EXT\_VOL1\_FINAL Register (Address = 0x1C) [Default = 0x00]**

EXT\_VOL1\_FINAL is shown in [Table 7-855](#).

Return to the [Summary Table](#).

**Table 7-855. EXT\_VOL1\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_FINAL	R	0x0	holds adc value for ext_vol1_final (Refer to External Voltage Sensing) for debug purposes

**7.6.2.11.12 LINE\_FAULT0\_FINAL Register (Address = 0x1D) [Default = 0x00]**

LINE\_FAULT0\_FINAL is shown in [Table 7-856](#).

Return to the [Summary Table](#).

**Table 7-856. LINE\_FAULT0\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_FINAL	R	0x0	holds adc value for line_fault0_final (Refer to Serial Link Fault Detect) for debug purposes

**7.6.2.11.13 LINE\_FAULT1\_FINAL Register (Address = 0x1E) [Default = 0x00]**

LINE\_FAULT1\_FINAL is shown in [Table 7-857](#).

Return to the [Summary Table](#).

**Table 7-857. LINE\_FAULT1\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_FINAL	R	0x0	holds adc value for line_fault1_final (Refer to Serial Link Fault Detect) for debug purposes

**7.6.2.11.14 LINE\_FAULT2\_FINAL Register (Address = 0x1F) [Default = 0x00]**

LINE\_FAULT2\_FINAL is shown in [Table 7-858](#).

Return to the [Summary Table](#).

**Table 7-858. LINE\_FAULT2\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_FINAL	R	0x0	holds adc value for line_fault2_final (Refer to Serial Link Fault Detect) for debug purposes

**7.6.2.11.15 LINE\_FAULT3\_FINAL Register (Address = 0x20) [Default = 0x00]**LINE\_FAULT3\_FINAL is shown in [Table 7-859](#).Return to the [Summary Table](#).**Table 7-859. LINE\_FAULT3\_FINAL Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_FINAL	R	0x0	holds adc value for line_fault3_final (Refer to Serial Link Fault Detect) for debug purposes

**7.6.2.11.16 INT\_STATUS\_LSB\_LOW Register (Address = 0x23) [Default = 0x00]**INT\_STATUS\_LSB\_LOW is shown in [Table 7-860](#).Return to the [Summary Table](#).**Table 7-860. INT\_STATUS\_LSB\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R	0x0	
5	INT_STATUS_LOW_IV4	RC	0x0	Interrupt status for IV4 if the value is below the set threshold
4	INT_STATUS_LOW_IV3	RC	0x0	Interrupt status for IV3 if the value is below the set threshold
3	INT_STATUS_LOW_IV2	RC	0x0	Interrupt status for IV2 if the value is below the set threshold
2	INT_STATUS_LOW_IV1	RC	0x0	Interrupt status for IV1 if the value is below the set threshold
1	RESERVED	R	0x0	
0	INT_STATUS_LOW_TEM P	RC	0x0	Interrupt status for temperature if the value is below the set threshold

**7.6.2.11.17 INT\_STATUS\_MSB\_LOW Register (Address = 0x24) [Default = 0x00]**INT\_STATUS\_MSB\_LOW is shown in [Table 7-861](#).Return to the [Summary Table](#).**Table 7-861. INT\_STATUS\_MSB\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	
6	RESERVED	R	0x0	
5	RESERVED	R	0x0	Interrupt status for IV4 if the value is below the set threshold
4	RESERVED	R	0x0	Interrupt status for IV3 if the value is below the set threshold
3	RESERVED	R	0x0	Interrupt status for IV2 if the value is below the set threshold
2	RESERVED	R	0x0	Interrupt status for IV1 if the value is below the set threshold
1	INT_STATUS_EXT_VOL1	RC	0x0	Interrupt status for external voltage 1 if the value is below the set threshold
0	INT_STATUS_EXT_VOL0	RC	0x0	Interrupt status for external voltage 0 if the value is below the set threshold

**7.6.2.11.18 INT\_STATUS\_LSB\_HIGH Register (Address = 0x25) [Default = 0x00]**INT\_STATUS\_LSB\_HIGH is shown in [Table 7-862](#).Return to the [Summary Table](#).

**Table 7-862. INT\_STATUS\_LSB\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7	INT_STATUS_HIGH_IV6	RC	0x0	Interrupt status for IV6 if the value is above the set threshold
6	INT_STATUS_HIGH_IV5	RC	0x0	Interrupt status for IV5 if the value is above the set threshold
5	INT_STATUS_HIGH_IV4	RC	0x0	Interrupt status for IV4 if the value is above the set threshold
4	INT_STATUS_HIGH_IV3	RC	0x0	Interrupt status for IV3 if the value is above the set threshold
3	INT_STATUS_HIGH_IV2	RC	0x0	Interrupt status for IV2 if the value is above the set threshold
2	INT_STATUS_HIGH_IV1	RC	0x0	Interrupt status for IV1 if the value is above the set threshold
1	RESERVED	RC	0x0	Reserved
0	INT_STATUS_HIGH_TEM_P	RC	0x0	Interrupt status for temprature if the value is above the set threshold

**7.6.2.11.19 INT\_STATUS\_MSB\_HIGH Register (Address = 0x26) [Default = 0x00]**INT\_STATUS\_MSB\_HIGH is shown in [Table 7-863](#).Return to the [Summary Table](#).**Table 7-863. INT\_STATUS\_MSB\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	INT_STATUS_HIGH_EXT_VOL1	RC	0x0	Interrupt status for ext_vol1 if the value is above the set threshold
0	INT_STATUS_HIGH_EXT_VOL0	RC	0x0	Interrupt status for ext_vol0 if the value is above the set threshold

**7.6.2.11.20 INT\_LINE\_FAULT0\_M0 Register (Address = 0x27) [Default = 0x00]**INT\_LINE\_FAULT0\_M0 is shown in [Table 7-864](#).Return to the [Summary Table](#).**Table 7-864. INT\_LINE\_FAULT0\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	SHORT_TO_3_3_0_M0	RC	0x0	Interrupt status for line_fault0 short to 3.3V
3	SHORT_TO_1_8_0_M0	RC	0x0	Interrupt status for line_fault0 short to 1.8V
2	SHORT_TO_1_15_0_M0	RC	0x0	Interrupt status for line_fault0 short to 1.15V
1	NORMAL_OP_0_M0	RC	0x0	Interrupt status for line_fault0 Normal operation
0	SHORT_TO_GND_0_M0	RC	0x0	Interrupt status for line_fault0 short to ground

### 7.6.2.11.21 INT\_LINE\_FAULT1\_M0 Register (Address = 0x28) [Default = 0x00]

INT\_LINE\_FAULT1\_M0 is shown in [Table 7-865](#).

Return to the [Summary Table](#).

**Table 7-865. INT\_LINE\_FAULT1\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RESERVED	RC	0x0	Reserved
5	RESERVED	RC	0x0	Reserved
4	SHORT_TO_3_3_1_M0	RC	0x0	Interrupt status for line_fault1 short to 3.3V
3	SHORT_TO_1_8_1_M0	RC	0x0	Interrupt status for line_fault1 short to 1.8V
2	SHORT_TO_1_15_1_M0	RC	0x0	Interrupt status for line_fault1 short to 1.15V
1	NORMAL_OP_1_M0	RC	0x0	Interrupt status for line_fault1 Normal operation
0	SHORT_TO_GND_1_M0	RC	0x0	Interrupt status for line_fault1 short to ground

### 7.6.2.11.22 INT\_LINE\_FAULT2\_M0 Register (Address = 0x29) [Default = 0x00]

INT\_LINE\_FAULT2\_M0 is shown in [Table 7-866](#).

Return to the [Summary Table](#).

**Table 7-866. INT\_LINE\_FAULT2\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RESERVED	RC	0x0	Reserved
5	RESERVED	RC	0x0	Reserved
4	SHORT_TO_3_3_2_M0	RC	0x0	Interrupt status for line_fault2 short to 3.3V
3	SHORT_TO_1_8_2_M0	RC	0x0	Interrupt status for line_fault2 short to 1.8V
2	SHORT_TO_1_15_2_M0	RC	0x0	Interrupt status for line_fault2 short to 1.15V
1	NORMAL_OP_2_M0	RC	0x0	Interrupt status for line_fault2 Normal operation
0	SHORT_TO_GND_2_M0	RC	0x0	Interrupt status for line_fault2 short to ground

### 7.6.2.11.23 INT\_LINE\_FAULT3\_M0 Register (Address = 0x2A) [Default = 0x00]

INT\_LINE\_FAULT3\_M0 is shown in [Table 7-867](#).

Return to the [Summary Table](#).

**Table 7-867. INT\_LINE\_FAULT3\_M0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RESERVED	RC	0x0	Reserved
5	RESERVED	RC	0x0	Reserved

**Table 7-867. INT\_LINE\_FAULT3\_M0 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
4	SHORT_TO_3_3_3_M0	RC	0x0	Interrupt status for line_fault3 short to 3.3V
3	SHORT_TO_1_8_3_M0	RC	0x0	Interrupt status for line_fault3 short to 1.8V
2	SHORT_TO_1_15_3_M0	RC	0x0	Interrupt status for line_fault3 short to 1.15V
1	NORMAL_OP_3_M0	RC	0x0	Interrupt status for line_fault3 Normal operation
0	SHORT_TO_GND_3_M0	RC	0x0	Interrupt status for line_fault3 short to ground

**7.6.2.11.24 INT\_LINE\_FAULT0\_M1 Register (Address = 0x2B) [Default = 0x00]**INT\_LINE\_FAULT0\_M1 is shown in [Table 7-868](#).Return to the [Summary Table](#).**Table 7-868. INT\_LINE\_FAULT0\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RESERVED	RC	0x0	Reserved
5	RESERVED	RC	0x0	Reserved
4	SHORT_TO_3_3_0_M1	RC	0x0	Interrupt status for line_fault0 short to 3.3V
3	SHORT_TO_1_8_0_M1	RC	0x0	Interrupt status for line_fault0 short to 1.8V
2	SHORT_TO_1_15_0_M1	RC	0x0	Interrupt status for line_fault0 short to 1.15V
1	NORMAL_OP_0_M1	RC	0x0	Interrupt status for line_fault0 Normal operation
0	SHORT_TO_GND_0_M1	RC	0x0	Interrupt status for line_fault0 short to ground

**7.6.2.11.25 INT\_LINE\_FAULT1\_M1 Register (Address = 0x2C) [Default = 0x00]**INT\_LINE\_FAULT1\_M1 is shown in [Table 7-869](#).Return to the [Summary Table](#).**Table 7-869. INT\_LINE\_FAULT1\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RESERVED	RC	0x0	Reserved
5	RESERVED	RC	0x0	Reserved
4	SHORT_TO_3_3_1_M1	RC	0x0	Interrupt status for line_fault1 short to 3.3V
3	SHORT_TO_1_8_1_M1	RC	0x0	Interrupt status for line_fault1 short to 1.8V
2	SHORT_TO_1_15_1_M1	RC	0x0	Interrupt status for line_fault1 short to 1.15V
1	NORMAL_OP_1_M1	RC	0x0	Interrupt status for line_fault1 Normal operation

**Table 7-869. INT\_LINE\_FAULT1\_M1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
0	SHORT_TO_GND_1_M1	RC	0x0	Interrupt status for line_fault1 short to ground

**7.6.2.11.26 INT\_LINE\_FAULT2\_M1 Register (Address = 0x2D) [Default = 0x00]**INT\_LINE\_FAULT2\_M1 is shown in [Table 7-870](#).Return to the [Summary Table](#).**Table 7-870. INT\_LINE\_FAULT2\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RESERVED	RC	0x0	Reserved
5	RESERVED	RC	0x0	Reserved
4	SHORT_TO_3_3_2_M1	RC	0x0	Interrupt status for line_fault2 short to 3.3V
3	SHORT_TO_1_8_2_M1	RC	0x0	Interrupt status for line_fault2 short to 1.8V
2	SHORT_TO_1_15_2_M1	RC	0x0	Interrupt status for line_fault2 short to 1.15V
1	NORMAL_OP_2_M1	RC	0x0	Interrupt status for line_fault2 Normal operation
0	SHORT_TO_GND_2_M1	RC	0x0	Interrupt status for line_fault2 short to ground

**7.6.2.11.27 INT\_LINE\_FAULT3\_M1 Register (Address = 0x2E) [Default = 0x00]**INT\_LINE\_FAULT3\_M1 is shown in [Table 7-871](#).Return to the [Summary Table](#).**Table 7-871. INT\_LINE\_FAULT3\_M1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RESERVED	RC	0x0	Reserved
5	RESERVED	RC	0x0	Reserved
4	SHORT_TO_3_3_3_M1	RC	0x0	Interrupt status for line_fault3 short to 3.3V
3	SHORT_TO_1_8_3_M1	RC	0x0	Interrupt status for line_fault3 short to 1.8V
2	SHORT_TO_1_15_3_M1	RC	0x0	Interrupt status for line_fault3 short to 1.15V
1	NORMAL_OP_3_M1	RC	0x0	Interrupt status for line_fault3 Normal operation
0	SHORT_TO_GND_3_M1	RC	0x0	Interrupt status for line_fault3 short to ground

**7.6.2.11.28 INT\_LINE\_FAULT\_UNDEF Register (Address = 0x2F) [Default = 0x00]**INT\_LINE\_FAULT\_UNDEF is shown in [Table 7-872](#).Return to the [Summary Table](#).

**Table 7-872. INT\_LINE\_FAULT\_UNDEF Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	INT_LINE_FAULT_UNDE F_M1	RC	0x0	Interrupt status to signal adc value in undefined threshold range for mode 1 0 - line fault 0 1 - line fault 1 2 - line fault 2 3 - line fault 3
3:0	INT_LINE_FAULT_UNDE F_M0	RC	0x0	Interrupt status to signal adc value in undefined threshold range for mode 0 0 - line fault 0 1 - line fault 1 2 - line fault 2 3 - line fault 3

**7.6.2.11.29 INT\_LINE\_FAULT\_SATURATE Register (Address = 0x30) [Default = 0x00]**INT\_LINE\_FAULT\_SATURATE is shown in [Table 7-873](#).Return to the [Summary Table](#).**Table 7-873. INT\_LINE\_FAULT\_SATURATE Register Field Descriptions**

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	INT_LINE_FAULT3_SATU RATE	RC	0x0	Indicates the ADC code for Line Fault Detection is saturated and the voltage sensed is beyond the ADC range
2	INT_LINE_FAULT2_SATU RATE	RC	0x0	Indicates the ADC code for Line Fault Detection is saturated and the voltage sensed is beyond the ADC range
1	INT_LINE_FAULT1_SATU RATE	RC	0x0	Indicates the ADC code for Line Fault Detection is saturated and the voltage sensed is beyond the ADC range
0	INT_LINE_FAULT0_SATU RATE	RC	0x0	Indicates the ADC code for Line Fault Detection is saturated and the voltage sensed is beyond the ADC range

**7.6.2.11.30 TEMP\_HIGH Register (Address = 0x33) [Default = 0xCE]**TEMP\_HIGH is shown in [Table 7-874](#).Return to the [Summary Table](#).**Table 7-874. TEMP\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TEMP_HIGH	R/W	0xCE	Upper threshold for the Die Temperature

**7.6.2.11.31 TEMP\_LOW Register (Address = 0x34) [Default = 0x7E]**TEMP\_LOW is shown in [Table 7-875](#).Return to the [Summary Table](#).**Table 7-875. TEMP\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TEMP_LOW	R/W	0x7E	Lower threshold for the Die Temperature

**7.6.2.11.32 TEMP\_ADC\_OFFSET Register (Address = 0x35) [Default = 0x00]**TEMP\_ADC\_OFFSET is shown in [Table 7-876](#).

Return to the [Summary Table](#).

**Table 7-876. TEMP\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	TEMP_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

**7.6.2.11.33 IV0\_HIGH Register (Address = 0x39) [Default = 0x86]**

IV0\_HIGH is shown in [Table 7-877](#).

Return to the [Summary Table](#).

**Table 7-877. IV0\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV0_HIGH	R/W	0x86	Upper threshold for iv0

**7.6.2.11.34 IV0\_LOW Register (Address = 0x3A) [Default = 0x7A]**

IV0\_LOW is shown in [Table 7-878](#).

Return to the [Summary Table](#).

**Table 7-878. IV0\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV0_LOW	R/W	0x7A	Lower threshold for iv0

**7.6.2.11.35 IV0\_ADC\_OFFSET Register (Address = 0x3B) [Default = 0x00]**

IV0\_ADC\_OFFSET is shown in [Table 7-879](#).

Return to the [Summary Table](#).

**Table 7-879. IV0\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV0_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

**7.6.2.11.36 IV1\_HIGH Register (Address = 0x3C) [Default = 0x86]**

IV1\_HIGH is shown in [Table 7-880](#).

Return to the [Summary Table](#).

**Table 7-880. IV1\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV1_HIGH	R/W	0x86	Upper threshold for iv1

**7.6.2.11.37 IV1\_LOW Register (Address = 0x3D) [Default = 0x7A]**

IV1\_LOW is shown in [Table 7-881](#).

Return to the [Summary Table](#).

**Table 7-881. IV1\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV1_LOW	R/W	0x7A	Lower threshold for iv1

**7.6.2.11.38 IV1\_ADC\_OFFSET Register (Address = 0x3E) [Default = 0x00]**IV1\_ADC\_OFFSET is shown in [Table 7-882](#).Return to the [Summary Table](#).**Table 7-882. IV1\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV1_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

**7.6.2.11.39 IV2\_HIGH Register (Address = 0x3F) [Default = 0x86]**IV2\_HIGH is shown in [Table 7-883](#).Return to the [Summary Table](#).**Table 7-883. IV2\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV2_HIGH	R/W	0x86	Upper threshold for iv2

**7.6.2.11.40 IV2\_LOW Register (Address = 0x40) [Default = 0x7A]**IV2\_LOW is shown in [Table 7-884](#).Return to the [Summary Table](#).**Table 7-884. IV2\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV2_LOW	R/W	0x7A	Lower threshold for iv2

**7.6.2.11.41 IV2\_ADC\_OFFSET Register (Address = 0x41) [Default = 0x00]**IV2\_ADC\_OFFSET is shown in [Table 7-885](#).Return to the [Summary Table](#).**Table 7-885. IV2\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV2_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

**7.6.2.11.42 IV3\_HIGH Register (Address = 0x42) [Default = 0x86]**IV3\_HIGH is shown in [Table 7-886](#).Return to the [Summary Table](#).**Table 7-886. IV3\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV3_HIGH	R/W	0x86	Upper threshold for iv3

**7.6.2.11.43 IV3\_LOW Register (Address = 0x43) [Default = 0x7A]**IV3\_LOW is shown in [Table 7-887](#).Return to the [Summary Table](#).**Table 7-887. IV3\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV3_LOW	R/W	0x7A	Lower threshold for iv3

**7.6.2.11.44 IV3\_ADC\_OFFSET Register (Address = 0x44) [Default = 0x00]**IV3\_ADC\_OFFSET is shown in [Table 7-888](#).Return to the [Summary Table](#).**Table 7-888. IV3\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	IV3_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

**7.6.2.11.45 TEMP\_IV\_MASK Register (Address = 0x4B) [Default = 0xC2]**TEMP\_IV\_MASK is shown in [Table 7-889](#).Return to the [Summary Table](#).**Table 7-889. TEMP\_IV\_MASK Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x1	Reserved
5	IV3_THRESH_MASK	R/W	0x0	iv3_thresh_mask
4	IV2_THRESH_MASK	R/W	0x0	iv2_thresh_mask
3	IV1_THRESH_MASK	R/W	0x0	iv1_thresh_mask
2	IV0_THRESH_MASK	R/W	0x0	iv0_thresh_mask
1	RESERVED	R/W	0x1	Reserved
0	TEMP_THRESH_MASK	R/W	0x0	temp_thresh_mask

**7.6.2.11.46 EXT\_VOL0\_HIGH Register (Address = 0x4C) [Default = 0x00]**EXT\_VOL0\_HIGH is shown in [Table 7-890](#).Return to the [Summary Table](#).**Table 7-890. EXT\_VOL0\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_HIGH	R/W	0x0	Upper threshold for ext_volt0

**7.6.2.11.47 EXT\_VOL0\_LOW Register (Address = 0x4D) [Default = 0x00]**EXT\_VOL0\_LOW is shown in [Table 7-891](#).Return to the [Summary Table](#).

**Table 7-891. EXT\_VOL0\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_LOW	R/W	0x0	Lower threshold for ext_vol0

**7.6.2.11.48 EXT\_VOL0\_ADC\_OFFSET Register (Address = 0x4E) [Default = 0x00]**EXT\_VOL0\_ADC\_OFFSET is shown in [Table 7-892](#).Return to the [Summary Table](#).**Table 7-892. EXT\_VOL0\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

**7.6.2.11.49 EXT\_VOL1\_HIGH Register (Address = 0x4F) [Default = 0x00]**EXT\_VOL1\_HIGH is shown in [Table 7-893](#).Return to the [Summary Table](#).**Table 7-893. EXT\_VOL1\_HIGH Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_HIGH	R/W	0x0	Upper threshold for ext_vol1

**7.6.2.11.50 EXT\_VOL1\_LOW Register (Address = 0x50) [Default = 0x00]**EXT\_VOL1\_LOW is shown in [Table 7-894](#).Return to the [Summary Table](#).**Table 7-894. EXT\_VOL1\_LOW Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_LOW	R/W	0x0	Lower threshold for ext_vol1

**7.6.2.11.51 EXT\_VOL1\_ADC\_OFFSET Register (Address = 0x51) [Default = 0x00]**EXT\_VOL1\_ADC\_OFFSET is shown in [Table 7-895](#).Return to the [Summary Table](#).**Table 7-895. EXT\_VOL1\_ADC\_OFFSET Register Field Descriptions**

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_ADC_OFFSET	R/W	0x0	Offset added to the final ADC code after the conversion.

**7.6.2.11.52 EXT\_VOL\_MASK Register (Address = 0x52) [Default = 0x00]**EXT\_VOL\_MASK is shown in [Table 7-896](#).Return to the [Summary Table](#).**Table 7-896. EXT\_VOL\_MASK Register Field Descriptions**

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved

**Table 7-896. EXT\_VOL\_MASK Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
1	EXT_VOL1_THRESH_MASK	R/W	0x0	ext_vol1_thresh_mask
0	EXT_VOL0_THRESH_MASK	R/W	0x0	ext_vol0_thresh_mask

### 7.6.3 Pattern Generator Registers

The pattern generator registers are accessed indirectly using the PGIA and PGID registers on the main register page or the FPD4\_PGIA\_VPx and FPD4\_PGID\_VPx registers on Page\_12. There are six copies of these registers, one for each FPD-Link Port on the page (0x66-0x67), and one for each video processor on Page\_12 (0x2A-0x2B, 0x6A-0x6B, 0xAA-0xAB, and 0xEA-0xEB).

This indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the PGIA register to set the register offset
2. Write the data value to the PGID register

If auto-increment is set in the PGIA register, repeating Step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the PGIA register to set the register offset
2. Read from the PGID register

If auto-increment is set in the PGIA register, repeating Step 3 will read additional data bytes from subsequent register offset locations.

#### 7.6.3.1 PATGEN Registers

[Table 7-897](#) lists the PATGEN registers. All register offset addresses not listed in [Table 7-897](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-897. PATGEN Registers**

Address	Acronym	Register Name	Section
0x0	PGRS1	PGRS1	<a href="#">Go</a>
0x1	PGRS2	PGRS2	<a href="#">Go</a>
0x2	PGGS1	PGGS1	<a href="#">Go</a>
0x3	PGGS2	PGGS2	<a href="#">Go</a>
0x4	PGBS1	PGBS1	<a href="#">Go</a>
0x5	PGBS2	PGBS2	<a href="#">Go</a>
0x6	PGTFS1	PGTFS1	<a href="#">Go</a>
0x7	PGTFS2	PGTFS2	<a href="#">Go</a>
0x8	PGTFS3	PGTFS3	<a href="#">Go</a>
0x9	PGTFS4	PGTFS4	<a href="#">Go</a>
0xA	PGAFS1	PGAFS1	<a href="#">Go</a>
0xB	PGAFS2	PGAFS2	<a href="#">Go</a>
0xC	PGAFS3	PGAFS3	<a href="#">Go</a>
0xD	PGAFS4	PGAFS4	<a href="#">Go</a>
0xE	PGHSW1	PGHSW1	<a href="#">Go</a>
0xF	PGHSW2	PGHSW2	<a href="#">Go</a>
0x10	PGVSW1	PGVSW1	<a href="#">Go</a>
0x11	PGVSW2	PGVSW2	<a href="#">Go</a>
0x12	PGHBP1	PGHBP1	<a href="#">Go</a>
0x13	PGHBP2	PGHBP2	<a href="#">Go</a>
0x14	PGVBP1	PGVBP1	<a href="#">Go</a>
0x15	PGVBP2	PGVBP2	<a href="#">Go</a>

**Table 7-897. PATGEN Registers (continued)**

Address	Acronym	Register Name	Section
0x16	PBSC	PBSC	<a href="#">Go</a>
0x17	PGFT	PGFT	<a href="#">Go</a>
0x18	PGTSC	PGTSC	<a href="#">Go</a>
0x19	PGTSO1	PGTSO1	<a href="#">Go</a>
0x1A	PGTSO2	PGTSO2	<a href="#">Go</a>
0x1B	PGTSO3	PGTSO3	<a href="#">Go</a>
0x1C	PGTSO4	PGTSO4	<a href="#">Go</a>
0x1D	PGTSO5	PGTSO5	<a href="#">Go</a>
0x1E	PGTSO6	PGTSO6	<a href="#">Go</a>
0x1F	PGTSO7	PGTSO7	<a href="#">Go</a>
0x20	PGTSO8	PGTSO8	<a href="#">Go</a>
0x21	PGTSO9	PGTSO9	<a href="#">Go</a>
0x22	PGTSO10	PGTSO10	<a href="#">Go</a>
0x23	PGTSO11	PGTSO11	<a href="#">Go</a>
0x24	PGTSO12	PGTSO12	<a href="#">Go</a>
0x25	PGTSO13	PGTSO13	<a href="#">Go</a>
0x26	PGTSO14	PGTSO14	<a href="#">Go</a>
0x27	PGTSO15	PGTSO15	<a href="#">Go</a>
0x28	PGTSO16	PGTSO16	<a href="#">Go</a>
0x29	PGBE	PGBE	<a href="#">Go</a>
0x2A	PGUPS	PGUPS	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. [Table 7-898](#) shows the codes that are used for access types in this section.

**Table 7-898. PATGEN Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

#### 7.6.3.1.1 PGRS1 Register (Address = 0x0) [reset = 0x0]

PGRS1 is shown in [Table 7-899](#).

Return to the [Summary Table](#).

**Table 7-899. PGRS1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_RSP	R/W	0x0	Red Sub-Pixel: This field is the 8 least significant bits of the Red sub-pixel for the custom color.

### 7.6.3.1.2 PGRS2 Register (Address = 0x1) [reset = 0x0]

PGRS2 is shown in [Table 7-900](#).

Return to the [Summary Table](#).

**Table 7-900. PGRS2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1-0	PATGEN_RSP	R/W	0x0	Red Sub-Pixel: This field is the most significant bits of the Red sub-pixel for the custom color.

### 7.6.3.1.3 PGGS1 Register (Address = 0x2) [reset = 0x0]

PGGS1 is shown in [Table 7-901](#).

Return to the [Summary Table](#).

**Table 7-901. PGGS1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_GSP	R/W	0x0	Green Sub-Pixel: This field is the 8 least significant bits of the Green sub-pixel for the custom color.

### 7.6.3.1.4 PGGS2 Register (Address = 0x3) [reset = 0x0]

PGGS2 is shown in [Table 7-902](#).

Return to the [Summary Table](#).

**Table 7-902. PGGS2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved
1-0	RESERVED	R	0x0	Reserved

### 7.6.3.1.5 PGBS1 Register (Address = 0x4) [reset = 0x0]

PGBS1 is shown in [Table 7-903](#).

Return to the [Summary Table](#).

**Table 7-903. PGBS1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_BSP	R/W	0x0	Blue Sub-Pixel: This field is the 8 least significant bits of the Blue sub-pixel for the custom color.

### 7.6.3.1.6 PGBS2 Register (Address = 0x5) [reset = 0x0]

PGBS2 is shown in [Table 7-904](#).

Return to the [Summary Table](#).

**Table 7-904. PGBS2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved

**Table 7-904. PGBS2 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
1-0	PATGEN_BSP	R/W	0x0	Blue Sub-Pixel: This field is the most significant bits of the Blue sub-pixel for the custom color.

**7.6.3.1.7 PGTFS1 Register (Address = 0x6) [reset = 0x98]**PGTFS1 is shown in [Table 7-905](#).Return to the [Summary Table](#).**Table 7-905. PGTFS1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_THW	R/W	0x98	Total Horizontal Width: This field is the 8 least significant bits of the 16-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

**7.6.3.1.8 PGTFS2 Register (Address = 0x7) [reset = 0x8]**PGTFS2 is shown in [Table 7-906](#).Return to the [Summary Table](#).**Table 7-906. PGTFS2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3-0	PATGEN_THW	R/W	0x8	Total Horizontal Width: This field is the 8 most significant bits of the 16-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

**7.6.3.1.9 PGTFS3 Register (Address = 0x8) [reset = 0x65]**PGTFS3 is shown in [Table 7-907](#).Return to the [Summary Table](#).**Table 7-907. PGTFS3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_TVW	R/W	0x65	Total Vertical Width: This field is the 8 least significant bits of the 16-bit Total Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

**7.6.3.1.10 PGTFS4 Register (Address = 0x9) [reset = 0x4]**PGTFS4 is shown in [Table 7-908](#).Return to the [Summary Table](#).**Table 7-908. PGTFS4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_TVW	R/W	0x4	Total Vertical Width: This field is the 8 most significant bits of the 16-bit Total Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

### 7.6.3.1.11 PGAFS1 Register (Address = 0xA) [reset = 0x80]

PGAFS1 is shown in [Table 7-909](#).

Return to the [Summary Table](#).

**Table 7-909. PGAFS1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_AHW	R/W	0x80	Active Horizontal Width: This field is the 8 least significant bits of the 16-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

### 7.6.3.1.12 PGAFS2 Register (Address = 0xB) [reset = 0x7]

PGAFS2 is shown in [Table 7-910](#).

Return to the [Summary Table](#).

**Table 7-910. PGAFS2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
3-0	PATGEN_AHW	R/W	0x7	Active Horizontal Width: This field is the 8 most significant bits of the 16-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

### 7.6.3.1.13 PGAFS3 Register (Address = 0xC) [reset = 0x38]

PGAFS3 is shown in [Table 7-911](#).

Return to the [Summary Table](#).

**Table 7-911. PGAFS3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_AVW	R/W	0x38	Active Vertical Width: This field is the 8 least significant bits of the 16-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

### 7.6.3.1.14 PGAFS4 Register (Address = 0xD) [reset = 0x4]

PGAFS4 is shown in [Table 7-912](#).

Return to the [Summary Table](#).

**Table 7-912. PGAFS4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_AVW	R/W	0x4	Active Vertical Width: This field is the 8 most significant bits of the 16-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

### 7.6.3.1.15 PGHSW1 Register (Address = 0xE) [reset = 0x2C]

PGHSW1 is shown in [Table 7-913](#).

Return to the [Summary Table](#).

**Table 7-913. PGHSW1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_HSW	R/W	0x2C	Horizontal Sync Width: This field controls the 8 least significant bits of the 12-bit Horizontal Sync pulse, in units of pixels. This field should only be written when the pattern generator is disabled.

**7.6.3.1.16 PGHSW2 Register (Address = 0xF) [reset = 0x0]**PGHSW2 is shown in [Table 7-914](#).Return to the [Summary Table](#).**Table 7-914. PGHSW2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	PATGEN_HSW	R/W	0x0	Horizontal Sync Width: This field controls the 4 most significant bits of the 12-bit Horizontal Sync pulse, in units of pixels. This field should only be written when the pattern generator is disabled.

**7.6.3.1.17 PGVSW1 Register (Address = 0x10) [reset = 0x5]**PGVSW1 is shown in [Table 7-915](#).Return to the [Summary Table](#).**Table 7-915. PGVSW1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_VSW	R/W	0x5	Vertical Sync Width: This field controls the 8 least significant bits of the 12-bit Vertical Sync pulse, in units of lines. This field should only be written when the pattern generator is disabled.

**7.6.3.1.18 PGVSW2 Register (Address = 0x11) [reset = 0x0]**PGVSW2 is shown in [Table 7-916](#).Return to the [Summary Table](#).**Table 7-916. PGVSW2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	PATGEN_VSW	R/W	0x0	Vertical Sync Width: This field controls the 4 most significant bits of the 12-bit Vertical Sync pulse, in units of lines. This field should only be written when the pattern generator is disabled.

**7.6.3.1.19 PGHBP1 Register (Address = 0x12) [reset = 0x94]**PGHBP1 is shown in [Table 7-917](#).Return to the [Summary Table](#).

**Table 7-917. PGHBP1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_HBP	R/W	0x94	Horizontal Back Porch Width: This field controls the 8 least significant bits of the 12-bit Horizontal Back Porch, in units of pixels. This field should only be written when the pattern generator is disabled.

**7.6.3.1.20 PGHBP2 Register (Address = 0x13) [reset = 0x0]**PGHBP2 is shown in [Table 7-918](#).Return to the [Summary Table](#).**Table 7-918. PGHBP2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	PATGEN_HBP	R/W	0x0	Horizontal Back Porch Width: This field controls the 4 most significant bits of the 12-bit Horizontal Back Porch, in units of pixels. This field should only be written when the pattern generator is disabled.

**7.6.3.1.21 PGVBP1 Register (Address = 0x14) [reset = 0x24]**PGVBP1 is shown in [Table 7-919](#).Return to the [Summary Table](#).**Table 7-919. PGVBP1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_VBP	R/W	0x24	Vertical Back Porch Width: This field controls the 8 least significant bits of the 12-bit Vertical Back Porch, in units of lines. This field should only be written when the pattern generator is disabled.

**7.6.3.1.22 PGVBP2 Register (Address = 0x15) [reset = 0x0]**PGVBP2 is shown in [Table 7-920](#).Return to the [Summary Table](#).**Table 7-920. PGVBP2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	PATGEN_VBP	R/W	0x0	Vertical Back Porch Width: This field controls the 4 most significant bits of the 12-bit Vertical Back Porch, in units of lines. This field should only be written when the pattern generator is disabled.

**7.6.3.1.23 PBSC Register (Address = 0x16) [reset = 0x3]**PBSC is shown in [Table 7-921](#).Return to the [Summary Table](#).**Table 7-921. PBSC Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved

**Table 7-921. PBSC Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3	PATGEN_VS_DIS	R/W	0x0	Vertical Sync Disable: Disable Vertical Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
2	PATGEN_HS_DIS	R/W	0x0	Horizontal Sync Disable: Disable Horizontal Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
1	PATGEN_VS_POL	R/W	0x1	Vertical Sync Polarity: When 1, the pattern generator will invert the Vertical Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
0	PATGEN_HS_POL	R/W	0x1	Horizontal Sync Polarity: When 1, the pattern generator will invert the Horizontal Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled

**7.6.3.1.24 PGFT Register (Address = 0x17) [reset = 0x1E]**PGFT is shown in [Table 7-922](#).Return to the [Summary Table](#).**Table 7-922. PGFT Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_FTIME	R/W	0x1E	Frame Time: When Auto-Scrolling is enabled, this field controls the number of frames to display each pattern in increments of two frames. Valid register values are 1-255, giving a programmable range of even numbers between 2 and 510, inclusive.

**7.6.3.1.25 PGTSC Register (Address = 0x18) [reset = 0x10]**PGTSC is shown in [Table 7-923](#).Return to the [Summary Table](#).**Table 7-923. PGTSC Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TSLOT	R/W	0x10	Time Slots: This field configures the number of enabled time slots for Auto-Scrolling. Valid Values are 1-16

**7.6.3.1.26 PGTSO1 Register (Address = 0x19) [reset = 0x1]**PGTSO1 is shown in [Table 7-924](#).Return to the [Summary Table](#).**Table 7-924. PGTSO1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS1	R/W	0x1	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.27 PGTSO2 Register (Address = 0x1A) [reset = 0x2]**

PGTSO2 is shown in [Table 7-925](#).

Return to the [Summary Table](#).

**Table 7-925. PGTSO2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS2	R/W	0x2	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.28 PGTSO3 Register (Address = 0x1B) [reset = 0x3]**

PGTSO3 is shown in [Table 7-926](#).

Return to the [Summary Table](#).

**Table 7-926. PGTSO3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS3	R/W	0x3	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.29 PGTSO4 Register (Address = 0x1C) [reset = 0x4]**

PGTSO4 is shown in [Table 7-927](#).

Return to the [Summary Table](#).

**Table 7-927. PGTSO4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS4	R/W	0x4	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.30 PGTSO5 Register (Address = 0x1D) [reset = 0x5]**

PGTSO5 is shown in [Table 7-928](#).

Return to the [Summary Table](#).

**Table 7-928. PGTSO5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS5	R/W	0x5	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.31 PGTSo6 Register (Address = 0x1E) [reset = 0x6]**

PGTSo6 is shown in [Table 7-929](#).

Return to the [Summary Table](#).

**Table 7-929. PGTSo6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS6	R/W	0x6	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.32 PGTSo7 Register (Address = 0x1F) [reset = 0x7]**

PGTSo7 is shown in [Table 7-930](#).

Return to the [Summary Table](#).

**Table 7-930. PGTSo7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS7	R/W	0x7	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.33 PGTSo8 Register (Address = 0x20) [reset = 0x8]**

PGTSo8 is shown in [Table 7-931](#).

Return to the [Summary Table](#).

**Table 7-931. PGTSo8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS8	R/W	0x8	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.34 PGTSo9 Register (Address = 0x21) [reset = 0x9]**

PGTSo9 is shown in [Table 7-932](#).

Return to the [Summary Table](#).

**Table 7-932. PGTSo9 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS9	R/W	0x9	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.35 PGTSO10 Register (Address = 0x22) [reset = 0xA]**

PGTSO10 is shown in [Table 7-933](#).

Return to the [Summary Table](#).

**Table 7-933. PGTSO10 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS10	R/W	0xA	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.36 PGTSO11 Register (Address = 0x23) [reset = 0xB]**

PGTSO11 is shown in [Table 7-934](#).

Return to the [Summary Table](#).

**Table 7-934. PGTSO11 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS11	R/W	0xB	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.37 PGTSO12 Register (Address = 0x24) [reset = 0xC]**

PGTSO12 is shown in [Table 7-935](#).

Return to the [Summary Table](#).

**Table 7-935. PGTSO12 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS12	R/W	0xC	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.38 PGTSO13 Register (Address = 0x25) [reset = 0xD]**

PGTSO13 is shown in [Table 7-936](#).

Return to the [Summary Table](#).

**Table 7-936. PGTSO13 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS13	R/W	0xD	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.39 PGTSO14 Register (Address = 0x26) [reset = 0xE]**PGTSO14 is shown in [Table 7-937](#).Return to the [Summary Table](#).**Table 7-937. PGTSO14 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS14	R/W	0xE	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.40 PGTSO15 Register (Address = 0x27) [reset = 0xF]**PGTSO15 is shown in [Table 7-938](#).Return to the [Summary Table](#).**Table 7-938. PGTSO15 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS15	R/W	0xF	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.41 PGTSO16 Register (Address = 0x28) [reset = 0x10]**PGTSO16 is shown in [Table 7-939](#).Return to the [Summary Table](#).**Table 7-939. PGTSO16 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4-0	PATGEN_TS16	R/W	0x10	Time Slot Pattern: This field configures the pattern enabled in the selected Time Slot Order register. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field.

**7.6.3.1.42 PGBE Register (Address = 0x29) [reset = 0x0]**PGBE is shown in [Table 7-940](#).Return to the [Summary Table](#).**Table 7-940. PGBE Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PATGEN_CHK_ERRS	R	0x0	Pattern Checker Errors: This field indicates the number of errors encountered during pattern checking, up to a maximum of 255. The value is cleared upon read.

**7.6.3.1.43 PGUPS Register (Address = 0x2A) [reset = 0x0]**PGUPS is shown in [Table 7-941](#).

Return to the [Summary Table](#).

**Table 7-941. PGUPS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-1	PATGEN_UNH1S_SCALE	R/W	0x0	<p>Scale the divider for one-second mode of UNH compliance test pattern</p> <p>The 1-second duration is scaled by <math>2^N</math>, where N is the value of this field.</p> <ul style="list-style-type: none"> <li>000b= 1 second</li> <li>001b= 1/2 second</li> <li>010b= 1/4 second</li> <li>011b= 1/8 second</li> <li>100b= 1/16 second</li> <li>101b= 1/32 second</li> <li>110b= 1/64 second</li> <li>111b= 1/128 second</li> </ul>
0	PATGEN_UNH1S	R/W	0x0	<p>One-second mode of UNH compliance test pattern</p> <p>0b= the UNH compliance test pattern is sent out as defined in the timing control registers</p> <p>1b= Each line of the UNH compliance test pattern is sent out roughly 1 second apart.</p>

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

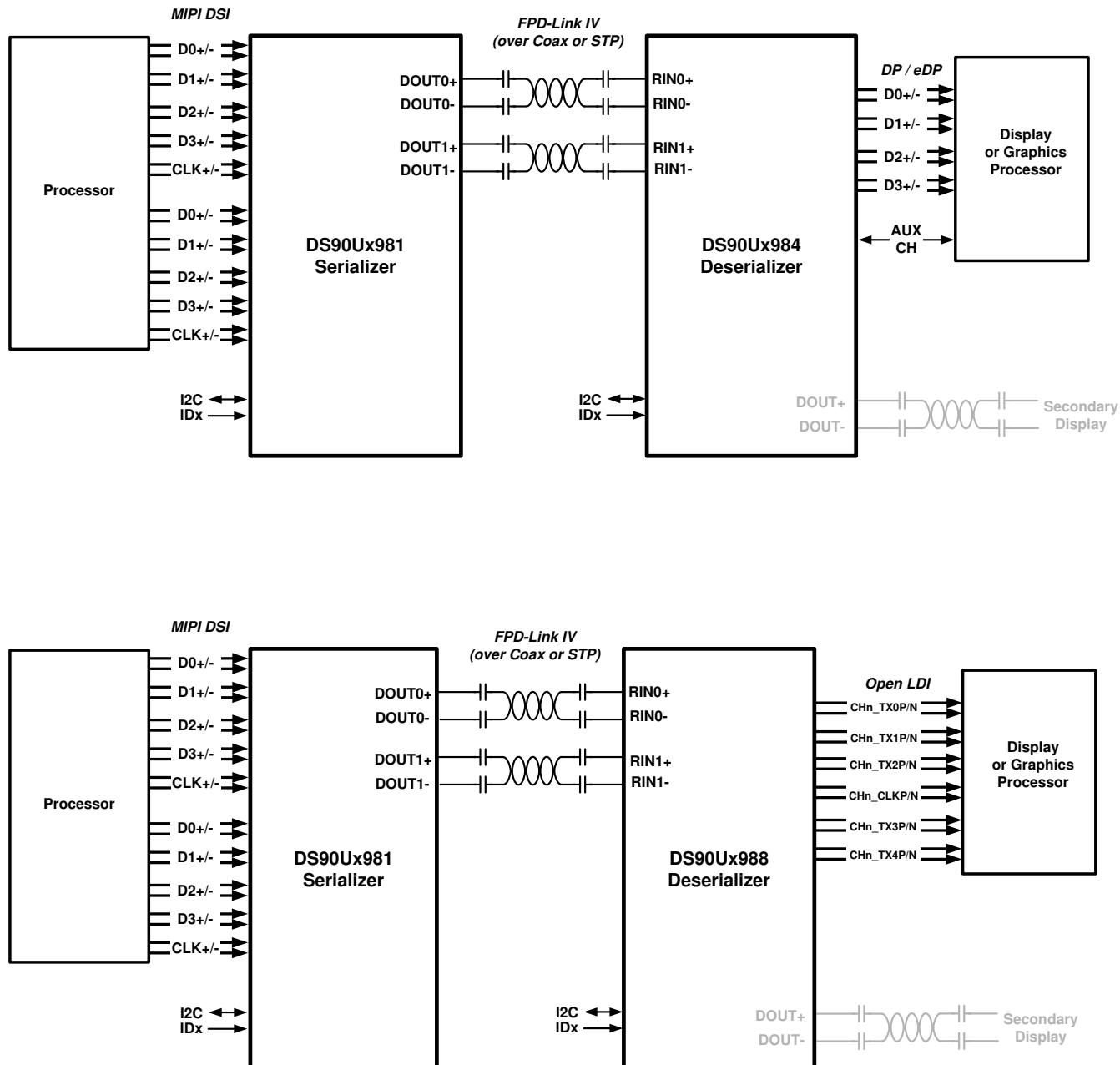
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### 8.1 Application Information

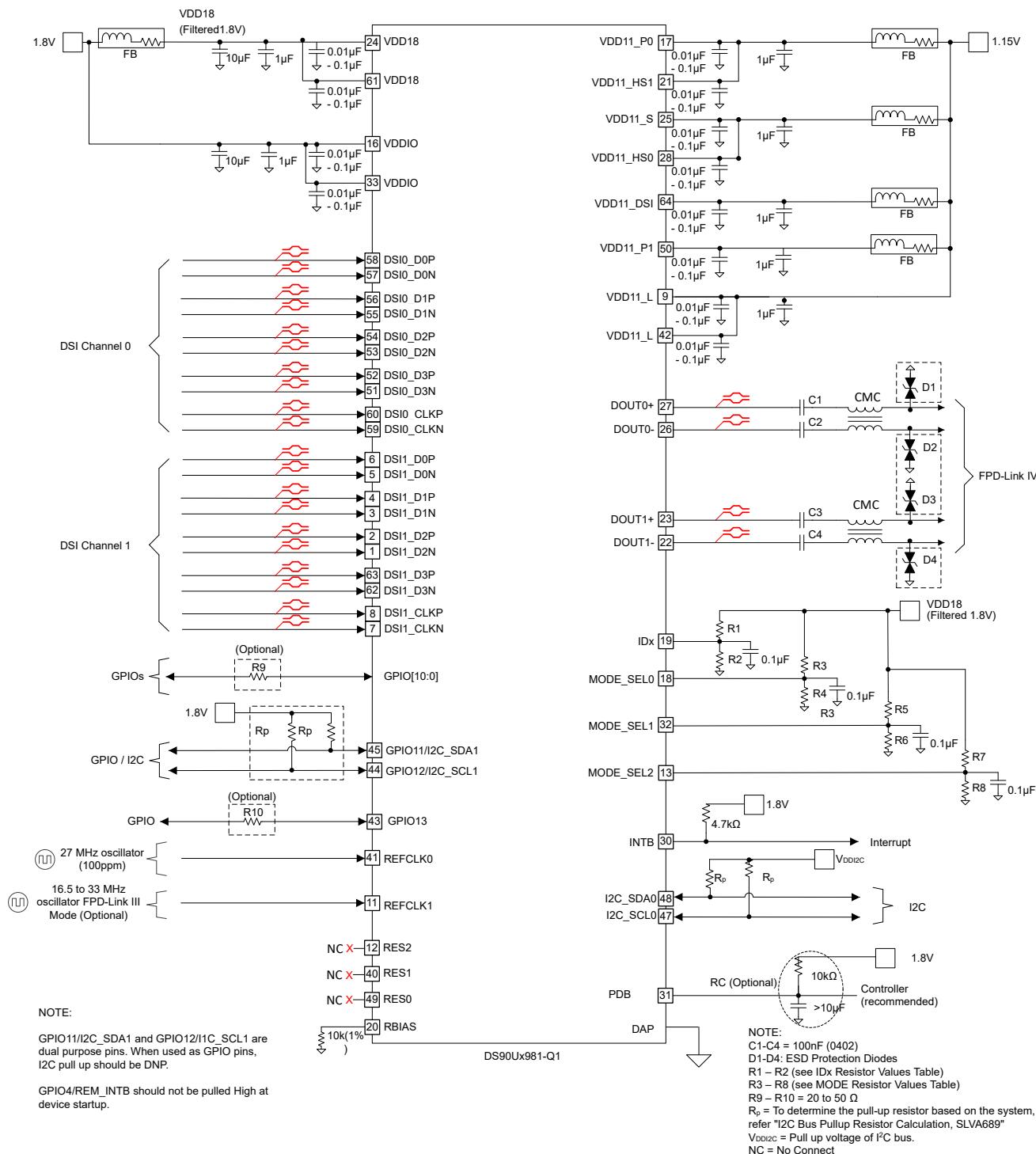
The DS90UH981-Q1, in conjunction with a FPD-Link IV or FPD-Link III deserializer, is intended to interface between a host (graphics processor) and one or more displays, supporting up to 30-bit color depth (RGB888) and high definition (4K) digital video format. The DS90UH981-Q1 can send video data with a bandwidth of up to 10.8 Gbps for FPD-Link IV. Four different video streams can be input into the DS90UH981-Q1 and be sent out to one or two deserializers. The DS90UH981-Q1 can send up to 8 GPIO signals to linked deserializers and receive 16 GPIO signals from linked deserializers.

The DS90UH981-Q1 is capable of interfacing with FPD-Link IV or FPD-Link III ADAS deserializer to interface between a processor and another processor.

## 8.2 Typical Application



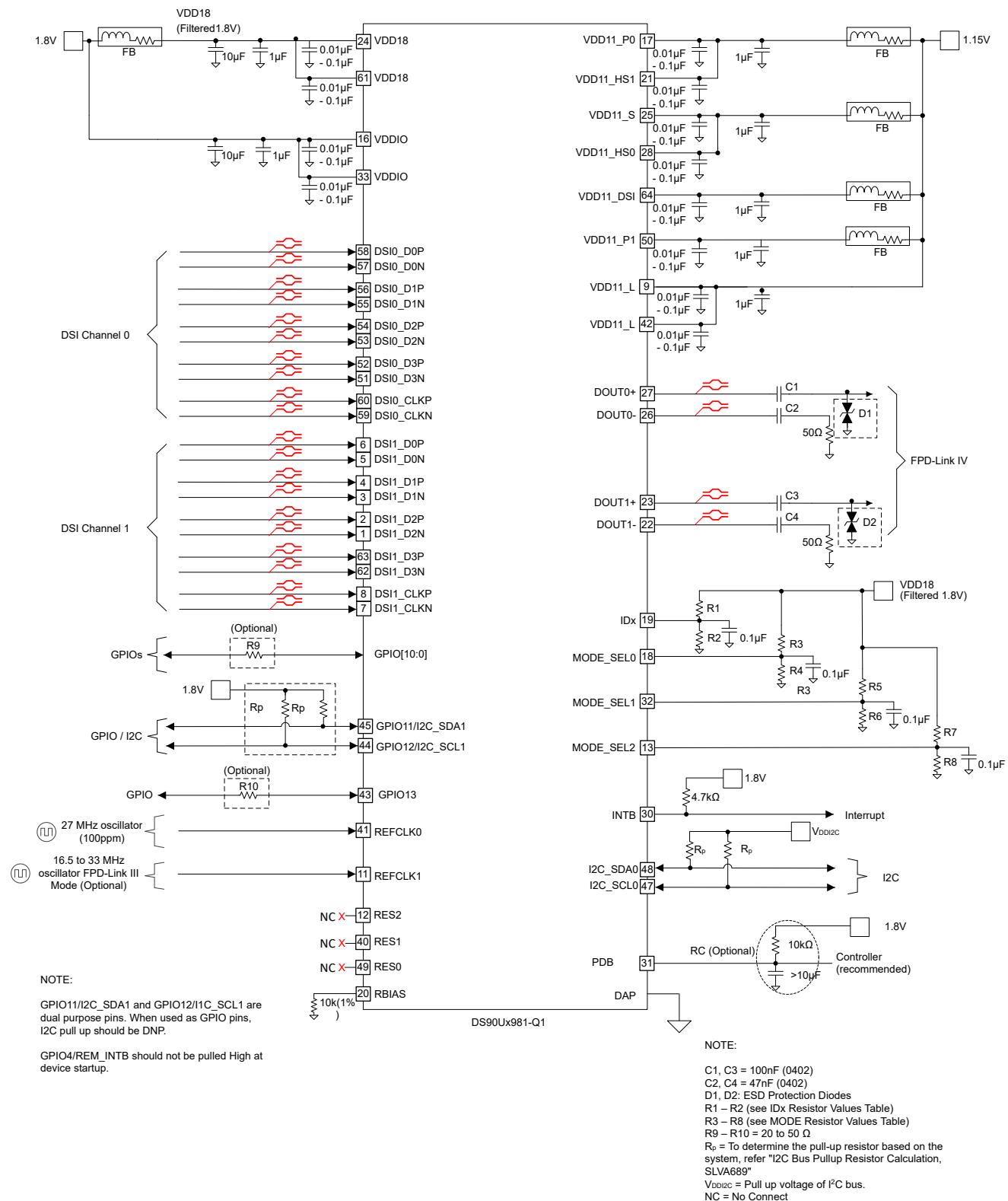
**Figure 8-1. Typical Application Diagram**



**Figure 8-2. Typical Connection Diagram - STP**

**DS90UH981-Q1**

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**Figure 8-3. Typical Connection Diagram - Coax**

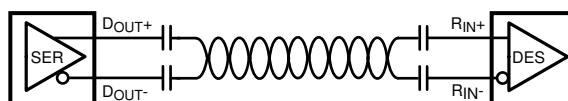
### 8.2.1 Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link IV signal path as illustrated in [Figure 8-4](#).

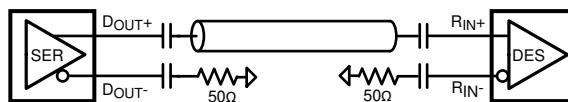
**Table 8-1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
VDD11	1.15 V
VDD18	1.8 V
AC Coupling Capacitor for DOUT± with 98x deserializers	100 nF
AC Coupling Capacitor for DOUT± with 94x or 92x deserializers	33 nF - 100 nF

For applications utilizing single-ended 50Ω coaxial cable, the unused data pins (DOUT-) must utilize a 47 nF capacitor and must be terminated with a 50Ω resistor.



**Figure 8-4. AC-Coupled Connection (STP)**



**Figure 8-5. AC-Coupled Connection (Coaxial)**

For high-speed FPD-Link IV transmissions, the smallest available package must be used for the AC coupling capacitor. This helps minimize degradation of signal quality due to package parasitics.

**Table 8-2. Oscillator Reference Clock Requirements**

Parameter	Conditions	Min	Typ	Max	Units
Frequency tolerance	-40C to 105C	-50		50	ppm
Frequency stability	Aging (10 years)	-50		50	ppm
Amplitude		800	1200	VDD18	mVpp
Reference clock Duty Cycle		40	50	60	%
Rise/Fall Time	20% - 80%		0.1	3	ns <a href="#">(1)</a>
Reference clock oscillator frequency	REFCLK0		27		MHz
	REFCLK1		16.5	33	MHz
RMS Jitter	12 kHz - 20 MHz			1	ps rms

- (1) 3 ns is the required rise/fall time at the pin. This typically corresponds to an oscillator spec of 10 ns @ 15 pF loading when the oscillator is driving only a single device.

**Table 8-3. Recommended Oscillators**

Manufacturer	Oscillator P/N	Package Dimension (mm)	Package Footprint	Supply Voltage	Description
TXC	AW27070503	2.5x2.0	4-SMD	1.8 V	Oscillator, 27 MHz, 1 ps Max RMS jitter, CMOS, AEC-Q200
Abracon	ASDAIG3-27.000MHZ-X-K-T	2.5x2.0	4-SMD	1.8 V	Oscillator, 27 MHz, <1 ps RMS jitter, HCMOS, AEC-Q200
Diodes	HX2127010Q	2.5x2.0	4-SMD	1.8 V	Oscillator, 27 MHz, 1 ps RMS jitter, CMOS, AEC-Q200

**Table 8-3. Recommended Oscillators (continued)**

Manufacturer	Oscillator P/N	Package Dimension (mm)	Package Footprint	Supply Voltage	Description
Seiko Epson	X1G005951000416	2.5x2.0	4-SMD	Min: 1.6 V, Max: 3.63 V	Oscillator, 27 MHz, 1 ps Max RMS jitter, L_Cmos, AEC-Q200

### 8.2.2 Line-Fault Detection Hardware Implementation

Line Fault Detection circuit is implemented at the system level using some external components. The faults that can be detected depends on the cable types and the actual system level implementation. The table below [STP vs Coax Line-Faults](#) provides a summary of the types of faults that can be detected in the example configurations using STP or the coax cable. Refer to application note *Diagnostic Features of FPD-Link IV Devices*, SNLA322 for more details.

The serializer device can detect fault conditions in the FPD-Link IV interconnect. If a fault condition occurs, the LINK\_DETECT status is '0' (cable is not detected). The serializer device can detect any of the following conditions:

**Table 8-4. STP vs Coax Line Faults**

Status	STP	Coax
Cable Open	Yes	Yes
“+” to “-” short	Yes	-
“+” to GND short	Yes	Yes
“-” to GND short	Yes	-
“+” to Battery Short	Yes	Yes
“-” to Battery Short	Yes	-

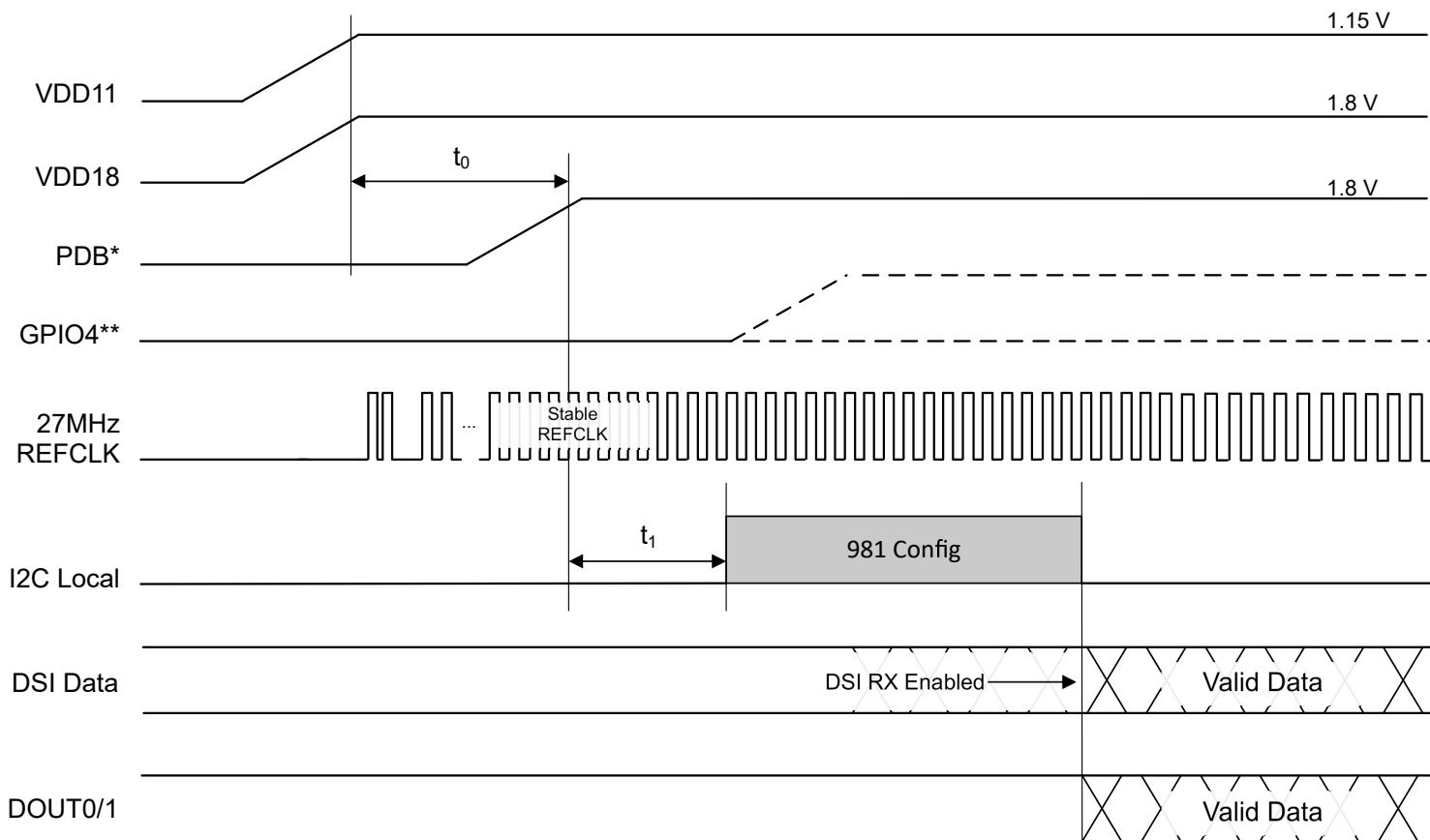
## 9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The Pin Functions table provides guidance on which circuit blocks are connected to which power pins. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

### 9.1 Power Up Requirements And PDB Pin

VDD11, VDD18 and VDDIO can rise in any order. A large capacitor on the PDB pin is needed to make sure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to V<sub>DDIO</sub>, a 10-kΩ pullup and a >10-µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until all power supplies have reached steady state.

The recommended power up sequence is shown in [Section 9.1](#)



\*27MHz REFCLK needs to be stable before PDB goes HIGH.

\*\*During power on reset, GPIO4 pin should remain low to prevent device going into test-mode.

**Figure 9-1. Recommended Power Sequencing**

**Table 9-1. Power-Up Sequencing Constraints**

SYMBOL	DESCRIPTION	REQUIREMENT DESCRIPTION	MIN	TYP	MAX	UNIT
	VDD11 Rise Time	10% to 90%	0.200		50	ms
	VDD18 Rise Time	10% to 90%	0.200		50	ms
$t_0$	Last power supply to PDB Delay	Time from when the last power supply reaches 90% to PDB reaches $V_{IL}$	0.05			ms
$t_1$	PDB to I <sup>2</sup> C ready delay		3			ms

## 10 Layout

### 10.1 Layout Guidelines

Circuit board layout and stack-up for the serializer/deserializer must be designed to provide low-noise power to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance can be greatly improved by using thin dielectrics ( $>4.4$  mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypassing must be low-ESR ceramic capacitors with high-quality dielectric. The voltage rating of the ceramic capacitors must be at least  $2\times$  the power supply voltage being used.

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the  $47\text{-}\mu\text{F}$  to  $100\text{-}\mu\text{F}$  range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

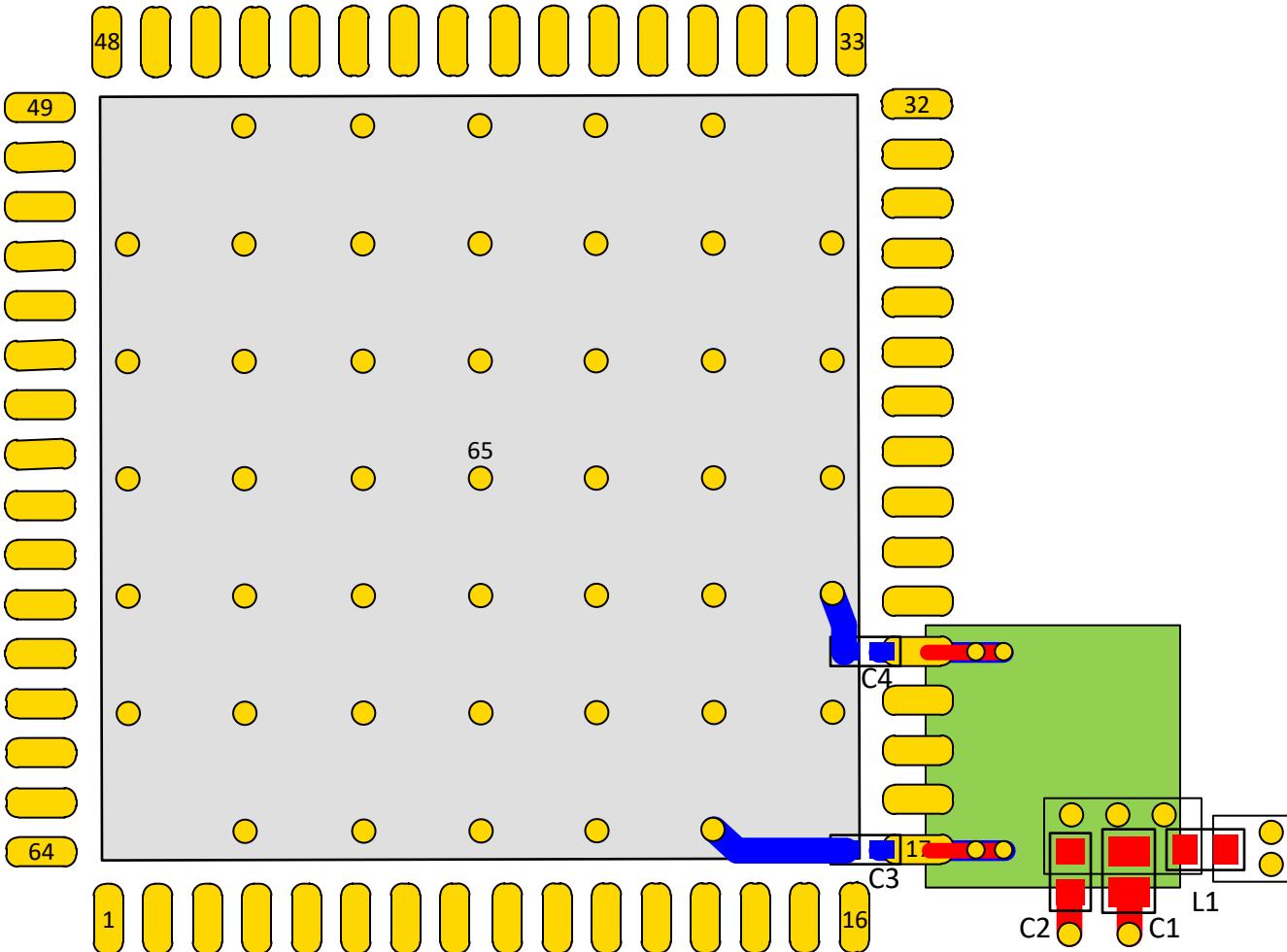
A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs. For serializer/deserializer, only one common ground plane is required to connect all device related ground pins.

TI suggests a six-layer board with dedicated power and ground plane. Locate DSI signals away from the single-ended or differential FPD-Link traces to prevent coupling from the DSI signals to the TX outputs. The following sections provide important details for routing the FPD-Link and DSI traces.

#### 10.1.1 Bypass Capacitors

Figure 10-1 shows an example of how to layout the capacitors. Place bypass capacitors with care avoid unwanted noise coupling into the device. If the device is placed on the top side of the board, then the capacitor must be placed underneath of the device or the other way around. The engineer can place the capacitor close to the power supply pin on the bottom side of the PCB to free up space on the top side of the board for high-speed routing. This bottom placement also allows other signals to access the device pins more easily. TI recommends using a via on each end of the bypass capacitors to connect the power and ground pins directly to the power and ground planes. Connecting the power or ground pins to an external bypass capacitor increases the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass, but a larger cap like  $10\text{-}\mu\text{F}$  is not always available in a smaller 0603 or 0402 package. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonant frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, common practice is to use two vias from the power and ground pins to the planes to reduce the impedance at high frequency.



**Figure 10-1. Recommended Capacitor Layout**

Figure 10-1 is an example of the layout, but not necessary to replicate the exact same layout. The QFN package has pins that surround the desired dimension with a vacant center courtyard available on the bottom sides. This is a great opportunity to use the space around the power and ground pins that are near the vacant center courtyard. In Figure 10-1, assuming the device is placed on the top side indicated in red, the lowest value bypass capacitor can be placed on the bottom side (blue) to maintain proximity to the part and utilize the extra DAP space available. This placement eases the placement of the bypass capacitors on the opposite side of the board in the courtyard area. C3 and C4 are the smallest values of the capacitor that can be placed right at the bottom of the power pin. This gives the lowest inductance path for power. C1 and C2 are the large value capacitors, and the inductor can be placed on the top side as shown in Figure 10-1. Each connection point of the components requires at least two vias with 10 mils minimum of hole diameter for the power path. The top red plane at C1 and C2 immediately drops down to the green plane of the power, which fanout the plane to pin 17 and 21 of the device. The trace widths around pins 17 and 21 must be equal and on the bottom side of the connection. The red traces on top of the plane and blue trace widths on the bottom of the plane shown in Figure 10-1 must also be of equal length. Pins 18, 19, and 20 are still accessible on the top side of the board after the connection.

### 10.1.2 Heat Conduction

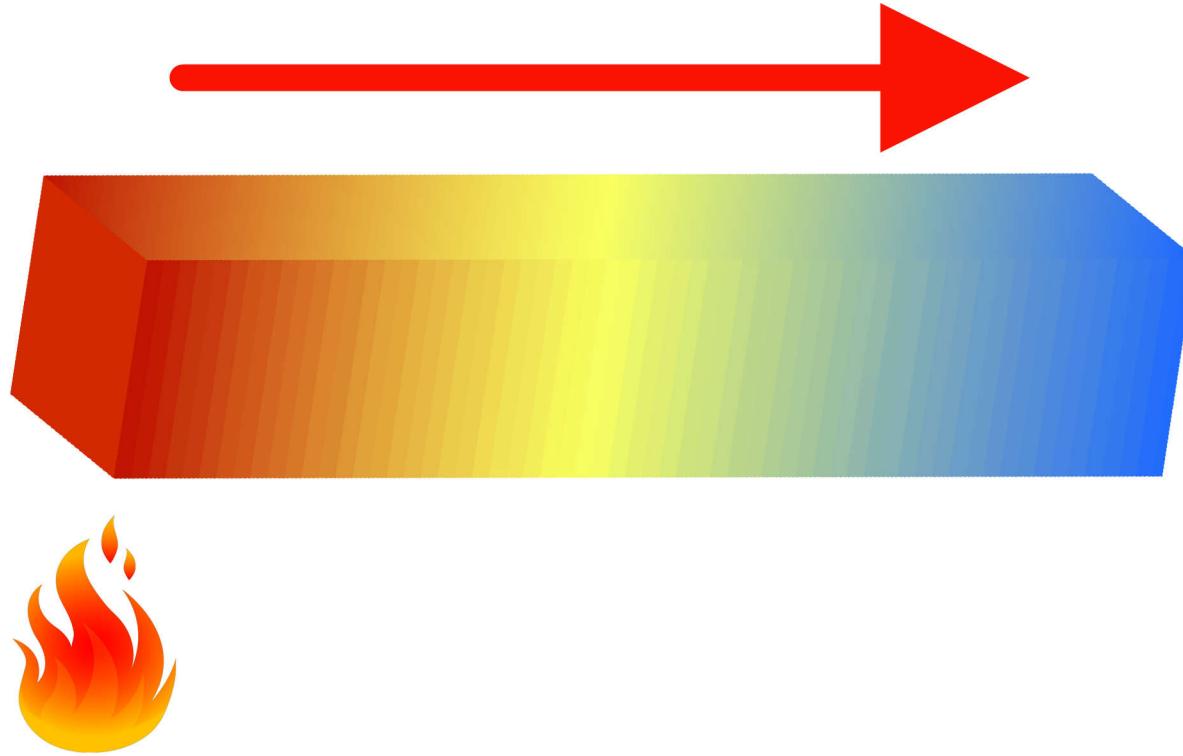
There are three methods of heat transfer: heat conduction through solids, heat convection through fluids and gases, and heat generated by radiation. The heat conduction dominates the heat transfer in PCBs and is therefore most relevant to temperature in the PCBs.

Heat conduction is defined as the transfer of heat through a volume or a body. Heat is transferred through microscopic collisions of particles; the more collisions, the hotter the object is. Heat transfer occurs when there is a temperature difference between two objects or between different areas of an object, and the rate depends on the geometry, thickness, and material of the object. Due to the law of equilibrium, heat transfers from a hotter body to a colder body until the whole system reaches final equilibrium, as shown in [Figure 10-2](#). There is no net heat transfer between two objects that are equilibrium temperature. The equation for heat transfer through conduction is shown below:

$$\frac{Q}{t} = kA \frac{(T_2 - T_1)}{d} \quad (33)$$

where

- $Q/t$ : The rate of heat transfer [J/s]
- $k$ : the thermal conductivity of the material [W/m×K]
- $A$ : Surface of the contact area [ $m^2$ ]
- $\Delta T$ : The temperature difference of  $T_1$  temperature of one object and  $T_2$  temperature of the other [K]
- $d$ : The thickness of the material [m]



**Figure 10-2. Heat Conduction Model**

Thermal conductivity ( $k$ ) is the measure of a material's capability to conduct heat and is used to describe how heat conducts through a material. Metals are highly thermally conductive whereas materials like air, wool, paper, or plastic are poor conductors of heat. Materials with a very low thermal conductivity, such as polystyrene foam, act like a thermal insulator.

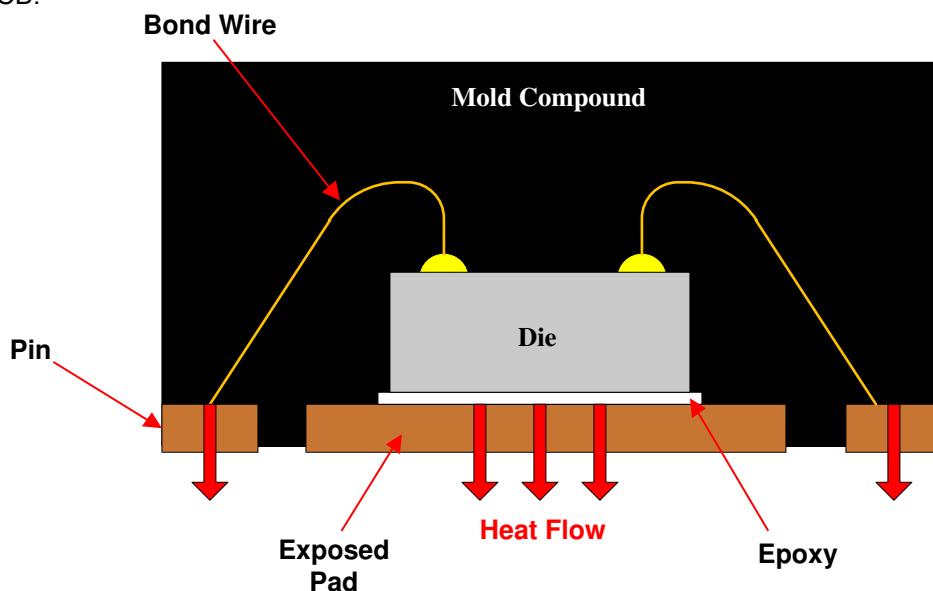
The materials that are most relevant to thermal analysis of PCBs are copper, FR4, and solder mask. Copper is an excellent conductor of heat and conducts heat significantly faster than FR4. The table below lists the thermal conductivities found in PCBs. The higher the value, the more efficient the material is in transferring heat, which results in a shorter thermal response time. For low  $k$  values, the temperature gradient between the source and the sensor can be significantly large and must be considered carefully during layout.

**Table 10-1. Material Thermal Conductivity Coefficients Of Selected Materials**

Material	Thermal Conductivity $k$ [W/(m×K)]
Air	0.0275
Solder Mask	0.245
FR4	0.25
Gold	314
Copper	385
Silver	406

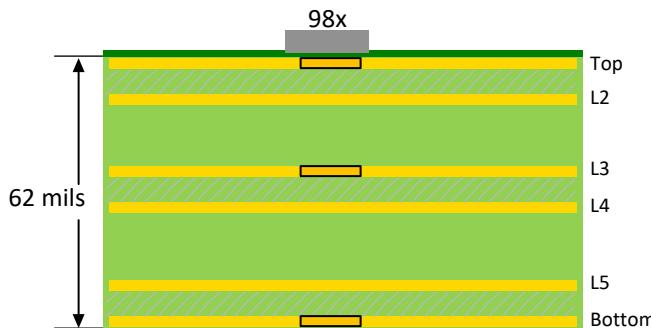
### 10.1.3 Exposed Pad Layout Design

Packages with a DAP, such as QFN package, have a large exposed surface area through which heat can transfer quickly. These package types respond quickly to temperature changes of the copper plane which the DAP is soldered onto. Since the die sits directly on top of the exposed pad, heat can transfer rapidly from the die to the thermal pad. In [Figure 10-3](#) depicts the cross section that the die is mounted on top of the metal plate leadframe with a conductive die adhesive, allowing for a fast thermal response transferring through the pins directly to the PCB.

**Figure 10-3. Heat Transfer QFN Package Cross Section Example**

The [Figure 10-4](#) illustrates the cross-section example when utilizing unused layer to create the similar to exposed pad within the layer stack-up. The copper areas of the PCB acts like a heat sinks for the QFN device where this helps extracting any heat dissipation from the device. The top copper areas of the PCB must be made per landing pattern guidelines. Any unused layer copper planes in the layer stack-up also can be connected to thermal pad using vias to create a thermal tunnel extracting the heat directly from the device out to the PCB bottom layer instead of spreading out across the PCB through the inner layers.

The dimensions of the thermal pad on the PCB must be equal to the exposed pad on the QFN as shown in [Figure 10-4](#). The thermal vias must make their electrical connection to the created exposed pad on the multiple layers stack-up ground plane with a solid connection around the entire circumference of the plated through hole and the copper pour. The connection of the thermal vias from an exposed pad of the device using direct connect. Thermal relief connection is not recommended.



**Figure 10-4. Exposed Pad Cross Section Example**

#### 10.1.4 Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the FPD-Link devices QFN package to the GND plane with vias. TI suggests 45 thermal vias per mechanical drawing from the device center DAP to the ground plane. Refer to the data sheet landing pattern recommendation for more information. Thermal vias connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the QFN style package, including PCB design and manufacturing requirements, is provided in TI [Application Note: AN-1187](#) and [QFN Package Application Note](#).

#### 10.1.5 High-Speed PCB Layout

Good layout practice involves separating high-frequency or high-level inputs and outputs to minimize unwanted noise coupling and interference. High-speed PCB design requires proper routing and stack-up techniques to ensure the signal integrity of the circuit. The performance of the high-speed FPD-Link device is heavily dependent on the PCB layout, so pay attention to the routing of high-speed lanes. A poor PCB layout can lead to poor performance. As high-speed PCB layouts become more complex the impedance control, crosstalk, reflection, discontinuities, and stack-up guidelines described in the following can help ensure optimal performance of the FPD-Link devices.

#### 10.1.6 PCB Stack-Up

During high-speed PCB design planning, constructing the multilayer stack-up prior to PCB design is critical. Planning an optimal circuit board stack up can help determine the routing methodologies quickly and easily. A well-defined stack-up can help reduce impedance mismatch and minimize the interference of external noise sources such as EMI. Circuit board layout and stack-up for the FPD-Link IV devices must be designed to provide low-noise power feed to the device. A four-layer board with a power and ground plane is feasible. TI recommends at least a 6-layer board to ensure optimal performance.

##### 10.1.6.1 Material Selection

Choosing the proper dielectric material is important for FPD-Link high-speed performance and impedance control. Each layer material is carefully chosen to meet the desired high-speed specification of the device. A hybrid version mixing high speed material with standard FR4 material can save on cost. The inner layers without high speed signals routing can use standard material for the prepreg/core substrates. When designing for high-speed signals above 10 Gbps, use premium PCB materials with low loss dielectric materials. Route high-speed SerDes traces with low loss PCB material. The PCB material thickness also dictates the characteristic 50- $\Omega$  and 100- $\Omega$  differential impedance requirements.

**Table 10-2. PCB Dielectric Material Insertion Loss**

Material	Board Class	Dk	Tan δ (Df)
FR4	Standard Loss	4.3	0.025
Isola 370HR		3.92	0.025
Isola FR406		3.92	0.0127
Isola FR408	Medium Loss	3.66	0.0127
Isola FR408HR		3.64	0.0098
GETEK		3.5	0.009
Isola I-SPEED		3.63	0.0067
Nelco 4000-13 EP		3.6	0.008
Megtron 6		3.33	0.003
Rogers 4350B	Low Loss	3.48	0.0037

Different laminate vendors offer a wide range of products as the value of the dielectric loss (Dk) and loss tangent (Df) differ from various cores and prepgs used in actual PCB constructions. Note that a small differences of Dk or Df can have a huge impact on controlled impedance lines and signal integrity. In order to prevent signal energy loss at high frequencies, the material uses must have a low Dk, Df and signal integrity features. A large loss tangent means higher dielectric absorption. Most of the high-speed material have a flatter Dk and Df as the frequency increasing and maintain a low dielectric loss.

**Table 10-3. FPD-Link PCB Recommendations**

Parameter	Min	Typ	Max	Units
PCB layer count	4	6	10	Layer
Dielectric (Dk) f < 10 Gbps		3.92	4.3	Er
f > 10 Gbps		3.2	3.6	
Loss tangent (Df) f < 10 Gbps		0.025	0.030	Tanδ
f > 10 Gbps		0.004	0.010	
T <sub>g</sub> glass transition temperature	170	180		°C
Copper weight (trace thickness)	0.5	1		Oz
Surface roughness		0.1		mil (RMS)
Trace length, L		2		Inch
Trace width, W	5	8	10	Mils
Single-ended: Gap between P-trace to N-trace, S		3W		W
Differential: Gap between P-trace to N-trace, S Tightly coupled		S<W S=2W		W
Loosely coupled				
Single-ended characteristic impedance	45	50	55	Ω
Differential characteristic impedance	90	100	110	Ω
Differential connector and landing pads impedance	80	100	120	Ω
Intra-pair skew (delay difference between P+ and N- trace)			1	ps

**Table 10-3. FPD-Link PCB Recommendations (continued)**

Parameter	Min	Typ	Max	Units
Inter-pair skew (pair-to-pair delay difference) <sup>1</sup>			<sup>4 *</sup> FPD_FRAME_PERIOD <sup>2</sup>	ns

1. The total inter-pair skew from both PCBs, cable, and connectors
2. For FPD-Link III - FPD\_FRAME\_PERIOD (ns) = 35 / FPD\_RATE (Gbps), for FPD-Link IV - FPD\_FRAME\_PERIOD (ns) = 132 / FPD\_RATE (Gbps)

### 10.1.6.2 FPD Linerates for $\leq 6.75$ Gbps

When designing for high-speed signals below  $\leq 6.75$  Gbps, a standard to medium loss material can be used for the stack-up construction. FR4 is the most commonly used PCB material in most lower frequency applications.

**Table 10-4. EVM Stack-up Details**

# OF LAYER	LAYER	TYPE	THICKNESS (MILS)	COPPER WEIGHT (oz)	DIELECTRIC CONSTANT	LOSS TANGENT	COUPLING TYPE
1	MASK	SURFACE	0.8		3.2	0.035	
	TOP	CONDUCTOR	1.4	0.5			COATED COUPLED MICROSTRIP
		PREPREG	3.324		3.8		
2	SIGNAL-1	CONDUCTOR	1.4	1			
		CORE	9.843		3.8		
3	GND 1	PLANE	1.4	1			
		PREPREG	6.469		4.25		
4	PWR1	PLANE	1.4	1			
		CORE	11.811		4.25		
5	PWR2	PLANE	1.4	1			
		PREPREG	5.907		4.25		
6	GND 2	PLANE	1.4	1			
		CORE	9.843		3.8		
7	SIGNAL-2	CONDUCTOR	1.4	1			
		PREPREG	3.234		3.8		
8	BOTTOM	CONDUCTOR	1.4	0.5			COATED COUPLED MICROSTRIP
		SURFACE	0.8		3.2	0.035	

### 10.1.7 Controlled Impedance

For DSI, DisplayPort, and OLDI interfaces maintaining a differential trace impedance of 100 ohm  $\pm 10\%$  is important to avoid impedance mismatches in the transmission line that can affect the signal integrity. Even though Embedded DisplayPort (eDP) differential impedance is targeted at  $85 \Omega \pm 15\%$  based on eDP standard specification, if no eDP connector is used then  $100 \Omega \pm 10\%$  trace impedance typically can be used to minimize impedance mismatch. The mismatch creates discontinuities, which causes reflections on the signal traces. The differential impedance is determined by the combination of the physical dimensions, the trace width, the adjacent ground, and the properties of material used in PCB substrate. Many software tools are available to calculate the properties of the transmission line structures.

**Table 10-5. Impedance Controlled for Various Interfaces**

Type of Interface	Differential Impedance
FPD-Link IV	$100 \Omega \pm 10\%$

### 10.1.8 Differential Traces

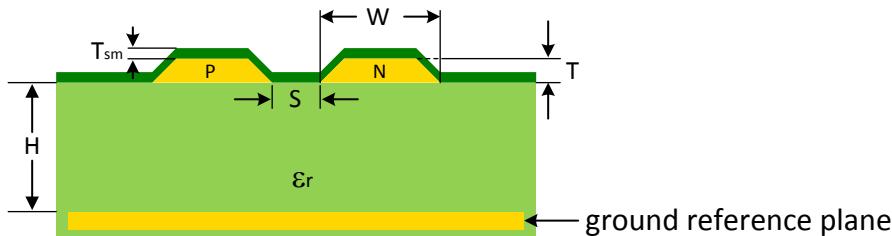
They are all tightly coupled in both separation and equal length to benefit from the electromagnetic field cancellation. When the differential pairs are symmetrical and have the same length, the pairs provide excellent noise immunity. This helps minimize impedance discontinuity because this setup prevents traces from branching out and other sudden changes in large landing pads as shown in [Figure 10-11](#).

### 10.1.9 Microstrip vs Stripline Methodologies

Microstrip and Stripline structures are often used in high-speed PCB design. Between microstrip and stripline, the decision of which method to use is based on the needs of the design and applications. Both methods are excellent performance for high-speed frequency. Both methods are designed for routed traces that have the correct structure when the return path signals travel along the traces through a plane that is separated by a certain width and height in [Figure 10-5](#) and [Figure 10-6](#).

In [Figure 10-5](#) shows a microstrip configuration with a soldermask top conductor and a dielectric layer separated by bottom ground plane. The P and N traces differential pairs are separated by a uniform distance of S. The spacing between two differential traces is set to S = W for tightly coupled traces.

- H = the height distance of the dielectric from the differential pair to the ground reference plane
- S = the separation distance between the two traces of the differential pair
- W = the width of the copper trace
- T = the thickness of the copper trace
- $T_{sm}$  = the thickness of the soldermask
- $\epsilon_r$  = the dielectric constant of the substrate between copper trace and the ground reference plane

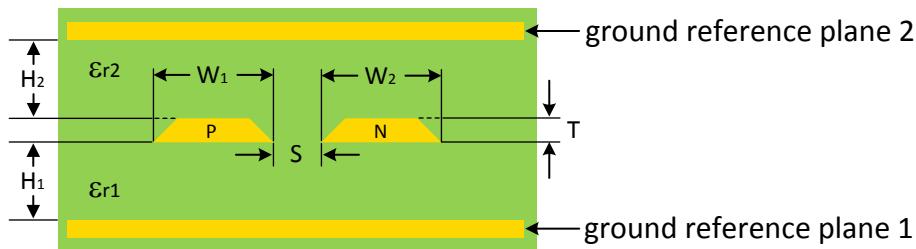


**Figure 10-5. Microstrip Differential Pair With Soldermask Coated**

For the microstrip, the electric field travels along the trace exposed to the air whereas the trace in the stripline is fully by reference planes.

In [Figure 10-6](#), stripline constructs top and bottom ground planes with dielectric insulator material surrounding a center conductor in a balanced configuration. The two differential traces are sandwiched between ground reference planes 1 and 2, as well as along the traces when there is a ground via stitching. The P and N traces differential pairs are also separated by a uniform distance of S.

- $H_1$  = the height distance of the dielectric from the ground reference plane 1 to the differential pair
- $H_2$  = the height distance of the dielectric from the differential pair to the ground reference plane 2
- S = the separation distance between the two traces of the differential pair
- $W = W_1 = W_2$  = the width of the copper trace
- T = the thickness of the copper trace
- $\epsilon_{r1}$  = the dielectric constant of the substrate between the ground reference plane 1 and copper trace
- $\epsilon_{r2}$  = the dielectric constant of the substrate between the copper trace and the ground reference plane 2



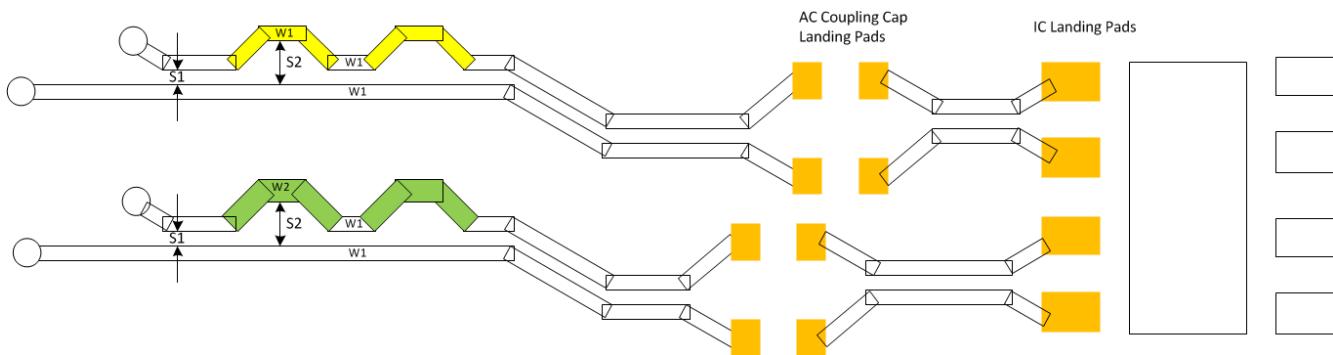
**Figure 10-6. Stripline Differential Pair**

### 10.1.10 Length Matching

Length matching is also a critical requirement parameter for DSI input, DisplayPort input and FPD-Link IV output differential pairs. When the high-speed signal lanes are length matched, it helps closely match the propagation delay between P and N. The mismatch of the P and N traces introduces skew. To compensate the length mismatch, serpentine routing must be used on the shorter trace length, and most CAD tools are available to implement the serpentine routing. It is very important that the engineer choose the dimensions of the trace tuning carefully so that all the critical signals simultaneously arrive together at their destination. The serpentine trace must be routed as close to the source as possible.

### 10.1.11 Intra-Pair Skew Matching

Intra-pair skew occurs when the differential signals of P and N are not equal length. When matching the intraskew of the P and N differential signals, the serpentine routing must be used on the shorter trace length at the source to match the lengths as close as possible. The skew adjustment can be used on the loosely coupled trace to implement the serpentine techniques.



**Figure 10-7. Intra-Pair Skew and Inter-Pair Matching**

### 10.1.12 Inter-Pair Skew Matching

Inter-pair skew is used to compare the difference between a differential pair from another differential pair of the same group, such as the four lanes of data and one clock lane for DSI per DSI port and two pairs of FPD-Link IV of the serializer device. The DSI requires that the difference in signal delay between any the data lanes and the clock lane must be less than the UI/50 for data rates less than or equal to 1.5Gbps.

### 10.1.13 Width and Spacing

The P and N traces along with the spacing between the P and N, are required to calculate characteristic impedance. The impedance of the differential trace is controlled by the width of the trace, air gap between P and N, stack-up, dielectric, and materials. To maintain a uniform-controlled impedance of the  $100\text{-}\Omega$  differential pair, the spacing between positive and negative not be exceed 2x the trace width.

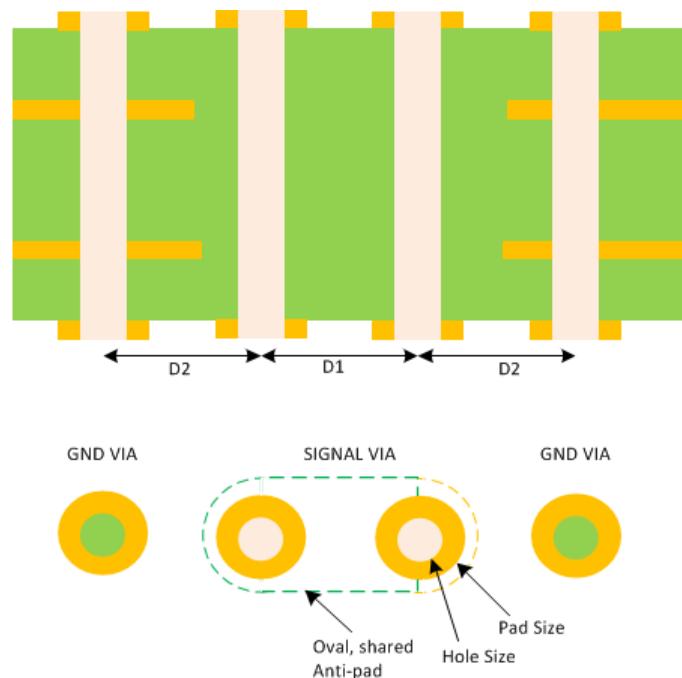
### 10.1.14 Crosstalk

The high-speed differential pair of P and N traces must be tightly coupled and routed in parallel with each other as much as possible, and the adjacent differential pair signals must maintain a constant distance away from the other traces to prevent coupling. The electromagnetic energy generally stays on track when traveling along the coupled traces, but the energy can escape if there is interference from an adjacent signal. If the electromagnetic energy escapes, the EMI coupling into the neighboring signals is called crosstalk.

### 10.1.15 Via

The controlled impedance of the differential via is also important to maintain  $100\text{-}\Omega$  impedance for the high-speed signals. The differential via impedance depends on many parameters, such as the hole size, pad size, anti-pad size, number of VDD/GND layers, via length, via stub, and via pitch. It is possible to create a controlled impedance via of the high-speed differential via by optimizing the physical dimensions of the PCB design. The differential via of the high-speed signal can be in close proximity with an oval anti-pad shared by the two vias to

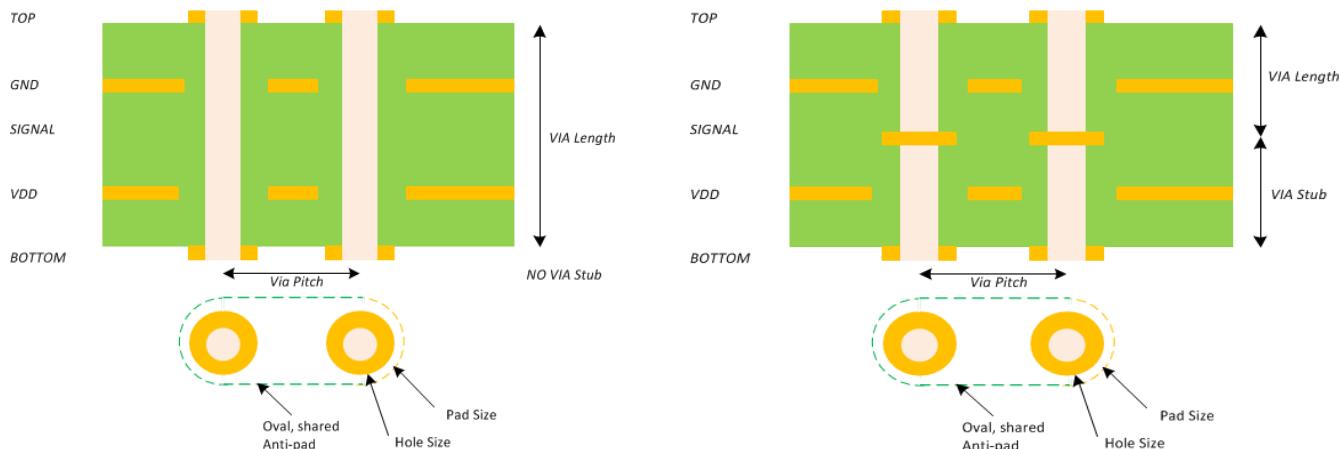
reduce parasitic capacitance. The engineer must also place a ground via next to each P and N differential via and evenly space the D1 and D2 lengths between the differential via signals to provide a good return path and isolation for the vias. See [Figure 10-8](#) for an example.



**Figure 10-8. Controlled Impedance Differential Via**

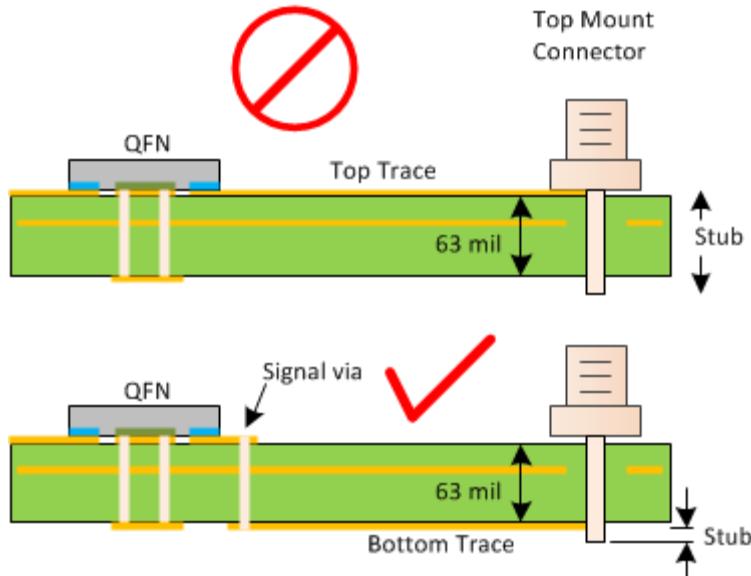
#### 10.1.16 Via Stub

Regardless of the routing techniques used for microstrip or stripline methodologies, via stub is not recommended for high-speed differential signals of the DSI, OLDI, DisplayPort and FPD-Link IV. This is because the via stub can bring a capacitive effect to the differential signals and increase the signal loss. Routing the high-speed differential signal traces on the top and bottom layers avoids the use of vias and allows a clean interconnect from the device to the device and the device to the output connector. To mitigate a via stub, the engineer can use a blind or buried via, back-drilling, or a through via from the top to bottom using microstrip techniques. For example, in the left image of [Figure 10-9](#), the device is placed on the top layer while the P and N differential signals are routed from the top layer to the bottom through a through via on a microstrip to avoid via stub. If the differential signals are routed through the internal layer, TI recommends a blind or buried via as well as back-drilling to create the shortest stub possible to avoid reflection.



**Figure 10-9. Example of Via Stub**

In Figure 10-10, the device is placed on the top layer as well as on a top-mount through-hole component. The differential signal traces, therefore, must use bottom trace routing to avoid the via stub. If the top trace routing restricts the top layer routing, the connector can be flipped and placed on the opposite side of the connector.

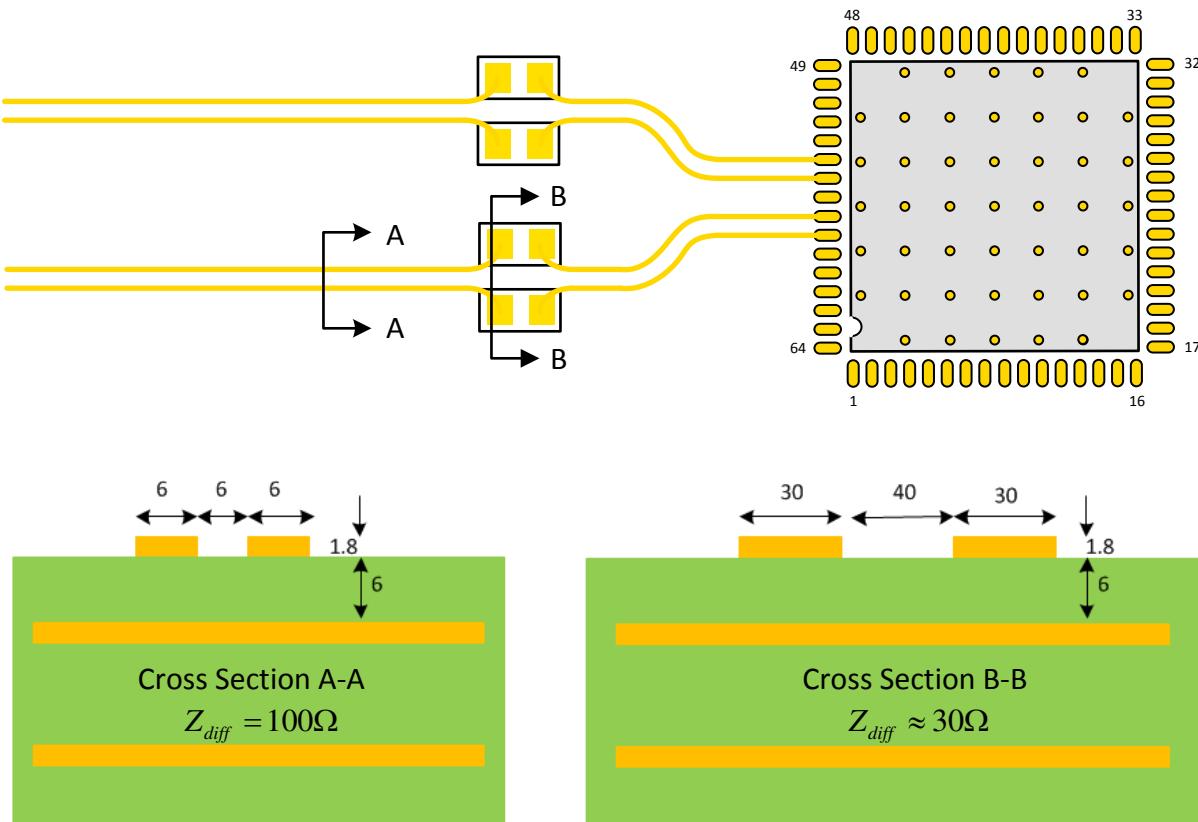


**Figure 10-10. Example of Voided Via Stub**

#### 10.1.17 Anti-Pad

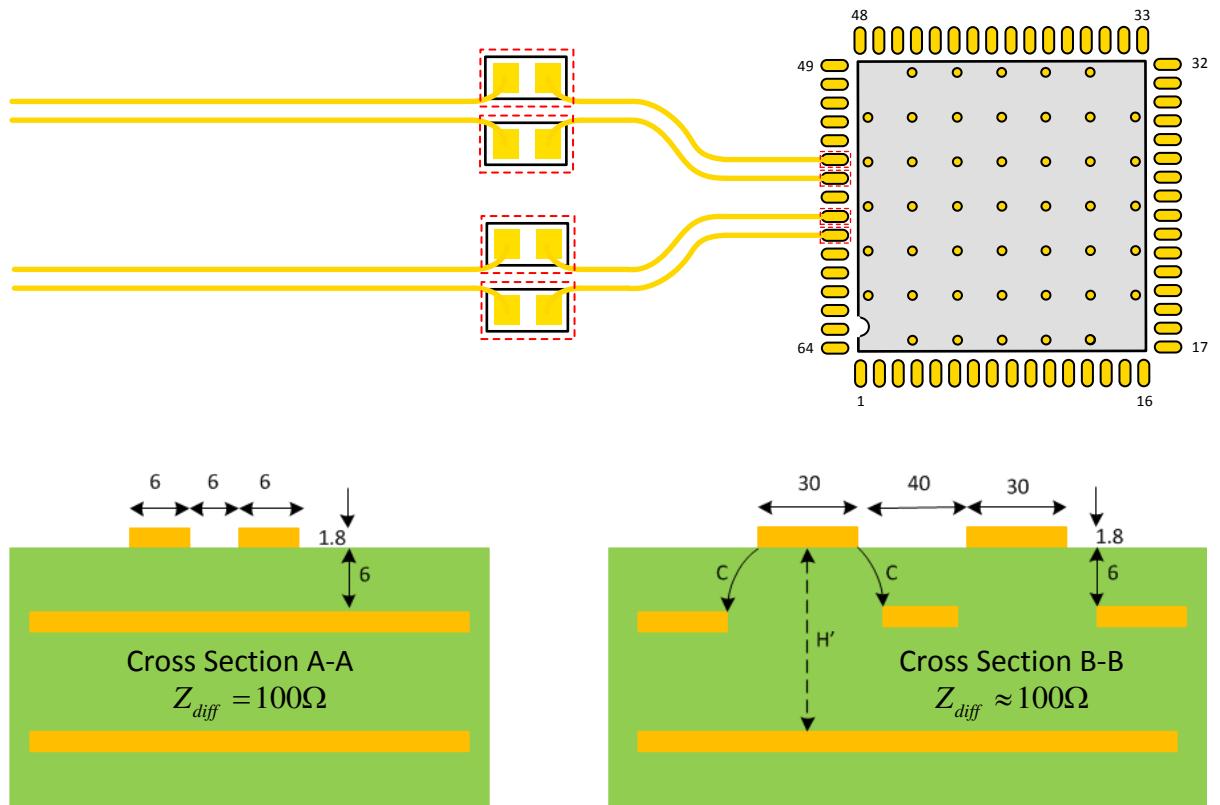
The anti-pad is the unwanted clearance area normally between the pad or trace to the copper plane, or the voided clearance area beneath the high-speed signals landing pad or blinded/buried via in the power or ground plane. Having the anti-pad can help maintain the impedance of the transmission line. The engineer cannot manually calculate the clearance of the anti-pad during layout process, but an electromagnetic field solver such as modeling software can be used to determine the effect and size of the high-speed signal trace behavior of the anti-pad for optimizing the impedance. The initial anti-pad clearance of 20 mils can be used from the trace to the copper plane for DSI, DisplayPort, OLDI and FPD-Link IV signals, and the engineer can add another 2-5 mils to the original discrete components. However, TI recommends to use the modeling software to determine the exact clearance for the design optimizing the impedance compensation.

Figure 10-11 is the example of mismatch when looking into A-A and B-B cross sections. The A-A section is excellently matched, but the cross section B-B does not match. This is due to the bottom ground plane. To achieve the  $100\Omega$  impedance, an anti-pad can be used as clearance from the pad to a shape or the next power or ground plane. This technique can reduce the parasitic capacitance.



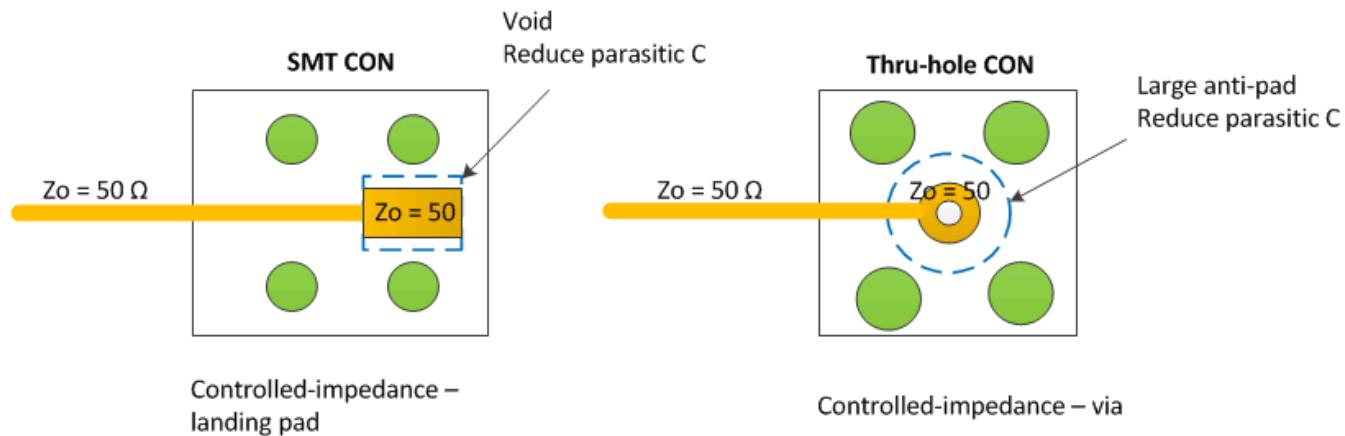
**Figure 10-11. Impedance Mismatch From Landing Pads**

To compensate the impedance mismatch of the cross section B-B of the landing pads, the power or ground relief layer, and sometimes the next internal layer, must open up and void the clearances underneath the landing pads. This can significantly increase the impedance to match cross section A-A. This method can be used along the high-speed lanes of the DSI, DisplayPort, OOLDI and FPD-Link IV to ensure the 100- $\Omega$  differential pair meets the specification.



**Figure 10-12. Controlled Impedance Landing Pads**

The anti-pad for the surface mount connector is very similar to other surface mount IC pad and other discrete components. The ground or power plane must void the clearance area under the landing pad of the connector. The through-hole connector uses the same techniques as a via.



**Figure 10-13. Controlled Impedance Footprint for Connectors**

#### 10.1.18 Routing FPD-Link Signal Traces

Routing the FPD-Link signal traces between the DOUT pins and the connector is one of the most critical pieces of a successful DS90UH981-Q1 PCB layout.

The following list provides essential recommendations for routing the FPD-Link signal traces between the DS90UH981-Q1 transmitter output pins (DOUT) and the cable connector

- The routing of the FPD-Link traces can be all on the top layer or partially embedded in middle layers if EMI is a concern.
- The AC-coupling capacitors must be on the top layer and very close to the DS90UH981-Q1 transmitter output pins to minimize the length of coupled differential trace pair between the pins and the capacitors.
- Route the DOUT traces between the AC-coupling capacitor and the cable connector as a 100- $\Omega$  differential trace with tight impedance control ( $\pm 10\%$ ). Calculate the proper width of the trace for a 100- $\Omega$  impedance based on the PCB stack-up. Make sure to length match the DOUT+ and DOUT- traces.

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- *Soldering Specifications Application Report*, [SNOA549](#)
- *Semiconductor and IC Package Thermal Metrics Application Report*, [SPRA953](#)
- *Leadless Leadframe Package (LLP) Application Report*, [SNOA401](#)
- *LVDS Owner's Manual*, [SNLA187](#)
- *I2C Communication Over FPD-Link III with Bidirectional Control Channel*, [SNLA131A](#)
- *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices*, [SNLA132](#)
- *I2C Bus Pullup Resistor Calculation*, [SLVA689](#)
- *FPD-Link Fundamental Material FPD-Link Learning Center*,
- *LVDS SerDes Gen I PCB and Interconnect Design-In Guidelines* [LVDS SerDes Gen I PCB and Interconnect Design-In Guidelines](#)
- *Ten tips for successfully designing with automotive EMC/EMI requirements* [Ten tips for successfully designing with automotive EMC/EMI requirements](#)

### 11.2 Trademarks

All trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## **12 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 12.1 Package Option Addendum

### Packaging Information

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(6)</sup>	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4)(5)</sup>
DS90UH981RTDRQ1	ACTIVE	VQFN	RTD	64	2000	RoHS & Green	NiPdAuAg	Level-3-260C-168 HR	-40 to 105	UH981
DS90UH981RTDTQ1	ACTIVE	VQFN	RTD	64	250	RoHS & Green	NiPdAuAg	Level-3-260C-168 HR	-40 to 105	UH981

- (1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OSOLETE:** TI has discontinued the production of the device.

- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

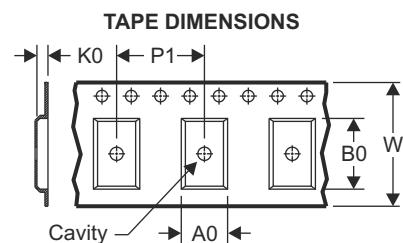
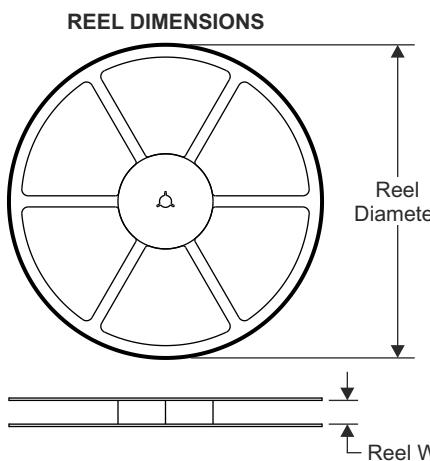
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

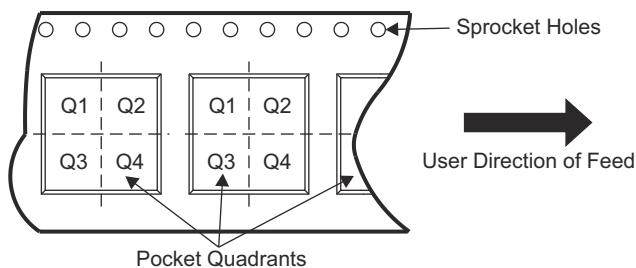
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## 12.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

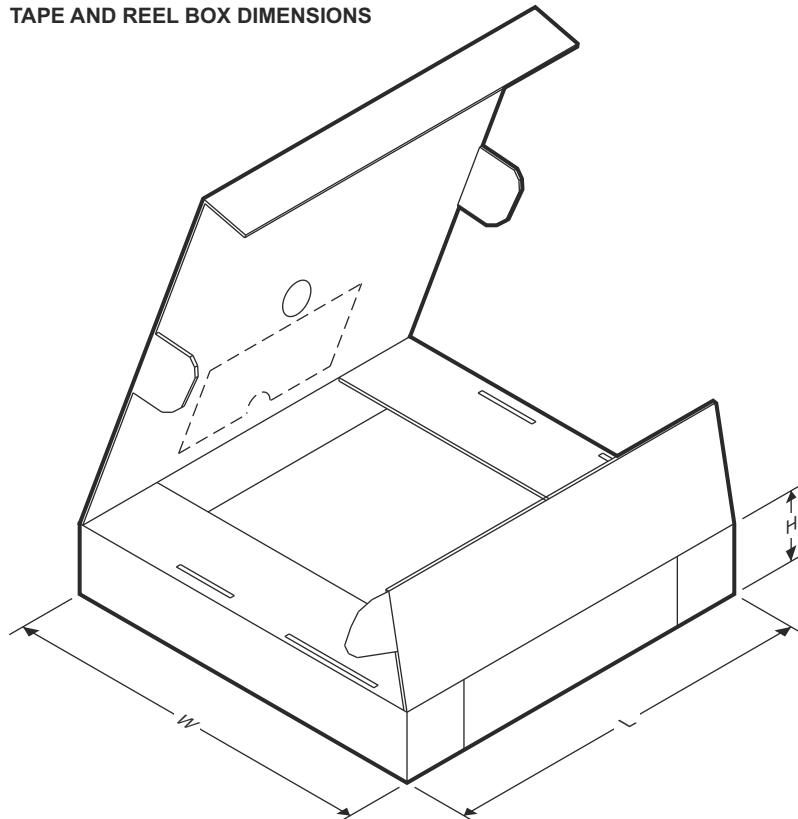


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH981RTDRQ1	VQFN	RTD	64	2000	330	16.4	9.3	9.3	1.1	12	16	Q2
DS90UH981RTDTQ1	VQFN	RTD	64	250	180	16.4	9.3	9.3	1.1	12	16	Q2

DS90UH981-Q1

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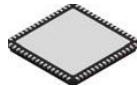
## TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH981RTDRQ1	VQFN	RTD	64	2000	367	367	38
DS90UH981RTDTQ1	VQFN	RTD	64	250	210	185	35

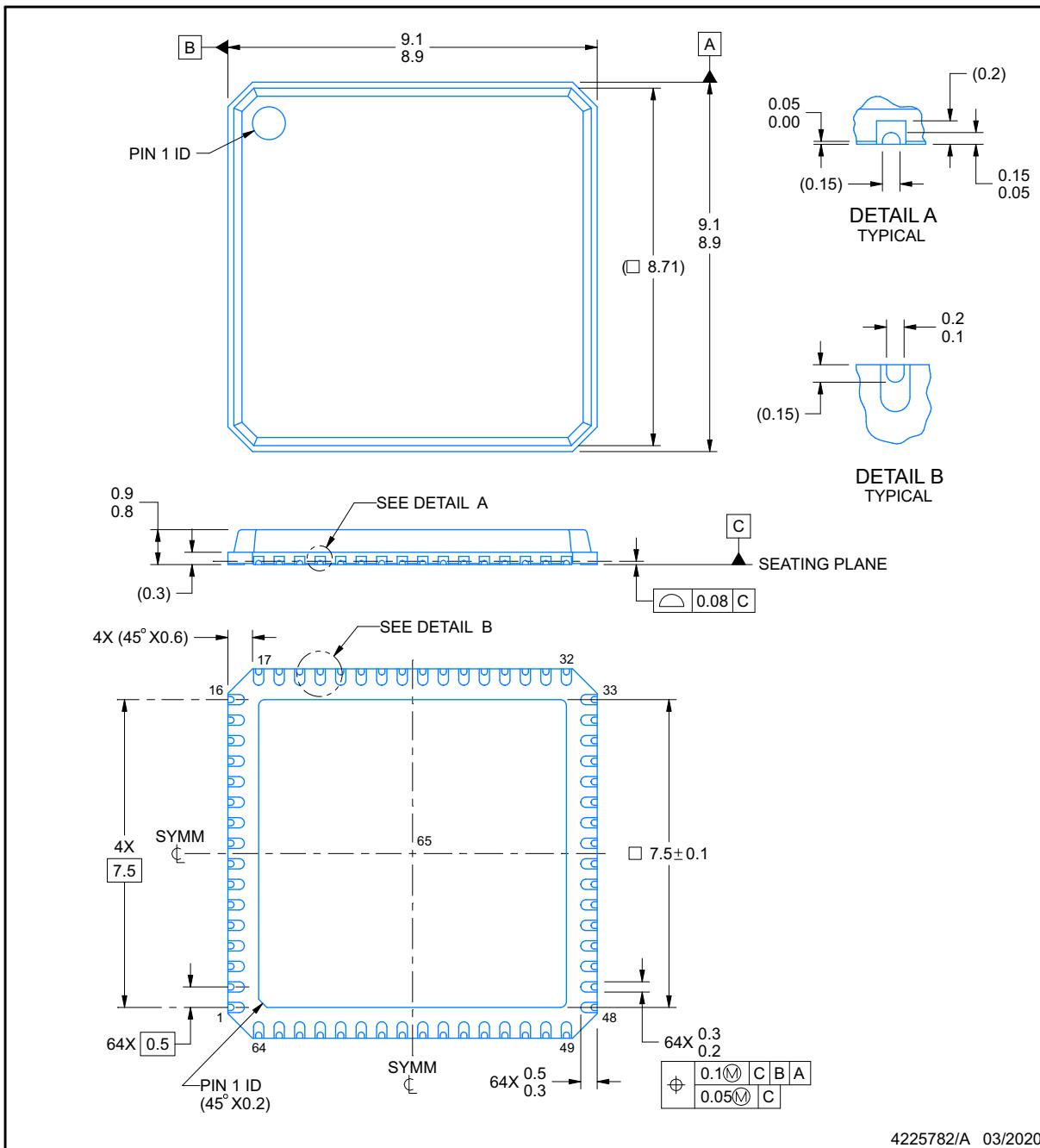
## PACKAGE OUTLINE

RTD0064M



## **VQFN - 0.9 mm max height**

## PLASTIC QUAD FLATPACK - NO LEAD



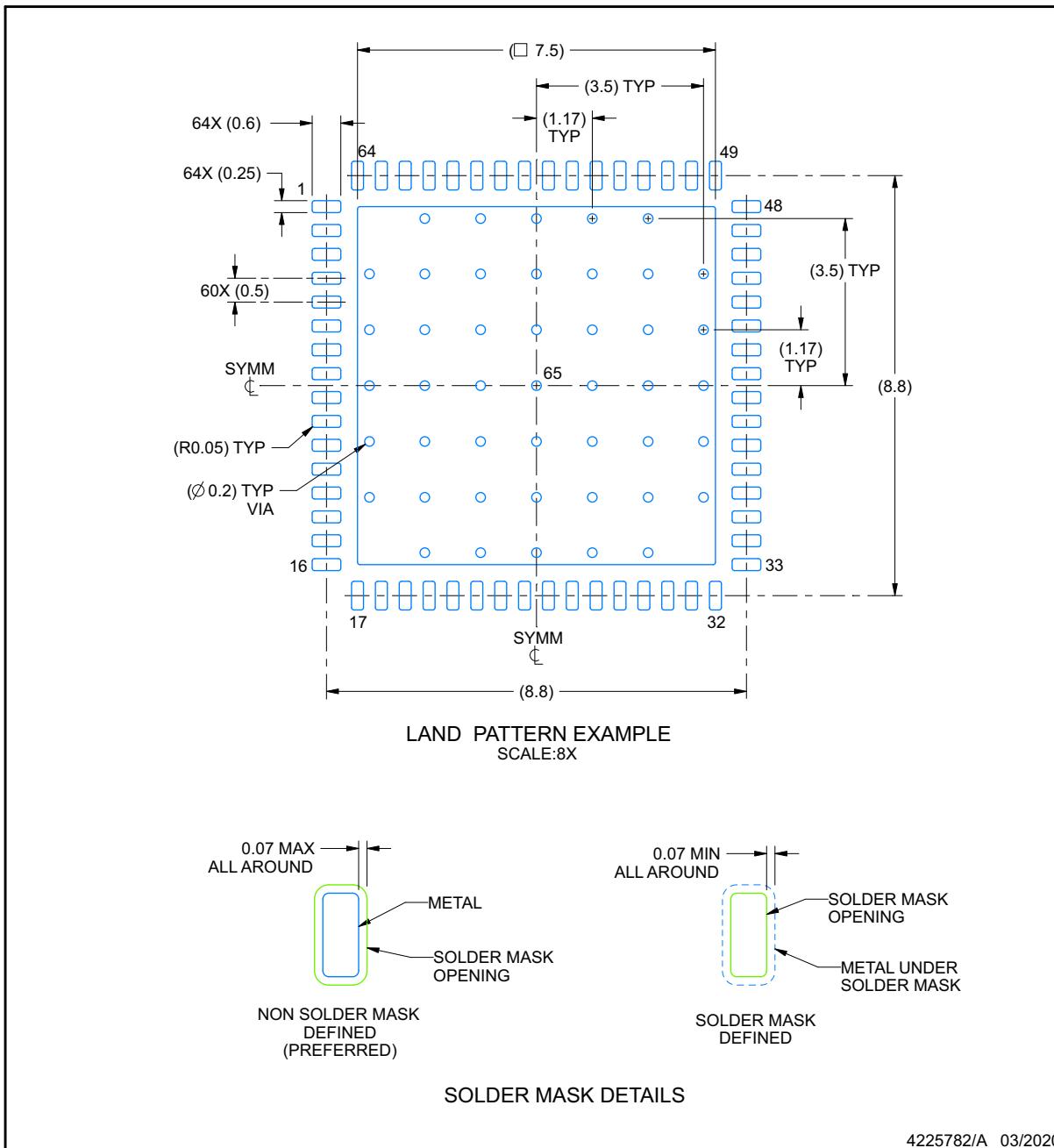
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

**RTD0064M****VQFN - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



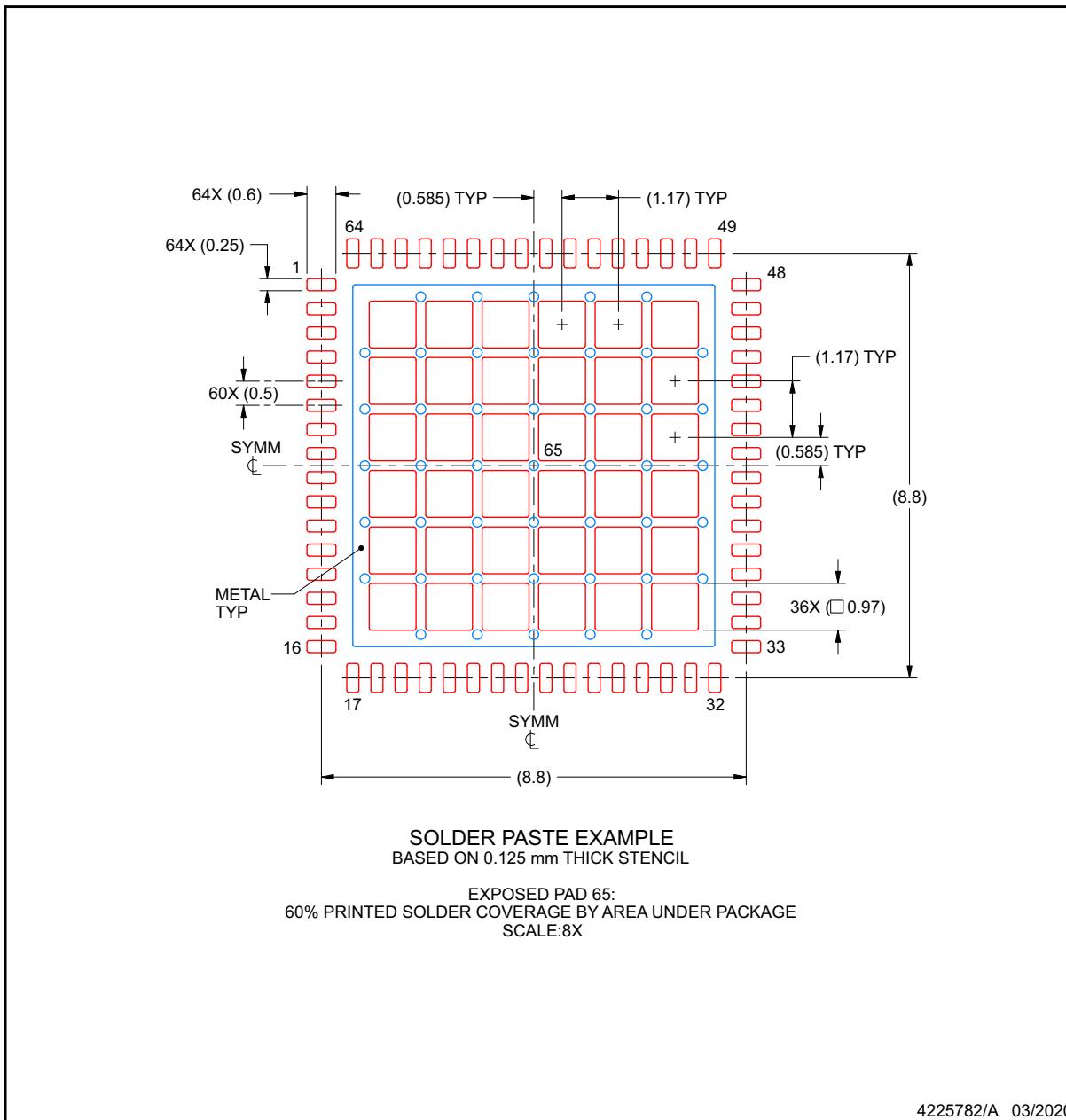
## NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**RTD0064M**
**VQFN - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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