ANALOG DEVICES

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MAX96772/MAX96774 GMSL2 eDP Deserializers with Decompression, FEC, and Optional HDCP

General Description

The MAX96772/MAX96774 deserializers convert single- or dual-link GMSL™ serial input to embedded DisplayPort (eDP) v1.4a. 600MHz PCLK capability and decompression of VESA 3:1 DSC v1.1 enable transport of 4K (UHD), 24-bit, 60fps video over a single coax or twisted pair link. The MAX96772/MAX96774 also send and receive side-channel and peripheral control data to enable full-duplex single-wire transmission of video and bidirectional data.

The MAX96774 adds HDCP 1.4 and HDCP 2.3 decryption to the GMSL2 links.

Each GMSL2 link operates at a fixed rate of 6Gbps or 3Gbps in the forward direction and 187.5Mbps in reverse, for a total capacity of 12Gbps forward and 375Mbps reverse (in dual-link mode).

The concurrent control channel supports I²C or UART. Two additional pass-through I²C or UART channels and a pass-through SPI channel are provided for peripheral control. The audio channel supports forward and reverse I²S stereo and up to 8 channels in TDM mode.

Data can be transmitted over low-cost 50Ω coax or 100Ω STP cables that meet the GMSL2 channel specification.

Table 1. Typical Maximum Cable Length

	3.2mm Ø 50Ω Coax, Foam Dielectric	2.7mm Ø 50Ω Coax, Solid Dielectric	100Ω Shielded Twisted Pair, AWG26
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, +105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at +105°C**		
3Gbps/187.5Mbps	20m	10m	11m
6Gbps/187.5Mbps	15m	9m	8m

Note: To receive the GMSL2 Channel Specification document, contact the factory.

Applications

- Cluster and Central Information Displays
- Rear-Seat Infotainment Displays

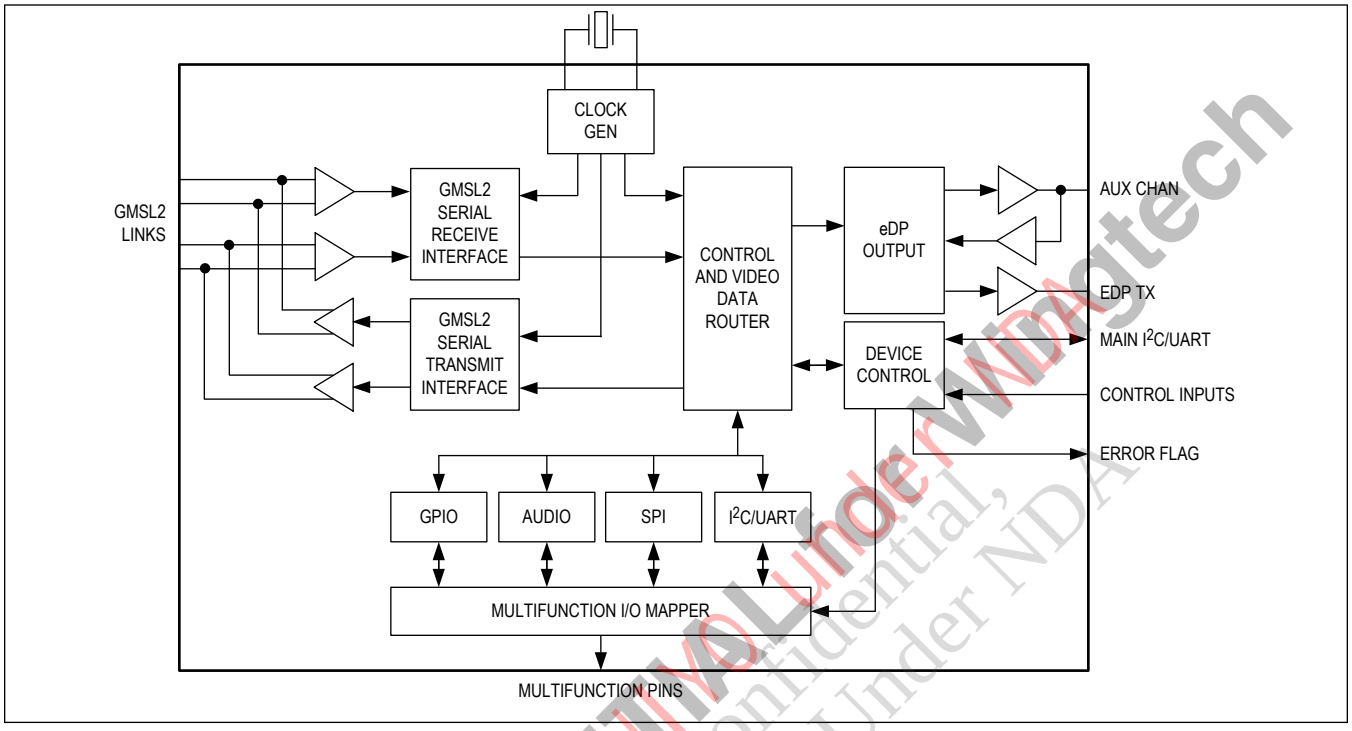
Benefits and Features

- Four-Lane RBR, HBR, HBR2, or HBR3 eDP Output
- 3Gbps or 6Gbps Forward Link Rates
- 187Mbps Reverse Link Rate
- Full-Duplex Capability Over a Single Wire
- 3:1 Display Stream Decompression with FEC
- Ideal for High-Definition RGB888 Video Applications
    - Up to 600MHz PCLK with VESA 3:1 DSC–Supports 3840x2160 (UHD), 24-Bit, 60Hz Over a Single GMSL2 Link
    - Up to 215MHz PCLK per Link Uncompressed
- Optional On-Board V_{DD} Regulator
- HDCP 1.4 and 2.3 Decryption (MAX96774 Only)
- Forward and Reverse I²S or 7.1 TDM Audio
- Uses Low-Cost 50Ω Coax or 100Ω STP Cables
- ASIL-Relevant Functional Safety Features
    - ASIL-B Compliant
    - 16-Bit CRC Protection of Control-Channel Data (I²C, UART, SPI, GPIO, Audio)
    - Retransmission on Error of All Control-Channel Data and Audio Data Upon Error Detection
    - Optional 32-Bit Video-Line CRC
    - Selectable Interrupts for Fault Detection
    - Video Watermark Generation
- Performance Tools Ensure High Link Margin
    - Continuous Adaptive Equalization on GMSL Links
    - Built-In Forward and Reverse Channel PRBS Generator for BER Testing of Serial I/O Links
    - Eye-Opening Monitor for Link Diagnosis
- Concurrent Control Channel for Device Configuration and Communicating with Remote Peripherals
    - Main and Pass-Through I²C/UART, SPI, and Tunneled or Register-Programmable GPIOs
    - Settable Priority Levels
    - Eight Hardware Programmable Device Addresses
    - Up to 16 Programmable GPIOs
    - Sleep Mode with Register State Retention
- Compact 7mm x 7mm TQFN Package with EP
- Operation Specified Over Automotive Ambient Temperature Range of -40°C to +105°C
- AEC-Q100 Qualified

Ordering Information appears at end of data sheet.

19-101268; Rev 0; 3/22

Simplified Block Diagram



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Absolute Maximum Ratings

(All voltages with respect to ground.) .....
V_{DDIO} ..... -0.3V to +3.9V
V_{DD18} ..... -0.3V to +2.0V
V_{DD} ..... -0.3V to +2.0V
CAP_VDD, V_{DDEDP} ..... -0.3V to +1.2V
SIO__, SIO__ (Active State) (*Note a*) ... (V_{DD18} - 1.1V) to V_{DD18}
SIO__, SIO__ (Inactive State) (*Note a*) ..... -0.3V to +1.1V
eTX_ ..... -0.3V to +1.1V
XRES, X2, AUX+/- ..... -0.3V to (V_{DD18} + 0.3V)
All Other Pins (*Note b*) ..... -0.3V to (V_{DDIO} + 0.3V)
Continuous Power Dissipation (T_A = +70°C, multilayer board, derate 40mW/°C above +70°C) 2200mW
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note a: An active state means the device is powered up and not in sleep or power-down modes. An inactive state means the device is not powered up, or powered up in sleep or power-down mode.

Note b: Specified maximum voltage or 3.9V, whichever is lower.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

48-Pin TQFN

Package Code	T4877+11
Outline Number	**21-0144**
Land Pattern Number	**90-0130**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

48-Pin TQFN-SW (Side-Wettable)

Package Code	T4877Y+11
Outline Number	**21-100045**
Land Pattern Number	**90-100016**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{DD18} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDEDP} = 0.95V to 1.05V, T_A = -40°C to +105°C, EP connected to PCB ground. Typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = V_{DDEDP} = 1.0V, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / REVERSE CHANNEL SERIAL OUTPUTS (SIO__)—SEE Figure 1							
Output Voltage Swing (Single-ended)	V_O	R_L = 100Ω ±1%		190	250	310	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, peak-to-peak differential voltage		380	500	620	mV
Change in V_{OD} between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)} - V_{OD(L)} \rvert$				25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state		V_{DD18} - 0.45	V_{DD18} - 0.3	V_{DD18} - 0.15	V
Change in V_{OS} between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)} \rvert$				25	mV
Termination Resistance (Internal)	R_T	Any Pin to V_{DD18}		50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / eDP OUTPUTS (eTX__)							
Differential Peak-to-Peak Output Voltage	V_{OD}	R_L = 100Ω ±1% V_{DDEDP} = 1.0V	Amplitude Setting 0	175	200	225	mV
			Amplitude Setting 1	220	250	280	
			Amplitude Setting 2	265	300	335	
			Amplitude Setting 3	305	350	395	
			Amplitude Setting 4	350	400	450	
			Amplitude Setting 5	395	450	505	
Amplitude Step Size	ΔV_{OD}				50		mV
Termination Resistance (Internal)	R_T	Single-ended measurement		40	50	60	Ω
DC ELECTRICAL CHARACTERISTICS / eDP AUX CHANNEL (AUX__)							
Differential Peak-to-Peak Output Voltage	V_{OD}	R_L = 100Ω ±1%	Amplitude Setting 0		200		mV
			Amplitude Setting 1		400		
			Amplitude Setting 2		600		
			Amplitude Setting 3		800		
			Amplitude Setting 4		1000		
			Amplitude Setting 5		1200		
			Amplitude Setting 6		1380		
Input Peak-to-Peak Voltage	V_{ID}			140		1360	mV
Input Common-Mode Voltage	V_{CMI}	Register setting at mid-scale			800		mV
Termination Resistance (Internal)	R_T	Single-ended measurement			50		Ω
DC ELECTRICAL CHARACTERISTICS / I/O PINS							
High-Level Input Voltage	V_{IH}			0.7 x V_{DDIO}			V

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDEDP} = 0.95V to 1.05V, T_A = -40°C to +105°C, EP connected to PCB ground. Typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = V_{DDEDP} = 1.0V, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup/Pulldown Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup Resistance	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Internal Pulldown Resistance	R_{PD}			1		MΩ
Input Capacitance	C_{IN}			3		pF
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2)						
X1 Input Capacitance	C_{IN_X1}			3		pF
X2 Input Capacitance	C_{IN_X2}			1		pF
Internal X2 Limit Resistor	R_{LIM}			1.2		kΩ

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDEDP} = 0.95V to 1.05V, T_A = -40°C to +105°C, EP connected to PCB ground. Typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = V_{DDEDP} = 1.0V, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Internal Feedback Resistor	R_{FB}				10		kΩ
Transconductance	g_m				28		mA/V
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS							
Supply Current (*Note 3*)	I_{DD}	3840x2160/60Hz Compressed Video Over Single 6Gbps Link, 4 HBR2 lanes, 594MHz PCLK, no HDCP	V_{DD18}		115	150	mA
			V_{DD}, regulator not used (*Note 4*)		300	800	
			V_{DD}, regulator used (*Note 4*)		295	820	
		2560x1080/60Hz Uncompressed Video Over Single 6Gbps Link, 187.5MHz Reverse, 2 HBR2 lanes, 198MHz PCLK, no HDCP	V_{DD18}		100	130	
			V_{DD}, regulator not used (*Note 4*)		240	700	
			V_{DD}, regulator used (*Note 4*)		235	740	
Maximum V_{DDIO} Supply Current	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} = 1.9V		44		µA/MHz
			V_{DDIO} = 3.6V		81		
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENTS							
Maximum Power-Down Current	I_{DD}	V_{DD18} at 1.9V	T_A = 25ºC		1		µA
			T_A = 105ºC		13		
		Regulator not used, V_{DD} = 1.05V (*Note 4*)	T_A = 25ºC		1		
			T_A = 105ºC		1		
		Regulator used, V_{DD} = 1.26V (*Note 4*)	T_A = 25ºC		1		
			T_A = 105ºC		1		
		V_{DDIO} at 3.6V	T_A = 25ºC		4		
			T_A = 105ºC		5		
DC ELECTRICAL CHARACTERISTICS / SLEEP CURRENTS							
Maximum Sleep Current	I_{DD}	V_{DD18} at 1.9V	T_A = 25ºC		19		µA
			T_A = 105ºC		36		
		Regulator not used, V_{DD} = 1.05V (*Note 4*)	T_A = 25ºC		1		
			T_A = 105ºC		1		
		Regulator used, V_{DD} = 1.26V (*Note 4*)	T_A = 25ºC		1		
			T_A = 105ºC		1		
		V_{DDIO} at 3.6V	T_A = 25ºC		4		
			T_A = 105ºC		5		

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDEDP} = 0.95V to 1.05V, T_A = -40°C to +105°C, EP connected to PCB ground. Typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = V_{DDEDP} = 1.0V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1, X2 UNCONNECTED)						
High-Level Input Voltage	V_{IH}		0.92			V
Low-Level Input Voltage	V_{IL}				0.4	V
Input Impedance	R_{IN}			10		kΩ
X1 Input Capacitance	C_{IN_X1}			3		pF
AC ELECTRICAL CHARACTERISTICS / FORWARD CHANNEL SWITCHING CHARACTERISTICS (SIO__)						
Lock Time	t_{LOCK}	(Note 7)		50		ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from GMSL2 video packet input at SIO± input to when pixels appear at video outputs. Assumes link is already established and eDP link training is complete. (See Figure 2)		5		ms
Maximum Video Latency	t_{VL}	Time from pixel within GMSL2 packet at SIO± to output at eDP interface. (See Figure 3)		50		µs
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip.		1		ms
AC ELECTRICAL CHARACTERISTICS / REVERSE CHANNEL SERIAL OUTPUTS (SIO__)—(Note 2)						
GMSL Reverse Channel Transmitter Rise/Fall Time	t_R, t_F	20% to 80%, V_O = 250mV, R_L = 100Ω		2300		ps
Total Serial Output P-P Jitter	t_{TSOJ}	PRBS7, single-ended or differential output		0.15		UI
Deterministic Serial Output P-P Jitter	t_{DSOJ}	PRBS7, single-ended or differential output		0.1		UI
AC ELECTRICAL CHARACTERISTICS / eDP OUTPUTS (eDP__)—(Note 2)						
Unit Interval	UI_Rate	1.62 to 4.32Gbps/lane (RBR, HBR)	231.5		617.3	ps
		5.4Gbps/lane (HBR2)		185		
	UI_Rate	8.1Gbps/lane (HBR3)		123		
Preemphasis		All output voltage settings: Preemphasis Setting 0		0		dB
		Preemphasis Setting 1		2		
		Preemphasis Setting 2		4		
		Preemphasis Setting 3		6		
Total Jitter (Note 5)	t_{TJO}	Lane rate ≤ 5.4Gbps			0.27	UI
		Lane rate = 8.1Gbps			0.28	
Deterministic Jitter (Note 5)	t_{DJO}	Lane rate ≤ 5.4Gbps			0.17	UI
		Lane rate = 8.1Gbps			0.2	

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDEDP} = 0.95V to 1.05V, T_A = -40°C to +105°C, EP connected to PCB ground. Typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = V_{DDEDP} = 1.0V, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Skew	t_{SKEW}	Intrapair			30	ps
		Lane-to-Lane			1250	
SSC Downspread					0.55	%
SSC Modulation Rate			30		33	kHz
AC ELECTRICAL CHARACTERISTICS / eDP AUX CHANNEL (AUX__)—(*Note 2*)						
Unit Interval	UI		0.4		0.6	µs
Cycle-to-Cycle Jitter	t_{JCC}	UI variation within a single transaction			0.08	UI
		UI variation between adjacent bits			0.04	
AC ELECTRICAL CHARACTERISTICS / I²C/UART PORT TIMING						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO} (*Note 2*)	20 x V_{DDIO}/5.5V		150	ns
I²C/UART Wake Time		From power-up, or rising edge of PWDNB to local register access. For remote register access, I²C/UART Wake Time is the same as Lock Time (t_{LOCK}). (*Note 2*)		2.4	4	ms
AC ELECTRICAL CHARACTERISTICS / I²C TIMING—SEE Figure 4						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range	9.6		100	kHz
		Mid f_{SCL} range	100		400	
		High f_{SCL} range	400		1000	
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDEDP} = 0.95V to 1.05V, T_A = -40°C to +105°C, EP connected to PCB ground. Typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = V_{DDEDP} = 1.0V, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load On Each Bus Line	C_B				100	pF
AC ELECTRICAL CHARACTERISTICS / SPI MASTER—SEE Figure 5						
Operating Frequency	f_{MCK}		0.588		25	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	(*Note 2*, *Note 6*)	$t_{MCK}/2$ - 3	$t_{MCK}/2$		ns
MOSI Data Output Delay	t_{MOD}	After SCLK falling edge (*Note 2*, *Note 6*)	-2.3		2.3	ns
MISO Input Setup Time	t_{MIS}	Before programmed sampling edge (*Note 2*, *Note 6*)	13.5			ns
MISO Input Hold Time	t_{MIH}	After programmed sampling edge (*Note 2*, *Note 6*)	-2			ns
AC ELECTRICAL CHARACTERISTICS / SPI SLAVE—SEE Figure 6						
Operating Frequency	f_{SCK}				50	MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
MISO Data Output Delay	t_{SOD}	After SCLK falling edge (*Note 2*, *Note 6*)	-1.5		11.3	ns
MOSI Input Setup Time	t_{SIS}	Before SCLK rising edge (*Note 6*)	5			ns
MOSI Input Hold Time	t_{SIH}	After SCLK rising edge (*Note 6*)	3			ns
AC ELECTRICAL CHARACTERISTICS / I^2S/TDM MASTER TIMING—SEE Figure 7 (*Note 2*, *Note 6*)						
WS Frequency	f_{WS}		8		192	kHz
Sample Word Length	n_{WS}		8		32	Bits

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDEDP} = 0.95V to 1.05V, T_A = -40°C to +105°C, EP connected to PCB ground. Typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = V_{DDEDP} = 1.0V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Frequency	f_{SCK}	f_{SCK} = f_{WS} x n_{WS} x (2 or 8)	0.512		49.152	MHz
SCK Clock High Time	t_{HC}	V_{SCK} ≥ V_{IH}, t_{SCK} = 1/f_{SCK}	0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	V_{SCK} ≤ V_{IL}, t_{SCK} = 1/f_{SCK}	0.35 x t_{SCK}			ns
SD, WS Valid Time Before SCK	t_{MAVS}	t_{SCK} = 1/f_{SCK}	0.2 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{MAVH}	t_{SCK} = 1/f_{SCK}	0.2 x t_{SCK}	0.5 x t_{SCK}		ns
AC ELECTRICAL CHARACTERISTICS / I^{2}S/TDM SLAVE TIMING—SEE Figure 8 (Note 6)						
WS Frequency	f_{WS}		8		192	kHz
Sample Word Length	n_{WS}		8		32	Bits
SCK Frequency	f_{SCK}	f_{SCK} = f_{WS} x n_{WS} x (2 or 8) (Note 2)	0.512		49.152	MHz
SD, WS Setup Time	t_{SAS}		4			ns
SD, WS Hold Time	t_{SAH}		4			ns
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2)—(Note 2)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1, X2 UNCONNECTED)—(Note 2)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
Input Jitter		6Gbps/187.5Mbps, sinusoidal jitter < 1MHz (falling edge), upstream serializer using crystal reference.			600	ps p-p
Input Duty Cycle	t_{DUTY}		40		60	%
Input Fall Time	t_F	80% to 20%			4	ns
ESD PROTECTION						
SIO__	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±8		kV
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, coax configuration		±6		
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, STP configuration		±4		
		ISO10605, R_D = 330Ω, C_S = 150pF, Air Discharge		±8		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DDIO} = 1.7V to 3.6V, V_{DD} = 0.95V to 1.05V or 1.14V to 1.26V, V_{DDEDP} = 0.95V to 1.05V, T_A = -40°C to +105°C, EP connected to PCB ground. Typical values are at V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = V_{DDEDP} = 1.0V, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Note 1: Limits are 100% tested at T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design.

Note 3: Color Bar pattern.

Note 4: V_{DD} current includes V_{DDEDP} current.

Note 5: 300mVp-p, 2dB preemphasis, CP2520 compliance pattern, measured at TP2. RBR (1.62Gbps) and HBR (2.7Gbps) characterized and guaranteed with external reference clock and crystal reference clock. All other rates characterized and guaranteed with crystal reference clock only. When using an external reference clock with rates above 2.7Gbps, a detailed system analysis needs to be completed to evaluate jitter impact on the system performance.

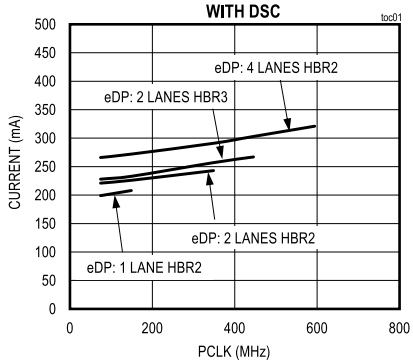
Note 6: Measured at 50MHz for SPI Slave, I^2S Master, and I^2S Slave. Measured at 25MHz for SPI Master. For the pin programming recommendations, see the *Speed Programming for SPI and I^2S* section.

Note 7: From power-up, one-shot reset, or rising edge of the PWDNB pin, to rising edge of the LOCK pin. For more information, see the *Link Lock* section.

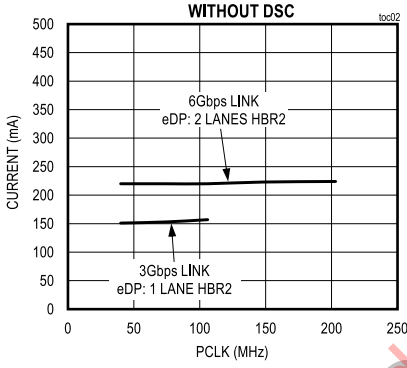
Typical Operating Characteristics

(V_{DD18} = 1.8V, V_{DDIO} = 3.3V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.)

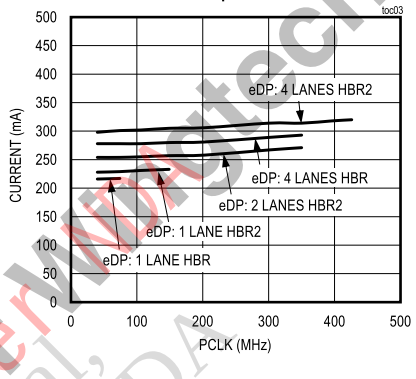
V_{DD} CURRENT
SINGLE 6Gbps GMSL2 LINK
WITH DSC



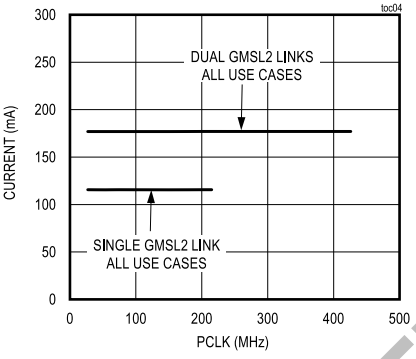
V_{DD} CURRENT
SINGLE GMSL2 LINK
WITHOUT DSC



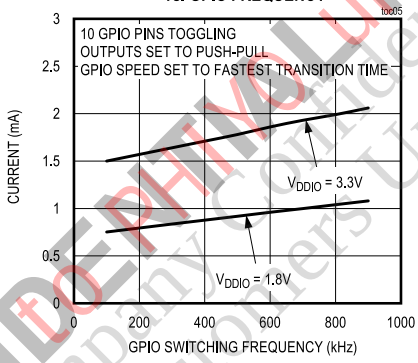
V_{DD} CURRENT
DUAL 6Gbps GMSL2 LINKS



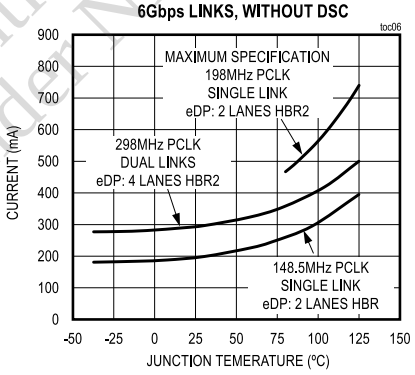
V_{DD18} CURRENT
SINGLE AND DUAL GMSL2 LINKS



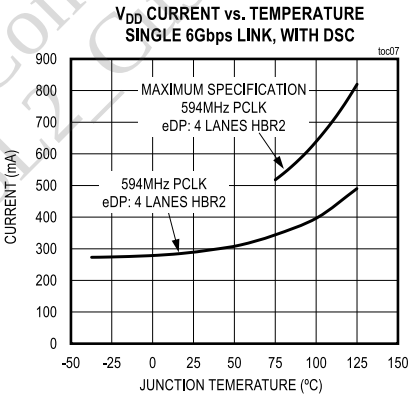
V_{DDIO} CURRENT
vs. GPIO FREQUENCY



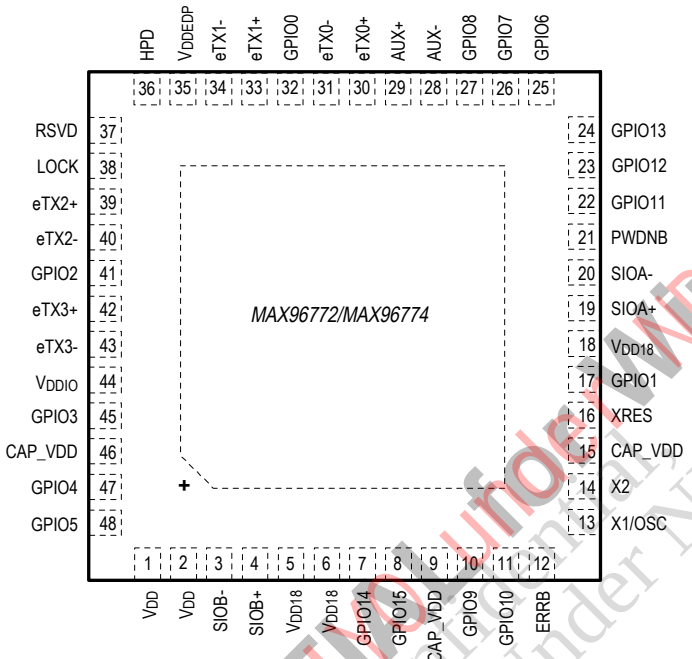
V_{DD} CURRENT vs. TEMPERATURE
6Gbps LINKS, WITHOUT DSC



V_{DD} CURRENT vs. TEMPERATURE
SINGLE 6Gbps LINK, WITH DSC



Pin Configuration



Pin Description

PIN	NAME	FUNCTION MODE	FUNCTION
		SIGNAL_NAME (Default)	
GMSL2 SERIAL LINK			
19	SIOA+	SIOA+	Noninverting Coax/Twisted-Pair Serial-Data Input 1.
20	SIOA-	SIOA-	Inverting Coax/Twisted-Pair Serial-Data Input 1.
4	SIOB+	SIOB+	Noninverting Coax/Twisted-Pair Serial-Data Input 2.
3	SIOB-	SIOB-	Inverting Coax/Twisted-Pair Serial-Data Input 2.
eDP INTERFACE			
36	HPD	HPD	eDP Hot Plug Detect Input. Configured as open-drain I/O with 1MΩ pulldown to ground.
29	AUX+	AUX+	eDP Noninverted AUX Channel.
28	AUX-	AUX-	eDP Inverted AUX Channel.
30	eTX0+	eTX0+	eDP Noninverted Data Output Channel 0.
31	eTX0-	eTX0-	eDP Inverted Data Output Channel 0.
33	eTX1+	eTX1+	eDP Noninverted Data Output Channel 1.
34	eTX1-	eTX1-	eDP Inverted Data Output Channel 1.
39	eTX2+	eTX2+	eDP Noninverted Data Output Channel 2.
40	eTX2-	eTX2-	eDP Inverted Data Output Channel 2.
42	eTX3+	eTX3+	eDP Noninverted Data Output Channel 3.

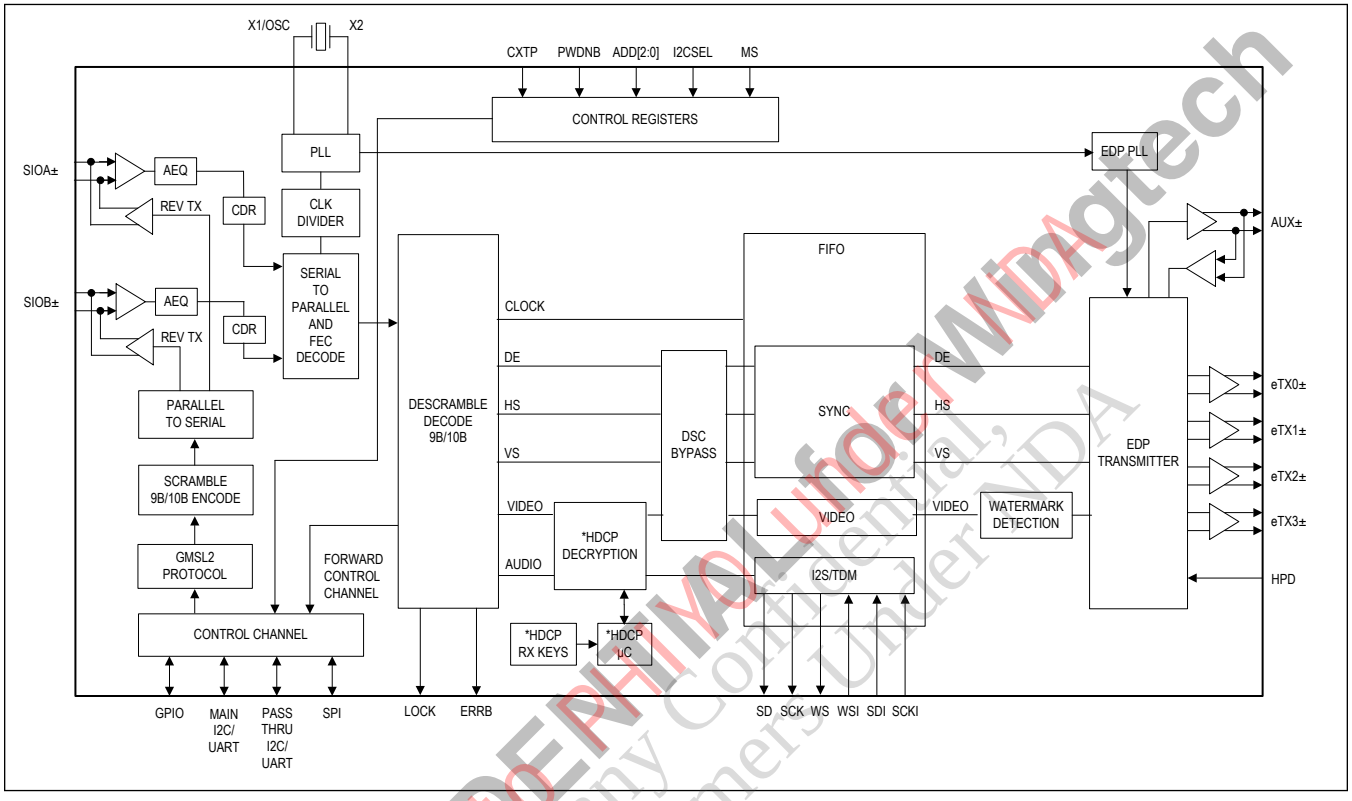
PIN	NAME	FUNCTION MODE SIGNAL NAME (Default)	FUNCTION
43	eTX3-	eTX3-	eDP Inverted Data Output Channel 3.
CONTROL AND GPIO (*DENOTES DEFAULT STATE AFTER POWER-UP)			
32	GPIO0	GPIO0* HS	GPIO0: Configurable General-Purpose Input or Output. Default is open-drain I/O with an internal 1MΩ pulldown to ground. HS: Horizontal Sync Push-Pull Output.
17	GPIO1	I2CSEL GPIO1* VS	I2CSEL: Configurable I²C Select. Control-Channel Interface Protocol Select Input with an Internal 1MΩ Pulldown to Ground. Set I2CSEL high to select I²C-to-I²C interface. Set I2CSEL low to select UART-to-UART interface. The state of I2CSEL latches at power-up. GPIO1: Configurable General-Purpose Input or Output. Default is push-pull output. VS: Vertical Sync Push-Pull Output.
41	GPIO2	GPIO2* MS WMD	GPIO2: Configurable General-Purpose Input or Output. Default is open-drain I/O with an internal 1MΩ pulldown to ground. MS: UART Mode Select with an Internal 1MΩ Pulldown to Ground. Set MS low to select base mode. Set MS high to select bypass mode. The MS state may also be temporarily overwritten by a register write. WMD: Watermark Detect Push-Pull Output. High when watermark is detected.
45	GPIO3	GPIO3* MOSI SDA1_RX1	GPIO3: Configurable General-Purpose Input or Output. Default is input with an internal 1MΩ pulldown to ground. MOSI: SPI Master Out Slave In. When configured as master, push-pull output that drives data to external slave. When configured as slave, input with an internal 1MΩ pulldown to ground that receives data from external master. SDA1_RX1: Pass-Through UART1 Receive/I²C1 Serial-Data Input/Output with an Internal 40kΩ Pullup to V_{DDIO}. SDA1_RX1 has an open-drain driver and requires an external pullup resistor. SDA1: Data Input/Output of the Deserializer's I²C1 Master/Slave. RX1: Input of the Deserializer's UART1.
47	GPIO4	GPIO4* MISO	GPIO4: Configurable General-Purpose Input or Output. Default is digital input with an internal 1MΩ pulldown to ground. MISO: SPI Master In Slave Out. When configured as master, push-pull output that drives data to external slave. When configured as slave, input with an internal 1MΩ pulldown to ground that receives data from external master.
48	GPIO5	GPIO5* SCLK SCL1_TX1	GPIO5: Configurable General-Purpose Input or Output. Default is open-drain output with an internal 1MΩ pulldown to ground. SCLK: SPI Clock. When configured as master, push-pull clock output. When configured as slave, clock input with internal 40kΩ pullup to V_{DDIO}. SCL1_TX1: Pass-Through UART1 Transmit/I²C1 Serial-Clock Input/Output with Internal 40kΩ pullup to V_{DDIO}. SCL1_TX1 has an open-drain driver and requires an external pullup resistor. SCL1: Clock Input/Output of the Deserializer's I²C1 Master/Slave. TX1: Output of the Deserializer's UART1.

PIN	NAME	FUNCTION MODE SIGNAL NAME (Default)	FUNCTION
25	GPIO6	SDIR* GPIO6 SDA2_RX2	SDIR: I²S/TDM Serial-Data Input with Internal 1MΩ Pulldown to Ground. Supports reverse audio from deserializer to serializer. GPIO6: Configurable General-Purpose Input or Output. Default is open-drain with internal 40kΩ pullup to V_{DDIO}. SDA2_RX2: Pass-Through UART2 Receive/I²C2 Serial-Data Input/ Output with Internal 40kΩ Pullup to V_{DDIO}. SDA2_RX2 has an open-drain driver and requires an external pullup resistor. SDA2: Data Input/Output of the Deserializer's I²C2 Master/Slave. RX2: Input of the Deserializer's UART2.
26	GPIO7	SCKIR* GPIO7	SCKIR: I²S/TDM Serial-Clock Input with Internal 1MΩ Pulldown to Ground. Supports reverse audio from deserializer to serializer. GPIO7: Configurable General-Purpose Input or Output. Default is open-drain I/O with 1MΩ pulldown to ground.
27	GPIO8	WSIR* GPIO8 SCL2_TX2	WSIR: I²S/TDM Serial-Word Select Input with Internal 1MΩ Pulldown to Ground. Supports reverse audio from deserializer to serializer. GPIO8: Configurable General-Purpose Input or Output. Default is open-drain I/O with 1MΩ pulldown to ground. SCL2_TX2: Pass-Through UART2 Transmit/I²C2 Serial-Clock Input/ Output with Internal 40kΩ Pullup to V_{DDIO}. SCL2_TX2 has an open-drain driver and requires an external pullup resistor. SCL2: Clock Input/Output of the Deserializer's I²C2 Master/Slave. TX2: Output of the Deserializer's UART2.
10	GPIO9	CXTP GPIO9* BNE SS1	CXTP: Coax/Twisted-Pair Select Input with an Internal 1MΩ Pulldown to Ground. State is latched at power-up. Set CXTP high for coax cable drive. Set CXTP low for twisted-pair cable. GPIO9: Configurable General-Purpose Input or Output. Default is push-pull output. BNE: When Configured as Slave, SPI Buffer Not Empty Push-Pull Output. When BNE is high, SPI data is available. SS1: SPI Slave Select. When configured as master, slave 1 select push-pull output.
11	GPIO10	GPIO10* RO SS2	GPIO10: Configurable General-Purpose Input or Output. Default is push-pull output. RO: When Configured as Slave, SPI Mode-Select Input with an Internal 1MΩ Pulldown to Ground. Setting RO high enables master read from MISO. Setting RO low enables master write to MOSI. SS2: SPI Slave Select. When configured as master, slave 2 select push-pull output.
22	GPIO11	ADD0 SD* GPIO11	ADD0: Address Selection Input with an Internal 1MΩ Pulldown to Ground. Latched at power-up. See Table 11. SD: I²S/TDM Serial-Data Push-Pull Output. Supports forward audio from serializer to deserializer. GPIO11: Configurable General-Purpose Input or Output. Default is open-drain I/O with 1MΩ pulldown to ground.
23	GPIO12	ADD1 SCK* GPIO12	ADD1: Address Selection Input with an Internal 1MΩ Pulldown to Ground. Latched at power-up. See Table 11. SCK: I²S/TDM Serial Clock Push-Pull Output. Supports forward audio from serializer to deserializer. GPIO12: Configurable General-Purpose Input or Output. Default is open-drain I/O with 1MΩ pulldown to ground.

PIN	NAME	FUNCTION MODE SIGNAL NAME (Default)	FUNCTION
24	GPIO13	ADD2 WS* GPIO13	ADD2: Address Selection Input with an Internal 1MΩ Pulldown to Ground. Latched at power-up. See Table 11. WS: I²S/TDM Word-Select Push-Pull Output. Supports forward audio from serializer to deserializer. GPIO13: Configurable General-Purpose Input or Output. Default is open-drain I/O with 1MΩ pulldown to ground.
7	GPIO14	SDA_RX* GPIO14	SDA_RX: UART Receive/I²C Serial-Data Input/Output with an Internal 40kΩ Pullup to V_{DDIO}. Function is determined by the state of I2CSEL at power-up. SDA: Data Input/Output of the Deserializer's I²C Master/Slave. RX: Input of the Deserializer's UART. GPIO14: Configurable General-Purpose Input or Output. Default is open-drain I/O with 40kΩ pullup to V_{DDIO}.
8	GPIO15	SCL_TX* GPIO15	SCL_TX: UART Transmit/I²C Serial-Clock Input/Output with an Internal 40kΩ Pullup to V_{DDIO}. Function is determined by the state of I2CSEL at power-up. SCL_TX has an open-drain driver and requires an external pullup resistor. SCL: Clock Input/Output of the Deserializer's I²C Master/Slave. TX: Output of the Deserializer's UART. GPIO15: Configurable General-Purpose Input or Output. Default is open-drain I/O with 40kΩ pullup to V_{DDIO}.
38	LOCK	LOCK	Open-Drain Lock Indication Output with an Internal 40kΩ Pullup to V_{DDIO}. If not used, leave unconnected.
12	ERRB	ERRB	When Selected as Error Output, ERRB is low when a Data Error or Interrupt is Detected. ERRB is high when PWDNB is low. Open-drain output with 40kΩ pullup to V_{DDIO}. If not used, leave unconnected.
21	PWDNB	PWDNB	Active-Low, Power-Down Input with an Internal 1MΩ Pulldown to Ground. Set PWDNB low to enter power-down mode.
MISCELLANEOUS—SEE Table 3			
13	X1/OSC	X1/OSC	Crystal/Oscillator Input. Connect to either a 25MHz crystal or 25MHz external clock source.
14	X2	X2	Crystal Input. Connect to one terminal of a 25MHz +200ppm crystal and connect a load capacitor from X1/OSC to ground (load capacitor value depends on crystal used).
16	XRES	XRES	External 402Ω Resistor Connection Between XRES and Ground. Used to calibrate SIO output driver swings.
15, 37	RSVD	RSVD	Reserved. Make no electrical connection to this pin.
POWER SUPPLY—SEE Table 3			
5, 6, 18	V_{DD18}	V_{DD18}	1.8V I/O Supply.
44	V_{DDIO}	V_{DDIO}	1.8-3.3V I/O Power Supply.
1, 2	V_{DD}	V_{DD}	Core Supply. Connect 1.0V ±5% external power supply or 1.2V ±5% supply to use internal 1.0V regulator.
9, 46	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1V Core Supply.
35	V_{DDEDP}	V_{DDEDP}	1V Power Supply for eDP Transmitter. MUST provide low resistance trace to CAP_VDD Pin 46.
EP	EP	VSS	Exposed Pad. EP is internally connected to device ground. EP MUST be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagrams

Functional Block Diagram



*AVAILABLE ONLY ON THE MAX96774

Recommended Operating Conditions

Table 2. Recommended Operating Conditions

PARAMETER	PIN NAME	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V_{DD18}		1.7	1.8	1.9	V
	V_{DDEDP}, V_{DD} (not using internal regulator)		0.95	1.0	1.05	V
	V_{DD} (using internal regulator)		1.14	1.2	1.26	V
	V_{DDIO}	1.8V	1.7	1.8		V
		3.3V		3.3	3.6	V
Maximum Supply Noise Supply Noise < 1MHz	V_{DD18}			25		mVp-p
	V_{DD}, V_{DDEDP}			25		mVp-p
	V_{DDIO}	1.8V		50		mVp-p
		3.3V		100		mVp-p
Operating Junction Temperature, T_J			-40		+125	ºC

External Component Requirements

See Figure 23 and Figure 24.

Table 3. External Component Requirements

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
XRES	R_{XRES}		402 ±1%. Use a single resistor	Ω
Line Fault Pulldown Resistor	R_{PD}	Install if the attached serializer is using the Line Fault Monitor.	49.9 ±1%	kΩ
Link Isolation Capacitors	C_{LINK}	Place close to the SIO pins (3, 4, 19, 20) used in the application.	0.1	µF
Coax Mode Termination Resistor	R_{TERM}	In coax mode, connect R_{TERM} between unused SIO_ pin and ground on each coax link.	49.9 ±1%	Ω
Crystal		Place as close as possible to pins 13 and 14.	25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values which compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible to pins 13 (X1/OSC) and 14 (X2).	Application specific	
V_{DDIO} Decoupling Capacitors*		Place a 0.1µF capacitor as close as possible to pin 44. Include a minimum of 10µF bulk decoupling on the PCB.	0.1 + 10	µF
V_{DD18} Decoupling Capacitors*		Place a 0.01µF capacitor as close as possible to pin 18. Place a 0.1µF capacitor as close as possible to pins 5 and 6. Run separate traces from each pin to the capacitor. Include a minimum of 10µF bulk decoupling on the PCB.	0.01 + 0.1 + 10	µF
V_{DD} Decoupling Capacitors*		Place a 0.1µF capacitor as close as possible to pins 1 and 2. If the internal V_{DD} regulator is used, include a minimum of 20µF bulk decoupling on the PCB. If the internal V_{DD} regulator is not used, include a minimum of 10µF bulk decoupling on the PCB.	0.1 + 20 or 10	µF

Table 3. External Component Requirements (continued)

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
CAP_VDD Decoupling Capacitors		Place 0.1µF capacitors as close as possible to pins 9 and 46. If the internal V_{DD} regulator is used, include a 47µF bulk decoupling capacitor on this node. If the internal V_{DD} regulator is not used, include a 10µF capacitor.	(2) 0.1 + 47 or 10	µF
V_{DDEDP} Decoupling Capacitors		Connect pin 35 to CAP_VDD pin 46 with a very low resistance (< 10mΩ) trace. Place a 1nF capacitor as close as possible to pin 35, with a 10µF capacitor in parallel.	0.001 + 10	µF
eDP Source Isolation Capacitors	C_{TX}	Two required per lane. See Figure 13.	75–265	nF
eDP Sink Isolation Capacitors	C_{RX}	Optional. Two required per lane if used. See Figure 13.	75–265	nF
eDP Pulldown Resistors	R_{EPD}	Required only if C_{RX} is used. Two required per lane if used. See Figure 13.	100k–1M	Ω
eDP AUX Isolation Capacitors	C_{AUX}	Two required. See Figure 14.	75–200	nF
Open-Drain Pullup Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations.	Application specific	

* With the exception of CAP_VDD, power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

Functional Diagrams

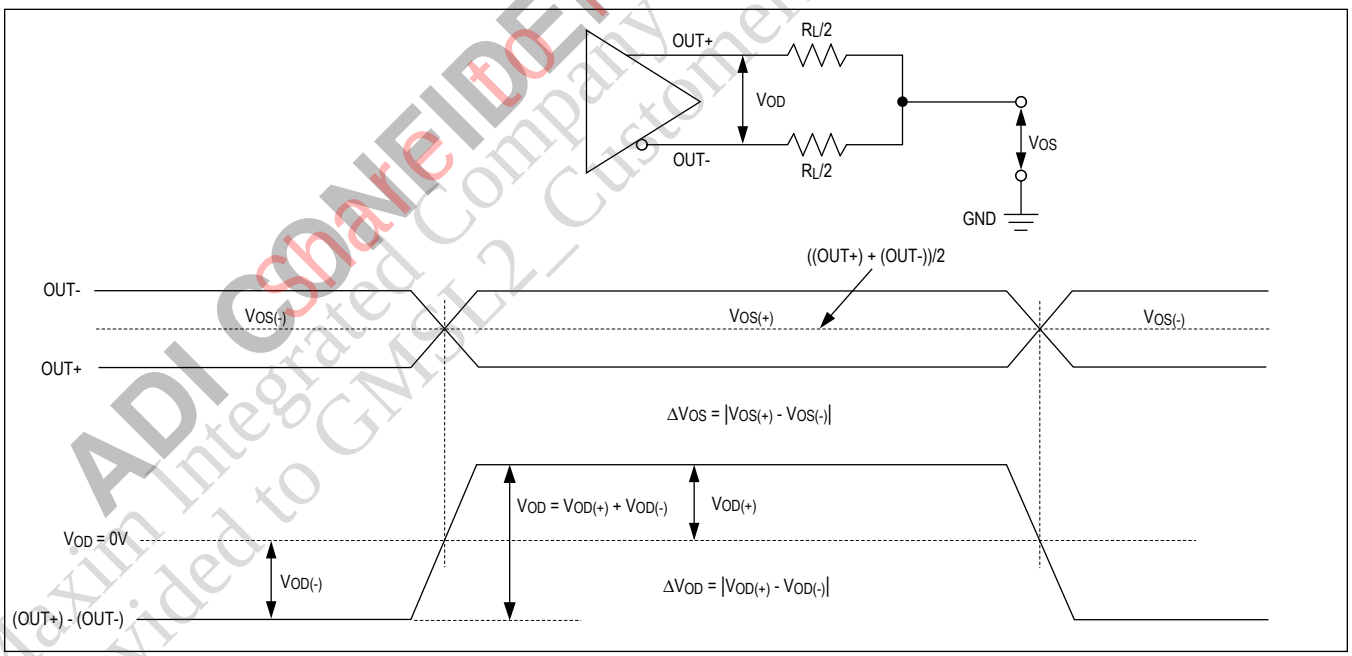


Figure 1. Serial Output Parameters

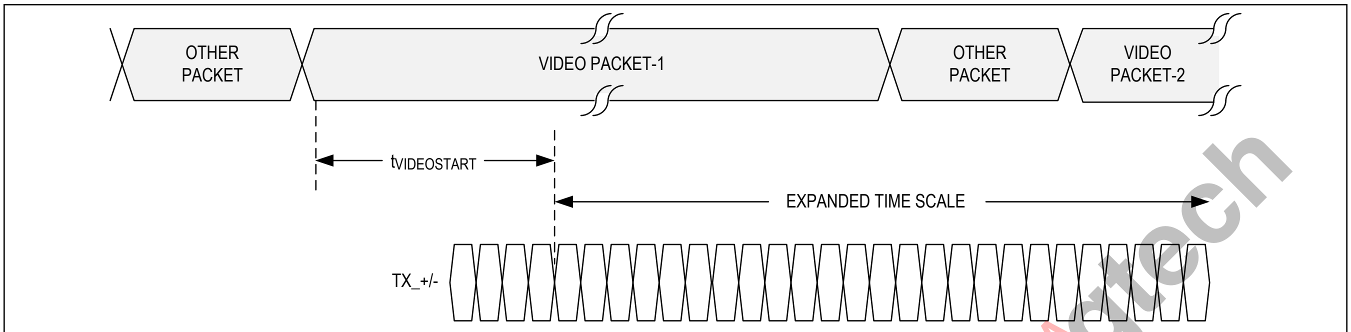


Figure 2. Video Initialization Time

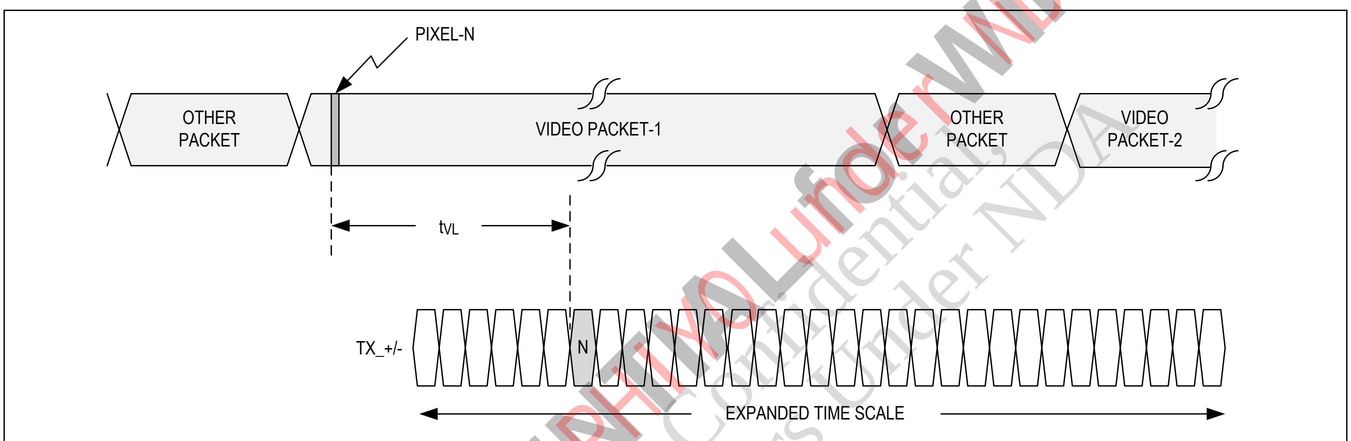


Figure 3. Video Latency

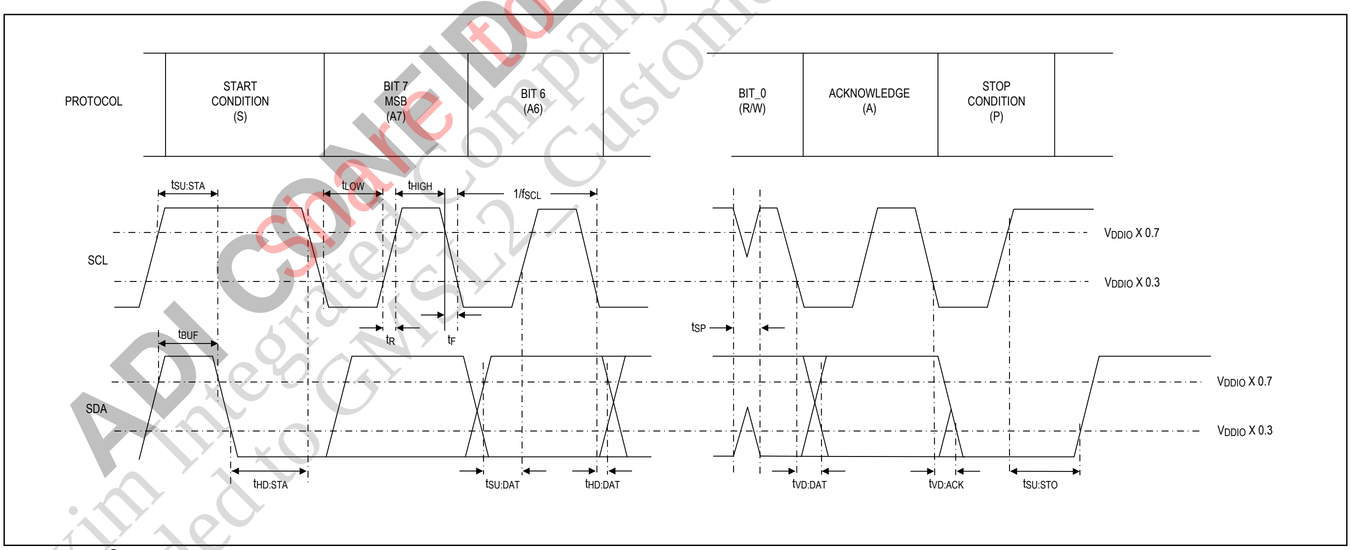


Figure 4. I²C Timing Parameters

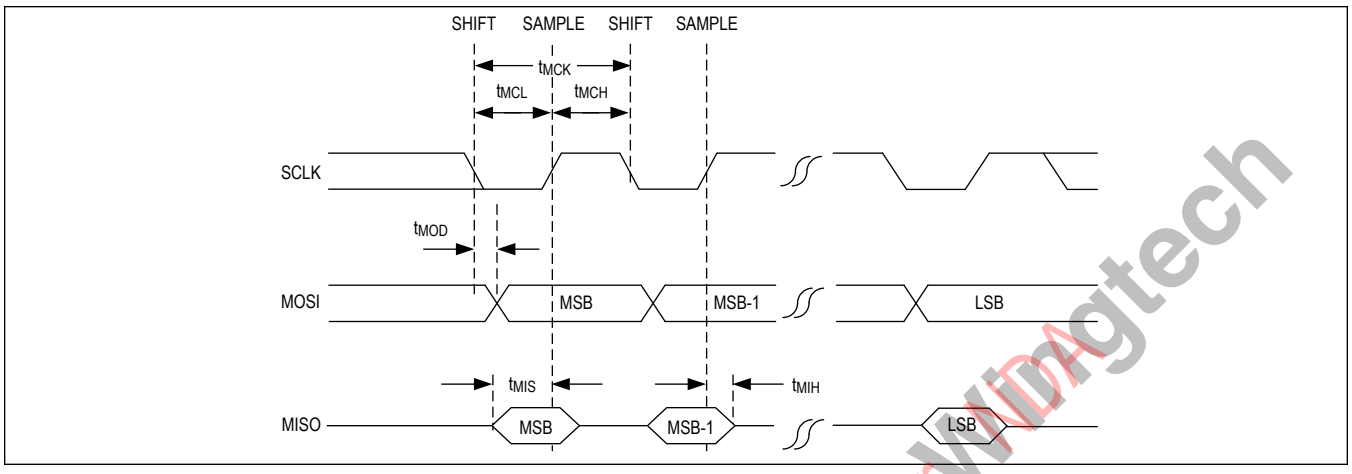


Figure 5. SPI Master Mode Timing Parameters

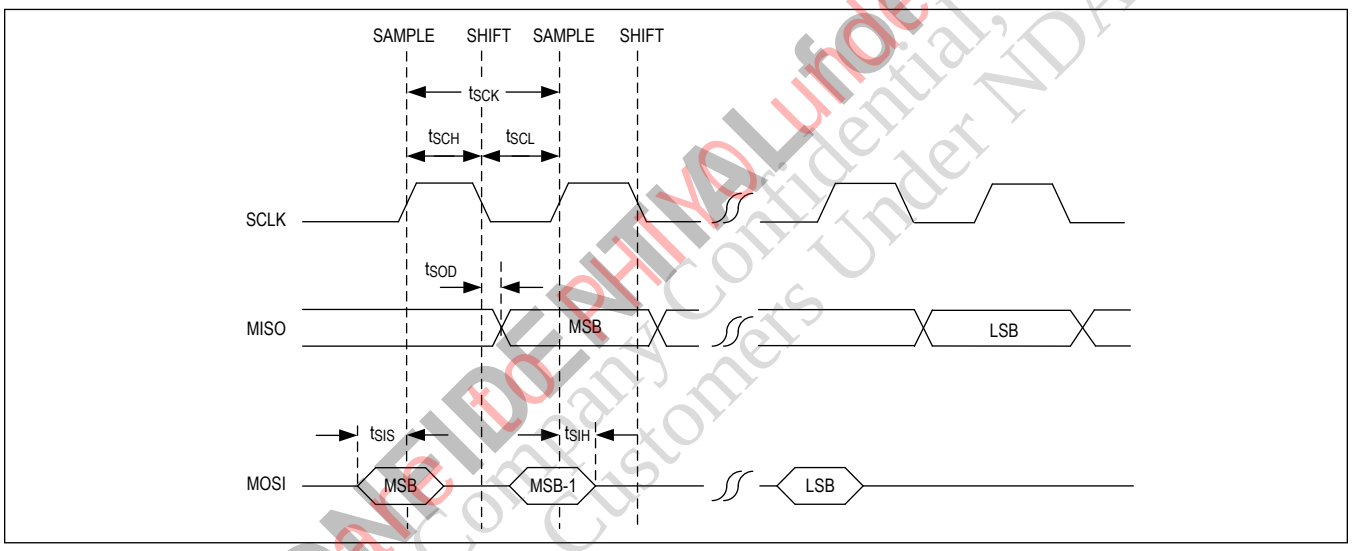


Figure 6. SPI Slave Mode Timing Parameters

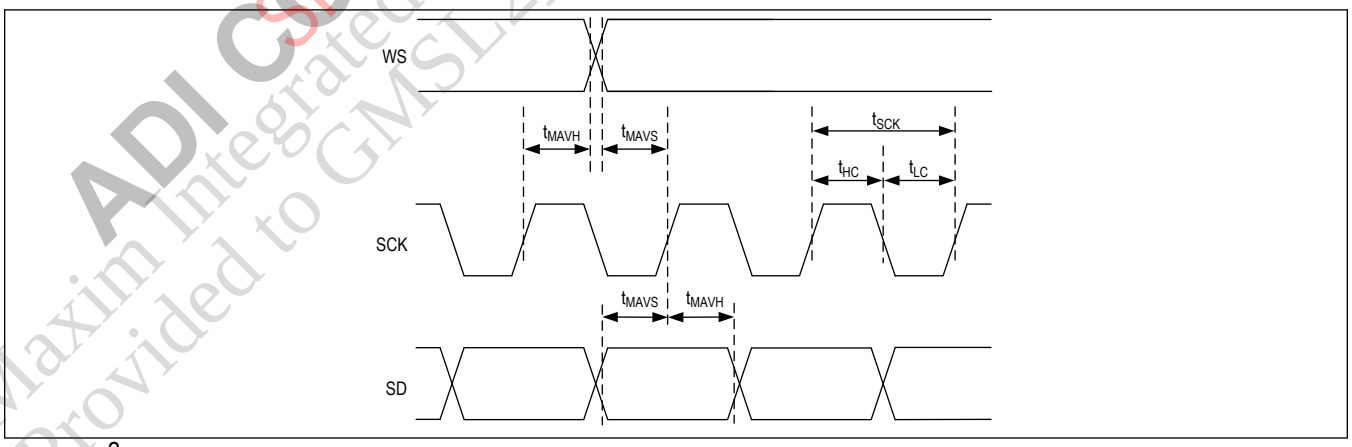


Figure 7. I^2S Master Mode Timing Parameters

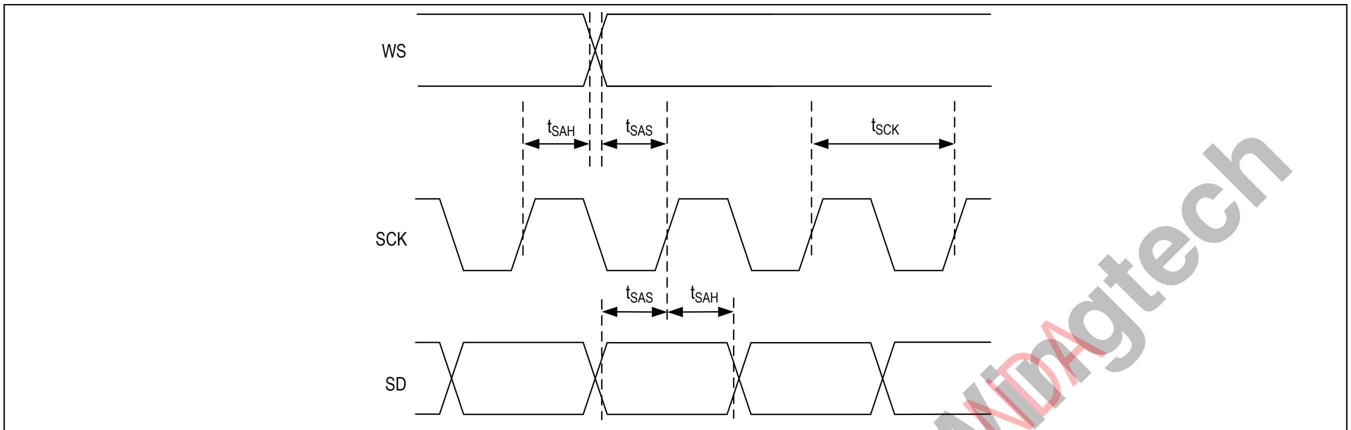


Figure 8. I²S Slave Mode Timing Parameters

Detailed Description

Additional Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews, and register definitions. Designers must also have the following information to correctly design using this device:

- The **GMSL2 Channel Specification** contains physical layer requirements for the PCB traces, cables, and connectors that constitute the GMSL2 link.
- The **GMSL2 Hardware Design Guide** contains recommendations for PCB design, application circuits, selection of external components, and guidelines for use of GMSL2 signal integrity tools.
- The **GMSL2 User Guide** contains detailed programming guidelines for GMSL2 device features.
- **Errata sheets** are specific to part number and revision ID and contain deviations from published device specifications.

Note: To receive these documents, and additional guidance on MAX96772/MAX96774 features, contact the factory.

Introduction

Maxim's GMSL2 serializers and deserializers provide sophisticated link management for high-speed, low bit error rate, serial data transport. They support a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL2 provides up to 6Gbps forward and 1.5Gbps reverse (device specific) packetized data transmission over each fixed-speed link. Devices with two GMSL2 links provide a total capacity of up to 12Gbps and 3Gbps reverse in specific configurations.

The following sections provide a brief overview of the device functions and features.

Note: For additional information and details on the configuration of each function and feature, contact the factory.

Product Overview

The MAX96772/MAX96774 convert a single or dual GMSL2 input to a single-stream transport (SST), embedded DisplayPort (eDP) v1.4a output for driving display panels. They support eDP link rates from 1.62Gbps/lane (R162) to 8.1Gbps/lane (R810). Forward GMSL2 link rates of 3Gbps and 6Gbps and a reverse-link rate of 187.5Mbps are provided. Only asynchronous clocking of the RGB888 video format is supported.

The MAX96772/MAX96774 provide decompression of video streams with VESA 3:1 display stream compression (DSC). This enables up to 600MHz pixel clocks and the transport of 4K (UHD), 24-bit, 60Hz video over a single coax or twisted pair cable. Forward error correction (FEC) of compressed video on the GMSL2 link significantly reduces the potential for bit errors.

Support for DSC and FEC is provided only on GMSL2 PHYA (SIOA).

While using decompression, the maximum horizonal and vertical resolutions are 5760 pixels/line and 4096 lines. Higher resolutions are available for uncompressed video.

Note: For more information on specific applications, contact the factory .

The MAX96774 adds HDCP 1.4 and HDCP 2.3 decryption. After HDCP is configured, the authentication and key exchange are fully automated without requiring additional external µC involvement.

Deserializer Modes

The MAX96772/MAX96774 support single-stream video over one or two GMSL2 links, with or without compression. Figure 9 through Figure 11 provide an overview of typical configurations.

Uncompressed Video, Single GMSL2 Link

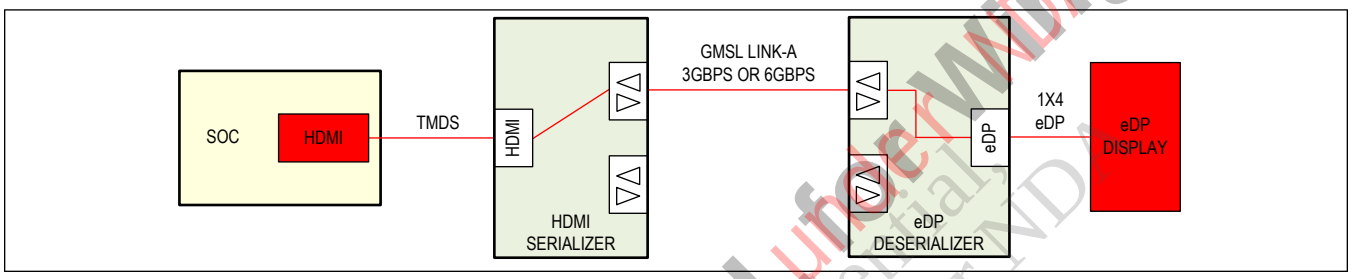


Figure 9. Uncompressed Video Stream over Single GMSL2 Link

The GMSL2 link can be configured with 3Gbps or 6Gbps bandwidth. Any serializer that is Maxim GMSL2-compatible can be used. Either MAX96772/MAX96774 GMSL2 port can be paired with either serializer GMSL2 port. A maximum of approximately 215MHz PCLK can be transmitted uncompressed over a 6Gbps link. This supports a single stream of 2560x1080, 24-bit, 60Hz, or equivalent video. At 3Gbps, a link can support up to 105MHz uncompressed. This supports 1920x720, 24-bit, 60Hz, or equivalent video.

As shown in Figure 9, the MAX96774 provides HDCP 1.4 decryption on either link and HDCP 2.3 on link A.

Uncompressed Video, Dual GMSL2 Links

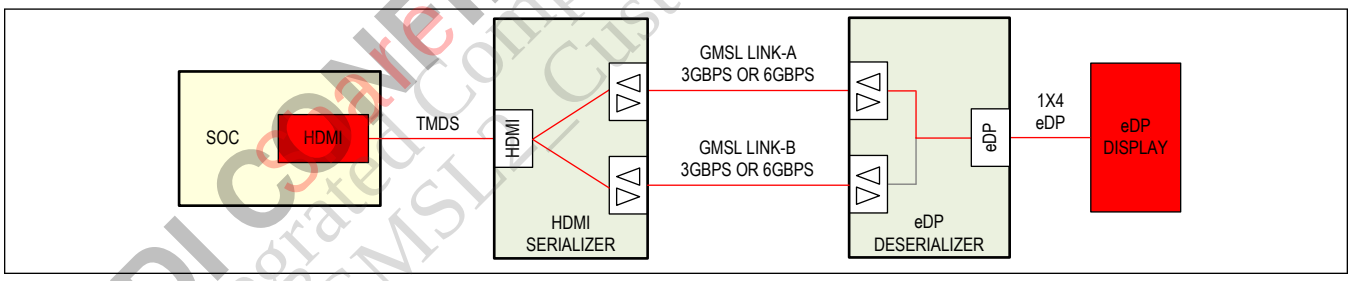


Figure 10. Uncompressed Video Stream over Dual GMSL2 Links

The GMSL2 links can be configured identically with 3Gbps or 6Gbps bandwidth. Any serializer that is Maxim GMSL2-compatible can be used. The serializer sends video and side-channel data over the A link until the total bandwidth utilization exceeds the A link capacity. Above this utilization, the data is split equally over the A and B links.

A maximum of approximately 215MHz PCLK can be transmitted uncompressed over each 6Gbps link. At 3Gbps, each link can support up to 105MHz uncompressed. The MAX96772/MAX96774 support a maximum combined PCLK of 430MHz.

As shown in Figure 10, the MAX96774 provides HDCP 1.4 decryption on both the links.

Compressed Video over Single GMSL2 Link

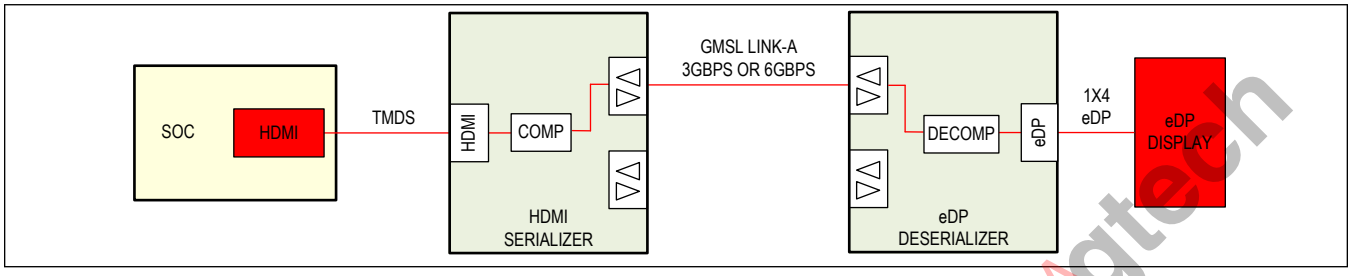


Figure 11. Compressed Video Stream over Single GMSL2 Link

The MAX96772/MAX96774 support decompression of VESA 3:1 compressed video on the A link. Any serializer that is Maxim GMSL2-compatible and supports compression can be used. The link can be programmed to 6Gbps or 3Gbps. A maximum of approximately 600MHz PCLK can be transmitted over a 6Gbps link. This supports 3840x2160 (UHD), 24-bit, 60Hz or equivalent video over a single coax or STP cable. A 3Gbps link supports approximately 300MHz PCLK.

As shown in Figure 11, the MAX96774 provides HDCP 1.4 or HDCP 2.3 decryption on the A link.

Other Functions

The GMSL2 serializers and deserializers have a main I^2C/UART control channel interface that an ECU uses to access serializer and deserializer registers, as well as peripheral devices, from either end of the link. Each device also has 2 pass-through I^2C/UART channels available for local or remote peripheral control. The pass-through I^2C/UART channels do not have access to the serializer and the deserializer registers.

The MAX96772/MAX96774 support both forward (serializer to deserializer) and reverse (deserializer to serializer) audio channels. The audio channels support I^2S stereo and up to 8 channels in TDM mode. Sample rates of 32kHz to 192kHz are supported with a sample depth from 8 bits to 32 bits.

The MAX96772/MAX96774 include an SPI master/slave interface, including two slave select pins, for peripheral control. The SPI interface enables a host SPI master on one side of the GMSL2 link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link or can swap ends by reprogramming the GMSL2 devices (a GMSL2 device can be configured as an SPI master or slave).

The MAX96772/MAX96774 provide up to 16 GPIOs, which depends on device feature utilization. GPIOs are typically used to tunnel low speed (<100kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in either the forward or reverse direction.

The devices include a watermark detector to verify that the video image is not frozen.

The GMSL2 devices incorporate several link margin optimization and monitoring functions to ensure high link margins. Continuous (1Hz) adaptive equalization optimizes link margin to adapt to environmental changes and cable aging. An eye-opening monitor function for continuous link margin diagnosis with various threshold alarm levels is available for runtime alerts of link degradation. PRBS checking verifies the correct link and video channel operation.

GMSL2 Protocol

The GMSL2 is a fixed-rate transmission medium that is designed to carry multiple types of communication channels concurrently. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator or an external reference frequency. The link clock is completely independent of the video pixel clock.

The GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. The maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. In most cases, the available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth.

The same data protocol is used on forward and reverse channels and for both video and control-channel data.

GMSL2 Physical Layer

Maxim's GMSL2 family of serial links has transmitter and receiver capability enabled simultaneously, allowing full-duplex operation on a single wire. A single cable between the serializer and the deserializer delivers data transmitted from each end of the link. Forward transmission refers to data being sent from the serializer to the deserializer. Reverse transmission refers to data being sent from the deserializer to the serializer.

The available forward rate options for both coax and STP links are fixed at 3Gbps or 6Gbps, with defaults of 6Gbps for coax and 3Gbps for STP. The MAX96772/MAX96774 reverse link rate is fixed at 187.5Mbps. Both forward and reverse rates are doubled in a dual-link configuration, in which a serializer and a paired deserializer are connected using two links. Dual-link mode is not available in all GMSL2 device configurations.

Cabling Options

To achieve robust full-duplex link performance, cable attenuation and return loss characteristics must stay within the requirements of the GMSL2 Channel Specification. These requirements vary with the selected link rate. The available link rates and GMSL2 adaptive equalization enable support of a wide range of cabling options.

Coax or STP mode and data rates are configured upon startup and determine which cabling option applies. For more information, see the *Latch-On-Power-Up Pins* section. The forward link rate may be programmed to either 3Gbps or 6Gbps in either Coax or STP configurations.

In coax mode, use the noninverted SIO pin only. AC-couple and terminate the inverting SIO pin using the series connection of a 100nF capacitor and a 49.9Ω resistor. In STP configuration, both the noninverted and inverted SIO pins are enabled by default. If one of the GMSL input ports is not used, leave both pins unconnected.

Maximum cable length is limited by the frequency-dependent attenuation of the cable. Additionally, PCB and in-line connectors degrade the return loss characteristic of the cable assembly. The GMSL2 channel specification allows two inline connectors and provides detailed requirements for cable attenuation and return loss, as well as insertion loss and return loss requirements for PCB traces. In general, any physical channel implementation that is compliant with the GMSL2 channel specification can be used with reliable results.

Note: To receive the GMSL2 Channel Specification document, contact the factory .

A 100nF AC coupling capacitor is normally used for GMSL2 links. For typical GMSL2 serial link configurations, see Figure 23 and Figure 24.

GMSL2 Bandwidth Sharing

The GMSL forward bandwidth is shared among the video, the I^2C/UART control channel, pass-through I^2C/UARTs, I^2S/TDM audio, SPI, and GPIOs, as well as various protocol-specific data exchanges (i.e., info frames, sync, and acknowledgments). The reverse channel bandwidth is also shared with all the above, with the exception of video packets.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

Link bandwidth is shared flexibly between the various communication channels requesting the link for packet transmissions. This flexibility comes from the packet-based transmission format and dynamic bandwidth allocation: if a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol limits the maximum packet size in order to prevent 1 single channel from monopolizing the link bandwidth and to ensure other channels are served.

The video and control channel packets can be assigned a priority level. There are four priority levels: low, normal, high, and urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with maximum latency requirements can be assigned an increased priority.

GMSL2 Bandwidth Calculations

The GMSL2 forward link has a fixed link rate of 3Gbps or 6Gbps. The MAX96772/MAX96774 reverse link rate is fixed at 187.5Mbps. The GMSL2 protocol overhead is approximately 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

Worst-case applications must not exceed the available throughput of the forward and reverse links. Maxim's evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that estimates initial bandwidth requirements. Maxim also has other tools that are useful for calculating link bandwidth utilization. For high-bandwidth use cases, consult the factory to ensure

error-free performance.

Table 4 provides rough estimates of the bandwidth utilization for each of the communication channels.

Table 4. Forward and Reverse Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video (Forward Path Only)	**Without VESA DSC compression** PCLK x (bpp + 0.5 + packet_CRC) x 10/9 x 2048/1047 x 128/120* (*only applies when GMSL FEC is enabled. GMSL FEC must be used with GMSL3 PAM4 modulation) **With VESA DSC compression** PCLK x (bpp + 0.5 + packet_CRC) x 10/9 x 2048/2047 x 128/120 x 1/3 (GMSL FEC must be used with VESA DSC compression)
I^2C	13 to 40 x I^2C clock rate
UART	6 x UART bit rate
SPI	1.7 to 3.1 x SPI rate, depending on SPI byte length
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled
I^2S/TDM	BW = sample_rate x 20 x (roundup(channelcnt x sample_depth/18 + 0.5) + 2)

Definitions:

- PCLK = Total Horizontal pixels x total Vertical lines x frame rate. Horizontal includes blanking pixels and Vertical includes blanking lines.
- bpp = bits per pixel, typically 24
- packet_CRC = 0.5 if packet CRC is enabled, 0 if not enabled. Packet CRC is disabled by default.
- sample_rate = audio sample rate (samples per second)
- channelcnt = number of audio channels
- sample_depth = bits per sample per audio channel (must be the same for all channels)

Power Supplies

The MAX96772/MAX96774 offer an array of power supply configuration options.

The 1V core supply can be provided directly or by an internal LDO regulator. For optimal power efficiency, connect 1.0V ±5% to V_{DD}. When using the internal regulator, connect 1.2V ±5% to V_{DD} and after power-up write LDOH_EN = 1 and LDOH_TEST_MODE = 1 in register REGLR_CTRL. Internal logic senses the voltages at V_{DD} and CAP_VDD. If V_{DD} < 1.1V and CAP_VDD < 1.05V, the regulator is disabled and low-resistance switches connect V_{DD} to the internal supply rails.

Power for the eDP outputs is supplied via pin V_{DDEDP}. Connect this pin to a CAP_VDD pin as detailed in Table 3.

The V_{DDIO} supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing with the MAX96772/MAX96774. The allowable supply voltage range is 1.7V (1.8V -6%) to 3.6V (3.3V +9%).

V_{DD18} is the primary analog supply. Connect 1.8V ±5%.

Proper power supply bypassing of all supplies is essential for high-frequency circuit stability. For more information, see Table 3. For power supply tolerances and noise requirements, see Table 2.

Note: For guidance on sharing supplies and optimizing supply decoupling, contact the factory.

Power supply ramp-time recommendation: 20µs < ramp time < 2ms. Power supply ramps should be monotonic. Once the supply voltage reaches the minimum supply voltage limit, it should not be allowed to drop below the specification.

Thermal Management

The power consumption of GMSL2 devices varies depending on how the device is used. Care must be taken by the user to provide sufficient heat dissipation with proper board and cooling design techniques. The package exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

To meet electrical specifications and avoid impacting device reliability, the system thermal management must keep the operating junction temperature below 125°C .

For guidance, refer to the *Tutorial 4083, Thermal Characterization of IC Packages*.

Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. All GMSL2 devices support the following interfaces:

- Main I^2C/UART (internal access)
- Pass-through I^2C/UART
- SPI
- GPIO

Some GMSL2 devices also support the following interfaces:

- I^2S/TDM Audio
- RGMII/RMII

All of the above interfaces can pass data through the GMSL2 link, but only the GMSL2 device registers can be accessed and configured through the main I^2C/UART interface.

The side channel and its various interfaces are accessed using multifunction GPIO pins—MFPs on some devices—(except for RGMII/RMII, which uses dedicated pins). Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit on the number of pins available on a given device, not all interfaces can be simultaneously supported. For default and alternate multifunction pin functions, as well as available combinations of interfaces, see Table 7 and the *Pin Description* section.

Main I^2C/UART

The main I^2C/UART is located on the SDA_RX and SCL_TX pins of each GMSL2 device. The I^2C (SDA, SCL) or UART (Tx, Rx) interface is selected by the CFG0 or I2CSEL configuration pin state at power-up (see the *Latch-On-Power-Up Pins* section). The selected interface provides master access to GMSL2 registers and peripheral device registers from either end of the link.

The master µC can be located at either end of the link (usually the serializer side for display applications and the deserializer side for camera applications). The MAX96772/MAX96774 support dual master microcontrollers provided that software arbitration (such as token passing) is used to prevent packet collisions. To avoid control channel bus contention in dual master configurations, it is recommended to disable the remote channel using the bit field DIS_REM_CC.

To configure peripheral devices over the link, the GMSL2 serializer and deserializer must use the same control channel interface (both I^2C or both UART). Unlike GMSL1 devices, there is no I^2C-to-UART conversion capability. I^2C/UART outputs are open drain and require appropriately-sized external pullup resistors for proper operation.

For detailed main channel programming information, see the *Control-Channel Programming* section.

Pass-Through I^2C/UART

The GMSL2 devices have 2 pass-through I^2C/UART channels. These channels have no access to the registers in either the GMSL2 serializer or the deserializer; they simply pass the I^2C or UART signal across the GMSL2 link. This allows I^2C channels to be separated so that multimaster conflicts do not occur. The operating mode of the UART2 tunnel must be selected before it is enabled. I^2C/UART outputs are open drain and require appropriately-sized external pullup resistors for proper operation.

SPI

The GMSL2 enables a host SPI master on one side of the GMSL2 link to control a peripheral SPI slave on the opposite side. Communication may be in either direction across the GMSL2 link. Although multiple SPI peripherals may be connected, it is recommended that only one be communicated with at a time.

Note: For guidance on configuring SPI connections, contact the factory.

The SPI clock range is 600kHz to 25MHz in Master mode and 600kHz to 50MHz in Slave mode. Care must be taken to meet setup and hold time requirements when operating at speeds higher than 20MHz. For more information, see the

Speed Programming for SPI and I²S section.

I²S/TDM Audio

The GMSL2 devices for display applications support I²S stereo and up to 8 channels of audio in TDM mode. In GMSL2 mode, most devices have 2 audio channels – one in the forward direction and one in the reverse direction. Sample rates of 8kHz to 192kHz and sample depths of 8- to 32-bits are supported. In GMSL2 mode, the maximum SCK frequency is 49.152MHz. For system flexibility, GMSL2 devices can act as either the slave or the master at either end of the link.

Control Channel Latencies

Table 5. Typical Control Channel Latencies

FUNCTION	FORWARD (µs)	REVERSE (µs)	NOTES
I²C	< 10	< 10	
UART	< 10	< 10	
Audio	< 100	< 100	For typical use cases
SPI	< 10	< 10	Round trip
Ethernet	< 10	< 10	Specific parts only

General-Purpose Inputs and Outputs (GPIO)

GPIOs are typically used to pass low speed (<100kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition based; a GPIO packet is created and transmitted on the GMSL2 link when a rising or falling edge transition is detected at a GPI pin. The transition is regenerated at a GPO on the other end of the link.

The multifunction pins GPIO can be programmed as GPI (input), GPO (push-pull output or open-drain output), or GPIO (bidirectional input/output). Each GPIO can also be programmed for 1MΩ or 40kΩ pullup or pulldown (or none). Although an internal pullup is provided, high-speed open-drain outputs require an appropriate value of an external pullup resistor to V_{DDIO}. Inputs cannot be left unconnected. Always ensure that every pin configured as an input has a pullup or pulldown programmed or is driven by another IC.

A GPI on one side of the serial link can be mapped to a single GPO or multiple GPOs on the other side of the link. Each GPI is assigned a pin ID with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0–GPIO0, GPIO1–GPIO1, GPIO2–GPIO2, etc. However, the GPIO mapping can be arbitrarily changed through register settings.

GPI transitions can be transmitted in two modes: delay-compensated and non-delay-compensated. When delay compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases, but jitter and skew decrease.

The state of each GPIO can be read or written by the register either locally or remotely over the GMSL2 link by a µC using the control channel I²C/UART interface.

In non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as link bandwidth is available. This variable delay is a result of multiple communication channels sharing the link. Non-delay-compensated mode should be used with signals tolerant to delay variation (i.e., µC interrupts).

Typical GMSL2-only device delays for 6Gbps forward and 187Mbps reverse link rates are shown in Table 6.

Table 6. Typical GPIO Delays for Forward and Reverse Link Transmission

	DELAY COMPENSATION	DELAY
GPIO forwarding from serializer to deserializer (6Gbps forward channel)	0	720ns
	1	3.5µs
GPIO forwarding from deserializer to serializer (187Mbps reverse channel)	0	6µs
	1	15µs

Multifunction GPIO Pin Assignments

The side-channel functions, such as pass-through I²C/UART, SPI, and audio, are enabled by programming multifunction GPIO pins. Each pin has several possible functions, but only one can be used at a time.

Some functions require only a single pin, but most are implemented across a group of pins. For example, VS is a single pin, but SPI requires several pins. The user selects pin functions to suit their use-case by programming the appropriate registers.

The *Pin Description* table shows the default and alternate functions for each GPIO pin.

The pins are grouped by speed settings with different output rise and fall times to facilitate optimizing for the different speed requirements of the different functions. Each pin is placed in one of three speed groups (A, B, or C), with each speed group having a default output transition time. The transition time of each speed group can be changed from the default value by register programming. However, if the pass-through I²C/UART function is selected, the transition time of these specific pins is fixed (at I²C speed) independent of the group's setting. The main channel I²C/UART is always fixed at I²C speed.

Table 7 shows how latch-on power-up, I²C/UART, audio, SPI, and other functions are mapped to the GPIO pins.

The transition times depend on the transition time setting and the V_{DDIO} supply voltage. For typical transition times, see Table 8.

Table 7. GPIO Pin Function Map

PIN	LATCH-ON POWER-UP	I²C/UART	AUDIO	SPI	OTHER FUNCTIONS	POWER-UP DEFAULT	SPEED GROUP AND (DEFAULT TTS)
GPIO0					HS	GPIO0	Group C (10)
GPIO1	I2CSEL				VS	GPIO1	Group C (10)
GPIO2		MS			WMD	GPIO2	Group C (10)
GPIO3		Pass-through #1 SDA/RX		MOSI		GPIO3	Group B (01) / I²C
GPIO4				MISO		GPIO4	Group B (01)
GPIO5		Pass-through #1 SCL/TX		SCLK		GPIO5	Group B (01) / I²C
GPIO6		Pass-through #2 SDA/RX	Rev Path SD			SDIR	Group C (10) / I²C
GPIO7			Rev Path SCK			SCKIR	Group C (10)
GPIO8		Pass-through #2 SCL/TX	Rev Path WS			WSIR	Group C (10) / I²C
GPIO9	CXTP			BNE, SS1		GPIO9	Group B (01)
GPIO10				RO, SS2		GPIO10	Group B (01)
GPIO11	ADD0		Fwd Path SD			SD	Group A (01)
GPIO12	ADD1		Fwd Path SCK			SCK	Group A (01)
GPIO13	ADD2		Fwd Path WS			WS	Group A (01)
GPIO14		Main channel SDA/ RX				SDA_RX	I²C

Table 7. GPIO Pin Function Map (continued)

PIN	LATCH-ON POWER-UP	I²C/UART	AUDIO	SPI	OTHER FUNCTIONS	POWER-UP DEFAULT	SPEED GROUP AND (DEFAULT TTS)
GPIO15		Main channel SCL/ TX				SCL_TX	I²C

Table 8. Control and Side Channel Typical Rise and Fall Times

TRANSITION TIME SETTING (TTS)	RISE TIME*		FALL TIME**	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
00	1.0ns	0.6ns	0.8ns	0.5ns
01	2.1ns	1.1ns	2.0ns	1.1ns
10	4.0ns	2.3ns	4.3ns	2.3ns
11	9ns	5ns	10ns	5ns
I²C	*	*	40ns	30ns

* 20 to 80%, 10pF load. Rise time is for push-pull output configuration. Rise time for open-drain outputs depends on external pullup resistor value.

** 80 to 20%, 10pF load.

Dedicated outputs ERRB and LOCK are in Group C.

Speed Programming for SPI and I²S

The SPI and I²S interfaces may be used over a wide range of frequencies. The MAX96772/MAX96774 provide flexible GPIO speed programming to maintain timing margins while minimizing radiated EMI.

Table 9 and Table 10 provide guidance on recommended speed settings for various I²S and SPI operating frequencies and V_{DDIO} supply voltages. For GPIO pin speed programming information, see Table 8.

At lower frequencies, SPI data is typically latched on the opposite clock edge from which it is shifted. For more information, see Figure 5 and Figure 6. However, at higher frequencies, the data must be latched on the same edge as the shift to meet setup and hold time requirements. Table 10 provides guidance on programming the latching clock edge.

Table 9. Recommended I²S Pin Programming

FREQUENCY (MHz)	V_{DDIO} (V)	RECOMMENDED SPEED SETTING
< 25	1.7–2.24	01
	2.25–3.6	10
25–50	1.7–2.24	00
	2.25–3.6	01

Table 10. Recommended SPI Pin Programming

FREQUENCY (MHz)	V_{DDIO} (V)	LATCHING EDGE	RECOMMENDED SPEED SETTING
< 12.5	1.7–2.24	Opposite from data shifting edge	01
	2.25–3.6		10
12.5–25	1.7–2.24	Opposite from data shifting edge	00
	2.25–3.6		01
25–50	1.7–2.24	Same as data shifting edge	00
	2.25–3.6		01

Latch-On-Power-Up Pins

The logic states at specific configuration input pins are latched on power-up. These states set initial register values and functional modes that cannot be easily programmed through I²C or UART after the IC powers up. Bias the pins to V_{DDIO} for a logic 1, or GND for a logic 0, using sufficiently high-value resistors (up to 10kΩ). Make sure that the voltage seen at the pin is at a valid logic level to ensure proper latching. All latch-on-power-up pins also double as general-purpose output-only pins after power-up. Before the pin states are latched, the chip does not drive the pin. GPIO pins that also function as latch-on-power-up pins should be used only as outputs unless the user can guarantee that the proper pin logic state is present at the pin at power-up. When the pin is used as an output, the pin should not be driven externally, and the power-up state is solely determined by the external resistor.

A list and description of latch-on-power-up bits are shown here:

ADD2, ADD1, ADD0: These bits set the device address (DEV_ADDR) that is used as the slave address by I²C and UART. They also set the default value of the TX_SRC_ID registers of each low bandwidth channel (Audio, Info-Frame, I²C, UART, SPI, GPIO). Device addresses can be changed after power-up by writing to the DEV_ADDR register. For more information, see Table 11.

CXTP: This bit sets the device into coaxial or twisted-pair mode, with the value reflected in both register bits CXTP_A and CXTP_B. This bit can be changed after power-up, as one link may be set as coax and the other as twisted-pair. CXTP = 0 sets differential mode operation at a 3Gbps GMSL2 forward link rate, while CXTP = 1 sets single-ended coax operation at a 6Gbps GMSL2 forward link rate. The default reverse channel rate is set to 187.5Mbps, independent of the CXTP setting.

I2CSEL: This bit selects either UART or I²C mode for internal register access and remote (over GMSL2 link) control channel communication. Set I2CSEL = 0 for UART or I2CSEL = 1 for I²C.

Table 11. Device Address Table

ADDRESS BITS ADD[2:0]	DEVICE ADDRESS
000	0x90
001	0x94
010	0x98
011	0xD0
100	0xD4
101	0xD8
110	0x50
111	0x54

Clocking

GMSL Reference Clock

The GMSL2 devices require a reference clock source to generate the 6GHz line rate clock and associated internal clocks. Both the serializer and the deserializer can be clocked with an external 25MHz crystal or an external clock source with a frequency accuracy of ±200ppm.

Spread-Spectrum Clocking

Maxim's GMSL2 links provide exceptional EMI performance. Optional spread-spectrum clocking (SSC) is available to reduce electromagnetic interference emitted from devices and interconnections and to provide additional margin. The SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile and is programmable to deviate up to ±2500ppm from the center frequency.

Power-Up and Link Start-Up

The GMSL2 ICs are in power-down mode when the PWDNB pin is low or when any of the power supplies are down. Register and configurations are set to default reset conditions.

The serializer and deserializer may power up in any order. After PWDNB is released and all power supplies are up, each

device starts its power-up sequence and performs these actions in sequence:

1. Set the latch-on-power-up pins register.
2. Set the internal registers according to the selected configuration: I2CSEL, CXTP, ADD0, ADD1, ADD2, RCLKEN (if available).
3. The control channel (I^2C or UART) is functional on the local side. The device registers are writable and readable.
4. The link is established based on the following settings:
   a. Single link auto-selection mode (AUTO_LINK = 1 and LINK_CFG = 1 or 2): Automatically select which PHY to use to establish a GMSL2 link by periodically trying to handshake using PHY A and PHY B. **Note: AUTO_LINK=1 is the default and recommended setting to optimize lock time.**
   b. Single link manual selection mode (AUTO_LINK = 0 and LINK_CFG = 1 or 2): If LINK_CFG = 1, establish a link using PHY A. If LINK_CFG = 2, establish a link using PHY B.
   c. Dual-link mode (LINK_CFG = 0): Establish a link using both PHYs.
   d. Splitter (serializer)/aggregator (deserializer) mode (LINK_CFG = 3): Establish a link using both PHYs (for specific applications only).
5. Each enabled PHY performs link calibration, equalizer adaptation, and data channel locking. Both devices set their LOCK pins high.
6. The control channel is available from the remote side.

After the devices are linked, they can be configured. This can be done locally or over the control channel, by a microcontroller on either the serializer side or the deserializer side.

Device Reset

There are three general-reset options available through the register writes:

1. RESET_ALL resets all blocks, including all registers, digital blocks, and analog blocks. This process is similar to driving the PWDNB pin low and then high. **Note:** If Sleep mode is being used, do not use RESET_ALL as it returns the device to Sleep mode.
2. Setting RESET_LINK resets all GMSL PHY-related digital logic and all data pipelines. After this bit is set, all control registers are still accessible through the local control channel. The link remains in RESET until the RESET_LINK is cleared.
3. RESET_ONESHOT resets all GMSL PHY-related digital logic and all data pipelines, and then automatically clears itself. This is similar to setting and clearing RESET_LINK.

Program registers that affect GMSL2 link operation (e.g., TX_RATE, RX_RATE, CXTP_A/B, AUTO_LINK, LINK_CFG, GMSL2) first, followed by RESET_LINK, or RESET_ONESHOT, or set these registers when RESET_LINK=1 and then set RESET_LINK=0. Setting LINK_CFG=3 is a special case that requires writing LINK_CFG=3 and RESET_ONESHOT=1 in the same register byte write.

Link and Video Lock

Link Lock

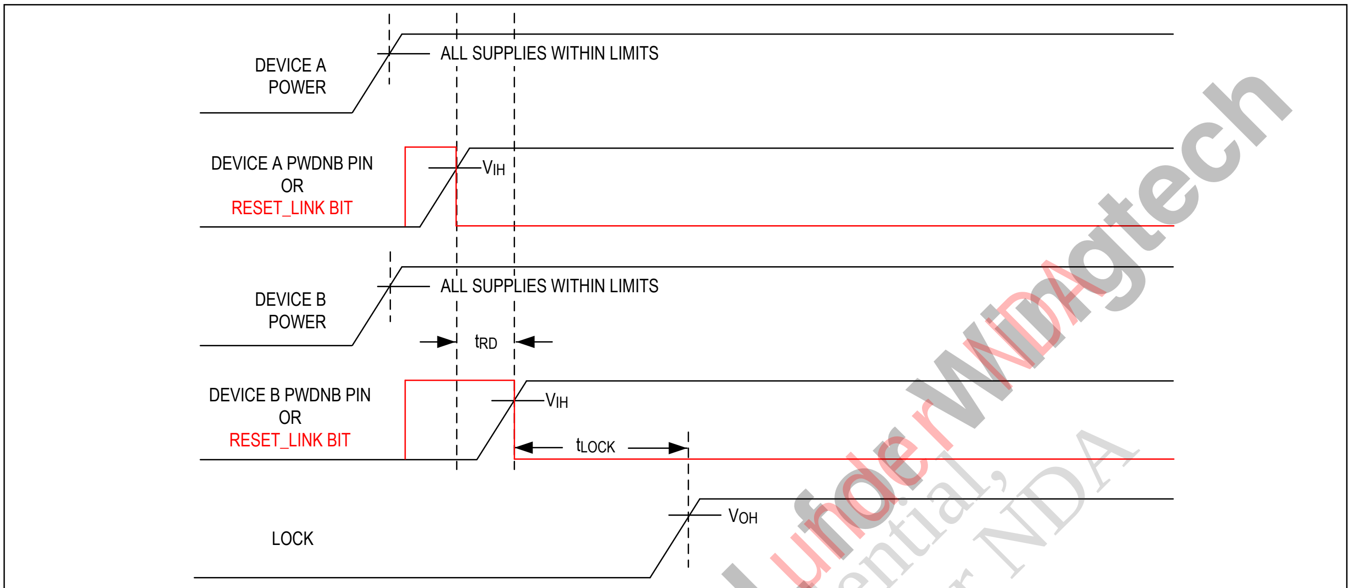


Figure 12. GMSL2 Lock Time

The link lock happens automatically on power-up and is an indication that the cable is plugged in and the system is up and running. The lock is obtained with no interaction or commands from the microcontroller to the GMSL parts. Both the serializers and the deserializers have an open-drain LOCK output pin and a related status register.

The link lock indicates that the PLLs for the GMSL2 link are locked to each other and the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). The video and control channel functions (I^2C/UART, SPI, GPIO, audio, Ethernet) can be used immediately after link lock is asserted.

Dual-link and splitter configurations require additional user programming. For guidance on enabling these configurations and optimizing the lock time, contact the factory.

The GMSL2 link uses the crystal or external reference input as the reference clock for the GMSL2 link, so a valid video input (pixel clock) is not needed for the GMSL2 link to lock. See Figure 12.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. The lock time is measured from the later of the PWDNB or the RESET_LINK release on either the serializer or the deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both the devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate the lock, the PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, the RESET_LINK is assumed to be low after power-up (normal operation).
6. Device A is the first device (serializer or deserializer) to be powered up. Device B is the device (deserializer or serializer) at the other end of the GMSL link.
7. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices), must be less than 90ms. If this timing cannot be guaranteed, contact the factory for the guidance.
8. The lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and the deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. For further guidance, contact the factory.

Video Lock

The video lock indicates that the deserializer is receiving valid video data. After the GMSL2 link has locked, the deserializer video output PLL starts its locking sequence. The deserializer normally starts outputting video data several milliseconds after it asserts line lock, provided that it is receiving video packets from the serializer. Video lock status is typically read from a register. However, the deserializer LOCK pin behavior can be changed by a register setting so that the LOCK pin is asserted only when the deserializer is outputting video.

The MAX96772/MAX96774 require that only stable video is received to ensure reliable operation. The transient video transmission can disrupt reliable operation. The Proper configuration of the connected serializer is required to avoid the transmission of transient video that may disrupt the MAX96772/MAX96774 video output.

Power Standby and Sleep Mode

A power manager block is present in all GSML2 products. Its primary function is to monitor supply voltages and control power-down (standby) and sleep modes.

There are two ways to go into low power mode while all power supplies are active: asserting the PWDNB pin or invoking the sleep state. Both states offer very low power supply currents.

Asserting the PWDNB pin (active-low) places the device in standby power mode and resets the digital registers and configurations to their default power-up condition. Any supply dropping below its internal threshold settings also places the device in power-down mode.

The sleep state provides preservation of critical register settings and configurations. The register table indicates which registers are retained. The device can be put into a sleep state through an I^2C/UART command. The resume state restores the device back to the pre-sleep condition without the need for additional register writes. A resume is invoked by an I^2C command or a low-frequency clock beacon transmitted from the master device over the GMSL2 link.

GPIOs are in Hi-Z during standby and sleep modes. The status of all GPIOs is retained in Sleep mode.

Error and Fault Condition Monitoring

Both the serializer and the deserializer have an open-drain, multipurpose error reporting and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers, so the reason for the assertion of ERRB can be determined by reading the register status.

Adaptive Equalization (AEQ)

The GMSL2 devices automatically adapt receiver characteristics to compensate for the insertion and return loss characteristics of the channel, which consists of the cables, connectors, and PCBs. This optimizes performance on any channel that meets the GMSL2 channel spec.

The equalizer architecture makes the GMSL2 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock and then is invoked at a rate of approximately 1Hz to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye-opening by using the built-in eye-opening monitor.

Video Pipeline

DSC, Watermark, and PRBS

Decompression, watermark detection, and the video PRBS checker are provided.

The decompression engine supports VESA 3:1 DSC.

The watermark block is used to check that the video image is not frozen.

The video PRBS checker can be enabled after the video is locked.

Video Line CRC

A CRC32 polynomial is used to generate a 32-bit code at the end of each DE or HS pulse. This code is transferred to

the receiver (deserializer) side using info frames. The CRC checker generates the same code on the receiver side and checks if the generated and received CRC codes are the same. If not, it asserts an error. The CRC check is done at every falling edge of DE on the receiver side, if the info frame is not received.

Eye-Opening Monitor

The eye-opening monitor (EOM) enables the GMSL2 parts to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error-free but have less link margin than desired. This allows the customer to proactively react to deteriorating cable performance before any link errors occur.

The GMSL2 devices can measure the horizontal or vertical eye-opening of the equalizer's output. The measurement is activated automatically at a rate of approximately 1Hz once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye-opening is then reported, and the EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds.

Watermarking

The watermarking block allows users to detect a frozen frame failure in a frame-based processing system between the generator and detector. This feature is specifically targeted to detect frozen frames caused by SoCs in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector. The GMSL2 devices contain both a watermark generator and a watermark detector. This allows both the serializers and the deserializers to insert a watermark or detect a watermark in a safety-relevant video stream. The watermark generator inserts a time-varying watermark that is highly redundant and robust to image processing and display stream compression. The watermark detector looks for this time-varying watermark. A failure to detect all of the generated watermarks indicates a frozen frame failure in a frame-based processing system between the generator and detector. Upon detection of this error condition, the watermark detector can generate an interrupt and/or blank the output video, returning the display to a safe-state in less than 500ms.

Vertical Sync Output for Backlight PWM Synchronization

The deserializer can optionally synchronize the backlight PWM output with the vertical sync (VS) signal to ensure that video output is accurately dimmed and video data is properly aligned with the start of the video frame. Very predictable video performance is achieved by aligning the PWM output with the start of the video frame. Write 1 to the VS_OUT_EN register field to enable this function; write 0 to the same field to disable it.

Note: Enabling VS output is a secondary function of a GPIO pin.

PRBS

Video PRBS

The video channel has a PRBS generator in the serializer and a PRBS checker in the deserializer to test the video channel operation. The video PRBS generator can work with the recovered PCLK received from an HDMI, parallel, or MIPI input. An external PCLK can also be provided to a designated GPIO pin to run the video PRBS generator.

Note: In GMSL2 mode, the video channel alone does not use all of the link bandwidth. Therefore, it is possible to have a bit error on the link that does not cause a video PRBS error.

Audio PRBS

The audio channel includes a PRBS generator on the transmitter side and a checker on the receiver side to test the audio channel operation. The audio PRBS generator can operate using the incoming I^2S signals SCK and WS or using an internally generated reference clock. When audio PRBS generation is enabled, the channel is reset unless the WS and SCK are used from the I^2S inputs. The detected audio channel bit errors are reported through a status register.

High-Bandwidth Digital Content Protection (HDCP)

Overview

The HDCP is a type of encryption scheme that is used to protect digital audio and video content in a variety of protocols. The MAX96774 supports HDCP 1.4 on both GMSL2 links and HDCP 2.2/2.3 on link A, or when in dual link mode.

For power savings, the HDCP circuits are powered down by default. Once the user enables HDCP, the function powers up and performs authentication, after which link integrity checks are periodically performed by hardware through a dedicated control channel over the GMSL2 link. The HDCP interrupts can be generated and status registers provide the status of authentication progress, indicating success and a ready state for the upstream video source.

Each HDCP device has a factory-programmed unique device ID called a key selection vector (KSV) and associated private keys. They are licensed by DCP LLC.

Repeater Support

The GMSL2 serializers and the deserializers with HDCP capability can be configured as HDCP repeaters. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits it on one or more downstream links. A maximum of 15 receivers is supported.

Auto HDCP Operation

The GMSL2 has an auto HDCP (AHDCP) feature that fully automates the GMSL2 HDCP key exchange authentication without requiring external µC involvement. Authentication and link integrity checks are done by hardware through a dedicated control channel over the GMSL2 link.

The GMSL2 AHDCP has an optional fast mode to perform link integrity checks every frame. This reduces the video out of encryption synchronization duration down to as low as two frames.

Dual GMSL2 Links

There are two HDCP 1.4 engines in the serializer that work independently for the HDCP authentication and link integrity check. This supports configurations that have one GMSL2 serializer connected to two GMSL2 deserializers with HDCP operation.

HSYNC Positive Pulse Width and HDCP 1.4

While using HDCP 1.4, the minimum recommended HSYNC positive pulse width is 31 pixel clocks with DSC disabled and 93 with DSC enabled.

Embedded DisplayPort (eDP) Output

Overview

The MAX96772/MAX96774 provide a subset of eDP features specifically to drive single displays in automotive applications. Only single-stream transport (SST) mode is supported. Hot-plug detect (HPD) functionality is supported. For detailed information on eDP and DP, refer to the VESA Embedded DisplayPort (eDP) Standard and the VESA DisplayPort (DP) Standard.

eDP Transmitter

The eDP transmitter sources isochronous data with 8b/10b encoding on 1, 2, or 4 lanes. It supports per-lane data rates over the range of 1.62Gbps to 8.1Gbps. Turn off unused lanes in LANE_COUNT (0xE792) and leave the pins unconnected.

The output differential swing is programmable over the range of 200mV to 450mV in 50mV steps. Preemphasis is programmable over the range from 0dB to 6dB in 2dB steps. Both are set automatically during link training.

Spread-spectrum clocking (SSC) reduces radiated EMI. The drivers include internal 100Ω differential source termination. The transmitter includes a disable feature.

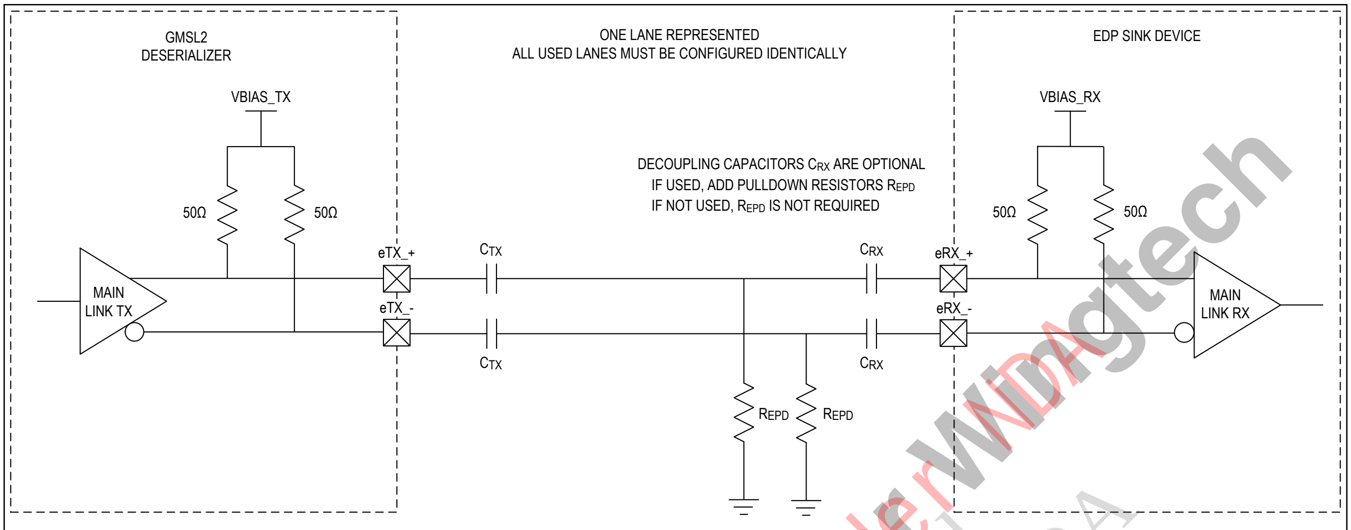


Figure 13. eDP Main Link Topology

Link Training

Upon triggering, the MAX96772/MAX96774 automatically configure the link through a training algorithm communicated over the AUX channel. Trained parameters include the number of lanes, link rate, amplitude, and equalization. Link settings are optimized to ensure robust clock and symbol recovery by the sink device. Video cannot be displayed until the link training is complete. The initial trigger must be done by register writes to USER_CMD_B0 (0xE776). Subsequent HPD events trigger link training.

Link Rate

The MAX96772/MAX96774 support R162 (RBR), R216, R243, R270 (HBR), R324, R432, R540 (HBR2), and R810 (HBR3) per-lane data rates.

The general preference for an eDP implementation is to minimize the number of lanes by designing with higher link rates. The eDP/DP bandwidth required per lane can be approximately calculated with the following formula:

$$\text{Lane Data Rate} = (H \times V \times fps \times bpp \times encoding)/lanes$$

Definitions:

H = horizontal line width including blanking

V = vertical frame height including blanking

fps = frames per second

bpp = 24 bits per pixel for RGB888

encoding = 8b/10b encoding (always 1.25)

lanes = number of DP lanes in use

AUX Channel

The 1Mbps, half-duplex, bidirectional AUX channel supports services that include link configuration, maintenance, and EDID access. The output differential swing is programmable over the range of 200mV to 1400mV, in 200mV steps. The received signal common-mode voltage is adjustable over the range of 400mV to 1200mV, in 100mV steps. The port includes an internal 100Ω differential termination.

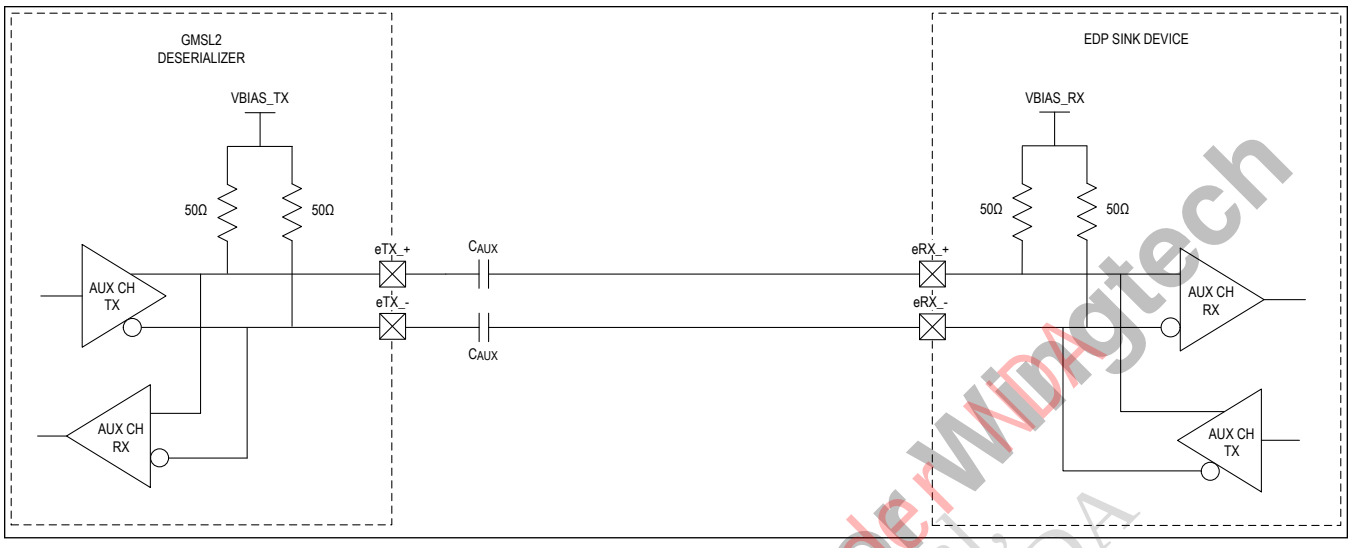


Figure 14. eDP AUX Channel Topology

Display Stream Compression (DSC)

The GMSL2 devices with DSC implement a video compression algorithm compliant with the VESA DSC v1.1 specification. It provides fixed, 3-to-1, visually lossless compression of the video stream. The 3-to-1 compression allows high frame-rate, high-resolution video (up to 4K at 60fps) to be passed through a single GMSL2 link, together with other traffic.

In the serializer, DSC encoding (compression) is performed on the 24-bit RGB pixel video stream prior to transmission across the GMSL2 link. In the deserializer, DSC decoding (decompression) is performed on the compressed video stream received from the GMSL2 link to reconstruct the RGB video.

In both the serializer and the deserializer DSC blocks, a set of SoC-programmable registers contains the picture parameter set (PPS) needed for the DSC encoding and decoding for a particular video resolution. Both devices implement profiles for 16 common and customer-specific video resolutions to support fast auto-loading of the pre-computed PPS parameters into the programmable registers for the selected video resolution of operation. This saves the SoC from having to load the entire PPS into the serializer and deserializer devices.

When DSC is not enabled, the raw video bypasses the DSC blocks.

Forward Error Correction (FEC)

An FEC is increasingly required to handle errors in high-speed links. The primary need for FEC in GMSL2 products arises from the use of compressed video. Errors on a compressed video stream corrupt far more pixels than errors on an uncompressed stream. An FEC is implemented on devices that support DSC to ensure that corrupted video is not noticeable on a link that passes the channel specification.

Features:

- Burst error correction capability equivalent to 2-3 link symbols
- Debug capability to enable analyzing quality of received data
  - Number of errors corrected, number of uncorrectable errors
  - Interrupt output when uncorrectable errors exceed threshold

Notes:

- Correction is available for all data traffic in the GMSL lanes supporting FEC.
- Enabling FEC reduces the available bandwidth by approximately 7%.
- FEC adds approximately 4300 UI latency to the link.

Applications Information

Control-Channel Programming

The GMSL device registers can only be accessed and configured through the I²C/UART interface in either I²C mode or UART mode. By default, the main I²C/UART channel is also sent to the remote-side device and any peripheral connections. This allows control of the GMSL devices from either end of the link. For multimaster configurations with microcontrollers connected to both the serializer and the deserializer, disabling the remote control channel using DIS_REM_CC is recommended to prevent bus contention.

The SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

The register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

Device Address

Each device on the I²C/UART control channel must have a unique address. The GMSL2 device address is set to one of several 7-bit addresses according to the state of the ADD[2:0] pins at power-up. For more information, see the *Latch-On-Power-Up Pins* section.

Note: The device address can be changed after power-up by writing to the DEV_ADDR register.

I²C Programming

Each device has an internal I²C slave for register access. The internal registers can be written and read according to the I²C protocol using the packet formats below.

I²C Write-Packet Format

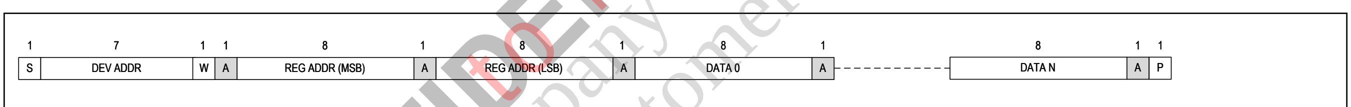


Figure 15. I²C Write-Packet Format

I²C Read-Packet Format

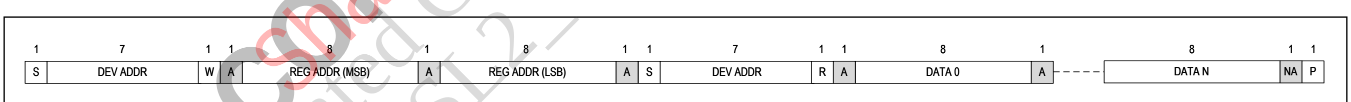


Figure 16. I²C Read-Packet Format

Host-to-Peripheral Main I²C and Pass-Through I²C Communication

When communicating between a host and peripheral, the main and pass-through I²C operations are the same. An I²C tunnel across the GMSL2 link connects the host's I²C master to the remote I²C slave. This logically connects separate I²C buses, enabling I²C transactions across the serial link to occur (with some delay) as if performed on the same physical I²C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I²C master connects to a GMSL2 device I²C slave, and the peripheral I²C slave connects to a GMSL2 device I²C master. For example, when the host I²C master transacts on one side of the link (local-side), data is forwarded to the other side (remote-side) by the I²C slave of the local-side GMSL2 device. Data is then received by the I²C master of the remote-side GMSL2 device, which in turn generates the same I²C transaction with the peripheral slave I²C. The remote-side GMSL2 device sends back any I²C data expected by the local-side.

The I²C interface uses clock stretching (holding SCL low) to account for timing differences between master and slave and to allow time for data to be forwarded and received across the serial link. All local-side I²C devices must support

clock stretching by the GMSL2 device; remote-side I2C devices are not required to support clock stretching.

The host can program the GMSL2 device registers to independently configure the pass-through I^2C/UART interfaces as either I^2C or UART.

UART Programming

When the main I^2C/UART interface is configured as a UART, there are two operating modes: base and bypass.

UART Base Mode

Base mode is the means of µC communication with the serializer and the deserializer in which registers in these devices, as well as registers in peripheral devices, can be accessed. Base mode is enabled by default at power-up. In base mode, the µC is the host and can access the registers of both the serializer and the deserializer from either side of the link using the GMSL2 UART packet protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings). The device addresses of the serializer and the deserializer in this mode are programmable.

In base mode, serializer, deserializer, and peripheral registers can be written and read using the half-duplex GMSL2 UART protocol.

Figure 17 shows the UART protocol for writing and reading in base mode.

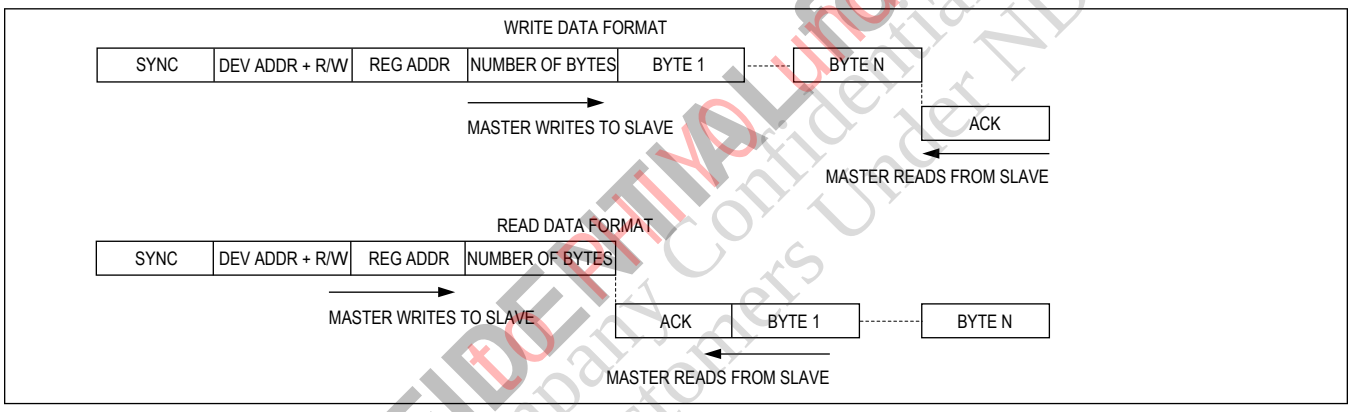


Figure 17. GMSL2 UART Protocol for Base Mode

UART Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the µC, allowing the µC to communicate only with peripheral devices. The µC cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL link. Ignoring UART transactions prevents inadvertent misprogramming of the serializer and the deserializer registers. The device addresses of the serializer and the deserializer in this mode are not programmable.

Switching Between UART Base and Bypass Modes

There are two ways to switch between base mode and bypass mode: programming the register and using the MS pin.

When the register is programmed, bypass mode is active only as long as there is UART activity. When there is no UART activity for a selected timeout, both devices exit bypass mode and the bit is automatically cleared.

When set by the MS pin, a high pin level puts the device into bypass mode, and a low level puts the device into base mode. MS is set on the fly and is not latched on power-up.

UART Frame Format

Regular UART frames with an even parity bit are used to carry 1 byte of data each. A frame consists of a low start bit followed by 8 data bits, a parity bit, and is finished with a high stop bit. The parity bit is high if the number of ones in the 8 bits of data is odd. Otherwise, the parity bit is low. There must be at least 1 high stop bit. If the next frame is in the same

packet, there can be at most 4 high bits from the end of the stop bit to the beginning of the next start bit.

Note: In the case of a parity bit error, the packet is discarded, starting from the frame with the error.

The start of each frame is always a high-to-low transition (i.e., the stop bit is high and the start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer calibrates the length of one UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with the UART data transmissions, and the recipient of the data must perform error checking. The parity bit (which is enabled by default in bypass mode) can be disabled before entering bypass mode.

Note: The bit rate in bypass mode must be the same as the bit rate last used in base mode.

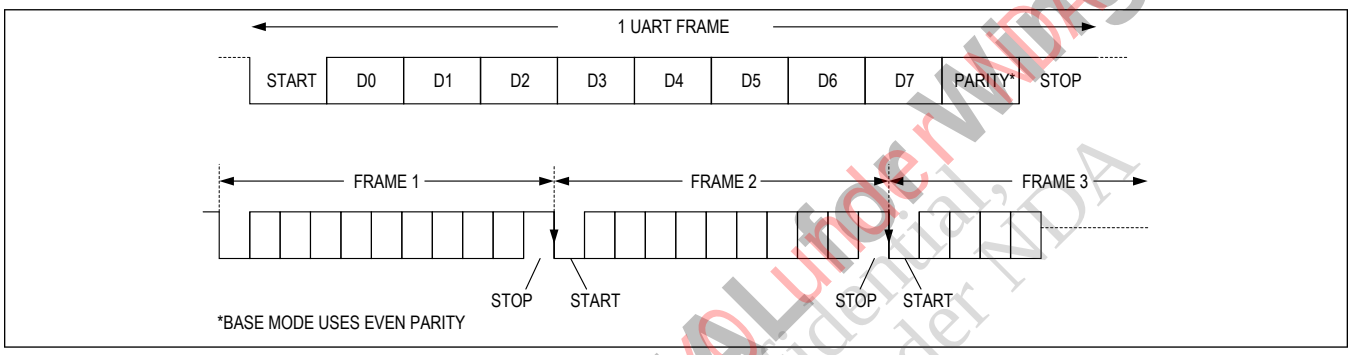


Figure 18. UART Data Format for Base Mode

Synchronization Frame

The serializer/deserializer must calibrate internal bit-length counters with the UART bit rate for proper recovery of UART frames. A sync frame (a regular UART frame with the value 0x79) is sent as the first frame of each data packet from the µC and is used to calibrate the bit length in terms of the device's internal 150MHz clock. The sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next sync frame.

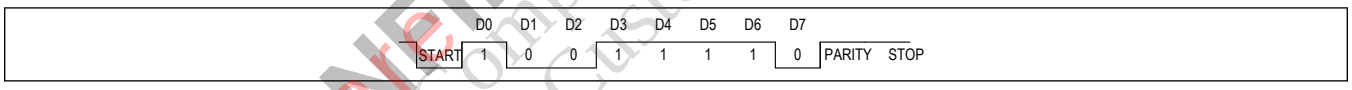


Figure 19. UART Synchronization Frame

Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors were detected in the transmitted packet, and it was recognized as valid. This is sent after the last bit of a successfully recognized packet has been received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

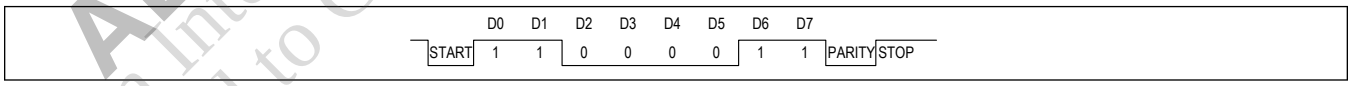


Figure 20. UART Acknowledge Frame

Write Packet

The write packets consist of a 5-byte packet header followed by one or more data bytes. A packet is recognized as a write packet when the LSb of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors were detected while receiving the write packet and the write packet is valid. Byte count indicates the number of data bytes to be written, and it cannot be 0.

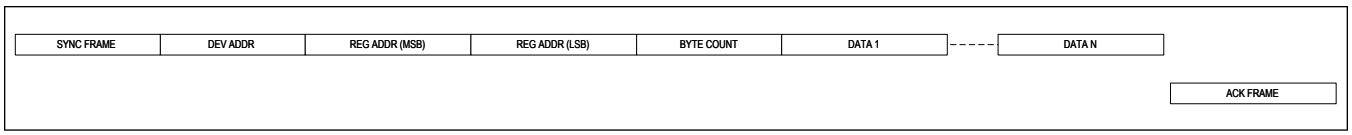


Figure 21. UART Write-Packet Format

Read Packet

A read packet consists of 5 bytes. The LSb of the device address frame is 1 for read packets. If no errors were detected while receiving the read packet and the packet is valid, the addressed device responds with an acknowledge frame followed by one or more data bytes. Byte count indicates the number of data bytes to be read, and it cannot be 0.

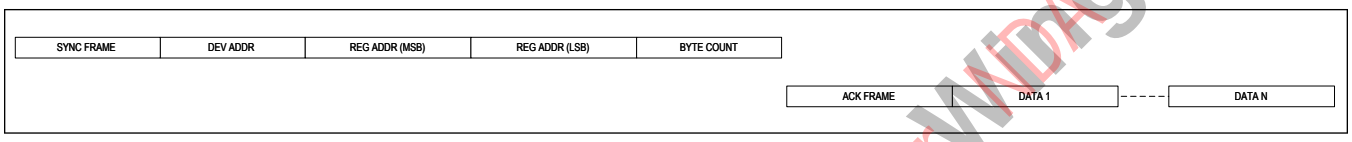


Figure 22. UART Read-Packet Format

Typical Application Circuits

Typical GMSL2 Link Application Circuit for Coax Cable

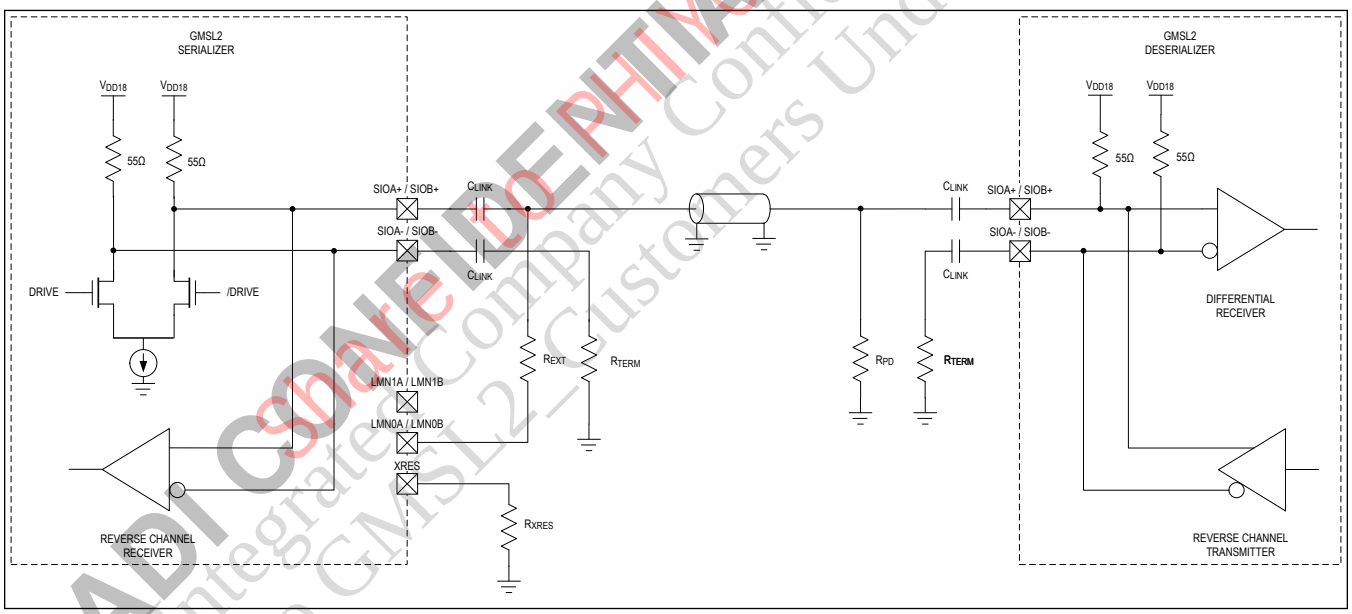


Figure 23. Typical GMSL2 Link Application Circuit for Coax Cable

Typical Application Circuits (continued)

Typical GMSL2 Link Application Circuit for Twisted Pair

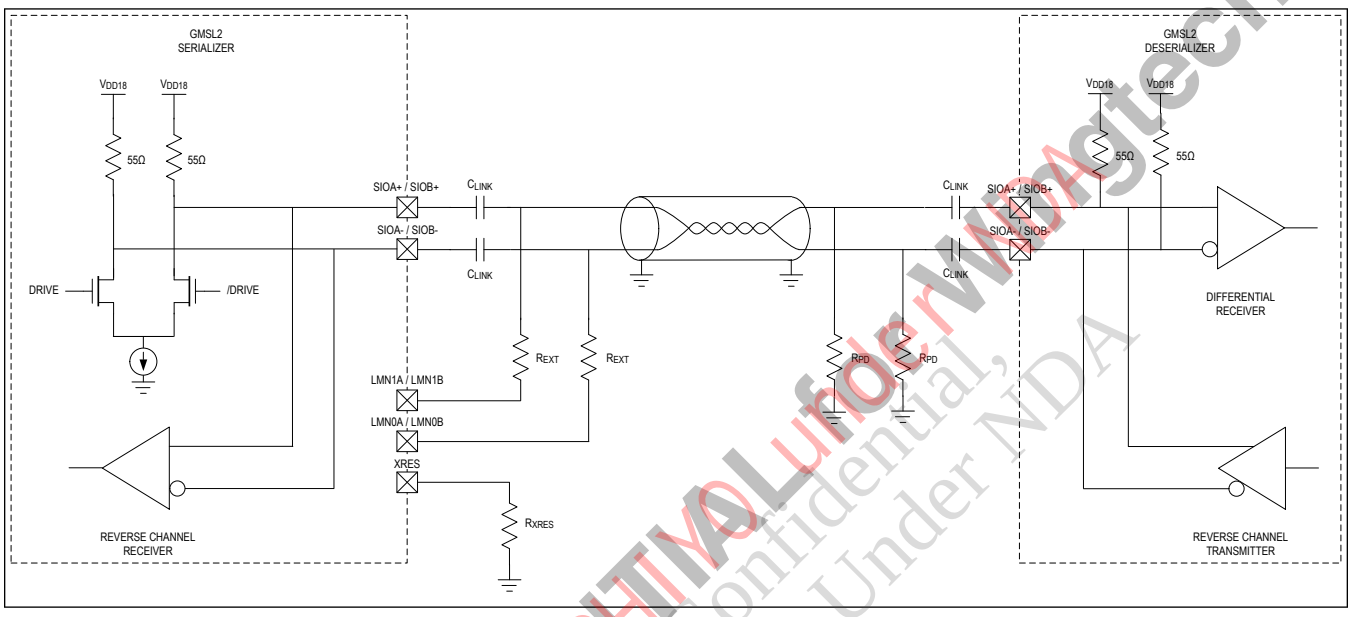


Figure 24. Typical GMSL2 Link Application Circuit for Twisted Pair

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	HDCP
MAX96772GTM/V+	−40°C to +105°C	48-lead TQFN-EP*	No
MAX96772GTM/V+T	−40°C to +105°C	48-lead TQFN-EP*	No
MAX96772GTM/VY+	−40°C to +105°C	48-lead TQFN-SW-EP*	No
MAX96772GTM/VY+T	−40°C to +105°C	48-lead TQFN-SW-EP*	No
MAX96774GTM/V+	−40°C to +105°C	48-lead TQFN-EP*	Yes**
MAX96774GTM/V+T	−40°C to +105°C	48-lead TQFN-EP*	Yes**
MAX96774GTM/VY+	−40°C to +105°C	48-lead TQFN-SW-EP*	Yes**
MAX96774GTM/VY+T	−40°C to +105°C	48-lead TQFN-SW-EP*	Yes**

/V Denotes an automotive qualified part

Y Denotes side-wettable package

+ Denotes a lead(Pb)-free/RoHS-compliant package

T Denotes tape and reel

EP Denotes Exposed Pad*

***HDCP parts require registration with Digital Content Protection, LLC*

Register Map

Reserved and Unused Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally, write the new byte to the register (Read/Replace/Write).

In this document, default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

HDCP

The MAX96774 has HDCP while the MAX96772 does not. The register blocks (shown below), registers, and bitfields that refer to the HDCP are reserved in the MAX96772, and should not be changed from the default state.

Table 12. HDCP Register Blocks (MAX96774 Only)

BLOCK NAME	REGISTER ADDRESS RANGE
HDCP_RX	0x1695–0x1699, 0x16B4–0x16B9
HDCP2_RX	0x1700–0x1703

Note: * Indicates that the register is stored when entering sleep mode and is restored upon exit from sleep mode.

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x90	REG0[7:0]*	DEV_ADDR[6:0]							CFG_BLOCK
0x01	0x02	REG1[7:0]*	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RX_RATE[1:0]	
0x02	0xF7	REG2[7:0]*	RSVD	RSVD	RSVD	VID_EN_X	–	AUD_TX_EN	RSVD	RSVD
0x03	0x00	REG3[7:0]*	LOCK_CFG	–	UART_2_EN	UART_1_EN	–	–	–	–
0x04	0x30	REG4[7:0]*	–	–	LINK_EN_B	LINK_EN_A	–	–	–	–
0x0D	0x8A	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x06	REG14[7:0]	RSVD[3:0]				DEV_REV[3:0]			
0x0F	0x00	REG15[7:0]	RSVD	RSVD	SPEED_CPBL[1:0]		RSVD	DUAL_CPBL	RSVD	HDCP_CPBL
0x3A	0x30	IO_CHK2[7:0]	PIN_DRV_SEL	–	RSVD[1:0]		RSVD	RSVD	PIN_DRV_EN_2[1:0]	
0x3D	0x00	IO_CHK5[7:0]	PIN_RXE_EN	–	–	–	–	–	PIN_IN_2[1:0]	
OVERLAP										
TCTRL										
0x07	0x50	REGLR_CTRL[7:0]	RSVD[1:0]		OV_LEVEL[1:0]		RSVD	LDOH_TEST_MODE	RSVD	LDOH_EN
0x08	0x00	PWR0[7:0]	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x0C	0x1A	PWR4[7:0]*	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x10	0x11	CTRL0[7:0]*	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	–	LINK_CFG[1:0]	
0x11	0x0A	CTRL1[7:0]*	RSVD	RSVD	RSVD	RSVD	RSVD	CXTP_B	RSVD	CXTP_A
0x13	0x00	CTRL3[7:0]	RSVD	RSVD	RSVD	DUAL_LINK_MODE	LOCKED	ERROR	CMU_LOCKED	–
0x18	0xA0	INTR0[7:0]*	RSVD	FW_OSC_PU	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x19	0x00	INTR1[7:0]*	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x1A	0x03	INTR2[7:0]*	RSVD	RSVD	REM_ERR_OEN	PMX_ERR_OEN	–	RSVD	DEC_ERR_OEN_B	DEC_ERR_OEN_A
0x1B	0x00	INTR3[7:0]	RSVD	RSVD	REM_ERR_FLAG	PMX_ERR_FLAG	–	RSVD	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x1C	0x09	INTR4[7:0]*	EOM_ERR_OEN_B	EOM_ERR_OEN_A	HDCP2_INT_OEN	HDCP_INT_OEN	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
0x1D	0x00	INTR5[7:0]	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	HDCP2_INT_FLAG	HDCP_INT_FLAG	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
0x1E	0x0E	INTR6[7:0]*	FEC_RX_ERR_OEN	DSCD_ERR_OEN	LOCK_B_OEN	LOCK_A_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	APRBS_ERR_OEN	VID_PXL_CRC_ERR_OEN
0x1F	0x00	INTR7[7:0]	FEC_RX_ERR_FLAG	DSCD_ERR_FLAG	LOCK_B	LOCK_A	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	APRBS_ERR_FLAG	VID_PXL_CRC_ERR_FLAG
0x20	0x1F	INTR8[7:0]*	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x21	0x5F	INTR9[7:0]*	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
0x22	0x00	CNT0[7:0]	DEC_ERR_A[7:0]							
0x23	0x00	CNT1[7:0]	DEC_ERR_B[7:0]							
0x26	0x00	CNT4[7:0]	PKT_CNT[7:0]							
GMSL										
0x29	0x00	TX1[7:0]*	LINK_PRBS_GEN	–	ERRG_EN_B	ERRG_EN_A	–	–	RSVD	RSVD
0x2A	0x20	TX2[7:0]*	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x2B	0x44	TX3[7:0]*	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x2C	0x00	RX0[7:0]*	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x30	0x41	GPIOA[7:0]*	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					

ADDRESS	RESET	NAME	MSB							LSB
0x31	0x88	GPIOB[7:0]*	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
CC										
0x40	0x26	I2C_0[7:0]*	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x41	0x56	I2C_1[7:0]*	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x42	0x00	I2C_2[7:0]*	SRC_A[6:0]							–
0x43	0x00	I2C_3[7:0]*	DST_A[6:0]							–
0x44	0x00	I2C_4[7:0]*	SRC_B[6:0]							–
0x45	0x00	I2C_5[7:0]*	DST_B[6:0]							–
0x47	0x00	I2C_7[7:0]	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
0x48	0x42	UART_0[7:0]*	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
0x49	0x96	UART_1[7:0]	BITLEN_LSB[7:0]							
0x4A	0x80	UART_2[7:0]	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
CFGH VIDEO_X										
0x50	0x00	RX0[7:0]*	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGL AUDIO										
0x58	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x59	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x5B	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x5C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x5D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x5E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x5F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGI INFOFR										
0x60	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x61	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x63	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x64	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
CFGL SPI										
0x68	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x69	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x6B	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x6C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x6D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x6E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x6F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC CC										
0x70	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x71	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x73	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x74	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x75	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x76	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x77	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL GPIO										
0x78	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x79	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x7B	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x7C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x7D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x7E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x7F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC IIC_X										
0x80	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x81	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x83	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x84	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x85	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x86	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x87	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						

ADDRESS	RESET	NAME	MSB							LSB
CFGC IIC_Y										
0x88	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x89	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x8B	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x8C	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x8D	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x8E	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x8F	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL AHDCP										
0x90	0xF0	TR0[7:0]*	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x91	0xB0	TR1[7:0]*	BW_MULT[1:0]		BW_VAL[5:0]					
0x93	0x30	TR3[7:0]*	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
0x94	0xFF	TR4[7:0]*	RX_SRC_SEL[7:0]							
0x95	0x98	ARQ0[7:0]*	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
0x96	0x72	ARQ1[7:0]*	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x97	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
VID_RX X										
0x100	0x32	VIDEO_RX0[7:0]*	LCRC_ERR	RSVD	RSVD	RSVD	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x103	0x40	VIDEO_RX3[7:0]*	RSVD	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x108	0x02	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
AUD_TX AX										
0x148	0xB0	AUDIO_TX0[7:0]*	RSVD[1:0]		RSVD[1:0]		INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
0x149	0x4E	AUDIO_TX1[7:0]*	AUD_PRIO[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	RSVD[1:0]	
0x14D	0x00	AUDIO_TX5[7:0]	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
0x14F	0x00	AUDIO_TX7[7:0]	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
0x150	0x40	AUDIO_TX8[7:0]	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					

ADDRESS	RESET	NAME	MSB							LSB
AUD_RX										
0x158	0x21	AUDIO_RX1[7:0]*	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
0x15B	0x00	AUDIO_RX4[7:0]	APRBS_ERR[7:0]							
0x15E	0x02	AUDIO_RX7[7:0]*	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
0x160	0x00	AUDIO_RX9[7:0]	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			
SPI										
0x170	0x08	SPI_0[7:0]*	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
0x171	0x1D	SPI_1[7:0]*	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
0x172	0x03	SPI_2[7:0]*	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
0x173	0x00	SPI_3[7:0]*	SPIM_SS_DLY_CLKS[7:0]							
0x174	0x00	SPI_4[7:0]*	SPIM_SCK_LO_CLKS[7:0]							
0x175	0x00	SPI_5[7:0]*	SPIM_SCK_HI_CLKS[7:0]							
0x176	0x00	SPI_6[7:0]*	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
0x177	0x00	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
0x178	0x00	SPI_8[7:0]*	REQ_HOLD_OFF_TO[7:0]							
WM										
0x190	0x00	WM_0[7:0]*	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
0x192	0x50	WM_2[7:0]*	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
0x193	0x0E	WM_3[7:0]*	–	WM_TH[6:0]						
0x194	0x10	WM_4[7:0]*	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
0x195	0x00	WM_5[7:0]	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR
0x196	0x00	WM_6[7:0]	WM_TIMER[7:0]							
0x1AE	0x00	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x1AF	0x00	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
VRX X										
0x1D8	0x00	BLANK_COLOR_A[7:0]*	BLANK_COLOR_A[7:0]							
0x1D9	0x00	BLANK_COLOR_B[7:0]*	BLANK_COLOR_B[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x1DA	0x00	BLANK_COLOR_C[7:0]*	BLANK_COLOR_C[7:0]							
0x1DB	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1DC	0x00	VPRBS[7:0]	–	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
0x1DD	0x80	DISP_CTRL[7:0]*	WM_SYNC_POL_CNV	INVERT_PIX	BLANK_VIDEO	VID_BYTE_SWAP	–	LUT_C_EN	LUT_B_EN	LUT_A_EN
0x1DF	0x00	VIDEO_CTRL_OUT[7:0]*	–	–	–	–	–	HS_OUT_EN	VS_OUT_EN	WM_DET_OUT_EN
GPIO0 0										
0x2B0	0x83	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B1	0xA0	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B2	0x40	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO1 1										
0x2B3	0x84	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B4	0xA1	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B5	0x41	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO2 2										
0x2B6	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B7	0xA2	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B8	0x42	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO3 3										
0x2B9	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2BA	0xA3	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2BB	0x43	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO4 4										
0x2BC	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2BD	0xA4	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2BE	0x44	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
GPIO5 5										
0x2BF	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C0	0xA5	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C1	0x45	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO6 6										
0x2C2	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C3	0xA6	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C4	0x46	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO7 7										
0x2C5	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C6	0xA7	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C7	0x47	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO8 8										
0x2C8	0x81	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C9	0xA8	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CA	0x48	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO9 9										
0x2CB	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2CC	0xA9	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CD	0x49	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO10 10										
0x2CE	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2CF	0xAA	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D0	0x4A	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO11 11										
0x2D1	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D2	0x2B	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x2D3	0x4B	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO12 12										
0x2D4	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D5	0x2C	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D6	0x4C	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO13 13										
0x2D7	0x80	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D8	0x2D	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D9	0x4D	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO14 14										
0x2DA	0x18	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2DB	0x4E	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
0x2DC	0x4E	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO15 15										
0x2DD	0x18	GPIO_A[7:0]*	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2DE	0x4F	GPIO_B[7:0]*	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
0x2DF	0x4F	GPIO_C[7:0]*	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
INTR_SP										
0x440	0x00	INTR10[7:0]*	–	–	–	–	VDD_OV_INT_OEN	VDDBAD_INT_OEN	VDDCMP_INT_OEN	RSVD
0x441	0x00	INTR11[7:0]	–	–	–	–	VDD_OV_INT_FLAG	VDDBAD_INT_FLAG	VDDCMP_INT_FLAG	RSVD
CC_SP										
0x480	0x26	I2C_PT_0[7:0]	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
0x481	0x56	I2C_PT_1[7:0]	RSVD	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
0x48A	0x00	I2C_PT_10[7:0]	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
0x490	0x00	UART_PT_0[7:0]	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1

ADDRESS	RESET	NAME	MSB							LSB
0x491	0xDC	UART_PT_1[7:0]*	BITLEN_PT_1_L[7:0]							
0x492	0x05	UART_PT_2[7:0]*	–	–	BITLEN_PT_1_H[5:0]					
0x494	0x05	UART_PT_4[7:0]*	–	–	BITLEN_PT_2_H[5:0]					
FEC_RX										
0x600	0x06	FEC_RX_CTRL[7:0]*	fec_clr_bit_errs_corrected	fec_clr_uncorrectable_blks	fec_clr_blks_processed	fec_clr_stats	–	fec_collect_stats_en	fec_crc_en	fec_en
0x602	0x00	FEC_RX_STATUS[7:0]*	–	–	–	–	–	–	fec_errs_exceeded	fec_active
0x604	0x00	FEC_MEASURE_DURATION_B0[7:0]*	RSVD[7:0]							
0x605	0x00	FEC_MEASURE_DURATION_B1[7:0]*	RSVD[7:0]							
0x606	0x00	FEC_MEASURE_DURATION_B2[7:0]*	RSVD[7:0]							
0x607	0x00	FEC_MEASURE_DURATION_B3[7:0]*	RSVD[7:0]							
0x608	0x00	FEC_UNCORRECTED_ERRS_THR_B0[7:0]*	fec_uncorrected_errs_thr_b0[7:0]							
0x609	0x00	FEC_UNCORRECTED_ERRS_THR_B1[7:0]*	fec_uncorrected_errs_thr_b1[7:0]							
0x60A	0x00	FEC_UNCORRECTED_ERRS_THR_B2[7:0]*	fec_uncorrected_errs_thr_b2[7:0]							
0x60B	0x00	FEC_UNCORRECTED_ERRS_THR_B3[7:0]*	fec_uncorrected_errs_thr_b3[7:0]							
0x60C	0xFF	FEC_BIT_ERRS_CORRECTED_THR_B0[7:0]*	fec_bit_errs_corrected_thr_b0[7:0]							
0x60D	0xFF	FEC_BIT_ERRS_CORRECTED_THR_B1[7:0]*	fec_bit_errs_corrected_thr_b1[7:0]							
0x60E	0xFF	FEC_BIT_ERRS_CORRECTED_THR_B2[7:0]*	fec_bit_errs_corrected_thr_b2[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x60F	0xFF	FEC_BIT_ERRS_CORRECTED_THR_B3[7:0]*	fec_bit_errs_corrected_thr_b3[7:0]							
0x610	0x00	FEC_BLKS_PROCESSED_B0[7:0]	fec_blks_processed_b0[7:0]							
0x611	0x00	FEC_BLKS_PROCESSED_B1[7:0]	fec_blks_processed_b1[7:0]							
0x612	0x00	FEC_BLKS_PROCESSED_B2[7:0]	fec_blks_processed_b2[7:0]							
0x613	0x00	FEC_BLKS_PROCESSED_B3[7:0]	fec_blks_processed_b3[7:0]							
0x614	0x00	FEC_UNCORRECTABLE_BLKS_B0[7:0]	fec_uncorrectable_blks_b0[7:0]							
0x615	0x00	FEC_UNCORRECTABLE_BLKS_B1[7:0]	fec_uncorrectable_blks_b1[7:0]							
0x616	0x00	FEC_UNCORRECTABLE_BLKS_B2[7:0]	fec_uncorrectable_blks_b2[7:0]							
0x617	0x00	FEC_UNCORRECTABLE_BLKS_B3[7:0]	fec_uncorrectable_blks_b3[7:0]							
0x618	0x00	FEC_BIT_ERRS_CORRECTED_B0[7:0]	fec_bit_errs_corrected_b0[7:0]							
0x619	0x00	FEC_BIT_ERRS_CORRECTED_B1[7:0]	fec_bit_errs_corrected_b1[7:0]							
0x61A	0x00	FEC_BIT_ERRS_CORRECTED_B2[7:0]	fec_bit_errs_corrected_b2[7:0]							
0x61B	0x00	FEC_BIT_ERRS_CORRECTED_B3[7:0]	fec_bit_errs_corrected_b3[7:0]							
MISC										
0x7F0	0x00	PMX_SS_STATE_B0[7:0]	PMX_SS_STATE_B0[7:0]							
0x7F1	0x00	PMX_SS_STATE_B1[7:0]	PMX_SS_STATE_B1[7:0]							
0x7FC	0x12	GPIO_SPEED[7:0]	RSVD[1:0]		GROUP_A_SPEED[1:0]		GROUP_B_SPEED[1:0]		GROUP_C_SPEED[1:0]	
SPI_CC_WR										
0x1300	0x00	SPI_CC_WR_[7:0]	–	–	–	–	–	–	–	–

ADDRESS	RESET	NAME	MSB							LSB
SPI_CC_RD										
0x1380	0x00	SPI_CC_RD_[7:0]	–	–	–	–	–	–	–	–
RLMS A										
0x1403	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x1404	0x4B	RLMS4[7:0]*	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1405	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1406	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1407	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1418	0x03	RLMS18[7:0]	–	–	–	–	–	VgaHiGain	RSVD[1:0]	
0x1434	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1435	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1437	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1438	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x1439	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x143A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x143B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x143D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x1449	0x75	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x1458	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1459	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1464	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x1470	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x1471	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1472	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x1473	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1474	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x1475	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x1476	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1495	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x14A4	0xBD	RLMSA4[7:0]*	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
0x14AC	0xCD	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						

ADDRESS	RESET	NAME	MSB							LSB
0x14AD	0x0D	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
0x14C4	0x40	RLMSC4[7:0]	RSVD	RSVD[2:0]			–	RevFast	–	–
RLMS B										
0x1503	0x0A	RLMS3[7:0]	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
0x1504	0x4B	RLMS4[7:0]*	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1505	0x10	RLMS5[7:0]*	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1506	0x80	RLMS6[7:0]*	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1507	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1518	0x03	RLMS18[7:0]	–	–	–	–	–	VgaHiGain	RSVD[1:0]	
0x1534	0x00	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1535	0x00	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1537	0x00	RLMS37[7:0]	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1538	0x00	RLMS38[7:0]	EyeMonErrCntL[7:0]							
0x1539	0x00	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x153A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x153B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x153D	0x01	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x1549	0x75	RLMS49[7:0]	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
0x1558	0x28	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1559	0x68	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x1564	0x00	RLMS64[7:0]*	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
0x1570	0x01	RLMS70[7:0]*	–	TxSSCFrqCtrl[6:0]						
0x1571	0x02	RLMS71[7:0]*	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1572	0xCF	RLMS72[7:0]*	TxSSCPreSclL[7:0]							
0x1573	0x00	RLMS73[7:0]*	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1574	0x00	RLMS74[7:0]*	TxSSCPhL[7:0]							
0x1575	0x00	RLMS75[7:0]*	–	TxSSCPhH[6:0]						
0x1576	0x00	RLMS76[7:0]*	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1595	0x69	RLMS95[7:0]	TxAmplManEn	RSVD	TxAmplMan[5:0]					
0x15A4	0xBD	RLMSA4[7:0]*	AEQ_PER_MULT[1:0]	AEQ_PER[5:0]						

ADDRESS	RESET	NAME	MSB						LSB
0x15AC	0xCD	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]					
0x15AD	0x0D	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]					
0x15C4	0x40	RLMSC4[7:0]	RSVD	RSVD[2:0]			–	RevFast	–	–
HDCP_RX										
0x1695	0x00	HDCP_15[7:0]	–	–	–	–	–	–	AUTH_START	ENC_EN
0x1696	0x00	HDCP_16[7:0]	RSVD	–	–	–	–	–	HDCP_NEW_DEV_CONN	HDCP_READY
0x1697	0x00	HDCP_17[7:0]	HDCP_BCAPS[6:0]							HDCP_REPEATER
0x1699	0x00	HDCP_19[7:0]*	–	–	–	–	–	–	–	DIS_AUDIO_ENC
0x16B4	0x00	HDCP_34[7:0]	HDCP_MAX_DEV_EXCEEDED	HDCP_DEV_CNT[6:0]						
0x16B5	0x00	HDCP_35[7:0]	RSVD[3:0]				HDCP_MAX_CASCADE_EXCEEDED	HDCP_DEPTH[2:0]		
0x16B6	0x00	HDCP_36[7:0]	HDCP_GPMEM[7:0]							
0x16B7	0xC0	HDCP_37[7:0]*	HDCP_PD	AH_MODE	–	–	–	–	–	–
0x16B8	0x00	HDCP_38[7:0]*	HDCP_INT	–	–	–	–	–	MASK_AUTH_ST	MASK_ENC_EN
0x16B9	0x35	HDCP_39[7:0]	LINK_LOCK	AH_VID_LOCK	AH_RESERVED[5:0]					
HDCP2_RX										
0x1700	0x40	SYS_CNTL_B0[7:0]	cmd_reset	clk_en	hdcp_repeat_mode	sys_int_en[4:0]				
0x1702	0x00	SYS_CNTL_B2[7:0]	cypher_gen_fail	–	–	sys_int_st[4:0]				
0x1703	0x00	SYS_CNTL_B3[7:0]	decrypt_status	video_mask_status	RSVD[5:0]					
DPLL AUD										
0x1B03	0x82	DPLL_3[7:0]*	config_sel_clock_out_use_external	config_disable_div_out_exp	config_use_internal_pll_mode_values	config_use_internal_divider_values	config_force_enable_ss	config_spread_bit_ratio[2:0]		

ADDRESS	RESET	NAME	MSB							LSB
COLOR_A LUT_X										
0x2000	0x00	LUT_A_[7:0]	–	–	–	–	–	–	–	–
COLOR_B LUT_X										
0x2100	0x00	LUT_B_[7:0]	–	–	–	–	–	–	–	–
COLOR_C LUT_X										
0x2200	0x00	LUT_C_[7:0]	–	–	–	–	–	–	–	–
COLOR_A LUT_Y										
0x2400	0x00	LUT_A_[7:0]	–	–	–	–	–	–	–	–
COLOR_B LUT_Y										
0x2500	0x00	LUT_B_[7:0]	–	–	–	–	–	–	–	–
COLOR_C LUT_Y										
0x2600	0x00	LUT_C_[7:0]	–	–	–	–	–	–	–	–
COLOR_A LUT_Z										
0x2800	0x00	LUT_A_[7:0]	–	–	–	–	–	–	–	–
COLOR_B LUT_Z										
0x2900	0x00	LUT_B_[7:0]	–	–	–	–	–	–	–	–
COLOR_C LUT_Z										
0x2A00	0x00	LUT_C_[7:0]	–	–	–	–	–	–	–	–
COLOR_A LUT_U										
0x2C00	0x00	LUT_A_[7:0]	–	–	–	–	–	–	–	–
COLOR_B LUT_U										
0x2D00	0x00	LUT_B_[7:0]	–	–	–	–	–	–	–	–
COLOR_C LUT_U										
0x2E00	0x00	LUT_C_[7:0]	–	–	–	–	–	–	–	–
DSC_DEC										
0x4500	0x00	DSCD_CTRL_B0[7:0]*	RSVD	–	RSVD	RSVD	–	dscd_rst_sc	dscd_rst	dscd_en
0x4501	0x00	DSCD_CTRL_B1[7:0]	prof_wr	–	–	–	prof_sel[3:0]			
0x4504	0x3F	DSCD_RATE_CTRL_B0[7:0]*	pix_out_rate_act[7:0]							
0x4505	0x4F	DSCD_RATE_CTRL_B1[7:0]*	pix_out_rate_inact[7:0]							
0x4507	0x00	DSCD_RATE_CTRL_B3[7:0]	pix_rate_ext_en	–	–	–	–	–	–	–
0x4508	0x00	DSCD_INT_ST_B0[7:0]	–	–	–	–	–	–	pb_ovfl_ist	vb_ovfl_ist
0x4509	0x00	DSCD_INT_ST_B1[7:0]	rcb1_ovfl_ist	tc_size1_err_ist	ib1_undfl_ist	ib1_ovfl_ist	rcb0_ovfl_ist	tc_size0_err_ist	ib0_undfl_ist	ib0_ovfl_ist
0x450C	0x00	DSCD_INT_EN_B0[7:0]*	–	–	–	–	–	–	pb_ovfl_ien	vb_ovfl_ien
0x450D	0x00	DSCD_INT_EN_B1[7:0]*	rcb1_ovfl_ien	tc_size1_err_ien	ib1_undfl_ien	ib1_ovfl_ien	rcb0_ovfl_ien	tc_size0_err_ien	ib0_undfl_ien	ib0_ovfl_ien

ADDRESS	RESET	NAME	MSB							LSB
0x4510	0x61	DEC0_DF_CTRL_B0[7:0]	hsync_delay_l[3:0]				initial_tc[3:0]			
0x4511	0x27	DEC0_DF_CTRL_B1[7:0]	hsync_delay_m[7:0]							
0x4524	0xC0	DEC_PICTURE_SIZE_B0[7:0]*	pic_width_b0[7:0]							
0x4525	0x12	DEC_PICTURE_SIZE_B1[7:0]*	pic_width_b1[7:0]							
0x4526	0x84	DEC_PICTURE_SIZE_B2[7:0]*	pic_height_b0[7:0]							
0x4527	0x03	DEC_PICTURE_SIZE_B3[7:0]*	pic_height_b1[7:0]							
0x4528	0x60	DEC_SLICE_SIZE_B0[7:0]*	slice_width_b0[7:0]							
0x4529	0x09	DEC_SLICE_SIZE_B1[7:0]*	slice_width_b1[7:0]							
0x452A	0x64	DEC_SLICE_SIZE_B2[7:0]*	slice_height_b0[7:0]							
0x452B	0x00	DEC_SLICE_SIZE_B3[7:0]*	slice_height_b1[7:0]							
0x452C	0x02	DEC_MISC_SIZE_B0[7:0]	–	–	–	–	–	–	slice_last_grp_sz[1:0]	
0x452E	0x60	DEC_MISC_SIZE_B2[7:0]	chunk_size_b0[7:0]							
0x452F	0x09	DEC_MISC_SIZE_B3[7:0]	chunk_size_b1[7:0]							
0x4532	0xDC	DEC_HRD_DELAYS_B2[7:0]	initial_dec_delay_b0[7:0]							
0x4533	0x06	DEC_HRD_DELAYS_B3[7:0]	initial_dec_delay_b1[7:0]							
0x4538	0x64	DEC_RC_SCALE_INC_DEC_B0[7:0]	scale_inc_interval_b0[7:0]							
0x4539	0x0D	DEC_RC_SCALE_INC_DEC_B1[7:0]	scale_inc_interval_b1[7:0]							
0x453A	0x21	DEC_RC_SCALE_INC_DEC_B2[7:0]	scale_dec_interval_b0[7:0]							
0x453B	0x00	DEC_RC_SCALE_INC_DEC_B3[7:0]	–	–	–	–	scale_dec_interval_b1[3:0]			
0x4540	0x37	DEC_RC_OFFSETS_2_B0[7:0]	nfl_bpg_off_b0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x4541	0x01	DEC_RC_OFFSETS_2_B1[7:0]	nfl_bpg_off_b1[7:0]							
0x4542	0x3B	DEC_RC_OFFSETS_2_B2[7:0]	slice_bpg_off_b0[7:0]							
0x4543	0x00	DEC_RC_OFFSETS_2_B3[7:0]	slice_bpg_off_b1[7:0]							
0x4546	0xF0	DEC_RC_OFFSETS_3_B2[7:0]	final_off_b0[7:0]							
0x4547	0x10	DEC_RC_OFFSETS_3_B3[7:0]	final_off_b1[7:0]							
EDP_TX_LINK										
0x6188	0x00	BAD_FRAMING_STATE[7:0]	–	–	–	–	RSVD	RSVD	RSVD	SRC0_LNK_FRM_STATE_BAD
0x6190	0x00	SOFT_RESET[7:0]	–	–	–	–	–	–	VIDEO_SOFT_RESET	LINK_SOFT_RESET
0x6230	0x00	AUX_STATE[7:0]	–	–	–	–	RSVD	RSVD	RSVD	HPD_STATE
VTRG X										
0x7000	0x00	VTRG_CTRL_B0[7:0]	–	–	–	–	vid_en_mode[1:0]		vtrg_rst	vtrg_en
0x7008	0x00	VTRG_INT_ST_B0[7:0]	rate_adj_max_ist	rate_adj_ist	pb_ovfl_ist	pb_undfl_ist	vs_inact_ist	vs_act_ist	de_inact_ist	de_act_ist
0x7010	0x00	PIX_RATE_CTRL_B0[7:0]	pix_rate_ctrl_en	–	–	pix_rate_clk_act[4:0]				
0x7011	0x00	PIX_RATE_CTRL_B1[7:0]	pix_rate_inact_red[7:0]							
0x7012	0x00	PIX_RATE_CTRL_B2[7:0]	–	–	–	–	–	–	pix_rate_div[1:0]	
0x7013	0x00	PIX_RATE_CTRL_B3[7:0]	–	–	–	–	dptx_mcnt_ovride	vtg_msa_auto_set	pix_rate_clkp_adj	pix_rate_clkp_en
0x7014	0x00	PIX_RATE_PER_B0[7:0]	pix_rate_act_lo[7:0]							
0x7015	0x00	PIX_RATE_PER_B1[7:0]	pix_rate_act_hi[7:0]							
0x7016	0x00	PIX_RATE_PER_B2[7:0]	pix_rate_inact_lo[7:0]							
0x7017	0x00	PIX_RATE_PER_B3[7:0]	–	–	–	–	–	pix_rate_inact_hi[2:0]		
0x7020	0x07	PB_DELTA_ACC_B0[7:0]	–	–	–	–	pb_del_acc_per[3:0]			
0x702C	0x01	PB_ADJ_STEP_B0[7:0]	–	–	pb_rate_adj_step_0[5:0]					

ADDRESS	RESET	NAME	MSB							LSB
0x702D	0x02	PB_ADJ_STEP_B1[7:0]	–	–	pb_rate_adj_step_1[5:0]					
0x702E	0x04	PB_ADJ_STEP_B2[7:0]	–	–	pb_rate_adj_step_2[5:0]					
0x702F	0x08	PB_ADJ_STEP_B3[7:0]	–	–	pb_rate_adj_step_3[5:0]					
0x7030	0x28	PB_ADJ_CTRL_B0[7:0]	–	pb_rate_adj_max[6:0]						
0x7038	0x00	PB_CLKP_ADJ_STATUS_B0[7:0]	clkp_m_b0[7:0]							
0x7039	0x00	PB_CLKP_ADJ_STATUS_B1[7:0]	clkp_m_b1[7:0]							
0x703A	0x00	PB_CLKP_ADJ_STATUS_B2[7:0]	–	–	–	–	clkp_m_b2[3:0]			
0x7040	0x01	VTG_CTRL_B0[7:0]	–	–	–	–	–	vtg_man_en	vtg_pclk_mode[1:0]	
0x7044	0x00	VTG_HORZ_LINE_B0[7:0]	vtg_htot_lo[7:0]							
0x7045	0x00	VTG_HORZ_LINE_B1[7:0]	vtg_htot_hi[7:0]							
0x7046	0x00	VTG_HORZ_LINE_B2[7:0]	vtg_hact_lo[7:0]							
0x7047	0x00	VTG_HORZ_LINE_B3[7:0]	vtg_hact_hi[7:0]							
0x7048	0x00	VTG_HORZ_SYNC_B0[7:0]	vtg_hstt_lo[7:0]							
0x7049	0x00	VTG_HORZ_SYNC_B1[7:0]	vtg_hstt_hi[7:0]							
0x704A	0x00	VTG_HORZ_SYNC_B2[7:0]	vtg_hsw_lo[7:0]							
0x704B	0x80	VTG_HORZ_SYNC_B3[7:0]	vtg_hsp	vtg_hsw_hi[6:0]						
0x704C	0x00	VTG_VERT_FRAME_B0[7:0]	vtg_vtot_lo[7:0]							
0x704D	0x00	VTG_VERT_FRAME_B1[7:0]	vtg_vtot_hi[7:0]							
0x704E	0x00	VTG_VERT_FRAME_B2[7:0]	vtg_vact_lo[7:0]							
0x704F	0x00	VTG_VERT_FRAME_B3[7:0]	vtg_vact_hi[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x7050	0x00	VTG_VERT_SYNC_B0[7:0]	vtg_vstt_lo[7:0]							
0x7051	0x00	VTG_VERT_SYNC_B1[7:0]	vtg_vstt_hi[7:0]							
0x7052	0x00	VTG_VERT_SYNC_B2[7:0]	vtg_vsw_lo[7:0]							
0x7053	0x80	VTG_VERT_SYNC_B3[7:0]	vtg_vsp	vtg_vsw_hi[6:0]						
0x7060	0x00	PIX_PAT_CTRL_B0[7:0]	–	pix_pat_color[2:0]			–	–	–	pix_pat_en
0x7064	0x00	PIX_PAT_BLOCK_B0[7:0]	pix_pat_hblk_lo[7:0]							
0x7065	0x00	PIX_PAT_BLOCK_B1[7:0]	–	–	pix_pat_hblk_hi[5:0]					
0x7066	0x00	PIX_PAT_BLOCK_B2[7:0]	pix_pat_vblk_lo[7:0]							
0x7067	0x00	PIX_PAT_BLOCK_B3[7:0]	–	–	pix_pat_vblk_hi[5:0]					
EDP_TRAIN_CFG										
0xE75A	0x00	WATCHDOGCNT_B0[7:0]	WATCHDOGCNT_B0[7:0]							
0xE75B	0x00	WATCHDOGCNT_B1[7:0]	WATCHDOGCNT_B1[7:0]							
0xE75E	0x00	HPD_STATUS[7:0]	–	–	–	–	–	–	–	HPD_PIN_STATE
0xE760	0x00	VLOCK_STATE[7:0]	–	–	–	–	–	–	–	VL_STATE
0xE762	0x00	VL_LOST_CNT_B0[7:0]	VL_LOST_CNT_B0[7:0]							
0xE763	0x00	VL_LOST_CNT_B1[7:0]	VL_LOST_CNT_B1[7:0]							
0xE764	0x00	eHPD_IRQ_COUNT_B0[7:0]	eHPD_IRQ_COUNT_B0[7:0]							
0xE765	0x00	eHPD_IRQ_COUNT_B1[7:0]	eHPD_IRQ_COUNT_B1[7:0]							
0xE766	0x00	eHPD_EVENT_COUNT_B0[7:0]	eHPD_EVENT_COUNT_B0[7:0]							
0xE767	0x00	eHPD_EVENT_COUNT_B1[7:0]	eHPD_EVENT_COUNT_B1[7:0]							
0xE768	0x00	NACK_DEFER_CNT_B0[7:0]	NACK_DEFER_CNT_B0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0xE769	0x00	NACK_DEFER_CNT_B1[7:0]	NACK_DEFER_CNT_B1[7:0]							
0xE776	0x00	USER_CMD_B0[7:0]	USER_CMD_B0[7:0]							
0xE777	0x00	USER_CMD_B1[7:0]	USER_CMD_EXECUTE	–	–	–	–	–	–	–
0xE778	0x00	USER_DATA1_B0[7:0]	USER_DATA1_B0[7:0]							
0xE779	0x00	USER_DATA1_B1[7:0]	USER_DATA1_B1[7:0]							
0xE77A	0x00	USER_DATA2_B0[7:0]	USER_DATA2_B0[7:0]							
0xE77C	0x00	USER_DATA3_B0[7:0]	USER_DATA3_B0[7:0]							
0xE790	0x00	LINK_RATE[7:0]	–	–	–	LINK_RATE[4:0]				
0xE792	0x00	LANE_COUNT[7:0]	–	–	–	–	–	LANE_COUNT[2:0]		
0xE794	0x00	HRES_B0[7:0]	HRES_B0[7:0]							
0xE795	0x00	HRES_B1[7:0]	HRES_B1[7:0]							
0xE796	0x00	HFP_B0[7:0]	HFP_B0[7:0]							
0xE797	0x00	HFP_B1[7:0]	HFP_B1[7:0]							
0xE798	0x00	HSW_B0[7:0]	HSW_B0[7:0]							
0xE799	0x00	HSW_B1[7:0]	HSW_B1[7:0]							
0xE79A	0x00	HBP_B0[7:0]	HBP_B0[7:0]							
0xE79B	0x00	HBP_B1[7:0]	HBP_B1[7:0]							
0xE79C	0x00	VRES_B0[7:0]	VRES_B0[7:0]							
0xE79D	0x00	VRES_B1[7:0]	VRES_B1[7:0]							
0xE79E	0x00	VFP_B0[7:0]	VFP_B0[7:0]							
0xE79F	0x00	VFP_B1[7:0]	VFP_B1[7:0]							
0xE7A0	0x00	VSW_B0[7:0]	VSW_B0[7:0]							
0xE7A1	0x00	VSW_B1[7:0]	VSW_B1[7:0]							
0xE7A2	0x00	VBP_B0[7:0]	VBP_B0[7:0]							
0xE7A3	0x00	VBP_B1[7:0]	VBP_B1[7:0]							
0xE7A4	0x00	HWORDS_B0[7:0]	HWORDS_B0[7:0]							
0xE7A5	0x00	HWORDS_B1[7:0]	HWORDS_B1[7:0]							
0xE7A6	0x00	MVID_B0[7:0]	MVID_B0[7:0]							
0xE7A7	0x00	MVID_B1[7:0]	MVID_B1[7:0]							
0xE7A8	0x00	NVID_B0[7:0]	NVID_B0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0xE7A9	0x00	NVID_B1[7:0]	NVID_B1[7:0]							
0xE7AA	0x00	TUC_VALUE_B0[7:0]	TUC_VALUE_B0[7:0]							
0xE7AB	0x00	TUC_VALUE_B1[7:0]	TUC_VALUE_B1[7:0]							
0xE7AC	0x00	HVPOL[7:0]	–	–	–	–	–	–	VSYNC_POL	HSYNC_POL
0xE7AE	0x00	ERRB_ENABLE_MASK_B0[7:0]	HPD_EVENT	RSVD	–	–	–	–	–	TRAIN_PASS
0xE7AF	0x00	ERRB_ENABLE_MASK_B1[7:0]	ERRB_ENABLE	TP1_FAIL	TP2_FAIL	NO_PARMS	NO_HPD	NO_VL	WD_TRIGGER	VL_LOST
0xE7B0	0x00	SS_ENABLE_B0[7:0]	–	–	–	–	–	–	–	SS_ENABLE
0xE7B1	0x00	SS_ENABLE_B1[7:0]	–	–	–	SSC_ENABLE	–	–	–	–
0xE7B2	0x00	CLK_REF_B0[7:0]	CLK_REF_B0[7:0]							
0xE7B3	0x00	CLK_REF_B1[7:0]	CLK_REF_B1[7:0]							
0xE7B4	0x00	CLK_REF_B2[7:0]	CLK_REF_B2[7:0]							
0xE7B5	0x00	CLK_REF_B3[7:0]	CLK_REF_B3[7:0]							
0xE7B6	0x00	CLK_REF_B4[7:0]	CLK_REF_B4[7:0]							
0xE7B7	0x00	CLK_REF_B5[7:0]	CLK_REF_B5[7:0]							
0xE7B8	0x00	CLK_REF_B6[7:0]	CLK_REF_B6[7:0]							
0xE7B9	0x00	CLK_REF_B7[7:0]	CLK_REF_B7[7:0]							
0xE7BA	0x00	CLK_REF_B8[7:0]	CLK_REF_B8[7:0]							
0xE7BB	0x00	CLK_REF_B9[7:0]	CLK_REF_B9[7:0]							
0xE7BC	0x00	CLK_REF_B10[7:0]	CLK_REF_B10[7:0]							
0xE7BD	0x00	CLK_REF_B11[7:0]	CLK_REF_B11[7:0]							
0xE7BE	0x00	CLK_REF_B12[7:0]	CLK_REF_B12[7:0]							
0xE7BF	0x00	CLK_REF_B13[7:0]	CLK_REF_B13[7:0]							
0xE7C4	0x00	HACT_DSC_VTRG_B0[7:0]	HACT_DSC_VTRG_B0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0xE7C5	0x00	HACT_DSC_VTRG_B1[7:0]	HACT_DSC_VTRG_B1[7:0]							
0xE7C6	0x00	AUTO_VTRG_ENABLE[7:0]	–	–	–	–	–	–	–	AUTO_VTRG_ENABLE
0xE7D1	0x00	HPD_MASK_B1[7:0]	–	–	–	–	–	–	–	HPD_DEBOUNCE_DISABLE
0xE7DE	0x01	NO_ALIGN_CHK[7:0]	–	–	–	–	–	–	–	NO_ALIGN_CHK

Register Details

REG0 (0x0)*

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1001000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device Address. Default value is set by the ADD[2:0] pins as follows: ADD[2:0] Device Address 000 0b1001000 001 0b1001010 010 0b1001100 011 0b1101000 100 0b1101010 101 0b1101100 110 0b0101000 111 0b0101010	0b0000000: I^2C write/read address is 0x00/0x01 0b0000001: I^2C write/read address is 0x02/0x03 ... ... 0b1001000: I^2C write/read address is 0x90/0x91 0b1001010: I^2C write/read address is 0x94/0x95 0b1001100: I^2C write/read address is 0x98/0x99 0b1101000: I^2C write/read address is 0xD0/0xD1 0b1101010: I^2C write/read address is 0xD4/0xD5 0b1101100: I^2C write/read address is 0xD8/0xD9 0b0101000: I^2C write/read address is 0x50/0x51 0b0101010: I^2C write/read address is 0x54/0x55 ... ... 0b1111111: I^2C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block. When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.	0b0: Not blocked 0b1: Blocked

REG1 (0x1)*

BIT	7	6	5	4	3	2	1	0
Field	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RX_RATE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b00		0b10	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
IIC_2_EN	7	Enables pass-through I2C Channel 2 (SDA2/RX2, SCL2/TX2).	0b0: Disable I2C pass-through for Channel 2 0b1: Enable I2C pass-through for Channel 2
IIC_1_EN	6	Enables pass-through I2C Channel 1 (SDA1/RX1, SCL1/TX1).	0b0: Disable I2C pass-through for Channel 1 0b1: Enable I2C pass-through for Channel 1
DIS_LOCAL_CC	5	Disables control-channel connection to RX/SDA and TX/SCL pins.	0b0: RX/SDA and TX/XCL connected to control channel 0b1: RX/SDA and TX/SCL disconnected from control channel
DIS_REM_CC	4	Disables remote control channel link over GMSL2 connection.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
TX_RATE	3:2	Transmitter Rate. When changed, becomes active after next link reset.	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE	1:0	Receiver Rate. When changed, becomes active after next link reset). Default value is set by CXTP pin at power-up: 6Gbps when CXTP = 1 (Coax cable) and 3Gbps when CXTP = 0 (Twisted-pair cable).	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

REG2 (0x2)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	VID_EN_X	–	AUD_TX_EN	RSVD	RSVD
Reset	0b1	0b1	0b1	0b1	–	0b1	0b1	0b1
Access Type				Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_X	4	Video Enable.	0b0: Video transmit Channel X disabled 0b1: Video transmit Channel X enabled
AUD_TX_EN	2	Audio Transmit Enable.	0b0: Audio transmit Channel X disabled 0b1: Audio transmit Channel X enabled

REG3 (0x3)*

BIT	7	6	5	4	3	2	1	0
Field	LOCK_CFG	–	UART_2_EN	UART_1_EN	–	–	–	–
Reset	0b0	–	0b0	0b0	–	–	–	–
Access Type	Write, Read	–	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_CFG	7	Configures LOCK pin behavior.	0b0: GMSL2 link locked 0b1: GMSL2 link locked and video output started
UART_2_EN	5	Enables pass-through UART Channel 2 (SDA2/RX2, SCL2/TX2).	0b0: Pass-through UART Channel 2 disabled 0b1: Pass-through UART Channel 2 enabled
UART_1_EN	4	Enables pass-through UART Channel 1 (SDA1/RX1, SCL1/TX1).	0b0: Pass-through UART Channel 1 disabled 0b1: Pass-through UART Channel 1 enabled

REG4 (0x4)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	LINK_EN_B	LINK_EN_A	–	–	–	–
Reset	–	–	0b1	0b1	–	–	–	–
Access Type	–	–	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_EN_B	5	Enables GMSL Link B.	0b0: Link B disabled 0b1: Link B enabled
LINK_EN_A	4	Enables GMSL Link A.	0b0: Link A disabled 0b1: Link A enabled

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0x8A							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device Identifier.	0xAE: MAX96772 0xAF: MAX96774

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				DEV_REV[3:0]			
Reset	0x0				0x6			
Access Type					Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision.	0xX: Revision number

REG15 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	SPEED_CPBL[1:0]		RSVD	DUAL_CPBL	RSVD	HDCP_CPBL
Reset	0b0	0b0	0b00		0b0	0b0	0b0	0b0
Access Type			Read Only			Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPEED_CPBL	5:4	Video Resolution Capability.	0b00: No PCLK frequency limit 0b01: Reserved 0b10: Reserved 0b11: Reserved
DUAL_CPBL	2	Dual-Link Capability.	0b0: Dual-link mode is not available 0b1: Dual-link mode is available
HDCP_CPBL	0	HDCP Capability.	0b0: HDCP not enabled on this device 0b1: HDCP enabled on this device

IO_CHK2 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	PIN_DRV_SEL	–	RSVD[1:0]		RSVD	RSVD	PIN_DRV_EN_2[1:0]	
Reset	0b0	–	0b11		0b0	0b0	0b00	
Access Type	Write, Read	–					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_DRV_SEL	7	Selects polarity for driving dedicated I/Os.	0b0: Drive low level 0b1: Drive high level
PIN_DRV_EN_2	1:0	Drives dedicated I/Os for register readback [17:16] = ERRB, LOCK.	0bX0: Disable LOCK output buffer 0bX1: Enable LOCK output buffer 0b0X: Disable ERRB output buffer 0b1X: Enable ERRB output buffer

IO_CHK5 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	PIN_RXE_EN	–	–	–	–	–	PIN_IN_2[1:0]	
Reset	0b0	–	–	–	–	–	0b00	
Access Type	Write, Read	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_RXE_EN	7	Enables the receivers on all GPIO and dedicated I/O to allow readback of I/O state.	0b0: Drive low level 0b1: Drive high level

BITFIELD	BITS	DESCRIPTION	DECODE
PIN_IN_2	1:0	Reads Dedicated I/O Pin Level [17:16] = ERRB, LOCK.	Bit 0: LOCK Bit 1: ERRB

REGLR_CTRL (0x7)

Regulator Control

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		OV_LEVEL[1:0]		RSVD	LDOH_TEST_MODE	RSVD	LDOH_EN
Reset	0x01		0x01		0b0	0b0	0b0	0b0
Access Type			Write, Read			Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OV_LEVEL	5:4	V_{DDSW} overvoltage comparator trip level V_{TRIP_OV}	0x0: 1.105V + V_{HYST_OV} 0x1: 1.124V + V_{HYST_OV} 0x2: 1.157V + V_{HYST_OV} 0x3: 1.184V + V_{HYST_OV}
LDOH_TEST_MODE	2	Enables VDD regulator test mode.	0b0: Disable VDD regulator test mode 0b1: Enable VDD regulator test mode
LDOH_EN	0	Enables VDD regulator.	0b0: Disable VDD regulator 0b1: Enable VDD regulator

PWR0 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
Reset	0b000			0b00000				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:5	Core 1V V_{DD_sw} Status. Bits 0 and 1 are identical latched high flags that indicate V_{DD_sw} < 0.82V when set. Status clears when read if V_{DD_sw} > 0.82V. This status indicator drivers VDDBAD_INT_FLAG.	0bX00: V_{DD_sw} > 0.82V 0bX11: V_{DD} < 0.82V observed since last read (latched, read to clear)
CMP_STATUS	4:0	Power Manager Comparator Status. Status indicators are latched low if an undervoltage occurs on the specified supply. Clear to read. Combined status indicators drive VDDCMP_INT_FLAG.	0bXXXX0: V_{DD18} < 1.617V (latched, read to clear) 0bXXXX1: V_{DD18} > 1.617V 0bXXX0X: V_{DDIO} < 1.617V (latched, read to clear) 0bXXX1X: V_{DDIO} > 1.617V 0bXX0XX: V_{DD_sw} < 0.802V (latched, read to clear) 0bXX1XX: V_{DD_sw} > 0.802V

PWR4 (0xC)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b1	0xA			
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable wake-up by local µC from SDA_RX pin.	0b0: Local wake-up enabled 0b1: Local wake-up disabled
WAKE_EN_B	5	Enable wake-up by remote chip connected to Link B.	0b0: Link B remote wake-up disabled 0b1: Link B remote wake-up enabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to Link A.	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled

CTRL0 (0x10)*

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	–	LINK_CFG[1:0]	
Reset	0b0	0b0	0b0	0b1	0b0	–	0b01	
Access Type	Write, Read	Write, Read	Write Clears All, Read	Write, Read	Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Writing 1 to this bit resets the device. All blocks, and registers are reset to defaults. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset
RESET_LINK	6	Resets the whole data path (keeps register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT	5	Resets the whole data path (keeps register settings) one shot. Write 1 to activate reset, bit self clears and automatically releases reset.	0b0: No action 0b1: Reset data path
AUTO_LINK	4	Automatically selects which link to enable (A or B). Dual-link mode is not automatic. For dual-link mode, set LINK_CFG = 00.	0b0: Disable auto-link configuration 0b1: Enable auto-link configuration
SLEEP	3	Activates sleep mode.	0b0: Sleep mode disabled 0b1: Sleep mode enabled

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_CFG	1:0	AUTO_LINK and this bitfield select the link configuration per the decode table.	0b00: If AUTO_LINK = 0, Dual-link selected. If AUTO_LINK = 1, Link mode is automatically selected 0b01: If AUTO_LINK = 0, Link A is selected. If AUTO_LINK = 1, Link mode is automatically selected 0b10: If AUTO_LINK = 0, Link B is selected. If AUTO_LINK = 1, Link mode is automatically selected 0b11: Reserved

CTRL1 (0x11)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	CXTP_B	RSVD	CXTP_A
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b1	0b0
Access Type						Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_B	2	Coax/twisted-pair cable select for Link B. Bit is set according to the latched CXTP pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/twisted-pair cable select for Link A. Bit is set according to the latched CXTP pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

CTRL3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	DUAL_LINK_MODE	LOCKED	ERROR	CMU_LOCKED	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type				Read Only	Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
DUAL_LINK_MODE	4	Dual-link mode active.	0b0: Dual-link mode not active 0b1: Dual-link mode active
LOCKED	3	GMSL2 link locked (bidirectional).	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects error status (inverse of ERRB pin value).	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock multiplier unit (CMU) locked.	0b0: CMU not locked 0b1: CMU locked

INTR0 (0x18)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	FW_OSC_PU	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	0b1	0b0	0b1	–	0b0	0b000		
Access Type		Write, Read		–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FW_OSC_PU	6	Firmware mode free running oscillator power-up.	0b0: Disable firmware mode free running oscillator power-up 0b1: Enable firmware mode free running oscillator power-up
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A, DEC_ERR_B and IDLE_ERR_x bitfields after ERRB pin is asserted for 1µs.	0b0: Auto reset disabled 0b1: Auto reset enabled
DEC_ERR_THR	2:0	Decoding and idle error reporting threshold DEC_ERR_FLAG_A is asserted when DEC_ERR_A ≥ DEC_ERR_THR DEC_ERR_FLAG_B is asserted when DEC_ERR_B ≥ DEC_ERR_THR IDLE_ERR_FLAG is asserted when IDLE_ERR_A ≥ DEC_ERR_THR or IDLE_ERR_B ≥ DEC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

INTR1 (0x19)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0x0				0b0	0b000		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet count multiplier exponent. See the description of PKT_CNT bitfield (register CNT4).	0bXXX: PKT_CNT exponent
AUTO_CNT_RST_EN	3	Automatically resets PKT_CNT bitfield (register CNT4) after ERRB pin is asserted for 1µs.	0b0: Auto reset disabled 0b1: Auto reset enabled
PKT_CNT_THR	2:0	Packet count reporting threshold. See the description of PKT_CNT bitfield (register CNT4). PKT_CNT_FLAG is asserted when PKT_CNT ≥ PKT_CNT_THR.	0b000: 1 packet 0b001: 2 packets 0b010: 4 packets 0b011: 8 packets 0b100: 16 packets 0b101: 32 packets 0b110: 64 packets 0b111: 128 packets

INTR2 (0x1A)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_OEN	PMX_ERR_OEN	–	RSVD	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	0b0	–	0b0	0b1	0b1
Access Type			Write, Read	Write, Read	–		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_OEN	5	Enables reporting of remote error status (REM_ERR) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
PMX_ERR_OEN	4	Enables reporting of picomax error status (PMX_ERR_FLAG) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_B	1	Enables reporting of decoding errors (DEC_ERR_FLAG_B) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enables reporting of decoding errors (DEC_ERR_FLAG_A) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_FLAG	PMX_ERR_FLAG	–	RSVD	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type			Read Only	Read Clears All	–		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_FLAG	5	Received remote side-error status (inverse of remote side ERRB pin level).	0b0: No remote side error 0b1: Remote side error
PMX_ERR_FLAG	4	Picomax Error Flag. Asserted when picomax signals it detected an error or other significant event.	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_B	1	Decoding Error Flag for Link B. Asserted when DEC_ERR_B ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_A	0	Decoding Error Flag for Link A. Asserted when DEC_ERR_A ≥ DEC_ERR_THR.	0b0: Flag not asserted 0b1: Flag asserted

INTR4 (0x1C)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_OEN_B	EOM_ERR_OEN_A	HDCP2_INT_OEN	HDCP_INT_OEN	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_B	7	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_B - 0x1D) for Link B at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
EOM_ERR_OEN_A	6	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_A - 0x1D) for Link A at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
HDCP2_INT_OEN	5	Enables reporting of GMSL HDCP2 interrupt (HDCP2_INT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
HDCP_INT_OEN	4	Enables reporting of GMSL HDCP interrupt (HDCP_INT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enables reporting of packet count flag (PKT_CNT_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
WM_ERR_OEN	0	Enables reporting of watermark errors (WM_ERR_FLAG - 0x1D) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	HDCP2_INT_FLAG	HDCP_INT_FLAG	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_B	7	Eye opening is below configured threshold for Link B.	0b0: No EOM error on Link B 0b1: EOM error on Link B
EOM_ERR_FLAG_A	6	Eye-opening is below the configured threshold for Link A.	0b0: No EOM error on Link A 0b1: EOM error on Link A
HDCP2_INT_FLAG	5	Asserted when there is a GMSL HDCP2 interrupt. See HDCP2 interrupts in HDCP2 register for more detail.	0b0: No HDCP2 interrupt 0b1: HDCP2 interrupt
HDCP_INT_FLAG	4	Asserted when there is a GMSL HDCP interrupt. See HDCP interrupts in HDCP register for more detail.	0b0: No HDCP interrupt 0b1: HDCP interrupt
MAX_RT_FLAG	3	Combined ARQ maximum retransmission limit error flag. Asserted when any of the selected channels ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN register bit.	0b0: Flag not asserted 0b1: Flag asserted

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_FLAG	2	Combined ARQ retransmission event flag. Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN register bit.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet Count Flag. Asserted when PKT_CNT ≥ PKT_CNT_THR.	0b0: Flag not asserted 0b1: Flag asserted
WM_ERR_FLAG	0	Watermark Error Flag. Asserted when a watermark error is detected.	0b0: Flag not asserted 0b1: Flag asserted

INTR6 (0x1E)*

BIT	7	6	5	4	3	2	1	0
Field	FEC_RX_ERR_OEN	DSCD_ERR_OEN	LOCK_B_OEN	LOCK_A_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	APRBS_ERR_OEN	VID_PXL_CRC_ERR_OEN
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_RX_ERR_OEN	7	Enables reporting of FEC receive errors (FEC_RX_ERR_FLAG - 0x1F) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
DSCD_ERR_OEN	6	Enables reporting of DSC decoder errors (DSCD_ERR_FLAG - 0x1F) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
LOCK_B_OEN	5	Enables reporting of Link B lock status (LOCK_B - 0x1F) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
LOCK_A_OEN	4	Enables reporting of Link A lock status (LOCK_A - 0x1F) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
LCRC_ERR_OEN	3	Enables reporting of video line CRC errors (LCRC_ERR_FLAG - 0x1F) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VPRBS_ERR_OEN	2	Enables reporting of video PRBS errors (VPRBS_ERR_FLAG - 0x1F) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
APRBS_ERR_OEN	1	Enables reporting of audio PRBS errors (APRBS_ERR_FLAG - 0x1F) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VID_PXL_CRC_ERR_OEN	0	Enables reporting of video pixel CRC errors (VID_PXL_CRC_ERR_FLAG - 0x1F) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	FEC_RX_ERR_FLAG	DSCD_ERR_FLAG	LOCK_B	LOCK_A	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	APRBS_ERR_FLAG	VID_PXL_CRC_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
FEC_RX_ERR_FLAG	7	FEC Receive Error Flag. Asserted when any FEC receive error exceeds its threshold. To properly clear the error flag write 1 to fec_clr_stats bit in register 0x600.	0b0: Flag not asserted 0b1: Flag asserted
DSCD_ERR_FLAG	6	DSC Decoder Error Flag. Asserted when any DSC decoder error occurs. This flag is set by changes in error status in DSC decoder error registers 0x4508 and x4509. To clear this flag write 0xFF to registers 0x4508 and 0x4509 to clear all the individual DSC decoder error bits.	0b0: Flag not asserted 0b1: Flag asserted
LOCK_B	5	Link B Lock Status.	0b0: Link B not locked 0b1: Link B locked
LOCK_A	4	Link A Lock Status.	0b0: Link A not locked 0b1: Link A locked
LCRC_ERR_FLAG	3	Video Line CRC Error Flag. Asserted when a video line CRC error is detected.	0b0: Flag not asserted 0b1: Flag asserted
VPRBS_ERR_FLAG	2	Video PRBS Error Flag. Asserted when VPRBS_ERR > 0.	0b0: Flag not asserted 0b1: Flag asserted
APRBS_ERR_FLAG	1	Audio PRBS Error Flag. Asserted when APRBS_ERR > 0.	0b0: Flag not asserted 0b1: Flag asserted
VID_PXL_CRC_ERR_FLAG	0	Video Pixel CRC Error Flag. Asserted when > 0.	0b0: Flag not asserted 0b1: Flag asserted

INTR8 (0x20)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0b0	–	–	0b11111				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmit local error status (inverse of ERRB pin level) to remote side through GPIO channel.	0b0: Transmit error status disabled 0b1: Transmit error status enabled
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX.	0bXXXXX: Value of GPIO ID for transmitting ERR_TX

INTR9 (0x21)*

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
Reset	0b0	0b1	–	0b11111				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Receive remote error status (inverse of ERRB pin level) through GPIO channel.	0b0: Receive error status disabled 0b1: Receive error status enabled
ERR_RX_ID	4:0	GPIO ID used for receiving ERR_RX.	0bXXXXX: Value of GPIO ID for receiving ERR_TX

CNT0 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	Number of decoding (disparity) errors detected at Link A. Resets after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

CNT1 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_B	7:0	Number of decoding (disparity) errors detected at Link B. Resets after reading or with the rising edge of LOCK.	0xXX: Number of Link B decoding errors detected

CNT4 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of received packets of a selected type. Packet type is selected with PKT_CNT_SEL (0x2C) bitfield Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT x ($2^{PKT\_CNT\_EXP}$) and < (PKT_CNT + 1) x ($2^{PKT\_CNT\_EXP}$). When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

TX1 (0x29)*

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_GEN	–	ERRG_EN_B	ERRG_EN_A	–	–	RSVD	RSVD
Reset	0b0	–	0b0	0b0	–	–	0b0	0b0
Access Type	Write, Read	–	Write, Read	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_GEN	7	Enables link PRBS-7 generator.	0b0: Link PRBS generator disabled 0b1: Link PRBS generator enabled
ERRG_EN_B	5	Enables Error Generator for Link B.	0b0: Link B error generator disabled 0b1: Link B error generator enabled
ERRG_EN_A	4	Enables Error Generator for Link A.	0b0: Link A error generator disabled 0b1: Link A error generator enabled

TX2 (0x2A)*

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0b00		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated.	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error-Generator Average Bit-Error Rate.	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_BURST	3:1	Error-Generator Burst-Error Length.	0b000: 1 bit 0b001: 2 bits 0b010: 3 bits 0b011: 4 bits 0b100: 8 bits 0b101: 12 bits 0b110: 16 bits 0b111: 20 bits
ERRG_PER	0	Error-Generator Error-Distribution Selection.	0b0: Pseudorandom 0b1: Periodic

TX3 (0x2B)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
Reset	0b01		–	–	–	0b100		
Access Type			–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	ARQ Timeout Duration Multiplier. Multiplies a timeout base constant to set the ARQ timeout. The timeout base is set by the reverse channel link rate (RX_RATE) as follows: RX_RATE Timeout Base 187.5Mbps 8µs	0b000: 0.5 x Timeout Base 0b001: 1.0 x Timeout Base 0b010: 1.5 x Timeout Base 0b011: 2.0 x Timeout Base 0b100: 2.5 x Timeout Base 0b101: 3.0 x Timeout Base 0b110: 3.5 x Timeout Base 0b111: 4.0 x Timeout Base

RX0 (0x2C)*

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
Reset	0b00		–	0b0	0x0			
Access Type	Write, Read		–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Select the sub-type of low bandwidth (LBW) packets to count at PKT_CNT (0x26) bitfield.	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_SEL	3:0	Selects the type of received packets to count at PKT_CNT (0x26) bitfield.	0x0: None 0x1: VIDEO 0x2: AUDIO 0x3: INFO Frame 0x4: SPI 0x5: I^2C 0x6: UART 0x7: GPIO 0x8: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All 0xF: Unknown and packets with error

GPIOA (0x30)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RX_FAST_BIDIR_EN	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0b1	0b000001					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_FAST_BIDIR_EN	7	GPIO Fast Direction Switch for Bidirectional IO.	0b0: Fast direction switch disabled 0b1: Fast direction switch enabled
GPIO_FWD_CDLY	5:0	Compensation Delay Multiplier for the Forward Direction. This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x31)*

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0b10		0b001000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet. This allows grouping transitions of different GPIO inputs in a single packet and so increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation Delay Multiplier for the Reverse Direction. This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

I2C_0 (0x40)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I^2C-to-I^2C master bit-rate setting. Configures the I^2C bit rate used by the internal I^2C master (in the device on remote side from the external I^2C master). Set this according to the I^2C speed mode.	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C Standard-mode speed 0b11: Reserved
SLV_TO	2:0	I^2C-to-I^2C slave timeout setting. Internal GMSL2 I^2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x41)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	0b0	0b101			–	0b110		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	I²C-to-I²C master bit-rate setting. Configures the I²C bit rate used by the internal I²C master (in the device on remote side from the external I²C master). Set this according to the I²C speed mode.	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO	2:0	I²C-to-I²C master timeout setting. Internal GMSL2 I²C master times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x42)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I²C address translator source A. When I²C device address matches I²C SRC_A, internal I²C master (on remote side) replaces the device address by I²C DST_A.	0bXXXXXXX: Value of I²C SRC_A

I2C_3 (0x43)*

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I²C address translator destination A. See the description of I²C SRC_A.	0bXXXXXXX: Value of I²C DST_A

I2C_4 (0x44)*

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I²C address translator source B. When I²C device address matches I²C SRC_B, internal I²C master (on remote side) replaces the device address by I²C DST_B.	0bXXXXXXX: Value of I²C SRC_B

I2C_5 (0x45)*

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I²C address translator destination B. See the description of I²C SRC_B.	0bXXXXXXX: Value of I²C DST_B

I2C_7 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
Reset	0b0	0b0	–	–	–	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
UART_RX_OVERFLOW	7	UART Rx FIFO Overflow Flag.	0b0: No overflow occurred 0b1: Overflow occurred
UART_TX_OVERFLOW	6	UART Tx FIFO Overflow Flag.	0b0: No overflow occurred 0b1: Overflow occurred
I2C_TIMED_OUT	2	Internal I²C-to-I²C slave or master has timed out while receiving packet from remote device.	0b0: Timeout has not occurred 0b1: Timeout has occurred
REM_ACK_ACKED	1	Inverse of the I²C acknowledge bit received from remote side.	0b0: I²C acknowledge bit received as 1 0b1: I²C acknowledge bit received as 0
REM_ACK_RECVED	0	I²C acknowledge bit for any I²C byte has been received from the remote side for the previous I²C packet.	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received

UART_0 (0x48)*

BIT	7	6	5	4	3	2	1	0
Field	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	0b01		0b0	0b0	0b0	0b01		0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ARB_TO_LEN	7:6	UART Rx source arbitration timeout duration. UART Rx processes packets from a single UART source at any time. When UART Rx does not receive any UART packets for this duration, it selects the next UART source according to the source ID of the next following received packet.	0b00: 1ms 0b01: 2ms 0b10: 8ms 0b11: 32ms
REM_MS_EN	5	Enables UART bypass mode control by remote GPIO pin. When set, remote chip's GPIO is used as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN	4	Enables UART bypass mode control by local GPIO pin. Set to use GPIO2 pin as MS pin (UART mode select). When MS is high, chip is in bypass mode, otherwise chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR	3	Selects whether or not to receive and send parity bit in bypass mode.	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO	2:1	UART soft-bypass timeout duration. When set to 11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power-down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled
BYPASS_EN	0	Enables UART soft-bypass mode. Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO register), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft-bypass mode disabled 0b1: UART soft-bypass mode enabled

UART_1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB[7:0]							
Reset	0x96							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB	7:0	UART detected bit length, low 8 bits.	0xXX: UART detected bit length (lower 8 bits)

UART_2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
Reset	0b10		0b000000					
Access Type	Write, Read		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_DELAY	7:6	UART Initial Output Delay. In base mode, first received UART byte of a packet (sync or acknowledge frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back to back on remote side.	0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit
BITLEN_MSB	5:0	UART detected bit length, high 6 bits.	0bXXXXXX: UART detected bit length (upper 6 bits)

RX0 (0x50)*

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0b00	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	Enables Receive Packet CRC.	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Receive packets with selected stream ID.	0bXX: Receive packets with this stream ID

TR0 (0x58)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x59)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x5B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSbs are set by ADD2 and ADD1. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x5C)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x5D)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0b1	0b0	0b0	0b1	0b1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enables ARQ.	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x5E)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ stops retransmission after trying to retransmit this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

TR0 (0x60)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x61)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x63)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSbs are set by ADD2 and ADD1. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x64)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x68)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x69)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x W_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel-base bandwidth value

TR3 (0x6B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSbs are set by ADD2 and ADD1. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x6C)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x6D)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0b1	0b0	0b0	0b1	0b1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enables ARQ.	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x6E)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ stops retransmission after trying to retransmit this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0x70)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x71)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x73)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSbs are set by ADD2 and ADD1. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x74)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received … … 0xFF: Packets from all source IDs received

ARQ0 (0x75)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0b1	0b0	0b0	0b1	0b1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values

BITFIELD	BITS	DESCRIPTION	DECODE
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enables ARQ.	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x76)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ stops retransmission after trying to retransmit this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x77)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0x78)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x79)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x7B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSbs are set by ADD2 and ADD1. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x7C)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x7D)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0b1	0b0	0b0	0b1	0b1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets

BITFIELD	BITS	DESCRIPTION	DECODE
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0: Use SRC_ID of the received data packet 1: Use TX_SRC_ID register
ARQ_EN	3	Enables ARQ.	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x7E)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ stops retransmission after trying to retransmit this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x7F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

TR0 (0x80)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x81)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x83)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSbs are set by ADD2 and ADD1. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x84)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x85)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0b1	0b0	0b0	0b1	0b1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0: All received acknowledge packets are accepted 1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0: Use SRC_ID of the received data packet 1: Use TX_SRC_ID register

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_EN	3	Enables ARQ.	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x86)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ stops retransmission after trying to retransmit this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x87)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

TR0 (0x88)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x89)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x8B)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSbs are set by ADD2 and ADD1. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x8C)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x8D)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0b1	0b0	0b0	0b1	0b1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enables ARQ.	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x8E)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ stops retransmission after trying to retransmit this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x8F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

TR0 (0x90)*

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel.	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[1:0] setting

TR1 (0x91)*

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0b10		0b110000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR3 (0x93)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD	–	TX_SRC_ID[2:0]		
Reset	–	–	0b1	0b1	–	0b000		
Access Type	–	–			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value of the 2 MSbs are set by ADD2 and ADD1. Default value of the LSb is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x94)*

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ0 (0x95)*

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	ARQ_EN	–	–	–
Reset	0b1	0b0	0b0	0b1	0b1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on splitter mode.	0b0: ARQ settings are selected based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are based on internal values
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: All received acknowledge packets are accepted 0b1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets. The SRC_ID selected in this bitfield is used only when ARQ_AUTO_CFG = 0.	0b0: Use SRC_ID of the received data packet 0b1: Use TX_SRC_ID register
ARQ_EN	3	Enables ARQ.	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x96)*

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ stops retransmission after trying to retransmit this many times for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x97)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel.	0xXX: Count of retransmissions for this channel

VIDEO_RX0 (0x100)*

BIT	7	6	5	4	3	2	1	0
Field	LCRC_ERR	RSVD	RSVD	RSVD	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
Reset	0b0	0b0	0b1	0b1	0b0	0b0	0b1	0b0
Access Type	Read Clears All						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR	7	Video Line CRC Error Flag.	0b0: No video line CRC detected 0b1: Video line CRC detected
LINE_CRC_EN	1	Enables Video Line CRC.	0b0: Video line CRC disabled 0b1: Video line CRC enabled

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_PKT_DET	0	Disable Packet Detector. If the video is restarted with a different BPP when the packet detector is disabled, toggle this register or the video receive enable register to make sure the video link restarts.	0b0: Packet detector enabled 0b1: Packet detector disabled

VIDEO_RX3 (0x103)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
Reset	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type		Write, Read	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HD_TR_MODE	6	Enables HS and DE tracking full periodic pattern.	0b0: Allow only partial periodic HS, DE 0b1: Allow partial periodic and full periodic HS, DE
DLOCKED	5	DE Tracking Locked Flag.	0b0: DE tracking not locked 0b1: DE tracking locked
VLOCKED	4	VS Tracking Locked Flag.	0b0: VS tracking not locked 0b1: VS tracking locked
HLOCKED	3	HS Tracking Locked Flag	0b0: HS tracking not locked 0b1: HS tracking locked
DTRACKEN	2	Enables DE Tracking (disables if FSYNC = 1). The system observes DE pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: DE tracking disabled 0b1: DE tracking enabled
VTRACKEN	1	Enables VS Tracking (disables if FSYNC = 1). The system observes VS pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: VS tracking disabled 0b1: VS tracking enabled
HTRACKEN	0	Enables HS Tracking (disables if FSYNC = 1). The system observes HS pulses and when it locks on the pattern, it can compensate for a limited number of missing pulses or suppress glitches.	0b0: HSYNC tracking disabled 0b1: HSYNC tracking enabled

VIDEO_RX8 (0x108)

BIT	7	6	5	4	3	2	1	0
Field	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x2			
Access Type	Read Clears All	Read Only	Read Only	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
VID_BLK_LEN_ERR	7	Video Rx Block Length Error Flag.	0b0: No error detected 0b1: Video Rx block length error detected
VID_LOCK	6	Video Pipeline Locked Flag.	0b0: Video pipeline not locked 0b1: Video pipeline locked
VID_PKT_DET	5	Sufficient Video Rx Packet Throughput Flag	0b0: Not enough throughput 0b1: Sufficient throughput detected
VID_SEQ_ERR	4	Video Rx Sequence Error Flag.	0b0: No error detected 0b1: Error detected

AUDIO_TX0 (0x148)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		INV_SCK	INV_WS	FORCE_AUD	AUD_SINK_SRC
Reset	0b10		0b11		0b0	0b0	0b0	0b0
Access Type					Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
INV_SCK	3	Inverts SCK (when using local I^2S interface).	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS	2	Inverts WS (when using local I^2S interface).	0b0: Do not invert WS 0b1: Invert WS
FORCE_AUD	1	Forces audio data to zero.	0b0: Normal audio data 0b1: Audio data forced to zero
AUD_SINK_SRC	0	Enables sink-sourced mode for audio Tx. For use on the deserializer side when forward audio clock is the master.	0b0: Transmit audio in normal mode 0b1: Transmit audio in sink-sourced mode

AUDIO_TX1 (0x149)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_PRIO[1:0]		AUD_STR_TX[1:0]		AUD_DRIFT_DET_EN	AUD_INF_PER	RSVD[1:0]	
Reset	0b01		0b00		0b1	0b1	0b10	
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_PRIO	7:6	Scheduler audio priority.	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 3
AUD_STR_TX	5:4	Audio Stream ID.	0b00: Use stream ID 0 0b01: Use stream ID 1 0b10: Use stream ID 2 0b11: Use stream ID 3
AUD_DRIFT_DET_EN	3	Enables audio clock drift detection. Resets subsystem on SCK frequency drift and reports it.	0b0: Audio clock drift detection disabled 0b1: Audio clock drift detection enabled
AUD_INF_PER	2	Enables audio periodic info frame transmission.	0b0: Audio periodic info frame transmission disabled 0b1: Audio periodic info frame transmission enabled

AUDIO_TX5 (0x14D)

BIT	7	6	5	4	3	2	1	0
Field	AUD_DRIFT_ERR	AUD_FIFO_WARN	AUD_OVERFLOW	ACLKDET	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_DRIFT_ERR	7	Audio clock frequency drift flag.	0b0: Audio clock frequency drift not detected 0b1: Audio clock frequency drift detected
AUD_FIFO_WARN	6	Audio FIFO half full flag.	0b0: Audio FIFO is less than or equal to half full 0b1: Audio FIFO is more than half full
AUD_OVERFLOW	5	Audio buffer overflow flag.	0b0: Audio buffer overflow not detected 0b1: Audio buffer overflow detected
ACLKDET	4	Audio clock flag.	0b0: Audio clock not detected 0b1: Audio clock detected

AUDIO_TX7 (0x14F)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_SEL	PRBSEN_AUD	RSVD[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_SEL	7	Audio PRBS clock selection. Set to 0 in sink-sourced mode.	0b0: SCK selected 0b1: Internal oscillator clock selected (150MHz)
PRBSEN_AUD	6	Enables audio PRBS.	0b0: Audio PRBS disabled 0b1: Audio PRBS enabled

AUDIO_TX8 (0x150)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_WS_LEN	PRBS_WS_GEN	RSVD[5:0]					
Reset	0b0	0b1	0b000000					
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_WS_LEN	7	Selects the length of the generated WS pulse.	0b0: 256 data bits per WS cycle 0b1: 32 data bits per WS cycle
PRBS_WS_GEN	6	Enables audio PRBS WS generation.	0b0: Audio PRBS WS generation disabled 0b1: Audio PRBS WS generation enabled

AUDIO_RX1 (0x158)*

BIT	7	6	5	4	3	2	1	0
Field	AUD_RX_SINK_SRC	RSVD	RSVD	RSVD	INV_SCK_RX	INV_WS_RX	–	AUD_EN_RX
Reset	0b0	0b0	0b1	0b0	0b0	0b0	–	0b1
Access Type	Write, Read				Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_RX_SINK_SRC	7	Enables sink-sourced mode for audio Rx (for use on the serializer side).	0b0: Received audio in normal mode 0b1: Received audio in sink-sourced mode
INV_SCK_RX	3	Inverts SCK at I^2S output.	0b0: Do not invert SCK 0b1: Invert SCK
INV_WS_RX	2	Inverts WS at I^2S output.	0b0: Do not invert WS 0b1: Invert WS
AUD_EN_RX	0	Enables audio receiver adapter.	0b0: Audio receiver disabled 0b1: Audio receiver enabled

AUDIO_RX4 (0x15B)

BIT	7	6	5	4	3	2	1	0
Field	APRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_ERR	7:0	Audio PRBS error counter Clears on read.	0xXX: Number of audio PRBS errors

AUDIO_RX7 (0x15E)*

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			APRBS_CHK_EN	AUD_STRM[1:0]		RSVD	RSVD
Reset	0b000			0b0	0b00		0b1	0b0
Access Type				Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
APRBS_CHK_EN	4	Enables audio PRBS checker.	0b0: Audio PRBS checker disabled 0b1: Audio PRBS checker enabled
AUD_STRM	3:2	Selected audio stream for reception.	0b00: Receive stream ID 0 0b01: Receive stream ID 1 0b10: Receive stream ID 2 0b11: Receive stream ID 3

AUDIO_RX9 (0x160)

BIT	7	6	5	4	3	2	1	0
Field	AUD_BLK_LEN_ERR	AUD_LOCK	AUD_PKT_DET	APRBS_VALID	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Read Clears All	Read Only	Read Only	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
AUD_BLK_LEN_ERR	7	Audio Rx Block Length Error Flag.	0b0: Received audio block length error not detected 0b1: Received audio block length error detected
AUD_LOCK	6	Audio pipeline frequency locked flag.	0b0: Audio pipeline frequency is not locked 0b1: Audio pipeline frequency is locked
AUD_PKT_DET	5	Audio Rx: Enough packet throughput detected.	0b0: Valid audio stream not detected 0b1: Valid audio stream detected
APRBS_VALID	4	Audio PRBS active flag.	0b0: Audio PRBS is not running 0b1: Audio PRBS is running

SPI_0 (0x170)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0b00		0b00		0b1	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Program to local ID if filtering packets based on header ID.	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_CC_TRG_ID	5:4	ID for GMSL2 header in SPI control channel bridge mode.	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_IGNR_ID	3	Selects if SPI should use or ignore header ID to decide on packet acceptance.	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_CC_EN	2	Enables control channel SPI bridge function.	0b0: SPI bridge disabled 0b1: SPI bridge enabled
MST_SLVN	1	Selects if SPI is master or slave.	0b0: SPI slave 0b1: SPI master
SPI_EN	0	Enables SPI Channel.	0b0: SPI channel disabled 0b1: SPI channel enabled

SPI_1 (0x171)*

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
Reset	0b000111						0b01	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Sets the packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value more than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes ... ... 0b111111: Packet size is 127 bytes
SPI_BASE_PRIO	1:0	Starting GMSL2 request priority. Advances by 1 (if room) if Tx buffer is over half full.	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 3

SPI_2 (0x172)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0b000			0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Suspends GMSL2 request until this number of extra bytes are received on SPI port.	0b00: No extra bytes 0b01: 1 extra byte 0b10: 2 extra bytes 0b11: 3 extra bytes
FULL_SCK_SETUP	4	Samples MISO after half or full SCK period.	0b0: MISO sampled after half SCK period 0b1: MISO sampled after full SCK period
SPI_MOD3_F	3	Allows the supression of an extra SCK prior to SS deassertion when SPI mode 3 is selected.	0b0: Extra SCK present prior to SS deassertion when in SPI mode 3 0b1: Extra SCK suppressed prior to SS deassertion when in SPI mode 3

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_MOD3	2	Selects SPI mode 0 or 3.	0b0: SPI mode 0 0b1: SPI mode 3
SPIM_SS2_ACT_H	1	Sets the polarity for SS2 when the SPI is a master.	0b0: Slave select 2 is active low 0b1: Slave select 2 is active high
SPIM_SS1_ACT_H	0	Sets the polarity for SS1 when the SPI is a master.	0b0: Slave select 1 is active low 0b1: Slave select 1 is active high

SPI_3 (0x173)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between: • Assertion of SS and start of SCK pulses • End of SCK pulses and deassertion of SS • Deassertion of SS and reassertion of SS (if necessary)	0xXX: Number of clock delays

SPI_4 (0x174)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time.	0xXX: Number of clocks for SCK low time

SPI_5 (0x175)*

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time.	0xXX: Number of clocks for SCK high time

SPI_6 (0x176)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	Alternate GPU status register to use for BNE status if GPIO is not available.	0b0: Buffer empty 0b1: Buffer not empty
SPIS_RWN	4	Alternate GPU control register to use for read/write control if GPIO is not available.	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enables GPIO for use as slave select 2 output.	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
SS_IO_EN_1	2	Enables GPIO for use as slave select 1 output.	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
BNE_IO_EN	1	Enables GPIO for use as BNE output for SPI data available status.	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function
RWN_IO_EN	0	Enables GPIO for use as RO input for control of SPI data movement.	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function

SPI_7 (0x177)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
Reset	0b0	0b0	–	0b00000				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	SPI Rx Buffer Overflow Flag.	0b0: No SPI Rx buffer overflow 0b1: SPI Rx buffer overflow
SPI_TX_OVRFLW	6	SPI Tx Buffer Overflow Flag.	0b0: No SPI Tx buffer overflow 0b1: SPI Tx buffer overflow
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer.	0bXXXXX: Number of bytes available

SPI_8 (0x178)*

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100nS increments) for GMSL2 request hold off (0 is disable).	0xXX: Number of 100nS delay increments for GMSL2 request hold off

WM_0 (0x190)*

BIT	7	6	5	4	3	2	1	0
Field	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
Reset	0b0	0b000			0b00		–	0b0
Access Type	Write, Read	Write, Read			Write, Read		–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_LEN	7	Watermark Length.	0b0: 32-bit 0b1: 64-bit
WM_MODE	6:4	Select Watermark Generation Mode.	0b000: Default generator mode - cycle through all four watermarks in video stream (default) 0b001: Error generator mode - cycle through only two watermarks to replicate a frozen frame error condition 0b010-0b111: Reserved
WM_DET	3:2	Watermark Detection/Generation.	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WM_EN	0	Watermark Enable.	0b0: Watermarking blocking disabled 0b1: Watermarking blocking enabled

WM_2 (0x192)*

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			HsyncPol	VsyncPol	WM_NPFILT[1:0]	
Reset	–	0b101			0b0	0b0	0b00	
Access Type	–				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HsyncPol	3	HSYNC polarity (only effective for watermark block).	0b0: Noninverting 0b1: Invert
VsyncPol	2	VSYNC polarity (only effective for watermark block).	0b0: Noninverting 0b1: Invert
WM_NPFILT	1:0	Phase accumulator terminal count.	0bXX: Phase accumulator terminal count

WM_3 (0x193)*

BIT	7	6	5	4	3	2	1	0
Field	–	WM_TH[6:0]						
Reset	–	0x0E						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TH	6:0	Matched filter threshold.	0bXXXXXXX: Matched filter threshold

WM_4 (0x194)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD[1:0]		RSVD	–	WM_MASKMODE[1:0]	
Reset	–	–	0b01		0b0	–	0b00	
Access Type	–	–				–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WM_MASKMODE	1:0	Sets watermark mask for the device.	0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved b011: Reserved

WM_5 (0x195)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	WM_DETOUT	WM_ERROR
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
WM_DETOUT	1	Live frame-based detection output.	0b0: Watermark not detected 0b1: Watermark detected
WM_ERROR	0	Live active-high watermark error.	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.

WM_6 (0x196)

BIT	7	6	5	4	3	2	1	0
Field	WM_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TIMER	7:0	Time in 2msec steps that the frozen frame condition must be observed before an error is generated. A value of 0 disables this filtering.	0xXX: Number of milliseconds

WM_WREN_0 (0x1AE)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_L	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise watermark registers are read-only.	0xBA: Enables writing to WM registers Others: WM registers remain read-only

WM_WREN_1 (0x1AF)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_H	7:0	Write 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise watermark registers are read-only.	0xDC: Enables writing to WM registers Others: WM registers remain read-only

BLANK_COLOR_A (0x1D8)*

Provides a color definition used when blanking video.

BIT	7	6	5	4	3	2	1	0
Field	BLANK_COLOR_A[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BLANK_COLOR_A	7:0	Blank Color Low Byte (bits 7-0). This color is used when video is blanked using the BLANK_VIDEO control.	0xXX: Blank color low byte

BLANK_COLOR_B (0x1D9)*

Provides a color definition used when blanking video.

BIT	7	6	5	4	3	2	1	0
Field	BLANK_COLOR_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BLANK_COLOR_B	7:0	Blank Color Middle Byte (bits 15-8). This color is used when video is blanked using the BLANK_VIDEO control.	0xXX: Blank color middle byte

BLANK_COLOR_C (0x1DA)*

Provides a color definition used when blanking video.

BIT	7	6	5	4	3	2	1	0
Field	BLANK_COLOR_C[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BLANK_COLOR_C	7:0	Blank Color High Byte (bits 23-16). This color is used when video is blanked using the BLANK_VIDEO control.	0xXX: Blank color high byte

PRBS_ERR (0x1DB)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_ERR	7:0	Video PRBS Error Counter. Clears on read.	0xXX: Number of video PRBS errors since last read

VPRBS (0x1DC)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
Reset	–	–	0b0	0b0	–	–	–	0b0
Access Type	–	–	Read Only	Write, Read	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_FAIL	5	Video PRBS Check Pass/Fail. Video pipeline should be locked for proper operation of this register.	0b0: Video PRBS check passed 0b1: Video check failed
VPRBS_CHK_EN	4	Enables Video PRBS Checker.	0b0: Video PRBS checker disabled 0b1: Video PRBS checker enabled
VIDEO_LOCK	0	Indicates whether or not video channel is locked and outputting valid video data.	0b0: Video channel not locked 0b1: Video channel locked

DISP_CTRL (0x1DD)*

BIT	7	6	5	4	3	2	1	0
Field	WM_SYNC_POL_CNV	INVERT_PIX	BLANK_VIDEO	VID_BYTE_SWAP	–	LUT_C_EN	LUT_B_EN	LUT_A_EN
Reset	0b1	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_SYNC_POL_CNV	7	Converts sync polarity to active high for watermark.	0b0: Do not convert sync polarity to active high 0b1: Convert sync polarity to active high
INVERT_PIX	6	Inverts video pixel color by inverting each pixel bit.	0b0: Do not invert pixel bits 0b1: Invert pixel bits
BLANK_VIDEO	5	Blanks video output using the color specified by BLANK_COLOR.	0b0: Do not blank video output 0b1: Blank video output
VID_BYTE_SWAP	4	Swaps video (pixel) bytes 0 and 2. For RGB pixels this swaps red (R) and blue (B).	0b0: Do not swap video bytes 0 and 2 0b1: Swap video bytes 0 and 2
LUT_C_EN	2	Enables Color C Lookup Table (LUT) for bits [7:0].	0b0: Color C LUT disabled 0b1: Color C LUT enabled
LUT_B_EN	1	Enables Color B Lookup Table (LUT) for bits [7:0].	0b0: Color B LUT disabled 0b1: Color B LUT enabled
LUT_A_EN	0	Enables Color A Lookup Table (LUT) for bits [7:0].	0b0: Color A LUT disabled 0b1: Color A LUT enabled

VIDEO_CTRL_OUT (0x1DF)*

Video Control Out

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	HS_OUT_EN	VS_OUT_EN	WM_DET_OUT_EN
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HS_OUT_EN	2	Enables HSYNC output on GPIO.	0b0: HSYNC not output 0b1: Output HSYNC from GPIO
VS_OUT_EN	1	Enables VSYNC output on GPIO.	0b0: VSYNC not output 0b1: Output VSYNC from GPIO
WM_DET_OUT_EN	0	Enables watermark detect live status output on GPIO.	0b0: Watermark detection not output 0b1: Output watermark detection from GPIO

GPIO_A (0x2B0)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2B1)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00000				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2B2)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00000				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B3)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2B4)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00001				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2B5)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00001				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B6)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2B7)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00010				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2B8)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00010				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B9)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO Out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2BA)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00011				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2BB)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00011				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2BC)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2BD)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00100				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2BE)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00100				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2BF)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C0)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00101				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C1)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00101				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C2)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C3)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00110				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C4)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00110				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C5)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C6)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00111				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C7)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00111				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C8)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C9)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01000				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2CA)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01000				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2CB)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2CC)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01001				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2CD)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01001				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2CE)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2CF)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b01010				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D0)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01010				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2D1)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2D2)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b00		0b1	0b01011				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D3)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01011				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2D4)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2D5)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b00		0b1	0b01100				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D6)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01100				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2D7)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2D8)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b00		0b1	0b01101				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection.	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D9)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01101				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2DA)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b0	0b0	0b0	0b1	0b1	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2DB)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
Reset	0b01		0b0	0b01110				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2DC)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01110				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

GPIO_A (0x2DD)*

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b0	0b0	0b0	0b1	0b1	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength.	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Enables jitter minimization compensation.	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level.	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control.	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control.	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver.	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2DE)*

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
Reset	0b01		0b0	0b01111				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting.	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2DF)*

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01111				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function I/O setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines I/O type.	0b0: Non-GPIO function determines I/O type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine I/O type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving.	0bXXXXX: This GPIO receive ID

INTR10 (0x440)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VDD_OV_INT_OEN	VDDBAD_INT_OEN	VDDCMP_INT_OEN	RSVD
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VDD_OV_INT_OEN	3	Enables reporting of V_{DD} overvoltage interrupt (VDD_OV_INT_FLAG) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VDDBAD_INT_OEN	2	Enables reporting of V_{DDBAD} interrupt (VDDBAD_INT_FLAG) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled
VDDCMP_INT_OEN	1	Enables reporting of V_{DD} comparator interrupt (VDDCMP_INT_FLAG) at ERRB pin.	0b0: Reporting disabled 0b1: Reporting enabled

INTR11 (0x441)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VDD_OV_INT_FLAG	VDDBAD_INT_FLAG	VDDCMP_INT_FLAG	RSVD
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
VDD_OV_INT_FLAG	3	V_{DD} Overvoltage Status Interrupt Flag. This flag is operational only when Video Lock is present.	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	2	Combined V_{DD} Bad Indicator. See VDDBAD_STATUS for details of error states that drive this flag. To clear, first read VDDBAD_STATUS and then read VDDBAD_INT_FLAG.	0b0: No V_{DD} bad error 0b1: V_{DD} bad error state asserted
VDDCMP_INT_FLAG	1	Combined V_{DD} Comparator Output Flag. See CMP_STATUS for details of error states that drive this flag. To clear, first read CMP_STATUS and then read VDDCMP_INT_FLAG.	0b0: No V_{DD} comparator error 0b1: V_{DD} comparator error state asserted

I2C_PT_0 (0x480)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_PT	5:4	Pass-through I²C-to-I²C slave setup and hold time setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I²C slave. Set this according to the I²C speed mode: Fast-mode Plus = 00 Fast-mode = 01 Standard-mode = 10	0b00: Set for I²C Fast-mode Plus speed 0b01: Set for I²C Fast-mode speed 0b10: Set for I²C standard-mode speed 0b11: Reserved
SLV_TO_PT	2:0	Pass-through I²C-to-I²C slave timeout setting. Internal GMSL2 I²C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_PT_1 (0x481)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
Reset	0b0	0b101			–	0b110		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT	6:4	Pass-through I²C-to-I²C master bit rate setting. Configures the I²C bit rate used by the internal I2C master (in the device on remote side from the external I²C master). Set this according to the I²C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed

BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_PT	2:0	Pass-through I²C-to-I²C master timeout setting. Internal GMSL2 I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_PT_10 (0x48A)

BIT	7	6	5	4	3	2	1	0
Field	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Read Only	Read Only	Read Only	Write, Read	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
XOVER_EN_2	7	Connects pass-through I²C/UART Channel 2 to main control channel on remote side.	0b0: Do not connect 0b1: Connect
I2C_TIMED_OUT_2	6	In pass-through I²C Channel 2, internal I²C-to-I²C slave or master has timed out while receiving packet from remote device.	0b0: Timeout has not occurred 0b1: Timeout has occurred
REM_ACK_ACKED_2	5	In pass-through I²C Channel 2, inverse of the I²C acknowledge bit received from remote side.	0b0: I²C acknowledge bit received as 1 0b1: Inverse I²C acknowledge bit received as 0
REM_ACK_RECVED_2	4	In pass-through I²C Channel 2, I²C acknowledge bit for any I²C byte is received from remote side for the previous I²C packet.	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received
XOVER_EN_1	3	Connects pass-through I²C/UART Channel 1 to main control channel on remote side.	0b0: Do not connect 0b1: Connect
I2C_TIMED_OUT_1	2	In pass-through I²C Channel 1, internal I²C-to-I²C slave or master has timed out while receiving packet from remote device.	0b0: Timeout has not occurred 0b1: Timeout has occurred
REM_ACK_ACKED_1	1	In pass-through I²C Channel 1, inverse of the I²C acknowledge bit received from remote side.	0b0: I²C acknowledge bit received as 1 0b1: I²C acknowledge bit received as 0
REM_ACK_RECVED_1	0	In pass-through I²C Channel 1, I²C acknowledge bit for any I²C byte is received from remote side for the previous I²C packet.	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received

UART_PT_0 (0x490)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Read Clears All	Read Clears All	Write, Read	Write, Read	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Uses the custom UART bit rate (selected by the BITLEN_PT_1_L and BITLEN_PT_1_H registers) in pass-through UART Channel 1.	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_2	6	Disables or enable parity bit in pass-through UART Channel 2.	0b0: Parity bit enabled 0b1: Parity bit disabled
UART_RX_OVERFLOW_2	5	Pass-Through UART Rx FIFO Overflow Flag.	0b0: No overflow occurred 0b1: Overflow occurred
UART_TX_OVERFLOW_2	4	Pass-Through UART Tx FIFO Overflow Flag.	0b0: No overflow occurred 0b1: Overflow occurred
BITLEN_MAN_CFG_1	3	Uses the custom UART bit rate (selected by the BITLEN_PT_1_L and BITLEN_PT_1_H registers) in pass-through UART Channel 1.	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_1	2	Disables or enables parity bit in pass-through UART Channel 1.	0b0: Parity bit enabled 0b1: Parity bit disabled
UART_RX_OVERFLOW_1	1	Pass-Through UART Rx FIFO Overflow Flag.	0b0: No overflow occurred 0b1: Overflow occurred
UART_TX_OVERFLOW_1	0	Pass-Through UART Tx FIFO Overflow Flag.	0b0: No overflow occurred 0b1: Overflow occurred

UART_PT_1 (0x491)*

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_1_L[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_L	7:0	Low byte of custom UART bit length for pass-through UART Channel 1. Set this register to the UART bit length divided by 6.666ns (LSb 8 bits). Set BITLEN_MAN_CFG_1 to 1 to use this value.	0xXX: Low byte of custom UART bit length for pass-through UART Channel 1

UART_PT_2 (0x492)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_1_H[5:0]					
Reset	–	–	0b000101					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_H	5:0	High byte of custom UART bit length for pass-through UART Channel 1. Set this register to the UART bit length divided by 6.666ns (LSb 8 bits). Set BITLEN_MAN_CFG_1 to 1 to use this value.	0xXX: High byte of custom UART bit length for pass-through UART Channel 1

UART_PT_4 (0x494)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_2_H[5:0]					
Reset	–	–	0b000101					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_H	5:0	High byte of custom UART bit length for pass-through UART Channel 1. Set this register to the UART bit length divided by 6.666ns (LSb 8 bits). Set BITLEN_MAN_CFG_1 to 2 to use this value.	0xXX: High byte of custom UART bit length for pass-through UART Channel 2

FEC_RX_CTRL (0x600)*

Provides general control for forward error correction (FEC) receive.

BIT	7	6	5	4	3	2	1	0
Field	fec_clr_bit_errs_corrected	fec_clr_uncorrectable_blks	fec_clr_blks_processed	fec_clr_stats	–	fec_collect_stats_en	fec_crc_en	fec_en
Reset	0b0	0b0	0b0	0b0	–	0b1	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
fec_clr_bit_errs_corrected	7	Clears bit errors corrected counter. This bit is self-clearing.	0b0: Counter not cleared 0b1: Counter cleared
fec_clr_uncorrectable_blks	6	Clears uncorrectable blocks counter. This bit is self-clearing.	0b0: Blocks not cleared 0b1: Blocks cleared
fec_clr_blks_processed	5	Clears blocks processed counter. This bit is self-clearing.	0b0: Counter not cleared 0b1: Counter cleared
fec_clr_stats	4	Clears all statistics counters. This bit is self-clearing.	0b0: Counters not cleared 0b1: Counters cleared
fec_collect_stats_en	2	Enables collecting statistics counts of various parameters.	0b0: Disable collecting 0b1: Enable collecting
fec_crc_en	1	Enables CRC checking for FEC receive.	0b0: CRC checking disabled 0b1: CRC checking enabled
fec_en	0	Enables FEC receive operation.	0b0: Disable FEC receive operation 0b1: Enable FEC receive operation

FEC_RX_STATUS (0x602)*

Provides general status for forward error correction (FEC) receive.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	fec_errs_exceeded	fec_active
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
fec_errs_exceeded	1	Indicates that the uncorrected blocks count or the bit error count has exceeded their respective thresholds.	0b0: Uncorrected blocks count or bit error count are within their respective thresholds 0b1: Uncorrected blocks count or bit error count have exceeded their respective thresholds
fec_active	0	Indicates whether or not FEC receive operation is active.	0x0: FEC receive operation is inactive 0x1: FEC receive operation is active

FEC_MEASURE_DURATION_B0 (0x604)*

Defines duration of measurement window for FEC receive.

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x00							
Access Type								

FEC_MEASURE_DURATION_B1 (0x605)*

Defines duration of measurement window for FEC receive.

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x00							
Access Type								

FEC_MEASURE_DURATION_B2 (0x606)*

Defines duration of measurement window for FEC receive.

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x00							
Access Type								

FEC_MEASURE_DURATION_B3 (0x607)*

Defines duration of measurement window for FEC receive.

BIT	7	6	5	4	3	2	1	0
Field	RSVD[7:0]							
Reset	0x00							
Access Type								

FEC_UNCORRECTED_ERRS_THR_B0 (0x608)*

Defines the threshold for uncorrected errors before link failure is declared.

BIT	7	6	5	4	3	2	1	0
Field	fec_uncorrected_errs_thr_b0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_uncorrected_errs_thr_b0	7:0	Threshold for uncorrected errors to determine link failure (bits 7-0).	0xXX: Threshold for uncorrected errors to determine link failure (bits 7-0)

FEC_UNCORRECTED_ERRS_THR_B1 (0x609)*

Defines the threshold for uncorrected errors before link failure is declared.

BIT	7	6	5	4	3	2	1	0
Field	fec_uncorrected_errs_thr_b1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_uncorrected_errs_thr_b1	7:0	Threshold for uncorrected errors to determine link failure (bits 15-8).	0xXX: Threshold for uncorrected errors to determine link failure (bits 15-8)

FEC_UNCORRECTED_ERRS_THR_B2 (0x60A)*

Defines the threshold for uncorrected errors before link failure is declared.

BIT	7	6	5	4	3	2	1	0
Field	fec_uncorrected_errs_thr_b2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_uncorrected_errs_thr_b2	7:0	Threshold for uncorrected errors to determine link failure (bits 23-16).	0xXX: Threshold for uncorrected errors to determine link failure (bits 23-16)

FEC_UNCORRECTED_ERRS_THR_B3 (0x60B)*

Defines the threshold for uncorrected errors before link failure is declared.

BIT	7	6	5	4	3	2	1	0
Field	fec_uncorrected_errs_thr_b3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_uncorrected_errs_thr_b3	7:0	Threshold for uncorrected errors to determine link failure (bits 31-24).	0xXX: Threshold for uncorrected errors to determine link failure (bits 31-24)

FEC_BIT_ERRS_CORRECTED_THR_B0 (0x60C)*

Defines the threshold for corrected bit errors before interrupt is generated.

BIT	7	6	5	4	3	2	1	0
Field	fec_bit_errs_corrected_thr_b0[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_bit_errs_corrected_thr_b0	7:0	Threshold for bit errors for asserting an interrupt (bits 7-0).	0xXX: Threshold for bit errors for asserting an interrupt (bits 7-0)

FEC_BIT_ERRS_CORRECTED_THR_B1 (0x60D)*

Defines the threshold for corrected bit errors before interrupt is generated.

BIT	7	6	5	4	3	2	1	0
Field	fec_bit_errs_corrected_thr_b1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_bit_errs_corrected_thr_b1	7:0	Threshold for bit errors for asserting an interrupt (bits 15-8).	0xXX: Threshold for bit errors for asserting an interrupt (bits 15-8)

FEC_BIT_ERRS_CORRECTED_THR_B2 (0x60E)*

Defines the threshold for corrected bit errors before interrupt is generated.

BIT	7	6	5	4	3	2	1	0
Field	fec_bit_errs_corrected_thr_b2[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_bit_errs_corrected_thr_b2	7:0	Threshold for bit errors for asserting an interrupt (bits 23-16).	0xXX: Threshold for bit errors for asserting an interrupt (bits 23-16)

FEC_BIT_ERRS_CORRECTED_THR_B3 (0x60F)*

Defines the threshold for corrected bit errors before interrupt is generated.

BIT	7	6	5	4	3	2	1	0
Field	fec_bit_errs_corrected_thr_b3[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_bit_errs_corrected_thr_b3	7:0	Threshold for bit errors for asserting an interrupt (bits 31-24).	0xXX: Threshold for bit errors for asserting an interrupt (bits 31-24)

FEC_BLKS_PROCESSED_B0 (0x610)

Count of blocks processed by FEC receive.

BIT	7	6	5	4	3	2	1	0
Field	fec_blks_processed_b0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_blks_processed_b0	7:0	Count of blocks processed (bits 7-0).	0xXX: Count of blocks processed (bits 7-0)

FEC_BLKS_PROCESSED_B1 (0x611)

Count of blocks processed by FEC receive.

BIT	7	6	5	4	3	2	1	0
Field	fec_blks_processed_b1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_blks_processed_b1	7:0	Count of blocks processed (bits 15-8).	0xXX: Count of blocks processed (bits 15-8)

FEC_BLKS_PROCESSED_B2 (0x612)

Count of blocks processed by FEC receive.

BIT	7	6	5	4	3	2	1	0
Field	fec_blks_processed_b2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_blks_processed_b2	7:0	Count of blocks processed (bits 23-16).	0xXX: Count of blocks processed (bits 23-16)

FEC_BLKS_PROCESSED_B3 (0x613)

Count of blocks processed by FEC receive.

BIT	7	6	5	4	3	2	1	0
Field	fec_blks_processed_b3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_blks_processed_b3	7:0	Count of blocks processed (bits 31-24).	0xXX: Count of blocks processed (bits 31-24)

FEC_UNCORRECTABLE_BLKS_B0 (0x614)

Count of uncorrectable blocks.

BIT	7	6	5	4	3	2	1	0
Field	fec_uncorrectable_blks_b0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_uncorrectable_blks_b0	7:0	Count of uncorrectable blocks (bits 7-0).	0xXX: Count of uncorrectable blocks (bits 7-0)

FEC_UNCORRECTABLE_BLKS_B1 (0x615)

Count of uncorrectable blocks.

BIT	7	6	5	4	3	2	1	0
Field	fec_uncorrectable_blks_b1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_uncorrectable_blks_b1	7:0	Count of uncorrectable blocks (bits 15-8).	0xXX: Count of uncorrectable blocks (bits 15-8)

FEC_UNCORRECTABLE_BLKS_B2 (0x616)

Count of uncorrectable blocks.

BIT	7	6	5	4	3	2	1	0
Field	fec_uncorrectable_blks_b2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_uncorrectable_blks_b2	7:0	Count of uncorrectable blocks (bits 23-16).	0xXX: Count of uncorrectable blocks (bits 23-16)

FEC_UNCORRECTABLE_BLKS_B3 (0x617)

Count of uncorrectable blocks.

BIT	7	6	5	4	3	2	1	0
Field	fec_uncorrectable_blks_b3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_uncorrectable_blks_b3	7:0	Count of uncorrectable blocks (bits 31-24).	0xXX: Count of uncorrectable blocks (bits 31-24)

FEC_BIT_ERRS_CORRECTED_B0 (0x618)

Count of bit errors corrected.

BIT	7	6	5	4	3	2	1	0
Field	fec_bit_errs_corrected_b0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_bit_errs_corrected_b0	7:0	Count of bit errors corrected (bits 7-0).	0xXX: Count of bit errors corrected (bits 7-0)

FEC_BIT_ERRS_CORRECTED_B1 (0x619)

Count of bit errors corrected.

BIT	7	6	5	4	3	2	1	0
Field	fec_bit_errs_corrected_b1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_bit_errs_corrected_b1	7:0	Count of bit errors corrected (bits 15-8).	0xXX: Count of bit errors corrected (bits 15-8)

FEC_BIT_ERRS_CORRECTED_B2 (0x61A)

Count of bit errors corrected.

BIT	7	6	5	4	3	2	1	0
Field	fec_bit_errs_corrected_b2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_bit_errs_corrected_b2	7:0	Count of bit errors corrected (bits 23-16).	0xXX: Count of bit errors corrected (bits 23-16)

FEC_BIT_ERRS_CORRECTED_B3 (0x61B)

Count of bit errors corrected.

BIT	7	6	5	4	3	2	1	0
Field	fec_bit_errs_corrected_b3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
fec_bit_errs_corrected_b3	7:0	Count of bit errors corrected (bits 31-24).	0xXX: Count of bit errors corrected (bits 31-24)

PMX_SS_STATE_B0 (0x7F0)

PicoMax subsystem state (read-only).

BIT	7	6	5	4	3	2	1	0
Field	PMX_SS_STATE_B0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PMX_SS_STATE_B0	7:0	Low byte of DP Controller (PMX) subsystem state (bits 7-0).	0bxxxxxxx0: Link training failed 0bxxxxxxx1: Link training succeeded 0b0xxxxxxx: HPD event or HPD IRQ did not occur 0b1xxxxxxx: HPD event or HPD IRQ occurred

PMX_SS_STATE_B1 (0x7F1)

PicoMax subsystem state (read-only).

BIT	7	6	5	4	3	2	1	0
Field	PMX_SS_STATE_B1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PMX_SS_STATE_B1	7:0	High byte of DP Controller (PMX) subsystem state (bits 15-8). Bit 15 (MSb, ERRB_ENABLE) is used to set PMX_ERR_FLAG in the INTR3 register. Reading this register clears the MSb/ ERRB_ENABLE. The content of 0x7F1/0x7F0 is only updated by the controller if 0x7F1[7] is cleared. If 0x7F1[7] = 1, then these registers are locked until the user reads 0x7F1 to check status and clear the MSb/ERRB_ENABLE bit.	0bxxxxxxx0: No loss of video lock detected 0bxxxxxxx1: Loss of video lock detected 0bxxxxxx0x: Watchdog timer not triggered 0bxxxxxx1x: Watchdog timer triggered 0bxxxxx0xx: Video Lock present 0bxxxxx1xx: No Video Lock 0bxxxx0xxx: HPD active (sink connected) 0bxxxx1xxx: HPD inactive (no sink) 0bxxx0xxxx: Link training parameters found 0bxxx1xxxx: Link training parameters not found 0bxx0xxxxx: Training Phase 2 succeeded 0bxx1xxxxx: Training Phase 2 failed (Equalization, Symbol lock, lane alignment) 0bx0xxxxxx: Training Phase 1 succeeded 0bx1xxxxxx: Training Phase1 failed (Clock recovery) 0b0xxxxxxx: Error not reported to INTR subsystem 0b1xxxxxxx: Error reported to INTR subsystem

GPIO_SPEED (0x7FC)

Reserved.

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		GROUP_A_SPEED[1:0]		GROUP_B_SPEED[1:0]		GROUP_C_SPEED[1:0]	
Reset	0b00		0b01		0b00		0b10	
Access Type			Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GROUP_A_SPEED	5:4	Controls GPIO Speed Group A transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0: 2ns, 1ns 1: 4ns, 2ns 2: 8ns, 4ns 3: 16ns, 8ns
GROUP_B_SPEED	3:2	Controls GPIO Speed Group B transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0: 2ns, 1ns 1: 4ns, 2ns 2: 8ns, 4ns 3: 16ns, 8ns
GROUP_C_SPEED	1:0	Controls GPIO Speed Group C transition time. First value is for V_{DDIO} = 1.8V, second value is for V_{DDIO} = 3.3V.	0: 2ns, 1ns 1: 4ns, 2ns 2: 8ns, 4ns 3: 16ns, 8ns

SPI_CC_WR_ (0x1300)

Internal write location for SPI to control channel bytes.

SPI_CC_RD_ (0x1380)

Internal read location for SPI to control channel bytes.

RLMS3 (0x1403, 0x1503)

BIT	7	6	5	4	3	2	1	0
Field	AdaptEn	RSVD	RSVD	RSVD	RSVD	–	RSVD[1:0]	
Reset	0b0	0b0	0b0	0b0	0b1	–	0b10	
Access Type	Write, Read					–		

BITFIELD	BITS	DESCRIPTION	DECODE
AdaptEn	7	Enables Adapt Process.	0b0: Manual adaptation process disabled 0b1: Manual adaptation process enabled

RLMS4 (0x1404, 0x1504)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x4				0b10		0b1	0b1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	A factor (N) used to select the order of number of observations in each eye-monitor window. N is used in the equation: Observations = $6.29 \times 10^{(N + 2)}$	0xX: N factor
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits to allow in a measurement window.	0b00: Allow no errors 0b01: Allow one error 0b10: Allow two errors 0b11: Allow three errors
EOM_PER_MODE	1	Enables eye-opening monitor periodic mode.	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Enables eye-opening monitor.	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

RLMS5 (0x1405, 0x1505)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0b0	0b0010000						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye-opening monitor manual trigger. For use when periodic mode is disabled.	0b0: No action 0b1: EOM manual trigger request
EOM_MIN_THR	6:0	The EOM minimum threshold as defined by the equation: % eye opening = EOM_MIN_THR/64. If the value is zero the EOM is disabled.	0bXXXXXXX: EOM minimum threshold factor

RLMS6 (0x1406, 0x1506)*

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	EOM_RST_THR[6:0]						
Reset	0b1	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_MODE	7	Selects whether eye-opening is measured vertically or horizontally.	0b0: Vertical opening mode 0b1: Horizontal opening mode
EOM_RST_THR	6:0	The EOM refresh threshold as defined by the equation: % eye opening = EOM_MIN_THR/64. If the value is zero the EOM is disabled.	0bXXXXXXX: EOM refresh threshold factor

RLMS7 (0x1407, 0x1507)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-opening monitor measurement done flag.	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Last completed EOM observation.	0bXXXXXXX: EOM measurement result

RLMS18 (0x1418, 0x1518)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	VgaHiGain	RSVD[1:0]	
Reset	–	–	–	–	–	0b0	0b11	
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VgaHiGain	2	55nm FR VGA has an addition gain stage instead of the FFE stage. This control bit (VgaHiGain) configures this gain stage to track the other stages or operate in a high gain mode.	0: High Gain Stage tracks VGA gain control 1: High Gain Stage forced into High Gain mode

RLMS34 (0x1434, 0x1534)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntL	7:0	Eye-monitor period count (RxClk20) LSb.	0xXX: Eye-monitor period count (LSb)

RLMS35 (0x1435, 0x1535)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntH	7:0	Eye-monitor period count (RxClk20) MSb.	0xXX: Eye-monitor period count (MSb)

RLMS37 (0x1437, 0x1537)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–			Read Only	Write Only	Write Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonDone	4	Eye-monitor period complete (read-only, reset on start).	0b0: Eye-monitor data collection not complete 0b1: Eye-monitor data collection complete
EyeMonCntClr	3	Eye-monitor error/valid count clear (one-shot). Readback is EyeMonClrPL from long pulse generation.	0b0: NA 0b1: Clear eye-monitor data collection counters
EyeMonStart	2	Eye-monitor start (one-shot). Readback is EyeMonStClrPL from long pulse generation for both start and clear.	0b0: NA 0b1: Start eye-monitor data collection

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPh	1	Eye-monitor phase.	0b0: Eye-monitor search early phase 0b1: Eye-monitor search late phase
EyeMonDPol	0	Eye-monitor data polarity.	0b0: Eye-monitor search for ones 0b1: Eye-monitor search for zeros

RLMS38 (0x1438, 0x1538)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntL	7:0	Eye-monitor error count (read-only).	0xXX: Eye-monitor error count (LSb)

RLMS39 (0x1439, 0x1539)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntH	7:0	Eye-monitor error count (read-only).	0xXX: Eye-monitor error count (MSb)

RLMS3A (0x143A, 0x153A)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntL	7:0	Eye-monitor valid (hit) count (read-only).	0xXX: Eye-monitor valid count (LSb)

RLMS3B (0x143B, 0x153B)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntH	7:0	Eye-monitor valid (hit) count (read-only).	0xXX: Eye-monitor valid count (MSb)

RLMS3D (0x143D, 0x153D)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPh[6:0]							ErrChPhTogEn
Reset	0b0000000							0b1
Access Type	Read Only							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPh	7:1	Error channel phase (read-only).	0bXXXXXXX: 5.6 degrees per step
ErrChPhTogEn	0	Enables error channel phase toggle.	0: Use primary phase only 1: Auto toggle phase between primary and secondary

RLMS49 (0x1449, 0x1549)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	–	RSVD
Reset	–	0b1	0b1	0b1	0b0	0b1	–	0b1
Access Type	–					Write, Read	–	

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPwrUp	2	Error channel power-down.	0b0: Error channel power disabled 0b1: Error channel power enabled

RLMS58 (0x1458, 0x1558)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh1[6:0]						
Reset	–	0x28						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh1	6:0	Error channel threshold voltage for ones.	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS59 (0x1459, 0x1559)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh0[6:0]						
Reset	–	0x68						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh0	6:0	Error channel threshold voltage for zeros.	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS64 (0x1464, 0x1564)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RSVD	TxSSCMode[1:0]	
Reset	–	–	–	–	–	0b0	0b00	
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx spread spectrum mode.	0b00: Spread spectrum disabled 0b01: Reserved 0b10: Reserved 0b11: Spread spectrum enabled (center spread)

RLMS70 (0x1470, 0x1570)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0b0000001						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx spread spectrum frequency control.	0bXXXXXXX: Tx spread spectrum center frequency control

RLMS71 (0x1471, 0x1571)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0b000001						0b0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx spread spectrum center spread startup control.	0bXXXXXX: Tx spread spectrum center spread startup control

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCEn	0	Enables Tx spread spectrum.	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x1472, 0x1572)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx spread spectrum frequency pre-scaler low byte.	0xXX: Tx spread spectrum frequency pre-scaler low byte

RLMS73 (0x1473, 0x1573)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclH	2:0	Tx spread spectrum frequency pre-scaler high bits.	0bXXX: Tx spread spectrum frequency pre-scaler high bits

RLMS74 (0x1474, 0x1574)*

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx spread spectrum interpolator phase low byte.	0xXX: Tx spread spectrum frequency interpolator phase low byte

RLMS75 (0x1475, 0x1575)*

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx spread spectrum interpolator phase high bits.	0bXXXXXXX: Tx spread spectrum frequency interpolator phase high bits

RLMS76 (0x1476, 0x1576)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx spread spectrum interpolator phase quadrant.	0bXX: Tx spread spectrum interpolator phase quadrant

RLMS95 (0x1495, 0x1595)

BIT	7	6	5	4	3	2	1	0
Field	TxAmplManEn	RSVD	TxAmplMan[5:0]					
Reset	0b0	0b1	0b101001					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplManEn	7	Tx amplitude manual override.	0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude
TxAmplMan	5:0	Tx amplitude.	0bXXXXXX: Binary amplitude 10mV per count

RLMSA4 (0x14A4, 0x15A4)*

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0b10		0b111101					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_PER_MULT	7:6	Adaptive EQ period multiplier.	0b00: 1ms 0b01: 4ms 0b10: 16ms 0b11: 64ms
AEQ_PER	5:0	Adaptive EQ period. Periodic adaptation is disabled when value is 0. Adaptive EQ period is set to (AEQ_PER value times AEQ_PER_MULT).	0b000000: Periodic adaptation disabled 0b000001-0b111111: Adaptive EQ period is set to (AEQ_PER value times AEQ_PER_MULT)

RLMSAC (0x14AC, 0x15AC)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
Reset	0b1	0b1001101						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTAFR3G	7	Error channel phase secondary timing adjust.	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecFR3G	6:0	Error channel phase secondary (odd).	0bXXXXXXX: 7'h4D

RLMSAD (0x14AD, 0x15AD)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
Reset	0b0	0b0001101						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTAFR3G	7	Error channel phase primary timing adjust.	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriFR3G	6:0	Error channel phase primary (even).	0bXXXXXXX: 7'h0D

RLMSC4 (0x14C4, 0x15C4)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD[2:0]			–	RevFast	–	–
Reset	0b0	0b100			–	0b0	–	–
Access Type					–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RevFast	2	GMSL1 reverse channel fast mode.	0x0: Reverse channel fast mode disabled 0x1: Reverse channel fast mode enabled

HDCP_15 (0x1695)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AUTH_START	ENC_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUTH_START	1	Indicates whether or not HDCP authentication has started.	0b0: HDCP encryption not started 0b1: HDCP encryption started
ENC_EN	0	Enables HDCP decryption.	0b0: HDCP encryption disabled 0b1: HDCP encryption enabled

HDCP_16 (0x1696)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	–	–	–	HDCP_NEW_DEV_CONN	HDCP_READY
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type		–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_NEW_DEV_CONN	1	Indicates whether or not a HDCP new device is connected.	0b0: HDCP new device not connected 0b1: HDCP new device connected
HDCP_READY	0	Indicates whether or not the HDCP repeater is ready.	0b0: HDCP repeater not ready 0b1: HDCP repeater ready

HDCP_17 (0x1697)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_BCAPS[6:0]							HDCP_REPEATER
Reset	0b0000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_BCAPS	7:1	HDCP BCAPS register.	0b0000000: Device is not a repeater 0b0000001: Device is a repeater 0b0000010 - 0b1111111: Reserved
HDCP_REPEATER	0	Enables HDCP repeater.	0b0: HDCP repeater not enabled 0b1: HDCP repeater enabled

HDCP_19 (0x1699)*

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DIS_AUDIO_ENC
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_AUDIO_ENC	0	Disable audio encryption.	0b0: Audio encryption disabled 0b1: Audio encryption enabled

HDCP_34 (0x16B4)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_MAX_DEV_EXCEEDED	HDCP_DEV_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_MAX_DEV_EXCEEDED	7	Maximum device count exceeded in repeater mode.	0b0: Maximum number of devices not exceeded (14 or less) 0b1: Maximum number of devices exceeded (more than 14)
HDCP_DEV_CNT	6:0	Repeater device count.	0bXXXXXXX: Number of devices attached

HDCP_35 (0x16B5)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				HDCP_MAX_CASCADE_EXCEEDED	HDCP_DEPTH[2:0]		
Reset	0x0				0b0	0b000		
Access Type					Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_MAX_CASCADE_EXCEEDED	3	Indicates whether or not HDCP repeater mode has exceeded maximum depth.	0b0: Maximum number of cascaded devices not exceeded (seven or less) 0b1: Maximum number of cascaded devices exceeded (more than seven)
HDCP_DEPTH	2:0	HDCP repeater depth.	0bXXX: Depth of cascaded devices

HDCP_36 (0x16B6)

BIT	7	6	5	4	3	2	1	0
Field	HDCP_GPMEM[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_GPMEM	7:0	General purpose memory byte. This has no effect on operation of the device, it can be used for handshaking between more than one microcontroller in the system.	0xXX: General purpose memory byte

HDCP_37 (0x16B7)*

BIT	7	6	5	4	3	2	1	0
Field	HDCP_PD	AH_MODE	–	–	–	–	–	–
Reset	0b1	0b1	–	–	–	–	–	–
Access Type	Write, Read	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_PD	7	Power-down HDCP blocks.	0b0: HDCP blocks powered up 0b1: Power-down HDCP blocks
AH_MODE	6	Enables auto HDCP operation.	0b0: Manual HDCP or non-HDCP mode 0b1: Auto-HDCP mode

HDCP_38 (0x16B8)*

BIT	7	6	5	4	3	2	1	0
Field	HDCP_INT	–	–	–	–	–	MASK_AUTH_ST	MASK_ENC_EN
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Read Clears All	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HDCP_INT	7	SPIHDCP interrupt is asserted (unless masked) when: • HDCP Encryption enable/disable • HDCP Authentication started Read to clear the interrupt.	0b0: HDCP interrupt not asserted 0b1: HDCP interrupt asserted
MASK_AUTH_ST	1	Mask authentication start interrupt.	0b0: Authentication start interrupt not masked 0b1: Authentication start interrupt masked
MASK_ENC_EN	0	Mask encryption enable/disable interrupt.	0b0: HDCP encryption not masked, HDCP interrupt available 0b1: Mask HDCP encryption, disable HDCP interrupt

HDCP_39 (0x16B9)

BIT	7	6	5	4	3	2	1	0
Field	LINK_LOCK	AH_VID_LOCK	AH_RESERVED[5:0]					
Reset	0b0	0b0	0b110101					
Access Type	Read Only	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_LOCK	7	GMSL2 link lock (control channel is operational).	0b0: GMSL2 link is not locked 0b1: GMSL2 link is locked. Control channel is operational.
AH_VID_LOCK	6	Indicates whether or not video receiver has started outputting video.	0b0: Video receiver not locked 0b1: Video receiver has started outputting video

BITFIELD	BITS	DESCRIPTION	DECODE
AH_RESERVED	5:0	Reserved.	0bXXXXXX: Reserved

SYS_CNTL_B0 (0x1700)

BIT	7	6	5	4	3	2	1	0
Field	cmd_reset	clk_en	hdcp_repeat_mode	sys_int_en[4:0]				
Reset	0b0	0b1	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_reset	7	Holds HDCP2 operation in reset.	0b0: Do not hold HDCP in reset 0b1: Hold HDCP in reset
clk_en	6	Enables clock operation.	0b0: Clock disabled (gates) 0b1: Clock enabled
hdcp_repeat_mode	5	Selects the mode of reciever operation.	0b0: Sink device 0b1: Upstream port of a repeater
sys_int_en	4:0	Enables interrupt for ERRB interrupt generation. This value is a bitfield with each bit enabling an interrupting event.	0b00000: Authentication failed 0b00001: Topology available 0b00010: Topology changed 0b00011: Cipher sync failure 0b00100: Authentication started

SYS_CNTL_B2 (0x1702)

BIT	7	6	5	4	3	2	1	0
Field	cypher_gen_fail	–	–	sys_int_st[4:0]				
Reset	0b0	–	–	0b00000				
Access Type	Read Only	–	–	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
cypher_gen_fail	7	Error in cypher generation flag.	0x0: No cypher generation error occurred 0x1: Cypher generation error occurred
sys_int_st	4:0	Interrupt status for ERRB interrupt generation. This value is a bitfield with each bit representing an interrupting event. These events are cleared when read.	0b00000: Authentication failed 0b00001: Topology available 0b00010: Topology changed 0b00011: Cipher sync failure 0b00100: Authentication started

SYS_CNTL_B3 (0x1703)

BIT	7	6	5	4	3	2	1	0
Field	decrypt_status	video_mask_status	RSVD[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
decrypt_status	7	Audio/video decryption status.	0x0: Audio/video is not being decrypted 0x1: Audio/video is being decrypted
video_mask_status	6	Audio/video masked (blanked) status.	0x0: Audio/video is not being masked 0x1: Audio/video is being masked

DPLL_3 (0x1B03)*

BIT	7	6	5	4	3	2	1	0
Field	config_sel_clock_out_use_external	config_disable_div_out_exp	config_use_internal_pll_mode_values	config_use_internal_divider_values	config_force_enable_ss	config_spread_bit_ratio[2:0]		
Reset	0b1	0b0	0b0	0b0	0b0	0b010		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
config_sel_clock_out_use_external	7	Output clock selection.	0b0: Use internal registers to select output clock 0b1: Use i_sel_clock_out to select output clock
config_disable_div_out_exp	6	Forces div_out_exp to 7, which disables the divider.	0b0: Do not force disablement of the divider 0b1: Force disablement of the divider
config_use_internal_pll_mode_values	5	Bypasses external pll_mode controls and use config_reg values.	0b0: Disable bypass and use external pll_mode controls 0b1: Enable bypass and use config_reg values
config_use_internal_divider_values	4	Forces all divider values to come from internal controls.	0: Do not force divider values to come from internal controls 1: Force divider values to come from internal controls
config_force_enable_ss	3	Enables the output of the triangle wave generator (overrides en_ss to force triangle_wave on).	0b0: Disable output of triangle wave generator 0b1: Enable output of triangle wave generator
config_spread_bit_ratio	2:0	Controls the magnitude of the triangle wave input to the divider dsm as a percentage of the nominal divider value. If config registers are reset, the spread_bit_ratio value does not propagate to the triangle wave without rewriting to it. Likewise, if the triangle wave module is reset, the user needs to rewrite to spread_bit_ratio to set it back to desired value.	000: Off 001: 0.25% 010: 0.5% 011: 1% 100: 2% 101: 4% 110: 4% 111: 4%

LUT_A_ (0x2000)

Start address for color lookup table COLOR_A LUT_X for Video Pipeline X.

LUT_B_ (0x2100)

Start address for color lookup table COLOR_B LUT_X for Video Pipeline X.

LUT_C_ (0x2200)

Start address for color lookup table COLOR_C LUT_X for Video Pipeline X.

LUT_A_ (0x2400)

Start address for color lookup table COLOR_A LUT_Y for Video Pipeline Y.

LUT_B_ (0x2500)

Start address for color lookup table COLOR_B LUT_Y for Video Pipeline Y.

LUT_C_ (0x2600)

Start address for color lookup table COLOR_C LUT_Y for Video Pipeline Y.

LUT_A_ (0x2800)

Start address for color lookup table COLOR_A LUT_Z for Video Pipeline Z.

LUT_B_ (0x2900)

Start address for color lookup table COLOR_B LUT_Z for Video Pipeline Z.

LUT_C_ (0x2A00)

Start address for color lookup table COLOR_C LUT_Z for Video Pipeline Z.

LUT_A_ (0x2C00)

Start address for color lookup table COLOR_A LUT_U for Video Pipeline U.

LUT_B_ (0x2D00)

Start address for color lookup table COLOR_B LUT_U for Video Pipeline U.

LUT_C_ (0x2E00)

Start address for color lookup table COLOR_C LUT_U for Video Pipeline U.

DSCD_CTRL_B0 (0x4500)*

Provides general control for DSC decoder operation.

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RSVD	RSVD	–	dscd_rst_sc	dscd_rst	dscd_en
Reset	0b0	–	0b0	0b0	–	0b0	0b0	0b0
Access Type		–			–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
dscd_rst_sc	2	Resets DSC decoder. This bit is self-clearing, providing a simple one-shot reset.	0b0: Do not reset DSC decoder 0b1: Reset DSC decoder
dscd_rst	1	Resets DSC decoder. This bit is not self-clearing and holds the reset condition as long as it is active.	0b0: Do not reset DSC decoder 0b1: Reset DSC decoder
dscd_en	0	Enables DSC decoder operation.	0b0: Do not enable DSC decoder operation 0b1: Enable DSC decoder operation

DSCD_CTRL_B1 (0x4501)

Provides general control for DSC decoder operation.

BIT	7	6	5	4	3	2	1	0
Field	prof_wr	–	–	–	prof_sel[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
prof_wr	7	Triggers the selected profile (bits 3-0) parameters to be loaded into registers.	0x0: Trigger not set 0x1: Trigger set
prof_sel	3:0	Selects a profile for initializing DSC decoder registers that differ based on resolution. See prof_wr (bit 7) for triggering the selected profile to load the registers.	0b0000: 4800x900 - 60Hz 0b0001: 2400x900 - 60Hz 0b0010: 2400x2376 - 30Hz 0b0011: 1920x1728 - 60Hz 0b0100: 1856x1720 - 60Hz 0b0101: 1624x1728 - 60Hz 0b0110: 3840x2160 - 60Hz 0b0111: 1920x1080 - 60Hz 0b1000: 5760x1080 - 60Hz 0b1001: 4096x2160 - 60Hz 0b1010: 2560x1600 - 60Hz 0b1011: 1280x720 - 60Hz 0b1100: 3304x2224 - 30Hz 0b1101: 1888x1728 - 60Hz 0b1110: 3088x1728 - 60Hz 0b1111: 1920x16 --

DSCD_RATE_CTRL_B0 (0x4504)*

Provides control of the internal rate of pixels output from the DSC decoder for internal buffer management.

BIT	7	6	5	4	3	2	1	0
Field	pix_out_rate_act[7:0]							
Reset	0x3F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
pix_out_rate_act	7:0	Pixel output rate active (burst) count. This limits the internal instantaneous pixel burst length and is used along with the pix_out_rate_inact parameter to set the average internal pixel rate for buffer management. For proper overall buffer operation, the active count should be a minimum of 4 and a maximum of 64. The register setting is zero relative (active - 1). Setting this register to the maximum value, 255, disables rate control resulting in unlimited burst length (effectively, an inactive count of zero).	0xXX: Pixel output rate active (burst) count

DSCD_RATE_CTRL_B1 (0x4505)*

Provides control of the internal rate of pixels output from the DSC decoder for internal buffer management.

BIT	7	6	5	4	3	2	1	0
Field	pix_out_rate_inact[7:0]							
Reset	0x4F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
pix_out_rate_inact	7:0	Pixel output rate inactive count. This, along with the pix_out_rate_act parameter, controls the average internal pixel rate for buffer management. The average rate should be set to be 5% faster than the pixel clock (pclk) rate of the original video source. The inactive count is calculated by: inactive = active x (600 - (pclk x 1.05))/(pclk x 1.05), rounded down to integer The register setting is zero relative (inactivex - 1). For inactive = 0, set pix_out_rate_act to 255.	0xXX: Pixel output rate inactive count

DSCD_RATE_CTRL_B3 (0x4507)

Provides control of the internal rate of pixels output from the DSC decoder for internal buffer management.

BIT	7	6	5	4	3	2	1	0
Field	pix_rate_ext_en	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
pix_rate_ext_en	7		0x0: Trigger not set 0x1: Trigger set

DSCD_INT_ST_B0 (0x4508)

Interrupt status for DSC decoder operations. Once set, a particular bit remains active (sticky) until it is written to '1' (i.e., write 1 to clear). Bits representing edge-triggered events are set when the event edge occurs, remain set until cleared and remain cleared until the next edge event (not live status).

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	pb_ovfl_ist	vb_ovfl_ist
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
pb_ovfl_ist	1	Pixel buffer overflow indicates an overflow condition occurred on the output pixel buffer. This bit is edge-triggered on the rising edge of an overflow event.	0x0: No overflow condition occurred 0x1: Overflow condition occurred
vb_ovfl_ist	0	Video buffer overflow indicates an overflow condition occurred on the input video buffer. This bit is edge-triggered on the rising edge of an overflow event.	0x0: No overflow condition occurred 0x1: Overflow condition occurred

DSCD_INT_ST_B1 (0x4509)

Interrupt status for DSC decoder operations. Once set, a particular bit remains active (sticky) until it is written to '1' (i.e., write 1 to clear). Bits representing edge-triggered events are set when the event edge occurs, remain set until cleared and remain cleared until the next edge event (not live status).

BIT	7	6	5	4	3	2	1	0
Field	rcb1_ovfl_ist	tc_size1_err_ist	ib1_undfl_ist	ib1_ovfl_ist	rcb0_ovfl_ist	tc_size0_err_ist	ib0_undfl_ist	ib0_ovfl_ist
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
rcb1_ovfl_ist	7	Decoder core 1 rate control model buffer fullness overflow. This bit is edge-triggered on the rising edge of an overflow event.	0x0: No overflow condition occurred 0x1: Overflow condition occurred
tc_size1_err_ist	6	Decoder core 1 transport chunk size error. This bit is edge-triggered on the rising edge of a transport chunk size error detection.	0x0: No chunk size error occurred 0x1: Chunk size error occurred
ib1_undfl_ist	5	Decoder core input buffer 1 underflow. This bit is edge-triggered on the rising edge of an underflow event.	0x0: No underflow condition occurred 0x1: Underflow condition occurred
ib1_ovfl_ist	4	Decoder core input buffer 1 overflow. This bit is edge-triggered on the rising edge of an overflow event.	0x0: No overflow condition occurred 0x1: Overflow condition occurred
rcb0_ovfl_ist	3	Decoder core 0 rate control model buffer fullness overflow. This bit is edge-triggered on the rising edge of an overflow event.	0x0: No overflow condition occurred 0x1: Overflow condition occurred

BITFIELD	BITS	DESCRIPTION	DECODE
tc_size0_err_ist	2	Decoder core 0 transport chunk size error. This bit is edge-triggered on the rising edge of a transport chunk size error detection.	0x0: No chunk size error occurred 0x1: Chunk size error occurred
ib0_undfl_ist	1	Decoder core input buffer 0 underflow. This bit is edge-triggered on the rising edge of an underflow event.	0x0: No underflow condition occurred 0x1: Underflow condition occurred
ib0_ovfl_ist	0	Decoder core input buffer 0 overflow. This bit is edge-triggered on the rising edge of an overflow event.	0x0: No overflow condition occurred 0x1: Overflow condition occurred

DSCD_INT_EN_B0 (0x450C)*

Interrupt enables for each interrupt status bit defined the DSCD Interrupt Status register. Each bit is ANDed with the corresponding bit of the DSCD Interrupt Status register, the results of which are ORed together to create the DSCD interrupt signal.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	pb_ovfl_ien	vb_ovfl_ien
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
pb_ovfl_ien	1	Pixel buffer overflow interrupt enables.	0x0: Disable interrupt 0x1: Enable interrupt
vb_ovfl_ien	0	Video buffer overflow interrupt enables.	0x0: Disable interrupt 0x1: Enable interrupt

DSCD_INT_EN_B1 (0x450D)*

Interrupt enables for each interrupt status bit defined the DSCD Interrupt Status register. Each bit is ANDed with the corresponding bit of the DSCD Interrupt Status register, the results of which are ORed together to create the DSCD interrupt signal.

BIT	7	6	5	4	3	2	1	0
Field	rcb1_ovfl_ien	tc_size1_err_ien	ib1_undfl_ien	ib1_ovfl_ien	rcb0_ovfl_ien	tc_size0_err_ien	ib0_undfl_ien	ib0_ovfl_ien
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
rcb1_ovfl_ien	7	Decoder core 1 rate control model buffer fullness overflow interrupt enable.	0x0: Disable interrupt 0x1: Enable interrupt
tc_size1_err_ien	6	Decoder core 1 transport chunk size error interrupt enable.	0x0: Disable interrupt 0x1: Enable interrupt
ib1_undfl_ien	5	Decoder core input buffer 1 underflow interrupt enable.	0x0: Disable interrupt 0x1: Enable interrupt
ib1_ovfl_ien	4	Decoder core input buffer 1 overflow interrupt enable.	0x0: Disable interrupt 0x1: Enable interrupt
rcb0_ovfl_ien	3	Decoder core 0 rate control model buffer fullness overflow interrupt enable.	0x0: Disable interrupt 0x1: Enable interrupt

BITFIELD	BITS	DESCRIPTION	DECODE
tc_size0_err_ien	2	Decoder core 0 transport chunk size error interrupt enable.	0x0: Disable interrupt 0x1: Enable interrupt
ib0_undfl_ien	1	Decoder core input buffer 0 underflow interrupt enable.	0x0: Disable interrupt 0x1: Enable interrupt
ib0_ovfl_ien	0	Decoder core input buffer 0 overflow interrupt enable.	0x0: Disable interrupt 0x1: Enable interrupt

DEC0_DF_CTRL_B0 (0x4510)

DSC hard slice decoder 0 data flow control.

BIT	7	6	5	4	3	2	1	0
Field	hsync_delay_l[3:0]				initial_tc[3:0]			
Reset	0x6				0x1			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
hsync_delay_l	7:4	HSYNC delay low bits (bits 3-0). The HSYNC delay value is the number of decoder core clocks from the leading edge of HSYNC until the decoded output line begins (after the initial_tc condition has been met).
initial_tc	3:0	This Initial Transport Chunk value is the amount of encoded data of a frame to accumulate in the decoder core before starting the first output line of decoded data. Effectively, this value amounts to numbers of horizontal lines of encoded data.

DEC0_DF_CTRL_B1 (0x4511)

DSC hard slice decoder 0 data flow control.

BIT	7	6	5	4	3	2	1	0
Field	hsync_delay_m[7:0]							
Reset	0x27							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
hsync_delay_m	7:0	HSYNC delay middle bits (bits 11-4). The HSYNC delay value is the number of decoder core clocks from the leading edge of HSYNC until the decoded output line begins (after the initial_tc condition has been met).

DEC_PICTURE_SIZE_B0 (0x4524)*

Sets the picture size (resolution) for the DSC decoder.

BIT	7	6	5	4	3	2	1	0
Field	pic_width_b0[7:0]							
Reset	0xC0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pic_width_b0	7:0	Picture width (horizontal active) low byte (bits 7-0).

DEC_PICTURE_SIZE_B1 (0x4525)*

Sets the picture size (resolution) for the DSC decoder.

BIT	7	6	5	4	3	2	1	0
Field	pic_width_b1[7:0]							
Reset	0x12							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pic_width_b1	7:0	Picture width (horizontal active) high byte (bits 15-8).

DEC_PICTURE_SIZE_B2 (0x4526)*

Sets the picture size (resolution) for the DSC decoder.

BIT	7	6	5	4	3	2	1	0
Field	pic_height_b0[7:0]							
Reset	0x84							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pic_height_b0	7:0	Picture height (vertical active) low byte (bits 7-0).

DEC_PICTURE_SIZE_B3 (0x4527)*

Sets the picture size (resolution) for the DSC decoder.

BIT	7	6	5	4	3	2	1	0
Field	pic_height_b1[7:0]							
Reset	0x03							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pic_height_b1	7:0	Picture height (vertical active) high byte (bits 15-8).

DEC_SLICE_SIZE_B0 (0x4528)*

Sets the slice size for the DSC decoder.

BIT	7	6	5	4	3	2	1	0
Field	slice_width_b0[7:0]							
Reset	0x60							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_width_b0	7:0	Slice width low byte (bits 7-0).

DEC_SLICE_SIZE_B1 (0x4529)*

Sets the slice size for the DSC decoder.

BIT	7	6	5	4	3	2	1	0
Field	slice_width_b1[7:0]							
Reset	0x09							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_width_b1	7:0	Slice width high byte (bits 15-8).

DEC_SLICE_SIZE_B2 (0x452A)*

Sets the slice size for the DSC decoder.

BIT	7	6	5	4	3	2	1	0
Field	slice_height_b0[7:0]							
Reset	0x64							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_height_b0	7:0	Slice height low byte (bits 7-0).

DEC_SLICE_SIZE_B3 (0x452B)*

Sets the slice size for the DSC decoder.

BIT	7	6	5	4	3	2	1	0
Field	slice_height_b1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_height_b1	7:0	Slice height high byte (bits 15-8).

DEC_MISC_SIZE_B0 (0x452C)

DSC decoder group and transport chunk size.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	slice_last_grp_sz[1:0]	
Reset	–	–	–	–	–	–	0b10	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
slice_last_grp_sz	1:0	Size of last pixel group of slice line (zero-relative). 00 - 1 pixel 01 - 2 pixels 10 - 3 pixels 11 - Invalid

DEC_MISC_SIZE_B2 (0x452E)

DSC decoder group and transport chunk size.

BIT	7	6	5	4	3	2	1	0
Field	chunk_size_b0[7:0]							
Reset	0x60							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
chunk_size_b0	7:0	Chunk size low byte (bits 7-0).

DEC_MISC_SIZE_B3 (0x452F)

DSC decoder group and transport chunk size.

BIT	7	6	5	4	3	2	1	0
Field	chunk_size_b1[7:0]							
Reset	0x09							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
chunk_size_b1	7:0	Chunk size high byte (bits 15-8).

DEC_HRD_DELAYS_B2 (0x4532)

DSC decoder hypothetical reference delays.

BIT	7	6	5	4	3	2	1	0
Field	initial_dec_delay_b0[7:0]							
Reset	0xDC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
initial_dec_delay_b0	7:0	Initial decoder delay low byte (bits 7-0).

DEC_HRD_DELAYS_B3 (0x4533)

DSC decoder hypothetical reference delays.

BIT	7	6	5	4	3	2	1	0
Field	initial_dec_delay_b1[7:0]							
Reset	0x06							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
initial_dec_delay_b1	7:0	Initial decoder delay high byte (bits 15-8).

DEC_RC_SCALE_INC_DEC_B0 (0x4538)

Rate control scale increment/decrement settings.

BIT	7	6	5	4	3	2	1	0
Field	scale_inc_interval_b0[7:0]							
Reset	0x64							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
scale_inc_interval_b0	7:0	Rate control scale increment interval low byte (bits 7-0).

DEC_RC_SCALE_INC_DEC_B1 (0x4539)

Rate control scale increment/decrement settings.

BIT	7	6	5	4	3	2	1	0
Field	scale_inc_interval_b1[7:0]							
Reset	0x0D							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
scale_inc_interval_b1	7:0	Rate control scale increment interval high byte (bits 15-8).

DEC_RC_SCALE_INC_DEC_B2 (0x453A)

Rate control scale increment/decrement settings.

BIT	7	6	5	4	3	2	1	0
Field	scale_dec_interval_b0[7:0]							
Reset	0x21							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
scale_dec_interval_b0	7:0	Rate control scale decrement interval low byte (bits 7-0).

DEC_RC_SCALE_INC_DEC_B3 (0x453B)

Rate control scale increment/decrement settings.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	scale_dec_interval_b1[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
scale_dec_interval_b1	3:0	Rate control scale decrement interval high byte (bits 11-8).

DEC_RC_OFFSETS_2_B0 (0x4540)

Rate control non-first line/slice-extra offset settings.

BIT	7	6	5	4	3	2	1	0
Field	nfl_bpg_off_b0[7:0]							
Reset	0x37							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
nfl_bpg_off_b0	7:0	Non-first line bits-per-group budget offset low byte (bits 7-0).

DEC_RC_OFFSETS_2_B1 (0x4541)

Rate control non-first line/slice-extra offset settings.

BIT	7	6	5	4	3	2	1	0
Field	nfl_bpg_off_b1[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
nfl_bpg_off_b1	7:0	Non-first line bits-per-group budget offset high byte (bits 15-8).

DEC_RC_OFFSETS_2_B2 (0x4542)

Rate control non-first line/slice-extra offset settings.

BIT	7	6	5	4	3	2	1	0
Field	slice_bpg_off_b0[7:0]							
Reset	0x3B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_bpg_off_b0	7:0	Extra bits-per-group budget offset low byte (bits 7-0).

DEC_RC_OFFSETS_2_B3 (0x4543)

Rate control non-first line/slice-extra offset settings.

BIT	7	6	5	4	3	2	1	0
Field	slice_bpg_off_b1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
slice_bpg_off_b1	7:0	Slice extra bits-per-group budget offset high byte (bits 15-8).

DEC_RC_OFFSETS_3_B2 (0x4546)

Rate control initial/final offset settings.

BIT	7	6	5	4	3	2	1	0
Field	final_off_b0[7:0]							
Reset	0xF0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
final_off_b0	7:0	Final offset low byte (bits 7-0).

DEC_RC_OFFSETS_3_B3 (0x4547)

Rate control initial/final offset settings.

BIT	7	6	5	4	3	2	1	0
Field	final_off_b1[7:0]							
Reset	0x10							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
final_off_b1	7:0	Final offset high byte (bits 15-8).

BAD_FRAMING_STATE (0x6188)

Status bits to indicate if a bad condition has been detected at the user VSYNC time for each of the 4 video sources.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	RSVD	RSVD	SRC0_LNK_FRM_STATE_BAD
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–				Read Only

BITFIELD	BITS	DESCRIPTION
SRC0_LNK_FRM_STATE_BAD	0	A value of '1' in this register indicates that at user VSYNC time, a bad state has been detected on source 0 which may leave display video pixel shifted. This is not a sticky flag and updates at every user VSYNC time.

SOFT_RESET (0x6190)

Performs a soft reset of specific core management functions. This reset only applies to the control portions of the core. The state of the programmable register set is not affected by the soft reset.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VIDEO_SOFT_RESET	LINK_SOFT_RESET
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
VIDEO_SOFT_RESET	1	Writing a 1 performs a soft reset of the video capture section.
LINK_SOFT_RESET	0	Writing a 1 performs a soft reset of the link management section.

AUX_STATE (0x6230)

Holds status bits which report the internal state of the AUX channel management logic. Some of these signals are used to generate interrupts and can be used as polled status for systems that do not implement interrupts.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	RSVD	RSVD	HPD_STATE
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–				Write, Read

BITFIELD	BITS	DESCRIPTION
HPD_STATE	0	Contains the raw state of the HPD pin on the DisplayPort connector.

VTRG_CTRL_B0 (0x7000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	vid_en_mode[1:0]		vtrg_rst	vtrg_en
Reset	–	–	–	–	0b00		0b0	0b0
Access Type	–	–	–	–	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
vid_en_mode	3:2	Video enable mode.	0: Video disabled 1: Video enabled
vtrg_rst	1	Video Timing Regenerator (VTRG) reset.	
vtrg_en	0	Video Timing Regenerator (VTRG) enable.	0: VTRG disabled 1: VTRG enabled (recommended)

VTRG_INT_ST_B0 (0x7008)

BIT	7	6	5	4	3	2	1	0
Field	rate_adj_max_ist	rate_adj_ist	pb_ovfl_ist	pb_undfl_ist	vs_inact_ist	vs_act_ist	de_inact_ist	de_act_ist
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
rate_adj_max_ist	7	Rate adjust event indicator.	0: No max rate adjust detected 1: Control loop integral path has reached rate adjust limit
rate_adj_ist	6	Rate adjust event indicator.	0: No rate adjust event has occurred 1: Rate adjust event has occurred
pb_ovfl_ist	5	Pixel buffer overflow indicator.	0: No overflow event (normal operation) 1: Overflow event has occurred (problem)
pb_undfl_ist	4	Pixel buffer underflow indicator.	0: No underflow event (normal operation) 1: Underflow event has occurred (problem)
vs_inact_ist	3	Vertical sync inactive indicates the end of vertical sync. This bit is edge-triggered on the trailing edge of vertical sync.	0: VS trailing edge event not detected 1: VS trailing edge event detected

BITFIELD	BITS	DESCRIPTION	DECODE
vs_act_ist	2	Vertical sync active indicates the start of vertical sync. This bit is edge-triggered on the leading edge of vertical sync.	0: VS leading edge event not detected 1: VS leading edge event detected
de_inact_ist	1	Display enable inactive indicates the end of an active video line. This bit is edge-triggered on the falling edge of display enable.	0: DE trailing edge event not detected 1: DE trailing edge event detected
de_act_ist	0	Display enable active indicates the start of an active video line. This bit is edge-triggered on the leading edge of display enable.	0: DE leading edge event not detected 1: DE leading edge event detected

PIX_RATE_CTRL_B0 (0x7010)

BIT	7	6	5	4	3	2	1	0
Field	pix_rate_ctrl_en	–	–	pix_rate_clk_act[4:0]				
Reset	0b0	–	–	0b00000				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
pix_rate_ctrl_en	7	Pixel rate control enable.
pix_rate_clk_act	4:0	Pixel rate clocks per active cycle.

PIX_RATE_CTRL_B1 (0x7011)

BIT	7	6	5	4	3	2	1	0
Field	pix_rate_inact_red[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pix_rate_inact_red	7:0	Pixel rate inactive-to-inactive redistribution count.

PIX_RATE_CTRL_B2 (0x7012)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	pix_rate_div[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
pix_rate_div	1:0	PCLK divide rate.

PIX_RATE_CTRL_B3 (0x7013)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	dptx_mcnt_ovride	vtg_msa_auto_set	pix_rate_clkp_adj	pix_rate_clkp_en
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
dptx_mcnt_ovride	3	DPTX Dynamic MVID Tracking.	0: Normal DPTX control 1: Override DPTX asynchronous clocking mode register programmed MVID control
vtg_msa_auto_set	2	VTG MSA auto-load from DPTX.	0: VTG parameters must be programmed directly 1: Automatically program VTG parameters from DPTX MSA video parameters
pix_rate_clkp_adj	1	VTRG Tracking Enable.	0: Pixel rate clock pulse does not adjust to pixel rate 1: Pixel rate clock pulse adjusts to pixel rate
pix_rate_clkp_en	0	VTRG Mode.	0: Pixel rate dynamic clock pulse mode disabled 1: Pixel rate dynamic clock pulse mode enabled

PIX_RATE_PER_B0 (0x7014)

BIT	7	6	5	4	3	2	1	0
Field	pix_rate_act_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pix_rate_act_lo	7:0	Pixel rate clock frequency (low byte).

PIX_RATE_PER_B1 (0x7015)

BIT	7	6	5	4	3	2	1	0
Field	pix_rate_act_hi[7:0]							
Reset	0b00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pix_rate_act_hi	7:0	Pixel rate clock frequency (high byte).

PIX_RATE_PER_B2 (0x7016)

BIT	7	6	5	4	3	2	1	0
Field	pix_rate_inact_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
pix_rate_inact_lo	7:0	Pixel rate clock frequency (low byte).

PIX_RATE_PER_B3 (0x7017)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	pix_rate_inact_hi[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
pix_rate_inact_hi	2:0	Pixel rate clock frequency (high byte).

PB_DELTA_ACC_B0 (0x7020)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	pb_del_acc_per[3:0]			
Reset	–	–	–	–	0x7			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
pb_del_acc_per	3:0	Sets the period (number of horizontal lines) for accumulating the pixel buffer fill delta information used to make rate adjustments. This value is the zero-relative number of lines. This is the control loop bandwidth.

PB_ADJ_STEP_B0 (0x702C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	pb_rate_adj_step_0[5:0]					
Reset	–	–	0b000001					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
pb_rate_adj_step_0	5:0	Sets the rate adjust step size for range 0. Each incremental step size changes the horizontal line length by 1 clock (1.6667ns).

PB_ADJ_STEP_B1 (0x702D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	pb_rate_adj_step_1[5:0]					
Reset	–	–	0b000010					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
pb_rate_adj_step_1	5:0	Sets the rate adjust step size for range 1. Each incremental step size changes the horizontal line length by 1 video pipeline clock (1.6667ns). This is the control loop gain for range 1.

PB_ADJ_STEP_B2 (0x702E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	pb_rate_adj_step_2[5:0]					
Reset	–	–	0b000100					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
pb_rate_adj_step_2	5:0	Sets the rate adjust step size for range 2. Each incremental step size changes the horizontal line length by 1 video pipeline clock (1.6667ns). This is the control loop gain for range 2.

PB_ADJ_STEP_B3 (0x702F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	pb_rate_adj_step_3[5:0]					
Reset	–	–	0b001000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
pb_rate_adj_step_3	5:0	Sets the rate adjust step size for range 3. Each incremental step size changes the horizontal line length by 1 video pipeline clock (1.6667ns). This is the control loop gain for range 3.

PB_ADJ_CTRL_B0 (0x7030)

BIT	7	6	5	4	3	2	1	0
Field	–	pb_rate_adj_max[6:0]						
Reset	–	0b0101000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
pb_rate_adj_max	6:0	Sets the maximum allowed rate adjustment. This 2's complement positive value is used as a ± limit. A value of zero disables the limit.

PB_CLKP_ADJ_STATUS_B0 (0x7038)

BIT	7	6	5	4	3	2	1	0
Field	clkp_m_b0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
clkp_m_b0	7:0	Pixel rate clock pulse mode adjusted M value bits 7-0. This is the adjusted pixel frequency in kHz.

PB_CLKP_ADJ_STATUS_B1 (0x7039)

BIT	7	6	5	4	3	2	1	0
Field	clkp_m_b1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
clkp_m_b1	7:0	Pixel rate clock pulse mode adjusted M value bits 15-8. This is the adjusted pixel frequency in kHz.

PB_CLKP_ADJ_STATUS_B2 (0x703A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	clkp_m_b2[3:0]			
Reset	–	–	–	–	0x00			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
clkp_m_b2	3:0	Pixel rate clock pulse mode adjusted M value bits 19-16. This is the adjusted pixel frequency in kHz.

VTG_CTRL_B0 (0x7040)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	vtg_man_en	vtg_pclk_mode[1:0]	
Reset	–	–	–	–	–	0b0	0b01	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
vtg_man_en	2	VTG Manual Mode Enable.	0: Manual mode disabled (VTG controlled by VTRG controller, normal VTRG operation) 1: Manual Mode Enabled (VPG mode)
vtg_pclk_mode	1:0	VTG PCLK Mode.	0b0: Horizontal total/sync counter uses pixel clock Horizontal active counter uses pixel clock 0b1: Horizontal total/sync counter uses pixel clock Horizontal active counter uses pixel valid (default) 0b10: Horizontal total/sync counter uses pixel clock Horizontal active counter uses pixel clock 0b11: Horizontal total/sync counter uses pixel clock Horizontal active counter uses pixel valid (VPG mode)

VTG_HORZ_LINE_B0 (0x7044)

BIT	7	6	5	4	3	2	1	0
Field	vtg_htot_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_htot_lo	7:0	VTG horizontal total (bits 7-0). This is the horizontal line period. The value depends on the pixel clock mode.

VTG_HORZ_LINE_B1 (0x7045)

BIT	7	6	5	4	3	2	1	0
Field	vtg_htot_hi[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_htot_hi	7:0	VTG horizontal total (bits 15-8). This is the horizontal line period. The value depends on the pixel clock mode.

VTG_HORZ_LINE_B2 (0x7046)

BIT	7	6	5	4	3	2	1	0
Field	vtg_hact_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_hact_lo	7:0	VTG horizontal active (bits 7-0). This is the horizontal active pixel time. The value depends on the pixel clock mode.

VTG_HORZ_LINE_B3 (0x7047)

BIT	7	6	5	4	3	2	1	0
Field	vtg_hact_hi[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_hact_hi	7:0	VTG horizontal active (bits 15-8). This is the horizontal active pixel time. The value depends on the pixel clock mode.

VTG_HORZ_SYNC_B0 (0x7048)

BIT	7	6	5	4	3	2	1	0
Field	vtg_hstt_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_hstt_lo	7:0	VTG horizontal sync start (bits 7-0). Horizontal sync start time is from the leading edge of sync to the start of active pixels (i.e., sync width + back porch). The value depends on the pixel clock mode.

VTG_HORZ_SYNC_B1 (0x7049)

BIT	7	6	5	4	3	2	1	0
Field	vtg_hstt_hi[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_hstt_hi	7:0	VTG horizontal sync start (bits 15-8). Horizontal sync start time is from the leading edge of sync to the start of active pixels (i.e., sync width + back porch). The value depends on the pixel clock mode.

VTG_HORZ_SYNC_B2 (0x704A)

BIT	7	6	5	4	3	2	1	0
Field	vtg_hsw_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_hsw_lo	7:0	VTG horizontal sync width (bits 7-0). The value depends on the pixel clock mode.

VTG_HORZ_SYNC_B3 (0x704B)

BIT	7	6	5	4	3	2	1	0
Field	vtg_hsp	vtg_hsw_hi[6:0]						
Reset	0b1	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
vtg_hsp	7	VTG horizontal sync polarity 0 - Active low (negative) 1 - Active high (positive)

BITFIELD	BITS	DESCRIPTION
vtg_hsw_hi	6:0	VTG horizontal sync width (bits 14-8). The value depends on the pixel clock mode.

VTG_VERT_FRAME_B0 (0x704C)

BIT	7	6	5	4	3	2	1	0
Field	vtg_vtot_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_vtot_lo	7:0	VTG vertical total (bits 7-0). This is the vertical frame period. The value is in horizontal lines.

VTG_VERT_FRAME_B1 (0x704D)

BIT	7	6	5	4	3	2	1	0
Field	vtg_vtot_hi[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_vtot_hi	7:0	VTG vertical total (bits 15-8). This is the vertical frame period. The value is in horizontal lines.

VTG_VERT_FRAME_B2 (0x704E)

BIT	7	6	5	4	3	2	1	0
Field	vtg_vact_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_vact_lo	7:0	VTG vertical active (bits 7-0). This is the vertical active pixel time. The value is in horizontal lines.

VTG_VERT_FRAME_B3 (0x704F)

BIT	7	6	5	4	3	2	1	0
Field	vtg_vact_hi[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_vact_hi	7:0	VTG vertical active (bits 15-8). This is the vertical active pixel time. The value is in horizontal lines.

VTG_VERT_SYNC_B0 (0x7050)

BIT	7	6	5	4	3	2	1	0
Field	vtg_vstt_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_vstt_lo	7:0	VTG vertical sync start (bits 7-0). Vertical sync start time is from the leading edge of sync to the start of active pixels (i.e., sync width + back porch). The value is in horizontal lines.

VTG_VERT_SYNC_B1 (0x7051)

BIT	7	6	5	4	3	2	1	0
Field	vtg_vstt_hi[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_vstt_hi	7:0	VTG vertical sync start (bits 15-8). Vertical sync start time is from the leading edge of sync to the start of active pixels (i.e., sync width + back porch). The value is in horizontal lines.

VTG_VERT_SYNC_B2 (0x7052)

BIT	7	6	5	4	3	2	1	0
Field	vtg_vsw_lo[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
vtg_vsw_lo	7:0	VTG vertical sync width (bits 7-0). The value is in horizontal lines.

VTG_VERT_SYNC_B3 (0x7053)

BIT	7	6	5	4	3	2	1	0
Field	vtg_vsp	vtg_vsw_hi[6:0]						
Reset	0b1	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
vtg_vsp	7	VTG vertical sync polarity. 0 - Active low (negative) 1 - Active high (positive)
vtg_vsw_hi	6:0	VTG vertical sync width (bits 14-8). The value is in horizontal lines.

PIX_PAT_CTRL_B0 (0x7060)

BIT	7	6	5	4	3	2	1	0
Field	–	pix_pat_color[2:0]			–	–	–	pix_pat_en
Reset	–	0b0			–	–	–	0b0
Access Type	–	Write, Read			–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
pix_pat_color	6:4	Pixel pattern color enable. Each bit enables a particular color component for the initial pixel value. Pixel values invert every pixel block. Bit 4 - Red Bit 5 - Green Bit 6 - Blue	0: Color component disabled 1: Color component enabled
pix_pat_en	0	Pattern Generator Enabled. When enabled, generated pattern replaces normal received video stream.	0: Pixel pattern generator disabled - normal output 1: Pixel pattern generator enabled - pixel pattern output

PIX_PAT_BLOCK_B0 (0x7064)

BIT	7	6	5	4	3	2	1	0
Field	pix_pat_hblk_lo[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
pix_pat_hblk_lo	7:0	Pixel pattern horizontal block size bits 7-0. Horizontal block size is in pixels. The pixel value is inverted every block.	0: 1 pixel 1: 2 pixels ...

PIX_PAT_BLOCK_B1 (0x7065)

BIT	7	6	5	4	3	2	1	0
Field	–	–	pix_pat_hblk_hi[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
pix_pat_hblk_hi	5:0	Pixel pattern horizontal block size bits 12-8. Horizontal block size is in pixels. The pixel value is inverted every block.

PIX_PAT_BLOCK_B2 (0x7066)

BIT	7	6	5	4	3	2	1	0
Field	pix_pat_vblk_lo[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
pix_pat_vblk_lo	7:0	Pixel pattern vertical block size bits 7-0. Vertical block size is in lines. The pixel value is inverted every block.	0: 1 line 1: 2 lines ...

PIX_PAT_BLOCK_B3 (0x7067)

BIT	7	6	5	4	3	2	1	0
Field	–	–	pix_pat_vblk_hi[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
pix_pat_vblk_hi	5:0	Pixel pattern vertical block size bits 12-8. Vertical block size is in lines. The pixel value is inverted every block.

WATCHDOGCNT_B0 (0xE75A)

BIT	7	6	5	4	3	2	1	0
Field	WATCHDOGCNT_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WATCHDOGCNT_B0	7:0	Lower 8 bits of watchdog timer. Increments whenever a watchdog timer event occurs. Default for watchdog timer is 1s.

WATCHDOGCNT_B1 (0xE75B)

BIT	7	6	5	4	3	2	1	0
Field	WATCHDOGCNT_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WATCHDOGCNT_B1	7:0	Upper 8 bits of watchdog timer. Increments whenever a watchdog timer event occurs. Default for watchdog timer is 1s.

HPD_STATUS (0xE75E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HPD_PIN_STATE
Reset	–	–	–	–	–	–	–	
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_PIN_STATE	0	Current value of HPD input to deserializer. HPD must be HIGH for link training to occur.	0x0: HPD not present 0x1: HPD present

VLOCK_STATE (0xE760)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VL_STATE
Reset	–	–	–	–	–	–	–	
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VL_STATE	0	Video Channel is locked and outputting valid video data. VL_STATE must be HIGH for link training to occur.	0x0: Video channel not locked. 0x1: Video channel locked.

VL_LOST_CNT_B0 (0xE762)

BIT	7	6	5	4	3	2	1	0
Field	VL_LOST_CNT_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VL_LOST_CNT_B0	7:0	Lower 8 bits of video lock lost counter. Increments whenever video lock transitions from a high to low state. Can be reset to 0 by writing 0 to this register.

VL_LOST_CNT_B1 (0xE763)

BIT	7	6	5	4	3	2	1	0
Field	VL_LOST_CNT_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VL_LOST_CNT_B1	7:0	Upper 8 of video lock lost counter. Increments whenever video lock transitions from a high to low state. Can be reset to 0 by writing 0 to this register.

eHPD_IRQ_COUNT_B0 (0xE764)

BIT	7	6	5	4	3	2	1	0
Field	eHPD_IRQ_COUNT_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
eHPD_IRQ_COUNT_B0	7:0	Lower 8 bits of HPD IRQ counter. Increments whenever an HPD IRQ event occurs. HPD IRQ events occur whenever the eDP sink drives HPD low for a period between 0.5ms and 1.0ms.

eHPD_IRQ_COUNT_B1 (0xE765)

BIT	7	6	5	4	3	2	1	0
Field	eHPD_IRQ_COUNT_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
eHPD_IRQ_COUNT_B1	7:0	Upper 8 bits of HPD IRQ counter. Increments whenever an HPD IRQ event occurs. HPD IRQ events occur whenever the eDP sink drives HPD low for a period between 0.5ms and 1.0ms.

eHPD_EVENT_COUNT_B0 (0xE766)

BIT	7	6	5	4	3	2	1	0
Field	eHPD_EVENT_COUNT_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
eHPD_EVENT_COUNT_B0	7:0	Lower 8 bits of HPD disconnect event counter. Increments whenever an HPD disconnect event occurs. HPD disconnect events occur whenever the eDP sink drives HPD low for a period greater than 2.0ms.

eHPD_EVENT_COUNT_B1 (0xE767)

BIT	7	6	5	4	3	2	1	0
Field	eHPD_EVENT_COUNT_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
eHPD_EVENT_COUNT_B1	7:0	Upper 8 bits of HPD disconnect event counter. Increments whenever an HPD disconnect event occurs. HPD disconnect events occur whenever the eDP sink drives HPD low for a period greater than 2.0ms.

NACK_DEFER_CNT_B0 (0xE768)

BIT	7	6	5	4	3	2	1	0
Field	NACK_DEFER_CNT_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
NACK_DEFER_CNT_B0	7:0	Lower 8 bits of counter which counts NACKs, DEFERs and timeout responses received from the DP sink device during a native AUX read or write.

NACK_DEFER_CNT_B1 (0xE769)

BIT	7	6	5	4	3	2	1	0
Field	NACK_DEFER_CNT_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
NACK_DEFER_CNT_B1	7:0	Upper 8 bits of counter which counts NACKs, DEFERs and timeout responses received from the DP sink device during a native AUX read or write.

USER_CMD_B0 (0xE776)

BIT	7	6	5	4	3	2	1	0
Field	USER_CMD_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
USER_CMD_B0	7:0	Command register for eDP link training state machine. Command must be loaded into USER_CMD_B0 first before setting run bit in USER_CMD_B1.	0x01: Reboot training state machine 0x02: Run link training 0x10: Read eDP sink DPCD register via AUX channel 0x20: Write eDP sink DPCD register via AUX channel

USER_CMD_B1 (0xE777)

BIT	7	6	5	4	3	2	1	0
Field	USER_CMD_EXECUTE	–	–	–	–	–	–	–
Reset	0x0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
USER_CMD _EXECUTE	7	Runs command stored in USER_CMD_B0.	0x0: Do nothing 0x1: Run command

USER_DATA1_B0 (0xE778)

BIT	7	6	5	4	3	2	1	0
Field	USER_DATA1_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
USER_DATA1_B0	7:0	Lower 8 bits of DPCD register adress when performing an AUX read or write command.

USER_DATA1_B1 (0xE779)

BIT	7	6	5	4	3	2	1	0
Field	USER_DATA1_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
USER_DATA1_B1	7:0	Upper 8 bits of DPCD register adress when performing an AUX read or write command.

USER_DATA2_B0 (0xE77A)

BIT	7	6	5	4	3	2	1	0
Field	USER_DATA2_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
USER_DATA2_B0	7:0	Contains the 8 bits of data returned by an AUX read command. Otherwise, contains 8 bits of data for use by the AUX write command.

USER_DATA3_B0 (0xE77C)

BIT	7	6	5	4	3	2	1	0
Field	USER_DATA3_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
USER_DATA3_B0	7:0	Most significant 4 bits of DPCD register address when performing a 20-bit AUX read or write command.

LINK_RATE (0xE790)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LINK_RATE[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_RATE	4:0	Link rate to be used on eDP links for training.	0x0: Reserved ... 0x5: Reserved 0x6: Set link rate to 1.62Gb/s 0x7: Reserved 0x8: Set link rate to 2.16Gb/s 0x9: Set link rate to 2.43Gb/s 0xA: Set link rate to 2.7Gb/s 0xB: Reserved 0xC: Set link rate to 3.24Gb/s 0xD: Reserved 0xE: Reserved 0xF: Reserved 0x10: Set link rate to 4.32Gb/s 0x11: Reserved ... 0x19: Reserved 0x1A: Set link rate to 5.4Gb/s 0x1B: Reserved 0x1C: Reserved 0x1D: Reserved 0x1E: Set link rate to 8.1Gb/s 0x1F: Reserved

LANE_COUNT (0xE792)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LANE_COUNT[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LANE_COUNT	2:0	Number of eDP links to be used.	0x0: Reserved 0x1: Use one link 0x2: Use two links 0x3: Reserved 0x4: Use four links 0x5: Reserved 0x6: Reserved 0x7: Reserved

HRES_B0 (0xE794)

BIT	7	6	5	4	3	2	1	0
Field	HRES_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HRES_B0	7:0	Lower 8 bits of the horizontal resolution of the mainstream video source. This value is the number of active pixels per line.	0xXX: Lower 8 bits of the horizontal resolution of the mainstream video source

HRES_B1 (0xE795)

BIT	7	6	5	4	3	2	1	0
Field	HRES_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HRES_B1	7:0	Upper 8 bits of the horizontal resolution of the mainstream video source. This value is the number of active pixels per line.	0xXX: Upper 8 bits of the horizontal resolution of the mainstream video source

HFP_B0 (0xE796)

BIT	7	6	5	4	3	2	1	0
Field	HFP_B0[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HFP_B0	7:0	Lower 8 bits of the horizontal front porch of the mainstream video source. This value is expressed in pixels.	0xXX: Lower 8 bits of the horizontal front porch of the mainstream video source

HFP_B1 (0xE797)

BIT	7	6	5	4	3	2	1	0
Field	HFP_B1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HFP_B1	7:0	Upper 8 bits of the horizontal front porch of the mainstream video source. This value is expressed in pixels.	0xXX: Upper 8 bits of the horizontal front porch of the mainstream video source

HSW_B0 (0xE798)

BIT	7	6	5	4	3	2	1	0
Field	HSW_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HSW_B0	7:0	Lower 8 bits of the horizontal sync width of the mainstream video source. This value is expressed in pixels.	0xXX: Lower 8 bits of the horizontal sync width of the mainstream video source

HSW_B1 (0xE799)

BIT	7	6	5	4	3	2	1	0
Field	HSW_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HSW_B1	7:0	Upper 8 bits of the horizontal sync width of the mainstream video source. This value is expressed in pixels.	0xXX: Upper 8 bits of the horizontal sync width of the mainstream video source

HBP_B0 (0xE79A)

BIT	7	6	5	4	3	2	1	0
Field	HBP_B0[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HBP_B0	7:0	Lower 8 bits of the horizontal back porch of the mainstream video source. This value is expressed in pixels.	0xXX: Lower 8 bits of the horizontal back porch of the mainstream video source

HBP_B1 (0xE79B)

BIT	7	6	5	4	3	2	1	0
Field	HBP_B1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HBP_B1	7:0	Upper 8 bits of the horizontal back porch of the mainstream video source. This value is expressed in pixels.	0xXX: Upper 8 bits of the horizontal back porch of the mainstream video source

VRES_B0 (0xE79C)

BIT	7	6	5	4	3	2	1	0
Field	VRES_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VRES_B0	7:0	Lower 8 bits of the vertical resolution of the mainstream video source This value is the number of active lines per frame.	0xXX: Lower 8 bits of the vertical resolution of the mainstream video source

VRES_B1 (0xE79D)

BIT	7	6	5	4	3	2	1	0
Field	VRES_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VRES_B1	7:0	Upper 8 bits of the vertical resolution of the mainstream video source This value is the number of active lines per frame.	0xXX: Upper 8 bits of the vertical resolution of the main stream video source

VFP_B0 (0xE79E)

BIT	7	6	5	4	3	2	1	0
Field	VFP_B0[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VFP_B0	7:0	Lower 8 bits of the vertical front porch of the mainstream video source. This value is expressed in lines.	0xXX: Lower 8 bits of the vertical front porch of the mainstream video source

VFP_B1 (0xE79F)

BIT	7	6	5	4	3	2	1	0
Field	VFP_B1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VFP_B1	7:0	Upper 8 bits of the vertical front porch of the mainstream video source. This value is expressed in lines.	0xXX: Upper 8 bits of the vertical front porch of the mainstream video source

VSW_B0 (0xE7A0)

BIT	7	6	5	4	3	2	1	0
Field	VSW_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VSW_B0	7:0	Lower 8 bits of the vertical sync width of the mainstream video source. This value is expressed in lines.	0xXX: Lower 8 bits of the vertical sync width of the mainstream video source

VSW_B1 (0xE7A1)

BIT	7	6	5	4	3	2	1	0
Field	VSW_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VSW_B1	7:0	Upper 8 bits of the vertical sync width of the mainstream video source. This value is expressed in lines.	0xXX: Upper 8 bits of the vertical sync width of the mainstream video source

VBP_B0 (0xE7A2)

BIT	7	6	5	4	3	2	1	0
Field	VBP_B0[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VBP_B0	7:0	Lower 8 bits of the vertical back porch of the mainstream video source. This value is expressed in lines.	0xXX: Lower 8 bits of the vertical back porch of the mainstream video source

VBP_B1 (0xE7A3)

BIT	7	6	5	4	3	2	1	0
Field	VBP_B1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VBP_B1	7:0	Upper 8 bits of the vertical back porch of the mainstream video source. This value is expressed in lines.	0xXX: Upper 8 bits of the vertical back porch of the mainstream video source

HWORDS_B0 (0xE7A4)

BIT	7	6	5	4	3	2	1	0
Field	HWORDS_B0[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HWORDS_B0	7:0	Lower 8 bits of this value is the total number of 16-bit words in a line of active data. This is calculated with the following formula: HWORDS = ((HRES x bits/pixel)/16) - LANE_COUNT.	0xXX: Lower 8 bits of this value is the total number of 16-bit words in a line of active data

HWORDS_B1 (0xE7A5)

BIT	7	6	5	4	3	2	1	0
Field	HWORDS_B1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HWORDS_B1	7:0	Upper 8 bits of this value is the total number of 16-bit words in a line of active data. This is calculated with the following formula: HWORDS = ((HRES x bits/pixel)/16) - LANE_COUNT.	0xXX: Upper 8 bits of this value is the total number of 16-bit words in a line of active data

MVID_B0 (0xE7A6)

BIT	7	6	5	4	3	2	1	0
Field	MVID_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MVID_B0	7:0	Lower 8 bits of the MSA parameter for asynchronous clocking. MVID = (PCLK_in_MHz x NVID)/(Link_Rate_in_GBs * 100).	0xXX: Lower 8 bits of the MSA parameter for asynchronous clocking

MVID_B1 (0xE7A7)

BIT	7	6	5	4	3	2	1	0
Field	MVID_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MVID_B1	7:0	Upper 8 bits of the MSA parameter for asynchronous clocking. MVID = (PCLK_in_MHz x NVID)/(Link_Rate_in_GBs * 100).	0xXX: Upper 8 bits of the MSA parameter for asynchronous clocking

NVID_B0 (0xE7A8)

BIT	7	6	5	4	3	2	1	0
Field	NVID_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
NVID_B0	7:0	Lower 8 bits of the MSA parameter for asynchronous clocking. Should always be set to 0x8000 (32768). MVID = (PCLK_in_MHz x NVID)/(Link_Rate_in_GBs * 100).	0xXX: Lower 8 bits of the MSA parameter for asynchronous clocking

NVID_B1 (0xE7A9)

BIT	7	6	5	4	3	2	1	0
Field	NVID_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
NVID_B1	7:0	Upper 8 bits of the MSA parameter for asynchronous clocking. Should always be set to 0x8000 (32768). MVID = (PCLK_in_MHz x NVID)/(Link_Rate_in_GBs * 100).	0xXX: Upper 8 bits of the MSA parameter for asynchronous clocking

TUC_VALUE_B0 (0xE7AA)

BIT	7	6	5	4	3	2	1	0
Field	TUC_VALUE_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TUC_VALUE_B0	7:0	Lower 8 bits of the transfer unit which is a display port packet and represents valid data symbols and stuffing symbols. This should always be set to 0x40.	0xXX: Lower 8 bits of the transfer unit which is a display port packet and represents valid data symbols and stuffing symbols

TUC_VALUE_B1 (0xE7AB)

BIT	7	6	5	4	3	2	1	0
Field	TUC_VALUE_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TUC_VALUE_B1	7:0	Upper 8 bits of the transfer unit which is a display port packet and represents valid data symbols and stuffing symbols. This should always be set to 0x00.	0xXX: Upper 8 bits of the transfer unit which is a display port packet and represents valid data symbols and stuffing symbols

HVPOL (0xE7AC)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VSYNC_POL	HSYNC_POL
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VSYNC_POL	1	Provides the polarity value for the video vertical sync signal. This bit is sent as a part of the main stream attributes as VSP.	0b0: Active high 0b1: Active low
HSYNC_POL	0	Provides the polarity value for the video horizontal sync signal. This bit is sent as a part of the main stream attributes as HSP.	0b0: Active high 0b1: Active low

ERRB_ENABLE_MASK_B0 (0xE7AE)

BIT	7	6	5	4	3	2	1	0
Field	HPD_EVENT	RSVD	–	–	–	–	–	TRAIN_PASS
Reset	0b0	0x0	–	–	–	–	–	0b0
Access Type	Write, Read		–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_EVENT	7	Allows reporting of the condition that either an HPD IRQ or HPD DISCONNECT event has occurred. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting that either an HPD IRQ or HPD DISCONNECT event has occurred. 0b1: Reporting that either an HPD IRQ or HPD DISCONNECT event has occurred.
TRAIN_PASS	0	Allow reporting of the condition that link training has completed successfully. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting that link training has completed successfully. 0b1: Reporting that link training has completed successfully

ERRB_ENABLE_MASK_B1 (0xE7AF)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_ENABLE	TP1_FAIL	TP2_FAIL	NO_PARMS	NO_HPD	NO_VL	WD_TRIGGER	VL_LOST
Reset	0x0	0x0	0x0	0x0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_ENABLE	7	When this bit is enabled, ERRB gets asserted whenever any of the conditions defined by ERRB_ENABLE_MASK_B0 or ERRB_ENABLE_MASK_B1 have been met.	0b0: No assertion of ERRB 0b1: Allow assertion of ERRN
TP1_FAIL	6	Allows reporting to training pattern 1 failure. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting of training phase 1 failure 0b1: Reporting of training phase 1 failure
TP2_FAIL	5	Allows reporting to training pattern 2 failure. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting of training phase 2 failure 0b1: Reporting of training phase 2 failure
NO_PARMS	4	Allows reporting of the condition that training was attempted but no training configuration was found. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting of training attempted but no training configuration was found 0b1: Reporting of training attempted but no training configuration was found
NO_HPD	3	Allows reporting of the condition that training was attempted but HPD was LOW. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting of training attempted with HPD LOW. 0b1: Reporting of training attempted with HPD LOW.
NO_VL	2	Allows reporting of the condition that training was attempted but video lock was LOW. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting of training attempted with video lock LOW. 0b1: Reporting of training attempted with video lock LOW.
WD_TRIGGER	1	Allows reporting of the condition that the watchdog timer has triggered. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting that the watchdog timer has triggered. 0b1: Reporting that the watchdog timer has triggered.
VL_LOST	0	Allows reporting of the condition that video lock was lost unexpectedly. ERRB_ENABLE must also be set to allow this condition to assert ERRB.	0b0: No reporting that video lock was lost unexpectedly 0b1: Reporting that video lock was lost unexpectedly

SS_ENABLE_B0 (0xE7B0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SS_ENABLE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SS_ENABLE	0	This bit must be set to allow waiting for the CMU to lock. It also should be set when using SSC. Otherwise, a fixed wait time of 20µS is used.	0x0: Wait for 20µS 0x1: Wait for CMU lock. Must use this setting if SSC is enabled to the DP sink.

SS_ENABLE_B1 (0xE7B1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	SSC_ENABLE	–	–	–	–
Reset	–	–	–	0x0	–	–	–	–
Access Type	–	–	–	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SSC_ENABLE	4	Determines whether spread spectrum clocking (SSC) is used with the DP sink device.	0x0: Disable SSC to DP sink device 0x1: Enable SSC to DP sink device

CLK_REF_B0 (0xE7B2)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B0	7:0	Provides control for the eDP PLL.

CLK_REF_B1 (0xE7B3)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B1	7:0	Provides control for the eDP PLL.

CLK_REF_B2 (0xE7B4)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B2	7:0	Provides control for the eDP PLL.

CLK_REF_B3 (0xE7B5)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B3[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B3	7:0	Provides control for the eDP PLL.

CLK_REF_B4 (0xE7B6)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B4[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B4	7:0	Provides control for the eDP PLL divisor values used for rate selection.

CLK_REF_B5 (0xE7B7)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B5[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B5	7:0	Provides control for the eDP PLL divisor values used for rate selection.

CLK_REF_B6 (0xE7B8)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B6[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B6	7:0	Provides control for the eDP PLL divisor values used for rate selection.

CLK_REF_B7 (0xE7B9)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B7[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B7	7:0	Provides control for the eDP PLL divisor values used for rate selection.

CLK_REF_B8 (0xE7BA)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B8[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B8	7:0	Provides control of eDP CMU for rate selection.

CLK_REF_B9 (0xE7BB)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B9[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B9	7:0	Provides control of eDP CMU for rate selection.

CLK_REF_B10 (0xE7BC)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B10[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B10	7:0	Provides control of eDP CMU for rate selection.

CLK_REF_B11 (0xE7BD)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B11[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B11	7:0	Provides control of eDP CMU for rate selection.

CLK_REF_B12 (0xE7BE)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B12[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B12	7:0	Provides control for the eDP DPLL.

CLK_REF_B13 (0xE7BF)

BIT	7	6	5	4	3	2	1	0
Field	CLK_REF_B13[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CLK_REF_B13	7:0	Provides control for the eDP DPLL.

HACT_DSC_VTRG_B0 (0xE7C4)

BIT	7	6	5	4	3	2	1	0
Field	HACT_DSC_VTRG_B0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HACT_DSC_VTRG_B0	7:0	Lower 8 bits of the horizontal resolution of the video stream. This value is required when using the auto VTRG functionality along with DSC. To calculate this value, take the actual horizontal resolution and divide by 3. If there is a remainder, then round up to the next integer. Take this value and multiply by 3 to get HACK_DSC_VTRG_B0/B1.

HACT_DSC_VTRG_B1 (0xE7C5)

BIT	7	6	5	4	3	2	1	0
Field	HACT_DSC_VTRG_B1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HACT_DSC_VTRG_B1	7:0	Upper 8 bits of the horizontal resolution of the video stream. This value is required when using the auto VTRG functionality along with DSC. To calculate this value, take the actual horizontal resolution and divide by three. If there is a remainder, then round up to the next integer. Take this value and multiply by 3 to get HACK_DSC_VTRG_B0/B1.

AUTO_VTRG_ENABLE (0xE7C6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	AUTO_VTRG_ENABLE
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_VTRG_ENABLE	0	Used to automatically enable the video timing regenerator logic upon completion of link training. Must have pixel clock frequency, in KHz, set in HS88 registers 0x7014, 0x7015 and 0x7016.	0x0: Disable auto VTRG functionality 0x1: Enable auto VTRG functionality

HPD_MASK_B1 (0xE7D1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HPD_DEBOUNCE_DISABLE
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HPD_DEBOUNCE_DISABLE	0	Whenever HPD transitions from low to high, the default is to wait 50ms to debounce. For systems that have HPD hardwired from the DP sink device, this debouncing is unnecessary and increases the link training time by 50ms. This debouncing can be eliminated by setting this bit just prior to sending the link training command.	0x0: Enable 50ms debounce of HPD 0x1: Disable 50ms debounce of HPD

NO_ALIGN_CHK (0xE7DE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	NO_ALIGN_CHK
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
NO_ALIGN_CHK	0	Determines whether the lane alignment check is executed after successfully passing training pattern 2.	0x0: Do lane alignment check 0x1: Skip lane alignment check

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/22	Release for market intro	—

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