DS90UH984-Q1 4K FPD-Link IV to Embedded DisplayPort Bridge Deserializer

1 Features

- DisplayPort (DP) / Embedded DisplayPort (eDP) Transmitter
  - VESA DP v1.4a/eDP v1.4b Transmitter
  - HBR3/HBR2/HBR/RBR Link Bit Rates
  - Main Link: 1, 2, or 4 lanes
  - Each lane up to 8.1Gbps
  - AUX CH 1Mbps
  - Hot Plug Detect (HPD)
  - Extracts Aggregated Video Streams to Local eDP Display
  - Suitable for 4K @ 60 Hz Video Resolution
  - Stream Synchronization and Splitting
- FPD-Link IV Interface
  - 13.5/12.528/10.8/6.75/3.375 Gbps per Channel; Up to 27 Gbps over Dual Channels
  - Coax/STP Interconnect Support
  - Selectable 1, 2 Channels
  - Daisy-Chain & Splitting
  - Adaptive Equalization
- Ultra-low Latency Control Channel
  - Two Fast-Mode Plus I2C up to 1MHz (up to 3.4MHz local bus access)
  - High-Speed GPIOs
  - Supports SPI and UART passthrough GPIOs
- Backwards Compatibility
  - Integrated HDCP v1.4 with on-chip keys
  - 720p 92x and 1080p/2K 94x FPD-Link III Product Families
- Security and Diagnostics
  - Voltage and Temperature Monitoring
  - BIST and Pattern Generation
  - CRC and Error Diagnostics
  - ECC on Control Bits
  - Unique ID for Counterfeit Protection
- Advanced Link robustness and EMC control
  - Spread spectrum clocking generation (SSCG)
  - Adaptive Receiver Equalization (AEQ)
- Low power operation
  - 1.8V and 1.15V Dual power supply
- AEC-Q100 Qualified for Automotive Applications
  - AEC-Q Grade-Level 2 , -40°C to 105°C
  - ISO 10605 and IEC 61000-4-2 ESD Compliant

2 Applications

- Automotive Displays:
  - Central Information Displays (CID)
  - Rear Seat Entertainment (RSE)
  - Digital Instrument Clusters
  - Head Units and HMI Modules
  - Head Up Display (HUD)
  - Rear View and Side Mirror Displays

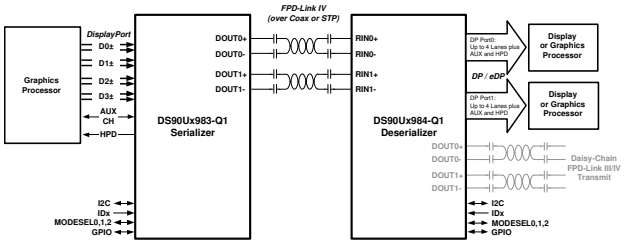
3 Description

The DS90UH984-Q1 is an FPD-Link IV to DisplayPort (DP) / Embedded DisplayPort (eDP) bridge device. In conjunction with an FPD-Link IV serializer, the chipset receives a high-speed serialized interface over low-cost 50Ω coax or STP/STQ cables. The DS90UH984-Q1 is a VESA DP v1.4a/eDP v1.4b compatible device that supports advanced features such as HBR3, and SuperFrame formats. The device supports video resolutions up to 4K 30-bit color. The FPD-Link IV interface supports video and audio data transmission and full duplex control, including I2C, and GPIO data over the same link. Consolidation of video data and control over FPD-Link IV lanes reduces the interconnect size and weight and simplifies system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, and randomization. In backward compatible FPD-Link III mode, the device supports up to 2K resolutions with 24-bit color depth over a single/dual link as well as HDCP v1.4 support when paired with an HDCP capable deserializer.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UH984-Q1	VQFNP (88)	12mm × 12mm

4 Simplified Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2022	*	Initial RTM NDA Release

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6 Pin Configuration and Functions

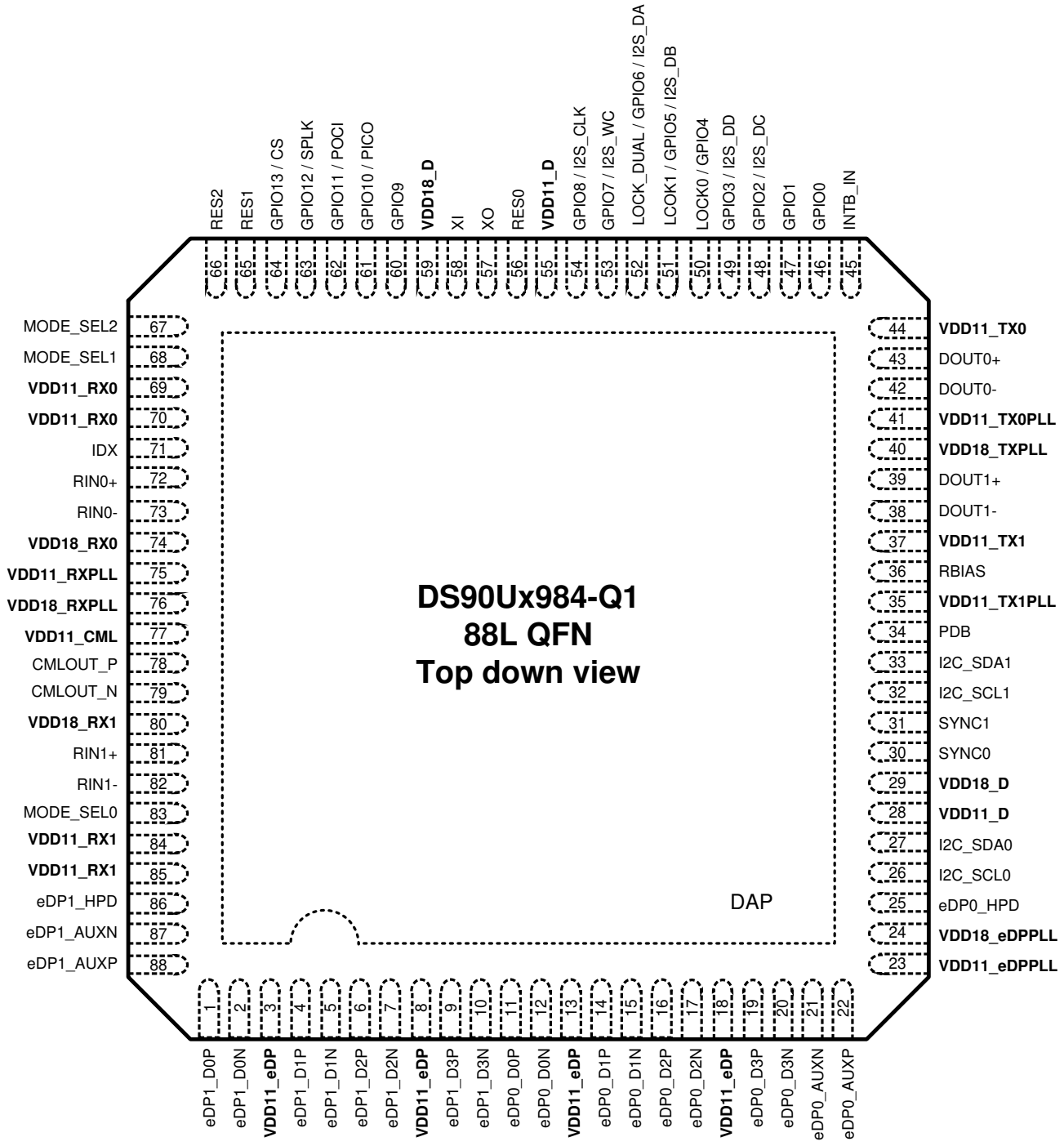

Figure 6-1. 88-Pin QFN Top View

Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	PIN NUMBER		
EMBEDDED DISPLAYPORT OUTPUT			
eDP0_D0P	11	O, eDP	Embedded DisplayPort / DisplayPort Main (eDP/DP) Link Port 0 Output. The eDP0 Main Link output consists of up to 4 differential pairs (data lanes). For DP mode, it is recommended these PCB traces maintain 100 Ω differential impedance. For eDP mode, it is recommended these PCB traces maintain 85 Ω differential impedance. The pin must be AC-coupled with a 0.1µF capacitor. If eDP port 0 or data pair is unused, leave as open. See Section 8.3.1
eDP0_D0N	12		
eDP0_D1P	14		
eDP0_D1N	15		
eDP0_D2P	16		
eDP0_D2N	17		
eDP0_D3P	19		
eDP0_D3N	20		
eDP1_D0P	1	O, eDP	Embedded DisplayPort / DisplayPort (eDP/DP) Main Link Port 1 Output. The eDP1 Main Link output consists of up to 4 differential pairs (data lanes). For DP mode, it is recommended these PCB traces maintain 100 Ω differential impedance. For eDP mode, it is recommended these PCB traces maintain 85 Ω differential impedance. The pin must be AC-coupled with a 0.1µF capacitor. If eDP port 1 or data pair is unused, leave as open. See Section 8.3.1
eDP1_D0N	2		
eDP1_D1P	4		
eDP1_D1N	5		
eDP1_D2P	6		
eDP1_D2N	7		
eDP1_D3P	9		
eDP1_D3N	10		
OTHER EMBEDDED DISPLAYPORT			
eDP0_HPD	25	I	Hot Plug Detect input signal for eDP0. 100k pull-down resistor required. Leave as open if eDP port 0 is unused.
eDP1_HPD	86	I	Hot Plug Detect input signal for eDP1. 100k pull-down resistor required. Leave as open if eDP port 1 is unused.
eDP0_AUXP	22	I/O	AUX Channel Differential Input/Output for eDP0. 100k pull-down resistor is optional for eDP connection but is required for DP connection. Leave as open if eDP/DP port 0 is unused.
eDP0_AUXN	21	I/O	AUX Channel Differential Input/Output for eDP0. 100k pull-up resistor is optional for eDP connection but is required for DP connection. Leave as open if eDP/DP port 0 is unused.
eDP1_AUXP	88	I/O	AUX Channel Differential Input/Output for eDP1. 100k pull-down resistor is optional for eDP connection but is required for DP connection. Leave as open if eDP/DP port 1 is unused.
eDP1_AUXN	87	I/O	AUX Channel Differential Input/Output for eDP0. 100k pull-up resistor is optional for eDP connection but is required for DP connection. Leave as open if eDP/DP port 1 is unused.
FPD-LINK INPUT INTERFACE			
RIN0+	72	I/O	FPD-Link Receiver Input Channel 0 and 1 FPD-Link inputs can be connected to a compatible FPD-Link III / FPD-Link IV transmitter through a STP or coaxial cable. For differential configurations, it is recommended these PCB traces maintain 100 Ω differential impedance and each pin must be AC-coupled with a 0.1µF capacitor placed as close as possible to the device. For single-ended configurations, RIN0+ and RIN1+ should be AC-coupled with 0.1µF, and RIN0- and RIN1- should be connected to a 47nF capacitor and 50ohm termination resistor as close to the pin as possible. If FPD-Link Input Port 1 is unused, leave RIN1+ and RIN1- open. See Section 9.2 for typical connection diagrams for STP and coax configurations.
RIN0-	73		
RIN1+	81	I/O	
RIN1-	82		

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PIN		I/O, TYPE	DESCRIPTION
NAME	PIN NUMBER		
FPD-LINK DAISY-CHAIN INTERFACE			
DOUT0+	43	I/O	FPD-Link Daisy-Chain Output Channel 0 It can interface with a compatible FPD-Link III / FPD-Link IV deserializer RX through a STP or coaxial cable. For differential configurations, it is recommended these PCB traces maintain 100 Ω differential impedance and each pin must be AC-coupled with a 0.1µF capacitor placed as close as possible to the device. For single-ended configurations, RIN0+ and RIN1+ should be AC-coupled with 0.1µF, and RIN0- and RIN1- should be connected to a 47nF capacitor and 50ohm termination resistor as close to the pin as possible. If FPD-Link Input Port 1 is unused, leave RIN1+ and RIN1- open. See Section 9.2 for typical connection diagrams for STP and coax configurations.
DOUT0-	42		
DOUT1+	39	I/O	
DOUT1-	38		
I2C BUS			
I2C_SDA0	27	I/O, Open-Drain	I2C Bus 0 Data Signal Pull-up resistor to either 1.8V or 3.3V required for I2C functionality. I2C voltage is selected by IDX pin. Refer to “I2C Bus Pullup Resistor Calculation” SLVA689 to size the pull up resistor. If pin is unused, a pullup is still required to the I2C bus voltage set by the IDX pin.
I2C_SCL0	26	I/O, Open-Drain	I2C Bus 0 Clock Signal Pull-up resistor to either 1.8V or 3.3V required for I2C functionality. I2C voltage is selected by IDX pin. Refer to “I2C Bus Pullup Resistor Calculation” SLVA689 to size the pull up resistor. If pin is unused, a pullup is still required to the I2C bus voltage set by the IDX pin.
I2C_SDA1	33	I/O, Open-Drain	I2C Bus 1 Data Signal Pull-up resistor to either 1.8V or 3.3V required for I2C functionality. I2C voltage is selected by IDX pin. Refer to “I2C Bus Pullup Resistor Calculation” SLVA689 to size the pull up resistor. If pin is unused, a pullup is still required to the I2C bus voltage set by the IDX pin.
I2C_SCL1	32	I/O, Open-Drain	I2C Bus 1 Clock Signal Pull-up resistor to either 1.8V or 3.3V required for I2C functionality. I2C voltage is selected by IDX pin. Refer to “I2C Bus Pullup Resistor Calculation” SLVA689 to size the pull up resistor. If pin is unused, a pullup is still required to the I2C bus voltage set by the IDX pin.
IDX	71	S	I2C Target Address Selection and I2C Voltage Selection. See Section 8.5.1.1. DO NOT LEAVE OPEN OR NO CONNECT. Connect to external pull-up and pull-down resistors to create a voltage divider.
CONTROL			
MODE_SEL0	83	S	Mode Select 0. MODE_SEL0 is used to select initial device configuration. See Section 8.4.1 for details. DO NOT LEAVE OPEN OR NO CONNECT. Connect to external pull-up and pull-down resistors to create a voltage divider.
MODE_SEL1	68	S	Mode Select 1. MODE_SEL1 is used to select initial device configuration. See Section 8.4.1 for details. DO NOT LEAVE OPEN OR NO CONNECT. Connect to external pull-up and pull-down resistors to create a voltage divider.
MODE_SEL2	67	S	Mode Select 2. MODE_SEL2 is used to select initial device configuration. See Section 8.4.1 for details. DO NOT LEAVE OPEN OR NO CONNECT. Connect to external pull-up and pull-down resistors to create a voltage divider.
PDB	34	I, LVCMOS	Power-Down Mode Input Pin. If PDB is High, the device is enabled (normal operation). If PDB is Low, the device is powered down. If not controlled by external controller, RC filter of 10k and >10uF recommended to ensure PDB is pulled high after power supplies are ramped and stable. Pin has internal 25 kΩ pull-down resistor. See Section 9.2.

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PIN		I/O, TYPE	DESCRIPTION
NAME	PIN NUMBER		
INTB_IN	45	I, Open-Drain	Interrupt input INTB_IN is an active low interrupt input pin. This interrupt signal will propagate to the paired serializer when driven low by external device. INTB_IN has minimum rise time requirement specified in Section 7.6, a series resistor and capacitor to ground is recommended between the device and the driving source to slow the edge rate when using a source with strong drive capability. Pull-up resistor to either 1.8V or 3.3V required. Recommended pull-up: 4.7kΩ to 1.8V or 3.3V.See Section 8.3.9.
SYNCHRONIZATION PINS			
SYNC0	30	I/O, LVCMOS	Synchronization input/output. This pin is used to link the two deserializers (primary and secondary) for the dual deserializer synchronization. See Section 8.3.20. Do not tie to VDD. Leave as open if unused. Pin has internal 25 kΩ pull-down resistor.
SYNC1	31	I/O, LVCMOS	Synchronization input/output. This pin is used to link the two deserializers (primary and secondary) for the dual deserializer synchronization. See Section 8.3.20. Do not tie to VDD. Leave as open if unused. Pin has internal 25 kΩ pull-down resistor.
GPIO PINS (GENERAL PURPOSE INPUT OUTPUT)			
GPIO0	46	I/O, LVCMOS	General Purpose Input/Output (GPIO) 0. See Section 8.3.10 GPIO0 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. Leave as open if unused.
GPIO1	47	I/O, LVCMOS	General Purpose Input/Output (GPIO) 1. See Section 8.3.10 GPIO1 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. Leave as open if unused.
GPIO2 / I2S_DC	48	I/O, LVCMOS	General Purpose Input/Output (GPIO) 2. See Section 8.3.10 GPIO2 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. Leave as open if unused. (Pin is shared with I2S_DC)
GPIO3 / I2S_DD	49	I/O, LVCMOS	General Purpose Input/Output (GPIO) 3. See Section 8.3.10 GPIO3 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. Leave as open if unused. (Pin is shared with I2S_DD)
LOCK0 / GPIO4	50	I/O, LVCMOS	General Purpose Input/Output (GPIO) 4. See Section 8.3.10 GPIO4 defaults to output lock status for FPD-Link Input Port 0. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. Leave as open if unused.
LOCK1 / GPIO5 / I2S_DB	51	I/O, LVCMOS	General Purpose Input/Output (GPIO) 5. See Section 8.3.10 GPIO5 defaults to output lock status for FPD-Link Input Port 1. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. (Pin is shared with I2S_DB) Leave as open if unused.
LOCK_DUAL / GPIO6 / I2S_DA	52	I/O, LVCMOS	General Purpose Input/Output (GPIO) 6. See Section 8.3.10 GPIO6 defaults to output the ANDed lock status of all active FPD-Link Input Ports (FPD-Link Port 0 and FPD-Link Port 1 in dual mode, FPD-Link Port 0 in single mode). Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. Can be used as a ADC input for voltage sensing, see Section 8.3.7.3. (Pin is shared with I2S_DA) Leave as open if unused.

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PIN		I/O, TYPE	DESCRIPTION
NAME	PIN NUMBER		
GPIO7 / I2S_WC	53	I/O, LVCMOS	General Purpose Input/Output (GPIO) 7. See Section 8.3.10 GPIO7 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. (Pin is shared with I2S_WC) Leave as open if unused.
GPIO8 / I2S_CLK	54	I/O, LVCMOS	General Purpose Input/Output (GPIO) 8. See Section 8.3.10 GPIO8 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. Can be used as a ADC input for voltage sensing, see Section 8.3.7.3. (Pin is shared with I2S_CLK) Leave as open if unused.
GPIO9	60	I/O, LVCMOS	General Purpose Input/Output (GPIO) 9. See Section 8.3.10 GPIO9 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. Leave as open if unused.
GPIO10 / PICO	61	I/O, LVCMOS	General Purpose Input/Output (GPIO) 10. See Section 8.3.10 GPIO10 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. When configured as an input, this pin can be used for sensing the input voltage of Line-Fault Detection. A 0.1µF decoupling capacitor requires as close to the device pin for filtering any high frequency noise when in Line-Fault Detection mode. See Section 8.3.8 (Pin is shared with PICO) Leave as open if unused.
GPIO11 / POCI	62	I/O, LVCMOS	General Purpose Input/Output (GPIO) 11. See Section 8.3.10 GPIO11 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. When configured as an input, this pin can be used for sensing the input voltage of Line-Fault Detection. A 0.1µF decoupling capacitor requires as close to the device pin for filtering any high frequency noise when in Line-Fault Detection mode. See Section 8.3.8 (Pin is shared with POCI) Leave as open if unused.
GPIO12 / SPLK	63	I/O, LVCMOS	General Purpose Input/Output (GPIO) 12. See Section 8.3.10 GPIO12 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. When configured as an input, this pin can be used for sensing the input voltage of Line-Fault Detection. A 0.1µF decoupling capacitor requires as close to the device pin for filtering any high frequency noise when in Line-Fault Detection mode. See Section 8.3.8 (Pin is shared with SPLK) Leave as open if unused.
GPIO13 / CS	64	I/O, LVCMOS	General Purpose Input/Output (GPIO) 13. See Section 8.3.10 GPIO13 defaults to an input state. Only while in input mode, the pin has an internal 25 kΩ pull down resistor. Using a pull-up resistor of 10 kΩ is recommended, do not tie directly to VDD. When configured as an input, this pin can be used for sensing the input voltage of Line-Fault Detection. A 0.1µF decoupling capacitor requires as close to the device pin for filtering any high frequency noise when in Line-Fault Detection mode. See Section 8.3.8 (Pin is shared with CS) Leave as open if unused.
I2S PINS			
GPIO2 / I2S_DC	48	O, LVCMOS	Slave Mode I2S Data Output Pin (Pin is shared with GPIO2) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. See Section 8.3.19.3 Leave as open if unused.

PIN		I/O, TYPE	DESCRIPTION
NAME	PIN NUMBER		
GPIO3 / I2S_DD	49	O, LVCMOS	Slave Mode I2S Data Output Pin (Pin is shared with GPIO3) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. See Section 8.3.19.3 Leave as open if unused.
LOCK1 / GPIO5 / I2S_DB	51	O, LVCMOS	Slave Mode I2S Data Output Pin (Pin is shared with GPIO5) Pin functionality defaults to output LOCK status. See Section 8.3.19.3 Leave as open if unused.
LOCK_DUAL / GPIO6 / I2S_DA	52	O, LVCMOS	Slave Mode I2S Data Output Pin (Pin is shared with GPIO6) Pin functionality defaults to output LOCK status. See Section 8.3.19.3 Leave as open if unused.
GPIO7 / I2S_WC	53	O, LVCMOS	Slave Mode I2S Word Clock Output Pin (Pin is shared with GPIO7) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. See Section 8.3.19.3 Leave as open if unused.
GPIO8 / I2S_CLK	54	O, LVCMOS	Slave Mode I2S Clock Output Pin (Pin is shared with GPIO8) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. See Section 8.3.19.3 Leave as open if unused.
SPI PINS			
GPIO10 / PICO	61	I/O, LVCMOS	SPI Peripheral IN Controller OUT (PICO) pin (Pin is shared with GPIO10) SPI is supported for backward compatibility mode only. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. Leave as open if unused.
GPIO11 / POCI	62	I/O, LVCMOS	SPI Peripheral OUT Controller IN (POCI) pin (Pin is shared with GPIO11) SPI is supported for backward compatibility mode only. Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. Leave as open if unused.
GPIO12 / SPLK	63	I/O, LVCMOS	SPI Clock pin (Pin is shared with GPIO12) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. Leave as open if unused.
GPIO13 / CS	64	I/O, LVCMOS	SPI Chip Select pin (Pin is shared with GPIO13) Pin functionality defaults to GPIO with an internal 25 kΩ pull down resistor. Leave as open if unused.
POWER and GROUND			
VDD18_eDPPLL	24	Power	1.8 V (±5%) supply Requires 1-µF and 0.1-µF capacitors to GND. See Section 9.2 for filtering recommendations.
VDD18_D	29		
VDD18_TXPLL	40		
VDD18_D	59		
VDD18_RX0	74		
VDD18_RXPLL	76		
VDD18_RX1	80		

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PIN		I/O, TYPE	DESCRIPTION
NAME	PIN NUMBER		
VDD11_eDP	3	Power	1.15V (±5%) supply Requires 1-µF and 0.1-µF capacitors to GND. See Section 9.2 for filtering recommendations.
VDD11_eDP	8		
VDD11_eDP	13		
VDD11_eDP	18		
VDD11_eDPPLL	23		
VDD11_D	28		
VDD11_TX1PLL	35		
VDD11_TX1	37		
VDD11_TX0PLL	41		
VDD11_TX0	44		
VDD11_D	55		
VDD11_RX0	69		
VDD11_RX0	70		
VDD11_RXPLL	75		
VDD11_CML	77		
VDD11_RX1	84		
VDD11_RX1	85		
GND	DAP	GND	Thermal pad is the large metal contact at the bottom side, located at the center of the VQFN package. Connect to the ground plane (GND).
CLOCK REFERENCE PINS			
XI	58	I	Crystal Input / External Oscillator Reference input A parallel resonance crystal should be attached between this pin and XO. An external 27 MHz 1.8V LVCMOS-level oscillator (±50 ppm) can also drive the XI input. Ensure matching capacitance (CL_1 and CL_2) calculation is as close as possible to the load capacitance of the crystal. The crystal should be placed as close as possible to the serializer device. Total capacitance must be <20pF. See Section 9.2.1.
XO	57	O	Crystal output Output Pin for providing crystal oscillator reference. A resistor should be added in series with XO pin for current limiting to maintain the power level to 100µW RMS maximum. The selection of series resistor value is based on crystal specification. Refer to Section 9.2.1 for details resistor value selection. Total capacitance must be <20pF. Leave this pin Not Connected (NC) when reference clock oscillator input is driving XI.
OTHER			
RBIAS	36	I	Resistor Bias Connect a 10 kΩ (±1% tol) resistor to GND. This resistor is used for internal reference current calibration and must be a high accuracy resistor ±1% to ensure proper operation.
CMLOUT_P	78	O	Channel Monitor Loop-through Output Driver Route to a test point or a pad with 100-Ω termination resistor between pins for channel monitoring up to 6.75Gbps in FPD-Link III mode (recommended). For monitoring the received eye diagram in FPD-Link IV mode, the Eye Monitoring Tool (EOM) should be utilized for the most accurate representation of the received eye (see Section 8.3.23 for more info). Leave as open if unused.
CMLOUT_N	79		
RES0	56	--	Reserved. Must be left as No Connect.
RES1	65	--	Reserved. Must be left as No Connect.
RES2	66	--	Reserved. Must be left as No Connect.

The definitions below define the functionality of the I/O cells for each pin. TYPE:

- P = Power Supply
- GND = Ground
- eDP = Embedded DisplayPort Interface
- LVCMOS = LVCMOS pin
- I = Input
- O = Output
- I/O = Input/Output
- S = Strap Input

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	VDD18 (VDD18_D, VDD18_RX0, VDD18_RX1, VDD18_eDPPLL, VDD18_RXPLL, VDD18_TXPLL)	–0.3	2.16	V
Supply voltage	VDD11 (VDD11_eDP, VDD11_TX0, VDD11_TX1, VDD11_D, VDD11_RX0, VDD11_RX1, VDD11_eDPPLL,VDD11_TX0PLL, VDD11_TX1PLL, VDD11_CML, VDD11_RXPLL)	–0.3	1.32	V
FPD-Link IV input voltage	RIN0+, RIN0-, RIN1+, RIN1-, DOUT0+, DOUT0-, DOUT1+, DOUT1-	–0.3	1.32	V
LVCMOS IO voltage	SYNC0, SYNC1, SYNC2, ZCLK_IN, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9, GPIO10, GPIO11, GPIO12, GPIO13, XI/XO, PDB	–0.3	2.16	V
eDP Output Voltage	eDP0_0P/N, eDP0_1P/N, eDP0_2P/N, eDP0_3P/N, eDP1_0P/N, eDP1_1P/N, eDP1_2P/N, eDP1_3P/N, eDP0_AUXP/N, eDP1_AUXP/N	-0.3	1.32	V
Analog voltage	RBIAS	-0.3	2.16	V
HPD	HPD	-0.3	3.96	V
Reserved pin voltage	RES	-0.3	1.32	
Configuration input voltage	MODE_SEL0, MODE_SEL1, MODE_SEL2, IDX	–0.3	2.16	V
Open-Drain voltage	INTB_IN, I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	–0.3	3.96	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	RIN0+, RIN0-, RIN1+, RIN1+, DOUT0+, DOUT0-, DOUT1+, DOUT1+	±8	kV
			All other pins	±2	kV
		Charged device model (CDM), per AEC Q100-011		±750	V
		IEC 61000-4-2 powered-up only R_D = 330 Ω, C_S = 150 pF	Contact Discharge (RIN0+, RIN0-, RIN1+, RIN1+, DOUT0+, DOUT0-, DOUT1+, DOUT1+)	±4	kV
			Air Discharge (RIN0+, RIN0-, RIN1+, RIN1+, DOUT0+, DOUT0-, DOUT1+, DOUT1+)	±8	kV
		ISO 10605 R_D = 330 Ω, C_S = 150 pF and 330 pF R_D = 2 kΩ,C_S = 150 pF and 330 pF	Contact Discharge (RIN0+, RIN0-, RIN1+, RIN1+, DOUT0+, DOUT0-, DOUT1+, DOUT1+)	±4	kV
			Air Discharge (RIN0+, RIN0-, RIN1+, RIN1+, DOUT0+, DOUT0-, DOUT1+, DOUT1+)	±8	kV

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Recommended Operating Conditions					
Supply voltage	$V_{(VDD18)}$	1.71	1.8	1.89	V
	$V_{(VDD11)}$	1.09	1.15	1.21	
LVCMOS supply voltage	$V_{(VDD18)}$	1.71	1.8	1.89	V
Open drain voltage	INTB_IN = $V_{(INTB_IN)}$	1.71		3.6	V
I2C Supply Voltage	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1 = $V_{(I2C)}$= 1.8 V	1.71	1.8	1.89	V
I2C Supply Voltage	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1 = $V_{(I2C)}$= 3.3 V	3	3.3	3.6	V
Supply noise(1)	$V_{(VDD11)}$			25	mVpp
	$V_{(VDD18)}$			50	
	$V_{(VDDI2C)}$ = 1.8V			50	
Operating free air temperature, T_A		–40	25	105	°C
eDP/DP data rate (per eDP/DP lane)	HBR3	8.05707	8.1	8.10243	Gbps
eDP/DP data rate (per eDP/DP lane)	HBR2	5.37138	5.4	5.40162	Gbps
eDP/DP data rate (per eDP/DP lane)	HBR	2.68569	2.7	2.70081	Gbps
eDP/DP data rate (per eDP/DP lane)	RBR	1.611414	1.62	1.620486	Gbps
eDP/DP data rate (per eDP/DP lane)	R432	4.297104	4.32	4.32196	Gbps
eDP/DP data rate (per eDP/DP lane)	R324	3.222828	3.24	3.240972	Gbps
eDP/DP data rate (per eDP/DP lane)	R243	2.417121	2.43	2.430729	Gbps
eDP/DP data rate (per eDP/DP lane)	R216	2.148552	2.16	2.160648	Gbps
Local I2C frequency, f_{I2C}	Local I2C frequency Standard Mode			0.1	MHz
Local I2C frequency, f_{I2C}	Local I2C frequency Fast Mode			0.4	
Local I2C frequency, f_{I2C}	Local I2C frequency Fast Plus Mode			1	
Local I2C frequency, f_{I2C}	Local I2C frequency High-Speed Mode			3.4	MHz

(1) DC - 50 MHz

7.4 Thermal Information

THERMAL METRIC(1)		DS90Ux984-Q1 QFN 88 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard)	18.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W

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THERMAL METRIC[1]		DS90Ux984-Q1 QFN 88 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	4.9	°C/W

(1) Thermal data in accordance with JESD51. For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 DC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
TOTAL POWER CONSUMPTION							
P_{T-1}	Total Power Consumption	Dual FPD-Link IV input (13.5 Gbps), 2 x eDP output 4 lanes each at HBR3 8.1 Gbps, dual FPD-Link IV daisy-chain output (6.75 Gbps)	VDD11 [1], VDD18 [2]			2.947	W
$I_{DD-18T-1}$	1.8 V Total Supply Current		VDD18			331	mA
I_{DD-18_RX0-1}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			140	mA
$I_{DD-18_RXPLL-1}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			3	mA
I_{DD-18_RX1-1}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			140	mA
$I_{DD-18_TXPLL-1}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			19	mA
I_{DD-18_D-1}	1.8 V Supply Current for VDD18_D		VDD18_D			23	mA
$I_{DD-18_eDPPLL-1}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-1}$	1.15 V Total supply current		VDD11			1918	mA
I_{DD-11_RX0-1}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			220	mA
$I_{DD-11_RXPLL-1}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			90	mA
I_{DD-11_CML-1}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-1}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			220	mA
I_{DD-11_eDP-1}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			535	mA
$I_{DD-11_eDPPLL-1}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-1}	1.15 V Supply Current for VDD11_D		VDD11_D			509	mA
$I_{DD-11_TX1PLL-1}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			73	mA
$I_{DD-11_TX0PLL-1}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			73	mA
I_{DD-11_TX1-1}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			68	mA
I_{DD-11_TX0-1}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			68	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-5}	Total Power Consumption	Dual FPD-Link IV input (13.5 Gbps), 2 x eDP output 4 lanes each at R432 4.32Gbps, dual FPD-Link III daisy-chain output (3.675 Gbps)	VDD11 (1), VDD18 (2)			2.7	W
$I_{DD-18T-5}$	1.8 V Total Supply Current		VDD18			331	mA
I_{DD-18_RX0-5}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			140	mA
$I_{DD-18_RXPLL-5}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			3	mA
I_{DD-18_RX1-5}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			140	mA
$I_{DD-18_TXPLL-5}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			19	mA
I_{DD-18_D-5}	1.8 V Supply Current for VDD18_D		VDD18_D			23	mA
$I_{DD-18_eDPPLL-5}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-5}$	1.15 V Total supply current		VDD11			1714	mA
I_{DD-11_RX0-5}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			220	mA
$I_{DD-11_RXPLL-5}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			90	mA
I_{DD-11_CML-5}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-5}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			220	mA
I_{DD-11_eDP-5}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			447	mA
$I_{DD-11_eDPPLL-5}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-5}	1.15 V Supply Current for VDD11_D		VDD11_D			449	mA
$I_{DD-11_TX1PLL-5}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			61	mA
$I_{DD-11_TX0PLL-5}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			61	mA
I_{DD-11_TX1-5}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			52	mA
I_{DD-11_TX0-5}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			52	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-6}	Total Power Consumption	Dual FPD-Link IV input (13.5 Gbps), 2 x eDP output 4 lanes each at R432 4.32Gbps, no daisy-chain output	VDD11 (1), VDD18 (2)			2.35	W
$I_{DD-18T-6}$	1.8 V Total Supply Current		VDD18			309	mA
I_{DD-18_RX0-6}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			140	mA
$I_{DD-18_RXPLL-6}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			2	mA
I_{DD-18_RX1-6}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			140	mA
$I_{DD-18_TXPLL-6}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			4	mA
I_{DD-18_D-6}	1.8 V Supply Current for VDD18_D		VDD18_D			17	mA
$I_{DD-18_eDPPLL-6}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-6}$	1.15 V Total supply current		VDD11			1459	mA
I_{DD-11_RX0-6}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			220	mA
$I_{DD-11_RXPLL-6}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			90	mA
I_{DD-11_CML-6}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-6}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			220	mA
I_{DD-11_eDP-6}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			427	mA
$I_{DD-11_eDPPLL-6}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-6}	1.15 V Supply Current for VDD11_D		VDD11_D			402	mA
$I_{DD-11_TX1PLL-6}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			13	mA
$I_{DD-11_TX0PLL-6}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			13	mA
I_{DD-11_TX1-6}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			6	mA
I_{DD-11_TX0-6}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			6	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-8}	Total Power Consumption	Dual FPD-Link IV input (13.5 Gbps), 1 x eDP output 4 lanes each at 8.1Gbps, dual FPD-Link III daisy-chain output (3.675 Gbps)	VDD11 (1), VDD18 (2)			2.646	W
$I_{DD-18T-8}$	1.8 V Total Supply Current		VDD18			332	mA
I_{DD-18_RX0-8}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			140	mA
$I_{DD-18_RXPLL-8}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			3	mA
I_{DD-18_RX1-8}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			140	mA
$I_{DD-18_TXPLL-8}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			19	mA
I_{DD-18_D-8}	1.8 V Supply Current for VDD18_D		VDD18_D			24	mA
$I_{DD-18_eDPPLL-8}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-8}$	1.15 V Total supply current		VDD11			1668	mA
I_{DD-11_RX0-8}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			220	mA
$I_{DD-11_RXPLL-8}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			90	mA
I_{DD-11_CML-8}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-8}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			220	mA
I_{DD-11_eDP-8}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			425	mA
$I_{DD-11_eDPPLL-8}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-8}	1.15 V Supply Current for VDD11_D		VDD11_D			435	mA
$I_{DD-11_TX1PLL-8}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			58	mA
$I_{DD-11_TX0PLL-8}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			58	mA
I_{DD-11_TX1-8}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			50	mA
I_{DD-11_TX0-8}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			50	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-9}	Total Power Consumption	Dual FPD-Link IV input (13.5 Gbps), 1 x eDP output 4 lanes each at 8.1Gbps, no daisy-chain output	VDD11 (1), VDD18 (2)			2.392	W
$I_{DD-18T-9}$	1.8 V Total Supply Current		VDD18			310	mA
I_{DD-18_RX0-9}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			140	mA
$I_{DD-18_RXPLL-9}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			2	mA
I_{DD-18_RX1-9}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			140	mA
$I_{DD-18_TXPLL-9}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			4	mA
I_{DD-18_D-9}	1.8 V Supply Current for VDD18_D		VDD18_D			18	mA
$I_{DD-18_eDPPLL-9}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-9}$	1.15 V Total supply current		VDD11			1492	mA
I_{DD-11_RX0-9}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			220	mA
$I_{DD-11_RXPLL-9}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			90	mA
I_{DD-11_CML-9}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-9}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			220	mA
I_{DD-11_eDP-9}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			426	mA
$I_{DD-11_eDPPLL-9}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-9}	1.15 V Supply Current for VDD11_D		VDD11_D			410	mA
$I_{DD-11_TX1PLL-9}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			12	mA
$I_{DD-11_TX0PLL-9}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			12	mA
I_{DD-11_TX1-9}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			15	mA
I_{DD-11_TX0-9}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			15	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-12}	Total Power Consumption	Single FPD-Link IV input (13.5 Gbps) , 1 x eDP output 4 lanes each at R432 4.32Gbps, no daisy-chain output	VDD11 (1), VDD18 (2)			2.041	W
$I_{DD-18T-12}$	1.8 V Total Supply Current		VDD18			310	mA
I_{DD-18_RX0-12}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			140	mA
$I_{DD-18_RXPLL-12}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			2	mA
I_{DD-18_RX1-12}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			140	mA
$I_{DD-18_TXPLL-12}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			4	mA
I_{DD-18_D-12}	1.8 V Supply Current for VDD18_D		VDD18_D			18	mA
$I_{DD-18_eDPPLL-12}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-12}$	1.15 V Total supply current		VDD11			1202	mA
I_{DD-11_RX0-12}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			189	mA
$I_{DD-11_RXPLL-12}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			78	mA
I_{DD-11_CML-12}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-12}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			183	mA
I_{DD-11_eDP-12}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			317	mA
$I_{DD-11_eDPPLL-12}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-12}	1.15 V Supply Current for VDD11_D		VDD11_D			326	mA
$I_{DD-11_TX1PLL-12}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			11	mA
$I_{DD-11_TX0PLL-12}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			10	mA
I_{DD-11_TX1-12}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			13	mA
I_{DD-11_TX0-12}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			13	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-13}	Total Power Consumption	Dual FPD-Link III input (3.675 Gbps), 2 x eDP output 4 lanes each at RBR 1.62Gbps, no daisy-chain output	VDD11 (1), VDD18 (2)			1.625	W
$I_{DD-18T-13}$	1.8 V Total Supply Current		VDD18			279	mA
I_{DD-18_RX0-13}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			125	mA
$I_{DD-18_RXPLL-13}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			2	mA
I_{DD-18_RX1-13}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			125	mA
$I_{DD-18_TXPLL-13}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			4	mA
I_{DD-18_D-13}	1.8 V Supply Current for VDD18_D		VDD18_D			17	mA
$I_{DD-18_eDPPLL-13}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-13}$	1.15 V Total supply current		VDD11			907	mA
I_{DD-11_RX0-13}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			104	mA
$I_{DD-11_RXPLL-13}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			90	mA
I_{DD-11_CML-13}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-13}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			104	mA
I_{DD-11_eDP-13}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			233	mA
$I_{DD-11_eDPPLL-13}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-13}	1.15 V Supply Current for VDD11_D		VDD11_D			254	mA
$I_{DD-11_TX1PLL-13}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			13	mA
$I_{DD-11_TX0PLL-13}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			13	mA
I_{DD-11_TX1-13}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			17	mA
I_{DD-11_TX0-13}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			17	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-14}	Total Power Consumption	Single FPD-Link III input (3.675 Gbps), 1 x eDP output 4 lanes each at RBR 1.62Gbps, no daisy-chain output	VDD11 (1), VDD18 (2)			1.593	W
$I_{DD-18T-14}$	1.8 V Total Supply Current		VDD18			279	mA
I_{DD-18_RX0-14}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			125	mA
$I_{DD-18_RXPLL-14}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			2	mA
I_{DD-18_RX1-14}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			125	mA
$I_{DD-18_TXPLL-14}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			4	mA
I_{DD-18_D-14}	1.8 V Supply Current for VDD18_D		VDD18_D			17	mA
$I_{DD-18_eDPPLL-14}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-14}$	1.15 V Total supply current		VDD11			880	mA
I_{DD-11_RX0-14}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			104	mA
$I_{DD-11_RXPLL-14}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			90	mA
I_{DD-11_CML-14}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-14}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			104	mA
I_{DD-11_eDP-14}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			216	mA
$I_{DD-11_eDPPLL-14}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-14}	1.15 V Supply Current for VDD11_D		VDD11_D			244	mA
$I_{DD-11_TX1PLL-14}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			13	mA
$I_{DD-11_TX0PLL-14}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			13	mA
I_{DD-11_TX1-14}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			17	mA
I_{DD-11_TX0-14}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			17	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-17}	Total Power Consumption	Dual FPD-Link IV input (6.75 Gbps), 2 x eDP output 4 lanes each at R216 2.16Gbps, dual FPD-Link IV daisy-chain output (6.75 Gbps)	VDD11 (1), VDD18 (2)			2.367	W
$I_{DD-18T-17}$	1.8 V Total Supply Current		VDD18			331	mA
I_{DD-18_RX0-17}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			140	mA
$I_{DD-18_RXPLL-17}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			3	mA
I_{DD-18_RX1-17}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			140	mA
$I_{DD-18_TXPLL-17}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			19	mA
I_{DD-18_D-17}	1.8 V Supply Current for VDD18_D		VDD18_D			23	mA
$I_{DD-18_eDPPLL-17}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-17}$	1.15 V Total supply current		VDD11			1439	mA
I_{DD-11_RX0-17}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			167	mA
$I_{DD-11_RXPLL-17}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			78	mA
I_{DD-11_CML-17}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-17}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			167	mA
I_{DD-11_eDP-17}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			317	mA
$I_{DD-11_eDPPLL-17}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-17}	1.15 V Supply Current for VDD11_D		VDD11_D			366	mA
$I_{DD-11_TX1PLL-17}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			73	mA
$I_{DD-11_TX0PLL-17}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			73	mA
I_{DD-11_TX1-17}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			68	mA
I_{DD-11_TX0-17}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			68	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
P_{T-18}	Total Power Consumption	Dual FPD-Link IV input (3.375 Gbps), 2 x eDP output 4 lanes each at RBR 1.62Gbps, dual FPD-Link IV daisy-chain output (3.375 Gbps)	VDD11 (1), VDD18 (2)			2.26	W
$I_{DD-18T-18}$	1.8 V Total Supply Current		VDD18			331	mA
I_{DD-18_RX0-18}	1.8 V Supply Current for VDD18_RX0		VDD18_RX0			140	mA
$I_{DD-18_RXPLL-18}$	1.8 V Supply Current for VDD18_RXPLL		VDD18_RXPLL			3	mA
I_{DD-18_RX1-18}	1.8 V Supply Current for VDD18_RX1		VDD18_RX1			140	mA
$I_{DD-18_TXPLL-18}$	1.8 V Supply Current for VDD18_TXPLL		VDD18_TXPLL			19	mA
I_{DD-18_D-18}	1.8 V Supply Current for VDD18_D		VDD18_D			23	mA
$I_{DD-18_eDPPLL-18}$	1.8 V Supply Current for VDD18_eDPPLL		VDD18_eDPPLL			6	mA
$I_{DD-11T-18}$	1.15 V Total supply current		VDD11			1350	mA
I_{DD-11_RX0-18}	1.15 V Supply Current for VDD11_RX0		VDD11_RX0			159	mA
$I_{DD-11_RXPLL-18}$	1.15 V Supply Current for VDD11_RXPLL		VDD11_RXPLL			78	mA
I_{DD-11_CML-18}	1.15 V Supply Current for VDD11_CML		VDD11_CML			2	mA
I_{DD-11_RX1-18}	1.15 V Supply Current for VDD11_RX1		VDD11_RX1			159	mA
I_{DD-11_eDP-18}	1.15 V Supply Current for VDD11_eDP		VDD11_eDP			296	mA
$I_{DD-11_eDPPLL-18}$	1.15 V Supply Current for VDD11_eDPPLL		VDD11_eDPPLL			60	mA
I_{DD-11_D-18}	1.15 V Supply Current for VDD11_D		VDD11_D			344	mA
$I_{DD-11_TX1PLL-18}$	1.15 V Supply Current for VDD11_TX1PLL		VDD11_TX1PLL			73	mA
$I_{DD-11_TX0PLL-18}$	1.15 V Supply Current for VDD11_TX0PLL		VDD11_TX0PLL			73	mA
I_{DD-11_TX1-18}	1.15 V Supply Current for VDD11_TX1		VDD11_TX1			53	mA
I_{DD-11_TX0-18}	1.15 V Supply Current for VDD11_TX0		VDD11_TX0			53	mA
P_Z	Total Power Consumption, Power Down Mode	PDB = LOW	VDD11 (1), VDD18 (2)			0.296	W
I_{DD-18Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD18			6	mA
I_{DD-18Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD18_RX0			1	mA
I_{DD-18Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD18_RXPLL			1	mA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{DD-18Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD18_RX1			1	mA
I_{DD-18Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD18_TXPLL			1	mA
I_{DD-18Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD18_D			1	mA
I_{DD-18Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD18_eDPPLL			1	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11			235	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_RX0			4	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_RXPLL			9	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_CML			2	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_RX1			13	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_eDP			81	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_eDPPLL			17	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_D			81	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_TX1PLL			9	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_TX0PLL			9	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_TX1			5	mA
I_{DD-11Z}	Deserializer supply current, Power Down Mode	PDB= LOW	VDD11_TX0			5	mA
1.8 V LVCMOS I/O							

7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V_{IH}	High-level Input Voltage	$V_{(VDD18)}$ = 1.71 V to 1.89 V	SYNC0, SYNC1, SYNC2, ZCLK_IN, GPIO[13:0], PDB	0.65 × VDD18		VDD18	V
V_{IL}	Low-level Input Voltage	$V_{(VDD18)}$ = 1.71 V to 1.89 V		0		0.35 × VDD18	V
I_{IH}	Input high current	V_{IN} = $V_{(VDDIO)}$ = 1.71 V to 1.89 V, Internal pulldown enabled			0	100	µA
		V_{IN} = $V_{(VDDIO)}$ = 1.71 V to 1.89 V, Internal pulldown disabled			0	25	µA
I_{IL}	Input Low Current	V_{IN} = 0V		–25	0		µA
V_{OH}	High-level Output Voltage	I_{OH} = -4mA	SYNC0, SYNC1, SYNC2, GPIO[13:0]	VDD18 – 0.45		VDD18	V
V_{OL}	Low-level Output Voltage	I_{OL} = +4mA		0		0.45	V
I_{OS}	Output short circuit current	V_{OUT} = 0 V			–25		mA
I_{IN_STRAP}	Strap pin input current	V_{IN} = 0 v to $V_{(VDD18)}$	MODE_SEL0, MODE_SEL1, MODE_SEL2, IDX	–2		2	µA
I_{OZ}	TRI-STATE output current	V_{OUT} = 0 V or $V_{(VDD18)}$, PDB = L, pull-down resistor enabled	SYNC0, SYNC1, SYNC2, GPIO[13:0]	–100		100	µA
FPD-LINK IV DC SPECIFICATIONS							
$\|V_{OUT}\|$	Single-Ended Output Amplitude		DOUT0+, DOUT0–, DOUT1+, DOUT1–	470	575	670	mV
$\|V_{OD}\|$	Differential Output Amplitude			940	1150	1340	mVpp
ΔV_{OD}	Output Differential Voltage Unbalance	R_L=100 Ω across DOUT+, DOUT-			1	50	mV
V_{OS}	Output Offset Voltage	R_L=100 Ω across DOUT+, DOUT-			VDD11/2		V
ΔV_{OS}	Offset Voltage Mismatch	R_L=100 Ω across DOUT+, DOUT-			1	50	mV
ΔV_{CM}	Common Mode Noise	(DOUT+) + (DOUT-)				20	mV
I_{OS}	Output Short Current	DOUT = 0V			–20		mA
V_{IN}	Input single-ended voltage		RIN0+, RIN0-, RIN1+, RIN1-		50		mV
V_{ID}	Input differential voltage		RIN0+, RIN0-, RIN1+, RIN1-		100		mV
V_{CM}	Common Mode Voltage	PDB = H	RIN0+, RIN0-, RIN1+, RIN1-		0.56		V
R_{T_IN}	Single-Ended Internal Termination	Single-ended RIN+ or RIN-	RIN0+, RIN0-, RIN1+, RIN1-	40	50	60	Ω
	Differential Internal Termination	Differential across RIN+ and RIN-		80	100	120	Ω
R_{T_OUT}	Single-Ended Internal Termination	Single-ended RIN+ or RIN-	DOUT0+, DOUT0–, DOUT1+, DOUT1–, CMLOUT_P, CMLOUT_N	40	50	60	Ω
	Differential Internal Termination	Differential across RIN+ and RIN-		80	100	120	Ω

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V_{IN-BC}	Single-ended back channel input amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate= 168.75, 156.6 Mbps. (FPD-Link IV mode)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	110			mV
V_{ID-BC}	Differential back channel input amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate= 168.75, 156.6 Mbps. (FPD-Link IV mode)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	220			mVpp
V_{IN-BC}	Single-ended back channel input amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate = 5, 10, 20 Mbps (FPD-Link III)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	130			mV
V_{ID-BC}	Differential back channel input amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate = 5, 10, 20 Mbps (FPD-Link III)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	260			mVpp
V_{OUT-BC}	Back channel launch amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate= 168.75, 156.6 Mbps. (FPD-Link IV mode)	RIN0+, RIN0-, RIN1+, RIN1-	127.5			mV
V_{OUT-BC}	Back channel launch amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate= 168.75, 156.6 Mbps. (FPD-Link IV mode)		255			mVpp
V_{OUT-BC}	Back channel launch amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate = 5, 10, 20 Mbps (FPD-Link III)	RIN0+, RIN0-, RIN1+, RIN1-	195			mV
V_{OUT-BC}	Back channel launch amplitude	R_L = 50 Ω Single-ended configuration. Back channel rate = 5, 10, 20 Mbps (FPD-Link III)	RIN0+, RIN0-, RIN1+, RIN1-	390			mVpp
C_{IN}	Input capacitance		RIN0+, RIN0-, RIN1+, RIN1-			880	fF
Open-Drain Input							
V_{IL}	Input low-level		INTB_IN	GND		0.3 × $V_{(INTB_IN)}$	V
V_{IH}	Input high-level		INTB_IN	0.7 × $V_{(INTB_IN)}$		$V_{(INTB_IN)}$	V
I_{IL}	Input low current	V_{IN} = 0V	INTB_IN	-40		40	µA
I_{IH}	Input high current	V_{IN} = $V_{(INTB_IN)}$	INTB_IN	-40		40	µA
SERIAL CONTROL BUS[3]							
V_{IL}	Input low-level	Standard/Fast/Fast Plus Mode	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	GND		0.3 × $V_{(I2C)}$	V
V_{IH}	Input high-level	Standard/Fast/Fast Plus Mode		0.7 × $V_{(I2C)}$		$V_{(I2C)}$	V
V_{HYS}	Input hysteresis	Standard/Fast/Fast Plus Mode			70		mV
V_{OL1}	Output low-level	Standard-mode/Fast-mode, I_{OL} = 3 mA, $V_{(I2C)}$ = 3.0 V to 3.6 V	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	0		0.4	V
		Fast-mode Plus, I_{OL} = 20 mA		0		0.4	V
V_{OL2}	Output low-level	Standard-mode/Fast-mode I_{OL} = 3 mA, $V_{(I2C)}$ = 1.71 V to 1.89 V	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	0		0.2 x $V_{(I2C)}$	V

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
I_{IL}	Input low current	V_{IN} = 0V	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	-65	0		µA
I_{IH}	Input high current	V_{IN} = $V_{(I2C)}$	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1		0	65	µA
I_{OL}	Output low-level current	Standard/Fast Mode, V_{OL} = 0.2 x $V_{(I2C)}$, $V_{(I2C)}$ = 1.71 V to 1.89 V	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	3			mA
I_{OL}	Output low-level current	Standard/Fast Mode, V_{OL} = 0.4, $V_{(I2C)}$ = 3.0 V to 3.6 V	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	3			mA
I_{OL}	Output low-level current	Fast Plus Mode	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	20			mA
C_{IN}	Input capacitance		I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1		5		pF
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	0.1 × $V_{(I2C)}$			V
V_{nH}	Noise margin at the HIGH level	For each connected device (including hysteresis)	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	0.2 × $V_{(I2C)}$			V
SERIAL CONTROL BUS HIGH SPEED MODE							
V_{IL}	Input low-level	High-Speed Mode	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	GND		0.3 × $V_{(I2C)}$	V
V_{IH}	Input high-level	High-Speed Mode	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	0.7 × $V_{(I2C)}$		$V_{(I2C)}$ + 0.5	V
V_{HYS}	Input hysteresis	High-Speed Mode	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1		70		mV
V_{OL}	Output low-level	High-Speed Mode, I_{OL} = 3 mA, $V_{(I2C)}$ = 1.71 V to 1.89 V	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	0		0.2 x $V_{(I2C)}$	V
I_{IL}	Input low current	V_{IN} = 0V	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	-65	0		µA
I_{IH}	Input high current	V_{IN} = $V_{(I2C)}$	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1		0	65	µA

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7.5 DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance		I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1		5		pF
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	0.1 × $V_{(I2C)}$			V
V_{nH}	Noise margin at the HIGH level	For each connected device (including hysteresis)	I2C_SDA0, I2C_SCL0, I2C_SDA1, I2C_SCL1	0.2 × $V_{(I2C)}$			V
Voltage and Temperature Sensing							
V_{ACC}	Voltage sensor accuracy			-2.5	±0.5	+2.5	%
T_{ACC}	Temperature sensor accuracy	-40 to 150 °C junction		-5.5	±2.5	+5.5	°C

(1) VDD11 = 1.15 V for typical, and 1.21 V for max
(2) VDD18 = 1.8 V for typical, and 1.89 V for max
(3) $V_{(VDDI2C)}$ = 1.8 V ± 5% OR 3.3 V ± 10%

7.6 AC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LVCMOS I/O							
$t_{r_INTB_IN}$	Rise time for INTB_IN	V_{INTB_IN} = 3.3 V	INTB_IN	100			ns
$t_{r_INTB_IN}$	Rise time for INTB_IN	V_{INTB_IN} = 1.8 V	INTB_IN	50			ns
t_{CLH}	LVCMOS low-to-high transition-time	C_L = 8 pF (lumped load) Default Registers	SYNC0, SYNC1, SYNC2, ZCLK_IN, GPIO[13:0]		2		ns
t_{CHL}	LVCMOS high-to-low transition-time	C_L = 8 pF (lumped load) Default Registers			2		ns
t_{PDB}	PDB reset pulse width	Voltage supplies applied and stable	PDB	2			ms
FPD-Link IV AC SPECIFICATIONS OUTPUT							
t_{DDLT}	Deserializer data lock time		RIN0±, RIN1±			20	ms
f_{FC}	Forward channel data rate	98x	RIN0±, RIN1±		13.5		Gbps
f_{FC}	Forward channel data rate	98x	RIN0±, RIN1±		12.528		Gbps
f_{FC}	Forward channel data rate	98x	RIN0±, RIN1±		10.8		Gbps
f_{FC}	Forward channel data rate	98x	RIN0±, RIN1±, DOUT0±, DOUT1±		6.75		Gbps
f_{FC}	Forward channel data rate	98x	RIN0±, RIN1±, DOUT0±, DOUT1±		3.375		Gbps
f_{FC}	Forward channel data rate	94x, FPD-Link III	RIN0±, RIN1±, DOUT0±, DOUT1±		3.675		Gbps
f_{BC}	Back channel data rate	98x, Forward Channel rate = 13.5 Gbps, 10.8 Gbps, 6.75 Gbps or 3.375 Gbps	RIN0±, RIN1±, DOUT0±, DOUT1±		168.75		Mbps
		94x			20		Mbps
					10		Mbps
					5		Mbps

7.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
f_{BC}	Back channel data rate	98x, Forward Channel rate = 12.528 Gbps	RIN0±, RIN1±		156.6		Mbps
$t_{JIT_BC_OUT}$	Back Channel Output Jitter	FPD-Link	RIN0±, RIN1±			0.1	UI_{BC}
$f_{DEV_DOWN-BC}$	Back Channel Spread Spectrum Clocking Generation Deviation Frequency Magnitude	Down Spread (-0.25%)	RIN0±, RIN1±, DOUT0±, DOUT1±			0.25	%
$f_{DEV_DOWN-FC}$	Forward Channel Spread Spectrum Clocking Generation Deviation Frequency Magnitude	Down Spread (-0.25%)	RIN0±, RIN1±, DOUT0±, DOUT1±			0.25	%
$f_{DEV_CENTER_SUM}$	Spread Spectrum Clocking Generation Deviation Frequency Magnitude Sum on Forward Channel and Back Channel	Foward Channel + Back Channel Center Spread (+/-0.25%)	RIN0±, RIN1±, DOUT0±, DOUT1±			0.5	%
$f_{DEV_CENTER_HALF}$	Back Channel or Forward Channel Spread Spectrum Clocking Generation Deviation Frequency Magnitude	Center Spread (+/-0.25%) (SSCG only applied to foward channel or to back channel)	RIN0±, RIN1±, DOUT0±, DOUT1±			0.5	%
f_{MOD}	Spread Spectrum Clocking Generation Modulation Frequency		RIN0±, RIN1±, DOUT0±, DOUT1±	30		33	kHz
t_{JIT}	Output Total Jitter - 13.5 Gbps	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.35	UI_{FC}
t_{JIT}	Output Total Jitter - 12.528 Gbps	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.35	UI_{FC}
t_{JIT}	Output Total Jitter - 10.8 Gbps FPD-Link IV	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.3	UI_{FC}
t_{JIT}	Output Total Jitter - 6.75 Gbps FPD-Link IV	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.25	UI_{FC}
t_{JIT}	Output Total Jitter - 3.375 Gbps FPD-Link IV	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.25	UI_{FC}
t_{JIT}	Output Total Jitter - 3.675 Gbps FPD-Link III	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–			0.25	UI_{FC}
t_{RF}	Forward Channel Rise/Fall Time	20% to 80%			30		ps
E_{FCH}	Output Eye Height - 13.5 Gbps	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	225			mVpp
E_{FCH}	Output Eye Height - 12.528 Gbps	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	260			mVpp
E_{FCH}	Output Eye Height - 10.8 Gbps NRZ FPD-Link IV	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	335			mVpp
E_{FCH}	Output Eye Height - 6.75 Gbps FPD-Link IV	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	510			mVpp
E_{FCH}	Output Eye Height - 3.375 Gbps FPD-Link IV	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	640			mVpp

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7.6 AC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
E_{FCH}	Output Eye Height - 3.675 Gbps FPD-Link III	R_L = 100 Ω. Measured with Type 2 CDR with JTF of 4 MHz, BER rate 10^{-12}, PRBS15. (1)	DOUT0+, DOUT0–, DOUT1+, DOUT1–	455			mVpp
S_{11}	Return Loss of RX	f_{FCMAX} = 1.6875 - 6.75 GHz (FPD-Link IV)	RIN0±, RIN1±		-15		dB
S_{11}	Return Loss of TX	f_{BCMIN} = 84.375MHz	DOUT0±, DOUT1±		–28		dB

(1) Measurement includes PCB and recommended external components

7.7 eDP/DP Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
eDP/DP AUX TX PARAMETERS						
UI_{MAN}	Manchester transaction unit interval		0.4		0.6	us
$PULSE_{PRECHG}$	Number of pre-charge pulses				16	pulses
$PULSE_{SYNC_PREAM}$	Number of Pulses in SYNC Preamble (DP mode)			16		pulses
$PULSE_{SYNC_PREAM}$	Number of Pulses in SYNC Preamble (eDP mode)			8		pulses
$T_{AUX\text{-}BUS\text{-}PARK}$	AUX CH bus park time		10			ns
$T_{CYCLE\text{-}CYCLE_JIT}$	Max allowable UI variation within a single transaction at connector pins of a transmitting device				0.08	UI
	Max allowable variation for adjacent bit times within a single transaction at connector pins of a transmitting device				0.04	UI
$T_{CYCLE\text{-}CYCLE_JIT}$	Max allowable UI variation within a single transaction at connector pins of a receiving device				0.10	UI
$T_{CYCLE\text{-}CYCLE_JIT}$	Max allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device				0.05	UI
$V_{AUX\text{-}DIFFp\text{-}p_TX}$	DP mode AUX peak-to-peak voltage from Main-Link Source/Sink when transmitting		0.29	0.40	1.38	V
$V_{AUX\text{-}DIFFp\text{-}p_RX}$	DP mode AUX peak-to-peak voltage received by Main-Link Source, TP2		0.27		1.36	V
$V_{AUX\text{-}DIFFp\text{-}p_TX}$	eDP mode AUX peak-to-peak voltage from Main-Link Source when transmitting		0.18	0.2	1.38	V
$V_{AUX\text{-}TERM_R}$	AUX CH termination DC resistance			100		Ω
$V_{AUX\text{-}DC\text{-}CM}$	DP mode AUX DC common mode voltage		0		2.0	V
$V_{AUX\text{-}DC\text{-}CM}$	eDP mode AUX DC common mode voltage		0		1.2	V
$V_{AUX\text{-}TURN\text{-}CM}$	AUX turn around common mode voltage				0.3	V
I_{AUX_SHORT}	AUX short circuit current limit				90	mA
C_{AUX}	AUX AC-coupling capacitor		75		200	nF
$SR_{AUX_20\text{-}80}$	AUX slew rate, 20% to 80%				375	mV/ns
R_{AUX_SRC}	AUX biasing resistor at DP Source device		10	100	105	kΩ

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7.7 eDP/DP Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
eDP/DP HOT PLUG DETECTION PARAMETERS						
$V_{TH_HPD_1V8}$	Hot Plug Detection Threshold for 1.8V HPD		1.23			V
	Hot Unplug Detection Threshold for 1.8V HPD				0.59	V
$V_{TH_HPD_3V3}$	Hot Plug Detection Threshold for 3.3V HPD		2			V
	Hot Unplug Detection Threshold for 3.3V HPD				0.8	V
R_{t_HPD}	HPD Upstream device termination		100			kΩ
PW_{IRQ}	IRQ_HPD Pulse Width driven by down stream device		0.5		1	ms
PW_{glitch}	IRQ_HPD Pulse Glitch Detection threshold for upstream device		0.25			ms
PW_{IRQ_UNPLUG}	IRQ_HPD Pulse/Hot Unplug Event Detection threshold for upstream device		2			ms
t_{IRQ_MIN}	IRQ_HPD Minimum Spacing	Min time after asserting HPD at the end of IRQ_HPD before de–asserting HPD at the start of the following IRQ_HPD	2			ms
eDP/DP MAIN LINK TX SYSTEM PARAMETERS						
f_{HBR3}	eDP/DP data rate (per eDP/DP lane) HBR3	@ +300ppm/ -5300ppm	8.05707	8.1	8.10243	Gbps
f_{HBR2}	eDP/DP data rate (per eDP/DP lane) HBR2	@ +300ppm/ -5300ppm	5.37138	5.4	5.40162	Gbps
f_{HBR}	eDP/DP data rate (per eDP/DP lane) HBR	@ +300ppm/ -5300ppm	2.68569	2.7	2.70081	Gbps
f_{RBR}	eDP/DP data rate (per eDP/DP lane) RBR	@ +300ppm/ -5300ppm	1.611414	1.62	1.620486	Gbps
f_{R432}	eDP data rate (per eDP lane)	@ +300ppm/ -5300ppm	4.297104	4.32	4.32196	Gbps
f_{R324}		@ +300ppm/ -5300ppm	3.222828	3.24	3.240972	Gbps
f_{R243}		@ +300ppm/ -5300ppm	2.417121	2.43	2.430729	Gbps
f_{R216}		@ +300ppm/ -5300ppm	2.148552	2.16	2.160648	Gbps
Down_Spread_Amplitude	Link clock down-spreading		0		0.5	%
Down_Spread_Frequency	Link clock down-spreading frequency		30		33	kHz
C_{TX}	AC-coupling Capacitor		75		265	nF
eDP/DP MAIN LINK TX TP2 PARAMETERS						
V_{HBR_EYE}	DP Mode HBR Upstream Eye Voltage Swing	Time = 0.21 UI	0			mV
		Time = 0.355 UI	280			mV
		Time = 0.50 UI	350			mV
		Time = 0.645 UI	350			mV
		Time = 0.790 UI	0			mV

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7.7 eDP/DP Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RBR_EYE}	DP Mode RBR Upstream Eye Voltage Swing	Time = 0.127 UI	0			mV
		Time = 0.291 UI	320			mV
		Time = 0.500 UI	400			mV
		Time = 0.709 UI	400			mV
		Time = 0.873 UI	0			mV
$V_{TX_OUTPUT_LEVEL0_RATIO_HBR2_HBR3}$	Ratio of Voltage Swing VSL[1] / VSL[0]	HBR3/HBR2	1.6		4.5	dB
$V_{TX_OUTPUT_LEVEL0_RATIO_HBR2_HBR3}$	Ratio of Voltage Swing VSL[2] / VSL[0]	HBR3/HBR2	3.2		7	dB
$V_{TX_OUTPUT_LEVEL0_RATIO_HBR2_HBR3}$	Ratio of Voltage Swing VSL[3] / VSL[0]	HBR3/HBR2	4.8		10.5	dB
$V_{TX_OUTPUT_RATIO_HBR2_HBR3}$	Ratio of Voltage Swing VSL[1] / VSL[0]	HBR3/HBR2	1.6			dB
$V_{TX_OUTPUT_RATIO_HBR2_HBR3}$	Ratio of Voltage Swing VSL[2] / VSL[1]	HBR3/HBR2	1.1			dB
$V_{TX_OUTPUT_RATIO_HBR2_HBR3}$	Ratio of Voltage Swing VSL[3] / VSL[2]	HBR3/HBR2	1.1			dB
$V_{TX_MEQ_LEVEL0_DELTA_HBR2_HBR3}$	Delta of TX Emphasis TX_EQL[1] / TX_EQL[0]	HBR3/HBR2	1.3		4	dB
$V_{TX_MEQ_LEVEL0_DELTA_HBR2_HBR3}$	Delta of TX Emphasis TX_EQL[2] / TX_EQL[0]	HBR3/HBR2	2.4		6	dB
$V_{TX_MEQ_LEVEL0_DELTA_HBR2_HBR3}$	Delta of TX Emphasis TX_EQL[3] / TX_EQL[0]	HBR3/HBR2	3.5		8	dB
$V_{TX_MEQ_DELTA_HBR2_HBR3}$	Delta of TX Emphasis TX_EQL[1] / TX_EQL[0]	HBR3/HBR2	1.3			dB
$V_{TX_MEQ_DELTA_HBR2_HBR3}$	Delta of TX Emphasis TX_EQL[2] / TX_EQL[1]	HBR3/HBR2	0.7			dB
$V_{TX_MEQ_DELTA_HBR2_HBR3}$	Delta of TX Emphasis TX_EQL[3] / TX_EQL[2]	HBR3/HBR2	0.7			dB
$V_{TX_PE_RATIO_HBR2_HBR3}$	Ratio of PE[N] / TX_MEQ[N]	HBR3/HBR2	2/3			Ratio
$V_{TX_TRANSITION_BIT_OUTPUT_RATIO_PEL[N] / PEL[N – 1]_HBR2_HBR3}$	Transition Bit Amplitude Ratio between TX_EQL[N] and TX_EQL[N – 1] for a Given VSL[M]	HBR3/HBR2	0			dB
$V_{TX\text{-}OUTPUT\text{-}RATIO_RBR_HBR}$	Ratio of output voltage level 1/level 0	HBR/RBR	0.8		6	dB
	Ratio of output voltage level 2/level 1	HBR/RBR	0.1		5.1	dB
	Ratio of output voltage level 3/level 2	HBR/RBR	0.8		6	dB
$V_{TX\text{-}PREEMP\text{-}OFF}$	Maximum Pre-emphasis when disabled	HBR/RBR			0.25	dB
$V_{TX\text{-}PREEMP\text{-}DELTA}$	Delta of Pre-emphasis Level 1 vs Level 0	HBR/RBR	2			dB
	Delta of Pre-emphasis Level 2 vs Level 1	HBR/RBR	1.6			dB
	Delta of Pre-emphasis Level 3 vs Level 2	HBR/RBR	1.6			dB
$V_{TX\text{-}DIFF_REDUCTION}$	Non-transition reduction output voltage level 2	HBR/RBR			3	dB
	Non-transition reduction output voltage level 1	HBR/RBR			3	dB
	Non-transition reduction output voltage level 0	HBR/RBR			1.4	dB
$V_{TX\text{-}DIFFp\text{-}p\text{-}MAX}$	Maximum Output Voltage Level	HBR3/ HBR2/HBR/RBR			1.38	V

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7.7 eDP/DP Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
eDP/DP DIFFERENTIAL NOISE						
f_{SSC_eDP}	Spread-spectrum modulation frequency		30		33	kHz
SSC_{TOL_eDP}	Spread-spectrum modulation deviation		–5000		0	ppm
f_{TOL_eDP}	TX frequency long-term stability		–5300		300	ppm
eDP/DP MAIN LINK TX TP3_EQ PARAMETERS						
V_{eDP_EYE}	eDP Mode Upstream Eye Mask	(1) Any UI location (x), where the EYE width is open from x to x +0.5UI	0			mV
V_{eDP_EYE}	eDP Mode Upstream Eye Mask	(2) Any Passing UI location between 0.375 and 0.625UI	37.5			mV
V_{eDP_EYE}	eDP Mode Upstream Eye Mask	(3) Point 1 + 0.5UI	0			mV
V_{eDP_EYE}	eDP Mode Upstream Eye Mask	(4) Any Passing UI location between 0.375 and 0.625UI			-37.5	mV
V_{HBR2_EYE}	DP mode HBR2 Upstream Eye Mask	(1) Any UI location (x), where the EYE width is open from x to x +0.35UI	0			mV
		(2) Any Passing UI location between 0.375 and 0.625UI	45			mV
		(3) Point 1 + 0.35UI	0			mV
V_{HBR2_EYE}	DP mode HBR2 Upstream Eye Mask	(4) Any Passing UI location between 0.375 and 0.625UI			-45	mV
V_{HBR3_EYE}	DP mode HBR3 Upstream Eye Voltage Swing	(1) Any UI location (x), where the EYE width is open from x to x +0.35UI	0			mV
		(2) Any Passing UI location between 0.375 and 0.625UI	37.5			mV
		(3) Point 1 + 0.35UI	0			mV
V_{HBR3_EYE}	DP mode HBR3 Upstream Eye Voltage Swing	(4) Any Passing UI location between 0.375 and 0.625UI			-37.5	mV
$t_{TX\text{-}TJ_TPS4_HBR3}$	Maximum TX Total Jitter HBR3	TPS4 Test Pattern			0.47	UI
$t_{TX\text{-}NonISI_TPS4_HBR3}$	Maximum TX Non-ISI Jitter HBR3	TPS4 Test Pattern			0.23	UI
$V_{TX\text{-}EH\text{-}HBR3}$	TX Differential Peak-to-peak Eye Height HBR3	TPS4 Test Pattern	65			mV
$t_{TX\text{-}TJ_CP2520_HBR2}$	Maximum TX Total Jitter HBR2	CP2520 Test Pattern			0.62	UI
$t_{TX\text{-}RJ_CP2520_HBR2}$	Maximum TX Random Jitter HBR2	CP2520 Test Pattern			0.49	UI
$t_{TX\text{-}DJ_CP2520_HBR2}$	Maximum TX Non-ISI Jitter HBR2	CP2520 Test Pattern			0.49	UI
$V_{TX\text{-}EH\text{-}HBR2}$	TX Differential Peak-to-peak Eye Height HBR2	CP2520 Test Pattern	90			mV
$t_{TX\text{-}DIFFp\text{-}p_RANGE_HBR2_HBR3}$	TX Differential Peak-to-peak EYE Voltage Measurement Range		0.375		0.625	UI

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7.7 eDP/DP Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
eDP/DP MAIN LINK TX SILICON PARAMETERS						
V_{BIAS_TX}	DP mode TX DC Bias Voltage (1)		0		2	V
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level0}$	Reduced Differential Peak-to-peak Output Voltage Swing Level 0 — Requires Register Programming		220	260	300	mV
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	Reduced Differential Peak-to-peak Output Voltage Swing Level 1 — Requires Register Programming		270	350	380	mV
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	Reduced Differential Peak-to-peak Output Voltage Swing Level 2 — Requires Register Programming		330	400	460	mV
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level3}$	Reduced Differential Peak-to-peak Output Voltage Swing Level 3 — Requires Register Programming		390	500	530	mV
$V_{TX\text{-}DIFFp\text{-}p\text{-}MAX}$	eDP mode Maximum Allowed Differential Peak-to-peak Output Voltage Swing Level				1380	mV
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level0}$	Differential Peak-to-peak Output Voltage Swing Level 0		0.34	0.4	0.46	V
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	Differential Peak-to-peak Output Voltage Swing Level 1		0.51	0.6	0.68	V
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	Differential Peak-to-peak Output Voltage Swing Level 2		0.69	0.8	0.92	V
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level3}$	Differential Peak-to-peak Output Voltage Swing Level 3		0.85	1.2	1.38	V

(1) In eDP mode, TX DC Bias Voltage is defined as the same as the common mode voltage (max 1.2 V)

7.8 Recommended Timing for the Serial Control Bus

Over I2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard-mode	>0		100	kHz
		Fast-mode	>0		400	kHz
		Fast-mode Plus	>0		1	MHz
		High-speed-mode	>0		3.4	MHz
t_{LOW}	SCL Low Period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
		High-speed-mode	0.16			µs
t_{HIGH}	SCL High Period	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
		High-speed-mode	0.06			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
		High-speed-mode	0.16			µs

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7.8 Recommended Timing for the Serial Control Bus (continued)

Over I2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{SU:STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
		High-speed-mode	0.16			µs
$t_{HD:DAT}$	Data hold time	Standard-mode	0		3.45	µs
$t_{HD:DAT}$	Data hold time	Fast-mode	0		0.9	µs
$t_{HD:DAT}$	Data hold time	High-speed-mode	0		0.15	µs
$t_{SU:DAT}$	Data set up time	Standard-mode	250			ns
		Fast-mode	100			ns
		Fast-mode Plus	50			ns
		High-speed-mode	10			ns
$t_{SU:STO}$	Set up time for STOP condition	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
		High-speed-mode	0.16			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
t_{BUF}	Bus free time between STOP and START	Fast-mode	1.3			µs
t_{BUF}	Bus free time between STOP and START (FPD-Link IV, FPD-Link III with PCLK ≥ 50 MHz)	Fast-mode Plus	0.5			µs
t_{BUF}	Bus free time between STOP and START (FPD-Link III mode, PCLK < 50 MHz)	Fast-mode Plus	1			µs
t_r	SCL and SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
		High-speed-mode			80	ns
t_f	SCL and SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
		High-speed-mode	10		40	ns
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	pF
		Fast-mode Plus			550	pF
		High-speed-mode			100	pF
$t_{VD:DAT}$	Data valid time	Standard-mode			3.45	µs
$t_{VD:DAT}$	Data valid time	Fast-mode			0.9	µs
$t_{VD:DAT}$	Data valid time	Fast-mode Plus			0.45	µs
$t_{VD:ACK}$	Data valid acknowledge time	Standard-mode			3.45	µs
$t_{VD:ACK}$	Data valid acknowledge time	Fast-mode			0.9	µs
$t_{VD:ACK}$	Data valid acknowledge time	Fast-mode Plus			0.45	µs
t_{SP}	Input filter	Standard-mode			50	ns
		Fast-mode			20	ns
		Fast-mode Plus			6	ns
		High-speed-mode			10	ns

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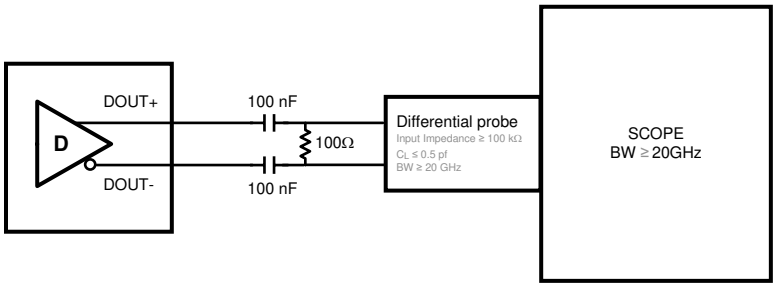
7.9 Timing Diagrams



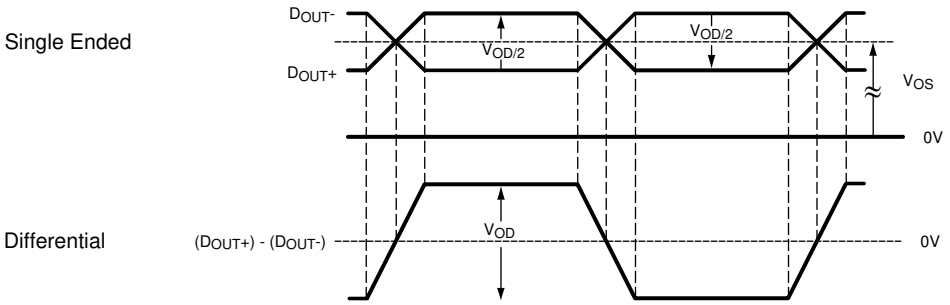


Figure 7-1. Deserializer V_{OD} Output

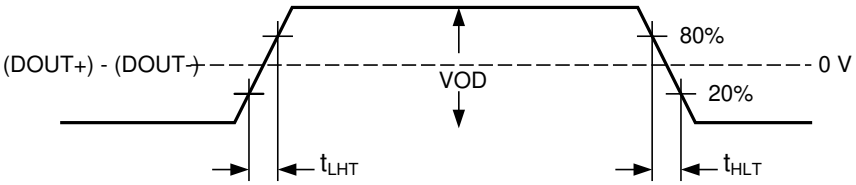


Figure 7-2. Output Transition Times

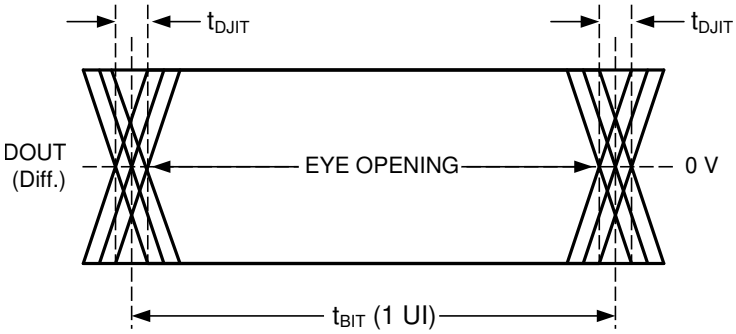


Figure 7-3. Deserializer Output Jitter

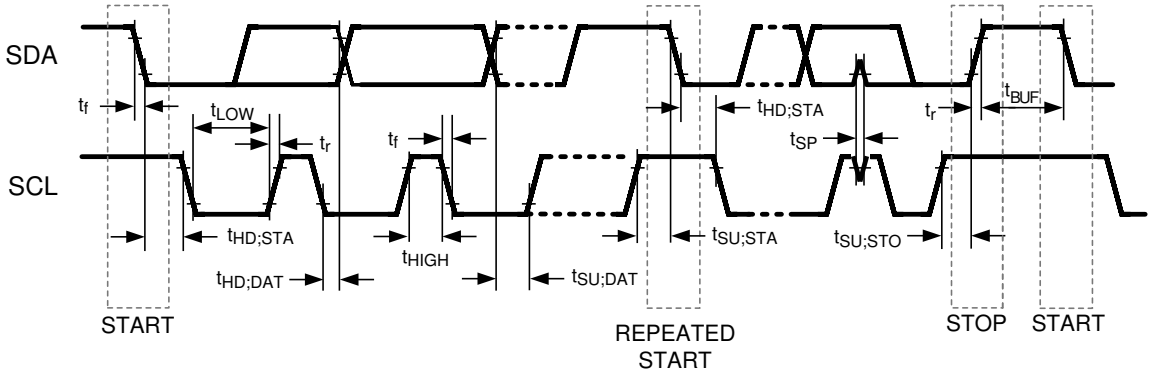


Figure 7-4. Serial Control Bus Timing Diagram

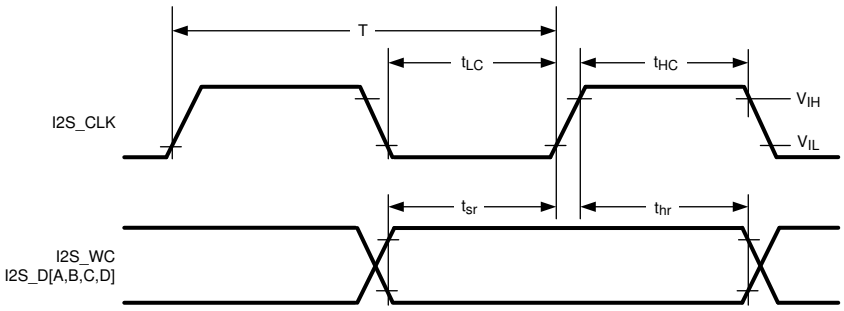


Figure 7-5. I2S Timing Diagram

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8 Detailed Description

8.1 Overview

The DS90UH984-Q1 deserializer accepts an FPD-Link IV input and converts the data to an embedded DisplayPort output or forwards the data onto the FPD-Link daisy-chain output. The DP/eDP transmitter supports up to HBR3 speed, a data rate of 8.1 Gbps with a total bandwidth of 32.4 Gbps link rate. This device receives an FPD-Link IV input over a single coax/STP cable operating up to 13.5 Gbps line rate or dual coax/STP cable operating up to 27 Gbps line rate. The FPD-Link IV serial stream contains an embedded clock, video control signals, video data, control information, and audio data. The payload is DC-balanced to enhance signal quality and to support AC coupling. The DS90UH984-Q1 deserializer is intended for use with a FPD-Link IV serializer such as DS90UH983-Q1, DS90UH981-Q1, or in backward compatibility mode with a FPD-Link III serializer such as DS90UH941AS-Q1, DS90UH949A-Q1, DS90UH949-Q1, DS90UH947-Q1, DS90UH921-Q1, DS90UH925-Q1, DS90UH927-Q1, DS90UH929-Q1 serializers. The DS90UH984-Q1 supports HDCP v1.4 with integrated on-chip keys when working with backward-compatibile HDCP capable FPD-Link III serializers.

The DS90UH984-Q1 deserializer and companion serializer incorporate an I2C compatible interface. The I2C interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer and deserializer as well as remote I2C target devices. The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the back channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another. The implementation allows for arbitration with other I2C compatible controllers at either side of the serial link.

Table 8-1. Specification Overview

FUNCTION	DESCRIPTION
DATA RATES	
Forward Channel Line Rate	• Up to 27 Gbps over dual coax/STP or up to 13.5 Gbps per STP/Coax (including frame and coding overhead) • Discrete rate of 13.5 Gbps, 12.528 Gbps, 10.8 Gbps, 6.75 Gbps, and 3.375 Gbps available per FPD-Link IV lane
DP/eDP Output Rate	• Up to 6.48 Gbps per lane (8.1 Gbps with 8b/10b overhead)
Back-channel Rate	• 168.75 Mbps for FPD-Link IV (13.5 Gbps, 10.8 Gbps, 6.75 Gbps, and 3.375 Gbps) • 156.6 Mbps for FPD-Link IV (12.528 Gbps)
Daisy-Chain Rate	• Up to 13.5 Gbps for FPD-Link IV
INTERFACE	
Cable	FPD-Link IV • 50 Ω coaxial single-ended cable • 100 Ω differential STP/STQ
Video	eDP v1.4b • Configurable 1,2 or 4 lanes
Control	I2C, GPIO, and pass-through SPI • 1MHz I2C (3.4 MHz local bus access) • High-Speed GPIO • Supports SPI and UART pass-through on GPIOs
NETWORKING TOPOLOGIES	
Topologies	• Point-to-point topology • Daisy-chain • One–to–Many Y topology

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Table 8-1. Specification Overview (continued)

FUNCTION	DESCRIPTION
DATA PROTECTION	
Video	• Error detection on deserializer input with error counter and pass signal • Video stream CRC and ECC monitoring • Video line length and count change detection
Control	• Robustness control channel with error detection and correction with error counter and alarm signal • Errors are communicated back to serializer via I2C NACK and link alarm bit.
HEALTH MONITORING AND DIAGNOSTICS	
Interrupts	Interrupts configurable to trigger on link status, bit errors, etc
EQ Monitor	Automatic adaptive equalizer value monitor for cable health observation
Voltage & Temperature	1. Measures up to 2 external voltages 2. Measure internal die temperature 3. 8-bit resolution
AEQ	Adaptive equalizer
BIST	Pseudo-random bit sequence (PRBS) Built-in self test (BIST) function
Line Fault Detect	Serial link line fault monitor to detect FPD port to FPD port short, power supply short, short to ground, or open.

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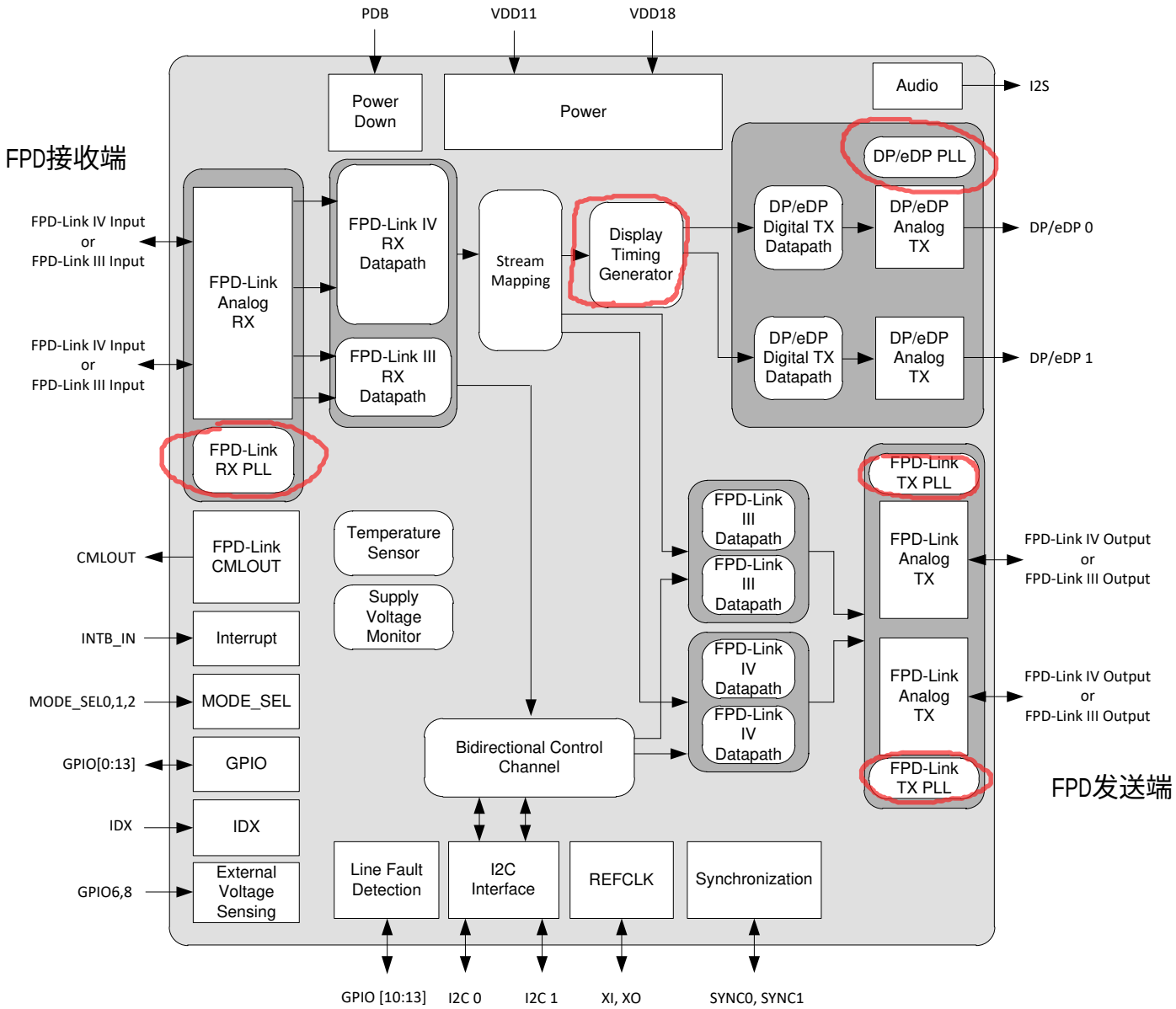
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DisplayPort (DP) / Embedded DisplayPort (eDP) Transmitter

The DP/eDP interface is capable of transmitting high-definition video as well as various control and status data that travel bidirectionally. Each DP/eDP interface consists of four data lanes, one auxiliary channel, and an HPD line. Each DP/eDP Transmitter is a VESA Embedded DisplayPort version 1.4b compatible transmitter. The DP/eDP transmitter (DP/eDP TX) is capable of operation with 4K2K resolutions at 60 Hz. The DS90UH984-Q1 includes DP/eDP support for 18-bit, 24-bit and 30-bit RGB data formats. The DP/eDP data lanes can operate at 1.62 Gbps (Reduced Bit Rate or RBR), 2.7 Gbps (High Bit Rate or HBR), 5.4 Gbps (High Bit Rate 2 or HBR2), or 8.1 Gbps (High Bit Rate 3, or HBR3). The DP/eDP interface incorporates a form of 8b/10b encoding and its differential signaling allows it to reduce electromagnetic interference (EMI) and achieve high skew tolerance.

8.3.1.1 DP/eDP Configuration

The two DP/eDP interface ports can be independently enabled or disabled individually, allowing one port to be enabled or both simultaneously to support dual displays or support high resolution displays that require two DP/eDP outputs. For dual display applications where the two DP/eDP ports are used independently, the pixel clock rate, frame rate, and all video timing parameters must match between the two ports. DP/eDP output state can be controlled either through MODE_SEL1 pin or the PORT_EN bit in the DISPLAY_PORT_CFG register (0x46[3]). Note that register 0x46 is a port specific register and is used in combination with the PORT_SEL register (0x0E) to select which DP/eDP ports are configured.

The two DP/eDP transmitters can be configured for DP or eDP operation. DP/eDP selection can be controlled either through MODE_SEL1 pin or the EDP_MODE bit in the DISPLAY_PORT_CFG register (0x46[5]). If the DP/eDP mode is changed via DISPLAY_PORT_CFG register, a DP/eDP TX PLL reset needs applied by writing 1 to PLL_DPTX_RESET bit in RESET_CTL register (0x01[6]).

Note that register 0x46 is a port specific register and is used in combination with the PORT_SEL register (0x0E) to select which DP/eDP ports are configured.

8.3.1.1.1 DP/eDP Set-Up and Programming

The DP/eDP TX ports require set-up of APB registers and DP/eDP configuration registers prior to successful transmission of video streams. A full example DP/eDP programming sequence is shown in Recommended DP/eDP Software Example.

8.3.1.1.1.1 Programming Quad Pixel Clock for DP/eDP Ports 0 and 1

The video generation uses a quad-pixel clock which is generated based on the DP/eDP rate. DP/eDP ports 0 and 1 share a common PLL, so both must have the same DP/eDP link rate regardless of operating mode: dual DP/eDP or independent DP/eDP. An M/N divider is programmed to generate the desired quad-pixel clock. The M/N divider should be programmed to 1/4 of the video stream's pixel clock frequency by setting DISP_QUAD_PIXEL_CLK_MVAL (0xB2-0xB4) and DISP_QUAD_PIXEL_CLK_NVAL (0xB5-0xB7) on the main page. These M/N divider registers are per port, therefore DP/eDP port 0 and 1 can have independent quad-pixel clocks.

$$\text{Quad Pixel Clock} = \text{Target PCLK} / 4 \tag{1}$$

$$\text{Quad Pixel Clock} = (\text{DP Lane Rate (Gbps)} * 100000) \times \text{DISP_QUAD_PIXEL_CLK_MVAL} / \text{DISP_QUAD_PIXEL_CLK_NVAL} \tag{2}$$

$$\text{DISP_QUAD_PIXEL_CLK_MVAL} = \text{Target PCLK in kHz} \tag{3}$$

$$\text{DISP_QUAD_PIXEL_CLK_NVAL} = \text{DP Lane Rate (kHz)} * 4 / 10 \tag{4}$$

8.3.1.1.1.2 DTG Reset, Setup, and Overrides

The DS90UH984-Q1 uses a timing generator to auto detect and regenerate the video timing signals HS, VS, and DE.

Each DP/eDP has its own DTG register block containing timing parameters. The DTG automatically detects timing parameters based on the incoming video from the serializer. Parameters that are recommended to be detected by DTG from incoming video are listed in Table 8-2. Horizontal start and sync widths are required to be forced. The DTG block should be held in reset while the DTG registers are being programmed, as shown in DTG Reset Hold and Release Script.

DTG可以使用解析参数，也可以使用内部配置参数；DTG作为pattern生成器，其配置时需要先锁住，配置完才能打开

Since the deserializer device uses a local reference clock to generate pixel clock output rate, the DTG is designed to automatically compensate for PPM offset between the received pixel clock rate from the serializer, and the pixel clock rate of the video output from the DP/eDP interface. This mechanism prevents overflow or underrun of the pixel FIFO within the device during operation. The recommended configuration for the DTG leaves the horizontal total pixels per line and the horizontal front porch pixel count flexible to allow for this PPM offset compensation. If the serializer PCLK is slightly faster than the deserializer PCLK, then blanking pixels will be removed from the horizontal front porch of the video within the DTG block before forwarding. If the serializer

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PCLK is slightly slower than the deserializer PCLK, then blanking pixels will be added to the horizontal front porch of the video within the DTG block before forwarding. It is expected to see variation in the measured Htotal and HFP pixel count from the DTG block during normal operation as a result. Overrides can be used to force DTG timing parameters if a display panel has a sensitivity to changing video timing parameters or strict tolerances. It is not suggested to force all display timing parameters in the DTG, as this may result in FIFO overflow/underrun in the presence of slight PCLK variation between the received video PCLK from the serializer and the deserializer PCLK.

确实是page_20

Table 8-2. DTG Registers

Port 0 Register (Page_20)	Port 1 Register (Page_20)	Field	Recommended Detection or Force	Description
0x20[3:2]	0x50[3:2]	POLARITY	Force	Polarity of the vertical and horizontal sync pulses
0x21-0x22	0x51-0x52	HTOTAL	Detected	Total horizontal pixels
0x23-0x24	0x53-0x54	VTOTAL	Detected	Total vertical pixels
0x25-0x26	0x55-0x56	HRES	Detected	Active horizontal pixels
0x27-0x28	0x57-0x58	VRES	Detected	Active vertical pixels
0x29-0x2A	0x59-0x5A	HSTART	Force	Number of clock cycles between the leading edge of the horizontal sync and the start of active data
0x2B-0x2C	0x5B-0x5C	VSTART	Detected	Number of lines between the leading edge of the vertical sync and the first line of active data
0x2D-0x2E	0x5D-0x5E	VSWIDTH	Detected	Width of the vertical sync in lines
0x2F-0x30	0x5F-0x60	HSWIDTH	Force	Width of the horizontal sync in clock cycles
0x31	0x61	START_DELAY	Detected	FIFO Read starts when there are no less than START_DELAY of Data Frame in FIFO.

DTG Reset Hold and Release Script

The following script holds and releases the DTG port 0 and 1 in reset. The DTG block should be held in reset while the DTG registers are being programmed.

```
## ********************************************
## Hold Des DTG in reset
## ********************************************
board.WriteI2C(desAlias0,0x40,0x50) #Select DTG Page
board.WriteI2C(desAlias0,0x41,0x32)
board.WriteI2C(desAlias0,0x42,0x6) #Hold Port 0 DTG in reset
board.WriteI2C(desAlias0,0x41,0x62)
board.WriteI2C(desAlias0,0x42,0x6) #Hold Port 1 DTG in reset

## ********************************************
## Release Des DTG reset
## ********************************************
board.WriteI2C(desAlias0,0x40,0x50) #Select DTG Page
board.WriteI2C(desAlias0,0x41,0x32)
board.WriteI2C(desAlias0,0x42,0x4) #Release Port 0 DTG
board.WriteI2C(desAlias0,0x41,0x62)
board.WriteI2C(desAlias0,0x42,0x4) #Release Port 1 DTG
```

8.3.1.1.1.3 DP/eDP Link Training and Forcing Link Parameters

The DS90UH984-Q1 supports two display port transmitters each with 1, 2 or 4 lane support and link speeds of 8.1/5.4/2.7/1.62 Gbps as per VESA DP standard v1.4a.

Each enabled DP/eDP TX port will automatically attempt to link train with a compatible sink device. Clock recovery and channel equalization phases of link training will be automatically completed. Lane count and rate parameters will be based upon the advertised capability from the sink's DPCD registers.

By default, the DP/eDP TX port will attempt to automatically link train with a compatible sink device based on the maximum advertised lanes and link speeds set in the sink's DPCD registers. The DP/eDP TX port will cycle through available lane counts and speeds until it can settle on an acceptable combination. If the lane count and link speed are not overridden, the user must ensure to use those resulting parameters when configuring DP/eDP APB registers, as described in Section 8.3.1.1.1.4. When properly link trained, lane count and link speed can be read from DPCD registers according to Section 8.3.1.2.

The DP/eDP ports have the following utilization constraints shown by Equation 5 and Equation 6. DP/eDP link rate and lane count should be chosen such that both are satisfied. When Equation 5 is not met, additional blanking symbols are output and might be detected as additional vertical blanking symbols depending on the DP/eDP sink implementation. During such condition, the actual vertical blanking time remains consistent with the input video stream. When Equation 6 is not met, one less blanking start symbol is output and may be detected as one less vertical blanking line.

$$\text{Link Rate} < (8192*10)/(\text{HTotal}/\text{PCLK}) \quad (5)$$

$$\text{Link Rate} > (8192*10)/(2*\text{HTotal}/\text{PCLK}) \quad (6)$$

Where

- Link Rate is DP/eDP link rate in Mbps per lane
- HTotal is total horizontal pixels
- PCLK is pixel clock rate in MHz

When DP/eDP is forced or trained to 8.1 Gbps, additional register configuration is required, as described in Section 8.3.1.1.1.3.2

8.3.1.1.1.3.1 Forcing DP/eDP Link Parameters

An alternative to using the lane count and rate parameters from initial automatic link training is to override lane count and link speed during configuration of the DP/eDP TX ports.

The DP/eDP port 0 and port 1 link rate can be overridden in field CURR_RATE_OV within Page_11 register DP_FIXED_RATE_VAL (0x81[7:5]). To enable the bypass of automatic rate training, FIXED_RATE_MODE in Page_11 register DP_RATE_BYPASS (0x82[1]) is set to 1. FIXED_RATE_MODE and DP_FIXED_RATE_VAL are common registers for both port 0 and 1. Setting the desired link rate by programming CURR_RATE_OV automatically adjusts the PLL settings within Page_12 for the DP/eDP port.

The DP/eDP lane count can be overridden to 1,2, or 4 lanes in Page_11 field NUM_LANES_OV (0x91[2:0] for port 0 and 0xB1[2:0] for port 1). To enable the bypass of automatic lane count training and force the lane count, Page_11 field NUM_LANES_OV_EN (0x91[3] for port 0 and 0xB1[3] for port 1) is set to 1.

To re-initiate link training after overriding lane count or link speed, a DP/eDP TX PLL reset needs applied by writing 1 to PLL_DPTX_RESET bit in RESET_CTL register (main page 0x01[6]).

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8.3.1.1.1.3.2 DP/eDP 8.1 Gbps Configuration

Only when operating at 8.1 Gbps DP/eDP rate, the following script needs to be applied during the initialization of DP/eDP registers. A PLL_DPTX_RESET then must be applied in the RESET_CTL register (0x01[6]).

```
# DP/eDP 8.1 Gbps configuration
board.WriteI2C(DEV_ADDR,0x40,11 * 4)
board.WriteI2C(DEV_ADDR,0x41,0x82)
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x40,20*4)
board.WriteI2C(DEV_ADDR,0x41,0x32)
board.WriteI2C(DEV_ADDR,0x42,0x06)
board.WriteI2C(DEV_ADDR,0x40,20*4)
board.WriteI2C(DEV_ADDR,0x41,0x62)
board.WriteI2C(DEV_ADDR,0x42,0x06)
board.WriteI2C(DEV_ADDR,0x01,0x40)
board.WriteI2C(DEV_ADDR,0x40,20*4)
board.WriteI2C(DEV_ADDR,0x41,0x32)
board.WriteI2C(DEV_ADDR,0x42,0x04)
board.WriteI2C(DEV_ADDR,0x40,20*4)
board.WriteI2C(DEV_ADDR,0x41,0x62)
board.WriteI2C(DEV_ADDR,0x42,0x04)
```

8.3.1.1.1.3.3 Link Training and Link Parameter Status

DP/eDP TX APB registers and sink device's DPCD registers contain various link training parameter and status information. DP/eDP link training status can be read from the sink's DPCD registers 0x202 and 0x203. Trained DP/eDP link speed can be read from the sink's DPCD register 0x100. Trained DP/eDP lane count can be read from the sink's DPCD register 0x101.

When properly link trained, lane count and link speed can be read from DPCD registers according to Section 8.3.1.2.

8.3.1.1.1.4 Programming DP/eDP TX APB Registers

The DP/eDP TX configuration is programmed via a combination of auto-measured and user programmed information into the DP/eDP APB registers. Instructions on how to read and write APB registers through indirect page can be found in Section 8.3.1.1.1.4.1.

The APB programming sequence is required in the video transmission setup phase. After video frames are received, the video timing information in Table 8-3 is automatically loaded from DTG block and written into the APB's MSA registers.

It is required to force the MSA horizontal total timing parameter (0x180) after the DTG reset has been released prior to enabling the DP/eDP ports.

Table 8-3. Auto-Programmed MSA APB Registers

Register	Bits	Name	Description
0x188	1	MAIN_VSYNC_POLARITY	Polarity of the vertical sync pulse.
0x188	0	MAIN_HSYNC_POLARITY	Polarity of the horizontal sync pulse.
0x18C	14:0	MAIN_STREAM_HSWIDTH	Horizontal sync width in clock cycles.
0x190	14:0	MAIN_STREAM_VSWIDTH	Vertical sync width in lines.
0x194	15:0	MAIN_STREAM_HRES	Number of active pixels per line of the main stream video.
0x198	15:0	MAIN_STREAM_VRES	Number of active lines of video in the main stream video source.
0x19C	15:0	MAIN_STREAM_HSTART	Horizontal start clock count. Includes the HSW and HBP time periods.
0x1A0	15:0	MAIN_STREAM_VSTART	Vertical start line count. Includes the VSW and VBP time periods.

In addition to the automatically measured information, the DP/eDP TX also requires user programmed APB configuration for all registers in Table 8-5. Fields such as Nvid, Mvid, BPP, TU mode, TU size, FIFO size, User data count, and sync polarity are all required to be programmed prior to DP/eDP video transmission.

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Equation 7 through Equation 17 are used to program the associated registers. Table 8-5 provides further description and instructions for programming. USER_DATA_COUNT_PER_LANE (0x1BC) is set based on Equation 8.

$$SYMBOL_COUNT = ((HRES + (HRES\%4)) * BPP) + 7) / 8 \quad (7)$$

$$USER_DATA_COUNT_PER_LANE = RoundUp((SYMBOL_COUNT + LANE_COUNT - 1) / LANE_COUNT) \quad (8)$$

Where

- LANE_COUNT is the number of DP/eDP Lanes
- HRES is the active horizontal resolution

MVID (0x1AC[23:0]) and NVID (0x1B4[23:0]) are set based on Equation 9 and Equation 10.

$$MVID = (PCLK * 10) / (LINK_BW_SET*1000) \quad (9)$$

$$NVID = 32768 \quad (10)$$

Where

- PCLK = Pixel clock rate in MHz
- LINK_BW_SET = DP/eDP rate in Gbps

TU size and utilization parameters are set in fields FRAC_SYMBOLS_PER_TU (0x1B0[27:24]), SYMBOLS_PER_TU (0x1B0[23:16]), and TRANSFER_UNIT_SIZE (0x1B0[6:0]) based on Equation 11 through Equation 13.

$$LINK_BW = LINK_BW_SET * 100 * LANE_COUNT_SET \quad (11)$$

$$REQUIRED_DATA_BW = (PCLK * BPP) / 8 \quad (12)$$

$$DATA_PER_TU = REQUIRED_DATA_BW / LINK_BW * TRANSFER_UNIT_SIZE \quad (13)$$

$$SYMBOL_PER_TU = RoundDown(DATA_PER_TU) \quad (14)$$

$$FRAC_SYMBOLS_PER_TU = RoundUp((DATA_PER_TU - SYMBOL_PER_TU)*8)*2 \quad (15)$$

Where

- TRANSFER_UNIT_SIZE = 64

FIFO and data accumulation parameters are set in fields DATA_ACCUMULATION_DELAY 0x0C8[15:8] based on Equation 16 and FIFO_ACCUMULATION_DEPTH 0x0C8[5:0] based on FIFO Accumulation Depth Settings.

$$DATA_ACCUMULATION_DELAY = RoundDown(TRANSFER_UNIT_SIZE / 2) \quad (16)$$

$$TU\ UTILIZATION = (DATA_PER_TU / TRANSFER_UNIT_SIZE) * 100 \quad (17)$$

FIFO_ACCUMULATION_DELAY is set based on FIFO Accumulation Depth Settings.

Table 8-4. FIFO Accumulation Depth Settings

TU UTILIZATION (%)	FIFO_ACCUMULATION_DEPTH (APB 0x0C8[5:0])
<7%	8
8%-25%	7
26%-74%	6
75%-92%	5
93%-95%	4

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Equations and settings provided above are intended for use cases with less than 95% TU utilization. For configuration support for resolutions requiring greater than 95% TU utilization, please contact TI.

Table 8-5. Required User Programmed DP TX APB Registers

APB ADDRESS	BITS	FIELD	DESCRIPTION
0x180	15:0	MAIN_STREAM_HTOTAL	Specifies the total number of clocks in the horizontal framing period for the main stream video signal. This value is sent as the Main Stream Attribute Htotal.
0x0C8	15:8	DATA_ACCUMULATION_DELAY	Specifies the number of link clock cycles for the internal data path controller to wait before sending
0x0C8	5:0	FIFO_ACCUMULATION_DEPTH	Specifies the number of words that must accumulate inside the data path FIFO before attempting to send a valid data packet on the link. This value is only valid once per line during the first active data packet.
0x1A4	7:5	BIT_DEPTH	Number of bits per color 000 = 6 bits 001 = 8 bits 010 = 10 bits
0x1AC	23:0	MVID	Unsigned value computed for clock divider using PCLK and DP/eDP rate
0x1B0	27:24	FRAC_SYMBOLS_PER_TU	Sets the fractional number of valid symbols per TU in units of 1/16th. An accumulator is used to increase the number of data per transaction unit by 1 every 1/N TUs.
0x1B0	23:16	SYMBOLS_PER_TU	Configures the number of valid symbols to transmit with each transaction unit. For most applications, this register can be set to a value of 64 (0x40) which allows the core to automatically manage the TU rate control. For bandwidth limited applications, this value can be set to any number less than or equal to 64. See Section 2.2.1.4.1 of the DisplayPort specification for an example that computes this value.
0x1B0	6:0	TRANSFER_UNIT_SIZE	This number must be in the range of 32 to 64 for DisplayPort compliance and is typically set to a fixed value which depends on the inbound video mode. Larger values should be used for video modes with slower pixel clock rates. Smaller values should be used for video modes with higher pixel clock rates. The size of the TU is limited to integer multiples of 4. Settings that are not a multiple of 4 will be truncated to the lowest multiple.
0x1B4	23:0	NVID	Set to a fixed value of 32768 for clock calculation
0x1B8	2:0	USER_PIXEL_WIDTH	Set to a value of 4 for a quad pixel wide interface.
0x1BC	17:0	USER_DATA_COUNT_PER_LANE	Sets the number of video data symbols per line of active.
0x1C4	2	USER_DATA_ENABLE_POLARITY	Polarity of the input user data enable signal.
0x1C4	1	USER_VSYNC_POLARITY	Polarity of the input user vertical sync pulse.
0x1C4	0	USER_HSYNC_POLARITY	Polarity of the input user horizontal sync.

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8.3.1.1.1.4.1 Reading and Writing APB Registers

When reading or writing APB registers, the DP/eDP port needs selected through the APB_SELECT field in APB_CTL register 0x48[7:3] on main page. APB_ENABLE field in the same register also is set 1 during read and writes to APB registers. Registers 0x49-0x4A contain the target APB register address. Registers 0x4B-0x4E contain the 32-bits of APB data. When reading APB registers, APB_READ field in APB_CTL register 0x48[1] on main page is set to 1. APB auto-increment mode can be enabled by setting APB_AUTO_INC field to 1 in APB_CTL register 0x48[2] on main page.

The following code demonstrates reading LANE_COUNT_SET register 0x004 from the port 0 DP/eDP APB registers.

```
def apb_read_reg(addr16b, channel, Device_ID):
    APB_CTL = 0x48
    APB_ADR0 = 0x49
    APB_ADR1 = 0x4A
    APB_DATA0 = 0x4B
    APB_DATA1 = 0x4C
    APB_DATA2 = 0x4D
    APB_DATA3 = 0x4E

    if channel == 0 :
        page = 0x03
    elif channel == 1:
        page = 0x0B
    else:
        page = 0x03

    addr16b_lsb= addr16b & 0xFF
    addr16b_msb= (addr16b & 0xFF00)>>8
    board.WriteI2C(Device_ID,APB_ADR0,addr16b_lsb)
    board.WriteI2C(Device_ID,APB_ADR1,addr16b_msb)
    board.WriteI2C(Device_ID,APB_CTL,page)
    apbData0=board.ReadI2C(Device_ID,APB_DATA0)
    apbData1=board.ReadI2C(Device_ID,APB_DATA1)
    apbData2=board.ReadI2C(Device_ID,APB_DATA2)
    apbData3=board.ReadI2C(Device_ID,APB_DATA3)
    apbData = (apbData3<<24) + (apbData2<<16) + (apbData1<<8) + (apbData0<<0)
    val32bit=apbData
    return val32bit

## DPTX Port 0 APB Read Example
## Read register 0x004
Port = 0
Device_RX = 0x58
print "PORT ",Port," DPTX APB Dump: Main Stream Attributes"
REG_004 = apb_read_reg(0x004,int(Port), Device_RX )
print "REG_004 (LANE_COUNT_SET) = ", (REG_004)
```


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The following code demonstrates writing MAIN_STREAM_ENABLE register 0x184 to 1 in port 0 DP/eDP APB registers.

```
def apb_write_reg(addr16b, data32b, channel, Device_ID):
    APB_CTL = 0x48
    APB_ADR0 = 0x49
    APB_ADR1 = 0x4A
    APB_DATA0 = 0x4B
    APB_DATA1 = 0x4C
    APB_DATA2 = 0x4D
    APB_DATA3 = 0x4E

    if channel == 0 :
        page = 0x01
    elif channel == 1:
        page = 0x09
    else:
        page = 0x01

    addr16b_lsb= addr16b & 0xFF
    addr16b_msb= (addr16b & 0xFF00)>>8
    board.WriteI2C(Device_ID,APB_ADR0,addr16b_lsb)
    board.WriteI2C(Device_ID,APB_ADR1,addr16b_msb)
    apbData0 = int((data32b & 0x000000FF)>>0)
    apbData1 = int((data32b & 0x0000FF00)>>8)
    apbData2 = int((data32b & 0x00FF0000)>>16)
    apbData3 = int((data32b & 0xFF000000)>>24)
    board.WriteI2C(Device_ID,APB_DATA0, apbData0)
    board.WriteI2C(Device_ID,APB_DATA1, apbData1)
    board.WriteI2C(Device_ID,APB_DATA2, apbData2)
    board.WriteI2C(Device_ID,APB_DATA3, apbData3)
    board.WriteI2C(Device_ID,APB_CTL,page)

## DPTX Port 0 APB Write Example
## Write 0x0001 to register 0x184
Port = 0
Device_RX = 0x58
apb_write_reg(0x0084,0x0001,int(Port),Device_RX)
```

8.3.1.1.1.5 Enabling DP/eDP TX Output

Once all of the DP/eDP configuration registers have been set and DTG reset is released, DP/eDP port 0 and 1 can be enabled to transmit the video stream. DP/eDP TX APB register MAIN_STREAM_ENABLE (0x84[0]) enables the output of active data on the DP/eDP main link.

Enabling DP/eDP Ports Example Script

```
## ********************************************
## Enable DP 0 output
## ********************************************
board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0x84) #Enable DP output
board.WriteI2C(desAlias0,0x4a,0x0)
board.WriteI2C(desAlias0,0x4b,0x1)
board.WriteI2C(desAlias0,0x4c,0x0)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

## ********************************************
## Enable DP 1 output
## ********************************************
board.WriteI2C(desAlias0,0x48,0x9)
board.WriteI2C(desAlias0,0x49,0x84) #Enable DP output
board.WriteI2C(desAlias0,0x4a,0x0)
board.WriteI2C(desAlias0,0x4b,0x1)
board.WriteI2C(desAlias0,0x4c,0x0)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)
```

8.3.1.1.1.6 DP/eDP Recovery After System Disruption

It is required to monitor the system for disruptions such as FPD-Link loss of lock or video stream errors. If disruption occurs during operation, a reset according to DP/eDP Transmit Core Soft Reset and DTG Reset Example Code is needed to recover the DP/eDP output. The DS90UH984 and partner serializer can be configured to detect errors or loss of lock and provide an interrupt to the host controller. Contact TI for additional info and example software flow.

DP/eDP Transmit Core Soft Reset and DTG Reset Example Code

```
# DPTX Core Reset & DTG for DP/eDP Port 0
board.WriteI2C(devAddr,0x40,0x50) #Select DTG Page
board.WriteI2C(devAddr,0x41,0x32)
board.WriteI2C(devAddr,0x42,0x6) #Hold Port 0 DTG in reset
board.WriteI2C(devAddr,0x01,0x40) #Reset DPTX PLL
board.WriteI2C(devAddr,0x41,0x32)
board.WriteI2C(devAddr,0x42,0x4) #Release Des DTG reset

board.WriteI2C(devAddr,0x48,0x1) # DP/eDP Port 0 TX core soft reset
board.WriteI2C(devAddr,0x49,0x90)
board.WriteI2C(devAddr,0x4a,0x0)
board.WriteI2C(devAddr,0x4b,0x01)
board.WriteI2C(devAddr,0x4c,0x00)
board.WriteI2C(devAddr,0x4d,0x0)
board.WriteI2C(devAddr,0x4e,0x0)
```

8.3.1.1.1.7 Optional Modes and Registers

Optional DP/eDP features can be enabled depending on user application and need.

8.3.1.1.1.7.1 Alternate Scrambler Seed Reset (ASSR)

For compatible DP/eDP sink devices, the DP/eDP ports can be configured to enable ASSR functionality, which resets the Linear Feedback Shift Register (LFSR) of the DP/eDP scrambler to 0xFFFE instead of the default 0xFFFF. A DP/eDP sink device must advertise ASSR support through the ALTERNATE_SCRAMBLER_RESET_CAPABLE bit in the eDP_CONFIGURATION_CAP register (DPCD address 0x00Dh, bit 0). To enable ASSR functionality, the EDP_ASSR field in DISPLAY_PORT_CFG register (0x46[7]) must be set to 1 before a DP PLL reset is issued.

Note that register 0x46 is a port specific register and is used in combination with the PORT_SEL register (0x0E) to select which DP/eDP ports are configured.

8.3.1.1.1.7.2 Training Table Voltage Swing Level and Pre-Emphasis Adjustment

The DP/eDP TX supports fine-tuning of the training table that the sink device uses to request adjustments to the differential signal voltages during the training process. Table 8-6 shows valid transmitter voltage swing (VOD) and pre-emphasis combinations. VOD and pre-emphasis are overridden or initialized based on per-port and per-lane basis. Each lane can be initialized to a particular location on the training table by setting a value 0 through 3 in DPx_LNx_INIT register INIT_VOD_SEL and INIT_POST_SEL fields on Page_11. Initializing VOD and pre-emphasis will start the sweep at that location instead of the default of VOD level 0 and pre-emphasis level 0.

Table 8-6. Training Table Initialization

Voltage Swing (VOD)	Training Pre-Emphasis 0	Training Pre-Emphasis 1	Training Pre-Emphasis 2	Training Pre-Emphasis 3
VOD #0	VOD, PRE = 0,0	VOD, PRE = 0,1	VOD, PRE = 0,2	VOD, PRE = 0,3
VOD #1	VOD, PRE = 1,0	VOD, PRE = 1,1	VOD, PRE = 1,2	N/A
VOD #2	VOD, PRE = 2,0	VOD, PRE = 2,1	N/A	N/A
VOD #3	VOD, PRE = 3,0	N/A	N/A	N/A

Table 8-7 shows the registers containing the training table voltage swing and pre-emphasis levels. Port 0 training table registers are 0x30-0x39 on Page_11, and port 1 training table registers are 0x70-0x79 on Page_11.

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Table 8-7. Training Table Registers (port 0 register / port 1 register)

Voltage Swing (VOD)	Training Pre-Emphasis 0	Training Pre-Emphasis 1	Training Pre-Emphasis 2	Training Pre-Emphasis 3
0	DPx_VS_PE_00 (0x30/0x70)	DPx_VS_PE_01 (0x31/0x71)	DPx_VS_PE_02 (0x32/0x72)	DPx_VS_PE_03 (0x33/0x73)
1	DPx_VS_PE_10 (0x34/0x74)	DPx_VS_PE_11 (0x35/0x75)	DPx_VS_PE_12 (0x36/0x76)	N/A
2	DPx_VS_PE_20 (0x37/0x77)	DPx_VS_PE_21 (0x38/0x78)	N/A	N/A
3	DPx_VS_PE_30 (0x39/0x79)	N/A	N/A	N/A

Each lane can force a specific VOD and pre-emphasis in DRV_SEL_POST_OV and DRV_SEL_MAIN_OV registers, respectively. To enable the override, DRV_OV_SEL is set to 1.

8.3.1.1.1.7.3 Fast Link Training

The DP/eDP TX supports fast training mode, also referred to as AUX-less link training. Fast link training allows link training without AUX channel handshaking. The DP/eDP sink device must be capable of supporting fast link training. To enable fast link training functionality, the FAST_TRAINING_MODE field in DISPLAY_PORT_CFG register (0x46[0]) must be set to 1. Note that register 0x46 is a port specific register and is used in combination with the PORT_SEL register (0x0E) to select which DP/eDP ports are configured.

8.3.1.1.1.7.4 Reading Display EDID

Using I2C over Aux transactions, the DS90Ux984-Q1 can read the display EDID. The following code shows how to read the EDID values from the display. Refer to Reading and Writing APB Registers for APB_READ_REG and APB_WRITE_APB functions.

```
Device_RX = 0x58
auxAddress = 0x108
auxWriteFifo = 0x104
auxCommand = 0x100
interruptState = 0x130
auxReplyCode = 0x138
auxReplyData = 0x134

for offset in range(0x00000, 0x000F0, 0x00010):
    # I2c over Aux transaction
    apb_write_reg(auxAddress, 0x00050, 0, Device_RX) # EDID Device ID
    apb_write_reg(auxWriteFifo, offset, 0, Device_RX) # Write the offset
    apb_write_reg(auxCommand, 0x400, 0, Device_RX) #  I2C over Aux write with MOT 1
    time.sleep(0.25)
    apb_write_reg(auxAddress, 0x50, 0, Device_RX) # EDID Device ID
    apb_write_reg(auxCommand, 0x10f, 0, Device_RX) # I2C over aux to read 16 bytes with MOT =0
    time.sleep(0.25)
    replyCode = apb_read_reg(auxReplyCode)
    if (replyCode == 8): # Received Defer
        apb_write_reg(auxAddress, 0x50, 0, Device_RX) # EDID Device ID
        apb_write_reg(auxCommand, 0x10f, 0, Device_RX) # I2C over aux to read 16 bytes with MOT =0
        time.sleep(0.25)    # Read ACK, retry transaction
        replyCode = apb_read_reg(auxReplyCode, 0, Device_RX)
        if (replyCode == 0):
            for i in range(0,16,1):
                replyData = apb_read_reg(auxReplyData, 0, Device_RX) # Read reply data
                print hex(replyData), 'replyData'
    elif (replyCode == 0): # Received ACK
        for i in range(0,16,1):
            replyData = apb_read_reg(auxReplyData, 0, Device_RX) # Read reply data
            print hex(replyData), 'replyData'
```

8.3.1.2 DP/eDP Auxiliary (AUX) Channel

The DP/eDP TX supports a 1 Mbps Manchester-encoded AUX channel used for link management and device control. The AUX channel is a half-duplex bidirectional channel, meaning that communication can only travel in one direction at a time. AUX transactions are initiated by an upstream (e.g. source) device, but a downstream device may prompt an AUX transaction via an IRQ pulse assertion over the HPD line.

100k pull-down resistor to GND is optional for eDP connection but is required for DP connection on the AUX Positive side. 100k pull-up resistor to 3.3V or 1.8V is optional for eDP connection but is required for DP connection on the AUX Negative side.

If the DP/eDP sink device receives a write request but is not ready to accept it, the sink device replies with an AUX_DEFER command. DP/eDP training will restart if 7 total AUX_DEFER commands are received during device operation, even if those DEFER commands are not consecutive and across multiple AUX transactions.

AUX channel read or write operation to the DP/eDP sink DPCD registers can be performed through the DPTX APB interface. Example code for read operations of link train status (0x202 and 0x203), link rate (0x100), and lane count (0x101) is shown in DPCD Register Read Operations.

DPCD Register Read Operations

```
import time
DevAddrRxMain=0x58

auxAddress = 0x108
auxWriteFifo = 0x104
auxCommand = 0x100
interruptState = 0x130
auxReplyCode = 0x138
auxReplyData = 0x134
dpVersion = 0x024
maxLinkRate = 0x00001
rAddr = 0x00000

def apb_read_reg(addr16b):
    APB_CTL = 0x48
    APB_AUTO_INC = {'pos':2, 'wid':1}
    APB_READ = {'pos':1, 'wid':1}
    APB_ENABLE = {'pos':0, 'wid':1}
    APB_ADR0 = 0x49
    APB_ADR1 = 0x4A
    APB_DATA0 = 0x4B
    APB_DATA1 = 0x4C
    APB_DATA2 = 0x4D
    APB_DATA3 = 0x4E

    addr16b_lsb= addr16b & 0xFF
    addr16b_msb= (addr16b & 0xFF00)>>8
    board.WriteI2C(DevAddrRxMain,APB_ADR0,addr16b_lsb)
    board.WriteI2C(DevAddrRxMain,APB_ADR1,addr16b_msb)

    board.WriteI2C(DevAddrRxMain,APB_CTL,0x03)

    apbData0=board.ReadI2C(DevAddrRxMain,APB_DATA0)
    apbData1=board.ReadI2C(DevAddrRxMain,APB_DATA1)
    apbData2=board.ReadI2C(DevAddrRxMain,APB_DATA2)
    apbData3=board.ReadI2C(DevAddrRxMain,APB_DATA3)
    apbData = (apbData3<<24) | (apbData2<<16) | (apbData1<<8) | (apbData0<<0)
    val32bit=apbData
    return val32bit

def apb_write_reg(addr16b, data32b):
    APB_CTL = 0x48
    APB_AUTO_INC = {'pos':2, 'wid':1}
    APB_READ = {'pos':1, 'wid':1}
    APB_ENABLE = {'pos':0, 'wid':1}
    APB_ADR0 = 0x49
    APB_ADR1 = 0x4A
    APB_DATA0 = 0x4B
    APB_DATA1 = 0x4C
    APB_DATA2 = 0x4D
    APB_DATA3 = 0x4E

    addr16b_lsb= addr16b & 0xFF
    addr16b_msb= (addr16b & 0xFF00)>>8
    board.WriteI2C(DevAddrRxMain,APB_ADR0,addr16b_lsb)
    board.WriteI2C(DevAddrRxMain,APB_ADR1,addr16b_msb)
    print 'data32b', data32b
    apbData0 = int((data32b & 0x000000FF)>>0)
```


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```
    print 'type', type(apbData0), apbData0
    apbData1 = int((data32b & 0x0000FF00)>>8)
    apbData2 = int((data32b & 0x00FF0000)>>16)
    apbData3 = int((data32b & 0xFF000000)>>24)
    board.WriteI2C(DevAddrRxMain,APB_DATA0, apbData0)
    board.WriteI2C(DevAddrRxMain,APB_DATA1, apbData1)
    board.WriteI2C(DevAddrRxMain,APB_DATA2, apbData2)
    board.WriteI2C(DevAddrRxMain,APB_DATA3, apbData3)

    board.WriteI2C(DevAddrRxMain,APB_CTL,0x01)

## AUX DP/eDP Train Status Read 0x202 and 0x203
for dpcdAddr in range(0x202, 0x204):
    # Aux read transaction to read DPCD registers
    apb_write_reg(0x108, dpcdAddr) # aux address
    apb_write_reg(0x100, 0x900) # aux Command to read
    time.sleep(0.25)
    replyData = apb_read_reg(0x134) # Read reply data
    print "DPCD addr " + hex(dpcdAddr)+  " is " + hex(replyData)

## AUX DP/eDP DP Rate Status 0x100
apb_write_reg(0x108, 0x100)
apb_write_reg(0x100, 0x900)
time.sleep(0.25)
replyData = apb_read_reg(0x134)
print "DP Rate (" + hex(dpcdAddr)+  ") is " + hex(replyData)

## AUX DP/eDP Lane Count Status 0x101
apb_write_reg(0x108, 0x101)
apb_write_reg(0x100, 0x900)
time.sleep(0.25)
replyData = apb_read_reg(0x134)
print "DP Lane Count (" + hex(dpcdAddr)+  ") is " + hex(replyData)
```

8.3.1.3 Hot Plug Detect (HPD)

The HPD line is asserted by the sink to let the source know that it is ready for AUX transactions. The HPD line may also be used for an interrupt request (IRQ) assertion by a downstream (e.g. sink) device. The HPD line is used by the upstream (e.g. source) device to detect the plugging of a downstream device. 100k pull-down resistor to GND is required. Similarly, the downstream device monitors AUX+ and AUX- DC voltage levels to detect the presence of an upstream device and the upstream device's power state. After the HPD pin is asserted, the AUX channel will be used to perform link training, and configure drive current / equalization levels.

8.3.1.4 eDP Backlight Control

The DS90UH984-Q1 supports eDP backlight brightness control through the PWM (pulse width modulation) generator. The duty cycle of the PWM signal represents the brightness of the display backlight. Each eDP port has its own PWM generator. The pulse output of eDP Port 0 goes to GPIO 10, and pulse of eDP Port 1 goes to GPIO 11. Both generators can run at the same time.

DPx_BACKLIGHT_CTL, DPx_BACKLIGHT_SCALE and DPx_BACKLIGHT_PRESCALE_DIV (0x9D to 0xA1 for eDP port 0, 0xBD to 0xC1 for eDP port 1 on indirect register Page_11) need to be programmed before enabling PWM generator.

Table 8-8. eDP Backlight Control

Register Name	Bits Name	Description
DPx_BACKLIGHT_CTL_0	BACKLIGHT_CTL[7:0]	The quotient of DPx_BACKLIGHT_CTL and DPx_BACKLIGHT_SCALE controls the duty cycle of the pulse (the brightness of the display backlight) See Equation 19
DPx_BACKLIGHT_CTL_1	BACKLIGHT_CTL[15:8]	
DPx_BACKLIGHT_SCALE_0	BACKLIGHT_SCALE[7:0]	Controls the granularity of the brightness and pulse frequency
DPx_BACKLIGHT_SCALE_1	BACKLIGHT_SCALE[15:8]	
DPx_BACKLIGHT_PRESCALE_DIV	BACKLIGHT_PRESCALE_DIV	Used to pre-scale PWM frequency. See Equation 18

$$\text{PWM frequency} = 27\text{MHz} / (\text{PRESCALE_DIV} \times (\text{BACKLIGHT_SCALE} + 1)) \quad (18)$$

PWM duty cycle = (BACKLIGHT_CTL +1) / (BACKLIGHT_SCALE + 1) (19)

After the DPx_BACKLIGHT_CTL, DPx_BACKLIGHT_SCALE and DPx_BACKLIGHT_PRESCALE_DIV register bits are programmed, DPx_PWM_CTL[0] (register 0xA2 for eDP Port 0, 0xC2 for eDP Port 1) needs to be enabled. DPx_PWM_CTL[1] configures the polarity of PWM pulse.

Table 8-9.

Register Name	Field Name	Description
DPx_PWM_CTL[1]	PWM_INV	0: High Active. Duty cycle = number of clock cycles of PWM staying high / total number of clock cycles. 1: Low Active. Duty cycle = number of clock cycles of PWM staying low / total number of clock cycles.
DPx_PWM_CTL[0]	PWM_EN	0: Disable PWM 1: Enable PWM

8.3.1.5 DP/eDP Transmitter Output Spread Spectrum Clock Generation (SSCG)

Spread spectrum clocking is available for the DP/eDP output as a triangular ramp between 30 kHz and 33 kHz modulation frequency and from 0% to 0.5% frequency deviation. Only down-spread is supported.

Not all DP/eDP panels can support SSCG on the DP/eDP interface, consult the panel supplier for information and make sure to disable SSCG if the panel can not support spread spectrum on the DP/eDP interface to avoid display issues. Further details on disabling SSCG or overriding enabled SSCG strap setting can be found in Section 8.3.1.5.2.

The DP/eDP transmitter output is generated based on a phase locked loop (PLL). By default, DP/eDP PLL parameters are automatically set based on trained or forced DP/eDP rates and strap modes. When SSCG is enabled via MODE_SEL2, DP/eDP PLL parameters, RAMPX_STOP and RAMPX_INC registers are automatically configured for a 32 kHz and 0.2% downspread SSCG profile. This profile applies to all DP/eDP data rates when enabled via MODE_SEL2. The default register configuration is shown in Table 8-10. The following overrides are available when a different profile or manual MODE_SEL2 SSCG enable override is desired:

1. When MODE_SEL2 is configured to enable SSCG and a different SSCG profile is desired:
   a. OVD_SSCG_AUTOCFG (Page_12 reg 0x0F[0]) set to 1
   b. SSCG_DOWNSPREAD (Page_12 0x14[7]) must be set to downspread mode.
   c. RAMPx_INC and RAMPx_STOP (Page_12 0x14, 0x15 and 0x16) should be programmed to desired SSCG profile based on Section 8.3.1.5.1.
2. When MODE_SEL2 is configured to disable SSCG, the following registers are programmed to override to enable SSCG:
   a. SSCG_EN (Page_12 0x17[6]) should be set to 1 to enable SSCG
   b. SSCG_DOWNSPREAD (Page_12 0x14[7]) must be set to downspread mode.
   c. If OVD_SSCG_AUTOCFG (Page_12 0x0F[0]) set to 0, default SSCG profile will be used.
   d. If OVD_SSCG_AUTOCFG (Page_12 0x0F[0]) set to 1, RAMPx_INC and RAMPx_STOP (Page_12, 0x14, 0x15 and 0x16) should be programmed to desired SSCG profile based on Section 8.3.1.5.1.

Table 8-10. Default SSCG Configuration: 32 kHz f_{MOD} and 0.2% f_{DEV}

DP/eDP Data Rate	1.62 Gbps	2.7 Gbps	5.4 Gbps	8.1 Gbps
Reference Source	XI (27 MHz)			
VCO Frequency	6.48 GHz	5.4 GHz	5.4 GHz	8.1 GHz
N-Divider	119	99	99	149
$Numerator_{FINAL}$	16777206			
$Denominator_{FINAL}$	16777206			
Post Divider	4	2	1	1
RAMPX_STOP	210			

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Table 8-10. Default SSCG Configuration: 32 kHz f_{MOD} and 0.2% f_{DEV} (continued)

DP/eDP Data Rate	1.62 Gbps	2.7 Gbps	5.4 Gbps	8.1 Gbps
RAMPX_INC	9587	7989	7989	11984

8.3.1.5.1 DP/eDP SSCG Calculations

To configure spread spectrum clock generation, the following equations can be used to calculate the RAMPX_STOP and RAMPX_INC.

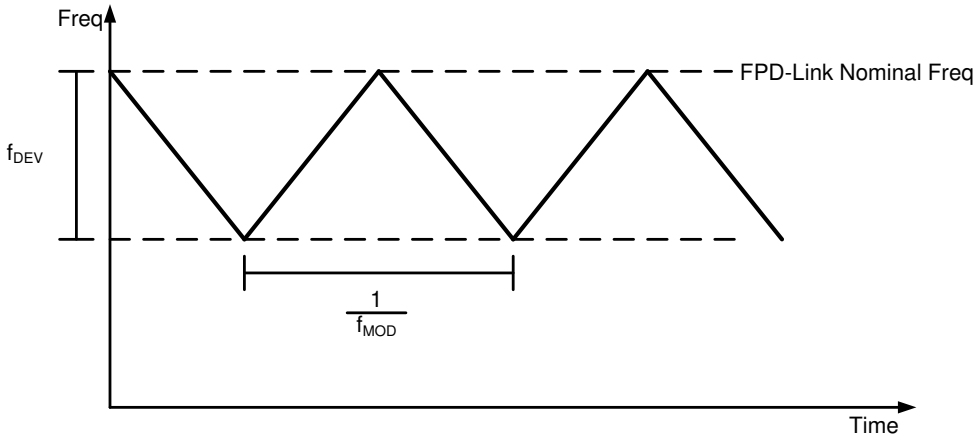

Figure 8-1. Down Spread SSCG

$$RAMPX_STOP = \frac{f_{REF}}{(4 \times f_{MOD})} \tag{20}$$

where

- f_{REF} is the reference clock in kHz (27000)
- f_{MOD} is the modulation frequency in kHz

$$RAMPX_INC_{Initial} = \frac{(VCO_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP)} \tag{21}$$

- $RAMPX_INC_{Initial}$ must be rounded to an integer number

where

- f_{DEV} is the deviation frequency as a percentage of the DP/eDP frequency (Example: deviation frequency = 0.5% = f_{DEV} = 0.5)
- i_{SPREAD} = 2
- $DEN_{Initial}$ is the denominator of the N-divider in the DP/eDP PLL (16,777,206)
- REFCLK is the reference clock frequency in MHz (27)
- VCO_freq is the DP/eDP rate in MHz

$$x = \begin{cases} \log_2 \frac{RAMPX_INC_{Initial}}{32767}, & RAMPX_INC_{Initial} > 32767 \\ 0, & RAMPX_INC_{Initial} \le 32767 \end{cases} \tag{22}$$

where

- x must be rounded up to the nearest integer

$$RAMPX_INC_{Final} = \frac{(VCO_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP \times 2^{x})} \quad (23)$$

$$DEN_{Final} = \left(\frac{DEN_{Initial}}{2^{x}}\right) \quad (24)$$

$$NUM_{Final} = \left(\frac{NUM_{Initial}}{2^{x}}\right) \quad (25)$$

where

- Initial numerator and denominator are determined based on the DP/eDP rate. If the original PLL setting is integer mode (numerator = 0) then the first step of applying SSCG is to convert to fractional mode (subtract one from the integer part of the n divider and set both numerator and denominator to 16,777,206).

$$VCO_{Freq,Final} = f_{REF} \times 2\left[Ndiv + \left(\frac{NUM_{Final}}{DEN_{Final}}\right)\right] \quad (26)$$

$$f_{DEV,Final} = \left[\frac{(RAMPX_INC_{Final} \times REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP)}{(VCO_{Freq,Final} \times DEN_{Final})}\right] \quad (27)$$

8.3.1.5.2 Disabling DP/eDP SSCG

When DP/eDP SSCG is not desired and MODE_SEL2 is configured to disabled, additional register configuration is required to disable the SSCG. The following script must be used to disable DP/eDP SSCG prior to enabling the DP/eDP output:

```
#Disable DP SSCG when MODE_SEL2 DP SSCG set to 0
board.WriteI2C(desAlias0,0x40,0x30)
board.WriteI2C(desAlias0,0x41,0xf)
board.WriteI2C(desAlias0,0x42,0x1)
board.WriteI2C(desAlias0,0x1,0x40)
```

To override the enabled DP/eDP SSCG MODE_SEL2 strap setting, SSCG_EN field in Page_12 register 0x17 must be set to 0.

```
#Override DP SSCG when MODE_SEL2 DP SSCG set to 1
board.WriteI2C(desAlias0,0x40,0x30)
board.WriteI2C(desAlias0,0x41,0x17)
board.WriteI2C(desAlias0,0x42,0x0)
board.WriteI2C(desAlias0,0x41,0xf)
board.WriteI2C(desAlias0,0x42,0x1)
board.WriteI2C(desAlias0,0x1,0x40)
```

8.3.1.6 Recommended DP/eDP Software Example

An example of the recommended DP/eDP configuration sequence based on Section 8.3.1.1 for deserializer can be found below. The DP/eDP is configured for receiving 1920x1080p video from upstream serializer.

1. Hold DTG reset, as described in Section 8.3.1.1.1.2
2. DP/eDP port configuration
   a. Forcing DP/eDP to 4 lanes and 2.7 Gbps rate, as described in Section 8.3.1.1.1.3
   b. Disabling DP/eDP SSCG, as described in Section 8.3.1.5.2
   c. Disable DP/eDP port 1, as described in Section 8.3.1.1
3. Programming Quad Pixel Clock for DP/eDP port 0, as described in Section 8.3.1.1.1.1
4. DTG set-up and forcing of parameters , as described in Section 8.3.1.1.1.2
5. DP/eDP APB register configuration, as described in Section 8.3.1.1.1.4

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6. Release DTG reset, as described in Section 8.3.1.1.1.2
7. Force MSA horizontal total value, as described in Section 8.3.1.1.1.4
8. Enable DP/eDP output, as described in Section 8.3.1.1.1.5

```
## DP Port 0 Enabled
## DP Port 1 Disabled
## DP lane number set to 4 lanes
## DP Rate set to 2.7 Gbps
## DP SSCG disabled
## Horizontal Sync Polarity = Positive
## Vertical Sync Polarity = Positive
## Bits per pixel = 24
## Pixel Clock = 148.5MHz

## ********************************************
## Hold Des DTG in reset
## ********************************************
board.WriteI2C(desAlias0,0x40,0x50) #Select DTG Page
board.WriteI2C(desAlias0,0x41,0x32)
board.WriteI2C(desAlias0,0x42,0x6) #Hold Port 0 DTG in reset
board.WriteI2C(desAlias0,0x41,0x62)
board.WriteI2C(desAlias0,0x42,0x6) #Hold Port 1 DTG in reset

## ********************************************
## DP / eDP Port Configuration
## ********************************************
board.WriteI2C(desAlias0,0x40,0x2c) #Select DP Page
board.WriteI2C(desAlias0,0x41,0x81)
board.WriteI2C(desAlias0,0x42,0x60) #Set DP Rate to 2.7Gbps
board.WriteI2C(desAlias0,0x41,0x82)
board.WriteI2C(desAlias0,0x42,0x2) #Enable force DP rate
board.WriteI2C(desAlias0,0x41,0x91)
board.WriteI2C(desAlias0,0x42,0xc) #Force 4 lanes
board.WriteI2C(desAlias0,0x40,0x30) #Disable DP SSCG
board.WriteI2C(desAlias0,0x41,0xf)
board.WriteI2C(desAlias0,0x42,0x1)
board.WriteI2C(desAlias0,0x1,0x40)
board.WriteI2C(desAlias0,0xe,0x12) #Select Port 1 registers
board.WriteI2C(desAlias0,0x46,0x0) #Disable DP Port 1
board.WriteI2C(desAlias0,0xe,0x1) #Select Port 0 registers
board.WriteI2C(desAlias0,0x1,0x40) #DP-TX-PLL RESET Applied

## ********************************************
## Program quad pixel clock for DP port 0
## ********************************************
board.WriteI2C(desAlias0,0xe,0x1) #Select Port0 registers
board.WriteI2C(desAlias0,0xb1,0x1) #Enable clock divider
board.WriteI2C(desAlias0,0xb2,0x14) #Program M value lower byte
board.WriteI2C(desAlias0,0xb3,0x44) #Program M value middle byte
board.WriteI2C(desAlias0,0xb4,0x2) #Program M value upper byte
board.WriteI2C(desAlias0,0xb5,0xc0) #Program N value lower byte
board.WriteI2C(desAlias0,0xb6,0x7a) #Program N value middle byte
board.WriteI2C(desAlias0,0xb7,0x10) #Program N value upper byte
board.WriteI2C(desAlias0,0xe,0x1) #Select Port 0 registers

## ********************************************
## Setup DTG for port 0
## ********************************************
board.WriteI2C(desAlias0,0x40,0x50) #Select DTG Page
board.WriteI2C(desAlias0,0x41,0x20)
board.WriteI2C(desAlias0,0x42,0x93) #Set up DTG BPP, Sync Polarities, and Measurement Type
board.WriteI2C(desAlias0,0x41,0x29) #Set Hstart
board.WriteI2C(desAlias0,0x42,0x80) #Hstart upper byte
board.WriteI2C(desAlias0,0x41,0x2a)
board.WriteI2C(desAlias0,0x42,0xc0) #Hstart lower byte
board.WriteI2C(desAlias0,0x41,0x2f) #Set HSW
board.WriteI2C(desAlias0,0x42,0x40) #HSW upper byte
board.WriteI2C(desAlias0,0x41,0x30)
board.WriteI2C(desAlias0,0x42,0x2c) #HSW lower byte

## ********************************************
## Program DPTX for DP port 0
## ********************************************
board.WriteI2C(desAlias0,0x48,0x1) #Enable APB interface
board.WriteI2C(desAlias0,0x48,0x1)
```

```
board.WriteI2C(desAlias0,0x49,0xa4) #Set bit per color
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0x20)
board.WriteI2C(desAlias0,0x4c,0x0)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xb8) #Set pixel width
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0x4)
board.WriteI2C(desAlias0,0x4c,0x0)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xac) #Set DP Mvid
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0x66)
board.WriteI2C(desAlias0,0x4c,0x46)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xb4) #Set DP Nvid
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0x0)
board.WriteI2C(desAlias0,0x4c,0x80)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xc8) #Set TU Mode
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0x0)
board.WriteI2C(desAlias0,0x4c,0x0)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xb0) #Set TU Size
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0x40)
board.WriteI2C(desAlias0,0x4c,0x0)
board.WriteI2C(desAlias0,0x4d,0x1a)
board.WriteI2C(desAlias0,0x4e,0x8)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xc8) #Set FIFO Size
board.WriteI2C(desAlias0,0x4a,0x0)
board.WriteI2C(desAlias0,0x4b,0x6)
board.WriteI2C(desAlias0,0x4c,0x40)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xbc) #Set data count
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0xa0)
board.WriteI2C(desAlias0,0x4c,0x5)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xc0) #Disable STREAM INTERLACED
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0x0)
board.WriteI2C(desAlias0,0x4c,0x0)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0xc4) #Set SYNC polarity
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0xc)
board.WriteI2C(desAlias0,0x4c,0x0)
```


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```
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

## ********************************************
## Release Des DTG reset
## ********************************************
board.WriteI2C(desAlias0,0x40,0x50) #Select DTG Page
board.WriteI2C(desAlias0,0x41,0x32)
board.WriteI2C(desAlias0,0x42,0x4) #Release Port 0 DTG
board.WriteI2C(desAlias0,0x41,0x62)
board.WriteI2C(desAlias0,0x42,0x4) #Release Port 1 DTG

board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0x80) #Set Htotal
board.WriteI2C(desAlias0,0x4a,0x1)
board.WriteI2C(desAlias0,0x4b,0x98)
board.WriteI2C(desAlias0,0x4c,0x8)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)

## ********************************************
## Enable DP 0 output
## ********************************************
board.WriteI2C(desAlias0,0x48,0x1)
board.WriteI2C(desAlias0,0x49,0x84) #Enable DP output
board.WriteI2C(desAlias0,0x4a,0x0)
board.WriteI2C(desAlias0,0x4b,0x1)
board.WriteI2C(desAlias0,0x4c,0x0)
board.WriteI2C(desAlias0,0x4d,0x0)
board.WriteI2C(desAlias0,0x4e,0x0)
```

8.3.2 FPD-Link IV High Speed Forward Channel Data Transfer

The High Speed Forward Channel transmits data according to the FPD-Link IV protocol. The protocol consists of control and data packets, referred to as frames. FPD-Link IV frames are composed of 132 bits of data containing video data, sync signals, I^2C, and GPIOs transmitted from serializer to deserializer. This 132 bit frame includes 128-bits of video data. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. FPD-Link IV protocol allows for up to six distinct streams to be transferred over a single link. To manage the bandwidth allocation of the FPD-Link, each FPD-Link includes 65 different time slots which are divided up between the different FPD-Link steams.

The FPD-Link IV serial stream rate supports fixed-rates of 13.5 Gbps, 12.528 Gbps, 10.8 Gbps, 6.75 Gbps and 3.375 Gbps. When operating over both FPD-Link channels, a total data rate of 27 Gbps, 25.056 Gbps, 21.6 Gbps, 13.5 Gbps, and 6.75 Gbps are supported, respectively.

8.3.2.1 FPD-Link IV RX Modes of Operation

The FPD-Link IV receive logic supports several modes of operation, dependent on the upstream transmitter as well as the video being delivered. The FPD-Link Port mode is set via FPD4_RX_CFG register 0x31 FPD4_INPUT_MODE field. Only the following modes are supported (Independent mode is not supported):

8.3.2.1.1 Single Link Operation

Single Link mode transmits the video over a single FPD-Link port to a single receiver.

8.3.2.1.2 Dual Link Operation

In Dual Link mode, the FPD-Link IV RX assumes the data on both links comes from a single source. Dual link mode supports a total line rate of 27 Gbps, with each FPD-Link IV RX port running at one-half the rate, 13.5 Gbps.

8.3.2.2 FPD-Link IV RX PLL, Clock Data Recovery, & SSCG

The FPD-Link IV RX is deserialized based on a phase locked loop (PLL). The 27MHz XI is used as the reference source. Both FPD-Link RX ports 0 and 1 share a single PLL block and post-divider. If both channels are in FPD-Link IV mode, the two channels will be at the same frequency. While operating in FPD-Link IV mode, a number of pre-programmed data rates are available to be strapped to, such as discrete rates of 13.5 Gbps, 12.528 Gbps, 10.8 Gbps, 6.75 Gbps, and 3.375 Gbps.

By default, the deserializer automatically calibrates registers and settings of the FPD RX PLL based on the link data rate strap upon start-up. Link lock and communication between the serializer and deserializer are automatic if all MODE_SEL straps are set to the correct link configuration and data rate.

While it is possible to manually configure the FPD-Link IV RX PLL, it is often undesirable since a typical SerDes use-case depends on a valid lock to initialize remote programming of the deserializer from the serializer. FPD-Link IV RX PLL override programming should only be implemented in systems which utilize local I2C control at the deserializer side. The manual process of configuring the FPD-Link IV RX PLL for a particular data rate consists of selecting a VCO, setting the division factor for the PLL feedback divisor, PLL post-divider, and phase interpolator (PI) post-divider inside the FPD-Link IV CDR. Further details for manually configuring the FPD-Link IV RX PLL can be referred to in Section 8.3.2.2.1.

8.3.2.2.1 Manual FPD-Link IV RX PLL Configuration

When manually setting the RX PLL in FPD-Link IV mode, the output clock should be half of the data rate of the link and is generated using the following settings, programmable via Page_2 of the indirect access registers. The FPD-Link IV RX PLL post-divider is programmed in main page register 0x33. After modifying the PLL values, issue a soft digital reset to the deserializer by setting register 0x01 = 0x01.

The following equation is used to calculate the VCO frequency:

$$f_{VCO} = f_{REF} \times 2 \times \left[N + \left(\frac{NUM}{DEN} \right) \right] \tag{28}$$

where

- f_{VCO} is the VCO frequency
- f_{Ref} is the reference frequency, either from the XI
- N is the integer portion of the N-divider (0 to 65,535)
- NUM is the numerator portion of the N-divider fraction (0 to 16,777,206), NUM ≤ DEN
- DEN is the denominator portion of the N-divider fraction (1 to 16,777,206)

Table 8-11. FPD-Link IV RX PLL

FPD-Link Data Rate	12.528 Gbps	10.8 Gbps	13.5 Gbps	6.75 Gbps	3.375 Gbps
Reference Source	XI (27 MHz)				
N-Divider	116 (NDIV[7:0] = 0x74, NDIV[15:8] = 0x00)	100 (NDIV[7:0] = 0x64, NDIV[15:8] = 0x00)	125 (NDIV[7:0] = 0x7D, NDIV[15:8] = 0x00)		
Numerator	0 (NUM[7:0] = 0x00, NUM[15:8] = 0x00, NUM[23:16] = 0x00)				
Denominator	16,777,206 (DEN[7:0] = 0xF6, DEN[15:8] = 0xFF, DEN[23:16] = 0xFF)				
MASH Order	Integer (MASH_ORDER_2_0 = 0x00)				
Post-Divider	0 (POST_DIV = 0x0)			1 (POST_DIV = 0x1)	2 (POST_DIV = 0x2)

8.3.3 Forward Channel Lock Output

GPIO4, GPIO5 and GPIO6 default to output forward channel lock status.

GPIO4 indicates lock status for FPD-Link Channel 0 and GPIO5 indicates lock status for FPD-Link Channel 1. GPIO6 defaults to output the ANDed lock status of all active FPD-Link Input Ports (FPD-Link Port 0 and FPD-Link Port 1 in dual mode, FPD-Link Port 0 in single mode).

In general, GPIO6 can be used as the primary lock status indication in either single or dual FPD-Link operation. GPIO4 and GPIO5 can be used in conjunction to provide detailed lock status in dual mode.

8.3.4 Back Channel Data Transfer

The back channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as back channel frames. The back channel control data is transferred over the serial link along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high speed

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forward channel. The back channel frame consists of 30 bits which contain the I2C, GPIO, and CRC information. Back channel rates of 168.75 Mbps (when paired with an FPD-Link IV serializer at forward channel line rate of 13.5 Gbps, 10.8 Gbps, 6.75 Gbps, or 3.375 Gbps) or 156.6 Mbps (when paired with an FPD-Link IV serializer at forward channel line rate of 12.528 Gbps) are supported.

8.3.4.1 Back Channel SSCG

If desired, spread spectrum clocking may be enabled for the FPD-Link back channel with between 30 kHz and 33 kHz modulation frequency and up to 0.5% frequency deviation with center spread or 0.25% deviation with down spread. FPD-Link forward channel SSCG and back channel SSCG combined should not exceed 0.5% total frequency deviation. Both center-spread and down-spread ramps are supported. The parameters for these two modes are shown in Table 8-12. The FPD RX PLL must be configured in fractional mode to enable SSCG on back channel, as described in Section 8.3.2.2. The FPD RX PLL registers are programmable via Page_2 of the indirect registers. If it is configured in integer mode (NUM[23:0] = 0), set NUM[23:0] = DEN[23:0], and subtract one from the NDIV[15:0] value. For instance, to enable SSCG using the default FPD-Link IV PLL settings for 3.375 Gbps, 6.75 Gbps, or 13.5 Gbps, set NDIV = 124 and NUM[23:0] = DEN[23:0] = 16,777,206. To configure spread spectrum clock generation, calculate the RAMPX_STOP (in Page_2 0x16-0x17 registers) and RAMPX_INC (in Page_2 0x14-0x15 registers) using the equations in Section 8.3.4.1.1.

Table 8-12. Back Channel SSCG

Enable	Spread Type	RAMPX_INC	RAMPX_STOP
Enable: SSCG_EN = 1	Down-spread: SSCG_CNTR_SPRD = 0	RAMPX_INC_6_0 = 7 LSB of calculated value	RAMPX_STOP_6_0 = 7 LSB of calculated value
Disable: SSCG_EN = 0	Center-spread: SSCG_CNTR_SPRD = 1	RAMPX_INC_14_7 = 8 MSB of calculated value	RAMPX_STOP_14_7 = 8 MSB of calculated value

Table 8-13. FPD-Link IV RX PLL: Example PLL Set-Up and SSCG Enable for Center Spread with 0.25% Deviation

FPD-Link Data Rate	12.528 Gbps	10.8 Gbps	13.5 Gbps	6.75 Gbps	3.375 Gbps
Reference Source	XI (f_{REF}=27 MHz)				
N-Divider	115 (NDIV[7:0] = 0x73, NDIV[15:8] = 0x00)	99 (NDIV[7:0] = 0x63, NDIV[15:8] = 0x00)	124 (NDIV[7:0] = 0x7C, NDIV[15:8] = 0x00)		
Numerator	16,777,206 (NUM[7:0] = 0xF6, NUM[15:8] = 0xFF, NUM[23:16] = 0xFF)				
Denominator	16,777,206 (DEN[7:0] = 0xF6, DEN[15:8] = 0xFF, DEN[23:16] = 0xFF)				
MASH Order	Fractional (MASH_ORDER_2_0 = 0x2)				
Post-Divider	1 (POST_DIV = 0x0)			2 (POST_DIV = 0x1)	4 (POST_DIV = 0x2)
FPD-Link Frequency	6.75 GHz	6.264 GHz	5.4 GHz	3.375 GHz	1.6875 GHz
SSCG Enable	SSCG_EN = 1				
SSCG Frequency	f_{MOD}=33,000 Hz				
SSCG Spread Amount	0.25%				
Spread Type	Center (SSCG_CNTR_SPRD=1)				
RAMPX_INC	11925	10280	12850	12850	12850
RAMPX_STOP	204				

Example Fractional PLL Setup and SSCG Enable

The following script configures the fractional divider and enables back channel SSCG for 6.75 Gbps forward channel rate and 168.75 Mbps back channel rate with above SSCG parameters:

```
board.WriteI2C(desAddr,0x33,0x5) # Post divider for 6.75Gbps
board.WriteI2C(desAddr,0x40,0xa)
board.WriteI2C(desAddr,0x41,0x5)
board.WriteI2C(desAddr,0x42,0x7c) #Set NDIV = 124
board.WriteI2C(desAddr,0x41,0x18)
board.WriteI2C(desAddr,0x42,0xf6) #Set DEN = 16777206
board.WriteI2C(desAddr,0x42,0xff)
board.WriteI2C(desAddr,0x42,0xff)
board.WriteI2C(desAddr,0x41,0x1e)
board.WriteI2C(desAddr,0x42,0xf6) #Set NUM = 16777206
board.WriteI2C(desAddr,0x42,0xff)
board.WriteI2C(desAddr,0x42,0xff)
board.WriteI2C(desAddr,0x41,0x14)
board.WriteI2C(desAddr,0x42,0xB2) #Set Spread Type = Center and Set RAMPX_INC = 24966
board.WriteI2C(desAddr,0x41,0x15)
board.WriteI2C(desAddr,0x42,0x64)
board.WriteI2C(desAddr,0x41,0x16)
board.WriteI2C(desAddr,0x42,0xCC) #Set RAMPX_STOP = 210
board.WriteI2C(desAddr,0x41,0x17)
board.WriteI2C(desAddr,0x42,0x40)
board.WriteI2C(desAddr,0x41,0x4)
board.WriteI2C(desAddr,0x42,0x9) #Set PLL Order to Fractional
board.WriteI2C(desAddr,0x01,0x01) # Digital Reset
```

8.3.4.1.1 Back Channel SSCG Calculations

The FPD PLL must be configured in fractional mode to enable SSCG. If the PLL was originally configured in integer mode (NUM[23:0] = 0), set NUM[23:0] equal to the value of DEN[23:0], and subtract one from the original NDIV[15:0] value. Additionally, set MASH_ORDER to fractional mode (e.g. MASH_ORDER[2:0] = 2).

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For instance, to enable SSCG using the default FPD-Link IV PLL settings set NDIV = 124 and NUM[23:0] = 16,777,206. To configure spread spectrum clock generation, the following equations can be used to calculate the RAMPX_STOP and RAMPX_INC.

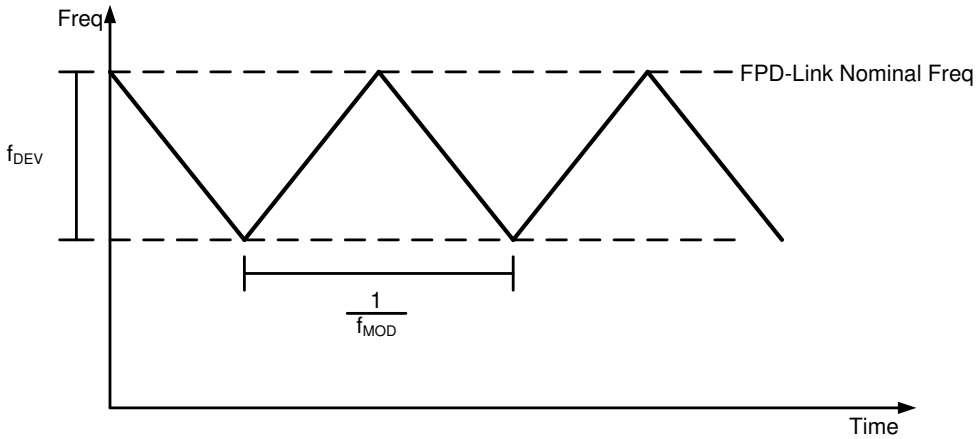

Figure 8-2. Down Spread SSCG

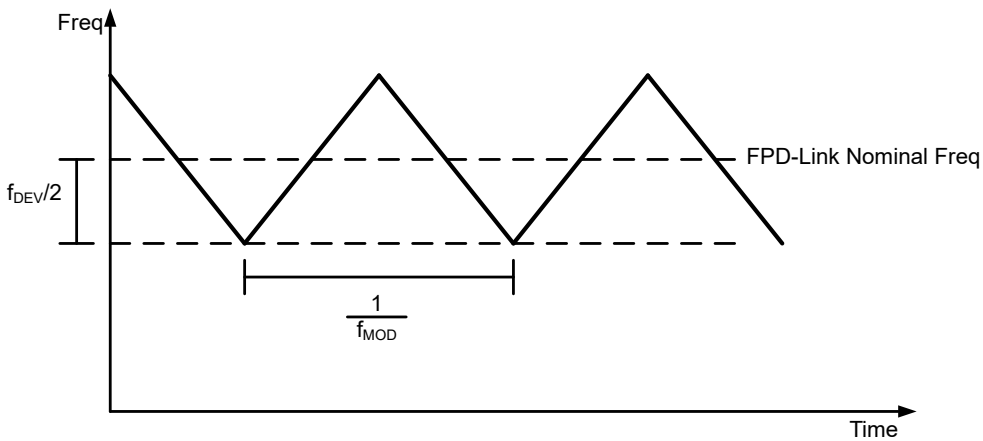

Figure 8-3. Center Spread SSCG

$$RAMPX_STOP = \frac{f_{REF}}{(4 \times f_{MOD})} \tag{29}$$

where

- f_{REF} is the reference clock in kHz (27000)
- f_{MOD} is the modulation frequency in kHz

$$RAMPX_INC_{Initial} = \frac{(VCO_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP)} \tag{30}$$

- $RAMPX_INC_{Initial}$ must be rounded to an integer number

where

- f_{DEV} is the deviation frequency as a percentage of the back channel frequency (Example: deviation frequency = 0.5% = f_{DEV} = 0.5)
- i_{SPREAD} = 2
- $DEN_{Initial}$ is the denominator of the N-divider in the FPD PLL (16,777,206 for FPD-Link IV Mode)
- REFCLK is the reference clock frequency in MHz (27)

- VCO_freq is the VCO frequency in MHz

$$x = \begin{cases} \log_2 \dfrac{RAMPX_INC_{Initial}}{32767}, & RAMPX_INC_{Initial} > 32767 \\ 0, & RAMPX_INC_{Initial} \le 32767 \end{cases} \tag{31}$$

where

- x must be rounded up to the nearest integer

$$RAMPX_INC_{Final} = \frac{(VCO_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP \times 2^x)} \tag{32}$$

$$DEN_{Final} = \left(\frac{DEN_{Initial}}{2^x}\right) \tag{33}$$

$$NUM_{Final} = \left(\frac{NUM_{Initial}}{2^x}\right) \tag{34}$$

where

- Initial numerator and denominator are determined based on the FPD-Link rate. If the original PLL setting is integer mode (numerator = 0) then the first step of applying SSCG is to convert to fractional mode (subtract one from the integer part of the n divider and set both numerator and denominator to 16,777,206).

$$VCO_{Freq,Final} = f_{REF} \times 2\left[Ndiv + \left(\frac{NUM_{Final}}{DEN_{Final}}\right)\right] \tag{35}$$

$$f_{DEV,Final} = \left[\frac{(RAMPX_INC_{Final} \times REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP)}{(VCO_{Freq,Final} \times DEN_{Final})}\right] \tag{36}$$

8.3.5 FPD-Link Port Register Access

Since the DS90UH984-Q1 contains two upstream ports, some registers need to be duplicated to allow control and monitoring of the two ports. To facilitate this, a PORT_SEL register 0x0E controls access to the two sets of registers. Registers that are shared between ports (not duplicated) will be available independent of the settings in the PORT_SEL register. Setting the READ_PORT bit will allow a read of the register for the selected port. Writes will occur to any port for which the WRITE_PORT_x select bit is set, allowing simultaneous writes to both ports if both write bits are set.

8.3.6 Power Down (PDB)

The deserializer has a PDB input pin to enable or power down the device. This pin may be controlled by an external device, or through VDD18, where VDD18 is between 1.71 V and 1.89 V. To save power, disable the device when the display is not needed (PDB = LOW). When turning the device back on, ensure that this pin is not driven HIGH before all power supplies have stabilized. This can be achieved through software programming when this pin is connected to an external device, or by using a RC circuit when this pin is connect to the VDD18 power rail. A 10 kΩ resistor and a >10 uF cap are recommended.

Pulling PDB LOW will power down the device and reset all control registers to default. During this time, PDB must be held low for a minimum of 2 ms before going high again.

8.3.7 Internal ADC

The deserializer device contains an 8-bit ADC that is used for various functions including line fault detection, temperature sensing, internal voltage sensing and external voltage monitoring. This ADC is configured using

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indirect register Page_27 in the deserializer devices. To enable the ADC, set the ADC_MODE (0x0D[7] = 0) on Page_27). The ADC can read the voltage of up to 11 different sources. These sources can be enabled or disabled in register 0x07 or 0x08 on Page_27. By default the ADC reads 5 voltage sources: the thermal sense element, and 4 internal supply voltages. Refer to *Diagnostic Features of FPD-Link IV Devices* for more details on ADC sources, update frequency configuration, and other configuration details.

8.3.7.1 Temperature Sensing

The DS90UH984-Q1 uses the ADC and a thermal sense element to measure the junction temperature of the DS90UH984-Q1. The junction temperature is periodically read and stored in the TEMP_FINAL (0x13) register on the ADC control register Page_27. The formula to convert the TEMP_FINAL to Celsius is below. The TEMP_FINAL has a resolution of 2°C.

$$Temperature = \left(2 \times TEMP_FINAL\right) - 273 \tag{37}$$

The DS90UH984-Q1 can also trigger an interrupt when the junction temperature exceeds the value of the TEMP_HIGH (0x33) register or falls below the TEMP_LOW (0x34) register on page_27. To enable this interrupt status, set bit 6 of the SAR_ADC_ICR_ISR (0xCE[6]) register on the main page to 1. By default, this interrupt will be triggered when internal junction temperatures exceed 140 °C or below -20 degrees C. These thresholds can be changed by writing to the TEMP_HIGH or TEMP_LOW register. For more details about temperature register settings, refer to *Diagnostic Features of FPD-Link IV Devices*.

8.3.7.2 Internal Supply Monitoring

The deserializer device uses the ADC to monitor the voltage levels of the 1.8V and 1.15V voltage supplies of the device. The ADC can read the voltages of four different pins of the device. Table 8-14 shows the register and pin locations for the four ADC voltage readings. The voltage sensors have a resolution of 2.5% for 1.15V and 1.8V.

For details information on registers setting refer to Page_27 Registers

Table 8-14. Voltage Sensing

Pin Number	Pin Name	Nominal Voltage	Register Name	Register Address (Page_27)	Correction Factor (CF)
40	VDD18_TXPLL pin	1.8V	IV0_FINAL	0x15	3.02
35	VDD18_D pin	1.8V	IV1_FINAL	0x16	3.02
36	VDD11_TX1 pin	1.15V	IV2_FINAL	0x17	1.868
19 and 55	VDD11_D pin	1.15V	IV3_FINAL	0x18	1.868

- Voltage equation for voltage sense

$$Pin_Voltage = CF * (1 / 255)* 1.207 * IVx_FINAL \tag{38}$$

The deserializer device can also trigger an interrupt when the voltage supply goes above or below specific voltages. To enable this interrupts status, set bit 5 of the SAR_ADC_ICR_ISR (0xCE[5]) register on the main page to 1. The voltage threshold values in Table 8-15 below, are the recommended voltage values and they are +/- 5% of the Nominal Voltage. Within these thresholds, the device is expected to follow the specs provided in the datasheet. The upper or lower voltage thresholds can be changed by changing the values of the IVx_HIGH and IVx_LOW registers in Page_27. Upper and lower voltage thresholds are calculated using Equation 38.

Table 8-15. Upper or Lower Internal Supply Voltage Threshold

Pin	Upper Voltage Threshold (V)	Upper Voltage Threshold Register (on Page_27)	Lower Voltage Threshold (V)	Lower Voltage Threshold Register (on Page_27)
VDD18_TXPLL pin	1.902	0x39	1.732	0x3A
VDD18_D pin	1.902	0x3C	1.732	0x3D
VDD11_TX1 pin	1.164	0x3F	1.060	0x40
VDD11_D pin	1.164	0x42	1.060	0x43

8.3.7.3 External Voltage Sensing

The ADC on the device can read and monitor the voltages of the GPIO6 and GPIO8 pins. The pins can read voltages from 0.4V to 1.207V. If a higher voltage is to be read, an external voltage divider is required. In order to read the voltage at the GPIO you must enable EXT_VOL0 (0x08[0]) for GPIO6 and EXT_VOL1 (0x08[1]) for GPIO8 on Page_27. Disable the 25KΩ pull down on GPIO6 by setting GPIO_EN_PULL_LOW_1 (0x0B[6]) on Page_15 to 0. Disable the 25KΩ pull down on GPIO8 by setting GPIO_EN_PULL_LOW_8 (0x0C[0]) on Page_15 to 0. The ADC voltage can be read in EXT_VOL0_FINAL (Page_27 0x1B) for GPIO6 and EXT_VOL1_FINAL (Page_27 0x1C) for GPIO8. The formula to convert the ADC reading to the voltage is in the Equation below. Refer to registers information in Page_27 Registers.

$$GPIOx_Voltage = \left(\frac{1.207}{255}\right) \times EXT_VOLx_FINAL \tag{39}$$

The device can also trigger an interrupt when the voltages on GPIO6 and GPIO8 go above or below specific voltages. To enable these interrupts, set bit 5 of the SAR_ADC_ICR_ISR (0xCE[5]) register on the main page to 1. The registers to set the upper and lower voltages are in Table 8-16. Upper and lower voltage thresholds are calculated using Equation 39.

Table 8-16. Upper or Lower External Voltage Threshold

Description	Register Name	Register Address (Page_27)
GPIO6 Upper Threshold	EXT_VOL0_HIGH	0x4C
GPIO6 Lower Threshold	EXT_VOL0_LOW	0x4D
GPIO8 Upper Threshold	EXT_VOL1_HIGH	0x4F
GPIO8 Lower Threshold	EXT_VOL1_LOW	0x50

8.3.8 Serial Link Fault Detect

As part of the diagnostic features of DS90UH984-Q1, the line fault detection circuitry can be used to detect faults with the connection between the serializer and deserializer. This is done by monitoring and sensing the voltage on the cable between the SerDes and transmitting that voltage to a GPIO on either the serializer or deserializer. Refer to application note *Diagnostic Features of FPD-Link IV Devices*, "SNLA322" for more details.

Line-fault detection is available for FPD-Link IV devices in a daisy-chain configuration, provided there is register access to the device. Figure 8-4 shows an example of line-fault circuit implementation for a daisy-chain configuration. There is only one set of line-fault detection circuitry necessary to monitor each cable.

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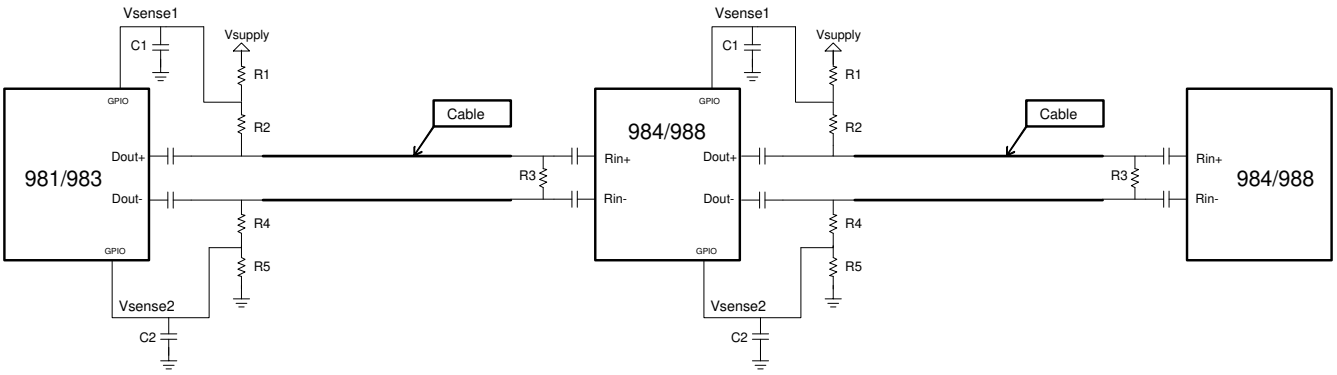

Figure 8-4. Daisy-Chain Example Configuration

8.3.9 Interrupt Pin (INTB_IN)

The INTB_IN pin is an active low interrupt input pin. This interrupt signal, when enabled, will propagate to the paired serializer. Consult the appropriate serializer datasheet for details of how to configure this interrupt functionality.

The following sequence is an example use-case of the INTB_IN pin:

1. INTB_IN and REM_INTB functionality must be enabled via setting register RX_INTN_CTL (0x44) bit 7 to 1.
2. Deserializer INTB_IN (pin 45) is set LOW by some downstream device.
3. Serializer pulls REM_INTB pin LOW. The signal is active LOW, so a LOW indicates an interrupt condition.
4. External controller detects REM_INTB = LOW; to determine interrupt source, read ISR register.
5. A read to ISR will clear the interrupt at the Serializer, releasing REM_INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INTB_IN. This would be when the downstream device releases the INTB_IN (pin 45) on the Deserializer. The system is now ready to return to step (1) at next falling edge of INTB_IN.

8.3.10 General-Purpose I/O

8.3.10.1 GPIO[13:0] Configuration

In normal operation, GPIO[13:0] may be used as general purpose inputs or outputs. GPIO modes are configured in the GPIOx_PIN_CTL registers (0x15 - 0x22). See Table 8-17 for GPIO configuration.

8.3.10.2 GPIO Input Control and Status

Upon initialization GPIO0 through GPIO3 and GPIO7 through GPIO13 are enabled as inputs by default. GPIO4 through GPIO6 are enabled as outputs by default, each communicating a link lock status. When the GPIO pin is configured as an input, the internal pull-down circuit for the GPIO is enabled. The GPIO_IN_EN1 (Main_Page 0x12) and GPIO_IN_EN0 (Main_Page 0x13) registers allow control of the input enable or disable for each respective GPIO. The GPIOx_OUTPUT_EN field in GPIOx_PIN_CTL enables or disables the GPIO as an output. For example, to disable GPIO1 and GPIO2 as inputs the user would program register 0x13[2:1] = 00. When a GPIO is configured as an input (GPIOx_INPUT_EN =1), the corresponding GPIOx_PIN_CTL[7] must be set to 0. When configured as an input, the status HIGH or LOW of each GPIO may be read through the GPIO_PIN_STS1 (0x10) and the GPIO_PIN_STS2 (0x11) registers.

8.3.10.3 GPIO Output Control

Individual GPIO output pin control is programmable through the GPIOx_PIN_CTL registers 0x15 to 0x22. To enable any of the GPIOs as an output, first disable GPIO as an input in register 0x12 and 0x13, and then set GPIOx_PIN_CTL[7] =1 in the respective register 0x15 to 0x22 to enable GPIO as an output. The configuration register for each GPIO is listed in Table 8-17.

Table 8-17. GPIOx Output Function Programming

GPIO OUTPUT FUNCTION	SOURCE	GPIO OUTPUT ENABLE GPIOx_PIN_CTL[7]	GPIOX OUTPUT SOURCE SELECT GPIOx_PIN_CTL[6:5]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[4:0]
GPIOx Output Disabled	X	0	X	X
GPIOx linked to BC_GPIO0	Received from Daisy-chain Port 0	1	00	00000
GPIOx linked to BC_GPIO1		1	00	00001
GPIOx linked to BC_GPIO2		1	00	00010
GPIOx linked to BC_GPIO3		1	00	00011
GPIOx linked to BC_GPIO4		1	00	00100
GPIOx linked to BC_GPIO5		1	00	00101
GPIOx linked to BC_GPIO6		1	00	00110
GPIOx linked to BC_GPIO7		1	00	00111
GPIOx linked to BC_GPIO8		1	00	01000
GPIOx linked to BC_GPIO9		1	00	01001
GPIOx linked to BC_GPIO10		1	00	01010
GPIOx linked to BC_GPIO11		1	00	01011
GPIOx linked to BC_GPIO12		1	00	01100
GPIOx linked to BC_GPIO13		1	00	01101
GPIOx linked to BC_GPIO14		1	00	01110
GPIOx linked to BC_GPIO15		1	00	01111
GPIOx linked to Remote Interrupt		1	00	10000
GPIOx linked to Daisy Chain Lock Detect		1	00	10001
GPIOx linked to FPD TX Interrupt (active low)		1	00	10010
GPIOx linked to FPD TX Interrupt (active high)		1	00	10011
Received FC_GPIO0	Received from forward channel (both FPD3 and FPD4)	1	00	10100
Received FC_GPIO1		1	00	10101
Received FC_GPIO2		1	00	10110
Received FC_GPIO3		1	00	10111
FPD4 BIST Pass Status	FPD-Link IV Mode Only	1	00	11000
Received FC_GPIO4	Received from Forward channel FPD-Link III Mode Only	1	00	
Received FC_GPIO5		1	00	11001
Received FC_GPIO6		1	00	11010
Received FC_GPIO7		1	00	11011
RX Lock Detect	Received from Forward channel	1	00	11100
FPD3 BIST Pass Status	FPD-Link III Mode Only	1	00	11101
Local Interrupt Status	Local Status	1	00	11110
Reserved	Reserved	1	00	11111

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Table 8-17. GPIOx Output Function Programming (continued)

GPIO OUTPUT FUNCTION	SOURCE	GPIO OUTPUT ENABLE GPIOx_PIN_CTL[7]	GPIOX OUTPUT SOURCE SELECT GPIOx_PIN_CTL[6:5]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[4:0]
GPIOx linked to BC_GPIO0	Received from Daisy-chain Port 1	1	01	00000
GPIOx linked to BC_GPIO1		1	01	00001
GPIOx linked to BC_GPIO2		1	01	00010
GPIOx linked to BC_GPIO3		1	01	00011
GPIOx linked to BC_GPIO4		1	01	00100
GPIOx linked to BC_GPIO5		1	01	00101
GPIOx linked to BC_GPIO6		1	01	00110
GPIOx linked to BC_GPIO7		1	01	00111
GPIOx linked to BC_GPIO8		1	01	01000
GPIOx linked to BC_GPIO9		1	01	01001
GPIOx linked to BC_GPIO10		1	01	01010
GPIOx linked to BC_GPIO11		1	01	01011
GPIOx linked to BC_GPIO12		1	01	01100
GPIOx linked to BC_GPIO13		1	01	01101
GPIOx linked to BC_GPIO14		1	01	01110
GPIOx linked to BC_GPIO15		1	01	01111
GPIOx linked to Remote Interrupt		1	01	10000
GPIOx linked to Daisy Chain Lock Detect		1	01	10001
GPIOx linked to FPD TX Interrupt (active low)		1	01	10010
GPIOx linked to FPD TX Interrupt (active high)		1	01	10011
Received FC_GPIO0	Received from forward channel (both FPD3 and FPD4)	1	01	10100
Received FC_GPIO1		1	01	10101
Received FC_GPIO2		1	01	10110
Received FC_GPIO3		1	01	10111
FPD4 BIST Pass Status	FPD-Link IV Mode Only	1	01	11000
RX Lock Detect	Received from Forward channel	1	01	11001
Reserved	Reserved	1	01	11010-11100
FPD3 BIST Pass Status	FPD-Link III Mode Only	1	01	11101
Local Interrupt Status	Local Status	1	01	11110
Reserved	Reserved	1	01	11111

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Table 8-17. GPIOx Output Function Programming (continued)

GPIO OUTPUT FUNCTION	SOURCE	GPIO OUTPUT ENABLE GPIOx_PIN_CTL[7]	GPIOX OUTPUT SOURCE SELECT GPIOx_PIN_CTL[6:5]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[4:0]
GPIOx linked to fixed output value of 0	Local Device	1	10	00000
GPIOx linked to fixed output value of 1		1	10	00001
GPIOx linked to FPD-Link RX mode dependent Lock indication from enabled RX Ports. If dual mode, logical AND of port 0 and port 1 RX Lock indication. If single mode, port 0 RX Lock indication only.		1	10	00010
GPIOx linked to logical OR of RX Lock indication from enabled RX Ports		1	10	00011
GPIOx linked to logical AND of RX Lock indication from enabled RX Ports		1	10	00100
Reserved	Reserved	1	10	00101
GPIOx linked to logical OR of RX Lock indication from enabled TX Ports (daisy chain)	Local Device	1	10	00110
GPIOx linked to logical AND of RX Lock indication from enabled TX Ports (daisy chain)		1	10	00111
I2S_DD		1	10	01000
I2S_DC		1	10	01001
I2S_WS		1	10	01010
I2S_DB		1	10	01011
I2S_DA		1	10	01100
I2S_CLK		1	10	01101
Inverted I2S_CLK		1	10	01110
I2S clock from FPD PLL		1	10	01111
GPIOx linked to FPD-Link TX mode dependent Lock indication from enabled TX Ports (daisy chain). If dual mode, logical AND of port 0 and port 1 RX Lock indication. If single mode, port 0 RX Lock indication only.		1	10	10000
Reserved	Reserved	1	10	10001-11111
GPIOx linked to FC_GPIO0	Received from RX Port 0	1	11	00000
GPIOx linked to FC_GPIO1		1	11	00001
GPIOx linked to FC_GPIO2		1	11	00010
GPIOx linked to FC_GPIO3		1	11	00011
GPIOx linked to FC_GPIO4	Received from RX Port 0 in FPD3 Mode only	1	11	00100
GPIOx linked to FC_GPIO5		1	11	00101
GPIOx linked to FC_GPIO6		1	11	00110
GPIOx linked to FC_GPIO7		1	11	00111
Reserved	Reserved	1	11	01000-01111

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Table 8-17. GPIOx Output Function Programming (continued)

GPIO OUTPUT FUNCTION	SOURCE	GPIO OUTPUT ENABLE GPIOx_PIN_CTL[7]	GPIOX OUTPUT SOURCE SELECT GPIOx_PIN_CTL[6:5]	GPIOX OUTPUT FUNCTION SELECT GPIOx_PIN_CTL[4:0]
GPIOx linked to BC_GPIO0	Received from RX Port 1	1	11	10000
GPIOx linked to BC_GPIO1		1	11	10001
GPIOx linked to BC_GPIO2		1	11	10010
GPIOx linked to BC_GPIO3		1	11	10011
GPIOx linked to BC_GPIO4	Received from RX Port 1	1	11	10100
GPIOx linked to BC_GPIO5		1	11	10101
GPIOx linked to BC_GPIO6		1	11	10110
GPIOx linked to BC_GPIO7		1	11	10111
GPIOx linked to BC_GPIO8	Received from RX Port 1 in FPD4 Mode only	1	11	11000
GPIOx linked to BC_GPIO9		1	11	11001
GPIOx linked to BC_GPIO10		1	11	11010
GPIOx linked to BC_GPIO11		1	11	11011
GPIOx linked to BC_GPIO12	Received from RX Port 1 in FPD4 Mode only	1	11	11100
GPIOx linked to BC_GPIO13		1	11	11101
GPIOx linked to BC_GPIO14		1	11	11110
GPIOx linked to BC_GPIO15		1	11	11111

8.3.10.4 Forward Channel GPIO Configuration

The DS90UH984-Q1 can recover forward channel GPIO data sent by the partner serializer. When GPIO[13:0] pins are configured to output forward channel GPIOs, the effective GPIO frequency will depend on the number of Forward Channel GPIOs assigned at the partner serializer, forward channel line rate, and number of daisy-chain hops. Consult the appropriate serializer datasheet for details on how to configure the serializer to send GPIO data on the forward channel using the serializer registers.

When a single GPIO input from the serializer is linked to a DS90UH984-Q1 deserializer, the GPIO output value is sampled every other forward channel frame. When two forward channel GPIOs are configured, each GPIO is sampled twice every ten frames. When three or four forward channel GPIOs are configured, each individual GPIO will be sampled every ten frames.

Daisy-Chain Hops	Link Rate	Max Recommended GPIO Frequency (MHz)			Max Jitter (us)		
		1 GPIO	2 GPIO	4 GPIO	1 GPIO	2 GPIO	4 GPIO
1 Link (1 Ser, 1 Des)	13.5	10.227	5.113	2.556	0.039	0.078	0.117
	12.528	9.49	4.745	2.372	0.042	0.084	0.126
	10.8	8.181	4.09	2.045	0.048	0.097	0.146
	6.75	5.113	2.556	1.278	0.078	0.156	0.234
	3.375	2.556	1.278	0.639	0.156	0.312	0.469
2 Links (1 Ser, 2 Des)	13.5	5.113	2.556	1.704	0.078	0.156	0.234
	12.528	4.745	2.372	1.581	0.084	0.168	0.252
	10.8	4.09	2.045	1.363	0.097	0.195	0.293
	6.75	2.556	1.278	0.852	0.156	0.312	0.469
	3.375	1.278	0.639	0.426	0.312	0.625	0.938
3 Links (1 Ser, 3 Des)	13.5	3.409	1.704	1.136	0.117	0.234	0.352
	12.528	3.163	1.581	1.054	0.126	0.252	0.379
	10.8	2.727	1.363	0.909	0.146	0.293	0.44
	6.75	1.704	0.852	0.568	0.234	0.469	0.704
	3.375	0.852	0.426	0.284	0.469	0.938	1.408

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Daisy-Chain Hops	Link Rate	Max Recommended GPIO Frequency (MHz)			Max Jitter (us)		
		1 GPIO	2 GPIO	4 GPIO	1 GPIO	2 GPIO	4 GPIO
4 Links (1 Ser, 4 Des)	13.5	2.556	1.278	0.852	0.156	0.312	0.469
	12.528	2.372	1.186	0.79	0.168	0.337	0.505
	10.8	2.045	1.022	0.681	0.195	0.391	0.586
	6.75	1.278	0.639	0.426	0.312	0.625	0.938
	3.375	0.639	0.319	0.213	0.625	1.251	1.877

8.3.10.5 Back Channel GPIO Configuration

The DS90UH984-Q1 can assign a GPIO pin input status to available back channel GPIO slots to send over the back channel. Each back channel frame carries 4 GPIO slots. 1, 4, 8, or 16 back channel GPIOs can be supported. The number of BC GPIOs configuration is done through indirect register Page_1 register 0x20[1:0]. The effective GPIO frequency will depend on the number of back channel GPIOs slots assigned as well as the back channel line rate. See Table 8-18.

Table 8-18. Maximum Effective Back-Channel GPIO Speed

Number of GPIOs		1	4	8	16
Sampling Frequency	168.75 Mbps BC	5.625 MHz (168.75/30)	1.406 MHz (168.75/30/4)	703.125 kHz (168.75/30/8)	351.563 kHz (168.75/30/16)
Recommended GPIO Frequency	168.75 Mbps BC (4x oversampling)	1.406 MHz	351.563 kHz	175.781 kHz	87.891 kHz
Max Jitter (ns)	1 Link (1 Ser, 1 Des)	177.8(0.25 UI)	711.2(0.25 UI)	1422.2(0.25 UI)	2844.4(0.25 UI)
	2 Links (1 Ser, 2 Des)	N/A	853.5(0.3 UI)	1706.7(0.3 UI)	3413.3(0.3 UI)
	3 Links (1 Ser, 3 Des)	N/A	995.7(0.35 UI)	1991.1(0.35 UI)	3982.2(0.35 UI)
	4 Links (1 Ser, 4 Des)	N/A	1138.0(0.4 UI)	2275.6(0.4 UI)	4551.1(0.4 UI)
Max Latency (us)	1 Link (1 Ser, 1 Des)	1	1	2	3
	2 Links (1 Ser, 2 Des)	N/A	2	4	6
	3 Links (1 Ser, 3 Des)	N/A	3	6	9
	4 Links (1 Ser, 4 Des)	N/A	4	8	12

Any of the fourteen GPIO pin data can be mapped to send over the available back channel slots. The same GPIO data on the deserializer pin can be mapped to multiple back channel GPIO slots. GPIOs may also be configured to send information received from the FPD-Link III or FPD-Link IV daisy-chain on either port. For more information, see Section 8.3.10.6.2.

8.3.10.6 GPIOs Over Daisy-Chain

8.3.10.6.1 Forward Channel GPIO Over Daisy-Chain

DS90UH984-Q1 supports forwarding up to four GPIO signals on each FPD-Link III or FPD-Link IV daisy-chain output to downstream devices. GPIO signals may be forwarded from FPD-Link III or FPD-Link IV input GPIO signals. GPIO data originating from Port 0 will always be forwarded to daisy-chain port 0, and GPIO data originating from Port 1 will always be forwarded to daisy-chain port 1.

8.3.10.6.2 Back Channel GPIO Over Daisy-Chain

DS90UH984-Q1 supports receiving up to 16 GPIO signals from each FPD-Link III or FPD-Link IV daisy-chain channel. GPIO signals received from either FPD-Link III or FPD-Link IV daisy-chain channel can be sent to upstream devices or outputted to local GPIOs. Configuration of each back channel GPIO signal is flexible, allowing any GPIO signal to be sent on any back channel GPIO. For each port, the following GPIO control is available through the BC_GPIO_CTLx registers in indirect register Page_1 0x10 to 0x1F:

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Table 8-19. Back Channel GPIO Over Daisy-Chain Configuration

Register Name	Bits	Bits Name	Description
BC_GPIO_CTLx	7:0	BC_GPIOx_SEL	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Port 0 backchannel 0x11: Port 1 backchannel 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x33: Reserved 0x34: EDID read status interrupt (Reg 0x75 on page 1) 0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 0 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 0 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 0 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 0 SM interrupt (0xEA on Page 11)

8.3.11 Interrupts

The DS90UH984-Q1 has several local and remote interrupt conditions. To enable interrupt statuses. the global interrupt must be enabled as well as the individual interrupts of interest via the INTERRUPT_CTL register 0x52.

Table 8-20. Interrupt Statuses

Status	Address	Description
Global Interrupt (GLOBAL_INT)	0x51[7]	Set when any of the enabled 0x51/0x52 register interrupts is set
DP/eDP Transmitter Interrupt Port 1 Interrupt (IS_DP1)	0x51[6]	Set when any of interrupt occurred for the DP/eDP transmitter port 0
FPD Transmitter Port 1 Interrupt (IS_FPD_TX1)	0x51[5]	Set when any of interrupt occurred for the FPD-Link transmitter port 1
EDID Read Interrupt (IS_EDID_RD)	0x51[4]	Set when any of interrupt occurred for the EDID read
DP/eDP Transmitter Interrupt Port 0 (IS_DP0)	0x51[3]	Set when any of interrupt occurred for the DP/eDP transmitter port 0
FPD Transmitter Port 0 Interrupt (IS_FPD_TX0)	0x51[2]	Set when any of interrupt occurred for the FPD-Link transmitter port 0
FPD Receiver Interrupt (IS_FPD_RX)	0x51[1]	Set when any of interrupt occurred for the FPD-Link receiver
INTB_IN Interrupt (IS_INTB_IN)	0x51[0]	Set when interrupt occurred on the INTB_IN pin

8.3.12 Internal Pattern Generation

The DS90UH984-Q1 deserializer provides an internal pattern generation feature. It allows basic testing and debugging of a panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no input is applied.

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8.3.12.1 Pattern Options

The DS90UH984-Q1 deserializer pattern generator is capable of generating 20 default patterns for use in basic testing and debugging of panels. Each can be inverted using register bits, shown below:

1. Checkerboard (White/Black)
2. White
3. Black
4. Red
5. Green
6. Blue
7. Horizontally Scaled Black to White
8. Horizontally Scaled Black to Red
9. Horizontally Scaled Black to Green
10. Horizontally Scaled Black to Blue
11. Vertically Scaled Black to White
12. Vertically Scaled Black to Red
13. Vertically Scaled Black to Green
14. Vertically Scaled Black to Blue
15. Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers
16. VCOM (Yellow, Cyan, Yellow, Red)
17. Alternate VCOM (Blue, Cyan, Yellow, Red)
18. Custom Color Checkerboard (Custom/Black)
19. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) – Note: not included in the auto-scrolling feature
20. UNH-IOL MIPI Compliance Test Pattern

Due to the quad pixel clock architecture of the FPD-Link IV deserializer devices, patterns #7-10 (horizontally scaled patterns) and #19 (color bars) should only be used when the active line length meets a minimum number of pixels based on the configured bits per color. If the minimum horizontal pixel count is not met, then the pattern will not correctly scale to the screen size (ex. less than 8 color bars shown). If the screen size does not meet the minimum number of horizontal pixels, then it is suggested to use one of the other available patterns instead.

Table 8-21. Minimum Pixels Per Line for PATGEN Horizontally Scaled or Color Bar Patterns

PATGEN Bits Per Pixel	Minimum Active Horizontal Pixels
30bpp	4096
24bpp	1024
18bpp	256

8.3.12.2 Color Modes

By default, the Pattern Generator operates in 24-bit color mode, where all bits of the Red, Green, and Blue outputs are enabled. 18-bit or 30-bit color mode can be activated from the configuration registers. In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled; the 2 least significant bits will be 0.

8.3.12.3 Pattern Inversion

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

8.3.12.4 Auto Scrolling

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. Auto scrolling is enabled by setting field PATGEN_ASCRL to 1. A sequence of up to 16 patterns may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

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8.3.13 Backward Compatibility

The DS90UH984-Q1 deserializer is backward compatible to DS90Ux94x, and DS90Ux92x serializers/deserializers. To enable backward capability, set the desired channel to FPD-Link III mode via FPD4_RX_ENABLE_Px in FPD4_RX_CFG (0x31) Register.

Table 8-22. Backward Compatibility

Mode	Serializer	PCLK	Forward Channel Rate	Back Channel Rate	Input Format	Typical Resolution Supported
Single Link	DS90Ux925	25 MHz ≤ PCLK ≤ 85 MHz	875 Mbps to 2.975 Gbps	5 Mbps	RGB	720p
Single Link	DS90Ux927	25 MHz ≤ PCLK ≤ 85 MHz	875 Mbps to 2.975 Gbps	5 Mbps	oLDI	720p
Single Link	DS90Ux929	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	HDMI	900p / 720p
Single Link	DS90Ux941AS	25 MHz ≤ PCLK ≤ 105 MHz	875 Mbps to 3.675 Gbps	5 Mbps 10 Mbps 20 Mbps	DSI	900p / 720p
Single Link	DS90Ux947	25 MHz ≤ PCLK ≤ 96MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	900p / 720p
Single Link	DS90Ux949	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	HDMI	900p / 720p
Single Link	DS90Ux949A	25 MHz ≤ PCLK ≤ 105 MHz	875 Mbps to 3.675 Gbps	5 Mbps 10 Mbps 20 Mbps	HDMI	900p / 720p
Dual Link	DS90Ux941AS	50 MHz ≤ PCLK ≤ 210 MHz	875 Mbps to 3.675 Gbps per Link	5 Mbps 10 Mbps 20 Mbps	DSI	2K (2880x1080) / FHD (1920x1080)
Dual Link	DS90Ux947	50 MHz ≤ PCLK ≤ 170MHz	875 Mbps to 2.975 Gbps per Link	5 Mbps 10 Mbps 20 Mbps	oLDI	WUXGA (1920x1200) / FHD (1920x1080)
Dual Link	DS90Ux949	50 MHz ≤ PCLK ≤ 170 MHz	875 Mbps to 2.975 Gbps per Link	5 Mbps 10 Mbps 20 Mbps	HDMI	WUXGA (1920x1200) / FHD (1920x1080)
Dual Link	DS90Ux949A	50 MHz ≤ PCLK ≤ 210 MHz	875 Mbps to 3.675 Gbps per Link	5 Mbps 10 Mbps 20 Mbps	HDMI	2K (2880x1080) / FHD (1920x1080)
Daisy-chain Single Link	DS90UB924	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps	oLDI	900p/720p
	DS90Ux926	25 MHz ≤ PCLK ≤ 85 MHz	875 Mbps to 2.975 Gbps	5 Mbps	RGB	720p
	DS90Ux928	25 MHz ≤ PCLK ≤ 85 MHz	875 Mbps to 2.975 Gbps	5 Mbps	oLDI	720p
	DS90Ux940	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	900p / 720p
	DS90Ux940N	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	CSI-2	900p / 720p
	DS90Ux948	25 MHz ≤ PCLK ≤ 96 MHz	875 Mbps to 3.36 Gbps	5 Mbps 10 Mbps 20 Mbps	oLDI	900p / 720p

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Table 8-22. Backward Compatibility (continued)

Mode	Serializer	PCLK	Forward Channel Rate	Back Channel Rate	Input Format	Typical Resolution Supported
Daisy-chain Dual Link	DS90Ux948	50 MHz ≤ PCLK ≤ 192 MHz	875 Mbps to 3.36 Gbps per Link 1.75 Gbps to 6.72 for Dual Link	5 Mbps 10 Mbps 20 Mbps	oLDI	2K (2048x1080) / FHD (1920x1080)
	DS90Ux940	50 MHz ≤ PCLK ≤ 170 MHz	875 Mbps to 2.975 Gbps per Link 1.75 Gbps to 5.95 for Dual Link	5 Mbps 10 Mbps 20 Mbps	CSI-2	WUXGA (1920×1200) / FHD (1920x1080)
	DS90Ux940N	50 MHz ≤ PCLK ≤ 170 MHz	875 Mbps to 2.975 Gbps per Link 1.75 Gbps to 5.95 for Dual Link	5 Mbps 10 Mbps 20 Mbps	CSI-2	WUXGA (1920×1200) / FHD (1920x1080)

8.3.13.1 FPD-Link III RX Modes of Operation

The FPD-Link III RX mode supports several modes of operation, dependent on the upstream transmitter as well as the video being delivered. The following modes are supported. See Section 8.3.21.1.2 for FPD-Link III TX modes of operation.

8.3.13.1.1 FPD-Link III Single Link Operation

Single Link mode receives the video over a single FPD-Link III from a single transmitter. Single link mode supports frequencies up to 105 MHz for 24-bit video when paired with the DS90Ux941AS and DS90Ux949A or up to 96 MHz when paired with the DS90Ux947. This mode is compatible with the DS90Ux929 when operating below 96 MHz PCLK or compatible with DS90Ux927 and DS90Ux925 when operating below 85 MHz PCLK. If the upstream device is capable, the secondary FPD-Link III link may be used for high-speed control.

8.3.13.1.2 FPD-Link III Dual Link Operation

In FPD-Link III Dual Link mode, the FPD-Link III receiver assumes the data on both links comes from a single source. The transmitter must be capable of splitting a single video stream and sending alternating pixels on two downstream links. Dual link mode is capable of supporting a pixel clock frequency of up to 210 MHz, with each FPD-Link III RX port running at one-half the frequency. This allows support for full 2K video.

Dual Link mode may be enabled using the register FPD3_RX_CTL[5:4], as long as both FPD-Link ports are configured for FPD-Link III mode in both the FPD4_RX_ENABLE_P1 and FPD4_RX_ENABLE_P0 fields of FPD4_RX_CFG (0x31) Register.

8.3.13.1.3 Setting FPD-Link III Modes

The RX ports can be configured for FPD III mode using register 0x31[1:0]. In FPD III mode, the DS90UH984-Q1 automatically detects the capabilities of upstream links and can resolve whether a single device, or dual-capable device is connected. Alternatively, forced FPD III modes can be configured using register FPD3_RX_CTL (0x32) [5:4].

8.3.13.1.3.1 FPD-Link III Link Configuration with Low PCLKs

During FPD-Link III use on main-link, PCLKs below 30MHz in single FPD-Link III mode and 60MHz in dual FPD-Link mode require additional link configuration prior to lock. The following script for the serializer in use should be executed from the serializer to initialize the link:

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Initialization Script for 94x or 929 Serializers

```
FPD3_LOCK_TIME=0.03
DEV_ADDR_RX=0x58
value = board.ReadI2C(DEV_ADDR_TX, 0x5a)
if ((value&0x40)==1): #Check bit 6
    board.WriteI2C(DEV_ADDR_TX, 0x27, 0x10) #Reg 0x27[4]
time.sleep(FPD3_LOCK_TIME)
board.WriteI2C(DEV_ADDR_RX, 0x40, 5*4)
board.WriteI2C(DEV_ADDR_RX, 0x41, 0x66)
board.WriteI2C(DEV_ADDR_RX, 0x42, 0x30)
board.WriteI2C(DEV_ADDR_RX, 0x41, 0x76)
board.WriteI2C(DEV_ADDR_RX, 0x42, 0x30)
time.sleep(0.001)
board.WriteI2C(DEV_ADDR_TX, 0x27, 0x00)
time.sleep(FPD3_LOCK_TIME)
board.WriteI2C(DEV_ADDR_RX, 0x01, 0x01)
time.sleep(FPD3_LOCK_TIME)
```

Initialization Script for 92x (non-929) Serializers

```
FPD3_LOCK_TIME=0.03
DEV_ADDR_RX=0x58
board.WriteI2C(DEV_ADDR_TX, 0x27, 0x08) #Reg 0x27[3]
board.WriteI2C(DEV_ADDR_RX, 0x40, 5*4)
board.WriteI2C(DEV_ADDR_RX, 0x41, 0x66)
board.WriteI2C(DEV_ADDR_RX, 0x42, 0x30)
board.WriteI2C(DEV_ADDR_RX, 0x41, 0x76)
board.WriteI2C(DEV_ADDR_RX, 0x42, 0x30)
time.sleep(0.001)
board.WriteI2C(DEV_ADDR_TX, 0x27, 0x00)
time.sleep(FPD3_LOCK_TIME)
board.WriteI2C(DEV_ADDR_RX, 0x01, 0x01)
time.sleep(FPD3_LOCK_TIME)
```

8.3.14 HDCP

The HDCP cipher function is implemented in the deserializer per the HDCP v1.4 specification. The DS90UH984-Q1 provides HDCP decryption of audiovisual content when connected to an HDCP capable FPD-Link III serializer. HDCP authentication and shared key generation is performed using the HDCP control channel, which is embedded in the forward and backward channels of the serial link. On-chip non-volatile memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

HDCP v1.4 is only available on the main-link and when DS90UH984-Q1 is configured to FPD-Link III Mode. HDCP is not available on the daisy-chain.

8.3.15 Built-In Self Test (BIST)

An optional Built-In Self Test (BIST) feature supports testing of the high speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

8.3.15.1 Main-Link BIST Configuration and Status

The BIST mode is enabled at the deserializer by the BIST_EN field of TX_BIST_CTL_FPD3 (0x14) or BIST_CONTROL (0x2D) register. When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the back channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors.

Forward channel BIST errors are counted and stored in DS90UH984-Q1 register 0xB8 for FPD-Link IV mode and Page_5 register 0x64 for FPD-Link III mode. Consult the partner serializer datasheet on checking back channel BIST errors.

BIST can only be disabled from the deserializer. During BIST, remote access to the deserializer from the serializer is disabled.

8.3.15.2 Daisy-Chain BIST Configuration and Status

Daisy-chain forward channel BIST is activated at the downstream deserializer, a BIST enable signal is sent to the deserializer through the Back Channel. The local deserializer outputs a test pattern and drives the link at speed. The downstream deserializer detects the test pattern and monitors it for errors. The downstream deserializer stores errors over the forward channel in its registers. The local deserializer also tracks errors indicated by the CRC fields in each back channel frame. Enabling BIST mode does not cause loss of lock.

Step 1: The local deserializer is paired with downstream deserializer, BIST Mode is enabled via the register on the downstream deserializer. Right after BIST is enabled, part of the BIST sequence requires bit 0x05[5] be toggled on the local deserializer (set 0x05[5]=1, then set 0x05[5]=0).

Step 2: An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link interface to the deserializer. Once the local deserializer and the downstream deserializer are in BIST mode, the downstream deserializer starts checking the data stream. If an error is detected, it is indicated in the error registers of the downstream deserializer. On the local deserializer, errors on the back channel are monitored and stored in the BIST_BC_ERROR register (0x6E).

Step 3: BIST is stopped via the downstream deserializer register and the downstream deserializer stops checking the data. The final test result is held in BIST_BC_ERROR and the BIST error register on the downstream deserializer. The BIST duration is user-controlled by the duration between enabling BIST mode and disabling BIST mode.

**BIST can only be disabled from the downstream deserializer. During BIST remote access to the downstream deserializer from the local deserializer is disabled.

8.3.16 Video Stream Mapping

When paired with compatible DS90Ux98x serializers, the DS90UH984-Q1 can support a maximum of 6 video streams. Each video stream can be mapped to any of the two DP/eDP output ports and to the daisy-chain outputs.

8.3.16.1 FPD-Link IV Input Map to DP/eDP Ports

For video streams originating from an FPD-Link IV source, register 0xD0[3:2] can be used to enable video stream mapping to DP/eDP ports. Once FPD-Link IV to display mapping is enabled, register 0xD6[5:3] and 0xD6[2:0] are used to control which video stream is mapped to the DP/eDP ports. By default, Video Stream 0 is mapped to DP/eDP Port 0 and Video Stream 1 is mapped to DP/eDP Port 1.

Figure 8-5. Video Stream to DP/eDP Port mapping

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For example, to map Video Stream 0 to DP/eDP Port 0, register 0xD0[2] shall be set to 1 and then register 0xD6[2:0] shall be set to 0x0. To map Video Stream 4 to DP/eDP Port 1, register 0xD0[3] shall be set to 1 and then register 0xD6[5:3] shall be set to 0x4.

8.3.16.2 FPD-Link IV Input Mapping to FPD-Link IV Daisy-Chain Outputs

Video streams originating from an FPD-Link IV source can be mapped to an FPD-Link IV daisy-chain output port. Daisy-chain outputs can forward up to 6 video streams. Register 0xD1[5:0] controls the number of video streams being forwarded. By default, each input video stream is mapped to the corresponding output video stream (i.e. input video stream 0 is mapped to output video stream 0). Register 0xD2 to 0xD4 can be used to change the default mapping method.

Each forwarded video stream requires to have the horizontal and vertical sync polarities set in Page_17 registers FPD_TX_HPOL_SEL 0x30 and FPD_TX_VPOL_SEL 0x31, and then enabled by setting field FPD_TX_POL_SEL_EN register 0x32[0] to 1.

8.3.16.3 FPD-Link IV Input Mapping to FPD-Link III Daisy-Chain Outputs

Video streams originating from FPD-Link IV source can be mapped to FPD-Link III daisy-chain output ports. In single or independent daisy-chain output mode, each daisy-chain output can forward one video stream. Register 0xD5[5:3] selects which video stream is forwarded through Daisy-chain Port 1. Register 0xD5[2:0] selects which video stream is forwarded through Daisy-chain Port 0.

8.3.16.4 FPD-Link III Input Mapping to DP/eDP Ports

When a video originated from an FPD-Link III source, register 0xD7[3:2] can be used to enable video stream mapping to DP/eDP ports. Register 0xD7[3] controls video mapping to DP/eDP Port 1 and register 0xD7[2] controls video mapping to DP/eDP Port 0. Since FPD-Link III sources can only carry a single video stream, video stream selection is not available.

8.3.16.5 FPD-Link III Input Mapping to FPD-Link III Daisy-Chain Outputs

Video originating from FPD-Link III sources can be mapped to FPD-Link III daisy-chain output ports. Register 0xD7[1:0] controls which daisy-chain output port will be used.

8.3.17 Auxiliary Buffers and Secondary-Data Packets (SDP)

The auxiliary buffer (ABUFF) architecture includes a non-video data path over FPD-Link IV forward channel only. The Auxiliary Buffers are meant to store SDPs (Meta-Data) and audio data formats. Each buffer can receive data packets from the auxiliary sources, which can then be mapped to one of the 6 streams on each of the two link layers or to either of the two DisplayPort outputs. More than one ABUFF can be mapped to a stream on the FPD-Link daisy-chain output.

If an ABUFF is mapped to a stream shared with one of the video buffers (VBUFF), the Link layer (LINK0/1) will fetch the data from ABUFF after the video data has been sent. The data in the ABUFF is sent over the FPD-Link IV link only during the horizontal blanking period of the video stream. Alternatively, an ABUFF could be mapped to a stream that is not mapped to any of the VBUFF. In this case, the auxiliary data is transmitted over the FPD-Link IV along with the video stream but on a different timeslot.

There are multiple sources for the ABUFF on the serializer side. The ABUFF destination for the serializers are the 6 streams inside each link layer. An ABUFF to Link Layer mapping muxes/demuxes nodes to/from Link 0 and Link 1 streams based on a per ABUFF register select bit (as part of serializer ABUFF register map). The deserializer has 6 stream destinations for daisy-chain transmitting and two SDP DP/eDP ports. Audio stream SDPs received on the DS90Ux983-Q1 or DS90Ux943A-Q1 DP/eDP port are converted to I2S data format prior to being sent across the FPD-Link IV link. The deserializer's I2S controller copies the audio auxiliary data from stream 0 or stream 1 if SDP_TYPE_IN (serializer register 0x81 plus offset) is 0 (audio packets). The DS90UH984-Q1 can output the I2S audio channels on I2S pins or regenerate the audio stream SDP on DP/eDP ports 0 and 1.

The DS90UH984 DP/eDP output only supports the following secondary data packets:

1. Audio stream

   a. Audio stream SDPs get converted to I2S data by setting serializer AUDIO_MODE field to 0.
   b. On the serializer, I2S data is sent to the ABUFF as data island transport mode. The deserializer receives the packetized I2S data on link layer, and then copies it to the I2S audio block which sends it to the DP/eDP output.
   c. DS90Ux984 DP/eDP APB registers require programming for audio SDP output, see DP/eDP Audio SDP Output Configuration for more information.
2. Audio timestamp
   a. Audio timestamps are generated at deserializer based on APB register programming, see DP/eDP Audio SDP Output Configuration for more information.
3. Audio & Non-Audio InfoFrames
   a. The following Infoframe types are supported:
      i. Vendor-Specific (defined in Section 6.1 of CTA-861)
      ii. Auxiliary Video Information (defined in Section 6.4 of CTA-861)
      iii. Source Product Description (defined in Section 6.5 of CTA-861)
      iv. Audio (defined in Section 6.6 of CTA-861)
      v. Dynamic Range and Mastering (defined in Section 6.9 of CTA-861)

Table 8-23. Supported Secondary Data Packets

Packet Type Value	Packet Type	Transmission Timing
0x01	Audio TimeStamp	At least once per video frame
0x02	Audio Stream	During horizontal and vertical blanking period of Main Video stream
0x81	Vendor-Specific	As per Section 6.1 of CTA-861
0x82	Auxiliary Video Information	As per Section 6.4 of CTA-861
0x83	Source Product Description	As per Section 6.5 of CTA-861
0x84	Audio InfoFrame	As per Section 6.6 of CTA-861
0x87	Dynamic Range and Mastering	As per Section 6.9 of CTA-861

DP/eDP Audio Stream packets can not be passed through as SDP over link. This packet type is converted to I2S audio data and transmitted via Data Island Transport or Audio over GPIO modes. DP/eDP Audio Stream packets can be regenerated for output on DS90UH984-Q1 DP/eDP ports 0 and/or 1.

The auxiliary data with respect to blanking time has the following constraint:

1. Highest number of bits to transmit in that time is 567 bits

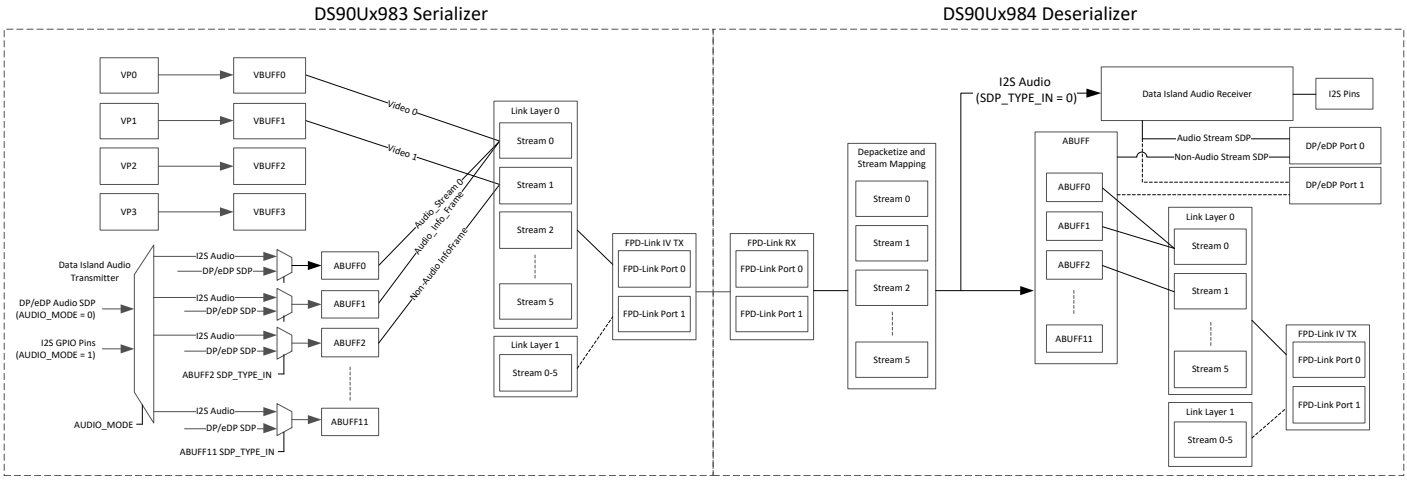

Figure 8-6. Example Auxiliary Buffer Configuration

8.3.17.1 ABUFF Deserializer Configuration and Registers

The deserializer auxiliary buffer registers are on Page_17 registers 0x80 through 0xDF. Each of the 12 ABUFFs have 8 registers (ABUFFx_CTL0 through ABUFFx_CTL8) assigned containing fields for configuration, mapping,

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and interrupts. Table 8-24 shows the primary registers for enabling and mapping ABUFF0. For additional debug and interrupt configuration, refer to the register map.

Table 8-24. Deserializer ABUFF0 Registers

Register	Bits	Field	Description
Page_17 0x80	1	ABUFF_TO_PORT_SEL	ABUFF0 Port Select This bit works in conjunction with ABUFF_TO_DEST_SEL. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
Page_17 0x80	0	ABUFFx_ENABLE	1: Activates the SDP block
Page_17 0x82	7:5	ABUFF_TO_DEST_SEL	ABUFF0 Destination Select ABUFF_TO_PORT_SEL to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved

8.3.17.2 Example ABUFF Set-Up

An example of ABUFF configuration sequence can be found below. The serializer initializes ABUFF2 as pass-through mode and transmits through two deserializers in a daisy chain configuration to output as SDP on DP/eDP Port 0 of the second deserializer.

```
serAddr = 0x18
des0Addr = 0x58
des1Addr = 0x60
# SER ABUFF programming
board.WriteI2C(serAddr, 0x40, 0x2C)
board.WriteI2C(serAddr, 0x41, 0x90)
board.WriteI2C(serAddr, 0x42, 0x01)  # SDP enable - ABUFF2
board.WriteI2C(serAddr, 0x41, 0x91)
board.WriteI2C(serAddr, 0x42, 0x07)  # SDP pass through mode - ABUFF2

#DES_1 ABUFF programming
board.WriteI2C(des0Addr, 0x40, 0x44)
board.WriteI2C(des0Addr, 0x41, 0x90)
board.WriteI2C(des0Addr, 0x42, 0x01)  # SDP enable - ABUFF2
board.WriteI2C(des0Addr, 0x41, 0x92)
board.WriteI2C(des0Addr, 0x42, (board.ReadI2C( des0Addr, 0x42) & 0xE0) | 0x00)  # Map to stream 0

#DES_2 ABUFF programming for daisy link 2nd DES
board.WriteI2C(des1Addr, 0x40, 0x44)
board.WriteI2C(des1Addr, 0x41, 0x90)
board.WriteI2C(des1Addr, 0x42, 0x01)  # SDP enable - ABUFF2

#DES_2 Enable SDP transmission on DP port 0 in APB 0x88 register
board.WriteI2C(des1Addr,0x49,0x88)
board.WriteI2C(des1Addr,0x4a,0x00)
board.WriteI2C(des1Addr,0x4b,0x01)
board.WriteI2C(des1Addr,0x4c,0x00)
board.WriteI2C(des1Addr,0x4d,0x00)
board.WriteI2C(des1Addr,0x4e,0x00)
board.WriteI2C(des1Addr,0x48,0x01)
```

8.3.18 RX Link Layer Diagnostics and Error Checking

The DS90UH984-Q1 deserializer has diagnostic and health monitoring mechanisms for each received video stream in FPD-Link IV and the single video stream in FPD-Link III. FPD-Link IV video streams have ECC error counters, CRC error counters, line length and line count reporting. The FPD-Link III video stream has checksum error counters, line length and line count reporting. For FPD-Link IV video streams, a pass status monitor can be configured for each DP/eDP port for reporting of error-free or errored video frames received.

Pass status control is configured in Page_18 PASS_STATUS_CONTROL register 0x52. FRAME_CAPTURE field captures the counters for error-free and errored video frames on DP/eDP ports 0 and 1. Counter levels for error-free and errored frames on DP/eDP port 0 can be read from Page_18 0x58-59 and Page_18 0x5A-0x5B, respectively. Counter levels for error-free and errored frames on DP/eDP port 1 can be read from Page_18 0x54-55 and Page_18 0x56-0x57, respectively. Counters levels for each can be cleared by the corresponding FRAME_CLEAR bit in PASS_STATUS_CONTROL register.

High-level error monitoring is reported by the FPD-Link RX interrupts shown in Table 8-25. Global ECC error, CRC error, control frame, data frame, and packet counters can be enabled for capture or cleared in Page_18 registers COUNT_CAPTURE (0x29) and COUNT_CLEAR (0x2A). After enabling capture in 0x29[5:0], ECC_ERROR_CNT, CTL_FRAME_CNT, DATA_FRAME_CNT, CRC_ERROR_CNT, and PACKET_CNT registers will report error and frame counts. After setting capture or clear bits in COUNT_CAPTURE (Page_18 0x29) or COUNTER_CLEAR (Page_18 0x30), field COUNTER_CHNG_EN (0x29[6]) must have a rising edge applied for the action to occur.

Table 8-25. FPD-Link IV RX Interrupts

Status	Address	Description
ECC Interrupt (STS_ECC_ERR)	Page_18 0x4E[7]	FPD4 Main Link ECC Error Interrupt Status This interrupt will trigger if an ECC error was detected.
CRC Interrupt (STS_CRC_ERR)	Page_18 0x4E[6]	FPD4 Main Link CRC Error Interrupt Status This interrupt will trigger if a CRC error was detected.
Horizontal Active Change Interrupt (STS_HACTIVE_CHG)	Page_18 0x4E[5]	HACTIVE Changed Global Interrupt Status This bit will be set when a change is detected between the HACTIVE reported for the current frame and the previous frame.
Vertical Total Change Interrupt (STS_VTOTAL_CHG)	Page_18 0x4E[4]	VTOTAL Changed Global Interrupt Status This bit will be set when a change is detected between the VTOTAL reported for the current line and the previous line.
Lock Status 1 Change Interrupt (STS_LOCK1_CHG)	Page_18 0x4E[3]	Port 1 Lock Status Changed Interrupt Status This bit will be set if LOCK is reacquired or if LOCK is lost.
Lock Status 0 Change Interrupt (STS_LOCK0_CHG)	Page_18 0x4E[2]	Port 0 Lock Status Changed Interrupt Status This bit will be set if LOCK is reacquired or if LOCK is lost.
Lock 1 Status (STS_LOCK1)	Page_18 0x4E[1]	Port 1 Locked This bit will be set if Port 1 had a LOCK condition.
Lock 0 Status (STS_LOCK0)	Page_18 0x4E[0]	Port 0 Locked This bit will be set if Port 0 had a LOCK condition.

Individual FPD-Link IV video stream status and error counters are available on Page_18 in registers 0x60-0x69 (stream 0), 0x70-0x79 (stream 1), 0x80-0x89 (stream 2), 0x90-0x99 (stream 3), 0xA0-0xA9 (stream 4), and

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0xB0-0xB9 (stream 5). Video stream active is reported in Page_18 registers 0x39-0x3A (stream 0), 0x3B-0x3C (stream 1), 0x3D-0x3E (stream 2), 0x3F-0x40 (stream 3), 0x41-0x42 (stream 4), and 0x43-0x44 (stream 5). Video stream video pixel formats are reported in Page_18 register 0x45 and 0x46.

FPD-Link III video stream status and error counters are available on Page_18 in registers 0xC0-0xC7.

Each video stream has its own capture and clear register for control of horizontal active, vertical total, CRC, and ECC counting for FPD-Link IV streams and horizontal active, vertical total, and check-sum for the FPD-Link III stream. Stream errors should be cleared after initialization to eliminate transient errors from the bring-up before monitoring for errors during operation. After setting capture or clear bits in STREAM_x_COUNT_CONTROL (Page_18 0x60+offset), field COUNTER_CHNG_EN (0x29[6]) must have a rising edge applied for the action to occur.

The following script can be used to clear then re-enable error counting of FPD-Link IV video stream 0:

```
import time
DEVICE_ADDR=0x58

#Change Offset for other streams
#Stream 0: 0x00
#Stream 1: 0x20
#Stream 2: 0x40
#Stream 3: 0x60
#Stream 4: 0x80
#Stream 5: 0xA0
Offset = 0x00

board.WriteI2C(DEVICE_ADDR, 0x40, 18 * 4)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x45)
# Disable All Captures (Main & Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x00)  # Disable All Captures & Update
board.WriteI2C(DEVICE_ADDR, 0x41, 0x60 + Offset)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x00)  # Disable All Captures & Update
# Select All Captures (Main & Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x3F)  # Select All Captures
board.WriteI2C(DEVICE_ADDR, 0x41, 0x60 + Offset)
board.WriteI2C(DEVICE_ADDR, 0x42, 0xF0)  # Select All Captures (Stream Based)
# Select All Clear Controls (Main & Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x2A)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x3F)  # Select All Clear Controls
board.WriteI2C(DEVICE_ADDR, 0x41, 0x60 + Offset)
board.WriteI2C(DEVICE_ADDR, 0x42, 0xFF)  # Select All Clear Controls (Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x40, 18 * 4)
# Toggle re_update_en to take effect
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x3F)  # Toggle re_update_en
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x7F)  # Toggle re_update_en
# De-Select All Clear Controls (Main & Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x2A)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x00)  # Select All Clear Controls
board.WriteI2C(DEVICE_ADDR, 0x41, 0x60 + Offset)
board.WriteI2C(DEVICE_ADDR, 0x42, 0xF0)  # Select All Clear Controls (Stream Based)
# Toggle re_update_en to take effect
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x3F)  # Toggle re_update_en
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x7F)  # Toggle re_update_en
```

The following script can be used to read FPD-Link IV video stream 0 errors:

```
DEVICE_ADDR=0x58

#Change Offset for other streams
#Stream 0: 0x00
#Stream 1: 0x20
#Stream 2: 0x40
#Stream 3: 0x60
#Stream 4: 0x80
#Stream 5: 0xA0
```

```
Offset = 0x00

# HACTIVE
board.WriteI2C(DEVICE_ADDR, 0x41, 0x66 + Offset)
HACTIVE = board.ReadI2C(DEVICE_ADDR, 0x42) << 8
board.WriteI2C(DEVICE_ADDR, 0x41, 0x65 + Offset)
HACTIVE = HACTIVE + board.ReadI2C(DEVICE_ADDR, 0x42)

# VTOTAL
board.WriteI2C(DEVICE_ADDR, 0x41, 0x68 + Offset)
VTOTAL = board.ReadI2C(DEVICE_ADDR, 0x42) << 8
board.WriteI2C(DEVICE_ADDR, 0x41, 0x67 + Offset)
VTOTAL = VTOTAL + board.ReadI2C(DEVICE_ADDR, 0x42)

# CRC
board.WriteI2C(DEVICE_ADDR, 0x41, 0x64 + Offset)
CRC = board.ReadI2C(DEVICE_ADDR, 0x42) << 8
board.WriteI2C(DEVICE_ADDR, 0x41, 0x63 + Offset)
CRC = CRC + board.ReadI2C(DEVICE_ADDR, 0x42)

# ECC
board.WriteI2C(DEVICE_ADDR, 0x41, 0x62 + Offset)
ECC = board.ReadI2C(DEVICE_ADDR, 0x42) << 8
board.WriteI2C(DEVICE_ADDR, 0x41, 0x61 + Offset)
ECC = ECC + board.ReadI2C(DEVICE_ADDR, 0x42)

# READ FLAGS
board.WriteI2C(DEVICE_ADDR, 0x40, 18 * 4 + 1)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x69 + Offset)
FLAGS = board.ReadI2C(DEVICE_ADDR, 0x42)
ECC_ERROR_FLAG = (FLAGS >> 3) & 0x01
CRC_ERROR_FLAG = (FLAGS >> 2) & 0x01
HACTIVE_CHNG = (FLAGS >> 1) & 0x01
VTOTAL_CHNG = FLAGS & 0x01
```

The following script can be used to clear then re-enable error counting of FPD-Link III video stream:

```
import time
DEVICE_ADDR=0x58

board.WriteI2C(DEVICE_ADDR, 0x40, 18 * 4)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x45)
# Disable All Captures (Main & Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x00)  # Disable All Captures & Update
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC0)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x00)  # Disable All Captures & Update
# Select All Captures (Main & Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x3F)  # Select All Captures
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC0)
board.WriteI2C(DEVICE_ADDR, 0x42, 0xF0)  # Select All Captures (Stream Based)
# Select All Clear Controls (Main & Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x2A)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x3F)  # Select All Clear Controls
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC0)
board.WriteI2C(DEVICE_ADDR, 0x42, 0xFF)  # Select All Clear Controls (Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x40, 18 * 4)
# Toggle re_update_en to take effect
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x3F)  # Toggle re_update_en
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x7F)  # Toggle re_update_en
# De-Select All Clear Controls (Main & Stream Based)
board.WriteI2C(DEVICE_ADDR, 0x41, 0x2A)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x00)  # Select All Clear Controls
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC0)
board.WriteI2C(DEVICE_ADDR, 0x42, 0xF0)  # Select All Clear Controls (Stream Based)
# Toggle re_update_en to take effect
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x3F)  # Toggle re_update_en
board.WriteI2C(DEVICE_ADDR, 0x41, 0x29)
board.WriteI2C(DEVICE_ADDR, 0x42, 0x7F)  # Toggle re_update_en
```


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The following script can be used to read FPD-Link III video stream errors:

```
import time
DEVICE_ADDR=0x58

# HACTIVE
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC4)
HACTIVE = board.ReadI2C(DEVICE_ADDR, 0x42) << 8
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC3)
HACTIVE = HACTIVE + board.ReadI2C(DEVICE_ADDR, 0x42)

# VTOTAL
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC6)
VTOTAL = board.ReadI2C(DEVICE_ADDR, 0x42) << 8
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC5)
VTOTAL = VTOTAL + board.ReadI2C(DEVICE_ADDR, 0x42)

# CHECKSUM_ERROR
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC2)
CRC = board.ReadI2C(DEVICE_ADDR, 0x42) << 8
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC1)
CRC = CRC + board.ReadI2C(DEVICE_ADDR, 0x42)

# READ FLAGS
board.WriteI2C(DEVICE_ADDR, 0x40, 18 * 4 + 1)
board.WriteI2C(DEVICE_ADDR, 0x41, 0xC7)
FLAGS = board.ReadI2C(DEVICE_ADDR, 0x42)
CKSUM_ERROR_FLAG = (FLAGS >> 2) & 0x01
HACTIVE_CHNG = (FLAGS >> 1) & 0x01
VTOTAL_CHNG = FLAGS & 0x01
```

8.3.19 Audio

The deserializer can receive audio sent over the serializer I2S pins or other audio interfaces, such as DP or HDMI. Audio streams support 32 to 192 kHz sampling rate (32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz), 2 to 8-channels, and 16 to 32 bit word size (all even intervals, e.g. 16, 18, 20, 22, 24, 26, 28, 30, 32, etc.). I2S audio is supported from serializer to deserializer but the reverse direction (deserializer to serializer) is not supported.

Many of the serializer and deserializer audio registers are configured in the serializer and sent over the FPD-Link to the deserializer. For DS90Ux981 and DS90Ux94x devices, audio is only received from I2S pins. In the case of DS90Ux983 and DS90Ux943A, I2S audio could be received from either DisplayPort audio packets or from I2S pins. Downstream deserializers do not have audio mode conversion capabilities, therefore converting audio modes must be performed by the serializer.

8.3.19.1 Audio Formats

8.3.19.1.1 Parallel I2S

I2S audio is supported externally through I2S pins (I2S_CLK, I2S_WC, and I2S_Dx) which are shared with GPIO pins. The bit clock (I2S_CLK) supports frequencies between 1 MHz to 12.288 MHz. Four I2S data inputs transport two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) input. The I2S interface supports a range of I2S sample rates as shown in the table below:

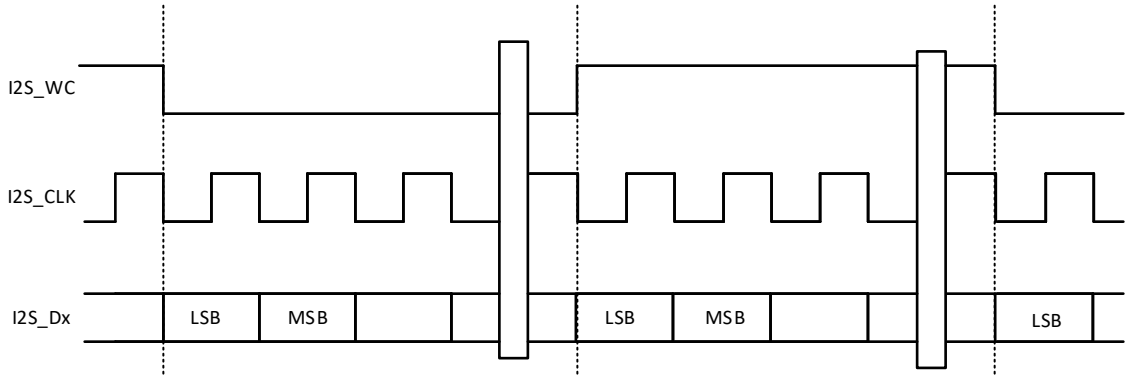

Figure 8-7. I2S Frame Timing Diagram

Table 8-26. I2S Audio Sample Rates

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

8.3.19.1.2 DP/eDP Audio Stream Packets

DS90Ux983 and DS90Ux943 serializer DP/eDP receive blocks can accept audio over the DisplayPort input. The DP/eDP audio packets are converted to I2S by the serializer by setting AUDIO_MODE field in AUDIO_CFG to 0. Once transmitted to downstream deserializer, the audio data can be output to I2S or sent to DP/eDP port as audio stream packets (SDP). Audio stream packets can be output from DS90Ux984 deserializer DP/eDP output ports, see DP/eDP Audio SDP Output Configuration for more information.

8.3.19.2 Transport Modes, Splitting, and Forwarding

The serializer or deserializer daisy-chain can send audio to downstream deserializers via Audio over GPIO and data island transport modes. Audio over GPIO and data island transport modes can be used in FPD-Link III and FPD-Link IV modes, depending on the capability of the serializer and deserializer. The user must pay attention to the FPD mode, transport mode, and port enabling when configuring audio registers since some registers only apply to certain transport and FPD-Link modes or ports.

Audio over GPIO transport mode utilizes the in-band forward channel GPIO bit stream to send the I2S clock, word clock, and 4 channels of audio data to the deserializer. In Audio over GPIO mode, the four GPIO signals are assigned as follows:

- FC_GPIO0 : I2S_CLK
- FC_GPIO1 : I2S_WC

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• FC_GPIO2 : I2S_DA

• FC_GPIO3 : I2S_DB

When Audio via GPIO is enabled, the Audio data will not be encrypted via HDCP. Audio via GPIO also only supports 2 or 4-channel audio.

Audio Data Island transport mode utilizes audio packet data in the video stream channel. This method allows 2, 4, or 8 channels of audio to be sent. Since the audio is sent over the video channel, the audio will be encrypted if HDCP content protection is enabled for the Audio/Video connection.

8.3.19.2.1 FPD-Link IV Audio Transport Modes

In FPD-Link IV mode, the serializer or local deserializer daisy-chain audio registers in FPD4_DATAPATH_CTL and FPD3_DATAPATH_CTL are configured based on desired transport mode, number of audio channels, and port configuration. Both I2S_TRANSPORT_SEL and FPD4_I2S_TRANSPORT need to be configured to the same transport mode. I2S_MODE and FPD4_I2SB_FC_EN are set based on the number of audio channels. I2S_TRANSPORT_SEL, FPD4_I2S_TRANSPORT, and FPD4_I2SB_FC_EN are port specific registers and are used in combination with the PORT_SEL register (0x0E for deserializer daisy chain and 0x2D for serializer) to select which FPD-Link IV port is configured. I2S transport on FPD-Link Port 0 is enabled by setting main page register 0x02[1] to 1. I2S transport on FPD-Link Port 1 is enabled by setting main page register 0x02[2] to 1. When enabled, transport mode for each port is set based on the I2S_TRANSPORT_SEL and FPD4_I2S_TRANSPORT.

When transporting audio via Data Island transport mode with video present, there is a minimum horizontal blanking constraint based the amount of audio bits accumulated during active video portion of the frame.

$$\text{AUDIO_FPD_FRAME_CNT} * \text{FPD_FRAME_PERIOD} < \text{HBLANK_PERIOD} \quad (40)$$

Where

AUDIO_FPD_FRAME_CNT = (AUDIO_BITS_PER_LINE / 128)+2
AUDIO_BITS_PER_LINE = (HTOTAL / PCLK) * (I2S_CLK * 4)
FPD_FRAME_PERIOD (in ns) = 132 / FPD_RATE (in Mbps)
PCLK = Pixel Clock in MHz
HBLANK_PERIOD (in ns) = (HTOTAL - HACTIVE) / PCLK (in MHz)

Where
If I2S: I2S_CLK=SAMPLE_RATE*WORD_SIZE
If TDM: I2S_CLK=SAMPLE_RATE*WORD_SIZE*NUMBER_CHANNELS

When operating in Data Island transport mode, the audio data is transmitted through the auxiliary buffers described in Auxiliary Buffers and Secondary-Data Packets (SDP) . By default, ABUFF0 and ABUFF1 are configured for packetized audio transport. When audio transport to both FPD-Link IV ports is required, ABUFF1 must be enabled and mapped to Link Layer 1. Audio data can be transmitted without video through Stream 1 by mapping ABUFF0 to Stream 1 and setting FPD4_I2S_TRANSPORT to 0b10.

Table 8-27. FPD-Link IV Transmit Audio Configuration

Serializer / Deserializer Daisy Chain Field		Field Name	Description
981/983/943A	984/8 Daisy Chain		
Main_Page 0x5A[3]	Port 0: Page_8 0x03[3] Port 1: Page_8 0x13[3]	I2S_TRANSPORT_SEL	Enable I2S data as Forward Channel Data Island 0: Enable I2S Data Island Transport 1: Enable I2S Data using Audio over GPIO, upto 4-CH max with I2S_CLK rate 3MHz limit. For 98x and 943A serializers: When PORT_SEL = 0, this applies to port 0. When PORT_SEL = 1, this applies to port 1. For 98x deserializer daisy chain: 0x03 applies to port 0 and 0x13 applies to port 1.

Table 8-27. FPD-Link IV Transmit Audio Configuration (continued)

Serializer / Deserializer Daisy Chain Field		Field Name	Description
981/983/943A	984/8 Daisy Chain		
Main_Page 0x5A[1:0]	Port 0: Page_8 0x03[1:0] Port 1: Page_8 0x13[1:0]	I2S_MODE	Select number of audio channels For 98x and 943A serializers: When PORT_SEL = 0, this applies to port 0. When PORT_SEL = 1, this applies to port 1. For 98x deserializer daisy chain: 0x03 applies to port 0 and 0x13 applies to port 1.
Main_Page 0x0D[6]	Main_Page 0xA4[6]	FPD4_I2SB_FC_EN	If FPD4 Audio uses forward channel GPIO, this bit enables 4-channel audio using FC_GPIO[3]. When PORT_SEL = 0, this applies to port 0. When PORT_SEL = 1, this applies to port 1.
Main_Page 0x0D[5:4]	Main_Page 0xA4[5:4]	FPD4_I2S_TRANSPORT	00: I2S disabled over FPD4 link 01: I2S audio is sent over the forward channel as GPIO data. 10: I2S over data island for FPD4 stream 1 data 11: I2S over data island for FPD4 stream 0 data When PORT_SEL = 0, this applies to port 0. When PORT_SEL = 1, this applies to port 1.
Main_Page 0x02[2:1]	N/A	I2S_EN	Enable I2S input and transport 1x: Enables I2S transport through FPD-Link Port 1 x1: Enabled I2S transport through FPD-Link Port 0
Main_Page 0x05[1:0]	N/A	I2S_AUDIO_SPLIT	Split audio for FPD4 Port 0 and Port 1; If I2S is enabled, and audio over GPIO is selected, select I2S_DA and I2S_DB or I2S_DC and I2S_DD.

8.3.19.2.2 FPD-Link III Audio Transport Modes

By default, audio transport in FPD-Link III mode is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames may be disabled from control registers if Audio over GPIO is desired. In this mode, I2S_DA and I2S_DB are transmitted to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer. If connected to a DS90UB926Q-Q1 deserializer, only I2S_DA is transmitted. Surround Sound Mode, which transmits all four I2S data inputs (I2S_D[A..D]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UB928Q-Q1, DS90UB940-Q1, or a DS90UB948-Q1 deserializer.

To disable Data Island Transport mode and use Audio over GPIO mode instead, set I2S_TRANSPORT_SEL to 1. Set the number of I2S channels in the I2S_MODE (0x5A[1:0]) register.

Table 8-28 shows I2S_MODE and I2S_TRANSPORT_SEL settings for the possible channel count and transport mode combinations for FPD-Link III audio transmitting from serializer or deserializer daisy-chain output. Table 8-29 shows the specific registers used for FPD-Link III audio transport configuration in either Audio over GPIO or Data Island transport modes.

Table 8-28. FPD-Link III TX Audio Example Configurations

I2S Pins	Number of Audio Channels	Transport Mode	I2S_MODE (Main_Page 0x5A[1:0])	I2S_TRANSPORT_SEL (Main_Page 0x5A[3])
1	2	Data Island	0b00	0
1	2	Audio over GPIO	0b00	1
2	4	Data Island	0b01	0
2	4	Audio over GPIO	0b01	1
3 or 4	6 or 8	Data Island	0b10	0

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Table 8-29. FPD-Link III Transmit Audio Configuration

Serializer / Deserializer Daisy Chain Field		Field Name	Description
981/983/943A	984/8 Daisy Chain		
Main_Page 0x5A[3]	Page_8 0x03[3] Page_8 0x13[3]	I2S_TRANSPORT_SEL	Enable I2S data as Forward Channel Data Island If 0, pack I2S data as 128bit SDP and send it over during video blanking. If 1 – send it over GPIO, upto 4-CH max with I2S_CLK rate 3MHz limit. For 98x and 943A serializers: When PORT_SEL = 0, this applies to port 0. When PORT_SEL = 1, this applies to port 1. For 98x deserializer daisy chain: 0x03 applies to port 0 and 0x13 applies to port 1.
Main_Page 0x5A[1:0]	Page_8 0x03[1:0] Page_8 0x13[1:0]	I2S_MODE	Select number of audio channels For 98x and 943A serializers: When PORT_SEL = 0, this applies to port 0. When PORT_SEL = 1, this applies to port 1. For 98x deserializer daisy chain: 0x03 applies to port 0 and 0x13 applies to port 1.
Main_Page 0x53[4]	N/A	SPLIT_AUDIO	Feature not supported in 98x devices
Main_Page 0x53[5]	N/A	AUDIO_MODE	Selects source for audio to be sent over the FPD-Link III downstream link. 0: DisplayPort 1: I2S audio from I2S pins

8.3.19.3 Deserializer Audio Output Configuration

The deserializer supports receiving audio in both FPD-Link III and FPD-Link IV modes using either audio over GPIO or packetized audio transport methods to be output on the I2S pins.

Transport Modes, Splitting, and Forwarding describes the required audio configuration for the upstream serializer or deserializer daisy chain transmit blocks. By default, deserializer FPD3_RX_DATAPATH_CTL (0x27) and FPD4_RX_DATAPATH_CTL (0x0C) registers are loaded from the forward channel and will indicate transport mode type based on the serializer audio register configuration. Both registers have an OVERRIDE_FC_CONFIG field bit 7, which will disable the loading of the register from forward channel and allow locally written values.

The following subsections describe register configurations for audio output from the deserializer via I2S or DP/eDP audio packets.

8.3.19.3.1 I2S Clock Divider Configuration

The deserializer audio clock divider needs configured to generate the required I2S clock rate. The I2S clock rate is dependent on the audio parameters, such as number of channels, sample rate, and number of bits.

Two I2S clock divider modes are available for generation of the I2S clock. Field I2S_DIV_CFG in Page_1 register 0x84 will set either always-on (AON) clock or I2S divider clock modes. When main link is operating in FPD-Link III mode, AON clock mode must be used for the audio clock configuration. I2S divider clock mode, which will have a tighter jitter tolerance, can be used in FPD-Link IV mode.

The FIFO adjust thresholds in Page_1 registers 0x88 through 0x8C must be programmed based on Table 8-30. These values are used as thresholds to detect over-flow and under-flow trends and adjust I2S clock speed based on Page_1 registers 0x85-0x86 in AON mode and 0x90-0x97 in I2S divider mode. The I2S FIFO size is 64.

Table 8-30. I2S FIFO Adjust Thresholds

Address	Name	Value (decimal)
0x8A	FIFO_2ND_HIGH	48
0x88	FIFO_1ST_HIGH	35
0x8C	FIFO Mid Threshold	32
0x89	FIFO_1ST_LOW	29
0x8B	FIFO_2ND_LOW	16

By default, I2S_DIV_CFG (Page_1 register 0x84) set to 0 will enable the AON clock mode and is compatible with both FPD-Link III and FPD-Link IV operating modes. In AON clock mode, DIV_RATIO is programmed to Page_1 register I2S_INT_DIV (0x80-0x81) according to Equation 43. 1 is programmed to Page_1 register I2S_FRAC_NUM (0x82-0x83). The measured reference clock frequency in main page register 0xAE is used to calculate the DIV_RATIO.

$$\text{ALWAYS_ON_FREQ} = 500 * (27 / \text{REFCLK_MEAS}) \quad (41)$$

Where

- REFCLK_MEAS = Value of PLL_REFCLK_FREQ_RXP register (Main_Page 0xAE)

$$\text{I2S_CLOCK_RATE} = \text{NUMBER_BITS} * \text{SAMPLE_RATE} * \text{NUMBER_CHANNELS} \quad (42)$$

$$\text{DIV_RATIO} = \text{RoundUp}(\text{ALWAYS_ON_FREQ} / \text{I2S_CLOCK_RATE}) \quad (43)$$

When operating in AON clock mode, Page_1 registers CLK_SPEEDUP_INT_ADD (0x85) and CLK_SLOWDOWN_INT_SUB (0x86) are set to 0x7F. When the FIFO threshold levels are detected, INT_DIV will be adjusted by CLK_SPEEDUP and CLK_SLOWDOWN values to adjust the clock frequency.

To enable analog divider mode only in FPD-Link IV mode, set I2S_DIV_CFG to 1. The I2S divider clock mode uses the FPD-Link VCO frequency and fractional divider to set the I2S clock rate. Set Page_1 register I2S_INT_DIV (0x80-0x81) according to Equation 46. Set Page_1 I2S_FRAC_NUM (0x82-0x83) according to Equation 47.

$$\text{I2S_CLOCK_RATE} = (\text{VCO_FREQ} / 8) / (\text{DIV}+12) \quad (44)$$

Where

- DIV = I2S_INT_DIV + I2S_FRAC_NUM / 2^{16}
- VCO_FREQ is 6750 for 3.375 Gbps, 6.75 Gbps, and 13.5 Gbps; 5400 for 10.8 Gbps; and 6264 for 12.528 Gbps

Therefore

$$\text{DIV} = \text{VCO_FREQ} / (\text{I2S_CLOCK_RATE} * 8) - 12 \quad (45)$$

$$\text{I2S_INT_DIV} = \text{DIV rounded down to nearest integer} \quad (46)$$

$$\text{I2S_FRAC_NUM} = (\text{DIV} - \text{I2S_INT_DIV}) * 2^{16} \quad (47)$$

Page_1 registers 0x90 through 0x97 should be set based on the I2S clock mode as shown in Table 8-31.

Table 8-31. Fractional Speed Up / Slow Down Settings

Register	Register Name	I2S Clock Divider 0x84[6]=1
0x90	FRAC_1ST_ADD_0	0x40
0x91	FRAC_1ST_ADD_1	0x40

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Table 8-31. Fractional Speed Up / Slow Down Settings (continued)

Register	Register Name	I2S Clock Divider 0x84[6]=1
0x92	FRAC_2ND_ADD_0	0x40
0x93	FRAC_2ND_ADD_1	0x40
0x94	FRAC_1ST_SUB_0	0x40
0x95	FRAC_1ST_SUB_1	0x40
0x96	FRAC_2ND_SUB_0	0x40
0x97	FRAC_2ND_SUB_1	0x40

8.3.19.3.2 I2S Pin Output Configuration

The deserializer GPIO control registers need configured to output each I2S signal. GPIO_IN_EN_HIGH (0x12) and GPIO_IN_EN_HIGH (0x13) need to set the corresponding GPIO pin enable bit to 0 to disable the inputs. The GPIOx_OUTPUT_EN (0x15[7]) bit will be set to 1 to enable the GPIO as an output. The GPIOx_OUT_SRC (0x15[6:5]) field will select Device Status (0b10), and GPIOx_OUT_SEL will select the specific I2S signal (I2S_WC, I2S_DA, I2S_DB, I2S_DC or I2S_DD). If multiple audio channels are sent to a deserializer, GPIOx_OUT_SEL provides flexibility to only map select channels out to GPIO pins and leave the remaining unmapped to utilize the GPIO pin for another function or left as open. I2S output is disabled by default and needs enabled by setting I2S_DISABLED (0x28[2]) to 0.

An example of configuring the GPIO pins for 8-channel Data Island I2S output can be found below:

```
# I2S GPIO Configuration - Data Island Transport Mode - 8 channel
board.WriteI2C( 0x58, 0x12, 0x1E) # GPIO8 input disable
board.WriteI2C( 0x58, 0x13, 0x70) # GPIO7/3/2/1/0 input disable
board.WriteI2C( 0x58, 0x17, 0xC9) # FC_GPIO2 I2S_DC FPD4
board.WriteI2C( 0x58, 0x18, 0xC8) # FC_GPIO3 I2S_DD FPD4
board.WriteI2C( 0x58, 0x1A, 0xCB) # FC_GPIO5 I2S_DB FPD4
board.WriteI2C( 0x58, 0x1B, 0xCC) # FC_GPIO6 I2S_DA FPD4
board.WriteI2C( 0x58, 0x1C, 0xCA) # FC_GPIO7 I2S_WS FPD4
board.WriteI2C( 0x58, 0x1D, 0xCD) # FC_GPIO8 I2S_CLK FPD4
```

An example of configuring the GPIO pins for 4-channel Audio over GPIO I2S output can be found below:

```
# I2S GPIO Configuration - Audio over GPIO Transport Mode - 4 channel
board.WriteI2C( 0x58, 0x13, 0xF0) # GPIO3/2/1/0 input disable
board.WriteI2C( 0x58, 0x14, 0xCE) # FC_GPIO0 I2S_CLK
board.WriteI2C( 0x58, 0x15, 0xCA) # FC_GPIO1 I2S_WS
board.WriteI2C( 0x58, 0x16, 0xCC) # FC_GPIO2 I2S_DA
board.WriteI2C( 0x58, 0x17, 0xCB) # FC_GPIO3 I2S_DB
```

8.3.19.3.3 DP/eDP Audio SDP Output Configuration

As an alternative to outputting via I2S pins, the DS90Ux984-Q1 can output the received audio data on the DP/eDP ports via audio SDPs.

For DP/eDP audio SDP operation, the following APB registers need configured. SEC_AUDIO_EN (0x300) is set to 1. SEC_AUDIO_FIFO_DEPTH is set to 0x80. SEC_CHANNEL_COUNT (0x308) is set to the audio channel count being sent. SECONDARY_DATA_WINDOW (0x08C[11:0]) is set based on Equation 48.

$$\text{SECONDARY_DATA_WINDOW} = (\text{HBLANK (in pixels)} / \text{PCLK (in MHz)}) * \text{LINK_SYMBOL_CLOCK (in MHz)} * 0.9 \quad (48)$$

Where

- SECONDARY_DATA_WINDOW is rounded to nearest integer
- LINK_SYMBOL_CLOCK (in MHz) = LINK_BW_SET * 100
- LINK_BW_SET = DP/eDP rate in Gbps

By default, the DP/eDP audio SDP will operate in asynchronous clock mode and can be overwritten to synchronous clock mode by setting APB register SEC_AUDIO_CLOCK_MODE (0x320) to 1. SEC_MAUD and

SEC_NAUD do not need programmed when operating in asynchronous mode. In synchronous clock mode, SEC_MAUD and SEC_NAUD are set based on Equation 49.

$$MAUD/NAUD = 512 * AUDIO_SAMPLING_FREQ / (LINK_BW_SET * 100 * 1000000) \quad (49)$$

Where

- AUDIO_SAMPLING_FREQ = Audio sampling frequency of the audio stream being transported in Hz
- LINK_BW_SET = DP/eDP rate in Gbps

8.3.19.4 Deserializer Audio Daisy-Chain

The deserializer has the capability to forward audio on the daisy-chain transmit ports in Audio via GPIO and Data Island transport modes.

The deserializer daisy chain transmit block has similar audio transport mode selection registers as the serializer transmit registers, as shown in Transport Modes, Splitting, and Forwarding. At each downstream deserializer, I2S audio channels can be independently mapped to each I2S output pin. For example, 8 channels of audio can be forwarded in a 4 deserializer daisy chain, and each deserializer can map separate, unique 2 audio channels to the I2S_DA pin. I2S Pin Output Configuration describes the configuration and mapping of I2S audio channels to each I2S pin.

Examples of various audio input, output, and daisy chain configurations are provided in Audio Daisy Chain and Splitting Examples

8.3.19.5 Audio Daisy Chain and Splitting Examples

The following sections provide examples of various audio forwarding and output configurations.

8.3.19.5.1 Single Deserializer with 2-Ch I2S Input

Figure 8-8 shows an example audio configuration with one deserializer and 2-Ch I2S input and output.

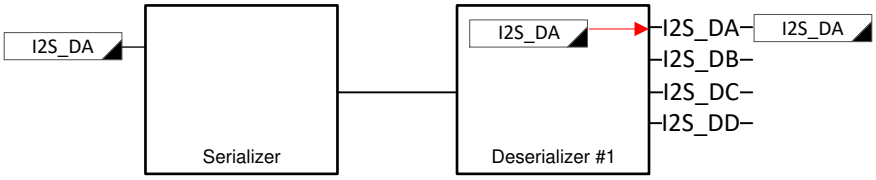

Figure 8-8. Single Deserializer with 2-Ch I2S Input

In the following code example, the deserializer receives audio via Data Island transport in FPD-Link IV mode and outputs to GPIO7 using AON I2S clock mode.

```
#I2S Config = 32 bits, 32 kHz, and number of channel = 2
#I2S Clock Mode = AON
#I2S CLK = 2.048 MHz
#FPD-Link Rate: 6.75 Gbps

I2S_CLOCK_RATE = 2.048

board.WriteI2C( 0x58, 0x12, 0x1E)  # GPIO13 input disable
board.WriteI2C( 0x58, 0x13, 0x70)  # GPIO7/3/2/1/0 input disable
board.WriteI2C( 0x58, 0x1D, 0xCE)  # FC_GPIO8 I2S_CLK FPD4
board.WriteI2C( 0x58, 0x1C, 0xCC)  # FC_GPIO7 I2S_DA FPD4
board.WriteI2C( 0x58, 0x17, 0xCA)  # FC_GPIO2 I2S_WS FPD4

REFCLK_MEAS = board.ReadI2C( 0x58, 0xAE)  # Read value of PLL_REFCLK_FREQ
AON_FREQ = 500 * (27.0/REFCLK_MEAS)
INV_DIV = int(AON_FREQ / I2S_CLOCK_RATE)
board.WriteI2C( 0x58, 0x40, 0x04)
board.WriteI2C( 0x58, 0x41, 0x80)
board.WriteI2C( 0x58, 0x42, 0x00)  # I2S_INT_DIV_15_8
board.WriteI2C( 0x58, 0x41, 0x81)
board.WriteI2C( 0x58, 0x42, 0x01)  # I2S_INT_DIV_7_0
board.WriteI2C( 0x58, 0x41, 0x82)
```


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```
board.WriteI2C( 0x58, 0x42, (INT_DIV & 0xFF00)>>8)  # I2S_FRAC_NUM_15_8
board.WriteI2C( 0x58, 0x41, 0x83)
board.WriteI2C( 0x58, 0x42, (INT_DIV & 0xFF))  # I2S_FRAC_NUM_7_0
board.WriteI2C( 0x58, 0x40, 0x05)
board.WriteI2C( 0x58, 0x41, 0x84)
idr_reg_rb = board.ReadI2C( 0x58, 0x42)
board.WriteI2C( 0x58, 0x40, 0x04)
board.WriteI2C( 0x58, 0x41, 0x84)
board.WriteI2C( 0x58, 0x42, (idr_reg_rb & 0xBF) | 0x00)    # Set AON I2S mode
board.WriteI2C( 0x58, 0x41, 0x85)
board.WriteI2C( 0x58, 0x42, 0x7F)  # CLK_SPEEDUP_INT_ADD
board.WriteI2C( 0x58, 0x41, 0x86)
board.WriteI2C( 0x58, 0x42, 0x7F)  # CLK_SLOWDOWN_INT_ADD
board.WriteI2C( 0x58, 0x41, 0x8C)
board.WriteI2C( 0x58, 0x42, 0x20)  # FIFO Drain
board.WriteI2C( 0x58, 0x41, 0x88)
board.WriteI2C( 0x58, 0x42, 0x23)  # FIFO Drain
board.WriteI2C( 0x58, 0x41, 0x89)
board.WriteI2C( 0x58, 0x42, 0x1D)  # FIFO Drain
board.WriteI2C( 0x58, 0x41, 0x8A)
board.WriteI2C( 0x58, 0x42, 0x30)  # FIFO Drain
board.WriteI2C( 0x58, 0x41, 0x8B)
board.WriteI2C( 0x58, 0x42, 0x10)  # FIFO Drain
```

In the following code example, the deserializer receives audio via Data Island transport in FPD-Link IV mode and outputs to GPIO7 using I2S divider clock mode.

```
#I2S Config = 32 bits, 32 kHz, and number of channel = 2
#I2S Clock Mode = AON
#I2S CLK = 2.048 MHz
#FPD-Link Rate: 6.75 Gbps

board.WriteI2C( 0x58, 0x12, 0x1E)  # GPIO13 input disable
board.WriteI2C( 0x58, 0x13, 0x70)  # GPIO7/3/2/1/0 input disable
board.WriteI2C( 0x58, 0x1D, 0xCE)  # FC_GPIO8 I2S_CLK FPD4
board.WriteI2C( 0x58, 0x1C, 0xCC)  # FC_GPIO7 I2S_DA FPD4
board.WriteI2C( 0x58, 0x17, 0xCA)  # FC_GPIO2 I2S_WS FPD4

I2S_CLOCK_RATE = 2.048
FPD_VCO_FREQ = 6750
INT_DIV = int(FPD_VCO_FREQ / (I2S_CLOCK_RATE * 8) - 12)
FRAC_NUM = ((FPD_VCO_FREQ / (I2S_CLOCK_RATE * 8) - 12) - INT_DIV) * 2^16
board.WriteI2C( 0x58, 0x40, 0x04)
board.WriteI2C( 0x58, 0x41, 0x80)
board.WriteI2C( 0x58, 0x42, (INT_DIV & 0xFF00)>>8)  # I2S_INT_DIV_15_8
board.WriteI2C( 0x58, 0x41, 0x81)
board.WriteI2C( 0x58, 0x42, (INT_DIV & 0xFF))  # I2S_INT_DIV_7_0
board.WriteI2C( 0x58, 0x41, 0x82)
board.WriteI2C( 0x58, 0x42, (FRAC_NUM & 0xFF00)>>8)  # I2S_FRAC_NUM_15_8
board.WriteI2C( 0x58, 0x41, 0x83)
board.WriteI2C( 0x58, 0x42, (FRAC_NUM & 0xFF))  # I2S_FRAC_NUM_7_0
board.WriteI2C( 0x58, 0x40, 0x05)
board.WriteI2C( 0x58, 0x41, 0x84)
idr_reg_rb = board.ReadI2C( 0x58, 0x42)
board.WriteI2C( 0x58, 0x40, 0x04)
board.WriteI2C( 0x58, 0x41, 0x84)
board.WriteI2C( 0x58, 0x42, (idr_reg_rb & 0xBF) | 0x40)  # Set I2S divider mode
board.WriteI2C( 0x58, 0x41, 0x90)
board.WriteI2C( 0x58, 0x42, 0x40)  # FRAC_1ST_ADD
board.WriteI2C( 0x58, 0x41, 0x91)
board.WriteI2C( 0x58, 0x42, 0x40)  # FRAC_1ST_ADD
board.WriteI2C( 0x58, 0x41, 0x92)
board.WriteI2C( 0x58, 0x42, 0x40)  # FRAC_2ND_ADD
board.WriteI2C( 0x58, 0x41, 0x93)
board.WriteI2C( 0x58, 0x42, 0x40)  # FRAC_2ND_ADD
board.WriteI2C( 0x58, 0x41, 0x94)
board.WriteI2C( 0x58, 0x42, 0x40)  # FRAC_1ST_SUB
board.WriteI2C( 0x58, 0x41, 0x95)
board.WriteI2C( 0x58, 0x42, 0x40)  # FRAC_1ST_SUB
board.WriteI2C( 0x58, 0x41, 0x96)
board.WriteI2C( 0x58, 0x42, 0x40)  # FRAC_2ND_SUB
board.WriteI2C( 0x58, 0x41, 0x97)
board.WriteI2C( 0x58, 0x42, 0x40)  # FRAC_2ND_SUB
```

8.3.19.5.2 Other Audio Configurations

Figure 8-9 shows an example audio configuration of 8-Ch I2S input and output to I2S_DA pin on each deserializer.

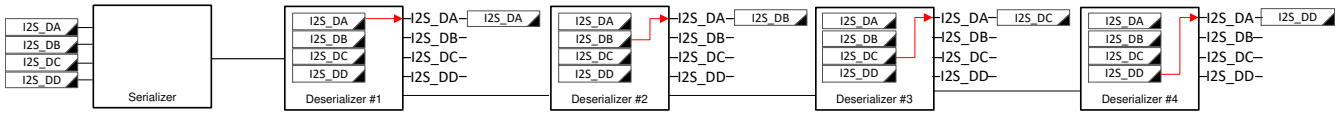

Figure 8-9. 1x4 Daisy Chain 8-Ch I2S Audio Input

Figure 8-10 shows an example audio configuration of 8-Ch I2S input and output using DP/eDP audio packets.

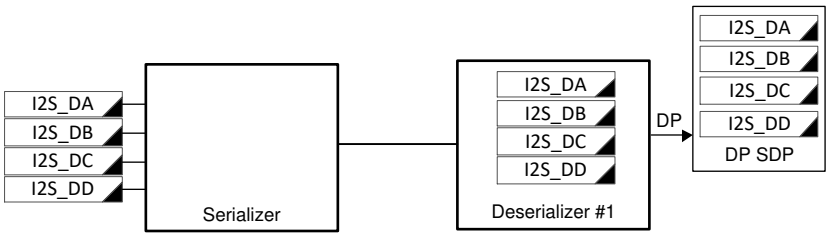

Figure 8-10. DP/eDP Audio Packet Output

8.3.20 Deserializer Synchronization and Splitting

It is common to use multiple interface ports to accommodate high resolution images at lower rates, such as eDP panels. Because of this, the DS90UH984-Q1 deserializers support synchronization both between two ports on a single deserializer and between two deserializers. Dual deserializer synchronization is done using the SYNC0 and SYNC1 pins to achieve synchronization within 100 pixels.

8.3.20.1 Single Deserializer Synchronization and Splitting

When paired with the proper serializer, symmetric splitting is available based on alternating pixel. This splitting results in two synchronized output streams, which must have the same timing parameters.

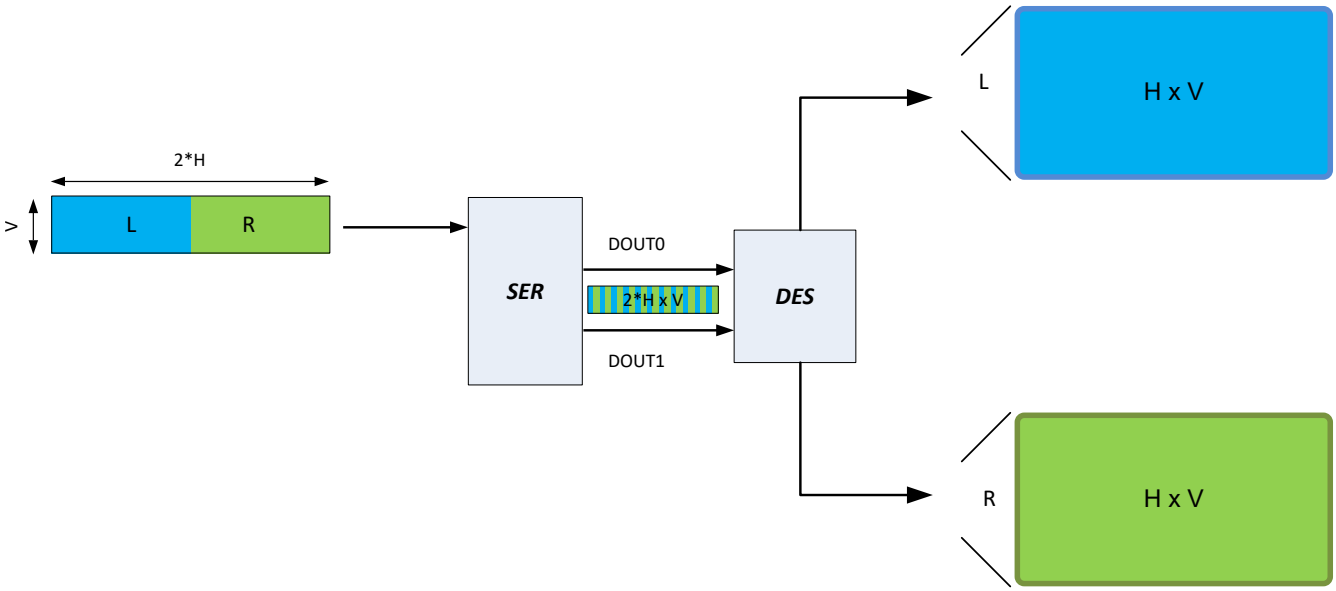

Figure 8-11. Synchronized Single Deserializer with Alternating Pixel Splitting

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8.3.20.2 Dual Deserializers Synchronization and Splitting

The DS90UH984-Q1 is able to accommodate synchronized outputs between one serializer and two deserializers, in alternate pixel splitting mode.

Dual deserializer synchronization is done using the SYNC0 and SYNC1 pins to achieve synchronization within 100 pixels. Each deserializer must have the SYNC pins attached to the other to allow proper synchronization setup. SYNC0 and SYNC1 pins will automatically be configured as inputs or outputs while in dual serializer synchronization mode.

Dual deserializers synchronization constraints:

- Reference clock port must be synchronized in phase at arrival of input port down to 150ps including board trace.
- The link layer configuration must be identical on both links (e.g. same timeslot & stream assignment on both links).
- All cable lengths are the same.
- The 4 images are identical resolutions.
- The same SSCG on the two Deserializers DPTX outputs (SSCG between SER and DES is not assumed synchronized).
- Streams should be synchronized between all DP/eDP outputs (two DS90UH984-Q1) within 100 pixels.
- The 2 inputs streams from the video source must always track within 50 pixels over the complete frame including any spread spectrum.

8.3.20.2.1 Single Serializer and Dual Deserializers

The DS90UH984-Q1 is able to accommodate synchronized outputs between one serializer and two deserializers, in alternate pixel splitting mode.

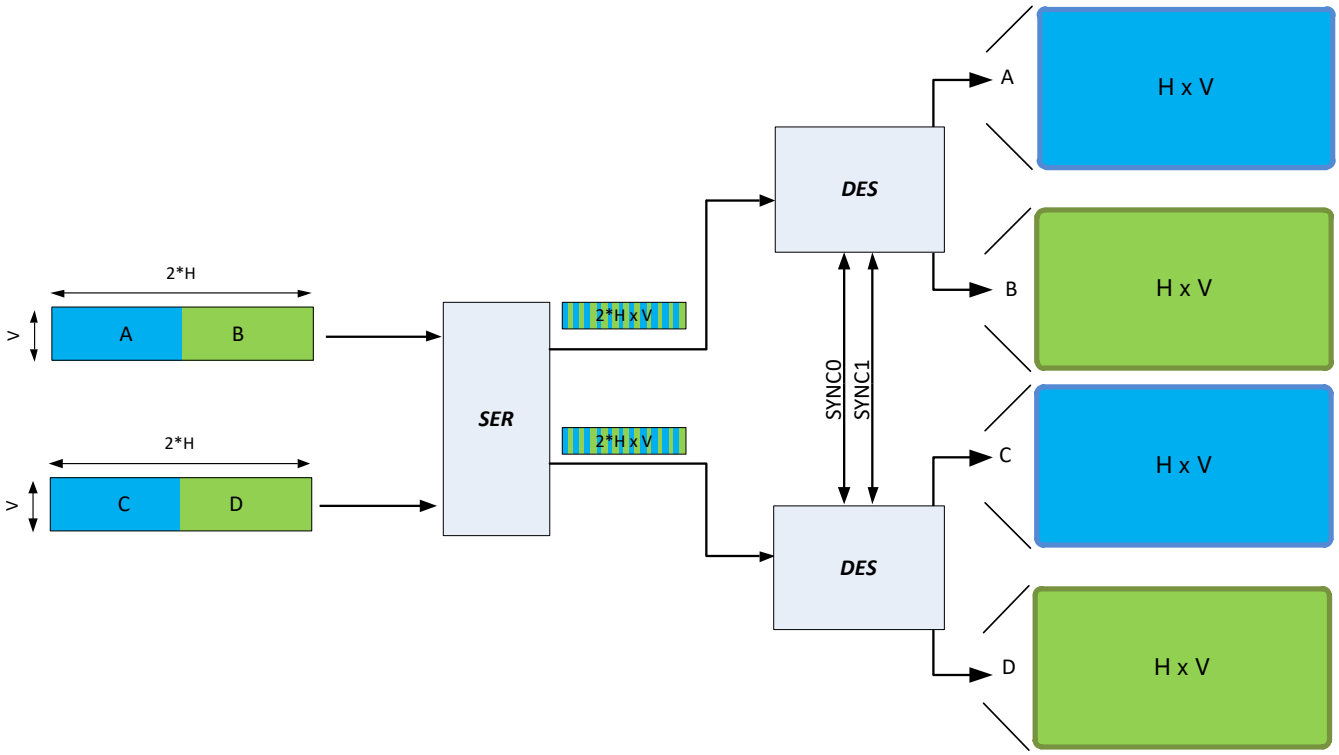

Figure 8-12. Synchronized Dual Deserializers With Alternating Pixel Splitting

8.3.20.2.2 Synchronized Dual Serializers and Dual Deserializers

The DS90UH984-Q1 is able to accommodate synchronized outputs between two serializers and two deserializers, in alternate pixel splitting mode.

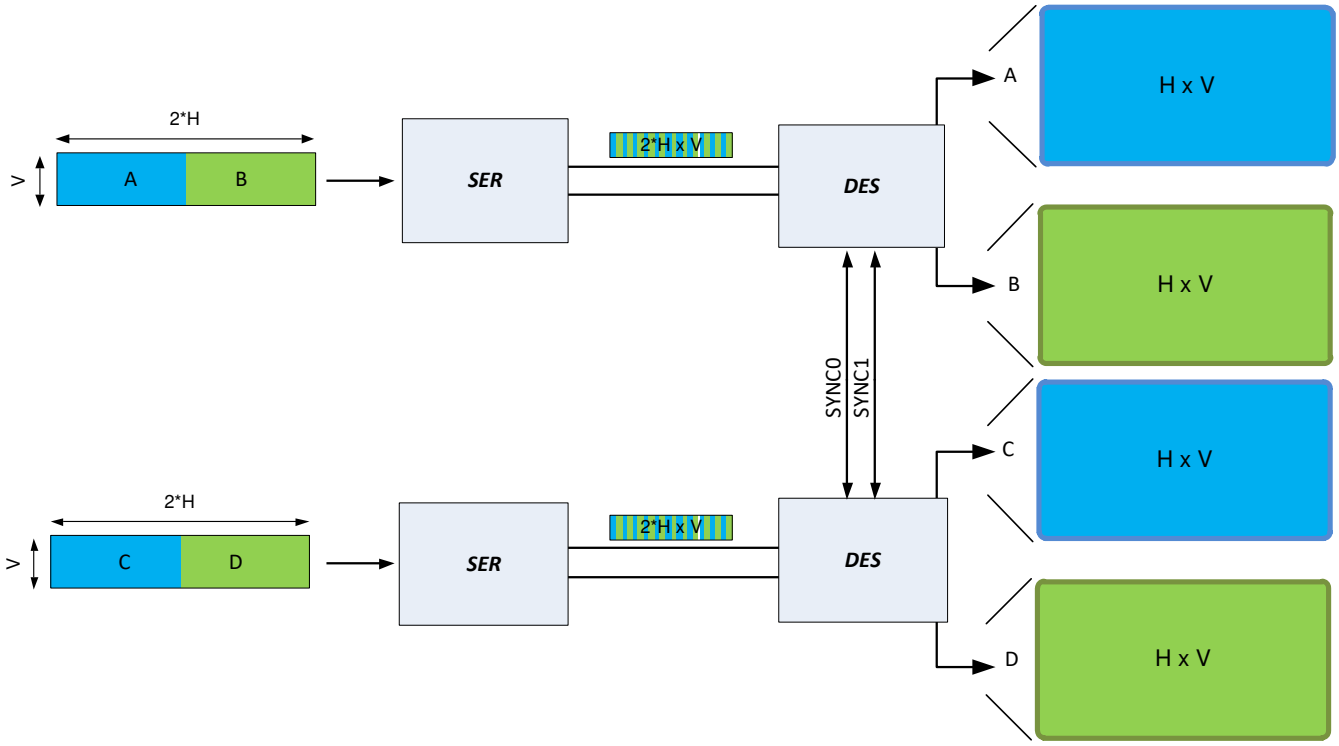

Figure 8-13. Synchronized Dual Serializers and Dual Deserializers

8.3.21 Daisy-Chain

The DS90UH984-Q1 can be used as a daisy-chain device to propagate video data received on single lane or dual lane FPD-Link IV connection and forward video to downstream deserializers. The DS90UH984-Q1 has two daisy-chain output ports DOUT0+/- and DOUT1+/- that can be configured into either single, dual, or independent FPD-Link III or FPD-Link IV up to 6.75Gbps. Daisy-chain operation is limited to a maximum of 3 daisy-chain capable devices plus one additional deserializer beyond the last daisy-chain. The last deserializer at the end of the daisy-chain can be either an FPD-Link IV deserializer or FPD-Link III deserializer.

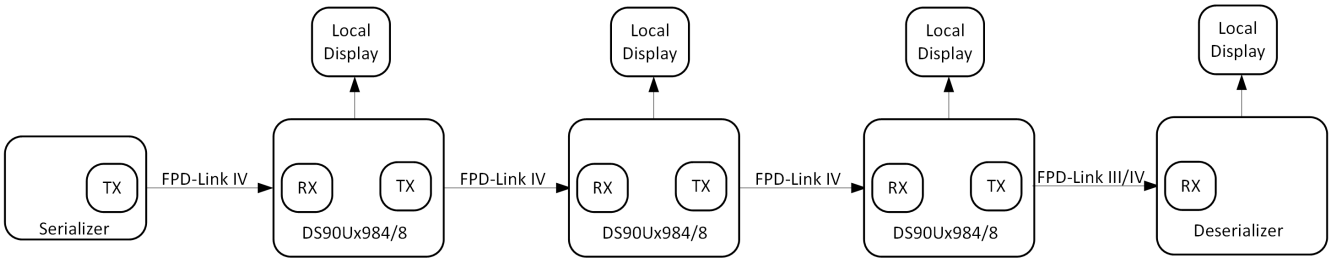

Figure 8-14. Maximum Daisy-Chain Supported

8.3.21.1 Daisy-Chain Mode of Operation

Each daisy-chain output channel can be configured for FPD-Link III or FPD-Link IV operation. Operation is controlled via register FPD4_TX_CFG 0xA8[5:2]. If both channels are in the same FPD-Link mode, the operation can be in single lane, dual lane, or independent mode. If the two channels are in different FPD-Link modes, each channel can only be in independent lane operation.

8.3.21.1.1 FPD-Link IV Daisy-Chain Output

When the DS90UH984-Q1 daisy-chain output is configured for FPD-Link IV operation, DS90UH984-Q1 can forward video to other DS90Ux98x deserializers for display. FPD-Link IV output can be configured as single, dual or independent output via register FPD4_TX_CFG 0xA8[5:2]. Daisy-chain on FPD-Link IV ports support up to 6

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video streams. Only video stream originating from an FPD-Link IV source can be forwarded on an FPD-Link IV daisy-chain output.

8.3.21.1.2 FPD-Link III Daisy-Chain Output

When the DS90UH984-Q1 daisy-chain output is configured for FPD-Link III operation, DS90UH984-Q1 can forward video to DS90Ux94x and DS90Ux92x deserializers. The FPD-Link III output can be configured as single, dual or independent output via indirect register Page_8 register 0x02[2:0]. In FPD-Link III mode, only a single video stream is supported. Any video stream which originated from an FPD-Link IV source can be forwarded on an FPD-Link III daisy-chain output.

8.3.21.1.2.1 FPD-Link III Single Link Operation

Single Link mode transmits the video over a single FPD-Link III to a single receiver. Single link mode supports frequencies up to 96 MHz for 24-bit video when paired with the DS90Ux940, DS90Ux940N, DS90Ux948, or DS90UB924. This mode is compatible with the DS90Ux926 or DS90Ux928 when operating below 85 MHz.

8.3.21.1.2.2 FPD-Link III Dual Link Operation

In Dual Link mode, the FPD-Link III TX splits a single video stream and sends alternating pixels on two downstream links. The receiver must be capable of receiving the dual-stream video. Dual link mode is capable of supporting a pixel clock frequency of up to 210 MHz (limited by deserializer capability), with each FPD-Link III TX port running at one-half the frequency. This allows support for full 2K video. The secondary FPD-Link III link could be used for high-speed control.

8.3.21.1.2.3 FPD-Link III Independent Operation

In this mode, the two FPD-Link channels operate as independent single link channels. When switching from independent to dual mode or vice-versa, a soft reset is required to establish the link.

8.3.21.2 FPD-Link IV Daisy-Chain PLL

The FPD-Link forward channel is generated based on a phase locked loop (PLL) as shown in Figure 8-15. The 27MHz XO is used as the reference source. In FPD-Link IV mode, the output of the PLL should be half of the data rate of the link. This output frequency is generated using the following settings, programmable via Page_3 of the indirect access registers. After modifying PLL values, reset the PLL using register 0x01 RESET_CTL[5:4]. When using daisy-chain FPD-Link rates greater than 6.75 Gbps, the TX LDO needs to be enabled through setting CHx_TX_LDO_EN field in Page_7 0x15[7:4] and 0x35[7:4] to 0b0000.

The following equation is used to calculate the VCO frequency:

$$f_{VCO} = f_{REF} \times 2 \times \left[N + \left(\frac{NUM}{DEN} \right) \right] \tag{50}$$

where

- f_{VCO} is the VCO frequency
- f_{Ref} is the reference frequency, either from XI
- N is the integer portion of the N-divider (0 to 65,535)
- NUM is the numerator portion of the N-divider fraction (0 to 16,777,206), NUM ≤ DEN
- DEN is the denominator portion of the N-divider fraction (1 to 16,777,206)

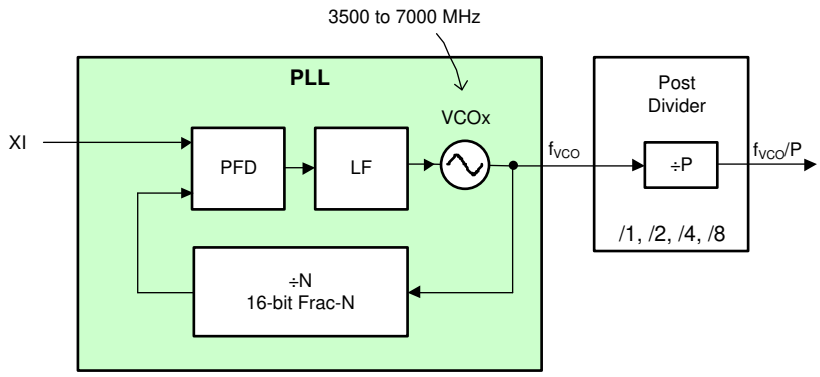

Figure 8-15. FPD-Link IV PLL

Table 8-32. FPD-Link IV PLL Settings for 13.5 Gbps, 12.528 Gbps, 10.8 Gbps, 6.75 Gbps and 3.375 Gbps

FPD-Link Data Rate	12.528 Gbps	10.8 Gbps	13.5 Gbps	6.75 Gbps	3.375 Gbps
FPD-Link Back Channel Rate	156.6 Mbps	168.75 Mbps			
Reference Source	XI (27 MHz)				
N-Divider	116 (NDIV[7:0] = 0x74, NDIV[15:8] = 0x00)	100 (NDIV[7:0] = 0x64, NDIV[15:8] = 0x00)	125 (NDIV[7:0] = 0x7D, NDIV[15:8] = 0x00)		
Numerator	0 (NUM[7:0] = 0x00, NUM[15:8] = 0x00, NUM[23:16] = 0x00)				
Denominator	16,777,206 (DEN[7:0] = 0xF6, DEN[15:8] = 0xFF, DEN[23:16] = 0xFF)				
MASH Order	Integer (MASH_ORDER = 0x0)				
Post-Divider	1 (POST_DIV = 0x0)			2 (POST_DIV = 0x1)	
FPD-Link Frequency	6.264 GHz	5.4 GHz	6.75 GHz	3.375 GHz	1.6875 GHz
Back Channel Down Sampling	1 (BC_DOWNSAMPLING_RATE = 0x1)	0 (BC_DOWNSAMPLING_RATE = 0x0)	1 (BC_DOWNSAMPLING_RATE = 0x1)	0 (BC_DOWNSAMPLING_RATE = 0x0)	
Half Rate Mode	1 (HALFRATE_MODE_CHx =0x1)				0 (HALFRATE_MODE_CHx =0x0)
TX LDO Enable	Enabled (CHx_TX_LDO_EN = 0b0000)	Enabled (CHx_TX_LDO_EN = 0b0000)	Enabled (CHx_TX_LDO_EN = 0b0000)	Disabled (CHx_TX_LDO_EN = 0b1111)	Disabled (CHx_TX_LDO_EN = 0b1111)

8.3.21.3 Daisy-Chain Output Spread Spectrum Clock Generation (SSCG)

If desired, spread spectrum clocking may be enabled for the FPD-Link forward channel ranging between 30 kHz and 33 kHz modulation frequency and up to 0.5% frequency deviation for center spread mode or 0.25% for down spread mode. Daisy-chain FPD-Link forward channel SSCG and back channel SSCG combined should not exceed 0.5% total frequency deviation. Both center-spread and down-spread ramps are supported. The deserializer spread spectrum capabilities should be checked to ensure proper spread spectrum compatibility. It is recommended to use center-spread SSC such that the average FPD-Link rate is maintained. If down-spread is desired, this will reduce the FPD-Link bandwidth and must be considered in bandwidth calculations. In FPD-Link IV mode, the effects of SSC should be considered when choosing the appropriate M and N values.

The FPD PLL must be configured in fractional mode to enable SSCG. If the PLL was originally configured in integer mode (NUM[23:0] = 0), set NUM[23:0] equal to the value of DEN[23:0], and subtract one from the original NDIV[15:0] value. Additionally, set MASH_ORDER to fractional mode (e.g. MASH_ORDER = 2).

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For instance, to enable SSCG using the default FPD-Link IV PLL settings set NDIV = 124 and NUM[23:0] = 16,777,206. To configure spread spectrum clock generation, the following equations can be used to calculate the RAMPX_STOP and RAMPX_INC.

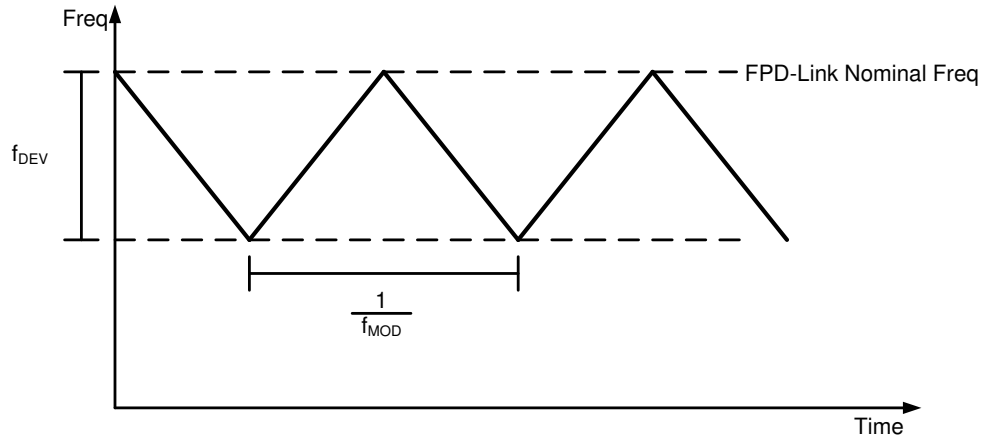

Figure 8-16. Down Spread SSCG

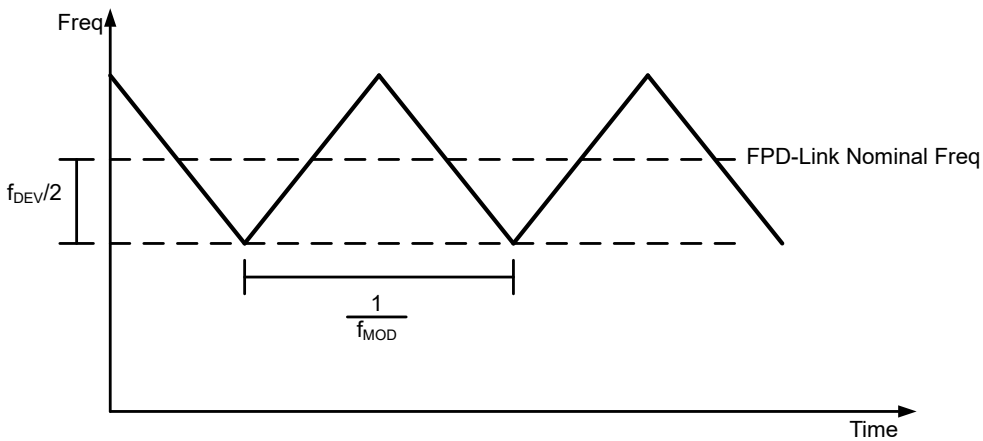

Figure 8-17. Center Spread SSCG

$$RAMPX_STOP = \frac{f_{REF}}{(4 \times f_{MOD})} \tag{51}$$

where

- f_{REF} is the reference clock in kHz (27000)
- f_{MOD} is the modulation frequency in kHz

$$RAMPX_INC_{Initial} = \frac{(VCO_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP)} \tag{52}$$

- $RAMPX_INC_{Initial}$ must be rounded to an integer number

where

- f_{DEV} is the deviation frequency as a percentage of the forward channel frequency (Example: deviation frequency = 0.5% = f_{DEV} = 0.5)
- i_{SPREAD} = 2
- $DEN_{Initial}$ is the denominator of the N-divider in the FPD PLL (16,777,206 for FPD-Link IV Mode)
- VCO_freq is the VCO frequency in MHz

- REFCLK is the reference clock frequency in MHz (27)

$$x = \begin{cases} \log_2 \dfrac{RAMPX_INC_{Initial}}{32767}, & RAMPX_INC_{Initial} > 32767 \\ 0, & RAMPX_INC_{Initial} \le 32767 \end{cases} \tag{53}$$

where

- x must be rounded up to the nearest integer

$$RAMPX_INC_{Final} = \frac{(VCO_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP \times 2^x)} \tag{54}$$

$$DEN_{Final} = \left(\frac{DEN_{Initial}}{2^x}\right) \tag{55}$$

$$NUM_{Final} = \left(\frac{NUM_{Initial}}{2^x}\right) \tag{56}$$

where

- Initial numerator and denominator are determined based on the FPD-Link rate. If the original PLL setting is integer mode (numerator = 0) then the first step of applying SSCG is to convert to fractional mode (subtract one from the integer part of the n divider and set both numerator and denominator to 16,777,206).

$$VCO_{Freq,Final} = f_{REF} \times 2\left[Ndiv + \left(\frac{NUM_{Final}}{DEN_{Final}}\right)\right] \tag{57}$$

$$f_{DEV,Final} = \left[\frac{(RAMPX_INC_{Final} \times REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP)}{(VCO_{Freq,Final} \times DEN_{Final})}\right] \tag{58}$$

For instance, to configure SSCG with f_{MOD} = 30 KHz SSCG with center-spread f_{DEV} = 0.5% frequency deviation and a reference clock of 27 MHz in FPD-Link IV Mode at a VCO frequency of 6.75 GHz.

$$RAMPX_STOP = \frac{f_{REF}}{(4 \times f_{MOD})} \tag{59}$$

$$RAMPX_STOP = \frac{27 \times 10^6}{(4 \times 30 \times 10^3)} = 225 \tag{60}$$

$$RAMPX_INC_{Initial} = \frac{(VCO_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP)} \tag{61}$$

$$RAMPX_INC_{Initial} = \frac{(6.75 \times 10^9 \times 0.5 \times 16{,}777{,}206)}{(27 \times 10^6 \times 2 \times 100 \times 2 \times 225)} = 23301.675 \approx 23302 \tag{62}$$

$$x = \log_2\left(\frac{23302}{32767}\right) = -0.49179 \approx 0 \tag{63}$$

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$$RAMPX_INC_{Final} = \frac{(VCO_freq \times f_{DEV} \times DEN_{Initial})}{(REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP \times 2^{x})} \tag{64}$$

$$RAMPX_INC_{Final} = \frac{(6.75 \times 10^{9} \times 0.5 \times 16{,}777{,}206)}{(27 \times 10^{6} \times 2 \times 100 \times 2 \times 225 \times 2^{0})} = 23301.675 \approx 23302 \tag{65}$$

$$DEN_{Final} = \left(\frac{DEN_{Initial}}{2^{x}}\right) \tag{66}$$

$$DEN_{Final} = \left(\frac{16{,}777{,}206}{2^{0}}\right) = 16{,}777{,}206 \tag{67}$$

$$NUM_{Final} = \left(\frac{NUM_{Initial}}{2^{x}}\right) \tag{68}$$

$$NUM_{Final} = \left(\frac{16{,}777{,}206}{2^{0}}\right) = 16{,}777{,}206 \tag{69}$$

$$VCO_{Freq,Final} = f_{REF} \times 2\left[Ndiv + \left(\frac{NUM_{Final}}{DEN_{Final}}\right)\right] \tag{70}$$

$$VCO_{Freq,Final} = 27 \times 10^{6} \times 2\left[124 + \left(\frac{16{,}777{,}206}{16{,}777{,}206}\right)\right] = 27 \times 10^{6} \times 250 = 6.75 \times 10^{9} \tag{71}$$

$$f_{DEV,Final} = \left[\frac{(RAMPX_INC_{Final} \times REFCLK \times 2 \times 100 \times i_{SPREAD} \times RAMPX_STOP)}{(VCO_{Freq,Final} \times DEN_{Final})}\right] \tag{72}$$

$$f_{DEV,Final} = \left[\frac{(23302 \times 27 \times 10^{6} \times 2 \times 100 \times 2 \times 225)}{(6.75 \times 10^{9} \times 16{,}777{,}206)}\right] = 0.5 \tag{73}$$

8.3.21.4 FPD-Link III Daisy-Chain PLL

The FPD-Link III clock is generated using a phase-locked loop (PLL) with the 27Mhz XO as reference source.The VCO (voltage controlled oscillator) covers a frequency range from 3500 MHz to 7000 MHz. Configuring the PLL requires selecting the VCO, setting the N-divider, numerator, denominator, MASH order (either integer or fractional), and the post-divider. After configuring these settings, the PLL should be reset using either the PLL_CH0_RESET or PLL_CH1_RESET bits (0x1[5] or 0x1[4]). The video processor clock is governed by the following equations:

$$\text{FPD-Link III Line Rate (Mbps)} = \text{Target PCLK} \times 35 \tag{74}$$

$$f_{VCO}\ \text{(MHz)} = \text{FPD-Link III Line Rate} / 2 \times P \tag{75}$$

where

- f_{VCO} is the VCO frequency
- P is the post-divider value (2, 4, 8, or 16)

$$f_{VCO} = f_{Ref} \times 2 \times (N + NUM / DEN) \tag{76}$$

where

- f_{Ref} is the reference frequency, either from the XO
- N is the integer portion of the N-divider (0 to 65,535)
- NUM is the numerator portion of the N-divider fraction (0 to 16,777,206), NUM ≤ DEN
- DEN is the denominator portion of the N-divider fraction (1 to 16,777,206)

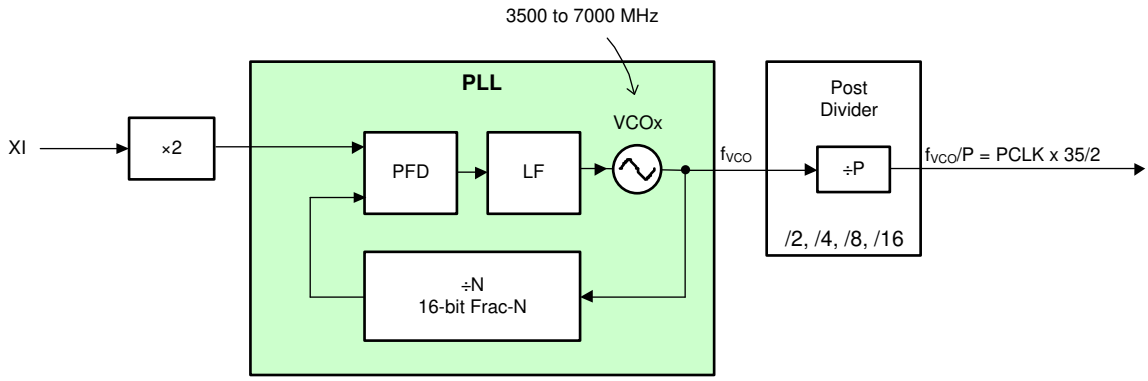

Figure 8-18. FPD-Link III PLL

Example FPD-Link III PLL Calculation

1. Start with the desired PCLK frequency and calculate the corresponding FPD-Link III Line Rate (PCLK × 35).
   - EX: PCLK = 95.75 MHz, so FPD-Link III Line Rate = 3351.25 MHz
2. Then consider all potential VCO frequencies (FPD-Link III Line Rate / 2 × P) and find the list of possible VCOs and VCO frequencies.
   - EX: Potential VCO frequencies are: 3351.25 / 2 × 2 = 3351.25 MHz, 3351.25 / 2 × 4 = 6702.5 MHz, 3351.25 / 2 × 8 = 13,405 MHz, and 3351.25 / 2 × 16 = 26,810 MHz. Only 6702.5 MHz is a valid VCO frequency, which can be generated only by VCO2. This means that VCO_SEL should be programmed to 0x1 (VCO2) and POST_DIV should be programmed to 0x6 (selects a post-divider of 4).
3. Determine the integer portion of the N-divider (integer portion of f_{VCO}/ (2 × f_{Ref})).
   - EX: 6702.5 / (2 × f_{Ref}) = 6702.5 / (2 × 27) = 124.12 so the integer portion will be 124. This means that NDIV[7:0] should be programmed to 0x7C and NDIV[15:8] should be programmed to 0x00.
4. Determine the numerator and denominator of the N-divider (fractional portion of f_{VCO}/ (2 × f_{Ref})).
   - EX: 6702.5 / (2 × 27) - 124 = 0.12 $\overline{037}$. It is preferred to use larger denominators when possible. To find the form of this fraction with the largest possible denominator, find the closest multiple of the denominator to the maximum denominator (16,777,206). Divide the maximum denominator (16,777,206) by the current denominator (108) and round down: 16,777,206 / 108 = 155,344.5 so use the 155,344th multiple of the original fraction. Multiplying our numerator and denominator by this factor gives us our final fraction: 2,019,472 / 16,777,152 [1]

Table 8-33. FPD-Link III Clock Register Configuration

VCO Select	VCO1: CHx_VCO_SEL = 0x0 VCO2: CHx_VCO_SEL = 0x1 VCO3: CHx_VCO_SEL = 0x2 VCO4: CHx_VCO_SEL = 0x3
N-Divider	NDIV[15:0] = Integer portion of N divider
Numerator	NUM[23:0] = Numerator portion of N divider
Denominator	DEN[23:0] = Denominator portion of N divider
MASH Order	Integer: MASH_ORDER= 0x0 Fractional: MASH_ORDER = 0x2

[1] Various methods may be used to find the fractional representation. Free tools to find a fractional representation of a decimal such as this one can simplify this process.

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Table 8-33. FPD-Link III Clock Register Configuration (continued)

Post-Divider	2: POST_DIV = 0x5 4: POST_DIV = 0x6 8: POST_DIV = 0x7 16: POST_DIV = 0x4

8.3.21.5 FPD-Link III Daisy-Chain Back Channel Configuration

For FPD-Link III daisy-chain mode only, the back channel needs to be enabled via the following script:

```
#FPD-Link III Port 0 Back channel enable
board.WriteI2C(DEV_ADDR,0x40,0x1C)
board.WriteI2C(DEV_ADDR,0x41,0x05)
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x41,0x0D)
board.WriteI2C(DEV_ADDR,0x42,0x70)
board.WriteI2C(DEV_ADDR,0x41,0x0E)
board.WriteI2C(DEV_ADDR,0x42,0x70)
board.WriteI2C(DEV_ADDR,0x41,0x06)
board.WriteI2C(DEV_ADDR,0x42,0xFF)
board.WriteI2C(DEV_ADDR,0x41,0x08)
board.WriteI2C(DEV_ADDR,0x42,0x1C)
#FPD-Link III Port 1 Back channel enable
board.WriteI2C(DEV_ADDR,0x40,0x1C)
board.WriteI2C(DEV_ADDR,0x41,0x25)
board.WriteI2C(DEV_ADDR,0x42,0x00)
board.WriteI2C(DEV_ADDR,0x41,0x2D)
board.WriteI2C(DEV_ADDR,0x42,0x70)
board.WriteI2C(DEV_ADDR,0x41,0x2E)
board.WriteI2C(DEV_ADDR,0x42,0x70)
board.WriteI2C(DEV_ADDR,0x41,0x26)
board.WriteI2C(DEV_ADDR,0x42,0xFF)
board.WriteI2C(DEV_ADDR,0x41,0x28)
board.WriteI2C(DEV_ADDR,0x42,0x1C)
```

8.3.21.6 FPD-Link Streams

FPD-Link IV protocol supports up to six distinct streams to be transferred over daisy-chain output. Stream ID assignment from the upstream device can be reassigned at DS90UH984-Q1 daisy-chain output. Stream ID assignment is controlled via indirect register Page_17 registers 0x02 - 0x04 (Daisy-chain Port 0) and registers 0x12 - 0x14 (Daisy-chain Port 1). Indirect register Page_17 registers 0x01[5:0] and 0x11[5:0] enable the corresponding video stream for each daisy-chain port.

8.3.21.7 FPD-Link Timeslots

There are 65 total timeslots, which are used to divide the available FPD-Link bandwidth between different streams. The number of timeslots allocated to each stream are configured through indirect register Page_17 registers LINK0_SLOT_REQx(0x06 to 0x0B) and registers LINK1_SLOT_REQx registers (0x16 to 0x1B). If fewer than 65 timeslots are requested, the additional timeslots will be assigned to Stream 0. If greater than 65 timeslots are requested (an invalid configuration), priority is given to lower stream numbers. Timeslot assignments are updated only after the LINK_LAYER_CTL register EN_NEW_TSLOTx bit is set. In Dual FPD-Link mode only the LINK0 registers are used. In general, timeslots should be assigned based on the proportion of the available bandwidth required by the individual stream. The FPD-Link IV link has a line rate of 6.75 Gbps, resulting in 6.55 Gbps of bandwidth for video data (6.75 Gbps * 128/132).

The time slot assignments are considered static and should not be modified during video transmission. It is recommended to adhere to the following procedure when modifying time slot assignments:

1. Disable the link layer (set LINK_LAYER_x_EN = 0)
2. Configure time slots through LINK0_SLOT_REQx and LINK1_SLOT_REQx registers
3. Set EN_NEW_TSLOTx = 1
4. Enable the link layer (set LINK_LAYER_x_EN = 1)

   If there is a change in link rate or SSCG configuration after time slots are enabled, the link layer timeslots should be refreshed by setting EN_NEW_TSLOTx = 1.

8.3.21.7.1 Example Timeslot Assignment

1. Calculate the required bandwidth for each image by multiplying the PCLK by the number of bits per pixel.
   - EX: Stream 0: PCLK = 200 MHz with 30 bpp. Required bandwidth = 200 MHz * 30 bpp = 6.0 Gbps
     Stream 1: PCLK = 112 MHz with 24 bpp. Required bandwidth = 112 MHz * 24 bpp = 2.688 Gbps
2. Calculate the proportion of the available bandwidth needed for each stream and the corresponding number of timeslots (Stream Bandwidth / Available Bandwidth * Total Number of Timeslots rounded up).
   - EX: Stream 0: Proportion of Available Bandwidth = 6.0 Gbps / 13.09 Gbps = 0.46.
   - Number of Timeslots = 65*0.46 = 29.9 ≈ 30 Timeslots
     Stream 1: Proportion of Available Bandwidth = 2.688 Gbps / 13.09 Gbps = 0.21.
   - Number of Timeslots = 65*0.21 = 13.35 ≈ 14 Timeslots
3. Verify the total number of timeslots is less than 65.
   - EX: 30 Timeslots for Stream 0 + 14 Timeslots for Stream 1 = 44 Timeslots is < 65 Timeslots so this configuration is valid.
4. (Optional) Assign extra timeslots evenly between streams. If this step is skipped, the remaining timeslots will be assigned to Stream 0.
   - EX: 65 - 44 = 21 remaining timeslots. Add 11 timeslots to Stream 0 and 10 timeslots to Stream 1. Stream 0 should be assigned 41 timeslots total (LINKx_SLOT_REQ0 = 0x29) and Stream 1 should be assigned 24 timeslots total (LINKx_SLOT_REQ1 = 0x18).

8.3.22 Channel Monitor Loop-Through Output Driver

The DS90UH984-Q1 includes an internal Channel Monitor Loop-through output on the CMLOUT_P/N pins. The CMLOUT_P/N supplies a buffered loop-through output driver to observe the jitter after equalization for each of the two RX receiver channels. The CMLOUT monitors the post CDR stage, thus providing the recovered input of the deserializer signal. The measured serial data width on the CMLOUT loop-through is the total jitter including the internal driver, AEQ, and back channel echo. It is recommended to enable the terminations for the loop-through path. CMLOUT is only available for FPD-Link rates up to 6.75 Gbps. In FPD-Link IV mode, it is recommended to use Internal Eye Open Monitor instead of monitoring CMLOUT pins.

The following script can be used to activate CMLOUT for FPD-Link III:

```
def SET_LOOPTHRU_CHANNEL(devAddr=0x58,CHANNEL=0, EN_TERM=0):
    Set the output of the loop through function
    :param CHANNEL: A value of 0 select channel 0 and a value of 1 select channel 1
    :param EN_TERM: 0 disable terminations for the loop through path. 1 enables it. Default is 0.

    if EN_TERM == 1:
        eq_index = board.ReadI2C(devAddr, reg_addr=(0x11 + CHANNEL * 0x30), page=14)
        set_ctle = eq_index + 0x40
        board.WriteI2C(devAddr, reg_addr=(0x1a + CHANNEL * 0x30), reg_value=set_ctle, page=14)

    board.WriteI2C(devAddr, reg_addr=0x05, reg_value=(1 - CHANNEL), page=0x04, msb=0, lsb=0)
    board.WriteI2C(devAddr, reg_addr=(0x05 + 0x20), reg_value=CHANNEL, page=0x4, msb=0, lsb=0)
    board.WriteI2C(devAddr, reg_addr=(0x07 + 0x20), reg_value=EN_TERM, page=0x4, msb=7, lsb=7)
    board.WriteI2C(devAddr, reg_addr=0x46, reg_value=EN_TERM, page=0x4, msb=1, lsb=1)
    board.WriteI2C(devAddr, reg_addr=0x49, reg_value=(EN_TERM << CHANNEL), page=0x4, msb=7, lsb=6)
    board.WriteI2C(devAddr, reg_addr=0x49, reg_value=0x5, page=0x4, msb=2, lsb=0)
    return
```

8.3.23 Internal Eye Open Monitor

The DS90UH984-Q1 includes an internal eye open monitor (EOM) tool to observe a representation of the eye opening. The eye sweep test starts from the eye center and sweeps horizontal phase and vertical amplitudes. Margin error count is read during the sweep to derive an eye opening representation.

The EOM tool is the preferred link analysis method over CMLOUT and can be applied for all rates.

8.3.24 Adaptive Equalizer

The FPD-Link IV receiver inputs incorporate an adaptive equalizer (AEQ), to compensate for signal degradation from the communications channel and interconnect components. Each RX port signal path continuously monitors cable characteristics from long-term cable aging and temperature changes. The AEQ is primarily

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intended to adapt and compensate for channel losses over the lifetime of a cable installed in an automobile. The AEQ attempts to optimize the equalization setting of the RX receiver. This adaption includes compensating insertion loss from temperature effects and aging degradation due to bending and flexion.

8.3.24.1 FPD-Link III Adaptive Equalizer

The FPD-Link III AEQ process steps through allowed values of the equalizer controls, and finds a value that allows the Clock Data Recovery (CDR) circuit to maintain valid lock condition. For each EQ setting, the circuit waits for a programmed re-lock time period, then checks results for valid lock. If valid lock is detected, the circuit will stop at the current EQ setting and maintain a constant value as long as the lock state persists. If the deserializer loses LOCK, the adaptive equalizer will resume the LOCK algorithm and the EQ setting is incremented to the next valid state. Once lock is lost, the circuit will continue searching EQ settings to find a valid setting to reacquire the serial data stream sent by the serializer that remains locked.

See Section 8.3.24.1.4 for a script example for forcing FPD-Link III AEQ settings.

8.3.24.1.1 FPD-Link III AEQ Min/Max Settings

The AEQ circuit can be programmed with minimum and maximum settings used during the EQ adaption. Using the full AEQ range provides the most flexible solution. However, if the channel conditions are known, an improved deserializer lock time can be achieved by narrowing the search window of the allowable EQ gain settings. For example, in a system use case with a longer cable and multiple interconnects creating higher channel attenuation, the AEQ would not adapt to the minimum EQ gain settings. The AEQ range is determined by the AEQ_MAX_FPD3 (Page_14 0x18) and AEQ_MIN_FPD3 (Page_14 0x19) registers.

8.3.24.1.2 FPD-Link III AEQ Timing

The dwell time for AEQ to wait for lock or error-free status is also programmable. When checking each EQ setting the AEQ will wait for a time interval, controlled by the ADAPTIVE_EQ_RELOCK_TIME_FPD3 field in the Page_14 AEQ_RELOCK_FPD3 register before incrementing to the next allowable EQ gain setting. The default wait time is set to 0.655 ms based on REFCLK = 27 MHz. When the maximum setting is reached and there is no lock acquired during the programmed relock time, the AEQ will restart adaption at minimum setting or AEQ_MIN value.

8.3.24.1.3 FPD-Link III AEQ SFILTER

The AEQ circuit may be programmed to adapt the SFILTER setting for clock/data phase correction in addition to the EQ setting. When the AEQ_SFILTER_EN bit is set in the Page_14 AEQ_SFILTER_CTL register 0x24, the SFILTER will be adapted as an outer-loop value with the EQ setting as the inner loop. In this mode, the circuit first searches through all EQ settings at the minimum SFILTER setting. If no error-free setting is detected, the circuit will increment SFILTER and search through all EQ settings. Once a valid setting is detected, the circuit will stop and indicate that AEQ is valid. By also setting the AEQ_OUTER_LOOP register bit, the EQ setting will be handled as the outer loop variable and the SFILTER as the inner loop. The AEQ_SFIL_ORDER controls the search order for the SFILTER. If set to 0, the settings will be searched from minimum to maximum. If set to 1, the settings will be searched starting at the mid-point (no additional clock data delay) and searching in the positive direction, then searching from mid-point in the negative direction. The SFILTER adaption can be programmed with minimum and maximum settings for the SFILTER adaption via the SFILTER_CFG register 0x26 on Page_14. The min/max settings may be between 0 and 12, with max always programmed greater than or equal to the min value.

8.3.24.1.4 Example FPD-Link III AEQ Optimization

The following script forces the FPD-Link III AEQ values including AEQ min/max settings, SFILTER min/max and enable, AEQ timing, and AEQ outer loop.

```
def
FPD3_AEQ_OPTIMIZATION(DEVICE_ADR,CHANNEL,SFILTER_EN=1,AEQ_MIN=0x00,AEQ_MAX=0x3F,SFIL_MIN=5,SFIL_MAX=
8,ADAPTIVE_EQ_RELOCK_TIME_FPD3=2,AEQ_RELOCK_WAIT_TIME=3,AEQ_SCAN_EN=1,AEQ_OUTER_LOOP=1):
    board.WriteI2C(DEVICE_ADR,0x40,14*4)
    if CHANNEL==0:
        Offset = 0x00
    elif CHANNEL==1:
        Offset = 0x30
```

```
    board.WriteI2C(DEVICE_ADR,0x41,0x18+Offset)
    board.WriteI2C(DEVICE_ADR,0x42,AEQ_MAX)
    board.WriteI2C(DEVICE_ADR,0x41,0x19+Offset)
    board.WriteI2C(DEVICE_ADR,0x42,AEQ_MIN)
    board.WriteI2C(DEVICE_ADR,0x41,0x17+Offset)
    WriteI2C_MASK (DEVICE_ADR,0x42,ADAPTIVE_EQ_RELOCK_TIME_FPD3, 0x0F)
    board.WriteI2C(DEVICE_ADR,0x41,0x24+Offset)
    WriteI2C_MASK (DEVICE_ADR,0x42,((SFILTER_EN<<6)), 0x40)
    WriteI2C_MASK (DEVICE_ADR,0x42,((AEQ_OUTER_LOOP<<5)), 0x20)
    board.WriteI2C(DEVICE_ADR,0x41,0x26+Offset)
    board.WriteI2C(DEVICE_ADR,0x42,(((SFIL_MAX<<4)))+SFIL_MIN)
    board.WriteI2C(DEVICE_ADR,0x41,0x2C+Offset)
    WriteI2C_MASK (DEVICE_ADR,0x42,(((AEQ_SCAN_EN<<4))),0x10)
    board.WriteI2C(DEVICE_ADR,0x41,0x2E+Offset)
    WriteI2C_MASK (DEVICE_ADR,0x42,((AEQ_RELOCK_WAIT_TIME<<4)), 0xF0) K)
    return
```

8.3.24.2 FPD-Link IV Adaptive Equalizer

The FPD-Link IV AEQ process is based on Least-Mean-Squared (LMS) along with 2-tap Decision-Feedback-Equalizer (DFE) algorithm, that adapts to the optimized EQ setting that tracks with voltage and temperature, and aging changes. The EQ portion of the adaptation is frozen once the algorithm finds an optimum EQ setting. However, the DFE coefficients continue to adapt to track over voltage and temperature changes. In the event that lock drops the LMS algorithm repeats with EQ adaptation followed by DFE adaptation.

The LMS-AEQ algorithm can be programmed with a minimum initial value set by Page_23 EQ_CTLE_ACC_INIT registers 0x1F-0x20 (Port 0) and 0x9F-0xA0 (Port 1) to optimize for the lock time and variability and channel losses.

8.4 Device Functional Modes

8.4.1 Mode Select Configuration Settings

Configuration of the device may be done via the MODE_SEL0, MODE_SEL1, and the MODE_SEL2 input pins, or via the configuration register bits. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[2:0] inputs. See Table 8-35. Changing the MODE_SEL[2:0] strap settings requires PDB to be toggled. These values will be latched into register location during power-up:

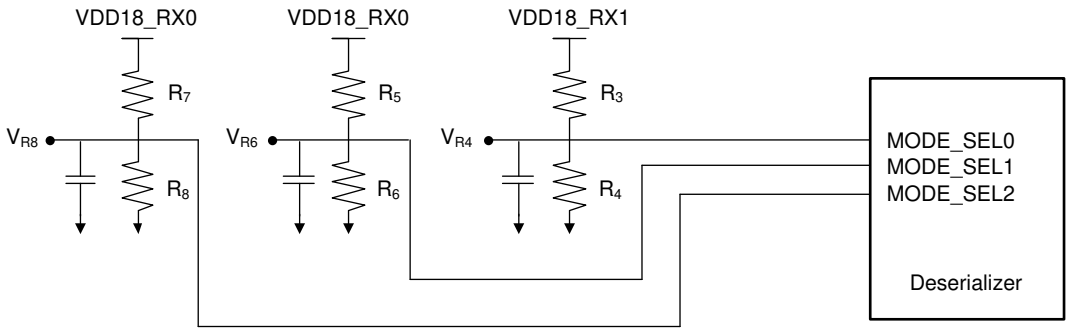

Figure 8-19. MODE_SEL[2:0] Connection Diagram

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Table 8-34. MODE_SEL[2:0] Settings Selection

MODE SELECTION	MODE	FUNCTION
MODE_SEL0	FPD RX Mode	FPD-Link IV protocol
		Backward compatible FPD-Link III
	FPD-Link IV Rates	13.5Gbps, 12.528 Gbps, 10.8Gbps, 6.75Gbps, 3.375Gbps
	FPD-Link III RX VCO Range	VCO_High (100 MHz ≤ PCLK ≤ 190 MHz)
		VCO_Mid (50 MHz ≤ PCLK ≤ 100 MHz)
		VCO_Low (25 MHz ≤ PCLK ≤ 50 MHz)
	Daisy-chain Mode	Dual
		Independent
		Disable
MODE_SEL1	DP/eDP	DP0
		DP0 & DP1
		eDP0
		eDP0 & eDP1
	HPD	3.3V IO
		1.8V IO
MODE_SEL2	MODE_SEL0 Table	Daisy-chain Enabled (FPD4 only)
		Daisy-chain Disabled (FPD3 & FPD4)
	Synchronization	Primary
		Secondary
		Disabled

Table 8-35. Configuration Select MODE_SEL0 When MODE_SEL2 Set To Daisy Chain Enabled

#	RATIO V_{R4}/V_{DD18}			TARGET V_{R4} (V)	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	FPD Rate (Gbps)	FPD RX Mode	FPD TX Mode	FPD Rate TX (Gbps)
	Min	Typical	Max							
1	0	0	0.135	0	OPEN	Any value less than 100	10.8	FPD4 Auto-detect	FPD Independent	6.75
2	0.176	0.213	0.247	0.384	42.2	11.5	10.8	FPD4 Auto-detect	FPD Dual	6.75
3	0.289	0.327	0.363	0.589	29.4	14.3	13.5	FPD4 Auto-detect	FPD Independent	6.75
4	0.407	0.441	0.467	0.793	28.7	22.6	13.5	FPD4 Auto-detect	FPD Dual	6.75
5	0.526	0.555	0.584	0.999	15	18.7	6.75	FPD4 Auto-detect	FPD Independent	6.75
6	0.64	0.671	0.701	1.208	13.7	28	6.75	FPD4 Auto-detect	FPD Dual	6.75
7	0.757	0.787	0.814	1.417	16.2	60.4	3.375	FPD4 Auto-detect	FPD Independent	3.375
8	0.877	0.924	1.0	1.663	Any value less than 100	OPEN	12.528	FPD4 Auto-detect	FPD Independent	Disabled – Register defaults for 6.75 Gbps Daisy-chain

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Table 8-36. Configuration Select MODE_SEL0 When MODE_SEL2 Set To Daisy Chain Disabled

#	RATIO V_{R4}/V_{DD18}			TARGET V_{R4} (V)	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	FPD Rate (Gbps)	FPD RX Mode	FPD TX Mode
	Min	Typical	Max						
1	0	0	0.135	0	OPEN	Any value less than 100	13.5	FPD4 Auto-detect	Disabled – Register defaults for 13.5 Gbps Daisy-chain
2	0.176	0.213	0.247	0.384	42.2	11.5	10.8	FPD4 Auto-detect	Disabled– Register defaults for 10.8 Gbps Daisy-chain
3	0.289	0.327	0.363	0.589	29.4	14.3	6.75	FPD4 Auto-detect	Disabled– Register defaults for 6.75 Gbps Daisy-chain
4	0.407	0.441	0.467	0.793	28.7	22.6	3.375	FPD4 Auto-detect	Disabled– Register defaults for 3.375 Gbps Daisy-chain
5	0.526	0.555	0.584	0.999	15	18.7	VCO (Auto-sweep)	FPD3 Auto-detect	Disabled– Register defaults for 6.75 Gbps Daisy-chain
6	0.64	0.671	0.701	1.208	13.7	28	VCO_High (100MHz-190 MHz)	FPD3 Auto-detect	Disabled– Register defaults for 6.75 Gbps Daisy-chain
7	0.757	0.787	0.814	1.417	16.2	60.4	VCO_Mid (50MHz-100MHz)	FPD3 Auto-detect	Disabled– Register defaults for 6.75 Gbps Daisy-chain
8	0.877	0.924	1.0	1.663	Any value less than 100	OPEN	VCO_Low (25-50MHz)	FPD3 Auto-detect	Disabled– Register defaults for 6.75 Gbps Daisy-chain

Table 8-37. Configuration Select MODE_SEL1

#	RATIO V_{R6}/V_{DD18}			TARGET V_{R6} (V)	SUGGESTED RESISTOR PULL-UP R5 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R6 kΩ (1% tol)	Display Output Enable	eDP_DP Mode	HPD
	Min	Typical	Max						
1	0	0	0.135	0	OPEN	Any value less than 100	eDP0 & eDP1	eDP	3.3V
2	0.176	0.213	0.247	0.384	42.2	11.5	eDP0 & eDP1	eDP	1.8V
3	0.289	0.327	0.363	0.589	29.4	14.3	eDP0	eDP	3.3V
4	0.407	0.441	0.467	0.793	28.7	22.6	eDP0	eDP	1.8V
5	0.526	0.555	0.584	0.999	15	18.7	DP0 & DP1	DP	3.3V
6	0.64	0.671	0.701	1.208	13.7	28	DP0 & DP1	DP	1.8V
7	0.757	0.787	0.814	1.417	16.2	60.4	DP0	DP	3.3V
8	0.877	0.924	1.0	1.663	Any value less than 100	OPEN	DP0	DP	1.8V

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Table 8-38. Configuration Select MODE_SEL2

#	RATIO V_{R8}/V_{DD18}			TARGET V_{R8} (V)	SUGGESTED RESISTOR PULL-UP R7 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R8 kΩ (1% tol)	Daisy Chain	DP/eDP SSCG fdev = 0.25%, fmod = 32kHz	Synchronization
	Min	Typical	Max						
1	0	0	0.135	0	OPEN	Any value less than 100	Daisy-Chain ON	0	Disabled
2	0.176	0.213	0.247	0.384	42.2	11.5	Daisy-Chain ON	1	Disabled
3	0.289	0.327	0.363	0.589	29.4	14.3	Daisy-Chain OFF	1	Primary
4	0.407	0.441	0.467	0.793	28.7	22.6	Daisy-Chain OFF	1	Secondary
5	0.526	0.555	0.584	0.999	15	18.7	Daisy-Chain OFF	1	Disabled
6	0.64	0.671	0.701	1.208	13.7	28	Daisy-Chain OFF	0	Primary
7	0.757	0.787	0.814	1.417	16.2	60.4	Daisy-Chain OFF	0	Secondary
8	0.877	0.924	1.0	1.663	Any value less than 100	OPEN	Daisy-Chain OFF	0	Disabled

8.5 Programming

8.5.1 Serial Control Bus

8.5.1.1 I2C Device Address

The DS90UH984-Q1 implements two I^{2}C-compatible serial control buses. The I^{2}C is for local device configuration and incorporates a Bidirectional Control Channel (BCC) that allows communication across the FPD-Link cable with remote serializers and deserializers as well as remote I^{2}C target devices. The DS90UH984-Q1 implements two I^{2}C compatible targets and up to two I^{2}C controllers (sends I^{2}C commands on both I^{2}C ports) capable of operation with Standard, Fast, and Fast-plus modes of operation. This allows I2C operation at up to 1 MHz clock frequencies. Local bus access is also supported up to High-Speed mode (3.4 MHz).

For accesses to local registers, the I^{2}C targets operate without stretching the clock. Accesses to remote devices over the Bidirectional Control Channel results in clock stretching to allow for response time across the link. The DS90UH984-Q1 can also act as I^{2}C Controller for regenerating Bidirectional Control Channel accesses originating from the remote devices across FPD-Link.

The primary device address and the used I^{2}C voltage level are set via a resistor divider (R1 and R2 — see Figure 8-20) connected to the IDx pin. Each of the two I^{2}C ports has its own target address. By default, the target address of I2C Target 0 is set to the primary I^{2}C address corresponding to the IDx pin. I^{2}C Target 1 is the primary I^{2}C address (7-bit form) plus 0x1. For instance, if the primary I^{2}C address is set to 0x58, I^{2}C Target 1 will have a target address of 0x5A. These addresses may be overwritten using the DEVICE_ID field (0x00[7:1]) and enabling the override by setting DES_ID (0x00[0]) to 1, which both have two copies, one for each I^{2}C target.

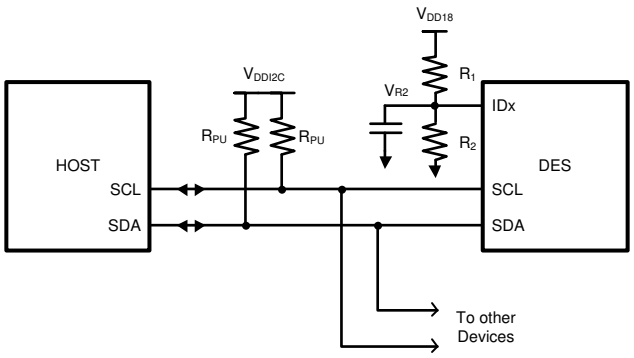

Figure 8-20. Serial Control Bus Connection

The IDx pin configures the control interface to one of 8 possible device addresses. A pull-up resistor and a pull-down resistor may be used to set the appropriate voltage on the IDx input pin See below.

Table 8-39. Serial Control Bus Addresses For IDx

MODE #	RATIO TYPICAL	VR2 (V); VDD = 1.8	I²C Voltage Level (Port 0 and 1)	SUGGESTED RESISTOR PULL-UP R1 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R2 kΩ (1% tol)	7-BIT ADDRESS I²C Target 0	8-BIT ADDRESS I²C Target 0	7-BIT ADDRES S I²C Target 1	8-BIT ADDRESS I²C Target 1
1	0	0	1.8	OPEN	10.0	0x2C	0x58	0x2D	0x5A
2	0.213	0.384	1.8	42.2	11.5	0x30	0x60	0x31	0x62
3	0.327	0.589	1.8	29.4	14.3	0x34	0x68	0x35	0x6A
4	0.441	0.793	1.8	28.7	22.6	0x38	0x70	0x39	0x72
5	0.551	0.999	3.3	15	18.7	0x2C	0x58	0x2D	0x5A
6	0.671	1.208	3.3	13.7	28	0x30	0x60	0x31	0x62
7	0.787	1.417	3.3	16.2	60.4	0x34	0x68	0x35	0x6A
8	1	1.8	3.3	10.0	OPEN	0x38	0x70	0x39	0x72

8.5.1.2 I2C Bus Operation

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V_{DD18} or V_{DD33}, depending on the IDx pin strapping. The pull-up resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled HIGH, or driven LOW. Refer to "*I2C Bus Pullup Resistor Calculation*, SLVA689" to determine the pull-up resistor value for the SCL and SDA rise time.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions LOW while SCL is HIGH. A STOP occurs when SDA transitions HIGH while SCL is also HIGH. See Figure 8-21

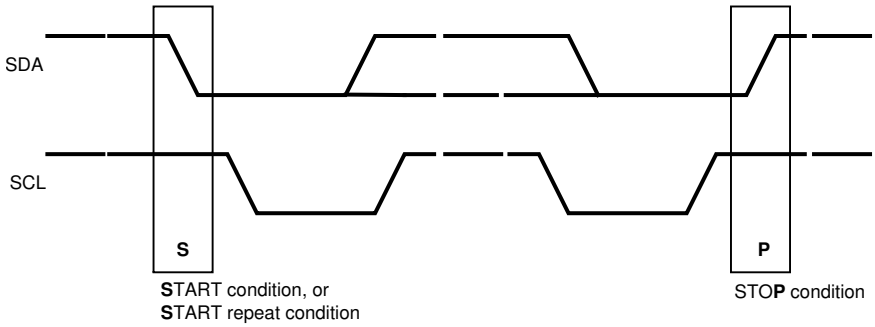

Figure 8-21. Start And Stop Conditions

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To communicate with an I²C target, the host controller (controller) sends the target address and listens for a response from the target. This response is referred to as an acknowledge bit (ACK). If a target on the bus is addressed correctly, it Acknowledges (ACKs) the controller by driving the SDA bus low. If the address doesn't match a device's target address, it Not-acknowledges (NACKs) the controller by letting SDA be pulled HIGH. ACKs also occur on the bus when data is being transmitted. When the controller is writing data, the target ACKs after every data byte is successfully received. When the controller is reading data, the controller ACKs after every data byte is received to let the target know it wants to receive another data byte. When the controller wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 8-22 and a WRITE is shown in Figure 8-23.

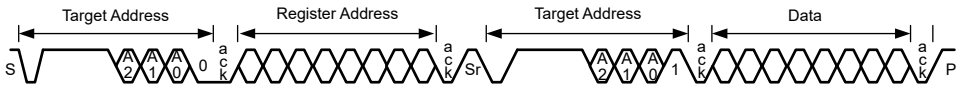

Figure 8-22. Serial Control Bus — Read

Figure 8-23. Serial Control Bus — Write

The I²C Controller located at the serializer must support I²C clock stretching. For more information on I²C interface requirements and throughput considerations, please refer to TI Application Note SNLA131.

8.5.2 Bidirectional Control

The Bidirectional Control Channel (BCC) is compatible with I2C devices, allowing local I2C target access to device registers as well as bidirectional I2C operation across the link to the deserializer and attached devices. I2C access should not be attempted across the link when RX Port Lock status is Low.

8.5.2.1 Local I2C Target Operation

The DS90UH984-Q1 implements two I2C-compatible targets capable of operation compliant to the Standard, Fast, and Fast-plus modes of operation allowing I2C operation at up to 1 MHz clock frequencies. Local I2C transactions to access DS90UH984-Q1 registers can be conducted 2 ms after power supplies are stable and PDB is brought high. For accesses to local registers, the I2C Target operates without stretching the clock (except when multiple I2C targets are being used to access the DS90UH984-Q1 registers simultaneously). Ensure that control registers for indirect access registers (e.g. 0x40-0x42) are not being accessed simultaneously by multiple I2C controllers. In cases where multiple I2C controllers attempt to access the same DS90UH984-Q1 register at the same time, priority is given to I2C Port 0, followed by Port 1, and then I2C commands sent over the FPD-Link channel.

A spurious one-byte I2C read or write transaction with a random address can be observed on the local bus when a downstream deserializer is reset, powered-on/off, hot-plugged, or connected/disconnected. On the serializer or deserializer, remote downstream I2C transactions can be disabled to prohibit the potential I2C transactions from being acknowledged. On the deserializer, set main page register TX_I2C_CONTROLLER_DISABLE (0x08[5]) to disable I2C transactions originating from a downstream controller.

8.5.2.2 Remote Target Operation

The Bidirectional Control Channel provides a mechanism to read or write I2C registers in remote devices over the FPD-Link interface. The I2C Controller located at the partner device must support I2C clock stretching. Accesses to partner devices or remote target devices over the Bidirectional Control Channel will result in clock stretching to allow for response time across the link. The DS90UH984-Q1 acts as an I2C target on the local bus, forwards read and write requests to the remote device, and returns the response from the remote device to the local I2C bus. To allow for the propagation and regeneration of the I2C transaction at the remote device, the DS90UH984-Q1 will stretch the I2C clock while waiting for the remote response.

To communicate with a remote target device, a routing mechanism is used to send BCC commands from a source to destination based on system topology. The serializer or deserializer that is connected to the host controller should control the BCC routing. If the DS90UH984-Q1 is not connected to the host controller, consult the appropriate serializer or deserializer datasheet for details on how to configure bidirectional channel communication routing. If the DS90UH984-Q1 is connected to host controller, registers TARGET_IDx(0x70 - 0x77), TARGET_ALIASx(0x78 - 0x7F), and DESTINATION_FIELDx(0x80 - 0x87) are grouped together to control the direction, routing port, source and destination of bidirectional communication. Each I2C port has its own copy of registers 0x70 - 0x87. Each I2C port can only write to its own copy, but can read the other port's register value by setting PORT_SEL register. A description of these registers are listed in Table 8-40

Table 8-40. Bidirectional Channel Communication Over Daisy-Chain Deserializer Registers

Register Name	Bits	Bits Name	Description
TARGET_IDx	7:1	TARGET_IDx	7-bit Remote Target Device ID x Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias IDx, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
	0	DEST_PKT_RXDIR_ID x	In a Deserializer with daisy-chain support, this bit configures any I2C transaction to either go upstream or downstream. When 1, the transaction is directed to the RX side. This bit is grouped with ID0.
TARGET_ALIASx	7:1	TARGET_ALIAS_IDx	7-bit Remote Target Device Alias ID x Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
	0	LCL_PORTSEL_IDx	In a daisy-chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.
DESTINATION_FIELDx	7:5	DEST_ADDR[2:0]	Destination port selection See Table 8-41
	4	FIRST_DC_PSEL	First daisy-chain port routing selection. Used for daisy-chain lengths of 3 only to select the port taken over the first daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port1
	3	MID_DC_PSEL	Middle daisy-chain port routing selection. Used for a daisy-chain length of 2 to select the port taken over the first daisy-chain link or for a daisy-chains length of 3 to select the port taken over the second daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port1
	2	FINAL_DC_PSEL	Final daisy-chain routing selection. Used for daisy-chain lengths of 1, 2, or 3 to select the port taken over the final daisy-chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port1
	1:0	REMAINING_DEPTH[1 :0]	Remaining depth to the destination 00: 0 remaining depth 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth

TARGET_IDx[0] controls the BCC message routing directions. When this bit is set to 1, BCC messages will be routed to upstream devices. When this bit is set to 0, BCC messages will be routed to downstream devices.

TARGET_ALIASx[0] controls the BCC message routing ports. When this bit is set to 1, BCC messages will be routed through either RX port 1 or daisy-chain TX port 1 depending on TARGET_IDx[0] settings. When this bit is set to 0, BCC messages will be routed through either RX port 0 or daisy-chain TX port 0 depending on TARGET_IDx[0] settings.

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DESTINATION_FIELDx controls the destination port selections (bits 7:5) , first daisy-chain port selection (bit 4), mid daisy-chain port selection (bit 3), final daisy-chain port selection (bit 2), and remaining depth (bits 1:0). Available destination port selections are listed in Table 8-41.

Daisy-chain operation supports a maximum of three daisy-chain devices (four deserializers total).

Table 8-41. Destination Port Selections

DESTINATION_FIELDx[7:5]	DS90Ux983 Serializer	DS90Ux981 Serializer	DS90Ux98x Deserializer
000	I2C Target 0	I2C Target 0	I2C Target 0
001	I2C Target 1	I2C Target 1	I2C Target 1
010	I2C Target 2	Reserved	Reserved
011	Reserved	Reserved	Reserved
100	Reserved	Reserved	Reserved
101	Reserved	Reserved	Reserved
110	Reserved	Reserved	Reserved
111	Internal Registers	Internal Registers	Reserved

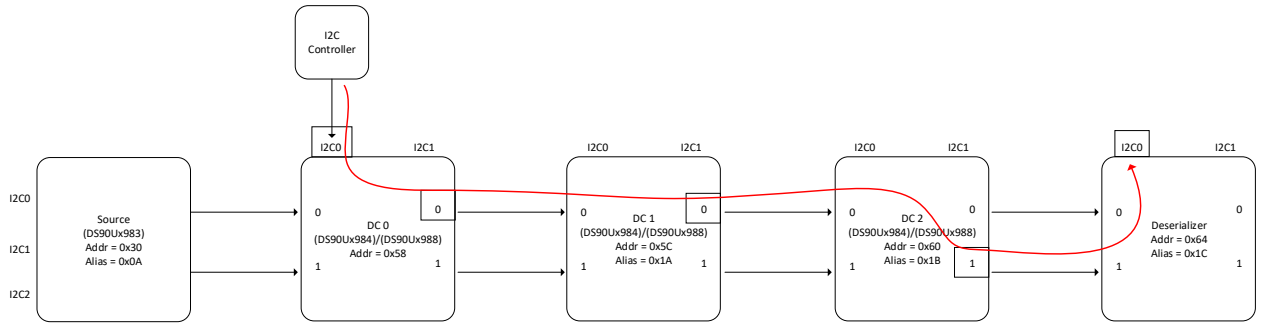

Figure 8-24. Deserializer Configuration BCC Communication Downstream Example #1

Table 8-42. Deserializer Configuration BCC Communication Downstream Example #1

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID_0	0110010	0x64
	0	DEST_PKT_RXDIR_ID0	0	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0001110	0x1C
	0	LCL_PORTSEL_ID0	0	
DESTINATION_FIELD0	7:5	DEST_ADDR[2:0]	000	0xA
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	1	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	10	

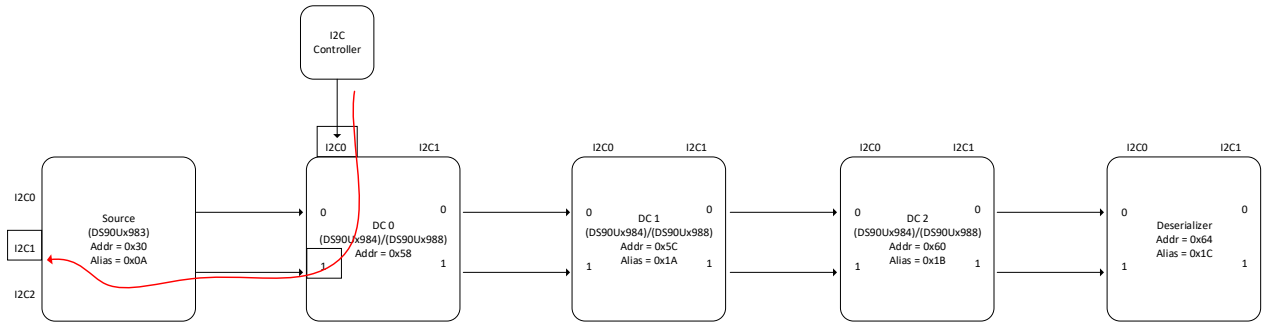

Figure 8-25. Deserializer Configuration BCC Communication Upstream Example #2

Table 8-43. Deserializer Configuration BCC Communication Upstream Example #2

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID_0	7:1	TARGET_ID_0	0011000	0x31
	0	DEST_PKT_RXDIR_ID0	1	
TARGET_ALIAS_0	7:1	TARGET_ALIAS_ID0	0000101	0x0B
	0	LCL_PORTSEL_ID0	1	
DESTINATION_FIELD0	7:5	DEST_ADDR[2:0]	001	0x20
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	0	

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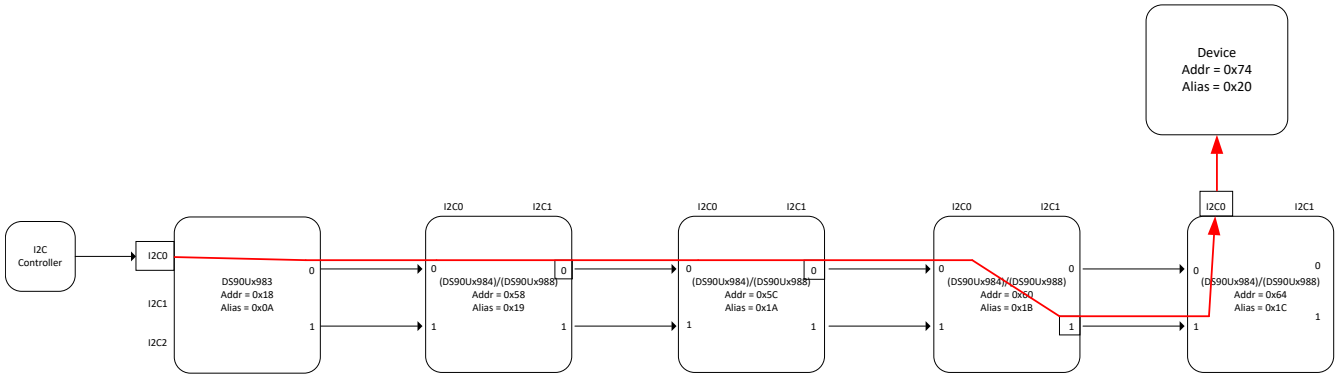

Figure 8-26. Serializer Configuration Daisy-Chain Communication Example #1

Table 8-44. Serializer Configuration Daisy-Chain Communication Example #1

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID0	7:1	TARGET_ID0	0111001	0x74
	0	RESERVED	0	
TARGET_ALIAS0	7:1	TARGET_ALIAS_ID0	0010000	0x20
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST0	7:5	DEST_ADDR[2:0]	000	0x07
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	1	
	1:0	REMAINING_DEPTH[1:0]	11	

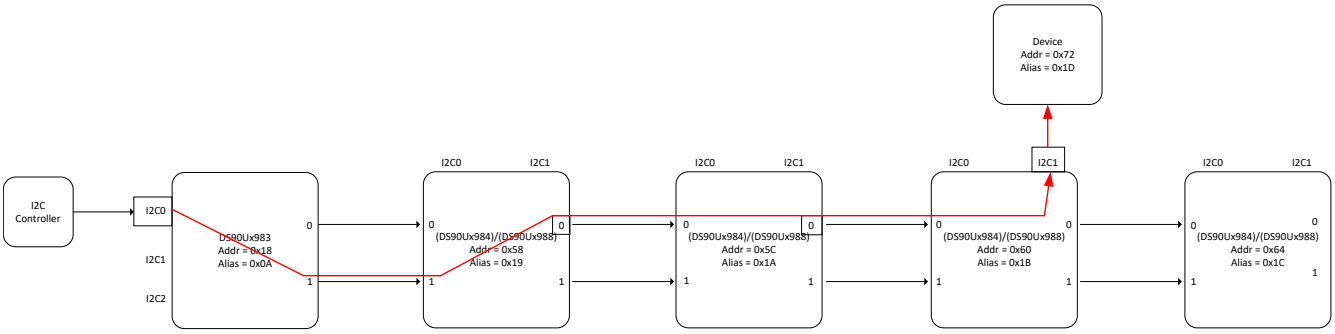

Figure 8-27. Daisy-Chain Communication Example #2

Table 8-45. Serializer Configuration Daisy-Chain Communication Example #2

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID0	7:1	TARGET_ID0	0111 001	0x72
	0	RESERVED	0	
TARGET_ALIAS0	7:1	TARGET_ALIAS_ID0	0001110	0x1D
	0	LCL_PORTSEL_ID0	1	
TARGET_DEST0	7:5	DEST_ADDR[2:0]	001	0x22
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	10	

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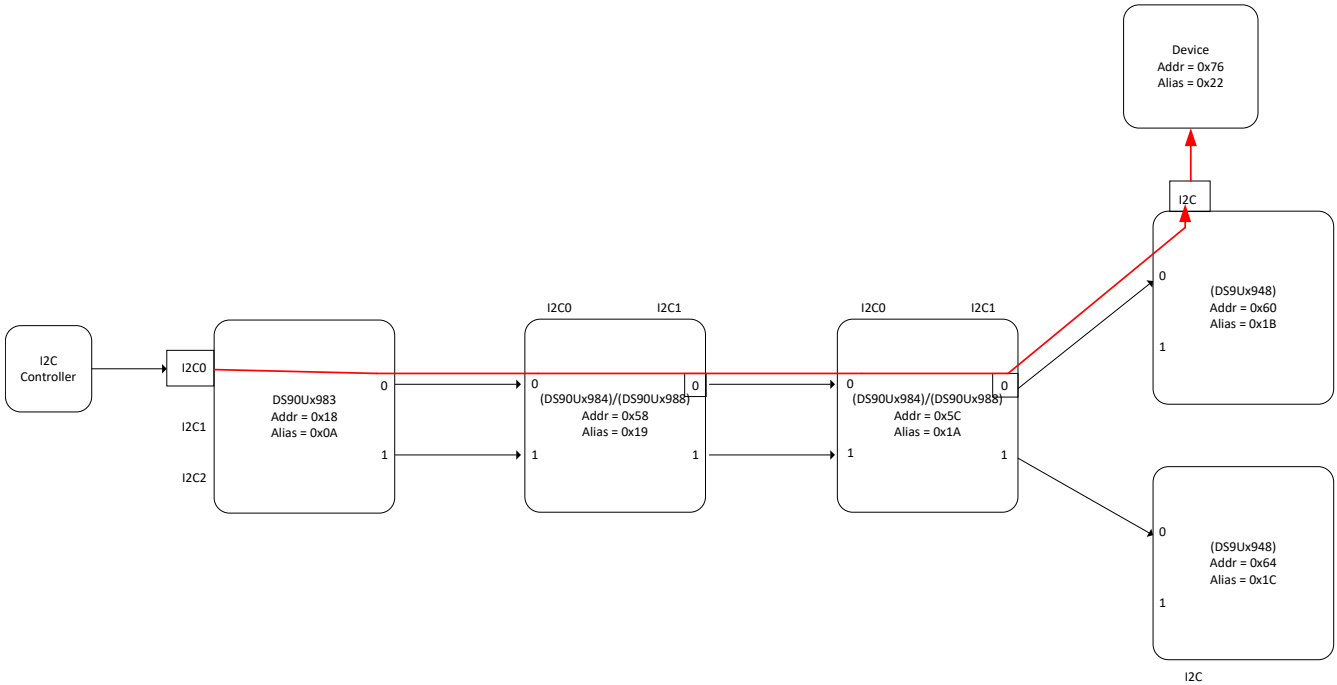

Figure 8-28. Serializer Configuration Daisy-Chain Communication Example #3

Table 8-46. Serializer Configuration Daisy-Chain Communication Example #3

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID0	7:1	TARGET_ID0	0111 011	0x76
	0	RESERVED	0	
TARGET_ALIAS0	7:1	TARGET_ALIAS_ID0	0010001	0x22
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST0	7:5	DEST_ADDR[2:0]	000	0x02
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	0	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	10	

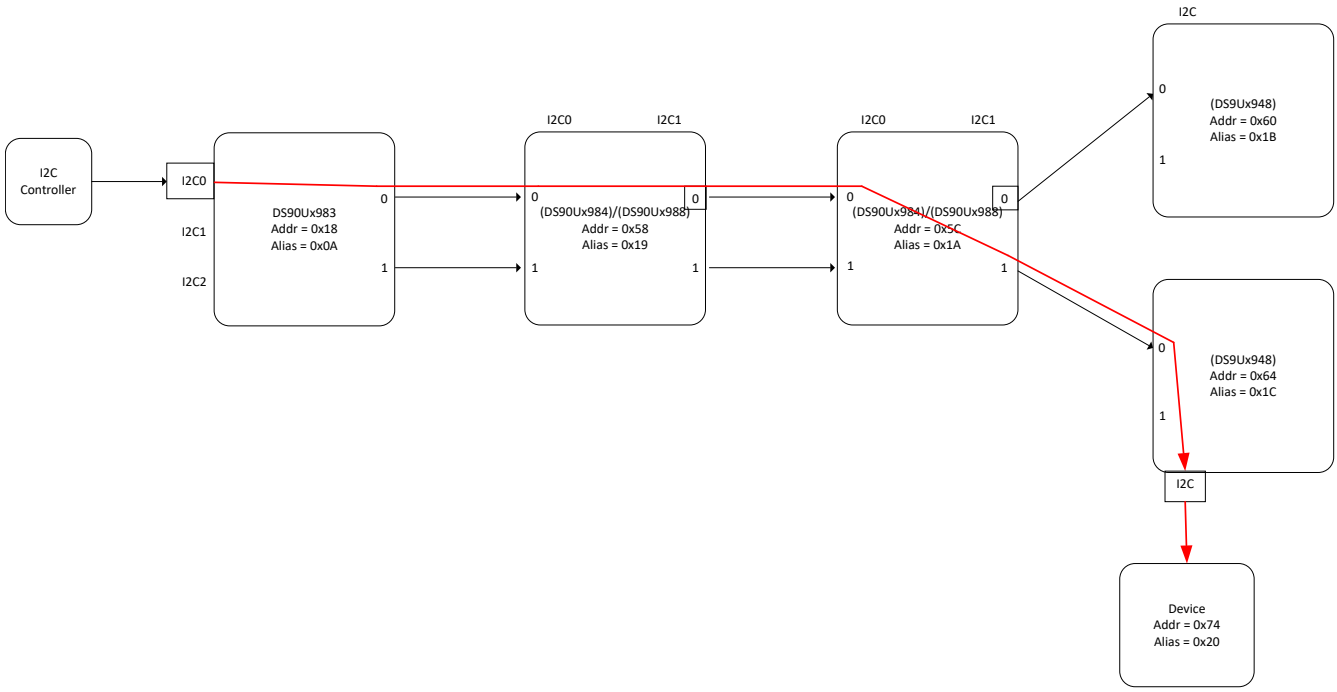

Figure 8-29. Serializer Configuration Daisy-Chain Communication Example #4

Table 8-47. Serializer Configuration Daisy-Chain Communication Example #4

Register Name	Bits	Bits Name	Bit Value	Register Hex Value
TARGET_ID0	7:1	TARGET_ID0	0111 010	0x74
	0	RESERVED	0	
TARGET_ALIAS0	7:1	TARGET_ALIAS_ID0	0010000	0x20
	0	LCL_PORTSEL_ID0	0	
TARGET_DEST0	7:5	DEST_ADDR[2:0]	000	0x0A
	4	FIRST_DC_PSEL	0	
	3	MID_DC_PSEL	1	
	2	FINAL_DC_PSEL	0	
	1:0	REMAINING_DEPTH[1:0]	10	

8.5.2.2.1 Remote Target Addressing

Various system use cases require multiple devices with the same fixed I2C target address to be remotely accessible from the same I2C bus at the serializer or deserializer. The DS90UH984-Q1 provides target ID virtual addressing to differentiate target addresses when connecting two or more remote devices. Eight pairs of TARGET_ALIAS and TARGET_ID registers are allocated for each I2C target in registers 0x70 through 0x7F. The alias registers allow programming virtual addresses which the host controller uses to access remote devices. The TARGET_ID register provides the actual target address for the device on the remote I2C bus. Since eight pairs of registers are available for each I2C target (total of 16 pairs), multiple devices may be directly accessible remotely without the need for reprogramming. Multiple aliases can be assigned to the same TARGET_ID as well.

8.5.2.3 Multi-Controller Arbitration Support

The Bidirectional Control Channel implements I2C compatible bus arbitration in the proxy I2C controller implementation. When sending a data bit, each I2C controller senses the value on the SDA line. If the controller is sending a logic 1 but senses a logic 0, the controller has lost arbitration. It will stop driving SDA, retrying the transaction when the bus becomes idle. Thus, multiple I2C controllers may be implemented in the system.

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If the system does require controller-target operation in both directions across the BCC, some method of communication must be used to ensure only one direction of operation occurs at any time. The communication method could include using available read/write registers in one of the devices to allow controllers to communicate with each other to pass control between the two controllers.

8.5.2.4 I2C Restrictions on Multi-Controller Operation

The I2C specification does not provide for arbitration between controllers under certain conditions. The system should make sure the following conditions cannot occur to prevent undefined conditions on the I2C bus:

- One controller generates a repeated Start while another controller is sending a data bit.
- One controller generates a Stop while another controller is sending a data bit.
- One controller generates a repeated Start while another controller sends a Stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I2C target.

8.5.2.5 Multi-Controller Access to Device Registers

When using the latest generation of FPD-Link devices, main page registers may be accessed simultaneously from both local and remote I2C controllers. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I2C targets is still allowed in only one direction at a time.

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8.6 Register Map

The DS90UH984-Q1 implements the following register blocks, accessible via I2C including over the bidirectional control channel:

- Shared Registers
- FPD-Link RX Port Registers (separate register block for each of the RX ports)
- I2C Port Registers (separate register block for each of the I2C ports)
- FPD-Link daisy-chain TX Port Registers (separate register block for each of the daisy-chain TX ports)

Table 8-48. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP	
0x00	I2C Port Registers	I2C Target 1	I2C Target 2
0x01 - 0x03	Digital Shared Registers	Shared	
0x04	Digital RX Port Registers	FPD RX Port 0 R:0x2D[5:4] =00	FPD RX Port 1 R:0x2D[5:4] =01
0x05	Digital Shared Registers	Shared	
0x06 - 0x0A	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x0B	Digital Shared Registers	Shared	
0x0C - 0x0D	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x0E	Digital Shared Registers	Shared	
0x0F	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x10 - 0x13	Digital Shared Registers	Shared	
0x14	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1
0x15 - 0x26	Digital Shared Registers	Shared	
0x27 - 0x28	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x29 - 0x2C	Digital Shared Registers	Shared	
0x2D	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x2E - 0x3A	Digital Shared Registers	Shared	
0x3B - 0x3F	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x40 - 0x43	Digital Shared Registers	Shared	
0x44	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x45	Digital Shared Registers	Shared	
0x46	Digital DP/eDP Port Registers	FPD DP/eDP Port 0	FPD DP/eDP Port 1
0x47 - 0x50	Digital Shared Registers	Shared	
0x51 - 0x52	Digital Port Registers	Port 0	Port 1
0x53	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x54	Digital Shared Registers	Shared	
0x55 - 0x56	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x57	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x58 - 0x63	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x64-0x67	Digital Shared Registers	Shared	
0x68 - 0x69	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1
0x6A - 0x6B	Digital Shared Registers	Shared	
0x6C - 0x6E	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x6F	Digital Shared Registers	Shared	
0x70 - 0x87	I2C Port Registers	I2C Target 1	I2C Target 2
0x88 - 0x8D	Digital Shared Registers	Shared	
0x8E	Digital Port Registers	Port 0	Port 1
0x8F	Digital Port Registers	Shared	

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Table 8-48. Main Register Map Descriptions (continued)

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP	
0x90 - 0x93	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x94	Digital Shared Registers	Shared	
0x95	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0x96 - 0x9F	Digital Shared Registers	Shared	
0xA0 - 0xA5	Digital TX Port Registers	FPD TX Port 0	FPD TX Port 1
0xA6 - 0xAF	Digital Shared Registers	Shared	
0xB0 - 0xBB	Digital RX Port Registers	FPD RX Port 0	FPD RX Port 1
0xBC - 0xF7	Digital Shared Registers	Shared	
0xF8 - 0xFF	I2C Port Registers	I2C Target 1	I2C Target 2

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8.6.1 MainPage Registers

MAINPAGE Registers lists the memory-mapped registers for the MainPage registers. All register offset addresses not listed in MAINPAGE Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-49. MAINPAGE Registers

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID	I2C_DEVICE_ID	Go
0x1	RESET_CTL	RESET_CTL	Go
0x2	I2C_CONTROLLER_CFG	I2C_CONTROLLER_CFG	Go
0x3	SDA_SETUP	SDA_SETUP	Go
0x4	GENERAL_CFG	GENERAL_CFG	Go
0x5	GENERAL_CFG2	GENERAL_CFG2	Go
0x6	UPSTREAM_ID	UPSTREAM_ID	Go
0x7	DOWNSTREAM_ID	DOWNSTREAM_ID	Go
0x8	TX_BCC_STATUS	TX_BCC_STATUS	Go
0x9	RX_BCC_STATUS	RX_BCC_STATUS_	Go
0xA	TRGT_BCC_STATUS	TRGT_BCC_STATUS	Go
0xB	BCC_CONFIG	BCC_CONFIG	Go
0xC	FPD4_RX_DATAPATH_CTL	FPD4_RX_DATAPATH_CTL	Go
0xE	PORT_SEL	PORT_SEL	Go
0xF	FORCE_BACK_CHANNEL_ERROR	FORCE_BACK_CHANNEL_ERROR	Go
0x10	GPI_PIN_STS1	GPI_PIN_STS1	Go
0x11	GPI_PIN_STS2	GPI_PIN_STS2	Go
0x12	GPIO_IN_EN1	GPIO_IN_EN1	Go
0x13	GPIO_IN_EN0	GPIO_IN_EN0	Go
0x14	TX_BIST_CTL_FPD3	TX_BIST_CTL_FPD3	Go
0x15	GPIO0_PIN_CTL	GPIO0_PIN_CTL	Go
0x16	GPIO1_PIN_CTL	GPIO1_PIN_CTL	Go
0x17	GPIO2_PIN_CTL	GPIO2_PIN_CTL	Go
0x18	GPIO3_PIN_CTL	GPIO3_PIN_CTL	Go
0x19	GPIO4_PIN_CTL	GPIO4_PIN_CTL	Go
0x1A	GPIO5_PIN_CTL	GPIO5_PIN_CTL	Go
0x1B	GPIO6_PIN_CTL	GPIO6_PIN_CTL	Go
0x1C	GPIO7_PIN_CTL	GPIO7_PIN_CTL	Go
0x1D	GPIO8_PIN_CTL	GPIO8_PIN_CTL	Go
0x1E	GPIO9_PIN_CTL	GPIO9_PIN_CTL	Go
0x1F	GPIO10_PIN_CTL	GPIO10_PIN_CTL	Go
0x20	GPIO11_PIN_CTL	GPIO11_PIN_CTL	Go
0x21	GPIO12_PIN_CTL	GPIO12_PIN_CTL	Go
0x22	GPIO13_PIN_CTL	GPIO13_PIN_CTL	Go
0x24	MODE_STS	MODE_STS	Go
0x27	FPD3_RX_DATAPATH_CTL	FPD3_RX_DATAPATH_CTL	Go
0x28	FPD3_RX_DATAPATH_CTL2	FPD3_RX_DATAPATH_CTL2	Go
0x29	BCC_WDOG_CTL	BCC_WDOG_CTL	Go
0x2A	I2C_CONTROL	I2C_CONTROL	Go
0x2B	SCL_HIGH_TIME	SCL_HIGH_TIME	Go

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Table 8-49. MAINPAGE Registers (continued)

Address	Acronym	Register Name	Section
0x2C	SCL_LOW_TIME	SCL_LOW_TIME	Go
0x2D	BIST_CONTROL	BIST_CONTROL	Go
0x2E	FPD_RX_CTL	FPD_RX_CTL	Go
0x2F	IO_CTL	IO_CTL	Go
0x30	MASK_ID_REV	MASK_ID_REV	Go
0x31	FPD4_RX_CFG	FPD4_RX_CFG	Go
0x32	FPD3_RX_CTL	FPD3_RX_CTL	Go
0x33	FPD_RX_DIVIDER_SEL	FPD_RX_DIVIDER_SEL	Go
0x34	LINK_ERROR_COUNT	LINK_ERROR_COUNT	Go
0x36	FPD_RX_BIST_ACTIVE	FPD_RX_BIST_ACTIVE	Go
0x38	I2C_CTRL_CHAIN_CTL1	I2C_CTRL_CHAIN_CTL1	Go
0x3B	FPD4_ERR_FLAGS	FPD4_ERR_FLAGS	Go
0x40	IND_ACC_CTL	IND_ACC_CTL	Go
0x41	IND_ACC_ADDR	IND_ACC_ADDR	Go
0x42	IND_ACC_DATA	IND_ACC_DATA	Go
0x43	RX_INT_STS	RX_INT_STS	Go
0x44	RX_INT_CTL	RX_INT_CTL	Go
0x45	LOCAL_INT_STS	LOCAL_INT_STS	Go
0x47	RX_MODE_STS2	RX_MODE_STS2	Go
0x48	APB_CTL	APB_CTL	Go
0x49	APB_ADR0	APB_ADR0	Go
0x4A	APB_ADR1	APB_ADR1	Go
0x4B	APB_DATA0	APB_DATA0	Go
0x4C	APB_DATA1	APB_DATA1	Go
0x4D	APB_DATA2	APB_DATA2	Go
0x4E	APB_DATA3	APB_DATA3	Go
0x50	BRIDGE_STS	BRIDGE_STS	Go
0x51	INTERRUPT_STS	INTERRUPT_STS	Go
0x52	INTERRUPT_CTL	INTERRUPT_CTL	Go
0x53	GENERAL_PURPOSE_STATUS_0	GENERAL_PURPOSE_STATUS_0	Go
0x54	GENERAL_PURPOSE_STATUS_1	GENERAL_PURPOSE_STATUS_1	Go
0x68	FC_POWERDOWN_CTL	FC_POWERDOWN_CTL	Go
0x6C	CRC_ERROR0_BC	CRC_ERROR0_BC	Go
0x6D	CRC_ERROR1_BC	CRC_ERROR1_BC	Go
0x6E	BIST_BC_ERRORS	BIST_BC_ERRORS	Go
0x6F	RX_BCC_TEST	RX_BCC_TEST	Go
0x70	TARGET_ID0	TARGET_ID0	Go
0x71	TARGET_ID1	TARGET_ID1	Go
0x72	TARGET_ID2	TARGET_ID2	Go
0x73	TARGET_ID3	TARGET_ID3	Go
0x74	TARGET_ID4	TARGET_ID4	Go
0x75	TARGET_ID5	TARGET_ID5	Go
0x76	TARGET_ID6	TARGET_ID6	Go
0x77	TARGET_ID7	TARGET_ID7	Go

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Table 8-49. MAINPAGE Registers (continued)

Address	Acronym	Register Name	Section
0x78	TARGET_ALIAS0	TARGET_ALIAS0	Go
0x79	TARGET_ALIAS1	TARGET_ALIAS1	Go
0x7A	TARGET_ALIAS2	TARGET_ALIAS2	Go
0x7B	TARGET_ALIAS3	TARGET_ALIAS3	Go
0x7C	TARGET_ALIAS4	TARGET_ALIAS4	Go
0x7D	TARGET_ALIAS5	TARGET_ALIAS5	Go
0x7E	TARGET_ALIAS6	TARGET_ALIAS6	Go
0x7F	TARGET_ALIAS7	TARGET_ALIAS7	Go
0x80	DESTINATION_FIELD0	DESTINATION_FIELD0	Go
0x81	DESTINATION_FIELD1	DESTINATION_FIELD1	Go
0x82	DESTINATION_FIELD2	DESTINATION_FIELD2	Go
0x83	DESTINATION_FIELD3	DESTINATION_FIELD3	Go
0x84	DESTINATION_FIELD4	DESTINATION_FIELD4	Go
0x85	DESTINATION_FIELD5	DESTINATION_FIELD5	Go
0x86	DESTINATION_FIELD6	DESTINATION_FIELD6	Go
0x87	DESTINATION_FIELD7	DESTINATION_FIELD7	Go
0x90	BC_PROCESSING_CFG	BC_PROCESSING_CFG	Go
0x91	DATAPATH_BC	DATAPATH_BC	Go
0x93	FC_BCC_TEST	FC_BCC_TEST	Go
0x94	LINK_DET_TIMER	LINK_DET_TIMER	Go
0x9B	FPD_RX_BC_TX_NCOUNTER_SEL_LSB	FPD_RX_BC_TX_NCOUNTER_SEL_LSB	Go
0xA0	FPD3_TX_DES_CAP1	FPD3_TX_DES_CAP1	Go
0xA1	FPD3_TX_DES_CAP2	FPD3_TX_DES_CAP2	Go
0xA2	FPD4_TX_REMOTE_PAR_CAP1	FPD4_TX_REMOTE_PAR_CAP1	Go
0xA3	FPD4_TX_REMOTE_PAR_CAP2	FPD4_TX_REMOTE_PAR_CAP2	Go
0xA4	FPD4_TX_DATAPATH_CTL	FPD4_TX_DATAPATH_CTL	Go
0xA5	FPD4_TX_DATAPATH_CTL2	FPD4_TX_DATAPATH_CTL2	Go
0xA8	FPD_TX_CFG	FPD_TX_CFG	Go
0xA9	FPD_TX_INVERT	FPD_TX_INVERT	Go
0xAB	PLL_REFCLK_STATUS	PLL_REFCLK_STATUS	Go
0xAC	PLL_REFCLK_FREQ_TXP0	PLL_REFCLK_FREQ_TXP0	Go
0xAD	PLL_REFCLK_FREQ_TXP1	PLL_REFCLK_FREQ_TXP1	Go
0xAE	PLL_REFCLK_FREQ_RXP	PLL_REFCLK_FREQ_RXP	Go
0xAF	XO_REFCLK_FREQ	XO_REFCLK_FREQ	Go
0xB1	DISP_QUAD_PIXEL_CLK_DIV_EN	DISP_QUAD_PIXEL_CLK_DIV_EN	Go
0xB2	DISP_QUAD_PIXEL_CLK_MVAL0	DISP_QUAD_PIXEL_CLK_MVAL0	Go
0xB3	DISP_QUAD_PIXEL_CLK_MVAL1	DISP_QUAD_PIXEL_CLK_MVAL1	Go
0xB4	DISP_QUAD_PIXEL_CLK_MVAL2	DISP_QUAD_PIXEL_CLK_MVAL2	Go
0xB5	DISP_QUAD_PIXEL_CLK_NVAL0	DISP_QUAD_PIXEL_CLK_NVAL0	Go
0xB6	DISP_QUAD_PIXEL_CLK_NVAL1	DISP_QUAD_PIXEL_CLK_NVAL1	Go

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Table 8-49. MAINPAGE Registers (continued)

Address	Acronym	Register Name	Section
0xB7	DISP_QUAD_PIXEL_CLK_NVAL 2	DISP_QUAD_PIXEL_CLK_NVAL2	Go
0xB8	FPD4_BIST_ERROR_COUNT	FPD4_BIST_ERROR_COUNT	Go
0xCE	SAR_ADC_ICR_ISR	SAR_ADC_ICR_ISR	Go
0xD0	FF_LINK_EN	FF_LINK_EN	Go
0xD1	DC_LINK_EN	DC_LINK_EN	Go
0xD2	DC_LINK_MAP0_MAP1	DC_LINK_MAP0_MAP1	Go
0xD3	DC_LINK_MAP2_MAP3	DC_LINK_MAP2_MAP3	Go
0xD4	DC_LINK_MAP4_MAP5	DC_LINK_MAP4_MAP5	Go
0xD5	FPD4_FPD3_MAP0_MAP1	FPD4_FPD3_MAP0_MAP1	Go
0xD6	FPD4_DISP_MAP0_MAP1	FPD4_DISP_MAP0_MAP1	Go
0xD7	SEL_FPD3_DISP	SEL_FPD3_DISP	Go
0xF0	FPD_ID0	FPD_ID0	Go
0xF1	FPD_ID1	FPD_ID1	Go
0xF2	FPD_ID2	FPD_ID2	Go
0xF3	FPD_ID3	FPD_ID3	Go
0xF4	FPD_ID4	FPD_ID4	Go
0xF5	FPD_ID5	FPD_ID5	Go
0xF6	FPD_ID6	FPD_ID6	Go

Complex bit access types are encoded to fit into small table cells. MainPage Access Type Codes shows the codes that are used for access types in this section.

Table 8-50. MainPage Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 I2C_DEVICE_ID Register (Address = 0x0) [Default = X]

I2C_DEVICE_ID is shown in I2C_DEVICE_ID Register Field Descriptions.

Return to the Summary Table.

Table 8-51. I2C_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	DEVICE_ID	R/W	X	7-bit address of Deserializer Address is configured by the IDx strap pin. The IDX strap pin value represents the device I2C address. When reading via I2C Block 0 (I2C_SCL0 and I2C_SDA0), the returned value will be the I2C Block 0 address. When reading via I2C Block 1 (I2C_SCL1 and I2C_SDA1), the returned value will be the I2C Block 1 address. In Dual Mode when reading this register over the FPD-Link, the I2C Block 0 address will be returned. In non-Dual Mode when reading this register over the FPD-Link, the I2C Block 1 address will always read as +1 the I2C Block 0 address (I2CAddr1= I2CAddr0 + 1). When programming this value, the least significant bit of DEVICE_ID must be set to 0 to allow proper configuration of the I2C Block 1 I2C address, as mentioned. Also, this value cannot be changed unless Bit[0]= 1. DEVICE_ID for I2C Block 1 is a READ ONLY register.
0	DES_ID	R/W	0x0	0: IDX strap populates the DEVICE_ID address field 1: DEVICE_ID register field can be overwritten

8.6.1.2 RESET_CTL Register (Address = 0x1) [Default = 0x00]

RESET_CTL is shown in RESET_CTL Register Field Descriptions.

Return to the Summary Table.

Table 8-52. RESET_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	PLL_RX_RESET	RH/W1S	0x0	RX PLL Reset
6	PLL_DPTX_RESET	RH/W1S	0x0	DPTX PLL Reset
5	TX_PLL0_RESET	RH/W1S	0x0	PLL for daisy-chain Port0 only reset
4	TX_PLL1_RESET	RH/W1S	0x0	PLL for daisy-chain Port1 only reset
3	RESERVED	RH/W1S	0x0	Reserved
2	RESERVED	RH/W1S	0x0	Reserved
1	DIGITAL_RESET_ALL	RH/W1S	0x0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
0	DIGITAL_RESET_NOREGS	RH/W1S	0x0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

8.6.1.3 I2C_CONTROLLER_CFG Register (Address = 0x2) [Default = 0x60]

I2C_CONTROLLER_CFG is shown in I2C_CONTROLLER_CFG Register Field Descriptions.

Return to the Summary Table.

Table 8-53. I2C_CONTROLLER_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	ARB_TIMEOUT_DIS	R/W	0x0	Disables the arbiter timeout for I2C. 1: ARB timeout disabled 0: ARB timeout enabled

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Table 8-53. I2C_CONTROLLER_CFG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:5	ARB_TIMEOUT	R/W	0x3	Length of arbiter timeout for I2C. 2'b00= 80 us 2'b01= 160 us 2'b10= 2.4 ms 2'b11= 10 ms
4:3	SDA_OUT_DELAY	R/W	0x0	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 200ns 01: 240ns 10: 280ns 11: 320ns Actual delays may be larger dependent on system capacitances and signal rise/fall times.
2	LOCAL_WRITE_DIS	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C Controller attached to the Deserializer. Setting this bit does not affect remote access to I2C Targets at the Serializer.
1	I2C_BUS_TIMER_SPEED UP	R/W	0x0	Speed up I2C Block Watchdog Timer The watchdog timer is for the local external I2C access, I2C_SDA0/1 and I2C_SCL0/1 pins. 1: Watchdog Timer expires after approximately 50 usec 0: Watchdog Timer expires after approximately 1 sec
0	I2C_BUS_TIMER_DISAB LE	R/W	0x0	Disable I2C Bus Watchdog Timer The watchdog timer is for the local external I2C access, I2C_SDA and I2C_SCL pins. The watchdog timer is used to determine if the bus is either free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs in the timer duration set by Bit 1, the bus can be confirmed free if a remote transaction completes successfully. If the SDA is low and no signaling occurs in the timer duration set by Bit 1, the bus will be cleared after a request for the bus is made by a remote I2C transaction and after 9 clocks are driven by the controller. 0: I2C Bus Watchdog Timer enabled 1: Disable I2C Bus Watchdog Timer

8.6.1.4 SDA_SETUP Register (Address = 0x3) [Default = 0x01]

SDA_SETUP is shown in SDA_SETUP Register Field Descriptions.

Return to the Summary Table.

Table 8-54. SDA_SETUP Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

Table 8-54. SDA_SETUP Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	TX_SDA_SETUP	R/W	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. The setup time can be calculated using the following equation: Setup time= 5 ns * ((TX_SDA_SETUP[3:0] * 16) + (2 + SDA_OUT_DELAY[4:3])) SDA_OUT_DELAY is found in register 0x2. Please note that this equation expects the binary value, not the listed delay value. Example (default config): TX_SDA_SETUP= 0b0001 and SDA_OUT_DELAY= 0b00 Setup time= 5 ns * ((1 * 16) + (2 + 0)) Setup time= 5 ns * 18= 90 ns

8.6.1.5 GENERAL_CFG Register (Address = 0x4) [Default = 0xC1]

GENERAL_CFG is shown in GENERAL_CFG Register Field Descriptions.

Return to the Summary Table.

Table 8-55. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	BC_CRC_GEN_EN_TX	R/W	0x1	Back Channel CRC Generator Enable - TX This bit enables the BC CRC generator on the daisy-chain link. 0: Disable 1: Enable
6	BC_CRC_GEN_EN_RX	R/W	0x1	Back Channel CRC Generator Enable - RX This bit enables the BC CRC generator on the main link. 0: Disable 1: Enable
5	AUTO_ACK	R/W	0x0	Automatically Acknowledge I2C writes independent of the forward channel lock state 0: Disable 1: Enable
4	I2C_PASS_THROUGH_ALL	R/W	0x0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
3	I2C_PASS-THROUGH	R/W	0x0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
2	I2C_PASS_ALL_BC	R/W	0x0	I2C Pass-Through Mode - Repeater functionality. Allows I2C transactions travelling from another linked upstream deserializer or serializer. 0: Back Channel Pass-Through Disabled 1: Back Channel Pass-Through Enabled - Valid only if I2C_PASS_ALL is not enabled. Each I2C Target maintains it's own copy of this register bit. This bit cannot be accessed remotely using the Bidirectional Control Channel.
1	FC_BCC_CRC_TX_EN	R/W	0x0	Enable enhanced CRC and start sequence for daisy chain forward channel
0	FC_BCC_CRC_RX_EN	R/W	0x1	Enable enhanced CRC and start sequence for main link receiver

8.6.1.6 GENERAL_CFG2 Register (Address = 0x5) [Default = X]

GENERAL_CFG2 is shown in GENERAL_CFG2 Register Field Descriptions.

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Table 8-56. GENERAL_CFG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HALFRATE_MODE_CH1	R/W	X	FPD Half/Full rate mode for Daisy Chain Channel 1 If the device is strapped for FPD4 mode at 3.375 Gbps (MODE_SEL0= Mode #6 AND MODE_SEL2= Modes #3 -> #0), then this bit will automatically be strapped to 0. 0: Full-rate. Internal frequency is matched to the rate of the FPD channel speed 1: Half-rate. Internal frequency is half the rate of the FPD channel speed
6	HALFRATE_MODE_CH0	R/W	X	FPD Half/Full rate mode for Daisy Chain Channel 0 If the device is strapped for FPD4 mode at 3.375 Gbps (MODE_SEL0= Mode #6 AND MODE_SEL2= Modes #3 -> #0), then this bit will automatically be strapped to 0. 0: Full-rate. Internal frequency is matched to the rate of the FPD channel speed 1: Half-rate. Internal frequency is half the rate of the FPD channel speed
5	CRC_ERROR_RESET	R/W	0x0	Clear CRC Error Counters. This bit is NOT self-clearing. 1: Clear Counters 0: Normal Operation
4	RESERVED	R/W	0x0	Reserved
3:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.1.7 UPSTREAM_ID Register (Address = 0x6) [Default = 0x00]

UPSTREAM_ID is shown in UPSTREAM_ID Register Field Descriptions.

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Table 8-57. UPSTREAM_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	REMOTE_ID_UPSTREAM	R/W	0x0	7-bit Main Link Upstream Partner Device ID Configures the I2C Target ID of the remote serializer or upstream deserializer (daisy-chain topology). A value of 0 in this field disables I2C access to the remote serializer or upstream deserializer. This field is automatically loaded from the main link partner device once RX Lock has been detected. Software may overwrite this value, but FREEZE_UPSTREAM_ID should be set to prevent an additional value being loaded by the Bidirectional Control Channel. If connected to a 98x device in dual mode, the Port1 field will default to +1 the Port0 value. If PORT1_SEL is set, this register indicates the main link partner device ID for the I2C block connected to Port1.
0	FREEZE_UPSTREAM_ID	R/W	0x0	Freeze Main Link Upstream Partner Device ID Prevent auto-loading of the Main Link Upstream Partner Device ID from the Forward Channel. The ID will be frozen at the value written. 0: REMOTE_ID_UPSTREAM value unfrozen 1: REMOTE_ID_UPSTREAM value frozen, FPD-Link channel cannot change ID value, but the register value can be written via I2C

8.6.1.8 DOWNSTREAM_ID Register (Address = 0x7) [Default = 0x00]

DOWNSTREAM_ID is shown in DOWNSTREAM_ID Register Field Descriptions.

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Table 8-58. DOWNSTREAM_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	REMOTE_ID_DOWNSTREAM	R/W	0x0	7-bit Downstream Deserializer Device ID Configures the I2C Target ID of the remote Deserializer (downstream in a daisy-chain configuration). A value of 0 in this field disables I2C access to the remote deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but FREEZE_DOWNSTREAM_ID should be set to prevent loading by the Bidirectional Control Channel. If PORT1_SEL is set, this register returns the deserializer device ID for the deserializer attached to Port1
0	FREEZE_DOWNSTREAM_ID	R/W	0x0	Freeze Downstream Deserializer Device ID Prevent auto-loading of the Downstream Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written. 0: REMOTE_ID_DOWNSTREAM value unfrozen 1: REMOTE_ID_DOWNSTREAM value frozen, BCC cannot change ID value, but the register value can be written via I2C

8.6.1.9 TX_BCC_STATUS Register (Address = 0x8) [Default = 0x00]

TX_BCC_STATUS is shown in TX_BCC_STATUS Register Field Descriptions.

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Daisy-chain BCC Status Register

Table 8-59. TX_BCC_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7	IE_TX_BCC_STS	R/W	0x0	Interrupt Enable (IE) for TX BCC Status 0: Clear-on-read status interrupts in this register are disabled. 1: Clear-on-read status interrupts will be enabled in this register. Interrupts will propagate to LOCAL_INT_STS register (address 0x45).
6	RESERVED	R	0x0	Reserved
5	TX_I2C_CONTROLLER_DISABLE	R/W	0x0	This bit will disable the remote reads and writes from the daisy-chained I2C Controller. Local I2C Controller writes and reads to the local registers will still work, as well as I2C Controller writes and reads from the upstream device. 0: I2C Controller remote read/write is enabled 1: I2C Controller remote read/writes is disabled
4	TX_CONTROLLER_DATA_ERROR	RC	0x0	I2C Controller Data Error on Daisy Chain Link (TX) This flag is set if there is no stop strobe at the end of an I2C transaction, or if there is no read data at the end of an I2C transaction. The I2C Controller is on the downstream deserializer for this error flag. This flag is cleared on read of this register.
3	TX_FRAME_SEQ_ERR	RC	0x0	FPD3 BCC Frame Sequence Error on Daisy Chain Link (TX) This flag is set if the sequence number in the BCC frame is incorrect. This flag is cleared on read of this register.
2	RESERVED	R	0x0	Reserved
1	BCC_CONTROLLER_ERR	RC	0x0	BCC Controller Error This flag indicates a back channel CRC error or loss of back channel lock has occurred while waiting for a response from the daisy-chained deserializer or other downstream I2C Targets while the BCC (Bidirectional Control Channel) I2C Controller is active. This flag is cleared on read of this register.

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Table 8-59. TX_BCC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	BCC_CONTROLLER_TO	RC	0x0	BCC Target Timeout Error This bit will be set if the BCC (Bidirectional Control Channel) Watchdog Timer expires will waiting for a response from the daisy-chained deserializer while the BCC (Bidirectional Control Channel) I2C Controller is active. This flag is cleared on read of this register.

8.6.1.10 RX_BCC_STATUS Register (Address = 0x9) [Default = 0x00]

RX_BCC_STATUS is shown in RX_BCC_STATUS Register Field Descriptions.

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Table 8-60. RX_BCC_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7	IE_RX_BCC_STS	R/W	0x0	Interrupt Enable (IE) for RX_BCC_STATUS 0: Clear-on-read status interrupts in this register are disabled. 1: Clear-on-read status interrupts will be enabled in this register. Interrupts will propagate to LOCAL_INT_STS register (address 0x45).
6	RXFC_CRC_ERR	RC	0x0	This is a CRC flag, when FC channel data packet is received and has a CRC error, this flag gets set. This bit is cleared on read of register.
5	RX_I2C_CONTROLLER_DISABLE	R/W	0x0	Remote I2C Controller Disable Setting this bit will prevent any I2C transactions originating from an upstream device. Local I2C access to the deserializer is still allowed. Additionally, I2C transactions to remote devices that originate from the local I2C bus are also allowed. This bit cannot be set by an upstream device. 0: I2C Controller remote read/write is enabled 1: I2C Controller remote read/writes is disabled
4	CONTROLLER_DATA_ERROR	RC	0x0	I2C Controller Data Error This bit is set if the response from the serializer or upstream deserializer has the incorrect value for the read data during the stop strobe. This bit is cleared on read of register.
3	FW_CH_SEQ_ERR	RC	0x0	Forward Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read of register.
2	RESERVED	R	0x0	Reserved
1	RX_BCC_CONTROLLER_ERR	RC	0x0	BCC Controller Error This flag indicates a Forward Channel BCC (Bidirectional Control Channel) Sequence, BCC CRC, or lock error occurred while waiting for a response from the serializer or upstream deserializer while the BCC I2C Controller is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR in register 0xB is set to 1.
0	RX_BCC_CONTROLLER_TO	RC	0x0	BCC Target Timeout Error This bit will be set if the BCC (Bidirectional Control Channel) Watchdog Timer expires will waiting for a response from the main link device (upstream device) while the BCC I2C Controller is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR in register 0xB is set to 1.

8.6.1.11 TRGT_BCC_STATUS Register (Address = 0xA) [Default = 0x00]

TRGT_BCC_STATUS is shown in TRGT_BCC_STATUS Register Field Descriptions.

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Table 8-61. TRGT_BCC_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7	IE_TRGT_BCC_STS	R/W	0x0	Interrupt Enable on Target BCC Status 0: Clear-on-read status interrupts in this register are disabled. 1: Clear-on-read status interrupts will be enabled in this register. Interrupts will propagate to LOCAL_INT_STS register (address 0x45).
6:3	RESERVED	R	0x0	Reserved
2	BCC_TRGT_ERR	RC	0x0	BCC Target Error Back channel error (loss of lock or CRC) while Target is waiting for response from a downstream deserializer. This flag indicates a back channel CRC error or loss of back channel lock occurred while waiting for a response from the deserializer while the BCC I2C Target is active. This flag is cleared on read of this register.
1	BCC_TARGET_TO	RC	0x0	BCC Target Timeout Error Time out error when waiting for remote response from either an upstream or downstream remote Target device. This bit will be set if the BCC Watchdog Timer expires will waiting for a response from the deserializer while the BCC I2C Target is active. This flag is cleared on read of this register.
0	TARGET_DATA_ERROR	RC	0x0	This bit is set upon a Target data error when a received BCC packet has a CRC error or loses lock. This flag applies when the local device is acting as the I2C Controller. This flag is cleared on read of this register.

8.6.1.12 BCC_CONFIG Register (Address = 0xB) [Default = 0x02]

BCC_CONFIG is shown in BCC_CONFIG Register Field Descriptions.

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Table 8-62. BCC_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	TX_BCC_EN_DATA_CHK	R/W	0x0	Enable checking of returned data Enhanced Error checking can check for errors on returned data during an acknowledge cycle for data sent to remote devices over the Bidirectional Control Channel. In addition, If an error is detected, this register control will allow changing a remote Ack to a Nack to indicate the data error on the local I2C interface. This bit should not be set when operating with Deserializers that do not support Enhanced Error checking as they will not always return the correct data during an Ack. Please check the respective datasheet to verify if the deserializer supports enhanced error checking. 0: Disable returned data error detection 1: Enable returned data error detection
5	TX_BCC_ACK_REMOTE_READ	R/W	0x0	Enable Control Channel to acknowledge start of remote read. When operating with a link partner that supports Enhanced Error Checking for the Bidirectional Control Channel, setting this bit allows the Serializer to generate an internal acknowledge to the beginning of a remote I2C Target read. This allows additional error detection at the Deserializer. This bit should not be set when operating with Deserializers that do not support Enhanced Error Checking. Please check the respective datasheet to verify if the deserializer supports enhanced error checking. 0: Disable 1: Enable

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Table 8-62. BCC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	TX_BCC_EN_ENH_ERROR	R/W	0x0	Enable Enhanced Error checking in Bidirectional Control Channel This bit enables enhanced error checking on the Bidirectional Control Channel. The enhanced error checking can detect certain error conditions and terminate transactions if an error is detected. 0: Disable enhanced error checking 1: Enable enhanced error checking
3	TX_BCC_TERM_ON_ERR	R/W	0x0	Terminate Control Channel transactions on CRC Error detection During control channel operations, if a CRC Error occurs, it is unlikely to affect control channel operation. Setting this bit will allow more conservative operation that terminates any active Control Channel operation if an error is detected in the back channel. 0: Don't terminate BCC transactions on CRC Errors 1: Terminate BCC transactions on CRC Errors This bit will have no effect if Enhanced Error checking is disabled (BCC_EN_ENH_ERROR in register 0xB set to 0).
2	RX_BCC_ACK_REMOTE_READ	R/W	0x0	Enable Control Channel to acknowledge start of remote read. When operating with a link partner that supports Enhanced Error Checking for the Bidirectional Control Channel, setting this bit allows the Deserializer to generate an internal acknowledge to the beginning of a remote I2C Target read. This allows additional error detection at the Serializer. This bit should not be set when operating with Serializers that do not support Enhanced Error Checking. 0: Disable 1: Enable
1	RX_BCC_EN_ENH_ERROR	R/W	0x1	Enable Enhanced Error checking in BidirectionalControl Channel The Bidirectional Control Channel can detect certain error conditions and terminate transactions if an error is detected. This capability can be disabled by setting this bit to 0. 0: Disable Enhanced Error checking 1: Enable Enhanced Error checking
0	RX_BCC_TERM_ON_ERROR	R/W	0x0	Terminate Control Channel transactions on CRC Error detection During control channel operations, if a CRC Error occurs, it is unlikely to affect control channel operation. Setting this bit will allow more conservative operation that terminates any active Control Channel operation if an error is detected in the back channel. 0: Don't terminate BCC transactions on CRC Errors 1: Terminate BCC transactions on CRC Errors This bit will have no effect if Enhanced Error checking is disabled (BCC_EN_ENH_ERROR in register 0xB set to 0).

8.6.1.13 FPD4_RX_DATAPATH_CTL Register (Address = 0xC) [Default = 0x00]

FPD4_RX_DATAPATH_CTL is shown in FPD4_RX_DATAPATH_CTL Register Field Descriptions.

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FPD4 Datapath Control Register 1 for Main Link Datapath (RX) The Datapath Control values are sent as part of the DCA sequence to the deserializer. The fields indicate capabilities and operational modes of the forward channel.

Table 8-63. FPD4_RX_DATAPATH_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	OVERRIDE_FC_CONFIG	R/W	0x0	0: Allow forward channel loading of this register 1: Disable loading of this register from the forward channel, keeps locally written values intact
6	FPD4_I2SB_FC_EN_P0	R/W	0x0	If FPD4 Audio uses forward channel GPIO, this bit enables 4-channel audio using FC_GPIO[3]. This is a per port register, meaning that the value in register 0xE PORT_SEL will allow this register to return different responses associated with the respective FPD Port.

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Table 8-63. FPD4_RX_DATAPATH_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:4	FPD4_I2S_TRANSPORT	R/W	0x0	FPD4 I2S Transport Select 00: I2S disabled over FPD4 link 01: I2S audio is sent over the forward channel as GPIO data. When PORT_SEL= 0, this applies to port 0. When PORT_SEL= 1, this applies to port 1. 10: I2S over data island for FPD4 stream 1 data 11: I2S over data island for FPD4 stream 0 data
3	VIDEO_DISABLED	R/W	0x0	FPD4 Forward Channel Video Disabled 0: Normal operation 1: Video is disabled, control channel is enabled This is a status bit only, indicating the forward channel is not sending active video. In this mode, the control channel and GPIO functions are enabled. Setting OVERRIDE_FC_CONFIG (bit[7]) allows override of this field and will prevent this bit from changing.
2	DUAL_LINK	R	0x0	FPD4 Link Mode 0: Single-Link mode enabled 1: Dual-Link mode enabled This bit will always be loaded from forward channel and cannot be written locally. To force DUAL_LINK receive mode, use the FPD4_RX_CFG register (address 0x31). Setting OVERRIDE_FC_CONFIG will prevent this bit from changing.
1:0	REG_GPIOEN_FC_P0	R/W	0x0	FPD4 Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: 1 GPIO 10: 2 GPIOs 11: 4 GPIOs Setting OVERRIDE_FC_CONFIG allows override of this field and will prevent this bit from changing. FPD3 mode has a fixed number of GPIOs.

8.6.1.14 PORT_SEL Register (Address = 0xE) [Default = 0x00]

PORT_SEL is shown in PORT_SEL Register Field Descriptions.

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FPD TX Port Register Page Select Select TX port register page for reading and writing port specific registers. The register provides separate controls for read selection and for write selection. The READ_PORT field provides access to read values from a single port. The WRITE_PORT_1 field and the WRITE_PORT_0 field provides individual enables for each port, allowing simultaneous writes to the 2 FPD Receive port register blocks. This register has a copy for each I2C access source. A separate copy of the TX_PORT_SEL register is maintained for each possible function that may access the registers, preventing conflict between the possible sources of register access.

Table 8-64. PORT_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PHYS_PORT_NUM	R	0x0	Physical port number. This filed provides the physical port connection when reading from a remote device via the Bidirectional Control Channel or through local I2C interface. When accessed via local I2C interfaces, the value returned is the I2C port connection. When accessed via Bidirectional Control Channel, the value returned is the port number of the received port connection.
5	RESERVED	R	0x0	Reserved

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Table 8-64. PORT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	READ_PORT	R/W	0x0	Select TX port for register read. This field selects one of the two TX port register blocks for readback. This applies to all paged FPD3/FPD4 Transmitter port registers. 0: Port 0 registers 1: Port 1 registers When access via local I2C interfaces, the default settings depends upon the interface as shown in the default value column.
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	WRITE_PORT_1	R/W	0x0	Write enable for TX port 1 registers. This bit enables writes to TX port 1 registers. Any combination of TX port registers can be written simultaneously. This applies to all paged FPD3/FPD4 transmitter port registers. 0: writes disabled 1: writes enabled
0	WRITE_PORT_0	R/W	0x0	Write enable for TX port 0 registers. This bit enables writes to TX port 0 registers. Any combination of TX port registers can be written simultaneously. This applies to all paged FPD3/FPD4 transmitter port registers. 0: writes disabled 1: writes enabled

8.6.1.15 FORCE_BACK_CHANNEL_ERROR Register (Address = 0xF) [Default = 0x00]

FORCE_BACK_CHANNEL_ERROR is shown in FORCE_BACK_CHANNEL_ERROR Register Field Descriptions.

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Table 8-65. FORCE_BACK_CHANNEL_ERROR Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R/W	0x0	Reserved
1	FORCE_BACK_CHANNEL_ERROR	R/W	0x0	This bit introduces errors into Back channel frame. This register also applies when the device is in BIST error checking mode.
0	FORCE_ONE_BACK_CHANNEL_ERROR	RH/W1S	0x0	This bit introduces one error into Back channel frame. This register also applies when the device is in BIST error checking mode. Self clearing bit.

8.6.1.16 GPI_PIN_STS1 Register (Address = 0x10) [Default = 0x00]

GPI_PIN_STS1 is shown in GPI_PIN_STS1 Register Field Descriptions.

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Table 8-66. GPI_PIN_STS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GPIO_PIN_STS[7:0]	R	0x0	Read Value of GPIO7:0 Pins Set as Input The returned value is only valid if the corresponding GPIO has been set as an input.

8.6.1.17 GPI_PIN_STS2 Register (Address = 0x11) [Default = 0x00]

GPI_PIN_STS2 is shown in GPI_PIN_STS2 Register Field Descriptions.

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Table 8-67. GPI_PIN_STS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	GPIO_PIN_STS[13:8]	R	0x0	Read Value of GPIO13:8 Pins Set as Input The returned value is only valid if the corresponding GPIO has been set as an input.

8.6.1.18 GPIO_IN_EN1 Register (Address = 0x12) [Default = 0xFF]

GPIO_IN_EN1 is shown in GPIO_IN_EN1 Register Field Descriptions.

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Table 8-68. GPIO_IN_EN1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x1	Reserved
5	GPIO13_INPUT_EN	R/W	0x1	GPIO13 Input Enable 0: Disabled 1: Enabled
4	GPIO12_INPUT_EN	R/W	0x1	GPIO12 Input Enable 0: Disabled 1: Enabled
3	GPIO11_INPUT_EN	R/W	0x1	GPIO11 Input Enable 0: Disabled 1: Enabled
2	GPIO10_INPUT_EN	R/W	0x1	GPIO10 Input Enable 0: Disabled 1: Enabled
1	GPIO9_INPUT_EN	R/W	0x1	GPIO9 Input Enable 0: Disabled 1: Enabled
0	GPIO8_INPUT_EN	R/W	0x1	GPIO8 Input Enable 0: Disabled 1: Enabled

8.6.1.19 GPIO_IN_EN0 Register (Address = 0x13) [Default = 0xFF]

GPIO_IN_EN0 is shown in GPIO_IN_EN0 Register Field Descriptions.

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Table 8-69. GPIO_IN_EN0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO7_INPUT_EN	R/W	0x1	GPIO7 Input Enable 0: Disabled 1: Enabled
6	GPIO6_INPUT_EN	R/W	0x1	GPIO6 Input Enable 0: Disabled 1: Enabled
5	GPIO5_INPUT_EN	R/W	0x1	GPIO5 Input Enable 0: Disabled 1: Enabled
4	GPIO4_INPUT_EN	R/W	0x1	GPIO4 Input Enable 0: Disabled 1: Enabled

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Table 8-69. GPIO_IN_EN0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable 0: Disabled 1: Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable 0: Disabled 1: Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable 0: Disabled 1: Enabled

8.6.1.20 TX_BIST_CTL_FPD3 Register (Address = 0x14) [Default = 0x00]

TX_BIST_CTL_FPD3 is shown in TX_BIST_CTL_FPD3 Register Field Descriptions.

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Table 8-70. TX_BIST_CTL_FPD3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	BISTEN_NO_RESET	R/W	0x0	FPD3 Enable BIST mode with FPD TX PLL reset This bit controls whether the BIST operation will reset the FPD TX PLL when BIST is enabled or disabled. When setting BIST_EN to 0, this bit should remain set to prevent resetting the PLL. 0: Reset FPD3 PLL 1: Don't reset FPD3 PLL
2:1	RESERVED	R/W	0x0	Reserved
0	FPD3_TX_BIST_EN	R/W	0x0	FPD3 Daisy Chain Transmit BIST Control Enables FPD3 BIST on the downstream FPD3 link. 0: Disabled 1: Enabled

8.6.1.21 GPIO0_PIN_CTL Register (Address = 0x15) [Default = 0x00]

GPIO0_PIN_CTL is shown in GPIO0_PIN_CTL Register Field Descriptions.

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Table 8-71. GPIO0_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO0_OUTPUT_EN	R/W	0x0	GPIO0 Output Enable 0: Disabled 1: Enabled
6:5	GPIO0_OUT_SRC	R/W	0x0	GPIO0 Output Source Select Selects output source for GPIO0 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present

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Table 8-71. GPIO0_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:0	GPIO0_OUT_SEL	R/W	0x0	GPIOx Output Select Determines the output data for the selected source. --If GPIOx_OUT_SRC is set to 0b0x (one of the FPD Ports: 00 -> Port 0, 01 -> Port 1), the following selections apply: 00000: Received BC_GPIO0 00001: Received BC_GPIO1 00010: Received BC_GPIO2 00011: Received BC_GPIO3 00100: Received BC_GPIO4 00101: Received BC_GPIO5 00110: Received BC_GPIO6 00111: Received BC_GPIO7 01000: Received BC_GPIO8 (valid only for FPD4) 01001: Received BC_GPIO9 (valid only for FPD4) 01010: Received BC_GPIO10 (valid only for FPD4) 01011: Received BC_GPIO11 (valid only for FPD4) 01100: Received BC_GPIO12 (valid only for FPD4) 01101: Received BC_GPIO13 (valid only for FPD4) 01110: Received BC_GPIO14 (valid only for FPD4) 01111: Received BC_GPIO15 (valid only for FPD4) 10000: Remote Interrupt 10001: Daisy Chain Lock Detect 10010: FPD TX Interrupt (active low) 10011: FPD TX Interrupt (active high) When GPIOx_OUT_SCR= 00: 10100: Received FC_GPIO0 10101: Received FC_GPIO1 10110: Received FC_GPIO2 10111: Received FC_GPIO3 11000: Received FC_GPIO4 (FPD3 Only) 11001: Received FC_GPIO5 (FPD3 Only) 11010: Received FC_GPIO6 (FPD3 Only) 11011: Received FC_GPIO7 (FPD3 Only) 11100: RX Lock Detect 11101: FPD-Link III BIST pass status 11110: Local interrupt status 11111: Reserved And when GPIOx_OUT_SCR= 01: 10100: Received FC_GPIO0 (In FPD3 DGPIO[0]) 10101: Received FC_GPIO1 (In FPD3 DGPIO[1]) 10110: Received FC_GPIO2 (In FPD3 DGPIO[2]) 10111: Received FC_GPIO3 (In FPD3 DGPIO[3]) 11000: FPD4 link BIST pass 11001: RX Lock Detect 11010: Reserved 11011: Reserved 11100: Reserved 11101: FPD-Link III BIST pass status 11110: Local interrupt status 11111: Reserved --If GPIOx_OUT_SRC is set to 10 (Device Status), the following selections apply: 00000: Fixed output value of 0 00001: Fixed output value of 1 00010: FPD-Link RX mode dependent Lock indication from enabled RX Ports. If dual mode, logical AND of port 0 and port 1 RX Lock indication. If single mode, port 0 RX Lock indication only 00011: Logical OR of RX Lock indication from enabled RX Ports 00100: Logical AND of RX Lock indication from RX Ports regardless of which ports are enabled 00101: Reserved with fixed output of 0 00110: Logical OR of RX Lock indication from enabled TX Ports (DC) 00111: Logical AND of RX Lock indication from enabled TX Ports (DC) 01000: I2S_DD 01001: I2S_DC

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Table 8-71. GPIO0_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
				01010: I2S_WS 01011: I2S_DB 01100: I2S_DA 01101: I2S_CLK 01110: Inverted I2S_CLK 01111: I2S clock from FPD PLL 10000: FPD-Link TX mode dependent Lock indication from enabled TX Ports (daisy chain). If dual mode, logical AND of port 0 and port 1 RX Lock indication. If single mode, port 0 RX Lock indication only 10001 - 11111: Reserved --If GPIOx_OUT_SRC is set to 11 (GPIOs received from forward channel as well as back channel), the following selections apply: 00000: Received Port 0 FC_GPIO0 00001: Received Port 0 FC_GPIO1 00010: Received Port 0 FC_GPIO2 00011: Received Port 0 FC_GPIO3 00100: Received Port 0 FC_GPIO4 (FPD3 Only) 00101: Received Port 0 FC_GPIO5 (FPD3 Only) 00110: Received Port 0 FC_GPIO6 (FPD3 Only) 00111: Received Port 0 FC_GPIO7 (FPD3 Only) 01000-01111: RESERVED 10000: Received Port 1 BC_GPIO0 10001: Received Port 1 BC_GPIO1 10010: Received Port 1 BC_GPIO2 10011: Received Port 1 BC_GPIO3 10100: Received Port 1 BC_GPIO4 10101: Received Port 1 BC_GPIO5 10110: Received Port 1 BC_GPIO6 10111: Received Port 1 BC_GPIO7 11000: Received Port 1 BC_GPIO8 (valid only for FPD4) 11001: Received Port 1 BC_GPIO9 (valid only for FPD4) 11010: Received Port 1 BC_GPIO10 (valid only for FPD4) 11011: Received Port 1 BC_GPIO11 (valid only for FPD4) 11100: Received Port 1 BC_GPIO12 (valid only for FPD4) 11101: Received Port 1 BC_GPIO13 (valid only for FPD4) 11110: Received Port 1 BC_GPIO14 (valid only for FPD4) 11111: Received Port 1 BC_GPIO15 (valid only for FPD4)

8.6.1.22 GPIO1_PIN_CTL Register (Address = 0x16) [Default = 0x00]

GPIO1_PIN_CTL is shown in GPIO1_PIN_CTL Register Field Descriptions.

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Table 8-72. GPIO1_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO1_OUTPUT_EN	R/W	0x0	GPIO1 Output Enable 0: Disabled 1: Enabled
6:5	GPIO1_OUT_SRC	R/W	0x0	GPIO1 Output Source Select Selects output source for GPIO1 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO1_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.23 GPIO2_PIN_CTL Register (Address = 0x17) [Default = 0x00]

GPIO2_PIN_CTL is shown in GPIO2_PIN_CTL Register Field Descriptions.

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Table 8-73. GPIO2_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO2_OUTPUT_EN	R/W	0x0	GPIO2 Output Enable 0: Disabled 1: Enabled
6:5	GPIO2_OUT_SRC	R/W	0x0	GPIO2 Output Source Select Selects output source for GPIO2 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO2_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.24 GPIO3_PIN_CTL Register (Address = 0x18) [Default = 0x00]

GPIO3_PIN_CTL is shown in GPIO3_PIN_CTL Register Field Descriptions.

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Table 8-74. GPIO3_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO3_OUTPUT_EN	R/W	0x0	GPIO3 Output Enable 0: Disabled 1: Enabled
6:5	GPIO3_OUT_SRC	R/W	0x0	GPIO3 Output Source Select Selects output source for GPIO3 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO3_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.25 GPIO4_PIN_CTL Register (Address = 0x19) [Default = 0x9C]

GPIO4_PIN_CTL is shown in GPIO4_PIN_CTL Register Field Descriptions.

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Table 8-75. GPIO4_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO4_OUTPUT_EN	R/W	0x1	GPIO4 Output Enable 0: Disabled 1: Enabled
6:5	GPIO4_OUT_SRC	R/W	0x0	GPIO4 Output Source Select Selects output source for GPIO4 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO4_OUT_SEL	R/W	0x1C	Same allocation as GPIO0_OUT_SEL

8.6.1.26 GPIO5_PIN_CTL Register (Address = 0x1A) [Default = 0xB9]

GPIO5_PIN_CTL is shown in GPIO5_PIN_CTL Register Field Descriptions.

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Table 8-76. GPIO5_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO5_OUTPUT_EN	R/W	0x1	GPIO5 Output Enable 0: Disabled 1: Enabled
6:5	GPIO5_OUT_SRC	R/W	0x1	GPIO5 Output Source Select Selects output source for GPIO5 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO5_OUT_SEL	R/W	0x19	Same allocation as GPIO0_OUT_SEL

8.6.1.27 GPIO6_PIN_CTL Register (Address = 0x1B) [Default = 0xC2]

GPIO6_PIN_CTL is shown in GPIO6_PIN_CTL Register Field Descriptions.

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Table 8-77. GPIO6_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO6_OUTPUT_EN	R/W	0x1	GPIO6 Output Enable 0: Disabled 1: Enabled
6:5	GPIO6_OUT_SRC	R/W	0x2	GPIO6 Output Source Select Selects output source for GPIO6 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO6_OUT_SEL	R/W	0x2	Same allocation as GPIO0_OUT_SEL

8.6.1.28 GPIO7_PIN_CTL Register (Address = 0x1C) [Default = 0x00]

GPIO7_PIN_CTL is shown in GPIO7_PIN_CTL Register Field Descriptions.

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Table 8-78. GPIO7_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO7_OUTPUT_EN	R/W	0x0	GPIO7 Output Enable 0: Disabled 1: Enabled
6:5	GPIO7_OUT_SRC	R/W	0x0	GPIO7 Output Source Select Selects output source for GPIO7 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO7_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.29 GPIO8_PIN_CTL Register (Address = 0x1D) [Default = 0x00]

GPIO8_PIN_CTL is shown in GPIO8_PIN_CTL Register Field Descriptions.

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Table 8-79. GPIO8_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO8_OUTPUT_EN	R/W	0x0	GPIO8 Output Enable 0: Disabled 1: Enabled
6:5	GPIO8_OUT_SRC	R/W	0x0	GPIO8 Output Source Select Selects output source for GPIO8 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO8_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.30 GPIO9_PIN_CTL Register (Address = 0x1E) [Default = 0x00]

GPIO9_PIN_CTL is shown in GPIO9_PIN_CTL Register Field Descriptions.

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Table 8-80. GPIO9_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO9_OUTPUT_EN	R/W	0x0	GPIO9 Output Enable 0: Disabled 1: Enabled
6:5	GPIO9_OUT_SRC	R/W	0x0	GPIO9 Output Source Select Selects output source for GPIO9 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO9_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.31 GPIO10_PIN_CTL Register (Address = 0x1F) [Default = 0x00]

GPIO10_PIN_CTL is shown in GPIO10_PIN_CTL Register Field Descriptions.

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Table 8-81. GPIO10_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO10_OUTPUT_EN	R/W	0x0	GPIO10 Output Enable 0: Disabled 1: Enabled
6:5	GPIO10_OUT_SRC	R/W	0x0	GPIO10 Output Source Select Selects output source for GPIO10 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO10_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.32 GPIO11_PIN_CTL Register (Address = 0x20) [Default = 0x00]

GPIO11_PIN_CTL is shown in GPIO11_PIN_CTL Register Field Descriptions.

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Table 8-82. GPIO11_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO11_OUTPUT_EN	R/W	0x0	GPIO11 Output Enable 0: Disabled 1: Enabled
6:5	GPIO11_OUT_SRC	R/W	0x0	GPIO11 Output Source Select Selects output source for GPIO11 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO11_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.33 GPIO12_PIN_CTL Register (Address = 0x21) [Default = 0x00]

GPIO12_PIN_CTL is shown in GPIO12_PIN_CTL Register Field Descriptions.

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Table 8-83. GPIO12_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO12_OUTPUT_EN	R/W	0x0	GPIO12 Output Enable 0: Disabled 1: Enabled
6:5	GPIO12_OUT_SRC	R/W	0x0	GPIO12 Output Source Select Selects output source for GPIO12 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO12_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.34 GPIO13_PIN_CTL Register (Address = 0x22) [Default = 0x00]

GPIO13_PIN_CTL is shown in GPIO13_PIN_CTL Register Field Descriptions.

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Table 8-84. GPIO13_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO13_OUTPUT_EN	R/W	0x0	GPIO13 Output Enable 0: Disabled 1: Enabled
6:5	GPIO13_OUT_SRC	R/W	0x0	GPIO13 Output Source Select Selects output source for GPIO13 data: 00: FPD Port 0 01: FPD Port 1 10: Device Status 11: Remote GPIO Info - repeats present
4:0	GPIO13_OUT_SEL	R/W	0x0	Same allocation as GPIO0_OUT_SEL

8.6.1.35 MODE_STS Register (Address = 0x24) [Default = X]

MODE_STS is shown in MODE_STS Register Field Descriptions.

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Table 8-85. MODE_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	MODE1_DONE	R	0x0	Indicates MODE_SEL1 strap value has stabilized and been latched
6:4	MODE1_DECODE	R	X	Returns the 3-bit decode of the MODE_SEL1 pin
3	MODE0_DONE	R	0x0	Indicates MODE_SEL0 strap value has stabilized and been latched
2:0	MODE0_DECODE	R	X	Returns the 3-bit decode of the MODE_SEL0 pin

8.6.1.36 FPD3_RX_DATAPATH_CTL Register (Address = 0x27) [Default = 0x00]

FPD3_RX_DATAPATH_CTL is shown in FPD3_RX_DATAPATH_CTL Register Field Descriptions.

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FPD-LINK III Datapath Control. This configures the selected FPD3 main link datapath (RX).

Table 8-86. FPD3_RX_DATAPATH_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	OVERRIDE_FC_CONFIG	R/W	0x0	0: Allow forward channel loading of this register 1: Disable loading of this register from the forward channel, keeping locally written values intact. Values can be written via I2C.
6	PASS_RGB	R/W	0x0	Setting this bit causes RGB data to be sent independent of DE (Date Enable, pin 64). This allows operation in systems which may not use DE to frame video data or send other data when DE is deasserted. Note that setting this bit prevents HDCP operation and blocks packetized audio. This bit does not need to be set in DS90UB984 0: Normal operation 1: Pass RGB independent of DE toggle This bit is automatically loaded from the remote serializer or upstream deserializer unless bit 7 of this register is set.
5	DE_POLARITY	R	0x0	DE (Data Enable) Polarity Status 0: DE is positive (active high, idle low) 1: DE is inverted (active low, idle high) - Not supported by 984. This bit is automatically loaded from the remote serializer unless bit 7 of this register is set. This bit must be 0 for proper FPD3 RGB DE functionality. The DE signal should be set in positive polairty mode at the serializer.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	18_BIT_VIDEO_SEL	R/W	0x0	0: 24-bit video mode 1: 18-bit video mode This bit is automatically loaded from the remote serializer or upstream deserializer unless bit 7 of this register is set.
1	I2S_TRANSPORT_SEL	R/W	0x0	0: Enable I2S Data Island Transport 1: Enable I2S In-Band Transport This bit is automatically loaded from the remote serializer or upstream deserializer unless bit 7 of this register is set.
0	I2S_4CH_EN	R/W	0x0	I2S 4-Channel Enable Bit3 of this register must be set in order for this bit to be valid. 0: Disable I2S 4-Channel 1: Enable I2S 4-Channel This bit is automatically loaded from the remote serializer unless bit 7 of this register is set.

8.6.1.37 FPD3_RX_DATAPATH_CTL2 Register (Address = 0x28) [Default = 0x24]

FPD3_RX_DATAPATH_CTL2 is shown in FPD3_RX_DATAPATH_CTL2 Register Field Descriptions.

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FPD-LINK III Datapath Control. This configures the selected FPD3 main link datapath (RX).

Table 8-87. FPD3_RX_DATAPATH_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OVERRIDE_FC_CONFIG	R/W	0x0	0: Allow forward channel loading of this register 1: Disable loading of this register from the forward channel, keeping locally written values intact. Values can still be written via I2C
6	RESERVED	R/W	0x0	Reserved
5	VIDEO_DISABLED	R/W	0x1	FPD3 Forward channel video disable 0: Normal operation 1: Video is disabled, control channel is enabled This is a status bit indicating the forward channel is not sending active video. In this mode, the control channel and GPIO functions are enabled. Note: This bit is automatically loaded from the remote serializer or upstream deserializer unless bit 7 of this register is set.
4	DUAL_LINK	R/W	0x0	0: Single-Link mode enabled 1: Dual-Link mode enabled This bit indicates whether the FPD3 serializer is in single link or dual link mode. This control is used for recovering forward channel data when the FPD3 receiver is in auto-detect mode. To force DUAL_LINK receive mode, use register 0x32[5:4] FPD_RX_CTL. Note: This bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
3	RESERVED	R/W	0x0	Reserved
2	I2S_DISABLE	R/W	0x1	0: Normal Operation 1: I2S Disabled
1	RESERVED	R/W	0x0	Reserved
0	I2S_SURROUND	R/W	0x0	0: I2S Surround disabled 1: I2S Surround enabled

8.6.1.38 BCC_WDOG_CTL Register (Address = 0x29) [Default = 0xFE]

BCC_WDOG_CTL is shown in BCC_WDOG_CTL Register Field Descriptions.

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Bidirectional Control Channel Watchdog Timer Control

Table 8-88. BCC_WDOG_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	BCC_WATCHDOG_TIMER	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0. Example: Time out= 127 * 2 ms= 254 ms
0	BCC_WDOG_DIS	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 0: Enables BCC Watchdog Timer operation 1: Disables BCC Watchdog Timer operation

8.6.1.39 I2C_CONTROL Register (Address = 0x2A) [Default = 0x1E]

I2C_CONTROL is shown in I2C_CONTROL Register Field Descriptions.

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Table 8-89. I2C_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

Table 8-89. I2C_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:4	SDA_HOLD_TIME	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 5 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xE	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be ignored. Units are 5 nanoseconds.

8.6.1.40 SCL_HIGH_TIME Register (Address = 0x2B) [Default = 0x7F]

SCL_HIGH_TIME is shown in SCL_HIGH_TIME Register Field Descriptions.

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Table 8-90. SCL_HIGH_TIME Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TX_SCL_HIGH	R/W	0x7F	I2C Controller SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. Units are 5 ns for the nominal oscillator clock frequency. Min_delay= 5ns * (TX_SCL_HIGH)

8.6.1.41 SCL_LOW_TIME Register (Address = 0x2C) [Default = 0x7F]

SCL_LOW_TIME is shown in SCL_LOW_TIME Register Field Descriptions.

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Table 8-91. SCL_LOW_TIME Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TX_SCL_LOW	R/W	0x7F	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional clock periods. Min_delay= 38.0952ns * (TX_SCL_LOW + 5)

8.6.1.42 BIST_CONTROL Register (Address = 0x2D) [Default = 0x00]

BIST_CONTROL is shown in BIST_CONTROL Register Field Descriptions.

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In FPD3 mode, only the Port 0 copy of this register needs to be changed. In FPD4 mode, both Port 0 and Port 1 copies need to be changed.

Table 8-92. BIST_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5:4	RESERVED	R/W	0x0	Reserved

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Table 8-92. BIST_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	REMOTE_BIST_EN	R/W	0x0	Remote BIST enable - Main Link BIST Setting this bit in the local deserializer allows Remote BIST operation to be initiated from the main link partner (serializer or upstream deserializer) rather than from the local device. This bit should be set to 1 prior to enabling the BIST from the main link partner, and set to 0 after disabling BIST from the main link partner. Once the main link partner (upstream device) begins BIST, control channel operations will be unavailable across the link and will remain unavailable until after the main link device stops sending the BIST pattern. In FPD3 mode, Port 1 control is not used. In FPD4 mode, Port 1 control is used.
2:1	RESERVED	R/W	0x0	Reserved
0	BIST_EN	R/W	0x0	Main Link BIST Control Setting this bit will enable BIST operation. The local deserializer will enter BIST mode and send a command to the serializer or upstream deserializer to send the BIST pattern. When this bit is cleared, the local deserializer will send a command to the upstream device to stop sending the BIST pattern. This bit should remain 0 if the REMOTE_BIST_EN control is used. 1: Enabled 0: Disabled In FPD3 mode, port 1 control is not used.

8.6.1.43 FPD_RX_CTL Register (Address = 0x2E) [Default = 0x22]

FPD_RX_CTL is shown in FPD_RX_CTL Register Field Descriptions.

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Table 8-93. FPD_RX_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R/W	0x1	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	PLL_REFCLK_SEL	R/W	0x0	FPD RX PLL Reference Clock 0: External oscillator clock (XO pin) 1: External reference clock (ZCLK pin)
1:0	FPD_RX_INVERSION	R/W	0x2	Invert FPD4 or FPD3 Rx Input Data 00: Port0 RIN0 pins are in their default configuration (RIN0+= pin 72 and RIN0-= pin 73). Port1 RIN1 pins are inverted (RIN1+= pin 82 and RIN1-= pin 81). 01: Port0 RIN0 pins are inverted (RIN0+= pin 73 and RIN0-= pin 72). Port1 RIN1 pins are in their default configuration (RIN1+= pin 81 and RIN1-= pin 82). 10: Port0 RIN0 pins are in their default configuration (RIN0+= pin 72 and RIN0-= pin 73). Port1 RIN1 pins are in their default configuration (RIN1+= pin 81 and RIN1-= pin 82). 11: Port0 RIN0 pins are inverted (RIN0+= pin 73 and RIN0-= pin 72). Port1 RIN1 pins are inverted (RIN1+= pin 82 and RIN1-= pin 81).

8.6.1.44 IO_CTL Register (Address = 0x2F) [Default = X]

IO_CTL is shown in IO_CTL Register Field Descriptions.

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Table 8-94. IO_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	I2C_SEL3P3V	R/W	X	I2C select 0: 1.8V 1: 3.3V Strapped from the IDx pin during power-up
6	HPD_SEL3P3V	R/W	X	HPD 3.3V select 0: 1.8V 1: 3.3V The default value for the register is strapped at power-on based on the MODE_SEL1 pin
5	INTB_SEL3P3V	R/W	0x1	INTB 3.3V select 0: 1.8V 1: 3.3V
4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	X	Reserved
2:0	RESERVED	R	0x0	Reserved

8.6.1.45 MASK_ID_REV Register (Address = 0x30) [Default = 0x10]

MASK_ID_REV is shown in MASK_ID_REV Register Field Descriptions.

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Table 8-95. MASK_ID_REV Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	REV_ID	R	0x1	Revision ID 0001: CS1.0 0011: CS2.0 0100: CS3.0
3:0	RESERVED	R	0x0	Reserved

8.6.1.46 FPD4_RX_CFG Register (Address = 0x31) [Default = X]

FPD4_RX_CFG is shown in FPD4_RX_CFG Register Field Descriptions.

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FPD4 Main Link Datapath (RX) Configuration

Table 8-96. FPD4_RX_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	FPD4_RX_LOCK_MODE	R/W	0x0	FPD4 Main Link (RX) Lock Mode: Determines operating conditions for indication of RX_LOCK and generation of video data. 0: RX_LOCK asserted only when receiving active video (forward channel VIDEO_DISABLED bit3 in register 0x0C must be 0 for RX_LOCK to assert when active video is received). Active video is determined when the correct DCA sequence is received by the deserializer. 1: RX_LOCK asserted when device is linked to a serializer or upstream deserializer even if active video is not being sent. This allows indication of valid link where Bidirectional Control Channel is enabled, but local deserializer is not receiving audio/video data.
6	RESERVED	R/W	0x1	Reserved
5	RESERVED	R/W	0x1	Reserved

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Table 8-96. FPD4_RX_CFG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	FPD4_INPUT_MODE	R/W	0x0	Selects operating mode for the FPD4 Receiver 000: Auto-detect mode -- auto-detect between single/dual operation 001: Forced single Port 0 010: Reserved 011: Forced Dual lane 1xx: Reserved Dual lane should only be set if both ports are enabled for FPD4 operation.
1	FPD4_RX_ENABLE_P1	R/W	X	FPD3 or FPD4 mode control for FPD Main Link (RX) Port 1 This bit controls the FPD3 operating mode for the FPD Receiver interface for Port 0. 0: Select FPD3 input mode 1: Select FPD4 input mode This field is loaded from the MODE_SEL0 and MODE_SEL1 pins at power-up.
0	FPD4_RX_ENABLE_P0	R/W	X	FPD3 or FPD4 mode control for FPD Main Link (RX) Port 0 This bit controls the FPD3 operating mode for the FPD Receiver interface for Port 0. 0: Select FPD3 input mode 1: Select FPD4 input mode This field is loaded from the MODE_SEL0 and MODE_SEL1 pins at power-up.

8.6.1.47 FPD3_RX_CTL Register (Address = 0x32) [Default = 0x00]

FPD3_RX_CTL is shown in FPD3_RX_CTL Register Field Descriptions.

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FPD3 Main Link Datapath (RX) Configuration

Table 8-97. FPD3_RX_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RX_LOCK_MODE	R/W	0x0	Main Link (RX) Lock Mode: Determines operating conditions for indication of RX_LOCK and generation of video data. 0: RX_LOCK asserted only when receiving active video (forward channel VIDEO_DISABLED bit5 in register 0x28 is 0) 1: RX_LOCK asserted when device is linked to a serializer or upstream deserializer even if active video is not being sent. This allows indication of valid link where Bidirectional Control Channel is enabled, but local deserializer is not receiving Audio/Video data.
6	RAW_2ND_BC	R/W	0x0	Enable Raw Secondary Back Channel This bit is only valid in FPD3 Dual Mode. 0: Secondary back channel has normal operation 1: Secondary back channel will operate in raw mode, which passes D_GPIO0 from the local device to the upstream main link device without any oversampling or filtering
5:4	FPD3_INPUT_MODE	R/W	0x0	FPD-Link III Input Mode Determines operating mode of dual FPD-Link III Receive interface 00: Auto-detect based on received data 01: Forced Mode: Dual link 10: Forced Mode: Single link, Port 0 11: Reserved
3	RESERVED	R/W	0x0	Reserved

Table 8-97. FPD3_RX_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2:0	HSCC_MODE	R/W	0x0	FPD3 High-Speed Control Channel Mode Enables high-speed modes for the secondary link back-channel, allowing higher speed signaling of GPIOs or SPI interface: These bits indicates the High Speed Control Channel mode of operation: 000: Normal frame, GPIO mode 001: High Speed GPIO mode, 1 GPIO 010: High Speed GPIO mode, 2 GPIOs 011: High Speed GPIO mode: 4 GPIOs 100: Reserved 101: Reserved 110: High Speed, Forward Channel SPI mode 111: High Speed, Reverse Channel SPI mode

8.6.1.48 FPD_RX_DIVIDER_SEL Register (Address = 0x33) [Default = X]

FPD_RX_DIVIDER_SEL is shown in FPD_RX_DIVIDER_SEL Register Field Descriptions.

Return to the Summary Table.

Table 8-98. FPD_RX_DIVIDER_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3:2	CH1_FPD_RX_POST_DIV	R/W	X	Post Divider in FPD4 RX Path for Channel 1 This field is strapped at start up. The strapped FPD4 operating speed will set this field as described: 00: 13.5 Gbps, 12.528 Gbps and 10.8 Gbps. Post divider value of 1 01: 6.75 Gbps. Post divider value of 2 10: 3.375 Gbps. Post divider value of 4 11: Reserved This information is highlighted in the Manual FPD-Link IV RX PLL Configuration section in the FPD-Link IV RX PLL table.
1:0	CH0_FPD_RX_POST_DIV	R/W	X	Post Divider in FPD4 RX Path for Channel 0 This field is strapped at start up. The strapped FPD4 operating speed will set this field as described: 00: 13.5 Gbps, 12.528 Gbps and 10.8 Gbps. Post divider value of 1 01: 6.75 Gbps. Post divider value of 2 10: 3.375 Gbps. Post divider value of 4 11: Reserved This information is highlighted in the Manual FPD-Link IV RX PLL Configuration section in the FPD-Link IV RX PLL table.

8.6.1.49 LINK_ERROR_COUNT Register (Address = 0x34) [Default = 0x03]

LINK_ERROR_COUNT is shown in LINK_ERROR_COUNT Register Field Descriptions.

Return to the Summary Table.

This is an FPD3 only register.

Table 8-99. LINK_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R/W	0x0	Reserved

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Table 8-99. LINK_ERROR_COUNT Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	LINK_ERROR_COUNT_ENABLE	R/W	0x0	Enable FPD3 Serial Link Data Integrity Error Count 0: Disable 1: Enable error count
3:0	LINK_ERROR_COUNT_THRES	R/W	0x3	Link Error Count Threshold FPD-Link frames are monitored for link errors. If error count is enabled (bit[4]), deserializer loses lock once error count reaches threshold. If disabled (bit[4]), deserilizer loses lock with one error.

8.6.1.50 FPD_RX_BIST_ACTIVE Register (Address = 0x36) [Default = 0x00]

FPD_RX_BIST_ACTIVE is shown in FPD_RX_BIST_ACTIVE Register Field Descriptions.

Return to the Summary Table.

Table 8-100. FPD_RX_BIST_ACTIVE Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	FPD4_BIST_ACT_P1	R	0x0	FPD4 RX BIST Active Port 1 This bit indicates when the FPD4 Receiver for Port 1 is receiving the BIST pattern
2	FPD4_BIST_ACT_P0	R	0x0	FPD4 RX BIST Active Port 0 This bit indicates when the FPD4 Receiver for Port 0 is receiving the BIST pattern
1	FPD3_BIST_ACT_P1	R	0x0	FPD3 RX BIST Active Port 1 This bit indicates when the FPD3 Receiver for Port 1 is receiving the BIST pattern
0	FPD3_BIST_ACT_P0	R	0x0	FPD3 RX BIST Active Port 0 This bit indicates when the FPD3 Receiver for Port 0 is receiving the BIST pattern

8.6.1.51 I2C_CTRL_CHAIN_CTL1 Register (Address = 0x38) [Default = 0x09]

I2C_CTRL_CHAIN_CTL1 is shown in I2C_CTRL_CHAIN_CTL1 Register Field Descriptions.

Return to the Summary Table.

Table 8-101. I2C_CTRL_CHAIN_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5	RX_LOCK_DIS_P1	R/W	0x0	FPD4 Main Link RX Lock Disable for I2C Transactions on Port 1 0: Forward channel RX lock required for remote I2C transactions to occur on port 1 1: Forward channel RX lock does not block remote I2C transactions on port 1 RX_LOCK status is in register 0x53
4	RX_LOCK_DIS_P0	R/W	0x0	FPD4 Main Link RX Lock Disable for I2C Transactions on Port 0 0: Forward channel RX lock required for remote I2C transactions to occur on port 0 1: Forward channel RX lock does not block remote I2C transactions on port 0 RX_LOCK status is in register 0x53

Table 8-101. I2C_CTRL_CHAIN_CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	FPD3_I2C_PORT_SWITCH	R/W	0x9	FPD3 Downstream Controller to I2C Block 1 (I2C_SDA1, I2C_SCL1) 0x0-0x5: Reserved 0x6: FPD3 daisy chain special setting: Used when the local deserializer is connected to a downstream daisy chained deserializer and their link uses FPD3. These bits should be set only if the downstream deserializer desires to send I2C communications to an external I2C device connected to I2C Port 1 (I2C_SDA1 and I2C_SCL1). The default configuration only allows the FPD3 downstream deserializer to communicate to an external device on I2C Port 0. 0x7-0x8: Reserved 0x9: Default setting (recommended for all cases except the aforementioned) 0xA-0xF: Reserved

8.6.1.52 FPD4_ERR_FLAGS Register (Address = 0x3B) [Default = 0x00]

FPD4_ERR_FLAGS is shown in FPD4_ERR_FLAGS Register Field Descriptions.

Return to the Summary Table.

Table 8-102. FPD4_ERR_FLAGS Register Field Descriptions

Bit	Field	Type	Default	Description
7	ALL_ERR_FLAG_ENABLE	R/W	0x0	Enable error flag detection located at register 0x45 bit[4]. This bit must be written in order for the error flag to occur in that bit.
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	ALL_ERR_FLAG	R	0x0	FPD4 Link Error Flag 0: No transaction error flag 1: Transaction error occurred. Can be caused by CRC, ECC or transmission packet errors.
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

8.6.1.53 IND_ACC_CTL Register (Address = 0x40) [Default = 0x00]

IND_ACC_CTL is shown in IND_ACC_CTL Register Field Descriptions.

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Table 8-103. IND_ACC_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved

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Table 8-103. IND_ACC_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:2	IND_ACC_SEL	R/W	0x0	Indirect Access Register Select: Selects target page for register access 00000: Reserved 00001: Secondary Data Control 00010: FPD4 RX PLL registers 00011: FPD3/4 TX PLL registers 00100: Reserved 00101: FPD RX Digital 00110: HDCP RX 00111: Reserved 01000: FPD3/4 TX Digital 01001: Reserved 01010: FPD3 TX INT 01011: eDP/DP Control registers 01100: eDP/DP PLL registers 01101: Reserved 01110: AEQ 01111: DFT/MBIST 10000: Reserved 10001: FPD Tx Link Layer 10010: FPD Rx Link Layer 10011: Reserved 10100: Display Timing and PATGEN registers 10101 - 10110: Reserved 10111: LMS-AEQ 11000 - 11010: Reserved 11011: SAR ADC Control
1	IND_ACC_AUTO_INC	R/W	0x0	Indirect Access Auto Increment 0: Address does not auto-increment after read / write 1: Address auto-increments after read / write
0	IND_ACC_READ	R/W	0x0	Indirect Access Register Read: 0: Indirect access write 1: Indirect access read

8.6.1.54 IND_ACC_ADDR Register (Address = 0x41) [Default = 0x00]

IND_ACC_ADDR is shown in IND_ACC_ADDR Register Field Descriptions.

Return to the Summary Table.

Table 8-104. IND_ACC_ADDR Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IND_ACC_ADDR	R/W	0x0	Indirect Access Register Offset This register contains the 8-bit register offset/address for the indirect access.

8.6.1.55 IND_ACC_DATA Register (Address = 0x42) [Default = 0x00]

IND_ACC_DATA is shown in IND_ACC_DATA Register Field Descriptions.

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Table 8-105. IND_ACC_DATA Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IND_ACC_DATA	R/W	0x0	Indirect Access Register Data: This register performs an indirect write to the selected analog block register. The data written to this register is the data written to the selected block register. Reading this register will return the value of the selected indirect access register.

8.6.1.56 RX_INT_STS Register (Address = 0x43) [Default = 0x00]

RX_INT_STS is shown in RX_INT_STS Register Field Descriptions.

Return to the Summary Table.

Interrupt Status Register - Backchannel The information in this register are sent via the backchannel to the upstream device. On the upstream device, these interrupt status bits can be muxed to GPIO pins.

Table 8-106. RX_INT_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	RX_INT	R	0x0	Back Channel Interrupt This bit is set if any of the enabled interrupts in this register occur. The interrupt status bit can be enabled in RX_INT_CTL register (address 0x44). There are separate versions of this register for each port, mainly to differentiate between the INTB interrupt condition. In FPD4, each back channel can enable a separate set of interrupts (only Port 0 is used for FPD3 mode).
6	RESERVED	R	0x0	Reserved
5	IS_FPD_TX1	R	0x0	Interrupt Status FPD Daisy Chain Link (TX) Port 1 This bit is set when an interrupt has occurred for FPD TX Port 1. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. For FPD3 mode, see the HDCP_ICR and HDCP_ISR registers on Page 10 For FPD4 mode, see the INTR_CTL_FPD4_PORT and INTR_STS_FPD4_PORT registers on Page 8 (registers 0x8C and 0x8D).
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	IS_FPD_TX0	R	0x0	Interrupt Status FPD Daisy Chain Link (TX) Port 0 This bit is set when an interrupt has occurred for FPD TX Port 0. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. For FPD3 mode, see the HDCP_ICR and HDCP_ISR registers on Page 10 For FPD4 mode, see the INTR_CTL_FPD4_PORT and INTR_STS_FPD4_PORT registers on Page 8 (registers 0x8C and 0x8D).
1	IS_FPD_RX	R	0x0	Interrupt Status for FPD (RX) Main Link This bit is set when an interrupt has occurred for the FPD Main Link. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. See the INTR_CTL_FPD4_RX and INTR_STS_FPD4_RX registers (address 0x4D and 0x4E) on indirect page 18.

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Table 8-106. RX_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	IS_DOWNSTRM_INTB_P0	R	0x0	Interrupt Status for INTB pin When set, an interrupt has occurred on INTB_IN Input Pin or on a remote interrupt signal from a downstream FPD link. The events that can be signaled on this interrupt are controlled by the INTB_ICR_P0/P1 registers (address 0x7E and 0x7F) on Main Registers 2 (Indirect Page 1). This interrupt signal (active low) is passed on the back channel without latching the interrupt. This event will be cleared when the downstream interrupt conditions are cleared.

8.6.1.57 RX_INT_CTL Register (Address = 0x44) [Default = 0x01]

RX_INT_CTL is shown in RX_INT_CTL Register Field Descriptions.

Return to the Summary Table.

This register maps the received interrupts to be sent on Main Link Port 0 or Port 1, based on which PORT_SEL is enabled when writing to this register.

Table 8-107. RX_INT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	IE_EN	R/W	0x0	Register Interrupt Enable 0: Interrupts in this register are disabled 1: Interrupts in this register are available to be enabled, the individual enable bit and this bit must be set.
6	IE_DP1	R/W	0x0	Interrupt Enable for Display Port 1 0: Interrupt disabled 1: Interrupt enabled
5	IE_FPD_TX1_P0	R/W	0x0	Interrupt Enable for FPD Daisy Chain (TX) Port 1 0: Interrupt disabled 1: Interrupt enabled
4	IE_EDID_RD	R/W	0x0	Interrupt Enable for EDID Read 0: Interrupt disabled 1: Interrupt enabled
3	IE_DP0_P0	R/W	0x0	Interrupt Enable for Display Port 0 0: Interrupt disabled 1: Interrupt enabled
2	IE_FPD_TX0_P0	R/W	0x0	Interrupt Enable for FPD Daisy Chain (TX) Port 0 0: Interrupt disabled 1: Interrupt enabled
1	IE_FPD_RX_P0	R/W	0x0	Interrupt Enable for FPD (RX) Main Link 0: Interrupt disabled 1: Interrupt enabled
0	IE_INTB_P0	R/W	0x1	INTB Interrupt Enable Enable interrupt from the INTB_IN input pin on the local deserializer or on a remote interrupt signal from a downstream FPD link. The events that can be signaled on this interrupt are controlled by the INTB_ICR_P0/P1 registers (address 0x7E and 0x7F) on Secondary Data Control (Indirect Page 1). 0: Interrupt disabled 1: Interrupt enabled

8.6.1.58 LOCAL_INT_STS Register (Address = 0x45) [Default = 0x00]

LOCAL_INT_STS is shown in LOCAL_INT_STS Register Field Descriptions.

Return to the Summary Table.

Table 8-108. LOCAL_INT_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	IE_LCL_INTB_P0	R/W	0x0	Interrupt Enable for INTB_STS indication If this bit is set to 1, an interrupt in the IS_LCL_INTB bit (bit[0]) will be passed to the IS_LOCAL_INT bit in the INTERRUPT_STS register (0x51[0]). If set to a 0, the LCL_INTB_STS will still be valid, but will not get propagated to the INTERRUPT_STS register (address 0x51).
6	RESERVED	R	0x0	Reserved
5	SAR_ADC_INT	R	0x0	Interrupt Status from SAR_ADC Controller This bit indicates if an interrupt has been reported by the SAR_ADC Controller via the temperature sensor, the voltage sensor, or line fault detection. Interrupt control/status for these events are available in the SAR_ADC_ICR_ISR register (address 0xCE).
4	IS_FPD4_ERR_FLAGS	R	0x0	Interrupt Status for FPD4_ERR_FLAGS events REQUIRES ENABLING 0x3B[7] FIRST. This bit will indicate if an interrupt from the FPD4_ERR_FLAGS register (address 0x3B) has occurred. This bit will be cleared upon read of the FPD4_ERR_FLAGS register. If this bit is set, the interrupt will automatically be propagated to the IS_LOCAL_INT bit in the INTERRUPT_STS register (address 0x51).
3	IS_TRGT_BCC_STS	R	0x0	Interrupt Status for TRGT_BCC_STATUS events This bit will indicate if an interrupt from the TRGT_BCC_STATUS register (address 0xA) has occurred. This bit will be cleared upon read of the TRGT_BCC_STATUS register. If this bit is set, the interrupt will automatically be propagated to the IS_LOCAL_INT bit in the INTERRUPT_STS register (address 0x51).
2	IS_RX_BCC_STS	R	0x0	Interrupt Status for RX_BCC_STATUS events This bit will indicate if an interrupt from the RX_BCC_STATUS register (address 0x9) has occurred. This bit will be cleared upon read of the RX_BCC_STATUS register. If this bit is set, the interrupt will automatically be propagated to the IS_LOCAL_INT bit in the INTERRUPT_STS register (address 0x51).
1	IS_TX_BCC_STS	R	0x0	Interrupt Status for TX_BCC_STATUS events This bit will indicate if an interrupt from the TX_BCC_STATUS register (address 0x8) has occurred. This bit will be cleared upon read of the TX_BCC_STATUS register. If this bit is set, the interrupt will automatically be propagated to the IS_LOCAL_INT bit in the INTERRUPT_STS register (address 0x51).
0	IS_LCL_INTB	RC	0x0	Interrupt Status for INTB events An interrupt has occurred on INTB_IN Input Pin or on a remote interrupt signal from a downstream FPD link. The events that can be signals on this interrupt are controlled by the INTB_ICR_P0/P1 registers (address 0x7E and 0x7F) on Main Registers 2 (Indirect Page 1). This register is a latched version of the interrupt signal and will be cleared when this register is read. To re-arm these interrupts it may be necessary to clear the remote interrupt condition that caused this event. Current status of the remote events is available in the INTB_ISR_P0/P1 registers on Main Registers 2 (Indirect Page 1).

8.6.1.59 RX_MODE_STS2 Register (Address = 0x47) [Default = X]

RX_MODE_STS2 is shown in RX_MODE_STS2 Register Field Descriptions.

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Table 8-109. RX_MODE_STS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	MODE2_DONE	R	0x0	Indicates MODE_SEL2 value has stabilized and been latched

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Table 8-109. RX_MODE_STS2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2:0	MODE2_DECODE	R	X	Returns the 3-bit decode of the MODE_SEL2 pin

8.6.1.60 APB_CTL Register (Address = 0x48) [Default = 0x00]

APB_CTL is shown in APB_CTL Register Field Descriptions.

Return to the Summary Table.

APB Control Register

Table 8-110. APB_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	APB_SELECT	R/W	0x0	APB Select: Selects target for register access: 00000: DisplayPort TX 0 APB registers 00001: DisplayPort TX 1 APB registers 00010: Reserved 00011: Unique ID (read only) 00100 - 11111: Reserved
2	APB_AUTO_INC	R/W	0x0	APB Auto-Increment 0: Auto-increment disabled 1: Auto-increment mode enabled. Upon completion of an APB read or write, the APB address will automatically be incremented by 1.
1	APB_READ	RH/W1S	0x0	Start APB Read Setting this bit to a 1 will begin an APB read. Read data will be available in the APB_DATA0 register (address 0x4B). The APB_ADR0 register (address 0x49) should be programmed prior to setting this bit. This bit will be cleared when the read is complete.
0	APB_ENABLE	R/W	0x0	APB Interface Enable 0: APB interface disabled 1: APB interface enabled. The APB_SELECT bits[7:3] indicate what device is selected.

8.6.1.61 APB_ADR0 Register (Address = 0x49) [Default = 0x00]

APB_ADR0 is shown in APB_ADR0 Register Field Descriptions.

Return to the Summary Table.

APB Address Register 0

Table 8-111. APB_ADR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	APB_ADR0	R/W	0x0	APB Address byte 0 (LSB)

8.6.1.62 APB_ADR1 Register (Address = 0x4A) [Default = 0x00]

APB_ADR1 is shown in APB_ADR1 Register Field Descriptions.

Return to the Summary Table.

APB Address Register 1

Table 8-112. APB_ADR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	APB_ADR1	R/W	0x0	APB Address byte 1 (MSB)

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8.6.1.63 APB_DATA0 Register (Address = 0x4B) [Default = 0x00]

APB_DATA0 is shown in APB_DATA0 Register Field Descriptions.

Return to the Summary Table.

APB Data Register 0

Table 8-113. APB_DATA0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	APB_DATA0	R/W	0x0	Byte 0 (LSB) of the APB Interface Data

8.6.1.64 APB_DATA1 Register (Address = 0x4C) [Default = 0x00]

APB_DATA1 is shown in APB_DATA1 Register Field Descriptions.

Return to the Summary Table.

APB Data Register 1

Table 8-114. APB_DATA1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	APB_DATA1	R/W	0x0	Byte 1 of the APB Interface Data

8.6.1.65 APB_DATA2 Register (Address = 0x4D) [Default = 0x00]

APB_DATA2 is shown in APB_DATA2 Register Field Descriptions.

Return to the Summary Table.

APB Data Register 2

Table 8-115. APB_DATA2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	APB_DATA2	R/W	0x0	Byte 2 of the APB Interface Data

8.6.1.66 APB_DATA3 Register (Address = 0x4E) [Default = 0x00]

APB_DATA3 is shown in APB_DATA3 Register Field Descriptions.

Return to the Summary Table.

APB Data Register 3

Table 8-116. APB_DATA3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	APB_DATA3	R/W	0x0	Byte 3 (MSB) of the APB Interface Data

8.6.1.67 BRIDGE_STS Register (Address = 0x50) [Default = 0x02]

BRIDGE_STS is shown in BRIDGE_STS Register Field Descriptions.

Return to the Summary Table.

Table 8-117. BRIDGE_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved

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Table 8-117. BRIDGE_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	RESERVED	R	0x0	Reserved
4	INIT_DONE	R	0x0	Initialization Done: Initialization sequence has completed. This step will complete after configuration complete (CFG_DONE)
3	RESERVED	R	0x0	Reserved
2	CFG_DONE	R	0x0	Configuration Complete: Indicates automatic configuration has completed. This step will complete prior to initialization complete (INIT_DONE).
1	CFG_CKSUM	R	0x1	Configuration checksum status: Indicates result of Configuration checksum during initialization. The device verifies the 2 's complement checksum in the last 128 bytes of the EEPROM. A value of 1 indicates the checksum passed.
0	RESERVED	R	0x0	Reserved

8.6.1.68 INTERRUPT_STS Register (Address = 0x51) [Default = 0x00]

INTERRUPT_STS is shown in INTERRUPT_STS Register Field Descriptions.

Return to the Summary Table.

Interrupt Status Register - INTB Pin The information in this register is sent to the INTB pin on the upstream device. Remote interrupts must be enabled on the upstream device.

Table 8-118. INTERRUPT_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	GLOBAL_INT_P0	R	0x0	Global Interrupt This bit reads 1 if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INTB_PIN_EN bit[0] in the INTERRUPT_CTL register (address 0x52). OR's the STS bits in this register only if corresponding IE* bit is set in INTERRUPT_CTL register There are separate versions of this register for each port, mainly to differentiate between the IS_INTB_IN interrupt condition. In FPD4, each back channel can enable a separate set of interrupts (only port 0 is used for FPD3 mode).
6	IS_DP1	R	0x0	DPTX Interrupt from DP TX 1 An interrupt has occurred for DP TX 1. This interrupt will be cleared upon reading the DP_TX_ISR register for port 1.
5	IS_FPD_TX1	R	0x0	FPD TX Port 1 Interrupt An interrupt has occurred for FPD TX Port 1 either in FPD3 or FPD4 datapath. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. For FPD3 mode, see the HDCP_ICR and HDCP_ISR registers on Page 10 For FPD4 mode, see the INTR_CTL_FPD4_PORT and INTR_STS_FPD4_PORT registers on Page 8 registers 0x8C and 0x8D.
4	RESERVED	R	0x0	Reserved
3	IS_DP0	R	0x0	DPTX Interrupt from DP TX 0 An interrupt has occurred for DP TX 0. This interrupt will be cleared upon reading the DP_TX_ISR register for port 0.

Table 8-118. INTERRUPT_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	IS_FPD_TX0	R	0x0	FPD TX Port 0 Interrupt An interrupt has occurred for FPD TX Port 0 either in FPD3 or FPD4 datapath. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. For FPD3 mode, see the HDCP_ICR and HDCP_ISR registers on Page 10 For FPD4 mode, see the INTR_CTL_FPD4_PORT and INTR_STS_FPD4_PORT registers on Page 8 registers 0x8C and 0x8D.
1	IS_FPD_RX	R	0x0	FPD RX Interrupt An interrupt has occurred for FPD RX either in FPD3 or FPD4 datapath. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. See the INTR_CTL_FPD4_RX and INTR_STS_FPD4_RX registers on indirect page 18.
0	IS_LOCAL_INT_P0	RC	0x0	Local Interrupt 0: No local interrupt detected in LOCAL_INT_STS register (address 0x45) 1: An interrupt has occurred that is represented in the LOCAL_INT_STS register (address 0x45)

8.6.1.69 INTERRUPT_CTL Register (Address = 0x52) [Default = 0xFF]

INTERRUPT_CTL is shown in INTERRUPT_CTL Register Field Descriptions.

Return to the Summary Table.

Table 8-119. INTERRUPT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	IE_GLOBAL_P0	R/W	0x1	Global Interrupt Enable 0: Interrupts disabled 1: Interrupts enabled
6	IE_DP1_P0	R/W	0x1	Display Port 1 Interrupt 0: Interrupt disabled 1: Interrupt enabled
5	IE_FPD_TX1_P0	R/W	0x1	FPD TX Port 1 Interrupt 0: Interrupt disabled 1: Interrupt enabled
4	RESERVED	R/W	0x1	Reserved
3	IE_DP0_P0	R/W	0x1	Display Port 0 Interrupt 0: Interrupt disabled 1: Interrupt enabled
2	IE_FPD_TX0_P0	R/W	0x1	FPD TX Port 0 Interrupt 0: Interrupt disabled 1: Interrupt enabled
1	IE_FPD_RX_P0	R/W	0x1	FPD RX Interrupt 0: Interrupt disabled 1: Interrupt enabled
0	IE_INTB_IN_P0	R/W	0x1	INTB Interrupt Enable Enable interrupt from the INTB_IN Input Pin or on a remote interrupt signal from a downstream FPD link. The events that can be signaled on this interrupt are controlled by the INTB_ICR_P0/P1 registers on Main Registers 2 (Indirect Page 1). 0: Interrupt disabled 1: Interrupt enabled

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8.6.1.70 GENERAL_PURPOSE_STATUS_0 Register (Address = 0x53) [Default = 0x00]

GENERAL_PURPOSE_STATUS_0 is shown in GENERAL_PURPOSE_STATUS_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-120. GENERAL_PURPOSE_STATUS_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FPD_DECODE_ERROR_P0	RC	0x0	FPD-Link Receiver Physical Layer Error Detected for selected port. It is combination of DCA alignment and 8b10b live error (NOT accumulated). In FPD4 mode, it also includes DCA CRC error. 0: No errors detected 1: Error is detected. This status is cleared on read of this register.
6	DAISY_RX_LOCK_DET_P0	R	0x0	Daisy chain RX Lock detect for selected port: This bit indicates current daisy chain remote receiver Lock Detect status for the selected port. This value is returned as part of the back channel information from the daisy chained deserializer.
5	DAISY_BC_LINK_LOST_FLAG_P0	R	0x0	Daisy chain back channel link lost flag for selected port This bit indicate whether the backchannel is the lost at least once after the backchannel link is detected.
4	FPD_LOCK_LOST_FLAG_P0	RC	0x0	Lock lost flag for FPD3 or FPD4 FC for the selected port. This status is cleared on read of this register.
3	RESERVED	R	0x0	
2	FPDTX_PLL_LOCK_P0	R	0x0	FPD Daisy Chain PLL Port Lock Status 0: Not locked 1: Receiver locked
1	FPD3RX_LOCK_P0	R	0x0	FPD3 Main Link Receiver Lock Status 0: Not locked 1: Receiver locked
0	FPD4RX_LOCK_P0	R	0x0	FPD4 Main Link Receiver Lock Status 0: Not locked 1: Receiver locked

8.6.1.71 GENERAL_PURPOSE_STATUS_1 Register (Address = 0x54) [Default = 0x00]

GENERAL_PURPOSE_STATUS_1 is shown in GENERAL_PURPOSE_STATUS_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-121. GENERAL_PURPOSE_STATUS_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FPD_PLL_LOCK	R	0x0	Main Link Receiver PLL Lock Status 0: Not locked 1: Locked
5	DUAL_TX_STS	R	0x0	Transmitter Dual Link Status: This bit indicates the current operating mode of the FPD-Link Transmit port for a daisy chain link. 0: Single-link mode active 1: Dual-link mode active
4	DUAL_RX_STS	R	0x0	Receiver Dual Link Status: This bit indicates the current operating mode of the FPD-Link Receive port for a main link. 0: Single-link mode active 1: Dual-link mode active
3	RESERVED	R	0x0	Reserved

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Table 8-121. GENERAL_PURPOSE_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	LOCK_STS_CHG	RC	0x0	FPD Main Link Lock Status Change 0: No change detected 1: Indicates lock status changed for FPD3/4 RX lock (either high to low or low to high)
1	SIGNAL_DETECT	R	0x0	0: No valid FPD-Link frame detected 1: Valid FPD-Link frame detected
0	LOCK	R	0x0	OR of Port 0 and Port 1 FPD3/4 RX Main Link Lock

8.6.1.72 FC_POWERDOWN_CTL Register (Address = 0x68) [Default = 0x00]

FC_POWERDOWN_CTL is shown in FC_POWERDOWN_CTL Register Field Descriptions.

Return to the Summary Table.

Table 8-122. FC_POWERDOWN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	PD_FCTX	R/W	0x0	FC Daisy Chain Transmitter Power Down Override This bit must be enabled by bit 2. 0: Don't power down FC transmitter 1: Power down FC transmitter
2	PD_FCTX_OV	R/W	0x0	FC Daisy Chain Transmitter Power Down Override Enable 0: PD_FCTX functionality disabled 1: PD_FCTX functionality enabled
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.1.73 CRC_ERROR0_BC Register (Address = 0x6C) [Default = 0x00]

CRC_ERROR0_BC is shown in CRC_ERROR0_BC Register Field Descriptions.

Return to the Summary Table.

Table 8-123. CRC_ERROR0_BC Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR[7:0]	R	0x0	Number of Backward Channel CRC Errors Lower Byte (8 least significant bits) This register is cleared using the CRC_ERROR_RESET bit in register 0x05[5]. Bit[5] is NOT self-clearing.

8.6.1.74 CRC_ERROR1_BC Register (Address = 0x6D) [Default = 0x00]

CRC_ERROR1_BC is shown in CRC_ERROR1_BC Register Field Descriptions.

Return to the Summary Table.

Table 8-124. CRC_ERROR1_BC Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR[15:8]	R	0x0	Number of Backward Channel CRC Errors Upper Byte (8 most significant bits) This register is cleared using the CRC_ERROR_RESET bit in register 0x05[5]. Bit[5] is NOT self-clearing.

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8.6.1.75 BIST_BC_ERRORS Register (Address = 0x6E) [Default = 0x00]

BIST_BC_ERRORS is shown in BIST_BC_ERRORS Register Field Descriptions.

Return to the Summary Table.

Table 8-125. BIST_BC_ERRORS Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BIST_BC_ERROR_COUNT	R	0x0	BIST Error count for Daisy Chain Link Back Channel for both FPD3 and FPD4 This register is cleared using the CRC_ERROR_RESET bit in register 0x05[5]. Bit[5] is NOT self-clearing. This will also clear when BIST is started.

8.6.1.76 RX_BCC_TEST Register (Address = 0x6F) [Default = 0x00]

RX_BCC_TEST is shown in RX_BCC_TEST Register Field Descriptions.

Return to the Summary Table.

Table 8-126. RX_BCC_TEST Register Field Descriptions

Bit	Field	Type	Default	Description
7	RX_FORCE_BCC_ERROR_P0	RH/W1S	0x0	Force Error on Main Link Back Channel BCC Frame Setting this bit will cause an error to be forced on an RX channel (main link) BCC frame. The RX_BCC_ERROR_SEL [6:3] and RX_BCC_ERROR_FRAME_SEL [2:0] fields in this register determine the type of error to be forced and which frame will include the error. This bit is self-clearing and will always return 0.

Table 8-126. RX_BCC_TEST Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:3	RX_BCC_ERROR_SEL_P0	R/W	0x0	RX BCC Error Select The RX BCC Error Select determines which type of error is forced on an RX (main link) channel BCC frame. --FPD4 mode-- In FPD4 mode, each I2C transaction takes 4 Back Channel Frames, called subFrames and these are sending source_id (subFrame1), destination_id(subFrame2), sequence_number(subFrame3), and i2c_data_cmd(subFrame4), respectively of an I2C transaction. Each subFrame has 2 bytes of control and 1 byte of data. 0000: No error 0001: Reserved 0010: Reserved 0011: CRC Error on normal frame following BCC frame occurs once Serializer is waiting for response (GPIO only frame) 0100: Force CRC error on 1st subFrame 0101: Force CRC error on 2nd subFrame 0110: Force CRC error on 3rd subFrame 0111: Force CRC error on 4th subFrame 1000: Force Data error on 1st subFrame (random bit 1 through 7) 1001: Force Data error on 2nd subFrame (random bit 1 through 7) 1010: Force Data error on 3rd subFrame (random bit 1 through 7) 1011: Force Data error on 4th subFrame (random bit 1 through 7) 1100: Force Data error on 1st subFrame (bit0) 1101: Force Data error on 2nd subFrame (bit0) 1110: Force Data error on 3rd subFrame (bit0) 1111: Force Data error on 4th subFrame (bit0) 2) FPD3 mode - 30-bit frames with 8 bits of I2C data where the error can be injected 0000: No error 0001: Reserved 0010: Reserved 0011: CRC Error on normal frame following BCC frame occurs once Serializer is waiting for response (GPIO only frame) 0100: Force CRC error on I2C frame 0101: Reserved 0110: Reserved 0111: Reserved 1000: Force Data error on I2C frame bit 0 1001: Force Data error on I2C frame bit 1 1010: Force Data error on I2C frame bit 2 1011: Force Data error on I2C frame bit 3 1100: Force Data error on I2C frame bit 4 1101: Force Data error on I2C frame bit 5 1110: Force Data error on I2C frame bit 6 1111: Force Data error on I2C frame bit 7
2:0	RX_BCC_ERROR_FRAME_SEL_P0	R/W	0x0	RX BCC Frame Select The RX BCC Frame Select allows selection of the RX channel BCC frame which will include the error condition selected in the force control bits of this register. BCC transfers are sent in bytes for each block transferred. This value may be set in range of 0 to 7 to force an error on any of the first 8 bytes sent on the RX BCC forward channel.

8.6.1.77 TARGET_ID0 Register (Address = 0x70) [Default = 0x00]

TARGET_ID0 is shown in TARGET_ID0 Register Field Descriptions.

Return to the Summary Table.

Remote Target ID Register 0 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

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Table 8-127. TARGET_ID0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID0	R/W	0x0	7-bit Remote Target Device ID 0 Configures the physical I2C address of the remote I2C Target device attached to the remote partner device. If an I2C transaction is addressed to the Target Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel.
0	DEST_PKT_RXDIR_ID0	R/W	0x0	Target Packet Direction In FPD4 mode, this bit configures any I2C transaction to either go upstream or downstream. In FPD3 mode, this bit should always be 0. 0: Packet is transmitted upstream, across the main link. 1: Packet is transmitted downstream, across the daisy chain link.

8.6.1.78 TARGET_ID1 Register (Address = 0x71) [Default = 0x00]

TARGET_ID1 is shown in TARGET_ID1 Register Field Descriptions.

Return to the Summary Table.

Remote Target ID Register 1 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-128. TARGET_ID1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID1	R/W	0x0	7-bit Remote Target Device ID 1 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID1	R/W	0x0	In a De-Serializer with daisy chain support, this bit configures any I2C transaction to either go upstream or downstream. When 1, the transaction is directed to the RX side as in a CAMERA mode. This bit is grouped with ID0.

8.6.1.79 TARGET_ID2 Register (Address = 0x72) [Default = 0x00]

TARGET_ID2 is shown in TARGET_ID2 Register Field Descriptions.

Return to the Summary Table.

Remote Target ID Register 2 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-129. TARGET_ID2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID2	R/W	0x0	7-bit Remote Target Device ID 2 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID2	R/W	0x0	In a De-Serializer with daisy chain support, this bit configures any I2C transaction to either go upstream or downstream. When 1, the transaction is directed to the RX side as in a CAMERA mode. This bit is grouped with ID0.

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8.6.1.80 TARGET_ID3 Register (Address = 0x73) [Default = 0x00]

TARGET_ID3 is shown in TARGET_ID3 Register Field Descriptions.

Return to the Summary Table.

Remote Target ID Register 3 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-130. TARGET_ID3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID3	R/W	0x0	7-bit Remote Target Device ID 3 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID3	R/W	0x0	In a De-Serializer with daisy chain support, this bit configures any I2C transaction to either go upstream or downstream. When 1, the transaction is directed to the RX side as in a CAMERA mode. This bit is grouped with ID0.

8.6.1.81 TARGET_ID4 Register (Address = 0x74) [Default = 0x00]

TARGET_ID4 is shown in TARGET_ID4 Register Field Descriptions.

Return to the Summary Table.

Remote Target ID Register 4 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-131. TARGET_ID4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID4	R/W	0x0	7-bit Remote Target Device ID 4 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID4	R/W	0x0	In a De-Serializer with daisy chain support, this bit configures any I2C transaction to either go upstream or downstream. When 1, the transaction is directed to the RX side as in a CAMERA mode. This bit is grouped with ID0.

8.6.1.82 TARGET_ID5 Register (Address = 0x75) [Default = 0x00]

TARGET_ID5 is shown in TARGET_ID5 Register Field Descriptions.

Return to the Summary Table.

Remote Target ID Register 5 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-132. TARGET_ID5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID5	R/W	0x0	7-bit Remote Target Device ID 5 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.

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Table 8-132. TARGET_ID5 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	DEST_PKT_RXDIR_ID5	R/W	0x0	In a De-Serializer with daisy chain support, this bit configures any I2C transaction to either go upstream or downstream. When 1, the transaction is directed to the RX side as in a CAMERA mode. This bit is grouped with ID0.

8.6.1.83 TARGET_ID6 Register (Address = 0x76) [Default = 0x00]

TARGET_ID6 is shown in TARGET_ID6 Register Field Descriptions.

Return to the Summary Table.

Remote Target ID Register 6 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-133. TARGET_ID6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID6	R/W	0x0	7-bit Remote Target Device ID 6 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID6	R/W	0x0	In a De-Serializer with daisy chain support, this bit configures any I2C transaction to either go upstream or downstream. When 1, the transaction is directed to the RX side as in a CAMERA mode. This bit is grouped with ID0.

8.6.1.84 TARGET_ID7 Register (Address = 0x77) [Default = 0x00]

TARGET_ID7 is shown in TARGET_ID7 Register Field Descriptions.

Return to the Summary Table.

Remote Target ID Register 7 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-134. TARGET_ID7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID7	R/W	0x0	7-bit Remote Target Device ID 7 Configures the physical I2C address of the remote I2C Target device attached to the remote Deserializer. If an I2C transaction is addressed to the Target Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
0	DEST_PKT_RXDIR_ID7	R/W	0x0	In a De-Serializer with daisy chain support, this bit configures any I2C transaction to either go upstream or downstream. When 1, the transaction is directed to the RX side as in a CAMERA mode. This bit is grouped with ID0.

8.6.1.85 TARGET_ALIAS0 Register (Address = 0x78) [Default = 0x00]

TARGET_ALIAS0 is shown in TARGET_ALIAS0 Register Field Descriptions.

Return to the Summary Table.

Remote Target Alias register 0 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-135. TARGET_ALIAS0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID0	R/W	0x0	7-bit Remote Target Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID0	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

8.6.1.86 TARGET_ALIAS1 Register (Address = 0x79) [Default = 0x00]

TARGET_ALIAS1 is shown in TARGET_ALIAS1 Register Field Descriptions.

Return to the Summary Table.

Remove Target Alias register 1 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-136. TARGET_ALIAS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID1	R/W	0x0	7-bit Remote Target Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID1 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID1	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

8.6.1.87 TARGET_ALIAS2 Register (Address = 0x7A) [Default = 0x00]

TARGET_ALIAS2 is shown in TARGET_ALIAS2 Register Field Descriptions.

Return to the Summary Table.

Remote Target Alias register 2 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-137. TARGET_ALIAS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID2	R/W	0x0	7-bit Remote Target Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID2 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID2	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

8.6.1.88 TARGET_ALIAS3 Register (Address = 0x7B) [Default = 0x00]

TARGET_ALIAS3 is shown in TARGET_ALIAS3 Register Field Descriptions.

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Remote Target Alias register 3 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-138. TARGET_ALIAS3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID3	R/W	0x0	7-bit Remote Target Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID3 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID3	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

8.6.1.89 TARGET_ALIAS4 Register (Address = 0x7C) [Default = 0x00]

TARGET_ALIAS4 is shown in TARGET_ALIAS4 Register Field Descriptions.

Return to the Summary Table.

Remote Target Alias register 4 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-139. TARGET_ALIAS4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID4	R/W	0x0	7-bit Remote Target Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID4 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID4	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

8.6.1.90 TARGET_ALIAS5 Register (Address = 0x7D) [Default = 0x00]

TARGET_ALIAS5 is shown in TARGET_ALIAS5 Register Field Descriptions.

Return to the Summary Table.

Remote Target Alias register 5 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-140. TARGET_ALIAS5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID5	R/W	0x0	7-bit Remote Target Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID5 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID5	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

8.6.1.91 TARGET_ALIAS6 Register (Address = 0x7E) [Default = 0x00]

TARGET_ALIAS6 is shown in TARGET_ALIAS6 Register Field Descriptions.

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Return to the Summary Table.

Remote Target Alias register 6 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-141. TARGET_ALIAS6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID6	R/W	0x0	7-bit Remote Target Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID6 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID6	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

8.6.1.92 TARGET_ALIAS7 Register (Address = 0x7F) [Default = 0x00]

TARGET_ALIAS7 is shown in TARGET_ALIAS7 Register Field Descriptions.

Return to the Summary Table.

Remote Target Alias register 7 Each I2C Target maintains it's own copy of this register. This register cannot be accessed remotely over the Bidirectional Control Channel.

Table 8-142. TARGET_ALIAS7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID7	R/W	0x0	7-bit Remote Target Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID7 register. A value of 0 in this field disables access to the remote I2C Target.
0	LCL_PORTSEL_ID7	R/W	0x0	In a daisy chain I2C transaction, this bit directs the transaction to either take port 0 or port 1 of the local FPD link to hop to the next device (Serializer or Deserializer), This bit is grouped with ID0.

8.6.1.93 DESTINATION_FIELD0 Register (Address = 0x80) [Default = 0x00]

DESTINATION_FIELD0 is shown in DESTINATION_FIELD0 Register Field Descriptions.

Return to the Summary Table.

The following register only needs to be programmed is the I2C Controller is connected to the local deserializer. They do not need to be programmed if the I2C Controller is connected to an upstream or downstream device.

Table 8-143. DESTINATION_FIELD0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination Address 000: I2C Target 0 001: I2C Target 1 010 - 111: Reserved
4	FIRST_DC_PSEL	R/W	0x0	First Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 3 only to select the port taken on the first daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1

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Table 8-143. DESTINATION_FIELD0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	MID_DC_PSEL	R/W	0x0	Middle Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 2 to select the port for the first daisy chain link or for daisy chain lengths of 3 to select the port for the second daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 1, 2 or 3 to select the port for the final daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining Depth to the Destination These bits will determine which deserializer in the daisy chain the current device is. 00: 0 remaining depth (i.e. This is the last deserializer of the daisy chain link) 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth (i.e. This is the first deserializer of a daisy chain link with 4 deserializers total).

8.6.1.94 DESTINATION_FIELD1 Register (Address = 0x81) [Default = 0x00]

DESTINATION_FIELD1 is shown in DESTINATION_FIELD1 Register Field Descriptions.

Return to the Summary Table.

The following register only needs to be programmed is the I2C Controller is connected to the local deserializer. They do not need to be programmed if the I2C Controller is connected to an upstream or downstream device.

Table 8-144. DESTINATION_FIELD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination Address 000: I2C Target 0 001: I2C Target 1 010 - 111: Reserved
4	FIRST_DC_PSEL	R/W	0x0	First Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 3 only to select the port taken on the first daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 2 to select the port for the first daisy chain link or for daisy chain lengths of 3 to select the port for the second daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 1, 2 or 3 to select the port for the final daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1

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Table 8-144. DESTINATION_FIELD1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	REMAINING_DEPTH	R/W	0x0	Remaining Depth to the Destination These bits will determine which deserializer in the daisy chain the current device is. 00: 0 remaining depth (i.e. This is the last deserializer of the daisy chain link) 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth (i.e. This is the first deserializer of a daisy chain link with 4 deserializers total).

8.6.1.95 DESTINATION_FIELD2 Register (Address = 0x82) [Default = 0x00]

DESTINATION_FIELD2 is shown in DESTINATION_FIELD2 Register Field Descriptions.

Return to the Summary Table.

The following register only needs to be programmed is the I2C Controller is connected to the local deserializer. They do not need to be programmed if the I2C Controller is connected to an upstream or downstream device.

Table 8-145. DESTINATION_FIELD2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination Address 000: I2C Target 0 001: I2C Target 1 010 - 111: Reserved
4	FIRST_DC_PSEL	R/W	0x0	First Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 3 only to select the port taken on the first daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 2 to select the port for the first daisy chain link or for daisy chain lengths of 3 to select the port for the second daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 1, 2 or 3 to select the port for the final daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining Depth to the Destination These bits will determine which deserializer in the daisy chain the current device is. 00: 0 remaining depth (i.e. This is the last deserializer of the daisy chain link) 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth (i.e. This is the first deserializer of a daisy chain link with 4 deserializers total).

8.6.1.96 DESTINATION_FIELD3 Register (Address = 0x83) [Default = 0x00]

DESTINATION_FIELD3 is shown in DESTINATION_FIELD3 Register Field Descriptions.

Return to the Summary Table.

The following register only needs to be programmed is the I2C Controller is connected to the local deserializer. They do not need to be programmed if the I2C Controller is connected to an upstream or downstream device.

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Table 8-146. DESTINATION_FIELD3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination Address 000: I2C Target 0 001: I2C Target 1 010 - 111: Reserved
4	FIRST_DC_PSEL	R/W	0x0	First Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 3 only to select the port taken on the first daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 2 to select the port for the first daisy chain link or for daisy chain lengths of 3 to select the port for the second daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 1, 2 or 3 to select the port for the final daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining Depth to the Destination These bits will determine which deserializer in the daisy chain the current device is. 00: 0 remaining depth (i.e. This is the last deserializer of the daisy chain link) 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth (i.e. This is the first deserializer of a daisy chain link with 4 deserializers total).

8.6.1.97 DESTINATION_FIELD4 Register (Address = 0x84) [Default = 0x00]

DESTINATION_FIELD4 is shown in DESTINATION_FIELD4 Register Field Descriptions.

Return to the Summary Table.

The following register only needs to be programmed is the I2C Controller is connected to the local deserializer. They do not need to be programmed if the I2C Controller is connected to an upstream or downstream device.

Table 8-147. DESTINATION_FIELD4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination Address 000: I2C Target 0 001: I2C Target 1 010 - 111: Reserved
4	FIRST_DC_PSEL	R/W	0x0	First Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 3 only to select the port taken on the first daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 2 to select the port for the first daisy chain link or for daisy chain lengths of 3 to select the port for the second daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1

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Table 8-147. DESTINATION_FIELD4 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	FINAL_DC_PSEL	R/W	0x0	Final Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 1, 2 or 3 to select the port for the final daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining Depth to the Destination These bits will determine which deserializer in the daisy chain the current device is. 00: 0 remaining depth (i.e. This is the last deserializer of the daisy chain link) 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth (i.e. This is the first deserializer of a daisy chain link with 4 deserializers total).

8.6.1.98 DESTINATION_FIELD5 Register (Address = 0x85) [Default = 0x00]

DESTINATION_FIELD5 is shown in DESTINATION_FIELD5 Register Field Descriptions.

Return to the Summary Table.

The following register only needs to be programmed is the I2C Controller is connected to the local deserializer. They do not need to be programmed if the I2C Controller is connected to an upstream or downstream device.

Table 8-148. DESTINATION_FIELD5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination Address 000: I2C Target 0 001: I2C Target 1 010 - 111: Reserved
4	FIRST_DC_PSEL	R/W	0x0	First Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 3 only to select the port taken on the first daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 2 to select the port for the first daisy chain link or for daisy chain lengths of 3 to select the port for the second daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 1, 2 or 3 to select the port for the final daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining Depth to the Destination These bits will determine which deserializer in the daisy chain the current device is. 00: 0 remaining depth (i.e. This is the last deserializer of the daisy chain link) 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth (i.e. This is the first deserializer of a daisy chain link with 4 deserializers total).

8.6.1.99 DESTINATION_FIELD6 Register (Address = 0x86) [Default = 0x00]

DESTINATION_FIELD6 is shown in DESTINATION_FIELD6 Register Field Descriptions.

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Return to the Summary Table.

The following register only needs to be programmed is the I2C Controller is connected to the local deserializer. They do not need to be programmed if the I2C Controller is connected to an upstream or downstream device.

Table 8-149. DESTINATION_FIELD6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination Address 000: I2C Target 0 001: I2C Target 1 010 - 111: Reserved
4	FIRST_DC_PSEL	R/W	0x0	First Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 3 only to select the port taken on the first daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 2 to select the port for the first daisy chain link or for daisy chain lengths of 3 to select the port for the second daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
2	FINAL_DC_PSEL	R/W	0x0	Final Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 1, 2 or 3 to select the port for the final daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining Depth to the Destination These bits will determine which deserializer in the daisy chain the current device is. 00: 0 remaining depth (i.e. This is the last deserializer of the daisy chain link) 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth (i.e. This is the first deserializer of a daisy chain link with 4 deserializers total).

8.6.1.100 DESTINATION_FIELD7 Register (Address = 0x87) [Default = 0x00]

DESTINATION_FIELD7 is shown in DESTINATION_FIELD7 Register Field Descriptions.

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The following register only needs to be programmed is the I2C Controller is connected to the local deserializer. They do not need to be programmed if the I2C Controller is connected to an upstream or downstream device.

Table 8-150. DESTINATION_FIELD7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	DEST_ADDR	R/W	0x0	Destination Address 000: I2C Target 0 001: I2C Target 1 010 - 111: Reserved
4	FIRST_DC_PSEL	R/W	0x0	First Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 3 only to select the port taken on the first daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
3	MID_DC_PSEL	R/W	0x0	Middle Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 2 to select the port for the first daisy chain link or for daisy chain lengths of 3 to select the port for the second daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1

Table 8-150. DESTINATION_FIELD7 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	FINAL_DC_PSEL	R/W	0x0	Final Daisy Chain Port Routing Selection This bit is used for daisy chain lengths of 1, 2 or 3 to select the port for the final daisy chain link. 0: BCC commands route through Port 0 1: BCC commands route through Port 1
1:0	REMAINING_DEPTH	R/W	0x0	Remaining Depth to the Destination These bits will determine which deserializer in the daisy chain the current device is. 00: 0 remaining depth (i.e. This is the last deserializer of the daisy chain link) 01: 1 remaining depth 10: 2 remaining depth 11: 3 remaining depth (i.e. This is the first deserializer of a daisy chain link with 4 deserializers total).

8.6.1.101 BC_PROCESSING_CFG Register (Address = 0x90) [Default = X]

BC_PROCESSING_CFG is shown in BC_PROCESSING_CFG Register Field Descriptions.

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Table 8-151. BC_PROCESSING_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	BC_DOWNSAMPLING_RATE_P0	R/W	X	Back channel down sampling rate 2'b00: downsample by 1 2'b01: downsample by 2 2'b10: downsample by 4 2'b11: downsample by 8 The default value for this control is strapped at power-up based on the MODE_SEL0 and MODE_SEL1 pins.
5	RESERVED	R/W	0x0	Reserved
4:0	RESERVED	R/W	0x2	Reserved

8.6.1.102 DATAPATH_BC Register (Address = 0x91) [Default = X]

DATAPATH_BC is shown in DATAPATH_BC Register Field Descriptions.

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Table 8-152. DATAPATH_BC Register Field Descriptions

Bit	Field	Type	Default	Description
7	DIS_MANCHESTER_P0	R/W	0x1	Backchannel Manchester Data Mode for FPD4 Disable 0: Manchester (binary phase-shift key) enabled 1: NRZ type back channel data (8B10B)
6	RESERVED	R/W	0x0	Reserved
5	ENH_BC_CHK_EN	R/W	0x0	Enable Back Channel Enhanced Check This bit enables the following enhanced back channel checks: Creates a valid_k_code_err_bc: if a valid k-code is used but it is not the 28.5 code Creates a invalid_code_err_bc: if there is a code violation within the 8b10b decode Creates a disparity_err_bc: if there is a running disparity error in the 8b10b decode
4	RESERVED	R/W	0x0	RESERVED

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Table 8-152. DATAPATH_BC Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	BC_FRACTIONAL_DOWNSAMPLE_EN	R/W	X	Fractional Downsampling Rate Enable This control should be set to 1 for FPD4 10.8 Gbps data rate. Otherwise it should be set to 0. The default value for this control is strapped at power-up based on the MODE_SEL0 and MODE_SEL1 pins.
2	WAIT_2_FRAMES_P0	R/W	0x0	Wait 2 frames This bit will cause the back channel to wait for 2 frames with valid k-codes before it locks
1:0	BC_FRACTIONAL_DOWNSAMPLING[1:0]	R/W	X	Back channel fractional downsampling rate[1:0]: 2'b00: 10/6 (Default if FPD3 mode or not 10.8 Gbps strap) 2'b01: 10/7 2'b10: 10/8 (Default for FPD4 10.8 Gbps strap) 2'b11: 10/9 The default value for this control is strapped at power-up based on the MODE_SEL0 and MODE_SEL1 pins.

8.6.1.103 FC_BCC_TEST Register (Address = 0x93) [Default = 0x00]

FC_BCC_TEST is shown in FC_BCC_TEST Register Field Descriptions.

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Table 8-153. FC_BCC_TEST Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	FORCE_BCC_ERROR_P0	RH/W1S	0x0	Force an Error on Forward Channel BCC Frame Setting this bit will cause an error to be forced on a forward channel BCC frame. The BCC_ERROR_SEL and BCC_FRAME_SEL fields in this register determine the type of error to be forced and which frame will include the error. This bit is self-clearing and will always return 0.
5:3	BCC_ERROR_SEL_P0	R/W	0x0	BCC Error Select The BCC Error Select determines which type of error is forced on a forward channel BCC frame. 000: No error 001: Force CRC Error 010: Force Sequence Error (skips one sequence number) 011: Drop BCC Frame (results in sequence error at downstream deserializer) 100: Force error on Data field (random bit 1 through 7) 101: Force error on Data field, bit 0 (RW bit if during Start command) 110 - 111: Reserved
2:0	BCC_FRAME_SEL_P0	R/W	0x0	BCC Frame Select The BCC Frame Select allows selection of the forward channel BCC frame which will include the error condition selected in the force control bits of this register. BCC transfers are sent in bytes for each block transferred. This value may be set in range of 0 to 7 to force an error on any of the first 8 bytes sent on the BCC forward channel.

8.6.1.104 LINK_DET_TIMER Register (Address = 0x94) [Default = 0x00]

LINK_DET_TIMER is shown in LINK_DET_TIMER Register Field Descriptions.

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Table 8-154. LINK_DET_TIMER Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R/W	0x0	Reserved

Table 8-154. LINK_DET_TIMER Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2:0	LINK_DETECT_TIMER	R/W	0x0	Bidirectional Control Channel Link Detect Timer This field configures the link detection timeout period. If the timer expires without valid communication over the reverse channel, link detect will be deasserted. 000: 162 us 001: 325 us 010: 650 us 011: 1.3 ms 100: 10.25 us 101: 20.5 us 110: 41 us 111: 82 us

8.6.1.105 FPD_RX_BC_TX_NCOUNTER_SEL_LSB Register (Address = 0x9B) [Default = 0x04]

FPD_RX_BC_TX_NCOUNTER_SEL_LSB is shown in FPD_RX_BC_TX_NCOUNTER_SEL_LSB Register Field Descriptions.

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Divider for the BC transmitter for the FPD RX link (serializer or upstream deserializer).

Table 8-155. FPD_RX_BC_TX_NCOUNTER_SEL_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_RX_BC_TX_NCOUNTER_SEL_LSB		0x4	Fractional Divider (LSB) Default for 10.8G= 8'h04 (fractional divide of 32) Default for all others= 8'h08 (fractional divide of 40) This register is strapped at power-up based on the MODE_SEL0 and MODE_SEL1 pins

8.6.1.106 FPD3_TX_DES_CAP1 Register (Address = 0xA0) [Default = 0x03]

FPD3_TX_DES_CAP1 is shown in FPD3_TX_DES_CAP1 Register Field Descriptions.

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FPD3 Deserializer Capabilities for Daisy Chain Datapath Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the downstream deserializer. If bit 7 is set, the bits become read/write rather than read-only.

Table 8-156. FPD3_TX_DES_CAP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FREEZE_DES_CAP	R/W	0x0	Freeze Deserializer Capabilities 0: Register bits 6:0 act as read only. Values will be auto-loaded from the back channel. 1: Prevent auto-loading of the Deserializer Capabilities by the Back Channel. The Capabilities will be frozen at the values written in registers 0xA0 and 0xA1.
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	DUAL_LINK_CAP	R/W	0x0	Dual link Capabilities Indicates if the local deserializer is capable of dual link operation. This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE_DES_CAP bit to prevent overwriting by the Back Channel.

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Table 8-156. FPD3_TX_DES_CAP1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	DUAL_CHANNEL	R/W	0x0	Dual Channel 0/1 Indication In a dual-link capable device, indicates if the selected port is the primary or secondary channel. The primary and secondary channels will determined which dedicated data is sent on the back channel. 0: Primary channel (channel 0) 1: Secondary channel (channel 1) This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
1	VID_24B_HD_AUD	R/W	0x1	Downstream deserializer supports 24-bit video concurrently with HD audio This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.
0	DES_CAP_FC_GPIO	R/W	0x1	Deserializer supports GPIO in the Forward Channel Frame This field is automatically configured by the Back Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Back Channel.

8.6.1.107 FPD3_TX_DES_CAP2 Register (Address = 0xA1) [Default = 0x00]

FPD3_TX_DES_CAP2 is shown in FPD3_TX_DES_CAP2 Register Field Descriptions.

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FPD3 Deserializer Capabilities for Daisy Chain Datapath This register contains the upper bits of the Deserializer Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control in the Back Channel signaling from the deserializer. If bit 7 of 0xA0 is set, the bits become read/write rather than read-only.

Table 8-157. FPD3_TX_DES_CAP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD3_DES_CAP2	R/W	0x0	FPD3 Downstream Deserializer Capabilities If 0xA0[7] is high, 0xA1 is able to be overridden. High-Speed Control Channel bit 0 Upper bits of the 3-bit HSCC indication. The lowest bit is contained in Deserializer Capabilities 1. 000: Normal back channel frame, GPIO mode 001: High Speed GPIO mode, 1 GPIO 010: High Speed GPIO mode, 2 GPIOs 011: High Speed GPIO mode: 4 GPIOs 100: Reserved 101: Reserved 110: High Speed, Forward Channel SPI mode 111: High Speed, Reverse Channel SPI mode In Single Link devices, only Normal back channel frame modes are supported.

8.6.1.108 FPD4_TX_REMOTE_PAR_CAP1 Register (Address = 0xA2) [Default = 0x00]

FPD4_TX_REMOTE_PAR_CAP1 is shown in FPD4_TX_REMOTE_PAR_CAP1 Register Field Descriptions.

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FPD4 Partner Capabilities for Daisy Chain Datapath This register contains the lower bits of the Partner Capabilities for the selected port. Typically, the values in bits 6:0 are loaded automatically via embedded control

in the Back Channel signaling from the downstream deserializer. If bit 7 is set, the bits become read/write rather than read-only.

Table 8-158. FPD4_TX_REMOTE_PAR_CAP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FREEZE_FPD4_DES_CAP	R/W	0x0	Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Back Channel. The Capabilities will be frozen at the values written in registers 0xA2 and 0xA3.
6	RESERVED	R/W	0x0	Reserved
5	BIST_EN	R/W	0x0	BIST Enable for FPD4 Daisy Chain Datapath This bit enables BIST for a daisy chain link.
4	RESERVED	R/W	0x0	Reserved
3:0	RESERVED	R/W	0x0	Reserved

8.6.1.109 FPD4_TX_REMOTE_PAR_CAP2 Register (Address = 0xA3) [Default = 0x00]

FPD4_TX_REMOTE_PAR_CAP2 is shown in FPD4_TX_REMOTE_PAR_CAP2 Register Field Descriptions.

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Table 8-159. FPD4_TX_REMOTE_PAR_CAP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DES_CAP_REG2	R/W	0x0	Contains the capabilities of the downstream deserializer. These bits are loaded from the daisy chain back channel. If 0xA0[7] is high, these bits can be overwritten Bits[7:5]: RESERVED Bit[4]: Send Enhanced CRC6 capable Bit[3]: Send HDCP RGB Checksum error Bits[2:0]: Send high speed control mode for GPIO/SPI (specified below) 000: Normal back channel frame, GPIO mode 001: High Speed GPIO mode, 1 GPIO 010: High Speed GPIO mode, 2 GPIOs 011: High Speed GPIO mode: 4 GPIOs 100: Reserved 101: Reserved 110: High Speed, Forward Channel SPI mode 111: High Speed, Reverse Channel SPI mode

8.6.1.110 FPD4_TX_DATAPATH_CTL Register (Address = 0xA4) [Default = 0x00]

FPD4_TX_DATAPATH_CTL is shown in FPD4_TX_DATAPATH_CTL Register Field Descriptions.

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Datapath Control for Daisy Chain Datapath The Datapath Control values are sent as part of the DCA sequence to the deserializer. The fields indicate capabilities and operational modes of the forward channel.

Table 8-160. FPD4_TX_DATAPATH_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	FPD4_I2SB_FC_EN_P0	R/W	0x0	If FPD4 Audio uses forward channel GPIO, this bit enables 4-channel audio using FC_GPIO[3]. This is a per port register, meaning that the value in register 0xE PORT_SEL will allow this register to return different responses associated with the respective FPD Port.

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Table 8-160. FPD4_TX_DATAPATH_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:4	FPD4_I2S_TRANSPORT	R/W	0x0	00: I2S disabled over FPD4 link 01: I2S audio is sent over the forward channel as GPIO data. 10: I2S over data island for FPD4 stream 1 data 11: I2S over data island for FPD4 stream 0 data When PORT_SEL= 0, this applies to port 0. When PORT_SEL= 1, this applies to port 1.
3	FPD4_VIDEO_DISABLE	R/W	0x0	If this bit is set, it disables video on paired deserializer
2	FPD4_DUAL_EN	R/W	0x0	This bit determines if FPD4 is operating with a dual link. This bit is ignored if the FPD4_RX_CFG register (address 0x31) bits[4:2] (FPD4_INPUT_MODE) do not equal 0. When 0x31[4:2]= 0, the device is in auto-detect mode and this bit applies. This bit must be set for the device to auto-detect and configure into dual link mode. 0: FPD4 is not configured as a dual link 1: FPD4 configured as dual link
1:0	REG_GPIOEN_FC_P0	R/W	0x0	FPD4 Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: 1 GPIO 10: 2 GPIOs 11: 4 GPIOs

8.6.1.111 FPD4_TX_DATAPATH_CTL2 Register (Address = 0xA5) [Default = 0x00]

FPD4_TX_DATAPATH_CTL2 is shown in FPD4_TX_DATAPATH_CTL2 Register Field Descriptions.

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Datapath Control Register 2 for serializer datapath (TX) If FREEZE_FPD4_DES_CAP (bit[7]) in register 0xA2 is set, this entire register is a Read Only register and auto loads values from the back channel. If FREEZE_FPD4_DES_CAP (bit[7]) in register 0xA2 is cleared, this entire register is a Read/Write register. The Datapath Control values are sent as part of the DCA sequence to the deserializer. The fields indicate capabilities and operational modes of the forward channel.

Table 8-161. FPD4_TX_DATAPATH_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	RESERVED
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	FC_ECC_P0	R/W	0x0	Forward Channel ECC Operation 00: No ECC present 01: 6-bit ECC 10: 7-bit ECC 11: 8-bit ECC

8.6.1.112 FPD_TX_CFG Register (Address = 0xA8) [Default = X]

FPD_TX_CFG is shown in FPD_TX_CFG Register Field Descriptions.

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Table 8-162. FPD_TX_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	CH1_PLL_REFCLK_SEL	R/W	0x0	FPD TX PLL Reference Clock 0: External oscillator clock (XO pin) 1: External reference clock (ZCLK pin)

Table 8-162. FPD_TX_CFG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	CH0_PLL_REFCLK_SEL	R/W	0x0	FPD TX PLL Reference Clock 0: External oscillator clock (XO pin) 1: External reference clock (ZCLK pin)
5:2	FPD_TX_MODE	R/W	X	FPD4 Transmit Mode Setting DISABLE_TX_FPD_PORTS (bit[1]) to 1 overrides these and disables all ports. This register is strapped at power-up based on the MODE_SEL0 and MODE_SEL1 pins. 0000: FPD3 Port 0, FPD3 Port 1 (FPD3 mode selected by FPD3_MODE_CTL_Px registers in Page8) 0011: FPD4 Port 0, FPD3 Port 1 (set FPD3_MODE_CTL_Px to forced single Port 1) 1010: FPD4 Dual 1011: Forced Single FPD4 Port0 (Port 1 disabled) 1100: FPD3 Port 0, FPD4 Port 1 (set FPD3_MODE_CTL_Px to forced single Port 0) 1110: Forced Single FPD4 Port1 (Port 0 disabled) 1111: FPD4 Independent Other configurations are unused
1	DISABLE_TX_FPD_PORTS	R/W	X	This bit overrides FPD_TX_MODE (bits[5:2] of this register) settings and is strapped at power-up based on the MODE_SEL0 and MODE_SEL1 pins. 0: Daisy chain ports available 1: All daisy-chain ports disabled
0	RESERVED	R	0x0	Reserved

8.6.1.113 FPD_TX_INVERT Register (Address = 0xA9) [Default = 0x00]

FPD_TX_INVERT is shown in FPD_TX_INVERT Register Field Descriptions.

Return to the Summary Table.

FPD4 and FPD3 Channel Inversion for Daisy Chain Link (TX)

Table 8-163. FPD_TX_INVERT Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R/W	0x0	Reserved
1	FPDTX_CH1_INV	R/W	0x0	Invert Daisy Chain Link Channel 1 0: Not inverted (DOUT1+= Pin 39 and DOUT1-= Pin 38) 1: Inverted (DOUT1+= Pin 38 and DOUT1-= Pin 39)
0	FPDTX_CH0_INV	R/W	0x0	Invert Daisy Chain Link Channel 0 0: Not inverted (DOUT0+= Pin 43 and DOUT0-= Pin 42) 1: Inverted (DOUT0+= Pin 42 and DOUT0-= Pin 43)

8.6.1.114 PLL_REFCLK_STATUS Register (Address = 0xAB) [Default = 0x00]

PLL_REFCLK_STATUS is shown in PLL_REFCLK_STATUS Register Field Descriptions.

Return to the Summary Table.

PLL Reference Clock Status Register

Table 8-164. PLL_REFCLK_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	XO_REFCLK_VALID	R	0x0	External Oscillator Reference Clock Valid (DPTX refclk)
2	PLL_REFCLK_VALID_RX	R	0x0	FPD Main Link (RX) PLL Reference Clock Valid
1	PLL_REFCLK_VALID_TXP1	R	0x0	FPD Daisy Chain Link (TX) Port 1 PLL Reference Clock Valid

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Table 8-164. PLL_REFCLK_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	PLL_REFCLK_VALID_TXP0	R	0x0	FPD Daisy Chain Link (TX) Port 0 PLL Reference Clock Valid

8.6.1.115 PLL_REFCLK_FREQ_TXP0 Register (Address = 0xAC) [Default = 0x00]

PLL_REFCLK_FREQ_TXP0 is shown in PLL_REFCLK_FREQ_TXP0 Register Field Descriptions.

Return to the Summary Table.

Table 8-165. PLL_REFCLK_FREQ_TXP0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PLL_REFCLK_FREQ_TXP0[7:0]	R	0x0	FPD Daisy Chain Link (TX) Port 0 PLL Reference Clock Detected Frequency The value is in MHz.

8.6.1.116 PLL_REFCLK_FREQ_TXP1 Register (Address = 0xAD) [Default = 0x00]

PLL_REFCLK_FREQ_TXP1 is shown in PLL_REFCLK_FREQ_TXP1 Register Field Descriptions.

Return to the Summary Table.

Table 8-166. PLL_REFCLK_FREQ_TXP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PLL_REFCLK_FREQ_TXP1[7:0]	R	0x0	FPD Daisy Chain Link (TX) Port 1 PLL Reference Clock Detected Frequency This value is in MHz.

8.6.1.117 PLL_REFCLK_FREQ_RXP Register (Address = 0xAE) [Default = 0x00]

PLL_REFCLK_FREQ_RXP is shown in PLL_REFCLK_FREQ_RXP Register Field Descriptions.

Return to the Summary Table.

Table 8-167. PLL_REFCLK_FREQ_RXP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PLL_REFCLK_FREQ_RX[7:0]	R	0x0	FPD Main Link (RX) PLL Reference Clock Detected Frequency This value is in MHz.

8.6.1.118 XO_REFCLK_FREQ Register (Address = 0xAF) [Default = 0x00]

XO_REFCLK_FREQ is shown in XO_REFCLK_FREQ Register Field Descriptions.

Return to the Summary Table.

Table 8-168. XO_REFCLK_FREQ Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	XO_REFCLK_FREQ[7:0]	R	0x0	External Oscillator Reference Clock Detected Frequency

8.6.1.119 DISP_QUAD_PIXEL_CLK_DIV_EN Register (Address = 0xB1) [Default = 0x01]

DISP_QUAD_PIXEL_CLK_DIV_EN is shown in DISP_QUAD_PIXEL_CLK_DIV_EN Register Field Descriptions.

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Table 8-169. DISP_QUAD_PIXEL_CLK_DIV_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RESERVED	R	0x0	Reserved
0	DISP_QUAD_PIXEL_CLK_DIV_EN	R/W	0x1	Quad Pixel Clock M/N Divider Enable (per port) 0: M/N divider disabled 1: M/N divider enabled

8.6.1.120 DISP_QUAD_PIXEL_CLK_MVAL0 Register (Address = 0xB2) [Default = 0xDB]

DISP_QUAD_PIXEL_CLK_MVAL0 is shown in DISP_QUAD_PIXEL_CLK_MVAL0 Register Field Descriptions.

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Table 8-170. DISP_QUAD_PIXEL_CLK_MVAL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DISP_QUAD_PIXEL_CLK_MVAL[7:0]	R/W	0xDB	Display Quad Pixel Clock M/N Divider M Value - lower 8 bits (per port)

8.6.1.121 DISP_QUAD_PIXEL_CLK_MVAL1 Register (Address = 0xB3) [Default = 0xFD]

DISP_QUAD_PIXEL_CLK_MVAL1 is shown in DISP_QUAD_PIXEL_CLK_MVAL1 Register Field Descriptions.

Return to the Summary Table.

Table 8-171. DISP_QUAD_PIXEL_CLK_MVAL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DISP_QUAD_PIXEL_CLK_MVAL[15:8]	R/W	0xFD	Display Quad Pixel Clock M/N Divider M Value - middle 8 bits (per port)

8.6.1.122 DISP_QUAD_PIXEL_CLK_MVAL2 Register (Address = 0xB4) [Default = 0x01]

DISP_QUAD_PIXEL_CLK_MVAL2 is shown in DISP_QUAD_PIXEL_CLK_MVAL2 Register Field Descriptions.

Return to the Summary Table.

Table 8-172. DISP_QUAD_PIXEL_CLK_MVAL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DISP_QUAD_PIXEL_CLK_MVAL[23:16]	R/W	0x1	Display Quad Pixel Clock M/N Divider M Value - upper 8 bits (per port)

8.6.1.123 DISP_QUAD_PIXEL_CLK_NVAL0 Register (Address = 0xB5) [Default = 0x10]

DISP_QUAD_PIXEL_CLK_NVAL0 is shown in DISP_QUAD_PIXEL_CLK_NVAL0 Register Field Descriptions.

Return to the Summary Table.

Table 8-173. DISP_QUAD_PIXEL_CLK_NVAL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DISP_QUAD_PIXEL_CLK_NVAL[7:0]	R/W	0x10	Display Quad Pixel Clock M/N Divider N Value - lower 8 bits (per port)

8.6.1.124 DISP_QUAD_PIXEL_CLK_NVAL1 Register (Address = 0xB6) [Default = 0x5C]

DISP_QUAD_PIXEL_CLK_NVAL1 is shown in DISP_QUAD_PIXEL_CLK_NVAL1 Register Field Descriptions.

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Table 8-174. DISP_QUAD_PIXEL_CLK_NVAL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DISP_QUAD_PIXEL_CLK_NVAL[15:8]	R/W	0x5C	Display Quad Pixel Clock M/N Divider N Value - middle 8 bits (per port)

8.6.1.125 DISP_QUAD_PIXEL_CLK_NVAL2 Register (Address = 0xB7) [Default = 0x0C]

DISP_QUAD_PIXEL_CLK_NVAL2 is shown in DISP_QUAD_PIXEL_CLK_NVAL2 Register Field Descriptions.

Return to the Summary Table.

Table 8-175. DISP_QUAD_PIXEL_CLK_NVAL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DISP_QUAD_PIXEL_CLK_NVAL[23:16]	R/W	0xC	Display Quad Pixel Clock M/N Divider N Value - upper 8 bits (per port)

8.6.1.126 FPD4_BIST_ERROR_COUNT Register (Address = 0xB8) [Default = 0x00]

FPD4_BIST_ERROR_COUNT is shown in FPD4_BIST_ERROR_COUNT Register Field Descriptions.

Return to the Summary Table.

Table 8-176. FPD4_BIST_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BIST_ERROR_COUNT	R	0x0	Value of BIST Error Count for FPD4 Link

8.6.1.127 SAR_ADC_ICR_ISR Register (Address = 0xCE) [Default = 0x00]

SAR_ADC_ICR_ISR is shown in SAR_ADC_ICR_ISR Register Field Descriptions.

Return to the Summary Table.

Table 8-177. SAR_ADC_ICR_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_TEMP_SENSOR	R/W	0x0	Interrupt on Temp Sensor When enabled, an interrupt will be generated from the Temperature Sensor. Temp Sensor interrupts are controlled by interrupt registers on Indirect page 27.
5	IE_VOLT_SENSOR	R/W	0x0	Interrupt on Voltage Sensor When enabled, an interrupt will be generated from the Voltage Sensor. Voltage Sensor interrupts are controlled by interrupt registers on Indirect page 27.
4	IE_LINE_FAULT	R/W	0x0	Interrupt on Line Fault When enabled, an interrupt will be generated from the Line Fault detection circuit. Line Fault interrupts are controlled by interrupt registers on Indirect page 27.
3	RESERVED	R	0x0	Reserved
2	IS_TEMP_SENSOR	R	0x0	Interrupt on Temp Sensor A Temperature Sensor interrupt condition has been detected. Temp Sensor interrupts are controlled by interrupt registers on Indirect page 27. This interrupt condition will be cleared by reading the interrupt status registers on page 27.
1	IS_VOLT_SENSOR	R	0x0	Interrupt on Voltage Sensor A Voltage Sensor interrupt condition has been detected. Voltage Sensor interrupts are controlled by interrupt registers on Indirect page 27. This interrupt condition will be cleared by reading the interrupt status registers on page 27.

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Table 8-177. SAR_ADC_ICR_ISR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	IS_LINE_FAULT	R	0x0	Interrupt on Line Fault A Line Fault interrupt condition has been detected. Line Fault interrupts are controlled by interrupt registers on Indirect page 27. This interrupt condition will be cleared by reading the interrupt status registers on page 27.

8.6.1.128 FF_LINK_EN Register (Address = 0xD0) [Default = 0x0C]

FF_LINK_EN is shown in FF_LINK_EN Register Field Descriptions.

Return to the Summary Table.

Table 8-178. FF_LINK_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	FPD4_TO_DISPLAYPORT1_EN	R/W	0x1	FPD4 Main Link to Display Port1 0: Disabled 1: Enabled
2	FPD4_TO_DISPLAYPORT0_EN	R/W	0x1	FPD4 Main Link to Display Port0 0: Disabled 1: Enabled
1	FPD4_TO_DAISYCHAIN1_EN	R/W	0x0	FPD4 Main Link to Daisy Chain Port1 0: Disabled 1: Enabled
0	FPD4_TO_DAISYCHAIN0_EN	R/W	0x0	FPD4 Main Link to Daisy Chain Port0 0: Disabled 1: Enabled

8.6.1.129 DC_LINK_EN Register (Address = 0xD1) [Default = 0x3C]

DC_LINK_EN is shown in DC_LINK_EN Register Field Descriptions.

Return to the Summary Table.

Daisy Chain Link Enable Register

Table 8-179. DC_LINK_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5	DC_STREAM5_EN	R/W	0x1	FPD4 Received Stream to FPD4 Daisy Chain Stream 5 Enable 0: Disable 1: Enable
4	DC_STREAM4_EN	R/W	0x1	FPD4 Received Stream to FPD4 Daisy Chain Stream 4 Enable 0: Disable 1: Enable
3	DC_STREAM3_EN	R/W	0x1	FPD4 Received Stream to FPD4 Daisy Chain Stream 3 Enable 0: Disable 1: Enable
2	DC_STREAM2_EN	R/W	0x1	FPD4 Received Stream to FPD4 Daisy Chain Stream 2 Enable 0: Disable 1: Enable
1	DC_STREAM1_EN	R/W	0x0	FPD4 Received Stream to FPD4 Daisy Chain Stream 1 Enable 0: Disable 1: Enable

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Table 8-179. DC_LINK_EN Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	DC_STREAM0_EN	R/W	0x0	FPD4 Received Stream to FPD4 Daisy Chain Stream 0 Enable 0: Disable 1: Enable

8.6.1.130 DC_LINK_MAP0_MAP1 Register (Address = 0xD2) [Default = 0x08]

DC_LINK_MAP0_MAP1 is shown in DC_LINK_MAP0_MAP1 Register Field Descriptions.

Return to the Summary Table.

The daisy chain streams assigned in this register are then allocated to the proper output port in register 0x2-0x4 and 0x12-0x14 on Page 17.

Table 8-180. DC_LINK_MAP0_MAP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5:3	FPD4TOFPD4_STREAM_MAP1	R/W	0x1	Stream Mapping to FPD4 Daisy Chain Output Stream 1 This field selects which incoming stream is mapped to daisy chain stream 1. 000: Incoming Stream 0 001: Incoming Stream 1 010: Incoming Stream 2 011: Incoming Stream 3 100: Incoming Stream 4 101: Incoming Stream 5
2:0	FPD4TOFPD4_STREAM_MAP0	R/W	0x0	Stream Mapping to FPD4 Daisy Chain Output Stream 0 This field selects which incoming stream is mapped to daisy chain stream 0. 000: Incoming Stream 0 001: Incoming Stream 1 010: Incoming Stream 2 011: Incoming Stream 3 100: Incoming Stream 4 101: Incoming Stream 5

8.6.1.131 DC_LINK_MAP2_MAP3 Register (Address = 0xD3) [Default = 0x1A]

DC_LINK_MAP2_MAP3 is shown in DC_LINK_MAP2_MAP3 Register Field Descriptions.

Return to the Summary Table.

The daisy chain streams assigned in this register are then allocated to the proper output port in register 0x2-0x4 and 0x12-0x14 on Page 17.

Table 8-181. DC_LINK_MAP2_MAP3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5:3	FPD4TOFPD4_STREAM_MAP3	R/W	0x3	Stream Mapping to FPD4 Daisy Chain Output Stream 3 This field selects which incoming stream is mapped to daisy chain stream 3. 000: Incoming Stream 0 001: Incoming Stream 1 010: Incoming Stream 2 011: Incoming Stream 3 100: Incoming Stream 4 101: Incoming Stream 5

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Table 8-181. DC_LINK_MAP2_MAP3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2:0	FPD4TOFPD4_STREAM_MAP2	R/W	0x2	Stream Mapping to FPD4 Daisy Chain Output Stream 2 This field selects which incoming stream is mapped to daisy chain stream 2. 000: Incoming Stream 0 001: Incoming Stream 1 010: Incoming Stream 2 011: Incoming Stream 3 100: Incoming Stream 4 101: Incoming Stream 5

8.6.1.132 DC_LINK_MAP4_MAP5 Register (Address = 0xD4) [Default = 0x2C]

DC_LINK_MAP4_MAP5 is shown in DC_LINK_MAP4_MAP5 Register Field Descriptions.

Return to the Summary Table.

The daisy chain streams assigned in this register are then allocated to the proper output port in register 0x2-0x4 and 0x12-0x14 on Page 17.

Table 8-182. DC_LINK_MAP4_MAP5 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5:3	FPD4TOFPD4_STREAM_MAP5	R/W	0x5	Stream Mapping to FPD4 Daisy Chain Output Stream 5 This field selects which incoming stream is mapped to daisy chain stream 5. 000: Incoming Stream 0 001: Incoming Stream 1 010: Incoming Stream 2 011: Incoming Stream 3 100: Incoming Stream 4 101: Incoming Stream 5
2:0	FPD4TOFPD4_STREAM_MAP4	R/W	0x4	Stream Mapping to FPD4 Daisy Chain Output Stream 4 This field selects which incoming stream is mapped to daisy chain stream 4. 000: Incoming Stream 0 001: Incoming Stream 1 010: Incoming Stream 2 011: Incoming Stream 3 100: Incoming Stream 4 101: Incoming Stream 5

8.6.1.133 FPD4_FPD3_MAP0_MAP1 Register (Address = 0xD5) [Default = 0x08]

FPD4_FPD3_MAP0_MAP1 is shown in FPD4_FPD3_MAP0_MAP1 Register Field Descriptions.

Return to the Summary Table.

Table 8-183. FPD4_FPD3_MAP0_MAP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved

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Table 8-183. FPD4_FPD3_MAP0_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:3	REG_FPD4TOFPD3_STREAM_MAP1	R/W	0x1	Stream Mapping to FPD3 Daisy Chain Port 1 This field selects which incoming FPD4 stream is mapped to daisy chain port 1 in FPD3 output mode. 000: Incoming Stream 0 001: Incoming Stream 1 010: Incoming Stream 2 011: Incoming Stream 3 100: Incoming Stream 4 101: Incoming Stream 5
2:0	REG_FPD4TOFPD3_STREAM_MAP0	R/W	0x0	Stream Mapping to FPD3 Daisy Chain Port 0 This field selects which incoming FPD4 stream is mapped to daisy chain port 0 in FPD3 output mode. 000: Incoming Stream 0 001: Incoming Stream 1 010: Incoming Stream 2 011: Incoming Stream 3 100: Incoming Stream 4 101: Incoming Stream 5

8.6.1.134 FPD4_DISP_MAP0_MAP1 Register (Address = 0xD6) [Default = 0x08]

FPD4_DISP_MAP0_MAP1 is shown in FPD4_DISP_MAP0_MAP1 Register Field Descriptions.

Return to the Summary Table.

Table 8-184. FPD4_DISP_MAP0_MAP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5:3	REG_FPD4TODISPLAY_STREAM_MAP1	R/W	0x1	FPD4_Rx to Display Port 1 000: Stream ID 0 to Display 001: Stream ID 1 to Display 010: Stream ID 2 to Display 011: Stream ID 3 to Display 100: Stream ID 4 to Display 101: Stream ID 5 to Display
2:0	REG_FPD4TODISPLAY_STREAM_MAP0	R/W	0x0	FPD4_Rx to Display Port 0 000: Stream ID 0 to Display 001: Stream ID 1 to Display 010: Stream ID 2 to Display 011: Stream ID 3 to Display 100: Stream ID 4 to Display 101: Stream ID 5 to Display

8.6.1.135 SEL_FPD3_DISP Register (Address = 0xD7) [Default = X]

SEL_FPD3_DISP is shown in SEL_FPD3_DISP Register Field Descriptions.

Return to the Summary Table.

Table 8-185. SEL_FPD3_DISP Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	FPD3_TO_DP1_CTL	R/W	X	FPD3 Received Link to Display Port 1 Control 0: DP1 does not receive FPD3 link data 1: DP1 receives FPD3 link data This register is strapped at power-up based on the MODE_SEL0 and MODE_SEL1 pins

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Table 8-185. SEL_FPD3_DISP Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	FPD3_TO_DP0_CTL	R/W	X	FPD3 Received Link to Display Port 0 Control 0: DP0 does not receive FPD3 link data 1: DP0 receives FPD3 link data This register is strapped at power-up based on the MODE_SEL0 and MODE_SEL1 pins
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

8.6.1.136 FPD_ID0 Register (Address = 0xF0) [Default = 0x5F]

FPD_ID0 is shown in FPD_ID0 Register Field Descriptions.

Return to the Summary Table.

Table 8-186. FPD_ID0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_ID0	R	0x5F	FPD_ID0: First byte ID code, '_ '

8.6.1.137 FPD_ID1 Register (Address = 0xF1) [Default = 0x55]

FPD_ID1 is shown in FPD_ID1 Register Field Descriptions.

Return to the Summary Table.

Table 8-187. FPD_ID1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_ID1	R	0x55	FPD_ID1: 2nd byte of ID code, 'U '

8.6.1.138 FPD_ID2 Register (Address = 0xF2) [Default = 0x48]

FPD_ID2 is shown in FPD_ID2 Register Field Descriptions.

Return to the Summary Table.

Table 8-188. FPD_ID2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_ID2	R	0x48	FPD_ID2: 3rd byte of ID code. Value will be either 'B ' or 'H '. 'H ' indicates an HDCP capable device.

8.6.1.139 FPD_ID3 Register (Address = 0xF3) [Default = 0x39]

FPD_ID3 is shown in FPD_ID3 Register Field Descriptions.

Return to the Summary Table.

Table 8-189. FPD_ID3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_ID3	R	0x39	FPD_ID3: 4th byte of ID code, '9 '

8.6.1.140 FPD_ID4 Register (Address = 0xF4) [Default = 0x38]

FPD_ID4 is shown in FPD_ID4 Register Field Descriptions.

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Table 8-190. FPD_ID4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_ID4	R	0x38	FPD_ID4: 5th byte of ID code, '8'

8.6.1.141 FPD_ID5 Register (Address = 0xF5) [Default = 0x34]

FPD_ID5 is shown in FPD_ID5 Register Field Descriptions.

Return to the Summary Table.

Table 8-191. FPD_ID5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_ID5	R	0x34	FPD_ID5: 6th byte of ID code, '4' This value depends on which device we use 984/988 For 984: 0x34 For 988: 0x38

8.6.1.142 FPD_ID6 Register (Address = 0xF6) [Default = 0x30]

FPD_ID6 is shown in FPD_ID6 Register Field Descriptions.

Return to the Summary Table.

Table 8-192. FPD_ID6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_ID6	R	0x30	FPD_ID5: 6th byte of ID code, '0'

8.6.2 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map (1). Register access is provided via an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0x40- 0x42 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Write the data value to the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating Step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Read from the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating Step 3 will read additional data bytes from subsequent register offset locations.

Table 8-193. Indirect Register Map Description

IA SELECT 0x40[6:2]	PAGE/BLOCK	INDIRECT REGISTERS	DESCRIPTION
00000	0	Reserved	Reserved

Table 8-193. Indirect Register Map Description (continued)

IA SELECT 0x40[6:2]	PAGE/BLOCK	INDIRECT REGISTERS	DESCRIPTION
00001	1	Page_1: Secondary Data Control	Secondary Data Control
00010	2	Page_2: FPD RX PLL	FPD RX PLL
00011	3	Page_3: FPD TX PLL	FPD TX PLL
00100	4	Page_4: FPD RX Analog	FPD RX Analog
00101	5	Page_5: FPD RX Digital	FPD RX Digital
00110	6	Page_6: HDCP RX	HDCP RX
00111	7	Reserved	Reserved
01000	8	Page_8: FPD TX Digital	FPD-Link Digital Control
01001	9	Reserved	Reserved
01010	10	Page_10: FPD TX INT	FPD-Link III TX Interrupt
01011	11	Page_11: DP/eDP Control	DP/eDP Digital Control
0x30 01100	12	Page_12: DP/eDP PLL	DP/eDP PLL Control
01101	13	Reserved	Reserved
01110	14	Page_14: AEQ	AEQ
01111	15	Page_15: DFT and MBIST	DFT and MBIST
10000	16	Reserved	Reserved
10001	17	Page_17: FPD TX Link Layer	Link Layer Control for Daisy-chain TX
10010	18	Page_18: FPD RX Link Layer	FPD RX Link Layer
10011	19	Reserved	Reserved
0x50 10100	20	Page_20: Display Timing and Pattern Generation	DP/eDP Display Timing and Pattern Generation
10101	21	Reserved	Reserved
10110	22	Reserved	Reserved
10111	23	Page_23: LMS-AEQ Port 0 and Port 1	LMS-AEQ Port 0 and Port 1
11000	24	Reserved	Reserved
11001	25	Reserved	Reserved
11010	26	Reserved	Reserved
11011	27	Page_27: SAR ADC	SAR ADC

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8.6.2.1 Page 1: Secondary Data Control Registers

PAGE_1 Registers lists the memory-mapped registers for the Page 1: Secondary Data Control registers. All register offset addresses not listed in PAGE_1 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-194. PAGE_1 Registers

Address	Acronym	Register Name	Section
0x10	BC_GPIO_CTL0_P0	BC_GPIO_CTL0_P0	Go
0x11	BC_GPIO_CTL1_P0	BC_GPIO_CTL1_P0	Go
0x12	BC_GPIO_CTL2_P0	BC_GPIO_CTL2_P0	Go
0x13	BC_GPIO_CTL3_P0	BC_GPIO_CTL3_P0	Go
0x14	BC_GPIO_CTL4_P0	BC_GPIO_CTL4_P0	Go
0x15	BC_GPIO_CTL5_P0	BC_GPIO_CTL5_P0	Go
0x16	BC_GPIO_CTL6_P0	BC_GPIO_CTL6_P0	Go
0x17	BC_GPIO_CTL7_P0	BC_GPIO_CTL7_P0	Go
0x18	BC_GPIO_CTL8_P0	BC_GPIO_CTL8_P0	Go
0x19	BC_GPIO_CTL9_P0	BC_GPIO_CTL9_P0	Go
0x1A	BC_GPIO_CTL10_P0	BC_GPIO_CTL10_P0	Go
0x1B	BC_GPIO_CTL11_P0	BC_GPIO_CTL11_P0	Go
0x1C	BC_GPIO_CTL12_P0	BC_GPIO_CTL12_P0	Go
0x1D	BC_GPIO_CTL13_P0	BC_GPIO_CTL13_P0	Go
0x1E	BC_GPIO_CTL14_P0	BC_GPIO_CTL14_P0	Go
0x1F	BC_GPIO_CTL15_P0	BC_GPIO_CTL15_P0	Go
0x20	GPIO_GEN_CONFIG_P0	GPIO_GEN_CONFIG_P0	Go
0x31	BC_GPIO_CTL0_P1	BC_GPIO_CTL0_P1	Go
0x32	BC_GPIO_CTL1_P1	BC_GPIO_CTL1_P1	Go
0x33	BC_GPIO_CTL2_P1	BC_GPIO_CTL2_P1	Go
0x34	BC_GPIO_CTL3_P1	BC_GPIO_CTL3_P1	Go
0x35	BC_GPIO_CTL4_P1	BC_GPIO_CTL4_P1	Go
0x36	BC_GPIO_CTL5_P1	BC_GPIO_CTL5_P1	Go
0x37	BC_GPIO_CTL6_P1	BC_GPIO_CTL6_P1	Go
0x38	BC_GPIO_CTL7_P1	BC_GPIO_CTL7_P1	Go
0x39	BC_GPIO_CTL8_P1	BC_GPIO_CTL8_P1	Go
0x3A	BC_GPIO_CTL9_P1	BC_GPIO_CTL9_P1	Go
0x3B	BC_GPIO_CTL10_P1	BC_GPIO_CTL10_P1	Go
0x3C	BC_GPIO_CTL11_P1	BC_GPIO_CTL11_P1	Go
0x3D	BC_GPIO_CTL12_P1	BC_GPIO_CTL12_P1	Go
0x3E	BC_GPIO_CTL13_P1	BC_GPIO_CTL13_P1	Go
0x3F	BC_GPIO_CTL14_P1	BC_GPIO_CTL14_P1	Go
0x40	BC_GPIO_CTL15_P1	BC_GPIO_CTL15_P1	Go
0x41	GPIO_GEN_CONFIG_P1	GPIO_GEN_CONFIG_P1	Go
0x6F	PATGEN_SIMUL_CTL	PATGEN_SIMUL_CTL	Go
0x7E	INTB_ICR_P0	INTB_ICR_P0	Go
0x7F	INTB_ICR_P1	INTB_ICR_P1	Go
0x80	I2S_INT_DIV_MSB	I2S_INT_DIV_MSB	Go
0x81	I2S_INT_DIV_LSB	I2S_INT_DIV_LSB	Go
0x82	I2S_FRAC_NUM_MSB	I2S_FRAC_NUM_MSB	Go
0x83	I2S_FRAC_NUM_LSB	I2S_FRAC_NUM_LSB	Go

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Table 8-194. PAGE_1 Registers (continued)

Address	Acronym	Register Name	Section
0x84	I2S_DIV_CFG	I2S_DIV_CFG	Go
0x85	CLK_SPEEDUP_INT_ADD	CLK_SPEEDUP_INT_ADD	Go
0x86	CLK_SLOWDWN_INT_SUB	CLK_SLOWDWN_INT_SUB	Go
0x88	FIFO_1ST_HIGH	FIFO_1ST_HIGH	Go
0x89	FIFO_1ST_LOW	FIFO_1ST_LOW	Go
0x8A	FIFO_2ND_HIGH	FIFO_2ND_HIGH	Go
0x8B	FIFO_2ND_LOW	FIFO_2ND_LOW	Go
0x8C	CFG_I2S	CFG_I2S	Go
0x8D	I2S_DATA_REG	I2S_DATA_REG	Go
0x8E	I2S_FORWARD_EN	I2S_FORWARD_EN	Go
0x90	FRAC_1ST_ADD_0	FRAC_1ST_ADD_0	Go
0x91	FRAC_1ST_ADD_1	FRAC_1ST_ADD_1	Go
0x92	FRAC_2ND_ADD_0	FRAC_2ND_ADD_0	Go
0x93	FRAC_2ND_ADD_1	FRAC_2ND_ADD_1	Go
0x94	FRAC_1ST_SUB_0	FRAC_1ST_SUB_0	Go
0x95	FRAC_1ST_SUB_1	FRAC_1ST_SUB_1	Go
0x96	FRAC_2ND_SUB_0	FRAC_2ND_SUB_0	Go
0x97	FRAC_2ND_SUB_1	FRAC_2ND_SUB_1	Go
0xC0	INTB_ISR_P0	INTB_ISR_P0	Go

Complex bit access types are encoded to fit into small table cells. Page 1: Secondary Data Control Access Type Codes shows the codes that are used for access types in this section.

Table 8-195. Page 1: Secondary Data Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.1.1 BC_GPIO_CTL0_P0 Register (Address = 0x10) [Default = 0x00]

BC_GPIO_CTL0_P0 is shown in BC_GPIO_CTL0_P0 Register Field Descriptions.

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Table 8-196. BC_GPIO_CTL0_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO0_SEL	R/W	0x0	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.2 BC_GPIO_CTL1_P0 Register (Address = 0x11) [Default = 0x01]

BC_GPIO_CTL1_P0 is shown in BC_GPIO_CTL1_P0 Register Field Descriptions.

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Table 8-197. BC_GPIO_CTL1_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO1_SEL	R/W	0x1	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.3 BC_GPIO_CTL2_P0 Register (Address = 0x12) [Default = 0x02]

BC_GPIO_CTL2_P0 is shown in BC_GPIO_CTL2_P0 Register Field Descriptions.

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Table 8-198. BC_GPIO_CTL2_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO2_SEL	R/W	0x2	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.4 BC_GPIO_CTL3_P0 Register (Address = 0x13) [Default = 0x03]

BC_GPIO_CTL3_P0 is shown in BC_GPIO_CTL3_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-199. BC_GPIO_CTL3_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO3_SEL	R/W	0x3	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.5 BC_GPIO_CTL4_P0 Register (Address = 0x14) [Default = 0x04]

BC_GPIO_CTL4_P0 is shown in BC_GPIO_CTL4_P0 Register Field Descriptions.

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Table 8-200. BC_GPIO_CTL4_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO4_SEL	R/W	0x4	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.6 BC_GPIO_CTL5_P0 Register (Address = 0x15) [Default = 0x05]

BC_GPIO_CTL5_P0 is shown in BC_GPIO_CTL5_P0 Register Field Descriptions.

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Table 8-201. BC_GPIO_CTL5_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO5_SEL	R/W	0x5	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.7 BC_GPIO_CTL6_P0 Register (Address = 0x16) [Default = 0x06]

BC_GPIO_CTL6_P0 is shown in BC_GPIO_CTL6_P0 Register Field Descriptions.

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Table 8-202. BC_GPIO_CTL6_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO6_SEL	R/W	0x6	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.8 BC_GPIO_CTL7_P0 Register (Address = 0x17) [Default = 0x07]

BC_GPIO_CTL7_P0 is shown in BC_GPIO_CTL7_P0 Register Field Descriptions.

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Table 8-203. BC_GPIO_CTL7_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO7_SEL	R/W	0x7	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.9 BC_GPIO_CTL8_P0 Register (Address = 0x18) [Default = 0x08]

BC_GPIO_CTL8_P0 is shown in BC_GPIO_CTL8_P0 Register Field Descriptions.

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Table 8-204. BC_GPIO_CTL8_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO8_SEL	R/W	0x8	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.10 BC_GPIO_CTL9_P0 Register (Address = 0x19) [Default = 0x09]

BC_GPIO_CTL9_P0 is shown in BC_GPIO_CTL9_P0 Register Field Descriptions.

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Table 8-205. BC_GPIO_CTL9_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO9_SEL	R/W	0x9	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.11 BC_GPIO_CTL10_P0 Register (Address = 0x1A) [Default = 0x0A]

BC_GPIO_CTL10_P0 is shown in BC_GPIO_CTL10_P0 Register Field Descriptions.

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Table 8-206. BC_GPIO_CTL10_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO10_SEL	R/W	0xA	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.12 BC_GPIO_CTL11_P0 Register (Address = 0x1B) [Default = 0x0B]

BC_GPIO_CTL11_P0 is shown in BC_GPIO_CTL11_P0 Register Field Descriptions.

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Table 8-207. BC_GPIO_CTL11_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO11_SEL	R/W	0xB	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.13 BC_GPIO_CTL12_P0 Register (Address = 0x1C) [Default = 0x0C]

BC_GPIO_CTL12_P0 is shown in BC_GPIO_CTL12_P0 Register Field Descriptions.

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Table 8-208. BC_GPIO_CTL12_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO12_SEL	R/W	0xC	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.14 BC_GPIO_CTL13_P0 Register (Address = 0x1D) [Default = 0x0D]

BC_GPIO_CTL13_P0 is shown in BC_GPIO_CTL13_P0 Register Field Descriptions.

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Table 8-209. BC_GPIO_CTL13_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO13_SEL	R/W	0xD	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.15 BC_GPIO_CTL14_P0 Register (Address = 0x1E) [Default = 0x00]

BC_GPIO_CTL14_P0 is shown in BC_GPIO_CTL14_P0 Register Field Descriptions.

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Table 8-210. BC_GPIO_CTL14_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO14_SEL	R/W	0x0	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.16 BC_GPIO_CTL15_P0 Register (Address = 0x1F) [Default = 0x00]

BC_GPIO_CTL15_P0 is shown in BC_GPIO_CTL15_P0 Register Field Descriptions.

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Table 8-211. BC_GPIO_CTL15_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO15_SEL	R/W	0x0	Back Channel Port 0 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.17 GPIO_GEN_CONFIG_P0 Register (Address = 0x20) [Default = 0x02]

GPIO_GEN_CONFIG_P0 is shown in GPIO_GEN_CONFIG_P0 Register Field Descriptions.

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Table 8-212. GPIO_GEN_CONFIG_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	DC_FC_GPIO3_FWD	R/W	0x0	Select Daisy Chain GPIO3 Forwarding Source The GPIO3 data is sent on the Port 0 daisy chain to the downstream deserializer. The data on this GPIO can be configured at the serializer or upstream deserializer. 0: Main Link Port 0 1: Main Link Port 1
6	DC_FC_GPIO2_FWD	R/W	0x0	Select Daisy Chain GPIO2 Forwarding Source The GPIO2 data is sent on the Port 0 daisy chain to the downstream deserializer. The data on this GPIO can be configured at the serializer or upstream deserializer. 0: Main Link Port 0 1: Main Link Port 1
5	DC_FC_GPIO1_FWD	R/W	0x0	Select Daisy Chain GPIO1 Forwarding Source The GPIO1 data is sent on the Port 0 daisy chain to the downstream deserializer. The data on this GPIO can be configured at the serializer or upstream deserializer. 0: Main Link Port 0 1: Main Link Port 1
4	DC_FC_GPIO0_FWD	R/W	0x0	Select Daisy Chain GPIO0 Forwarding Source The GPIO0 data is sent on the Port 0 daisy chain to the downstream deserializer. The data on this GPIO can be configured at the serializer or upstream deserializer. 0: Main Link Port 0 1: Main Link Port 1
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1:0	BC_GPIO_NUMBER	R/W	0x2	Number of GPIOs sent over the back channel 00: 4 GPIOs 01: 8 GPIOs 10: 16 GPIOs 11: 1 GPIO

8.6.2.1.18 BC_GPIO_CTL0_P1 Register (Address = 0x31) [Default = 0x00]

BC_GPIO_CTL0_P1 is shown in BC_GPIO_CTL0_P1 Register Field Descriptions.

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Table 8-213. BC_GPIO_CTL0_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO0_SEL	R/W	0x0	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.19 BC_GPIO_CTL1_P1 Register (Address = 0x32) [Default = 0x01]

BC_GPIO_CTL1_P1 is shown in BC_GPIO_CTL1_P1 Register Field Descriptions.

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Table 8-214. BC_GPIO_CTL1_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO1_SEL	R/W	0x1	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.20 BC_GPIO_CTL2_P1 Register (Address = 0x33) [Default = 0x02]

BC_GPIO_CTL2_P1 is shown in BC_GPIO_CTL2_P1 Register Field Descriptions.

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Table 8-215. BC_GPIO_CTL2_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO2_SEL	R/W	0x2	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.21 BC_GPIO_CTL3_P1 Register (Address = 0x34) [Default = 0x03]

BC_GPIO_CTL3_P1 is shown in BC_GPIO_CTL3_P1 Register Field Descriptions.

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Table 8-216. BC_GPIO_CTL3_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO3_SEL	R/W	0x3	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.22 BC_GPIO_CTL4_P1 Register (Address = 0x35) [Default = 0x04]

BC_GPIO_CTL4_P1 is shown in BC_GPIO_CTL4_P1 Register Field Descriptions.

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Table 8-217. BC_GPIO_CTL4_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO4_SEL	R/W	0x4	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.23 BC_GPIO_CTL5_P1 Register (Address = 0x36) [Default = 0x05]

BC_GPIO_CTL5_P1 is shown in BC_GPIO_CTL5_P1 Register Field Descriptions.

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Table 8-218. BC_GPIO_CTL5_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO5_SEL	R/W	0x5	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.24 BC_GPIO_CTL6_P1 Register (Address = 0x37) [Default = 0x06]

BC_GPIO_CTL6_P1 is shown in BC_GPIO_CTL6_P1 Register Field Descriptions.

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Table 8-219. BC_GPIO_CTL6_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO6_SEL	R/W	0x6	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.25 BC_GPIO_CTL7_P1 Register (Address = 0x38) [Default = 0x07]

BC_GPIO_CTL7_P1 is shown in BC_GPIO_CTL7_P1 Register Field Descriptions.

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Table 8-220. BC_GPIO_CTL7_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO7_SEL	R/W	0x7	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.26 BC_GPIO_CTL8_P1 Register (Address = 0x39) [Default = 0x08]

BC_GPIO_CTL8_P1 is shown in BC_GPIO_CTL8_P1 Register Field Descriptions.

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Table 8-221. BC_GPIO_CTL8_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO8_SEL	R/W	0x8	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.27 BC_GPIO_CTL9_P1 Register (Address = 0x3A) [Default = 0x09]

BC_GPIO_CTL9_P1 is shown in BC_GPIO_CTL9_P1 Register Field Descriptions.

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Table 8-222. BC_GPIO_CTL9_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO9_SEL	R/W	0x9	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.28 BC_GPIO_CTL10_P1 Register (Address = 0x3B) [Default = 0x0A]

BC_GPIO_CTL10_P1 is shown in BC_GPIO_CTL10_P1 Register Field Descriptions.

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Table 8-223. BC_GPIO_CTL10_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO10_SEL	R/W	0xA	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.29 BC_GPIO_CTL11_P1 Register (Address = 0x3C) [Default = 0x0B]

BC_GPIO_CTL11_P1 is shown in BC_GPIO_CTL11_P1 Register Field Descriptions.

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Table 8-224. BC_GPIO_CTL11_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO11_SEL	R/W	0xB	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.30 BC_GPIO_CTL12_P1 Register (Address = 0x3D) [Default = 0x0C]

BC_GPIO_CTL12_P1 is shown in BC_GPIO_CTL12_P1 Register Field Descriptions.

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Table 8-225. BC_GPIO_CTL12_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO12_SEL	R/W	0xC	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.31 BC_GPIO_CTL13_P1 Register (Address = 0x3E) [Default = 0x0D]

BC_GPIO_CTL13_P1 is shown in BC_GPIO_CTL13_P1 Register Field Descriptions.

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Table 8-226. BC_GPIO_CTL13_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO13_SEL	R/W	0xD	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.32 BC_GPIO_CTL14_P1 Register (Address = 0x3F) [Default = 0x00]

BC_GPIO_CTL14_P1 is shown in BC_GPIO_CTL14_P1 Register Field Descriptions.

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Table 8-227. BC_GPIO_CTL14_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO14_SEL	R/W	0x0	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.33 BC_GPIO_CTL15_P1 Register (Address = 0x40) [Default = 0x00]

BC_GPIO_CTL15_P1 is shown in BC_GPIO_CTL15_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-228. BC_GPIO_CTL15_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BC_GPIO15_SEL	R/W	0x0	Back Channel Port 1 GPIOx Select: Determines the data sent on GPIO Slot x for the selected port back channel. 0x00 – 0x0D: Pin GPIOx 0x10: Daisy-Chain Port 0 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x11: Daisy-Chain Port 1 Received Back Channel GPIO (BC_GPIOx must be sending data for this to be valid) 0x20: Constant value of 0 0x21: Constant value of 1 0x30: SAR ADC interrupt (Reg 0xCE on main page) 0x31-0x35: Reserved 0x36: DP port 0 interrupt for HPD event (0xD9[0] on Page 11) 0x37: DP port 0 interrupt for HPD IRQ (0xD9[1] on Page 11) 0x38: DP port 0 interrupt for AUX reply received or timeout (0xD9[3:2] on Page 11) 0x39: DP port 0 SM interrupt (0xDA on Page 11) 0x3A: DP port 1 interrupt for HPD event (0xE9[0] on Page 11) 0x3B: DP port 1 interrupt for HPD IRQ (0xE9[1] on Page 11) 0x3C: DP port 1 interrupt for AUX reply received or timeout (0xE9[3:2] on Page 11) 0x3D: DP port 1 SM interrupt (0xEA on Page 11)

8.6.2.1.34 GPIO_GEN_CONFIG_P1 Register (Address = 0x41) [Default = 0x02]

GPIO_GEN_CONFIG_P1 is shown in GPIO_GEN_CONFIG_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-229. GPIO_GEN_CONFIG_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	DC_FC_GPIO3_FWD	R/W	0x0	Select Daisy Chain GPIO3 Forwarding Source The GPIO3 data is sent on the Port 1 daisy chain to the downstream deserializer. The data on this GPIO can be configured at the serializer or upstream deserializer. 0: Main Link Port 0 1: Main Link Port 1
6	DC_FC_GPIO2_FWD	R/W	0x0	Select Daisy Chain GPIO2 Forwarding Source The GPIO2 data is sent on the Port 1 daisy chain to the downstream deserializer. The data on this GPIO can be configured at the serializer or upstream deserializer. 0: Main Link Port 0 1: Main Link Port 1
5	DC_FC_GPIO1_FWD	R/W	0x0	Select Daisy Chain GPIO1 Forwarding Source The GPIO1 data is sent on the Port 1 daisy chain to the downstream deserializer. The data on this GPIO can be configured at the serializer or upstream deserializer. 0: Main Link Port 0 1: Main Link Port 1
4	DC_FC_GPIO0_FWD	R/W	0x0	Select Daisy Chain GPIO0 Forwarding Source The GPIO0 data is sent on the Port 1 daisy chain to the downstream deserializer. The data on this GPIO can be configured at the serializer or upstream deserializer. 0: Main Link Port 0 1: Main Link Port 1
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1:0	BC_GPIO_NUMBER	R/W	0x2	Number of GPIOs sent over the back channel 00: 4 GPIOs 01: 8 GPIOs 10: 16 GPIOs 11: 1 GPIO

8.6.2.1.35 PATGEN_SIMUL_CTL Register (Address = 0x6F) [Default = 0x00]

PATGEN_SIMUL_CTL is shown in PATGEN_SIMUL_CTL Register Field Descriptions.

Return to the Summary Table.

Table 8-230. PATGEN_SIMUL_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	PATGEN_SIMUL_CTL	R/W	0x0	P1 Simultaneous control Enable Setting this bit to 1 will enable simultaneous control of both P0 and P1 pattern generators. Register writes in the range of 0x00 to 0x05 will write to the equivalent registers in P1 (i.e. 0x10 to 0x15). 1: Enable Simultaneous control 0: Disable Simultaneous control

8.6.2.1.36 INTB_ICR_P0 Register (Address = 0x7E) [Default = 0x01]

INTB_ICR_P0 is shown in INTB_ICR_P0 Register Field Descriptions.

Return to the Summary Table.

INTB Interrupt Control Register for Back Channel on Main Link Port 0 The bits in this register enable the interrupt statuses for indicating INTB interrupts via the remote RX_INTN or DES_INT interrupts. When enabled,

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the selected interrupt (or interrupts) will be provided to the back channel logic for the RX_INTN and DES_INT signaling.

Table 8-231. INTB_ICR_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	IC_DES_INT_P1	R/W	0x0	Interrupt Control for DES_INT from FPD4 Daisy Chain Port 1 0: Disable 1: Enable
3	IC_DES_INT_P0	R/W	0x0	Interrupt Control for DES_INT from FPD4 Daisy Chain Port 0 0: Disable 1: Enable
2	IC_RX_INTN_P1	R/W	0x0	Interrupt Control for RX_INTN from FPD3/4 Daisy Chain Port 1 0: Disable 1: Enable
1	IC_RX_INTN_P0	R/W	0x0	Interrupt Control for RX_INTN from FPD3/4 Daisy Chain Port 0 0: Disable 1: Enable
0	IC_INTB_IN_P0	R/W	0x1	Interrupt Control for INTB_IN from Daisy Chain Device INTB_IN Pin 0: Disable 1: Enable

8.6.2.1.37 INTB_ICR_P1 Register (Address = 0x7F) [Default = 0x01]

INTB_ICR_P1 is shown in INTB_ICR_P1 Register Field Descriptions.

Return to the Summary Table.

INTB Interrupt Control Register for Back Channel on Main Link Port 1 The bits in this register enable the interrupt statuses for indicating INTB interrupts via the remote RX_INTN or DES_INT interrupts. When enabled, the selected interrupt (or interrupts) will be provided to the back channel logic for the RX_INTN and DES_INT signaling.

Table 8-232. INTB_ICR_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	IC_DES_INT_P1	R/W	0x0	Interrupt Control for DES_INT from FPD4 Daisy Chain Port 1 0: Disable 1: Enable
3	IC_DES_INT_P0	R/W	0x0	Interrupt Control for DES_INT from FPD4 Daisy Chain Port 0 0: Disable 1: Enable
2	IC_RX_INTN_P1	R/W	0x0	Interrupt Control for RX_INTN from FPD3/4 Daisy Chain Port 1 0: Disable 1: Enable
1	IC_RX_INTN_P0	R/W	0x0	Interrupt Control for RX_INTN from FPD3/4 Daisy Chain Port 0 0: Disable 1: Enable
0	IC_INTB_IN_P0	R/W	0x1	Interrupt Control for INTB_IN from Daisy Chain Device INTB_IN Pin 0: Disable 1: Enable

8.6.2.1.38 I2S_INT_DIV_MSB Register (Address = 0x80) [Default = 0x03]

I2S_INT_DIV_MSB is shown in I2S_INT_DIV_MSB Register Field Descriptions.

Return to the Summary Table.

Table 8-233. I2S_INT_DIV_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	I2S_INT_DIV_15_8	R/W	0x3	Integer Divider for I2S Clock (SCK)

8.6.2.1.39 I2S_INT_DIV_LSB Register (Address = 0x81) [Default = 0xE8]

I2S_INT_DIV_LSB is shown in I2S_INT_DIV_LSB Register Field Descriptions.

Return to the Summary Table.

Table 8-234. I2S_INT_DIV_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	I2S_INT_DIV_7_0	R/W	0xE8	Integer Divider for I2S Clock (SCK)

8.6.2.1.40 I2S_FRAC_NUM_MSB Register (Address = 0x82) [Default = 0x9E]

I2S_FRAC_NUM_MSB is shown in I2S_FRAC_NUM_MSB Register Field Descriptions.

Return to the Summary Table.

Table 8-235. I2S_FRAC_NUM_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	I2S_FRAC_NUM_15_8	R/W	0x9E	Fractional Divider for I2S Clock

8.6.2.1.41 I2S_FRAC_NUM_LSB Register (Address = 0x83) [Default = 0xF2]

I2S_FRAC_NUM_LSB is shown in I2S_FRAC_NUM_LSB Register Field Descriptions.

Return to the Summary Table.

Table 8-236. I2S_FRAC_NUM_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	I2S_FRAC_NUM_7_0	R/W	0xF2	Fractional Divider for I2S Clock

8.6.2.1.42 I2S_DIV_CFG Register (Address = 0x84) [Default = 0x00]

I2S_DIV_CFG is shown in I2S_DIV_CFG Register Field Descriptions.

Return to the Summary Table.

Table 8-237. I2S_DIV_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	I2S_DIV_CFG	R/W	0x0	I2S Divider Configuration 0: I2S always-on clock mode 1: I2S divider mode
5:0	RESERVED	R	0x0	

8.6.2.1.43 CLK_SPEEDUP_INT_ADD Register (Address = 0x85) [Default = 0x37]

CLK_SPEEDUP_INT_ADD is shown in CLK_SPEEDUP_INT_ADD Register Field Descriptions.

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Table 8-238. CLK_SPEEDUP_INT_ADD Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	INT_1ST_ADD	R/W	0x3	Clock speed-up option. When FIFO level overflow trend is detected in AON mode, INT_DIV is adjusted by programmed amount.
3:0	INT_2ND_ADD	R/W	0x7	Clock speed-up option. When FIFO level overflow trend is detected in AON mode, INT_DIV is adjusted by programmed amount.

8.6.2.1.44 CLK_SLOWDWN_INT_SUB Register (Address = 0x86) [Default = 0x26]

CLK_SLOWDWN_INT_SUB is shown in CLK_SLOWDWN_INT_SUB Register Field Descriptions.

Return to the Summary Table.

Table 8-239. CLK_SLOWDWN_INT_SUB Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	INT_1ST_SUB	R/W	0x2	Clock slow-down option. When FIFO level underflow trend is detected in AON mode, INT_DIV is adjusted by programmed amount.
3:0	INT_2ND_SUB	R/W	0x6	Clock slow-down option. When FIFO level underflow trend is detected in AON mode, INT_DIV is adjusted by programmed amount.

8.6.2.1.45 FIFO_1ST_HIGH Register (Address = 0x88) [Default = 0x0F]

FIFO_1ST_HIGH is shown in FIFO_1ST_HIGH Register Field Descriptions.

Return to the Summary Table.

Table 8-240. FIFO_1ST_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FIFO_1ST_HIGH	R/W	0xF	When this level is detected, decrease INT_DIV indicated by INT_1ST_SUB

8.6.2.1.46 FIFO_1ST_LOW Register (Address = 0x89) [Default = 0x06]

FIFO_1ST_LOW is shown in FIFO_1ST_LOW Register Field Descriptions.

Return to the Summary Table.

Table 8-241. FIFO_1ST_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FIFO_1ST_LOW	R/W	0x6	When this level is detected, increase INT_DIV indicated by INT_1ST_ADD

8.6.2.1.47 FIFO_2ND_HIGH Register (Address = 0x8A) [Default = 0x12]

FIFO_2ND_HIGH is shown in FIFO_2ND_HIGH Register Field Descriptions.

Return to the Summary Table.

Table 8-242. FIFO_2ND_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FIFO_2ND_HIGH	R/W	0x12	When this level is detected, decrease INT_DIV indicated by INT_2ND_SUB

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8.6.2.1.48 FIFO_2ND_LOW Register (Address = 0x8B) [Default = 0x09]

FIFO_2ND_LOW is shown in FIFO_2ND_LOW Register Field Descriptions.

Return to the Summary Table.

Table 8-243. FIFO_2ND_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FIFO_2ND_LOW	R/W	0x9	When this level is detected, increase INT_DIV indicated by INT_2ND_ADD

8.6.2.1.49 CFG_I2S Register (Address = 0x8C) [Default = 0x0A]

CFG_I2S is shown in CFG_I2S Register Field Descriptions.

Return to the Summary Table.

Table 8-244. CFG_I2S Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CFG_I2S_DRAIN_THR	R/W	0xA	FIFO Mid Threshold This contains the FIFO threshold to enable a FIFO read.

8.6.2.1.50 I2S_DATA_REG Register (Address = 0x8D) [Default = 0x00]

I2S_DATA_REG is shown in I2S_DATA_REG Register Field Descriptions.

Return to the Summary Table.

Table 8-245. I2S_DATA_REG Register Field Descriptions

Bit	Field	Type	Default	Description
7	I2S_DATA_FALL_EDGE	R/W	0x0	I2S clock edge select for output
6:0	RESERVED	R	0x0	Reserved

8.6.2.1.51 I2S_FORWARD_EN Register (Address = 0x8E) [Default = 0x00]

I2S_FORWARD_EN is shown in I2S_FORWARD_EN Register Field Descriptions.

Return to the Summary Table.

Table 8-246. I2S_FORWARD_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1:0	I2S_GPIO_FORWARD_EN	R/W	0x0	Forward input I2S data received from port1. 2 'b00= I2S Audio Forwarding disabled; Forwards Received GPIO 2 'b01= Forward recovered FC_GPIO I2S on port0 GPIO (FPD3/4 --> FPD3/4). 2 'b10= Forward recovered FC_GPIO I2S on port1 GPIO (FPD3/4 --> FPD3/4). 2 'b11= Forward recovered FC_GPIO I2S on both ports GPIO (FPD3/4 --> FPD3/4).

8.6.2.1.52 FRAC_1ST_ADD_0 Register (Address = 0x90) [Default = 0x00]

FRAC_1ST_ADD_0 is shown in FRAC_1ST_ADD_0 Register Field Descriptions.

Return to the Summary Table.

This register helps adjust the I2S clock in I2S divider mode when FIFO level overflow or underflow trends are observed. Please use the recommended values.

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Table 8-247. FRAC_1ST_ADD_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAC_1ST_ADD_0	R/W	0x0	Clock speed up 1st option for Analog divider [7:0] If 0x84[6]= 1, program this register to 0x40. If 0x84[6]= 0, programming not required.

8.6.2.1.53 FRAC_1ST_ADD_1 Register (Address = 0x91) [Default = 0x00]

FRAC_1ST_ADD_1 is shown in FRAC_1ST_ADD_1 Register Field Descriptions.

Return to the Summary Table.

This register helps adjust the I2S clock in I2S divider mode when FIFO level overflow or underflow trends are observed. Please use the recommended values.

Table 8-248. FRAC_1ST_ADD_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAC_1ST_ADD_1	R/W	0x0	Clock speed up 1st option for Analog divider [15:8] If 0x84[6]= 1, program this register to 0x40. If 0x84[6]= 0, programming not required.

8.6.2.1.54 FRAC_2ND_ADD_0 Register (Address = 0x92) [Default = 0x00]

FRAC_2ND_ADD_0 is shown in FRAC_2ND_ADD_0 Register Field Descriptions.

Return to the Summary Table.

This register helps adjust the I2S clock in I2S divider mode when FIFO level overflow or underflow trends are observed. Please use the recommended values.

Table 8-249. FRAC_2ND_ADD_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAC_2ND_ADD_0	R/W	0x0	Clock speed up 2nd option for Analog divider [7:0] If 0x84[6]= 1, program this register to 0x40. If 0x84[6]= 0, programming not required.

8.6.2.1.55 FRAC_2ND_ADD_1 Register (Address = 0x93) [Default = 0x00]

FRAC_2ND_ADD_1 is shown in FRAC_2ND_ADD_1 Register Field Descriptions.

Return to the Summary Table.

This register helps adjust the I2S clock in I2S divider mode when FIFO level overflow or underflow trends are observed. Please use the recommended values.

Table 8-250. FRAC_2ND_ADD_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAC_2ND_ADD_1	R/W	0x0	Clock speed up 2nd option for Analog divider [15:8] If 0x84[6]= 1, program this register to 0x40. If 0x84[6]= 0, programming not required.

8.6.2.1.56 FRAC_1ST_SUB_0 Register (Address = 0x94) [Default = 0x00]

FRAC_1ST_SUB_0 is shown in FRAC_1ST_SUB_0 Register Field Descriptions.

Return to the Summary Table.

This register helps adjust the I2S clock in I2S divider mode when FIFO level overflow or underflow trends are observed. Please use the recommended values.

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Table 8-251. FRAC_1ST_SUB_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAC_1ST_SUB_0	R/W	0x0	Clock speed slow down 1st option for Analog divider [7:0] If 0x84[6]= 1, program this register to 0x40. If 0x84[6]= 0, programming not required.

8.6.2.1.57 FRAC_1ST_SUB_1 Register (Address = 0x95) [Default = 0x00]

FRAC_1ST_SUB_1 is shown in FRAC_1ST_SUB_1 Register Field Descriptions.

Return to the Summary Table.

This register helps adjust the I2S clock in I2S divider mode when FIFO level overflow or underflow trends are observed. Please use the recommended values.

Table 8-252. FRAC_1ST_SUB_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAC_1ST_SUB_1	R/W	0x0	Clock speed slow down 1st option for Analog divider [15:8] If 0x84[6]= 1, program this register to 0x40. If 0x84[6]= 0, programming not required.

8.6.2.1.58 FRAC_2ND_SUB_0 Register (Address = 0x96) [Default = 0x00]

FRAC_2ND_SUB_0 is shown in FRAC_2ND_SUB_0 Register Field Descriptions.

Return to the Summary Table.

This register helps adjust the I2S clock in I2S divider mode when FIFO level overflow or underflow trends are observed. Please use the recommended values.

Table 8-253. FRAC_2ND_SUB_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAC_2ND_SUB_0	R/W	0x0	Clock speed slow down 2nd option for Analog divider [7:0] If 0x84[6]= 1, program this register to 0x40. If 0x84[6]= 0, programming not required.

8.6.2.1.59 FRAC_2ND_SUB_1 Register (Address = 0x97) [Default = 0x00]

FRAC_2ND_SUB_1 is shown in FRAC_2ND_SUB_1 Register Field Descriptions.

Return to the Summary Table.

This register helps adjust the I2S clock in I2S divider mode when FIFO level overflow or underflow trends are observed. Please use the recommended values.

Table 8-254. FRAC_2ND_SUB_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAC_2ND_SUB_1	R/W	0x0	Clock speed slow down 2nd option for Analog divider [15:8] If 0x84[6]= 1, program this register to 0x40. If 0x84[6]= 0, programming not required.

8.6.2.1.60 INTB_ISR_P0 Register (Address = 0xC0) [Default = 0x03]

INTB_ISR_P0 is shown in INTB_ISR_P0 Register Field Descriptions.

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INTB Interrupt Status for Main Link Port 0 Back Channel This register returns the Interrupt Status for each of the potential signals that can generate interrupts via INTB over the DES_INT or RX_INTN signal. See the

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LOCAL_INT_STS and RX_INTN_STS registers on the Main register page for details.The INTB_ICR_P0 register 0x7E enables interrupt generation for each of these signals. This register provides current status for these signals, independent of whether an interrupt has been enabled in the INTB_ICR_P0 register. Although RX_INTN and INTB_IN signals are active low, a value of 1 in this register indicates an active interrupt condition. For example, if the INTB_IN pin is 0, this register will report a 1.

Table 8-255. INTB_ISR_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	IS_DES_INT_P1	R	0x0	Interrupt Status for DES_INT from FPD4 Daisy Chain Port 1 0: No interrupt detected 1: Interrupt detected
3	IS_DES_INT_P0	R	0x0	Interrupt Status for DES_INT from FPD4 Daisy Chain Port 0 0: No interrupt detected 1: Interrupt detected
2	IS_RX_INTN_P1	R	0x0	Interrupt Status for RX_INTN from FPD3/4 Daisy Chain Port 1 0: No interrupt detected 1: Interrupt detected
1	IS_RX_INTN_P0	R	0x1	Interrupt Status for RX_INTN from FPD3/4 Daisy Chain Port 0 0: No interrupt detected 1: Interrupt detected
0	IS_INTB_IN_P0	R	0x1	Interrupt Status for INTB_IN from Daisy Chain Device INTB_IN Pin 0: No interrupt detected 1: Interrupt detected

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8.6.2.2 Page 2: FPD4 RX PLL Registers

PAGE_2 Registers lists the memory-mapped registers for the Page 2: FPD4 RX PLL registers. All register offset addresses not listed in PAGE_2 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-256. PAGE_2 Registers

Address	Acronym	Register Name	Section
0x0	PLL_LOCK_RX	PLL_LOCK_RX	Go
0x4	MASH_ORDER_RX	MASH_ORDER_RX	Go
0x5	NDIV_7:0_RX	NDIV_7:0_RX	Go
0x6	NDIV_15:8_RX	NDIV_15:8_RX	Go
0xE	VCO_RX	VCO_RX	Go
0x14	SSCG_CTL1_RX	SSCG_CTL1_RX	Go
0x15	SSCG_CTL2_RX	SSCG_CTL2_RX	Go
0x16	SSCG_CTL3_RX	SSCG_CTL3_RX	Go
0x17	SSCG_CTL4_RX	SSCG_CTL4_RX	Go
0x18	DEN_7:0_RX	DEN_7:0_RX	Go
0x19	DEN_15:8_RX	DEN_15:8_RX	Go
0x1A	DEN_23:16_RX	DEN_23:16_RX	Go
0x1E	NUM_7:0_RX	NUM_7:0_RX	Go
0x1F	NUM_15:8_RX	NUM_15:8_RX	Go
0x20	NUM_23:16_RX	NUM_23:16_RX	Go

Complex bit access types are encoded to fit into small table cells. Page 2: FPD4 RX PLL Access Type Codes shows the codes that are used for access types in this section.

Table 8-257. Page 2: FPD4 RX PLL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.2.1 PLL_LOCK_RX Register (Address = 0x0) [Default = 0x01]

PLL_LOCK_RX is shown in PLL_LOCK_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-258. PLL_LOCK_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7	PLL_LOCK_LOST	RC	0x0	Checks to see if PLL_LOCK has been lost since the last read of this register bit. Clears after each read.
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved

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Table 8-258. PLL_LOCK_RX Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.2.2 MASH_ORDER_RX Register (Address = 0x4) [Default = X]

MASH_ORDER_RX is shown in MASH_ORDER_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-259. MASH_ORDER_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:2	MASH_ORDER_2_0	R/W	X	MASH Order This field should be set by strap upon start up. When strapped in FPD3 mode, the mash order defaults to fractional. When strapped in FPD4 mode, the mash order defaults to integer. 000: Integer 010: Fractional
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.2.3 NDIV_7:0_RX Register (Address = 0x5) [Default = 0x6E]

NDIV_7:0_RX is shown in NDIV_7:0_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-260. NDIV_7:0_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT_7_0		0x6E	Bits 7:0 of the feedback Ncount's divider value for the VCO frequency

8.6.2.2.4 NDIV_15:8_RX Register (Address = 0x6) [Default = 0x00]

NDIV_15:8_RX is shown in NDIV_15:8_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-261. NDIV_15:8_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT_15_8		0x0	Bits 15:8 of the feedback Ncount's divider value for the VCO frequency

8.6.2.2.5 VCO_RX Register (Address = 0xE) [Default = 0xC3]

VCO_RX is shown in VCO_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-262. VCO_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7	TEMP_CMP_EN	R/W	0x1	Enables temperature compensation scheme.
6:4	PLL_LOCK_WAIT_2_0	R/W	0x4	Wait time after calibration to make sure the PLL has locked. 000: 25us 001: 50us 010: 75us 011: 100us 100: 150us 101: 200us 110: 300us 111: 400us
3:2	RESERVED	R	0x0	Reserved
1:0	RESERVED	R/W	0x3	Reserved

8.6.2.2.6 SSCG_CTL1_RX Register (Address = 0x14) [Default = 0x80]

SSCG_CTL1_RX is shown in SSCG_CTL1_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-263. SSCG_CTL1_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7	SSCG_CNTR_SPRD	R/W	0x1	FPD BC SSCG spread selection: 0: down-spread ramp 1: center-spread ramp
6:0	RAMPX_INC_6_0	R/W	0x0	Bits 6:0 of the increment value per step that will be added to the ramp for FPD BC SSCG

8.6.2.2.7 SSCG_CTL2_RX Register (Address = 0x15) [Default = 0x00]

SSCG_CTL2_RX is shown in SSCG_CTL2_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-264. SSCG_CTL2_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_INC_14_7	R/W	0x0	Bits 14:7 of the increment value per step that will be added to the ramp for FPD BC SSCG

8.6.2.2.8 SSCG_CTL3_RX Register (Address = 0x16) [Default = 0x00]

SSCG_CTL3_RX is shown in SSCG_CTL3_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-265. SSCG_CTL3_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_STOP_7_0	R/W	0x0	Bits 7:0 of the number of PFD cyles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

8.6.2.2.9 SSCG_CTL4_RX Register (Address = 0x17) [Default = 0x00]

SSCG_CTL4_RX is shown in SSCG_CTL4_RX Register Field Descriptions.

Return to the Summary Table.

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Table 8-266. SSCG_CTL4_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	SSCG_EN	R/W	0x0	Enable spread spectrum clock generation. 0: disabled 1: enabled
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	RAMPX_STOP_9_8	R/W	0x0	Bits 9:8 of the number of PFD cyles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

8.6.2.2.10 DEN_7:0_RX Register (Address = 0x18) [Default = 0xF6]

DEN_7:0_RX is shown in DEN_7:0_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-267. DEN_7:0_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_7_0	R/W	0xF6	Bits 7:0 of the denominator value of MASH

8.6.2.2.11 DEN_15:8_RX Register (Address = 0x19) [Default = 0xFF]

DEN_15:8_RX is shown in DEN_15:8_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-268. DEN_15:8_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_15_8	R/W	0xFF	Bits 15:8 of the denominator value of MASH

8.6.2.2.12 DEN_23:16_RX Register (Address = 0x1A) [Default = 0xFF]

DEN_23:16_RX is shown in DEN_23:16_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-269. DEN_23:16_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_23_16	R/W	0xFF	Bits 23:16 of the denominator value of MASH

8.6.2.2.13 NUM_7:0_RX Register (Address = 0x1E) [Default = 0x4A]

NUM_7:0_RX is shown in NUM_7:0_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-270. NUM_7:0_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_7_0		0x4A	Bits 7:0 of the numerator value of MASH

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8.6.2.2.14 NUM_15:8_RX Register (Address = 0x1F) [Default = 0x68]

NUM_15:8_RX is shown in NUM_15:8_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-271. NUM_15:8_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_15_8		0x68	Bits 15:8 of the numerator value of MASH

8.6.2.2.15 NUM_23:16_RX Register (Address = 0x20) [Default = 0x2F]

NUM_23:16_RX is shown in NUM_23:16_RX Register Field Descriptions.

Return to the Summary Table.

Table 8-272. NUM_23:16_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_23_16		0x2F	Bits 23:16 of the numerator value of MASH

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8.6.2.3 Page 3: FPD3/4 TX PLL Registers

PAGE_3 Registers lists the memory-mapped registers for the Page 3: FPD3/4 TX PLL registers. All register offset addresses not listed in PAGE_3 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-273. PAGE_3 Registers

Address	Acronym	Register Name	Section
0x0	PLL_LOCK_TX_P0	PLL_LOCK_TX_P0	Go
0x4	MASH_ORDER_TX_P0	MASH_ORDER_TX_P0	Go
0x5	NDIV_7:0_TX_P0	NDIV_7:0_TX_P0	Go
0x6	NDIV_15:8_TX_P0	NDIV_15:8_TX_P0	Go
0xE	VCO_TX_P0	VCO_TX_P0	Go
0x14	SSCG_CTL1_TX_P0	SSCG_CTL1_TX_P0	Go
0x15	SSCG_CTL2_TX_P0	SSCG_CTL2_TX_P0	Go
0x16	SSCG_CTL3_TX_P0	SSCG_CTL3_TX_P0	Go
0x17	SSCG_CTL4_TX_P0	SSCG_CTL4_TX_P0	Go
0x18	DEN_7:0_TX_P0	DEN_7:0_TX_P0	Go
0x19	DEN_15:8_TX_P0	DEN_15:8_TX_P0	Go
0x1A	DEN_23:16_TX_P0	DEN_23:16_TX_P0	Go
0x1E	NUM_7:0_TX_P0	NUM_7:0_TX_P0	Go
0x1F	NUM_15:8_TX_P0	NUM_15:8_TX_P0	Go
0x20	NUM_23:16_TX_P0	NUM_23:16_TX_P0	Go
0x40	PLL_LOCK_TX_P1	PLL_LOCK_TX_P1	Go
0x44	MASH_ORDER_TX_P1	MASH_ORDER_TX_P1	Go
0x45	NDIV_7:0_TX_P1	NDIV_7:0_TX_P1	Go
0x46	NDIV_15:8_TX_P1	NDIV_15:8_TX_P1	Go
0x4E	VCO_TX_P1	VCO_TX_P1	Go
0x54	SSCG_CTL1_TX_P1	SSCG_CTL1_TX_P1	Go
0x55	SSCG_CTL2_TX_P1	SSCG_CTL2_TX_P1	Go
0x56	SSCG_CTL3_TX_P1	SSCG_CTL3_TX_P1	Go
0x57	SSCG_CTL4_TX_P1	SSCG_CTL4_TX_P1	Go
0x58	DEN_7:0_TX_P1	DEN_7:0_TX_P1	Go
0x59	DEN_15:8_TX_P1	DEN_15:8_TX_P1	Go
0x5A	DEN_23:16_TX_P1	DEN_23:16_TX_P1	Go
0x5E	NUM_7:0_TX_P1	NUM_7:0_TX_P1	Go
0x5F	NUM_15:8_TX_P1	NUM_15:8_TX_P1	Go
0x60	NUM_23:16_TX_P1	NUM_23:16_TX_P1	Go

Complex bit access types are encoded to fit into small table cells. Page 3: FPD3/4 TX PLL Access Type Codes shows the codes that are used for access types in this section.

Table 8-274. Page 3: FPD3/4 TX PLL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		

Table 8-274. Page 3: FPD3/4 TX PLL Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.3.1 PLL_LOCK_TX_P0 Register (Address = 0x0) [Default = 0x01]

PLL_LOCK_TX_P0 is shown in PLL_LOCK_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-275. PLL_LOCK_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PLL_LOCK_LOST	RC	0x0	Checks to see if PLL_LOCK on Tx Port 0 has been lost since the last read of this register bit. Clears after each read.
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.3.2 MASH_ORDER_TX_P0 Register (Address = 0x4) [Default = 0x09]

MASH_ORDER_TX_P0 is shown in MASH_ORDER_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-276. MASH_ORDER_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:2	MASH_ORDER_2_0		0x2	Bits to set MASH order: 000: Integer 010: Fractional
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.3.3 NDIV_7:0_TX_P0 Register (Address = 0x5) [Default = 0x7D]

NDIV_7:0_TX_P0 is shown in NDIV_7:0_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-277. NDIV_7:0_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT_7_0		0x7D	Bits 7:0 of the feedback Ncount's divider value for the VCO frequency

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8.6.2.3.4 NDIV_15:8_TX_P0 Register (Address = 0x6) [Default = 0x00]

NDIV_15:8_TX_P0 is shown in NDIV_15:8_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-278. NDIV_15:8_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT_15_8		0x0	Bits 15:8 of the feedback Ncount's divider value for the VCO frequency

8.6.2.3.5 VCO_TX_P0 Register (Address = 0xE) [Default = 0xC3]

VCO_TX_P0 is shown in VCO_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-279. VCO_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	TEMP_CMP_EN	R/W	0x1	Enables temperature compensation scheme.
6:4	PLL_LOCK_WAIT_2_0	R/W	0x4	Wait time after calibration to make sure the PLL has locked. 000: 25us 001: 50us 010: 75us 011: 100us 100: 150us 101: 200us 110: 300us 111: 400us
3:2	RESERVED	R	0x0	Reserved
1:0	RESERVED	R/W	0x3	Reserved

8.6.2.3.6 SSCG_CTL1_TX_P0 Register (Address = 0x14) [Default = 0x80]

SSCG_CTL1_TX_P0 is shown in SSCG_CTL1_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-280. SSCG_CTL1_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SSCG_CNTR_SPRD	R/W	0x1	SSCG spread selection: 1: center-spread ramp 0: down-spread ramp
6:0	RAMPX_INC_6_0	R/W	0x0	Bits 6:0 of the increment value per step that will be added to the ramp for SSCG

8.6.2.3.7 SSCG_CTL2_TX_P0 Register (Address = 0x15) [Default = 0x00]

SSCG_CTL2_TX_P0 is shown in SSCG_CTL2_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-281. SSCG_CTL2_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_INC_14_7	R/W	0x0	Bits 14:7 of the increment value per step that will be added to the ramp for SSCG

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8.6.2.3.8 SSCG_CTL3_TX_P0 Register (Address = 0x16) [Default = 0x00]

SSCG_CTL3_TX_P0 is shown in SSCG_CTL3_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-282. SSCG_CTL3_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_STOP_7_0	R/W	0x0	Bits 7:0 of the number of PFD cycles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

8.6.2.3.9 SSCG_CTL4_TX_P0 Register (Address = 0x17) [Default = 0x00]

SSCG_CTL4_TX_P0 is shown in SSCG_CTL4_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-283. SSCG_CTL4_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OVD_SSCG_EN	R/W	0x0	Override enable for the spread spectrum clock generation. 0: disabled 1: enabled (enable changes in SSCG_EN)
6	SSCG_EN	R/W	0x0	Override value for spread spectrum clock generation. 0: disabled 1: enabled Note: Make sure to set OVD_SSCG_EN before modifying this register field.
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	RAMPX_STOP_9_8	R/W	0x0	Bits 9:8 of the number of PFD cycles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

8.6.2.3.10 DEN_7:0_TX_P0 Register (Address = 0x18) [Default = 0xF6]

DEN_7:0_TX_P0 is shown in DEN_7:0_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-284. DEN_7:0_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_7_0	R/W	0xF6	Bits 7:0 of the denominator value of MASH

8.6.2.3.11 DEN_15:8_TX_P0 Register (Address = 0x19) [Default = 0xFF]

DEN_15:8_TX_P0 is shown in DEN_15:8_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-285. DEN_15:8_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_15_8	R/W	0xFF	Bits 15:8 of the denominator value of MASH

8.6.2.3.12 DEN_23:16_TX_P0 Register (Address = 0x1A) [Default = 0xFF]

DEN_23:16_TX_P0 is shown in DEN_23:16_TX_P0 Register Field Descriptions.

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Return to the Summary Table.

Table 8-286. DEN_23:16_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_23_16	R/W	0xFF	Bits 23:16 of the denominator value of MASH

8.6.2.3.13 NUM_7:0_TX_P0 Register (Address = 0x1E) [Default = 0x00]

NUM_7:0_TX_P0 is shown in NUM_7:0_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-287. NUM_7:0_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_7_0		0x0	Bits 7:0 of the numerator value of MASH

8.6.2.3.14 NUM_15:8_TX_P0 Register (Address = 0x1F) [Default = 0x00]

NUM_15:8_TX_P0 is shown in NUM_15:8_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-288. NUM_15:8_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_15_8		0x0	Bits 15:8 of the numerator value of MASH

8.6.2.3.15 NUM_23:16_TX_P0 Register (Address = 0x20) [Default = 0x00]

NUM_23:16_TX_P0 is shown in NUM_23:16_TX_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-289. NUM_23:16_TX_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_23_16		0x0	Bits 23:16 of the numerator value of MASH

8.6.2.3.16 PLL_LOCK_TX_P1 Register (Address = 0x40) [Default = 0x01]

PLL_LOCK_TX_P1 is shown in PLL_LOCK_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-290. PLL_LOCK_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PLL_LOCK_LOST	RC	0x0	Checks to see if PLL_LOCK has been lost since the last read of this register bit. Clears after each read.
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

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8.6.2.3.17 MASH_ORDER_TX_P1 Register (Address = 0x44) [Default = 0x09]

MASH_ORDER_TX_P1 is shown in MASH_ORDER_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-291. MASH_ORDER_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:2	MASH_ORDER_2_0		0x2	Bits to set MASH order: 000: Integer 010: Fractional
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.3.18 NDIV_7:0_TX_P1 Register (Address = 0x45) [Default = 0x7D]

NDIV_7:0_TX_P1 is shown in NDIV_7:0_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-292. NDIV_7:0_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT_7_0		0x7D	Bits 7:0 of the feedback Ncount's divider value for the VCO frequency

8.6.2.3.19 NDIV_15:8_TX_P1 Register (Address = 0x46) [Default = 0x00]

NDIV_15:8_TX_P1 is shown in NDIV_15:8_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-293. NDIV_15:8_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT_15_8		0x0	Bits 15:8 of the feedback Ncount's divider value for the VCO frequency

8.6.2.3.20 VCO_TX_P1 Register (Address = 0x4E) [Default = 0xC3]

VCO_TX_P1 is shown in VCO_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-294. VCO_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	TEMP_CMP_EN	R/W	0x1	Enables temperature compensation scheme.
6:4	PLL_LOCK_WAIT_2_0	R/W	0x4	Wait time after calibration to make sure the PLL has locked. 000: 25us 001: 50us 010: 75us 011: 100us 100: 150us 101: 200us 110: 300us 111: 400us
3:2	RESERVED	R	0x0	Reserved

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Table 8-294. VCO_TX_P1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1:0	RESERVED	R/W	0x3	Reserved

8.6.2.3.21 SSCG_CTL1_TX_P1 Register (Address = 0x54) [Default = 0x80]

SSCG_CTL1_TX_P1 is shown in SSCG_CTL1_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-295. SSCG_CTL1_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SSCG_CNTR_SPRD	R/W	0x1	SSCG spread selection: 1: center-spread ramp 0: down-spread ramp
6:0	RAMPX_INC_6_0	R/W	0x0	Bits 6:0 of the increment value per step that will be added to the ramp for SSCG

8.6.2.3.22 SSCG_CTL2_TX_P1 Register (Address = 0x55) [Default = 0x00]

SSCG_CTL2_TX_P1 is shown in SSCG_CTL2_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-296. SSCG_CTL2_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_INC_14_7	R/W	0x0	Bits 14:7 of the increment value per step that will be added to the ramp for SSCG

8.6.2.3.23 SSCG_CTL3_TX_P1 Register (Address = 0x56) [Default = 0x00]

SSCG_CTL3_TX_P1 is shown in SSCG_CTL3_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-297. SSCG_CTL3_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_STOP_7_0	R/W	0x0	Bits 7:0 of the number of PFD cycles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

8.6.2.3.24 SSCG_CTL4_TX_P1 Register (Address = 0x57) [Default = 0x00]

SSCG_CTL4_TX_P1 is shown in SSCG_CTL4_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-298. SSCG_CTL4_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OVD_SSCG_EN	R/W	0x0	Override enable for the spread spectrum clock generation. 0: disabled 1: enabled (enable changes in SSCG_EN)
6	SSCG_EN	R/W	0x0	Override value for spread spectrum clock generation. 0: disabled 1: enabled Note: Make sure to set OVD_SSCG_EN before modifying this register field.
5	RESERVED	R/W	0x0	Reserved

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Table 8-298. SSCG_CTL4_TX_P1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	RAMPX_STOP_9_8	R/W	0x0	Bits 9:8 of the number of PFD cycles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

8.6.2.3.25 DEN_7:0_TX_P1 Register (Address = 0x58) [Default = 0xF6]

DEN_7:0_TX_P1 is shown in DEN_7:0_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-299. DEN_7:0_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_7_0	R/W	0xF6	Bits 7:0 of the denominator value of MASH

8.6.2.3.26 DEN_15:8_TX_P1 Register (Address = 0x59) [Default = 0xFF]

DEN_15:8_TX_P1 is shown in DEN_15:8_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-300. DEN_15:8_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_15_8	R/W	0xFF	Bits 15:8 of the denominator value of MASH

8.6.2.3.27 DEN_23:16_TX_P1 Register (Address = 0x5A) [Default = 0xFF]

DEN_23:16_TX_P1 is shown in DEN_23:16_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-301. DEN_23:16_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_23_16	R/W	0xFF	Bits 23:16 of the denominator value of MASH

8.6.2.3.28 NUM_7:0_TX_P1 Register (Address = 0x5E) [Default = 0x00]

NUM_7:0_TX_P1 is shown in NUM_7:0_TX_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-302. NUM_7:0_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_7_0		0x0	Bits 7:0 of the numerator value of MASH

8.6.2.3.29 NUM_15:8_TX_P1 Register (Address = 0x5F) [Default = 0x00]

NUM_15:8_TX_P1 is shown in NUM_15:8_TX_P1 Register Field Descriptions.

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Table 8-303. NUM_15:8_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_15_8		0x0	Bits 15:8 of the numerator value of MASH

8.6.2.3.30 NUM_23:16_TX_P1 Register (Address = 0x60) [Default = 0x00]

NUM_23:16_TX_P1 is shown in NUM_23:16_TX_P1 Register Field Descriptions.

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Table 8-304. NUM_23:16_TX_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_23_16		0x0	Bits 23:16 of the numerator value of MASH

8.6.2.4 Page 4: FPD RX Analog Registers

PAGE_4 Registers lists the memory-mapped registers for the Page 4: FPD RX Analog registers. All register offset addresses not listed in PAGE_4 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-305. PAGE_4 Registers

Address	Acronym	Register Name	Section
0x5	LOOP_THRU_EN_CH0	LOOP_THRU_EN_CH0	Go
0x25	LOOP_THRU_EN_CH1	LOOP_THRU_EN_CH1	Go
0x46	CMLOUT_TERM	CMLOUT_TERM	Go
0x49	CMLOUT_CFG	CMLOUT_CFG	Go

Complex bit access types are encoded to fit into small table cells. Page 4: FPD RX Analog Access Type Codes shows the codes that are used for access types in this section.

Table 8-306. Page 4: FPD RX Analog Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.4.1 LOOP_THRU_EN_CH0 Register (Address = 0x5) [Default = 0x00]

LOOP_THRU_EN_CH0 is shown in LOOP_THRU_EN_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-307. LOOP_THRU_EN_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5:4	RESERVED	R/W	0x0	Reserved
3:1	RESERVED	R/W	0x0	Reserved
0	LOOP_THRU_EN	R/W	0x0	Enable Channel Monitoring Loop Through (CMLOUT) on Rx CH0 0: Disable CMLOUT loop through 1: Enable CMLOUT loop through Note: Make sure to override the AEQ setting (Page 14) before configuring CMLOUT in order to ensure LOCK.

8.6.2.4.2 LOOP_THRU_EN_CH1 Register (Address = 0x25) [Default = 0x00]

LOOP_THRU_EN_CH1 is shown in LOOP_THRU_EN_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-308. LOOP_THRU_EN_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5:4	RESERVED	R/W	0x0	Reserved
3:1	RESERVED	R/W	0x0	Reserved

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Table 8-308. LOOP_THRU_EN_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	LOOP_THRU_EN	R/W	0x0	Enable Channel Monitoring Loop Through (CMLOUT) on Rx CH1 0: Disable CMLOUT loop through 1: Enable CMLOUT loop through Note: Make sure to override the AEQ setting (Page 14) before configuring CMLOUT in order to ensure LOCK.

8.6.2.4.3 CMLOUT_TERM Register (Address = 0x46) [Default = 0x01]

CMLOUT_TERM is shown in CMLOUT_TERM Register Field Descriptions.

Return to the Summary Table.

Table 8-309. CMLOUT_TERM Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R/W	0x0	Reserved
1	EN_TERM_LV	R/W	0x0	Enables Termination on Channel Monitor Loop-Through Path 0: Disable termination 1: Enable termination
0	RESERVED	R/W	0x1	Reserved

8.6.2.4.4 CMLOUT_CFG Register (Address = 0x49) [Default = 0x00]

CMLOUT_CFG is shown in CMLOUT_CFG Register Field Descriptions.

Return to the Summary Table.

Table 8-310. CMLOUT_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_TERM_LV_CH1	R/W	0x0	Enable CMLOUT Termination on CH1 0: Disable termination on CMLOUT path for CH1 1: Enable termination on CMLOUT path for CH1
6	EN_TERM_LV_CH0	R/W	0x0	Enable CMLOUT Termination on CH0 0: Disable termination on CMLOUT path for CH0 1: Enable termination on CMLOUT path for CH0
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	LPDR_EN_DRIVER	R/W	0x0	Enables Channel Monitor Loop-Through Driver 0: Disable CMLOUT driver (turn off CMLOUT output) 1: Enable CMLOUT driver (turn on CMLOUT output)
1	SEL_CHANNEL_LV	R/W	0x0	Select Rx channel to monitor on CMLOUT (through MUX) 0: CH0 1: CH1
0	EN_LV	R/W	0x0	Enables Loop Through MUX Control and Termination Path 0: Ignore MUX channel select and termination path settings 1: Enable MUX channel select and termination path settings

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8.6.2.5 Page 5: FPD RX Digital Registers

PAGE_5 Registers lists the memory-mapped registers for the Page 5: FPD RX Digital registers. All register offset addresses not listed in PAGE_5 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-311. PAGE_5 Registers

Address	Acronym	Register Name	Section
0x1E	RX_MODE_STATUS	RX_MODE_STATUS	Go
0x26	I2S_CONTROL	I2S_CONTROL	Go
0x43	SPI_CONTROL	SPI_CONTROL	Go
0x64	BIST_ERROR_COUNT_P0	BIST_ERROR_COUNT_P0	Go
0x66	BAND_FSM_CONTROL_P0	BAND_FSM_CONTROL_P0	Go
0x67	BAND_FSM_STATUS_P0	BAND_FSM_STATUS_P0	Go
0x68	FREQ_COUNT_LOWER_P0	FREQ_COUNT_LOWER_P0	Go
0x69	FREQ_COUNT_HIGHER_P0	FREQ_COUNT_HIGHER_P0	Go
0x74	BIST_ERROR_COUNT_P1	BIST_ERROR_COUNT_P1	Go
0x76	BAND_FSM_CONTROL_P1	BAND_FSM_CONTROL_P1	Go
0x77	BAND_FSM_STATUS_P1	BAND_FSM_STATUS_P1	Go
0x78	FREQ_COUNT_LOWER_P1	FREQ_COUNT_LOWER_P1	Go
0x79	FREQ_COUNT_HIGHER_P1	FREQ_COUNT_HIGHER_P1	Go

Complex bit access types are encoded to fit into small table cells. Page 5: FPD RX Digital Access Type Codes shows the codes that are used for access types in this section.

Table 8-312. Page 5: FPD RX Digital Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.5.1 RX_MODE_STATUS Register (Address = 0x1E) [Default = 0x00]

RX_MODE_STATUS is shown in RX_MODE_STATUS Register Field Descriptions.

Return to the Summary Table.

Table 8-313. RX_MODE_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7	RX_RGB_CHECKSUM	R/W	0x0	RX RGB Checksum Enable Setting this bit enables the Receiver to validate a one-byte checksum following each video line. Checksum failures are reported in the Page 6 HDCP_STS register.

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Table 8-313. RX_MODE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	BC_FREQ_SELECT	R/W	0x0	Back Channel Frequency Select (FPD-Link III) 0: Back channel runs at 5 Mbps 1: Back channel runs at 10 Mbps If BC_HIGH_SPEED= 1, then BC_FREQ_SELECT is ignored and the back channel frequency is set to 20 Mbps (not available when paired with 92x serializers). Note: Changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer.
5	RESERVED	R/W	0x0	Reserved
4	BC_HIGH_SPEED	R/W	0x0	Back-Channel High-Speed control (FPD-Link III) Enables high-speed back-channel at 20 Mbps. This bit will override the BC_FREQ_SELECT setting. Note: Changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer.
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

8.6.2.5.2 I2S_CONTROL Register (Address = 0x26) [Default = 0x00]

I2S_CONTROL is shown in I2S_CONTROL Register Field Descriptions.

Return to the Summary Table.

Table 8-314. I2S_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5:4	PACKET_FIFO_DRAIN_THRESHOLD	R/W	0x0	I2S Packet FIFO Drain Threshold 00: Half-full 01: 3/4 full 10: 1/4 full 11: reserved
3	I2S_FIFO_OVERRUN_STATUS	R	0x0	I2S FIFO Overrun Status
2	I2S_FIFO_UNDERRUN_STATUS	R	0x0	I2S FIFO Underrun Status
1	I2S_FIFO_ERROR_RESET	R/W	0x0	I2S Fifo Error Reset 1: Clears FIFO Error
0	I2S_DATA_FALLING_EDGE	R/W	0x0	I2S Clock Edge Select 1: I2S Data is strobed on the Rising Clock Edge. 0: I2S Data is strobed on the Falling Clock Edge.

8.6.2.5.3 SPI_CONTROL Register (Address = 0x43) [Default = 0x00]

SPI_CONTROL is shown in SPI_CONTROL Register Field Descriptions.

Return to the Summary Table.

Table 8-315. SPI_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	SPI_MISO_MODE	R/W	0x0	SPI MISO pin mode during Reverse SPI mode During Reverse SPI mode, SPI_MISO is typically an output signal. For bused SPI applications, it may be necessary to tri-state the SPI_MISO output if the device is not selected (SPI_SS= 0). 0: Always enable SPI_MISO output driver 1: Tri-state SPI_MISO output if SPI_SS is not asserted (low)
3	SPI_CPOL	R/W	0x0	SPI Clock Polarity Control 0: SPI Data driven on Falling clock edge, sampled on Rising clock edge 1: SPI Data driven on Rising clock edge, sampled on Falling clock edge
2:0	RESERVED	R	0x0	Reserved

8.6.2.5.4 BIST_ERROR_COUNT_P0 Register (Address = 0x64) [Default = 0x00]

BIST_ERROR_COUNT_P0 is shown in BIST_ERROR_COUNT_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-316. BIST_ERROR_COUNT_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BIST_ERROR_COUNT	R	0x0	Bist Error Count for Port 0 Returns BIST error count. A value of 0xFF indicates failure to start BIST or loss of Lock during BIST. Otherwise the value indicates number of errors detected during BIST. The counter will saturate at a value of 0xFE.

8.6.2.5.5 BAND_FSM_CONTROL_P0 Register (Address = 0x66) [Default = 0x01]

BAND_FSM_CONTROL_P0 is shown in BAND_FSM_CONTROL_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-317. BAND_FSM_CONTROL_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	P0_BAND_SEL_SM_EN	R/W	0x1	Enable BAND_SEL_SM Functionality If this bit is set to 1, then the receiver will automatically toggle frequency bands if it detects a LOCK to a frequency that is outside of the expected range of its current band. 0: Disable BAND_SEL_SM functionality 1: Enable BAND_SEL_SM functionality

8.6.2.5.6 BAND_FSM_STATUS_P0 Register (Address = 0x67) [Default = 0x00]

BAND_FSM_STATUS_P0 is shown in BAND_FSM_STATUS_P0 Register Field Descriptions.

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Table 8-318. BAND_FSM_STATUS_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	P0_CDR_FSM_STATE	R	0x0	Current band-select FSM state. 000: IDLE 001: SET_CDR_LOW 010: CDR_LOW (PCLK=25-50MHz) 011: SET_CDR_MID 100: CDR_MID (PCLK=50-100MHz) 101: SET_CDR_HI 110: CDR_HI (100-190MHz)
4	P0_CDR_FREQ_STABLE	R	0x0	Output of the frequency detect circuit. Indicates whether the recovered PCLK from the FPD-Link III link is stable. 0: PCLK is not stable 1: PCLK is stable
3	P0_LOCK_OSC	R	0x0	Indicates whether the FPD-Link III RX is locked (CDR is locked and the correct DCA sequence is received). 0: No LOCK is detected 1: LOCK is detected
2	P0_RANGE_LOCK	R	0x0	Indicates whether the device is locked onto a single CDR band. 0: No LOCK onto CDR band 1: LOCK onto CDR band
1:0	RESERVED	R	0x0	Reserved

8.6.2.5.7 FREQ_COUNT_LOWER_P0 Register (Address = 0x68) [Default = 0x00]

FREQ_COUNT_LOWER_P0 is shown in FREQ_COUNT_LOWER_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-319. FREQ_COUNT_LOWER_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	P0_FREQ_COUNT_LOWER	R	0x0	Frequency Counter Lower 8 bits [7:0] (1/256 MHz) Reports the measured frequency for the FPD3 RX. This portion of the field is the fractional value in 1/256 MHz. Frequency measurements scale with clock frequency.

8.6.2.5.8 FREQ_COUNT_HIGHER_P0 Register (Address = 0x69) [Default = 0x00]

FREQ_COUNT_HIGHER_P0 is shown in FREQ_COUNT_HIGHER_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-320. FREQ_COUNT_HIGHER_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	P0_FREQ_COUNT_HIGHER	R	0x0	Frequency Counter Upper 8 bits [15:8] (MHz) Reports the measured frequency for the FPD3 RX. This portion of the field is the integer value in MHz. Frequency measurements scale with clock frequency.

8.6.2.5.9 BIST_ERROR_COUNT_P1 Register (Address = 0x74) [Default = 0x00]

BIST_ERROR_COUNT_P1 is shown in BIST_ERROR_COUNT_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-321. BIST_ERROR_COUNT_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BIST_ERROR_COUNT	R	0x0	Bist Error Count for Port 1 Returns BIST error count. A value of 0xFF indicates failure to start BIST or loss of Lock during BIST. Otherwise the value indicates number of errors detected during BIST. The counter will saturate at a value of 0xFE.

8.6.2.5.10 BAND_FSM_CONTROL_P1 Register (Address = 0x76) [Default = 0x31]

BAND_FSM_CONTROL_P1 is shown in BAND_FSM_CONTROL_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-322. BAND_FSM_CONTROL_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x3	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	P1_BAND_SEL_SM_EN	R/W	0x1	Enable BAND_SEL_SM Functionality If this bit is set to 1, then the receiver will automatically toggle frequency bands if it detects a LOCK to a frequency that is outside of the expected range of its current band. 0: Disable BAND_SEL_SM functionality 1: Enable BAND_SEL_SM functionality

8.6.2.5.11 BAND_FSM_STATUS_P1 Register (Address = 0x77) [Default = 0x00]

BAND_FSM_STATUS_P1 is shown in BAND_FSM_STATUS_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-323. BAND_FSM_STATUS_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	P1_CDR_FSM_STATE	R	0x0	Current band-select FSM state. 000: IDLE 001: SET_CDR_LOW 010: CDR_LOW (PCLK=25-50MHz) 011: SET_CDR_MID 100: CDR_MID (PCLK=50-100MHz) 101: SET_CDR_HI 110: CDR_HI (100-190MHz)
4	P1_CDR_FREQ_STABLE	R	0x0	Output of the frequency detect circuit. Indicates whether the recovered PCLK from the FPD-Link III link is stable. 0: PCLK is not stable 1: PCLK is stable
3	P1_LOCK_OSC	R	0x0	Indicates whether the FPD-Link III RX is locked (CDR is locked and the correct DCA sequence is received). 0: No LOCK is detected 1: LOCK is detected
2	P1_RANGE_LOCK	R	0x0	Indicates whether the device is locked onto a single CDR band. 0: No LOCK onto CDR band 1: LOCK onto CDR band
1:0	RESERVED	R	0x0	Reserved

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8.6.2.5.12 FREQ_COUNT_LOWER_P1 Register (Address = 0x78) [Default = 0x00]

FREQ_COUNT_LOWER_P1 is shown in FREQ_COUNT_LOWER_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-324. FREQ_COUNT_LOWER_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	P1_FREQ_COUNT_LOWER	R	0x0	Frequency Counter Lower 8 bits [7:0] (1/256 MHz) Reports the measured frequency for the FPD3 RX. This portion of the field is the fractional value in 1/256 MHz. Frequency measurements scale with clock frequency.

8.6.2.5.13 FREQ_COUNT_HIGHER_P1 Register (Address = 0x79) [Default = 0x00]

FREQ_COUNT_HIGHER_P1 is shown in FREQ_COUNT_HIGHER_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-325. FREQ_COUNT_HIGHER_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	P1_FREQ_COUNT_HIGHER	R	0x0	Frequency Counter Upper 8 bits [15:8] (MHz) Reports the measured frequency for the FPD3 RX. This portion of the field is the integer value in MHz. Frequency measurements scale with clock frequency.

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8.6.2.6 Page 6: HDCP RX Registers

PAGE_6 Registers lists the memory-mapped registers for the Page 6: HDCP RX registers. All register offset addresses not listed in PAGE_6 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-326. PAGE_6 Registers

Address	Acronym	Register Name	Section
0x0	RX_BKSV0	RX_BKSV0	Go
0x1	RX_BKSV1	RX_BKSV1	Go
0x2	RX_BKSV2	RX_BKSV2	Go
0x3	RX_BKSV3	RX_BKSV3	Go
0x4	RX_BKSV4	RX_BKSV4	Go
0x10	TX_KSV0	TX_KSV0	Go
0x11	TX_KSV1	TX_KSV1	Go
0x12	TX_KSV2	TX_KSV2	Go
0x13	TX_KSV3	TX_KSV3	Go
0x14	TX_KSV4	TX_KSV4	Go
0x43	HDCP_CTL	HDCP_CTL	Go
0x44	HDCP_STS	HDCP_STS	Go
0x48	NVM_CTL	NVM_CTL	Go

Complex bit access types are encoded to fit into small table cells. Page 6: HDCP RX Access Type Codes shows the codes that are used for access types in this section.

Table 8-327. Page 6: HDCP RX Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.6.1 RX_BKSV0 Register (Address = 0x0) [Default = 0x00]

RX_BKSV0 is shown in RX_BKSV0 Register Field Descriptions.

Return to the Summary Table.

Table 8-328. RX_BKSV0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BKSV0	R	0x0	Value of byte0 of the Receiver KSV.

8.6.2.6.2 RX_BKSV1 Register (Address = 0x1) [Default = 0x00]

RX_BKSV1 is shown in RX_BKSV1 Register Field Descriptions.

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Table 8-329. RX_BKSV1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BKSV1	R	0x0	Value of byte1 of the Receiver KSV.

8.6.2.6.3 RX_BKSV2 Register (Address = 0x2) [Default = 0x00]

RX_BKSV2 is shown in RX_BKSV2 Register Field Descriptions.

Return to the Summary Table.

Table 8-330. RX_BKSV2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BKSV2	R	0x0	Value of byte2 of the Receiver KSV.

8.6.2.6.4 RX_BKSV3 Register (Address = 0x3) [Default = 0x00]

RX_BKSV3 is shown in RX_BKSV3 Register Field Descriptions.

Return to the Summary Table.

Table 8-331. RX_BKSV3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BKSV3	R	0x0	Value of byte3 of the Receiver KSV.

8.6.2.6.5 RX_BKSV4 Register (Address = 0x4) [Default = 0x00]

RX_BKSV4 is shown in RX_BKSV4 Register Field Descriptions.

Return to the Summary Table.

Table 8-332. RX_BKSV4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BKSV4	R	0x0	Value of byte4 of the Receiver KSV.

8.6.2.6.6 TX_KSV0 Register (Address = 0x10) [Default = 0x00]

TX_KSV0 is shown in TX_KSV0 Register Field Descriptions.

Return to the Summary Table.

Table 8-333. TX_KSV0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TX_KSV0	R	0x0	Value of byte0 of the Transmitter KSV.

8.6.2.6.7 TX_KSV1 Register (Address = 0x11) [Default = 0x00]

TX_KSV1 is shown in TX_KSV1 Register Field Descriptions.

Return to the Summary Table.

Table 8-334. TX_KSV1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TX_KSV1	R	0x0	Value of byte1 of the Transmitter KSV.

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8.6.2.6.8 TX_KSV2 Register (Address = 0x12) [Default = 0x00]

TX_KSV2 is shown in TX_KSV2 Register Field Descriptions.

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Table 8-335. TX_KSV2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TX_KSV2	R	0x0	Value of byte2 of the Transmitter KSV.

8.6.2.6.9 TX_KSV3 Register (Address = 0x13) [Default = 0x00]

TX_KSV3 is shown in TX_KSV3 Register Field Descriptions.

Return to the Summary Table.

Table 8-336. TX_KSV3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TX_KSV3	R	0x0	Value of byte3 of the Transmitter KSV.

8.6.2.6.10 TX_KSV4 Register (Address = 0x14) [Default = 0x00]

TX_KSV4 is shown in TX_KSV4 Register Field Descriptions.

Return to the Summary Table.

Table 8-337. TX_KSV4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TX_KSV4	R	0x0	Value of byte4 of the Transmitter KSV.

8.6.2.6.11 HDCP_CTL Register (Address = 0x43) [Default = 0x00]

HDCP_CTL is shown in HDCP_CTL Register Field Descriptions.

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HDCP Receive Control Register

Table 8-338. HDCP_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	HDCP_RST	RH/W1S	0x0	HDCP Reset: Setting this bit will reset the HDCP transmitter and disable HDCP authentication, by resetting certain registers. This bit should only be used to recover from improper operation. This bit is self-clearing.
6:0	RESERVED	R	0x0	Reserved

8.6.2.6.12 HDCP_STS Register (Address = 0x44) [Default = 0x00]

HDCP_STS is shown in HDCP_STS Register Field Descriptions.

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Table 8-339. HDCP_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved

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Table 8-339. HDCP_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	RGB_CHKSUM_ERR	R	0x0	RGB Checksum Error Detected: If RGB Checksum in enabled through the HDCP Transmitter HDCP_DBG register, this bit will indicate if a checksum error is detected. This register may be cleared by writing any value to this register
0	AUTHED	R	0x0	HDCP Authenticated: Indicates the HDCP authentication has completed successfully. The controller may now send video data requiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authentication.

8.6.2.6.13 NVM_CTL Register (Address = 0x48) [Default = X]

NVM_CTL is shown in NVM_CTL Register Field Descriptions.

Return to the Summary Table.

Table 8-340. NVM_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	NVM_PASS	R	0x0	NVM Verify pass: This bit indicates the completion status of the NVM verification process. This bit is valid only when NVM_DONE is asserted. 0: NVM Verify failed 1: NVM Verify passed
6	NVM_DONE	R	0x0	NVM Verify done: This bit indicates that the NVM Verification has completed.
5:3	RESERVED	R	0x0	Reserved
2	NVM_VERIFY	R/W	0x0	NVM Verify: Setting this bit will enable a verification of the NVM contents. This is done by reading all NVM keys, computing a SHA-1 hash value, and verifying against the SHA-1 hash stored in NVM. This bit will be cleared upon completion of the NVM Verification.
1:0	RESERVED	R	X	Reserved

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8.6.2.7 Page 7: FPD TX Control Registers

Table 8-341 lists the memory-mapped registers for the Page 7: FPD TX Control registers. All register offset addresses not listed in Table 8-341 should be considered as reserved locations and the register contents should not be modified.

Table 8-341. PAGE_7 Registers

Address	Acronym	Register Name	Section
0x5	CH0_BC_CTL0	CH0_BC_CTL0	Go
0x6	CH0_BC_CTL3	CH0_BC_CTL3	Go
0x8	CH0_BC_CTL4	CH0_BC_CTL4	Go
0xD	CH0_BC_CTL1	CH0_BC_CTL1	Go
0xE	CH0_BC_CTL2	CH0_BC_CTL2	Go
0x15	CH0_TX_LDO_EN	CH0_TX_LDO_EN	Go
0x25	CH1_BC_CTL0	CH1_BC_CTL0	Go
0x26	CH1_BC_CTL3	CH1_BC_CTL3	Go
0x28	CH1_BC_CTL4	CH1_BC_CTL4	Go
0x2D	CH1_BC_CTL1	CH1_BC_CTL1	Go
0x2E	CH1_BC_CTL2	CH1_BC_CTL2	Go
0x35	CH1_TX_LDO_EN	CH1_TX_LDO_EN	Go

Complex bit access types are encoded to fit into small table cells. Table 8-342 shows the codes that are used for access types in this section.

Table 8-342. Page 7: FPD TX Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.7.1 CH0_BC_CTL0 Register (Address = 0x5) [Default = X]

CH0_BC_CTL0 is shown in Table 8-343.

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Table 8-343. CH0_BC_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH0_BC_CTL0	R/W	X	FPD3 Back Channel Configuration 0 for Channel 0 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0x00.

8.6.2.7.2 CH0_BC_CTL3 Register (Address = 0x6) [Default = X]

CH0_BC_CTL3 is shown in Table 8-344.

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Table 8-344. CH0_BC_CTL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH0_BC_CTL3	R/W	X	FPD3 Back Channel Configuration 3 for Channel 0 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0xFF.

8.6.2.7.3 CH0_BC_CTL4 Register (Address = 0x8) [Default = X]

CH0_BC_CTL4 is shown in Table 8-345.

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Table 8-345. CH0_BC_CTL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH0_BC_CTL4	R/W	X	FPD3 Back Channel Configuration 4 for Channel 0 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0x1C.

8.6.2.7.4 CH0_BC_CTL1 Register (Address = 0xD) [Default = X]

CH0_BC_CTL1 is shown in Table 8-346.

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Table 8-346. CH0_BC_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH0_BC_CTL1	R/W	X	FPD3 Back Channel Configuration 1 for Channel 0 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0x70.

8.6.2.7.5 CH0_BC_CTL2 Register (Address = 0xE) [Default = X]

CH0_BC_CTL2 is shown in Table 8-347.

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Table 8-347. CH0_BC_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH0_BC_CTL2	R/W	X	FPD3 Back Channel Configuration 2 for Channel 0 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0x70.

8.6.2.7.6 CH0_TX_LDO_EN Register (Address = 0x15) [Default = 0xF0]

CH0_TX_LDO_EN is shown in Table 8-348.

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Table 8-348. CH0_TX_LDO_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	CH0_TX_LDO_EN	R/W	0xF	Daisy Chain LDO Enable for Channel 0 0000: Enabled 1111: Disabled Any other bit configuration is invalid.
3:0	RESERVED	R	0x0	Reserved

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8.6.2.7.7 CH1_BC_CTL0 Register (Address = 0x25) [Default = X]

CH1_BC_CTL0 is shown in Table 8-349.

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Table 8-349. CH1_BC_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH1_BC_CTL0	R/W	X	FPD3 Back Channel Configuration 0 for Channel 1 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0x00.

8.6.2.7.8 CH1_BC_CTL3 Register (Address = 0x26) [Default = X]

CH1_BC_CTL3 is shown in Table 8-350.

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Table 8-350. CH1_BC_CTL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH1_BC_CTL3	R/W	X	FPD3 Back Channel Configuration 3 for Channel 1 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0xFF.

8.6.2.7.9 CH1_BC_CTL4 Register (Address = 0x28) [Default = X]

CH1_BC_CTL4 is shown in Table 8-351.

Return to the Summary Table.

Table 8-351. CH1_BC_CTL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH1_BC_CTL4	R/W	X	FPD3 Back Channel Configuration 4 for Channel 1 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0x1C.

8.6.2.7.10 CH1_BC_CTL1 Register (Address = 0x2D) [Default = X]

CH1_BC_CTL1 is shown in Table 8-352.

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Table 8-352. CH1_BC_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH1_BC_CTL1	R/W	X	FPD3 Back Channel Configuration 1 for Channel 1 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0x70.

8.6.2.7.11 CH1_BC_CTL2 Register (Address = 0x2E) [Default = X]

CH1_BC_CTL2 is shown in Table 8-353.

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Table 8-353. CH1_BC_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CH1_BC_CTL2	R/W	X	FPD3 Back Channel Configuration 2 for Channel 1 This register is set by strap at start up. When working in FPD3 mode, this register must be manually set to 0x70.

8.6.2.7.12 CH1_TX_LDO_EN Register (Address = 0x35) [Default = 0xF0]

CH1_TX_LDO_EN is shown in Table 8-354.

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Table 8-354. CH1_TX_LDO_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	CH1_TX_LDO_EN	R/W	0xF	Daisy Chain LDO Enable for Channel 1 0000: Enabled 1111: Disabled Any other bit configuration is invalid.
3:0	RESERVED	R	0x0	Reserved

8.6.2.8 Page 8: FPD3/4 TX Digital Registers

PAGE_8 Registers lists the memory-mapped registers for the Page 8: FPD3/4 TX Digital registers. All register offset addresses not listed in PAGE_8 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-355. PAGE_8 Registers

Address	Acronym	Register Name	Section
0x1	FPD3_TX_LINK_STS_P0	FPD3_TX_LINK_STS_P0	Go
0x2	FPD3_TX_MODE_CTL_P0	FPD3_TX_MODE_CTL_P0	Go
0x3	FPD3_TX_DATAPATH_CTL_P0	FPD3_TX_DATAPATH_CTL_P0	Go
0x4	FPD3_TX_FIFO_CFG_P0	FPD3_TX_FIFO_CFG_P0	Go
0x5	FPD3_TX_FIFO_STS_P0	FPD3_TX_FIFO_STS_P0	Go
0x6	FPD3_TX_FIFO_STS2	FPD3_TX_FIFO_STS2	Go
0x11	FPD3_TX_DUAL_STS_P1	FPD3_TX_DUAL_STS_P1	Go
0x12	FPD3_TX_MODE_CTL_P1	FPD3_TX_MODE_CTL_P1	Go
0x13	FPD3_TX_DATAPATH_CTL_P1	FPD3_TX_DATAPATH_CTL_P1	Go
0x14	FPD3_TX_FIFO_CFG_P1	FPD3_TX_FIFO_CFG_P1	Go
0x15	FPD3_TX_FIFO_STS_P1	FPD3_TX_FIFO_STS_P1	Go
0x40	FPD3_TX_PGCTL_P0	FPD3_TX_PGCTL_P0	Go
0x41	FPD3_TX_PGCFG_P0	FPD3_TX_PGCFG_P0	Go
0x42	FPD3_TX_PGIA_P0	FPD3_TX_PGIA_P0	Go
0x43	FPD3_TX_PGID_P0	FPD3_TX_PGID_P0	Go
0x45	FPD3_TX_PGTSTDAT_P0	FPD3_TX_PGTSTDAT_P0	Go
0x50	FPD3_TX_PGCTL_P1	FPD3_TX_PGCTL_P1	Go
0x51	FPD3_TX_PGCFG_P1	FPD3_TX_PGCFG_P1	Go
0x52	FPD3_TX_PGIA_P1	FPD3_TX_PGIA_P1	Go
0x53	FPD3_TX_PGID_P1	FPD3_TX_PGID_P1	Go
0x55	FPD3_TX_PGTSTDAT_P1	FPD3_TX_PGTSTDAT_P1	Go
0x84	PRBS_TEST_EN_P0	PRBS_TEST_EN_P0	Go
0x89	FPD_PRBS_P0	FPD_PRBS_P0	Go
0x8C	INTR_CTL_FPD4_PORT0	INTR_CTL_FPD4_PORT0	Go
0x94	PRBS_TEST_EN_P1	PRBS_TEST_EN_P1	Go
0x99	FPD_PRBS_P1	FPD_PRBS_P1	Go
0x9C	INTR_CTL_FPD4_PORT1	INTR_CTL_FPD4_PORT1	Go
0x9D	INTR_STS_FPD4_PORT1	INTR_STS_FPD4_PORT1	Go

Complex bit access types are encoded to fit into small table cells. Page 8: FPD3/4 TX Digital Access Type Codes shows the codes that are used for access types in this section.

Table 8-356. Page 8: FPD3/4 TX Digital Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		

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Table 8-356. Page 8: FPD3/4 TX Digital Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

8.6.2.8.1 FPD3_TX_LINK_STS_P0 Register (Address = 0x1) [Default = 0x00]

FPD3_TX_LINK_STS_P0 is shown in FPD3_TX_LINK_STS_P0 Register Field Descriptions.

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FPD-Link III Daisy Chain Status This register shows status for the selected FPD3 link; it also includes information about daisy chain Port 0 and daisy chain Port 1. This is the only register in the Port 0 section that contains data about Port 1.

Table 8-357. FPD3_TX_LINK_STS_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FPD3_LINK_RDY	R	0x0	FPD3 Daisy Chain Port 0 Link Ready 0: Link is not ready 1: FPD3 link has detected a valid downstream connection with satisfactory capabilities for the downstream link.
6	FPD3_TX_STS	R	0x0	FPD3 Daisy Chain Port 0 Transmit Status This bit indicates that the FPD3 Transmitter is active and the receiver is locked to the transmit clock. It is only asserted once a valid input has been detected, and the FPD3 Transmit connection has entered the correct mode (i.e. Single vs Dual mode).
5:4	FPD3_TX_PORT_STS	R	0x0	FPD3 Daisy Chain Port 0 and Port 1 Mode If FPD3_TX_STS is set to a 1, this field indicates the port mode status as follows: 00: Dual FPD-Link III Transmitter mode 01: Single FPD-Link III Transmit on port 0 10: Single FPD-Link III Transmit on port 1 11: FPD-Link III Transmit on both ports (Replicate or Splitter mode)
3:0	RESERVED	R	0x0	Reserved

8.6.2.8.2 FPD3_TX_MODE_CTL_P0 Register (Address = 0x2) [Default = X]

FPD3_TX_MODE_CTL_P0 is shown in FPD3_TX_MODE_CTL_P0 Register Field Descriptions.

Return to the Summary Table.

FPD-Link III Daisy Chain Mode Control for Port 0 and Port 1

Table 8-358. FPD3_TX_MODE_CTL_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	DUAL_ALIGN_DE	R/W	0x0	Dual Align on DE This bit only applies for dual link mode. 0: Data is sent on alternating links without regard to odd/even pixel position 1: Odd/even data is sent on the primary/secondary links respectively, based on the assertion of DE
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	FORCE_LINK_RDY	R/W	0x0	Force Link Ready on Port 0 0: Normal operation 1: Link ready indication is forced. This bypasses back channel link detection and sends link ready on the back channel.

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Table 8-358. FPD3_TX_MODE_CTL_P0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2:0	RESERVED	R/W	X	Reserved

8.6.2.8.3 FPD3_TX_DATAPATH_CTL_P0 Register (Address = 0x3) [Default = 0x42]

FPD3_TX_DATAPATH_CTL_P0 is shown in FPD3_TX_DATAPATH_CTL_P0 Register Field Descriptions.

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FPD-Link III Daisy Chain Datapath Control for Port 0

Table 8-359. FPD3_TX_DATAPATH_CTL_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	PASS_RGB	R/W	0x1	This bit determines if RGB data can be sent independent of DE, which allows the device to interoperate with the DS90UB926, DS90UB928, DS90UB940, and DS90UB948. Setting this bit prevents HDCP operation and blocks packetized audio. 0: Block RGB data when DE is deasserted 1: Pass RGB data independent of DE
5	DE_POLARITY	R/W	0x0	This bit indicates the polarity of the DE (Data Enable) signal. 0: DE is positive (active high, idle low) 1: DE is inverted (active low, idle high)
4	RESERVED	R/W	0x0	Reserved
3	I2S_TRANSPORT_SEL	R/W	0x0	0: Enable I2S Data Island Transport 1: Enable I2S Data Forward Channel Frame Transport
2	VIDEO_18B_EN	R/W	0x0	18-bit Video Select 0: Select 24-bit video mode 1: Select 18-bit video mode
1:0	I2S_MODE	R/W	0x2	I2S Channel Mode 00: 2-channel I2S audio 01: 4-channel I2S audio 10: 5.1- or 7.1-channel surround audio is enabled 11: Reserved Note that I2S Data Island Transport (Bit3= 0) must be set for surround audio.

8.6.2.8.4 FPD3_TX_FIFO_CFG_P0 Register (Address = 0x4) [Default = X]

FPD3_TX_FIFO_CFG_P0 is shown in FPD3_TX_FIFO_CFG_P0 Register Field Descriptions.

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Table 8-360. FPD3_TX_FIFO_CFG_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R/W	0x2	Reserved
3	ENABLE_FPD3_FIFO	R/W	0x0	Enable FPD3 FIFO for Daisy Chain Port 0 This bit must be enabled for the FPD3 link to function. 0: FPD3 TX FIFO disabled 1: FPD3 TX FIFO enabled
2:0	RESERVED	R/W	X	Reserved

8.6.2.8.5 FPD3_TX_FIFO_STS_P0 Register (Address = 0x5) [Default = 0x00]

FPD3_TX_FIFO_STS_P0 is shown in FPD3_TX_FIFO_STS_P0 Register Field Descriptions.

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Table 8-361. FPD3_TX_FIFO_STS_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	FPD3_CHAN_ALIGN_ERR	RC	0x0	FPD-Link III Channel Alignment Error 0: No channel alignment error detected 1: Channel alignment error detected
3:0	RESERVED	R	0x0	Reserved

8.6.2.8.6 FPD3_TX_FIFO_STS2 Register (Address = 0x6) [Default = 0x00]

FPD3_TX_FIFO_STS2 is shown in FPD3_TX_FIFO_STS2 Register Field Descriptions.

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This register details the FIFO errors for both Port 0 and Port 1 daisy chain FPD3 links.

Table 8-362. FPD3_TX_FIFO_STS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	P1_FPD3_FIFO_PTR_ERR	RC	0x0	FIFO Pointer Error for FPD3 Daisy Chain Port 1 0: No error detected 1: A FIFO pointer error has been detected
5	P1_FPD3_FIFO_OVER	RC	0x0	FIFO Overflow for FPD3 Daisy Chain Port 1 0: No error detected 1: A FIFO overflow is detected (too many writes)
4	P1_FPD3_FIFO_UNDER	RC	0x0	FIFO Underflow for FPD3 Daisy Chain Port 1 0: No error detected 1: A FIFO underflow is detected (too many reads)
3	RESERVED	R	0x0	Reserved
2	P0_FPD3_FIFO_PTR_ERR	RC	0x0	FIFO Pointer Error for FPD3 Daisy Chain Port 0 0: No error detected 1: A FIFO pointer error has been detected
1	P0_FPD3_FIFO_OVER	RC	0x0	FIFO Overflow for FPD3 Daisy Chain Port 0 0: No error detected 1: A FIFO overflow is detected (too many writes)
0	P0_FPD3_FIFO_UNDER	RC	0x0	FIFO Underflow for FPD3 Daisy Chain Port 0 0: No error detected 1: A FIFO underflow is detected (too many reads)

8.6.2.8.7 FPD3_TX_DUAL_STS_P1 Register (Address = 0x11) [Default = 0x00]

FPD3_TX_DUAL_STS_P1 is shown in FPD3_TX_DUAL_STS_P1 Register Field Descriptions.

Return to the Summary Table.

FPD-Link III Daisy Chain Status for Port 1

Table 8-363. FPD3_TX_DUAL_STS_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FPD3_LINK_RDY	R	0x0	FPD3 Daisy Chain Port 1 Link Ready 0: Link is not ready 1: FPD3 link has detected a valid downstream connection with satisfactory capabilities for the downstream link.

Table 8-363. FPD3_TX_DUAL_STS_P1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	FPD3_TX_STS	R	0x0	FPD3 Daisy Chain Port 1 Transmit Status This bit indicates that the FPD3 Transmitter is active and the receiver is locked to the transmit clock. It is only asserted once a valid input has been detected, and the FPD3 Transmit connection has entered the correct mode (i.e. Single vs Dual mode).
5	RESERVED	R	0x0	Reserved
4	FPD3_LINK_TRANSMIT_STS	R	0x0	FPD-Link III Port 1 Status 0: Port 1 is not available for transmission 1: Port 1 is available for transmission
3:0	RESERVED	R	0x0	Reserved

8.6.2.8.8 FPD3_TX_MODE_CTL_P1 Register (Address = 0x12) [Default = X]

FPD3_TX_MODE_CTL_P1 is shown in FPD3_TX_MODE_CTL_P1 Register Field Descriptions.

Return to the Summary Table.

FPD-Link III Daisy Chain Mode Control for Port 1

Table 8-364. FPD3_TX_MODE_CTL_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	FORCE_LINK_RDY	R/W	0x0	Force Link Ready on Port 1 0: Normal operation 1: Link ready indication is forced. This bypasses back channel link detection and sends link ready on the back channel.
2:0	RESERVED	R/W	X	Reserved

8.6.2.8.9 FPD3_TX_DATAPATH_CTL_P1 Register (Address = 0x13) [Default = 0x42]

FPD3_TX_DATAPATH_CTL_P1 is shown in FPD3_TX_DATAPATH_CTL_P1 Register Field Descriptions.

Return to the Summary Table.

FPD-Link III Daisy Chain Datapath Control for Port 1

Table 8-365. FPD3_TX_DATAPATH_CTL_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	PASS_RGB	R/W	0x1	This bit determines if RGB data can be sent independent of DE, which allows the device to interoperate with the DS90UB926, DS90UB928, DS90UB940, and DS90UB948. Setting this bit prevents HDCP operation and blocks packetized audio. 0: Block RGB data when DE is deasserted 1: Pass RGB data independent of DE
5	DE_POLARITY	R/W	0x0	This bit indicates the polarity of the DE (Data Enable) signal. 0: DE is positive (active high, idle low) 1: DE is inverted (active low, idle high)
4	RESERVED	R/W	0x0	Reserved
3	I2S_TRANSPORT_SEL	R/W	0x0	0: Enable I2S Data Island Transport 1: Enable I2S Data Forward Channel Frame Transport

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Table 8-365. FPD3_TX_DATAPATH_CTL_P1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	VIDEO_18B_EN	R/W	0x0	18-bit Video Select 0: Select 24-bit video mode 1: Select 18-bit video mode
1:0	I2S_MODE	R/W	0x2	I2S Channel Mode 00: 2-channel I2S audio 01: 4-channel I2S audio 10: 5.1- or 7.1-channel surround audio is enabled 11: Reserved Note that I2S Data Island Transport (Bit3= 0) must be set for surround audio.

8.6.2.8.10 FPD3_TX_FIFO_CFG_P1 Register (Address = 0x14) [Default = 0x23]

FPD3_TX_FIFO_CFG_P1 is shown in FPD3_TX_FIFO_CFG_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-366. FPD3_TX_FIFO_CFG_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R/W	0x2	Reserved
3	ENABLE_FPD3_FIFO	R/W	0x0	Enable FPD3 FIFO for Daisy Chain Port 1 This bit must be enabled for the FPD3 link to function. 0: FPD3 TX FIFO disabled 1: FPD3 TX FIFO enabled
2:0	RESERVED	R/W	0x3	Reserved

8.6.2.8.11 FPD3_TX_FIFO_STS_P1 Register (Address = 0x15) [Default = 0x00]

FPD3_TX_FIFO_STS_P1 is shown in FPD3_TX_FIFO_STS_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-367. FPD3_TX_FIFO_STS_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	FPD3_CHAN_ALIGN_ERR	RC	0x0	FPD-Link III Channel Alignment Error 0: No channel alignment error detected 1: Channel alignment error detected
3:0	RESERVED	R	0x0	Reserved

8.6.2.8.12 FPD3_TX_PGCTL_P0 Register (Address = 0x40) [Default = 0x08]

FPD3_TX_PGCTL_P0 is shown in FPD3_TX_PGCTL_P0 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-368. FPD3_TX_PGCTL_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: White and Black Checkerboard 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers on the Pattern Generator register page 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom and Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 0: Enable Pattern Generator synchronous to video input 1: Enable Pattern Generator asynchronous to video input
1	PATCHK_EN	R/W	0x0	Pattern Checker Enable: 0: Disable Pattern Checker 1: Enable Pattern Checker
0	PATGEN_EN	R/W	0x0	Pattern Generator Enable: 0: Disable Pattern Generator 1: Enable Pattern Generator

8.6.2.8.13 FPD3_TX_PGCFG_P0 Register (Address = 0x41) [Default = 0x08]

FPD3_TX_PGCFG_P0 is shown in FPD3_TX_PGCFG_P0 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-369. FPD3_TX_PGCFG_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHKR	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 00: Normal operation (each square is 1x1 pixel) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 11: Scale checkered patterns by 16 (each square is 16x16 pixels)
5	RESERVED	R/W	0x0	Reserved

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Table 8-369. FPD3_TX_PGCFG_P0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 1x: Reserved
2	PATGEN_TSEL	R/W	0x0	Pattern Generator Timing Control 0: External video timing from the pixel clock, DE, HSYNC and VSYNC is used for PATGEN 1: Video timing is configured using these registers on the PATGEN register page: Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration (Note: Not Page 20)
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns 0: Do not invert the color output 1: Invert the color output
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable 0: The Pattern Generator retains the current pattern 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register

8.6.2.8.14 FPD3_TX_PGIA_P0 Register (Address = 0x42) [Default = 0x00]

FPD3_TX_PGIA_P0 is shown in FPD3_TX_PGIA_P0 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-370. FPD3_TX_PGIA_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment for FPD3 TX PATGEN When this bit is 1, reads or writes to the data register (0x43) will automatically increment the indirect address in bits6:0.
6:0	PATGEN_IND_ADDR	R/W	0x0	Indirect Address for FPD3 TX PATGEN Sets the target indirect address for a read or write. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-increment is enabled and the next address is the desired address.

8.6.2.8.15 FPD3_TX_PGID_P0 Register (Address = 0x43) [Default = 0x00]

FPD3_TX_PGID_P0 is shown in FPD3_TX_PGID_P0 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-371. FPD3_TX_PGID_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_IND_DATA	R/W	0x0	Indirect Data for FPD3 TX PATGEN Contains write data when writing to indirect register. Contains read data when reading to indirect register.

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8.6.2.8.16 FPD3_TX_PGTSTDAT_P0 Register (Address = 0x45) [Default = X]

FPD3_TX_PGTSTDAT_P0 is shown in FPD3_TX_PGTSTDAT_P0 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-372. FPD3_TX_PGTSTDAT_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag 0: No errors detected by the pattern checker 1: An error was detected by the pattern checker This bit is cleared by a read to the PGCE register 0x29 on the Pattern Generation Register page.
6	RESERVED	R	X	Reserved
5:0	RESERVED	R	0x0	Reserved

8.6.2.8.17 FPD3_TX_PGCTL_P1 Register (Address = 0x50) [Default = 0x08]

FPD3_TX_PGCTL_P1 is shown in FPD3_TX_PGCTL_P1 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-373. FPD3_TX_PGCTL_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: White and Black Checkerboard 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers on the Pattern Generator register page 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom and Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 0: Enable Pattern Generator synchronous to video input 1: Enable Pattern Generator asynchronous to video input
1	PATCHK_EN	R/W	0x0	Pattern Checker Enable: 0: Disable Pattern Checker 1: Enable Pattern Checker

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Table 8-373. FPD3_TX_PGCTL_P1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	PATGEN_EN	R/W	0x0	Pattern Generator Enable: 0: Disable Pattern Generator 1: Enable Pattern Generator

8.6.2.8.18 FPD3_TX_PGCFG_P1 Register (Address = 0x51) [Default = 0x08]

FPD3_TX_PGCFG_P1 is shown in FPD3_TX_PGCFG_P1 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-374. FPD3_TX_PGCFG_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHKR	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 00: Normal operation (each square is 1x1 pixel) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 11: Scale checkered patterns by 16 (each square is 16x16 pixels)
5	RESERVED	R/W	0x0	Reserved
4:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 00: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 01: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 1x: Reserved
2	PATGEN_TSEL	R/W	0x0	Pattern Generator Timing Control 0: External video timing from the pixel clock, DE, HSYNC and VSYNC is used for PATGEN 1: Video timing is configured using these registers on the PATGEN register page: Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration (Note: Not Page 20)
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns 0: Do not invert the color output 1: Invert the color output
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable 0: The Pattern Generator retains the current pattern 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register

8.6.2.8.19 FPD3_TX_PGIA_P1 Register (Address = 0x52) [Default = 0x00]

FPD3_TX_PGIA_P1 is shown in FPD3_TX_PGIA_P1 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-375. FPD3_TX_PGIA_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment for FPD3 TX PATGEN When this bit is 1, reads or writes to the data register (0x43) will automatically increment the indirect address in bits6:0.

Table 8-375. FPD3_TX_PGIA_P1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	PATGEN_IND_ADDR	R/W	0x0	Indirect Address for FPD3 TX PATGEN Sets the target indirect address for a read or write. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-increment is enabled and the next address is the desired address.

8.6.2.8.20 FPD3_TX_PGID_P1 Register (Address = 0x53) [Default = 0x00]

FPD3_TX_PGID_P1 is shown in FPD3_TX_PGID_P1 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-376. FPD3_TX_PGID_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_IND_DATA	R/W	0x0	Indirect Data for FPD3 TX PATGEN Contains write data when writing to indirect register. Contains read data when reading to indirect register.

8.6.2.8.21 FPD3_TX_PGTSTDAT_P1 Register (Address = 0x55) [Default = X]

FPD3_TX_PGTSTDAT_P1 is shown in FPD3_TX_PGTSTDAT_P1 Register Field Descriptions.

Return to the Summary Table.

These PATGEN registers are for the FPD3 transmitter.

Table 8-377. FPD3_TX_PGTSTDAT_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATCHK_ERR_FLAG	R	0x0	Pattern Checker Error Flag 0: No errors detected by the pattern checker 1: An error was detected by the pattern checker This bit is cleared by a read to the PGCE register 0x29 on the Pattern Generation Register page.
6	RESERVED	R	X	Reserved
5:0	RESERVED	R	X	Reserved

8.6.2.8.22 PRBS_TEST_EN_P0 Register (Address = 0x84) [Default = 0x02]

PRBS_TEST_EN_P0 is shown in PRBS_TEST_EN_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-378. PRBS_TEST_EN_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R/W	0x0	Reserved
2:0	FPD4_ENCODER_MODE	R/W	0x2	FPD4 Encoder Mode 000: PRBS test mode 001: Reserved 010: Normal FPD-Link operation, PRBS test mode disabled 011 - 111: Reserved

8.6.2.8.23 FPD_PRBS_P0 Register (Address = 0x89) [Default = 0x00]

FPD_PRBS_P0 is shown in FPD_PRBS_P0 Register Field Descriptions.

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Return to the Summary Table.

Table 8-379. FPD_PRBS_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	FPD_PRBS_EN	R/W	0x0	Enable PRBS15 Pattern at the FPD Transmitter 0: Disable 1: Enable
2:1	FPD_PRBS_PATT	R/W	0x0	Select PRBS Pattern If testing uisng PRBS, this bit should be set to 0b10. Both 0x89[3] and 0x84[2:0] must be enabled for proper PRBS testing functionality. 00: Reserved 01: Reserved 10: PRBS15 11: Reserved
0	RESERVED	R	0x0	Reserved

8.6.2.8.24 INTR_CTL_FPD4_PORT0 Register (Address = 0x8C) [Default = 0x00]

INTR_CTL_FPD4_PORT0 is shown in INTR_CTL_FPD4_PORT0 Register Field Descriptions.

Return to the Summary Table.

All the interrupt enable bits are independent.

Table 8-380. INTR_CTL_FPD4_PORT0 Register Field Descriptions

Bit	Field	Type	Default	Description
6	IE_DES_LOCK	R/W	0x0	Interrupt Enable for Downstream Deserializer Lock Detect 0: Interrupt disabled 1: Interrupt enabled
5	IE_RX_REM_INT	R/W	0x0	Interrupt Enable for Combination of Back Channel Interrupts from all Downstream Deserializers 0: Interrupt disabled 1: Interrupt enabled
4	IE_DES_INT	R/W	0x0	Interrupt Enable on Downstream Deserializer 0: Interrupt disabled 1: Interrupt enabled
3	IE_RX_LOCK_LOST_DET_INT	R/W	0x0	Interrupt Enable for Downstream Deserializer Lost Lock Detect 0: Interrupt disabled 1: Interrupt enabled
2:0	RESERVED	R	0x0	Reserved

8.6.2.8.25 PRBS_TEST_EN_P1 Register (Address = 0x94) [Default = 0x02]

PRBS_TEST_EN_P1 is shown in PRBS_TEST_EN_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-381. PRBS_TEST_EN_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R/W	0x0	Reserved
2:0	FPD4_ENCODER_MODE	R/W	0x2	FPD4 Encoder Mode 000: PRBS test mode 001: Reserved 010: Normal FPD-Link operation, PRBS test mode disabled 011 - 111: Reserved

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8.6.2.8.26 FPD_PRBS_P1 Register (Address = 0x99) [Default = 0x00]

FPD_PRBS_P1 is shown in FPD_PRBS_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-382. FPD_PRBS_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	FPD_PRBS_EN	R/W	0x0	Enable PRBS15 Pattern at the FPD Transmitter 0: Disable 1: Enable
2:1	FPD_PRBS_PATT	R/W	0x0	Select PRBS Pattern If testing uisng PRBS, this bit should be set to 0b10. Both 0x89[3] and 0x84[2:0] must be enabled for proper PRBS testing functionality. 00: Reserved 01: Reserved 10: PRBS15 11: Reserved
0	RESERVED	R	0x0	Reserved

8.6.2.8.27 INTR_CTL_FPD4_PORT1 Register (Address = 0x9C) [Default = 0x00]

INTR_CTL_FPD4_PORT1 is shown in INTR_CTL_FPD4_PORT1 Register Field Descriptions.

Return to the Summary Table.

All the interrupt enable bits are independent.

Table 8-383. INTR_CTL_FPD4_PORT1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IE_DES_LOCK	R/W	0x0	Interrupt Enable for Downstream Deserializer Lock Detect 0: Interrupt disabled 1: Interrupt enabled
5	IE_RX_REM_INT	R/W	0x0	Interrupt Enable for Combination of Back Channel Interrupts from all Downstream Deserializers 0: Interrupt disabled 1: Interrupt enabled The received interrupts are set in registers 0x44 and 0x52 (for 98x deserializers) on the downstream deserializers.
4	IE_DES_INT	R/W	0x0	Interrupt Enable on Downstream Deserializer 0: Interrupt disabled 1: Interrupt enabled The received interrupts are set in registers 0x44 and 0x52 (for 98x deserializers) on the downstream deserializer.
3	IE_RX_LOCK_LOST_DET_INT	R/W	0x0	Interrupt Enable for Downstream Deserializer Lost Lock Detect 0: Interrupt disabled 1: Interrupt enabled
2:0	RESERVED	R	0x0	Reserved

8.6.2.8.28 INTR_STS_FPD4_PORT1 Register (Address = 0x9D) [Default = 0x00]

INTR_STS_FPD4_PORT1 is shown in INTR_STS_FPD4_PORT1 Register Field Descriptions.

Return to the Summary Table.

Table 8-384. INTR_STS_FPD4_PORT1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

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Table 8-384. INTR_STS_FPD4_PORT1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	IS_DES_LOCK	RC	0x0	Interrupt Status for Downstream Deserializer Lock Detect 0: No interrupt detected 1: Interrupt detected
5	IS_BC_REM_INT	RC	0x0	Interrupt Status for Combination of Back Channel Interrupts from all Downstream Deserializers 0: No interrupt detected 1: Interrupt detected The received interrupts are set in registers 0x44 and 0x52 (for 98x deserializers) on the downstream deserializers.
4	IS_DES_INT	RC	0x0	Interrupt Status on Downstream Deserializer 0: No interrupt detected 1: Interrupt detected, types of interrupts that can be sent are controlled by the interrupt registers on the downstream deserializer. The received interrupts are set in registers 0x44 and 0x52 (for 98x deserializers) on the downstream deserializers.
3	IS_RX_LOCK_LOST_DET_INT	RC	0x0	Interrupt Status for Downstream Deserializer Lost Lock Detect 0: No interrupt detected 1: Interrupt detected
2:0	RESERVED	R	0x0	Reserved

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8.6.2.9 Page 10: FPD3 TX INT Registers

PAGE_10 Registers lists the memory-mapped registers for the Page 10: FPD3 TX INT registers. All register offset addresses not listed in PAGE_10 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-385. PAGE_10 Registers

Address	Acronym	Register Name	Section
0x42	TX_INT_CFG_P0	TX_INT_CFG_P0	Go
0x44	TX_INT_STS_P0	TX_INT_STS_P0	Go
0x46	TX_INT_ICR_P0	TX_INT_ICR_P0	Go
0x47	TX_INT_ISR_P0	TX_INT_ISR_P0	Go
0xC2	TX_INT_CFG_P1	TX_INT_CFG_P1	Go
0xC4	TX_INT_STS_P1	TX_INT_STS_P1	Go
0xC6	TX_INT_ICR_P1	TX_INT_ICR_P1	Go
0xC7	HDCP_ISR_P1	HDCP_ISR_P1	Go

Complex bit access types are encoded to fit into small table cells. Page 10: FPD3 TX INT Access Type Codes shows the codes that are used for access types in this section.

Table 8-386. Page 10: FPD3 TX INT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.9.1 TX_INT_CFG_P0 Register (Address = 0x42) [Default = 0x9A]

TX_INT_CFG_P0 is shown in TX_INT_CFG_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-387. TX_INT_CFG_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:3	RESERVED	R/W	0x3	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RX_DET_SEL	R/W	0x1	RX Detect Select: Controls assertion of the Downstream Interrupt Detect. 0: Downstream Interrupt Detect will be asserted on detection of a downstream FPD-Link Receiver. 1: Downstream Interrupt Detect also requires a LOCK indication from the downstream receiver.
0	RESERVED	R/W	0x0	Reserved

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8.6.2.9.2 TX_INT_STS_P0 Register (Address = 0x44) [Default = 0x00]

TX_INT_STS_P0 is shown in TX_INT_STS_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-388. TX_INT_STS_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RX_INT	R	0x0	RX Interrupt: Status of the INTB_IN pin from the connected downstream deserializer. The signal is received over the back channel. The signal is active low, so a 0 indicates an interrupt condition.
5	RX_LOCK_DET	R	0x0	Receiver Lock Detect: This bit indicates that the downstream deserializer connected to this TX port has indicated Lock to incoming serial data.
4	RESERVED	RC	0x0	Reserved
3	RX_DETECT	R	0x0	Receiver Detect: This bit indicates that a downstream deserializer has been detected.
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

8.6.2.9.3 TX_INT_ICR_P0 Register (Address = 0x46) [Default = 0x00]

TX_INT_ICR_P0 is shown in TX_INT_ICR_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-389. TX_INT_ICR_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	IE_RXDET_INT	R/W	0x0	Interrupt on Receiver Detect: Enables interrupt on detection of a downstream Receiver. If RX_DET_SEL is set to 1, the interrupt will wait for Receiver Lock Detect (RX_LOCK_DET) to be asserted before triggering interrupt.
5	IE_RX_REM_INT	R/W	0x0	Interrupt on Receiver interrupt: Enables interrupt on indication from the downstream Receiver. Allows propagation of interrupts from downstream devices.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	INT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.

8.6.2.9.4 TX_INT_ISR_P0 Register (Address = 0x47) [Default = 0x00]

TX_INT_ISR_P0 is shown in TX_INT_ISR_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-390. TX_INT_ISR_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

Table 8-390. TX_INT_ISR_P0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	IS_RXDET_INT	R	0x0	Interrupt on Receiver Detect interrupt: A downstream receiver has been detected. If RX_DET_SEL is set to 1, the interrupt will wait for Receiver Lock Detect (RX_LOCK_DET) to be asserted before setting this bit.
5	IS_RX_REM_INT	R	0x0	Interrupt on Receiver interrupt: Downstream device has indicated an interrupt request.
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	INT	R	0x0	Global Interrupt Status Set if any enabled interrupt is indicated.

8.6.2.9.5 TX_INT_CFG_P1 Register (Address = 0xC2) [Default = 0x9A]

TX_INT_CFG_P1 is shown in TX_INT_CFG_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-391. TX_INT_CFG_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:3	RESERVED	R/W	0x3	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RX_DET_SEL	R/W	0x1	RX Detect Select: Controls assertion of the Downstream Interrupt Detect. 0: Downstream Interrupt Detect will be asserted on detection of a downstream FPD-Link Receiver. 1: Downstream Interrupt Detect also requires a LOCK indication from the downstream receiver.
0	RESERVED	R/W	0x0	Reserved

8.6.2.9.6 TX_INT_STS_P1 Register (Address = 0xC4) [Default = 0x00]

TX_INT_STS_P1 is shown in TX_INT_STS_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-392. TX_INT_STS_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	RC	0x0	Reserved
6	RX_INT	R	0x0	RX Interrupt: Status of the INTB_IN pin from the connected downstream deserializer. The signal is received over the back channel. The signal is active low, so a 0 indicates an interrupt condition.
5	RX_LOCK_DET	R	0x0	Receiver Lock Detect: This bit indicates that the downstream deserializer connected to this TX port has indicated Lock to incoming serial data.
4	RESERVED	RC	0x0	Reserved
3	RX_DETECT	R	0x0	Receiver Detect: This bit indicates that a downstream deserializer has been detected.

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Table 8-392. TX_INT_STS_P1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

8.6.2.9.7 TX_INT_ICR_P1 Register (Address = 0xC6) [Default = 0x00]

TX_INT_ICR_P1 is shown in TX_INT_ICR_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-393. TX_INT_ICR_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	IE_RXDET_INT	R/W	0x0	Interrupt on Receiver Detect: Enables interrupt on detection of a downstream Receiver. If RX_DET_SEL is set to 1, the interrupt will wait for Receiver Lock Detect (RX_LOCK_DET) to be asserted before triggering interrupt.
5	IE_RX_REM_INT	R/W	0x0	Interrupt on Receiver interrupt: Enables interrupt on indication from the downstream Receiver. Allows propagation of interrupts from downstream devices.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	INT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.

8.6.2.9.8 HDCP_ISR_P1 Register (Address = 0xC7) [Default = 0x00]

HDCP_ISR_P1 is shown in HDCP_ISR_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-394. HDCP_ISR_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	IS_RXDET_INT	R	0x0	Interrupt on Receiver Detect interrupt: A downstream receiver has been detected. If RX_DET_SEL is set to 1, the interrupt will wait for Receiver Lock Detect (RX_LOCK_DET) to be asserted before setting this bit.
5	IS_RX_REM_INT	R	0x0	Interrupt on Receiver interrupt: Downstream device has indicated an interrupt request.
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	INT	R	0x0	Global Interrupt Status Set if any enabled interrupt is indicated.

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8.6.2.10 Page 11: eDP/DP Control Registers

PAGE_11 Registers lists the memory-mapped registers for the Page 11: eDP/DP Control registers. All register offset addresses not listed in PAGE_11 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-395. PAGE_11 Registers

Address	Acronym	Register Name	Section
0x0	DP0_LN0_POL	DP0_LN0_POL	Go
0x2	DP0_LN0_EDP_LOW_VDIFF	DP0_LN0_EDP_LOW_VDIFF	Go
0x3	DP0_LN0_INIT	DP0_LN0_INIT	Go
0x8	DP0_LN1_POL	DP0_LN1_POL	Go
0xA	DP0_LN1_EDP_LOW_VDIFF	DP0_LN1_EDP_LOW_VDIFF	Go
0xB	DP0_LN1_INIT	DP0_LN1_INIT	Go
0x10	DP0_LN2_POL	DP0_LN2_POL	Go
0x12	DP0_LN2_EDP_LOW_VDIFF	DP0_LN2_EDP_LOW_VDIFF	Go
0x13	DP0_LN2_INIT	DP0_LN2_INIT	Go
0x18	DP0_LN3_POL	DP0_LN3_POL	Go
0x1A	DP0_LN3_EDP_LOW_VDIFF	DP0_LN3_EDP_LOW_VDIFF	Go
0x1B	DP0_LN3_INIT	DP0_LN3_INIT	Go
0x20	DP0_LN0_OVD_VAL	DP0_LN0_OVD_VAL	Go
0x24	DP0_LN1_OVD_VAL	DP0_LN1_OVD_VAL	Go
0x28	DP0_LN2_OVD_VAL	DP0_LN2_OVD_VAL	Go
0x2C	DP0_LN3_OVD_VAL	DP0_LN3_OVD_VAL	Go
0x30	DP0_VS_PE_00	DP0_VS_PE_00	Go
0x31	DP0_VS_PE_01	DP0_VS_PE_01	Go
0x32	DP0_VS_PE_02	DP0_VS_PE_02	Go
0x33	DP0_VS_PE_03	DP0_VS_PE_03	Go
0x34	DP0_VS_PE_10	DP0_VS_PE_10	Go
0x35	DP0_VS_PE_11	DP0_VS_PE_11	Go
0x36	DP0_VS_PE_12	DP0_VS_PE_12	Go
0x37	DP0_VS_PE_20	DP0_VS_PE_20	Go
0x38	DP0_VS_PE_21	DP0_VS_PE_21	Go
0x39	DP0_VS_PE_30	DP0_VS_PE_30	Go
0x3D	DP0_AUX_POL	DP0_AUX_POL	Go
0x3E	DP0_OVD_SEL	DP0_OVD_SEL	Go
0x40	DP1_LN0_POL	DP1_LN0_POL	Go
0x42	DP1_LN0_EDP_LOW_VDIFF	DP1_LN0_EDP_LOW_VDIFF	Go
0x43	DP1_LN0_INIT	DP1_LN0_INIT	Go
0x48	DP1_LN1_POL	DP1_LN1_POL	Go
0x4A	DP1_LN1_EDP_LOW_VDIFF	DP1_LN1_EDP_LOW_VDIFF	Go
0x4B	DP1_LN1_INIT	DP1_LN1_INIT	Go
0x50	DP1_LN2_POL	DP1_LN2_POL	Go
0x52	DP1_LN2_EDP_LOW_VDIFF	DP1_LN2_EDP_LOW_VDIFF	Go
0x53	DP1_LN2_INIT	DP1_LN2_INIT	Go
0x58	DP1_LN3_POL	DP1_LN3_POL	Go
0x5A	DP1_LN3_EDP_LOW_VDIFF	DP1_LN3_EDP_LOW_VDIFF	Go
0x5B	DP1_LN3_INIT	DP1_LN3_INIT	Go
0x60	DP1_LN0_OVD_VAL	DP1_LN0_OVD_VAL	Go

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Table 8-395. PAGE_11 Registers (continued)

Address	Acronym	Register Name	Section
0x64	DP1_LN1_OVD_VAL	DP1_LN1_OVD_VAL	Go
0x68	DP1_LN2_OVD_VAL	DP1_LN2_OVD_VAL	Go
0x6C	DP1_LN3_OVD_VAL	DP1_LN3_OVD_VAL	Go
0x70	DP1_VS_PE_00	DP1_VS_PE_00	Go
0x71	DP1_VS_PE_01	DP1_VS_PE_01	Go
0x72	DP1_VS_PE_02	DP1_VS_PE_02	Go
0x73	DP1_VS_PE_03	DP1_VS_PE_03	Go
0x74	DP1_VS_PE_10	DP1_VS_PE_10	Go
0x75	DP1_VS_PE_11	DP1_VS_PE_11	Go
0x76	DP1_VS_PE_12	DP1_VS_PE_12	Go
0x77	DP1_VS_PE_20	DP1_VS_PE_20	Go
0x78	DP1_VS_PE_21	DP1_VS_PE_21	Go
0x79	DP1_VS_PE_30	DP1_VS_PE_30	Go
0x7D	DP1_AUX_POL	DP1_AUX_POL	Go
0x7E	DP1_OVD_SEL	DP1_OVD_SEL	Go
0x81	DP_FIXED_RATE_VAL	DP_FIXED_RATE_VAL	Go
0x82	DP_RATE_BYPASS	DP_RATE_BYPASS	Go
0x90	DP0_LANE_REMAP	DP0_LANE_REMAP	Go
0x91	DP0_OVD_HPD	DP0_OVD_HPD	Go
0x93	DP0_EQ_STS	DP0_EQ_STS	Go
0x9D	DP0_BACKLIGHT_CTL_0	DP0_BACKLIGHT_CTL_0	Go
0x9E	DP0_BACKLIGHT_CTL_1	DP0_BACKLIGHT_CTL_1	Go
0x9F	DP0_BACKLIGHT_SCALE_0	DP0_BACKLIGHT_SCALE_0	Go
0xA0	DP0_BACKLIGHT_SCALE_1	DP0_BACKLIGHT_SCALE_1	Go
0xA1	DP0_BACKLIGHT_PRESCALE_DIV	DP0_BACKLIGHT_PRESCALE_DIV	Go
0xA2	DP0_PWM_CTL	DP0_PWM_CTL	Go
0xA5	DP0_OVD_LINK_RATE	DP0_OVD_LINK_RATE	Go
0xA6	DP0_CONFG_TEST	DP0_CONFG_TEST	Go
0xA7	DP0_OVD_EN_HTOTAL	DP0_OVD_EN_HTOTAL	Go
0xA8	DP0_OVD_VAL_HTOTAL_LSB	DP0_OVD_VAL_HTOTAL_LSB	Go
0xA9	DP0_OVD_VAL_HTOTAL_MSB	DP0_OVD_VAL_HTOTAL_MSB	Go
0xB0	DP1_LANE_REMAP	DP1_LANE_REMAP	Go
0xB1	DP1_OVD_HPD	DP1_OVD_HPD	Go
0xB3	DP1_EQ_STS	DP1_EQ_STS	Go
0xBD	DP1_BACKLIGHT_CTL_0	DP1_BACKLIGHT_CTL_0	Go
0xBE	DP1_BACKLIGHT_CTL_1	DP1_BACKLIGHT_CTL_1	Go
0xBF	DP1_BACKLIGHT_SCALE_0	DP1_BACKLIGHT_SCALE_0	Go
0xC0	DP1_BACKLIGHT_SCALE_1	DP1_BACKLIGHT_SCALE_1	Go
0xC1	DP1_BACKLIGHT_PRESCALE_DIV	DP1_BACKLIGHT_PRESCALE_DIV	Go
0xC2	DP1_PWM_CTL	DP1_PWM_CTL	Go
0xC5	DP1_OVD_LINK_RATE	DP1_OVD_LINK_RATE	Go
0xC6	DP1_CONFG_TEST	DP1_CONFG_TEST	Go
0xC7	DP1_OVD_EN_HTOTAL	DP1_OVD_EN_HTOTAL	Go
0xC8	DP1_OVD_VAL_HTOTAL_LSB	DP1_OVD_VAL_HTOTAL_LSB	Go

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Table 8-395. PAGE_11 Registers (continued)

Address	Acronym	Register Name	Section
0xC9	DP1_OVD_VAL_HTOTAL_MSB	DP1_OVD_VAL_HTOTAL_MSB	Go
0xD0	DP0_TX_ICR	DP0_TX_ICR	Go
0xD1	DP0_TX_CORE_ICR	DP0_TX_CORE_ICR	Go
0xD2	DP0_PORT_SM_ICR	DP0_PORT_SM_ICR	Go
0xD3	DP0_HPD_IRQ_ICR0	DP0_HPD_IRQ_ICR0	Go
0xD4	DP0_HPD_IRQ_ICR1	DP0_HPD_IRQ_ICR1	Go
0xD5	DP0_AUTO_TEST_ICR	DP0_AUTO_TEST_ICR	Go
0xD8	DP0_TX_ISR	DP0_TX_ISR	Go
0xD9	DP0_TX_CORE_ISR	DP0_TX_CORE_ISR	Go
0xDA	DP0_PORT_SM_ISR	DP0_PORT_SM_ISR	Go
0xDB	DP0_HPD_IRQ_ISR0	DP0_HPD_IRQ_ISR0	Go
0xDC	DP0_HPD_IRQ_ISR1	DP0_HPD_IRQ_ISR1	Go
0xDD	DP0_AUTO_TEST_ISR	DP0_AUTO_TEST_ISR	Go
0xE0	DP1_TX_ICR	DP1_TX_ICR	Go
0xE1	DP1_TX_CORE_ICR	DP1_TX_CORE_ICR	Go
0xE2	DP1_PORT_SM_ICR	DP1_PORT_SM_ICR	Go
0xE3	DP1_HPD_IRQ_ICR0	DP1_HPD_IRQ_ICR0	Go
0xE4	DP1_HPD_IRQ_ICR1	DP1_HPD_IRQ_ICR1	Go
0xE5	DP1_AUTO_TEST_ICR	DP1_AUTO_TEST_ICR	Go
0xE8	DP1_TX_ISR	DP1_TX_ISR	Go
0xE9	DP1_TX_CORE_ISR	DP1_TX_CORE_ISR	Go
0xEA	DP1_PORT_SM_ISR	DP1_PORT_SM_ISR	Go
0xEB	DP1_HPD_IRQ_ISR0	DP1_HPD_IRQ_ISR0	Go
0xEC	DP1_HPD_IRQ_ISR1	DP1_HPD_IRQ_ISR1	Go
0xED	DP1_AUTO_TEST_ISR	DP1_AUTO_TEST_ISR	Go

Complex bit access types are encoded to fit into small table cells. Page 11: eDP/DP Control Access Type Codes shows the codes that are used for access types in this section.

Table 8-396. Page 11: eDP/DP Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.10.1 DP0_LN0_POL Register (Address = 0x0) [Default = 0x20]

DP0_LN0_POL is shown in DP0_LN0_POL Register Field Descriptions.

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Table 8-397. DP0_LN0_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	LN_POL_SEL	R/W	0x1	DP Port0 Lane0 Polarity Inversion Switch the polarity of these lane pins by changing the default value of this register. 0: Switch polarity of the P/N pins for this lane 1: Keep the default polarity (as defined in the Pin Functions table) Note: The default value of this register is different across different DPx_LNx_POL registers.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.2 DP0_LN0_EDP_LOW_VDIFF Register (Address = 0x2) [Default = 0x06]

DP0_LN0_EDP_LOW_VDIFF is shown in DP0_LN0_EDP_LOW_VDIFF Register Field Descriptions.

Return to the Summary Table.

Table 8-398. DP0_LN0_EDP_LOW_VDIFF Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x3	Reserved
0	EDP_LOW_VDIFF_SUPPORT	R/W	0x0	eDP Low Vdiff Support Set this bit to 1 to enable the use of the low Vdiff training table for eDP. Training tables are in accordance with VESA Embedded DisplayPort (eDP) Standard v1.4b.

8.6.2.10.3 DP0_LN0_INIT Register (Address = 0x3) [Default = 0x00]

DP0_LN0_INIT is shown in DP0_LN0_INIT Register Field Descriptions.

Return to the Summary Table.

Table 8-399. DP0_LN0_INIT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	INIT_VOD_SEL	R/W	0x0	DP Port0 Lane0 Initial Voltage Swing Level Selection
5:4	INIT_PRE_SEL	R/W	0x0	DP Port0 Lane0 Initial Pre-emphasis Level Selection
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.4 DP0_LN1_POL Register (Address = 0x8) [Default = 0x00]

DP0_LN1_POL is shown in DP0_LN1_POL Register Field Descriptions.

Return to the Summary Table.

Table 8-400. DP0_LN1_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

Table 8-400. DP0_LN1_POL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	LN_POL_SEL	R/W	0x0	DP Port0 Lane1 Polarity Inversion Switch the polarity of these lane pins by changing the default value of this register. 0: Keep the default polarity (as defined in the Pin Functions table) 1: Switch polarity of the P/N pins for this lane Note: The default value of this register is different across different DPx_LNx_POL registers.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.5 DP0_LN1_EDP_LOW_VDIFF Register (Address = 0xA) [Default = 0x06]

DP0_LN1_EDP_LOW_VDIFF is shown in DP0_LN1_EDP_LOW_VDIFF Register Field Descriptions.

Return to the Summary Table.

Table 8-401. DP0_LN1_EDP_LOW_VDIFF Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x3	Reserved
0	EDP_LOW_VDIFF_SUPPORT	R/W	0x0	eDP Low Vdiff Support Set this bit to 1 to enable the use of the low Vdiff training table for eDP. Training tables are in accordance with VESA Embedded DisplayPort (eDP) Standard v1.4b.

8.6.2.10.6 DP0_LN1_INIT Register (Address = 0xB) [Default = 0x00]

DP0_LN1_INIT is shown in DP0_LN1_INIT Register Field Descriptions.

Return to the Summary Table.

Table 8-402. DP0_LN1_INIT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	INIT_VOD_SEL	R/W	0x0	DP Port0 Lane1 Initial Voltage Swing Level Selection
5:4	INIT_PRE_SEL	R/W	0x0	DP Port0 Lane1 Initial Pre-emphasis Level Selection
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.7 DP0_LN2_POL Register (Address = 0x10) [Default = 0x20]

DP0_LN2_POL is shown in DP0_LN2_POL Register Field Descriptions.

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Table 8-403. DP0_LN2_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

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Table 8-403. DP0_LN2_POL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	LN_POL_SEL	R/W	0x1	DP Port0 Lane2 Polarity Inversion Switch the polarity of these lane pins by changing the default value of this register. 0: Switch polarity of the P/N pins for this lane 1: Keep the default polarity (as defined in the Pin Functions table) Note: The default value of this register is different across different DPx_LNx_POL registers.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.8 DP0_LN2_EDP_LOW_VDIFF Register (Address = 0x12) [Default = 0x06]

DP0_LN2_EDP_LOW_VDIFF is shown in DP0_LN2_EDP_LOW_VDIFF Register Field Descriptions.

Return to the Summary Table.

Table 8-404. DP0_LN2_EDP_LOW_VDIFF Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x3	Reserved
0	EDP_LOW_VDIFF_SUPPORT	R/W	0x0	eDP Low Vdiff Support Set this bit to 1 to enable the use of the low Vdiff training table for eDP. Training tables are in accordance with VESA Embedded DisplayPort (eDP) Standard v1.4b.

8.6.2.10.9 DP0_LN2_INIT Register (Address = 0x13) [Default = 0x00]

DP0_LN2_INIT is shown in DP0_LN2_INIT Register Field Descriptions.

Return to the Summary Table.

Table 8-405. DP0_LN2_INIT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	INIT_VOD_SEL	R/W	0x0	DP Port0 Lane2 Initial Voltage Swing Level Selection
5:4	INIT_PRE_SEL	R/W	0x0	DP Port0 Lane2 Initial Pre-emphasis Level Selection
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.10 DP0_LN3_POL Register (Address = 0x18) [Default = 0x00]

DP0_LN3_POL is shown in DP0_LN3_POL Register Field Descriptions.

Return to the Summary Table.

Table 8-406. DP0_LN3_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

Table 8-406. DP0_LN3_POL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	LN_POL_SEL	R/W	0x0	DP Port0 Lane3 Polarity Inversion Switch the polarity of these lane pins by changing the default value of this register. 0: Keep the default polarity (as defined in the Pin Functions table) 1: Switch polarity of the P/N pins for this lane Note: The default value of this register is different across different DPx_LNx_POL registers.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.11 DP0_LN3_EDP_LOW_VDIFF Register (Address = 0x1A) [Default = 0x06]

DP0_LN3_EDP_LOW_VDIFF is shown in DP0_LN3_EDP_LOW_VDIFF Register Field Descriptions.

Return to the Summary Table.

Table 8-407. DP0_LN3_EDP_LOW_VDIFF Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x3	Reserved
0	EDP_LOW_VDIFF_SUPPORT	R/W	0x0	eDP Low Vdiff Support Set this bit to 1 to enable the use of the low Vdiff training table for eDP. Training tables are in accordance with VESA Embedded DisplayPort (eDP) Standard v1.4b.

8.6.2.10.12 DP0_LN3_INIT Register (Address = 0x1B) [Default = 0x00]

DP0_LN3_INIT is shown in DP0_LN3_INIT Register Field Descriptions.

Return to the Summary Table.

Table 8-408. DP0_LN3_INIT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	INIT_VOD_SEL	R/W	0x0	DP Port0 Lane3 Initial Voltage Swing Level Selection
5:4	INIT_PRE_SEL	R/W	0x0	DP Port0 Lane3 Initial Pre-emphasis Level Selection
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.13 DP0_LN0_OVD_VAL Register (Address = 0x20) [Default = 0x00]

DP0_LN0_OVD_VAL is shown in DP0_LN0_OVD_VAL Register Field Descriptions.

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Table 8-409. DP0_LN0_OVD_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DRV_SEL_PE_OV	R/W	0x0	DP Port0 Lane0 Pre-emphasis Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x30-0x39 to select a specific pre-emphasis level in this register.
3:0	DRV_SEL_VS_OV	R/W	0x0	DP Port0 Lane0 Voltage Swing Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x30-0x39 to select a specific voltage swing level in this register.

8.6.2.10.14 DP0_LN1_OVD_VAL Register (Address = 0x24) [Default = 0x00]

DP0_LN1_OVD_VAL is shown in DP0_LN1_OVD_VAL Register Field Descriptions.

Return to the Summary Table.

Table 8-410. DP0_LN1_OVD_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DRV_SEL_PE_OV	R/W	0x0	DP Port0 Lane1 Pre-emphasis Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x30-0x39 to select a specific pre-emphasis level in this register.
3:0	DRV_SEL_VS_OV	R/W	0x0	DP Port0 Lane1 Voltage Swing Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x30-0x39 to select a specific voltage swing level in this register.

8.6.2.10.15 DP0_LN2_OVD_VAL Register (Address = 0x28) [Default = 0x00]

DP0_LN2_OVD_VAL is shown in DP0_LN2_OVD_VAL Register Field Descriptions.

Return to the Summary Table.

Table 8-411. DP0_LN2_OVD_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DRV_SEL_PE_OV	R/W	0x0	DP Port0 Lane2 Pre-emphasis Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x30-0x39 to select a specific pre-emphasis level in this register.
3:0	DRV_SEL_VS_OV	R/W	0x0	DP Port0 Lane2 Voltage Swing Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x30-0x39 to select a specific voltage swing level in this register.

8.6.2.10.16 DP0_LN3_OVD_VAL Register (Address = 0x2C) [Default = 0x00]

DP0_LN3_OVD_VAL is shown in DP0_LN3_OVD_VAL Register Field Descriptions.

Return to the Summary Table.

Table 8-412. DP0_LN3_OVD_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DRV_SEL_PE_OV	R/W	0x0	DP Port0 Lane3 Pre-emphasis Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x30-0x39 to select a specific pre-emphasis level in this register.

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Table 8-412. DP0_LN3_OVD_VAL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	DRV_SEL_VS_OV	R/W	0x0	DP Port0 Lane3 Voltage Swing Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x30-0x39 to select a specific voltage swing level in this register.

8.6.2.10.17 DP0_VS_PE_00 Register (Address = 0x30) [Default = 0x20]

DP0_VS_PE_00 is shown in DP0_VS_PE_00 Register Field Descriptions.

Return to the Summary Table.

Table 8-413. DP0_VS_PE_00 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL00	R/W	0x2	DP Port0 Training Table Voltage Swing Level 0
3:0	DP_POST_SEL00	R/W	0x0	DP Port0 Training Table Pre-emphasis Level 0

8.6.2.10.18 DP0_VS_PE_01 Register (Address = 0x31) [Default = 0x53]

DP0_VS_PE_01 is shown in DP0_VS_PE_01 Register Field Descriptions.

Return to the Summary Table.

Table 8-414. DP0_VS_PE_01 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL01	R/W	0x5	DP Port0 Training Table Voltage Swing Level 0
3:0	DP_POST_SEL01	R/W	0x3	DP Port0 Training Table Pre-emphasis Level 1

8.6.2.10.19 DP0_VS_PE_02 Register (Address = 0x32) [Default = 0x96]

DP0_VS_PE_02 is shown in DP0_VS_PE_02 Register Field Descriptions.

Return to the Summary Table.

Table 8-415. DP0_VS_PE_02 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL02	R/W	0x9	DP Port0 Training Table Voltage Swing Level 0
3:0	DP_POST_SEL02	R/W	0x6	DP Port0 Training Table Pre-emphasis Level 2

8.6.2.10.20 DP0_VS_PE_03 Register (Address = 0x33) [Default = 0xDA]

DP0_VS_PE_03 is shown in DP0_VS_PE_03 Register Field Descriptions.

Return to the Summary Table.

Table 8-416. DP0_VS_PE_03 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL03	R/W	0xD	DP Port0 Training Table Voltage Swing Level 0
3:0	DP_POST_SEL03	R/W	0xA	DP Port0 Training Table Pre-emphasis Level 3

8.6.2.10.21 DP0_VS_PE_10 Register (Address = 0x34) [Default = 0x50]

DP0_VS_PE_10 is shown in DP0_VS_PE_10 Register Field Descriptions.

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Return to the Summary Table.

Table 8-417. DP0_VS_PE_10 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL10	R/W	0x5	DP Port0 Training Table Voltage Swing Level 1
3:0	DP_POST_SEL10	R/W	0x0	DP Port0 Training Table Pre-emphasis Level 0

8.6.2.10.22 DP0_VS_PE_11 Register (Address = 0x35) [Default = 0xA4]

DP0_VS_PE_11 is shown in DP0_VS_PE_11 Register Field Descriptions.

Return to the Summary Table.

Table 8-418. DP0_VS_PE_11 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL11	R/W	0xA	DP Port0 Training Table Voltage Swing Level 1
3:0	DP_POST_SEL11	R/W	0x4	DP Port0 Training Table Pre-emphasis Level 1

8.6.2.10.23 DP0_VS_PE_12 Register (Address = 0x36) [Default = 0xD7]

DP0_VS_PE_12 is shown in DP0_VS_PE_12 Register Field Descriptions.

Return to the Summary Table.

Table 8-419. DP0_VS_PE_12 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL12	R/W	0xD	DP Port0 Training Table Voltage Swing Level 1
3:0	DP_POST_SEL12	R/W	0x7	DP Port0 Training Table Pre-emphasis Level 2

8.6.2.10.24 DP0_VS_PE_20 Register (Address = 0x37) [Default = 0x90]

DP0_VS_PE_20 is shown in DP0_VS_PE_20 Register Field Descriptions.

Return to the Summary Table.

Table 8-420. DP0_VS_PE_20 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL20	R/W	0x9	DP Port0 Training Table Voltage Swing Level 2
3:0	DP_POST_SEL20	R/W	0x0	DP Port0 Training Table Pre-emphasis Level 0

8.6.2.10.25 DP0_VS_PE_21 Register (Address = 0x38) [Default = 0xD4]

DP0_VS_PE_21 is shown in DP0_VS_PE_21 Register Field Descriptions.

Return to the Summary Table.

Table 8-421. DP0_VS_PE_21 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL21	R/W	0xD	DP Port0 Training Table Voltage Swing Level 2
3:0	DP_POST_SEL21	R/W	0x4	DP Port0 Training Table Pre-emphasis Level 1

8.6.2.10.26 DP0_VS_PE_30 Register (Address = 0x39) [Default = 0xD0]

DP0_VS_PE_30 is shown in DP0_VS_PE_30 Register Field Descriptions.

Return to the Summary Table.

Table 8-422. DP0_VS_PE_30 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL30	R/W	0xD	DP Port0 Training Table Voltage Swing Level 3
3:0	DP_POST_SEL30	R/W	0x0	DP Port0 Training Table Pre-emphasis Level 0

8.6.2.10.27 DP0_AUX_POL Register (Address = 0x3D) [Default = 0xD5]

DP0_AUX_POL is shown in DP0_AUX_POL Register Field Descriptions.

Return to the Summary Table.

Table 8-423. DP0_AUX_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7	AUX_DATA_OUT_POL	R/W	0x1	DP Port0 AUX RX Polarity Inversion
6	AUX_DATA_IN_POL	R/W	0x1	DP Port0 AUX TX Polarity Inversion
5:0	AUX_R1_EN	R/W	0x15	DP Port0 AUX TX Voltage Swing Level. Controls the output voltage swing of the AUX channel (VOD). The range of the AUX voltage swing is between 0.2V to 1.15V and is set by increasing the value in this register. Starting at 0.2V, there is an increment of approximately 18mV in the voltage swing as you increase the value in this register. 001011: 0.2V AUX voltage swing (Min) 010111: 0.42V AUX voltage swing (Default) 111111: 1.15V AUX voltage swing (Max) Note: AUX_R1_EN must be equal to AUX_R2_EN in order to maintain output impedance.

8.6.2.10.28 DP0_OVD_SEL Register (Address = 0x3E) [Default = 0x15]

DP0_OVD_SEL is shown in DP0_OVD_SEL Register Field Descriptions.

Return to the Summary Table.

Table 8-424. DP0_OVD_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7	DRV_OV_SEL	R/W	0x0	Override select for Port 0 DRV_SEL_PE_OV and DRV_SEL_VS_OV. 0: Control is from state machine 1: Control is from DRV_SEL_PE_OV and DRV_SEL_VS_OV register bits (per lane values)
6	RESERVED	R	0x0	Reserved
5:0	AUX_R2_EN	R/W	0x15	DP Port0 AUX TX Voltage Swing Level. Controls the output voltage swing of the AUX channel (VOD). The range of the AUX voltage swing is between 0.2V to 1.15V and is set by increasing the value in this register. Starting at 0.2V, there is an increment of approximately 18mV in the voltage swing as you increase the value in this register. 001011: 0.2V AUX voltage swing (Min) 010111: 0.42V AUX voltage swing (Default) 111111: 1.15V AUX voltage swing (Max) Note: AUX_R1_EN must be equal to AUX_R2_EN in order to maintain output impedance.

8.6.2.10.29 DP1_LN0_POL Register (Address = 0x40) [Default = 0x20]

DP1_LN0_POL is shown in DP1_LN0_POL Register Field Descriptions.

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Table 8-425. DP1_LN0_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	LN_POL_SEL	R/W	0x1	DP Port1 Lane0 Polarity Inversion Switch the polarity of these lane pins by changing the default value of this register. 0: Switch polarity of the P/N pins for this lane 1: Keep the default polarity (as defined in the Pin Functions table) Note: The default value of this register is different across different DPx_LNx_POL registers.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.30 DP1_LN0_EDP_LOW_VDIFF Register (Address = 0x42) [Default = 0x06]

DP1_LN0_EDP_LOW_VDIFF is shown in DP1_LN0_EDP_LOW_VDIFF Register Field Descriptions.

Return to the Summary Table.

Table 8-426. DP1_LN0_EDP_LOW_VDIFF Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x3	Reserved
0	EDP_LOW_VDIFF_SUPPORT	R/W	0x0	eDP Low Vdiff Support Set this bit to 1 to enable the use of the low Vdiff training table for eDP. Training tables are in accordance with VESA Embedded DisplayPort (eDP) Standard v1.4b.

8.6.2.10.31 DP1_LN0_INIT Register (Address = 0x43) [Default = 0x00]

DP1_LN0_INIT is shown in DP1_LN0_INIT Register Field Descriptions.

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Table 8-427. DP1_LN0_INIT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	INIT_VOD_SEL	R/W	0x0	DP Port1 Lane0 Initial Voltage Swing Level Selection
5:4	INIT_PRE_SEL	R/W	0x0	DP Port1 Lane0 Initial Pre-emphasis Level Selection
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.32 DP1_LN1_POL Register (Address = 0x48) [Default = 0x00]

DP1_LN1_POL is shown in DP1_LN1_POL Register Field Descriptions.

Return to the Summary Table.

Table 8-428. DP1_LN1_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	LN_POL_SEL	R/W	0x0	DP Port1 Lane1 Polarity Inversion Switch the polarity of these lane pins by changing the default value of this register. 0: Keep the default polarity (as defined in the Pin Functions table) 1: Switch polarity of the P/N pins for this lane Note: The default value of this register is different across different DPx_LNx_POL registers.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.33 DP1_LN1_EDP_LOW_VDIFF Register (Address = 0x4A) [Default = 0x06]

DP1_LN1_EDP_LOW_VDIFF is shown in DP1_LN1_EDP_LOW_VDIFF Register Field Descriptions.

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Table 8-429. DP1_LN1_EDP_LOW_VDIFF Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x3	Reserved
0	EDP_LOW_VDIFF_SUPPORT	R/W	0x0	eDP Low Vdiff Support Set this bit to 1 to enable the use of the low Vdiff training table for eDP. Training tables are in accordance with VESA Embedded DisplayPort (eDP) Standard v1.4b.

8.6.2.10.34 DP1_LN1_INIT Register (Address = 0x4B) [Default = 0x00]

DP1_LN1_INIT is shown in DP1_LN1_INIT Register Field Descriptions.

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Table 8-430. DP1_LN1_INIT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	INIT_VOD_SEL	R/W	0x0	DP Port1 Lane1 Initial Voltage Swing Level Selection
5:4	INIT_PRE_SEL	R/W	0x0	DP Port1 Lane1 Initial Pre-emphasis Level Selection
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.35 DP1_LN2_POL Register (Address = 0x50) [Default = 0x20]

DP1_LN2_POL is shown in DP1_LN2_POL Register Field Descriptions.

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Table 8-431. DP1_LN2_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

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Table 8-431. DP1_LN2_POL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	LN_POL_SEL	R/W	0x1	DP Port1 Lane2 Polarity Inversion Switch the polarity of these lane pins by changing the default value of this register. 0: Switch polarity of the P/N pins for this lane 1: Keep the default polarity (as defined in the Pin Functions table) Note: The default value of this register is different across different DPx_LNx_POL registers.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.36 DP1_LN2_EDP_LOW_VDIFF Register (Address = 0x52) [Default = 0x06]

DP1_LN2_EDP_LOW_VDIFF is shown in DP1_LN2_EDP_LOW_VDIFF Register Field Descriptions.

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Table 8-432. DP1_LN2_EDP_LOW_VDIFF Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x3	Reserved
0	EDP_LOW_VDIFF_SUPPORT	R/W	0x0	eDP Low Vdiff Support Set this bit to 1 to enable the use of the low Vdiff training table for eDP. Training tables are in accordance with VESA Embedded DisplayPort (eDP) Standard v1.4b.

8.6.2.10.37 DP1_LN2_INIT Register (Address = 0x53) [Default = 0x00]

DP1_LN2_INIT is shown in DP1_LN2_INIT Register Field Descriptions.

Return to the Summary Table.

Table 8-433. DP1_LN2_INIT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	INIT_VOD_SEL	R/W	0x0	DP Port1 Lane2 Initial Voltage Swing Level Selection
5:4	INIT_PRE_SEL	R/W	0x0	DP Port1 Lane2 Initial Pre-emphasis Level Selection
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.38 DP1_LN3_POL Register (Address = 0x58) [Default = 0x00]

DP1_LN3_POL is shown in DP1_LN3_POL Register Field Descriptions.

Return to the Summary Table.

Table 8-434. DP1_LN3_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

Table 8-434. DP1_LN3_POL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	LN_POL_SEL	R/W	0x0	DP Port1 Lane3 Polarity Inversion Switch the polarity of these lane pins by changing the default value of this register. 0: Keep the default polarity (as defined in the Pin Functions table) 1: Switch polarity of the P/N pins for this lane Note: The default value of this register is different across different DPx_LNx_POL registers.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.39 DP1_LN3_EDP_LOW_VDIFF Register (Address = 0x5A) [Default = 0x06]

DP1_LN3_EDP_LOW_VDIFF is shown in DP1_LN3_EDP_LOW_VDIFF Register Field Descriptions.

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Table 8-435. DP1_LN3_EDP_LOW_VDIFF Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x3	Reserved
0	EDP_LOW_VDIFF_SUPPORT	R/W	0x0	eDP Low Vdiff Support Set this bit to 1 to enable the use of the low Vdiff training table for eDP. Training tables are in accordance with VESA Embedded DisplayPort (eDP) Standard v1.4b.

8.6.2.10.40 DP1_LN3_INIT Register (Address = 0x5B) [Default = 0x00]

DP1_LN3_INIT is shown in DP1_LN3_INIT Register Field Descriptions.

Return to the Summary Table.

Table 8-436. DP1_LN3_INIT Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	INIT_VOD_SEL	R/W	0x0	DP Port1 Lane3 Initial Voltage Swing Level Selection
5:4	INIT_PRE_SEL	R/W	0x0	DP Port1 Lane3 Initial Pre-emphasis Level Selection
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.41 DP1_LN0_OVD_VAL Register (Address = 0x60) [Default = 0x00]

DP1_LN0_OVD_VAL is shown in DP1_LN0_OVD_VAL Register Field Descriptions.

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Table 8-437. DP1_LN0_OVD_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DRV_SEL_PE_OV	R/W	0x0	DP Port1 Lane0 Pre-emphasis Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x70-0x79 to select a specific pre-emphasis level in this register.
3:0	DRV_SEL_VS_OV	R/W	0x0	DP Port1 Lane0 Voltage Swing Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x70-0x79 to select a specific voltage swing level in this register.

8.6.2.10.42 DP1_LN1_OVD_VAL Register (Address = 0x64) [Default = 0x00]

DP1_LN1_OVD_VAL is shown in DP1_LN1_OVD_VAL Register Field Descriptions.

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Table 8-438. DP1_LN1_OVD_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DRV_SEL_PE_OV	R/W	0x0	DP Port1 Lane1 Pre-emphasis Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x70-0x79 to select a specific pre-emphasis level in this register.
3:0	DRV_SEL_VS_OV	R/W	0x0	DP Port1 Lane1 Voltage Swing Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x70-0x79 to select a specific voltage swing level in this register.

8.6.2.10.43 DP1_LN2_OVD_VAL Register (Address = 0x68) [Default = 0x00]

DP1_LN2_OVD_VAL is shown in DP1_LN2_OVD_VAL Register Field Descriptions.

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Table 8-439. DP1_LN2_OVD_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DRV_SEL_PE_OV	R/W	0x0	DP Port1 Lane2 Pre-emphasis Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x70-0x79 to select a specific pre-emphasis level in this register.
3:0	DRV_SEL_VS_OV	R/W	0x0	DP Port1 Lane2 Voltage Swing Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x70-0x79 to select a specific voltage swing level in this register.

8.6.2.10.44 DP1_LN3_OVD_VAL Register (Address = 0x6C) [Default = 0x00]

DP1_LN3_OVD_VAL is shown in DP1_LN3_OVD_VAL Register Field Descriptions.

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Table 8-440. DP1_LN3_OVD_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DRV_SEL_PE_OV	R/W	0x0	DP Port1 Lane3 Pre-emphasis Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x70-0x79 to select a specific pre-emphasis level in this register.

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Table 8-440. DP1_LN3_OVD_VAL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	DRV_SEL_VS_OV	R/W	0x0	DP Port1 Lane3 Voltage Swing Level Override Value. Active when DRV_OV_SEL= 1. Reference the default values in registers 0x70-0x79 to select a specific voltage swing level in this register.

8.6.2.10.45 DP1_VS_PE_00 Register (Address = 0x70) [Default = 0x20]

DP1_VS_PE_00 is shown in DP1_VS_PE_00 Register Field Descriptions.

Return to the Summary Table.

Table 8-441. DP1_VS_PE_00 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL00	R/W	0x2	DP Port1 Training Table Voltage Swing Level 0
3:0	DP_POST_SEL00	R/W	0x0	DP Port1 Training Table Pre-emphasis Level 0

8.6.2.10.46 DP1_VS_PE_01 Register (Address = 0x71) [Default = 0x53]

DP1_VS_PE_01 is shown in DP1_VS_PE_01 Register Field Descriptions.

Return to the Summary Table.

Table 8-442. DP1_VS_PE_01 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL01	R/W	0x5	DP Port1 Training Table Voltage Swing Level 0
3:0	DP_POST_SEL01	R/W	0x3	DP Port1 Training Table Pre-emphasis Level 1

8.6.2.10.47 DP1_VS_PE_02 Register (Address = 0x72) [Default = 0x96]

DP1_VS_PE_02 is shown in DP1_VS_PE_02 Register Field Descriptions.

Return to the Summary Table.

Table 8-443. DP1_VS_PE_02 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL02	R/W	0x9	DP Port1 Training Table Voltage Swing Level 0
3:0	DP_POST_SEL02	R/W	0x6	DP Port1 Training Table Pre-emphasis Level 2

8.6.2.10.48 DP1_VS_PE_03 Register (Address = 0x73) [Default = 0xDA]

DP1_VS_PE_03 is shown in DP1_VS_PE_03 Register Field Descriptions.

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Table 8-444. DP1_VS_PE_03 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL03	R/W	0xD	DP Port1 Training Table Voltage Swing Level 0
3:0	DP_POST_SEL03	R/W	0xA	DP Port1 Training Table Pre-emphasis Level 3

8.6.2.10.49 DP1_VS_PE_10 Register (Address = 0x74) [Default = 0x50]

DP1_VS_PE_10 is shown in DP1_VS_PE_10 Register Field Descriptions.

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Table 8-445. DP1_VS_PE_10 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL10	R/W	0x5	DP Port1 Training Table Voltage Swing Level 1
3:0	DP_POST_SEL10	R/W	0x0	DP Port1 Training Table Pre-emphasis Level 0

8.6.2.10.50 DP1_VS_PE_11 Register (Address = 0x75) [Default = 0xA4]

DP1_VS_PE_11 is shown in DP1_VS_PE_11 Register Field Descriptions.

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Table 8-446. DP1_VS_PE_11 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL11	R/W	0xA	DP Port1 Training Table Voltage Swing Level 1
3:0	DP_POST_SEL11	R/W	0x4	DP Port1 Training Table Pre-emphasis Level 1

8.6.2.10.51 DP1_VS_PE_12 Register (Address = 0x76) [Default = 0xD7]

DP1_VS_PE_12 is shown in DP1_VS_PE_12 Register Field Descriptions.

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Table 8-447. DP1_VS_PE_12 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL12	R/W	0xD	DP Port1 Training Table Voltage Swing Level 1
3:0	DP_POST_SEL12	R/W	0x7	DP Port1 Training Table Pre-emphasis Level 2

8.6.2.10.52 DP1_VS_PE_20 Register (Address = 0x77) [Default = 0x90]

DP1_VS_PE_20 is shown in DP1_VS_PE_20 Register Field Descriptions.

Return to the Summary Table.

Table 8-448. DP1_VS_PE_20 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL20	R/W	0x9	DP Port1 Training Table Voltage Swing Level 2
3:0	DP_POST_SEL20	R/W	0x0	DP Port1 Training Table Pre-emphasis Level 0

8.6.2.10.53 DP1_VS_PE_21 Register (Address = 0x78) [Default = 0xD4]

DP1_VS_PE_21 is shown in DP1_VS_PE_21 Register Field Descriptions.

Return to the Summary Table.

Table 8-449. DP1_VS_PE_21 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL21	R/W	0xD	DP Port1 Training Table Voltage Swing Level 2
3:0	DP_POST_SEL21	R/W	0x4	DP Port1 Training Table Pre-emphasis Level 1

8.6.2.10.54 DP1_VS_PE_30 Register (Address = 0x79) [Default = 0xD0]

DP1_VS_PE_30 is shown in DP1_VS_PE_30 Register Field Descriptions.

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Table 8-450. DP1_VS_PE_30 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	DP_VOD_SEL30	R/W	0xD	DP Port1 Training Table Voltage Swing Level 3
3:0	DP_POST_SEL30	R/W	0x0	DP Port1 Training Table Pre-emphasis Level 0

8.6.2.10.55 DP1_AUX_POL Register (Address = 0x7D) [Default = 0xD5]

DP1_AUX_POL is shown in DP1_AUX_POL Register Field Descriptions.

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Table 8-451. DP1_AUX_POL Register Field Descriptions

Bit	Field	Type	Default	Description
7	AUX_DATA_OUT_POL	R/W	0x1	DP Port1 AUX RX Polarity Inversion
6	AUX_DATA_IN_POL	R/W	0x1	DP Port1 AUX TX Polarity Inversion
5:0	AUX_R1_EN	R/W	0x15	DP Port1 AUX TX Voltage Swing Level Controls the output voltage swing of the AUX channel (VOD). The range of the AUX voltage swing is between 0.2V to 1.15V and is set by increasing the value in this register. Starting at 0.2V, there is an increment of approximately 18mV in the voltage swing as you increase the value in this register. 001011: 0.2V AUX voltage swing (Min) 010111: 0.42V AUX voltage swing (Default) 111111: 1.15V AUX voltage swing (Max) Note: AUX_R1_EN must be equal to AUX_R2_EN in order to maintain output impedance.

8.6.2.10.56 DP1_OVD_SEL Register (Address = 0x7E) [Default = 0x15]

DP1_OVD_SEL is shown in DP1_OVD_SEL Register Field Descriptions.

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Table 8-452. DP1_OVD_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7	DRV_OV_SEL	R/W	0x0	Override select for Port 1 DRV_SEL_PE_OV and DRV_SEL_VS_OV. 0: Control is from state machine 1: Control is from DRV_SEL_PE_OV and DRV_SEL_VS_OV register bits (per lane values)
6	RESERVED	R	0x0	Reserved
5:0	AUX_R2_EN	R/W	0x15	DP Port1 AUX TX Voltage Swing Level Controls the output voltage swing of the AUX channel (VOD). The range of the AUX voltage swing is between 0.2V to 1.15V and is set by increasing the value in this register. Starting at 0.2V, there is an increment of approximately 18mV in the voltage swing as you increase the value in this register. 001011: 0.2V AUX voltage swing (Min) 010111: 0.42V AUX voltage swing (Default) 111111: 1.15V AUX voltage swing (Max) Note: AUX_R1_EN must be equal to AUX_R2_EN in order to maintain output impedance.

8.6.2.10.57 DP_FIXED_RATE_VAL Register (Address = 0x81) [Default = 0x00]

DP_FIXED_RATE_VAL is shown in DP_FIXED_RATE_VAL Register Field Descriptions.

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Table 8-453. DP_FIXED_RATE_VAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	CURR_RATE_OV	R/W	0x0	DP Rate Selection. Active when FIXED_RATE_MODE=1 000: 1.62 Gbps 001: 2.16 Gbps 010: 2.43 Gbps 011: 2.7 Gbps 100: 3.24 Gbps 101: 4.32 Gbps 110: 5.4 Gbps 111: 8.1 Gbps
4	RESERVED	R/W	0x0	Reserved
3:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.58 DP_RATE_BYPASS Register (Address = 0x82) [Default = 0x00]

DP_RATE_BYPASS is shown in DP_RATE_BYPASS Register Field Descriptions.

Return to the Summary Table.

Table 8-454. DP_RATE_BYPASS Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5:2	RESERVED	R/W	0x0	Reserved
1	FIXED_RATE_MODE	R/W	0x0	Bypass automatic rate training and run at fixed rate. 0: enable automatic rate training 1: enable fixed rate mode for DP rate (register 0x81[7:5])
0	RESERVED	R/W	0x0	Reserved

8.6.2.10.59 DP0_LANE_REMAP Register (Address = 0x90) [Default = 0x00]

DP0_LANE_REMAP is shown in DP0_LANE_REMAP Register Field Descriptions.

Return to the Summary Table.

Table 8-455. DP0_LANE_REMAP Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	REMAP_EN	R/W	0x0	Remap Enable Enabling this bit allows the remapping defined in the APB registers. APB register 0x02C defines the physical remapping of lanes between the DP TX and the DP RX. 0: Disable 1: Enable
3:0	ACTIVE_LANES_REMAP	R/W	0x0	Active Lanes After Remap Indicates which lanes are active when Remap is enabled. The corresponding bits should be set if it is an active lane in the DP TX port after remapped configurations. Bit [3]: DP0 Lane 3 Bit [2]: DP0 Lane 2 Bit [1]: DP0 Lane 1 Bit [0]: DP0 Lane 0

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8.6.2.10.60 DP0_OVD_HPD Register (Address = 0x91) [Default = 0x00]

DP0_OVD_HPD is shown in DP0_OVD_HPD Register Field Descriptions.

Return to the Summary Table.

Table 8-456. DP0_OVD_HPD Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	HPD_OV_EN	R/W	0x0	DP Port0 HPD Override Enable
4	HPD_OV	R/W	0x0	DP Port0 HPD Override Value
3	NUM_LANES_OV_EN	R/W	0x0	DP Port0 Lane Count Override Enable
2:0	NUM_LANES_OV	R/W	0x0	DP Port0 Lane Count Override Value 001: 1 Lane 010: 2 Lane 100: 4 Lane

8.6.2.10.61 DP0_EQ_STS Register (Address = 0x93) [Default = 0x00]

DP0_EQ_STS is shown in DP0_EQ_STS Register Field Descriptions.

Return to the Summary Table.

Table 8-457. DP0_EQ_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	EQ_DONE	R	0x0	EQ training status
6	CR_DONE	R	0x0	Clock recovery training status
5	RESERVED	R/W	0x0	Reserved
4:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.62 DP0_BACKLIGHT_CTL_0 Register (Address = 0x9D) [Default = 0x00]

DP0_BACKLIGHT_CTL_0 is shown in DP0_BACKLIGHT_CTL_0 Register Field Descriptions.

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Table 8-458. DP0_BACKLIGHT_CTL_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_CTL[7:0]	R/W	0x0	Bits 7:0 of the BACKLIGHT_CTL value for eDP Port 0. This is used to control the duty cycle of the PWM pulse that controls the brightness of the display backlight.

8.6.2.10.63 DP0_BACKLIGHT_CTL_1 Register (Address = 0x9E) [Default = 0x00]

DP0_BACKLIGHT_CTL_1 is shown in DP0_BACKLIGHT_CTL_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-459. DP0_BACKLIGHT_CTL_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_CTL[15:8]	R/W	0x0	Bits 15:8 of the BACKLIGHT_CTL value for eDP Port 0. This is used to control the duty cycle of the PWM pulse that controls the brightness of the display backlight.

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8.6.2.10.64 DP0_BACKLIGHT_SCALE_0 Register (Address = 0x9F) [Default = 0x00]

DP0_BACKLIGHT_SCALE_0 is shown in DP0_BACKLIGHT_SCALE_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-460. DP0_BACKLIGHT_SCALE_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_SCALE[7:0]	R/W	0x0	Bits 7:0 of the BACKLIGHT_SCALE value for eDP Port 0. This value controls the granularity of the brightness and pulse frequency. This is used in the PWM frequency and duty cycle calculations.

8.6.2.10.65 DP0_BACKLIGHT_SCALE_1 Register (Address = 0xA0) [Default = 0x00]

DP0_BACKLIGHT_SCALE_1 is shown in DP0_BACKLIGHT_SCALE_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-461. DP0_BACKLIGHT_SCALE_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_SCALE[15:8]	R/W	0x0	Bits 15:8 of the BACKLIGHT_SCALE value for eDP Port 0. This value controls the granularity of the brightness and pulse frequency. This is used in the PWM frequency and duty cycle calculations.

8.6.2.10.66 DP0_BACKLIGHT_PRESCALE_DIV Register (Address = 0xA1) [Default = 0x00]

DP0_BACKLIGHT_PRESCALE_DIV is shown in DP0_BACKLIGHT_PRESCALE_DIV Register Field Descriptions.

Return to the Summary Table.

Table 8-462. DP0_BACKLIGHT_PRESCALE_DIV Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_PRESCALE_DIV	R/W	0x0	PRESCALE_DIV value used to pre-scale the PWM frequency for eDP Port 0.

8.6.2.10.67 DP0_PWM_CTL Register (Address = 0xA2) [Default = 0x00]

DP0_PWM_CTL is shown in DP0_PWM_CTL Register Field Descriptions.

Return to the Summary Table.

Table 8-463. DP0_PWM_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	USER_VID_SETUP_DONE	R/W	0x0	Indicates if 984 device will respond to HPD IRQ when PATGEN is enabled: 0: No ACK response from 984 to sink device 1: ACK response from 984 to sink device Note: Set this bit if PATGEN is enabled. Do not set this bit when PATGEN is disabled and the device is in normal functional mode.
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	PWM_INV	R/W	0x0	0: Configure PWM for eDP Port 0 to Active-High. 1: Configure PWM for eDP Port 0 to Active-Low.
0	PWM_EN	R/W	0x0	0: Disable PWM for eDP Port 0. 1: Enable PWM for eDP Port 0.

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8.6.2.10.68 DP0_OVD_LINK_RATE Register (Address = 0xA5) [Default = 0x00]

DP0_OVD_LINK_RATE is shown in DP0_OVD_LINK_RATE Register Field Descriptions.

Return to the Summary Table.

Table 8-464. DP0_OVD_LINK_RATE Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	LINK_RATE_TABLE_INDEX_OV_EN	R/W	0x0	Override enable for link rate table index of the DPRX at Port 0: 0: Disable override for link rate 1: Enable override for link rate
2:0	LINK_RATE_TABLE_INDEX_OV	R/W	0x0	Override value for link rate table index. This value chooses a fixed link rate from the 8-entry table defined in the DPRX DPCD register (SUPPORTED_LINK_RATES) of the eDP Sink device. Enabling the override will write this register value to the DPRX DPCD register (LINK_RATE_SET) of the eDP Sink device. This register is only used in eDP mode. See separate documentation of VESA Embedded DisplayPort (eDP) Standard for more details.

8.6.2.10.69 DP0_CONFG_TEST Register (Address = 0xA6) [Default = 0x61]

DP0_CONFG_TEST is shown in DP0_CONFG_TEST Register Field Descriptions.

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Table 8-465. DP0_CONFG_TEST Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	AT_NAK_MASK	R/W	0x6	Auto-Test NAK Mask For each of the bits in the DPCD TEST_REQUEST register (register 0x00218) of the DP Receiver, the associated bit in this register controls whether the Automated Compliance Test logic will generate a NAK for that request. If set to a 1 a NAK will be generated. If set to a 0, a NAK will not be generated. Bit 0: TEST_LINK_TRAINING Bit 1: TEST_PATTERN Bit 2: TEST_EDID_READ Bit 3: PHY_TEST_PATTERN Typically, both TEST_LINK_TRAINING and PHY_TEST_PATTERN are handled locally, so there is no need to generate a NAK for those. For TEST_PATTERN and TEST_EDID_READ, normally a NAK will be generated, but it might be desirable to have an external or upstream processor handle those events, in which case, the control bits for those should be set to 0.
3	RESERVED	R	0x0	Reserved
2	AT_DIS_LQ_LANE_SET	R/W	0x0	During PHY_TEST_PATTERN automated compliance testing, normally the Automated Compliance Test logic will set the LINK_QUAL_LANEx_SET registers in the DP Receiver DPCD registers 0x0010B - 0x0010E based on the requested pattern. If this bit is set to 1, the Automated Compliance Test logic will not program those registers.
1	AT_IGNORE_VS_PE	R/W	0x0	During PHY_TEST_PATTERN automated compliance testing, normally the Automated Compliance Test logic will read the DPCD registers 0x00206-7 to determine requested Voltage Swing and Pre-emphasis levels. It will use those levels and also copy those values to the DP RX registers 0x00103-0x00106. If this bit is set to 1, the Automated Compliance Test logic will ignore VS/PE adjustment requests.
0	AUTO_TEST_EN	R/W	0x1	Enable Automated Compliance Test handling by the internal DP TX controller

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8.6.2.10.70 DP0_OVD_EN_HTOTAL Register (Address = 0xA7) [Default = 0x00]

DP0_OVD_EN_HTOTAL is shown in DP0_OVD_EN_HTOTAL Register Field Descriptions.

Return to the Summary Table.

Table 8-466. DP0_OVD_EN_HTOTAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RESERVED	R	0x0	Reserved
0	DPTX_HTOTAL_OV_EN	R/W	0x0	Override Enable for DTG HTOTAL Enable override on the value that was written by the DTG to the DP TX APB register (0x180). Use this register instead of directly overwriting the APB register.

8.6.2.10.71 DP0_OVD_VAL_HTOTAL_LSB Register (Address = 0xA8) [Default = 0x00]

DP0_OVD_VAL_HTOTAL_LSB is shown in DP0_OVD_VAL_HTOTAL_LSB Register Field Descriptions.

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Table 8-467. DP0_OVD_VAL_HTOTAL_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DPTX_HTOTAL_OV_LSB	R/W	0x0	Bits[7:0] of the DTG HTOTAL override value

8.6.2.10.72 DP0_OVD_VAL_HTOTAL_MSB Register (Address = 0xA9) [Default = 0x00]

DP0_OVD_VAL_HTOTAL_MSB is shown in DP0_OVD_VAL_HTOTAL_MSB Register Field Descriptions.

Return to the Summary Table.

Table 8-468. DP0_OVD_VAL_HTOTAL_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DPTX_HTOTAL_OV_MSB	R/W	0x0	Bits[15:8] of the DTG HTOTAL override value

8.6.2.10.73 DP1_LANE_REMAP Register (Address = 0xB0) [Default = 0x00]

DP1_LANE_REMAP is shown in DP1_LANE_REMAP Register Field Descriptions.

Return to the Summary Table.

Table 8-469. DP1_LANE_REMAP Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	REMAP_EN	R/W	0x0	Remap Enable Enabling this bit allows the remapping defined in the APB registers. APB register 0x02C defines the physical remapping of lanes between the DP TX and the DP RX. 0: Disable 1: Enable
3:0	ACTIVE_LANES_REMAP	R/W	0x0	Active Lanes After Remap Indicates which lanes are active when Remap is enabled. The corresponding bits should be set if it is an active lane in the DP TX port after remapped configurations. Bit [3]: DP1 Lane 3 Bit [2]: DP1 Lane 2 Bit [1]: DP1 Lane 1 Bit [0]: DP1 Lane 0

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8.6.2.10.74 DP1_OVD_HPD Register (Address = 0xB1) [Default = 0x00]

DP1_OVD_HPD is shown in DP1_OVD_HPD Register Field Descriptions.

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Table 8-470. DP1_OVD_HPD Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	HPD_OV_EN	R/W	0x0	DP Port1 HPD Override Enable
4	HPD_OV	R/W	0x0	DP Port1 HPD Override Value
3	NUM_LANES_OV_EN	R/W	0x0	DP Port1 Lane Count Override Enable
2:0	NUM_LANES_OV	R/W	0x0	DP Port1 Lane Count Override Value 001: 1 Lane 010: 2 Lane 100: 4 Lane

8.6.2.10.75 DP1_EQ_STS Register (Address = 0xB3) [Default = 0x00]

DP1_EQ_STS is shown in DP1_EQ_STS Register Field Descriptions.

Return to the Summary Table.

Table 8-471. DP1_EQ_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	EQ_DONE	R	0x0	EQ training status
6	CR_DONE	R	0x0	Clock recovery training status
5	RESERVED	R/W	0x0	Reserved
4:0	RESERVED	R/W	0x0	Reserved

8.6.2.10.76 DP1_BACKLIGHT_CTL_0 Register (Address = 0xBD) [Default = 0x00]

DP1_BACKLIGHT_CTL_0 is shown in DP1_BACKLIGHT_CTL_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-472. DP1_BACKLIGHT_CTL_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_CTL[7:0]	R/W	0x0	Bits 7:0 of the BACKLIGHT_CTL value for eDP Port 1. This is used to control the duty cycle of the PWM pulse that controls the brightness of the display backlight.

8.6.2.10.77 DP1_BACKLIGHT_CTL_1 Register (Address = 0xBE) [Default = 0x00]

DP1_BACKLIGHT_CTL_1 is shown in DP1_BACKLIGHT_CTL_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-473. DP1_BACKLIGHT_CTL_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_CTL[15:8]	R/W	0x0	Bits 15:8 of the BACKLIGHT_CTL value for eDP Port 1. This is used to control the duty cycle of the PWM pulse that controls the brightness of the display backlight.

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8.6.2.10.78 DP1_BACKLIGHT_SCALE_0 Register (Address = 0xBF) [Default = 0x00]

DP1_BACKLIGHT_SCALE_0 is shown in DP1_BACKLIGHT_SCALE_0 Register Field Descriptions.

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Table 8-474. DP1_BACKLIGHT_SCALE_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_SCALE[7:0]	R/W	0x0	Bits 7:0 of the BACKLIGHT_SCALE value for eDP Port 1. This value controls the granularity of the brightness and pulse frequency. This is used in the PWM frequency and duty cycle calculations.

8.6.2.10.79 DP1_BACKLIGHT_SCALE_1 Register (Address = 0xC0) [Default = 0x00]

DP1_BACKLIGHT_SCALE_1 is shown in DP1_BACKLIGHT_SCALE_1 Register Field Descriptions.

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Table 8-475. DP1_BACKLIGHT_SCALE_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_SCALE[15:8]	R/W	0x0	Bits 15:8 of the BACKLIGHT_SCALE value for eDP Port 1. This value controls the granularity of the brightness and pulse frequency. This is used in the PWM frequency and duty cycle calculations.

8.6.2.10.80 DP1_BACKLIGHT_PRESCALE_DIV Register (Address = 0xC1) [Default = 0x00]

DP1_BACKLIGHT_PRESCALE_DIV is shown in DP1_BACKLIGHT_PRESCALE_DIV Register Field Descriptions.

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Table 8-476. DP1_BACKLIGHT_PRESCALE_DIV Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BACKLIGHT_PRESCALE_DIV	R/W	0x0	PRESCALE_DIV value used to pre-scale the PWM frequency for eDP Port 1.

8.6.2.10.81 DP1_PWM_CTL Register (Address = 0xC2) [Default = 0x00]

DP1_PWM_CTL is shown in DP1_PWM_CTL Register Field Descriptions.

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Table 8-477. DP1_PWM_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	USER_VID_SETUP_DONE	R/W	0x0	Indicates if 984 device will respond to HPD IRQ when PATGEN is enabled: 0: No ACK response from 984 to sink device 1: ACK response from 984 to sink device Note: Set this bit if PATGEN is enabled. Do not set this bit when PATGEN is disabled and the device is in normal functional mode.
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	PWM_INV	R/W	0x0	0: Configure PWM for eDP Port 1 to Active-High. 1: Configure PWM for eDP Port 1 to Active-Low.
0	PWM_EN	R/W	0x0	0: Disable PWM for eDP Port 1. 1: Enable PWM for eDP Port 1.

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8.6.2.10.82 DP1_OVD_LINK_RATE Register (Address = 0xC5) [Default = 0x00]

DP1_OVD_LINK_RATE is shown in DP1_OVD_LINK_RATE Register Field Descriptions.

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Table 8-478. DP1_OVD_LINK_RATE Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	LINK_RATE_TABLE_INDEX_OV_EN	R/W	0x0	Override enable for link rate table index of the DPRX at Port 1: 0: Disable override for link rate 1: Enable override for link rate
2:0	LINK_RATE_TABLE_INDEX_OV	R/W	0x0	Override value for link rate table index. This value chooses a fixed link rate from the 8-entry table defined in the DPRX DPCD register (SUPPORTED_LINK_RATES) of the eDP Sink device. Enabling the override will write this register value to the DPRX DPCD register (LINK_RATE_SET) of the eDP Sink device. This register is only used in eDP mode. See separate documentation of VESA Embedded DisplayPort (eDP) Standard for more details.

8.6.2.10.83 DP1_CONFG_TEST Register (Address = 0xC6) [Default = 0x61]

DP1_CONFG_TEST is shown in DP1_CONFG_TEST Register Field Descriptions.

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Table 8-479. DP1_CONFG_TEST Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	AT_NAK_MASK	R/W	0x6	Auto-Test NAK Mask For each of the bits in the DPCD TEST_REQUEST register (register 0x00218) of the DP Receiver, the associated bit in this register controls whether the Automated Compliance Test logic will generate a NAK for that request. If set to a 1 a NAK will be generated. If set to a 0, a NAK will not be generated. Bit 0: TEST_LINK_TRAINING Bit 1: TEST_PATTERN Bit 2: TEST_EDID_READ Bit 3: PHY_TEST_PATTERN Typically, both TEST_LINK_TRAINING and PHY_TEST_PATTERN are handled locally, so there is no need to generate a NAK for those. For TEST_PATTERN and TEST_EDID_READ, normally a NAK will be generated, but it might be desirable to have an external or upstream processor handle those events, in which case, the control bits for those should be set to 0.
3	RESERVED	R	0x0	Reserved
2	AT_DIS_LQ_LANE_SET	R/W	0x0	During PHY_TEST_PATTERN automated compliance testing, normally the Automated Compliance Test logic will set the LINK_QUAL_LANEx_SET registers in the DP Receiver DPCD registers 0x0010B - 0x0010E based on the requested pattern. If this bit is set to 1, the Automated Compliance Test logic will not program those registers.
1	AT_IGNORE_VS_PE	R/W	0x0	During PHY_TEST_PATTERN automated compliance testing, normally the Automated Compliance Test logic will DPCD registers 0x00206-7 to determine requested Voltage Swing and Pre-emphasis levels. It will use those levels and also copy those values to the DP RX registers 0x00103-0x00106. If this bit is set to 1, the Automated Compliance Test logic will ignore VS/PE adjustment requests.
0	AUTO_TEST_EN	R/W	0x1	Enable Automated Compliance Test handling by the internal DP TX controller

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8.6.2.10.84 DP1_OVD_EN_HTOTAL Register (Address = 0xC7) [Default = 0x00]

DP1_OVD_EN_HTOTAL is shown in DP1_OVD_EN_HTOTAL Register Field Descriptions.

Return to the Summary Table.

Table 8-480. DP1_OVD_EN_HTOTAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RESERVED	R	0x0	Reserved
0	DPTX_HTOTAL_OV_EN	R/W	0x0	Override Enable for DTG HTOTAL Enable override on the value that was written by the DTG to the DP TX APB register (0x180). Use this register instead of directly overwriting the APB register.

8.6.2.10.85 DP1_OVD_VAL_HTOTAL_LSB Register (Address = 0xC8) [Default = 0x00]

DP1_OVD_VAL_HTOTAL_LSB is shown in DP1_OVD_VAL_HTOTAL_LSB Register Field Descriptions.

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Table 8-481. DP1_OVD_VAL_HTOTAL_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DPTX_HTOTAL_OV_LSB	R/W	0x0	Bits[7:0] of the DTG HTOTAL override value

8.6.2.10.86 DP1_OVD_VAL_HTOTAL_MSB Register (Address = 0xC9) [Default = 0x00]

DP1_OVD_VAL_HTOTAL_MSB is shown in DP1_OVD_VAL_HTOTAL_MSB Register Field Descriptions.

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Table 8-482. DP1_OVD_VAL_HTOTAL_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DPTX_HTOTAL_OV_MSB	R/W	0x0	Bits[15:8] of the DTG HTOTAL override value

8.6.2.10.87 DP0_TX_ICR Register (Address = 0xD0) [Default = 0x00]

DP0_TX_ICR is shown in DP0_TX_ICR Register Field Descriptions.

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Table 8-483. DP0_TX_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DP_TX_ICR	R/W	0x0	Interrupt Control Register for DP TX Port 0 The bits in this register control the interrupt generation based on the DP Transmit status bits. When enabled, the selected interrupt (or interrupts) will be propagated to the main page INTERRUPT_STS and/or RX_INTN_STS registers. For each of these interrupt enables, see the associated ICR/ISR registers. [4] Automated Test (registers 0xD5, 0xDD) [3] HPD_IRQ1 (registers 0xD4, 0xDC) [2] HPD_IRQ0 (registers 0xD3, 0xDB) [1] DP TX Port State Machine (registers 0xD2, 0xDA) [0] DP Transmit Core (registers 0xD1, 0xD9)

8.6.2.10.88 DP0_TX_CORE_ICR Register (Address = 0xD1) [Default = 0x00]

DP0_TX_CORE_ICR is shown in DP0_TX_CORE_ICR Register Field Descriptions.

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Table 8-484. DP0_TX_CORE_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DP_TX_CORE_ICR	R/W	0x0	Interrupt Control Register for DP Transmit Core interrupts The bits in this register control the interrupt generation based on the DP Transmit Core. These interrupts are copied from the DP Transmit Core INTERRUPT_STATUS register (0x140) when the DP Transmit Core generates an interrupt. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [5] HDCP_TIMER_IRQ [4] GP_TIMER_IRQ [3] REPLY_TIMEOUT [2] REPLY_RECEIVED [1] HPD_IRQ [0] HPD_EVENT

8.6.2.10.89 DP0_PORT_SM_ICR Register (Address = 0xD2) [Default = 0x00]

DP0_PORT_SM_ICR is shown in DP0_PORT_SM_ICR Register Field Descriptions.

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Table 8-485. DP0_PORT_SM_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_PORT_SM_ICR	R/W	0x0	Interrupt Control Register for DP Port State Machine interrupts The bits in this register control the interrupt generation based on the DP Transmit Port State Machine. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [7] Video Setup Done [6] AUX Fail [5] Link Capabilities Change [4] Link Rate Change [3] Lane Count Change [2] Link Training Done [1] Link Lost [0] PLL Lock Done

8.6.2.10.90 DP0_HPD_IRQ_ICR0 Register (Address = 0xD3) [Default = 0x00]

DP0_HPD_IRQ_ICR0 is shown in DP0_HPD_IRQ_ICR0 Register Field Descriptions.

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Table 8-486. DP0_HPD_IRQ_ICR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

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Table 8-486. DP0_HPD_IRQ_ICR0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	IRQ_ESI0_ICR	R/W	0x0	Interrupt Control Register for interrupts from the DP Receiver DEVICE_SERVICE_IRQ_VECTOR(ESI0). After a read of the DP Receiver DPCD register 0x00201, an interrupt may be generated for each of the bits in that register. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [6] SINK_SPECIFIC_IRQ [5] UP_REQ_MSG_RDY [4] DOWN_REP_MSG_RDY [3] MCCS_IRQ [2] CP_IRQ [1] AUTOMATED_TEST_REQUEST [0] RESERVED (for FUTURE) Note: if the DP Transmitter is enabled to handle automated test requests, the AUTOMATED_TEST_REQUEST interrupt enable will typically not be used. Instead, the interrupts in the DP_AUTO_TEST_ICR/ISR would be used instead.

8.6.2.10.91 DP0_HPD_IRQ_ICR1 Register (Address = 0xD4) [Default = 0x00]

DP0_HPD_IRQ_ICR1 is shown in DP0_HPD_IRQ_ICR1 Register Field Descriptions.

Return to the Summary Table.

Table 8-487. DP0_HPD_IRQ_ICR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	IRQ_ESI1_ICR	R/W	0x0	Interrupt Control Register for interrupts from the DP Receiver DEVICE_SERVICE_IRQ_VECTOR_ESI1. After a read of the DP Receiver DPCD register 0x02004, an interrupt may be generated for each of the bits in that register. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [2] CEC_IRQ [1] LOCK_ACQUISITION_REQUEST [0] RX_GTC_MSTR_REQ_STATUS_CHANGE
3:0	IRQ_LINK_ESI0_ICR	R/W	0x0	Interrupt Control Register for interrupts from the DP Receiver LINK_SERVICE_IRQ_VECTOR_ESI0. After a read of the DP Receiver DPCD register 0x02005, an interrupt may be generated for each of the bits in that register. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [3] HDMI_LINK_STATUS_CHANGED [2] STREAM_STATUS_CHANGED [1] LINK_STATUS_CHANGED [0] RX_CAP_CHANGED

8.6.2.10.92 DP0_AUTO_TEST_ICR Register (Address = 0xD5) [Default = 0x00]

DP0_AUTO_TEST_ICR is shown in DP0_AUTO_TEST_ICR Register Field Descriptions.

Return to the Summary Table.

Table 8-488. DP0_AUTO_TEST_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

Table 8-488. DP0_AUTO_TEST_ICR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	AUTO_TEST_ICR	R/W	0x0	Interrupt Control Register for interrupts from the DP Receiver Automated Test Request. If Automated Test mode is enabled, these registers allow interrupt generation for the test requested in the DPCD Receiver register 0x00218. Note, the DP Transmitter typically will automatically handle the TEST_LINK_TRAINING and PHY_TEST_PATTERN requests, so those should typically not be enabled via this register. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. This allows for remote control of the unsupported automated tests. [3] PHY_TEST_PATTERN [2] TEST_EDID_READ [1] TEST_PATTERN [0] TEST_LINK_TRAINING

8.6.2.10.93 DP0_TX_ISR Register (Address = 0xD8) [Default = 0x00]

DP0_TX_ISR is shown in DP0_TX_ISR Register Field Descriptions.

Return to the Summary Table.

Table 8-489. DP0_TX_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DP_TX_ISR	R	0x0	Interrupt Status Register for DP TX Port 0 The bits in this register indicate when a lower level interrupt status register has generated an interrupt condition. For each of these status bits, an interrupt will be passed to the INTERRUPT_STS or RX_INTN_STS register if the associated enable bit in the DP_TX_ICR register is set to 1. For each of these, see the associated ICR/ISR registers. [4] Automated Test (registers 0xD5, 0xE5) [3] HPD_IRQ1 (registers 0xD4, 0xE4) [2] HPD_IRQ0 (registers 0xD3, 0xE3) [1] DP TX Port State Machine (registers 0xD2, 0xDA) [0] DP Transmit Core (registers 0xD1, 0xD9) These interrupt status bits will be cleared upon reading the lower level Interrupt Status register.

8.6.2.10.94 DP0_TX_CORE_ISR Register (Address = 0xD9) [Default = 0x00]

DP0_TX_CORE_ISR is shown in DP0_TX_CORE_ISR Register Field Descriptions.

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Table 8-490. DP0_TX_CORE_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

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Table 8-490. DP0_TX_CORE_ISR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:0	DP_TX_CORE_ISR	RC	0x0	Interrupt Status Register for DP Transmit Core interrupts The bits in this register indicate latched status based on interrupts from the DP Transmit Core. These interrupts are copied from the DP Transmit Core INTERRUPT_STATUS register (0x140) when the DP Transmit Core generates an interrupt. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [5] HDCP_TIMER_IRQ [4] GP_TIMER_IRQ [3] REPLY_TIMEOUT [2] REPLY_RECEIVED [1] HPD_IRQ [0] HPD_EVENT These status registers will be cleared on read.

8.6.2.10.95 DP0_PORT_SM_ISR Register (Address = 0xDA) [Default = 0x00]

DP0_PORT_SM_ISR is shown in DP0_PORT_SM_ISR Register Field Descriptions.

Return to the Summary Table.

Table 8-491. DP0_PORT_SM_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_PORT_SM_ISR	RC	0x0	Interrupt Status Register for DP Port State Machine interrupts The bits in this register indicate latched status from the DP Transmit Port State Machine. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [7] Video Setup Done [6] AUX Fail [5] Link Capabilities Change [4] Link Rate Change [3] Lane Count Change [2] Link Training Done [1] Link Lost [0] PLL Lock Done These status registers will be cleared on read.

8.6.2.10.96 DP0_HPD_IRQ_ISR0 Register (Address = 0xDB) [Default = 0x00]

DP0_HPD_IRQ_ISR0 is shown in DP0_HPD_IRQ_ISR0 Register Field Descriptions.

Return to the Summary Table.

Table 8-492. DP0_HPD_IRQ_ISR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	IRQ_ESI0_ISR	RC	0x0	Interrupt Status Register for interrupts from the DP Receiver DEVICE_SERVICE_IRQ_VECTOR(ESI0). Upon detection of an IRQ_HPD interrupt from the DP Receiver, the DP Transmitter will read the DP Receiver's IRQ vector registers. This register latches the values read from the DP Receiver DPCD register 0x00201. If enabled via the IRQ_ESI0_ICR interrupt enables, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [6] SINK_SPECIFIC_IRQ [5] UP_REQ_MSG_RDY [4] DOWN_REP_MSG_RDY [3] MCCS_IRQ [2] CP_IRQ [1] AUTOMATED_TEST_REQUEST [0] RESERVED (for FUTURE) These status registers will be cleared on read.

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8.6.2.10.97 DP0_HPD_IRQ_ISR1 Register (Address = 0xDC) [Default = 0x00]

DP0_HPD_IRQ_ISR1 is shown in DP0_HPD_IRQ_ISR1 Register Field Descriptions.

Return to the Summary Table.

Table 8-493. DP0_HPD_IRQ_ISR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	IRQ_ESI1_ISR	RC	0x0	Interrupt Status Register for interrupts from the DP Receiver DEVICE_SERVICE_IRQ_VECTOR_ESI1. Upon detection of an IRQ_HPD interrupt from the DP Receiver, the DP Transmitter will read the DP Receiver's IRQ vector registers. This register latches the values read from the DP Receiver DPCD register 0x02004. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [2] CEC_IRQ [1] LOCK_ACQUISITION_REQUEST [0] RX_GTC_MSTR_REQ_STATUS_CHANGE These status registers will be cleared on read.
3:0	IRQ_LINK_ESI0_ISR	RC	0x0	Interrupt Status Register for interrupts from the DP Receiver LINK_SERVICE_IRQ_VECTOR_ESI0. Upon detection of an IRQ_HPD interrupt from the DP Receiver, the DP Transmitter will read the DP Receiver's IRQ vector registers. This register latches the values read from the DP Receiver DPCD register 0x02005. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [3] HDMI_LINK_STATUS_CHANGED [2] STREAM_STATUS_CHANGED [1] LINK_STATUS_CHANGED [0] RX_CAP_CHANGED These status registers will be cleared on read.

8.6.2.10.98 DP0_AUTO_TEST_ISR Register (Address = 0xDD) [Default = 0x00]

DP0_AUTO_TEST_ISR is shown in DP0_AUTO_TEST_ISR Register Field Descriptions.

Return to the Summary Table.

Table 8-494. DP0_AUTO_TEST_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	AUTO_TEST_ISR	RC	0x0	Interrupt Status Register for interrupts from the DP Receiver Automated Test Request. If Automated Test mode is enabled, these registers allow interrupt generation for the test requested in the DPCD Receiver register 0x00218. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. This allows for remote control of the unsupported automated tests. Note, the DP Transmitter typically will automatically handle the TEST_LINK_TRAINING and PHY_TEST_PATTERN requests. [3] PHY_TEST_PATTERN [2] TEST_EDID_READ [1] TEST_PATTERN [0] TEST_LINK_TRAINING These status registers will be cleared on read.

8.6.2.10.99 DP1_TX_ICR Register (Address = 0xE0) [Default = 0x00]

DP1_TX_ICR is shown in DP1_TX_ICR Register Field Descriptions.

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Table 8-495. DP1_TX_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DP_TX_ICR	R/W	0x0	Interrupt Control Register for DP TX Port 1 The bits in this register control the interrupt generation based on the DP Transmit status bits. When enabled, the selected interrupt (or interrupts) will be propagated to the main page INTERRUPT_STS and/or RX_INTN_STS registers. For each of these interrupt enables, see the associated ICR/ISR registers. [4] Automated Test (registers 0xE5, 0xED) [3] HPD_IRQ1 (registers 0xE4, 0xEC) [2] HPD_IRQ0 (registers 0xE3, 0xEB) [1] DP TX Port State Machine (registers 0xE2, 0xEA) [0] DP Transmit Core (registers 0xE1, 0xE9)

8.6.2.10.100 DP1_TX_CORE_ICR Register (Address = 0xE1) [Default = 0x00]

DP1_TX_CORE_ICR is shown in DP1_TX_CORE_ICR Register Field Descriptions.

Return to the Summary Table.

Table 8-496. DP1_TX_CORE_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DP_TX_CORE_ICR	R/W	0x0	Interrupt Control Register for DP Transmit Core interrupts The bits in this register control the interrupt generation based on the DP Transmit Core. These interrupts are copied from the DP Transmit Core INTERRUPT_STATUS register (0x140) when the DP Transmit Core generates an interrupt. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [5] HDCP_TIMER_IRQ [4] GP_TIMER_IRQ [3] REPLY_TIMEOUT [2] REPLY_RECEIVED [1] HPD_IRQ [0] HPD_EVENT

8.6.2.10.101 DP1_PORT_SM_ICR Register (Address = 0xE2) [Default = 0x00]

DP1_PORT_SM_ICR is shown in DP1_PORT_SM_ICR Register Field Descriptions.

Return to the Summary Table.

Table 8-497. DP1_PORT_SM_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_PORT_SM_ICR	R/W	0x0	Interrupt Control Register for DP Port State Machine interrupts The bits in this register control the interrupt generation based on the DP Transmit Port State Machine. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [7] Video Setup Done [6] AUX Fail [5] Link Capabilities Change [4] Link Rate Change [3] Lane Count Change [2] Link Training Done [1] Link Lost [0] PLL Lock Done

8.6.2.10.102 DP1_HPD_IRQ_ICR0 Register (Address = 0xE3) [Default = 0x00]

DP1_HPD_IRQ_ICR0 is shown in DP1_HPD_IRQ_ICR0 Register Field Descriptions.

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Table 8-498. DP1_HPD_IRQ_ICR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	IRQ_ESI0_ICR	R/W	0x0	Interrupt Control Register for interrupts from the DP Receiver DEVICE_SERVICE_IRQ_VECTOR(ESI0). After a read of the DP Receiver DPCD register 0x00201, an interrupt may be generated for each of the bits in that register. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [6] SINK_SPECIFIC_IRQ [5] UP_REQ_MSG_RDY [4] DOWN_REP_MSG_RDY [3] MCCS_IRQ [2] CP_IRQ [1] AUTOMATED_TEST_REQUEST [0] RESERVED (for FUTURE) Note: if the DP Transmitter is enabled to handle automated test requests, the AUTOMATED_TEST_REQUEST interrupt enable will typically not be used. Instead, the interrupts in the DP_AUTO_TEST_ICR/ISR would be used instead.

8.6.2.10.103 DP1_HPD_IRQ_ICR1 Register (Address = 0xE4) [Default = 0x00]

DP1_HPD_IRQ_ICR1 is shown in DP1_HPD_IRQ_ICR1 Register Field Descriptions.

Return to the Summary Table.

Table 8-499. DP1_HPD_IRQ_ICR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	IRQ_ESI1_ICR	R/W	0x0	Interrupt Control Register for interrupts from the DP Receiver DEVICE_SERVICE_IRQ_VECTOR_ESI1. After a read of the DP Receiver DPCD register 0x02004, an interrupt may be generated for each of the bits in that register. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [2] CEC_IRQ [1] LOCK_ACQUISITION_REQUEST [0] RX_GTC_MSTR_REQ_STATUS_CHANGE
3:0	IRQ_LINK_ESI0_ICR	R/W	0x0	Interrupt Control Register for interrupts from the DP Receiver LINK_SERVICE_IRQ_VECTOR_ESI0. After a read of the DP Receiver DPCD register 0x02005, an interrupt may be generated for each of the bits in that register. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [3] HDMI_LINK_STATUS_CHANGED [2] STREAM_STATUS_CHANGED [1] LINK_STATUS_CHANGED [0] RX_CAP_CHANGED

8.6.2.10.104 DP1_AUTO_TEST_ICR Register (Address = 0xE5) [Default = 0x00]

DP1_AUTO_TEST_ICR is shown in DP1_AUTO_TEST_ICR Register Field Descriptions.

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Table 8-500. DP1_AUTO_TEST_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

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Table 8-500. DP1_AUTO_TEST_ICR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	AUTO_TEST_ICR	R/W	0x0	Interrupt Control Register for interrupts from the DP Receiver Automated Test Request. If Automated Test mode is enabled, these registers allow interrupt generation for the test requested in the DPCD Receiver register 0x00218. Note, the DP Transmitter typically will automatically handle the TEST_LINK_TRAINING and PHY_TEST_PATTERN requests, so those should typically not be enabled via this register. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. This allows for remote control of the unsupported automated tests. [3] PHY_TEST_PATTERN [2] TEST_EDID_READ [1] TEST_PATTERN [0] TEST_LINK_TRAINING

8.6.2.10.105 DP1_TX_ISR Register (Address = 0xE8) [Default = 0x00]

DP1_TX_ISR is shown in DP1_TX_ISR Register Field Descriptions.

Return to the Summary Table.

Table 8-501. DP1_TX_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DP_TX_ISR	R	0x0	Interrupt Status Register for DP TX Port 1 The bits in this register indicate when a lower level interrupt status register has generated an interrupt condition. For each of these status bits, an interrupt will be passed to the INTERRUPT_STS or RX_INTN_STS register if the associated enable bit in the DP_TX_ICR register is set to 1. For each of these, see the associated ICR/ISR registers. [4] Automated Test (registers 0xE5, 0xED) [3] HPD_IRQ1 (registers 0xE4, 0xEC) [2] HPD_IRQ0 (registers 0xE3, 0xEB) [1] DP TX Port State Machine (registers 0xE2, 0xEA) [0] DP Transmit Core (registers 0xE1, 0xE9) These interrupt status bits will be cleared upon reading the lower level Interrupt Status register.

8.6.2.10.106 DP1_TX_CORE_ISR Register (Address = 0xE9) [Default = 0x00]

DP1_TX_CORE_ISR is shown in DP1_TX_CORE_ISR Register Field Descriptions.

Return to the Summary Table.

Table 8-502. DP1_TX_CORE_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

Table 8-502. DP1_TX_CORE_ISR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:0	DP_TX_CORE_ISR	RC	0x0	Interrupt Status Register for DP Transmit Core interrupts The bits in this register indicate latched status based on interrupts from the DP Transmit Core. These interrupts are copied from the DP Transmit Core INTERRUPT_STATUS register (0x140) when the DP Transmit Core generates an interrupt. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [5] HDCP_TIMER_IRQ [4] GP_TIMER_IRQ [3] REPLY_TIMEOUT [2] REPLY_RECEIVED [1] HPD_IRQ [0] HPD_EVENT These status registers will be cleared on read.

8.6.2.10.107 DP1_PORT_SM_ISR Register (Address = 0xEA) [Default = 0x00]

DP1_PORT_SM_ISR is shown in DP1_PORT_SM_ISR Register Field Descriptions.

Return to the Summary Table.

Table 8-503. DP1_PORT_SM_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DP_PORT_SM_ISR	RC	0x0	Interrupt Status Register for DP Port State Machine interrupts The bits in this register indicate latched status from the DP Transmit Port State Machine. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [7] Video Setup Done [6] AUX Fail [5] Link Capabilities Change [4] Link Rate Change [3] Lane Count Change [2] Link Training Done [1] Link Lost [0] PLL Lock Done These status registers will be cleared on read.

8.6.2.10.108 DP1_HPD_IRQ_ISR0 Register (Address = 0xEB) [Default = 0x00]

DP1_HPD_IRQ_ISR0 is shown in DP1_HPD_IRQ_ISR0 Register Field Descriptions.

Return to the Summary Table.

Table 8-504. DP1_HPD_IRQ_ISR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	IRQ_ESI0_ISR	RC	0x0	Interrupt Status Register for interrupts from the DP Receiver DEVICE_SERVICE_IRQ_VECTOR(ESI0). Upon detection of an IRQ_HPD interrupt from the DP Receiver, the DP Transmitter will read the DP Receiver's IRQ vector registers. This register latches the values read from the DP Receiver DPCD register 0x00201. If enabled via the IRQ_ESI0_ICR interrupt enables, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [6] SINK_SPECIFIC_IRQ [5] UP_REQ_MSG_RDY [4] DOWN_REP_MSG_RDY [3] MCCS_IRQ [2] CP_IRQ [1] AUTOMATED_TEST_REQUEST [0] RESERVED (for FUTURE) These status registers will be cleared on read.

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8.6.2.10.109 DP1_HPD_IRQ_ISR1 Register (Address = 0xEC) [Default = 0x00]

DP1_HPD_IRQ_ISR1 is shown in DP1_HPD_IRQ_ISR1 Register Field Descriptions.

Return to the Summary Table.

Table 8-505. DP1_HPD_IRQ_ISR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	IRQ_ESI1_ISR	RC	0x0	Interrupt Status Register for interrupts from the DP Receiver DEVICE_SERVICE_IRQ_VECTOR_ESI1. Upon detection of an IRQ_HPD interrupt from the DP Receiver, the DP Transmitter will read the DP Receiver's IRQ vector registers. This register latches the values read from the DP Receiver DPCD register 0x02004. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [2] CEC_IRQ [1] LOCK_ACQUISITION_REQUEST [0] RX_GTC_MSTR_REQ_STATUS_CHANGE These status registers will be cleared on read.
3:0	IRQ_LINK_ESI0_ISR	RC	0x0	Interrupt Status Register for interrupts from the DP Receiver LINK_SERVICE_IRQ_VECTOR_ESI0. Upon detection of an IRQ_HPD interrupt from the DP Receiver, the DP Transmitter will read the DP Receiver's IRQ vector registers. This register latches the values read from the DP Receiver DPCD register 0x02005. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. [3] HDMI_LINK_STATUS_CHANGED [2] STREAM_STATUS_CHANGED [1] LINK_STATUS_CHANGED [0] RX_CAP_CHANGED These status registers will be cleared on read.

8.6.2.10.110 DP1_AUTO_TEST_ISR Register (Address = 0xED) [Default = 0x00]

DP1_AUTO_TEST_ISR is shown in DP1_AUTO_TEST_ISR Register Field Descriptions.

Return to the Summary Table.

Table 8-506. DP1_AUTO_TEST_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	AUTO_TEST_ISR	RC	0x0	Interrupt Status Register for interrupts from the DP Receiver Automated Test Request. If Automated Test mode is enabled, these registers allow interrupt generation for the test requested in the DPCD Receiver register 0x00218. When enabled, the selected interrupt (or interrupts) will be propagated to the DP_TX_ISR. This allows for remote control of the unsupported automated tests. Note, the DP Transmitter typically will automatically handle the TEST_LINK_TRAINING and PHY_TEST_PATTERN requests. [3] PHY_TEST_PATTERN [2] TEST_EDID_READ [1] TEST_PATTERN [0] TEST_LINK_TRAINING These status registers will be cleared on read.

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8.6.2.11 Page 12: eDP/DP PLL Registers

PAGE_12 Registers lists the memory-mapped registers for the Page 12: eDP/DP PLL registers. All register offset addresses not listed in PAGE_12 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-507. PAGE_12 Registers

Address	Acronym	Register Name	Section
0x0	PLL_LOCK_EDP	PLL_LOCK_EDP	Go
0x4	MASH_ORDER_EDP	MASH_ORDER_EDP	Go
0x5	NDIV_7:0_EDP	NDIV_7:0_EDP	Go
0x6	NDIV_15:8_EDP	NDIV_15:8_EDP	Go
0xE	VCO_EDP	VCO_EDP	Go
0xF	OVD_RAMPX_EDP	OVD_RAMPX_EDP	Go
0x14	SSCG_CTL1_EDP	SSCG_CTL1_EDP	Go
0x15	SSCG_CTL2_EDP	SSCG_CTL2_EDP	Go
0x16	SSCG_CTL3_EDP	SSCG_CTL3_EDP	Go
0x17	SSCG_CTL4_EDP	SSCG_CTL4_EDP	Go
0x18	DEN_7:0_EDP	DEN_7:0_EDP	Go
0x19	DEN_15:8_EDP	DEN_15:8_EDP	Go
0x1A	DEN_23:16_EDP	DEN_23:16_EDP	Go
0x1B	PLL_OVD_EN_CH0	PLL_OVD_EN_CH0	Go
0x1E	NUM_7:0_EDP	NUM_7:0_EDP	Go
0x1F	NUM_15:8_EDP	NUM_15:8_EDP	Go
0x20	NUM_23:16_EDP	NUM_23:16_EDP	Go

Complex bit access types are encoded to fit into small table cells. Page 12: eDP/DP PLL Access Type Codes shows the codes that are used for access types in this section.

Table 8-508. Page 12: eDP/DP PLL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.11.1 PLL_LOCK_EDP Register (Address = 0x0) [Default = 0x01]

PLL_LOCK_EDP is shown in PLL_LOCK_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-509. PLL_LOCK_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7	PLL_LOCK_LOST	RC	0x0	Checks to see if PLL_LOCK has been lost since the last read of this register bit. Clears after each read.

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Table 8-509. PLL_LOCK_EDP Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.11.2 MASH_ORDER_EDP Register (Address = 0x4) [Default = 0x09]

MASH_ORDER_EDP is shown in MASH_ORDER_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-510. MASH_ORDER_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4:2	MASH_ORDER_2_0	R/W	0x2	Bits to set MASH order: 000: Integer 010: Fractional
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.11.3 NDIV_7:0_EDP Register (Address = 0x5) [Default = 0x96]

NDIV_7:0_EDP is shown in NDIV_7:0_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-511. NDIV_7:0_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT_7_0	R/W	0x96	Bits 7:0 of the feedback Ncount's divider value for the VCO frequency

8.6.2.11.4 NDIV_15:8_EDP Register (Address = 0x6) [Default = 0x00]

NDIV_15:8_EDP is shown in NDIV_15:8_EDP Register Field Descriptions.

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Table 8-512. NDIV_15:8_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NCOUNT_15_8	R/W	0x0	Bits 15:8 of the feedback Ncount's divider value for the VCO frequency

8.6.2.11.5 VCO_EDP Register (Address = 0xE) [Default = 0x9B]

VCO_EDP is shown in VCO_EDP Register Field Descriptions.

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Table 8-513. VCO_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7	TEMP_CMP_EN	R/W	0x1	Enables temperature compensation scheme.
6:4	PLL_LOCK_WAIT_2_0	R/W	0x1	Wait time after calibration to make sure the PLL has locked. 000: 25us 001: 50us 010: 75us 011: 100us 100: 150us 101: 200us 110: 300us 111: 400us
3:2	RESERVED	R/W	0x2	Reserved
1:0	RESERVED	R/W	0x3	Reserved

8.6.2.11.6 OVD_RAMPX_EDP Register (Address = 0xF) [Default = 0x00]

OVD_RAMPX_EDP is shown in OVD_RAMPX_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-514. OVD_RAMPX_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	OVD_SSCG_AUTOCFG	R/W	0x0	Spread Spectrum Auto Configuration Override Enable 0: Do not override SSCG auto-configuration 1: Override SSCG auto-configuration Note: Override enable is for RAMPx_INC, RAMPx_STOP, and SSCG_CNTR_SPRD. Override values are stored in registers 0x14-0x16.

8.6.2.11.7 SSCG_CTL1_EDP Register (Address = 0x14) [Default = 0x80]

SSCG_CTL1_EDP is shown in SSCG_CTL1_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-515. SSCG_CTL1_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7	SSCG_CNTR_SPRD	R/W	0x1	SSCG spread selection: 0: down-spread ramp 1: center-spread ramp
6:0	RAMPX_INC_6_0	R/W	0x0	Bits 6:0 of the increment value per step that will be added to the ramp for SSCG

8.6.2.11.8 SSCG_CTL2_EDP Register (Address = 0x15) [Default = 0x00]

SSCG_CTL2_EDP is shown in SSCG_CTL2_EDP Register Field Descriptions.

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Table 8-516. SSCG_CTL2_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_INC_14_7	R/W	0x0	Bits 14:7 of the increment value per step that will be added to the ramp for SSCG

8.6.2.11.9 SSCG_CTL3_EDP Register (Address = 0x16) [Default = 0x00]

SSCG_CTL3_EDP is shown in SSCG_CTL3_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-517. SSCG_CTL3_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RAMPX_STOP_7_0	R/W	0x0	Bits 7:0 of the number of PFD cyles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

8.6.2.11.10 SSCG_CTL4_EDP Register (Address = 0x17) [Default = 0x00]

SSCG_CTL4_EDP is shown in SSCG_CTL4_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-518. SSCG_CTL4_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	SSCG_EN		0x0	Enable spread spectrum clock generation. 0: disabled 1: enabled This register control is strapped at power-up based on the MODE_SEL2 pin.
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	RAMPX_STOP_9_8	R/W	0x0	Bits 9:8 of the number of PFD cyles to complete a single ramp segment, Total ramp cycles: rampx_stop x 4

8.6.2.11.11 DEN_7:0_EDP Register (Address = 0x18) [Default = 0xF6]

DEN_7:0_EDP is shown in DEN_7:0_EDP Register Field Descriptions.

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Table 8-519. DEN_7:0_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_7_0	R/W	0xF6	Bits 7:0 of the denominator value of MASH

8.6.2.11.12 DEN_15:8_EDP Register (Address = 0x19) [Default = 0xFF]

DEN_15:8_EDP is shown in DEN_15:8_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-520. DEN_15:8_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_15_8	R/W	0xFF	Bits 15:8 of the denominator value of MASH

8.6.2.11.13 DEN_23:16_EDP Register (Address = 0x1A) [Default = 0xFF]

DEN_23:16_EDP is shown in DEN_23:16_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-521. DEN_23:16_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DEN_MASH_23_16	R/W	0xFF	Bits 23:16 of the denominator value of MASH

8.6.2.11.14 PLL_OVD_EN_CH0 Register (Address = 0x1B) [Default = 0x00]

PLL_OVD_EN_CH0 is shown in PLL_OVD_EN_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-522. PLL_OVD_EN_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	OVD_EN_PLL_TOP_EN	R/W	0x0	Override enable for PLL 0: disable override 1: enable override The eDP PLL is always running. This override bit is needed to manually turn off the eDP PLL.
2	OVD_EN_PLL_TOP_VAL	R/W	0x0	Override value for PLL 0: disable PLL 1: enable PLL The eDP PLL is always running. This override bit is needed to manually turn off the eDP PLL.
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

8.6.2.11.15 NUM_7:0_EDP Register (Address = 0x1E) [Default = 0xF6]

NUM_7:0_EDP is shown in NUM_7:0_EDP Register Field Descriptions.

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Table 8-523. NUM_7:0_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_7_0	R/W	0xF6	Bits 7:0 of the numerator value of MASH

8.6.2.11.16 NUM_15:8_EDP Register (Address = 0x1F) [Default = 0xFF]

NUM_15:8_EDP is shown in NUM_15:8_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-524. NUM_15:8_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_15_8	R/W	0xFF	Bits 15:8 of the numerator value of MASH

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8.6.2.11.17 NUM_23:16_EDP Register (Address = 0x20) [Default = 0xFF]

NUM_23:16_EDP is shown in NUM_23:16_EDP Register Field Descriptions.

Return to the Summary Table.

Table 8-525. NUM_23:16_EDP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	NUM_MASH_23_16	R/W	0xFF	Bits 23:16 of the numerator value of MASH

8.6.2.12 Page 14: AEQ Registers

PAGE_14 Registers lists the memory-mapped registers for the Page 14: AEQ registers. All register offset addresses not listed in PAGE_14 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-526. PAGE_14 Registers

Address	Acronym	Register Name	Section
0x11	AEQ_INDEX_CH0	AEQ_INDEX_CH0	Go
0x17	AEQ_RELOCK_FPD3_CH0	AEQ_RELOCK_FPD3_CH0	Go
0x18	AEQ_MAX_FPD3_CH0	AEQ_MAX_FPD3_CH0	Go
0x19	AEQ_MIN_FPD3_CH0	AEQ_MIN_FPD3_CH0	Go
0x1A	AEQ_INDEX_OV_CH0	AEQ_INDEX_OV_CH0	Go
0x20	AEQ_CTL_0_CH0	AEQ_CTL_0_CH0	Go
0x21	AEQ_ERR_THRESH_CH0	AEQ_ERR_THRESH_CH0	Go
0x22	AEQ_MAX_FPD4_CH0	AEQ_MAX_FPD4_CH0	Go
0x23	AEQ_MIN_FPD4_CH0	AEQ_MIN_FPD4_CH0	Go
0x24	AEQ_SFILTER_CTL_CH0	AEQ_SFILTER_CTL_CH0	Go
0x26	SFILTER_CFG_CH0	SFILTER_CFG_CH0	Go
0x2C	AEQ_CTL_1_CH0	AEQ_CTL_1_CH0	Go
0x2D	AEQ_CTL_2_CH0	AEQ_CTL_2_CH0	Go
0x2E	AEQ_WAIT_CTL_CH0	AEQ_WAIT_CTL_CH0	Go
0x41	AEQ_INDEX_CH1	AEQ_INDEX_CH1	Go
0x47	AEQ_RELOCK_FPD3_CH1	AEQ_RELOCK_FPD3_CH1	Go
0x48	AEQ_MAX_FPD3_CH1	AEQ_MAX_FPD3_CH1	Go
0x49	AEQ_MIN_FPD3_CH1	AEQ_MIN_FPD3_CH1	Go
0x4A	AEQ_INDEX_OV_CH1	AEQ_INDEX_OV_CH1	Go
0x50	AEQ_CTL_0_CH1	AEQ_CTL_0_CH1	Go
0x51	AEQ_ERR_THRESH_CH1	AEQ_ERR_THRESH_CH1	Go
0x52	AEQ_MAX_FPD4_CH1	AEQ_MAX_FPD4_CH1	Go
0x53	AEQ_MIN_FPD4_CH1	AEQ_MIN_FPD4_CH1	Go
0x54	AEQ_SFILTER_CTL_CH1	AEQ_SFILTER_CTL_CH1	Go
0x56	SFILTER_CFG_CH1	SFILTER_CFG_CH1	Go
0x5C	AEQ_CTL_1_CH1	AEQ_CTL_1_CH1	Go
0x5D	AEQ_CTL_2_CH1	AEQ_CTL_2_CH1	Go
0x5E	AEQ_WAIT_CTL_CH1	AEQ_WAIT_CTL_CH1	Go

Complex bit access types are encoded to fit into small table cells. Page 14: AEQ Access Type Codes shows the codes that are used for access types in this section.

Table 8-527. Page 14: AEQ Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.6.2.12.1 AEQ_INDEX_CH0 Register (Address = 0x11) [Default = 0x00]

AEQ_INDEX_CH0 is shown in AEQ_INDEX_CH0 Register Field Descriptions.

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Table 8-528. AEQ_INDEX_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	AEQ_INDEX	R	0x0	AEQ_INDEX for CH0

8.6.2.12.2 AEQ_RELOCK_FPD3_CH0 Register (Address = 0x17) [Default = 0x72]

AEQ_RELOCK_FPD3_CH0 is shown in AEQ_RELOCK_FPD3_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-529. AEQ_RELOCK_FPD3_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R/W	0x7	Reserved
3:0	ADAPTIVE_EQ_RELOCK_TIME_FPD3	R/W	0x2	FPD3 AEQ Relock Time Time to wait for lock and error checking, before incrementing the EQ to next setting (for FPD3 only). For Relock time settings 0-7, wait time is: $2^{value + 12}$ * 40ns For Relock time settings 8-15, wait time is: $2^{value + 12}$ * 60ns

8.6.2.12.3 AEQ_MAX_FPD3_CH0 Register (Address = 0x18) [Default = 0x32]

AEQ_MAX_FPD3_CH0 is shown in AEQ_MAX_FPD3_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-530. AEQ_MAX_FPD3_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	AEQ_MAX_FPD3	R/W	0x32	Adaptive Equalizer Maximum value for FPD3 This register sets the maximum value for the Adaptive EQ algorithm for FPD3-mode only.

8.6.2.12.4 AEQ_MIN_FPD3_CH0 Register (Address = 0x19) [Default = 0x0E]

AEQ_MIN_FPD3_CH0 is shown in AEQ_MIN_FPD3_CH0 Register Field Descriptions.

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Table 8-531. AEQ_MIN_FPD3_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	AEQ_MIN_FPD3	R/W	0xE	Adaptive Equalizer Minimum value for FPD3 This register sets the minimum value for the Adaptive EQ algorithm in FPD3-mode only.

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8.6.2.12.5 AEQ_INDEX_OV_CH0 Register (Address = 0x1A) [Default = 0x16]

AEQ_INDEX_OV_CH0 is shown in AEQ_INDEX_OV_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-532. AEQ_INDEX_OV_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	AEQ_INDEX_OV_SEL	R/W	0x0	AEQ_INDEX override select 0: Disable AEQ index override. AEQ index is selected from the state machine. 1: Enable AEQ index override. AEQ index is selected from the AEQ_INDEX_OV field.
5:0	AEQ_INDEX_OV	R/W	0x16	Override value for AEQ_INDEX.

8.6.2.12.6 AEQ_CTL_0_CH0 Register (Address = 0x20) [Default = 0xA7]

AEQ_CTL_0_CH0 is shown in AEQ_CTL_0_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-533. AEQ_CTL_0_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	AEQ_RESTART	R/W	0x0	Set high to restart AEQ adaptation from initial value. Method is to write HIGH and then write LOW. This bit is not self clearing. Adaption will be restarted on both ports.
5	RESERVED	R/W	0x1	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:0	RESERVED	R/W	0x7	Reserved

8.6.2.12.7 AEQ_ERR_THRESH_CH0 Register (Address = 0x21) [Default = 0x0A]

AEQ_ERR_THRESH_CH0 is shown in AEQ_ERR_THRESH_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-534. AEQ_ERR_THRESH_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	AEQ_ERR_THRESHOLD	R/W	0xA	AEQ Error Threshold This register controls the error threshold to determine when to re-adapt the EQ settings. This register should not be programmed to a value of 0.

8.6.2.12.8 AEQ_MAX_FPD4_CH0 Register (Address = 0x22) [Default = 0x3F]

AEQ_MAX_FPD4_CH0 is shown in AEQ_MAX_FPD4_CH0 Register Field Descriptions.

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Table 8-535. AEQ_MAX_FPD4_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

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Table 8-535. AEQ_MAX_FPD4_CH0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:0	AEQ_MAX_FPD4	R/W	0x3F	FPD4 Adaptive Equalizer Maximum value This register sets the maximum value for the FPD4 Adaptive EQ algorithm.

8.6.2.12.9 AEQ_MIN_FPD4_CH0 Register (Address = 0x23) [Default = 0x00]

AEQ_MIN_FPD4_CH0 is shown in AEQ_MIN_FPD4_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-536. AEQ_MIN_FPD4_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	AEQ_MIN_FPD4	R/W	0x0	FPD4 Adaptive Equalizer Minimum value This register sets the minimum value for the FPD4 Adaptive EQ algorithm.

8.6.2.12.10 AEQ_SFILTER_CTL_CH0 Register (Address = 0x24) [Default = 0x61]

AEQ_SFILTER_CTL_CH0 is shown in AEQ_SFILTER_CTL_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-537. AEQ_SFILTER_CTL_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	AEQ_SFILTER_EN	R/W	0x1	Enable SFILTER Adaption with AEQ Setting this bit allows SFILTER adaption as part of the Adaptive Equalizer algorithm.
5	AEQ_OUTER_LOOP	R/W	0x1	AEQ outer loop control This bit controls whether the Equalizer or SFILTER adaption is the outer loop when the AEQ adaption includes SFILTER adaption. 0: AEQ is inner loop, SFILTER is outer loop 1: AEQ is outer loop, SFILTER is inner loop
4	AEQ_SFIL_ORDER	R/W	0x0	AEQ SFILTER Adapt order This bit controls the order of adaption for SFILTER values during Adaptive Equalization. 0: Default order, start at largest clock delay 1: Start at midpoint, no additional clock or data delay
3:0	ADAPTIVE_EQ_RELOCK_TIME	R/W	0x1	FPD4 AEQ Relock time Time to wait for lock and check for errors before incrementing the EQ to next setting (for FPD4 only). For Relock time settings 0-7, wait time is: $2^{value + 12}$ * 40ns For Relock time settings 8-15, wait time is: $2^{value + 12}$ * 60ns

8.6.2.12.11 SFILTER_CFG_CH0 Register (Address = 0x26) [Default = 0x87]

SFILTER_CFG_CH0 is shown in SFILTER_CFG_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-538. SFILTER_CFG_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	SFILTER_MAX	R/W	0x8	SFILTER Maximum setting This field controls the maximum SFILTER setting. Allowed values are 0-12 with 6 being the mid point. These values are used during AEQ adaption, but not with dynamic SFILTER control.
3:0	SFILTER_MIN	R/W	0x7	SFILTER Maximum setting This field controls the maximum SFILTER setting. Allowed values are 0-12, where 6 is the mid point. These values are used during AEQ adaption, but not with dynamic SFILTER control.

8.6.2.12.12 AEQ_CTL_1_CH0 Register (Address = 0x2C) [Default = 0x19]

AEQ_CTL_1_CH0 is shown in AEQ_CTL_1_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-539. AEQ_CTL_1_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	AEQ_SCAN_EN_FPD3	R/W	0x1	Enable AEQ Scan operation for FPD3 When enabled, the AEQ State machine will scan each EQ setting, searching for the largest window of error-free operation. At completion of scan, it will set the EQ to the mid-point of the largest detected operating window.
3	AEQ_SCAN_EN_FPD4	R/W	0x1	Enable AEQ Scan operation for FPD4 When enabled, the AEQ State machine will scan each EQ setting, searching for the largest window of error-free operation. At completion of scan, it will set the EQ to the mid-point of the largest detected operating window.
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.12.13 AEQ_CTL_2_CH0 Register (Address = 0x2D) [Default = 0x10]

AEQ_CTL_2_CH0 is shown in AEQ_CTL_2_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-540. AEQ_CTL_2_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x1	Reserved
3:0	EQ_OFFSET	R/W	0x0	EQ Offset At completion of Adaptive Equalization, when the EQ has stabilized, this offset value will be added to the EQ setting to attempt to better center the EQ setting. This value is a two's-complement value ranging from +7 (0x7) to -8 (0x8). EQ Offset value will not be used if AEQ_SCAN_EN_FPDx is enabled.

8.6.2.12.14 AEQ_WAIT_CTL_CH0 Register (Address = 0x2E) [Default = 0x00]

AEQ_WAIT_CTL_CH0 is shown in AEQ_WAIT_CTL_CH0 Register Field Descriptions.

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Table 8-541. AEQ_WAIT_CTL_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	AEQ_RELOCK_WAIT_FPD3	R/W	0x0	FPD3 AEQ Relock wait time Time to wait for lock checking for errors during AEQ adaption. For AEQ_RELOCK_WAIT_FPD4 values 0-7, wait time is: $2^{value + 9}$ * 40ns For AEQ_RELOCK_WAIT_FPD4 values 8-15, wait time is: $2^{value + 9}$ * 60ns Note: Relock wait time should be set smaller than the Relock time controlled be the ADAPTIVE_EQ_RELOCK_TIME_FPD3 field.
3:0	AEQ_RELOCK_WAIT_FPD4	R/W	0x0	FPD4 AEQ Relock wait time Time to wait for lock checking for errors during AEQ adaption. For Relock wait settings 0-7, wait time is: $2^{value + 9}$ * 40ns For Relock wait settings 8-15, wait time is: $2^{value + 9}$ * 60ns Note: Relock wait time should be set smaller than the Relock time controlled be the ADAPTIVE_EQ_RELOCK_TIME field.

8.6.2.12.15 AEQ_INDEX_CH1 Register (Address = 0x41) [Default = 0x00]

AEQ_INDEX_CH1 is shown in AEQ_INDEX_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-542. AEQ_INDEX_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	AEQ_INDEX	R	0x0	AEQ_INDEX for CH1

8.6.2.12.16 AEQ_RELOCK_FPD3_CH1 Register (Address = 0x47) [Default = 0x72]

AEQ_RELOCK_FPD3_CH1 is shown in AEQ_RELOCK_FPD3_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-543. AEQ_RELOCK_FPD3_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R/W	0x7	Reserved
3:0	ADAPTIVE_EQ_RELOCK_TIME_FPD3	R/W	0x2	FPD3 AEQ Relock Time Time to wait for lock and check for errors before incrementing the EQ to next setting (for FPD3 only). For Relock time settings 0-7, wait time is: $2^{value + 12}$ * 40ns For Relock time settings 8-15, wait time is: $2^{value + 4}$ * 60ns

8.6.2.12.17 AEQ_MAX_FPD3_CH1 Register (Address = 0x48) [Default = 0x32]

AEQ_MAX_FPD3_CH1 is shown in AEQ_MAX_FPD3_CH1 Register Field Descriptions.

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Table 8-544. AEQ_MAX_FPD3_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

Table 8-544. AEQ_MAX_FPD3_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:0	AEQ_MAX_FPD3	R/W	0x32	Adaptive Equalizer Maximum value for FPD3 This register sets the maximum value for the Adaptive EQ algorithm for FPD3-mode only.

8.6.2.12.18 AEQ_MIN_FPD3_CH1 Register (Address = 0x49) [Default = 0x0E]

AEQ_MIN_FPD3_CH1 is shown in AEQ_MIN_FPD3_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-545. AEQ_MIN_FPD3_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	AEQ_MIN_FPD3	R/W	0xE	Adaptive Equalizer Minimum value for FPD3 This register sets the minimum value for the Adaptive EQ algorithm in FPD3-mode only.

8.6.2.12.19 AEQ_INDEX_OV_CH1 Register (Address = 0x4A) [Default = 0x16]

AEQ_INDEX_OV_CH1 is shown in AEQ_INDEX_OV_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-546. AEQ_INDEX_OV_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	AEQ_INDEX_OV_SEL	R/W	0x0	AEQ_INDEX override select 0: Disable AEQ index override. AEQ index is selected from the state machine. 1: Enable AEQ index override. AEQ index is selected from the AEQ_INDEX_OV field.
5:0	AEQ_INDEX_OV	R/W	0x16	Override value for AEQ_INDEX.

8.6.2.12.20 AEQ_CTL_0_CH1 Register (Address = 0x50) [Default = 0xA7]

AEQ_CTL_0_CH1 is shown in AEQ_CTL_0_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-547. AEQ_CTL_0_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	AEQ_RESTART	R/W	0x0	Set high to restart AEQ adaptation from initial value. Method is to write HIGH and then write LOW. This bit is not self clearing. Adaption will be restarted on both ports.
5	RESERVED	R/W	0x1	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:0	RESERVED	R/W	0x7	Reserved

8.6.2.12.21 AEQ_ERR_THRESH_CH1 Register (Address = 0x51) [Default = 0x0A]

AEQ_ERR_THRESH_CH1 is shown in AEQ_ERR_THRESH_CH1 Register Field Descriptions.

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Return to the Summary Table.

Table 8-548. AEQ_ERR_THRESH_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	AEQ_ERR_THRESHOLD	R/W	0xA	AEQ Error Threshold This register controls the error threshold to determine when to re-adapt the EQ settings. This register should not be programmed to a value of 0.

8.6.2.12.22 AEQ_MAX_FPD4_CH1 Register (Address = 0x52) [Default = 0x3F]

AEQ_MAX_FPD4_CH1 is shown in AEQ_MAX_FPD4_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-549. AEQ_MAX_FPD4_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	AEQ_MAX_FPD4	R/W	0x3F	FPD4 Adaptive Equalizer Maximum value This register sets the maximum value for the FPD4 Adaptive EQ algorithm.

8.6.2.12.23 AEQ_MIN_FPD4_CH1 Register (Address = 0x53) [Default = 0x00]

AEQ_MIN_FPD4_CH1 is shown in AEQ_MIN_FPD4_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-550. AEQ_MIN_FPD4_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	AEQ_MIN_FPD4	R/W	0x0	FPD4 Adaptive Equalizer Minimum value This register sets the minimum value for the FPD4 Adaptive EQ algorithm.

8.6.2.12.24 AEQ_SFILTER_CTL_CH1 Register (Address = 0x54) [Default = 0x61]

AEQ_SFILTER_CTL_CH1 is shown in AEQ_SFILTER_CTL_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-551. AEQ_SFILTER_CTL_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	AEQ_SFILTER_EN	R/W	0x1	Enable SFILTER Adaption with AEQ Setting this bit allows SFILTER adaption as part of the Adaptive Equalizer algorithm.
5	AEQ_OUTER_LOOP	R/W	0x1	AEQ outer loop control This bit controls whether the Equalizer or SFILTER adaption is the outer loop when the AEQ adaption includes SFILTER adaption. 0: AEQ is inner loop, SFILTER is outer loop 1: AEQ is outer loop, SFILTER is inner loop
4	AEQ_SFIL_ORDER	R/W	0x0	AEQ SFILTER Adapt order This bit controls the order of adaption for SFILTER values during Adaptive Equalization. 0: Default order, start at largest clock delay 1: Start at midpoint, no additional clock or data delay

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Table 8-551. AEQ_SFILTER_CTL_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	ADAPTIVE_EQ_RELOCK_TIME	R/W	0x1	FPD4 AEQ Relock time Time to wait for lock and check for errors before incrementing the EQ to next setting (for FPD4 only). For Relock time settings 0-7, wait time is: $2^{value + 12}$ * 40ns For Relock time settings 8-15, wait time is: $2^{value + 4}$ * 60ns

8.6.2.12.25 SFILTER_CFG_CH1 Register (Address = 0x56) [Default = 0x87]

SFILTER_CFG_CH1 is shown in SFILTER_CFG_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-552. SFILTER_CFG_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	SFILTER_MAX	R/W	0x8	SFILTER Maximum setting This field controls the maximum SFILTER setting. Allowed values are 0-12 with 6 being the mid point. These values are used during AEQ adaption, but not with dynamic SFILTER control.
3:0	SFILTER_MIN	R/W	0x7	SFILTER Maximum setting This field controls the maximum SFILTER setting. Allowed values are 0-12, where 6 is the mid point. These values are used during AEQ adaption, but not with dynamic SFILTER control.

8.6.2.12.26 AEQ_CTL_1_CH1 Register (Address = 0x5C) [Default = 0x19]

AEQ_CTL_1_CH1 is shown in AEQ_CTL_1_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-553. AEQ_CTL_1_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	AEQ_SCAN_EN_FPD3	R/W	0x1	Enable AEQ Scan operation for FPD3 When enabled, the AEQ State machine will scan each EQ setting, searching for the largest window of error-free operation. At completion of scan, it will set the EQ to the mid-point of the largest detected operating window.
3	AEQ_SCAN_EN_FPD4	R/W	0x1	Enable AEQ Scan operation for FPD4 When enabled, the AEQ State machine will scan each EQ setting, searching for the largest window of error-free operation. At completion of scan, it will set the EQ to the mid-point of the largest detected operating window.
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

8.6.2.12.27 AEQ_CTL_2_CH1 Register (Address = 0x5D) [Default = 0x10]

AEQ_CTL_2_CH1 is shown in AEQ_CTL_2_CH1 Register Field Descriptions.

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Table 8-554. AEQ_CTL_2_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x1	Reserved
3:0	EQ_OFFSET	R/W	0x0	EQ Offset At completion of Adaptive Equalization, when the EQ has stabilized, this offset value will be added to the EQ setting to attempt to better center the EQ setting. This value is a two's-complement value ranging from +7 (0x7) to -8 (0x8). EQ Offset value will not be used if AEQ_SCAN_EN_FPDx is enabled.

8.6.2.12.28 AEQ_WAIT_CTL_CH1 Register (Address = 0x5E) [Default = 0x00]

AEQ_WAIT_CTL_CH1 is shown in AEQ_WAIT_CTL_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-555. AEQ_WAIT_CTL_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	AEQ_RELOCK_WAIT_FPD3	R/W	0x0	FPD3 AEQ Relock wait time Time to wait for lock checking for errors during AEQ adaption. For AEQ_RELOCK_WAIT_FPD4 values 0-7, wait time is: $2^{value + 9}$ * 40ns For AEQ_RELOCK_WAIT_FPD4 values 8-15, wait time is: $2^{value + 9}$ * 60ns Note: Relock wait time should be set smaller than the Relock time controlled be the ADAPTIVE_EQ_RELOCK_TIME_FPD3 field.
3:0	AEQ_RELOCK_WAIT_FPD4	R/W	0x0	FPD4 AEQ Relock wait time Time to wait for lock checking for errors during AEQ adaption. For Relock wait settings 0-7, wait time is: $2^{value + 9}$ * 40ns For Relock wait settings 8-15, wait time is: $2^{value + 9}$ * 60ns Note: Relock wait time should be set smaller than the Relock time controlled be the ADAPTIVE_EQ_RELOCK_TIME field.

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8.6.2.13 Page 15: DFT/MBIST Registers

PAGE_15 Registers lists the memory-mapped registers for the Page 15: DFT/MBIST registers. All register offset addresses not listed in PAGE_15 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-556. PAGE_15 Registers

Address	Acronym	Register Name	Section
0xB	GPIO_EN_PULL_LOW_1	GPIO_EN_PULL_LOW_1	Go
0xC	GPIO_EN_PULL_LOW_2	GPIO_EN_PULL_LOW_2	Go

Complex bit access types are encoded to fit into small table cells. Page 15: DFT/MBIST Access Type Codes shows the codes that are used for access types in this section.

Table 8-557. Page 15: DFT/MBIST Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.13.1 GPIO_EN_PULL_LOW_1 Register (Address = 0xB) [Default = 0xFF]

GPIO_EN_PULL_LOW_1 is shown in GPIO_EN_PULL_LOW_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-558. GPIO_EN_PULL_LOW_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GPIO_EN_PULL_LOW_7_0	R/W	0xFF	GPIO[7:0] Enable Pull Low Enables the 25 kΩ pull-down resistor on GPIO[7:0]. 0: Disable pull-down resistor 1: Enable pull-down resistor

8.6.2.13.2 GPIO_EN_PULL_LOW_2 Register (Address = 0xC) [Default = 0x3F]

GPIO_EN_PULL_LOW_2 is shown in GPIO_EN_PULL_LOW_2 Register Field Descriptions.

Return to the Summary Table.

Table 8-559. GPIO_EN_PULL_LOW_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	GPIO_EN_PULL_LOW_13_8	R/W	0x3F	GPIO[13:8] Enable Pull Low Enables the 25 kΩ pull-down resistor on GPIO[13:8]. 0: Disable pull-down resistor 1: Enable pull-down resistor

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8.6.2.14 Page 17: FPD TX Link Layer Registers

PAGE_17 Registers lists the memory-mapped registers for the Page 17: FPD TX Link Layer registers. All register offset addresses not listed in PAGE_17 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-560. PAGE_17 Registers

Address	Acronym	Register Name	Section
0x0	LINK_LAYER_CTL	LINK_LAYER_CTL	Go
0x1	LINK0_STREAM_EN	LINK0_STREAM_EN	Go
0x2	LINK0_MAP_REG0	LINK0_MAP_REG0	Go
0x3	LINK0_MAP_REG1	LINK0_MAP_REG1	Go
0x4	LINK0_MAP_REG2	LINK0_MAP_REG2	Go
0x6	LINK0_SLOT_REQ0	LINK0_SLOT_REQ0	Go
0x7	LINK0_SLOT_REQ1	LINK0_SLOT_REQ1	Go
0x8	LINK0_SLOT_REQ2	LINK0_SLOT_REQ2	Go
0x9	LINK0_SLOT_REQ3	LINK0_SLOT_REQ3	Go
0xA	LINK0_SLOT_REQ4	LINK0_SLOT_REQ4	Go
0xB	LINK0_SLOT_REQ5	LINK0_SLOT_REQ5	Go
0xE	LINK0_CONFIG	LINK0_CONFIG	Go
0x11	LINK1_STREAM_EN	LINK1_STREAM_EN	Go
0x12	LINK1_MAP_REG0	LINK1_MAP_REG0	Go
0x13	LINK1_MAP_REG1	LINK1_MAP_REG1	Go
0x14	LINK1_MAP_REG2	LINK1_MAP_REG2	Go
0x16	LINK1_SLOT_REQ0	LINK1_SLOT_REQ0	Go
0x17	LINK1_SLOT_REQ1	LINK1_SLOT_REQ1	Go
0x18	LINK1_SLOT_REQ2	LINK1_SLOT_REQ2	Go
0x19	LINK1_SLOT_REQ3	LINK1_SLOT_REQ3	Go
0x1A	LINK1_SLOT_REQ4	LINK1_SLOT_REQ4	Go
0x1B	LINK1_SLOT_REQ5	LINK1_SLOT_REQ5	Go
0x1E	LINK1_CONFIG	LINK1_CONFIG	Go
0x22	PKT_FIFO_OVRFLW_STS	PKT_FIFO_OVRFLW_STS	Go
0x23	PKT_FIFO_OVRFLW_CLR	PKT_FIFO_OVRFLW_CLR	Go
0x25	LINK_ECC_TEST0	LINK_ECC_TEST0	Go
0x26	LINK_ECC_TEST1	LINK_ECC_TEST1	Go
0x30	FPD_TX_HPOL_CTL	FPD_TX_HPOL_CTL	Go
0x31	FPD_TX_VPOL_CTL	FPD_TX_VPOL_CTL	Go
0x32	FPD_TX_POL_CTL	FPD_TX_POL_CTL	Go
0x80	ABUFF0_CTL0	ABUFF0_CTL0	Go
0x82	ABUFF0_CTL2	ABUFF0_CTL2	Go
0x86	ABUFF0_CTL6	ABUFF0_CTL6	Go
0x88	ABUFF1_CTL0	ABUFF1_CTL0	Go
0x8A	ABUFF1_CTL2	ABUFF1_CTL2	Go
0x8E	ABUFF1_CTL6	ABUFF1_CTL6	Go
0x90	ABUFF2_CTL0	ABUFF2_CTL0	Go
0x92	ABUFF2_CTL2	ABUFF2_CTL2	Go
0x96	ABUFF2_CTL6	ABUFF2_CTL6	Go
0x98	ABUFF3_CTL0	ABUFF3_CTL0	Go
0x9A	ABUFF3_CTL2	ABUFF3_CTL2	Go

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Table 8-560. PAGE_17 Registers (continued)

Address	Acronym	Register Name	Section
0x9E	ABUFF3_CTL6	ABUFF3_CTL6	Go
0xA0	ABUFF4_CTL0	ABUFF4_CTL0	Go
0xA2	ABUFF4_CTL2	ABUFF4_CTL2	Go
0xA6	ABUFF4_CTL6	ABUFF4_CTL6	Go
0xA8	ABUFF5_CTL0	ABUFF5_CTL0	Go
0xAA	ABUFF5_CTL2	ABUFF5_CTL2	Go
0xAE	ABUFF5_CTL6	ABUFF5_CTL6	Go
0xB0	ABUFF6_CTL0	ABUFF6_CTL0	Go
0xB2	ABUFF6_CTL2	ABUFF6_CTL2	Go
0xB6	ABUFF6_CTL6	ABUFF6_CTL6	Go
0xB8	ABUFF7_CTL0	ABUFF7_CTL0	Go
0xBA	ABUFF7_CTL2	ABUFF7_CTL2	Go
0xBE	ABUFF7_CTL6	ABUFF7_CTL6	Go
0xC0	ABUFF8_CTL0	ABUFF8_CTL0	Go
0xC2	ABUFF8_CTL2	ABUFF8_CTL2	Go
0xC6	ABUFF8_CTL6	ABUFF8_CTL6	Go
0xC8	ABUFF9_CTL0	ABUFF9_CTL0	Go
0xCA	ABUFF9_CTL2	ABUFF9_CTL2	Go
0xCE	ABUFF9_CTL6	ABUFF9_CTL6	Go
0xD0	ABUFF10_CTL0	ABUFF10_CTL0	Go
0xD2	ABUFF10_CTL2	ABUFF10_CTL2	Go
0xD6	ABUFF10_CTL6	ABUFF10_CTL6	Go
0xD8	ABUFF11_CTL0	ABUFF11_CTL0	Go
0xDA	ABUFF11_CTL2	ABUFF11_CTL2	Go
0xDE	ABUFF11_CTL6	ABUFF11_CTL6	Go

Complex bit access types are encoded to fit into small table cells. Page 17: FPD TX Link Layer Access Type Codes shows the codes that are used for access types in this section.

Table 8-561. Page 17: FPD TX Link Layer Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.14.1 LINK_LAYER_CTL Register (Address = 0x0) [Default = 0x00]

LINK_LAYER_CTL is shown in LINK_LAYER_CTL Register Field Descriptions.

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Return to the Summary Table.

Table 8-562. LINK_LAYER_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	RESERVED
3	EN_NEW_TSLOT1	W1S	0x0	Enable New Time-slot Assignments for Link Layer 1 Setting this bit to a 1 will enable the device to begin using the new time-slot information programmed into the LINK1_SLOT_REQ registers. This register bit will be cleared once the new time-slot information has been enabled
2	LINK_LAYER_1_EN	R/W	0x0	Link Layer Enable for Link Layer 1 0: All link layer 1 daisy chain streams disabled 1: Streams with LINK1_STREAM_EN (address 0x11) bits set will be enabled
1	EN_NEW_TSLOT0	W1S	0x0	Enable New Time-slot Assignments for Link Layer 0 Setting this bit to a 1 will enable the device to begin using the new time-slot information programmed into the LINK0_SLOT_REQ registers. This register bit will be cleared once the new time-slot information has been enabled
0	LINK_LAYER_0_EN	R/W	0x0	Link Layer Enable for Link Layer 0 0: All link layer 0 daisy chain streams disabled 1: Streams with LINK0_STREAM_EN (address 0x1) bits set will be enabled

8.6.2.14.2 LINK0_STREAM_EN Register (Address = 0x1) [Default = 0x00]

LINK0_STREAM_EN is shown in LINK0_STREAM_EN Register Field Descriptions.

Return to the Summary Table.

This register enables the output streams for daisy chain port 0 (link layer 0).

Table 8-563. LINK0_STREAM_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	RESERVED
5	LINK0_STREAM_EN5	R/W	0x0	Link Layer 0 Daisy Chain Output Stream 5 Enable 0: Output stream 5 disabled 1: Output stream 5 link layer processing enabled
4	LINK0_STREAM_EN4	R/W	0x0	Link Layer 0 Daisy Chain Output Stream 4 Enable 0: Output stream 4 disabled 1: Output stream 4 link layer processing enabled
3	LINK0_STREAM_EN3	R/W	0x0	Link Layer 0 Daisy Chain Output Stream 3 Enable 0: Output stream 3 disabled 1: Output stream 3 link layer processing enabled
2	LINK0_STREAM_EN2	R/W	0x0	Link Layer 0 Daisy Chain Output Stream 2 Enable 0: Output stream 2 disabled 1: Output stream 2 link layer processing enabled
1	LINK0_STREAM_EN1	R/W	0x0	Link Layer 0 Daisy Chain Output Stream 1 Enable 0: Output stream 1 disabled 1: Output stream 1 link layer processing enabled
0	LINK0_STREAM_EN0	R/W	0x0	Link Layer 0 Daisy Chain Output Stream 0 Enable 0: Output stream 0 disabled 1: Output stream 0 link layer processing enabled

8.6.2.14.3 LINK0_MAP_REG0 Register (Address = 0x2) [Default = 0x10]

LINK0_MAP_REG0 is shown in LINK0_MAP_REG0 Register Field Descriptions.

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Return to the Summary Table.

This register assigns the incoming streams mapped on the main page 0xD2-0xD4.

Table 8-564. LINK0_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:4	LINK0_STREAM_MAP1	R/W	0x1	Link Layer 0 Stream 1 Map Selects the input stream for assignment to daisy chain output stream 1. If the LINK0_STREAM_EN[1] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 1 1: Input stream 1 is mapped to output stream 1 2: Input stream 2 is mapped to output stream 1 3: Input stream 3 is mapped to output stream 1 4: Input stream 4 is mapped to output stream 1 5: Input stream 5 is mapped to output stream 1 6: Reserved 7: Reserved
3	RESERVED	R	0x0	RESERVED
2:0	LINK0_STREAM_MAP0	R/W	0x0	Link Layer 0 Stream 0 Map Selects the input stream for assignment to daisy chain output stream 0. If the LINK0_STREAM_EN[0] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 0 1: Input stream 1 is mapped to output stream 0 2: Input stream 2 is mapped to output stream 0 3: Input stream 3 is mapped to output stream 0 4: Input stream 4 is mapped to output stream 0 5: Input stream 5 is mapped to output stream 0 6: Reserved 7: Reserved

8.6.2.14.4 LINK0_MAP_REG1 Register (Address = 0x3) [Default = 0x32]

LINK0_MAP_REG1 is shown in LINK0_MAP_REG1 Register Field Descriptions.

Return to the Summary Table.

This register assigns the incoming streams mapped on the main page 0xD2-0xD4.

Table 8-565. LINK0_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:4	LINK0_STREAM_MAP3	R/W	0x3	Link Layer 0 Stream 3 Map Selects the input stream for assignment to daisy chain output stream 3. If the LINK0_STREAM_EN[3] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 3 1: Input stream 1 is mapped to output stream 3 2: Input stream 2 is mapped to output stream 3 3: Input stream 3 is mapped to output stream 3 4: Input stream 4 is mapped to output stream 3 5: Input stream 5 is mapped to output stream 3 6: Reserved 7: Reserved
3	RESERVED	R	0x0	RESERVED

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Table 8-565. LINK0_MAP_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2:0	LINK0_STREAM_MAP2	R/W	0x2	Link Layer 0 Stream 2 Map Selects the input stream for assignment to daisy chain output stream 2. If the LINK0_STREAM_EN[2] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 2 1: Input stream 1 is mapped to output stream 2 2: Input stream 2 is mapped to output stream 2 3: Input stream 3 is mapped to output stream 2 4: Input stream 4 is mapped to output stream 2 5: Input stream 5 is mapped to output stream 2 6: Reserved 7: Reserved

8.6.2.14.5 LINK0_MAP_REG2 Register (Address = 0x4) [Default = 0x00]

LINK0_MAP_REG2 is shown in LINK0_MAP_REG2 Register Field Descriptions.

Return to the Summary Table.

This register assigns the incoming streams mapped on the main page 0xD2-0xD4.

Table 8-566. LINK0_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:4	LINK0_STREAM_MAP5	R/W	0x0	Link Layer 0 Stream 5 Map Selects the input stream for assignment to daisy chain output stream 5. If the LINK0_STREAM_EN[5] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 5 1: Input stream 1 is mapped to output stream 5 2: Input stream 2 is mapped to output stream 5 3: Input stream 3 is mapped to output stream 5 4: Input stream 4 is mapped to output stream 5 5: Input stream 5 is mapped to output stream 5 6: Reserved 7: Reserved
3	RESERVED	R	0x0	RESERVED
2:0	LINK0_STREAM_MAP4	R/W	0x0	Link Layer 0 Stream 4 Map Selects the input stream for assignment to daisy chain output stream 4. If the LINK0_STREAM_EN[4] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 4 1: Input stream 1 is mapped to output stream 4 2: Input stream 2 is mapped to output stream 4 3: Input stream 3 is mapped to output stream 4 4: Input stream 4 is mapped to output stream 4 5: Input stream 5 is mapped to output stream 4 6: Reserved 7: Reserved

8.6.2.14.6 LINK0_SLOT_REQ0 Register (Address = 0x6) [Default = 0x00]

LINK0_SLOT_REQ0 is shown in LINK0_SLOT_REQ0 Register Field Descriptions.

Return to the Summary Table.

Table 8-567. LINK0_SLOT_REQ0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED

Table 8-567. LINK0_SLOT_REQ0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	LINK0_SLOT_REQ0	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending daisy chain stream 0. The total number of LINK0 (link layer 0) slots should add up to 65. If less than 65 are assigned, the extra slots will be assigned to stream 0.

8.6.2.14.7 LINK0_SLOT_REQ1 Register (Address = 0x7) [Default = 0x00]

LINK0_SLOT_REQ1 is shown in LINK0_SLOT_REQ1 Register Field Descriptions.

Return to the Summary Table.

Table 8-568. LINK0_SLOT_REQ1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:0	LINK0_SLOT_REQ1	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending daisy chain stream 1.

8.6.2.14.8 LINK0_SLOT_REQ2 Register (Address = 0x8) [Default = 0x00]

LINK0_SLOT_REQ2 is shown in LINK0_SLOT_REQ2 Register Field Descriptions.

Return to the Summary Table.

Table 8-569. LINK0_SLOT_REQ2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:0	LINK0_SLOT_REQ2	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending daisy chain stream 2.

8.6.2.14.9 LINK0_SLOT_REQ3 Register (Address = 0x9) [Default = 0x00]

LINK0_SLOT_REQ3 is shown in LINK0_SLOT_REQ3 Register Field Descriptions.

Return to the Summary Table.

Table 8-570. LINK0_SLOT_REQ3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:0	LINK0_SLOT_REQ3	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending daisy chain stream 3.

8.6.2.14.10 LINK0_SLOT_REQ4 Register (Address = 0xA) [Default = 0x00]

LINK0_SLOT_REQ4 is shown in LINK0_SLOT_REQ4 Register Field Descriptions.

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Table 8-571. LINK0_SLOT_REQ4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED

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Table 8-571. LINK0_SLOT_REQ4 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	LINK0_SLOT_REQ4	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending daisy chain stream 4.

8.6.2.14.11 LINK0_SLOT_REQ5 Register (Address = 0xB) [Default = 0x00]

LINK0_SLOT_REQ5 is shown in LINK0_SLOT_REQ5 Register Field Descriptions.

Return to the Summary Table.

Table 8-572. LINK0_SLOT_REQ5 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6:0	LINK0_SLOT_REQ5	R/W	0x0	Link Layer 0 Slot Request Register Set to the number of slots requested for sending daisy chain stream 5.

8.6.2.14.12 LINK0_CONFIG Register (Address = 0xE) [Default = 0x00]

LINK0_CONFIG is shown in LINK0_CONFIG Register Field Descriptions.

Return to the Summary Table.

Table 8-573. LINK0_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	RESERVED
1	RESERVED	R/W	0x0	Reserved
0	LINK0_EVENT_MODE_EN	R/W	0x0	Link Layer 0 Event Mode enable This bit controls how the link layer sends HSync/VSync information. 0: Send HSync/VSync pulses with active period matching incoming video 1: Send a single cycle event to indicate HSync and VSync

8.6.2.14.13 LINK1_STREAM_EN Register (Address = 0x11) [Default = 0x00]

LINK1_STREAM_EN is shown in LINK1_STREAM_EN Register Field Descriptions.

Return to the Summary Table.

Table 8-574. LINK1_STREAM_EN Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	RESERVED
5	LINK1_STREAM_EN5	R/W	0x0	Link Layer 1 Daisy Chain Output Stream 5 Enable 0: Output stream 5 disabled 1: Output stream 5 link layer processing enabled
4	LINK1_STREAM_EN4	R/W	0x0	Link Layer 1 Daisy Chain Output Stream 4 Enable 0: Output stream 4 disabled 1: Output stream 4 link layer processing enabled
3	LINK1_STREAM_EN3	R/W	0x0	Link Layer 1 Daisy Chain Output Stream 3 Enable 0: Output stream 3 disabled 1: Output stream 3 link layer processing enabled
2	LINK1_STREAM_EN2	R/W	0x0	Link Layer 1 Daisy Chain Output Stream 2 Enable 0: Output stream 2 disabled 1: Output stream 2 link layer processing enabled

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Table 8-574. LINK1_STREAM_EN Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	LINK1_STREAM_EN1	R/W	0x0	Link Layer 1 Daisy Chain Output Stream 1 Enable 0: Output stream 1 disabled 1: Output stream 1 link layer processing enabled
0	LINK1_STREAM_EN0	R/W	0x0	Link Layer 1 Daisy Chain Output Stream 0 Enable 0: Output stream 0 disabled 1: Output stream 0 link layer processing enabled

8.6.2.14.14 LINK1_MAP_REG0 Register (Address = 0x12) [Default = 0x10]

LINK1_MAP_REG0 is shown in LINK1_MAP_REG0 Register Field Descriptions.

Return to the Summary Table.

This register assigns the incoming streams mapped on the main page 0xD2-0xD4.

Table 8-575. LINK1_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK1_STREAM_MAP1	R/W	0x1	Link Layer 1 Stream 1 Map Selects the input stream for assignment to daisy chain output stream 1. If the LINK0_STREAM_EN[1] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 1 1: Input stream 1 is mapped to output stream 1 2: Input stream 2 is mapped to output stream 1 3: Input stream 3 is mapped to output stream 1 4: Input stream 4 is mapped to output stream 1 5: Input stream 5 is mapped to output stream 1 6: Reserved 7: Reserved
3	RESERVED	R	0x0	RESERVED
2:0	LINK1_STREAM_MAP0	R/W	0x0	Link Layer 1 Stream 0 Map Selects the input stream for assignment to daisy chain output stream 0. If the LINK0_STREAM_EN[0] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 0 1: Input stream 1 is mapped to output stream 0 2: Input stream 2 is mapped to output stream 0 3: Input stream 3 is mapped to output stream 0 4: Input stream 4 is mapped to output stream 0 5: Input stream 5 is mapped to output stream 0 6: Reserved 7: Reserved

8.6.2.14.15 LINK1_MAP_REG1 Register (Address = 0x13) [Default = 0x32]

LINK1_MAP_REG1 is shown in LINK1_MAP_REG1 Register Field Descriptions.

Return to the Summary Table.

This register assigns the incoming streams mapped on the main page 0xD2-0xD4.

Table 8-576. LINK1_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved

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Table 8-576. LINK1_MAP_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:4	LINK1_STREAM_MAP3	R/W	0x3	Link Layer 1 Stream 3 Map Selects the input stream for assignment to daisy chain output stream 3. If the LINK0_STREAM_EN[3] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 3 1: Input stream 1 is mapped to output stream 3 2: Input stream 2 is mapped to output stream 3 3: Input stream 3 is mapped to output stream 3 4: Input stream 4 is mapped to output stream 3 5: Input stream 5 is mapped to output stream 3 6: Reserved 7: Reserved
3	RESERVED	R	0x0	RESERVED
2:0	LINK1_STREAM_MAP2	R/W	0x2	Link Layer 1 Stream 2 Map Selects the input stream for assignment to daisy chain output stream 2. If the LINK0_STREAM_EN[2] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 2 1: Input stream 1 is mapped to output stream 2 2: Input stream 2 is mapped to output stream 2 3: Input stream 3 is mapped to output stream 2 4: Input stream 4 is mapped to output stream 2 5: Input stream 5 is mapped to output stream 2 6: Reserved 7: Reserved

8.6.2.14.16 LINK1_MAP_REG2 Register (Address = 0x14) [Default = 0x00]

LINK1_MAP_REG2 is shown in LINK1_MAP_REG2 Register Field Descriptions.

Return to the Summary Table.

This register assigns the incoming streams mapped on the main page 0xD2-0xD4.

Table 8-577. LINK1_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:4	LINK1_STREAM_MAP5	R/W	0x0	Link Layer 1 Stream 5 Map Selects the input stream for assignment to daisy chain output stream 5. If the LINK0_STREAM_EN[5] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 5 1: Input stream 1 is mapped to output stream 5 2: Input stream 2 is mapped to output stream 5 3: Input stream 3 is mapped to output stream 5 4: Input stream 4 is mapped to output stream 5 5: Input stream 5 is mapped to output stream 5 6: Reserved 7: Reserved
3	RESERVED	R	0x0	RESERVED
2:0	LINK1_STREAM_MAP4	R/W	0x0	Link Layer 1 Stream 4 Map Selects the input stream for assignment to daisy chain output stream 4. If the LINK0_STREAM_EN[4] is set to 0, this value will be ignored. 0: Input stream 0 is mapped to output stream 4 1: Input stream 1 is mapped to output stream 4 2: Input stream 2 is mapped to output stream 4 3: Input stream 3 is mapped to output stream 4 4: Input stream 4 is mapped to output stream 4 5: Input stream 5 is mapped to output stream 4 6: Reserved 7: Reserved

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8.6.2.14.17 LINK1_SLOT_REQ0 Register (Address = 0x16) [Default = 0x00]

LINK1_SLOT_REQ0 is shown in LINK1_SLOT_REQ0 Register Field Descriptions.

Return to the Summary Table.

Table 8-578. LINK1_SLOT_REQ0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ0	R/W	0x0	Link Layer 1 Slot Request Register Set to the number of slots requested for sending Video Stream 0. The total number of LINK1 slots should add up to 65. If less than 65 are assigned, the extra slots will be assigned to stream 0.

8.6.2.14.18 LINK1_SLOT_REQ1 Register (Address = 0x17) [Default = 0x00]

LINK1_SLOT_REQ1 is shown in LINK1_SLOT_REQ1 Register Field Descriptions.

Return to the Summary Table.

Table 8-579. LINK1_SLOT_REQ1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ1	R/W	0x0	Link Layer 1 Slot Request Register Set to the number of slots requested for sending Video Stream 1.

8.6.2.14.19 LINK1_SLOT_REQ2 Register (Address = 0x18) [Default = 0x00]

LINK1_SLOT_REQ2 is shown in LINK1_SLOT_REQ2 Register Field Descriptions.

Return to the Summary Table.

Table 8-580. LINK1_SLOT_REQ2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ2	R/W	0x0	Link Layer 1 Slot Request Register Set to the number of slots requested for sending Video Stream 2.

8.6.2.14.20 LINK1_SLOT_REQ3 Register (Address = 0x19) [Default = 0x00]

LINK1_SLOT_REQ3 is shown in LINK1_SLOT_REQ3 Register Field Descriptions.

Return to the Summary Table.

Table 8-581. LINK1_SLOT_REQ3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ3	R/W	0x0	Link Layer 1 Slot Request Register Set to the number of slots requested for sending Video Stream 3.

8.6.2.14.21 LINK1_SLOT_REQ4 Register (Address = 0x1A) [Default = 0x00]

LINK1_SLOT_REQ4 is shown in LINK1_SLOT_REQ4 Register Field Descriptions.

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Table 8-582. LINK1_SLOT_REQ4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ4	R/W	0x0	Link Layer 1 Slot Request Register Set to the number of slots requested for sending Video Stream 4.

8.6.2.14.22 LINK1_SLOT_REQ5 Register (Address = 0x1B) [Default = 0x00]

LINK1_SLOT_REQ5 is shown in LINK1_SLOT_REQ5 Register Field Descriptions.

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Table 8-583. LINK1_SLOT_REQ5 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	LINK1_SLOT_REQ5	R/W	0x0	Link Layer 1 Slot Request Register Set to the number of slots requested for sending Video Stream 5.

8.6.2.14.23 LINK1_CONFIG Register (Address = 0x1E) [Default = 0x00]

LINK1_CONFIG is shown in LINK1_CONFIG Register Field Descriptions.

Return to the Summary Table.

Table 8-584. LINK1_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	LINK1_EVENT_MODE_EN	R/W	0x0	Link Layer 1 Event Mode enable This bit controls how the link layer sends HSync/VSync information. 0: Send HSync/VSync pulses with active period matching incoming video 1: Send a single cycle event to indicate HSync and VSync

8.6.2.14.24 PKT_FIFO_OVRFLW_STS Register (Address = 0x22) [Default = 0x00]

PKT_FIFO_OVRFLW_STS is shown in PKT_FIFO_OVRFLW_STS Register Field Descriptions.

Return to the Summary Table.

Table 8-585. PKT_FIFO_OVRFLW_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	PKT_FIFO_OVRFLW_STS_0	R	0x0	Packet FIFO Overflow Status for each Stream 0 0: No FIFO overflow detected 1: FIFO overflow detected

8.6.2.14.25 PKT_FIFO_OVRFLW_CLR Register (Address = 0x23) [Default = 0x00]

PKT_FIFO_OVRFLW_CLR is shown in PKT_FIFO_OVRFLW_CLR Register Field Descriptions.

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Return to the Summary Table.

Table 8-586. PKT_FIFO_OVRFLW_CLR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	PKT_FIFO_OVRFLW_CLR_0	R/W	0x0	Clear Packet FIFO Overflow Status for Stream 0 0: No change 1: PKT_FIFO_OVRFLW_STS register 0x22[0] is reset to 0 This bit is not self-clearing and must be programmed back to 0.

8.6.2.14.26 LINK_ECC_TEST0 Register (Address = 0x25) [Default = 0x00]

LINK_ECC_TEST0 is shown in LINK_ECC_TEST0 Register Field Descriptions.

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Table 8-587. LINK_ECC_TEST0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FORCE_ECC_STREAM_EN	R/W	0x0	Force ECC Errors on Selected Stream Enable 0: FORCE_ECC_STREAM control in the LINK_ECC_TEST1 register(0x26) will be ignored and errors will be forced on all active streams 1: FORCE_ECC_STREAM field will be used to only force errors on the selected stream.
5	RESERVED	R/W	0x0	Reserved
4	FORCE_ECC_2BIT_SEL	R/W	0x0	Number of Bit Errors Injected in Control Field Indicates the number of bits which will have errors forced in the control field 0: 1-bit error 1: 2-bit error
3:2	FORCE_ECC_ERR_FIELD_SEL	R/W	0x0	Force Errors on Control Fields 0: Normal operation 1: Reserved 2: Reserved 3: Forces ECC errors on control fields
1	FORCE_1_ECC_ERR	R/W	0x0	FORCE ERROR SINGLE 0: Normal operation 1: A single ECC error is forced under the conditions specified in the LINK_ECC_TEST registers
0	FORCE_CONT_ECC_ERR	R/W	0x0	FORCE ERROR CONTINUOUS 0: Normal operation 1: An ECC error is forced continually under the conditions specified in the LINK_ECC_TEST registers This bit overrides Bit 1.

8.6.2.14.27 LINK_ECC_TEST1 Register (Address = 0x26) [Default = 0x08]

LINK_ECC_TEST1 is shown in LINK_ECC_TEST1 Register Field Descriptions.

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Table 8-588. LINK_ECC_TEST1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	FORCE_ECC_LINK1_SEL	R/W	0x0	Select Link Layer 1 0: No errors forced on Link 1 1: Force errors on Link 1
3	FORCE_ECC_LINK0_SEL	R/W	0x1	Select Link Layer 0 0: No errors forced on Link 0 1: Force errors on Link 0
2:0	FORCE_ECC_STREAM	R/W	0x0	Force ECC Stream control If FORCE_ECC_STREAM_EN is set, errors will be forced only on the selected stream. Errors can only be forced onto one stream at a time. 000: Stream 0 001: Stream 1 010: Stream 2 011: Stream 3 100: Stream 4 101: Stream 5 11x: Reserved

8.6.2.14.28 FPD_TX_HPOL_CTL Register (Address = 0x30) [Default = 0x00]

FPD_TX_HPOL_CTL is shown in FPD_TX_HPOL_CTL Register Field Descriptions.

Return to the Summary Table.

This register must be enabled by setting FPD_TX_POL_CTL register 0x32[0]= 1.

Table 8-589. FPD_TX_HPOL_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	FPD_TX_HPOL_SEL5	R/W	0x0	HSYNC Polarity Select for Input Stream 5 0: Active high polarity 1: Active low polarity
4	FPD_TX_HPOL_SEL4	R/W	0x0	HSYNC Polarity Select for Input Stream 4 0: Active high polarity 1: Active low polarity
3	FPD_TX_HPOL_SEL3	R/W	0x0	HSYNC Polarity Select for Input Stream 3 0: Active high polarity 1: Active low polarity
2	FPD_TX_HPOL_SEL2	R/W	0x0	HSYNC Polarity Select for Input Stream 2 0: Active high polarity 1: Active low polarity
1	FPD_TX_HPOL_SEL1	R/W	0x0	HSYNC Polarity Select for Input Stream 1 0: Active high polarity 1: Active low polarity
0	FPD_TX_HPOL_SEL0	R/W	0x0	HSYNC Polarity Select for Input Stream 0 0: Active high polarity 1: Active low polarity

8.6.2.14.29 FPD_TX_VPOL_CTL Register (Address = 0x31) [Default = 0x00]

FPD_TX_VPOL_CTL is shown in FPD_TX_VPOL_CTL Register Field Descriptions.

Return to the Summary Table.

This register must be enabled by setting FPD_TX_POL_CTL register 0x32[0]= 1.

Table 8-590. FPD_TX_VPOL_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	FPD_TX_VPOL_SEL5	R/W	0x0	VSYNC Polarity Select for Input Stream 5 0: Active high polarity 1: Active low polarity
4	FPD_TX_VPOL_SEL4	R/W	0x0	VSYNC Polarity Select for Input Stream 4 0: Active high polarity 1: Active low polarity
3	FPD_TX_VPOL_SEL3	R/W	0x0	VSYNC Polarity Select for Input Stream 3 0: Active high polarity 1: Active low polarity
2	FPD_TX_VPOL_SEL2	R/W	0x0	VSYNC Polarity Select for Input Stream 2 0: Active high polarity 1: Active low polarity
1	FPD_TX_VPOL_SEL1	R/W	0x0	VSYNC Polarity Select for Input Stream 1 0: Active high polarity 1: Active low polarity
0	FPD_TX_VPOL_SEL0	R/W	0x0	VSYNC Polarity Select for Input Stream 0 0: Active high polarity 1: Active low polarity

8.6.2.14.30 FPD_TX_POL_CTL Register (Address = 0x32) [Default = 0x00]

FPD_TX_POL_CTL is shown in FPD_TX_POL_CTL Register Field Descriptions.

Return to the Summary Table.

Table 8-591. FPD_TX_POL_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RESERVED	R	0x0	Reserved
0	FPD_TX_POL_SEL_EN	R/W	0x0	Stream Polarity Select Enable Setting this bit to 1 enables the HSYNC and VSYNC polarity controls. These controls are in registers 0x30-0x31 and should be used if a stream requires active low polarity.

8.6.2.14.31 ABUFF0_CTL0 Register (Address = 0x80) [Default = 0x01]

ABUFF0_CTL0 is shown in ABUFF0_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF0 Control Register 0

Table 8-592. ABUFF0_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved

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Table 8-592. ABUFF0_CTL0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF0_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF0_ENABLE	R/W	0x1	0: ABUFF0 disabled 1: ABUFF0 enabled

8.6.2.14.32 ABUFF0_CTL2 Register (Address = 0x82) [Default = 0x00]

ABUFF0_CTL2 is shown in ABUFF0_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF0 Control Register 2

Table 8-593. ABUFF0_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF0 Destination Select ABUFF0_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF0 Source Select These bits should not be written to. The local deserializer's ABUFF0 is loaded with the data from the upstream device's ABUFF0.

8.6.2.14.33 ABUFF0_CTL6 Register (Address = 0x86) [Default = 0x00]

ABUFF0_CTL6 is shown in ABUFF0_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF0 Control Register 6 - Status Register

Table 8-594. ABUFF0_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF0 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved

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Table 8-594. ABUFF0_CTL6 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	STS_ABUFF_OF	RC	0x0	ABUFF0 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF0 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.34 ABUFF1_CTL0 Register (Address = 0x88) [Default = 0x01]

ABUFF1_CTL0 is shown in ABUFF1_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF1 Control Register 0

Table 8-595. ABUFF1_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF1_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF1_ENABLE	R/W	0x1	0: ABUFF1 disabled 1: ABUFF1 enabled

8.6.2.14.35 ABUFF1_CTL2 Register (Address = 0x8A) [Default = 0x00]

ABUFF1_CTL2 is shown in ABUFF1_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF1 Control Register 2

Table 8-596. ABUFF1_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF1 Destination Select ABUFF1_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF1 Source Select These bits should not be written to. The local deserializer's ABUFF1 is loaded with the data from the upstream device's ABUFF1.

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8.6.2.14.36 ABUFF1_CTL6 Register (Address = 0x8E) [Default = 0x00]

ABUFF1_CTL6 is shown in ABUFF1_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF1 Control Register 6 - Status Register

Table 8-597. ABUFF1_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF1 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF1 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF1 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.37 ABUFF2_CTL0 Register (Address = 0x90) [Default = 0x01]

ABUFF2_CTL0 is shown in ABUFF2_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF2 Control Register 0

Table 8-598. ABUFF2_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF2_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF2_ENABLE	R/W	0x1	0: ABUFF2 disabled 1: ABUFF2 enabled

8.6.2.14.38 ABUFF2_CTL2 Register (Address = 0x92) [Default = 0x00]

ABUFF2_CTL2 is shown in ABUFF2_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF2 Control Register 2

Table 8-599. ABUFF2_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF2 Destination Select ABUFF2_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF2 Source Select These bits should not be written to. The local deserializer's ABUFF2 is loaded with the data from the upstream device's ABUFF2.

8.6.2.14.39 ABUFF2_CTL6 Register (Address = 0x96) [Default = 0x00]

ABUFF2_CTL6 is shown in ABUFF2_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF2 Control Register 6 - Status Register

Table 8-600. ABUFF2_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF2 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF2 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF2 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.40 ABUFF3_CTL0 Register (Address = 0x98) [Default = 0x01]

ABUFF3_CTL0 is shown in ABUFF3_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF3 Control Register 0

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Table 8-601. ABUFF3_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF3_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF3_ENABLE	R/W	0x1	0: ABUFF3 disabled 1: ABUFF3 enabled

8.6.2.14.41 ABUFF3_CTL2 Register (Address = 0x9A) [Default = 0x00]

ABUFF3_CTL2 is shown in ABUFF3_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF3 Control Register 2

Table 8-602. ABUFF3_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF3 Destination Select ABUFF3_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF3 Source Select These bits should not be written to. The local deserializer's ABUFF3 is loaded with the data from the upstream device's ABUFF3.

8.6.2.14.42 ABUFF3_CTL6 Register (Address = 0x9E) [Default = 0x00]

ABUFF3_CTL6 is shown in ABUFF3_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF3 Control Register 6 - Status Register

Table 8-603. ABUFF3_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected

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Table 8-603. ABUFF3_CTL6 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF3 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF3 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF3 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.43 ABUFF4_CTL0 Register (Address = 0xA0) [Default = 0x01]

ABUFF4_CTL0 is shown in ABUFF4_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF4 Control Register 0

Table 8-604. ABUFF4_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF4_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF4_ENABLE	R/W	0x1	0: ABUFF4 disabled 1: ABUFF4 enabled

8.6.2.14.44 ABUFF4_CTL2 Register (Address = 0xA2) [Default = 0x00]

ABUFF4_CTL2 is shown in ABUFF4_CTL2 Register Field Descriptions.

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ABUFF4 Control Register 2

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Table 8-605. ABUFF4_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF4 Destination Select ABUFF4_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF4 Source Select These bits should not be written to. The local deserializer's ABUFF4 is loaded with the data from the upstream device's ABUFF4.

8.6.2.14.45 ABUFF4_CTL6 Register (Address = 0xA6) [Default = 0x00]

ABUFF4_CTL6 is shown in ABUFF4_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF4 Control Register 6 - Status Register

Table 8-606. ABUFF4_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF4 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF4 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF4 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.46 ABUFF5_CTL0 Register (Address = 0xA8) [Default = 0x01]

ABUFF5_CTL0 is shown in ABUFF5_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF5 Control Register 0

Table 8-607. ABUFF5_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved

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Table 8-607. ABUFF5_CTL0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF5_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF5_ENABLE	R/W	0x1	0: ABUFF5 disabled 1: ABUFF5 enabled

8.6.2.14.47 ABUFF5_CTL2 Register (Address = 0xAA) [Default = 0x00]

ABUFF5_CTL2 is shown in ABUFF5_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF5 Control Register 2

Table 8-608. ABUFF5_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF5 Destination Select ABUFF5_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF5 Source Select These bits should not be written to. The local deserializer's ABUFF5 is loaded with the data from the upstream device's ABUFF5.

8.6.2.14.48 ABUFF5_CTL6 Register (Address = 0xAE) [Default = 0x00]

ABUFF5_CTL6 is shown in ABUFF5_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF5 Control Register 6 - Status Register

Table 8-609. ABUFF5_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF5 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved

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Table 8-609. ABUFF5_CTL6 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	STS_ABUFF_OF	RC	0x0	ABUFF5 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF5 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.49 ABUFF6_CTL0 Register (Address = 0xB0) [Default = 0x01]

ABUFF6_CTL0 is shown in ABUFF6_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF6 Control Register 0

Table 8-610. ABUFF6_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF6_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF6_ENABLE	R/W	0x1	0: ABUFF6 disabled 1: ABUFF6 enabled

8.6.2.14.50 ABUFF6_CTL2 Register (Address = 0xB2) [Default = 0x00]

ABUFF6_CTL2 is shown in ABUFF6_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF6 Control Register 2

Table 8-611. ABUFF6_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF6 Destination Select ABUFF6_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF6 Source Select These bits should not be written to. The local deserializer's ABUFF6 is loaded with the data from the upstream device's ABUFF6.

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8.6.2.14.51 ABUFF6_CTL6 Register (Address = 0xB6) [Default = 0x00]

ABUFF6_CTL6 is shown in ABUFF6_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF6 Control Register 6 - Status Register

Table 8-612. ABUFF6_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF6 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF6 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF6 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.52 ABUFF7_CTL0 Register (Address = 0xB8) [Default = 0x01]

ABUFF7_CTL0 is shown in ABUFF7_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF7 Control Register 0

Table 8-613. ABUFF7_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF7_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF7_ENABLE	R/W	0x1	0: ABUFF7 disabled 1: ABUFF7 enabled

8.6.2.14.53 ABUFF7_CTL2 Register (Address = 0xBA) [Default = 0x00]

ABUFF7_CTL2 is shown in ABUFF7_CTL2 Register Field Descriptions.

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Return to the Summary Table.

ABUFF7 Control Register 2

Table 8-614. ABUFF7_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF7 Destination Select ABUFF7_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF7 Source Select These bits should not be written to. The local deserializer's ABUFF7 is loaded with the data from the upstream device's ABUFF7.

8.6.2.14.54 ABUFF7_CTL6 Register (Address = 0xBE) [Default = 0x00]

ABUFF7_CTL6 is shown in ABUFF7_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF7 Control Register 6 - Status Register

Table 8-615. ABUFF7_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF7 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF7 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF7 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.55 ABUFF8_CTL0 Register (Address = 0xC0) [Default = 0x01]

ABUFF8_CTL0 is shown in ABUFF8_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF8 Control Register 0

Table 8-616. ABUFF8_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF8_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF8_ENABLE	R/W	0x1	0: ABUFF8 disabled 1: ABUFF8 enabled

8.6.2.14.56 ABUFF8_CTL2 Register (Address = 0xC2) [Default = 0x00]

ABUFF8_CTL2 is shown in ABUFF8_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF8 Control Register 2

Table 8-617. ABUFF8_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF8 Destination Select ABUFF8_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF8 Source Select These bits should not be written to. The local deserializer's ABUFF8 is loaded with the data from the upstream device's ABUFF8.

8.6.2.14.57 ABUFF8_CTL6 Register (Address = 0xC6) [Default = 0x00]

ABUFF8_CTL6 is shown in ABUFF8_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF8 Control Register 6 - Status Register

Table 8-618. ABUFF8_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected

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Table 8-618. ABUFF8_CTL6 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF8 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF8 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF8 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.58 ABUFF9_CTL0 Register (Address = 0xC8) [Default = 0x01]

ABUFF9_CTL0 is shown in ABUFF9_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF9 Control Register 0

Table 8-619. ABUFF9_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF9_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF9_ENABLE	R/W	0x1	0: ABUFF9 disabled 1: ABUFF9 enabled

8.6.2.14.59 ABUFF9_CTL2 Register (Address = 0xCA) [Default = 0x00]

ABUFF9_CTL2 is shown in ABUFF9_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF9 Control Register 2

Table 8-620. ABUFF9_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF9 Destination Select ABUFF9_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF9 Source Select These bits should not be written to. The local deserializer's ABUFF9 is loaded with the data from the upstream device's ABUFF9.

8.6.2.14.60 ABUFF9_CTL6 Register (Address = 0xCE) [Default = 0x00]

ABUFF9_CTL6 is shown in ABUFF9_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF9 Control Register 6 - Status Register

Table 8-621. ABUFF9_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF9 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF9 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF9 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.61 ABUFF10_CTL0 Register (Address = 0xD0) [Default = 0x01]

ABUFF10_CTL0 is shown in ABUFF10_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF10 Control Register 0

Table 8-622. ABUFF10_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved

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Table 8-622. ABUFF10_CTL0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF10_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF10_ENABLE	R/W	0x1	0: ABUFF10 disabled 1: ABUFF10 enabled

8.6.2.14.62 ABUFF10_CTL2 Register (Address = 0xD2) [Default = 0x00]

ABUFF10_CTL2 is shown in ABUFF10_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF10 Control Register 2

Table 8-623. ABUFF10_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF10 Destination Select ABUFF10_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF10 Source Select These bits should not be written to. The local deserializer's ABUFF10 is loaded with the data from the upstream device's ABUFF10.

8.6.2.14.63 ABUFF10_CTL6 Register (Address = 0xD6) [Default = 0x00]

ABUFF10_CTL6 is shown in ABUFF10_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF10 Control Register 6 - Status Register

Table 8-624. ABUFF10_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF10 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved

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Table 8-624. ABUFF10_CTL6 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	STS_ABUFF_OF	RC	0x0	ABUFF10 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF10 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

8.6.2.14.64 ABUFF11_CTL0 Register (Address = 0xD8) [Default = 0x01]

ABUFF11_CTL0 is shown in ABUFF11_CTL0 Register Field Descriptions.

Return to the Summary Table.

ABUFF11 Control Register 0

Table 8-625. ABUFF11_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SDP_OFFSET_CRCTN_BYP	R/W	0x0	0: Offset correction feature enabled -> if the previous packet was read incompletely, the offset will be set to the beginning of a new ABUF packet 1: Offset correction feature is bypassed
6:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	ABUFF_TO_PORT_SEL	R/W	0x0	ABUFF Port Select This bit works in conjunction with ABUFF11_CTL2[7:5]. If ABUFF is mapped to an FPD-Link: 0: Maps to Port 0 Link Layer 1: Maps to Port 1 Link Layer If ABUF is mapped to eDP output: 0: Selects both eDP0 and eDP1 1: Selects eDP0 only
0	ABUFF11_ENABLE	R/W	0x1	0: ABUFF11 disabled 1: ABUFF11 enabled

8.6.2.14.65 ABUFF11_CTL2 Register (Address = 0xDA) [Default = 0x00]

ABUFF11_CTL2 is shown in ABUFF11_CTL2 Register Field Descriptions.

Return to the Summary Table.

ABUFF11 Control Register 2

Table 8-626. ABUFF11_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	ABUFF_TO_DEST_SEL	R/W	0x0	ABUFF11 Destination Select ABUFF11_CTL0[1] to selects the desired port 000: AUBFF mapped to stream 0 001: ABUFF mapped to stream 1 010: ABUFF mapped to stream 2 011: ABUFF mapped to stream 3 100: ABUFF mapped to stream 4 101: ABUFF mapped to stream 5 110: ABUFF mapped to eDP 111: Reserved
4:0	ABUFF_SRC	R/W	0x0	ABUFF11 Source Select These bits should not be written to. The local deserializer's ABUFF11 is loaded with the data from the upstream device's ABUFF11.

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8.6.2.14.66 ABUFF11_CTL6 Register (Address = 0xDE) [Default = 0x00]

ABUFF11_CTL6 is shown in ABUFF11_CTL6 Register Field Descriptions.

Return to the Summary Table.

ABUFF11 Control Register 6 - Status Register

Table 8-627. ABUFF11_CTL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	STS_INT_GLOBAL	R	0x0	Global Interrupt This bit indicates if a local interrupt has occurred in any of the 12 ABUFF blocks. 0: No interrupt 1: Global interrupt detected
4	STS_INT_LOCAL	R	0x0	Local Interrupt for ABUFF11 This bit indicates if an overflow or packet loss occurred. (See bits1:0 for specifics) 0: No interrupt 1: Local interrupt detected.
3:2	RESERVED	R	0x0	Reserved
1	STS_ABUFF_OF	RC	0x0	ABUFF11 FIFO Overflow 0: No FIFO overflow 1: FIFO overflow detected
0	STS_FIFO_PKT_DROPPED	RC	0x0	ABUFF11 FIFO Packet Drop 0: No packets dropped 1: Packet(s) were dropped due to an offset correction feature

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8.6.2.15 Page 18: FPD RX Link Layer Registers

PAGE_18 Registers lists the memory-mapped registers for the Page 18: FPD RX Link Layer registers. All register offset addresses not listed in PAGE_18 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-628. PAGE_18 Registers

Address	Acronym	Register Name	Section
0x29	COUNTER_CAPTURE	COUNTER_CAPTURE	Go
0x2A	COUNTER_CLEAR	COUNTER_CLEAR	Go
0x2B	ECC_ERROR_COUNTER_0	ECC_ERROR_COUNTER_0	Go
0x2C	ECC_ERROR_COUNTER_1	ECC_ERROR_COUNTER_1	Go
0x2E	CTL_FRAME_COUNTER_0	CTL_FRAME_COUNTER_0	Go
0x2F	CTL_FRAME_COUNTER_1	CTL_FRAME_COUNTER_1	Go
0x30	CTL_FRAME_COUNTER_2	CTL_FRAME_COUNTER_2	Go
0x31	DATA_FRAME_COUNTER_0	DATA_FRAME_COUNTER_0	Go
0x32	DATA_FRAME_COUNTER_1	DATA_FRAME_COUNTER_1	Go
0x33	DATA_FRAME_COUNTER_2	DATA_FRAME_COUNTER_2	Go
0x34	CRC_COUNTERS_0	CRC_COUNTERS_0	Go
0x35	CRC_COUNTERS_1	CRC_COUNTERS_1	Go
0x36	PACKET_CNT_COUNTER_0	PACKET_CNT_COUNTER_0	Go
0x37	PACKET_CNT_COUNTER_1	PACKET_CNT_COUNTER_1	Go
0x39	S0_HACTIVE0	S0_HACTIVE0	Go
0x3A	S0_HACTIVE1	S0_HACTIVE1	Go
0x3B	S1_HACTIVE0	S1_HACTIVE0	Go
0x3C	S1_HACTIVE1	S1_HACTIVE1	Go
0x3D	S2_HACTIVE0	S2_HACTIVE0	Go
0x3E	S2_HACTIVE1	S2_HACTIVE1	Go
0x3F	S3_HACTIVE0	S3_HACTIVE0	Go
0x40	S3_HACTIVE1	S3_HACTIVE1	Go
0x41	S4_HACTIVE0	S4_HACTIVE0	Go
0x42	S4_HACTIVE1	S4_HACTIVE1	Go
0x43	S5_HACTIVE0	S5_HACTIVE0	Go
0x44	S5_HACTIVE1	S5_HACTIVE1	Go
0x45	VIDEO_PIXEL_SIZE0	VIDEO_PIXEL_SIZE0	Go
0x46	VIDEO_PIXEL_SIZE1	VIDEO_PIXEL_SIZE1	Go
0x47	DATA_FRAME_PASS_THRESHOLD_0	DATA_FRAME_PASS_THRESHOLD_0	Go
0x48	DATA_FRAME_PASS_THRESHOLD_1	DATA_FRAME_PASS_THRESHOLD_1	Go
0x49	DATA_FRAME_FAIL_THRESHOLD_0	DATA_FRAME_FAIL_THRESHOLD_0	Go
0x4A	DATA_FRAME_FAIL_THRESHOLD_1	DATA_FRAME_FAIL_THRESHOLD_1	Go
0x4D	INTR_CTL_FPD4_RX	INTR_CTL_FPD4_RX	Go
0x4E	FPD4_RX_INT_STS	FPD4_RX_INT_STS	Go
0x50	STS_FPD4_LOCK	STS_FPD4_LOCK	Go
0x51	PASS_STATUS_CONFIG	PASS_STATUS_CONFIG	Go
0x52	PASS_STATUS_CONTROL	PASS_STATUS_CONTROL	Go
0x53	STS_PASS	STS_PASS	Go

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Table 8-628. PAGE_18 Registers (continued)

Address	Acronym	Register Name	Section
0x54	VID_FRAME_CNT_P1_LSB	VID_FRAME_CNT_P1_LSB	Go
0x55	VID_FRAME_CNT_P1_MSB	VID_FRAME_CNT_P1_MSB	Go
0x56	VID_ERR_CNT_P1_LSB	VID_ERR_CNT_P1_LSB	Go
0x57	VID_ERR_CNT_P1_MSB	VID_ERR_CNT_P1_MSB	Go
0x58	VID_FRAME_CNT_P0_LSB	VID_FRAME_CNT_P0_LSB	Go
0x59	VID_FRAME_CNT_P0_MSB	VID_FRAME_CNT_P0_MSB	Go
0x5A	VID_ERR_CNT_P0_LSB	VID_ERR_CNT_P0_LSB	Go
0x5B	VID_ERR_CNT_P0_MSB	VID_ERR_CNT_P0_MSB	Go
0x60	STREAM_0_COUNT_CONTROL	STREAM_0_COUNT_CONTROL	Go
0x61	S0_ECC_ERR_COUNTER0	S0_ECC_ERR_COUNTER0	Go
0x62	S0_ECC_ERR_COUNTER1	S0_ECC_ERR_COUNTER1	Go
0x63	S0_CRC_COUNTER0	S0_CRC_COUNTER0	Go
0x64	S0_CRC_COUNTER1	S0_CRC_COUNTER1	Go
0x65	S0_HACTIVE_COUNTER0	S0_HACTIVE_COUNTER0	Go
0x66	S0_HACTIVE_COUNTER1	S0_HACTIVE_COUNTER1	Go
0x67	S0_VTOTAL_COUNTER0	S0_VTOTAL_COUNTER0	Go
0x68	S0_VTOTAL_COUNTER1	S0_VTOTAL_COUNTER1	Go
0x69	S0_STATUS	S0_STATUS	Go
0x70	S1_COUNT_CONTROL	S1_COUNT_CONTROL	Go
0x71	S1_ECC_ERR_COUNTER0	S1_ECC_ERR_COUNTER0	Go
0x72	S1_ECC_ERR_COUNTER1	S1_ECC_ERR_COUNTER1	Go
0x73	S1_CRC_COUNTER0	S1_CRC_COUNTER0	Go
0x74	S1_CRC_COUNTER1	S1_CRC_COUNTER1	Go
0x75	S1_HACTIVE_COUNTER0	S1_HACTIVE_COUNTER0	Go
0x76	S1_HACTIVE_COUNTER1	S1_HACTIVE_COUNTER1	Go
0x77	S1_VTOTAL_COUNTER0	S1_VTOTAL_COUNTER0	Go
0x78	S1_VTOTAL_COUNTER1	S1_VTOTAL_COUNTER1	Go
0x79	S1_STATUS	S1_STATUS	Go
0x80	S2_COUNT_CONTROL	S2_COUNT_CONTROL	Go
0x81	S2_ECC_ERR_COUNTER0	S2_ECC_ERR_COUNTER0	Go
0x82	S2_ECC_ERR_COUNTER1	S2_ECC_ERR_COUNTER1	Go
0x83	S2_CRC_COUNTER0	S2_CRC_COUNTER0	Go
0x84	S2_CRC_COUNTER1	S2_CRC_COUNTER1	Go
0x85	S2_HACTIVE_COUNTER0	S2_HACTIVE_COUNTER0	Go
0x86	S2_HACTIVE_COUNTER1	S2_HACTIVE_COUNTER1	Go
0x87	S2_VTOTAL_COUNTER0	S2_VTOTAL_COUNTER0	Go
0x88	S2_VTOTAL_COUNTER1	S2_VTOTAL_COUNTER1	Go
0x89	S2_STATUS	S2_STATUS	Go
0x90	S3_COUNT_CONTROL	S3_COUNT_CONTROL	Go
0x91	S3_ECC_ERR_COUNTER0	S3_ECC_ERR_COUNTER0	Go
0x92	S3_ECC_ERR_COUNTER1	S3_ECC_ERR_COUNTER1	Go
0x93	S3_CRC_COUNTER0	S3_CRC_COUNTER0	Go
0x94	S3_CRC_COUNTER1	S3_CRC_COUNTER1	Go
0x95	S3_HACTIVE_COUNTER0	S3_HACTIVE_COUNTER0	Go
0x96	S3_HACTIVE_COUNTER1	S3_HACTIVE_COUNTER1	Go

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Table 8-628. PAGE_18 Registers (continued)

Address	Acronym	Register Name	Section
0x97	S3_VTOTAL_COUNTER0	S3_VTOTAL_COUNTER0	Go
0x98	S3_VTOTAL_COUNTER1	S3_VTOTAL_COUNTER1	Go
0x99	S3_STATUS	S3_STATUS	Go
0xA0	S4_COUNT_CONTROL	S4_COUNT_CONTROL	Go
0xA1	S4_ECC_ERR_COUNTER0	S4_ECC_ERR_COUNTER0	Go
0xA2	S4_ECC_ERR_COUNTER1	S4_ECC_ERR_COUNTER1	Go
0xA3	S4_CRC_COUNTER0	S4_CRC_COUNTER0	Go
0xA4	S4_CRC_COUNTER1	S4_CRC_COUNTER1	Go
0xA5	S4_HACTIVE_COUNTER0	S4_HACTIVE_COUNTER0	Go
0xA6	S4_HACTIVE_COUNTER1	S4_HACTIVE_COUNTER1	Go
0xA7	S4_VTOTAL_COUNTER0	S4_VTOTAL_COUNTER0	Go
0xA8	S4_VTOTAL_COUNTER1	S4_VTOTAL_COUNTER1	Go
0xA9	S4_STATUS	S4_STATUS	Go
0xB0	S5_COUNT_CONTROL	S5_COUNT_CONTROL	Go
0xB1	S5_ECC_ERR_COUNTER0	S5_ECC_ERR_COUNTER0	Go
0xB2	S5_ECC_ERR_COUNTER1	S5_ECC_ERR_COUNTER1	Go
0xB3	S5_CRC_COUNTER0	S5_CRC_COUNTER0	Go
0xB4	S5_CRC_COUNTER1	S5_CRC_COUNTER1	Go
0xB5	S5_HACTIVE_COUNTER0	S5_HACTIVE_COUNTER0	Go
0xB6	S5_HACTIVE_COUNTER1	S5_HACTIVE_COUNTER1	Go
0xB7	S5_VTOTAL_COUNTER0	S5_VTOTAL_COUNTER0	Go
0xB8	S5_VTOTAL_COUNTER1	S5_VTOTAL_COUNTER1	Go
0xB9	S5_STATUS	S5_STATUS	Go
0xC0	FPD3_COUNT_CTL	FPD3_COUNT_CTL	Go
0xC1	CHECKSUM_ERROR_COUNTER_0_FPD3	CHECKSUM_ERROR_COUNTER_0_FPD3	Go
0xC2	CHECKSUM_ERROR_COUNTER_1_FPD3	CHECKSUM_ERROR_COUNTER_1_FPD3	Go
0xC3	FPD3_HACTIVE_0	FPD3_HACTIVE_0	Go
0xC4	FPD3_HACTIVE_1	FPD3_HACTIVE_1	Go
0xC5	FPD3_VTOTAL_0	FPD3_VTOTAL_0	Go
0xC6	FPD3_VTOTAL_1	FPD3_VTOTAL_1	Go
0xC7	FPD3_STATUS	FPD3_STATUS	Go

Complex bit access types are encoded to fit into small table cells. Page 18: FPD RX Link Layer Access Type Codes shows the codes that are used for access types in this section.

Table 8-629. Page 18: FPD RX Link Layer Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RCP	R C P	Read to Clear Requires privileged access
Write Type		

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Table 8-629. Page 18: FPD RX Link Layer Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.15.1 COUNTER_CAPTURE Register (Address = 0x29) [Default = 0x00]

COUNTER_CAPTURE is shown in COUNTER_CAPTURE Register Field Descriptions.

Return to the Summary Table.

To capture the listed counter below, the capture bit should be set and a rising edge should be applied to 0x29[6]. If 0x29[6] is already 0, setting the capture bits and applying the rising edge can occur in the same transaction.

Table 8-630. COUNTER_CAPTURE Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	COUNTER_CHNG_EN	R/W	0x0	Counter Update Enable (Clear or Capture) 0: Captures and clears released 0->1: Captures and clears updated 1: Captures and clears released When this bit is toggled from 0 to 1, it will enable the counters to be either cleared or captured based on the corresponding bits set in registers 0x2A and 0x29. The capture or clear bits must be set before applying a rising edge to this bit. Only one capture or clear bit should be set at a time for the corresponding counter. If both capture and clear are set, the clear will override the capture. The clear bit must be set to 0 before a valid capture can be performed. Setting the clear or capture bits to 1 will not continuously clear or capture the counter, each action only occurs when this bit transitions from 0 to 1. Also used with clear and capture bits in registers 0x52, 0x60, 0x70, 0x80, 0x90, 0xA0, 0xB0, and 0xC0.
5	PACKET_CNT_CAPTURE	R/W	0x0	Capture Video Packet Counter Registers 0x36-0x37 A rising edge must be applied to 0x29[6] when this bit is set for the action to occur.
4	DATA_CRC_ERROR_CAPTURE	R/W	0x0	Capture CRC Error Counter for Data Frame Registers 0x34-0x35 A rising edge must be applied to 0x29[6] when this bit is set for the action to occur.
3	RESERVED	R/W	0x0	Reserved
2	CTL_ECC_ERROR_CAPTURE	R/W	0x0	Capture ECC Error Counter for Control Frame Registers 0x2B-0x2C A rising edge must be applied to 0x29[6] when this bit is set for the action to occur.
1	DATA_FRAME_CAPTURE	R/W	0x0	Capture Data Frame Counter Registers 0x31-0x33 A rising edge must be applied to 0x29[6] when this bit is set for the action to occur.
0	CTL_FRAME_CAPTURE	R/W	0x0	Capture Control Frame Counter Registers 0x2E-0x30 A rising edge must be applied to 0x29[6] when this bit is set for the action to occur.

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8.6.2.15.2 COUNTER_CLEAR Register (Address = 0x2A) [Default = 0x00]

COUNTER_CLEAR is shown in COUNTER_CLEAR Register Field Descriptions.

Return to the Summary Table.

To clear the listed counters below, their clear bit must first be set. Then, 0x29[6] must receive a rising edge.

Table 8-631. COUNTER_CLEAR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	PACKET_CNT_CLEAR	R/W	0x0	Clear Video Packet Counter Registers 0x36-0x37 After this bit is set, a rising edge must be applied to 0x29[6] for the action to occur.
4	DATA_CRC_ERROR_CLEAR	R/W	0x0	Clear CRC Error Counter for Data Frame Registers 0x34-0x35 After this bit is set, a rising edge must be applied to 0x29[6] for the action to occur.
3	RESERVED	R/W	0x0	Reserved
2	CTL_ECC_ERROR_CLEAR	R/W	0x0	Clear ECC Error Counter for Control Frame Registers 0x2B-0x2C After this bit is set, a rising edge must be applied to 0x29[6] for the action to occur.
1	DATA_FRAME_CLEAR	R/W	0x0	Clear Data Frame Counter Registers 0x31-0x33 After this bit is set, a rising edge must be applied to 0x29[6] for the action to occur.
0	CTL_FRAME_CLEAR	R/W	0x0	Clear Control Frame Counter Registers 0x2E-0x30 After this bit is set, a rising edge must be applied to 0x29[6] for the action to occur.

8.6.2.15.3 ECC_ERROR_COUNTER_0 Register (Address = 0x2B) [Default = 0x00]

ECC_ERROR_COUNTER_0 is shown in ECC_ERROR_COUNTER_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-632. ECC_ERROR_COUNTER_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_LSB	R	0x0	ECC Error counter[7:0] This counter can be cleared by setting 0x2A[2] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.4 ECC_ERROR_COUNTER_1 Register (Address = 0x2C) [Default = 0x00]

ECC_ERROR_COUNTER_1 is shown in ECC_ERROR_COUNTER_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-633. ECC_ERROR_COUNTER_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_MID	R	0x0	ECC Error counter[15:8] This counter can be cleared by setting 0x2A[2] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

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8.6.2.15.5 CTL_FRAME_COUNTER_0 Register (Address = 0x2E) [Default = 0x00]

CTL_FRAME_COUNTER_0 is shown in CTL_FRAME_COUNTER_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-634. CTL_FRAME_COUNTER_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CTL_FRAME_CNT_LSB	R	0x0	Control Frame Counter [7:0] This counter can be cleared by setting 0x2A[0] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.6 CTL_FRAME_COUNTER_1 Register (Address = 0x2F) [Default = 0x00]

CTL_FRAME_COUNTER_1 is shown in CTL_FRAME_COUNTER_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-635. CTL_FRAME_COUNTER_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CTL_FRAME_CNT_MID	R	0x0	Control Frame Counter [15:8] This counter can be cleared by setting 0x2A[0] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.7 CTL_FRAME_COUNTER_2 Register (Address = 0x30) [Default = 0x00]

CTL_FRAME_COUNTER_2 is shown in CTL_FRAME_COUNTER_2 Register Field Descriptions.

Return to the Summary Table.

Table 8-636. CTL_FRAME_COUNTER_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CTL_FRAME_CNT_MSB	R	0x0	Control Frame Counter [16:23] This counter can be cleared by setting 0x2A[0] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.8 DATA_FRAME_COUNTER_0 Register (Address = 0x31) [Default = 0x00]

DATA_FRAME_COUNTER_0 is shown in DATA_FRAME_COUNTER_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-637. DATA_FRAME_COUNTER_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DATA_FRAME_CNT_LSB	R	0x0	Data Frame Counter [7:0] This counter can be cleared by setting 0x2A[1] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.9 DATA_FRAME_COUNTER_1 Register (Address = 0x32) [Default = 0x00]

DATA_FRAME_COUNTER_1 is shown in DATA_FRAME_COUNTER_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-638. DATA_FRAME_COUNTER_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DATA_FRAME_CNT_MID	R	0x0	Data Frame Counter [15:8] This counter can be cleared by setting 0x2A[1] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.10 DATA_FRAME_COUNTER_2 Register (Address = 0x33) [Default = 0x00]

DATA_FRAME_COUNTER_2 is shown in DATA_FRAME_COUNTER_2 Register Field Descriptions.

Return to the Summary Table.

Table 8-639. DATA_FRAME_COUNTER_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DATA_FRAME_CNT_MSB	R	0x0	Data Frame Counter [16:23] This counter can be cleared by setting 0x2A[1] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.11 CRC_COUNTERS_0 Register (Address = 0x34) [Default = 0x00]

CRC_COUNTERS_0 is shown in CRC_COUNTERS_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-640. CRC_COUNTERS_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_LSB	R	0x0	CRC Error Counter for Data Frame [7:0] This counter can be cleared by setting 0x2A[4] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.12 CRC_COUNTERS_1 Register (Address = 0x35) [Default = 0x00]

CRC_COUNTERS_1 is shown in CRC_COUNTERS_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-641. CRC_COUNTERS_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_MSB	R	0x0	CRC Error Counter for Data Frame [15:8] This counter can be cleared by setting 0x2A[4] and then applying a rising edge to 0x29[6]. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.13 PACKET_CNT_COUNTER_0 Register (Address = 0x36) [Default = 0x00]

PACKET_CNT_COUNTER_0 is shown in PACKET_CNT_COUNTER_0 Register Field Descriptions.

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Table 8-642. PACKET_CNT_COUNTER_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PACKET_CNT_LSB	R	0x0	Packet Count [7:0] This counter increments with every vertical video line received from any of the streams. This captured value will only clear when PACKET_CNT_CLEAR is properly set. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.14 PACKET_CNT_COUNTER_1 Register (Address = 0x37) [Default = 0x00]

PACKET_CNT_COUNTER_1 is shown in PACKET_CNT_COUNTER_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-643. PACKET_CNT_COUNTER_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PACKET_CNT_MSB	R	0x0	Packet Count [15:8] This counter increments with every vertical video line received from any of the streams. This counter will only clear when PACKET_CNT_CLEAR is properly set. The counting mechanism will saturate and must be cleared to begin counting again.

8.6.2.15.15 S0_HACTIVE0 Register (Address = 0x39) [Default = 0x01]

S0_HACTIVE0 is shown in S0_HACTIVE0 Register Field Descriptions.

Return to the Summary Table.

Table 8-644. S0_HACTIVE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S0_HACTIVE_LSB	R	0x1	Stream 0 HACTIVE[7:0] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.16 S0_HACTIVE1 Register (Address = 0x3A) [Default = 0x00]

S0_HACTIVE1 is shown in S0_HACTIVE1 Register Field Descriptions.

Return to the Summary Table.

Table 8-645. S0_HACTIVE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S0_HACTIVE_MSB	R	0x0	Stream 0 HACTIVE[15:8] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.17 S1_HACTIVE0 Register (Address = 0x3B) [Default = 0x01]

S1_HACTIVE0 is shown in S1_HACTIVE0 Register Field Descriptions.

Return to the Summary Table.

Table 8-646. S1_HACTIVE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S1_HACTIVE_LSB	R	0x1	Stream 1 HACTIVE[7:0] This field updates with the latest HACTIVE count at the end of every transaction frame.

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8.6.2.15.18 S1_HACTIVE1 Register (Address = 0x3C) [Default = 0x00]

S1_HACTIVE1 is shown in S1_HACTIVE1 Register Field Descriptions.

Return to the Summary Table.

Table 8-647. S1_HACTIVE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S1_HACTIVE_MSB	R	0x0	Stream 1 HACTIVE[15:8] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.19 S2_HACTIVE0 Register (Address = 0x3D) [Default = 0x01]

S2_HACTIVE0 is shown in S2_HACTIVE0 Register Field Descriptions.

Return to the Summary Table.

Table 8-648. S2_HACTIVE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S2_HACTIVE_LSB	R	0x1	Stream 2 HACTIVE[7:0] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.20 S2_HACTIVE1 Register (Address = 0x3E) [Default = 0x00]

S2_HACTIVE1 is shown in S2_HACTIVE1 Register Field Descriptions.

Return to the Summary Table.

Table 8-649. S2_HACTIVE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S2_HACTIVE_MSB	R	0x0	Stream 2 HACTIVE[15:8] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.21 S3_HACTIVE0 Register (Address = 0x3F) [Default = 0x01]

S3_HACTIVE0 is shown in S3_HACTIVE0 Register Field Descriptions.

Return to the Summary Table.

Table 8-650. S3_HACTIVE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S3_HACTIVE_LSB	R	0x1	Stream 3 HACTIVE[7:0] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.22 S3_HACTIVE1 Register (Address = 0x40) [Default = 0x00]

S3_HACTIVE1 is shown in S3_HACTIVE1 Register Field Descriptions.

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Table 8-651. S3_HACTIVE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S3_HACTIVE_MSB	R	0x0	Stream 3 HACTIVE[15:8] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.23 S4_HACTIVE0 Register (Address = 0x41) [Default = 0x01]

S4_HACTIVE0 is shown in S4_HACTIVE0 Register Field Descriptions.

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Table 8-652. S4_HACTIVE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S4_HACTIVE_LSB	R	0x1	Stream 4 HACTIVE[7:0] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.24 S4_HACTIVE1 Register (Address = 0x42) [Default = 0x00]

S4_HACTIVE1 is shown in S4_HACTIVE1 Register Field Descriptions.

Return to the Summary Table.

Table 8-653. S4_HACTIVE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S4_HACTIVE_MSB	R	0x0	Stream 4 HACTIVE[15:8] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.25 S5_HACTIVE0 Register (Address = 0x43) [Default = 0x01]

S5_HACTIVE0 is shown in S5_HACTIVE0 Register Field Descriptions.

Return to the Summary Table.

Table 8-654. S5_HACTIVE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S5_HACTIVE_LSB	R	0x1	Stream 5 HACTIVE[7:0] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.26 S5_HACTIVE1 Register (Address = 0x44) [Default = 0x00]

S5_HACTIVE1 is shown in S5_HACTIVE1 Register Field Descriptions.

Return to the Summary Table.

Table 8-655. S5_HACTIVE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	S5_HACTIVE_MSB	R	0x0	Stream 5 HACTIVE[15:8] This field updates with the latest HACTIVE count at the end of every transaction frame.

8.6.2.15.27 VIDEO_PIXEL_SIZE0 Register (Address = 0x45) [Default = 0xFF]

VIDEO_PIXEL_SIZE0 is shown in VIDEO_PIXEL_SIZE0 Register Field Descriptions.

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Table 8-656. VIDEO_PIXEL_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	S3_VIDEO_PIXEL	R	0x3	Video Pixel Format for Stream 3 00: 18BPP 01: 24BPP 10: 30BPP 11: Reserved
5:4	S2_VIDEO_PIXEL	R	0x3	Video Pixel Format for Stream 2 00: 18BPP 01: 24BPP 10: 30BPP 11: Reserved
3:2	S1_VIDEO_PIXEL	R	0x3	Video Pixel Format for Stream 1 00: 18BPP 01: 24BPP 10: 30BPP 11: Reserved
1:0	S0_VIDEO_PIXEL	R	0x3	Video Pixel Format for Stream 0 00: 18BPP 01: 24BPP 10: 30BPP 11: Reserved

8.6.2.15.28 VIDEO_PIXEL_SIZE1 Register (Address = 0x46) [Default = 0x0F]

VIDEO_PIXEL_SIZE1 is shown in VIDEO_PIXEL_SIZE1 Register Field Descriptions.

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Table 8-657. VIDEO_PIXEL_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:2	S5_VIDEO_PIXEL	R	0x3	Video Pixel Format for Stream 5 00: 18BPP 01: 24BPP 10: 30BPP 11: Reserved
1:0	S4_VIDEO_PIXEL	R	0x3	Video Pixel Format for Stream 4 00: 18BPP 01: 24BPP 10: 30BPP 11: Reserved

8.6.2.15.29 DATA_FRAME_PASS_THRESHOLD_0 Register (Address = 0x47) [Default = 0x04]

DATA_FRAME_PASS_THRESHOLD_0 is shown in DATA_FRAME_PASS_THRESHOLD_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-658. DATA_FRAME_PASS_THRESHOLD_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DATA_FRAME_PASS_THRESH_LSB	R/W	0x4	Data Frame Counter Pass Threshold This threshold is in number of video frames. PASS/FAIL is reported in 0x53[1:0].

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8.6.2.15.30 DATA_FRAME_PASS_THRESHOLD_1 Register (Address = 0x48) [Default = 0x00]

DATA_FRAME_PASS_THRESHOLD_1 is shown in DATA_FRAME_PASS_THRESHOLD_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-659. DATA_FRAME_PASS_THRESHOLD_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DATA_FRAME_PASS_THRESH_MSB	R/W	0x0	Data Frame Counter Pass Threshold This threshold is in number of video frames. PASS/FAIL is reported in 0x53[1:0].

8.6.2.15.31 DATA_FRAME_FAIL_THRESHOLD_0 Register (Address = 0x49) [Default = 0x01]

DATA_FRAME_FAIL_THRESHOLD_0 is shown in DATA_FRAME_FAIL_THRESHOLD_0 Register Field Descriptions.

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Table 8-660. DATA_FRAME_FAIL_THRESHOLD_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DATA_FRAME_FAIL_THRESH_LSB	R/W	0x1	Data Frame Counter Fail Threshold This threshold is in number of video frames. PASS/FAIL is reported in 0x53[1:0].

8.6.2.15.32 DATA_FRAME_FAIL_THRESHOLD_1 Register (Address = 0x4A) [Default = 0x00]

DATA_FRAME_FAIL_THRESHOLD_1 is shown in DATA_FRAME_FAIL_THRESHOLD_1 Register Field Descriptions.

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Table 8-661. DATA_FRAME_FAIL_THRESHOLD_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	DATA_FRAME_FAIL_THRESH_MSB	R/W	0x0	Data Frame Counter Fail Threshold This threshold is in number of video frames. PASS/FAIL is reported in 0x53[1:0].

8.6.2.15.33 INTR_CTL_FPD4_RX Register (Address = 0x4D) [Default = 0xFF]

INTR_CTL_FPD4_RX is shown in INTR_CTL_FPD4_RX Register Field Descriptions.

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Table 8-662. INTR_CTL_FPD4_RX Register Field Descriptions

Bit	Field	Type	Default	Description
7	IE_ECC_ERR	R/W	0x1	FPD4 Main Link ECC Error Interrupt Enable 1: Interrupt enabled 0: Interrupt disabled
6	IE_CRC_ERR	R/W	0x1	FPD4 Main Link CRC Error Interrupt Enable 1: Interrupt enabled 0: Interrupt disabled
5	IE_HACTIVE_CHG	R/W	0x1	HACTIVE Length Change Interrupt Enable 1: Interrupt enabled 0: Interrupt disabled
4	IE_VTOTAL_CHG	R/W	0x1	VTOTAL Length Change Interrupt Enable 1: Interrupt enabled 0: Interrupt disabled

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Table 8-662. INTR_CTL_FPD4_RX Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	IE_LOCK1_CHG	R/W	0x1	FPD4 Main Link Port 1 LOCK Change Interrupt Enable 1: Interrupt enabled. Interrupt triggered when LOCK1 value changes. 0: Interrupt disabled
2	IE_LOCK0_CHG	R/W	0x1	FPD4 Main Link Port 0 LOCK Change Interrupt Enable 1: Interrupt enabled. Interrupt triggered when LOCK0 value changes. 0: Interrupt disabled
1	IE_LOCK1	R/W	0x1	FPD4 Main Link Port 1 LOCK Interrupt Enable 1: Interrupt enabled. Interrupt triggered when LOCK1 is true. 0: Interrupt disabled
0	IE_LOCK0	R/W	0x1	FPD4 Main Link Port 0 LOCK Interrupt Enable 1: Interrupt enabled. Interrupt triggered when LOCK0 is true. 0: Interrupt disabled

8.6.2.15.34 FPD4_RX_INT_STS Register (Address = 0x4E) [Default = 0x00]

FPD4_RX_INT_STS is shown in FPD4_RX_INT_STS Register Field Descriptions.

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Table 8-663. FPD4_RX_INT_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	STS_ECC_ERR	RCP	0x0	FPD4 Main Link ECC Error Interrupt Status This interrupt will trigger if an ECC error was detected. To read the number of detected ECC errors, set the capture bit 0x29[2] and apply a rising edge to 0x29[6], and read 0x2B-0x2C. To clear the interrupt source, set the clear bit 0x2A[2] and then apply a rising edge to 0x29[6]. This bit will re-trigger if the ECC counter registers have not been cleared.
6	STS_CRC_ERR	RCP	0x0	FPD4 Main Link CRC Error Interrupt Status This interrupt will trigger if a CRC error was detected. To read the number of detected CRC errors, set the capture bit 0x29[4] and apply a rising edge to 0x29[6], and read 0x34-0x35. To clear the interrupt source, set the clear bit 0x2A[4] and then apply a rising edge to 0x29[6]. This bit will re-trigger if the CRC counter registers have not been cleared.
5	STS_HACTIVE_CHG	RCP	0x0	HACTIVE Changed Global Interrupt Status This bit will be set when a change is detected between the HACTIVE reported for the current frame and the previous frame. Registers 0x39 - 0x44 will contain the current HACTIVE value for the corresponding stream. To clear this bit, apply a rising edge to 0x29[6], and read this register. The FPD3 HACTIVE counter which can be captured in registers 0xC3-0xC4 will also trigger this global interrupt.
4	STS_VTOTAL_CHG	RCP	0x0	VTOTAL Changed Global Interrupt Status This bit will be set when a change is detected between the VTOTAL reported for the current line and the previous line. To read the VTOTAL value for each stream use the capture bit (i.e. 0x60[2] for Stream 0) followed by a rising edge to 0x29[6], and then read the corresponding counter registers (i.e. 0x63-0x64 for Stream 0). To clear this bit, apply a rising edge to 0x29[6], and read this register. The FPD3 VTOTAL counter which can be captured in registers 0xC5-0xC6 will also trigger this global interrupt.
3	STS_LOCK1_CHG	RC	0x0	Port 1 Lock Status Changed Interrupt Status This bit will be set if LOCK is reacquired or if LOCK is lost. This bit is cleared on read.
2	STS_LOCK0_CHG	RC	0x0	Port 0 Lock Status Changed Interrupt Status This bit will be set if LOCK is reacquired or if LOCK is lost. This bit is cleared on read.

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Table 8-663. FPD4_RX_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	STS_LOCK1	RC	0x0	Port 1 Locked This bit will be set if Port 1 had a LOCK condition. This bit is cleared on read.
0	STS_LOCK0	RC	0x0	Port 0 Locked This bit will be set if Port 0 had a LOCK condition. This bit is cleared on read.

8.6.2.15.35 STS_FPD4_LOCK Register (Address = 0x50) [Default = 0x00]

STS_FPD4_LOCK is shown in STS_FPD4_LOCK Register Field Descriptions.

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Table 8-664. STS_FPD4_LOCK Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_FIRST_LOCK1	R	0x0	Port 1 LOCK Status This bit will remain 1 even if LOCK is lost. 0: No LOCK detected 1: LOCK is detected
0	STS_FIRST_LOCK0	R	0x0	Port 0 LOCK Status This bit will remain 1 even if LOCK is lost. 0: No LOCK detected 1: LOCK is detected

8.6.2.15.36 PASS_STATUS_CONFIG Register (Address = 0x51) [Default = 0x03]

PASS_STATUS_CONFIG is shown in PASS_STATUS_CONFIG Register Field Descriptions.

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Table 8-665. PASS_STATUS_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	ECC_ERR_EN	R/W	0x1	0: ECC errors do not enable the pass status failure 1: ECC errors enabled to trigger a pass status failure. Status can be found in register 0x53.
0	CRC_ERR_EN	R/W	0x1	0: CRC errors do not enable the pass status failure 1: CRC errors enabled to trigger a pass status failure. Status can be found in register 0x53.

8.6.2.15.37 PASS_STATUS_CONTROL Register (Address = 0x52) [Default = 0x00]

PASS_STATUS_CONTROL is shown in PASS_STATUS_CONTROL Register Field Descriptions.

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Register 0x29[6] must be have a rising edge for these counters to capture a value (Bits 7:4).

Table 8-666. PASS_STATUS_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	DP1_ERROR_FREE_CAPTURE	R/W	0x0	Capture DP Port 1 Error-free Video Frame Counter Registers 0x54-0x55
6	DP1_ERRORED_CAPTURE	R/W	0x0	Capture DP Port 1 Errored Video Frame Counter Registers 0x56-0x57

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Table 8-666. PASS_STATUS_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	DP0_ERROR_FREE_CAPTURE	R/W	0x0	Capture DP Port 0 Error-free Video Frame Counter Registers 0x58-0x59
4	DP0_ERRORED_CAPTURE	R/W	0x0	Capture DP Port 0 Errored Video Frame Counter Registers 0x5A-0x5B
3	DP1_ERROR_FREE_CLEAR	R/W	0x0	Clear DP Port 1 Error-free Video Frame Counter Registers 0x54-0x55
2	DP1_ERRORED_CLEAR	R/W	0x0	Clear DP Port 1 Errored Video Frame Counter Registers 0x56-0x57
1	DP0_ERROR_FREE_CLEAR	R/W	0x0	Clear DP Port 0 Error-free Video Frame Counter Registers 0x58-0x59
0	DP0_ERRORED_CLEAR	R/W	0x0	Clear DP Port 0 Errored Video Frame Counter Registers 0x5A-0x5B

8.6.2.15.38 STS_PASS Register (Address = 0x53) [Default = 0x00]

STS_PASS is shown in STS_PASS Register Field Descriptions.

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Reference registers 0x47-0x4A for the thresholds.

Table 8-667. STS_PASS Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	STS_PASS1	R	0x0	Pass Status of FPD-Link RX Sent to Display Port 1 Based on error-free frames received 0: FAIL. Error-free frames < pass threshold or errored frames >= fail threshold 1: PASS. Error free frames >= threshold and errored frames < fail threshold FPD encoding errors will also drive the pass status low.
0	STS_PASS0	R	0x0	Pass Status of FPD-Link RX Sent to Display Port 0 Based on error-free frames received 0: FAIL. Error-free frames < pass threshold or errored frames >= fail threshold 1: PASS. Error free frames >= threshold and errored frames < fail threshold FPD encoding errors will also drive the pass status low.

8.6.2.15.39 VID_FRAME_CNT_P1_LSB Register (Address = 0x54) [Default = 0x00]

VID_FRAME_CNT_P1_LSB is shown in VID_FRAME_CNT_P1_LSB Register Field Descriptions.

Return to the Summary Table.

Table 8-668. VID_FRAME_CNT_P1_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_FRAME_CNT_P1_LSB	R	0x0	Display Port 1 Error-Free Video Frame Counter

8.6.2.15.40 VID_FRAME_CNT_P1_MSB Register (Address = 0x55) [Default = 0x00]

VID_FRAME_CNT_P1_MSB is shown in VID_FRAME_CNT_P1_MSB Register Field Descriptions.

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Table 8-669. VID_FRAME_CNT_P1_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_FRAME_CNT_P1_MSB	R	0x0	Display Port 1 Error-Free Video Frame Counter

8.6.2.15.41 VID_ERR_CNT_P1_LSB Register (Address = 0x56) [Default = 0x00]

VID_ERR_CNT_P1_LSB is shown in VID_ERR_CNT_P1_LSB Register Field Descriptions.

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Table 8-670. VID_ERR_CNT_P1_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_ERR_CNT_P1_LSB	R	0x0	Display Port 1 Errored Video Frame Counter

8.6.2.15.42 VID_ERR_CNT_P1_MSB Register (Address = 0x57) [Default = 0x00]

VID_ERR_CNT_P1_MSB is shown in VID_ERR_CNT_P1_MSB Register Field Descriptions.

Return to the Summary Table.

Table 8-671. VID_ERR_CNT_P1_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_ERR_CNT_P1_MSB	R	0x0	Display Port 1 Errored Video Frame Counter

8.6.2.15.43 VID_FRAME_CNT_P0_LSB Register (Address = 0x58) [Default = 0x00]

VID_FRAME_CNT_P0_LSB is shown in VID_FRAME_CNT_P0_LSB Register Field Descriptions.

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Table 8-672. VID_FRAME_CNT_P0_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_FRAME_CNT_P0_LSB	R	0x0	Display Port 0 Error-Free Video Frame Counter

8.6.2.15.44 VID_FRAME_CNT_P0_MSB Register (Address = 0x59) [Default = 0x00]

VID_FRAME_CNT_P0_MSB is shown in VID_FRAME_CNT_P0_MSB Register Field Descriptions.

Return to the Summary Table.

Table 8-673. VID_FRAME_CNT_P0_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_FRAME_CNT_P0_MSB	R	0x0	Display Port 0 Error-Free Video Frame Counter

8.6.2.15.45 VID_ERR_CNT_P0_LSB Register (Address = 0x5A) [Default = 0x00]

VID_ERR_CNT_P0_LSB is shown in VID_ERR_CNT_P0_LSB Register Field Descriptions.

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Table 8-674. VID_ERR_CNT_P0_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_ERR_CNT_P0_LSB	R	0x0	Display Port 0 Errored Video Frame Counter

8.6.2.15.46 VID_ERR_CNT_P0_MSB Register (Address = 0x5B) [Default = 0x00]

VID_ERR_CNT_P0_MSB is shown in VID_ERR_CNT_P0_MSB Register Field Descriptions.

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Table 8-675. VID_ERR_CNT_P0_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VID_ERR_CNT_P0_MSB	R	0x0	Display Port 0 Errored Video Frame Counter

8.6.2.15.47 STREAM_0_COUNT_CONTROL Register (Address = 0x60) [Default = 0x00]

STREAM_0_COUNT_CONTROL is shown in STREAM_0_COUNT_CONTROL Register Field Descriptions.

Return to the Summary Table.

Register 0x29[6] must have a rising edge to either capture or clear the listed counters.

Table 8-676. STREAM_0_COUNT_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	S0_HACTIVE_CAPTURE	R/W	0x0	Capture Stream 0 HACTIVE Counter Registers 0x65-0x66 reserved because capturing hactive counter provides not value to customer. It will mirror 0x39-0x44
6	S0_VTOTAL_CAPTURE	R/W	0x0	Capture Stream 0 VTOTAL Counter Registers 0x67-0x68
5	S0_CRC_ERROR_CAPTURE	R/W	0x0	Capture Stream 0 CRC Error Counter for Data Frame Register 0x63-0x64
4	S0_ECC_ERROR_CAPTURE	R/W	0x0	Capture Stream 0 ECC Error Counter for Control Frame Registers 0x61-62
3	S0_HACTIVE_CLEAR	R/W	0x0	Clear Stream 0 HACTIVE Counter Registers 0x65-0x66
2	S0_VTOTAL_CLEAR	R/W	0x0	Clear Stream 0 VTOTAL Counter Registers 0x67-0x68
1	S0_CRC_ERROR_CLEAR	R/W	0x0	Clear Stream 0 CRC Error Counter for Data Frame Register 0x63-0x64
0	S0_ECC_ERROR_CLEAR	R/W	0x0	Clear Stream 0 ECC Error Counter for Control Frame Registers 0x61-62

8.6.2.15.48 S0_ECC_ERR_COUNTER0 Register (Address = 0x61) [Default = 0x00]

S0_ECC_ERR_COUNTER0 is shown in S0_ECC_ERR_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-677. S0_ECC_ERR_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S0_LSB	R	0x0	Stream 0 ECC Error Counter [7:0]

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8.6.2.15.49 S0_ECC_ERR_COUNTER1 Register (Address = 0x62) [Default = 0x00]

S0_ECC_ERR_COUNTER1 is shown in S0_ECC_ERR_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-678. S0_ECC_ERR_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S0_MSB	R	0x0	Stream 0 ECC Error Counter [8:15]

8.6.2.15.50 S0_CRC_COUNTER0 Register (Address = 0x63) [Default = 0x00]

S0_CRC_COUNTER0 is shown in S0_CRC_COUNTER0 Register Field Descriptions.

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Table 8-679. S0_CRC_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S0_LSB	R	0x0	Stream 0 CRC Error Counter [7:0]

8.6.2.15.51 S0_CRC_COUNTER1 Register (Address = 0x64) [Default = 0x00]

S0_CRC_COUNTER1 is shown in S0_CRC_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-680. S0_CRC_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S0_MSB	R	0x0	Stream 0 CRC Error Counter [8:15]

8.6.2.15.52 S0_HACTIVE_COUNTER0 Register (Address = 0x65) [Default = 0x00]

S0_HACTIVE_COUNTER0 is shown in S0_HACTIVE_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-681. S0_HACTIVE_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_CNT_S0_LSB	R	0x0	Stream 0 HACTIVE Counter [7:0]

8.6.2.15.53 S0_HACTIVE_COUNTER1 Register (Address = 0x66) [Default = 0x00]

S0_HACTIVE_COUNTER1 is shown in S0_HACTIVE_COUNTER1 Register Field Descriptions.

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Table 8-682. S0_HACTIVE_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_CNT_S0_MSB	R	0x0	Stream 0 HACTIVE Counter [8:15]

8.6.2.15.54 S0_VTOTAL_COUNTER0 Register (Address = 0x67) [Default = 0x00]

S0_VTOTAL_COUNTER0 is shown in S0_VTOTAL_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-683. S0_VTOTAL_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_CNT_S0_LSB	R	0x0	Stream 0 VTOTAL Counter [7:0]

8.6.2.15.55 S0_VTOTAL_COUNTER1 Register (Address = 0x68) [Default = 0x00]

S0_VTOTAL_COUNTER1 is shown in S0_VTOTAL_COUNTER1 Register Field Descriptions.

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Table 8-684. S0_VTOTAL_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_CNT_S0_MSB	R	0x0	Stream 0 VTOTAL Counter [8:15]

8.6.2.15.56 S0_STATUS Register (Address = 0x69) [Default = 0x00]

S0_STATUS is shown in S0_STATUS Register Field Descriptions.

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Table 8-685. S0_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	STS_ECC_ERR_S0	RCP	0x0	FPD4 Received Stream 0 Control Frame ECC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S0_ECC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
2	STS_CRC_ERR_S0	RCP	0x0	FPD4 Received Stream 0 Data Frame CRC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S0_CRC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
1	STS_HACTIVE_CHG_S0	RCP	0x0	Stream 0 HACTIVE Changed This bit will trigger when the current HACTIVE value for Stream 0 in registers 0x39-0x3A is different from the previous value. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. This flag is also set when this stream receives its first video frame.
0	VTOTAL_CHG_S0	RCP	0x0	Stream 0 VTOTAL Changed This bit will trigger when the current VTOTAL value is different from the previous VTOTAL value. To read the current VTOTAL value, apply a rising edge on 0x29[6] after setting S0_VTOTAL_CAPTURE in 0x60, then read the VTOTAL registers in 0x67-0x68. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)

8.6.2.15.57 S1_COUNT_CONTROL Register (Address = 0x70) [Default = 0x00]

S1_COUNT_CONTROL is shown in S1_COUNT_CONTROL Register Field Descriptions.

Return to the Summary Table.

Register 0x29[6] must have a rising edge to either capture or clear the listed counters.

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Table 8-686. S1_COUNT_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	S1_HACTIVE_CAPTURE	R/W	0x0	Capture Stream 1 HACTIVE Counter Registers 0x75-0x76
6	S1_VTOTAL_CAPTURE	R/W	0x0	Capture Stream 1 VTOTAL Counter Registers 0x77-0x78
5	S1_CRC_ERROR_CAPTURE	R/W	0x0	Capture Stream 1 CRC Error Counter for Data Frame Register 0x73-0x74
4	S1_ECC_ERROR_CAPTURE	R/W	0x0	Capture Stream 1 ECC Error Counter for Control Frame Registers 0x71-0x72
3	S1_HACTIVE_CLEAR	R/W	0x0	Clear Stream 1 HACTIVE Counter Registers 0x75-0x76
2	S1_VTOTAL_CLEAR	R/W	0x0	Clear Stream 1 VTOTAL Counter Registers 0x77-0x78
1	S1_CRC_ERROR_CLEAR	R/W	0x0	Clear Stream 1 CRC Error Counter for Data Frame Register 0x73-0x74
0	S1_ECC_ERROR_CLEAR	R/W	0x0	Clear Stream 1 ECC Error Counter for Control Frame Registers 0x71-0x72

8.6.2.15.58 S1_ECC_ERR_COUNTER0 Register (Address = 0x71) [Default = 0x00]

S1_ECC_ERR_COUNTER0 is shown in S1_ECC_ERR_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-687. S1_ECC_ERR_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S1_LSB	R	0x0	Stream 1 ECC Error counter [7:0]

8.6.2.15.59 S1_ECC_ERR_COUNTER1 Register (Address = 0x72) [Default = 0x00]

S1_ECC_ERR_COUNTER1 is shown in S1_ECC_ERR_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-688. S1_ECC_ERR_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S1_MSB	R	0x0	Stream 1 ECC Error counter [15:8]

8.6.2.15.60 S1_CRC_COUNTER0 Register (Address = 0x73) [Default = 0x00]

S1_CRC_COUNTER0 is shown in S1_CRC_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-689. S1_CRC_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S1_LSB	R	0x0	Stream 1 CRC error counter [7:0]

8.6.2.15.61 S1_CRC_COUNTER1 Register (Address = 0x74) [Default = 0x00]

S1_CRC_COUNTER1 is shown in S1_CRC_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-690. S1_CRC_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S1_MSB	R	0x0	Stream 1 CRC error counter [15:8]

8.6.2.15.62 S1_HACTIVE_COUNTER0 Register (Address = 0x75) [Default = 0x00]

S1_HACTIVE_COUNTER0 is shown in S1_HACTIVE_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-691. S1_HACTIVE_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S1_LSB	R	0x0	Stream 1 HACTIVE Counter [7:0]

8.6.2.15.63 S1_HACTIVE_COUNTER1 Register (Address = 0x76) [Default = 0x00]

S1_HACTIVE_COUNTER1 is shown in S1_HACTIVE_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-692. S1_HACTIVE_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S1_MSB	R	0x0	Stream 1 HACTIVE Counter [8:15]

8.6.2.15.64 S1_VTOTAL_COUNTER0 Register (Address = 0x77) [Default = 0x00]

S1_VTOTAL_COUNTER0 is shown in S1_VTOTAL_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-693. S1_VTOTAL_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S1_LSB	R	0x0	Stream 1 VTOTAL Counter [7:0]

8.6.2.15.65 S1_VTOTAL_COUNTER1 Register (Address = 0x78) [Default = 0x00]

S1_VTOTAL_COUNTER1 is shown in S1_VTOTAL_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-694. S1_VTOTAL_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S1_MSB	R	0x0	Stream 1 VTOTAL Counter [8:15]

8.6.2.15.66 S1_STATUS Register (Address = 0x79) [Default = 0x00]

S1_STATUS is shown in S1_STATUS Register Field Descriptions.

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Table 8-695. S1_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

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Table 8-695. S1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	STS_ECC_ERR_S1	RCP	0x0	FPD4 Received Stream 1 Control Frame ECC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S1_ECC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
2	STS_CRC_ERR_S1	RCP	0x0	FPD4 Received Stream 1 Data Frame CRC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S1_CRC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
1	STS_HACTIVE_CHG_S1	RCP	0x0	Stream 1 HACTIVE Changed This bit will trigger when the current HACTIVE value for Stream 1 in registers 0x3B-0x3C is different from the previous value. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. This flag is also set when this stream receives its first video frame.
0	VTOTAL_CHG_S1	RCP	0x0	Stream 1 VTOTAL Changed This bit will trigger when the current VTOTAL value is different from the previous VTOTAL value. To read the current VTOTAL value, apply a rising edge on 0x29[6] after setting S1_VTOTAL_CAPTURE in 0x70, then read the VTOTAL registers in 0x77-0x78. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)

8.6.2.15.67 S2_COUNT_CONTROL Register (Address = 0x80) [Default = 0x00]

S2_COUNT_CONTROL is shown in S2_COUNT_CONTROL Register Field Descriptions.

Return to the Summary Table.

Register 0x29[6] must have a rising edge to either capture or clear the listed counters.

Table 8-696. S2_COUNT_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	S2_HACTIVE_CAPTURE	R/W	0x0	Capture Stream 2 HACTIVE Counter Registers 0x85-0x86
6	S2_VTOTAL_CAPTURE	R/W	0x0	Capture Stream 2 VTOTAL Counter Registers 0x87-0x88
5	S2_CRC_ERROR_CAPTURE	R/W	0x0	Capture Stream 2 CRC Error Counter for Data Frame Register 0x83-0x84
4	S2_ECC_ERROR_CAPTURE	R/W	0x0	Capture Stream 2 ECC Error Counter for Control Frame Registers 0x81-0x82
3	S2_HACTIVE_CLEAR	R/W	0x0	Clear Stream 2 HACTIVE Counter Registers 0x85-0x86
2	S2_VTOTAL_CLEAR	R/W	0x0	Clear Stream 2 VTOTAL Counter Registers 0x87-0x88
1	S2_CRC_ERROR_CLEAR	R/W	0x0	Clear Stream 2 CRC Error Counter for Data Frame Register 0x83-0x84
0	S2_ECC_ERROR_CLEAR	R/W	0x0	Clear Stream 2 ECC Error Counter for Control Frame Registers 0x81-0x82

8.6.2.15.68 S2_ECC_ERR_COUNTER0 Register (Address = 0x81) [Default = 0x00]

S2_ECC_ERR_COUNTER0 is shown in S2_ECC_ERR_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-697. S2_ECC_ERR_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S2_LSB	R	0x0	Stream 2 ECC Error counter [7:0]

8.6.2.15.69 S2_ECC_ERR_COUNTER1 Register (Address = 0x82) [Default = 0x00]

S2_ECC_ERR_COUNTER1 is shown in S2_ECC_ERR_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-698. S2_ECC_ERR_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S2_MSB	R	0x0	Stream 2 ECC Error counter [15:8]

8.6.2.15.70 S2_CRC_COUNTER0 Register (Address = 0x83) [Default = 0x00]

S2_CRC_COUNTER0 is shown in S2_CRC_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-699. S2_CRC_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S2_LSB	R	0x0	Stream 2 CRC error counter [7:0]

8.6.2.15.71 S2_CRC_COUNTER1 Register (Address = 0x84) [Default = 0x00]

S2_CRC_COUNTER1 is shown in S2_CRC_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-700. S2_CRC_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S2_MSB	R	0x0	Stream 2 CRC error counter [15:8]

8.6.2.15.72 S2_HACTIVE_COUNTER0 Register (Address = 0x85) [Default = 0x00]

S2_HACTIVE_COUNTER0 is shown in S2_HACTIVE_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-701. S2_HACTIVE_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S2_LSB	R	0x0	Stream 2 HACTIVE Counter [7:0]

8.6.2.15.73 S2_HACTIVE_COUNTER1 Register (Address = 0x86) [Default = 0x00]

S2_HACTIVE_COUNTER1 is shown in S2_HACTIVE_COUNTER1 Register Field Descriptions.

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Table 8-702. S2_HACTIVE_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S2_MSB	R	0x0	Stream 2 HACTIVE Counter [8:15]

8.6.2.15.74 S2_VTOTAL_COUNTER0 Register (Address = 0x87) [Default = 0x00]

S2_VTOTAL_COUNTER0 is shown in S2_VTOTAL_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-703. S2_VTOTAL_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S2_LSB	R	0x0	Stream 2 VTOTAL Counter [7:0]

8.6.2.15.75 S2_VTOTAL_COUNTER1 Register (Address = 0x88) [Default = 0x00]

S2_VTOTAL_COUNTER1 is shown in S2_VTOTAL_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-704. S2_VTOTAL_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S2_MSB	R	0x0	Stream 2 VTOTAL Counter [8:15]

8.6.2.15.76 S2_STATUS Register (Address = 0x89) [Default = 0x00]

S2_STATUS is shown in S2_STATUS Register Field Descriptions.

Return to the Summary Table.

Table 8-705. S2_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	STS_ECC_ERR_S2	RCP	0x0	FPD4 Received Stream 2 Control Frame ECC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S2_ECC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
2	STS_CRC_ERR_S2	RCP	0x0	FPD4 Received Stream 2 Data Frame CRC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S2_CRC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
1	STS_HACTIVE_CHG_S2	RCP	0x0	Stream 2 HACTIVE Changed This bit will trigger when the current HACTIVE value for Stream 2 in registers 0x3D-0x3E is different from the previous value. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. This flag is also set when this stream receives its first video frame.
0	VTOTAL_CHG_S2	RCP	0x0	Stream 2 VTOTAL Changed This bit will trigger when the current VTOTAL value is different from the previous VTOTAL value. To read the current VTOTAL value, apply a rising edge on 0x29[6] after setting S2_VTOTAL_CAPTURE in 0x80, then read the VTOTAL registers in 0x87-0x88. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)

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8.6.2.15.77 S3_COUNT_CONTROL Register (Address = 0x90) [Default = 0x00]

S3_COUNT_CONTROL is shown in S3_COUNT_CONTROL Register Field Descriptions.

Return to the Summary Table.

Register 0x29[6] must have a rising edge to either capture or clear the listed counters.

Table 8-706. S3_COUNT_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	S3_HACTIVE_CAPTURE	R/W	0x0	Capture Stream 3 HACTIVE Counter Registers 0x95-0x96
6	S3_VTOTAL_CAPTURE	R/W	0x0	Capture Stream 3 VTOTAL Counter Registers 0x97-0x98
5	S3_CRC_ERROR_CAPTURE	R/W	0x0	Capture Stream 3 CRC Error Counter for Data Frame Register 0x93-0x94
4	S3_ECC_ERROR_CAPTURE	R/W	0x0	Capture Stream 3 ECC Error Counter for Control Frame Registers 0x91-0x92
3	S3_HACTIVE_CLEAR	R/W	0x0	Clear Stream 3 HACTIVE Counter Registers 0x95-0x96
2	S3_VTOTAL_CLEAR	R/W	0x0	Clear Stream 3 VTOTAL Counter Registers 0x97-0x98
1	S3_CRC_ERROR_CLEAR	R/W	0x0	Clear Stream 3 CRC Error Counter for Data Frame Register 0x93-0x94
0	S3_ECC_ERROR_CLEAR	R/W	0x0	Clear Stream 3 ECC Error Counter for Control Frame Registers 0x91-0x92

8.6.2.15.78 S3_ECC_ERR_COUNTER0 Register (Address = 0x91) [Default = 0x00]

S3_ECC_ERR_COUNTER0 is shown in S3_ECC_ERR_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-707. S3_ECC_ERR_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S3_LSB	R	0x0	Stream 3 ECC Error counter [7:0]

8.6.2.15.79 S3_ECC_ERR_COUNTER1 Register (Address = 0x92) [Default = 0x00]

S3_ECC_ERR_COUNTER1 is shown in S3_ECC_ERR_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-708. S3_ECC_ERR_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S3_MSB	R	0x0	Stream 3 ECC Error counter [15:8]

8.6.2.15.80 S3_CRC_COUNTER0 Register (Address = 0x93) [Default = 0x00]

S3_CRC_COUNTER0 is shown in S3_CRC_COUNTER0 Register Field Descriptions.

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Table 8-709. S3_CRC_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S3_LSB	R	0x0	Stream 3 CRC error counter [7:0]

8.6.2.15.81 S3_CRC_COUNTER1 Register (Address = 0x94) [Default = 0x00]

S3_CRC_COUNTER1 is shown in S3_CRC_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-710. S3_CRC_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S3_MSB	R	0x0	Stream 3 CRC error counter [15:8]

8.6.2.15.82 S3_HACTIVE_COUNTER0 Register (Address = 0x95) [Default = 0x00]

S3_HACTIVE_COUNTER0 is shown in S3_HACTIVE_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-711. S3_HACTIVE_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S3_LSB	R	0x0	Stream 3 HACTIVE Counter [7:0]

8.6.2.15.83 S3_HACTIVE_COUNTER1 Register (Address = 0x96) [Default = 0x00]

S3_HACTIVE_COUNTER1 is shown in S3_HACTIVE_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-712. S3_HACTIVE_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S3_MSB	R	0x0	Stream 3 HACTIVE Counter [8:15]

8.6.2.15.84 S3_VTOTAL_COUNTER0 Register (Address = 0x97) [Default = 0x00]

S3_VTOTAL_COUNTER0 is shown in S3_VTOTAL_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-713. S3_VTOTAL_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S3_LSB	R	0x0	Stream 3 VTOTAL Counter [7:0]

8.6.2.15.85 S3_VTOTAL_COUNTER1 Register (Address = 0x98) [Default = 0x00]

S3_VTOTAL_COUNTER1 is shown in S3_VTOTAL_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-714. S3_VTOTAL_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S3_MSB	R	0x0	Stream 3 VTOTAL Counter [8:15]

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8.6.2.15.86 S3_STATUS Register (Address = 0x99) [Default = 0x00]

S3_STATUS is shown in S3_STATUS Register Field Descriptions.

Return to the Summary Table.

Table 8-715. S3_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	STS_ECC_ERR_S3	RCP	0x0	FPD4 Received Stream 3 Control Frame ECC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S3_ECC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
2	STS_CRC_ERR_S3	RCP	0x0	FPD4 Received Stream 3 Data Frame CRC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S3_CRC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
1	STS_HACTIVE_CHG_S3	RCP	0x0	Stream 3 HACTIVE Changed This bit will trigger when the current HACTIVE value for Stream 3 in registers 0x3F-0x40 is different from the previous value. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. This flag is also set when this stream receives its first video frame.
0	VTOTAL_CHG_S3	RCP	0x0	Stream 3 VTOTAL Changed This bit will trigger when the current VTOTAL value is different from the previous VTOTAL value. To read the current VTOTAL value, apply a rising edge on 0x29[6] after setting S3_VTOTAL_CAPTURE in 0x90, then read the VTOTAL registers in 0x97-0x98. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)

8.6.2.15.87 S4_COUNT_CONTROL Register (Address = 0xA0) [Default = 0x00]

S4_COUNT_CONTROL is shown in S4_COUNT_CONTROL Register Field Descriptions.

Return to the Summary Table.

Register 0x29[6] must have a rising edge to either capture or clear the listed counters.

Table 8-716. S4_COUNT_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	S4_HACTIVE_CAPTURE	R/W	0x0	Capture Stream 4 HACTIVE Counter Registers 0xA5-0xA6
6	S4_VTOTAL_CAPTURE	R/W	0x0	Capture Stream 4 VTOTAL Counter Registers 0xA7-0xA8
5	S4_CRC_ERROR_CAPTURE	R/W	0x0	Capture Stream 4 CRC Error Counter for Data Frame Register 0xA3-0xA4
4	S4_ECC_ERROR_CAPTURE	R/W	0x0	Capture Stream 4 ECC Error Counter for Control Frame Registers 0xA1-0xA2
3	S4_HACTIVE_CLEAR	R/W	0x0	Clear Stream 4 HACTIVE Counter Registers 0xA5-0xA6
2	S4_VTOTAL_CLEAR	R/W	0x0	Clear Stream 4 VTOTAL Counter Registers 0xA7-0xA8
1	S4_CRC_ERROR_CLEAR	R/W	0x0	Clear Stream 4 CRC Error Counter for Data Frame Register 0xA3-0xA4
0	S4_ECC_ERROR_CLEAR	R/W	0x0	Clear Stream 4 ECC Error Counter for Control Frame Registers 0xA1-0xA2

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8.6.2.15.88 S4_ECC_ERR_COUNTER0 Register (Address = 0xA1) [Default = 0x00]

S4_ECC_ERR_COUNTER0 is shown in S4_ECC_ERR_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-717. S4_ECC_ERR_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S4_LSB	R	0x0	Stream 4 ECC Error counter [7:0]

8.6.2.15.89 S4_ECC_ERR_COUNTER1 Register (Address = 0xA2) [Default = 0x00]

S4_ECC_ERR_COUNTER1 is shown in S4_ECC_ERR_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-718. S4_ECC_ERR_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S4_MSB	R	0x0	Stream 4 ECC Error counter [15:8]

8.6.2.15.90 S4_CRC_COUNTER0 Register (Address = 0xA3) [Default = 0x00]

S4_CRC_COUNTER0 is shown in S4_CRC_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-719. S4_CRC_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S4_LSB	R	0x0	Stream 4 CRC error counter [7:0]

8.6.2.15.91 S4_CRC_COUNTER1 Register (Address = 0xA4) [Default = 0x00]

S4_CRC_COUNTER1 is shown in S4_CRC_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-720. S4_CRC_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S4_MSB	R	0x0	Stream 4 CRC error counter [15:8]

8.6.2.15.92 S4_HACTIVE_COUNTER0 Register (Address = 0xA5) [Default = 0x00]

S4_HACTIVE_COUNTER0 is shown in S4_HACTIVE_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-721. S4_HACTIVE_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S4_LSB	R	0x0	Stream 4 HACTIVE Counter [7:0]

8.6.2.15.93 S4_HACTIVE_COUNTER1 Register (Address = 0xA6) [Default = 0x00]

S4_HACTIVE_COUNTER1 is shown in S4_HACTIVE_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-722. S4_HACTIVE_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S4_MSB	R	0x0	Stream 4 HACTIVE Counter [8:15]

8.6.2.15.94 S4_VTOTAL_COUNTER0 Register (Address = 0xA7) [Default = 0x00]

S4_VTOTAL_COUNTER0 is shown in S4_VTOTAL_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-723. S4_VTOTAL_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S4_LSB	R	0x0	Stream 4 VTOTAL Counter [7:0]

8.6.2.15.95 S4_VTOTAL_COUNTER1 Register (Address = 0xA8) [Default = 0x00]

S4_VTOTAL_COUNTER1 is shown in S4_VTOTAL_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-724. S4_VTOTAL_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S4_MSB	R	0x0	Stream 4 VTOTAL Counter [8:15]

8.6.2.15.96 S4_STATUS Register (Address = 0xA9) [Default = 0x00]

S4_STATUS is shown in S4_STATUS Register Field Descriptions.

Return to the Summary Table.

Table 8-725. S4_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	STS_ECC_ERR_S4	RCP	0x0	FPD4 Received Stream 4 Control Frame ECC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S4_ECC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
2	STS_CRC_ERR_S4	RCP	0x0	FPD4 Received Stream 4 Data Frame CRC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S4_CRC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
1	STS_HACTIVE_CHG_S4	RCP	0x0	Stream 4 HACTIVE Changed This bit will trigger when the current HACTIVE value for Stream 4 in registers 0x41-0x42 is different from the previous value. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. This flag is also set when this stream receives its first video frame.

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Table 8-725. S4_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	VTOTAL_CHG_S4	RCP	0x0	Stream 4 VTOTAL Changed This bit will trigger when the current VTOTAL value is different from the previous VTOTAL value. To read the current VTOTAL value, apply a rising edge on 0x29[6] after setting S4_VTOTAL_CAPTURE in 0xA0, then read the VTOTAL registers in 0xA7-0xA8. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)

8.6.2.15.97 S5_COUNT_CONTROL Register (Address = 0xB0) [Default = 0x00]

S5_COUNT_CONTROL is shown in S5_COUNT_CONTROL Register Field Descriptions.

Return to the Summary Table.

Register 0x29[6] must have a rising edge to either capture or clear the listed counters.

Table 8-726. S5_COUNT_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	S5_HACTIVE_CAPTURE	R/W	0x0	Capture Stream 5 HACTIVE Counter Registers 0xB5-0xB6
6	S5_VTOTAL_CAPTURE	R/W	0x0	Capture Stream 5 VTOTAL Counter Registers 0xB7-0xB8
5	S5_CRC_ERROR_CAPTURE	R/W	0x0	Capture Stream 5 CRC Error Counter for Data Frame Register 0xB3-0xB4
4	S5_ECC_ERROR_CAPTURE	R/W	0x0	Capture Stream 5 ECC Error Counter for Control Frame Registers 0xB1-0xB2
3	S5_HACTIVE_CLEAR	R/W	0x0	Clear Stream 5 HACTIVE Counter Registers 0xB5-0xB6
2	S5_VTOTAL_CLEAR	R/W	0x0	Clear Stream 5 VTOTAL Counter Registers 0xB7-0xB8
1	S5_CRC_ERROR_CLEAR	R/W	0x0	Clear Stream 5 CRC Error Counter for Data Frame Register 0xB3-0xB4
0	S5_ECC_ERROR_CLEAR	R/W	0x0	Clear Stream 5 ECC Error Counter for Control Frame Registers 0xB1-0xB2

8.6.2.15.98 S5_ECC_ERR_COUNTER0 Register (Address = 0xB1) [Default = 0x00]

S5_ECC_ERR_COUNTER0 is shown in S5_ECC_ERR_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-727. S5_ECC_ERR_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S5_LSB	R	0x0	Stream 5 ECC Error counter [7:0]

8.6.2.15.99 S5_ECC_ERR_COUNTER1 Register (Address = 0xB2) [Default = 0x00]

S5_ECC_ERR_COUNTER1 is shown in S5_ECC_ERR_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-728. S5_ECC_ERR_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ECC_ERROR_CNT_S5_MSB	R	0x0	Stream 5 ECC Error counter [15:8]

8.6.2.15.100 S5_CRC_COUNTER0 Register (Address = 0xB3) [Default = 0x00]

S5_CRC_COUNTER0 is shown in S5_CRC_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-729. S5_CRC_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S5_LSB	R	0x0	Stream 5 CRC error counter [7:0]

8.6.2.15.101 S5_CRC_COUNTER1 Register (Address = 0xB4) [Default = 0x00]

S5_CRC_COUNTER1 is shown in S5_CRC_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-730. S5_CRC_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CRC_ERROR_CNT_S5_MSB	R	0x0	Stream 5 CRC error counter [15:8]

8.6.2.15.102 S5_HACTIVE_COUNTER0 Register (Address = 0xB5) [Default = 0x00]

S5_HACTIVE_COUNTER0 is shown in S5_HACTIVE_COUNTER0 Register Field Descriptions.

Return to the Summary Table.

Table 8-731. S5_HACTIVE_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S5_LSB	R	0x0	Stream 5 HACTIVE Counter [7:0]

8.6.2.15.103 S5_HACTIVE_COUNTER1 Register (Address = 0xB6) [Default = 0x00]

S5_HACTIVE_COUNTER1 is shown in S5_HACTIVE_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-732. S5_HACTIVE_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_S5_MSB	R	0x0	Stream 5 HACTIVE Counter [8:15]

8.6.2.15.104 S5_VTOTAL_COUNTER0 Register (Address = 0xB7) [Default = 0x00]

S5_VTOTAL_COUNTER0 is shown in S5_VTOTAL_COUNTER0 Register Field Descriptions.

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Table 8-733. S5_VTOTAL_COUNTER0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S5_LSB	R	0x0	Stream 5 VTOTAL Counter [7:0]

8.6.2.15.105 S5_VTOTAL_COUNTER1 Register (Address = 0xB8) [Default = 0x00]

S5_VTOTAL_COUNTER1 is shown in S5_VTOTAL_COUNTER1 Register Field Descriptions.

Return to the Summary Table.

Table 8-734. S5_VTOTAL_COUNTER1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_S5_MSB	R	0x0	Stream 5 VTOTAL Counter [8:15]

8.6.2.15.106 S5_STATUS Register (Address = 0xB9) [Default = 0x00]

S5_STATUS is shown in S5_STATUS Register Field Descriptions.

Return to the Summary Table.

Table 8-735. S5_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	STS_ECC_ERR_S5	RCP	0x0	FPD4 Received Stream 5 Control Frame ECC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S5_ECC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
2	STS_CRC_ERR_S5	RCP	0x0	FPD4 Received Stream 5 Data Frame CRC Error Status This bit will re-trigger if the corresponding counter registers are not cleared before reading this bit. Use a rising edge on 0x29[6] and S5_CRC_ERROR_CLEAR to clear the source. This bit can be cleared on read after the source is cleared.
1	STS_HACTIVE_CHG_S5	RCP	0x0	Stream 5 HACTIVE Changed This bit will trigger when the current HACTIVE value for Stream 5 in registers 0x43-0x44 is different from the previous value. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. This flag is also set when this stream receives its first video frame.
0	VTOTAL_CHG_S5	RCP	0x0	Stream 5 VTOTAL Changed This bit will trigger when the current VTOTAL value is different from the previous VTOTAL value. To read the current VTOTAL value, apply a rising edge on 0x29[6] after setting S5_VTOTAL_CAPTURE in 0xB0, then read the VTOTAL registers in 0xB7-0xB8. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)

8.6.2.15.107 FPD3_COUNT_CTL Register (Address = 0xC0) [Default = 0x00]

FPD3_COUNT_CTL is shown in FPD3_COUNT_CTL Register Field Descriptions.

Return to the Summary Table.

Register 0x29[6] must have a rising edge to either capture or clear the listed counters.

Table 8-736. FPD3_COUNT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	FPD3_HACTIVE_CAPTURE	R/W	0x0	Capture FPD3 HACTIVE Counter Registers 0xC3-0xC4
6	FPD3_VTOTAL_CAPTURE	R/W	0x0	Capture FPD3 VTOTAL Counter Registers 0xC5-0xC6
5	FPD3_CHECKSUM_CAPTURE	R/W	0x0	Capture FPD3 Checksum Error Counter Registers 0xC1-C2 Requires Page 5 0x1E[7]= 1 for operation.
4:3	RESERVED	R/W	0x0	Reserved
2	FPD3_HACTIVE_CLEAR	R/W	0x0	Clear FPD3 HACTIVE Counter Registers 0xC3-0xC4
1	FPD3_VTOTAL_CLEAR	R/W	0x0	Clear FPD3 VTOTAL Counter Registers 0xC5-0xC6
0	FPD3_CHECKSUM_CLEAR	R/W	0x0	Clear FPD3 Checksum Error Counter Registers 0xC1-C2 Requires Page 5 0x1E[7]= 1 for operation.

8.6.2.15.108 CHECKSUM_ERROR_COUNTER_0_FPD3 Register (Address = 0xC1) [Default = 0x00]

CHECKSUM_ERROR_COUNTER_0_FPD3 is shown in CHECKSUM_ERROR_COUNTER_0_FPD3 Register Field Descriptions.

Return to the Summary Table.

Table 8-737. CHECKSUM_ERROR_COUNTER_0_FPD3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CKSUM_ERROR_CNT_LSB	R	0x0	FPD3 Checksum Error counter [7:0] Requires Page 5 0x1E[7]= 1 for operation.

8.6.2.15.109 CHECKSUM_ERROR_COUNTER_1_FPD3 Register (Address = 0xC2) [Default = 0x00]

CHECKSUM_ERROR_COUNTER_1_FPD3 is shown in CHECKSUM_ERROR_COUNTER_1_FPD3 Register Field Descriptions.

Return to the Summary Table.

Table 8-738. CHECKSUM_ERROR_COUNTER_1_FPD3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CKSUM_ERROR_CNT_MSB	R	0x0	FPD3 Checksum Error Counter [15:8] Requires Page 5 0x1E[7]= 1 for operation.

8.6.2.15.110 FPD3_HACTIVE_0 Register (Address = 0xC3) [Default = 0x00]

FPD3_HACTIVE_0 is shown in FPD3_HACTIVE_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-739. FPD3_HACTIVE_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_FPD3_LSB	R	0x0	FPD3 HACTIVE Value [7:0]

8.6.2.15.111 FPD3_HACTIVE_1 Register (Address = 0xC4) [Default = 0x00]

FPD3_HACTIVE_1 is shown in FPD3_HACTIVE_1 Register Field Descriptions.

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Table 8-740. FPD3_HACTIVE_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_FPD3_MSB	R	0x0	FPD3 HACTIVE Value [15:8]

8.6.2.15.112 FPD3_VTOTAL_0 Register (Address = 0xC5) [Default = 0x00]

FPD3_VTOTAL_0 is shown in FPD3_VTOTAL_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-741. FPD3_VTOTAL_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_FPD3_LSB	R	0x0	FPD3 VTOTAL Value [7:0]

8.6.2.15.113 FPD3_VTOTAL_1 Register (Address = 0xC6) [Default = 0x00]

FPD3_VTOTAL_1 is shown in FPD3_VTOTAL_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-742. FPD3_VTOTAL_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_FPD3_MSB	R	0x0	FPD3 VTOTAL Value [15:8]

8.6.2.15.114 FPD3_STATUS Register (Address = 0xC7) [Default = 0x00]

FPD3_STATUS is shown in FPD3_STATUS Register Field Descriptions.

Return to the Summary Table.

Table 8-743. FPD3_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	Reserved
2	CKSUM_ERR	RCP	0x0	FPD3_RX Checksum Error Status Requires Page 5 0x1E[7] for operation This bit will trigger when the checksum error status is non-zero. This read the current checksum value, apply a rising edge on 0x29[6] after setting FPD3_CHECKSUM_CAPTURE, then read the checksum registers in 0xC1-0xC2. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)
1	HACTIVE_CHG_FPD3	RCP	0x0	FPD3 Video HACTIVE Changed This bit will trigger when the current HACTIVE value is different from the previous HACTIVE value. To read the current HACTIVE value, apply a rising edge on 0x29[6] after setting FPD3_HACTIVE_CAPTURE in 0xC0, then read the HACTIVE registers in 0xC3-0xC4. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)

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Table 8-743. FPD3_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	VTOTAL_CHG_FPD3	RCP	0x0	FPD3 Video VTOTAL Changed This bit will trigger when the current VTOTAL value is different from the previous VTOTAL value. To read the current VTOTAL value, apply a rising edge on 0x29[6] after setting FPD3_VTOTAL_CAPTURE in 0xC0, then read the VTOTAL registers in 0xC5-0xC6. This bit can be cleared by applying a rising edge to 0x29[6] and reading this register. (If a capture or clear was preformed after this flag was set, a second rising edge does not need to be applied to 0x29[6].)

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8.6.2.16 Page 20: Display Timing and PATGEN Registers

PAGE_20 Registers lists the memory-mapped registers for the Page 20: Display Timing and PATGEN registers. All register offset addresses not listed in PAGE_20 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-744. PAGE_20 Registers

Address	Acronym	Register Name	Section
0x0	PGCTL_P0	PGCTL_P0	Go
0x1	PGCFG_P0	PGCFG_P0	Go
0x2	PG_IND_ADDR_P0	PG_IND_ADDR_P0	Go
0x3	PG_IND_DATA_P0	PG_IND_DATA_P0	Go
0x10	PGCTL_P1	PGCTL_P1	Go
0x11	PGCFG_P1	PGCFG_P1	Go
0x12	PG_IND_ADDR_P1	PG_IND_ADDR_P1	Go
0x13	PG_IND_DATA_P1	PG_IND_DATA_P1	Go
0x20	DTG_CTL_P0	DTG_CTL_P0	Go
0x21	HTOTAL_MSB_P0	HTOTAL_MSB_P0	Go
0x22	HTOTAL_LSB_P0	HTOTAL_LSB_P0	Go
0x23	VTOTAL_MSB_P0	VTOTAL_MSB_P0	Go
0x24	VTOTAL_LSB_P0	VTOTAL_LSB_P0	Go
0x25	HACTIVE_MSB_P0	HACTIVE_MSB_P0	Go
0x26	HACTIVE_LSB_P0	HACTIVE_LSB_P0	Go
0x27	VRES_MSB_P0	VRES_MSB_P0	Go
0x28	VRES_LSB_P0	VRES_LSB_P0	Go
0x29	HSTART_MSB_P0	HSTART_MSB_P0	Go
0x2A	HSTART_LSB_P0	HSTART_LSB_P0	Go
0x2B	VSTART_MSB_P0	VSTART_MSB_P0	Go
0x2C	VSTART_LSB_P0	VSTART_LSB_P0	Go
0x2D	VSYNC_MSB_P0	VSYNC_MSB_P0	Go
0x2E	VSYNC_LSB_P0	VSYNC_LSB_P0	Go
0x2F	HSYNC_MSB_P0	HSYNC_MSB_P0	Go
0x30	HSYNC_LSB_P0	HSYNC_LSB_P0	Go
0x32	DTG_RESET_CTL_P0	DTG_RESET_CTL_P0	Go
0x40	MEAS_HTOTAL_MSB_P0	MEAS_HTOTAL_MSB_P0	Go
0x41	MEAS_HTOTAL_LSB_P0	MEAS_HTOTAL_LSB_P0	Go
0x42	MEAS_VTOTAL_MSB_P0	MEAS_VTOTAL_MSB_P0	Go
0x43	MEAS_VTOTAL_LSB_P0	MEAS_VTOTAL_LSB_P0	Go
0x44	MEAS_HACTIVE_MSB_P0	MEAS_HACTIVE_MSB_P0	Go
0x45	MEAS_HACTIVE_LSB_P0	MEAS_HACTIVE_LSB_P0	Go
0x46	MEAS_VRES_MSB_P0	MEAS_VRES_MSB_P0	Go
0x47	MEAS_VRES_LSB_P0	MEAS_VRES_LSB_P0	Go
0x48	MEAS_HSTART_MSB_P0	MEAS_HSTART_MSB_P0	Go
0x49	MEAS_HSTART_LSB_P0	MEAS_HSTART_LSB_P0	Go
0x4A	MEAS_VSTART_MSB_P0	MEAS_VSTART_MSB_P0	Go
0x4B	MEAS_VSTART_LSB_P0	MEAS_VSTART_LSB_P0	Go
0x4C	MEAS_HSYNC_MSB_P0	MEAS_HSYNC_MSB_P0	Go
0x4D	MEAS_HSYNC_LSB_P0	MEAS_HSYNC_LSB_P0	Go
0x4E	MEAS_VSYNC_MSB_P0	MEAS_VSYNC_MSB_P0	Go

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Table 8-744. PAGE_20 Registers (continued)

Address	Acronym	Register Name	Section
0x4F	MEAS_VSYNC_LSB_P0	MEAS_VSYNC_LSB_P0	Go
0x50	DTG_CTL_P1	DTG_CTL_P1	Go
0x51	HTOTAL_MSB_P1	HTOTAL_MSB_P1	Go
0x52	HTOTAL_LSB_P1	HTOTAL_LSB_P1	Go
0x53	VTOTAL_MSB_P1	VTOTAL_MSB_P1	Go
0x54	VTOTAL_LSB_P1	VTOTAL_LSB_P1	Go
0x55	HACTIVE_MSB_P1	HACTIVE_MSB_P1	Go
0x56	HACTIVE_LSB_P1	HACTIVE_LSB_P1	Go
0x57	VRES_MSB_P1	VRES_MSB_P1	Go
0x58	VRES_LSB_P1	VRES_LSB_P1	Go
0x59	HSTART_MSB_P1	HSTART_MSB_P1	Go
0x5A	HSTART_LSB_P1	HSTART_LSB_P1	Go
0x5B	VSTART_MSB_P1	VSTART_MSB_P1	Go
0x5C	VSTART_LSB_P1	VSTART_LSB_P1	Go
0x5D	VSYNC_MSB_P1	VSYNC_MSB_P1	Go
0x5E	VSYNC_LSB_P1	VSYNC_LSB_P1	Go
0x5F	HSYNC_MSB_P1	HSYNC_MSB_P1	Go
0x60	HSYNC_LSB_P1	HSYNC_LSB_P1	Go
0x62	DTG_RESET_CTL_P1	DTG_RESET_CTL_P1	Go
0x70	MEAS_HTOTAL_MSB_P1	MEAS_HTOTAL_MSB_P1	Go
0x71	MEAS_HTOTAL_LSB_P1	MEAS_HTOTAL_LSB_P1	Go
0x72	MEAS_VTOTAL_MSB_P1	MEAS_VTOTAL_MSB_P1	Go
0x73	MEAS_VTOTAL_LSB_P1	MEAS_VTOTAL_LSB_P1	Go
0x74	MEAS_HACTIVE_MSB_P1	MEAS_HACTIVE_MSB_P1	Go
0x75	MEAS_HACTIVE_LSB_P1	MEAS_HACTIVE_LSB_P1	Go
0x76	MEAS_VRES_MSB_P1	MEAS_VRES_MSB_P1	Go
0x77	MEAS_VRES_LSB_P1	MEAS_VRES_LSB_P1	Go
0x78	MEAS_HSTART_MSB_P1	MEAS_HSTART_MSB_P1	Go
0x79	MEAS_HSTART_LSB_P1	MEAS_HSTART_LSB_P1	Go
0x7A	MEAS_VSTART_MSB_P1	MEAS_VSTART_MSB_P1	Go
0x7B	MEAS_VSTART_LSB_P1	MEAS_VSTART_LSB_P1	Go
0x7C	MEAS_HSWIDTH_MSB_P1	MEAS_HSWIDTH_MSB_P1	Go
0x7D	MEAS_HSWIDTH_LSB_P1	MEAS_HSWIDTH_LSB_P1	Go
0x7E	MEAS_VSWIDTH_MSB_P1	MEAS_VSWIDTH_MSB_P1	Go
0x7F	MEAS_VSWIDTH_LSB_P1	MEAS_VSWIDTH_LSB_P1	Go

Complex bit access types are encoded to fit into small table cells. Page 20: Display Timing and PATGEN Access Type Codes shows the codes that are used for access types in this section.

Table 8-745. Page 20: Display Timing and PATGEN Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

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Table 8-745. Page 20: Display Timing and PATGEN Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.16.1 PGCTL_P0 Register (Address = 0x0) [Default = 0x08]

PGCTL_P0 is shown in PGCTL_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-746. PGCTL_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: White and Black Checkerboard 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers on the Pattern Generator register page 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom and Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 0: Enable Pattern Generator synchronous to video input 1: Enable Pattern Generator asynchronous to video input
1	PATCHK_EN	R/W	0x0	Pattern Checker Enable: 0: Disable Pattern Checker 1: Enable Pattern Checker
0	PATGEN_EN	R/W	0x0	Pattern Generator Enable: 0: Disable Pattern Generator 1: Enable Pattern Generator

8.6.2.16.2 PGCFG_P0 Register (Address = 0x1) [Default = 0x08]

PGCFG_P0 is shown in PGCFG_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-747. PGCFG_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHKR	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 00: Normal operation (each square is 1x1 pixel) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 11: Scale checkered patterns by 16 (each square is 16x16 pixels)
5:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 000: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 001: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 010: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 011-111: Reserved
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 0: Do not invert the color output. 1: Invert the color output.
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 0: The Pattern Generator retains the current pattern. 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register (register 0x16 on the PATGEN register page).

8.6.2.16.3 PG_IND_ADDR_P0 Register (Address = 0x2) [Default = 0x00]

PG_IND_ADDR_P0 is shown in PG_IND_ADDR_P0 Register Field Descriptions.

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Table 8-748. PG_IND_ADDR_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment When this bit is 1, reads or writes to the PG_IND_DATA_P0 (0x03) register will automatically increment the indirect address in bits6:0.
6:0	PATGEN_IA	R/W	0x0	Indirect Address Sets the target indirect address for a read or write. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-increment is enabled and the next address is the desired address.

8.6.2.16.4 PG_IND_DATA_P0 Register (Address = 0x3) [Default = 0x00]

PG_IND_DATA_P0 is shown in PG_IND_DATA_P0 Register Field Descriptions.

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Table 8-749. PG_IND_DATA_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data Contains write data when writing to indirect register. Contains read data when reading to indirect register.

8.6.2.16.5 PGCTL_P1 Register (Address = 0x10) [Default = 0x08]

PGCTL_P1 is shown in PGCTL_P1 Register Field Descriptions.

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Table 8-750. PGCTL_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	PATGEN_SEL	R/W	0x1	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. Note that these patterns are inverted if PGCFG:PATGEN_INV is set to 1. 00000: White and Black Checkerboard 00001: White 00010: Black 00011: Red 00100: Green 00101: Blue 00110: Horizontally Scaled Black to White 00111: Horizontally Scaled Black to Red 01000: Horizontally Scaled Black to Green 01001: Horizontally Scaled Black to Blue 01010: Vertically Scaled Black to White 01011: Vertically Scaled Black to Red 01100: Vertically Scaled Black to Green 01101: Vertically Scaled Black to Blue 01110: Custom color configured in PGRS, PGGS, PGBS registers on the Pattern Generator register page 01111: VCOM (Yellow, Cyan, Blue, Red) 10000: Alternate VCOM (Blue, Cyan, Yellow, Red) 10001: Custom Color Checkerboard (Custom and Black) 10010: Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) 10011: UNH-IOL MIPI D-PHY compliance test pattern 11010-11111: Reserved
2	PATGEN_FREERUN	R/W	0x0	Pattern Generator Free-Running 0: Enable Pattern Generator synchronous to video input 1: Enable Pattern Generator asynchronous to video input
1	PATCHK_EN	R/W	0x0	Pattern Checker Enable: 0: Disable Pattern Checker 1: Enable Pattern Checker
0	PATGEN_EN	R/W	0x0	Pattern Generator Enable: 0: Disable Pattern Generator 1: Enable Pattern Generator

8.6.2.16.6 PGCFG_P1 Register (Address = 0x11) [Default = 0x08]

PGCFG_P1 is shown in PGCFG_P1 Register Field Descriptions.

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Table 8-751. PGCFG_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PATGEN_SCALE_CHKR	R/W	0x0	Scale Checkered Patterns (VCOM and checkerboard): 00: Normal operation (each square is 1x1 pixel) 01: Scale checkered patterns by 4 (each square is 4x4 pixels) 10: Scale checkered patterns by 8 (each square is 8x8 pixels) 11: Scale checkered patterns by 16 (each square is 16x16 pixels)
5:3	PATGEN_COLOR_DEPTH	R/W	0x1	Color Depth: 000: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 001: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness and the R, G, and B outputs use the eight most significant color bits 010: Enable 30-bit pattern generation. Scaled patterns use 1024 levels of brightness and the R, G, and B outputs use the ten most significant color bits 011-111: Reserved for future expansion
2	PATGEN_TSEL	R/W	0x0	Timing Select Control: 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers.
1	PATGEN_INV	R/W	0x0	Enable Inverted Color Patterns: 0: Do not invert the color output. 1: Invert the color output.
0	PATGEN_ASCRL	R/W	0x0	Auto-Scroll Enable: 0: The Pattern Generator retains the current pattern. 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register (register 0x16 on the PATGEN register page).

8.6.2.16.7 PG_IND_ADDR_P1 Register (Address = 0x12) [Default = 0x00]

PG_IND_ADDR_P1 is shown in PG_IND_ADDR_P1 Register Field Descriptions.

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Table 8-752. PG_IND_ADDR_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PATGEN_IND_AUTO_INC	R/W	0x0	Indirect Address Auto-Increment When this bit is 1, reads or writes to the PG_IND_DATA_P1 (0x13) register will automatically increment the indirect address in bits6:0.
6:0	PATGEN_IA	R/W	0x0	Indirect Address Sets the target indirect address for a read or write. It should be written prior to reading or writing the Pattern Generator Indirect Data register unless auto-increment is enabled and the next address is the desired address.

8.6.2.16.8 PG_IND_DATA_P1 Register (Address = 0x13) [Default = 0x00]

PG_IND_DATA_P1 is shown in PG_IND_DATA_P1 Register Field Descriptions.

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Table 8-753. PG_IND_DATA_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_ID	R/W	0x0	Indirect Data Contains write data when writing to indirect register. Contains read data when reading to indirect register.

8.6.2.16.9 DTG_CTL_P0 Register (Address = 0x20) [Default = 0x03]

DTG_CTL_P0 is shown in DTG_CTL_P0 Register Field Descriptions.

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Table 8-754. DTG_CTL_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	DTG_MODE		0x0	This bit is set by MODE_SEL1 strap. 00: Reserved 01: Reserved 1x: Quad-pixel
5:4	RESERVED	R/W	0x0	Reserved
3	VSYNC_POLARITY	R/W	0x0	Polarity of the vertical sync pulse 0: High values are TRUE (active high) 1: Low values are TRUE (active low)
2	HSYNC_POLARITY	R/W	0x0	Polarity of the horizontal sync pulse 0: High values are TRUE (active high) 1: Low values are TRUE (active low)
1:0	PG_DATA_SOURCE_SEL	R/W	0x3	Select Pattern Generator Parameter Source The PATGEN parameters can be sourced from the measurement counter in the device or through control registers. 00: Use register values from HTOTAL through HSYNC override registers below (0x21-0x30). Individual override enable bits for each video timing parameter in registers 0x21-0x30 do not need to be set with this SOURCE_SEL setting. 01: Measured video timing parameters (0x40-0x4F) will be used by DTG. Individual video timing parameters may be overwritten by setting the override enable bit in 0x21-0x30. 10: Use register values from HTOTAL through HSYNC override registers below (0x21-0x30). Individual override enable bits for each video timing parameter in registers 0x21-0x30 do not need to be set with this SOURCE_SEL setting. 11: DTG will use HActive value received over the main link and all other timing parameters will use the measured values in 0x40-0x43 and 0x46-0x4F. Individual override enable bits for each video timing parameter in 0x21-0x30 may still be used.

8.6.2.16.10 HTOTAL_MSB_P0 Register (Address = 0x21) [Default = 0x00]

HTOTAL_MSB_P0 is shown in HTOTAL_MSB_P0 Register Field Descriptions.

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Table 8-755. HTOTAL_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HTOTAL_OVRR_EN	R/W	0x0	Override Enable for HTOTAL 0: Measured or overwritten determined by 0x20[1:0] 1: HTOTAL can be overwritten (Bits6:0 and 0x22[7:0])
6:0	HTOTAL_MSB	R/W	0x0	HTOTAL MSB HTOTAL is the horizontal line length total in clocks. This field contains the most significant bits.

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8.6.2.16.11 HTOTAL_LSB_P0 Register (Address = 0x22) [Default = 0x00]

HTOTAL_LSB_P0 is shown in HTOTAL_LSB_P0 Register Field Descriptions.

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Table 8-756. HTOTAL_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HTOTAL_LSB	R/W	0x0	HTOTAL LSB HTOTAL is the horizontal line length total in clocks. This field contains the least significant bits.

8.6.2.16.12 VTOTAL_MSB_P0 Register (Address = 0x23) [Default = 0x00]

VTOTAL_MSB_P0 is shown in VTOTAL_MSB_P0 Register Field Descriptions.

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Table 8-757. VTOTAL_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VTOTAL_OVRR_EN	R/W	0x0	Override Enable for VTOTAL 0: Measured or overwritten determined by 0x20[1:0] 1: VTOTAL can be overwritten (Bits6:0 and 0x24[7:0])
6:0	VTOTAL_MSB	R/W	0x0	VTOTAL MSB VTOTAL is the total number of lines (rows) per video frame. This field contains the most significant bits.

8.6.2.16.13 VTOTAL_LSB_P0 Register (Address = 0x24) [Default = 0x00]

VTOTAL_LSB_P0 is shown in VTOTAL_LSB_P0 Register Field Descriptions.

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Table 8-758. VTOTAL_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_LSB	R/W	0x0	VTOTAL LSB VTOTAL is the total number of lines (rows) per video frame. This field contains the least significant bits.

8.6.2.16.14 HACTIVE_MSB_P0 Register (Address = 0x25) [Default = 0x00]

HACTIVE_MSB_P0 is shown in HACTIVE_MSB_P0 Register Field Descriptions.

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Table 8-759. HACTIVE_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HACTIVE_OVRR_EN	R/W	0x0	Override Enable for HACTIVE 0: Measured, received or overwritten determined by 0x20[1:0] 1: HACTIVE can be overwritten (Bits6:0 and 0x26[7:0])
6:0	HACTIVE_MSB	R/W	0x0	HACTIVE MSB HACTIVE is the number of active pixels per horizontal line. This field contains the most significant bits.

8.6.2.16.15 HACTIVE_LSB_P0 Register (Address = 0x26) [Default = 0x00]

HACTIVE_LSB_P0 is shown in HACTIVE_LSB_P0 Register Field Descriptions.

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Table 8-760. HACTIVE_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_LSB	R/W	0x0	HACTIVE LSB HACTIVE is the number of active pixels per horizontal line. This field contains the least significant bits.

8.6.2.16.16 VRES_MSB_P0 Register (Address = 0x27) [Default = 0x00]

VRES_MSB_P0 is shown in VRES_MSB_P0 Register Field Descriptions.

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Table 8-761. VRES_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VRES_OVRR_EN	R/W	0x0	Override Enable for VRES 0: Measured or overwritten determined by 0x20[1:0] 1: VRES can be overwritten (Bits6:0 and 0x28[7:0])
6:0	VRES_MSB	R/W	0x0	VRES MSB VRES is the number of active lines (rows) per frame. This field contains the most significant bits.

8.6.2.16.17 VRES_LSB_P0 Register (Address = 0x28) [Default = 0x00]

VRES_LSB_P0 is shown in VRES_LSB_P0 Register Field Descriptions.

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Table 8-762. VRES_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VRES_LSB	R/W	0x0	VRES LSB VRES is the number of active lines (rows) per frame. This field contains the least significant bits.

8.6.2.16.18 HSTART_MSB_P0 Register (Address = 0x29) [Default = 0x00]

HSTART_MSB_P0 is shown in HSTART_MSB_P0 Register Field Descriptions.

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Table 8-763. HSTART_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HSTART_OVRR_EN	R/W	0x0	Override Enable for HSTART 0: Measured or overwritten determined by 0x20[1:0] 1: HSTART can be overwritten (Bits6:0 and 0x30[7:0])
6:0	HSTART_MSB	R/W	0x0	HSTART MSB HSTART is the number of clocks between the leading edge of the horizontal sync and the start of active data. This field contains the most significant bits.

8.6.2.16.19 HSTART_LSB_P0 Register (Address = 0x2A) [Default = 0x00]

HSTART_LSB_P0 is shown in HSTART_LSB_P0 Register Field Descriptions.

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Table 8-764. HSTART_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HSTART_LSB	R/W	0x0	HSTART LSB HSTART is the number of clocks between the leading edge of the horizontal sync and the start of active data. This field contains the least significant bits.

8.6.2.16.20 VSTART_MSB_P0 Register (Address = 0x2B) [Default = 0x00]

VSTART_MSB_P0 is shown in VSTART_MSB_P0 Register Field Descriptions.

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Table 8-765. VSTART_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VSTART_OVRR_EN	R/W	0x0	Override Enable for VSTART 0: Measured or overwritten determined by 0x20[1:0] 1: VSTART can be overwritten (Bits6:0 and 0x2C[7:0])
6:0	VSTART_MSB	R/W	0x0	VSTART MSB VSTART is the number of lines between the leading edge of the vertical sync and the first line of active data. This field contains the most significant bits.

8.6.2.16.21 VSTART_LSB_P0 Register (Address = 0x2C) [Default = 0x00]

VSTART_LSB_P0 is shown in VSTART_LSB_P0 Register Field Descriptions.

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Table 8-766. VSTART_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VSTART_LSB	R/W	0x0	VSTART LSB VSTART is the number of lines between the leading edge of the vertical sync and the first line of active data. This field contains the least significant bits.

8.6.2.16.22 VSYNC_MSB_P0 Register (Address = 0x2D) [Default = 0x00]

VSYNC_MSB_P0 is shown in VSYNC_MSB_P0 Register Field Descriptions.

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Table 8-767. VSYNC_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	VSYNC_OVRR_EN	R/W	0x0	Override Enabled for VSYNC 0: Measured or overwritten determined by 0x20[1:0] 1: VSYNC can be overwritten (Bits5:0 and 0x2E[7:0])
5:0	VSYNC_MSB	R/W	0x0	VSYNC MSB VSYNC is the width of the vertical sync in lines. This field contains the most significant bits.

8.6.2.16.23 VSYNC_LSB_P0 Register (Address = 0x2E) [Default = 0x00]

VSYNC_LSB_P0 is shown in VSYNC_LSB_P0 Register Field Descriptions.

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Table 8-768. VSYNC_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VSYNC_LSB	R/W	0x0	VSYNC LSB VSYNC is the width of the vertical sync in lines. This field contains the least significant bits.

8.6.2.16.24 HSYNC_MSB_P0 Register (Address = 0x2F) [Default = 0x00]

HSYNC_MSB_P0 is shown in HSYNC_MSB_P0 Register Field Descriptions.

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Table 8-769. HSYNC_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	HSYNC_OVRR_EN	R/W	0x0	Override Enable for HSYNC 0: Measured or overwritten determined by 0x20[1:0] 1: HSYNC can be overwritten (Bits5:0 and 0x30[7:0])
5:0	HSYNC_MSB	R/W	0x0	HSYNC MSB HSYNC is the horizontal sync width in clock cycles. This field contains the most significant bits.

8.6.2.16.25 HSYNC_LSB_P0 Register (Address = 0x30) [Default = 0x00]

HSYNC_LSB_P0 is shown in HSYNC_LSB_P0 Register Field Descriptions.

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Table 8-770. HSYNC_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HSYNC_LSB	R/W	0x0	HSYNC LSB HSYNC is the horizontal sync width in clock cycles. This field contains the least significant bits.

8.6.2.16.26 DTG_RESET_CTL_P0 Register (Address = 0x32) [Default = 0x04]

DTG_RESET_CTL_P0 is shown in DTG_RESET_CTL_P0 Register Field Descriptions.

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Table 8-771. DTG_RESET_CTL_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R/W	0x0	Reserved
2	DTG_RESET_LOCK_EN	R/W	0x1	Enable DTG reset based on FPD Lock 0: DTG reset unaffected by FPD lock 1: DTG will go into reset when lock goes low and come out of reset when lock goes high
1	DTG_RESET	R/W	0x0	Manual DTG Reset 0: Normal operation 1: DTG is reset. This re-initializes the display DTG.
0	DTG_WATCHDOG_DIS	R/W	0x0	Disable DTG Watchdog Timer If the watchdog detectes >4 missed HSYNC pulses, it resets the DTG. 0: Normal operation, watchdog enabled 1: Watchdog disabled

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8.6.2.16.27 MEAS_HTOTAL_MSB_P0 Register (Address = 0x40) [Default = 0x00]

MEAS_HTOTAL_MSB_P0 is shown in MEAS_HTOTAL_MSB_P0 Register Field Descriptions.

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Table 8-772. MEAS_HTOTAL_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HTOTAL_MSB	R	0x0	Measured HTOTAL MSB

8.6.2.16.28 MEAS_HTOTAL_LSB_P0 Register (Address = 0x41) [Default = 0x00]

MEAS_HTOTAL_LSB_P0 is shown in MEAS_HTOTAL_LSB_P0 Register Field Descriptions.

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Table 8-773. MEAS_HTOTAL_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HTOTAL_LSB	R	0x0	Measured HTOTAL LSB

8.6.2.16.29 MEAS_VTOTAL_MSB_P0 Register (Address = 0x42) [Default = 0x00]

MEAS_VTOTAL_MSB_P0 is shown in MEAS_VTOTAL_MSB_P0 Register Field Descriptions.

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Table 8-774. MEAS_VTOTAL_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VTOTAL_MSB	R	0x0	Measured VTOTAL MSB

8.6.2.16.30 MEAS_VTOTAL_LSB_P0 Register (Address = 0x43) [Default = 0x00]

MEAS_VTOTAL_LSB_P0 is shown in MEAS_VTOTAL_LSB_P0 Register Field Descriptions.

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Table 8-775. MEAS_VTOTAL_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VTOTAL_LSB	R	0x0	Measured VTOTAL LSB

8.6.2.16.31 MEAS_HACTIVE_MSB_P0 Register (Address = 0x44) [Default = 0x00]

MEAS_HACTIVE_MSB_P0 is shown in MEAS_HACTIVE_MSB_P0 Register Field Descriptions.

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Table 8-776. MEAS_HACTIVE_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HACTIVE_MSB	R	0x0	Measured HACTIVE MSB

8.6.2.16.32 MEAS_HACTIVE_LSB_P0 Register (Address = 0x45) [Default = 0x00]

MEAS_HACTIVE_LSB_P0 is shown in MEAS_HACTIVE_LSB_P0 Register Field Descriptions.

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Table 8-777. MEAS_HACTIVE_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HACTIVE_LSB	R	0x0	Measured HACTIVE LSB

8.6.2.16.33 MEAS_VRES_MSB_P0 Register (Address = 0x46) [Default = 0x00]

MEAS_VRES_MSB_P0 is shown in MEAS_VRES_MSB_P0 Register Field Descriptions.

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Table 8-778. MEAS_VRES_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VRES_MSB	R	0x0	Measured VRES MSB

8.6.2.16.34 MEAS_VRES_LSB_P0 Register (Address = 0x47) [Default = 0x00]

MEAS_VRES_LSB_P0 is shown in MEAS_VRES_LSB_P0 Register Field Descriptions.

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Table 8-779. MEAS_VRES_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VRES_LSB	R	0x0	Measured VRES LSB

8.6.2.16.35 MEAS_HSTART_MSB_P0 Register (Address = 0x48) [Default = 0x00]

MEAS_HSTART_MSB_P0 is shown in MEAS_HSTART_MSB_P0 Register Field Descriptions.

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Table 8-780. MEAS_HSTART_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HSTART_MSB	R	0x0	Measured HSTART MSB

8.6.2.16.36 MEAS_HSTART_LSB_P0 Register (Address = 0x49) [Default = 0x00]

MEAS_HSTART_LSB_P0 is shown in MEAS_HSTART_LSB_P0 Register Field Descriptions.

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Table 8-781. MEAS_HSTART_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HSTART_LSB	R	0x0	Measured HSTART LSB

8.6.2.16.37 MEAS_VSTART_MSB_P0 Register (Address = 0x4A) [Default = 0x00]

MEAS_VSTART_MSB_P0 is shown in MEAS_VSTART_MSB_P0 Register Field Descriptions.

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Table 8-782. MEAS_VSTART_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VSTART_MSB	R	0x0	Measured VSTART MSB

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8.6.2.16.38 MEAS_VSTART_LSB_P0 Register (Address = 0x4B) [Default = 0x00]

MEAS_VSTART_LSB_P0 is shown in MEAS_VSTART_LSB_P0 Register Field Descriptions.

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Table 8-783. MEAS_VSTART_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VSTART_LSB	R	0x0	Measured VSTART LSB

8.6.2.16.39 MEAS_HSYNC_MSB_P0 Register (Address = 0x4C) [Default = 0x00]

MEAS_HSYNC_MSB_P0 is shown in MEAS_HSYNC_MSB_P0 Register Field Descriptions.

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Table 8-784. MEAS_HSYNC_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MEAS_HSYNC_MSB	R	0x0	Measured HSYNC MSB

8.6.2.16.40 MEAS_HSYNC_LSB_P0 Register (Address = 0x4D) [Default = 0x00]

MEAS_HSYNC_LSB_P0 is shown in MEAS_HSYNC_LSB_P0 Register Field Descriptions.

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Table 8-785. MEAS_HSYNC_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HSYNC_LSB	R	0x0	Measured HSYNC LSB

8.6.2.16.41 MEAS_VSYNC_MSB_P0 Register (Address = 0x4E) [Default = 0x00]

MEAS_VSYNC_MSB_P0 is shown in MEAS_VSYNC_MSB_P0 Register Field Descriptions.

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Table 8-786. MEAS_VSYNC_MSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MEAS_VSWIDTH_MSB	R	0x0	Measured VSYNC MSB

8.6.2.16.42 MEAS_VSYNC_LSB_P0 Register (Address = 0x4F) [Default = 0x00]

MEAS_VSYNC_LSB_P0 is shown in MEAS_VSYNC_LSB_P0 Register Field Descriptions.

Return to the Summary Table.

Table 8-787. MEAS_VSYNC_LSB_P0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VSWIDTH_LSB	R	0x0	Measured VSYNC LSB

8.6.2.16.43 DTG_CTL_P1 Register (Address = 0x50) [Default = 0x03]

DTG_CTL_P1 is shown in DTG_CTL_P1 Register Field Descriptions.

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Table 8-788. DTG_CTL_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	DTG_MODE		0x0	This bit is set by MODE_SEL1 strap. 00: Reserved 01: Reserved 1x: Quad-pixel
5:4	RESERVED	R/W	0x0	Reserved
3	VSYNC_POLARITY	R/W	0x0	Polarity of the vertical sync pulse 0: High values are TRUE (active high) 1: Low values are TRUE (active low)
2	HSYNC_POLARITY	R/W	0x0	Polarity of the horizontal sync pulse 0: High values are TRUE (active high) 1: Low values are TRUE (active low)
1:0	PG_DATA_SOURCE_SEL	R/W	0x3	Select Pattern Generator Parameter Source The PATGEN parameters can be sourced from the measurement counter in the device or through control registers. 00: Use register values from HTOTAL through HSYNC below. The override enable bits do not need to be set with this SOURCE_SEL setting. 01: Use measurement counters. Individual overrides can be done using the registers that follow. 10: Use register values from htotal through hswidth below. The override enable bits do not need to be set with this SOURCE_SEL setting. 11: Use measurement counters for all values except HACTIVE. HACTIVE will be set using the value received over the main link.

8.6.2.16.44 HTOTAL_MSB_P1 Register (Address = 0x51) [Default = 0x00]

HTOTAL_MSB_P1 is shown in HTOTAL_MSB_P1 Register Field Descriptions.

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Table 8-789. HTOTAL_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HTOTAL_OVRR_EN	R/W	0x0	Override Enable for HTOTAL 0: Normal operation 1: HTOTAL can be overwritten (Bits6:0 and 0x22[7:0])
6:0	HTOTAL_MSB	R/W	0x0	HTOTAL MSB HTOTAL is the horizontal line length total in clocks. This field contains the most significant bits.

8.6.2.16.45 HTOTAL_LSB_P1 Register (Address = 0x52) [Default = 0x00]

HTOTAL_LSB_P1 is shown in HTOTAL_LSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-790. HTOTAL_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HTOTAL_LSB	R/W	0x0	HTOTAL LSB HTOTAL is the horizontal line length total in clocks. This field contains the least significant bits.

8.6.2.16.46 VTOTAL_MSB_P1 Register (Address = 0x53) [Default = 0x00]

VTOTAL_MSB_P1 is shown in VTOTAL_MSB_P1 Register Field Descriptions.

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Table 8-791. VTOTAL_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VTOTAL_OVRR_EN	R/W	0x0	Override Enable for VTOTAL 0: Normal operation 1: VTOTAL can be overwritten (Bits6:0 and 0x24[7:0])
6:0	VTOTAL_MSB	R/W	0x0	VTOTAL MSB VTOTAL is the total number of lines (rows) per video frame. This field contains the most significant bits.

8.6.2.16.47 VTOTAL_LSB_P1 Register (Address = 0x54) [Default = 0x00]

VTOTAL_LSB_P1 is shown in VTOTAL_LSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-792. VTOTAL_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VTOTAL_LSB	R/W	0x0	VTOTAL LSB VTOTAL is the total number of lines (rows) per video frame. This field contains the least significant bits.

8.6.2.16.48 HACTIVE_MSB_P1 Register (Address = 0x55) [Default = 0x00]

HACTIVE_MSB_P1 is shown in HACTIVE_MSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-793. HACTIVE_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HACTIVE_OVRR_EN	R/W	0x0	Override Enable for HACTIVE 0: Normal operation 1: HACTIVE can be overwritten (Bits6:0 and 0x26[7:0])
6:0	HACTIVE_MSB	R/W	0x0	HACTIVE MSB HACTIVE is the number of active pixels per horizontal line. This field contains the most significant bits.

8.6.2.16.49 HACTIVE_LSB_P1 Register (Address = 0x56) [Default = 0x00]

HACTIVE_LSB_P1 is shown in HACTIVE_LSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-794. HACTIVE_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HACTIVE_LSB	R/W	0x0	HACTIVE LSB HACTIVE is the number of active pixels per horizontal line. This field contains the least significant bits.

8.6.2.16.50 VRES_MSB_P1 Register (Address = 0x57) [Default = 0x00]

VRES_MSB_P1 is shown in VRES_MSB_P1 Register Field Descriptions.

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Table 8-795. VRES_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VRES_OVRR_EN	R/W	0x0	Override Enable for VRES 0: Normal operation 1: VRES can be overwritten (Bits6:0 and 0x28[7:0])
6:0	VRES_MSB	R/W	0x0	VRES MSB VRES is the number of active lines (rows) per frame. This field contains the most significant bits.

8.6.2.16.51 VRES_LSB_P1 Register (Address = 0x58) [Default = 0x00]

VRES_LSB_P1 is shown in VRES_LSB_P1 Register Field Descriptions.

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Table 8-796. VRES_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VRES_LSB	R/W	0x0	VRES LSB VRES is the number of active lines (rows) per frame. This field contains the least significant bits.

8.6.2.16.52 HSTART_MSB_P1 Register (Address = 0x59) [Default = 0x00]

HSTART_MSB_P1 is shown in HSTART_MSB_P1 Register Field Descriptions.

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Table 8-797. HSTART_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HSTART_OVRR_EN	R/W	0x0	Override Enable for HSTART 0: Normal operation 1: HSTART can be overwritten (Bits6:0 and 0x30[7:0])
6:0	HSTART_MSB	R/W	0x0	HSTART MSB HSTART is the number of clocks between the leading edge of the horizontal sync and the start of active data. This field contains the most significant bits.

8.6.2.16.53 HSTART_LSB_P1 Register (Address = 0x5A) [Default = 0x00]

HSTART_LSB_P1 is shown in HSTART_LSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-798. HSTART_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HSTART_LSB	R/W	0x0	HSTART LSB HSTART is the number of clocks between the leading edge of the horizontal sync and the start of active data. This field contains the least significant bits.

8.6.2.16.54 VSTART_MSB_P1 Register (Address = 0x5B) [Default = 0x00]

VSTART_MSB_P1 is shown in VSTART_MSB_P1 Register Field Descriptions.

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Table 8-799. VSTART_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	VSTART_OVRR_EN	R/W	0x0	Override Enable for VSTART 0: Normal operation 1: VSTART can be overwritten (Bits6:0 and 0x2C[7:0])
6:0	VSTART_MSB	R/W	0x0	VSTART MSB VSTART is the number of lines between the leading edge of the vertical sync and the first line of active data. This field contains the most significant bits.

8.6.2.16.55 VSTART_LSB_P1 Register (Address = 0x5C) [Default = 0x00]

VSTART_LSB_P1 is shown in VSTART_LSB_P1 Register Field Descriptions.

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Table 8-800. VSTART_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VSTART_LSB	R/W	0x0	VSTART LSB VSTART is the number of lines between the leading edge of the vertical sync and the first line of active data. This field contains the least significant bits.

8.6.2.16.56 VSYNC_MSB_P1 Register (Address = 0x5D) [Default = 0x00]

VSYNC_MSB_P1 is shown in VSYNC_MSB_P1 Register Field Descriptions.

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Table 8-801. VSYNC_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	VSYNC_OVRR_EN	R/W	0x0	Override Enabled for VSYNC 0: Normal operation 1: VSYNC can be overwritten (Bits5:0 and 0x2E[7:0])
5:0	VSYNC_MSB	R/W	0x0	VSYNC MSB VSYNC is the width of the vertical sync in lines. This field contains the most significant bits.

8.6.2.16.57 VSYNC_LSB_P1 Register (Address = 0x5E) [Default = 0x00]

VSYNC_LSB_P1 is shown in VSYNC_LSB_P1 Register Field Descriptions.

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Table 8-802. VSYNC_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	VSYNC_LSB	R/W	0x0	VSYNC LSB VSYNC is the width of the vertical sync in lines. This field contains the least significant bits.

8.6.2.16.58 HSYNC_MSB_P1 Register (Address = 0x5F) [Default = 0x00]

HSYNC_MSB_P1 is shown in HSYNC_MSB_P1 Register Field Descriptions.

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Table 8-803. HSYNC_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	HSYNC_OVRR_EN	R/W	0x0	Override Enable for HSYNC 0: Normal operation 1: HSYNC can be overwritten (Bits5:0 and 0x30[7:0])
5:0	HSYNC_MSB	R/W	0x0	HSYNC MSB HSYNC is the horizontal sync width in clock cycles. This field contains the most significant bits.

8.6.2.16.59 HSYNC_LSB_P1 Register (Address = 0x60) [Default = 0x00]

HSYNC_LSB_P1 is shown in HSYNC_LSB_P1 Register Field Descriptions.

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Table 8-804. HSYNC_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	HSYNC_LSB	R/W	0x0	HSYNC LSB HSYNC is the horizontal sync width in clock cycles. This field contains the least significant bits.

8.6.2.16.60 DTG_RESET_CTL_P1 Register (Address = 0x62) [Default = 0x04]

DTG_RESET_CTL_P1 is shown in DTG_RESET_CTL_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-805. DTG_RESET_CTL_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R/W	0x0	Reserved
2	DTG_RESET_LOCK_EN	R/W	0x1	Enable DTG reset based on FPD Lock 0: DTG reset unaffected by FPD lock 1: DTG will go into reset when lock goes low and come out of reset when lock goes high
1	DTG_RESET	R/W	0x0	Manual DTG Reset 0: Normal operation 1: DTG is reset. This re-initializes the display DTG.
0	DTG_WATCHDOG_DIS	R/W	0x0	Disable DTG Watchdog Timer If the watchdog detectes >4 missed HSYNC pulses, it resets the DTG. 0: Normal operation, watchdog enabled 1: Watchdog disabled

8.6.2.16.61 MEAS_HTOTAL_MSB_P1 Register (Address = 0x70) [Default = 0x00]

MEAS_HTOTAL_MSB_P1 is shown in MEAS_HTOTAL_MSB_P1 Register Field Descriptions.

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Table 8-806. MEAS_HTOTAL_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HTOTAL_MSB	R	0x0	Measured HTOTAL MSB

8.6.2.16.62 MEAS_HTOTAL_LSB_P1 Register (Address = 0x71) [Default = 0x00]

MEAS_HTOTAL_LSB_P1 is shown in MEAS_HTOTAL_LSB_P1 Register Field Descriptions.

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Table 8-807. MEAS_HTOTAL_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HTOTAL_LSB	R	0x0	Measured HTOTAL LSB

8.6.2.16.63 MEAS_VTOTAL_MSB_P1 Register (Address = 0x72) [Default = 0x00]

MEAS_VTOTAL_MSB_P1 is shown in MEAS_VTOTAL_MSB_P1 Register Field Descriptions.

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Table 8-808. MEAS_VTOTAL_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VTOTAL_MSB	R	0x0	Measured VTOTAL MSB

8.6.2.16.64 MEAS_VTOTAL_LSB_P1 Register (Address = 0x73) [Default = 0x00]

MEAS_VTOTAL_LSB_P1 is shown in MEAS_VTOTAL_LSB_P1 Register Field Descriptions.

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Table 8-809. MEAS_VTOTAL_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VTOTAL_LSB	R	0x0	Measured VTOTAL LSB

8.6.2.16.65 MEAS_HACTIVE_MSB_P1 Register (Address = 0x74) [Default = 0x00]

MEAS_HACTIVE_MSB_P1 is shown in MEAS_HACTIVE_MSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-810. MEAS_HACTIVE_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HACTIVE_MSB	R	0x0	Measured HACTIVE MSB

8.6.2.16.66 MEAS_HACTIVE_LSB_P1 Register (Address = 0x75) [Default = 0x00]

MEAS_HACTIVE_LSB_P1 is shown in MEAS_HACTIVE_LSB_P1 Register Field Descriptions.

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Table 8-811. MEAS_HACTIVE_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HACTIVE_LSB	R	0x0	Measured HACTIVE LSB

8.6.2.16.67 MEAS_VRES_MSB_P1 Register (Address = 0x76) [Default = 0x00]

MEAS_VRES_MSB_P1 is shown in MEAS_VRES_MSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-812. MEAS_VRES_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VRES_MSB	R	0x0	Measured VRES MSB

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8.6.2.16.68 MEAS_VRES_LSB_P1 Register (Address = 0x77) [Default = 0x00]

MEAS_VRES_LSB_P1 is shown in MEAS_VRES_LSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-813. MEAS_VRES_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VRES_LSB	R	0x0	Measured VRES LSB

8.6.2.16.69 MEAS_HSTART_MSB_P1 Register (Address = 0x78) [Default = 0x00]

MEAS_HSTART_MSB_P1 is shown in MEAS_HSTART_MSB_P1 Register Field Descriptions.

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Table 8-814. MEAS_HSTART_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HSTART_MSB	R	0x0	Measured HSTART MSB

8.6.2.16.70 MEAS_HSTART_LSB_P1 Register (Address = 0x79) [Default = 0x00]

MEAS_HSTART_LSB_P1 is shown in MEAS_HSTART_LSB_P1 Register Field Descriptions.

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Table 8-815. MEAS_HSTART_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HSTART_LSB	R	0x0	Measured HSTART LSB

8.6.2.16.71 MEAS_VSTART_MSB_P1 Register (Address = 0x7A) [Default = 0x00]

MEAS_VSTART_MSB_P1 is shown in MEAS_VSTART_MSB_P1 Register Field Descriptions.

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Table 8-816. MEAS_VSTART_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VSTART_MSB	R	0x0	Measured VSTART MSB

8.6.2.16.72 MEAS_VSTART_LSB_P1 Register (Address = 0x7B) [Default = 0x00]

MEAS_VSTART_LSB_P1 is shown in MEAS_VSTART_LSB_P1 Register Field Descriptions.

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Table 8-817. MEAS_VSTART_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VSTART_LSB	R	0x0	Measured VSTART LSB

8.6.2.16.73 MEAS_HSWIDTH_MSB_P1 Register (Address = 0x7C) [Default = 0x00]

MEAS_HSWIDTH_MSB_P1 is shown in MEAS_HSWIDTH_MSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-818. MEAS_HSWIDTH_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MEAS_HSYNC_MSB	R	0x0	Measured HSYNC MSB

8.6.2.16.74 MEAS_HSWIDTH_LSB_P1 Register (Address = 0x7D) [Default = 0x00]

MEAS_HSWIDTH_LSB_P1 is shown in MEAS_HSWIDTH_LSB_P1 Register Field Descriptions.

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Table 8-819. MEAS_HSWIDTH_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_HSYNC_LSB	R	0x0	Measured HSYNC LSB

8.6.2.16.75 MEAS_VSWIDTH_MSB_P1 Register (Address = 0x7E) [Default = 0x00]

MEAS_VSWIDTH_MSB_P1 is shown in MEAS_VSWIDTH_MSB_P1 Register Field Descriptions.

Return to the Summary Table.

Table 8-820. MEAS_VSWIDTH_MSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6:0	MEAS_VSWIDTH_MSB	R	0x0	Measured VSYNC MSB

8.6.2.16.76 MEAS_VSWIDTH_LSB_P1 Register (Address = 0x7F) [Default = 0x00]

MEAS_VSWIDTH_LSB_P1 is shown in MEAS_VSWIDTH_LSB_P1 Register Field Descriptions.

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Table 8-821. MEAS_VSWIDTH_LSB_P1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MEAS_VSWIDTH_LSB	R	0x0	Measured VSYNC LSB

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8.6.2.17 Page 23: LMS-AEQ Registers

PAGE_23 Registers lists the memory-mapped registers for the Page 23: LMS-AEQ registers. All register offset addresses not listed in PAGE_23 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-822. PAGE_23 Registers

Address	Acronym	Register Name	Section
0x1F	LMS_AEQ_INIT_7_0_CH0	LMS_AEQ_INIT_7_0_CH0	Go
0x20	LMS_AEQ_INIT_15_8_CH0	LMS_AEQ_INIT_15_8_CH0	Go
0x9F	LMS_AEQ_INIT_7_0_CH1	LMS_AEQ_INIT_7_0_CH1	Go
0xA0	LMS_AEQ_INIT_15_8_CH1	LMS_AEQ_INIT_15_8_CH1	Go

Complex bit access types are encoded to fit into small table cells. Page 23: LMS-AEQ Access Type Codes shows the codes that are used for access types in this section.

Table 8-823. Page 23: LMS-AEQ Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.17.1 LMS_AEQ_INIT_7_0_CH0 Register (Address = 0x1F) [Default = 0xFF]

LMS_AEQ_INIT_7_0_CH0 is shown in LMS_AEQ_INIT_7_0_CH0 Register Field Descriptions.

Return to the Summary Table.

Table 8-824. LMS_AEQ_INIT_7_0_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EQ_CTLE_ACC_INIT_7_0	R/W	0xFF	Initial value for EQ CTLE accumulator (Bits 7:0)

8.6.2.17.2 LMS_AEQ_INIT_15_8_CH0 Register (Address = 0x20) [Default = 0x3C]

LMS_AEQ_INIT_15_8_CH0 is shown in LMS_AEQ_INIT_15_8_CH0 Register Field Descriptions.

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Table 8-825. LMS_AEQ_INIT_15_8_CH0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EQ_CTLE_ACC_INIT_15_8	R/W	0x3C	Initial value for EQ CTLE accumulator (Bits 15:8)

8.6.2.17.3 LMS_AEQ_INIT_7_0_CH1 Register (Address = 0x9F) [Default = 0xFF]

LMS_AEQ_INIT_7_0_CH1 is shown in LMS_AEQ_INIT_7_0_CH1 Register Field Descriptions.

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Table 8-826. LMS_AEQ_INIT_7_0_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EQ_CTLE_ACC_INIT_7_0	R/W	0xFF	Initial value for EQ CTLE accumulator (Bits 7:0)

8.6.2.17.4 LMS_AEQ_INIT_15_8_CH1 Register (Address = 0xA0) [Default = 0x3C]

LMS_AEQ_INIT_15_8_CH1 is shown in LMS_AEQ_INIT_15_8_CH1 Register Field Descriptions.

Return to the Summary Table.

Table 8-827. LMS_AEQ_INIT_15_8_CH1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EQ_CTLE_ACC_INIT_15_8	R/W	0x3C	Initial value for EQ CTLE accumulator (Bits 15:8)

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8.6.2.18 Page 27: SAR ADC Registers

PAGE_27 Registers lists the memory-mapped registers for the Page 27: SAR ADC registers. All register offset addresses not listed in PAGE_27 Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-828. PAGE_27 Registers

Address	Acronym	Register Name	Section
0x4	SAR_ADC_CLK_SAMPLE_SEL	SAR_ADC_CLK_SAMPLE_SEL	Go
0x7	SAR_ADC_INPUT_EN_LSB	SAR_ADC_INPUT_EN_LSB	Go
0x8	SAR_ADC_INPUT_EN_MSB	SAR_ADC_INPUT_EN_MSB	Go
0xD	ADC_MODE	ADC_MODE	Go
0xF	ADC_SRC_CNTR_0	ADC_SRC_CNTR_0	Go
0x10	ADC_SRC_CNTR_1	ADC_SRC_CNTR_1	Go
0x11	ADC_SRC_CNTR_2	ADC_SRC_CNTR_2	Go
0x12	ADC_SRC_CNTR_3	ADC_SRC_CNTR_3	Go
0x13	TEMP_FINAL	TEMP_FINAL	Go
0x15	IV0_FINAL	IV0_FINAL	Go
0x16	IV1_FINAL	IV1_FINAL	Go
0x17	IV2_FINAL	IV2_FINAL	Go
0x18	IV3_FINAL	IV3_FINAL	Go
0x1B	EXT_VOL0_FINAL	EXT_VOL0_FINAL	Go
0x1C	EXT_VOL1_FINAL	EXT_VOL1_FINAL	Go
0x1D	LINE_FAULT0_FINAL	LINE_FAULT0_FINAL	Go
0x1E	LINE_FAULT1_FINAL	LINE_FAULT1_FINAL	Go
0x1F	LINE_FAULT2_FINAL	LINE_FAULT2_FINAL	Go
0x20	LINE_FAULT3_FINAL	LINE_FAULT3_FINAL	Go
0x23	INT_STATUS_LSB_LOW	INT_STATUS_LSB_LOW	Go
0x24	INT_STATUS_MSB_LOW	INT_STATUS_MSB_LOW	Go
0x25	INT_STATUS_LSB_HIGH	INT_STATUS_LSB_HIGH	Go
0x26	INT_STATUS_MSB_HIGH	INT_STATUS_MSB_HIGH	Go
0x27	INT_LINE_FAULT0_M0	INT_LINE_FAULT0_M0	Go
0x28	INT_LINE_FAULT1_M0	INT_LINE_FAULT1_M0	Go
0x29	INT_LINE_FAULT2_M0	INT_LINE_FAULT2_M0	Go
0x2A	INT_LINE_FAULT3_M0	INT_LINE_FAULT3_M0	Go
0x2B	INT_LINE_FAULT0_M1	INT_LINE_FAULT0_M1	Go
0x2C	INT_LINE_FAULT1_M1	INT_LINE_FAULT1_M1	Go
0x2D	INT_LINE_FAULT2_M1	INT_LINE_FAULT2_M1	Go
0x2E	INT_LINE_FAULT3_M1	INT_LINE_FAULT3_M1	Go
0x2F	INT_LINE_FAULT_UNDEF	INT_LINE_FAULT_UNDEF	Go
0x30	INT_LINE_FAULT_SATURATE	INT_LINE_FAULT_SATURATE	Go
0x33	TEMP_HIGH	TEMP_HIGH	Go
0x34	TEMP_LOW	TEMP_LOW	Go
0x35	TEMP_ADC_OFFSET	TEMP_ADC_OFFSET	Go
0x39	IV0_HIGH	IV0_HIGH	Go
0x3A	IV0_LOW	IV0_LOW	Go
0x3B	IV0_ADC_OFFSET	IV0_ADC_OFFSET	Go
0x3C	IV1_HIGH	IV1_HIGH	Go
0x3D	IV1_LOW	IV1_LOW	Go

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Table 8-828. PAGE_27 Registers (continued)

Address	Acronym	Register Name	Section
0x3E	IV1_ADC_OFFSET	IV1_ADC_OFFSET	Go
0x3F	IV2_HIGH	IV2_HIGH	Go
0x40	IV2_LOW	IV2_LOW	Go
0x41	IV2_ADC_OFFSET	IV2_ADC_OFFSET	Go
0x42	IV3_HIGH	IV3_HIGH	Go
0x43	IV3_LOW	IV3_LOW	Go
0x44	IV3_ADC_OFFSET	IV3_ADC_OFFSET	Go
0x4B	TEMP_IV_MASK	TEMP_IV_MASK	Go
0x4C	EXT_VOL0_HIGH	EXT_VOL0_HIGH	Go
0x4D	EXT_VOL0_LOW	EXT_VOL0_LOW	Go
0x4E	EXT_VOL0_ADC_OFFSET	EXT_VOL0_ADC_OFFSET	Go
0x4F	EXT_VOL1_HIGH	EXT_VOL1_HIGH	Go
0x50	EXT_VOL1_LOW	EXT_VOL1_LOW	Go
0x51	EXT_VOL1_ADC_OFFSET	EXT_VOL1_ADC_OFFSET	Go
0x52	EXT_VOL_MASK	EXT_VOL_MASK	Go
0x53	LINE_FAULT0_THRESH_0_HI_M0	LINE_FAULT0_THRESH_0_HI_M0	Go
0x54	LINE_FAULT0_THRESH_0_LO_M0	LINE_FAULT0_THRESH_0_LO_M0	Go
0x55	LINE_FAULT0_THRESH_1_HI_M0	LINE_FAULT0_THRESH_1_HI_M0	Go
0x56	LINE_FAULT0_THRESH_1_LO_M0	LINE_FAULT0_THRESH_1_LO_M0	Go
0x57	LINE_FAULT0_THRESH_2_HI_M0	LINE_FAULT0_THRESH_2_HI_M0	Go
0x58	LINE_FAULT0_THRESH_2_LO_M0	LINE_FAULT0_THRESH_2_LO_M0	Go
0x59	LINE_FAULT0_THRESH_3_HI_M0	LINE_FAULT0_THRESH_3_HI_M0	Go
0x5A	LINE_FAULT0_THRESH_3_LO_M0	LINE_FAULT0_THRESH_3_LO_M0	Go
0x5B	LINE_FAULT0_THRESH_4_HI_M0	LINE_FAULT0_THRESH_4_HI_M0	Go
0x5C	LINE_FAULT0_THRESH_4_LO_M0	LINE_FAULT0_THRESH_4_LO_M0	Go
0x5D	LINE_FAULT0_THRESH_5_HI_M0	LINE_FAULT0_THRESH_5_HI_M0	Go
0x5E	LINE_FAULT0_THRESH_5_LO_M0	LINE_FAULT0_THRESH_5_LO_M0	Go
0x5F	LINE_FAULT0_THRESH_6_HI_M0	LINE_FAULT0_THRESH_6_HI_M0	Go
0x60	LINE_FAULT0_THRESH_6_LO_M0	LINE_FAULT0_THRESH_6_LO_M0	Go
0x61	LINE_FAULT0_THRESH_7_HI_M0	LINE_FAULT0_THRESH_7_HI_M0	Go
0x62	LINE_FAULT0_THRESH_7_LO_M0	LINE_FAULT0_THRESH_7_LO_M0	Go
0x63	LINE_FAULT0_THRESH_MASK_M0	LINE_FAULT0_THRESH_MASK_M0	Go
0x64	LINE_FAULT0_ADC_OFFSET_M0	LINE_FAULT0_ADC_OFFSET_M0	Go

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Table 8-828. PAGE_27 Registers (continued)

Address	Acronym	Register Name	Section
0x65	LINE_FAULT1_THRESH_0_HI_M0	LINE_FAULT1_THRESH_0_HI_M0	Go
0x66	LINE_FAULT1_THRESH_0_LO_M0	LINE_FAULT1_THRESH_0_LO_M0	Go
0x67	LINE_FAULT1_THRESH_1_HI_M0	LINE_FAULT1_THRESH_1_HI_M0	Go
0x68	LINE_FAULT1_THRESH_1_LO_M0	LINE_FAULT1_THRESH_1_LO_M0	Go
0x69	LINE_FAULT1_THRESH_2_HI_M0	LINE_FAULT1_THRESH_2_HI_M0	Go
0x6A	LINE_FAULT1_THRESH_2_LO_M0	LINE_FAULT1_THRESH_2_LO_M0	Go
0x6B	LINE_FAULT1_THRESH_3_HI_M0	LINE_FAULT1_THRESH_3_HI_M0	Go
0x6C	LINE_FAULT1_THRESH_3_LO_M0	LINE_FAULT1_THRESH_3_LO_M0	Go
0x6D	LINE_FAULT1_THRESH_4_HI_M0	LINE_FAULT1_THRESH_4_HI_M0	Go
0x6E	LINE_FAULT1_THRESH_4_LO_M0	LINE_FAULT1_THRESH_4_LO_M0	Go
0x6F	LINE_FAULT1_THRESH_5_HI_M0	LINE_FAULT1_THRESH_5_HI_M0	Go
0x70	LINE_FAULT1_THRESH_5_LO_M0	LINE_FAULT1_THRESH_5_LO_M0	Go
0x71	LINE_FAULT1_THRESH_6_HI_M0	LINE_FAULT1_THRESH_6_HI_M0	Go
0x72	LINE_FAULT1_THRESH_6_LO_M0	LINE_FAULT1_THRESH_6_LO_M0	Go
0x73	LINE_FAULT1_THRESH_7_HI_M0	LINE_FAULT1_THRESH_7_HI_M0	Go
0x74	LINE_FAULT1_THRESH_7_LO_M0	LINE_FAULT1_THRESH_7_LO_M0	Go
0x75	LINE_FAULT1_THRESH_MASK_M0	LINE_FAULT1_THRESH_MASK_M0	Go
0x76	LINE_FAULT1_ADC_OFFSET_M0	LINE_FAULT1_ADC_OFFSET_M0	Go
0x77	LINE_FAULT2_THRESH_0_HI_M0	LINE_FAULT2_THRESH_0_HI_M0	Go
0x78	LINE_FAULT2_THRESH_0_LO_M0	LINE_FAULT2_THRESH_0_LO_M0	Go
0x79	LINE_FAULT2_THRESH_1_HI_M0	LINE_FAULT2_THRESH_1_HI_M0	Go
0x7A	LINE_FAULT2_THRESH_1_LO_M0	LINE_FAULT2_THRESH_1_LO_M0	Go
0x7B	LINE_FAULT2_THRESH_2_HI_M0	LINE_FAULT2_THRESH_2_HI_M0	Go
0x7C	LINE_FAULT2_THRESH_2_LO_M0	LINE_FAULT2_THRESH_2_LO_M0	Go
0x7D	LINE_FAULT2_THRESH_3_HI_M0	LINE_FAULT2_THRESH_3_HI_M0	Go
0x7E	LINE_FAULT2_THRESH_3_LO_M0	LINE_FAULT2_THRESH_3_LO_M0	Go
0x7F	LINE_FAULT2_THRESH_4_HI_M0	LINE_FAULT2_THRESH_4_HI_M0	Go

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Table 8-828. PAGE_27 Registers (continued)

Address	Acronym	Register Name	Section
0x80	LINE_FAULT2_THRESH_4_LO_M0	LINE_FAULT2_THRESH_4_LO_M0	Go
0x81	LINE_FAULT2_THRESH_5_HI_M0	LINE_FAULT2_THRESH_5_HI_M0	Go
0x82	LINE_FAULT2_THRESH_5_LO_M0	LINE_FAULT2_THRESH_5_LO_M0	Go
0x83	LINE_FAULT2_THRESH_6_HI_M0	LINE_FAULT2_THRESH_6_HI_M0	Go
0x84	LINE_FAULT2_THRESH_6_LO_M0	LINE_FAULT2_THRESH_6_LO_M0	Go
0x85	LINE_FAULT2_THRESH_7_HI_M0	LINE_FAULT2_THRESH_7_HI_M0	Go
0x86	LINE_FAULT2_THRESH_7_LO_M0	LINE_FAULT2_THRESH_7_LO_M0	Go
0x87	LINE_FAULT2_THRESH_MASK_M0	LINE_FAULT2_THRESH_MASK_M0	Go
0x88	LINE_FAULT2_ADC_OFFSET_M0	LINE_FAULT2_ADC_OFFSET_M0	Go
0x89	LINE_FAULT3_THRESH_0_HI_M0	LINE_FAULT3_THRESH_0_HI_M0	Go
0x8A	LINE_FAULT3_THRESH_0_LO_M0	LINE_FAULT3_THRESH_0_LO_M0	Go
0x8B	LINE_FAULT3_THRESH_1_HI_M0	LINE_FAULT3_THRESH_1_HI_M0	Go
0x8C	LINE_FAULT3_THRESH_1_LO_M0	LINE_FAULT3_THRESH_1_LO_M0	Go
0x8D	LINE_FAULT3_THRESH_2_HI_M0	LINE_FAULT3_THRESH_2_HI_M0	Go
0x8E	LINE_FAULT3_THRESH_2_LO_M0	LINE_FAULT3_THRESH_2_LO_M0	Go
0x8F	LINE_FAULT3_THRESH_3_HI_M0	LINE_FAULT3_THRESH_3_HI_M0	Go
0x90	LINE_FAULT3_THRESH_3_LO_M0	LINE_FAULT3_THRESH_3_LO_M0	Go
0x91	LINE_FAULT3_THRESH_4_HI_M0	LINE_FAULT3_THRESH_4_HI_M0	Go
0x92	LINE_FAULT3_THRESH_4_LO_M0	LINE_FAULT3_THRESH_4_LO_M0	Go
0x93	LINE_FAULT3_THRESH_5_HI_M0	LINE_FAULT3_THRESH_5_HI_M0	Go
0x94	LINE_FAULT3_THRESH_5_LO_M0	LINE_FAULT3_THRESH_5_LO_M0	Go
0x95	LINE_FAULT3_THRESH_6_HI_M0	LINE_FAULT3_THRESH_6_HI_M0	Go
0x96	LINE_FAULT3_THRESH_6_LO_M0	LINE_FAULT3_THRESH_6_LO_M0	Go
0x97	LINE_FAULT3_THRESH_7_HI_M0	LINE_FAULT3_THRESH_7_HI_M0	Go
0x98	LINE_FAULT3_THRESH_7_LO_M0	LINE_FAULT3_THRESH_7_LO_M0	Go
0x99	LINE_FAULT3_THRESH_MASK_M0	LINE_FAULT3_THRESH_MASK_M0	Go
0x9A	LINE_FAULT3_ADC_OFFSET_M0	LINE_FAULT3_ADC_OFFSET_M0	Go

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Table 8-828. PAGE_27 Registers (continued)

Address	Acronym	Register Name	Section
0x9B	LINE_FAULT0_THRESH_0_HI_M1	LINE_FAULT0_THRESH_0_HI_M1	Go
0x9C	LINE_FAULT0_THRESH_0_LO_M1	LINE_FAULT0_THRESH_0_LO_M1	Go
0x9D	LINE_FAULT0_THRESH_1_HI_M1	LINE_FAULT0_THRESH_1_HI_M1	Go
0x9E	LINE_FAULT0_THRESH_1_LO_M1	LINE_FAULT0_THRESH_1_LO_M1	Go
0x9F	LINE_FAULT0_THRESH_2_HI_M1	LINE_FAULT0_THRESH_2_HI_M1	Go
0xA0	LINE_FAULT0_THRESH_2_LO_M1	LINE_FAULT0_THRESH_2_LO_M1	Go
0xA1	LINE_FAULT0_THRESH_3_HI_M1	LINE_FAULT0_THRESH_3_HI_M1	Go
0xA2	LINE_FAULT0_THRESH_3_LO_M1	LINE_FAULT0_THRESH_3_LO_M1	Go
0xA3	LINE_FAULT0_THRESH_4_HI_M1	LINE_FAULT0_THRESH_4_HI_M1	Go
0xA4	LINE_FAULT0_THRESH_4_LO_M1	LINE_FAULT0_THRESH_4_LO_M1	Go
0xA5	LINE_FAULT0_THRESH_5_HI_M1	LINE_FAULT0_THRESH_5_HI_M1	Go
0xA6	LINE_FAULT0_THRESH_5_LO_M1	LINE_FAULT0_THRESH_5_LO_M1	Go
0xA7	LINE_FAULT0_THRESH_6_HI_M1	LINE_FAULT0_THRESH_6_HI_M1	Go
0xA8	LINE_FAULT0_THRESH_6_LO_M1	LINE_FAULT0_THRESH_6_LO_M1	Go
0xA9	LINE_FAULT0_THRESH_7_HI_M1	LINE_FAULT0_THRESH_7_HI_M1	Go
0xAA	LINE_FAULT0_THRESH_7_LO_M1	LINE_FAULT0_THRESH_7_LO_M1	Go
0xAB	LINE_FAULT0_THRESH_MASK_M1	LINE_FAULT0_THRESH_MASK_M1	Go
0xAC	LINE_FAULT0_ADC_OFFSET_M1	LINE_FAULT0_ADC_OFFSET_M1	Go
0xAD	LINE_FAULT1_THRESH_0_HI_M1	LINE_FAULT1_THRESH_0_HI_M1	Go
0xAE	LINE_FAULT1_THRESH_0_LO_M1	LINE_FAULT1_THRESH_0_LO_M1	Go
0xAF	LINE_FAULT1_THRESH_1_HI_M1	LINE_FAULT1_THRESH_1_HI_M1	Go
0xB0	LINE_FAULT1_THRESH_1_LO_M1	LINE_FAULT1_THRESH_1_LO_M1	Go
0xB1	LINE_FAULT1_THRESH_2_HI_M1	LINE_FAULT1_THRESH_2_HI_M1	Go
0xB2	LINE_FAULT1_THRESH_2_LO_M1	LINE_FAULT1_THRESH_2_LO_M1	Go
0xB3	LINE_FAULT1_THRESH_3_HI_M1	LINE_FAULT1_THRESH_3_HI_M1	Go
0xB4	LINE_FAULT1_THRESH_3_LO_M1	LINE_FAULT1_THRESH_3_LO_M1	Go
0xB5	LINE_FAULT1_THRESH_4_HI_M1	LINE_FAULT1_THRESH_4_HI_M1	Go

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Table 8-828. PAGE_27 Registers (continued)

Address	Acronym	Register Name	Section
0xB6	LINE_FAULT1_THRESH_4_LO_M1	LINE_FAULT1_THRESH_4_LO_M1	Go
0xB7	LINE_FAULT1_THRESH_5_HI_M1	LINE_FAULT1_THRESH_5_HI_M1	Go
0xB8	LINE_FAULT1_THRESH_5_LO_M1	LINE_FAULT1_THRESH_5_LO_M1	Go
0xB9	LINE_FAULT1_THRESH_6_HI_M1	LINE_FAULT1_THRESH_6_HI_M1	Go
0xBA	LINE_FAULT1_THRESH_6_LO_M1	LINE_FAULT1_THRESH_6_LO_M1	Go
0xBB	LINE_FAULT1_THRESH_7_HI_M1	LINE_FAULT1_THRESH_7_HI_M1	Go
0xBC	LINE_FAULT1_THRESH_7_LO_M1	LINE_FAULT1_THRESH_7_LO_M1	Go
0xBD	LINE_FAULT1_THRESH_MASK_M1	LINE_FAULT1_THRESH_MASK_M1	Go
0xBE	LINE_FAULT1_ADC_OFFSET_M1	LINE_FAULT1_ADC_OFFSET_M1	Go
0xBF	LINE_FAULT2_THRESH_0_HI_M1	LINE_FAULT2_THRESH_0_HI_M1	Go
0xC0	LINE_FAULT2_THRESH_0_LO_M1	LINE_FAULT2_THRESH_0_LO_M1	Go
0xC1	LINE_FAULT2_THRESH_1_HI_M1	LINE_FAULT2_THRESH_1_HI_M1	Go
0xC2	LINE_FAULT2_THRESH_1_LO_M1	LINE_FAULT2_THRESH_1_LO_M1	Go
0xC3	LINE_FAULT2_THRESH_2_HI_M1	LINE_FAULT2_THRESH_2_HI_M1	Go
0xC4	LINE_FAULT2_THRESH_2_LO_M1	LINE_FAULT2_THRESH_2_LO_M1	Go
0xC5	LINE_FAULT2_THRESH_3_HI_M1	LINE_FAULT2_THRESH_3_HI_M1	Go
0xC6	LINE_FAULT2_THRESH_3_LO_M1	LINE_FAULT2_THRESH_3_LO_M1	Go
0xC7	LINE_FAULT2_THRESH_4_HI_M1	LINE_FAULT2_THRESH_4_HI_M1	Go
0xC8	LINE_FAULT2_THRESH_4_LO_M1	LINE_FAULT2_THRESH_4_LO_M1	Go
0xC9	LINE_FAULT2_THRESH_5_HI_M1	LINE_FAULT2_THRESH_5_HI_M1	Go
0xCA	LINE_FAULT2_THRESH_5_LO_M1	LINE_FAULT2_THRESH_5_LO_M1	Go
0xCB	LINE_FAULT2_THRESH_6_HI_M1	LINE_FAULT2_THRESH_6_HI_M1	Go
0xCC	LINE_FAULT2_THRESH_6_LO_M1	LINE_FAULT2_THRESH_6_LO_M1	Go
0xCD	LINE_FAULT2_THRESH_7_HI_M1	LINE_FAULT2_THRESH_7_HI_M1	Go
0xCE	LINE_FAULT2_THRESH_7_LO_M1	LINE_FAULT2_THRESH_7_LO_M1	Go
0xCF	LINE_FAULT2_THRESH_MASK_M1	LINE_FAULT2_THRESH_MASK_M1	Go
0xD0	LINE_FAULT2_ADC_OFFSET_M1	LINE_FAULT2_ADC_OFFSET_M1	Go

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Table 8-828. PAGE_27 Registers (continued)

Address	Acronym	Register Name	Section
0xD1	LINE_FAULT3_THRESH_0_HI_M1	LINE_FAULT3_THRESH_0_HI_M1	Go
0xD2	LINE_FAULT3_THRESH_0_LO_M1	LINE_FAULT3_THRESH_0_LO_M1	Go
0xD3	LINE_FAULT3_THRESH_1_HI_M1	LINE_FAULT3_THRESH_1_HI_M1	Go
0xD4	LINE_FAULT3_THRESH_1_LO_M1	LINE_FAULT3_THRESH_1_LO_M1	Go
0xD5	LINE_FAULT3_THRESH_2_HI_M1	LINE_FAULT3_THRESH_2_HI_M1	Go
0xD6	LINE_FAULT3_THRESH_2_LO_M1	LINE_FAULT3_THRESH_2_LO_M1	Go
0xD7	LINE_FAULT3_THRESH_3_HI_M1	LINE_FAULT3_THRESH_3_HI_M1	Go
0xD8	LINE_FAULT3_THRESH_3_LO_M1	LINE_FAULT3_THRESH_3_LO_M1	Go
0xD9	LINE_FAULT3_THRESH_4_HI_M1	LINE_FAULT3_THRESH_4_HI_M1	Go
0xDA	LINE_FAULT3_THRESH_4_LO_M1	LINE_FAULT3_THRESH_4_LO_M1	Go
0xDB	LINE_FAULT3_THRESH_5_HI_M1	LINE_FAULT3_THRESH_5_HI_M1	Go
0xDC	LINE_FAULT3_THRESH_5_LO_M1	LINE_FAULT3_THRESH_5_LO_M1	Go
0xDD	LINE_FAULT3_THRESH_6_HI_M1	LINE_FAULT3_THRESH_6_HI_M1	Go
0xDE	LINE_FAULT3_THRESH_6_LO_M1	LINE_FAULT3_THRESH_6_LO_M1	Go
0xDF	LINE_FAULT3_THRESH_7_HI_M1	LINE_FAULT3_THRESH_7_HI_M1	Go
0xE0	LINE_FAULT3_THRESH_7_LO_M1	LINE_FAULT3_THRESH_7_LO_M1	Go
0xE1	LINE_FAULT3_THRESH_MASK_M1	LINE_FAULT3_THRESH_MASK_M1	Go
0xE2	LINE_FAULT3_ADC_OFFSET_M1	LINE_FAULT3_ADC_OFFSET_M1	Go
0xE3	LINE_FAULT10_PD_SEL	LINE_FAULT10_PD_SEL	Go
0xE4	LINE_FAULT32_PD_SEL	LINE_FAULT32_PD_SEL	Go
0xE6	ADC_OFFSET_POL1	ADC_OFFSET_POL1	Go
0xE7	ADC_OFFSET_POL2	ADC_OFFSET_POL2	Go

Complex bit access types are encoded to fit into small table cells. Page 27: SAR ADC Access Type Codes shows the codes that are used for access types in this section.

Table 8-829. Page 27: SAR ADC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		

Table 8-829. Page 27: SAR ADC Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

8.6.2.18.1 SAR_ADC_CLK_SAMPLE_SEL Register (Address = 0x4) [Default = 0xD0]

SAR_ADC_CLK_SAMPLE_SEL is shown in SAR_ADC_CLK_SAMPLE_SEL Register Field Descriptions.

Return to the Summary Table.

Table 8-830. SAR_ADC_CLK_SAMPLE_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	SAR_ADC_AVERAGING_SEL	R/W	0x3	Moving Average Filter Selection 00: No average 01: 2 samples 10: 4 samples 11: 8 samples (Default)
5:4	SAR_ADC_CNTRL_CLK_DIV	R/W	0x1	Clock Divider Selection 00: Divide by 1 01: Divide by 2 (Default) 10: Divide by 3 11: Divide by 4
3:0	RESERVED	R	0x0	Reserved

8.6.2.18.2 SAR_ADC_INPUT_EN_LSB Register (Address = 0x7) [Default = 0x3D]

SAR_ADC_INPUT_EN_LSB is shown in SAR_ADC_INPUT_EN_LSB Register Field Descriptions.

Return to the Summary Table.

Table 8-831. SAR_ADC_INPUT_EN_LSB Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	SAR_ADC_INPUT_EN_IV3	R/W	0x1	Enable ADC Reading of IV3 Reading of VDD11_D is stored in register 0x18.
4	SAR_ADC_INPUT_EN_IV2	R/W	0x1	Enable ADC Reading of IV2 Reading of VDD11_TX1PLL is stored in register 0x17.
3	SAR_ADC_INPUT_EN_IV1	R/W	0x1	Enable ADC Reading of IV1 Reading of VDD18_D/VDD18_CH is stored in register 0x16.
2	SAR_ADC_INPUT_EN_IV0	R/W	0x1	Enable ADC Reading of IV0 Reading of VDD18_TXPLL is stored in register 0x15.
1	RESERVED	R/W	0x0	Reserved
0	SAR_ADC_INPUT_EN_TEMP	R/W	0x1	Enable ADC Reading of Temperature Sensor Reading of junction temperature is stored in register 0x13.

8.6.2.18.3 SAR_ADC_INPUT_EN_MSB Register (Address = 0x8) [Default = 0x00]

SAR_ADC_INPUT_EN_MSB is shown in SAR_ADC_INPUT_EN_MSB Register Field Descriptions.

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Table 8-832. SAR_ADC_INPUT_EN_MSB Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	SAR_ADC_INPUT_EN_LINE_FAULT3	R/W	0x0	Enable ADC Reading of LINE_FAULT3 Reading of GPIO13 is stored in register 0x20.
4	SAR_ADC_INPUT_EN_LINE_FAULT2	R/W	0x0	Enable ADC Reading of LINE_FAULT2 Rreading of GPIO12 is stored in register 0x1F.
3	SAR_ADC_INPUT_EN_LINE_FAULT1	R/W	0x0	Enable ADC Reading of LINE_FAULT1 Reading of GPIO11 is stored in register 0x1E.
2	SAR_ADC_INPUT_EN_LINE_FAULT0	R/W	0x0	Enable ADC Reading of LINE_FAULT0 Reading of GPIO10 is stored in register 0x1D.
1	SAR_ADC_INPUT_EN_EXT_VOL1	R/W	0x0	Enable ADC Reading of EXT_VOL1 Reading of GPIO8 is stored in register 0x1C.
0	SAR_ADC_INPUT_EN_EXT_VOL0	R/W	0x0	Enable ADC Reading of EXT_VOL0 Reading of GPIO6 is stored in register 0x1B.

8.6.2.18.4 ADC_MODE Register (Address = 0xD) [Default = 0x00]

ADC_MODE is shown in ADC_MODE Register Field Descriptions.

Return to the Summary Table.

Table 8-833. ADC_MODE Register Field Descriptions

Bit	Field	Type	Default	Description
7	ADC_MANUAL_MODE	R/W	0x0	Enable the SAR ADC 0: SAR ADC is enabled 1: SAR ADC is disabled
6	RESERVED	R/W	0x0	Reserved
5:3	RESERVED	R/W	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

8.6.2.18.5 ADC_SRC_CNTR_0 Register (Address = 0xF) [Default = 0xC8]

ADC_SRC_CNTR_0 is shown in ADC_SRC_CNTR_0 Register Field Descriptions.

Return to the Summary Table.

Table 8-834. ADC_SRC_CNTR_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_SRC_CNTR_0	R/W	0xC8	Bits [7:0] of the ADC_SRC_CNTR[31:0] value Set the number of clock cycles to average for each source. (# cycles per second/number of sources enabled)

8.6.2.18.6 ADC_SRC_CNTR_1 Register (Address = 0x10) [Default = 0x32]

ADC_SRC_CNTR_1 is shown in ADC_SRC_CNTR_1 Register Field Descriptions.

Return to the Summary Table.

Table 8-835. ADC_SRC_CNTR_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_SRC_CNTR_1	R/W	0x32	Bits [15:8] of the ADC_SRC_CNTR[31:0] value Set the number of clock cycles to average for each source. (# cycles per second/number of sources enabled)

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8.6.2.18.7 ADC_SRC_CNTR_2 Register (Address = 0x11) [Default = 0x00]

ADC_SRC_CNTR_2 is shown in ADC_SRC_CNTR_2 Register Field Descriptions.

Return to the Summary Table.

Table 8-836. ADC_SRC_CNTR_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_SRC_CNTR_2	R/W	0x0	Bits [23:16] of the ADC_SRC_CNTR[31:0] value Set the number of clock cycles to average for each source. (# cycles per second/number of sources enabled)

8.6.2.18.8 ADC_SRC_CNTR_3 Register (Address = 0x12) [Default = 0x00]

ADC_SRC_CNTR_3 is shown in ADC_SRC_CNTR_3 Register Field Descriptions.

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Table 8-837. ADC_SRC_CNTR_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	ADC_SRC_CNTR_3	R/W	0x0	Bits [31:24] of the ADC_SRC_CNTR[31:0] value Set the number of clock cycles to average for each source. (# cycles per second/number of sources enabled)

8.6.2.18.9 TEMP_FINAL Register (Address = 0x13) [Default = 0x00]

TEMP_FINAL is shown in TEMP_FINAL Register Field Descriptions.

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Table 8-838. TEMP_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_FINAL	R	0x0	Holds ADC value for junction temperature of the 98x device.

8.6.2.18.10 IV0_FINAL Register (Address = 0x15) [Default = 0x00]

IV0_FINAL is shown in IV0_FINAL Register Field Descriptions.

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Table 8-839. IV0_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV0_FINAL	R	0x0	Holds ADC value of IV0_FINAL. IV0 is an internal voltage measurement of the VDD18_TXPLL pin.

8.6.2.18.11 IV1_FINAL Register (Address = 0x16) [Default = 0x00]

IV1_FINAL is shown in IV1_FINAL Register Field Descriptions.

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Table 8-840. IV1_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV1_FINAL	R	0x0	Holds ADC value of IV1_FINAL. IV1 is an internal voltage measurement of the VDD18_D/VDD18_CH pin.

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8.6.2.18.12 IV2_FINAL Register (Address = 0x17) [Default = 0x00]

IV2_FINAL is shown in IV2_FINAL Register Field Descriptions.

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Table 8-841. IV2_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV2_FINAL	R	0x0	Holds ADC value of IV2_FINAL. IV2 is an internal voltage measurement of the VDD11_TX1PLL pin.

8.6.2.18.13 IV3_FINAL Register (Address = 0x18) [Default = 0x00]

IV3_FINAL is shown in IV3_FINAL Register Field Descriptions.

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Table 8-842. IV3_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV3_FINAL	R	0x0	Holds ADC value of IV3_FINAL. IV3 is an internal voltage measurement of the VDD11_D pins.

8.6.2.18.14 EXT_VOL0_FINAL Register (Address = 0x1B) [Default = 0x00]

EXT_VOL0_FINAL is shown in EXT_VOL0_FINAL Register Field Descriptions.

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Table 8-843. EXT_VOL0_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_FINAL	R	0x0	Holds ADC value for EXT_VOL0_FINAL (GPIO6 pin).

8.6.2.18.15 EXT_VOL1_FINAL Register (Address = 0x1C) [Default = 0x00]

EXT_VOL1_FINAL is shown in EXT_VOL1_FINAL Register Field Descriptions.

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Table 8-844. EXT_VOL1_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_FINAL	R	0x0	Holds ADC value for EXT_VOL1_FINAL (GPIO8 pin).

8.6.2.18.16 LINE_FAULT0_FINAL Register (Address = 0x1D) [Default = 0x00]

LINE_FAULT0_FINAL is shown in LINE_FAULT0_FINAL Register Field Descriptions.

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Table 8-845. LINE_FAULT0_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_FINAL	R	0x0	Holds ADC value for LINE_FAULT0_FINAL (GPIO10 pin).

8.6.2.18.17 LINE_FAULT1_FINAL Register (Address = 0x1E) [Default = 0x00]

LINE_FAULT1_FINAL is shown in LINE_FAULT1_FINAL Register Field Descriptions.

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Table 8-846. LINE_FAULT1_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_FINAL	R	0x0	Holds ADC value for LINE_FAULT1_FINAL (GPIO11 pin).

8.6.2.18.18 LINE_FAULT2_FINAL Register (Address = 0x1F) [Default = 0x00]

LINE_FAULT2_FINAL is shown in LINE_FAULT2_FINAL Register Field Descriptions.

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Table 8-847. LINE_FAULT2_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_FINAL	R	0x0	Holds ADC value for LINE_FAULT2_FINAL (GPIO12 pin).

8.6.2.18.19 LINE_FAULT3_FINAL Register (Address = 0x20) [Default = 0x00]

LINE_FAULT3_FINAL is shown in LINE_FAULT3_FINAL Register Field Descriptions.

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Table 8-848. LINE_FAULT3_FINAL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_FINAL	R	0x0	Holds ADC value for LINE_FAULT3_FINAL (GPIO13 pin).

8.6.2.18.20 INT_STATUS_LSB_LOW Register (Address = 0x23) [Default = 0x00]

INT_STATUS_LSB_LOW is shown in INT_STATUS_LSB_LOW Register Field Descriptions.

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Table 8-849. INT_STATUS_LSB_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	INT_STATUS_LOW_IV3	R	0x0	Interrupt status of IV3 if the value is below the set threshold
4	INT_STATUS_LOW_IV2	R	0x0	Interrupt status of IV2 if the value is below the set threshold
3	INT_STATUS_LOW_IV1	R	0x0	Interrupt status of IV1 if the value is below the set threshold
2	INT_STATUS_LOW_IV0	R	0x0	Interrupt status of IV0 if the value is below the set threshold
1	RESERVED	R	0x0	Reserved
0	INT_STATUS_LOW_TEMP	R	0x0	Interrupt status of temperature if the value is below the set threshold

8.6.2.18.21 INT_STATUS_MSB_LOW Register (Address = 0x24) [Default = 0x00]

INT_STATUS_MSB_LOW is shown in INT_STATUS_MSB_LOW Register Field Descriptions.

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Table 8-850. INT_STATUS_MSB_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	INT_STATUS_EXT_VOL1	R	0x0	Interrupt status for EXT_VOL1 if the value is below the set threshold
0	INT_STATUS_EXT_VOL0	R	0x0	Interrupt status for EXT_VOL0 if the value is below the set threshold

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8.6.2.18.22 INT_STATUS_LSB_HIGH Register (Address = 0x25) [Default = 0x00]

INT_STATUS_LSB_HIGH is shown in INT_STATUS_LSB_HIGH Register Field Descriptions.

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Table 8-851. INT_STATUS_LSB_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	INT_STATUS_HIGH_IV3	R	0x0	Interrupt status of IV3 if the value is above the set threshold
4	INT_STATUS_HIGH_IV2	R	0x0	Interrupt status of IV2 if the value is above the set threshold
3	INT_STATUS_HIGH_IV1	R	0x0	Interrupt status of IV1 if the value is above the set threshold
2	INT_STATUS_HIGH_IV0	R	0x0	Interrupt status of IV0 if the value is above the set threshold
1	RESERVED	R	0x0	Reserved
0	INT_STATUS_HIGH_TEMP	R	0x0	Interrupt status of temperature if the value is above the set threshold

8.6.2.18.23 INT_STATUS_MSB_HIGH Register (Address = 0x26) [Default = 0x00]

INT_STATUS_MSB_HIGH is shown in INT_STATUS_MSB_HIGH Register Field Descriptions.

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Table 8-852. INT_STATUS_MSB_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	INT_STATUS_HIGH_EXT_VOL1	R	0x0	Interrupt status for EXT_VOL1 if the value is above the set threshold
0	INT_STATUS_HIGH_EXT_VOL0	R	0x0	Interrupt status for EXT_VOL0 if the value is above the set threshold

8.6.2.18.24 INT_LINE_FAULT0_M0 Register (Address = 0x27) [Default = 0x00]

INT_LINE_FAULT0_M0 is shown in INT_LINE_FAULT0_M0 Register Field Descriptions.

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Table 8-853. INT_LINE_FAULT0_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	INT_LINE_FAULT0_M0	R	0x0	Interrupt status of LINE_FAULT0 in Mode 0 (Normal Mode) 00001: Short to ground (Threshold 0) 00010: Normal operation (Threshold 1) 00100: Short to 1.1V (Threshold 2) 01000: Short to 1.8V (Threshold 3) 10000: Short to 3.3V (Threshold 4)

8.6.2.18.25 INT_LINE_FAULT1_M0 Register (Address = 0x28) [Default = 0x00]

INT_LINE_FAULT1_M0 is shown in INT_LINE_FAULT1_M0 Register Field Descriptions.

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Table 8-854. INT_LINE_FAULT1_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved

Table 8-854. INT_LINE_FAULT1_M0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:0	INT_LINE_FAULT1_M0	R	0x0	Interrupt status of LINE_FAULT1 in Mode 0 (Normal Mode) 00001: Short to ground (Threshold 0) 00010: Normal operation (Threshold 1) 00100: Short to 1.1V (Threshold 2) 01000: Short to 1.8V (Threshold 3) 10000: Short to 3.3V (Threshold 4)

8.6.2.18.26 INT_LINE_FAULT2_M0 Register (Address = 0x29) [Default = 0x00]

INT_LINE_FAULT2_M0 is shown in INT_LINE_FAULT2_M0 Register Field Descriptions.

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Table 8-855. INT_LINE_FAULT2_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	INT_LINE_FAULT2_M0	R	0x0	Interrupt status of LINE_FAULT2 in Mode 0 (Normal Mode) 00001: Short to ground (Threshold 0) 00010: Normal operation (Threshold 1) 00100: Short to 1.1V (Threshold 2) 01000: Short to 1.8V (Threshold 3) 10000: Short to 3.3V (Threshold 4)

8.6.2.18.27 INT_LINE_FAULT3_M0 Register (Address = 0x2A) [Default = 0x00]

INT_LINE_FAULT3_M0 is shown in INT_LINE_FAULT3_M0 Register Field Descriptions.

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Table 8-856. INT_LINE_FAULT3_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	INT_LINE_FAULT3_M0	R	0x0	Interrupt status of LINE_FAULT3 in Mode 0 (Normal Mode) 00001: Short to ground (Threshold 0) 00010: Normal operation (Threshold 1) 00100: Short to 1.1V (Threshold 2) 01000: Short to 1.8V (Threshold 3) 10000: Short to 3.3V (Threshold 4)

8.6.2.18.28 INT_LINE_FAULT0_M1 Register (Address = 0x2B) [Default = 0x00]

INT_LINE_FAULT0_M1 is shown in INT_LINE_FAULT0_M1 Register Field Descriptions.

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Table 8-857. INT_LINE_FAULT0_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	INT_LINE_FAULT0_M1	R	0x0	Interrupt status of LINE_FAULT0 in Mode 1 (Divide-By-2 Mode) 00001: Short to ground (Threshold 0) 00010: Normal operation (Threshold 1) 00100: Short to 1.1V (Threshold 2) 01000: Short to 1.8V (Threshold 3) 10000: Short to 3.3V (Threshold 4)

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8.6.2.18.29 INT_LINE_FAULT1_M1 Register (Address = 0x2C) [Default = 0x00]

INT_LINE_FAULT1_M1 is shown in INT_LINE_FAULT1_M1 Register Field Descriptions.

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Table 8-858. INT_LINE_FAULT1_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	INT_LINE_FAULT1_M1	R	0x0	Interrupt status of LINE_FAULT1 in Mode 1 (Divide-By-2 Mode) 00001: Short to ground (Threshold 0) 00010: Normal operation (Threshold 1) 00100: Short to 1.1V (Threshold 2) 01000: Short to 1.8V (Threshold 3) 10000: Short to 3.3V (Threshold 4)

8.6.2.18.30 INT_LINE_FAULT2_M1 Register (Address = 0x2D) [Default = 0x00]

INT_LINE_FAULT2_M1 is shown in INT_LINE_FAULT2_M1 Register Field Descriptions.

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Table 8-859. INT_LINE_FAULT2_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	INT_LINE_FAULT2_M1	R	0x0	Interrupt status of LINE_FAULT2 in Mode 1 (Divide-By-2 Mode) 00001: Short to ground (Threshold 0) 00010: Normal operation (Threshold 1) 00100: Short to 1.1V (Threshold 2) 01000: Short to 1.8V (Threshold 3) 10000: Short to 3.3V (Threshold 4)

8.6.2.18.31 INT_LINE_FAULT3_M1 Register (Address = 0x2E) [Default = 0x00]

INT_LINE_FAULT3_M1 is shown in INT_LINE_FAULT3_M1 Register Field Descriptions.

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Table 8-860. INT_LINE_FAULT3_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	INT_LINE_FAULT3_M1	R	0x0	Interrupt status of LINE_FAULT3 in Mode 1 (Divide-By-2 Mode) 00001: Short to ground (Threshold 0) 00010: Normal operation (Threshold 1) 00100: Short to 1.1V (Threshold 2) 01000: Short to 1.8V (Threshold 3) 10000: Short to 3.3V (Threshold 4)

8.6.2.18.32 INT_LINE_FAULT_UNDEF Register (Address = 0x2F) [Default = 0x00]

INT_LINE_FAULT_UNDEF is shown in INT_LINE_FAULT_UNDEF Register Field Descriptions.

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Table 8-861. INT_LINE_FAULT_UNDEF Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	INT_LINE_FAULT_UNDEF_M1	R	0x0	Interrupt status to indicate that the sensed voltage is in an undefined threshold range for Mode 1 0000: Line Fault 0 0001: Line Fault 1 0010: Line Fault 2 0011: Line fault 3
3:0	INT_LINE_FAULT_UNDEF_M0	R	0x0	Interrupt status to indicate that the sensed voltage is in an undefined threshold range for Mode 0 0000: Line Fault 0 0001: Line Fault 1 0010: Line Fault 2 0011: Line fault 3

8.6.2.18.33 INT_LINE_FAULT_SATURATE Register (Address = 0x30) [Default = 0x00]

INT_LINE_FAULT_SATURATE is shown in INT_LINE_FAULT_SATURATE Register Field Descriptions.

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Table 8-862. INT_LINE_FAULT_SATURATE Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3	INT_LINE_FAULT3_SATURATE	R	0x0	Indicates the ADC code for Line Fault 3 is saturated and the voltage sensed is beyond the ADC range
2	INT_LINE_FAULT2_SATURATE	R	0x0	Indicates the ADC code for Line Fault 2 is saturated and the voltage sensed is beyond the ADC range
1	INT_LINE_FAULT1_SATURATE	R	0x0	Indicates the ADC code for Line Fault 1 is saturated and the voltage sensed is beyond the ADC range
0	INT_LINE_FAULT0_SATURATE	R	0x0	Indicates the ADC code for Line Fault 0 is saturated and the voltage sensed is beyond the ADC range

8.6.2.18.34 TEMP_HIGH Register (Address = 0x33) [Default = 0xCE]

TEMP_HIGH is shown in TEMP_HIGH Register Field Descriptions.

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Table 8-863. TEMP_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_HIGH	R/W	0xCE	Upper threshold for Temperature Sensing interrupt.

8.6.2.18.35 TEMP_LOW Register (Address = 0x34) [Default = 0x7E]

TEMP_LOW is shown in TEMP_LOW Register Field Descriptions.

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Table 8-864. TEMP_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_LOW	R/W	0x7E	Lower threshold for Temperature Sensing interrupt.

8.6.2.18.36 TEMP_ADC_OFFSET Register (Address = 0x35) [Default = 0x00]

TEMP_ADC_OFFSET is shown in TEMP_ADC_OFFSET Register Field Descriptions.

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Table 8-865. TEMP_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TEMP_ADC_OFFSET	R/W	0x0	Offset added to the TEMP_FINAL ADC code after the conversion

8.6.2.18.37 IV0_HIGH Register (Address = 0x39) [Default = 0x86]

IV0_HIGH is shown in IV0_HIGH Register Field Descriptions.

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Table 8-866. IV0_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV0_HIGH	R/W	0x86	Upper threshold for IV0 (VDD18_TXPLL pin).

8.6.2.18.38 IV0_LOW Register (Address = 0x3A) [Default = 0x7A]

IV0_LOW is shown in IV0_LOW Register Field Descriptions.

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Table 8-867. IV0_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV0_LOW	R/W	0x7A	Lower threshold for IV0 (VDD18_TXPLL pin).

8.6.2.18.39 IV0_ADC_OFFSET Register (Address = 0x3B) [Default = 0x00]

IV0_ADC_OFFSET is shown in IV0_ADC_OFFSET Register Field Descriptions.

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Table 8-868. IV0_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV0_ADC_OFFSET	R/W	0x0	Offset added to the IV0_FINAL ADC code after the conversion

8.6.2.18.40 IV1_HIGH Register (Address = 0x3C) [Default = 0x86]

IV1_HIGH is shown in IV1_HIGH Register Field Descriptions.

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Table 8-869. IV1_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV1_HIGH	R/W	0x86	Upper threshold for IV1 (VDD18_D/VDD18_CH pin).

8.6.2.18.41 IV1_LOW Register (Address = 0x3D) [Default = 0x7A]

IV1_LOW is shown in IV1_LOW Register Field Descriptions.

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Table 8-870. IV1_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV1_LOW	R/W	0x7A	Lower threshold for IV1 (VDD18_D/VDD18_CH pin).

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8.6.2.18.42 IV1_ADC_OFFSET Register (Address = 0x3E) [Default = 0x00]

IV1_ADC_OFFSET is shown in IV1_ADC_OFFSET Register Field Descriptions.

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Table 8-871. IV1_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV1_ADC_OFFSET	R/W	0x0	Offset added to the IV1_FINAL ADC code after the conversion

8.6.2.18.43 IV2_HIGH Register (Address = 0x3F) [Default = 0x86]

IV2_HIGH is shown in IV2_HIGH Register Field Descriptions.

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Table 8-872. IV2_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV2_HIGH	R/W	0x86	Upper threshold for IV2 (VDD11_TX1PLL pin).

8.6.2.18.44 IV2_LOW Register (Address = 0x40) [Default = 0x7A]

IV2_LOW is shown in IV2_LOW Register Field Descriptions.

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Table 8-873. IV2_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV2_LOW	R/W	0x7A	Lower threshold for IV2 (VDD11_TX1PLL pin).

8.6.2.18.45 IV2_ADC_OFFSET Register (Address = 0x41) [Default = 0x00]

IV2_ADC_OFFSET is shown in IV2_ADC_OFFSET Register Field Descriptions.

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Table 8-874. IV2_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV2_ADC_OFFSET	R/W	0x0	Offset added to the IV2_FINAL ADC code after the conversion

8.6.2.18.46 IV3_HIGH Register (Address = 0x42) [Default = 0x86]

IV3_HIGH is shown in IV3_HIGH Register Field Descriptions.

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Table 8-875. IV3_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV3_HIGH	R/W	0x86	Upper threshold for IV3 (VDD11_D pin).

8.6.2.18.47 IV3_LOW Register (Address = 0x43) [Default = 0x7A]

IV3_LOW is shown in IV3_LOW Register Field Descriptions.

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Table 8-876. IV3_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV3_LOW	R/W	0x7A	Lower threshold for IV3 (VDD11_D pin).

8.6.2.18.48 IV3_ADC_OFFSET Register (Address = 0x44) [Default = 0x00]

IV3_ADC_OFFSET is shown in IV3_ADC_OFFSET Register Field Descriptions.

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Table 8-877. IV3_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IV3_ADC_OFFSET	R/W	0x0	Offset added to the IV3_FINAL ADC code after the conversion

8.6.2.18.49 TEMP_IV_MASK Register (Address = 0x4B) [Default = 0xC2]

TEMP_IV_MASK is shown in TEMP_IV_MASK Register Field Descriptions.

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Table 8-878. TEMP_IV_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x1	Reserved
5	IV3_THRESH_MASK	R/W	0x0	IV3 Threshold Mask 0: Do not mask threshold interrupts on IV3 (Allow threshold interrupts to occur for IV3) 1: Mask threshold interrupts on IV3
4	IV2_THRESH_MASK	R/W	0x0	IV2 Threshold Mask 0: Do not mask threshold interrupts on IV2 (Allow threshold interrupts to occur for IV2) 1: Mask threshold interrupts on IV2
3	IV1_THRESH_MASK	R/W	0x0	IV1 Threshold Mask 0: Do not mask threshold interrupts on IV1 (Allow threshold interrupts to occur for IV1) 1: Mask threshold interrupts on IV1
2	IV0_THRESH_MASK	R/W	0x0	IV0 Threshold Mask 0: Do not mask threshold interrupts on IV0 (Allow threshold interrupts to occur for IV0) 1: Mask threshold interrupts on IV0
1	RESERVED	R/W	0x1	Reserved
0	TEMP_THRESH_MASK	R/W	0x0	Temperature Threshold Mask 0: Do not mask temperature threshold interrupts (Allow temperature threshold interrupts to occur) 1: Mask temperature threshold interrupts

8.6.2.18.50 EXT_VOL0_HIGH Register (Address = 0x4C) [Default = 0x00]

EXT_VOL0_HIGH is shown in EXT_VOL0_HIGH Register Field Descriptions.

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Table 8-879. EXT_VOL0_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_HIGH	R/W	0x0	Upper threshold for EXT_VOL0 (GPIO6 pin).

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8.6.2.18.51 EXT_VOL0_LOW Register (Address = 0x4D) [Default = 0x00]

EXT_VOL0_LOW is shown in EXT_VOL0_LOW Register Field Descriptions.

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Table 8-880. EXT_VOL0_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_LOW	R/W	0x0	Lower threshold for EXT_VOL0 (GPIO6 pin).

8.6.2.18.52 EXT_VOL0_ADC_OFFSET Register (Address = 0x4E) [Default = 0x00]

EXT_VOL0_ADC_OFFSET is shown in EXT_VOL0_ADC_OFFSET Register Field Descriptions.

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Table 8-881. EXT_VOL0_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL0_ADC_OFFSET	R/W	0x0	Offset added to the EXT_VOL0_FINAL ADC code after conversion

8.6.2.18.53 EXT_VOL1_HIGH Register (Address = 0x4F) [Default = 0x00]

EXT_VOL1_HIGH is shown in EXT_VOL1_HIGH Register Field Descriptions.

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Table 8-882. EXT_VOL1_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_HIGH	R/W	0x0	Upper threshold for EXT_VOL1 (GPIO8 pin).

8.6.2.18.54 EXT_VOL1_LOW Register (Address = 0x50) [Default = 0x00]

EXT_VOL1_LOW is shown in EXT_VOL1_LOW Register Field Descriptions.

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Table 8-883. EXT_VOL1_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_LOW	R/W	0x0	Lower threshold for EXT_VOL1 (GPIO8 pin).

8.6.2.18.55 EXT_VOL1_ADC_OFFSET Register (Address = 0x51) [Default = 0x00]

EXT_VOL1_ADC_OFFSET is shown in EXT_VOL1_ADC_OFFSET Register Field Descriptions.

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Table 8-884. EXT_VOL1_ADC_OFFSET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	EXT_VOL1_ADC_OFFSET	R/W	0x0	Offset added to the EXT_VOL1_FINAL ADC code after conversion

8.6.2.18.56 EXT_VOL_MASK Register (Address = 0x52) [Default = 0x00]

EXT_VOL_MASK is shown in EXT_VOL_MASK Register Field Descriptions.

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Table 8-885. EXT_VOL_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	EXT_VOL1_THRESH_MASK	R/W	0x0	EXT_VOL1 Threshold Mask 0: Do not mask threshold interrupts on EXT_VOL1 (Allow threshold interrupts to occur for EXT_VOL1) 1: Mask threshold interrupts on EXT_VOL1
0	EXT_VOL0_THRESH_MASK	R/W	0x0	EXT_VOL0 Threshold Mask 0: Do not mask threshold interrupts on EXT_VOL0 (Allow threshold interrupts to occur for EXT_VOL0) 1: Mask threshold interrupts on EXT_VOL0

8.6.2.18.57 LINE_FAULT0_THRESH_0_HI_M0 Register (Address = 0x53) [Default = 0xAD]

LINE_FAULT0_THRESH_0_HI_M0 is shown in LINE_FAULT0_THRESH_0_HI_M0 Register Field Descriptions.

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Table 8-886. LINE_FAULT0_THRESH_0_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_0_HI_M0	R/W	0xAD	Holds Upper threshold voltage for LF condition 0 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.58 LINE_FAULT0_THRESH_0_LO_M0 Register (Address = 0x54) [Default = 0x72]

LINE_FAULT0_THRESH_0_LO_M0 is shown in LINE_FAULT0_THRESH_0_LO_M0 Register Field Descriptions.

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Table 8-887. LINE_FAULT0_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_0_LO_M0	R/W	0x72	Holds Lower threshold voltage for LF condition 0 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.59 LINE_FAULT0_THRESH_1_HI_M0 Register (Address = 0x55) [Default = 0xDC]

LINE_FAULT0_THRESH_1_HI_M0 is shown in LINE_FAULT0_THRESH_1_HI_M0 Register Field Descriptions.

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Table 8-888. LINE_FAULT0_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_1_HI_M0	R/W	0xDC	Holds Upper threshold voltage for LF condition 1 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.60 LINE_FAULT0_THRESH_1_LO_M0 Register (Address = 0x56) [Default = 0xCD]

LINE_FAULT0_THRESH_1_LO_M0 is shown in LINE_FAULT0_THRESH_1_LO_M0 Register Field Descriptions.

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Table 8-889. LINE_FAULT0_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_1_LO_M0	R/W	0xCD	Holds Lower threshold voltage for LF condition 1 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.61 LINE_FAULT0_THRESH_2_HI_M0 Register (Address = 0x57) [Default = 0xF8]

LINE_FAULT0_THRESH_2_HI_M0 is shown in LINE_FAULT0_THRESH_2_HI_M0 Register Field Descriptions.

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Table 8-890. LINE_FAULT0_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_2_HI_M0	R/W	0xF8	Holds Upper threshold voltage for LF condition 2 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.62 LINE_FAULT0_THRESH_2_LO_M0 Register (Address = 0x58) [Default = 0xE6]

LINE_FAULT0_THRESH_2_LO_M0 is shown in LINE_FAULT0_THRESH_2_LO_M0 Register Field Descriptions.

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Table 8-891. LINE_FAULT0_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_2_LO_M0	R/W	0xE6	Holds Lower threshold voltage for LF condition 2 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.63 LINE_FAULT0_THRESH_3_HI_M0 Register (Address = 0x59) [Default = 0x00]

LINE_FAULT0_THRESH_3_HI_M0 is shown in LINE_FAULT0_THRESH_3_HI_M0 Register Field Descriptions.

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Table 8-892. LINE_FAULT0_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_3_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 3 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.64 LINE_FAULT0_THRESH_3_LO_M0 Register (Address = 0x5A) [Default = 0x00]

LINE_FAULT0_THRESH_3_LO_M0 is shown in LINE_FAULT0_THRESH_3_LO_M0 Register Field Descriptions.

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Table 8-893. LINE_FAULT0_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_3_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 3 at LF sensing node 0 (LINE_FAULT0) in Mode 0

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8.6.2.18.65 LINE_FAULT0_THRESH_4_HI_M0 Register (Address = 0x5B) [Default = 0x00]

LINE_FAULT0_THRESH_4_HI_M0 is shown in LINE_FAULT0_THRESH_4_HI_M0 Register Field Descriptions.

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Table 8-894. LINE_FAULT0_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_4_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 4 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.66 LINE_FAULT0_THRESH_4_LO_M0 Register (Address = 0x5C) [Default = 0x00]

LINE_FAULT0_THRESH_4_LO_M0 is shown in LINE_FAULT0_THRESH_4_LO_M0 Register Field Descriptions.

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Table 8-895. LINE_FAULT0_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_4_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 4 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.67 LINE_FAULT0_THRESH_5_HI_M0 Register (Address = 0x5D) [Default = 0x00]

LINE_FAULT0_THRESH_5_HI_M0 is shown in LINE_FAULT0_THRESH_5_HI_M0 Register Field Descriptions.

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Table 8-896. LINE_FAULT0_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_5_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 5 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.68 LINE_FAULT0_THRESH_5_LO_M0 Register (Address = 0x5E) [Default = 0x00]

LINE_FAULT0_THRESH_5_LO_M0 is shown in LINE_FAULT0_THRESH_5_LO_M0 Register Field Descriptions.

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Table 8-897. LINE_FAULT0_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_5_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 5 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.69 LINE_FAULT0_THRESH_6_HI_M0 Register (Address = 0x5F) [Default = 0x00]

LINE_FAULT0_THRESH_6_HI_M0 is shown in LINE_FAULT0_THRESH_6_HI_M0 Register Field Descriptions.

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Table 8-898. LINE_FAULT0_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_6_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 6 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.70 LINE_FAULT0_THRESH_6_LO_M0 Register (Address = 0x60) [Default = 0x00]

LINE_FAULT0_THRESH_6_LO_M0 is shown in LINE_FAULT0_THRESH_6_LO_M0 Register Field Descriptions.

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Table 8-899. LINE_FAULT0_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_6_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 6 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.71 LINE_FAULT0_THRESH_7_HI_M0 Register (Address = 0x61) [Default = 0x00]

LINE_FAULT0_THRESH_7_HI_M0 is shown in LINE_FAULT0_THRESH_7_HI_M0 Register Field Descriptions.

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Table 8-900. LINE_FAULT0_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_7_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 7 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.72 LINE_FAULT0_THRESH_7_LO_M0 Register (Address = 0x62) [Default = 0x00]

LINE_FAULT0_THRESH_7_LO_M0 is shown in LINE_FAULT0_THRESH_7_LO_M0 Register Field Descriptions.

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Table 8-901. LINE_FAULT0_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_7_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 7 at LF sensing node 0 (LINE_FAULT0) in Mode 0

8.6.2.18.73 LINE_FAULT0_THRESH_MASK_M0 Register (Address = 0x63) [Default = 0xF8]

LINE_FAULT0_THRESH_MASK_M0 is shown in LINE_FAULT0_THRESH_MASK_M0 Register Field Descriptions.

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Table 8-902. LINE_FAULT0_THRESH_MASK_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT0_THRESH_7_MASK_M0	R/W	0x1	Line Fault 0 Threshold 7 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_7_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_7_HI/LO_M0 interrupt

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Table 8-902. LINE_FAULT0_THRESH_MASK_M0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	LINE_FAULT0_THRESH_6_MASK_M0	R/W	0x1	Line Fault 0 Threshold 6 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_6_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_6_HI/LO_M0 interrupt
5	LINE_FAULT0_THRESH_5_MASK_M0	R/W	0x1	Line Fault 0 Threshold 5 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_5_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_5_HI/LO_M0 interrupt
4	LINE_FAULT0_THRESH_4_MASK_M0	R/W	0x1	Line Fault 0 Threshold 4 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_4_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_4_HI/LO_M0 interrupt
3	LINE_FAULT0_THRESH_3_MASK_M0	R/W	0x1	Line Fault 0 Threshold 3 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_3_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_3_HI/LO_M0 interrupt
2	LINE_FAULT0_THRESH_2_MASK_M0	R/W	0x0	Line Fault 0 Threshold 2 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_2_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_2_HI/LO_M0 interrupt
1	LINE_FAULT0_THRESH_1_MASK_M0	R/W	0x0	Line Fault 0 Threshold 1 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_1_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_1_HI/LO_M0 interrupt
0	LINE_FAULT0_THRESH_0_MASK_M0	R/W	0x0	Line Fault 0 Threshold 0 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_0_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_0_HI/LO_M0 interrupt

8.6.2.18.74 LINE_FAULT0_ADC_OFFSET_M0 Register (Address = 0x64) [Default = 0x00]

LINE_FAULT0_ADC_OFFSET_M0 is shown in LINE_FAULT0_ADC_OFFSET_M0 Register Field Descriptions.

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Table 8-903. LINE_FAULT0_ADC_OFFSET_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_ADC_OFFSET_M0	R/W	0x0	Offset value added to LINE_FAULT0_FINAL ADC code after the ADC conversion (sensed voltage at node to ADC code). This value is for LF sensing node 0 (in Mode 0).

8.6.2.18.75 LINE_FAULT1_THRESH_0_HI_M0 Register (Address = 0x65) [Default = 0x0B]

LINE_FAULT1_THRESH_0_HI_M0 is shown in LINE_FAULT1_THRESH_0_HI_M0 Register Field Descriptions.

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Table 8-904. LINE_FAULT1_THRESH_0_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_0_HI_M0	R/W	0xB	Holds Upper threshold voltage for LF condition 0 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.76 LINE_FAULT1_THRESH_0_LO_M0 Register (Address = 0x66) [Default = 0x00]

LINE_FAULT1_THRESH_0_LO_M0 is shown in LINE_FAULT1_THRESH_0_LO_M0 Register Field Descriptions.

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Table 8-905. LINE_FAULT1_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_0_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 0 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.77 LINE_FAULT1_THRESH_1_HI_M0 Register (Address = 0x67) [Default = 0xE9]

LINE_FAULT1_THRESH_1_HI_M0 is shown in LINE_FAULT1_THRESH_1_HI_M0 Register Field Descriptions.

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Table 8-906. LINE_FAULT1_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_1_HI_M0	R/W	0xE9	Holds Upper threshold voltage for LF condition 1 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.78 LINE_FAULT1_THRESH_1_LO_M0 Register (Address = 0x68) [Default = 0x60]

LINE_FAULT1_THRESH_1_LO_M0 is shown in LINE_FAULT1_THRESH_1_LO_M0 Register Field Descriptions.

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Table 8-907. LINE_FAULT1_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_1_LO_M0	R/W	0x60	Holds Lower threshold voltage for LF condition 1 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.79 LINE_FAULT1_THRESH_2_HI_M0 Register (Address = 0x69) [Default = 0x00]

LINE_FAULT1_THRESH_2_HI_M0 is shown in LINE_FAULT1_THRESH_2_HI_M0 Register Field Descriptions.

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Table 8-908. LINE_FAULT1_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_2_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 2 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.80 LINE_FAULT1_THRESH_2_LO_M0 Register (Address = 0x6A) [Default = 0x00]

LINE_FAULT1_THRESH_2_LO_M0 is shown in LINE_FAULT1_THRESH_2_LO_M0 Register Field Descriptions.

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Table 8-909. LINE_FAULT1_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_2_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 2 at LF sensing node 1 (LINE_FAULT1) in Mode 0

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8.6.2.18.81 LINE_FAULT1_THRESH_3_HI_M0 Register (Address = 0x6B) [Default = 0x00]

LINE_FAULT1_THRESH_3_HI_M0 is shown in LINE_FAULT1_THRESH_3_HI_M0 Register Field Descriptions.

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Table 8-910. LINE_FAULT1_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_3_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 3 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.82 LINE_FAULT1_THRESH_3_LO_M0 Register (Address = 0x6C) [Default = 0x00]

LINE_FAULT1_THRESH_3_LO_M0 is shown in LINE_FAULT1_THRESH_3_LO_M0 Register Field Descriptions.

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Table 8-911. LINE_FAULT1_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_3_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 3 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.83 LINE_FAULT1_THRESH_4_HI_M0 Register (Address = 0x6D) [Default = 0x00]

LINE_FAULT1_THRESH_4_HI_M0 is shown in LINE_FAULT1_THRESH_4_HI_M0 Register Field Descriptions.

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Table 8-912. LINE_FAULT1_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_4_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 4 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.84 LINE_FAULT1_THRESH_4_LO_M0 Register (Address = 0x6E) [Default = 0x00]

LINE_FAULT1_THRESH_4_LO_M0 is shown in LINE_FAULT1_THRESH_4_LO_M0 Register Field Descriptions.

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Table 8-913. LINE_FAULT1_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_4_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 4 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.85 LINE_FAULT1_THRESH_5_HI_M0 Register (Address = 0x6F) [Default = 0x00]

LINE_FAULT1_THRESH_5_HI_M0 is shown in LINE_FAULT1_THRESH_5_HI_M0 Register Field Descriptions.

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Table 8-914. LINE_FAULT1_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_5_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 5 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.86 LINE_FAULT1_THRESH_5_LO_M0 Register (Address = 0x70) [Default = 0x00]

LINE_FAULT1_THRESH_5_LO_M0 is shown in LINE_FAULT1_THRESH_5_LO_M0 Register Field Descriptions.

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Table 8-915. LINE_FAULT1_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_5_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 5 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.87 LINE_FAULT1_THRESH_6_HI_M0 Register (Address = 0x71) [Default = 0x00]

LINE_FAULT1_THRESH_6_HI_M0 is shown in LINE_FAULT1_THRESH_6_HI_M0 Register Field Descriptions.

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Table 8-916. LINE_FAULT1_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_6_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 6 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.88 LINE_FAULT1_THRESH_6_LO_M0 Register (Address = 0x72) [Default = 0x00]

LINE_FAULT1_THRESH_6_LO_M0 is shown in LINE_FAULT1_THRESH_6_LO_M0 Register Field Descriptions.

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Table 8-917. LINE_FAULT1_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_6_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 6 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.89 LINE_FAULT1_THRESH_7_HI_M0 Register (Address = 0x73) [Default = 0x00]

LINE_FAULT1_THRESH_7_HI_M0 is shown in LINE_FAULT1_THRESH_7_HI_M0 Register Field Descriptions.

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Table 8-918. LINE_FAULT1_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_7_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 7 at LF sensing node 1 (LINE_FAULT1) in Mode 0

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8.6.2.18.90 LINE_FAULT1_THRESH_7_LO_M0 Register (Address = 0x74) [Default = 0x00]

LINE_FAULT1_THRESH_7_LO_M0 is shown in LINE_FAULT1_THRESH_7_LO_M0 Register Field Descriptions.

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Table 8-919. LINE_FAULT1_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_7_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 7 at LF sensing node 1 (LINE_FAULT1) in Mode 0

8.6.2.18.91 LINE_FAULT1_THRESH_MASK_M0 Register (Address = 0x75) [Default = 0xFC]

LINE_FAULT1_THRESH_MASK_M0 is shown in LINE_FAULT1_THRESH_MASK_M0 Register Field Descriptions.

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Table 8-920. LINE_FAULT1_THRESH_MASK_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT1_THRESH_7_MASK_M0	R/W	0x1	Line Fault 1 Threshold 7 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_7_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_7_HI/LO_M0 interrupt
6	LINE_FAULT1_THRESH_6_MASK_M0	R/W	0x1	Line Fault 1 Threshold 6 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_6_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_6_HI/LO_M0 interrupt
5	LINE_FAULT1_THRESH_5_MASK_M0	R/W	0x1	Line Fault 1 Threshold 5 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_5_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_5_HI/LO_M0 interrupt
4	LINE_FAULT1_THRESH_4_MASK_M0	R/W	0x1	Line Fault 1 Threshold 4 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_4_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_4_HI/LO_M0 interrupt
3	LINE_FAULT1_THRESH_3_MASK_M0	R/W	0x1	Line Fault 1 Threshold 3 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_3_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_3_HI/LO_M0 interrupt
2	LINE_FAULT1_THRESH_2_MASK_M0	R/W	0x1	Line Fault 1 Threshold 2 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_2_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_2_HI/LO_M0 interrupt
1	LINE_FAULT1_THRESH_1_MASK_M0	R/W	0x0	Line Fault 1 Threshold 1 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_1_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_1_HI/LO_M0 interrupt
0	LINE_FAULT1_THRESH_0_MASK_M0	R/W	0x0	Line Fault 1 Threshold 0 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_0_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_0_HI/LO_M0 interrupt

8.6.2.18.92 LINE_FAULT1_ADC_OFFSET_M0 Register (Address = 0x76) [Default = 0x00]

LINE_FAULT1_ADC_OFFSET_M0 is shown in LINE_FAULT1_ADC_OFFSET_M0 Register Field Descriptions.

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Table 8-921. LINE_FAULT1_ADC_OFFSET_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_ADC_OFFSET_M0	R/W	0x0	Offset value added to LINE_FAULT1_FINAL ADC code after the ADC conversion (sensed voltage at node to ADC code). This value is for LF sensing node 1 (in Mode 0).

8.6.2.18.93 LINE_FAULT2_THRESH_0_HI_M0 Register (Address = 0x77) [Default = 0xAD]

LINE_FAULT2_THRESH_0_HI_M0 is shown in LINE_FAULT2_THRESH_0_HI_M0 Register Field Descriptions.

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Table 8-922. LINE_FAULT2_THRESH_0_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_0_HI_M0	R/W	0xAD	Holds Upper threshold voltage for LF condition 0 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.94 LINE_FAULT2_THRESH_0_LO_M0 Register (Address = 0x78) [Default = 0x72]

LINE_FAULT2_THRESH_0_LO_M0 is shown in LINE_FAULT2_THRESH_0_LO_M0 Register Field Descriptions.

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Table 8-923. LINE_FAULT2_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_0_LO_M0	R/W	0x72	Holds Lower threshold voltage for LF condition 0 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.95 LINE_FAULT2_THRESH_1_HI_M0 Register (Address = 0x79) [Default = 0xDC]

LINE_FAULT2_THRESH_1_HI_M0 is shown in LINE_FAULT2_THRESH_1_HI_M0 Register Field Descriptions.

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Table 8-924. LINE_FAULT2_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_1_HI_M0	R/W	0xDC	Holds Upper threshold voltage for LF condition 1 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.96 LINE_FAULT2_THRESH_1_LO_M0 Register (Address = 0x7A) [Default = 0xCD]

LINE_FAULT2_THRESH_1_LO_M0 is shown in LINE_FAULT2_THRESH_1_LO_M0 Register Field Descriptions.

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Table 8-925. LINE_FAULT2_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_1_LO_M0	R/W	0xCD	Holds Lower threshold voltage for LF condition 1 at LF sensing node 2 (LINE_FAULT2) in Mode 0

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8.6.2.18.97 LINE_FAULT2_THRESH_2_HI_M0 Register (Address = 0x7B) [Default = 0xF8]

LINE_FAULT2_THRESH_2_HI_M0 is shown in LINE_FAULT2_THRESH_2_HI_M0 Register Field Descriptions.

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Table 8-926. LINE_FAULT2_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_2_HI_M0	R/W	0xF8	Holds Upper threshold voltage for LF condition 2 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.98 LINE_FAULT2_THRESH_2_LO_M0 Register (Address = 0x7C) [Default = 0xE6]

LINE_FAULT2_THRESH_2_LO_M0 is shown in LINE_FAULT2_THRESH_2_LO_M0 Register Field Descriptions.

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Table 8-927. LINE_FAULT2_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_2_LO_M0	R/W	0xE6	Holds Lower threshold voltage for LF condition 2 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.99 LINE_FAULT2_THRESH_3_HI_M0 Register (Address = 0x7D) [Default = 0x00]

LINE_FAULT2_THRESH_3_HI_M0 is shown in LINE_FAULT2_THRESH_3_HI_M0 Register Field Descriptions.

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Table 8-928. LINE_FAULT2_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_3_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 3 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.100 LINE_FAULT2_THRESH_3_LO_M0 Register (Address = 0x7E) [Default = 0x00]

LINE_FAULT2_THRESH_3_LO_M0 is shown in LINE_FAULT2_THRESH_3_LO_M0 Register Field Descriptions.

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Table 8-929. LINE_FAULT2_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_3_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 3 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.101 LINE_FAULT2_THRESH_4_HI_M0 Register (Address = 0x7F) [Default = 0x00]

LINE_FAULT2_THRESH_4_HI_M0 is shown in LINE_FAULT2_THRESH_4_HI_M0 Register Field Descriptions.

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Table 8-930. LINE_FAULT2_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_4_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 4 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.102 LINE_FAULT2_THRESH_4_LO_M0 Register (Address = 0x80) [Default = 0x00]

LINE_FAULT2_THRESH_4_LO_M0 is shown in LINE_FAULT2_THRESH_4_LO_M0 Register Field Descriptions.

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Table 8-931. LINE_FAULT2_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_4_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 4 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.103 LINE_FAULT2_THRESH_5_HI_M0 Register (Address = 0x81) [Default = 0x00]

LINE_FAULT2_THRESH_5_HI_M0 is shown in LINE_FAULT2_THRESH_5_HI_M0 Register Field Descriptions.

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Table 8-932. LINE_FAULT2_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_5_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 5 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.104 LINE_FAULT2_THRESH_5_LO_M0 Register (Address = 0x82) [Default = 0x00]

LINE_FAULT2_THRESH_5_LO_M0 is shown in LINE_FAULT2_THRESH_5_LO_M0 Register Field Descriptions.

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Table 8-933. LINE_FAULT2_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_5_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 5 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.105 LINE_FAULT2_THRESH_6_HI_M0 Register (Address = 0x83) [Default = 0x00]

LINE_FAULT2_THRESH_6_HI_M0 is shown in LINE_FAULT2_THRESH_6_HI_M0 Register Field Descriptions.

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Table 8-934. LINE_FAULT2_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_6_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 6 at LF sensing node 2 (LINE_FAULT2) in Mode 0

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8.6.2.18.106 LINE_FAULT2_THRESH_6_LO_M0 Register (Address = 0x84) [Default = 0x00]

LINE_FAULT2_THRESH_6_LO_M0 is shown in LINE_FAULT2_THRESH_6_LO_M0 Register Field Descriptions.

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Table 8-935. LINE_FAULT2_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_6_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 6 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.107 LINE_FAULT2_THRESH_7_HI_M0 Register (Address = 0x85) [Default = 0x00]

LINE_FAULT2_THRESH_7_HI_M0 is shown in LINE_FAULT2_THRESH_7_HI_M0 Register Field Descriptions.

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Table 8-936. LINE_FAULT2_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_7_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 7 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.108 LINE_FAULT2_THRESH_7_LO_M0 Register (Address = 0x86) [Default = 0x00]

LINE_FAULT2_THRESH_7_LO_M0 is shown in LINE_FAULT2_THRESH_7_LO_M0 Register Field Descriptions.

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Table 8-937. LINE_FAULT2_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_7_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 7 at LF sensing node 2 (LINE_FAULT2) in Mode 0

8.6.2.18.109 LINE_FAULT2_THRESH_MASK_M0 Register (Address = 0x87) [Default = 0xF8]

LINE_FAULT2_THRESH_MASK_M0 is shown in LINE_FAULT2_THRESH_MASK_M0 Register Field Descriptions.

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Table 8-938. LINE_FAULT2_THRESH_MASK_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT2_THRESH_7_MASK_M0	R/W	0x1	Line Fault 2 Threshold 7 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_7_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_7_HI/LO_M0 interrupt
6	LINE_FAULT2_THRESH_6_MASK_M0	R/W	0x1	Line Fault 2 Threshold 6 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_6_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_6_HI/LO_M0 interrupt
5	LINE_FAULT2_THRESH_5_MASK_M0	R/W	0x1	Line Fault 2 Threshold 5 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_5_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_5_HI/LO_M0 interrupt

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Table 8-938. LINE_FAULT2_THRESH_MASK_M0 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	LINE_FAULT2_THRESH_4_MASK_M0	R/W	0x1	Line Fault 2 Threshold 4 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_4_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_4_HI/LO_M0 interrupt
3	LINE_FAULT2_THRESH_3_MASK_M0	R/W	0x1	Line Fault 2 Threshold 3 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_3_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_3_HI/LO_M0 interrupt
2	LINE_FAULT2_THRESH_2_MASK_M0	R/W	0x0	Line Fault 2 Threshold 2 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_2_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_2_HI/LO_M0 interrupt
1	LINE_FAULT2_THRESH_1_MASK_M0	R/W	0x0	Line Fault 2 Threshold 1 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_1_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_1_HI/LO_M0 interrupt
0	LINE_FAULT2_THRESH_0_MASK_M0	R/W	0x0	Line Fault 2 Threshold 0 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_0_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_0_HI/LO_M0 interrupt

8.6.2.18.110 LINE_FAULT2_ADC_OFFSET_M0 Register (Address = 0x88) [Default = 0x00]

LINE_FAULT2_ADC_OFFSET_M0 is shown in LINE_FAULT2_ADC_OFFSET_M0 Register Field Descriptions.

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Table 8-939. LINE_FAULT2_ADC_OFFSET_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_ADC_OFFSET_M0	R/W	0x0	Offset value added to LINE_FAULT2_FINAL ADC code after the ADC conversion (sensed voltage at node to ADC code). This value is for LF sensing node 2 (in Mode 0).

8.6.2.18.111 LINE_FAULT3_THRESH_0_HI_M0 Register (Address = 0x89) [Default = 0x0B]

LINE_FAULT3_THRESH_0_HI_M0 is shown in LINE_FAULT3_THRESH_0_HI_M0 Register Field Descriptions.

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Table 8-940. LINE_FAULT3_THRESH_0_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_0_HI_M0	R/W	0xB	Holds Upper threshold voltage for LF condition 0 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.112 LINE_FAULT3_THRESH_0_LO_M0 Register (Address = 0x8A) [Default = 0x00]

LINE_FAULT3_THRESH_0_LO_M0 is shown in LINE_FAULT3_THRESH_0_LO_M0 Register Field Descriptions.

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Table 8-941. LINE_FAULT3_THRESH_0_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_0_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 0 at LF sensing node 3 (LINE_FAULT3) in Mode 0

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8.6.2.18.113 LINE_FAULT3_THRESH_1_HI_M0 Register (Address = 0x8B) [Default = 0xE9]

LINE_FAULT3_THRESH_1_HI_M0 is shown in LINE_FAULT3_THRESH_1_HI_M0 Register Field Descriptions.

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Table 8-942. LINE_FAULT3_THRESH_1_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_1_HI_M0	R/W	0xE9	Holds Upper threshold voltage for LF condition 1 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.114 LINE_FAULT3_THRESH_1_LO_M0 Register (Address = 0x8C) [Default = 0x60]

LINE_FAULT3_THRESH_1_LO_M0 is shown in LINE_FAULT3_THRESH_1_LO_M0 Register Field Descriptions.

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Table 8-943. LINE_FAULT3_THRESH_1_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_1_LO_M0	R/W	0x60	Holds Lower threshold voltage for LF condition 1 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.115 LINE_FAULT3_THRESH_2_HI_M0 Register (Address = 0x8D) [Default = 0x00]

LINE_FAULT3_THRESH_2_HI_M0 is shown in LINE_FAULT3_THRESH_2_HI_M0 Register Field Descriptions.

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Table 8-944. LINE_FAULT3_THRESH_2_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_2_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 2 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.116 LINE_FAULT3_THRESH_2_LO_M0 Register (Address = 0x8E) [Default = 0x00]

LINE_FAULT3_THRESH_2_LO_M0 is shown in LINE_FAULT3_THRESH_2_LO_M0 Register Field Descriptions.

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Table 8-945. LINE_FAULT3_THRESH_2_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_2_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 2 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.117 LINE_FAULT3_THRESH_3_HI_M0 Register (Address = 0x8F) [Default = 0x00]

LINE_FAULT3_THRESH_3_HI_M0 is shown in LINE_FAULT3_THRESH_3_HI_M0 Register Field Descriptions.

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Table 8-946. LINE_FAULT3_THRESH_3_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_3_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 3 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.118 LINE_FAULT3_THRESH_3_LO_M0 Register (Address = 0x90) [Default = 0x00]

LINE_FAULT3_THRESH_3_LO_M0 is shown in LINE_FAULT3_THRESH_3_LO_M0 Register Field Descriptions.

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Table 8-947. LINE_FAULT3_THRESH_3_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_3_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 3 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.119 LINE_FAULT3_THRESH_4_HI_M0 Register (Address = 0x91) [Default = 0x00]

LINE_FAULT3_THRESH_4_HI_M0 is shown in LINE_FAULT3_THRESH_4_HI_M0 Register Field Descriptions.

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Table 8-948. LINE_FAULT3_THRESH_4_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_4_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 4 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.120 LINE_FAULT3_THRESH_4_LO_M0 Register (Address = 0x92) [Default = 0x00]

LINE_FAULT3_THRESH_4_LO_M0 is shown in LINE_FAULT3_THRESH_4_LO_M0 Register Field Descriptions.

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Table 8-949. LINE_FAULT3_THRESH_4_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_4_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 4 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.121 LINE_FAULT3_THRESH_5_HI_M0 Register (Address = 0x93) [Default = 0x00]

LINE_FAULT3_THRESH_5_HI_M0 is shown in LINE_FAULT3_THRESH_5_HI_M0 Register Field Descriptions.

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Table 8-950. LINE_FAULT3_THRESH_5_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_5_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 5 at LF sensing node 3 (LINE_FAULT3) in Mode 0

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8.6.2.18.122 LINE_FAULT3_THRESH_5_LO_M0 Register (Address = 0x94) [Default = 0x00]

LINE_FAULT3_THRESH_5_LO_M0 is shown in LINE_FAULT3_THRESH_5_LO_M0 Register Field Descriptions.

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Table 8-951. LINE_FAULT3_THRESH_5_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_5_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 5 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.123 LINE_FAULT3_THRESH_6_HI_M0 Register (Address = 0x95) [Default = 0x00]

LINE_FAULT3_THRESH_6_HI_M0 is shown in LINE_FAULT3_THRESH_6_HI_M0 Register Field Descriptions.

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Table 8-952. LINE_FAULT3_THRESH_6_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_6_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 6 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.124 LINE_FAULT3_THRESH_6_LO_M0 Register (Address = 0x96) [Default = 0x00]

LINE_FAULT3_THRESH_6_LO_M0 is shown in LINE_FAULT3_THRESH_6_LO_M0 Register Field Descriptions.

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Table 8-953. LINE_FAULT3_THRESH_6_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_6_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 6 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.125 LINE_FAULT3_THRESH_7_HI_M0 Register (Address = 0x97) [Default = 0x00]

LINE_FAULT3_THRESH_7_HI_M0 is shown in LINE_FAULT3_THRESH_7_HI_M0 Register Field Descriptions.

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Table 8-954. LINE_FAULT3_THRESH_7_HI_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_7_HI_M0	R/W	0x0	Holds Upper threshold voltage for LF condition 7 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.126 LINE_FAULT3_THRESH_7_LO_M0 Register (Address = 0x98) [Default = 0x00]

LINE_FAULT3_THRESH_7_LO_M0 is shown in LINE_FAULT3_THRESH_7_LO_M0 Register Field Descriptions.

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Table 8-955. LINE_FAULT3_THRESH_7_LO_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_7_LO_M0	R/W	0x0	Holds Lower threshold voltage for LF condition 7 at LF sensing node 3 (LINE_FAULT3) in Mode 0

8.6.2.18.127 LINE_FAULT3_THRESH_MASK_M0 Register (Address = 0x99) [Default = 0xFC]

LINE_FAULT3_THRESH_MASK_M0 is shown in LINE_FAULT3_THRESH_MASK_M0 Register Field Descriptions.

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Table 8-956. LINE_FAULT3_THRESH_MASK_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT3_THRESH_7_MASK_M0	R/W	0x1	Line Fault 3 Threshold 7 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_7_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_7_HI/LO_M0 interrupt
6	LINE_FAULT3_THRESH_6_MASK_M0	R/W	0x1	Line Fault 3 Threshold 6 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_6_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_6_HI/LO_M0 interrupt
5	LINE_FAULT3_THRESH_5_MASK_M0	R/W	0x1	Line Fault 3 Threshold 5 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_5_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_5_HI/LO_M0 interrupt
4	LINE_FAULT3_THRESH_4_MASK_M0	R/W	0x1	Line Fault 3 Threshold 4 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_4_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_4_HI/LO_M0 interrupt
3	LINE_FAULT3_THRESH_3_MASK_M0	R/W	0x1	Line Fault 3 Threshold 3 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_3_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_3_HI/LO_M0 interrupt
2	LINE_FAULT3_THRESH_2_MASK_M0	R/W	0x1	Line Fault 3 Threshold 2 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_2_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_2_HI/LO_M0 interrupt
1	LINE_FAULT3_THRESH_1_MASK_M0	R/W	0x0	Line Fault 3 Threshold 1 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_1_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_1_HI/LO_M0 interrupt
0	LINE_FAULT3_THRESH_0_MASK_M0	R/W	0x0	Line Fault 3 Threshold 0 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_0_HI/LO_M0 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_0_HI/LO_M0 interrupt

8.6.2.18.128 LINE_FAULT3_ADC_OFFSET_M0 Register (Address = 0x9A) [Default = 0x00]

LINE_FAULT3_ADC_OFFSET_M0 is shown in LINE_FAULT3_ADC_OFFSET_M0 Register Field Descriptions.

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Table 8-957. LINE_FAULT3_ADC_OFFSET_M0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_ADC_OFFSET_M0	R/W	0x0	Offset value added to LINE_FAULT3_FINAL ADC code after the ADC conversion (sensed voltage at node to ADC code). This value is for LF sensing node 3 (in Mode 0).

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8.6.2.18.129 LINE_FAULT0_THRESH_0_HI_M1 Register (Address = 0x9B) [Default = 0x56]

LINE_FAULT0_THRESH_0_HI_M1 is shown in LINE_FAULT0_THRESH_0_HI_M1 Register Field Descriptions.

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Table 8-958. LINE_FAULT0_THRESH_0_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_0_HI_M1	R/W	0x56	Holds Upper threshold voltage for LF condition 0 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.130 LINE_FAULT0_THRESH_0_LO_M1 Register (Address = 0x9C) [Default = 0x39]

LINE_FAULT0_THRESH_0_LO_M1 is shown in LINE_FAULT0_THRESH_0_LO_M1 Register Field Descriptions.

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Table 8-959. LINE_FAULT0_THRESH_0_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_0_LO_M1	R/W	0x39	Holds Lower threshold voltage for LF condition 0 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.131 LINE_FAULT0_THRESH_1_HI_M1 Register (Address = 0x9D) [Default = 0x6E]

LINE_FAULT0_THRESH_1_HI_M1 is shown in LINE_FAULT0_THRESH_1_HI_M1 Register Field Descriptions.

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Table 8-960. LINE_FAULT0_THRESH_1_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_1_HI_M1	R/W	0x6E	Holds Upper threshold voltage for LF condition 1 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.132 LINE_FAULT0_THRESH_1_LO_M1 Register (Address = 0x9E) [Default = 0x64]

LINE_FAULT0_THRESH_1_LO_M1 is shown in LINE_FAULT0_THRESH_1_LO_M1 Register Field Descriptions.

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Table 8-961. LINE_FAULT0_THRESH_1_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_1_LO_M1	R/W	0x64	Holds Lower threshold voltage for LF condition 1 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.133 LINE_FAULT0_THRESH_2_HI_M1 Register (Address = 0x9F) [Default = 0x7C]

LINE_FAULT0_THRESH_2_HI_M1 is shown in LINE_FAULT0_THRESH_2_HI_M1 Register Field Descriptions.

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Table 8-962. LINE_FAULT0_THRESH_2_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_2_HI_M1	R/W	0x7C	Holds Upper threshold voltage for LF condition 2 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.134 LINE_FAULT0_THRESH_2_LO_M1 Register (Address = 0xA0) [Default = 0x71]

LINE_FAULT0_THRESH_2_LO_M1 is shown in LINE_FAULT0_THRESH_2_LO_M1 Register Field Descriptions.

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Table 8-963. LINE_FAULT0_THRESH_2_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_2_LO_M1	R/W	0x71	Holds Lower threshold voltage for LF condition 2 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.135 LINE_FAULT0_THRESH_3_HI_M1 Register (Address = 0xA1) [Default = 0x9A]

LINE_FAULT0_THRESH_3_HI_M1 is shown in LINE_FAULT0_THRESH_3_HI_M1 Register Field Descriptions.

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Table 8-964. LINE_FAULT0_THRESH_3_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_3_HI_M1	R/W	0x9A	Holds Upper threshold voltage for LF condition 3 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.136 LINE_FAULT0_THRESH_3_LO_M1 Register (Address = 0xA2) [Default = 0x89]

LINE_FAULT0_THRESH_3_LO_M1 is shown in LINE_FAULT0_THRESH_3_LO_M1 Register Field Descriptions.

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Table 8-965. LINE_FAULT0_THRESH_3_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_3_LO_M1	R/W	0x89	Holds Lower threshold voltage for LF condition 3 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.137 LINE_FAULT0_THRESH_4_HI_M1 Register (Address = 0xA3) [Default = 0xC8]

LINE_FAULT0_THRESH_4_HI_M1 is shown in LINE_FAULT0_THRESH_4_HI_M1 Register Field Descriptions.

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Table 8-966. LINE_FAULT0_THRESH_4_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_4_HI_M1	R/W	0xC8	Holds Upper threshold voltage for LF condition 4 at LF sensing node 0 (LINE_FAULT0) in Mode 1

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8.6.2.18.138 LINE_FAULT0_THRESH_4_LO_M1 Register (Address = 0xA4) [Default = 0xB8]

LINE_FAULT0_THRESH_4_LO_M1 is shown in LINE_FAULT0_THRESH_4_LO_M1 Register Field Descriptions.

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Table 8-967. LINE_FAULT0_THRESH_4_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_4_LO_M1	R/W	0xB8	Holds Lower threshold voltage for LF condition 4 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.139 LINE_FAULT0_THRESH_5_HI_M1 Register (Address = 0xA5) [Default = 0x00]

LINE_FAULT0_THRESH_5_HI_M1 is shown in LINE_FAULT0_THRESH_5_HI_M1 Register Field Descriptions.

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Table 8-968. LINE_FAULT0_THRESH_5_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_5_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 5 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.140 LINE_FAULT0_THRESH_5_LO_M1 Register (Address = 0xA6) [Default = 0x00]

LINE_FAULT0_THRESH_5_LO_M1 is shown in LINE_FAULT0_THRESH_5_LO_M1 Register Field Descriptions.

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Table 8-969. LINE_FAULT0_THRESH_5_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_5_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 5 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.141 LINE_FAULT0_THRESH_6_HI_M1 Register (Address = 0xA7) [Default = 0x00]

LINE_FAULT0_THRESH_6_HI_M1 is shown in LINE_FAULT0_THRESH_6_HI_M1 Register Field Descriptions.

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Table 8-970. LINE_FAULT0_THRESH_6_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_6_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 6 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.142 LINE_FAULT0_THRESH_6_LO_M1 Register (Address = 0xA8) [Default = 0x00]

LINE_FAULT0_THRESH_6_LO_M1 is shown in LINE_FAULT0_THRESH_6_LO_M1 Register Field Descriptions.

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Table 8-971. LINE_FAULT0_THRESH_6_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_6_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 6 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.143 LINE_FAULT0_THRESH_7_HI_M1 Register (Address = 0xA9) [Default = 0x00]

LINE_FAULT0_THRESH_7_HI_M1 is shown in LINE_FAULT0_THRESH_7_HI_M1 Register Field Descriptions.

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Table 8-972. LINE_FAULT0_THRESH_7_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_7_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 7 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.144 LINE_FAULT0_THRESH_7_LO_M1 Register (Address = 0xAA) [Default = 0x00]

LINE_FAULT0_THRESH_7_LO_M1 is shown in LINE_FAULT0_THRESH_7_LO_M1 Register Field Descriptions.

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Table 8-973. LINE_FAULT0_THRESH_7_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_THRESH_7_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 7 at LF sensing node 0 (LINE_FAULT0) in Mode 1

8.6.2.18.145 LINE_FAULT0_THRESH_MASK_M1 Register (Address = 0xAB) [Default = 0xE0]

LINE_FAULT0_THRESH_MASK_M1 is shown in LINE_FAULT0_THRESH_MASK_M1 Register Field Descriptions.

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Table 8-974. LINE_FAULT0_THRESH_MASK_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT0_THRESH_7_MASK_M1	R/W	0x1	Line Fault 0 Threshold 7 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_7_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_7_HI/LO_M1 interrupt
6	LINE_FAULT0_THRESH_6_MASK_M1	R/W	0x1	Line Fault 0 Threshold 6 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_6_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_6_HI/LO_M1 interrupt
5	LINE_FAULT0_THRESH_5_MASK_M1	R/W	0x1	Line Fault 0 Threshold 5 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_5_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_5_HI/LO_M1 interrupt
4	LINE_FAULT0_THRESH_4_MASK_M1	R/W	0x0	Line Fault 0 Threshold 4 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_4_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_4_HI/LO_M1 interrupt

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Table 8-974. LINE_FAULT0_THRESH_MASK_M1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	LINE_FAULT0_THRESH_3_MASK_M1	R/W	0x0	Line Fault 0 Threshold 3 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_3_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_3_HI/LO_M1 interrupt
2	LINE_FAULT0_THRESH_2_MASK_M1	R/W	0x0	Line Fault 0 Threshold 2 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_2_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_2_HI/LO_M1 interrupt
1	LINE_FAULT0_THRESH_1_MASK_M1	R/W	0x0	Line Fault 0 Threshold 1 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_1_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_1_HI/LO_M1 interrupt
0	LINE_FAULT0_THRESH_0_MASK_M1	R/W	0x0	Line Fault 0 Threshold 0 Mask Setting 0: Do not mask LINE_FAULT0_THRESH_0_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT0_THRESH_0_HI/LO_M1 interrupt

8.6.2.18.146 LINE_FAULT0_ADC_OFFSET_M1 Register (Address = 0xAC) [Default = 0x00]

LINE_FAULT0_ADC_OFFSET_M1 is shown in LINE_FAULT0_ADC_OFFSET_M1 Register Field Descriptions.

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Table 8-975. LINE_FAULT0_ADC_OFFSET_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT0_ADC_OFFSET_M1	R/W	0x0	Offset value added to LINE_FAULT0_FINAL ADC code after the ADC conversion (sensed voltage at node to ADC code). This value is for LF sensing node 0 (in Mode 1).

8.6.2.18.147 LINE_FAULT1_THRESH_0_HI_M1 Register (Address = 0xAD) [Default = 0x00]

LINE_FAULT1_THRESH_0_HI_M1 is shown in LINE_FAULT1_THRESH_0_HI_M1 Register Field Descriptions.

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Table 8-976. LINE_FAULT1_THRESH_0_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_0_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 0 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.148 LINE_FAULT1_THRESH_0_LO_M1 Register (Address = 0xAE) [Default = 0x00]

LINE_FAULT1_THRESH_0_LO_M1 is shown in LINE_FAULT1_THRESH_0_LO_M1 Register Field Descriptions.

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Table 8-977. LINE_FAULT1_THRESH_0_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_0_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 0 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.149 LINE_FAULT1_THRESH_1_HI_M1 Register (Address = 0xAF) [Default = 0x00]

LINE_FAULT1_THRESH_1_HI_M1 is shown in LINE_FAULT1_THRESH_1_HI_M1 Register Field Descriptions.

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Table 8-978. LINE_FAULT1_THRESH_1_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_1_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 1 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.150 LINE_FAULT1_THRESH_1_LO_M1 Register (Address = 0xB0) [Default = 0x00]

LINE_FAULT1_THRESH_1_LO_M1 is shown in LINE_FAULT1_THRESH_1_LO_M1 Register Field Descriptions.

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Table 8-979. LINE_FAULT1_THRESH_1_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_1_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 1 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.151 LINE_FAULT1_THRESH_2_HI_M1 Register (Address = 0xB1) [Default = 0x00]

LINE_FAULT1_THRESH_2_HI_M1 is shown in LINE_FAULT1_THRESH_2_HI_M1 Register Field Descriptions.

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Table 8-980. LINE_FAULT1_THRESH_2_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_2_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 2 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.152 LINE_FAULT1_THRESH_2_LO_M1 Register (Address = 0xB2) [Default = 0x00]

LINE_FAULT1_THRESH_2_LO_M1 is shown in LINE_FAULT1_THRESH_2_LO_M1 Register Field Descriptions.

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Table 8-981. LINE_FAULT1_THRESH_2_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_2_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 2 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.153 LINE_FAULT1_THRESH_3_HI_M1 Register (Address = 0xB3) [Default = 0x00]

LINE_FAULT1_THRESH_3_HI_M1 is shown in LINE_FAULT1_THRESH_3_HI_M1 Register Field Descriptions.

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Table 8-982. LINE_FAULT1_THRESH_3_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_3_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 3 at LF sensing node 1 (LINE_FAULT1) in Mode 1

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8.6.2.18.154 LINE_FAULT1_THRESH_3_LO_M1 Register (Address = 0xB4) [Default = 0x00]

LINE_FAULT1_THRESH_3_LO_M1 is shown in LINE_FAULT1_THRESH_3_LO_M1 Register Field Descriptions.

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Table 8-983. LINE_FAULT1_THRESH_3_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_3_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 3 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.155 LINE_FAULT1_THRESH_4_HI_M1 Register (Address = 0xB5) [Default = 0x00]

LINE_FAULT1_THRESH_4_HI_M1 is shown in LINE_FAULT1_THRESH_4_HI_M1 Register Field Descriptions.

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Table 8-984. LINE_FAULT1_THRESH_4_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_4_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 4 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.156 LINE_FAULT1_THRESH_4_LO_M1 Register (Address = 0xB6) [Default = 0x00]

LINE_FAULT1_THRESH_4_LO_M1 is shown in LINE_FAULT1_THRESH_4_LO_M1 Register Field Descriptions.

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Table 8-985. LINE_FAULT1_THRESH_4_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_4_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 4 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.157 LINE_FAULT1_THRESH_5_HI_M1 Register (Address = 0xB7) [Default = 0x00]

LINE_FAULT1_THRESH_5_HI_M1 is shown in LINE_FAULT1_THRESH_5_HI_M1 Register Field Descriptions.

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Table 8-986. LINE_FAULT1_THRESH_5_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_5_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 5 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.158 LINE_FAULT1_THRESH_5_LO_M1 Register (Address = 0xB8) [Default = 0x00]

LINE_FAULT1_THRESH_5_LO_M1 is shown in LINE_FAULT1_THRESH_5_LO_M1 Register Field Descriptions.

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Table 8-987. LINE_FAULT1_THRESH_5_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_5_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 5 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.159 LINE_FAULT1_THRESH_6_HI_M1 Register (Address = 0xB9) [Default = 0x00]

LINE_FAULT1_THRESH_6_HI_M1 is shown in LINE_FAULT1_THRESH_6_HI_M1 Register Field Descriptions.

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Table 8-988. LINE_FAULT1_THRESH_6_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_6_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 6 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.160 LINE_FAULT1_THRESH_6_LO_M1 Register (Address = 0xBA) [Default = 0x00]

LINE_FAULT1_THRESH_6_LO_M1 is shown in LINE_FAULT1_THRESH_6_LO_M1 Register Field Descriptions.

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Table 8-989. LINE_FAULT1_THRESH_6_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_6_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 6 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.161 LINE_FAULT1_THRESH_7_HI_M1 Register (Address = 0xBB) [Default = 0x00]

LINE_FAULT1_THRESH_7_HI_M1 is shown in LINE_FAULT1_THRESH_7_HI_M1 Register Field Descriptions.

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Table 8-990. LINE_FAULT1_THRESH_7_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_7_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 7 at LF sensing node 1 (LINE_FAULT1) in Mode 1

8.6.2.18.162 LINE_FAULT1_THRESH_7_LO_M1 Register (Address = 0xBC) [Default = 0x00]

LINE_FAULT1_THRESH_7_LO_M1 is shown in LINE_FAULT1_THRESH_7_LO_M1 Register Field Descriptions.

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Table 8-991. LINE_FAULT1_THRESH_7_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_THRESH_7_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 7 at LF sensing node 1 (LINE_FAULT1) in Mode 1

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8.6.2.18.163 LINE_FAULT1_THRESH_MASK_M1 Register (Address = 0xBD) [Default = 0xFF]

LINE_FAULT1_THRESH_MASK_M1 is shown in LINE_FAULT1_THRESH_MASK_M1 Register Field Descriptions.

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Table 8-992. LINE_FAULT1_THRESH_MASK_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT1_THRESH_7_MASK_M1	R/W	0x1	Line Fault 1 Threshold 7 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_7_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_7_HI/LO_M1 interrupt
6	LINE_FAULT1_THRESH_6_MASK_M1	R/W	0x1	Line Fault 1 Threshold 6 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_6_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_6_HI/LO_M1 interrupt
5	LINE_FAULT1_THRESH_5_MASK_M1	R/W	0x1	Line Fault 1 Threshold 5 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_5_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_5_HI/LO_M1 interrupt
4	LINE_FAULT1_THRESH_4_MASK_M1	R/W	0x1	Line Fault 1 Threshold 4 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_4_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_4_HI/LO_M1 interrupt
3	LINE_FAULT1_THRESH_3_MASK_M1	R/W	0x1	Line Fault 1 Threshold 3 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_3_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_3_HI/LO_M1 interrupt
2	LINE_FAULT1_THRESH_2_MASK_M1	R/W	0x1	Line Fault 1 Threshold 2 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_2_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_2_HI/LO_M1 interrupt
1	LINE_FAULT1_THRESH_1_MASK_M1	R/W	0x1	Line Fault 1 Threshold 1 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_1_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_1_HI/LO_M1 interrupt
0	LINE_FAULT1_THRESH_0_MASK_M1	R/W	0x1	Line Fault 1 Threshold 0 Mask Setting 0: Do not mask LINE_FAULT1_THRESH_0_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT1_THRESH_0_HI/LO_M1 interrupt

8.6.2.18.164 LINE_FAULT1_ADC_OFFSET_M1 Register (Address = 0xBE) [Default = 0x00]

LINE_FAULT1_ADC_OFFSET_M1 is shown in LINE_FAULT1_ADC_OFFSET_M1 Register Field Descriptions.

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Table 8-993. LINE_FAULT1_ADC_OFFSET_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT1_ADC_OFFSET_M1	R/W	0x0	Offset value added to LINE_FAULT1_FINAL ADC code after the ADC conversion (sensed voltage at node to ADC code). This value is for LF sensing node 1 (in Mode 1).

8.6.2.18.165 LINE_FAULT2_THRESH_0_HI_M1 Register (Address = 0xBF) [Default = 0x56]

LINE_FAULT2_THRESH_0_HI_M1 is shown in LINE_FAULT2_THRESH_0_HI_M1 Register Field Descriptions.

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Table 8-994. LINE_FAULT2_THRESH_0_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_0_HI_M1	R/W	0x56	Holds Upper threshold voltage for LF condition 0 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.166 LINE_FAULT2_THRESH_0_LO_M1 Register (Address = 0xC0) [Default = 0x39]

LINE_FAULT2_THRESH_0_LO_M1 is shown in LINE_FAULT2_THRESH_0_LO_M1 Register Field Descriptions.

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Table 8-995. LINE_FAULT2_THRESH_0_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_0_LO_M1	R/W	0x39	Holds Lower threshold voltage for LF condition 0 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.167 LINE_FAULT2_THRESH_1_HI_M1 Register (Address = 0xC1) [Default = 0x6E]

LINE_FAULT2_THRESH_1_HI_M1 is shown in LINE_FAULT2_THRESH_1_HI_M1 Register Field Descriptions.

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Table 8-996. LINE_FAULT2_THRESH_1_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_1_HI_M1	R/W	0x6E	Holds Upper threshold voltage for LF condition 1 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.168 LINE_FAULT2_THRESH_1_LO_M1 Register (Address = 0xC2) [Default = 0x64]

LINE_FAULT2_THRESH_1_LO_M1 is shown in LINE_FAULT2_THRESH_1_LO_M1 Register Field Descriptions.

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Table 8-997. LINE_FAULT2_THRESH_1_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_1_LO_M1	R/W	0x64	Holds Lower threshold voltage for LF condition 1 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.169 LINE_FAULT2_THRESH_2_HI_M1 Register (Address = 0xC3) [Default = 0x7C]

LINE_FAULT2_THRESH_2_HI_M1 is shown in LINE_FAULT2_THRESH_2_HI_M1 Register Field Descriptions.

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Table 8-998. LINE_FAULT2_THRESH_2_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_2_HI_M1	R/W	0x7C	Holds Upper threshold voltage for LF condition 2 at LF sensing node 2 (LINE_FAULT2) in Mode 1

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8.6.2.18.170 LINE_FAULT2_THRESH_2_LO_M1 Register (Address = 0xC4) [Default = 0x71]

LINE_FAULT2_THRESH_2_LO_M1 is shown in LINE_FAULT2_THRESH_2_LO_M1 Register Field Descriptions.

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Table 8-999. LINE_FAULT2_THRESH_2_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_2_LO_M1	R/W	0x71	Holds Lower threshold voltage for LF condition 2 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.171 LINE_FAULT2_THRESH_3_HI_M1 Register (Address = 0xC5) [Default = 0x9A]

LINE_FAULT2_THRESH_3_HI_M1 is shown in LINE_FAULT2_THRESH_3_HI_M1 Register Field Descriptions.

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Table 8-1000. LINE_FAULT2_THRESH_3_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_3_HI_M1	R/W	0x9A	Holds Upper threshold voltage for LF condition 3 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.172 LINE_FAULT2_THRESH_3_LO_M1 Register (Address = 0xC6) [Default = 0x89]

LINE_FAULT2_THRESH_3_LO_M1 is shown in LINE_FAULT2_THRESH_3_LO_M1 Register Field Descriptions.

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Table 8-1001. LINE_FAULT2_THRESH_3_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_3_LO_M1	R/W	0x89	Holds Lower threshold voltage for LF condition 3 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.173 LINE_FAULT2_THRESH_4_HI_M1 Register (Address = 0xC7) [Default = 0xC8]

LINE_FAULT2_THRESH_4_HI_M1 is shown in LINE_FAULT2_THRESH_4_HI_M1 Register Field Descriptions.

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Table 8-1002. LINE_FAULT2_THRESH_4_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_4_HI_M1	R/W	0xC8	Holds Upper threshold voltage for LF condition 4 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.174 LINE_FAULT2_THRESH_4_LO_M1 Register (Address = 0xC8) [Default = 0xB8]

LINE_FAULT2_THRESH_4_LO_M1 is shown in LINE_FAULT2_THRESH_4_LO_M1 Register Field Descriptions.

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Table 8-1003. LINE_FAULT2_THRESH_4_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_4_LO_M1	R/W	0xB8	Holds Lower threshold voltage for LF condition 4 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.175 LINE_FAULT2_THRESH_5_HI_M1 Register (Address = 0xC9) [Default = 0x00]

LINE_FAULT2_THRESH_5_HI_M1 is shown in LINE_FAULT2_THRESH_5_HI_M1 Register Field Descriptions.

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Table 8-1004. LINE_FAULT2_THRESH_5_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_5_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 5 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.176 LINE_FAULT2_THRESH_5_LO_M1 Register (Address = 0xCA) [Default = 0x00]

LINE_FAULT2_THRESH_5_LO_M1 is shown in LINE_FAULT2_THRESH_5_LO_M1 Register Field Descriptions.

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Table 8-1005. LINE_FAULT2_THRESH_5_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_5_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 5 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.177 LINE_FAULT2_THRESH_6_HI_M1 Register (Address = 0xCB) [Default = 0x00]

LINE_FAULT2_THRESH_6_HI_M1 is shown in LINE_FAULT2_THRESH_6_HI_M1 Register Field Descriptions.

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Table 8-1006. LINE_FAULT2_THRESH_6_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_6_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 6 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.178 LINE_FAULT2_THRESH_6_LO_M1 Register (Address = 0xCC) [Default = 0x00]

LINE_FAULT2_THRESH_6_LO_M1 is shown in LINE_FAULT2_THRESH_6_LO_M1 Register Field Descriptions.

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Table 8-1007. LINE_FAULT2_THRESH_6_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_6_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 6 at LF sensing node 2 (LINE_FAULT2) in Mode 1

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8.6.2.18.179 LINE_FAULT2_THRESH_7_HI_M1 Register (Address = 0xCD) [Default = 0x00]

LINE_FAULT2_THRESH_7_HI_M1 is shown in LINE_FAULT2_THRESH_7_HI_M1 Register Field Descriptions.

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Table 8-1008. LINE_FAULT2_THRESH_7_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_7_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 7 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.180 LINE_FAULT2_THRESH_7_LO_M1 Register (Address = 0xCE) [Default = 0x00]

LINE_FAULT2_THRESH_7_LO_M1 is shown in LINE_FAULT2_THRESH_7_LO_M1 Register Field Descriptions.

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Table 8-1009. LINE_FAULT2_THRESH_7_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_THRESH_7_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 7 at LF sensing node 2 (LINE_FAULT2) in Mode 1

8.6.2.18.181 LINE_FAULT2_THRESH_MASK_M1 Register (Address = 0xCF) [Default = 0xE0]

LINE_FAULT2_THRESH_MASK_M1 is shown in LINE_FAULT2_THRESH_MASK_M1 Register Field Descriptions.

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Table 8-1010. LINE_FAULT2_THRESH_MASK_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT2_THRESH_7_MASK_M1	R/W	0x1	Line Fault 2 Threshold 7 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_7_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_7_HI/LO_M1 interrupt
6	LINE_FAULT2_THRESH_6_MASK_M1	R/W	0x1	Line Fault 2 Threshold 6 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_6_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_6_HI/LO_M1 interrupt
5	LINE_FAULT2_THRESH_5_MASK_M1	R/W	0x1	Line Fault 2 Threshold 5 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_5_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_5_HI/LO_M1 interrupt
4	LINE_FAULT2_THRESH_4_MASK_M1	R/W	0x0	Line Fault 2 Threshold 4 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_4_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_4_HI/LO_M1 interrupt
3	LINE_FAULT2_THRESH_3_MASK_M1	R/W	0x0	Line Fault 2 Threshold 3 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_3_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_3_HI/LO_M1 interrupt
2	LINE_FAULT2_THRESH_2_MASK_M1	R/W	0x0	Line Fault 2 Threshold 2 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_2_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_2_HI/LO_M1 interrupt

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Table 8-1010. LINE_FAULT2_THRESH_MASK_M1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	LINE_FAULT2_THRESH_1_MASK_M1	R/W	0x0	Line Fault 2 Threshold 1 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_1_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_1_HI/LO_M1 interrupt
0	LINE_FAULT2_THRESH_0_MASK_M1	R/W	0x0	Line Fault 2 Threshold 0 Mask Setting 0: Do not mask LINE_FAULT2_THRESH_0_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT2_THRESH_0_HI/LO_M1 interrupt

8.6.2.18.182 LINE_FAULT2_ADC_OFFSET_M1 Register (Address = 0xD0) [Default = 0x00]

LINE_FAULT2_ADC_OFFSET_M1 is shown in LINE_FAULT2_ADC_OFFSET_M1 Register Field Descriptions.

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Table 8-1011. LINE_FAULT2_ADC_OFFSET_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT2_ADC_OFFSET_M1	R/W	0x0	Offset value added to LINE_FAULT2_FINAL ADC code after the ADC conversion (sensed voltage at node to ADC code). This value is for LF sensing node 2 (in Mode 1).

8.6.2.18.183 LINE_FAULT3_THRESH_0_HI_M1 Register (Address = 0xD1) [Default = 0x00]

LINE_FAULT3_THRESH_0_HI_M1 is shown in LINE_FAULT3_THRESH_0_HI_M1 Register Field Descriptions.

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Table 8-1012. LINE_FAULT3_THRESH_0_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_0_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 0 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.184 LINE_FAULT3_THRESH_0_LO_M1 Register (Address = 0xD2) [Default = 0x00]

LINE_FAULT3_THRESH_0_LO_M1 is shown in LINE_FAULT3_THRESH_0_LO_M1 Register Field Descriptions.

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Table 8-1013. LINE_FAULT3_THRESH_0_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_0_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 0 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.185 LINE_FAULT3_THRESH_1_HI_M1 Register (Address = 0xD3) [Default = 0x00]

LINE_FAULT3_THRESH_1_HI_M1 is shown in LINE_FAULT3_THRESH_1_HI_M1 Register Field Descriptions.

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Table 8-1014. LINE_FAULT3_THRESH_1_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_1_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 1 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.186 LINE_FAULT3_THRESH_1_LO_M1 Register (Address = 0xD4) [Default = 0x00]

LINE_FAULT3_THRESH_1_LO_M1 is shown in LINE_FAULT3_THRESH_1_LO_M1 Register Field Descriptions.

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Table 8-1015. LINE_FAULT3_THRESH_1_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_1_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 1 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.187 LINE_FAULT3_THRESH_2_HI_M1 Register (Address = 0xD5) [Default = 0x00]

LINE_FAULT3_THRESH_2_HI_M1 is shown in LINE_FAULT3_THRESH_2_HI_M1 Register Field Descriptions.

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Table 8-1016. LINE_FAULT3_THRESH_2_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_2_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 2 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.188 LINE_FAULT3_THRESH_2_LO_M1 Register (Address = 0xD6) [Default = 0x00]

LINE_FAULT3_THRESH_2_LO_M1 is shown in LINE_FAULT3_THRESH_2_LO_M1 Register Field Descriptions.

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Table 8-1017. LINE_FAULT3_THRESH_2_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_2_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 2 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.189 LINE_FAULT3_THRESH_3_HI_M1 Register (Address = 0xD7) [Default = 0x00]

LINE_FAULT3_THRESH_3_HI_M1 is shown in LINE_FAULT3_THRESH_3_HI_M1 Register Field Descriptions.

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Table 8-1018. LINE_FAULT3_THRESH_3_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_3_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 3 at LF sensing node 3 (LINE_FAULT3) in Mode 1

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8.6.2.18.190 LINE_FAULT3_THRESH_3_LO_M1 Register (Address = 0xD8) [Default = 0x00]

LINE_FAULT3_THRESH_3_LO_M1 is shown in LINE_FAULT3_THRESH_3_LO_M1 Register Field Descriptions.

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Table 8-1019. LINE_FAULT3_THRESH_3_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_3_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 3 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.191 LINE_FAULT3_THRESH_4_HI_M1 Register (Address = 0xD9) [Default = 0x00]

LINE_FAULT3_THRESH_4_HI_M1 is shown in LINE_FAULT3_THRESH_4_HI_M1 Register Field Descriptions.

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Table 8-1020. LINE_FAULT3_THRESH_4_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_4_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 4 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.192 LINE_FAULT3_THRESH_4_LO_M1 Register (Address = 0xDA) [Default = 0x00]

LINE_FAULT3_THRESH_4_LO_M1 is shown in LINE_FAULT3_THRESH_4_LO_M1 Register Field Descriptions.

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Table 8-1021. LINE_FAULT3_THRESH_4_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_4_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 4 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.193 LINE_FAULT3_THRESH_5_HI_M1 Register (Address = 0xDB) [Default = 0x00]

LINE_FAULT3_THRESH_5_HI_M1 is shown in LINE_FAULT3_THRESH_5_HI_M1 Register Field Descriptions.

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Table 8-1022. LINE_FAULT3_THRESH_5_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_5_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 5 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.194 LINE_FAULT3_THRESH_5_LO_M1 Register (Address = 0xDC) [Default = 0x00]

LINE_FAULT3_THRESH_5_LO_M1 is shown in LINE_FAULT3_THRESH_5_LO_M1 Register Field Descriptions.

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Table 8-1023. LINE_FAULT3_THRESH_5_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_5_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 5 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.195 LINE_FAULT3_THRESH_6_HI_M1 Register (Address = 0xDD) [Default = 0x00]

LINE_FAULT3_THRESH_6_HI_M1 is shown in LINE_FAULT3_THRESH_6_HI_M1 Register Field Descriptions.

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Table 8-1024. LINE_FAULT3_THRESH_6_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_6_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 6 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.196 LINE_FAULT3_THRESH_6_LO_M1 Register (Address = 0xDE) [Default = 0x00]

LINE_FAULT3_THRESH_6_LO_M1 is shown in LINE_FAULT3_THRESH_6_LO_M1 Register Field Descriptions.

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Table 8-1025. LINE_FAULT3_THRESH_6_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_6_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 6 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.197 LINE_FAULT3_THRESH_7_HI_M1 Register (Address = 0xDF) [Default = 0x00]

LINE_FAULT3_THRESH_7_HI_M1 is shown in LINE_FAULT3_THRESH_7_HI_M1 Register Field Descriptions.

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Table 8-1026. LINE_FAULT3_THRESH_7_HI_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_7_HI_M1	R/W	0x0	Holds Upper threshold voltage for LF condition 7 at LF sensing node 3 (LINE_FAULT3) in Mode 1

8.6.2.18.198 LINE_FAULT3_THRESH_7_LO_M1 Register (Address = 0xE0) [Default = 0x00]

LINE_FAULT3_THRESH_7_LO_M1 is shown in LINE_FAULT3_THRESH_7_LO_M1 Register Field Descriptions.

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Table 8-1027. LINE_FAULT3_THRESH_7_LO_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_THRESH_7_LO_M1	R/W	0x0	Holds Lower threshold voltage for LF condition 7 at LF sensing node 3 (LINE_FAULT3) in Mode 1

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8.6.2.18.199 LINE_FAULT3_THRESH_MASK_M1 Register (Address = 0xE1) [Default = 0xFF]

LINE_FAULT3_THRESH_MASK_M1 is shown in LINE_FAULT3_THRESH_MASK_M1 Register Field Descriptions.

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Table 8-1028. LINE_FAULT3_THRESH_MASK_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT3_THRESH_7_MASK_M1	R/W	0x1	Line Fault 3 Threshold 7 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_7_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_7_HI/LO_M1 interrupt
6	LINE_FAULT3_THRESH_6_MASK_M1	R/W	0x1	Line Fault 3 Threshold 6 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_6_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_6_HI/LO_M1 interrupt
5	LINE_FAULT3_THRESH_5_MASK_M1	R/W	0x1	Line Fault 3 Threshold 5 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_5_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_5_HI/LO_M1 interrupt
4	LINE_FAULT3_THRESH_4_MASK_M1	R/W	0x1	Line Fault 3 Threshold 4 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_4_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_4_HI/LO_M1 interrupt
3	LINE_FAULT3_THRESH_3_MASK_M1	R/W	0x1	Line Fault 3 Threshold 3 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_3_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_3_HI/LO_M1 interrupt
2	LINE_FAULT3_THRESH_2_MASK_M1	R/W	0x1	Line Fault 3 Threshold 2 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_2_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_2_HI/LO_M1 interrupt
1	LINE_FAULT3_THRESH_1_MASK_M1	R/W	0x1	Line Fault 3 Threshold 1 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_1_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_1_HI/LO_M1 interrupt
0	LINE_FAULT3_THRESH_0_MASK_M1	R/W	0x1	Line Fault 3 Threshold 0 Mask Setting 0: Do not mask LINE_FAULT3_THRESH_0_HI/LO_M1 (ADC output in this range will cause interrupt) 1: Mask LINE_FAULT3_THRESH_0_HI/LO_M1 interrupt

8.6.2.18.200 LINE_FAULT3_ADC_OFFSET_M1 Register (Address = 0xE2) [Default = 0x00]

LINE_FAULT3_ADC_OFFSET_M1 is shown in LINE_FAULT3_ADC_OFFSET_M1 Register Field Descriptions.

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Table 8-1029. LINE_FAULT3_ADC_OFFSET_M1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_FAULT3_ADC_OFFSET_M1	R/W	0x0	Offset value added to LINE_FAULT3_FINAL ADC code after the ADC conversion (sensed voltage at node to ADC code). This value is for LF sensing node 3 (in Mode 1).

8.6.2.18.201 LINE_FAULT10_PD_SEL Register (Address = 0xE3) [Default = 0x33]

LINE_FAULT10_PD_SEL is shown in LINE_FAULT10_PD_SEL Register Field Descriptions.

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Table 8-1030. LINE_FAULT10_PD_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	LINE_FAULT1_PD_SEL	R/W	0x3	Configure the 25 kΩ pull-down resistor for GPIO 10 - 13 when Line Fault 1 is enabled. Bit 3 - GPIO 13 Bit 2 - GPIO 12 Bit 1 - GPIO 11 Bit 0 - GPIO 10 Set bit to 0 to disable pull-down at GPIO. Set bit to 1 to enable pull-down at GPIO.
3:0	LINE_FAULT0_PD_SEL	R/W	0x3	Configure the 25 kΩ pull-down resistor for GPIO 10 - 13 when Line Fault 0 is enabled. Bit 3 - GPIO 13 Bit 2 - GPIO 12 Bit 1 - GPIO 11 Bit 0 - GPIO 10 Set bit to 0 to disable pull-down at GPIO. Set bit to 1 to enable pull-down at GPIO.

8.6.2.18.202 LINE_FAULT32_PD_SEL Register (Address = 0xE4) [Default = 0xCC]

LINE_FAULT32_PD_SEL is shown in LINE_FAULT32_PD_SEL Register Field Descriptions.

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Table 8-1031. LINE_FAULT32_PD_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	LINE_FAULT3_PD_SEL	R/W	0xC	Configure the 25 kΩ pull-down resistor for GPIO 10 - 13 when Line Fault 3 is enabled. Bit 3 - GPIO 13 Bit 2 - GPIO 12 Bit 1 - GPIO 11 Bit 0 - GPIO 10 Set bit to 0 to disable pull-down at GPIO. Set bit to 1 to enable pull-down at GPIO.
3:0	LINE_FAULT2_PD_SEL	R/W	0xC	Configure the 25 kΩ pull-down resistor for GPIO 10 - 13 when Line Fault 2 is enabled. Bit 3 - GPIO 13 Bit 2 - GPIO 12 Bit 1 - GPIO 11 Bit 0 - GPIO 10 Set bit to 0 to disable pull-down at GPIO. Set bit to 1 to enable pull-down at GPIO.

8.6.2.18.203 ADC_OFFSET_POL1 Register (Address = 0xE6) [Default = 0x00]

ADC_OFFSET_POL1 is shown in ADC_OFFSET_POL1 Register Field Descriptions.

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Table 8-1032. ADC_OFFSET_POL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1	EXT_VOL1_ADC_OFFSET_POL	R/W	0x0	Select polarity for EXT_VOL1_ADC_OFFSET 0: Positive polarity 1: Negative polarity
0	EXT_VOL0_ADC_OFFSET_POL	R/W	0x0	Select polarity for EXT_VOL0_ADC_OFFSET 0: Positive polarity 1: Negative polarity

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8.6.2.18.204 ADC_OFFSET_POL2 Register (Address = 0xE7) [Default = 0x00]

ADC_OFFSET_POL2 is shown in ADC_OFFSET_POL2 Register Field Descriptions.

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Table 8-1033. ADC_OFFSET_POL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_FAULT3_M1_ADC_OFFSET_POL	R/W	0x0	Select polarity for LINE_FAULT3_M1_ADC_OFFSET 0: Positive polarity 1: Negative polarity
6	LINE_FAULT3_M0_ADC_OFFSET_POL	R/W	0x0	Select polarity for LINE_FAULT3_M0_ADC_OFFSET 0: Positive polarity 1: Negative polarity
5	LINE_FAULT2_M1_ADC_OFFSET_POL	R/W	0x0	Select polarity for LINE_FAULT2_M1_ADC_OFFSET 0: Positive polarity 1: Negative polarity
4	LINE_FAULT2_M0_ADC_OFFSET_POL	R/W	0x0	Select polarity for LINE_FAULT2_M0_ADC_OFFSET 0: Positive polarity 1: Negative polarity
3	LINE_FAULT1_M1_ADC_OFFSET_POL	R/W	0x0	Select polarity for LINE_FAULT1_M1_ADC_OFFSET 0: Positive polarity 1: Negative polarity
2	LINE_FAULT1_M0_ADC_OFFSET_POL	R/W	0x0	Select polarity for LINE_FAULT1_M0_ADC_OFFSET 0: Positive polarity 1: Negative polarity
1	LINE_FAULT0_M1_ADC_OFFSET_POL	R/W	0x0	Select polarity for LINE_FAULT0_M1_ADC_OFFSET 0: Positive polarity 1: Negative polarity
0	LINE_FAULT0_M0_ADC_OFFSET_POL	R/W	0x0	Select polarity for LINE_FAULT0_M0_ADC_OFFSET 0: Positive polarity 1: Negative polarity

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8.6.2.19 PATGEN Registers

PATGEN Registers lists the memory-mapped registers for the PATGEN registers. All register offset addresses not listed in PATGEN Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-1034. PATGEN Registers

Address	Acronym	Register Name	Section
0x0	PGRS1	PGRS1	Go
0x1	PGRS2	PGRS2	Go
0x2	PGGS1	PGGS1	Go
0x3	PGGS2	PGGS2	Go
0x4	PGBS1	PGBS1	Go
0x5	PGBS2	PGBS2	Go
0x6	PGTFS1	PGTFS1	Go
0x7	PGTFS2	PGTFS2	Go
0x8	PGTFS3	PGTFS3	Go
0x9	PGTFS4	PGTFS4	Go
0xA	PGAFS1	PGAFS1	Go
0xB	PGAFS2	PGAFS2	Go
0xC	PGAFS3	PGAFS3	Go
0xD	PGAFS4	PGAFS4	Go
0xE	PGHSW1	PGHSW1	Go
0xF	PGHSW2	PGHSW2	Go
0x10	PGVSW1		Go
0x11	PGVSW2	PGVSW2	Go
0x12	PGHBP1	PGHBP1	Go
0x13	PGHBP2	PGHBP2	Go
0x14	PGVBP1		Go
0x15	PGVBP2	PGVBP2	Go
0x16	PBSC	PBSC	Go
0x17	PGFT	PGFT	Go
0x18	PGTSC	PGTSC	Go
0x19	PGTSO1	PGTSO1	Go
0x1A	PGTSO2	PGTSO2	Go
0x1B	PGTSO3	PGTSO3	Go
0x1C	PGTSO4	PGTSO4	Go
0x1D	PGTSO5	PGTSO5	Go
0x1E	PGTSO6	PGTSO6	Go
0x1F	PGTSO7	PGTSO7	Go
0x20	PGTSO8	PGTSO8	Go
0x21	PGTSO9	PGTSO9	Go
0x22	PGTSO10	PGTSO10	Go
0x23	PGTSO11	PGTSO11	Go
0x24	PGTSO12	PGTSO12	Go
0x25	PGTSO13	PGTSO13	Go
0x26	PGTSO14	PGTSO14	Go
0x27	PGTSO15	PGTSO15	Go
0x28	PGTSO16	PGTSO16	Go

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Table 8-1034. PATGEN Registers (continued)

Address	Acronym	Register Name	Section
0x29	PGCE	PGCE	Go
0x2A	PGUPS	PGUPS	Go
0x2B	PGCF	PGCF	Go
0x2C	PGFC	PGFC	Go
0x2D	PGCEF	PGCEF	Go

Complex bit access types are encoded to fit into small table cells. PATGEN Access Type Codes shows the codes that are used for access types in this section.

Table 8-1035. PATGEN Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.19.1 PGRS1 Register (Address = 0x0) [Default = 0x00]

PGRS1 is shown in PGRS1 Register Field Descriptions.

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Table 8-1036. PGRS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_RSP	R/W	0x0	Red Sub-Pixel: This field is the 8 least significant bits of the Red sub-pixel for the custom color. If Sub pixel bits less than 10, LSB bits are unused to generate custom color patterns. For 24 BPP: bits 1:0 are unused For 18 BPP: bits 3:0 are unused For 30 BPP: all bits are used

8.6.2.19.2 PGRS2 Register (Address = 0x1) [Default = 0x00]

PGRS2 is shown in PGRS2 Register Field Descriptions.

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Table 8-1037. PGRS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1:0	PATGEN_RSP	R/W	0x0	Red Sub-Pixel: This field is the most significant bits of the Red sub-pixel for the custom color. Configure the MSB Values for all BPP

8.6.2.19.3 PGGS1 Register (Address = 0x2) [Default = 0x00]

PGGS1 is shown in PGGS1 Register Field Descriptions.

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Table 8-1038. PGGS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_GSP	R/W	0x0	Green Sub-Pixel: This field is the 8 least significant bits of the Green sub-pixel for the custom color. If Sub pixel bits less than 10, LSB bits are unused to generate custom color patterns. For 24 BPP: bits 1:0 are unused For 18 BPP: bits 3:0 are unused For 30 BPP: all bits are used

8.6.2.19.4 PGGS2 Register (Address = 0x3) [Default = 0x00]

PGGS2 is shown in PGGS2 Register Field Descriptions.

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Table 8-1039. PGGS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1:0	PATGEN_GSP	R/W	0x0	Green Sub-Pixel: This field is the most significant bits of the Green sub-pixel for the custom color. Configure MSB Values for all BPP

8.6.2.19.5 PGBS1 Register (Address = 0x4) [Default = 0x00]

PGBS1 is shown in PGBS1 Register Field Descriptions.

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Table 8-1040. PGBS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_BSP	R/W	0x0	Blue Sub-Pixel: This field is the 8 least significant bits of the Blue sub-pixel for the custom color. If Sub pixel bits less than 10, LSB bits are unused to generate custom color patterns. For 24 BPP: bits 1:0 are unused For 18 BPP: bits 3:0 are unused For 30 BPP: all bits are used.

8.6.2.19.6 PGBS2 Register (Address = 0x5) [Default = 0x00]

PGBS2 is shown in PGBS2 Register Field Descriptions.

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Table 8-1041. PGBS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:2	RESERVED	R	0x0	Reserved
1:0	PATGEN_BSP	R/W	0x0	Blue Sub-Pixel: This field is the most significant bits of the Blue sub-pixel for the custom color. Configure MSB Values for all BPP

8.6.2.19.7 PGTFS1 Register (Address = 0x6) [Default = 0x98]

PGTFS1 is shown in PGTFS1 Register Field Descriptions.

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Table 8-1042. PGTFS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_THW	R/W	0x98	Total Horizontal Width: This field is the 8 least significant bits of the 16-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.2.19.8 PGTFS2 Register (Address = 0x7) [Default = 0x08]

PGTFS2 is shown in PGTFS2 Register Field Descriptions.

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Table 8-1043. PGTFS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_THW	R/W	0x8	Total Horizontal Width: This field is the 8 most significant bits of the 16-bit Total Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.2.19.9 PGTFS3 Register (Address = 0x8) [Default = 0x65]

PGTFS3 is shown in PGTFS3 Register Field Descriptions.

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Table 8-1044. PGTFS3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_TVW	R/W	0x65	Total Vertical Width: This field is the 8 least significant bits of the 16-bit Total Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

8.6.2.19.10 PGTFS4 Register (Address = 0x9) [Default = 0x04]

PGTFS4 is shown in PGTFS4 Register Field Descriptions.

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Table 8-1045. PGTFS4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_TVW	R/W	0x4	Total Vertical Width: This field is the 8 most significant bits of the 16-bit Total Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

8.6.2.19.11 PGAFS1 Register (Address = 0xA) [Default = 0x80]

PGAFS1 is shown in PGAFS1 Register Field Descriptions.

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Table 8-1046. PGAFS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_AHW	R/W	0x80	Active Horizontal Width: This field is the 8 least significant bits of the 16-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

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8.6.2.19.12 PGAFS2 Register (Address = 0xB) [Default = 0x07]

PGAFS2 is shown in PGAFS2 Register Field Descriptions.

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Table 8-1047. PGAFS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_AHW	R/W	0x7	Active Horizontal Width: This field is the 8 most significant bits of the 16-bit Active Horizontal Width of the frame, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.2.19.13 PGAFS3 Register (Address = 0xC) [Default = 0x38]

PGAFS3 is shown in PGAFS3 Register Field Descriptions.

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Table 8-1048. PGAFS3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_AVW	R/W	0x38	Active Vertical Width: This field is the 8 least significant bits of the 16-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

8.6.2.19.14 PGAFS4 Register (Address = 0xD) [Default = 0x04]

PGAFS4 is shown in PGAFS4 Register Field Descriptions.

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Table 8-1049. PGAFS4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_AVW	R/W	0x4	Active Vertical Width: This field is the 8 most significant bits of the 16-bit Active Vertical Width of the frame, in units of lines. This field should only be written when the pattern generator is disabled.

8.6.2.19.15 PGHSW1 Register (Address = 0xE) [Default = 0x2C]

PGHSW1 is shown in PGHSW1 Register Field Descriptions.

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Table 8-1050. PGHSW1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_HSW	R/W	0x2C	Horizontal Sync Width: This field controls the 8 least significant bits of the 12-bit Horizontal Sync pulse, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.2.19.16 PGHSW2 Register (Address = 0xF) [Default = 0x00]

PGHSW2 is shown in PGHSW2 Register Field Descriptions.

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Table 8-1051. PGHSW2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PATGEN_HSW	R/W	0x0	Horizontal Sync Width: This field controls the 4 most significant bits of the 12-bit Horizontal Sync pulse, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.2.19.17 PGVSW1 Register (Address = 0x10) [Default = 0x2C]

PGVSW1 is shown in PGVSW1 Register Field Descriptions.

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Table 8-1052. PGVSW1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_VSW	R/W	0x2C	Vertical Sync Width: This field controls the 8 least significant bits of the 12-bit Vertical Sync pulse, in units of lines. This field should only be written when the pattern generator is disabled.

8.6.2.19.18 PGVSW2 Register (Address = 0x11) [Default = 0x00]

PGVSW2 is shown in PGVSW2 Register Field Descriptions.

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Table 8-1053. PGVSW2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PATGEN_VSW	R/W	0x0	Vertical Sync Width: This field controls the 4 most significant bits of the 12-bit Vertical Sync pulse, in units of lines. This field should only be written when the pattern generator is disabled.

8.6.2.19.19 PGHBP1 Register (Address = 0x12) [Default = 0x94]

PGHBP1 is shown in PGHBP1 Register Field Descriptions.

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Table 8-1054. PGHBP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_HBP	R/W	0x94	Horizontal Back Porch Width: This field controls the 8 least significant bits of the 12-bit Horizontal Back Porch, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.2.19.20 PGHBP2 Register (Address = 0x13) [Default = 0x00]

PGHBP2 is shown in PGHBP2 Register Field Descriptions.

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Table 8-1055. PGHBP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

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Table 8-1055. PGHBP2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	PATGEN_HBP	R/W	0x0	Horizontal Back Porch Width: This field controls the 4 most significant bits of the 12-bit Horizontal Back Porch, in units of pixels. This field should only be written when the pattern generator is disabled.

8.6.2.19.21 PGVBP1 Register (Address = 0x14) [Default = 0x94]

PGVBP1 is shown in PGVBP1 Register Field Descriptions.

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Table 8-1056. PGVBP1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	RESERVED	R/W	0x94	Reserved

8.6.2.19.22 PGVBP2 Register (Address = 0x15) [Default = 0x00]

PGVBP2 is shown in PGVBP2 Register Field Descriptions.

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Table 8-1057. PGVBP2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PATGEN_VBP	R/W	0x0	Vertical Back Porch Width: This field controls the 4 most significant bits of the 12-bit Vertical Back Porch, in units of lines. This field should only be written when the pattern generator is disabled.

8.6.2.19.23 PBSC Register (Address = 0x16) [Default = 0x03]

PBSC is shown in PBSC Register Field Descriptions.

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Table 8-1058. PBSC Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R/W	0x0	Reserved
3	PATGEN_VS_DIS	R/W	0x0	Vertical Sync Disable: Disable Vertical Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
2	PATGEN_HS_DIS	R/W	0x0	Horizontal Sync Disable: Disable Horizontal Sync signaling when the pattern generator is in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
1	PATGEN_VS_POL	R/W	0x1	Vertical Sync Polarity: When 1, the pattern generator will invert the Vertical Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled.
0	PATGEN_HS_POL	R/W	0x1	Horizontal Sync Polarity: When 1, the pattern generator will invert the Horizontal Sync signal when in internal timing mode. This bit has no effect when the pattern generator is in external timing mode. This bit should only be written when the pattern generator is disabled

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8.6.2.19.24 PGFT Register (Address = 0x17) [Default = 0x1E]

PGFT is shown in PGFT Register Field Descriptions.

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Table 8-1059. PGFT Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_FTIME	R/W	0x1E	Frame Time: When Auto-Scrolling is enabled (Page 20 - register 0x01[0]), the output pattern cycles through a list of enabled pattern types instead of outputting a single static pattern. This field controls the number of frames to display each pattern in increments of two frames. Valid register values are 1-255, giving a programmable range of even numbers between 2 and 510, inclusive.

8.6.2.19.25 PGTSC Register (Address = 0x18) [Default = 0x10]

PGTSC is shown in PGTSC Register Field Descriptions.

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Table 8-1060. PGTSC Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R/W	0x0	Reserved
4:0	PATGEN_TSLOT	R/W	0x10	Time Slots: This field configures the number of enabled time slots for Auto-Scrolling. Valid Values are 1-16

8.6.2.19.26 PGTSO1 Register (Address = 0x19) [Default = 0x01]

PGTSO1 is shown in PGTSO1 Register Field Descriptions.

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Table 8-1061. PGTSO1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS1	R/W	0x1	Time Slot Pattern: This field configures the pattern enabled in Time Slot 1 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.27 PGTSO2 Register (Address = 0x1A) [Default = 0x02]

PGTSO2 is shown in PGTSO2 Register Field Descriptions.

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Table 8-1062. PGTSO2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS2	R/W	0x2	Time Slot Pattern: This field configures the pattern enabled in Time Slot 2 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

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8.6.2.19.28 PGTSO3 Register (Address = 0x1B) [Default = 0x03]

PGTSO3 is shown in PGTSO3 Register Field Descriptions.

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Table 8-1063. PGTSO3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS3	R/W	0x3	Time Slot Pattern: This field configures the pattern enabled in Time Slot 3 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.29 PGTSO4 Register (Address = 0x1C) [Default = 0x04]

PGTSO4 is shown in PGTSO4 Register Field Descriptions.

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Table 8-1064. PGTSO4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS4	R/W	0x4	Time Slot Pattern: This field configures the pattern enabled in Time Slot 4 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.30 PGTSO5 Register (Address = 0x1D) [Default = 0x05]

PGTSO5 is shown in PGTSO5 Register Field Descriptions.

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Table 8-1065. PGTSO5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS5	R/W	0x5	Time Slot Pattern: This field configures the pattern enabled in Time Slot 5 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.31 PGTSO6 Register (Address = 0x1E) [Default = 0x06]

PGTSO6 is shown in PGTSO6 Register Field Descriptions.

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Table 8-1066. PGTSO6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved

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Table 8-1066. PGTSO6 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:0	PATGEN_TS6	R/W	0x6	Time Slot Pattern: This field configures the pattern enabled in Time Slot 6 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.32 PGTSO7 Register (Address = 0x1F) [Default = 0x07]

PGTSO7 is shown in PGTSO7 Register Field Descriptions.

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Table 8-1067. PGTSO7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS7	R/W	0x7	Time Slot Pattern: This field configures the pattern enabled in Time Slot 7 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.33 PGTSO8 Register (Address = 0x20) [Default = 0x08]

PGTSO8 is shown in PGTSO8 Register Field Descriptions.

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Table 8-1068. PGTSO8 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS8	R/W	0x8	Time Slot Pattern: This field configures the pattern enabled in Time Slot 8 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.34 PGTSO9 Register (Address = 0x21) [Default = 0x09]

PGTSO9 is shown in PGTSO9 Register Field Descriptions.

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Table 8-1069. PGTSO9 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS9	R/W	0x9	Time Slot Pattern: This field configures the pattern enabled in Time Slot 9 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.35 PGTSO10 Register (Address = 0x22) [Default = 0x0A]

PGTSO10 is shown in PGTSO10 Register Field Descriptions.

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Table 8-1070. PGTSO10 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS10	R/W	0xA	Time Slot Pattern: This field configures the pattern enabled in Time Slot 10 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.36 PGTSO11 Register (Address = 0x23) [Default = 0x0B]

PGTSO11 is shown in PGTSO11 Register Field Descriptions.

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Table 8-1071. PGTSO11 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS11	R/W	0xB	Time Slot Pattern: This field configures the pattern enabled in Time Slot 11 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.37 PGTSO12 Register (Address = 0x24) [Default = 0x0C]

PGTSO12 is shown in PGTSO12 Register Field Descriptions.

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Table 8-1072. PGTSO12 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS12	R/W	0xC	Time Slot Pattern: This field configures the pattern enabled in Time Slot 12 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.38 PGTSO13 Register (Address = 0x25) [Default = 0x0D]

PGTSO13 is shown in PGTSO13 Register Field Descriptions.

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Table 8-1073. PGTSO13 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS13	R/W	0xD	Time Slot Pattern: This field configures the pattern enabled in Time Slot 13 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.39 PGTSO14 Register (Address = 0x26) [Default = 0x0E]

PGTSO14 is shown in PGTSO14 Register Field Descriptions.

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Table 8-1074. PGTSO14 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS14	R/W	0xE	Time Slot Pattern: This field configures the pattern enabled in Time Slot 14 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.40 PGTSO15 Register (Address = 0x27) [Default = 0x0F]

PGTSO15 is shown in PGTSO15 Register Field Descriptions.

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Table 8-1075. PGTSO15 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS15	R/W	0xF	Time Slot Pattern: This field configures the pattern enabled in Time Slot 15 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.41 PGTSO16 Register (Address = 0x28) [Default = 0x10]

PGTSO16 is shown in PGTSO16 Register Field Descriptions.

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Table 8-1076. PGTSO16 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PATGEN_TS16	R/W	0x10	Time Slot Pattern: This field configures the pattern enabled in Time Slot 16 when Auto-Scrolling is enabled. Valid values are any pattern supported in the PGCTL:PATGEN_SEL register field (Page 20 - register 0x00[7:3] or register 0x10[7:3]).

8.6.2.19.42 PGCE Register (Address = 0x29) [Default = 0x00]

PGCE is shown in PGCE Register Field Descriptions.

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Table 8-1077. PGCE Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_CHK_ERRS	R	0x0	Pattern Checker Errors: This field indicates the number of errors encountered during pattern checking, up to a maximum of 255. The value is cleared upon read.

8.6.2.19.43 PGUPS Register (Address = 0x2A) [Default = 0x00]

PGUPS is shown in PGUPS Register Field Descriptions.

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Table 8-1078. PGUPS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved
3:1	PATGEN_UNH1S_SCALE	R/W	0x0	Scale the divider for one-second mode of UNH compliance test pattern. By default, a pulse is provided every ~1 second to increment the line count of the UNH pattern. The 1-second duration can be scaled by ($1/2^N$) to speed up the simulation, where N is the value of this field. 000: 1 second 001: 1/2 second 010: 1/4 second 011: 1/8 second 100: 1/16 second 101: 1/32 second 110: 1/64 second 111: 1/128 second
0	PATGEN_UNH1S	R/W	0x0	Enable bit for One-Second Mode of the UNH compliance test pattern (which is selected in Page 20 - register 0x00[7:3] or register 0x10[7:3]). 0: the UNH compliance test pattern is sent out as defined in the PATGEN_UNH1S_SCALE field (register 0x2A[3:1]) 1: Each line of the UNH compliance test pattern is sent out roughly 1 second apart.

8.6.2.19.44 PGCF Register (Address = 0x2B) [Default = 0x00]

PGCF is shown in PGCF Register Field Descriptions.

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Table 8-1079. PGCF Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_CHK_FRAME_CNT	RC	0x0	Pattern Checker Frame Counts: This field indicates the number of frames received during pattern checking, up to a maximum of 255. The value is cleared upon read.

8.6.2.19.45 PGFC Register (Address = 0x2C) [Default = 0x00]

PGFC is shown in PGFC Register Field Descriptions.

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Table 8-1080. PGFC Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN__FRAME_CNT	RC	0x0	Pattern Generator Frame Counts: This field indicates the number of frames generated/detected by the pattern generator, up to a maximum of 255. The value is cleared upon read.

8.6.2.19.46 PGCEF Register (Address = 0x2D) [Default = 0x00]

PGCEF is shown in PGCEF Register Field Descriptions.

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Table 8-1081. PGCEF Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PATGEN_CHK_ERR_FRAME_CNT	RC	0x0	Pattern Checker Error Frame Counts: This field indicates the number of frames received with errors during pattern checking, up to a maximum of 255. The value is cleared upon read.

8.6.3 APB Registers

The APB registers are accessed indirectly using 0x48-0x4E.

This indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the APB_CTL register to select the desired register block and enable the APB interface
2. Write to the APB_ADR0 and APB_ADR1 registers to set the register offset
3. Write the data value to the APB_DATA1, APB_DATA2, and APB_DATA3 registers

If auto-increment is set in the APB_CTL register, repeating Step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the APB_ADR0 and APB_ADR1 registers to set the register offset
2. Write to the APB_CTL register to select the desired register block, enable the APB interface, and start APB read
3. Read the data value from the APB_DATA1, APB_DATA2, and APB_DATA3 registers

If auto-increment is set in the APB_CTL register, repeating Step 3 will read additional data bytes from subsequent register offset locations.

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8.6.3.1 UNIQUE_ID Registers

UNIQUE_ID Registers lists the memory-mapped registers for the UNIQUE_ID registers. All register offset addresses not listed in UNIQUE_ID Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-1082. UNIQUE_ID Registers

Address	Acronym	Register Name	Section
0x0	UNIQUE_ID_0	UNIQUE_ID_0	Go
0x1	UNIQUE_ID_1	UNIQUE_ID_1	Go
0x2	UNIQUE_ID_2	UNIQUE_ID_2	Go
0x3	UNIQUE_ID_3	UNIQUE_ID_3	Go
0x4	UNIQUE_ID_4	UNIQUE_ID_4	Go
0x5	UNIQUE_ID_5	UNIQUE_ID_5	Go
0x6	UNIQUE_ID_6	UNIQUE_ID_6	Go
0x7	UNIQUE_ID_7	UNIQUE_ID_7	Go
0x8	UNIQUE_ID_8	UNIQUE_ID_8	Go
0x9	UNIQUE_ID_9	UNIQUE_ID_9	Go

Complex bit access types are encoded to fit into small table cells. UNIQUE_ID Access Type Codes shows the codes that are used for access types in this section.

Table 8-1083. UNIQUE_ID Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.6.3.1.1 UNIQUE_ID_0 Register (Address = 0x0) [Default = 0x0000]

UNIQUE_ID_0 is shown in UNIQUE_ID_0 Register Field Descriptions.

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Table 8-1084. UNIQUE_ID_0 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID0	R	0x0	Contains the unique ID information byte 0 - 1. This register is read only.

8.6.3.1.2 UNIQUE_ID_1 Register (Address = 0x1) [Default = 0x0000]

UNIQUE_ID_1 is shown in UNIQUE_ID_1 Register Field Descriptions.

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Table 8-1085. UNIQUE_ID_1 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID1	R	0x0	Contains the unique ID information byte 2 - 3. This register is read only.

8.6.3.1.3 UNIQUE_ID_2 Register (Address = 0x2) [Default = 0x0000]

UNIQUE_ID_2 is shown in UNIQUE_ID_2 Register Field Descriptions.

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Table 8-1086. UNIQUE_ID_2 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID2	R	0x0	Contains the unique ID information byte 4 - 5. This register is read only.

8.6.3.1.4 UNIQUE_ID_3 Register (Address = 0x3) [Default = 0x0000]

UNIQUE_ID_3 is shown in UNIQUE_ID_3 Register Field Descriptions.

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Table 8-1087. UNIQUE_ID_3 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID3	R	0x0	Contains the unique ID information byte 6 - 7. This register is read only.

8.6.3.1.5 UNIQUE_ID_4 Register (Address = 0x4) [Default = 0x0000]

UNIQUE_ID_4 is shown in UNIQUE_ID_4 Register Field Descriptions.

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Table 8-1088. UNIQUE_ID_4 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID4	R	0x0	Contains the unique ID information byte 8 - 9. This register is read only.

8.6.3.1.6 UNIQUE_ID_5 Register (Address = 0x5) [Default = 0x0000]

UNIQUE_ID_5 is shown in UNIQUE_ID_5 Register Field Descriptions.

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Table 8-1089. UNIQUE_ID_5 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID5	R	0x0	Contains the unique ID information byte 10 - 11. This register is read only.

8.6.3.1.7 UNIQUE_ID_6 Register (Address = 0x6) [Default = 0x0000]

UNIQUE_ID_6 is shown in UNIQUE_ID_6 Register Field Descriptions.

Return to the Summary Table.

Table 8-1090. UNIQUE_ID_6 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID6	R	0x0	Contains the unique ID information byte 12 - 13. This register is read only.

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8.6.3.1.8 UNIQUE_ID_7 Register (Address = 0x7) [Default = 0x0000]

UNIQUE_ID_7 is shown in UNIQUE_ID_7 Register Field Descriptions.

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Table 8-1091. UNIQUE_ID_7 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID7	R	0x0	Contains the unique ID information byte 14 - 15. This register is read only.

8.6.3.1.9 UNIQUE_ID_8 Register (Address = 0x8) [Default = 0x0000]

UNIQUE_ID_8 is shown in UNIQUE_ID_8 Register Field Descriptions.

Return to the Summary Table.

Table 8-1092. UNIQUE_ID_8 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID8	R	0x0	Contains the unique ID information byte 16 - 17. This register is read only.

8.6.3.1.10 UNIQUE_ID_9 Register (Address = 0x9) [Default = 0x0000]

UNIQUE_ID_9 is shown in UNIQUE_ID_9 Register Field Descriptions.

Return to the Summary Table.

Table 8-1093. UNIQUE_ID_9 Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	UNIQUE_ID9	R	0x0	Contains the unique ID information byte 18 - 19. This register is read only.

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8.6.3.2 APB Registers

APB Registers lists the memory-mapped registers for the APB registers. All register offset addresses not listed in APB Registers should be considered as reserved locations and the register contents should not be modified.

Table 8-1094. APB Registers

Address	Acronym	Register Name	Section
0x0	LINK_BW_SET	LINK_BW_SET	Go
0x4	LANE_COUNT_SET	LANE_COUNT_SET	Go
0x8	ENHANCED_FRAME_EN	ENHANCED_FRAME_EN	Go
0xC	TRAINING_PATTERN_SET	TRAINING_PATTERN_SET	Go
0x10	LINK_QUAL_PATTERN_SET	LINK_QUAL_PATTERN_SET	Go
0x14	SCRAMBLING_DISABLE	SCRAMBLING_DISABLE	Go
0x1C	EDP_CAPABILITY_CONFIG	EDP_CAPABILITY_CONFIG	Go
0x20	HBR2_COMPLIANCE_SCRAMBLER_RESET	HBR2_COMPLIANCE_SCRAMBLER_RESET	Go
0x2C	LANE_REMAP_CONTROL	LANE_REMAP_CONTROL	Go
0x30	CUSTOM_80BIT_PATTERN_0	CUSTOM_80BIT_PATTERN_0	Go
0x34	CUSTOM_80BIT_PATTERN_1	CUSTOM_80BIT_PATTERN_1	Go
0x38	CUSTOM_80BIT_PATTERN_2	CUSTOM_80BIT_PATTERN_2	Go
0x80	TRANSMITTER_OUTPUT_ENABLE	TRANSMITTER_OUTPUT_ENABLE	Go
0x84	MAIN_STREAM_ENABLE	MAIN_STREAM_ENABLE	Go
0x88	SECONDARY_STREAM_ENABLE	SECONDARY_STREAM_ENABLE	Go
0x8C	SECONDARY_DATA_WINDOW	SECONDARY_DATA_WINDOW	Go
0x90	SOFT_RESET	SOFT_RESET	Go
0xC0	FORCE_SCRAMBLER_RESET	FORCE_SCRAMBLER_RESET	Go
0xC8	DATA_CONTROL	DATA_CONTROL	Go
0x100	AUX_COMMAND	AUX_COMMAND	Go
0x104	AUX_WRITE_FIFO	AUX_WRITE_FIFO	Go
0x108	AUX_ADDRESS	AUX_ADDRESS	Go
0x130	INTERRUPT_STATE	INTERRUPT_STATE	Go
0x134	AUX_REPLY_DATA	AUX_REPLY_DATA	Go
0x138	AUX_REPLY_CODE	AUX_REPLY_CODE	Go
0x13C	AUX_REPLY_COUNT	AUX_REPLY_COUNT	Go
0x140	INTERRUPT_STATUS	INTERRUPT_STATUS	Go
0x144	INTERRUPT_MASK	INTERRUPT_MASK	Go
0x148	REPLY_DATA_COUNT	REPLY_DATA_COUNT	Go
0x14C	AUX_STATUS	AUX_STATUS	Go
0x150	AUX_REPLY_CLOCK_WIDTH	AUX_REPLY_CLOCK_WIDTH	Go
0x180	MAIN_STREAM_HTOTAL	MAIN_STREAM_HTOTAL	Go
0x184	MAIN_STREAM_VTOTAL	MAIN_STREAM_VTOTAL	Go
0x188	MAIN_STREAM_POLARITY	MAIN_STREAM_POLARITY	Go
0x18C	MAIN_STREAM_HSWIDTH	MAIN_STREAM_HSWIDTH	Go
0x190	MAIN_STREAM_VSWIDTH	MAIN_STREAM_VSWIDTH	Go
0x194	MAIN_STREAM_HRES	MAIN_STREAM_HRES	Go
0x198	MAIN_STREAM_VRES	MAIN_STREAM_VRES	Go
0x19C	MAIN_STREAM_HSTART	MAIN_STREAM_HSTART	Go
0x1A0	MAIN_STREAM_VSTART	MAIN_STREAM_VSTART	Go

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Table 8-1094. APB Registers (continued)

Address	Acronym	Register Name	Section
0x1A4	MAIN_STREAM_MISC0	MAIN_STREAM_MISC0	Go
0x1A8	MAIN_STREAM_MISC1	MAIN_STREAM_MISC1	Go
0x1AC	M_VID	M_VID	Go
0x1B0	TRANSFER_UNIT_CONFIG	TRANSFER_UNIT_CONFIG	Go
0x1B4	N_VID	N_VID	Go
0x1B8	USER_PIXEL_WIDTH	USER_PIXEL_WIDTH	Go
0x1BC	USER_DATA_COUNT_PER_LANE	USER_DATA_COUNT_PER_LANE	Go
0x1C4	USER_SYNC_POLARITY	USER_SYNC_POLARITY	Go
0x1C8	USER_CONTROL	USER_CONTROL	Go
0x1CC	USER_FIFO_STATUS	USER_FIFO_STATUS	Go
0x300	SEC_AUDIO_ENABLE	SEC_AUDIO_ENABLE	Go
0x308	SEC_CHANNEL_COUNT	SEC_CHANNEL_COUNT	Go
0x318	SEC_MAUD	SEC_MAUD	Go
0x31C	SEC_NAUD	SEC_NAUD	Go
0x320	SEC_AUDIO_CLOCK_MODE	SEC_AUDIO_CLOCK_MODE	Go
0x33C	SEC_TIMESTAMP_INTERVAL	SEC_TIMESTAMP_INTERVAL	Go
0x35C	SEC_AUDIO_CHANNEL_MAP	SEC_AUDIO_CHANNEL_MAP	Go
0x370	SEC_AUDIO_FIFO_OVERFLOW	SEC_AUDIO_FIFO_OVERFLOW	Go
0x374	SEC_PACKET_COUNT	SEC_PACKET_COUNT	Go

Complex bit access types are encoded to fit into small table cells. APB Access Type Codes shows the codes that are used for access types in this section.

Table 8-1095. APB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

8.6.3.2.1 LINK_BW_SET Register (Address = 0x0) [Default = 0x00]

LINK_BW_SET is shown in LINK_BW_SET Register Field Descriptions.

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Holds the value of the main link bandwidth setting. The register uses the same values as those supported by the DPCD register of the same name in the sink device. This value is used in some PHY implementations and is unused by the digital portion of the core.

Table 8-1096. LINK_BW_SET Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINK_BW_SET	R/W	0x0	Sets the value of the main link bandwidth for the sink device. The value of this register after a reset is indeterminate. 0x06= 1.62Gbps 0x0A= 2.7 Gbps 0x0C= 3.24Gbps 0x14= 5.4Gbps

8.6.3.2.2 LANE_COUNT_SET Register (Address = 0x4) [Default = 0x00]

LANE_COUNT_SET is shown in LANE_COUNT_SET Register Field Descriptions.

Return to the Summary Table.

The transmitter uses this register to set the number of lanes that will be used to configure and operate the link. Unused lanes will not be active during training or video transmission.

Table 8-1097. LANE_COUNT_SET Register Field Descriptions

Bit	Field	Type	Default	Description
4:0	LANE_COUNT_SET	R/W	0x0	This field is equivalent to the DPCD register of the same name. Supported values are 1, 2, or 4 lanes.

8.6.3.2.3 ENHANCED_FRAME_EN Register (Address = 0x8) [Default = 0x1]

ENHANCED_FRAME_EN is shown in ENHANCED_FRAME_EN Register Field Descriptions.

Return to the Summary Table.

Enables the enhanced framing mode as supported by the DisplayPort specification.

Table 8-1098. ENHANCED_FRAME_EN Register Field Descriptions

Bit	Field	Type	Default	Description
0	ENHANCED_FRAME_EN	R/W	0x1	Set to a 1 by the source to enable the enhanced framing symbols.

8.6.3.2.4 TRAINING_PATTERN_SET Register (Address = 0xC) [Default = 0x0]

TRAINING_PATTERN_SET is shown in TRAINING_PATTERN_SET Register Field Descriptions.

Return to the Summary Table.

Settings this register to a non-zero value sets the output of the transmitter core to the specified training pattern. When set, all other main link information such as video and audio data are blocked in favor of the training pattern.

Table 8-1099. TRAINING_PATTERN_SET Register Field Descriptions

Bit	Field	Type	Default	Description
1:0	TRAINING_PATTERN_SET	R/W	0x0	Set the link training pattern according to the two bit code 00= Training off 01= Training pattern 1, clock recovery 10= Training pattern 2, interlane alignment and symbol recovery (DisplayPort 1.1a) 11= Training pattern 3, interlane alignment and symbol recovery (DisplayPort 1.2)

8.6.3.2.5 LINK_QUAL_PATTERN_SET Register (Address = 0x10) [Default = 0x0000000]

LINK_QUAL_PATTERN_SET is shown in LINK_QUAL_PATTERN_SET Register Field Descriptions.

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Return to the Summary Table.

This configuration register is used to instruct the transmitter core to enable one of the following test patterns for link quality measurements on the selected lane. These measurements are not required for the establishment and maintenance of the link and are supported for test purposes. Pattern Encoding 2:0 Enable transmission of the link quality test patterns 000= Link quality test pattern not transmitted 001= D10.2 test pattern (unscrambled) transmitted 010= Symbol Error Rate measurement pattern 011= PRBS7 transmitted 100= 80-bit custom pattern 101= HBR2 eye pattern 110= Reserved 111= Reserved

Table 8-1100. LINK_QUAL_PATTERN_SET Register Field Descriptions

Bit	Field	Type	Default	Description
26:24	LANE_3_PATTERN_SET	R/W	0x0	Link quality pattern setting for lane 3
23:19	RESERVED	R	0x0	
18:16	LANE_2_PATTERN_SET	R/W	0x0	Link quality pattern setting for lane 2
15:11	RESERVED	R	0x0	
10:8	LANE_1_PATTERN_SET	R/W	0x0	Link quality pattern setting for lane 1
7:3	RESERVED	R	0x0	
2:0	LANE_0_PATTERN_SET	R/W	0x0	Link quality pattern setting for lane 0

8.6.3.2.6 SCRAMBLING_DISABLE Register (Address = 0x14) [Default = 0x0]

SCRAMBLING_DISABLE is shown in SCRAMBLING_DISABLE Register Field Descriptions.

Return to the Summary Table.

Used to disable the internal scrambling function of the DisplayPort transmitter. This bit must be set during the link training process.

Table 8-1101. SCRAMBLING_DISABLE Register Field Descriptions

Bit	Field	Type	Default	Description
0	RESERVED	R/W	0x0	Reserved

8.6.3.2.7 EDP_CAPABILITY_CONFIG Register (Address = 0x1C) [Default = 0x0]

EDP_CAPABILITY_CONFIG is shown in EDP_CAPABILITY_CONFIG Register Field Descriptions.

Return to the Summary Table.

For embedded DisplayPort implementations, the core supports the use of the alternate scrambler reset pattern. This bit should only be enabled for embedded applications. Setting this bit in box-to-box DisplayPort applications will result in link failure.

Table 8-1102. EDP_CAPABILITY_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
1	ENABLE_REDUCED_AUX_SYNC	R/W	0x0	For eDP applications only, enabling this control bit reduces the number of sync pulses sent during AUX channel transactions from 16 to 8.
0	ALTERNATE_SCRAMBLER_RESET	R/W	0x0	Set this bit to a 1 to force the transmitter core to use the alternate scrambler reset value.

8.6.3.2.8 HBR2_COMPLIANCE_SCRAMBLER_RESET Register (Address = 0x20) [Default = 0x0000]

HBR2_COMPLIANCE_SCRAMBLER_RESET is shown in HBR2_COMPLIANCE_SCRAMBLER_RESET Register Field Descriptions.

Return to the Summary Table.

Defines the interval for the transmission of the scrambler reset pattern during the transmission of the HBR2 compliance link quality pattern.

Table 8-1103. HBR2_COMPLIANCE_SCRAMBLER_RESET Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	HBR2_COMPLIANCE_SCRAMBLER_RESET	R/W	0x0	The value of this register should be set to the same value as reported by the DisplayPort sink device through the DPCD register address 0x0024A-0x0024B.

8.6.3.2.9 LANE_REMAP_CONTROL Register (Address = 0x2C) [Default = 0x00000]

LANE_REMAP_CONTROL is shown in LANE_REMAP_CONTROL Register Field Descriptions.

Return to the Summary Table.

Used to map the physical lanes of the DisplayPort link to the internal symbol lanes of the controller. Using these register bits, any of the four physical lanes may be mapped to any other internal lane for processing. For lane remapping, Page_2 register 0x90[4] needs set to 1 and 0x90[3:0] need set based on active lanes. Data transmitted on each lane may also be inverted.

Table 8-1104. LANE_REMAP_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
19	INVERT_LANE_3	R/W	0x0	Inverts the state of all bits transmitted to the PHY layer on lane 3.
18	INVERT_LANE_2	R/W	0x0	Inverts the state of all bits transmitted to the PHY layer on lane 2.
17	INVERT_LANE_1	R/W	0x0	Inverts the state of all bits transmitted to the PHY layer on lane 1.
16	INVERT_LANE_0	R/W	0x0	Inverts the state of all bits transmitted to the PHY layer on lane 0.
15:9	RESERVED	R	0x0	
8	REMAP_ENABLE	R/W	0x0	Set to a '1 ' to enable the remapping function. When set to a '0 ', bits 7:0 of the LANE_REMAP control register will be ignored.
7:6	REMAP_LANE_3	R/W	0x0	Specifies which internal lane number (0-3) will be mapped to the PHY lane 3.
5:4	REMAP_LANE_2	R/W	0x0	Specifies which internal lane number (0-3) will be mapped to the PHY lane 2.
3:2	REMAP_LANE_1	R/W	0x0	Specifies which internal lane number (0-3) will be mapped to the PHY lane 1.
1:0	REMAP_LANE_0	R/W	0x0	Specifies which internal lane number (0-3) will be mapped to the PHY lane 0.

8.6.3.2.10 CUSTOM_80BIT_PATTERN_0 Register (Address = 0x30) [Default = 0x00000000]

CUSTOM_80BIT_PATTERN_0 is shown in CUSTOM_80BIT_PATTERN_0 Register Field Descriptions.

Return to the Summary Table.

Contains the least significant thirty-two bits of the 80-bit custom pattern used in link quality testing. These bits should not be modified while the link quality pattern is active.

Table 8-1105. CUSTOM_80BIT_PATTERN_0 Register Field Descriptions

Bit	Field	Type	Default	Description
31:0	CUSTOM_80BIT_PATTERN_0	R/W	0x0	Bits 31:0 of the 80-bit custom pattern.

8.6.3.2.11 CUSTOM_80BIT_PATTERN_1 Register (Address = 0x34) [Default = 0x00000000]

CUSTOM_80BIT_PATTERN_1 is shown in CUSTOM_80BIT_PATTERN_1 Register Field Descriptions.

Return to the Summary Table.

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Contains the middle thirty-two bits of the 80-bit custom pattern used in link quality testing. These bits should not be modified while the link quality pattern is active.

Table 8-1106. CUSTOM_80BIT_PATTERN_1 Register Field Descriptions

Bit	Field	Type	Default	Description
31:0	CUSTOM_80BIT_PATTERN_1	R/W	0x0	Bits 63:32 of the 80-bit custom pattern.

8.6.3.2.12 CUSTOM_80BIT_PATTERN_2 Register (Address = 0x38) [Default = 0x00000000]

CUSTOM_80BIT_PATTERN_2 is shown in CUSTOM_80BIT_PATTERN_2 Register Field Descriptions.

Return to the Summary Table.

Contains the most significant sixteen bits of the 80-bit custom pattern used in link quality testing. These bits should not be modified while the link quality pattern is active.

Table 8-1107. CUSTOM_80BIT_PATTERN_2 Register Field Descriptions

Bit	Field	Type	Default	Description
31:0	CUSTOM_80BIT_PATTERN_2	R/W	0x0	Bits 79:64 of the 80-bit custom pattern.

8.6.3.2.13 TRANSMITTER_OUTPUT_ENABLE Register (Address = 0x80) [Default = 0x0]

TRANSMITTER_OUTPUT_ENABLE is shown in TRANSMITTER_OUTPUT_ENABLE Register Field Descriptions.

Return to the Summary Table.

This bit is used to disable all output of the main link framing logic. When set to 0, the transmitter core will output only stuffing symbols onto the link. No control symbols or valid link data are transmitted when disabled. This bit prevents the link controller core from interfering with the PHY power up sequence.

Table 8-1108. TRANSMITTER_OUTPUT_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
0	TRANSMITTER_OUTPUT_ENABLE	R/W	0x0	Set to a 1 after the link output has been configured and the external PHY is ready to begin operations.

8.6.3.2.14 MAIN_STREAM_ENABLE Register (Address = 0x84) [Default = 0x0]

MAIN_STREAM_ENABLE is shown in MAIN_STREAM_ENABLE Register Field Descriptions.

Return to the Summary Table.

Once the link is properly trained and is ready to begin transmitting user video data, this bit may be written to a 1. Prior to receiving a vertical sync pulse on the associated video input port, the DisplayPort transmitter will output the No Video pattern for the selected lane.

Table 8-1109. MAIN_STREAM_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
0	MAIN_STREAM_ENABLE	R/W	0x0	When set to 0, the active lanes of the DisplayPort transmitter will output only stuffing characters on the link for the associated video port.

8.6.3.2.15 SECONDARY_STREAM_ENABLE Register (Address = 0x88) [Default = 0x0]

SECONDARY_STREAM_ENABLE is shown in SECONDARY_STREAM_ENABLE Register Field Descriptions.

Return to the Summary Table.

When the host system is ready to begin the transmission of secondary packets including audio information, this bit is written to a 1. When set to 0, the active lanes of the DisplayPort transmitter will not send secondary data as a part of the stream.

Table 8-1110. SECONDARY_STREAM_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
0	SECONDARY_STREAM_ENABLE	R/W	0x0	A value of 0 in this register will disable secondary data and will set the AudioMute flag in the VB-ID to a 1.

8.6.3.2.16 SECONDARY_DATA_WINDOW Register (Address = 0x8C) [Default = 0x000]

SECONDARY_DATA_WINDOW is shown in SECONDARY_DATA_WINDOW Register Field Descriptions.

Return to the Summary Table.

Specifies the width in link symbol clocks of the horizontal blanking window during which secondary channel data packets are allowed to be transmitted.

Table 8-1111. SECONDARY_DATA_WINDOW Register Field Descriptions

Bit	Field	Type	Default	Description
11:0	SECONDARY_DATA_WINDOW	R/W	0x0	Width of the data valid window. This value should be set using the following equation. Reg= HBLANK_PERIOD / LINK_SYMBOL_CLOCK * 0.9

8.6.3.2.17 SOFT_RESET Register (Address = 0x90) [Default = 0x0]

SOFT_RESET is shown in SOFT_RESET Register Field Descriptions.

Return to the Summary Table.

Performs a soft reset of specific core management functions. This reset only applies to the control portions of the core. The state of the programmable register set is not affected by the soft reset.

Table 8-1112. SOFT_RESET Register Field Descriptions

Bit	Field	Type	Default	Description
1	VIDEO_SOFT_RESET	RH/W1S	0x0	Writing a 1 performs a soft reset of the video capture section. This bit is self-clearing.
0	LINK_SOFT_RESET	RH/W1S	0x0	Writing a 1 performs a soft reset of the link management section. This bit is self-clearing.

8.6.3.2.18 FORCE_SCRAMBLER_RESET Register (Address = 0xC0) [Default = 0x0]

FORCE_SCRAMBLER_RESET is shown in FORCE_SCRAMBLER_RESET Register Field Descriptions.

Return to the Summary Table.

Typically used for debug purposes, this register allows the host processor to force the link controller to insert a scrambler reset symbol into the stream. In normal operation, the scrambler reset replaces the blanking start symbol. When set to a 1, the link controller will replace the next scheduled blanking start symbol with a scrambler reset symbol.

Table 8-1113. FORCE_SCRAMBLER_RESET Register Field Descriptions

Bit	Field	Type	Default	Description
0	FORCE_SCRAMBLER_RESET	W	0x0	Write to a 1 to force a scrambler reset for debug purposes. This bit is write only and will always read back as a 0.

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8.6.3.2.19 DATA_CONTROL Register (Address = 0xC8) [Default = 0x00000000]

DATA_CONTROL is shown in DATA_CONTROL Register Field Descriptions.

Return to the Summary Table.

Controls the internal user data path by allowing pixels to accumulate inside the core before transmitting.

Table 8-1114. DATA_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
30:24	RESERVED	R/W	0x0	Reserved
23:22	RESERVED	R	0x0	
21:16	RESERVED	R/W	0x0	Reserved
15:8	DATA_ACCUMULATION_DELAY	R/W	0x0	Specifies the number of link clock cycles for the internal data path controller to wait before sending the first TU of an active line after detecting that valid data is ready to be transmitted. All seven bits are RW, however, the internal logic will only recognize even multiples of 4 for this register. Bits 9 and 8 will be ignored by the internal framing logic.
7:6	RESERVED	R/W	0x0	Reserved
5:0	FIFO_ACCUMULATION_DEPTH	R/W	0x0	Specifies the number of words that must accumulate inside the data path FIFO before attempting to send a valid data packet on the link. This value is only valid once per line during the first active data packet.

8.6.3.2.20 AUX_COMMAND Register (Address = 0x100) [Default = 0x0000]

AUX_COMMAND is shown in AUX_COMMAND Register Field Descriptions.

Return to the Summary Table.

Initiates an AUX channel command of the specified length when written. This register is written last as part of the AUX channel request set up process. When written, the internal state machines will begin transmitting the request to the sink device. The AUX_ADDRESS and, when applicable, the AUX_WRITE_FIFO must be set up before writing this register.

Table 8-1115. AUX_COMMAND Register Field Descriptions

Bit	Field	Type	Default	Description
12	ADDRESS_ONLY	R/W	0x0	Set to a 1 to initiate an address only request.
11:8	COMMAND	R/W	0x0	AUX Channel Command. The field is equivalent to the commands defined in section 2.4.1 of the DisplayPort specification. 0x8= AUX Write 0x9= AUX Read 0x0= I2C over AUX Write 0x4= I2C over AUX Write, Middle of Transaction bit set 0x1= I2C over AUX Read 0x5= I2C over AUX Read, Middle of Transaction bit set 0x2= I2C over AUX Write Status
7:4	RESERVED	R	0x0	
3:0	BYTE_COUNT	R/W	0x0	Specifies the number of bytes to transfer with the current command. The range of the register is 0 to 15 indicating between 1 and 16 bytes of data.

8.6.3.2.21 AUX_WRITE_FIFO Register (Address = 0x104) [Default = 0x00]

AUX_WRITE_FIFO is shown in AUX_WRITE_FIFO Register Field Descriptions.

Return to the Summary Table.

Before initiating a native or I2C write request on the AUX channel, the host system must provide the write data to the FIFO mapped to this address. Only the number of bytes required to support the current transaction must be written to the FIFO. Subsequent writes to the FIFO must not be performed until the REQUEST_IN_PROGRESS bit is clear.

Table 8-1116. AUX_WRITE_FIFO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	AUX_WRITE_FIFO	W	0x0	Write only AUX Channel byte data. A read from this register is not supported, but will return the last data byte written.

8.6.3.2.22 AUX_ADDRESS Register (Address = 0x108) [Default = 0x00000]

AUX_ADDRESS is shown in AUX_ADDRESS Register Field Descriptions.

Return to the Summary Table.

Each AUX request requires a 20-bit address for native AUX requests or an 8-bit address for I2C over AUX requests. This register specifies the address for the current AUX channel command. These bits are used without modification for the address field of the request.

Table 8-1117. AUX_ADDRESS Register Field Descriptions

Bit	Field	Type	Default	Description
19:0	AUX_ADDRESS	R/W	0x0	Twenty bit address for the start of the AUX Channel burst.

8.6.3.2.23 INTERRUPT_STATE Register (Address = 0x130) [Default = 0x0]

INTERRUPT_STATE is shown in INTERRUPT_STATE Register Field Descriptions.

Return to the Summary Table.

Holds status bits which report the internal state of the AUX channel management logic. Some of these signals are used to generate interrupts and can be used as polled status for systems that do not implement interrupts..

Table 8-1118. INTERRUPT_STATE Register Field Descriptions

Bit	Field	Type	Default	Description
3	REPLY_TIMEOUT	R	0x0	A 1 indicates that a reply timeout has occurred.
2	REPLY_RECEIVED	R	0x0	A 1 indicates that a reply has been received.
1	REQUEST_IN_PROGRESS	R	0x0	A 1 indicates that a request is currently being sent by the AUX request controller.
0	HPD_STATE	R	0x0	Contains the raw state of the HPD pin on the DisplayPort connector.

8.6.3.2.24 AUX_REPLY_DATA Register (Address = 0x134) [Default = 0x00]

AUX_REPLY_DATA is shown in AUX_REPLY_DATA Register Field Descriptions.

Return to the Summary Table.

This read only address maps to the internal FIFO which contains up to 16 bytes of information received during the AUX channel reply. Reply data is read from the FIFO starting with byte 0. The number of valid bytes in the FIFO corresponds to the number of bytes received as indicated by the REPLY_DATA_COUNT register.

Table 8-1119. AUX_REPLY_DATA Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	AUX_REPLY_DATA	R	0x0	AUX reply data from the sink device. Each read advances the internal read pointer.

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8.6.3.2.25 AUX_REPLY_CODE Register (Address = 0x138) [Default = 0x0]

AUX_REPLY_CODE is shown in AUX_REPLY_CODE Register Field Descriptions.

Return to the Summary Table.

Contains the reply code received from the most recent AUX Channel request. This code is the four bit field received by the reply controller from the sink device. The value of the code maps to the DisplayPort specification section 2.4.1.2 which is repeated below for clarity.

Table 8-1120. AUX_REPLY_CODE Register Field Descriptions

Bit	Field	Type	Default	Description
3:0	AUX_REPLY_CODE	R	0x0	AUX channel reply code received from the sink device. 0x0= Native AUX ACK 0x1= Native AUX NACK 0x2= Native AUX Defer 0x0= I2C over AUX ACK 0x4= I2C over AUX NACK 0x8= I2C over AUX Defer

8.6.3.2.26 AUX_REPLY_COUNT Register (Address = 0x13C) [Default = 0x00]

AUX_REPLY_COUNT is shown in AUX_REPLY_COUNT Register Field Descriptions.

Return to the Summary Table.

Provides an internal count of the number of reply transactions received on the AUX Channel. Each reply received from the sink device increments the count by 1. The reply code is not considered when incrementing this counter. Writing a 1 to this register clears the count.

Table 8-1121. AUX_REPLY_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	AUX_REPLY_COUNT	R/W	0x0	Current reply count. The value of this register will automatically roll over after reaching 255 replies received. Write a 1 to this bit to clear the value

8.6.3.2.27 INTERRUPT_STATUS Register (Address = 0x140) [Default = 0x0]

INTERRUPT_STATUS is shown in INTERRUPT_STATUS Register Field Descriptions.

Return to the Summary Table.

The transmitter core interrupt status register contains the cause of an interrupt asserted by the core. The specific events that can cause an interrupt and the associated status bits are shown below. A read from this register clears all values.

Table 8-1122. INTERRUPT_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
3	REPLY_TIMEOUT	R/W	0x0	A reply timeout has occurred when the sink has not sent a response 400us after the transmitter has sent a request.
2	REPLY_RECIEVED	R/W	0x0	An AUX reply transaction has been detected. This value may be used to allow a system to process other events while waiting for a response from the sink device.
1	HPD_EVENT	R/W	0x0	The core has detected the presence of the HPD signal. This interrupt asserts immediately after the detection of HPD and after the loss of HPD for 2 msec.
0	HPD_IRQ	R/W	0x0	An IRQ framed with the proper timing on the HPD signal has been detected.

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8.6.3.2.28 INTERRUPT_MASK Register (Address = 0x144) [Default = 0xF]

INTERRUPT_MASK is shown in INTERRUPT_MASK Register Field Descriptions.

Return to the Summary Table.

Each interrupt source for the transmitter core may be individually masked. When the corresponding bit in this register is set to a 1, an interrupt will not be generated for the event. At power up, all of the interrupt sources are masked and this register will have a value of 0xF.

Table 8-1123. INTERRUPT_MASK Register Field Descriptions

Bit	Field	Type	Default	Description
3	REPLY_TIMEOUT_MASK	R/W	0x1	Write a 0 to this bit to allow reply timeout events to cause an interrupt to be asserted.
2	REPLY_RECEIVED_MASK	R/W	0x1	Write a 0 to this bit to allow reply received events to cause an interrupt.
1	HPD_EVENT_MASK	R/W	0x1	Write a 0 to this bit to allow HPD present events to cause an interrupt.
0	HPD_IRQ_EVENT	R/W	0x1	Write a 0 to this bit to allow HPD_IRQ events to cause an interrupt.

8.6.3.2.29 REPLY_DATA_COUNT Register (Address = 0x148) [Default = 0x00]

REPLY_DATA_COUNT is shown in REPLY_DATA_COUNT Register Field Descriptions.

Return to the Summary Table.

Returns the total number of data bytes received during a reply transaction from the sink device. This register does not use the length byte of the transaction header. The number of bytes is independently counted by the reply controller. The value of this register is cleared when a request transaction is initiated by the transmitter.

Table 8-1124. REPLY_DATA_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
4:0	REPLY_DATA_COUNT	R/W	0x0	Total number of data bytes received during the reply phase of the AUX transaction.

8.6.3.2.30 AUX_STATUS Register (Address = 0x14C) [Default = 0x0]

AUX_STATUS is shown in AUX_STATUS Register Field Descriptions.

Return to the Summary Table.

This register contains the status of the internal AUX channel controllers. The progress of request and reply transactions are monitored an reply transactions are checked for errors. These bits are valid at all times.

Table 8-1125. AUX_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
3	REPLY_ERROR	R	0x0	When set to a 1, the AUX reply logic has detected an error in the reply to the most recent AUX transaction. Errors are detected when the precharge and sync phases of the reply last more than 38 cycles instead of the maximum 32. This condition typically indicates noise on the AUX channel data signals.
2	REQUEST_IN_PROGRESS	R	0x0	The AUX transaction request controller sets this bit to a 1 while actively transmitting a request on the AUX channel. The bit is set to 0 when the AUX transaction request controller is idle.
1	REPLY_IN_PROGRESS	R	0x0	The AUX reply detection logic sets this bit to a 1 while receiving a reply on the AUX channel. The bit is 0 otherwise.

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Table 8-1125. AUX_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	REPLY_RECEIVED	R	0x0	This bit is set to 0 when the AUX request controller begins sending bits on the AUX serial bus. The AUX reply controller sets this bit to 1 when a complete and valid reply transaction has been received. This bit is cleared when a request transaction has been initiated by the request controller.

8.6.3.2.31 AUX_REPLY_CLOCK_WIDTH Register (Address = 0x150) [Default = 0x000]

AUX_REPLY_CLOCK_WIDTH is shown in AUX_REPLY_CLOCK_WIDTH Register Field Descriptions.

Return to the Summary Table.

Reports the width of the AUX channel reply clock in APB_CLK cycles. This register is only valid after a properly formatted reply transaction has been received. The clock width is measured during the sync stage of the AUX channel transaction.

Table 8-1126. AUX_REPLY_CLOCK_WIDTH Register Field Descriptions

Bit	Field	Type	Default	Description
9:0	AUX_REPLY_CLOCK_WIDTH	R	0x0	Width of the AUX channel receive clock in APB_CLK cycles.

8.6.3.2.32 MAIN_STREAM_HTOTAL Register (Address = 0x180) [Default = 0x0000]

MAIN_STREAM_HTOTAL is shown in MAIN_STREAM_HTOTAL Register Field Descriptions.

Return to the Summary Table.

Specifies the total number of clocks in the horizontal framing period for the main stream video signal. This value is sent as the Main Stream Attribute Htotal.

Table 8-1127. MAIN_STREAM_HTOTAL Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	MAIN_STREAM_HTOTAL	R/W	0x0	Horizontal line length total in clocks.

8.6.3.2.33 MAIN_STREAM_VTOTAL Register (Address = 0x184) [Default = 0x0000]

MAIN_STREAM_VTOTAL is shown in MAIN_STREAM_VTOTAL Register Field Descriptions.

Return to the Summary Table.

Provides the total number of lines between vertical sync pulses in the main stream video frame. This value is provided as the Main Stream Attribute Vtotal.

Table 8-1128. MAIN_STREAM_VTOTAL Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	MAIN_STREAM_VTOTAL	R/W	0x0	Total number of lines per video frame.

8.6.3.2.34 MAIN_STREAM_POLARITY Register (Address = 0x188) [Default = 0x0]

MAIN_STREAM_POLARITY is shown in MAIN_STREAM_POLARITY Register Field Descriptions.

Return to the Summary Table.

Provides the polarity values for the video horizontal and vertical sync signals. These bits are sent as a part of the Main Stream Attributes as VSP and HSP.

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Table 8-1129. MAIN_STREAM_POLARITY Register Field Descriptions

Bit	Field	Type	Default	Description
1	VSYNC_POLARITY	R/W	0x0	Polarity of the vertical sync pulse.
0	HSYNC_POLARITY	R/W	0x0	Polarity of the horizontal sync pulse.

8.6.3.2.35 MAIN_STREAM_HSWIDTH Register (Address = 0x18C) [Default = 0x0000]

MAIN_STREAM_HSWIDTH is shown in MAIN_STREAM_HSWIDTH Register Field Descriptions.

Return to the Summary Table.

Sets the width of the horizontal sync pulse measured in pixel clock periods. This value is provided on the link as the Main Stream Attribute field HSW.

Table 8-1130. MAIN_STREAM_HSWIDTH Register Field Descriptions

Bit	Field	Type	Default	Description
14:0	MAIN_STREAM_HSWIDTH	R/W	0x0	Horizontal sync width in clock cycles.

8.6.3.2.36 MAIN_STREAM_VSWIDTH Register (Address = 0x190) [Default = 0x0000]

MAIN_STREAM_VSWIDTH is shown in MAIN_STREAM_VSWIDTH Register Field Descriptions.

Return to the Summary Table.

Sets the width of the vertical sync pulse in lines. The Main Stream Attribute VSW is used to carry this information on the link.

Table 8-1131. MAIN_STREAM_VSWIDTH Register Field Descriptions

Bit	Field	Type	Default	Description
14:0	MAIN_STREAM_VSWIDTH	R/W	0x0	Width of the vertical sync in lines.

8.6.3.2.37 MAIN_STREAM_HRES Register (Address = 0x194) [Default = 0x0000]

MAIN_STREAM_HRES is shown in MAIN_STREAM_HRES Register Field Descriptions.

Return to the Summary Table.

Horizontal resolution of the main stream video source. This value is the number of active pixels per line and is represented in the Main Stream Attributes as the HWidth field.

Table 8-1132. MAIN_STREAM_HRES Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	MAIN_STREAM_HRES	R/W	0x0	Number of active pixels per line of the main stream video.

8.6.3.2.38 MAIN_STREAM_VRES Register (Address = 0x198) [Default = 0x0000]

MAIN_STREAM_VRES is shown in MAIN_STREAM_VRES Register Field Descriptions.

Return to the Summary Table.

Vertical resolution of the main stream video source. The resolution is the number of active lines per frame. The Main Stream Attribute field Vheight carries this information to the sink.

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Table 8-1133. MAIN_STREAM_VRES Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	MAIN_STREAM_VRES	R/W	0x0	Number of active lines of video in the main stream video source.

8.6.3.2.39 MAIN_STREAM_HSTART Register (Address = 0x19C) [Default = 0x0000]

MAIN_STREAM_HSTART is shown in MAIN_STREAM_HSTART Register Field Descriptions.

Return to the Summary Table.

Specifies the number of clocks between the leading edge of the horizontal sync and the start of active data. This value is used for the Main Stream Attribute Hstart and is measured in pixel clocks.

Table 8-1134. MAIN_STREAM_HSTART Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	MAIN_STREAM_HSTART	R/W	0x0	Horizontal start clock count. Includes the HSW and HBP time periods.

8.6.3.2.40 MAIN_STREAM_VSTART Register (Address = 0x1A0) [Default = 0x0000]

MAIN_STREAM_VSTART is shown in MAIN_STREAM_VSTART Register Field Descriptions.

Return to the Summary Table.

Number of lines between the leading edge of the vertical sync and the first line of active data. This value is carried in the Main Stream Attributes as the Vstart field.

Table 8-1135. MAIN_STREAM_VSTART Register Field Descriptions

Bit	Field	Type	Default	Description
15:0	MAIN_STREAM_VSTART	R/W	0x0	Vertical start line count. Includes the VSW and VBP time periods.

8.6.3.2.41 MAIN_STREAM_MISC0 Register (Address = 0x1A4) [Default = 0x00]

MAIN_STREAM_MISC0 is shown in MAIN_STREAM_MISC0 Register Field Descriptions.

Return to the Summary Table.

This 8-bit value contains information about the main link video stream clocking and color representation. These bits are mapped from the DisplayPort specification MISC0 register definitions.

Table 8-1136. MAIN_STREAM_MISC0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	BIT_DEPTH	R/W	0x0	Number of bits per color. 000= 6 bits 001= 8 bits 010= 10 bits 011= Reserved 100= Reserved 101, 110, 111= Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2:1	COMPONENT_FORMAT	R/W	0x0	Color representation format. 00= RGB 01= YCbCr 4:2:2 10= YCbCr 4:4:4 11= Reserved
0	RESERVED	R/W	0x0	Reserved

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8.6.3.2.42 MAIN_STREAM_MISC1 Register (Address = 0x1A8) [Default = 0x00]

MAIN_STREAM_MISC1 is shown in MAIN_STREAM_MISC1 Register Field Descriptions.

Return to the Summary Table.

These bits represent the Main Stream Attribute field MISC1 as defined in the DisplayPort specification. These bits provide interlaced and stereo video information.

Table 8-1137. MAIN_STREAM_MISC1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	ZERO	R/W	0x0	This field must be set to a 0 for proper operation. Any other value in this field may cause unpredictable operation.
2:1	STEREO_VIDEO_ATTRIBUTE	R/W	0x0	Stereo attribute for 3D video support. 00= No stereo video transported 01= Top field or frame is for the RIGHT eye 10= Reserved 11= Top field or frame is for the LEFT eye
0	INTERLACED_TOTAL_EVEN	R/W	0x0	Indicates the number of lines per interlaced frame. 0= number of lines per interlaced frame is odd 1= number of lines per interlaced frame is even

8.6.3.2.43 M_VID Register (Address = 0x1AC) [Default = 0x000000]

M_VID is shown in M_VID Register Field Descriptions.

Return to the Summary Table.

The clocking values for the main stream video must be calculated by the host processor and provided in this register for transmission to the sink device.

Table 8-1138. M_VID Register Field Descriptions

Bit	Field	Type	Default	Description
23:0	M_VID	R/W	0x0	Unsigned value computed for clock divider using PCLK and DP/eDP rate

8.6.3.2.44 TRANSFER_UNIT_CONFIG Register (Address = 0x1B0) [Default = 0x0000020]

TRANSFER_UNIT_CONFIG is shown in TRANSFER_UNIT_CONFIG Register Field Descriptions.

Return to the Summary Table.

A transfer unit is a DisplayPort micro-packet and represents valid data symbols and stuffing symbols. This register value sets the size of a transfer unit in the transmitter framing logic. Due to the design of the core, only even values are supported by this register.

Table 8-1139. TRANSFER_UNIT_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
27:24	FRAC_SYMBOLS_PER_TU	R/W	0x0	sets the fractional number of valid symbols per TU in units of 1/16th. An accumulator is used to increase the number of data per transaction unit by 1 every 1/N Transaction Units.
23:16	SYMBOLS_PER_TU	R/W	0x0	Configures the number of valid symbols to transmit with each transaction unit. See Section 2.2.1.4.1 of the DisplayPort specification for an example that computes this value or set to 64 (0x40) for automatic rate management.
15:7	RESERVED	R	0x0	

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Table 8-1139. TRANSFER_UNIT_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	TRANSFER_UNIT_SIZE	R/W	0x20	This number must be in the range of 32 to 64 for DisplayPort compliance and is typically set to a fixed value which depends on the inbound video mode. Larger values should be used for video modes with slower pixel clock rates. Smaller values should be used for video modes with higher pixel clock rates.

8.6.3.2.45 N_VID Register (Address = 0x1B4) [Default = 0x000000]

N_VID is shown in N_VID Register Field Descriptions.

Return to the Summary Table.

Table 8-1140. N_VID Register Field Descriptions

Bit	Field	Type	Default	Description
23:0	N_VID	R/W	0x0	Set to a fixed value of 32768 for clock calculation

8.6.3.2.46 USER_PIXEL_WIDTH Register (Address = 0x1B8) [Default = 0x1]

USER_PIXEL_WIDTH is shown in USER_PIXEL_WIDTH Register Field Descriptions.

Return to the Summary Table.

The user data interface to the transmitter core accepts either one or two pixels per clock cycle. This register selects the width of the user data input port and should be set before main link video is enabled. At reset, this register defaults to 1.

Table 8-1141. USER_PIXEL_WIDTH Register Field Descriptions

Bit	Field	Type	Default	Description
1:0	USER_PIXEL_WIDTH	R/W	0x1	Set to a value of 1 for a single pixel wide interface or 2 for a dual pixel wide interface.

8.6.3.2.47 USER_DATA_COUNT_PER_LANE Register (Address = 0x1BC) [Default = 0x00000]

USER_DATA_COUNT_PER_LANE is shown in USER_DATA_COUNT_PER_LANE Register Field Descriptions.

Return to the Summary Table.

Determines the total data count for the transmitter framing logic to read from the user FIFO before sending a blanking start symbol. In other words, this value is the total number of 16-bit words in a line of active data. The calculated value should be rounded up.

Table 8-1142. USER_DATA_COUNT_PER_LANE Register Field Descriptions

Bit	Field	Type	Default	Description
17:0	USER_DATA_COUNT_PER_LANE	R/W	0x0	Sets the number of video data symbols per line of active.

8.6.3.2.48 USER_SYNC_POLARITY Register (Address = 0x1C4) [Default = 0xF]

USER_SYNC_POLARITY is shown in USER_SYNC_POLARITY Register Field Descriptions.

Return to the Summary Table.

Indicates the polarity of the video source sync signals. Set each bit to a 1 for active high or a 0 for active low.

Table 8-1143. USER_SYNC_POLARITY Register Field Descriptions

Bit	Field	Type	Default	Description
3	RESERVED	R/W	0x1	Reserved
2	USER_DATA_ENABLE_POLARITY	R/W	0x1	Polarity of the input user data enable signal.
1	USER_VSYNC_POLARITY	R/W	0x1	Polarity of the input user vertical sync pulse.
0	USER_HSYNC_POLARITY	R/W	0x1	Polarity of the input user horizontal sync pulse.

8.6.3.2.49 USER_CONTROL Register (Address = 0x1C8) [Default = 0x0]

USER_CONTROL is shown in USER_CONTROL Register Field Descriptions.

Return to the Summary Table.

Controls the behavior of the DisplayPort link packet framing logic.

Table 8-1144. USER_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
2	BYPASS_NO_VIDEO_DELAY	R/W	0x0	By default, the transmitter SST framing logic waits for the transmission of 5 NO_VIDEO symbol patterns as required by the DisplayPort specification. This control bit is intended for debug purposes only and disables that delay.
1	USER_STREAM_ENABLE_NO_VSYNC	R/W	0x0	When set to a 1, the main and secondary streams become active immediately rather than waiting for the next input vertical sync pulse.
0	USER_SPARSE_MODE_ENABLE	R/W	0x0	A variable number of valid data symbols per transaction unit are supported when this bit is set to a 1. The value of the SYMBOLS_PER_TU and FRAC_SYMBOLS_PER_TU fields of the TRANSFER_UNIT_CONFIG register will be ignored when the sparse mode is enabled.

8.6.3.2.50 USER_FIFO_STATUS Register (Address = 0x1CC) [Default = 0x0]

USER_FIFO_STATUS is shown in USER_FIFO_STATUS Register Field Descriptions.

Return to the Summary Table.

These R bits report the internal status of the video data FIFO buffers. A one in either of these bits indicates a programming error for the current video mode. These bits are cleared at the input vsync of every frame.

Table 8-1145. USER_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
1	OVERFLOW	R	0x0	A 1 indicates that the internal user FIFO has detected a video data underflow condition. This can occur if the TU transmit data rate is greater than the input data rate.
0	UNDERFLOW	R	0x0	A 1 indicates that the internal user FIFO has detected an overflow condition. This can occur if the TU transmit data rate is less than the input data rate.

8.6.3.2.51 SEC_AUDIO_ENABLE Register (Address = 0x300) [Default = 0x0]

SEC_AUDIO_ENABLE is shown in SEC_AUDIO_ENABLE Register Field Descriptions.

Return to the Summary Table.

Single bit register to enable support of secondary channel audio. This bit can be used to globally enable or disable secondary channel audio packets. When set to a 0, the audio mute bit in the VBID will also be set.

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Table 8-1146. SEC_AUDIO_ENABLE Register Field Descriptions

Bit	Field	Type	Default	Description
0	SEC_AUDIO_ENABLE	R/W	0x0	Writing a 1 to this bit will globally enable the secondary channel audio functions. The control registers should be properly set before enabling the secondary channel audio.

8.6.3.2.52 SEC_CHANNEL_COUNT Register (Address = 0x308) [Default = 0x0]

SEC_CHANNEL_COUNT is shown in SEC_CHANNEL_COUNT Register Field Descriptions.

Return to the Summary Table.

Used to select the number of audio channels included in the secondary audio stream. Up to eight channels can be supported over I2S.

Table 8-1147. SEC_CHANNEL_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
2:0	SEC_CHANNEL_COUNT	R/W	0x0	Number of audio channels. 000= Audio mute set in the VBID field. 010= Two channel audio 011= Two channel audio with LFE 110= 5.1 channel surround sound 111= 7.1 channel surround sound

8.6.3.2.53 SEC_MAUD Register (Address = 0x318) [Default = 0x000000]

SEC_MAUD is shown in SEC_MAUD Register Field Descriptions.

Return to the Summary Table.

This register is used when the audio clock generation has been set to the synchronous mode. The clocking values for the secondary channel audio must be calculated by the host system and provided in this register for transmission to the sink device. Example Maud and Naud values may be found in section 2.2.5.2.2 of the DisplayPort 1.2a specification.

Table 8-1148. SEC_MAUD Register Field Descriptions

Bit	Field	Type	Default	Description
23:0	SEC_MAUD	R/W	0x0	Unsigned value computed in the synchronous clock mode.

8.6.3.2.54 SEC_NAUD Register (Address = 0x31C) [Default = 0x000000]

SEC_NAUD is shown in SEC_NAUD Register Field Descriptions.

Return to the Summary Table.

This register is used when the audio clock generation has been set to the synchronous mode. The clocking values for the secondary channel audio must be calculated by the host system and provided in this register for transmission to the sink device. Example Maud and Naud values may be found in section 2.2.5.2.2 of the DisplayPort 1.2a specification.

Table 8-1149. SEC_NAUD Register Field Descriptions

Bit	Field	Type	Default	Description
23:0	SEC_NAUD	R/W	0x0	Unsigned value computed in the synchronous clock mode.

8.6.3.2.55 SEC_AUDIO_CLOCK_MODE Register (Address = 0x320) [Default = 0x0]

SEC_AUDIO_CLOCK_MODE is shown in SEC_AUDIO_CLOCK_MODE Register Field Descriptions.

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Return to the Summary Table.

Sets the clock mode for the generation of the Maud and Naud values. The M and N values for audio are transmitted in the audio time stamp packet as well as the LSBs in the Main Link.

Table 8-1150. SEC_AUDIO_CLOCK_MODE Register Field Descriptions

Bit	Field	Type	Default	Description
0	SEC_AUDIO_CLOCK_MODE	R/W	0x0	Set this value to a 1 for synchronous clock mode. Set this value to a 0 for asynchronous clock mode.

8.6.3.2.56 SEC_TIMESTAMP_INTERVAL Register (Address = 0x33C) [Default = 0x0000]

SEC_TIMESTAMP_INTERVAL is shown in SEC_TIMESTAMP_INTERVAL Register Field Descriptions.

Return to the Summary Table.

Specifies the number of microseconds to wait between transmissions of each audio timestamp packet. An audio timestamp packet will be sent during the vertical blanking interval shortly after the vertical sync pulse. Subsequent packets will be generated every N microseconds during the video frame as specified by this register.

Table 8-1151. SEC_TIMESTAMP_INTERVAL Register Field Descriptions

Bit	Field	Type	Default	Description
14:0	SEC_TIMESTAMP_INTERVAL	R/W	0x0	Number of microseconds to wait after the initial audio timestamp packet to send a subsequent audio timestamp packet. Timestamp packets will continue to be generated during the video frame. A value of 0 in this register will cause the transmitter to send only a single audio timestamp packet during the vertical blanking interval.

8.6.3.2.57 SEC_AUDIO_CHANNEL_MAP Register (Address = 0x35C) [Default = 0x00000000]

SEC_AUDIO_CHANNEL_MAP is shown in SEC_AUDIO_CHANNEL_MAP Register Field Descriptions.

Return to the Summary Table.

Allows for any of the eight input audio channels from the audio stream secondary data packet to be mapped to any of the eight output audio channels.

Table 8-1152. SEC_AUDIO_CHANNEL_MAP Register Field Descriptions

Bit	Field	Type	Default	Description
31:28	CHANNEL_7_MAP	R/W	0x0	Remaps the input audio channel 7 to the selected output audio channel. Values from 0 to 7 are valid for this register.
27:24	CHANNEL_6_MAP	R/W	0x0	Remaps the input audio channel 6 to the selected output audio channel. Values from 0 to 7 are valid for this register.
23:20	CHANNEL_5_MAP	R/W	0x0	Remaps the input audio channel 5 to the selected output audio channel. Values from 0 to 7 are valid for this register.
19:16	CHANNEL_4_MAP	R/W	0x0	Remaps the input audio channel 4 to the selected output audio channel. Values from 0 to 7 are valid for this register.
15:12	CHANNEL_3_MAP	R/W	0x0	Remaps the input audio channel 3 to the selected output audio channel. Values from 0 to 7 are valid for this register.
11:8	CHANNEL_2_MAP	R/W	0x0	Remaps the input audio channel 2 to the selected output audio channel. Values from 0 to 7 are valid for this register.
7:4	CHANNEL_1_MAP	R/W	0x0	Remaps the input audio channel 1 to the selected output audio channel. Values from 0 to 7 are valid for this register.
3:0	CHANNEL_0_MAP	R/W	0x0	Remaps the input audio channel 0 to the selected output audio channel. Values from 0 to 7 are valid for this register.

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8.6.3.2.58 SEC_AUDIO_FIFO_OVERFLOW Register (Address = 0x370) [Default = 0x0]

SEC_AUDIO_FIFO_OVERFLOW is shown in SEC_AUDIO_FIFO_OVERFLOW Register Field Descriptions.

Return to the Summary Table.

Status bit from the internal secondary data audio packet FIFO. This bit is set when the number of sample packets in the audio packet FIFO exceeds the depth of the buffer. When an overflow occurs, previous sample packets in the audio FIFO will be overwritten.

Table 8-1153. SEC_AUDIO_FIFO_OVERFLOW Register Field Descriptions

Bit	Field	Type	Default	Description
0	SEC_AUDIO_FIFO_OVERFLOW	R/W	0x0	A value of 1 in this status register indicates that an overflow has occurred. The status bit is only cleared by setting the SEC_AUDIO_ENABLE bit to a 0.

8.6.3.2.59 SEC_PACKET_COUNT Register (Address = 0x374) [Default = 0x000]

SEC_PACKET_COUNT is shown in SEC_PACKET_COUNT Register Field Descriptions.

Return to the Summary Table.

Internal debug register containing a running count of the number of secondary data packets that have been transmitted since the secondary channel was enabled. This register clears to zero when the secondary channel is disabled.

Table 8-1154. SEC_PACKET_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
11:0	SEC_PACKET_COUNT	R	0x0	Running count of the number of secondary packets transmitted.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Applications

The DS90UH984-Q1 has two FPD-Link inputs, two DP/eDP outputs and two daisy-chain outputs. It can be connected to either FPD-Link IV or FPD-Link III serializer, as shown in Figure 9-1 and Figure 9-2. See Typical Application Connection — STP for typical STP connection diagram. See Figure 9-4 for typical coax connection diagram.

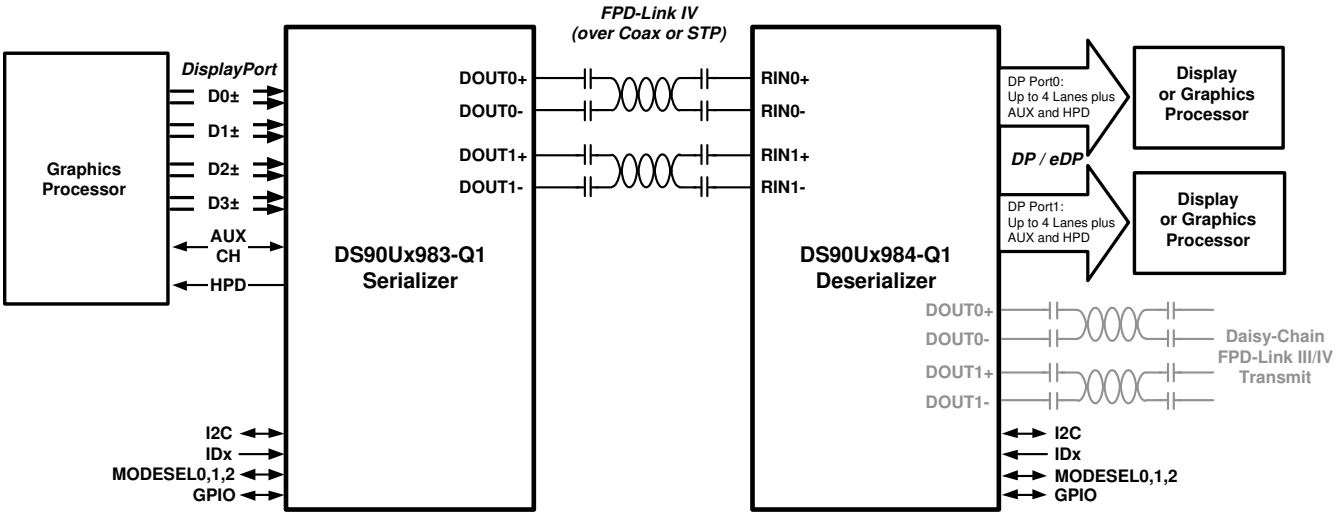

Figure 9-1. FPD-Link IV Typical Application

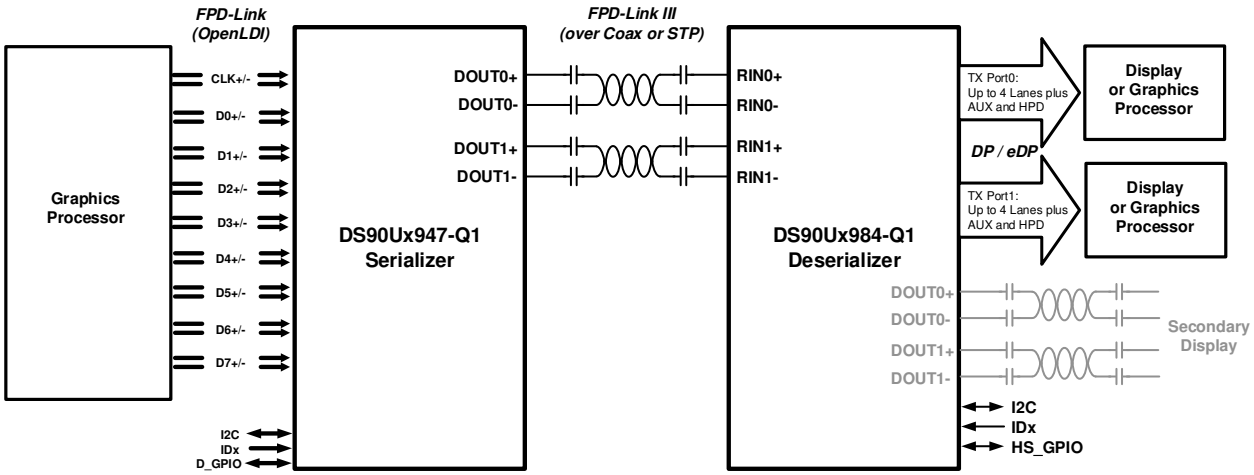

Figure 9-2. FPD-Link III Typical Application

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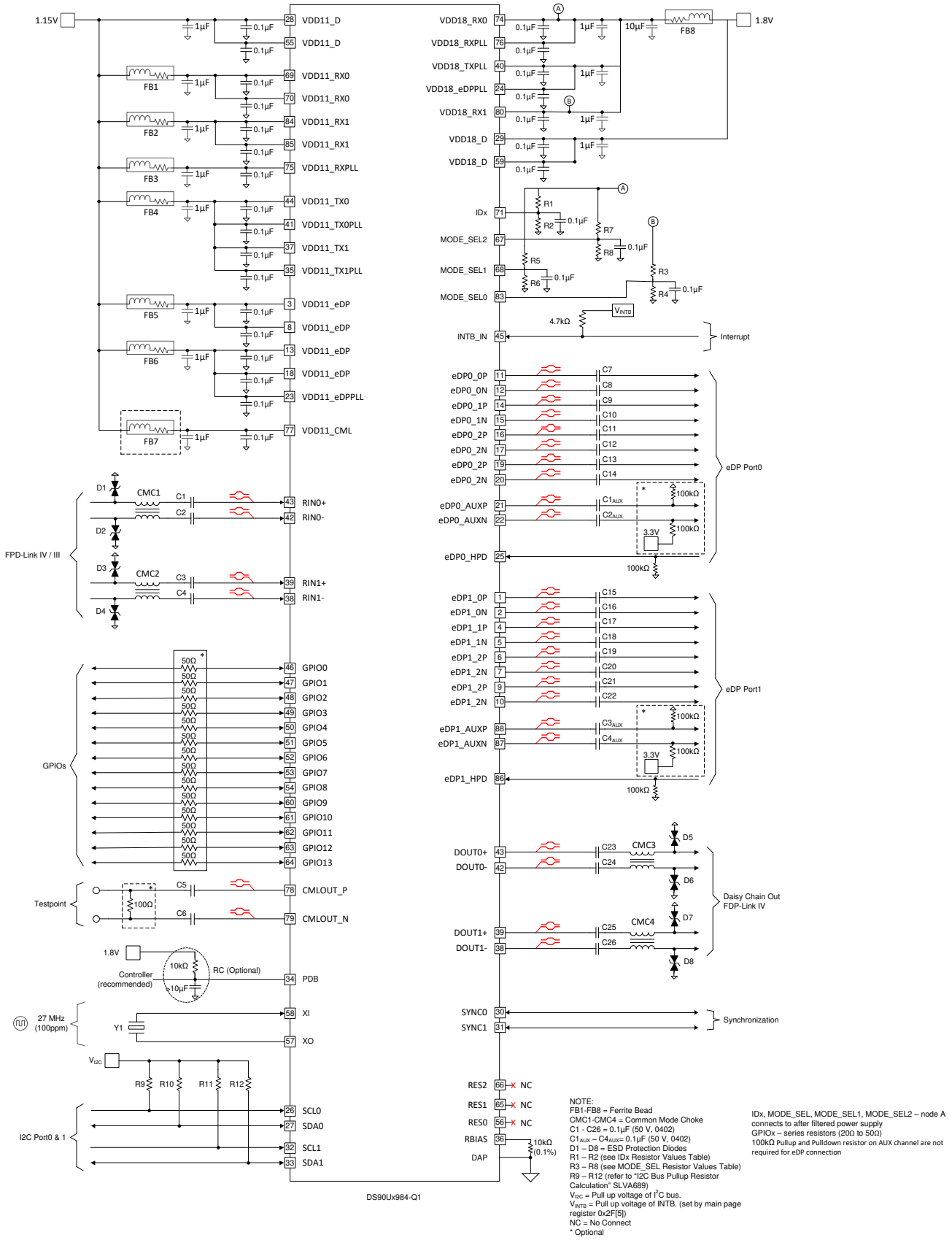

Figure 9-3. Typical Application Connection — STP

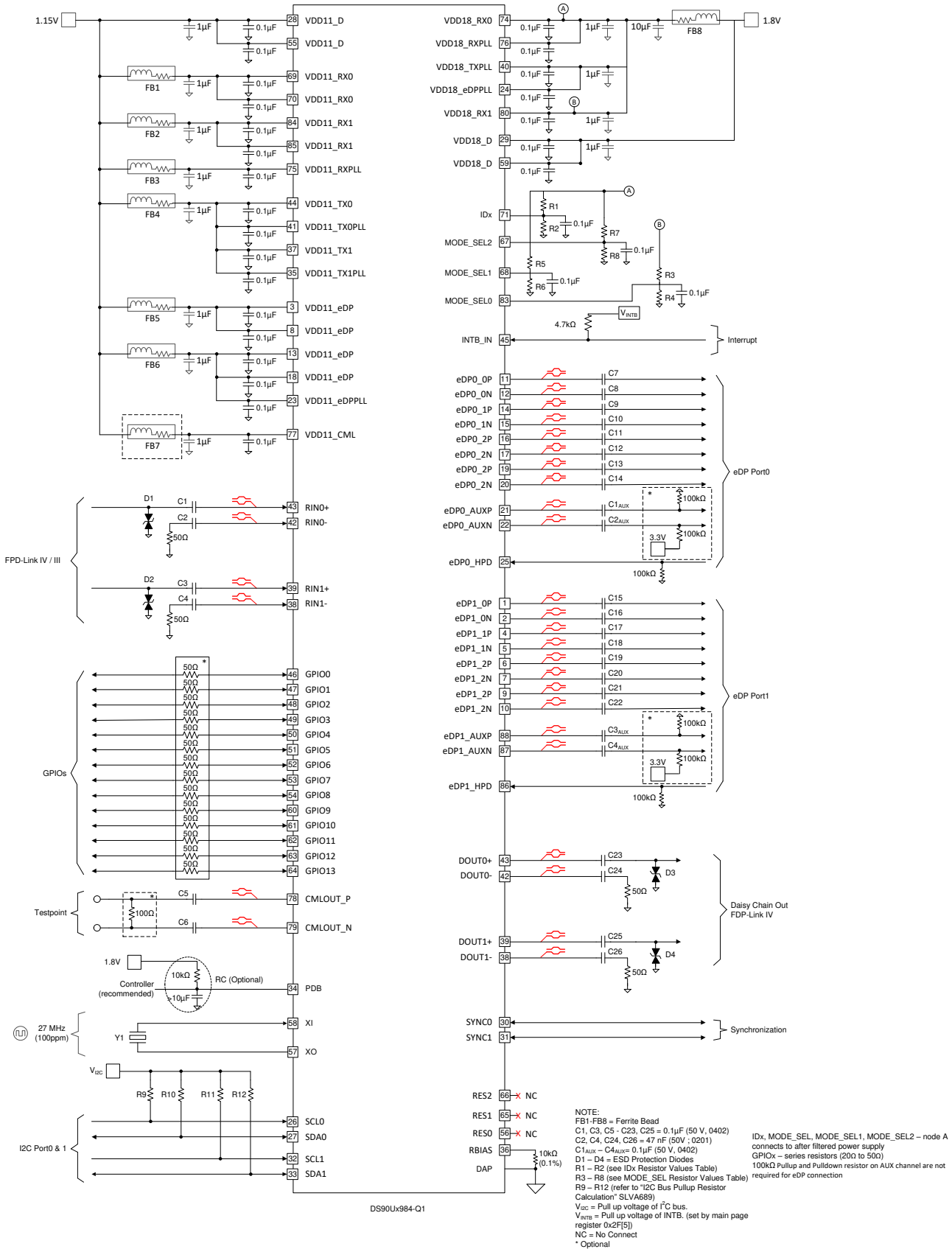

Figure 9-4. Typical Application Connection — Coax

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9.2.1 Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link IV signal path as illustrated in Figure 9-5.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD11	1.15 V
VDD18	1.8 V
AC Coupling Capacitor for RIN± with 98x serializers	100 nF
AC Coupling Capacitor for DOUT± with 98x serializers	100 nF
AC Coupling Capacitor for RIN± with 94x or 92x serializers	33 nF - 100 nF
AC Coupling Capacitor for DOUT± with 94x or 92x serializers	33 nF - 100 nF

Table 9-2. Oscillator Reference Clock Requirements

Parameter	Conditions	Min	Typ	Max	Units
Frequency tolerance	-40C to 105C	-50		50	ppm
Frequency stability	Aging	-50		50	ppm
V_{IH}		0.65 × VDD18		VDD18	mVpp
V_{IL}				0.35 × VDD18	mVpp
Reference clock Duty Cycle		40	50	60	%
Rise/Fall Time	20% - 80%		0.1	3	ns @ 15 pF loading
Reference clock oscillator frequency	+-100ppm, XO input		27		MHz
RMS Jitter	40 kHz - 20 MHz			1.5	ps rms
Load Capacitance				20	pF

Table 9-3. Crystal Reference Clock Requirements

Parameter	Conditions	Min	Typ	Max	Units
Frequency tolerance	-40C to 105C	-50		50	ppm
Frequency stability	Aging	-50		50	ppm
Frequency			27		MHz
Load Capacitance				20	pF
ESR				70	Ohm
Drive Level				100	uW_{RMS}

Table 9-4. Recommended Series Resistor for Different Crystals

Crystal Spec	Recommended series resistor value (ohm)
Drive Level < 100uW RMS, ESR = 50, Co = 2pF, C_{LOAD} = 12pF	2200
Drive Level < 100uW RMS, ESR = 22, Co = 2pF, C_{LOAD} = 8pF	910
Drive Level < 200uW RMS, ESR = 50, Co = 2pF, C_{LOAD} = 12pF	390

For applications utilizing single-ended 50Ω coaxial cable, the unused data pins (RIN0-, RIN1-) should utilize a 15nF - 47nF capacitor and should be terminated with a 50Ω resistor.

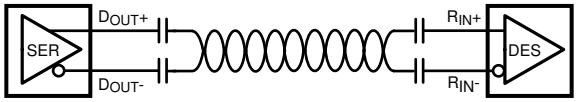

Figure 9-5. AC-Coupled Connection (STP)

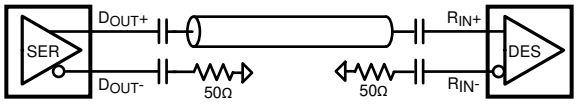

Figure 9-6. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link IV transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

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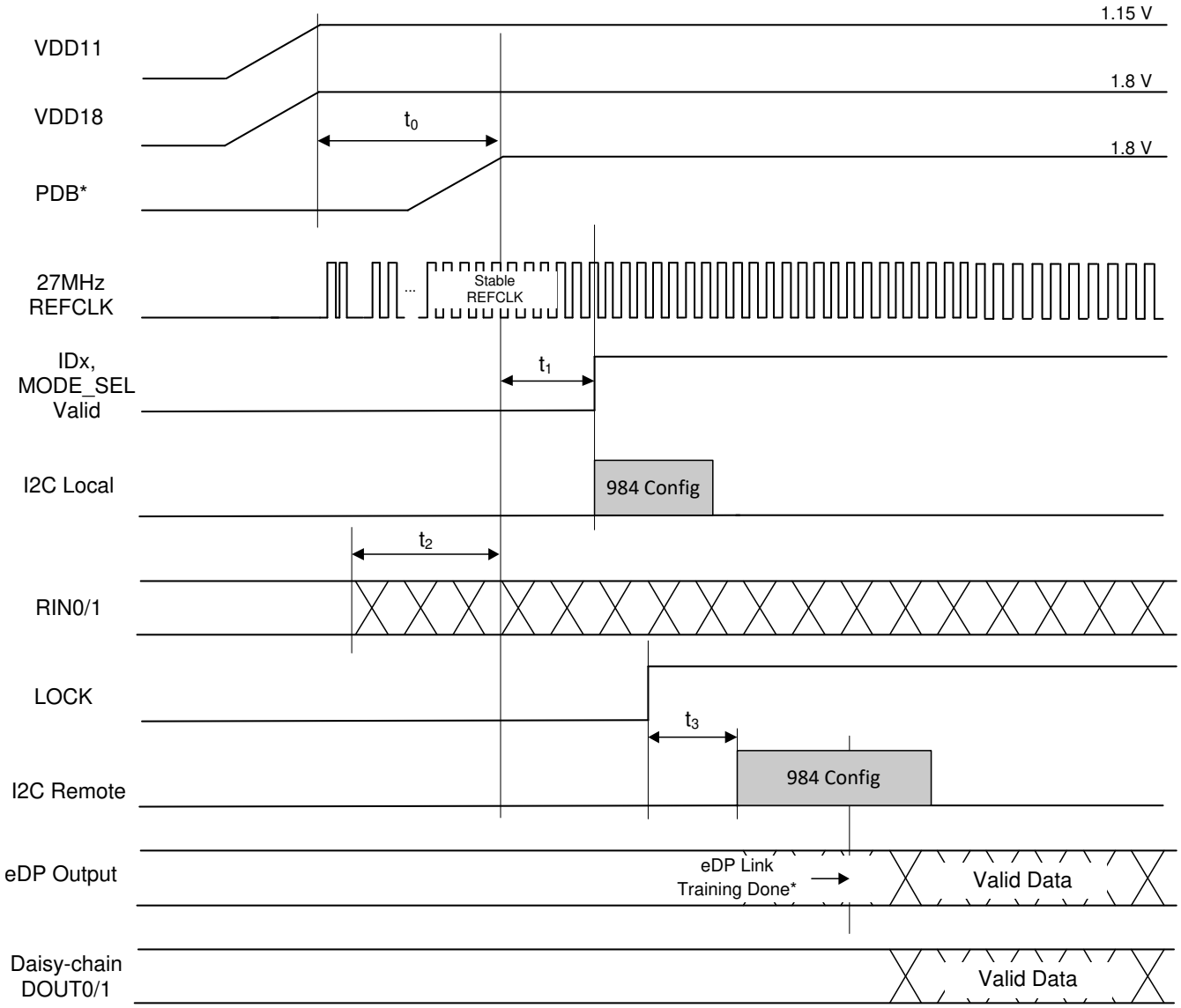
10 Power Supply Recommendations

10.1 Power Up Requirements And PDB Pin

VDD11 and VDD18 can rise in any order. The power supply ramp should be faster than 50 ms with a monotonic rise. A large capacitor on the PDB pin may be used to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. All inputs must not be driven until all power supplies have reached steady state.

The recommended power up sequence is shown in Figure 10-1



*27MHz REFCLK needs to be stable before PDB goes HIGH.

*eDP link training time is system dependent.

Figure 10-1. Recommended Power Sequencing

Table 10-1. Power-Up Sequencing Constraints

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VDD11 Rise Time	@10%/90%	0.200		50	ms
	VDD18 Rise Time	@10%/90%	0.200		50	ms
t_0	Last power supply to PDB Delay	Time from when the last power supply reaches 90% to PDB reaches V_{IL}	0.05			ms
t_1	PDB to Local I2C programming start and strap mode valid		3			ms
t_2	RIN data available to PDB Rise[1]		0			ms
t_3	LOCK high to Remote I2C programming start		500			us

1. Note that the DS90UH984-Q1 should be powered up after a compatible upstream device has started sending valid video data. If this condition is not satisfied, then a digital (software) reset or hard reset (toggling PDB pin) is required after receiving the input data. This requirement prevents the DS90UH984-Q1 from locking to any random or noise signal, ensures DS90UH984-Q1 has a deterministic start-up behavior, specified lock time, and optimal adaptive equalizer setting.

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11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the DS90UH984-Q1 should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypassing should be low-ESR ceramic capacitors with high-quality dielectric. The voltage rating of the ceramic capacitors must be at least 2× the power supply voltage being used.

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 47-µF to 100-µF range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs. For DS90UH984-Q1, only one common ground plane is required to connect all device related ground pins.

Use at least a six-layer board with a power and ground plane. Locate DP signals away from the single-ended or differential FPD-Link traces to prevent coupling from the DP signals to the TX outputs. The following sections provide important details for routing the FPD-Link and DP traces.

11.1.1 Bypass Capacitors

Figure 11-1 shows an example of how to layout the capacitors. It is important to determine where to place the bypass capacitors so there is no unwanted noise coupling into the device. If the device is placed on the top side of the board, then the capacitor should be placed underneath of the device or the other way around. The engineer can place the capacitor close to the power supply pin on the bottom side of the PCB to free up space on the top side of the board for high-speed routing. This bottom placement also allows other signals to access the device pins more easily. TI recommends using a via on each end of the bypass capacitors to connect the power and ground pins directly to the power and ground planes. Connecting the power or ground pins to an external bypass capacitor increases the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass, but a larger cap like 10-µF might not available in a smaller 0603 or 0402 package. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonant frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also common practice to use two vias from the power and ground pins to the planes to reduce the impedance at high frequency.

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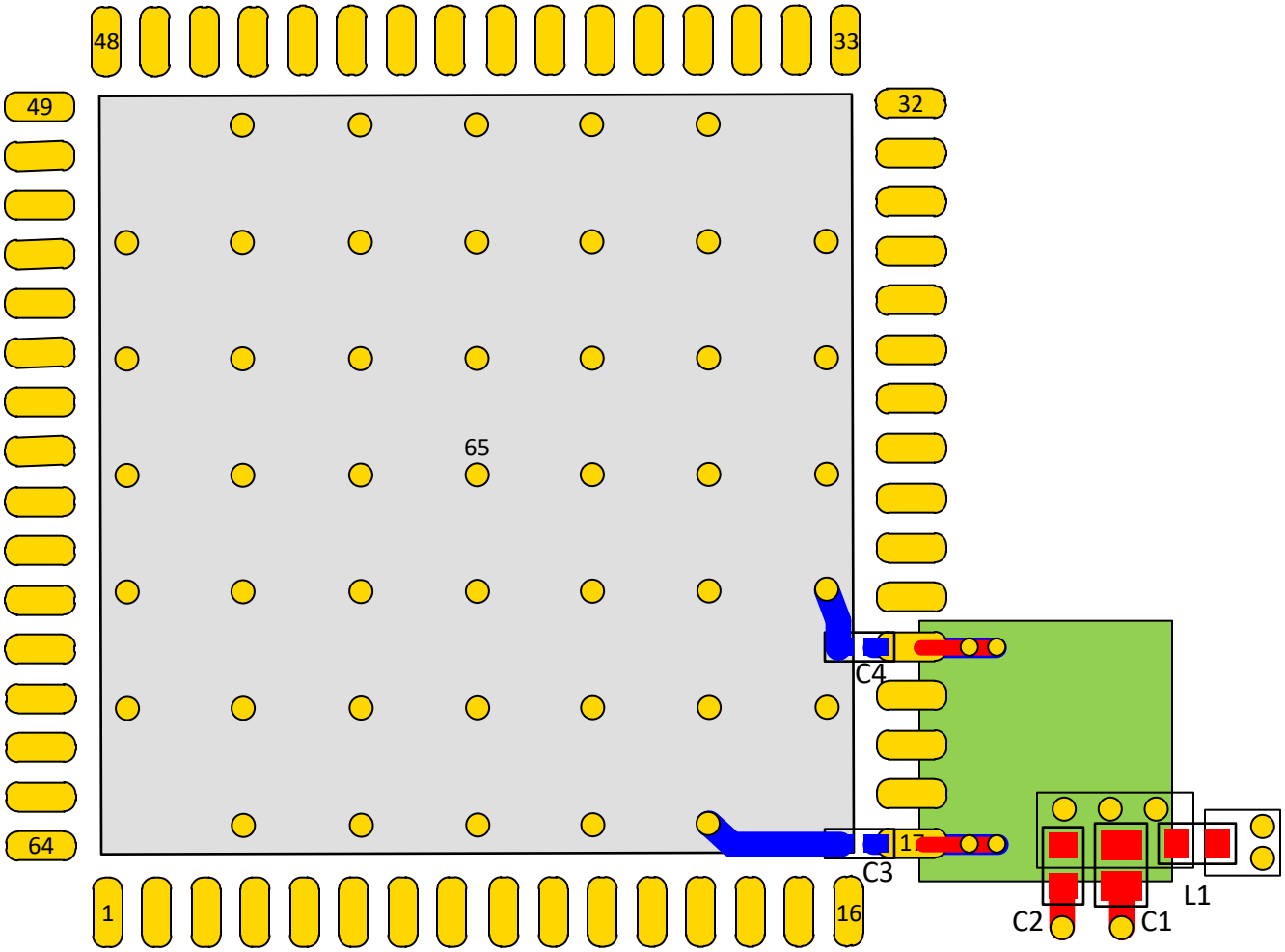

Figure 11-1. Recommended Capacitor Layout

Figure 11-1 is an example of the layout, but it is not necessary to replicate the exact same layout. The QFN package has pins that surround the desired dimension with a vacant center courtyard available on the bottom sides. This is a great opportunity to use the space around the power and ground pins that are near the vacant center courtyard. In Figure 11-1, assuming the device is placed on the top side indicated in red, it is better to place the lowest value bypass capacitor on the bottom side (blue) for ideal proximity while using the extra DAP space available. This makes it easy to place the bypass capacitors on the opposite side of the board in the courtyard area. C3 and C4 are the smallest values of the capacitor that can be placed right at the bottom of the power pin. This gives the lowest inductance path for power. C1 and C2 are the large value capacitors, and the inductor can be placed on the top side as shown in Figure 11-1. Each connection point of the components requires at least two vias with 10 mils minimum of hole diameter for the power path. The top red plane at C1 and C2 immediately drops down to the green plane of the power, which fanout the plane to pin 17 and 21 of the device. The trace widths around pins 17 and 21 should be equal and on the bottom side of the connection. The red traces on top of the plane and blue trace widths on the bottom of the plane shown in Figure 11-1 should also be of equal length. Pins 18, 19, and 20 will still accessible on the top side of the board after the connection.

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11.1.2 Thermal Analysis of Board Design

Thermal analysis of board design should be performed to ensure that junction temperature of the device does not exceed maximum junction temperature of 150 ℃ and any other system-level constraints are met. Equation 77 can be used to calculate approximate required Θ_{JA} for a given use case based off maximum temperature and power dissipation.

$$\text{Required effective } \Theta_{JA} < (T_{J\text{-}MAX} - T_{A\text{-}MAX})/P_{MAX} \tag{77}$$

Where

- $T_{J\text{-}MAX}$ = Maximum junction temperature of 150 ℃
- $T_{A\text{-}MAX}$ = Maximum ambient temperature (such as 105 ℃)
- P_{MAX} = Maximum power of device

For example, when considering $T_{A\text{-}MAX}$ of 105 ℃ and P_{MAX} of 2.5 W, Θ_{JA}=18 ℃/W.

Θ_{JA} is largely determined by design including the board stack-up, via plating, and proximity to other heat dissipating devices. As an example, Table 11-1 shows a comparison of Θ_{JA} for the same board with different plating options.

Table 11-1. Θ_{JA} Examples

Layout	JEDEC Standard	Enhanced #1	Enhanced #2
Layer Count	4-layer	4-layer	4-layer
Layer Stack-Up	Standard	1 oz Cu on all layers and 2 GND planes	1 oz Cu on all layers and 2 GND planes
Via Configuration	Standard	45 with 12 mil diameter	45 with 12 mil diameter
Via Type	Standard	0.035 mm Cu Plating	Solid Copper
Θ_{JA} [1]	18.1 ℃/W	15.0 ℃/W	14.4 ℃/W

1. This is a thermal test PCB and not intended to reflect an actual use case

Since the effective Θ_{JA} is implementation specific and dependent on many variables, it is recommended to further validate thermal design via software simulation using PCB layout and power dissipation directly.

11.1.3 Heat Conduction

There are three methods of heat transfer: heat conduction through solids, heat convection through fluids and gases, and heat generated by radiation. The heat conduction as it dominates the heat transfer in PCBs and is therefore most relevant to temperature in the PCBs.

Heat conduction is defined as the transfer of heat through a volume or a body. Heat is transferred through microscopic collisions of particles; the more collisions, the hotter the object is. Heat transfer occurs when there is a temperature difference between two objects or between different areas of an object, and its rate depends on the geometry, thickness, and material of the object. Due to the law of equilibrium, heat transfers from a hotter body to a colder body until the whole system reaches final equilibrium, as shown in Figure 11-2. There is no net heat transfer between two objects that are equilibrium temperature. The equation for heat transfer through conduction is shown below:

$$\frac{Q}{t} = kA\frac{(T_2 - T_1)}{d} \tag{78}$$

where

- Q/t: The rate of heat transfer [J/s]
- k: the thermal conductivity of the material [W/m×K]
- A: Surface of the contact area [m^2]
- ΔT: The temperature difference of T1 temperature of one object and T2 temperature of the other [K]

- d: The thickness of the material [m]

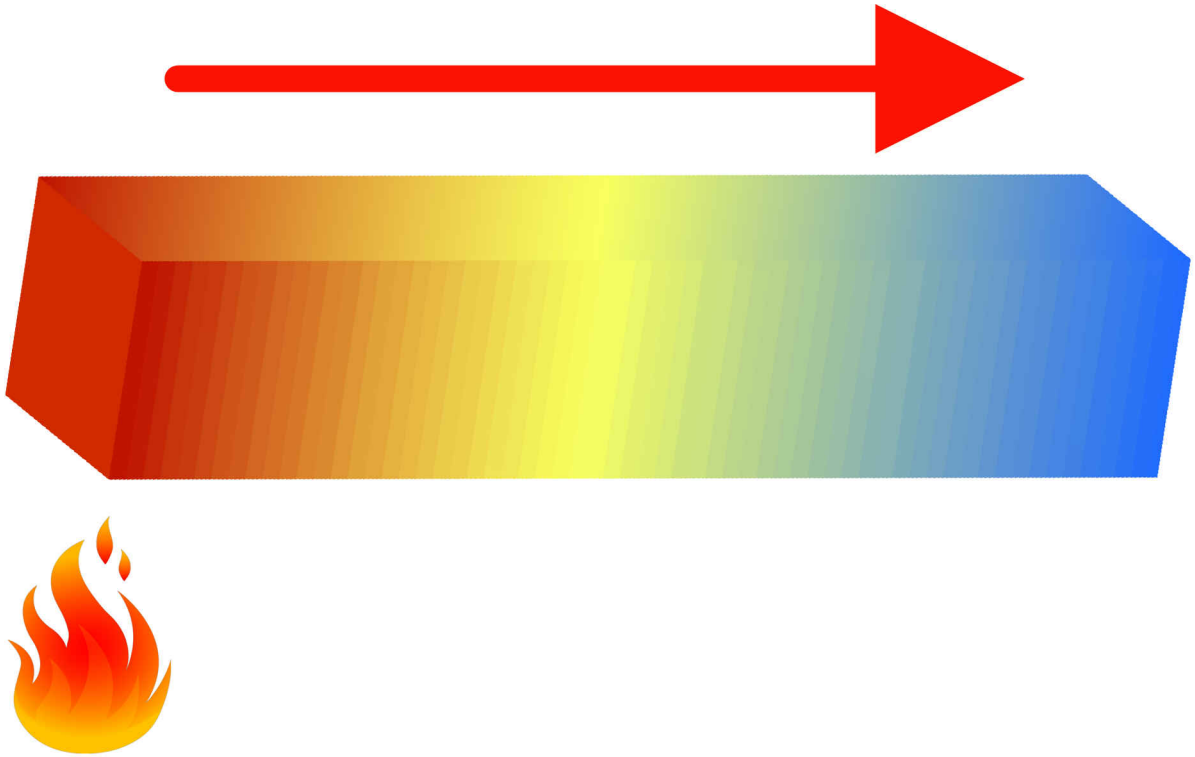

Figure 11-2. Heat Conduction Model

Thermal conductivity (k) is the measure of a material's capability to conduct heat. It is used to describe how heat conducts through a material. Metals are highly thermally conductive whereas materials like air, wool, paper, or plastic are poor conductors of heat. Materials with a very low thermal conductivity, such as polystyrene foam, act like a thermal insulator.

The materials that are most relevant to thermal analysis of PCBs are copper, FR4, and solder mask. Copper is an excellent conductor of heat; it conducts heat significantly faster than FR4. The table below lists the thermal conductivities found in PCBs. The higher the value, the more efficient the material is in transferring heat, which results in a shorter thermal response time. For low k values, the temperature gradient between the source and the sensor can be significantly large and must be considered carefully during layout.

Table 11-2. Material Thermal Conductivity Coefficients Of Selected Materials

Material	Thermal Conductivity k [W/(m×K)]
Air	0.0275
Solder Mask	0.245
FR4	0.25
Gold	314
Copper	385
Silver	406

11.1.3.1 Exposed Pad Layout Design

Packages with a DAP, such as QFN package, have a large exposed surface area through which heat can transfer quickly. These package types will respond quickly to temperature changes of the copper plane which the DAP is soldered onto. Since the die sits directly on top of the exposed pad, heat can transfer rapidly from the die to the thermal pad. In Figure 11-3 depicts the cross section that the die is mounted on top of the metal plate leadframe with a conductive die adhesive, allowing for a fast thermal response transferring through the pins directly to the PCB.

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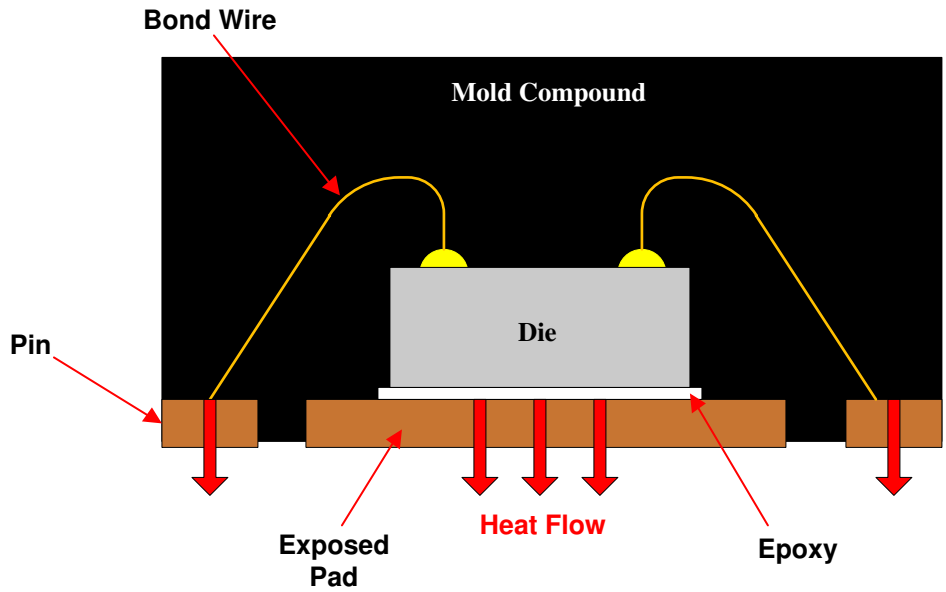

Figure 11-3. Heat Transfer QFN Package Cross Section Example

The Figure 11-4 illustrates the cross-section example when utilizing unused layer to create the similar to exposed pad within the layer stack-up. The copper areas of the PCB acts like a heat sinks for the QFN device where this helps extracting any heat dissipation from the device. The top copper areas of the PCB should be made per landing pattern guidelines. Any unused layer copper planes in the layer stack-up also can be connected to thermal pad using vias to create a thermal tunnel extracting the heat directly from the device out to the PCB bottom layer instead of spreading out across the PCB through the inner layers.

The dimensions of the thermal pad on the PCB should be equal to the exposed pad on the QFN as shown in Figure 11-4. The thermal vias should make their electrical connection to the created exposed pad on the multiple layers stack-up ground plane with a solid connection around the entire circumference of the plated through hole and the copper pour. The connection of the thermal vias from and exposed pad of the device using direct connect. Thermal relief connection is not recommended.

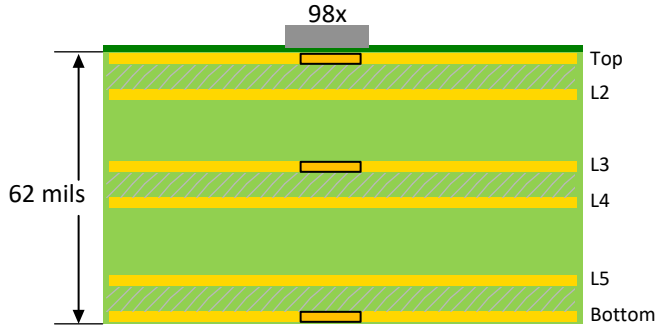

Figure 11-4. Exposed Pad Cross Section Example

11.1.4 Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the FPD-Link devices QFN package to the GND plane with vias. TI suggests 45 thermal vias per mechanical drawing from the device center DAP to the ground plane. Refer to the datasheet landing pattern recommendation for more information. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the QFN style package, including PCB design and manufacturing requirements, is provided in TI Application Note: AN-1187 and QFN Package Application Note.

11.1.5 High-Speed PCB Layout

Good layout practice involves separating high-frequency or high-level inputs and outputs to minimize unwanted noise coupling and interference. High-speed PCB design requires proper routing and stack-up techniques to ensure the signal integrity of the circuit. The performance of the high-speed FPD-Link device is heavily dependent on the PCB layout, so pay attention to the routing of high-speed lanes. A poor PCB layout can lead to poor performance. As high-speed PCB layouts become more complex the impedance control, crosstalk, reflection, discontinuities, and stack-up guidelines described in the following can help ensure optimal performance of the FPD-Link devices.

11.1.5.1 PCB Stack-Up

During high-speed PCB design planning, constructing the multilayer stack-up prior to PCB design is critical. Planning an optimal circuit board stack up can help determine the routing methodologies quickly and easily. A well-defined stack-up can help reduce impedance mismatch and minimize the interference of external noise sources such as EMI. Circuit board layout and stack-up for the FPD-Link IV devices must be designed to provide low-noise power feed to the device. A four-layer board with a power and ground plane is feasible. TI recommends at least a 6-layer board to ensure optimal performance. Table 11-5 and Table 11-6 show each layer of the multilayer distribution as symmetrical and balanced.

11.1.5.1.1 Material Selection

Choosing the proper dielectric material is important for FPD-Link high-speed performance and impedance control. Each layer material is carefully chosen to meet the desired high-speed specification of the device. A hybrid version mixing high speed material with standard FR4 material can save on cost. The inner layers without high speed signals routing can use standard material for the prepreg/core substrates. When designing for high-speed signals above 10 Gbps, use premium PCB materials with low loss dielectric materials. Route high-speed SerDes traces with low loss PCB material. The PCB material thickness also dictates the characteristic 50-Ω and 100-Ω differential impedance requirements.

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Table 11-3. PCB Dielectric Material Insertion Loss

Material	Board Class	Dk	Tan δ (Df)
FR4	Standard Loss	4.3	0.025
Isola 370HR		3.92	0.025
Isola FR406		3.92	0.0127
Isola FR408	Medium Loss	3.66	0.0127
Isola FR408HR		3.64	0.0098
GETEK		3.5	0.009
Isola I-SPEED		3.63	0.0067
Nelco 4000-13 EP		3.6	0.008
Megtron 6	Low Loss	3.33	0.003
Rogers 4350B		3.48	0.0037

Different laminate vendors offer a wide range of products as the value of the dielectric loss (Dk) and loss tangent (Df) differ from various cores and prepregs used in actual PCB constructions. Note that a small differences of Dk or Df can have a huge impact on controlled impedance lines and signal integrity. In order to prevent signal energy loss at high frequencies, the material uses must have a low Dk, Df and signal integrity features. A large loss tangent means higher dielectric absorption. Most of the high-speed material have a flatter Dk and Df as the frequency increasing and maintain a low dielectric loss.

Table 11-4. FPD-Link PCB Recommendations

Parameter	Min	Typ	Max	Units
PCB layer count	4	6	10	Layer
Dielectric (Dk) f < 10 Gbps f > 10 Gbps		 3.92 3.2	 4.3 3.6	Er
Loss tangent (Df) f < 10 Gbps f > 10 Gbps		 0.025 0.004	 0.030 0.010	Tanδ
T_g glass transition temperature	170	180		°C
Copper weight (trace thickness)	0.5	1		Oz
Surface roughness		0.1		mil (RMS)
Trace length, L		2		Inch
Trace width, W	5	8	10	Mils
Single-ended: Gap between P-trace to N-trace, S		3W		W
Differential: Gap between P-trace to N-trace, S Tightly coupled Loosely coupled		 S≤W S=2W		W
Single-ended characteristic impedance	45	50	55	Ω
Differential characteristic impedance	90	100	110	Ω
Differential connector and landing pads impedance	80	100	120	Ω
Intra-pair skew (delay difference between P+ and N- trace)			1	ps

Table 11-4. FPD-Link PCB Recommendations (continued)

Parameter	Min	Typ	Max	Units
Inter-pair skew (pair-to-pair delay difference)			10	ps

11.1.5.1.2 FPD Linerates for 10.8 Gbps or 13.5 Gbps

For linerates exceeding 10 Gbps, TI recommends low-loss dielectric material to ensure impedances are maintained for high-frequency electrical performance such as Megtron-6 and Rogers-4350. Use premium dielectric only where needed for high-speed interface and FPD-Link routing. The 98xEVMs are designed with Megtron6 material to accommodate up to the highest data rates >10Gbps.

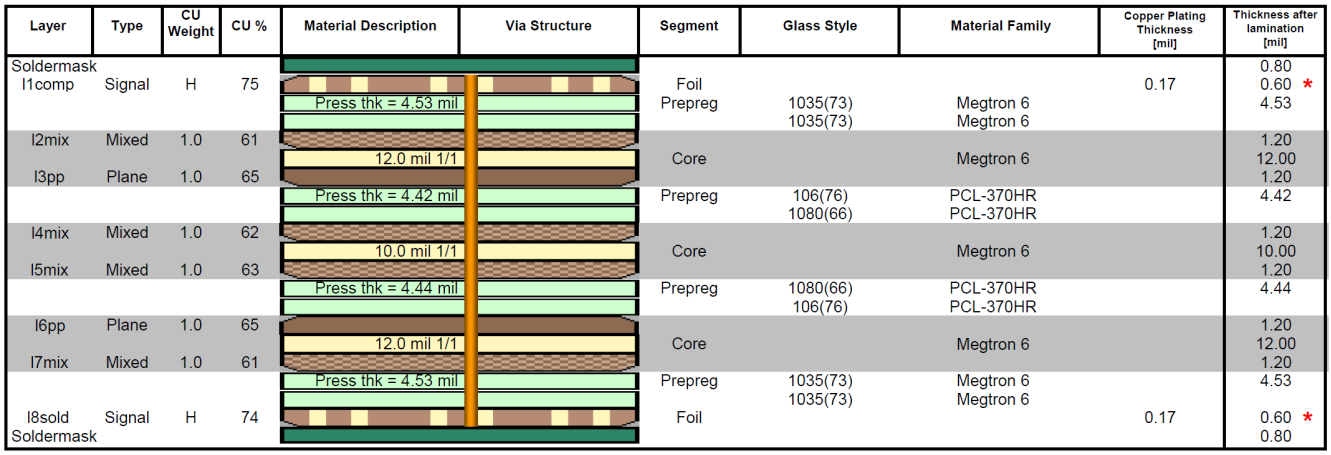

Figure 11-5. 8 Layers Stack-Up Information

Table 11-5. EVM Stack-up Details

# OF LAYER	LAYER	TYPE	THICKNESS(MILS)	COPPER WEIGHT (oz)	DIELECTRIC CONSTANT	LOSS TANGENT	COUPLING TYPE
	MASK	SURFACE	0.8		3.2	0.035	
1	TOP	CONDUCTOR	0.7	0.5			COATED COUPLED MICROSTRIP
		PREPREG	4.53		3.2	0.004	
2	SIGNAL-1	CONDUCTOR	1.4	1			
		CORE	12		3.6	0.004	
3	GND 1	PLANE	1.4	1			
		PREPREG	4.42		3.92	0.025	
4	PWR1	PLANE	1.4	1			
		CORE	10		3.6	0.004	
5	PWR2	PLANE	1.4	1			
		PREPREG	4.44		3.92	0.025	
6	GND 2	PLANE	1.4	1			
		CORE	12		3.6	0.004	
7	SIGNAL-2	CONDUCTOR	1.4	1			
		PREPREG	4.53		3.2	0.004	
8	BOTTOM	CONDUCTOR	0.7	0.5			COATED COUPLED MICROSTRIP
	MASK	SURFACE	0.8		3.2	0.035	

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11.1.5.1.3 FPD Linerates for ≤ 6.75 Gbps

When designing for high-speed signals below ≤ 6.75 Gbps, a standard to medium loss material can be used for the stack-up construction. FR4 is the most commonly used PCB material in most lower frequency applications.

Table 11-6. EVM Stack-up Details

# OF LAYER	LAYER	TYPE	THICKNESS (MILS)	COPPER WEIGHT (oz)	DIELECTRIC CONSTANT	LOSS TANGENT	COUPLING TYPE
	MASK	SURFACE	0.8		3.2	0.035	
1	TOP	CONDUCTOR	1.4	0.5			COATED COUPLED MICROSTRIP
		PREPREG	3.324		3.8		
2	SIGNAL-1	CONDUCTOR	1.4	1			
		CORE	9.843		3.8		
3	GND 1	PLANE	1.4	1			
		PREPREG	6.469		4.25		
4	PWR1	PLANE	1.4	1			
		CORE	11.811		4.25		
5	PWR2	PLANE	1.4	1			
		PREPREG	5.907		4.25		
6	GND 2	PLANE	1.4	1			
		CORE	9.843		3.8		
7	SIGNAL-2	CONDUCTOR	1.4	1			
		PREPREG	3.234		3.8		
8	BOTTOM	CONDUCTOR	1.4	0.5			COATED COUPLED MICROSTRIP
	MASK	SURFACE	0.8		3.2	0.035	

11.1.5.2 Controlled Impedance

It is important to maintain DSI, DisplayPort and FPD-Link IV differential trace impedance of 100 Ω with a ±10% differential and Embedded DisplayPort differential trace impedance of 85 Ω with a ±15% differential to avoid impedance mismatches in the transmission line that could affect the signal integrity. The mismatch creates discontinuities, which causes reflections on the signal traces. The differential impedance is determined by the combination of the physical dimensions, the trace width, the adjacent ground, and the properties of material used in PCB substrate. Many software tools are available to calculate the properties of the transmission line structures.

Table 11-7. Impedance Controlled for Various Interfaces

Type of Interface	Differential Impedance
DisplayPort (DP)	100 Ω ±10%
Embedded DisplayPort (eDP)	85 Ω ±15%
DSI	100 Ω ±10%
FPD-Link IV	100 Ω ±10%

11.1.5.3 Differential Traces

They are all tightly coupled in both separation and equal length to benefit from the electromagnetic field cancellation. When the differential pairs are symmetrical and have the same length, the pairs provide excellent noise immunity. This helps minimize impedance discontinuity because this setup prevents traces from branching out and other sudden changes in large landing pads as shown in Figure 11-13.

11.1.5.4 Microstrip vs Stripline Methodologies

Microstrip and Stripline structures are often used in high-speed PCB design. Between the microstrip and stripline, the decision of which method to use should be based on the needs of the design and applications. Both methods are excellent performance for high-speed frequency. They are designed for routed traces that have the correct structure when the return path signals travel along the traces through a plane that is separated by a certain width and height in Figure 11-6 and Figure 11-7.

In Figure 11-6 shows a microstrip configuration with a soldermask top conductor and a dielectric layer separated by bottom ground plane. The P and N traces differential pairs are separated by a uniform distance of S. The spacing between two differential traces should be S = W for tightly coupled traces.

- H = the height distance of the dielectric from the differential pair to the ground reference plane
- S = the separation distance between the two traces of the differential pair
- W = the width of the copper trace
- T = the thickness of the copper trace
- T_{sm} = the thickness of the soldermask
- E_r = the dielectric constant of the substrate between copper trace and the ground reference plane

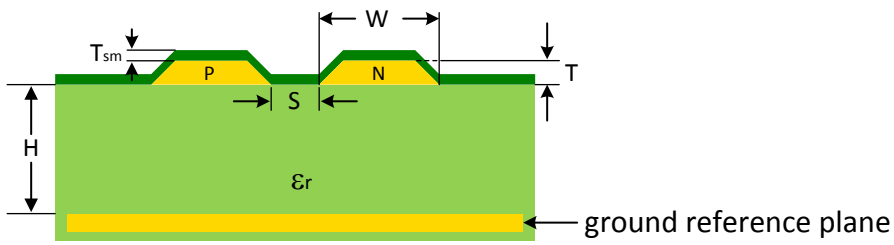

Figure 11-6. Microstrip Differential Pair With Soldermask Coated

For the microstrip, the electric field travels along the trace exposed to the air whereas the trace in the stripline is fully by reference planes.

In Figure 11-7, stripline constructs top and bottom ground planes with dielectric insulator material surrounding a center conductor in a balanced configuration. The two differential traces are sandwiched between ground reference planes 1 and 2, as well as along the traces when there is a ground via stitching. The P and N traces differential pairs are also separated by a uniform distance of S.

- H_1 = the height distance of the dielectric from the ground reference plane 1 to the differential pair
- H_2 = the height distance of the dielectric from the differential pair to the ground reference plane 2
- S = the separation distance between the two traces of the differential pair
- W = W_1 = W_2 = the width of the copper trace
- T = the thickness of the copper trace
- E_{r1} = the dielectric constant of the substrate between the ground reference plane 1 and copper trace
- E_{r2} = the dielectric constant of the substrate between the copper trace and the ground reference plane 2

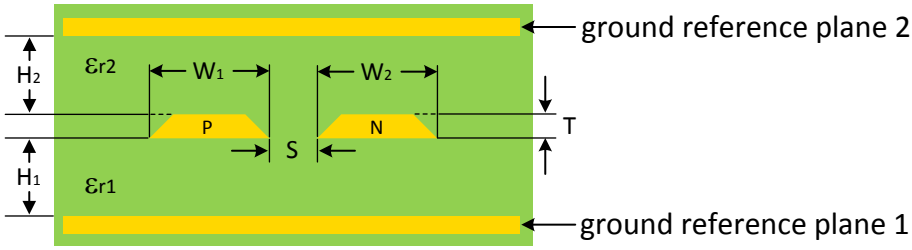

Figure 11-7. Stripline Differential Pair

11.1.5.5 Length Matching

Length matching is also a critical requirement parameter for DSI input, DisplayPort input and FPD-Link IV output differential pairs. When the high-speed signal lanes are length matched, it helps closely match the propagation

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delay between P and N. The mismatch of the P and N traces introduces skew. To compensate the length mismatch, serpentine routing should be used on the shorter trace length, and most CAD tools are available to implement the serpentine routing as shown in Figure 11-8 by using trace tuning. It is very important that the engineer choose the dimensions of the trace tuning carefully so that all the critical signals simultaneously arrive together at their destination. The serpentine trace should be routed as close to the source as possible.

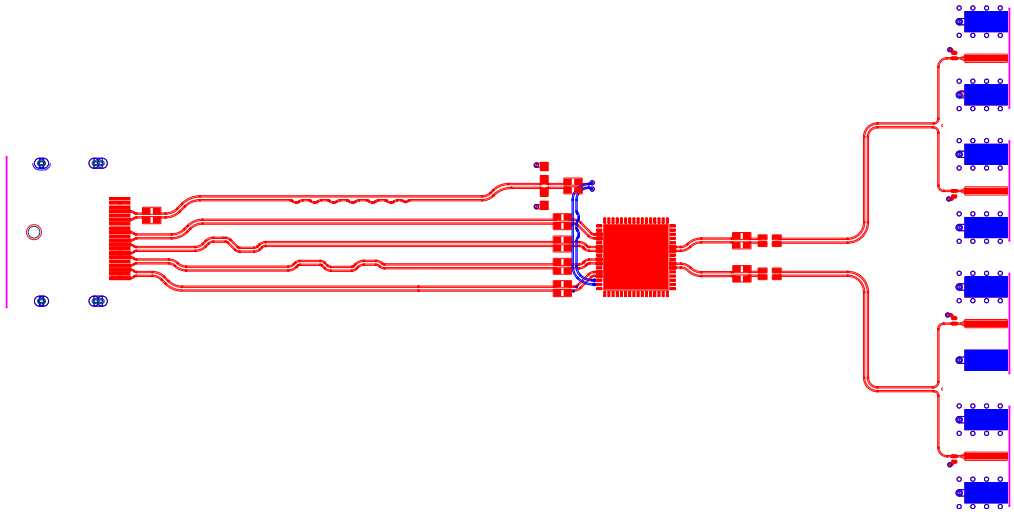

Figure 11-8. Example Layout for Length Matching

11.1.5.5.1 Intra-Pair Skew Matching

Intra-pair skew occurs when the differential signals of P and N are not equal length. When matching the intra-skew of the P and N differential signals, the serpentine routing should be used on the shorter trace length at the source to match the lengths as close as possible. The skew adjustment can be used on the loosely coupled trace to implement the serpentine techniques.

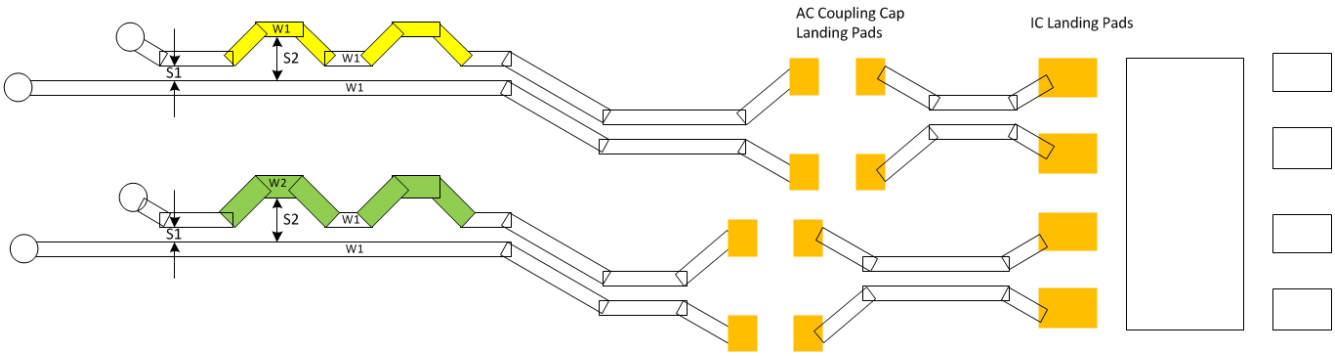

Figure 11-9. Intra-Pair Skew and Inter-Pair Matching

11.1.5.5.2 Inter-Pair Skew Matching

Inter-pair skew is used to compare the difference between a differential pair from another differential pair of the same group, such as the four pairs of DisplayPort and two pairs of FPD-Link IV of the serializer device. It is recommended to route DisplayPort inter-pair skew under 150 ps. Note that it is not necessary to match the lengths of the differential pairs outside the same groups, such as DP/eDP port 0 differential pairs to port 1 differential pairs.

11.1.5.6 Width and Spacing

The P and N traces along with the spacing between the P and N, are required to calculate characteristic impedance. The impedance of the differential trace is controlled by the width of the trace, air gap between P and

N, stack-up, dielectric, and materials. To maintain a uniform-controlled impedance of the 100-Ω differential pair, the spacing between positive and negative not be exceed 2x the trace width.

11.1.5.7 Crosstalk

The high-speed differential pair of P and N traces must be tightly coupled and routed in parallel with each other as much as possible, and the adjacent differential pair signals should maintain a constant distance away from the other traces to prevent coupling. When the electromagnetic energy should stay on track when traveling along the coupled traces, but the energy could escape if there is interfere from an adjacent signal. If the electromagnetic energy escapes, the EMI coupling in to the neighboring signals is called crosstalk.

11.1.5.8 Via

The controlled impedance of the differential via is also important to maintain 100-Ω impedance for the high-speed signals. The differential via impedance depends on many parameters, such as the hole size, pad size, anti-pad size, number of VDD/GND layers, via length, via stub, and via pitch. It is possible to create a controlled impedance via of the high-speed differential via by optimizing the physical dimensions of the PCB design. The differential via of the high-speed signal should be in close proximity with oval anti-pad shared by the two vias reduces parasitic capacitance. The engineer must also place a ground via next to each P and N differential via and evenly space the D1 and D2 lengths between the differential via signals to provide a good return path and isolation for the vias. See Figure 11-10 for an example.

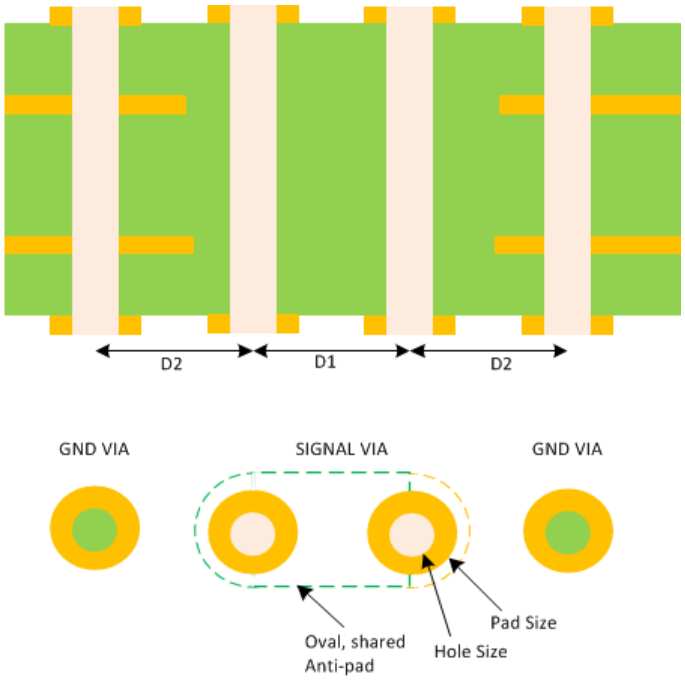

Figure 11-10. Controlled Impedance Differential Via

11.1.5.8.1 Via Stub

Regardless of the routing techniques used for microstrip or stripline methodologies, via stub is not recommended for high-speed differential signals of the DSI, DisplayPort and FPD-Link IV. This is because the via stub can bring a capacitive effect to the differential signals and increase the signal loss. Routing the high-speed differential signal traces on the top and bottom layers avoids the use of vias and allows a clean interconnect from the DisplayPort to the device and the device to the output connector. To mitigate a via stub, the engineer can use a blind or buried via, back-drilling, or a through via from the top to bottom using microstrip techniques. For example, in the left image of Figure 11-11, the device is placed on the top layer while the P and N differential signals are routed from the top layer to the bottom through a through via on a microstrip to avoid via stub. If the differential signals are routed through the internal layer, TI recommends a blind or buried via as well as back-drilling to create the shortest stub possible to avoid reflection.

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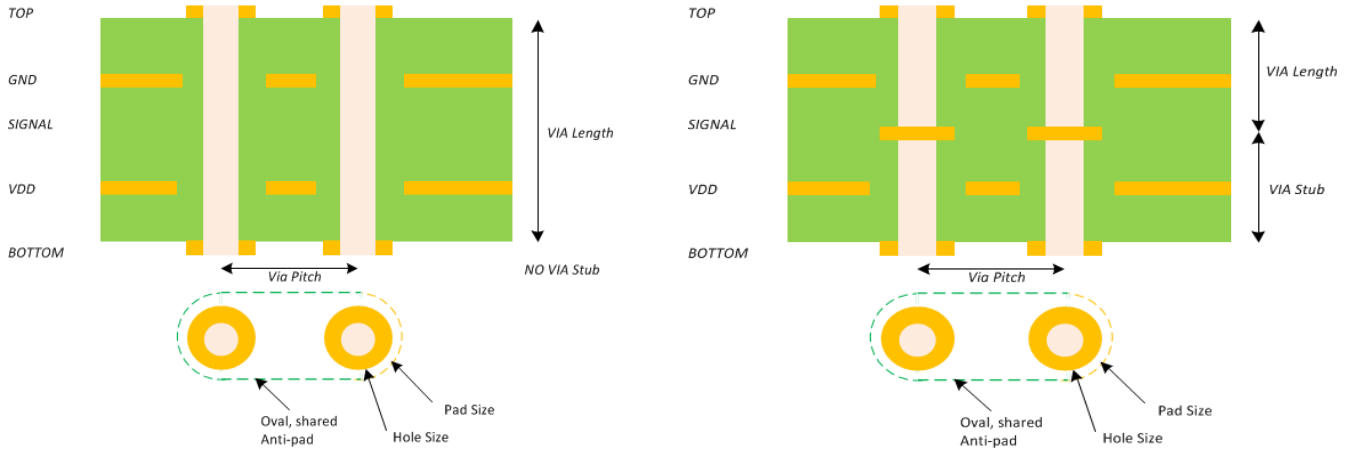

Figure 11-11. Example of Via Stub

In Figure 11-12, the device is placed on the top layer as well as on a top-mount through-hole component. The differential signal traces, therefore, should use bottom trace routing to avoid the via stub. If the top trace routing restricts the top layer routing, the connector should be flipped and placed on the opposite side of the connector.

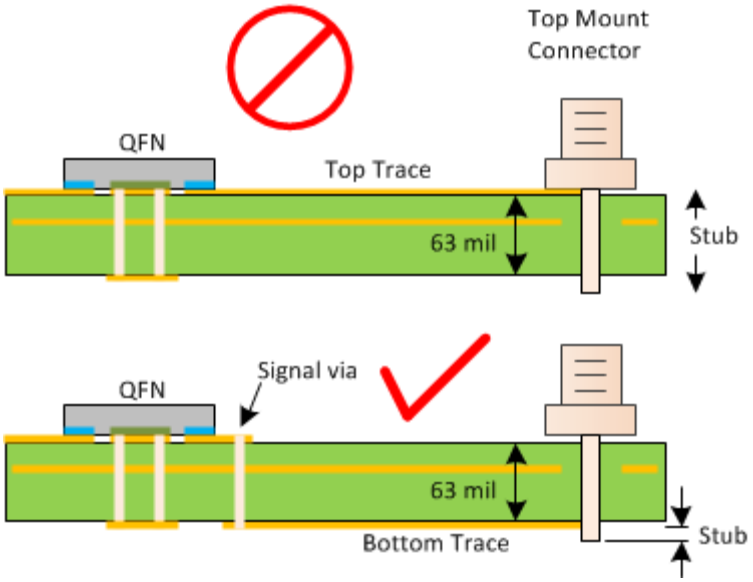

Figure 11-12. Example of Voided Via Stub

11.1.5.9 Anti-Pad

The anti-pad is the unwanted clearance area normally between the pad or trace to the copper plane, or the voided clearance area beneath the high-speed signals landing pad or blinded/buried via in the power or ground plane. Having the anti-pad can help maintain the impedance of the transmission line. The engineer cannot manually calculate the clearance of the anti-pad during layout process, but an electromagnetic field solver such as modeling software can be used to determine the effect and size of the high-speed signal trace behavior of the anti-pad for optimizing the impedance. The initial anti-pad clearance of 20 mils can be used from the trace to the copper plane for DSI, DisplayPort and FPD-Link IV signals, and the engineer can add another 2-5 mils to the original discrete components. However, TI recommends to use the modeling software to determine the exact clearance for the design optimizing the impedance compensation.

Figure 11-13 is the example of mismatch when looking into A-A and B-B cross sections. The A-A section is perfectly matched, but the cross section B-B does not match. This is due to the bottom ground plane. To achieve

the 100-Ω impedance, an anti-pad can be used as clearance from the pad to a shape or the next power or ground plane. This technique can reduce the parasitic capacitance.

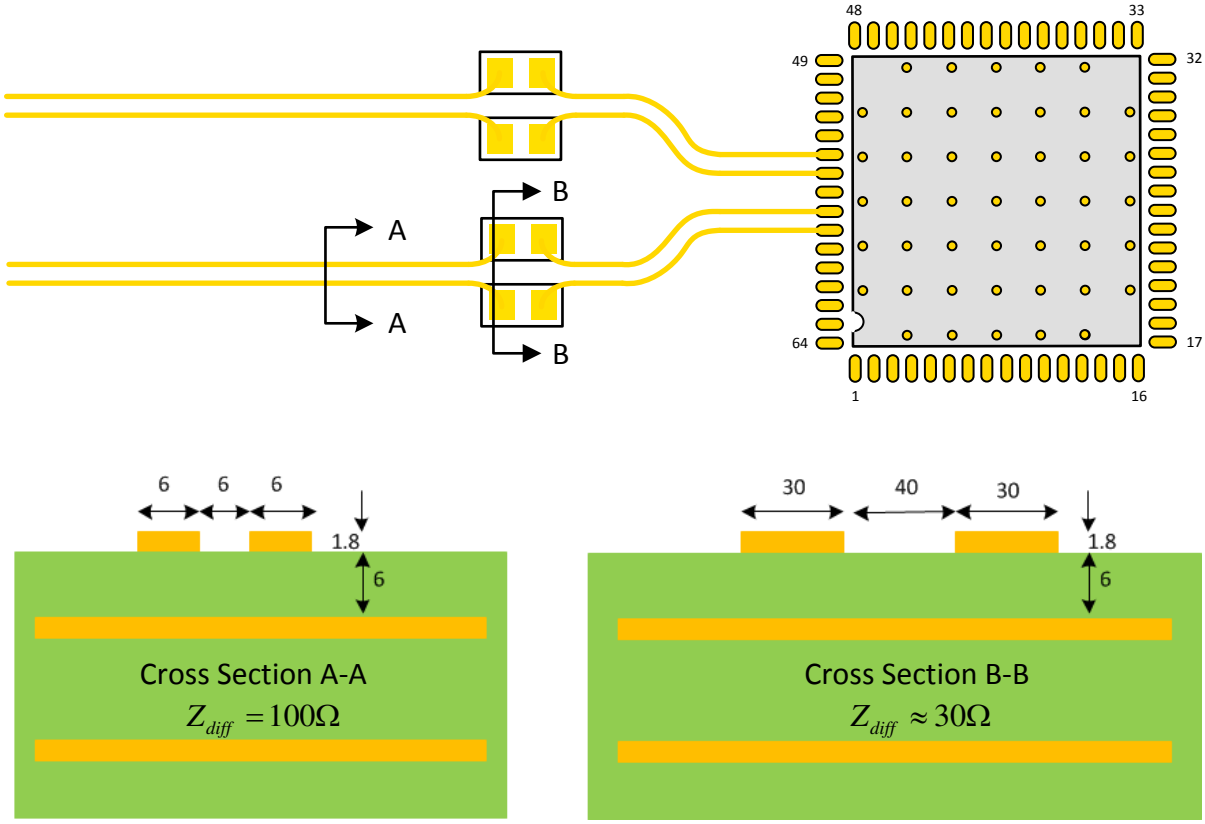

Figure 11-13. Impedance Mismatch From Landing Pads

To compensate the impedance mismatch of the cross section B-B of the landing pads, the power or ground relief layer, and sometimes the next internal layer, must open up and void the clearances underneath the landing pads. This should significantly increase the impedance to match cross section A-A. This should be done along the high-speed lanes of the DSI, DisplayPort and FPD-Link IV to ensure the 100-Ω differential pair meets the specification.

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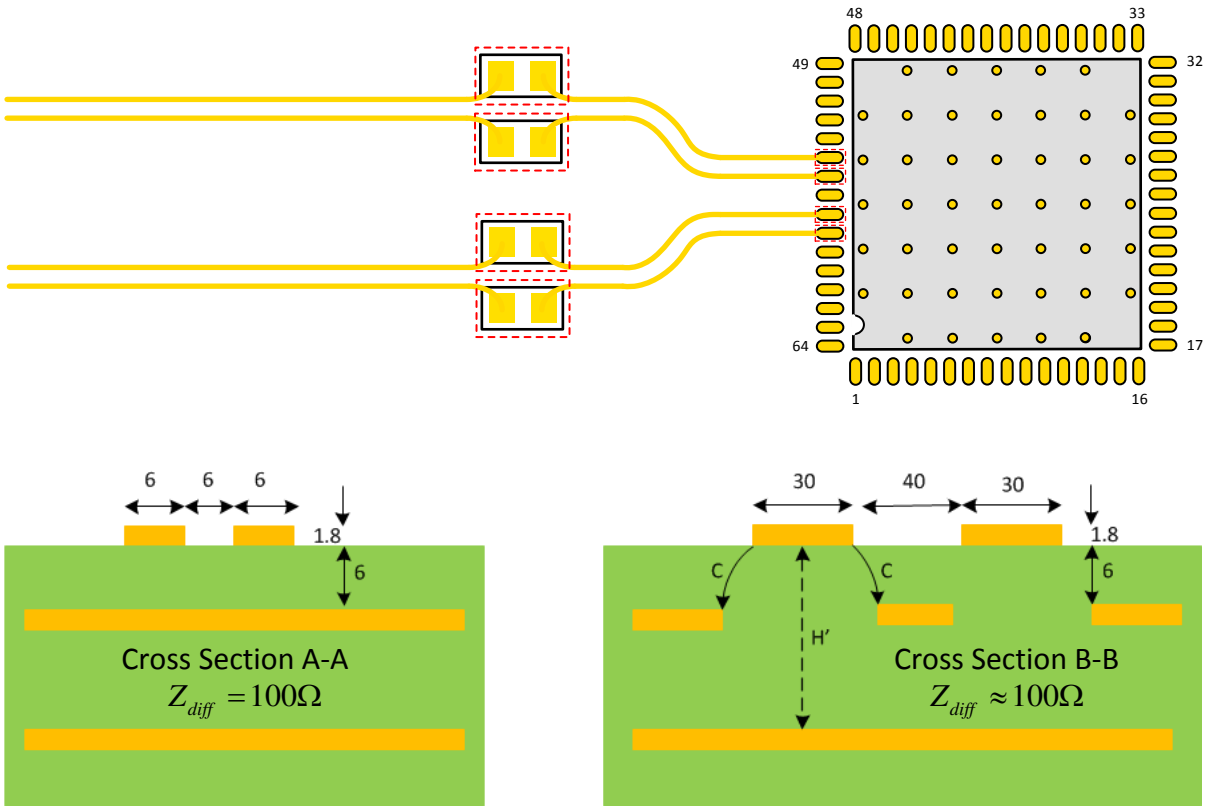

Figure 11-14. Controlled Impedance Landing Pads

The anti-pad for the surface mount connector is very similar to other surface mount IC pad and other discrete components. The ground or power plane should void the clearance area under the landing pad of the connector. The through-hole connector uses the same techniques as a via.

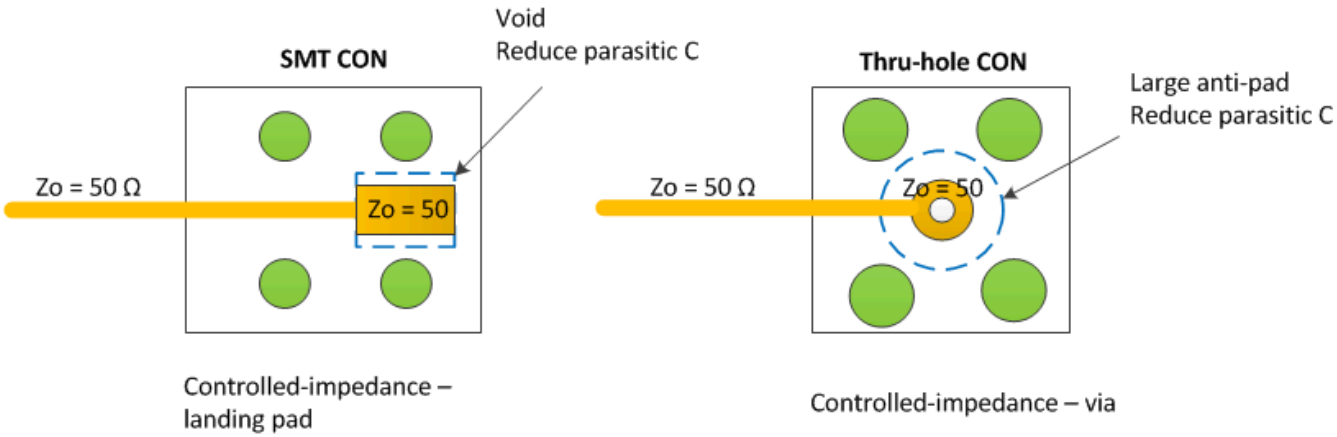

Figure 11-15. Controlled Impedance Footprint for Connectors

11.1.6 Routing FPD-Link Signal Traces

Routing the FPD-Link signal traces between the DOUT pins and the connector is one of the most critical pieces of a successful DS90UH984-Q1 PCB layout.

The following list provides essential recommendations for routing the FPD-Link signal traces between the DS90UH984-Q1 transmitter output pins (DOUT) and the cable connector

- The routing of the FPD-Link traces may be all on the top layer or partially embedded in middle layers if EMI is a concern
- The AC-coupling capacitors should be on the top layer and very close to the DS90UH984-Q1 transmitter output pins to minimize the length of coupled differential trace pair between the pins and the capacitors.
- Route the DOUT traces between the AC-coupling capacitor and the cable connector as a 100-Ω differential trace with tight impedance control (±10%). Calculate the proper width of the trace for a 100-Ω impedance based on the PCB stack-up. Make sure to length match the DOUT+ and DOUT- traces.

11.1.7 Routing DisplayPort Signal Traces

Routing the DisplayPort signal traces between the DP/eDP pins and the DP/eDP connector is also important for a successful DS90UH984-Q1 PCB layout. Recommendations are given in the following list:

1. Route DP pairs as differential coupled with controlled 100-Ω differential impedance (±10%)
2. Route eDP pairs as differential coupled with controlled 85-Ω differential impedance (±15%)
3. Keep the trace length difference between DP/eDP traces to 5 mils of each other.
4. Length matching should be near the location of mismatch.
5. Each pair should be separated at least by 5 times the signal trace width.
6. Keep away from other high-speed signals.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on one or two layers.
9. Keep the number of signal vias to a minimum — TI recommends keeping the via count to a maximum of two per DP/eDP trace.
10. Keep traces on layers adjacent to ground plane.
11. Do NOT route differential pairs over any plane split.
12. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

Table 11-8. DisplayPort Layout Parameters

Parameter	Value
Frequency	DisplayPort RBR: 0.81 GHz (1.62 Gbps)
	DisplayPort HBR: 1.35 GHz (2.7 Gbps)
	DisplayPort HBR2: 2.7 GHz (5.4 Gbps)
	DisplayPort HBR3: 4.05 GHz (8.1 Gbps)
Max Intra-Pair Skew	1 ps (TI recommends about 5 mils)
Trace Impedance (DP)	100Ω ±10% differential
Trace Impedance (eDP)	85Ω ±15% differential

11.1.8 Summary of High-Speed Differential Signal Design Layout Consideration

- Planning helps avoid re-spin and unexpected issues.
- Do not create a test pad or test points on any high-speed differential signal.
- Avoid high-speed routing near crystals, oscillators, clock signal generators, switching power regulators, or magnetic devices.
- When possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent ground layer to avoid via stub.

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- Maintain a constant 100-Ω impedance for the differential signal traces along the high-speed path.
- Minimize the use of vias on high-speed signal traces as much as possible.
- Maximize differential pair-to-pair spacing when possible to avoid crosstalk.
- Place ESD and EMI protection devices as close to the connector as possible.
- Place the AC-coupling capacitors on the protected side of the CMC and as close to the CMC as possible.
- Keep the FPD-Link IV high-speed differential signal trace that is close to the connector as short as possible.
- Create a ground pours on the top and bottom layers.
- Do not use splitting ground. Always use solid ground plane.
- Put the largest-value filter bypass capacitors near power entry, and place high-quality X7R decoupling 0.1-µF capacitors close to device pins.
- Minimize intra-pair skew.
- Keep both P and N differential pair signal traces tightly coupled.
- Use angle smoothing techniques for routing traces and do not use right-angle bends.
- To minimize crosstalk, keep the distance between two traces approximately 2 to 3 times the width of the trace.

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Soldering Specifications Application Report,* SNOA549
- *IC Package Thermal Metrics Application Report,* SPRA953
- *Leadless Leadframe Package (LLP) Application Report,* SNOA401

12.2 Trademarks

All trademarks are the property of their respective owners.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Table 13-1. Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4/5)
DS90UH984RURRQ1	ACTIVE	VQFNP	RUR0088D	88	2500	TBD	NiPdAuAg	Level-3-260C-16 8 HR	-40 to 105	UH984
DS90UH984RURTQ1	ACTIVE	VQFNP	RUR0088D	88	250	TBD	NiPdAuAg	Level-3-260C-16 8 HR	-40 to 105	UH984

(1) The marketing status values are defined as follows:

- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no SB/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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13.1 Package Option Addendum

Packaging Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
DS90UH984RURTQ1	ACTIVE	VQFN	RUR0088D	88	250	RoHS & Green	NiPdAuAg	Level-3-260C-168 HR	-40 to 105	UH984
DS90UH984RURRQ1	ACTIVE	VQFN	RUR0088D	88	2500	RoHS & Green	NiPdAuAg	Level-3-260C-168 HR	-40 to 105	UH984

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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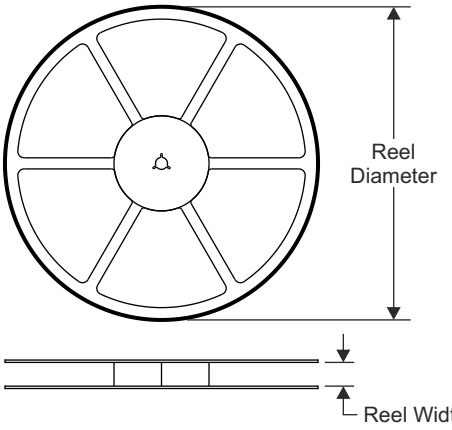
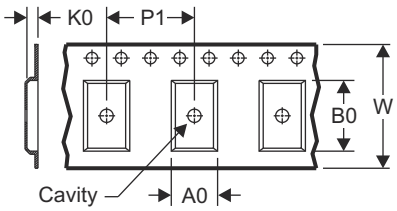
13.2 Tape and Reel Information

REEL DIMENSIONS

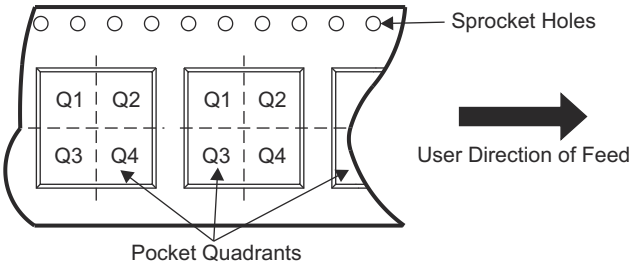


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH984RURTQ1	VQFN	RUR0088 D	88	250	180	24.4	12.30	12.30	1.10	16.00	24.00	Q2
DS90UH984RURRQ1	VQFN	RUR0088 D	88	2500	330	24.4	12.30	12.30	1.10	16.00	24.00	Q2

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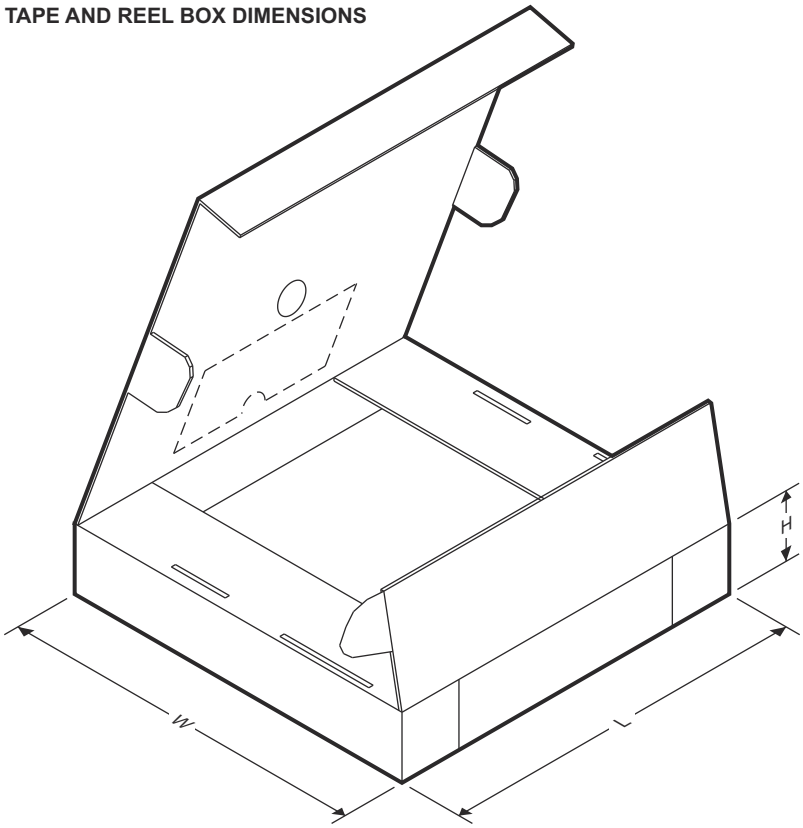
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH984RURTQ1	VQFN	RUR0088D	88	250	210	185	35
DS90UH984RURRQ1	VQFN	RUR0088D	88	2500	360	360	36
DS90UH984RURRQ1	VQFN	RUR0088D	88	2500	367	367	35

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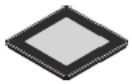
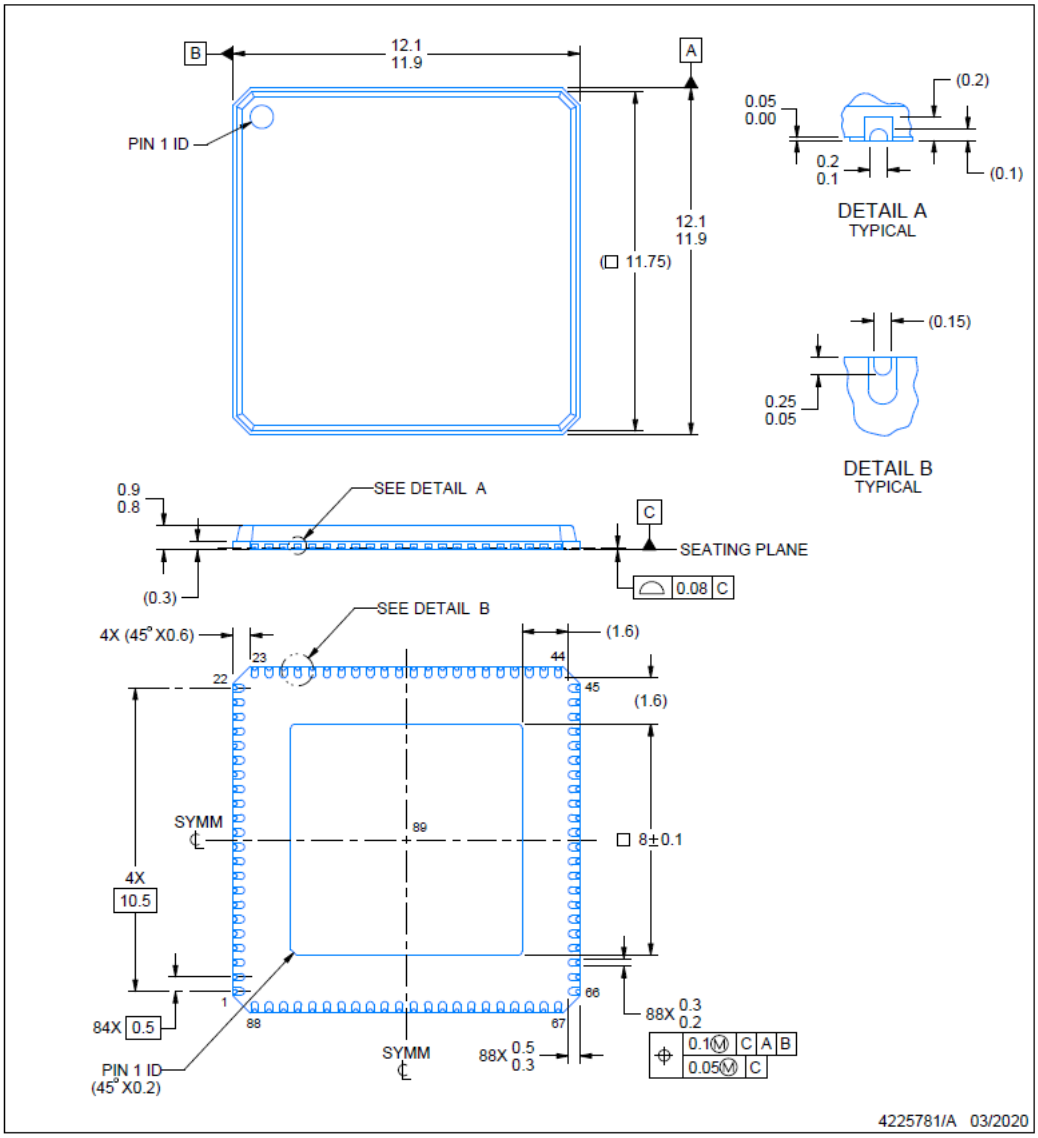
RUR0088D



PACKAGE OUTLINE

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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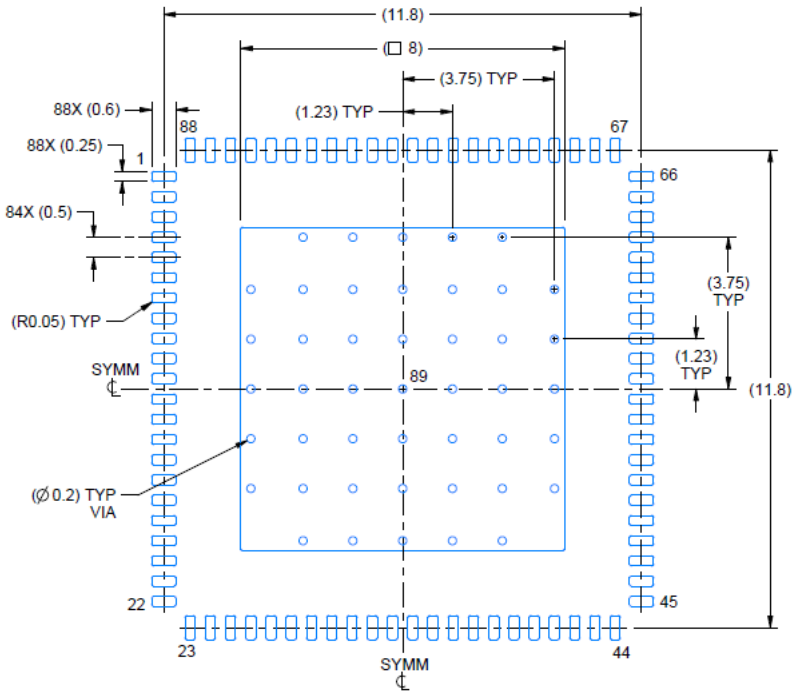
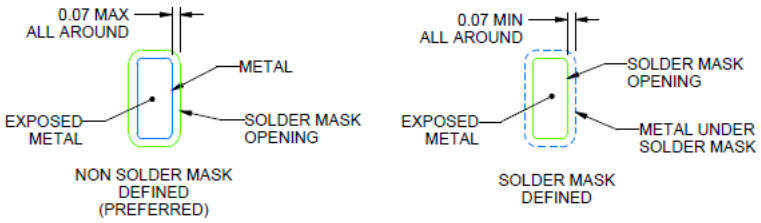
EXAMPLE BOARD LAYOUT

RUR0088D **VQFNP - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:7X



SOLDER MASK DETAILS

4225781/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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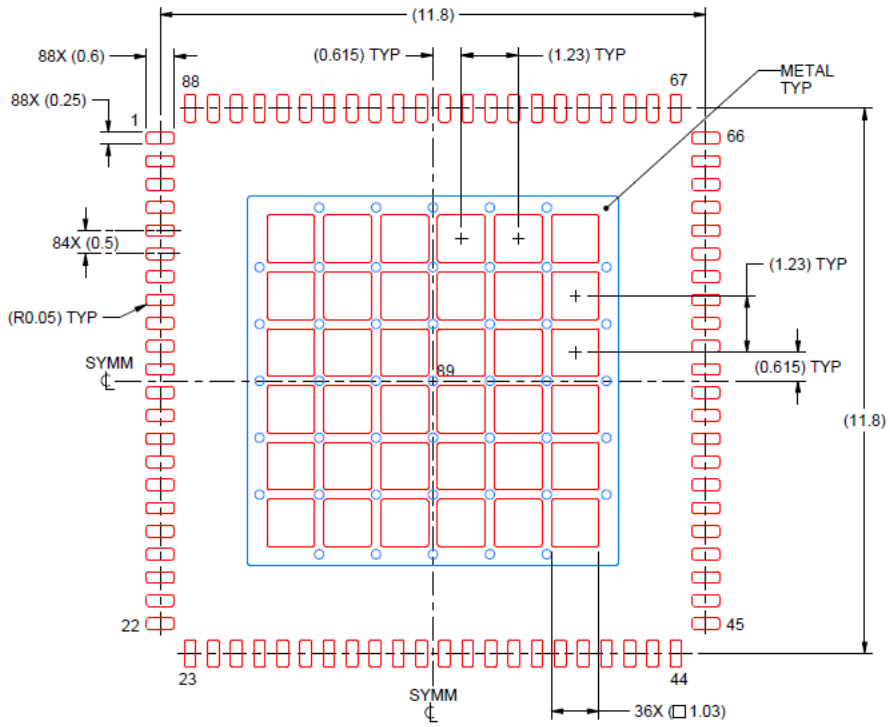
EXAMPLE STENCIL DESIGN

RUR0088D **VQFNP - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 89:
60% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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