
STM32
CubeMX

1. Description

1.1. Project

Project Name	MCU.Unirecon.Ecliptar
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 6.2.0
Date	04/15/2021

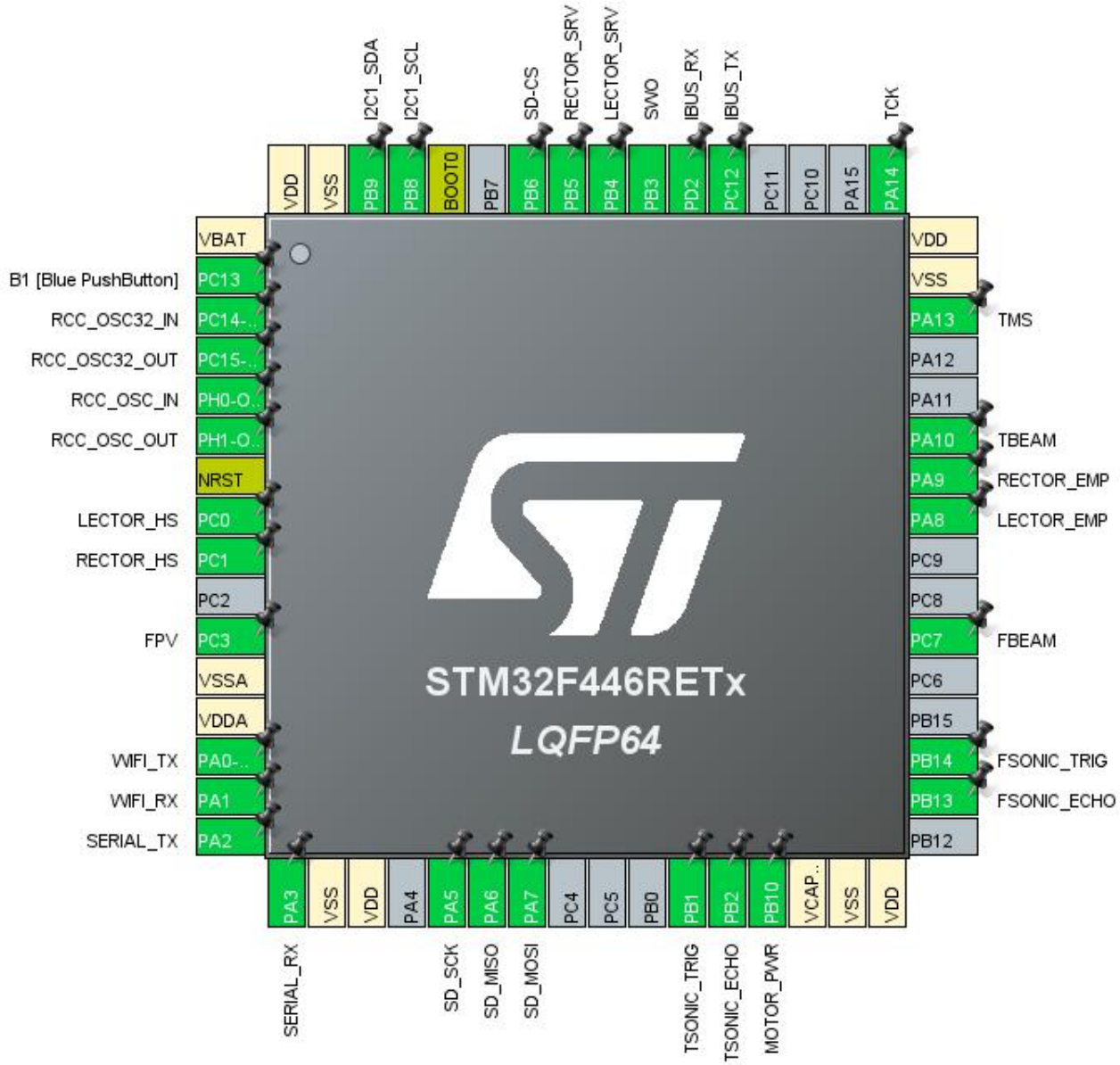
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



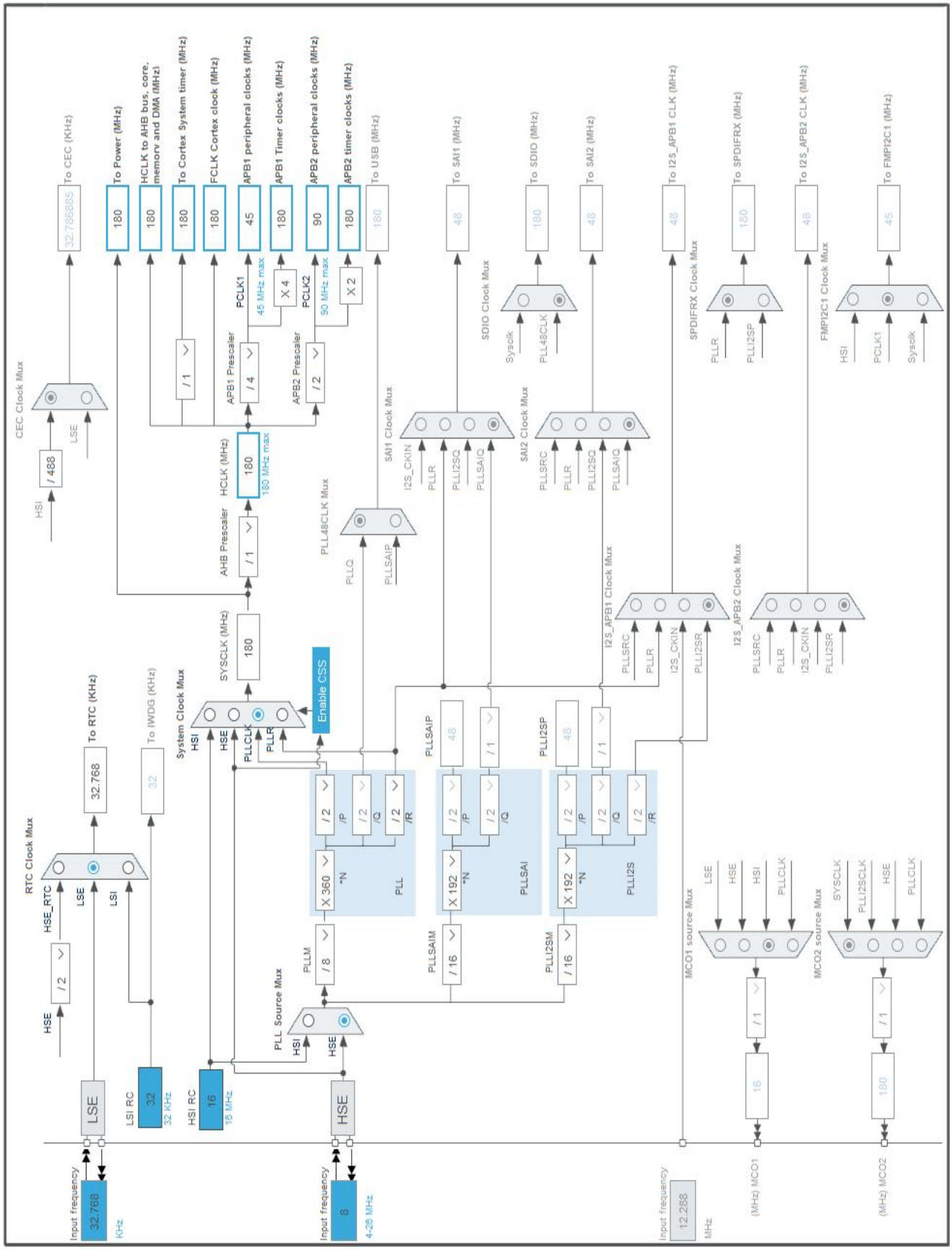
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN10, ADC3_IN10	LECTOR_HS
9	PC1	I/O	ADC2_IN11, ADC3_IN11	RECTOR_HS
11	PC3 *	I/O	GPIO_Output	FPV
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	UART4_TX	WIFI_TX
15	PA1	I/O	UART4_RX	WIFI_RX
16	PA2	I/O	USART2_TX	SERIAL_TX
17	PA3	I/O	USART2_RX	SERIAL_RX
18	VSS	Power		
19	VDD	Power		
21	PA5	I/O	SPI1_SCK	SD_SCK
22	PA6	I/O	SPI1_MISO	SD_MISO
23	PA7	I/O	SPI1_MOSI	SD_MOSI
27	PB1 *	I/O	GPIO_Output	TSONIC_TRIG
28	PB2 *	I/O	GPIO_Input	TSONIC_ECHO
29	PB10	I/O	TIM2_CH3	MOTOR_PWR
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
34	PB13 *	I/O	GPIO_Input	FSONIC_ECHO
35	PB14 *	I/O	GPIO_Output	FSONIC_TRIG
38	PC7 *	I/O	GPIO_Output	FBEAM
41	PA8	I/O	TIM1_CH1	LECTOR_EMP
42	PA9	I/O	TIM1_CH2	RECTOR_EMP
43	PA10 *	I/O	GPIO_Output	TBEAM
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
53	PC12	I/O	UART5_TX	IBUS_TX
54	PD2	I/O	UART5_RX	IBUS_RX
55	PB3	I/O	SYS_JTDO-SWO	SWO
56	PB4	I/O	TIM3_CH1	LECTOR_SRV
57	PB5	I/O	TIM3_CH2	RECTOR_SRV
58	PB6 *	I/O	GPIO_Output	SD-CS
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MCU.Unirecon.Ecliptar.Vos
Project Folder	E:_DEVELING_PROJECTS\MCU\Unirecon\EcliptarSTM\Ecliptar4
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_USART2_UART_Init	USART2
5	MX_SPI1_Init	SPI1
6	MX_TIM1_Init	TIM1
7	MX_TIM2_Init	TIM2
8	MX_TIM3_Init	TIM3
9	MX_UART5_Init	UART5
10	MX_I2C1_Init	I2C1
11	MX_CRC_Init	CRC

Rank	Function Name	Peripheral Instance Name
12	MX_UART4_Init	UART4
13	MX_ADC1_Init	ADC1
14	MX_ADC2_Init	ADC2
15	MX_RTC_Init	RTC
16	MX_ADC3_Init	ADC3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

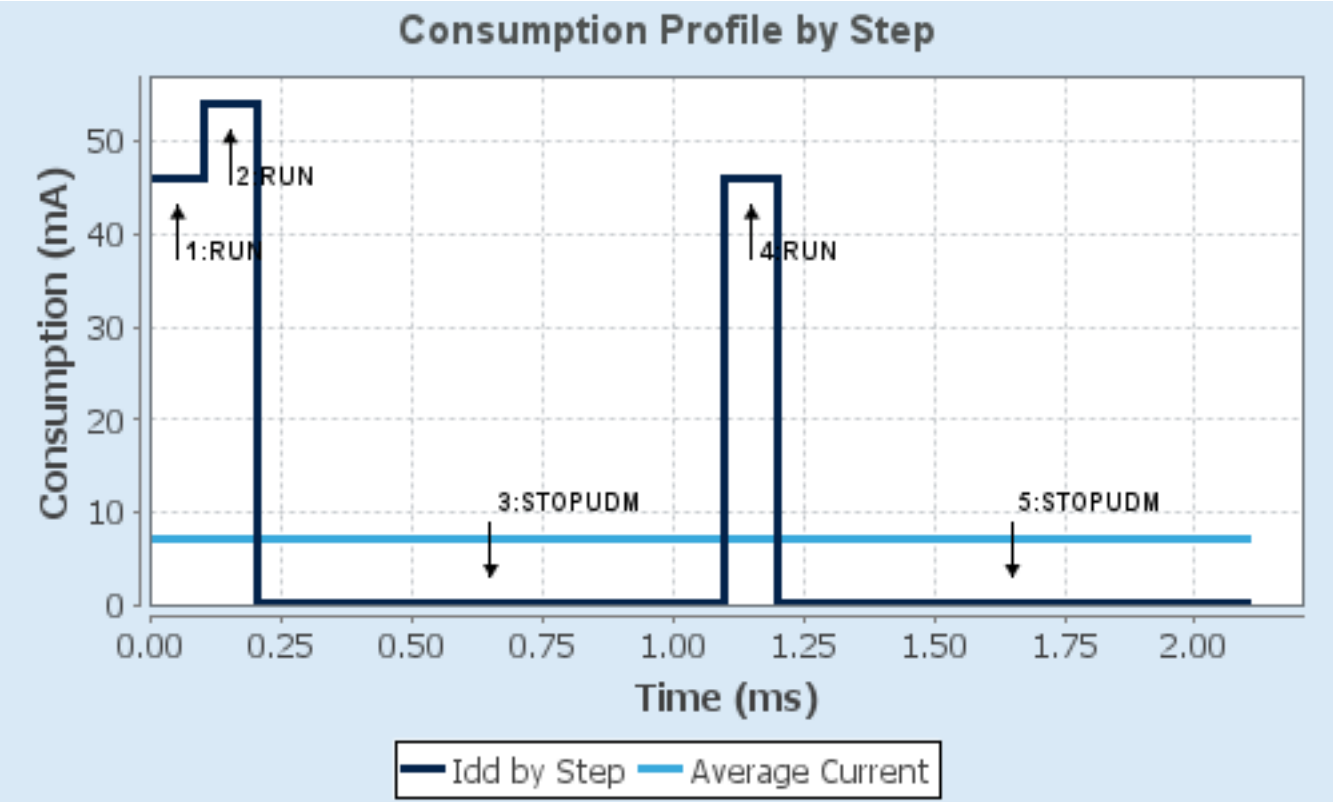
6.4. Sequence

Step	Step1	Step2	Step3	Step4	Step5
Mode	RUN	RUN	STOP_UDM (Under Drive)	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3	3.3	3.3	3.3
Voltage Source	Battery	Battery	Battery	Battery	Battery
Range	Scale1-High	Scale1-High	No Scale	Scale1-High	No Scale
Fetch Type	RAM/FLASH/ REGON/ART/ PREFETCH	RAM/FLASH/ REGON/ART/ PREFETCH	n/a	RAM/FLASH/ REGON/ART/ PREFETCH	n/a
CPU Frequency	180 MHz	180 MHz	0 Hz	180 MHz	0 Hz
Clock Configuration	HSE PLL	HSE PLL	Regulator_LP Flash-PwrDwn	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	4 MHz	0 Hz	4 MHz	0 Hz
Peripherals		ADC1 GPIOA GPIOB GPIOC GPIOD GPIOH I2C1 SPI1 SYS TIM1 TIM2 TIM3 UART5 USART2 USART3			
Additional Cons.	0 mA	0 mA	0 mA	0 mA	0 mA
Average Current	46 mA	54.17 mA	55 µA	46 mA	55 µA
Duration	0.1 ms	0.1 ms	0.9 ms	0.1 ms	0.9 ms
DMIPS	225.0	225.0	0.0	225.0	0.0
Ta Max	98.02	96.78	104.99	98.02	104.99
Category	In DS Table	In DS Table	In DS Table	In DS Table	In DS Table

6.5. Results

Sequence Time	2 ms	Average Current	7.01 mA
Battery Life	20 days, 4 hours	Average DMIPS	225.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN10

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 6 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 10
Sampling Time	**112 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN11

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 6 ***
Resolution	12 bits (15 ADC Clock cycles)

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Enabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 11
Sampling Time	**112 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. ADC3

mode: IN10

mode: IN11

7.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 6 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Enabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 10
Sampling Time	

	144 Cycles *
Rank	**2 ***
Channel	**Channel 11 ***
Sampling Time	**144 Cycles ***
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

7.4. CRC

mode: Activated

7.5. I2C1

I2C: I2C

7.5.1. Parameter Settings:

Master Features:	
I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000
Slave Features:	
Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.6.1. Parameter Settings:

System Parameters:	
VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled

Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	**Enabled ***
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

7.7. RTC

mode: Activate Clock Source

mode: Activate Calendar

7.7.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

7.8. SPI1

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**2.8125 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.9. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

7.10. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2047 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	**Enable ***
BRK Polarity	**Low ***

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable

Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	**Enable ***
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.11. TIM2

Clock Source : Internal Clock

Channel3: PWM Generation CH3

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**2047 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.12. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**44 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**39999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**3000 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**3000 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.13. UART4

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.14. UART5

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.15. USART2

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	LECTOR_HS
ADC2	PC1	ADC2_IN11	Analog mode	No pull-up and no pull-down	n/a	RECTOR_HS
ADC3	PC0	ADC3_IN10	Analog mode	No pull-up and no pull-down	n/a	LECTOR_HS
	PC1	ADC3_IN11	Analog mode	No pull-up and no pull-down	n/a	RECTOR_HS
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_SCK
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	LECTOR_EMP
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	RECTOR_EMP
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	MOTOR_PWR
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	LECTOR_SRV
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	RECTOR_SRV
UART4	PA0-WKUP	UART4_TX	Alternate Function Push Pull	Pull-up	**Very High ***	WIFI_TX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA1	UART4_RX	Alternate Function Push Pull	Pull-up	**Very High ***	WIFI_RX
UART5	PC12	UART5_TX	Alternate Function Push Pull	Pull-up	**Very High ***	IBUS_TX
	PD2	UART5_RX	Alternate Function Push Pull	Pull-up	**Very High ***	IBUS_RX
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SERIAL_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SERIAL_RX
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FPV
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TSONIC_TRIG
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TSONIC_ECHO
	PB13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FSONIC_ECHO
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FSONIC_TRIG
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FBEAM
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TBEAM
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SD-CS

8.2. DMA configuration

DMA request	Stream	Direction	Priority
UART4_RX	DMA1_Stream2	Peripheral To Memory	Low
UART4_TX	DMA1_Stream4	Memory To Peripheral	Low
ADC1	DMA2_Stream0	Peripheral To Memory	Low
ADC2	DMA2_Stream2	Peripheral To Memory	Low
UART5_RX	DMA1_Stream0	Peripheral To Memory	Low
UART5_TX	DMA1_Stream7	Memory To Peripheral	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low
ADC3	DMA2_Stream1	Peripheral To Memory	Low

UART4_RX: DMA1_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

UART5_RX: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART5_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC3: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream2 global interrupt	true	0	0
DMA1 stream4 global interrupt	true	0	0
DMA1 stream5 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
ADC1, ADC2 and ADC3 interrupts	true	0	0
USART2 global interrupt	true	0	0
DMA1 stream7 global interrupt	true	0	0
UART4 global interrupt	true	0	0
UART5 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream2 global interrupt	false	true	true
DMA1 stream4 global interrupt	false	true	true
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true
ADC1, ADC2 and ADC3 interrupts	false	true	true
USART2 global interrupt	false	true	true
DMA1 stream7 global interrupt	false	true	true
UART4 global interrupt	false	true	true
UART5 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream1 global interrupt	false	true	true
DMA2 stream2 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00141306.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00135183.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00155929.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note	http://www.st.com/resource/en/application_note/DM00161778.pdf
Application note	http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf