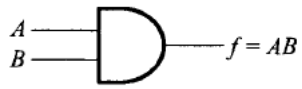
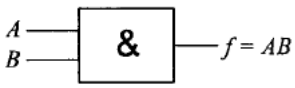
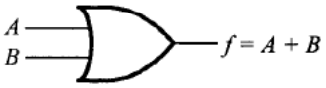
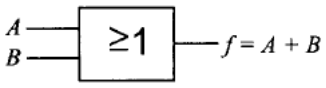
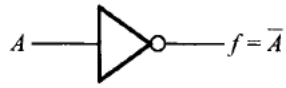
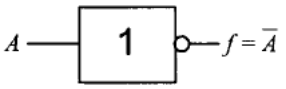
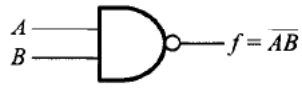
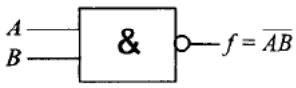
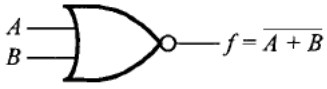
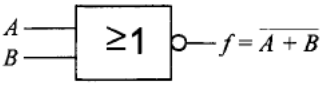
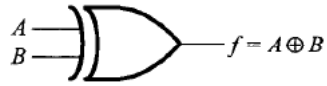
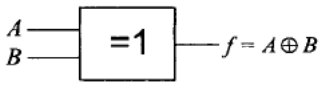
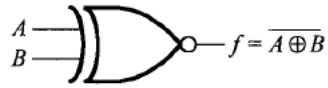
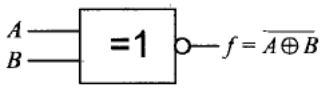
Gate	Common Symbol	IEEE Symbol
AND		
OR		
NOT		
NAND		
NOR		
Exclusive-OR		
Exclusive-NOR		

Truth table

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

x	F
0	1
1	0

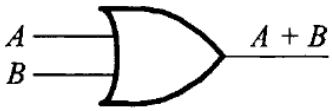
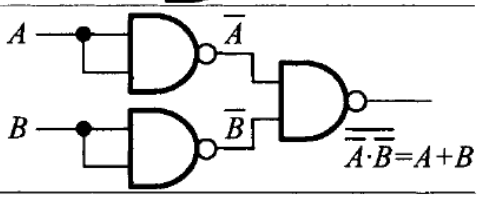
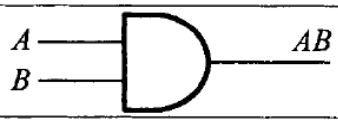
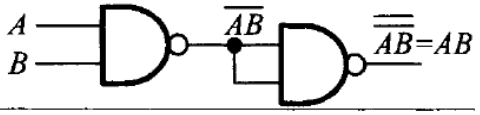
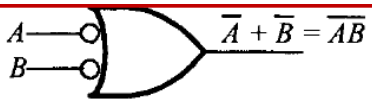
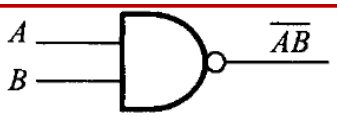
x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

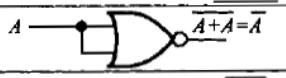
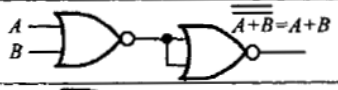
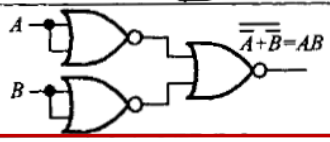
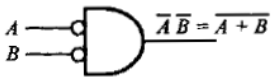
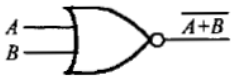
x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

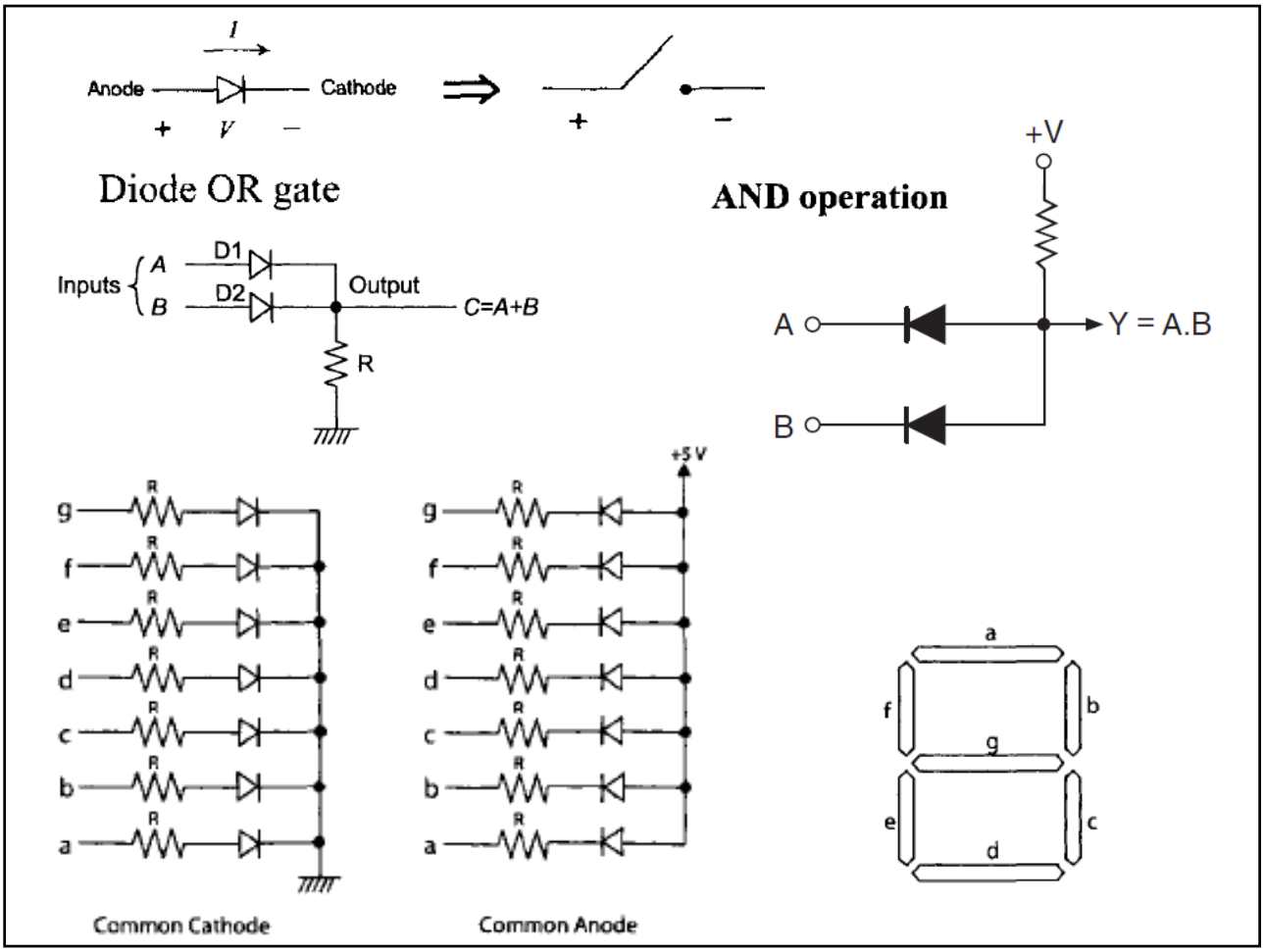
x	y	F
0	0	1
0	1	0
1	0	0
1	1	1

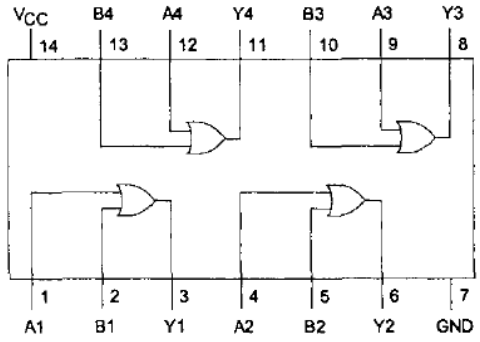
Logic equivalents using NAND gates

Gate	Symbol		Equivalent Logic Diagram using NAND Gates
NOT		⇒	
Two-input OR		⇒	
Two-input AND		⇒	
Invert-OR		⇒	

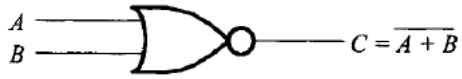
Logic equivalents using NOR gates

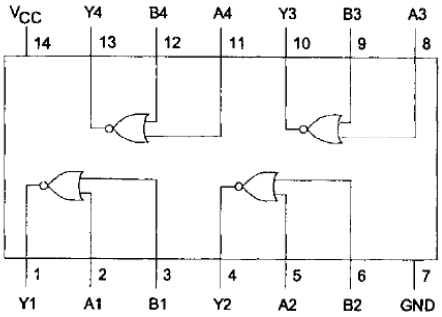
Gate	Symbol	Equivalent Logic Diagram using NOR Gates
NOT		
OR		
AND		
Invert-AND		


I
Anode
Cathode
+
V
–
+
–
Diode OR gate
Inputs
A
B
D1
D2
Output
C=A+B
R
AND operation
+V
A
B
Y = A.B
+5 V
g
f
e
d
c
b
a
R
Common Cathode
Common Anode

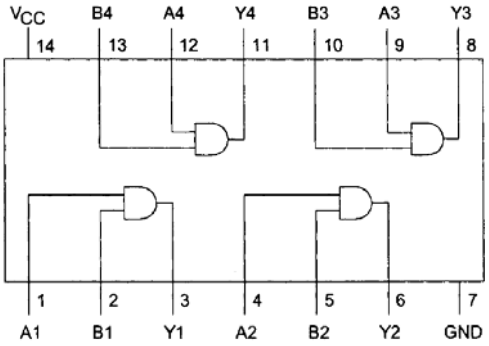


Pin diagram for 74HC32 or 74LS32

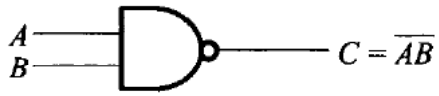


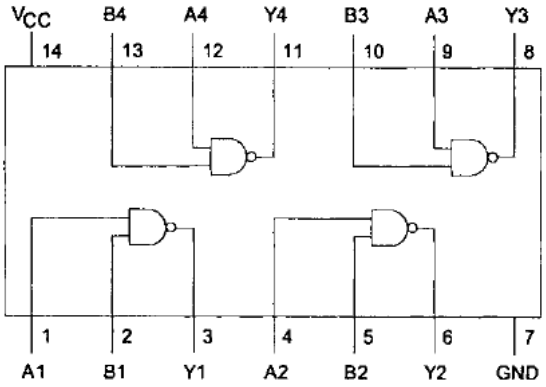


Pin diagram for 74HC02 or 74LS02



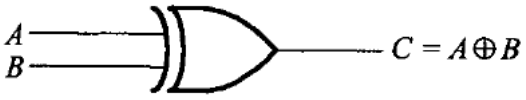
Pin Diagram for 74HC08 or 74LS08

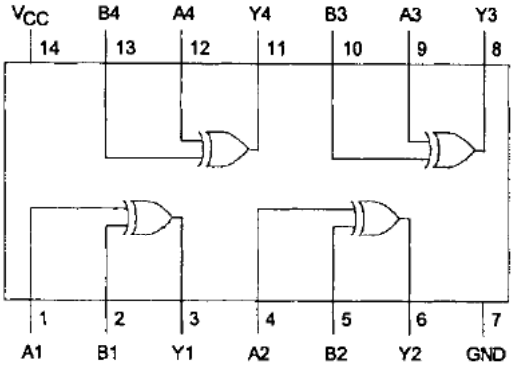




Pin diagram for 74HC00 or 74LS00

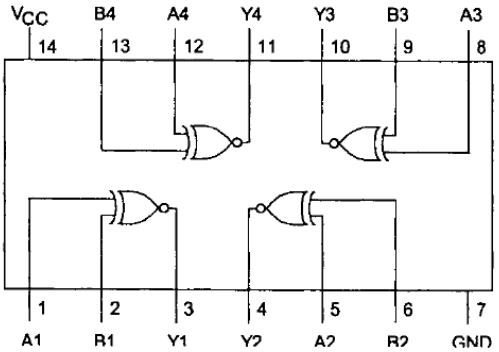
XOR symbol





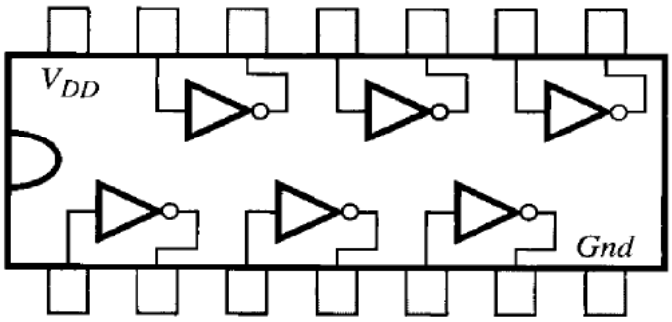
Pin diagram for 74HC86 or 74LS86

XNOR gate

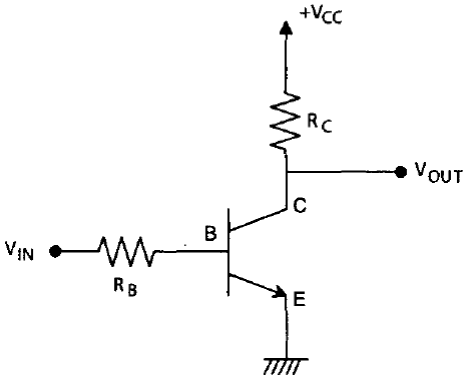


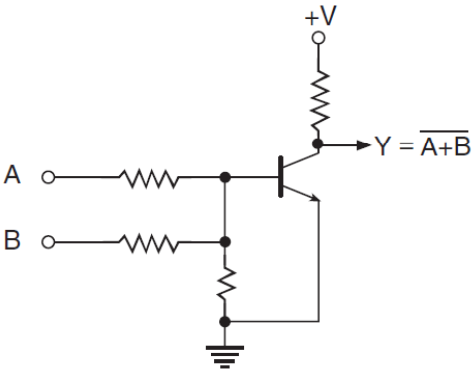
Pin Diagram for 74HC266 or 74LS266

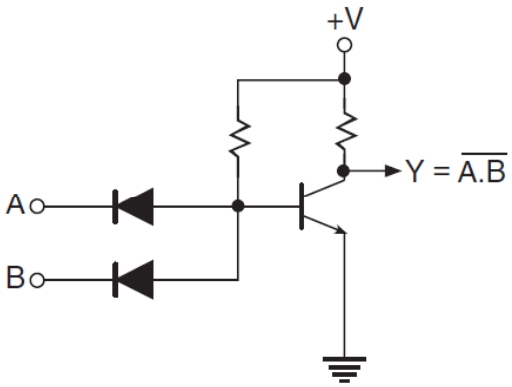
Not gate

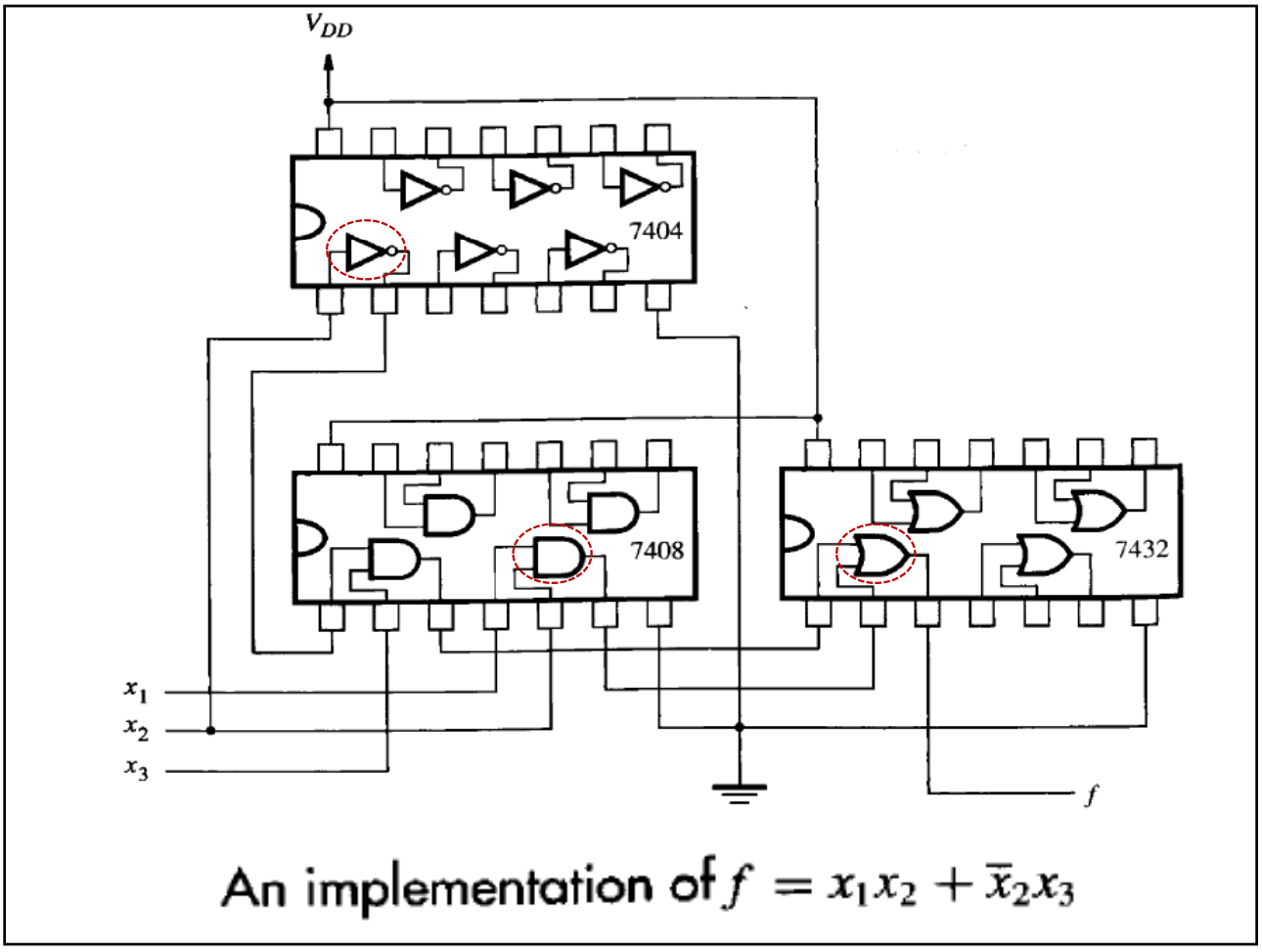


(b) Structure of 7404 chip









An implementation of $f = x_1x_2 + \bar{x}_2x_3$

IMPLEMENTATION IN FPGAs