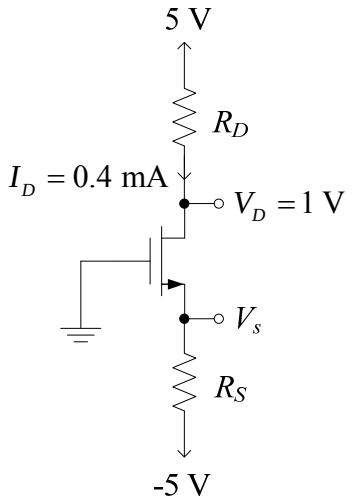
Lecture 27: MOSFET Circuits at DC.

We will illustrate the DC analysis of MOSFET circuits through a number of examples.

Example N27.1 (similar to text example 4.2). Design the circuit below so that the MOSFET operates with $I_D = 0.4$ mA and $V_D = 1$ V. The MOSFET has $V_t = 2$ V, $\mu_n C_{ox} = 20$ μA/V^2, $L = 10$ μm, and $W = 400$ μm. Neglect the channel-length modulation effect ($\lambda = 0$).



This last statement (i.e., $\lambda = 0$) means we can neglect the MOSFET output resistance ($r_o \to \infty$).

$$R_D = \frac{5 - 1}{0.4 \text{ mA}} = 10 \text{ k}\Omega$$

From this circuit we can see that $V_{GD} = -1$ V, which is less than V_t. Consequently, the channel is pinched off at the drain end. Therefore, the MOSFET is operating in the saturation or cutoff modes (not the triode).

We'll assume operation in the saturation mode. In this mode

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

Substituting

$$0.4 \text{ mA} = \frac{1}{2} 20 \times 10^{-6} \frac{\text{A}}{\text{V}^2} \cdot \frac{400}{10} (V_{GS} - 2)^2$$

Therefore

$$(V_{GS} - 2)^2 = 1 \quad \Rightarrow \quad V_{GS} - 2 = \pm 1$$

or

$$V_{GS} = +1 \text{ V or } +3 \text{ V}$$

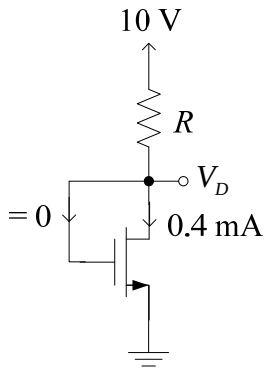
The first solution is not consistent with our initial assumption of operation in the saturation mode since it is less than V_t. Therefore,

$$V_{GS} = 3 \text{ V} \quad \Rightarrow \quad V_S = -3 \text{ V}$$

Finally,

$$R_S = \frac{V_S - (-5)}{I_S} = \frac{V_S + 5}{I_D} = \frac{-3 + 5}{0.4 \text{ mA}} = 5 \text{ k}\Omega$$

Example N27.2 (similar to text example 4.3). Design the circuit below so $I_D = 0.4$ mA. The MOSFET has $V_t = 2$ V, $\mu_n C_{ox} = 20$ μA/V^2, $L = 10$ μm, and $W = 100$ μm. Neglect r_o.



With the gate and drain terminals connected together $V_{GD} = 0$, which is not greater than V_t. This means the channel is not continuous and the MOSFET is not operating in the triode mode. We'll assume the device is operating in the saturation mode.

In saturation, $$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_t\right)^2$$

or $$0.4\times10^{-3} = \frac{1}{2}20\times10^{-6}\frac{100}{10}\left(V_{GS}-2\right)^2 \quad \Rightarrow \quad V_{GS}-2 = \pm 2$$

Consequently,

$$V_{GS} = 0 \text{ or } 4 \text{ V}$$

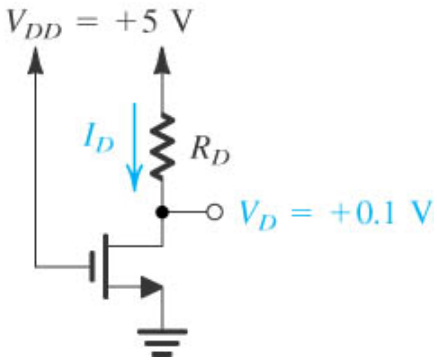
The first solution is not consistent with operation in the saturation mode since $V_{GS} < V_t$.

Hence, with $V_{GS} = 4$ V and $V_{DG} = 0$ V $\Rightarrow$ $V_D = 4$ V.

Finally, since $I_G = 0$ then

$$R = \frac{10 - V_D}{0.4 \text{ mA}} = \frac{10-4}{0.4}\ \text{k}\Omega = 15\ \text{k}\Omega$$

Example N27.3 (text example 4.4). Design the circuit below for a drain voltage of 0.1 V. Determine r_{DS}. The MOSFET has $V_t = 1$ V and $k_n' W/L = 1$ mA/V^2. Neglect r_o.



(Fig. 4.22)

With $V_{GS} = 5$ V and greater than V_t, the MOSFET has an induced channel and is not cutoff.

Next, let's check to see if the channel is pinched off at the drain end. We can do this two (equivalent) ways. First, with $V_D = 0.1$ V then

$$V_{GD} = 5 - 0.1 = 4.9 \text{ V}$$

which is greater than V_t (= 1 V), so the channel is not pinched off at the drain. Alternatively, we can compute

$$V_{GS} - V_t = 5 - 1 = 4 \text{ V}$$

which is greater than V_{DS} (= 0.1 V). So again we find that the channel is not pinched off at the drain.

Either of these two results means the MOSFET is operating in the triode mode (continuous channel).

In the triode region,

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$= 1\times 10^{-3}\left[(5-1)0.1 - \frac{1}{2}(0.1)^2\right]$$

so that $I_D = 0.395 \text{ mA}$

Then $R_D = \dfrac{5-0.1}{0.395} \text{ k}\Omega = 12.41 \text{ k}\Omega$

and $r_{DS} = \dfrac{V_{DS}}{I_D} = \dfrac{0.1}{0.395} \text{ k}\Omega = 253 \ \Omega$

We could also use (4.13) for this last result, but the work was already done here. From the text,

$$r_{DS} \equiv \left.\frac{v_{DS}}{i_D}\right|_{\substack{v_{DS} \text{ small} \\ v_{GS}=V_{GS}}} = \left[k_n' \frac{W}{L}(V_{GS} - V_t)\right]^{-1} \qquad (4.13)$$

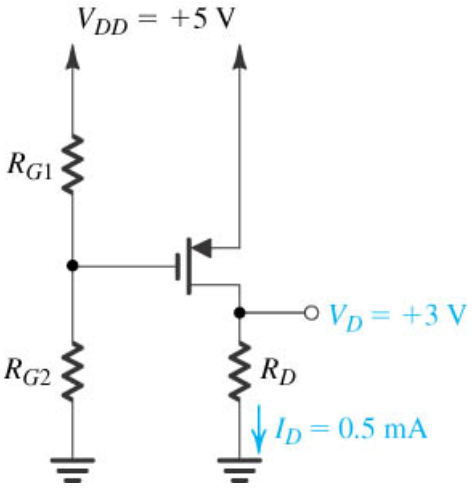
Using the values above,

$$r_{DS} = \left[10^{-3}\cdot(5-1)\right]^{-1} = 250 \ \Omega.$$

This value is slightly different than what was calculated earlier. Which one is correct? Why is the other not as accurate?

Example N27.4 (text example 4.6). Design the circuit below so that the MOSFET is operating in the saturation mode with $I_D = 0.5$ mA and $V_D = 3$ V. What is the largest R_D such that the

MOSFET remains in the saturation mode? The MOSFET has $V_t = -1$ V and $k_p' W/L = 1$ mA/V^2. Neglect r_o.



(Fig. 4.24)

For saturation in an enhancement type PMOS device requires

$$V_{GS} \le V_t \text{ (induced)} \quad \text{or} \quad V_{SG} \ge |V_t| \text{ (induced)} \qquad (4.27)$$

and

$$V_{DS} \le V_{GS} - V_t \quad \text{(pinched off)} \qquad (4.31)$$

In words, this last equation states that the drain-to-source voltage must be less than the gate-to-source voltage plus $|V_t|$.

In the saturation mode (with $\lambda = 0$)

$$I_D = \frac{1}{2} k_p' \frac{W}{L} (V_{GS} - V_t)^2 \qquad (4.32)$$

or $$0.5 \times 10^{-3} = \frac{1}{2} \cdot 1 \times 10^{-3} (V_{GS} + 1)^2$$

Therefore, $V_{GS} + 1 = \pm 1 \Rightarrow V_{GS} = 0$ or -2 V.

The first result is not consistent with operation in the saturation mode since $V_{GS} \le V_t$ must be met for saturation. Consequently,

$$V_G = 5 + V_{GS} = 5 - 2 = 3 \text{ V}$$

R_{G1} and R_{G2} must be chosen such that

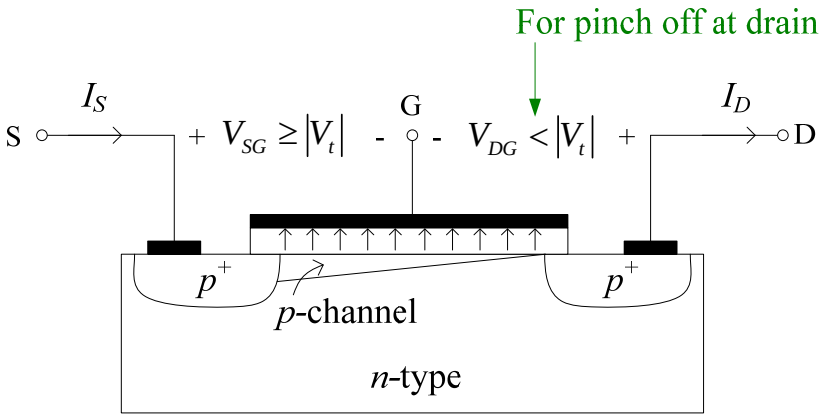
$$V_G = \frac{R_{G2}}{R_{G1}+R_{G2}} \cdot V_S \quad \text{or} \quad \frac{3}{5} = \frac{R_{G2}}{R_{G1}+R_{G2}}$$

The text chooses $R_{G1} = 2\ \text{M}\Omega$ and $R_{G2} = 3\ \text{M}\Omega$ to satisfy this requirement. (Why did the book use such large values for R_{G1} and R_{G2}?)

The drain resistor can be determined from the circuit above

$$R_D = \frac{3}{0.5}\ \text{k}\Omega = 6\ \text{k}\Omega$$

For the largest R_D, remember that the PMOS device remains in the saturation mode as long as the drain end of the channel is pinched off.



Pinch off at the drain end requires

$$V_{DG} < |V_t| \quad \text{(pinched off)}$$

which holds up to the point where V_D exceeds V_G by $|V_t|$. That is,

$$V_{D_{\max}} = V_G + |V_t| = 3 + 1 = 4\ \text{V}.$$

From this result,

$$R_{D_{\max}} = \frac{V_{D_{\max}}}{I_D} = \frac{4\ \text{V}}{0.5\ \text{mA}} = 8\ \text{k}\Omega.$$