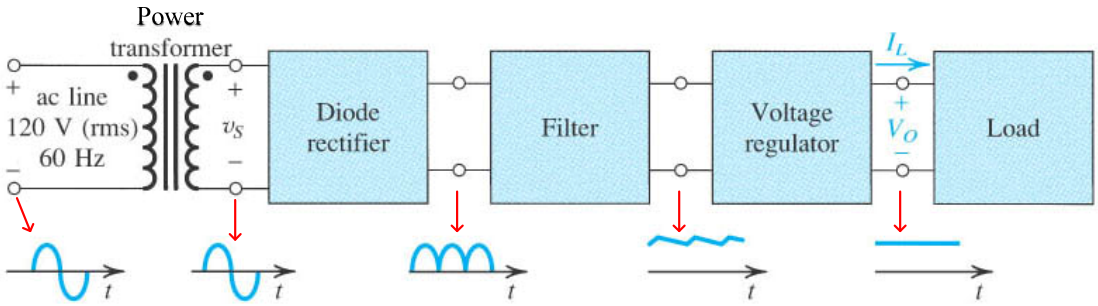
Lecture 7: Diode Rectifier Circuits (Half Cycle, Full Cycle, and Bridge).

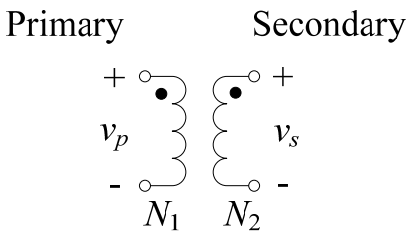
We saw in the previous lecture that Zener diodes can be used in circuits that provide (1) voltage overload protection, and (2) voltage regulation.

An important application of "regular" diodes is in rectification circuits. These circuits are used to convert AC signals to DC in power supplies.

A block diagram of this process in a DC power supply is shown below in text figure 3.24:



In this DC power supply, the first stage is a transformer:



An ideal transformer changes the amplitude of **time varying voltages** as

$$v_s = \frac{N_2}{N_1} v_p \tag{1}$$

This occurs even though there is no direct contact between the input and output sections. This "magic" is described by Faraday's law:

$$\oint_{C(S)} \bar{E} \cdot d\bar{l} = \frac{-d}{dt} \int_{S(C)} \bar{B} \cdot d\bar{s}$$

or

$$\text{emf} = -\frac{d\psi_m}{dt} \tag{2}$$

By varying the ratio N_2/N_1 in (1) we can increase or decrease the output voltage relative to the input voltage:

- If $N_2 > N_1$, have a step-up transformer
- If $N_2 < N_1$, have a step-down transformer.

For example, to convert wall AC at ~120 V_{RMS} to DC at, say, 13.8 V_{DC}, we need a step down transformer with a ratio of:

$$\frac{N_2}{N_1} \approx \frac{15}{120} = \frac{1}{8} \quad \text{or} \quad 8{:}1 \text{ ratio } (N_1 : N_2).$$

We choose $v_s \approx 15$ V_{DC} for a margin.

For the remaining stages in this DC power supply:

- Diode rectifier. Gives a "unipolar" voltage, but pulsating with time.
- Filter. Smoothes out the pulsation in the voltage.

- Regulator. Removes the ripple to produce a nearly pure DC voltage.

We will now concentrate on the rectification of the AC signal. We'll cover filtering in the next lecture.

Diode Rectification

We will discuss three methods for diode rectification:

1. Half-cycle rectification.
2. Full-cycle rectification.
3. Bridge rectification. (This is probably the most widely used.)

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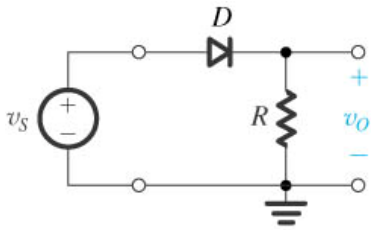
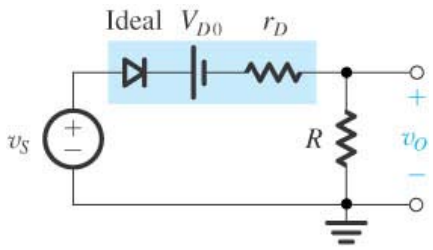
1. Half-Cycle Rectification

We've actually already seen this circuit before in this class!



(Fig. 3.25a)

We will use the PWL model for the diode to construct the equivalent circuit for the rectifier:



(Fig. 3.25b)

From this circuit, the output voltage will be zero if $v_S(t) < V_{D0}$.

Conversely, if $v_S(t) > V_{D0}$ we can determine v_O by superposition of the two sources (DC and AC) in the circuit sources since we have linearized the diode:

- DC: $v_O'(t) = -V_{D0}\dfrac{R}{R+r_D}$
- AC: $v_O''(t) = v_S(t)\dfrac{R}{R+r_D}$

Notice that we're not making a small AC signal assumption here. Rather, we have used the assumption of the PWL model to completely linearize this problem when $v_S(t) > V_{D0}$ and then used superposition of the two sources, which just happen to be DC and AC sources. (Consequently, we should not use r_d here.)

The total voltage is the sum of the DC and AC components:

$$v_O(t) = v_O'(t) + v_O''(t) = \left[v_S(t) - V_{D0}\right]\frac{R}{R+r_D} \quad v_S(t) > V_{D0}$$

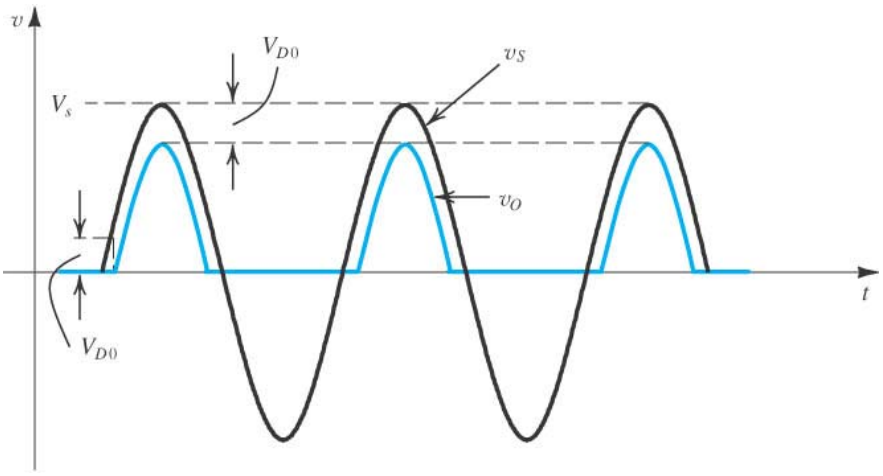
(3.21),(3)

For $v_S(t) < V_{D0}$, $v_O(t) = 0$.

In many applications, $r_D \ll R$ so that $R/(R+r_D) \approx 1$. Hence,

$$v_O(t) = \begin{cases} 0 & v_S(t) < V_{D0} \\ v_S(t) - V_{D0} & v_S(t) > V_{D0} \end{cases} \qquad (3.22),(4)$$

A sketch of this last result is shown in the figure below.



(Fig. 3.25d)

There are two important device parameters that must be considered when selecting rectifier diodes:

1. Diode current carrying capacity.
2. Peak inverse voltage (PIV). This is the largest reverse voltage across the diode. The diode must be able to withstand this voltage without shifting into breakdown.

For the half-cycle rectifier with a periodic waveform input having a zero average value

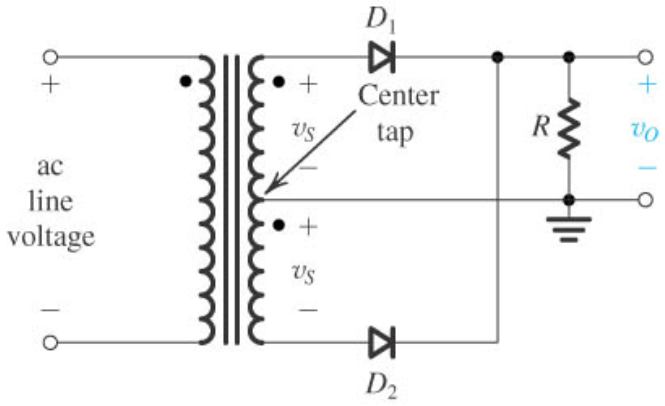
$$\text{PIV} = V_s \qquad (5)$$

where V_s is the amplitude of v_S.

2. Full-Cycle Rectification

One disadvantage of half-cycle rectification is that one half of the source waveform is not utilized. No power from the source will be converted to DC during these half cycles when the input waveform is negative in Fig. 3.25d.

The full-cycle rectifier, on the other hand, utilizes both the positive and negative portions of the input waveform. An example of a full-cycle rectifier circuit is:

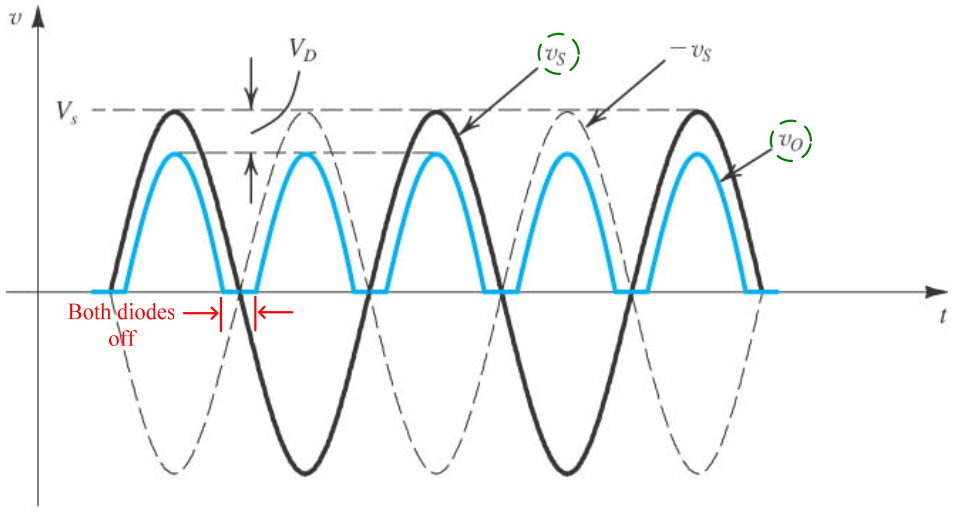


(Fig. 3.26a)

Notice that the transformer has a center tap that is connected to ground.

On the positive half of the input cycle $v_S > 0$, which implies that D_1 is "on" and D_2 is "off." Conversely, on the negative half of the input cycle, $v_S < 0$ which implies that D_1 is "off" and D_2 is "on."

In both cases, the output current $i_O(t) \geq 0$ and the output voltage $v_O(t) \geq 0$:



(Fig. 3.26c)

While this full-cycle rectifier is a big improvement over the half-cycle, there are a couple of disadvantages:

- $\text{PIV} = 2V_s - V_{D0}$, which is about twice that of the half-cycle rectifier. This fact may require expensive or hard-to-find diodes.
- Requires twice as many transformer windings on the secondary as does the half-cycle rectifier.

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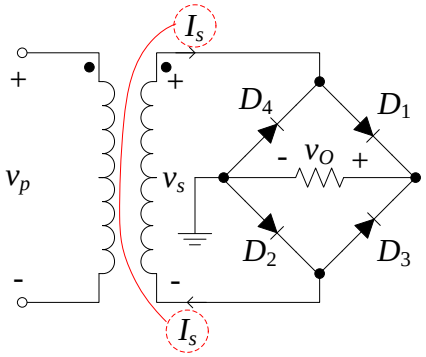
3. Bridge Rectification

The bridge rectifier uses four diodes connected in the famous bridge pattern:

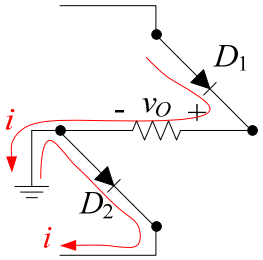


Oftentimes these diodes can be purchased as a single, four-terminal device.

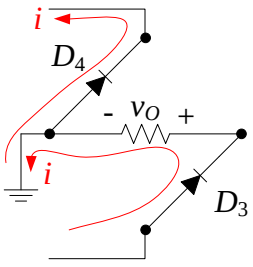
Note that the bridge rectifier does not require a center-tapped transformer, but uses four diodes instead.

The operation of the bridge rectifier can be summarized as:

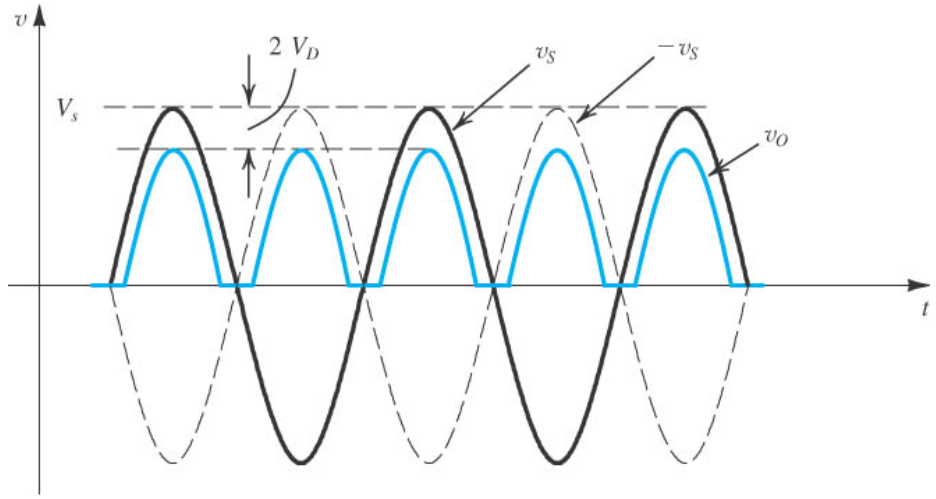
1. When $v_S(t) > 0$ then D_1 and D_2 are "on" while D_3 and D_4 are "off":



2. When $v_S(t) < 0$ then D_1 and D_2 are "off" while D_3 and D_4 are "on":



In both cases, though, $v_O(t) > 0$:



(Fig. 3.27b)

The bridge rectifier is the most popular rectifier circuit. Advantages include:

- PIV $= V_s - V_{D0}$, which is approximately the same as the half-cycle rectifier.
- No center tapped transformer is required, as with the half-cycle rectifier.