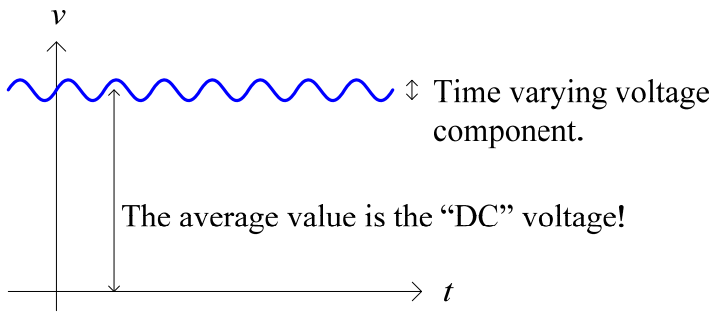
Lecture 4: Small-Signal Diode Model and Its Application.

The diode analysis so far has focused only on DC signals. We must also consider the application of diodes in circuits with time varying signals. This analysis is also complicated by the nonlinear nature of the diode.

"Large signal" analysis of diode circuits is often best left for circuit simulation packages. Conversely, "small signal" analysis of nonlinear diode circuits can sometimes be done by hand.

The concept behind small-signal operation is that a time varying signal with small amplitude "rides" on a DC value that may or may not be large.

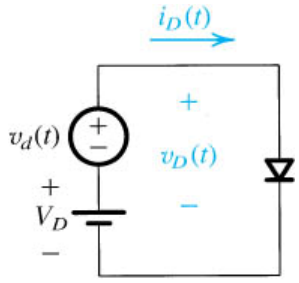


The analysis of the circuit is then divided into two parts:

1. DC "bias"
2. AC "signal" of small amplitude.

and the solutions are added together using superposition.

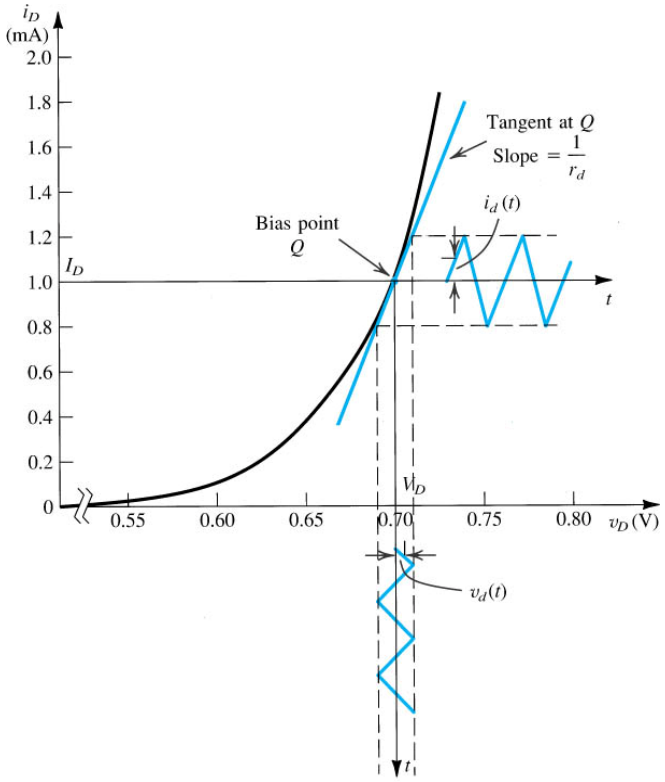
For example:



(Fig. 3.17a)

where $v_d(t)$ is some time varying waveform, perhaps periodic such as a sinusoid or triangle signal.

The purpose of V_D in this circuit is to set the operation of the diode about a point on the forward bias *i-v* characteristic curve of the diode. This is called the quiescent point, or Q point, and the process of setting these DC values is called biasing the diode.



(Fig. 3.17b)

The total voltage at any time t is the sum of the DC and AC components

$$v_D(t) = V_D + v_d(t) \qquad (3.10),(1)$$

provided the AC signal is small enough that the diode operates approximately in a linear fashion. (See Section 1.4.9 for a discussion on the symbol convention used in your text.)

The diode current is (3.1) with $i_D(t) >> I_S$ such that

$$i_D(t) \approx I_S e^{\frac{v_D(t)}{nV_T}} = \underbrace{I_S e^{\frac{V_D}{nV_T}}}_{=I_D} e^{\frac{v_d(t)}{nV_T}}$$

or

$$i_D(t) = I_D e^{\frac{v_d(t)}{nV_T}} \qquad (3.12),(2)$$

where I_D is the DC diode current.

We can series expand the exponential term using

$$e^x = 1 + x + \frac{x^2}{2!} + \cdots$$

and if $v_d(t)$ is small enough so that $v_d(t)/(nV_T) << 2$, truncate the series to two terms:

$$e^{\frac{v_d(t)}{nV_T}} \approx 1 + \frac{v_d(t)}{nV_T} \qquad (3)$$

Substituting (3) in (2) gives

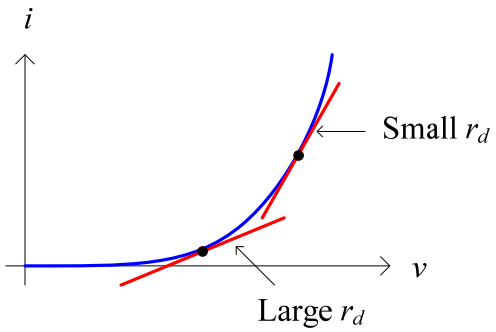
$$i_D(t) \approx I_D + \frac{I_D}{nV_T} v_d(t) \qquad (3.14),(4)$$

So, if $v_d(t)$ is small enough we can see from this last equation that i_D is the sum (or superposition) of two components: DC and AC signals. What we've done is to linearize the problem by limiting the AC portion of v_D to small values.

The term nV_T/I_D has units of ohms. It is called the diode small-signal resistance:

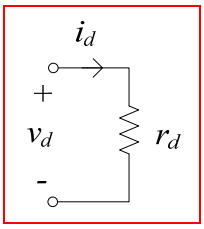
$$r_d \equiv \frac{nV_T}{I_D} \ [\Omega] \qquad (3.18),(5)$$

From a physical viewpoint, r_d is the inverse slope of the tangent line at a particular bias point along the characteristic curve of the diode. Note that r_d changes depending on the (DC) bias:



(Note that this r_d is a fundamentally different quantity than r_D used in the PWL model of the diode discussed in the previous lecture.)

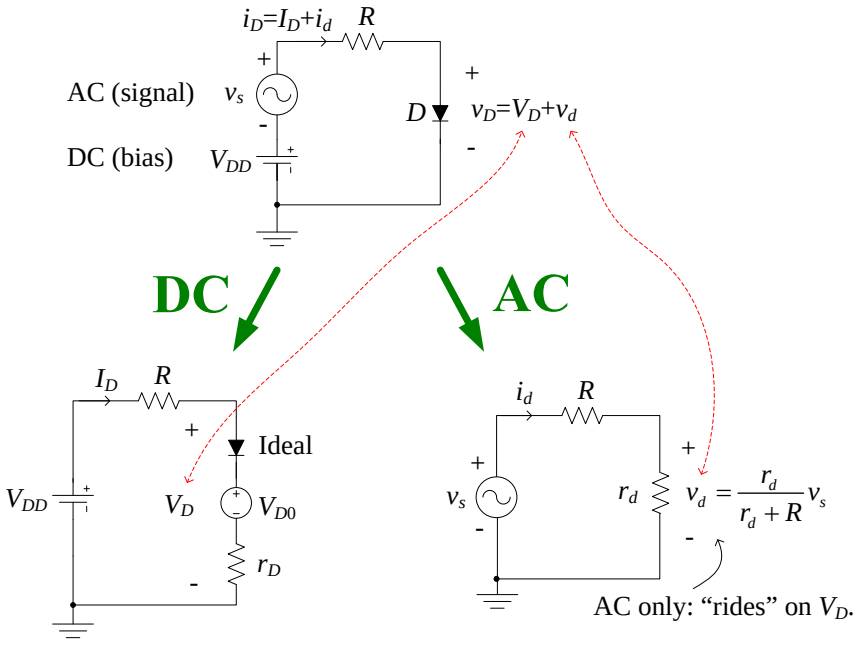
The equivalent circuit for the small-signal operation of diodes is:



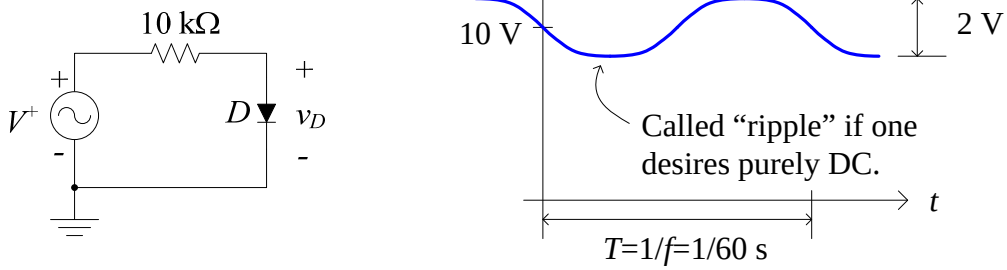
Because we have linearized the operation of the diode (by restricting the analysis to small AC signals), we can use superposition to analyze the composite DC and AC signals.

That is, "signal analysis is performed by eliminating all DC sources" (short out DC voltage sources/open circuit DC current sources) "and replacing the diode with its small-signal resistance r_d."

This process is illustrated below:



Example N4.1 (Text example 3.6). For the circuit shown below, determine v_D when $V^+ = 10 + 1 \cdot \cos\left(2\pi \cdot 60t\right)$ V.



The diode specifications are

- 0.7-V drop at 1 mAdc
- n = 2.

As we discussed, for small AC signals we can separate the DC analysis from the AC (i.e., linearized). We need to start with the DC bias. Assuming $V_D \approx 0.7$ V for a silicon diode the DC current is

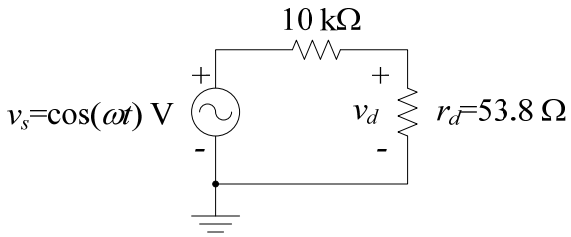
$$I_D = \frac{10 - 0.7}{10{,}000} = 0.93 \text{ mA}$$

Since $I_D \approx 1$ mA, then V_D will be very close to the assumed value.

At this DC bias, then the small-signal resistance at the Q point is

$$r_d = \frac{nV_T}{I_D} = \frac{2 \cdot 25 \times 10^{-3}}{0.93 \times 10^{-3}} = 53.8 \ \Omega$$

We use this r_d as the equivalent resistance in the small-signal model of the diode



The AC voltage across the diode is found from voltage division as

$$v_d(t) = \frac{r_d}{r_d + 10{,}000} v_s = \frac{53.8}{53.8 + 10{,}000} \cdot \cos(\omega t)$$

$$= 5.35 \cos(\omega t) \text{ mV}$$

The corresponding phasor diode voltage is then

$$v_d = 5.35 \text{ mV}_\text{p} = 10.70 \text{ mV}_\text{pp}$$

where the subscript "p" indicates a peak value and the "pp" subscript means a peak-to-peak value.

Were we justified in using a small-signal assumption for this problem? From page 3, let's check if $v_d(t)/(nV_T) << 2$:

$$\frac{v_d}{nV_T} = \frac{5.35 \times 10^{-3}}{2 \cdot 25 \times 10^{-3}} = 0.107$$

which is much less than 2. So, yes, the small-signal assumption is valid here.

As an aside, note that in this circuit the ripple in the voltage has been reduced at the output. At the input, the ripple is 2/10=20%

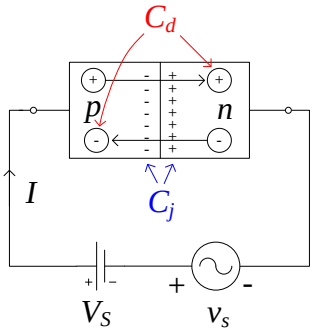
of the DC component while at the output the ripple is 0.0107/0.7=1.5% of the DC component.

See text example 3.7 for another example of this ripple reduction.

Diode High Frequency Model

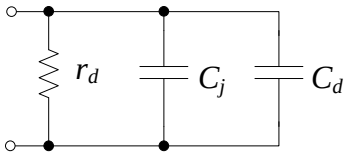
This purely resistive AC model for the diode works well when the frequency of the AC signals is sufficiently low.

At high frequencies, we need to include the effects that arise due to these time varying signals and the charge separation that exists in the depletion region and in the bulk *p* and *n* regions of the diode under forward bias conditions.



Within the device and the depletion region there exists an electric field, as discussed in Lecture 2. For AC signals, this electric field is varying with time.

As you've learned in electromagnetics, a time varying electric field is a displacement current. The effects of a displacement current are modeled by equivalent circuit capacitances:



We won't do anything with this effect now. This is presented primarily as an FYI. (However, later in the course we will investigate this capacitive junction effect in transistors and how it affects the gain of transistor amplifier circuits at high frequencies.)