6

MOS Field-Effect Transistors (MOSFETs)

- A three-terminal device that uses the voltages of the two terminals to control the current flowing in the third terminal.
  - The basis for amplifier design.
  - The basis for switch design.
  - The basic element of integrated circuits.
- Applications
  - Signal amplification.
  - Digital logic.
  - Memory, and so on.
- Circuit symbol

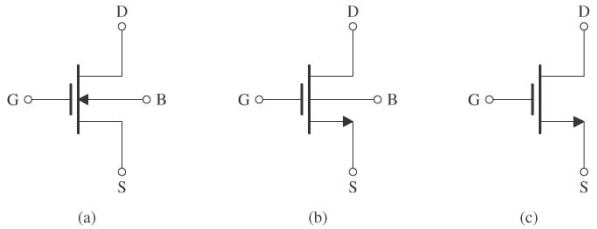


Figure 6.1: (a) Circuit symbol for the n-channel enhancement-type MOSFET. (b) Modified circuit symbol. (c) Simplified circuit symbol.

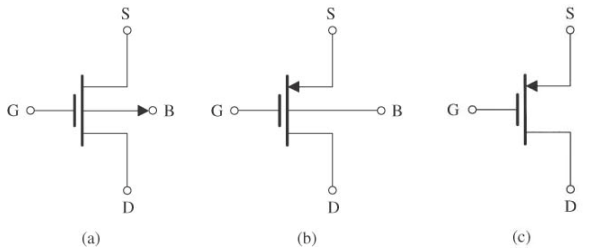


Figure 6.2: (a) Circuit symbol for the p-channel enhancement-type MOSFET. (b) Modified circuit symbol. (c) Simplified circuit symbol.

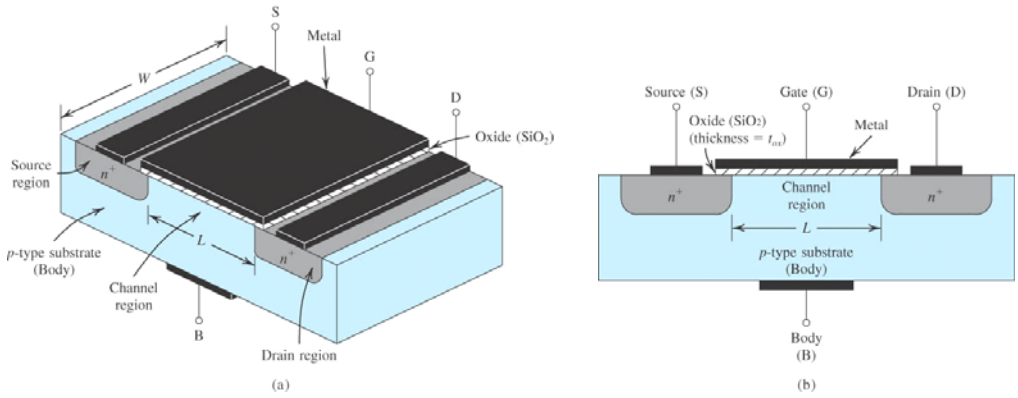


Figure 6.3: Physical structure of the enhancement-type NMOS transistor.

6.1 Structure

6.1.1 Physical Structure

- Enhancement-type NMOS transistor (Figure 6.3)
  - Structure
    - Body (B)
      - The device is fabricated on a *p-type* substrate.
    - Source (S) and Drain (D)
      - Two heavily doped *n-type* regions.
      - Charges carriers are electrons.
      - Current flows from drain to source.
    - Gate electrode (G)
      - A thin layer of silicon dioxide (SiO_2), which is an electrical insulator.
      - Polysilicon is deposited on top of the oxide layer.
    - Mental contacts are made to the regions of source, drain, and body.
  - The substrate forms *pn*-junctions with the source and drain regions.
    - The *pn*-junctions are reverse-biased.
      - The drain (D) is at a positive voltage relative to the source (S).
      - The *pn*-junctions is cut-off by connecting the body (B) to the source (S).
      - The MOSFET is thus treated as a three-terminal device.
- Enhancement-type PMOS transistor
  - Structure
    - Body (B)
      - The device is fabricated on a *n-type* substrate.
    - Source (S) and Drain (D)
      - Two heavily doped *p-type* regions.

        - Charges carriers are holes.
        - Current flows from source to drain.
      - Gate electrode (G)
        - A thin layer of silicon dioxide (SiO_2), which is an electrical insulator.
        - Polysilicon is deposited on top of the oxide layer.
      - Mental contacts are made to the regions of source, drain, and body.
  - The source and drain regions form *pn*-junctions with the substrate.
    - The *pn*-junctions are reverse-biased.
      - The source (S) is at a positive voltage relative to the drain (D).
      - The *pn*-junctions is cut-off by connecting the body (B) to the drain (D).
      - The MOSFET is thus treated as a three-terminal device.
  - NMOS transistor is smaller and faster than PMOS transistor.
  - PMOS operates in the same manner as NMOS excepts that v_{GS} and v_{DS} are negative and the threshold voltage V_t is negative.
- Complementary MOS (CMOS, Figure 6.4)
  - CMOS employs MOS transistors of both polarities.
    - NMOS is implemented directly in *p-type* substrate.
    - PMOS is fabricated in a created *n* region, known as **n well**.
    - The two devices are isolated by a thick region of SiO_2.
  - CMOS is widely used in both analog and digital circuits and virtually replace designs based on NMOS alone.

6.2 Characteristics of NMOS Transistor

- Figure 6.5 depict the $i_D - v_{DS}$ characteristic of a NMOS transistor.

6.2.1 Cut-off Region ($v_{GS} < V_t$)

- When $v_{GS} < V_t$, the transistor is turned off.
  - No current flow from drain to source.
  - As $v_{GS} = 0$, two back-to-back diodes exists in series between source and drain.
- In reality, for values of v_{GS} smaller than V_t but close to V_t, a small drain current flows.
  - The subthreshold current is an exponential function of v_{GS}.

6.2.2 Triode ($v_{GS} > V_t$, $0 < v_{DS} < v_{GS} - V_t$)

- $v_{GS} > 0$ (refer to Figure 6.6).
  - Holes in substrate.
    - The holes are pushed downward, leaving behind a carrier-depletion region.

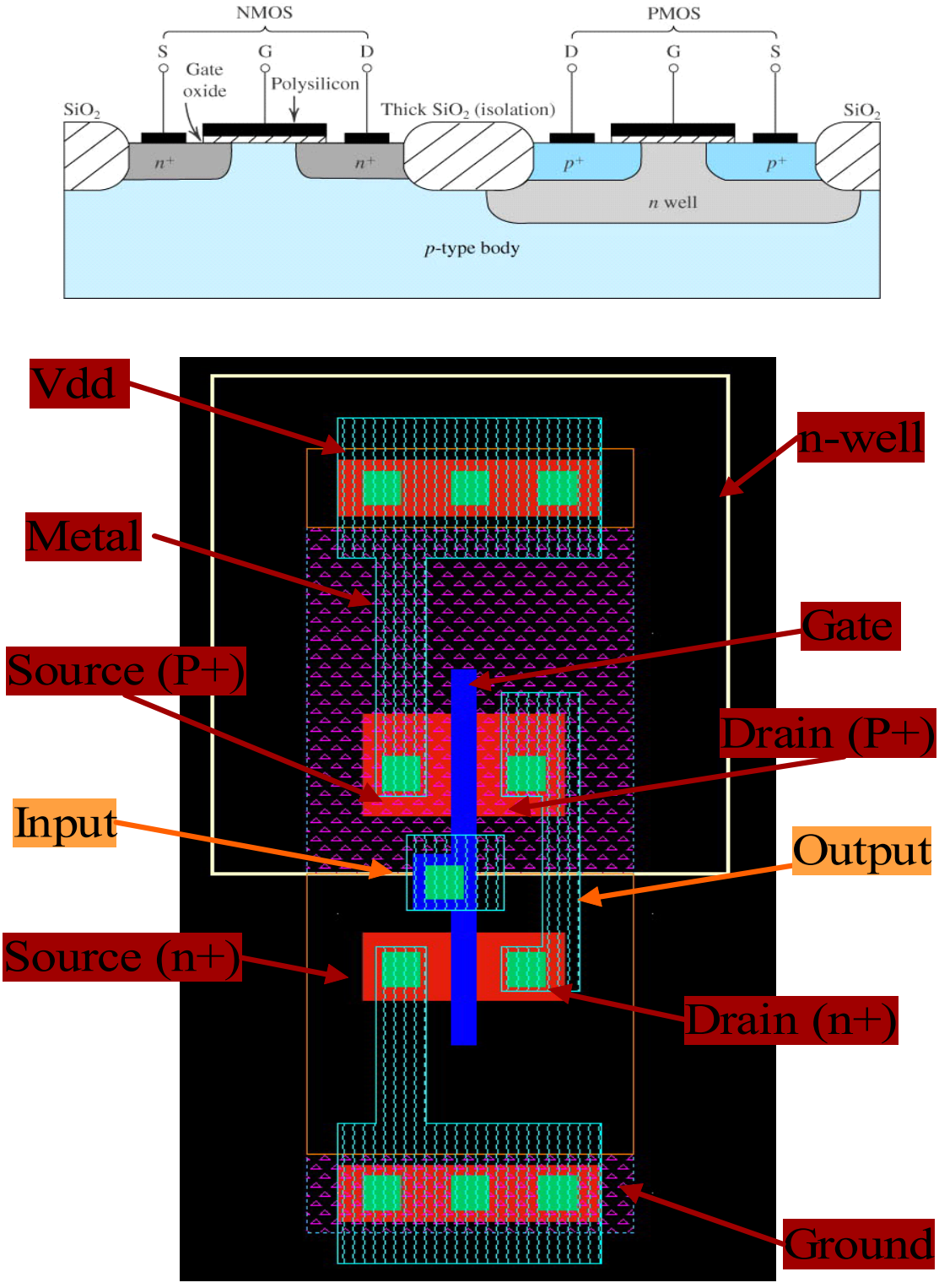


Figure 6.4: Corss-section of a CMOS integrated circuit and the layout mask (Courtesy of NCTU Si2 Lab).

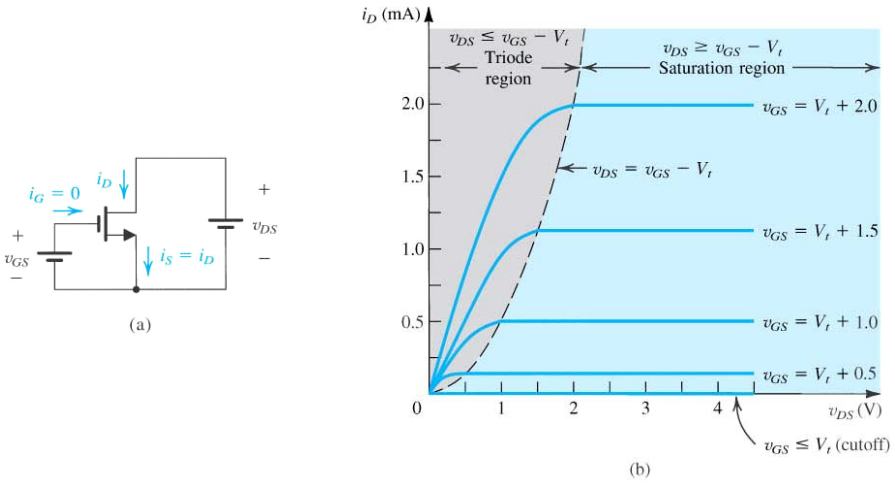


Figure 6.5: $i_D - v_{DS}$ characteristic for a NMOS transistor .

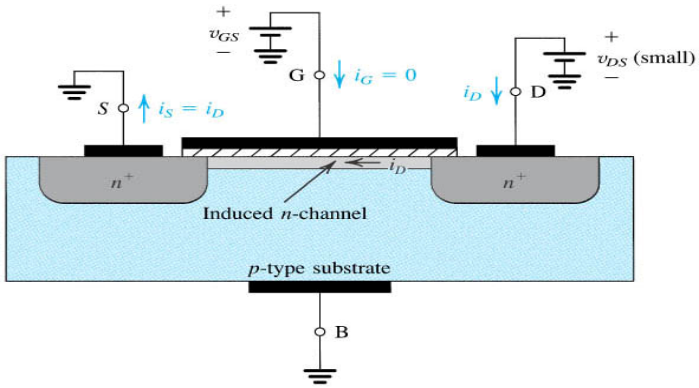


Figure 6.6: The enhancement-type NMOS with $v_{GS} > V_T$ and with a small v_{DS}.

  - ∗ The depletion region is populated by the bound negative charge.
  - Electrons in drain and source.
    - ∗ Positive gate voltage attracts electrons from the n^+ source and drain.
    - ∗ Electrons accumulate near the surface of the substrate under the gate and form a "channel" connecting the source and the drain.
  - The threshold voltage V_t is the value of v_{GS} at which a sufficient number of electrons form a channel.
- The $i_D - v_{DS}$ curve in triode region ($v_{GS} > V_t$) is specified by Eq. (6.1).

$$i_D = k'_n \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \tag{6.1}$$

  - ∗ L is the length of the channel.

  - $*$ W is the width of the channel.
  - $*$ k'_n is a constant (process transconductance parameter) determined by the process technology.
- Drain current is proportional to the aspect ratio W/L.
- For a given process technology, there is a minimum channel length $L_{\min}$ and a minimum channel width $W_{\min}$.

- $v_{DS} \simeq 0$ (refer to Figure 6.6).
  - v_{DS} causes a current i_D to flow through the induced n channel from drain to source.
  - i_D depends on the density of electrons in the channel, which in turn depends on v_{GS}.
  - The transistor acts like a resistor with the resistance controlled by v_{GS}.
    - The conductance of the channel is proportional to the excess gate voltage $(v_{GS} - V_t)$, as shown in Figure 6.7 and Eq. (6.2).

$$\begin{aligned} r_{DS} &= g_{DS}^{-1} = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1} \\ &= \left[k'_n \frac{W}{L}\left[(v_{GS} - V_t) - v_{DS}\right]\right]^{-1} \\ &\simeq \left[k'_n \frac{W}{L}(v_{GS} - V_t)\right]^{-1} \\ &\simeq \frac{v_{DS}}{i_D} \end{aligned} \tag{6.2}$$

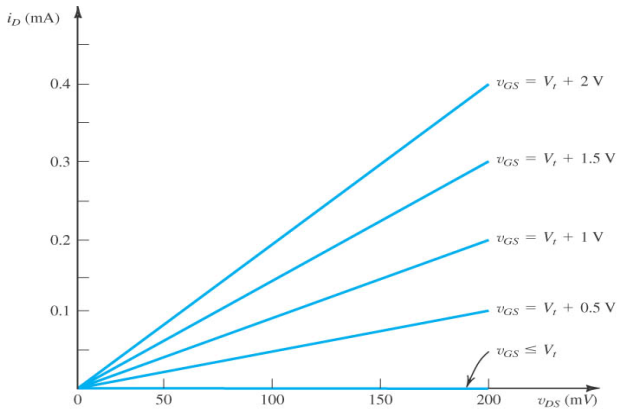


Figure 6.7: The $i_D - v_{DS}$ characteristics of the MOSFET with small v_{DS}.

- $0 < v_{DS} < v_{GS} - V_t$ (refer to Figure 6.8).
  - The voltage between the gate and points along the channel decreases from v_{GS} at the source to $v_{GS} - v_{DS}$ at the drain, as shown in Figure 6.8.
    - Channel becomes more tapered when v_{DS} is increased.
    - Resistance of channel increases when v_{DS} is increased.

· The $i_D - v_{DS}$ curve bends as shown in Figure 6.5.

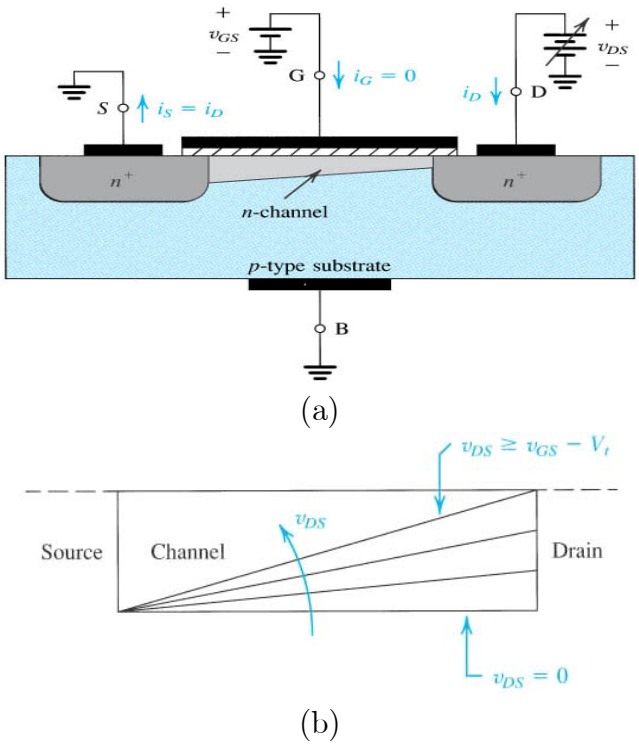


Figure 6.8: The change of channel shape when the drain-source voltage is increased.

6.2.3 Saturation ($v_{GS} > V_t$, $v_{DS} > v_{GS} - V_t$)

- As $v_{DS} = v_{GS} - V_t$, the channel pinches-off.
  - The drain current i_D can be obtained by substituting $v_{DS} = v_{DS_{sat}} = v_{GS} - V_t$ in Eq. (6.1).

$$i_D = k'_n \frac{W}{L} \frac{1}{2} (v_{GS} - V_t)^2 \tag{6.3}$$

  - The drain current i_D is independent of the drain voltage v_{DS} (in a first-order approximation) and is determined by the gate voltage v_{GS}.
    - Ideally, the Large-Signal model for NMOS is an ideal current source controlled by v_{GS}.
- Finite output resistance
  - In practice, increasing v_{DS} beyond v_{DSsat} does affect the channel.
  - **Channel-length modulation** (refer to Figure 6.10)
    - As v_{DS} is increased, the depletion region increases and the pinch-off point moves toward the source.

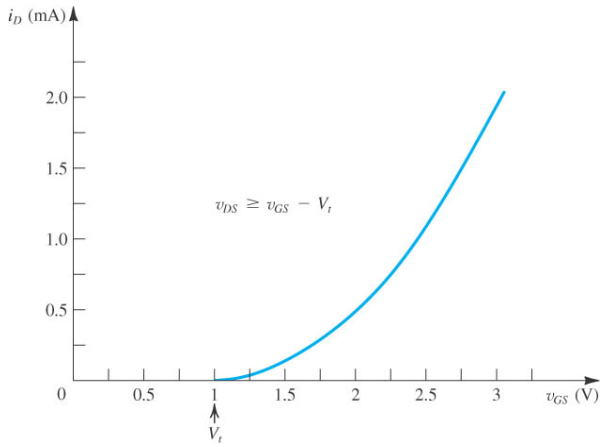


Figure 6.9: The $i_D - v_{GS}$ characteristic for a NMOS transistor in saturation region.

∗ Eq (6.4) shows the $i_D - v_{DS}$ characteristic with channel-length modulation.

$$\begin{aligned} i_D &= \frac{1}{2}k'_n\frac{W}{L-\triangle L}(v_{GS}-V_t)^2 \\ &\simeq \frac{1}{2}k'_n\frac{W}{L}(1+\frac{\triangle L}{L})(v_{GS}-V_t)^2 \\ &= \frac{1}{2}k'_n\frac{W}{L}(1+\frac{\lambda' v_{DS}}{L})(v_{GS}-V_t)^2 \\ &= \frac{1}{2}k'_n\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) \end{aligned} \tag{6.4}$$

∗ λ is a process technology parameter and can be obtained as in Figure 6.11.
- V_A is referred to as the Early voltage.
- V_A typically falls in the range of $0.9V - 9V$.

$$\begin{aligned} i_D &\simeq \frac{1}{2}k'_n\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) = 0 \\ &\Rightarrow \lambda = -\frac{1}{v_{DS}} = \frac{1}{V_A} \end{aligned} \tag{6.5}$$

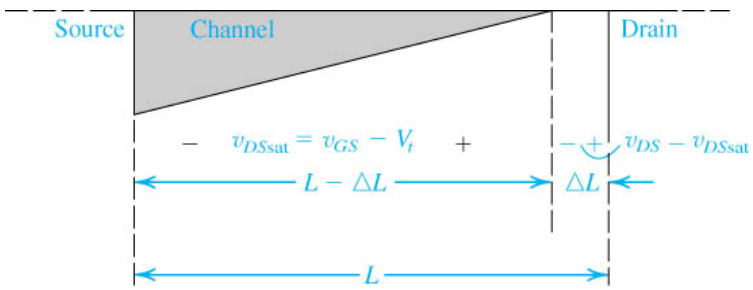


Figure 6.10: As v_{DS} is increased beyond v_{DSsat}, the pinch-off point is moved toward the source.

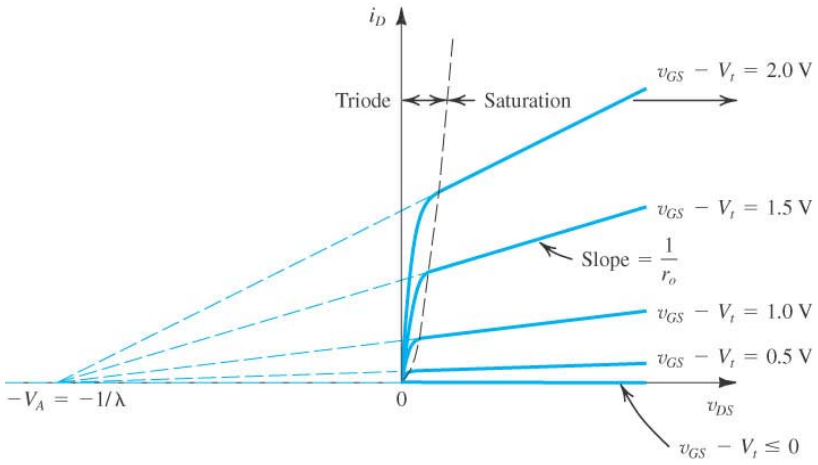


Figure 6.11: Effect of v_{DS} on i_D in saturation region.

- – Equivalent output resistance r_o
  - ∗ Inversely proportional to the drain current I_D without considering Early effect.

$$i_D = \frac{1}{2}k'_n\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) = I_D(1 + \lambda v_{DS}) \tag{6.6}$$

  - ∗ Controlled by $(v_{GS} - V_t)$.

$$\begin{aligned} r_o &= \frac{\Delta v_{DS}}{\Delta i_D} = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \\ &= \frac{V_A}{i_D}(1 + \lambda v_{DS}) \\ &= \frac{V_A}{i_D} + \frac{v_{DS}}{i_D} \end{aligned} \tag{6.7}$$

  – Figure 6.12 shows the large signal equivalent model of the NMOS in saturation region.

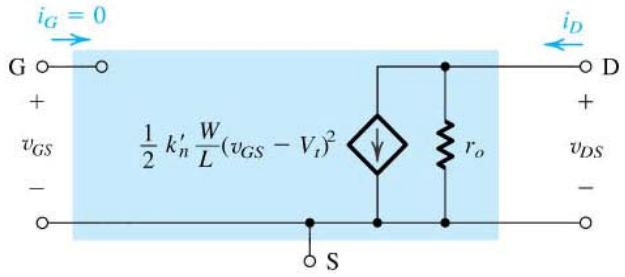


Figure 6.12: Large signal equivalent model of the NMOS in saturation region.

- Figure 6.13 recaps the relative levels of terminal voltage of the NMOS transistor for operation in different regions.

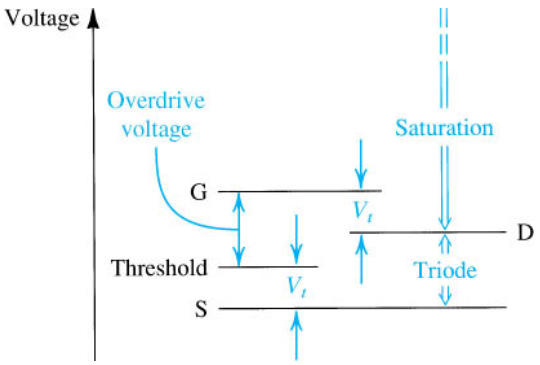
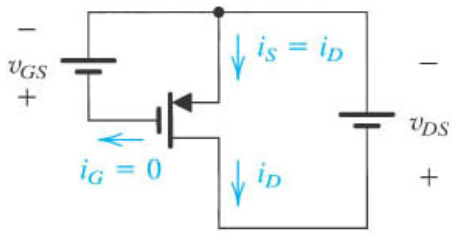


Figure 6.13: The relative levels of the terminal voltages of the NMOS transistor for operation in the triode region and in the saturation region.

6.3 Characteristics of PMOS Transistor



(d)

Figure 6.14: The PMOS with voltages applied and the directions of current flow indicated.

- The threshold voltage V_t (relative to the source terminal) is negative.
- Cut-off region
  - The gate voltage v_{GS} (relative to the source terminal) is greater than V_t.

$$\begin{aligned} & v_{GS} > V_t = -|V_t| \\ \Rightarrow \quad & v_{SG} < |V_t| \end{aligned} \tag{6.8}$$

- Triode region
  - To induce a channel, we apply a gate voltage that is more negative than V_t.

$$\begin{aligned} & v_{GS} \leq V_t = -|V_t| \\ \Rightarrow \quad & v_{SG} \geq |V_t| \end{aligned} \tag{6.9}$$

  - To prevent the channel from pinch-off, drain voltage v_{DS} must be higher than

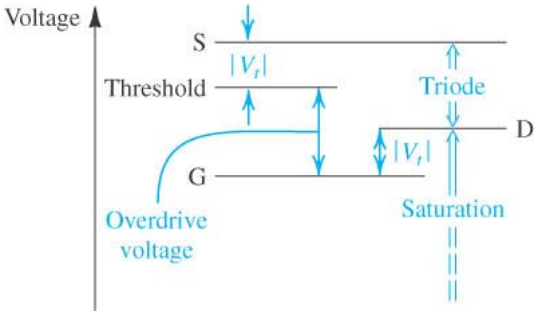


Figure 6.15: The relative levels of the terminal voltages of the PMOS.

gate voltage v_{GS} by at least $|V_t|$.

$$\begin{aligned} & v_{DS} > v_{GS} - V_t = v_{GS} + |V_t| \\ \Rightarrow \quad & v_{SD} \leq v_{SG} - |V_t| \end{aligned} \tag{6.10}$$

- The $i_D - v_{DS}$ characteristic is exactly the same as the NMOS.
  - v_{DS}, v_{GS},and V_t are negative values.

$$\begin{aligned} i_D &= k_p' \frac{W}{L} \left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right] \\ &= k_p' \frac{W}{L} \left[(v_{SG} - |V_t|) v_{SD} - \frac{1}{2} v_{SD}^2 \right] \end{aligned} \tag{6.11}$$

- Saturation
  - To operate in saturation, drain voltage v_{DS} must be <u>lower</u> than $(v_{GS} + |V_t|)$.

$$\begin{aligned} & v_{DS} \leq v_{GS} - V_t = v_{GS} + |V_t| \\ \Rightarrow \quad & v_{SD} > v_{SG} - |V_t| \end{aligned} \tag{6.12}$$

  - The $i_D - v_{DS}$ characteristic is exactly the same as the NMOS.
    - λ, v_{DS}, v_{GS},and V_t are negative values.

$$\begin{aligned} i_D &\simeq \frac{1}{2} k_p' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \\ &= \frac{1}{2} k_p' \frac{W}{L} (v_{SG} - |V_t|)^2 (1 + |\lambda| \, v_{SD}) \end{aligned} \tag{6.13}$$

- Figure 6.15 recaps the relative levels of terminal voltage of the PMOS transistor for operation in different regions.

6.3.1 Body Effect

- In integrated circuits, the substrate (body) is common to many MOS transistors.

- To maintain cut-off for all the substrate-to-channel junctions
  - The body is connected to the most negative power supply in an NMOS circuit.
  - The body is connected to the most positive power supply in a PMOS circuit.
- The reverse bias voltage v_{SB} widens the depletion regions and decreases the depth of the channel.
  - The increasing of v_{SB} causes an increase in the threshold voltage V_t.
    - V_{t0} is the threshold voltage with $v_{SB} = 0$.
    - γ is the body effect parameter.
    - 2ϕ is the surface potential parameter.

$$V_t = V_{t0} + \gamma \left[\sqrt{\left(2\phi_f + V_{SB}\right)} - \sqrt{2\phi_f} \right] \tag{6.14}$$

- Body Effect (Back-Gate Effect)
  - The body acts as a second gate.
  - When v_{GS} is kept constant, $v_{SB} \uparrow \Rightarrow V_t \uparrow \Rightarrow i_D \downarrow$.

6.3.2 Internal Capacitances

- Device has internal capacitances
  - C_{gs}: Gate to Source capacitance.
    - The source diffusion extends slightly under the gate. (Overlap capacitance)
  - C_{gd}: Gate to Drain capacitance.
    - The drain diffusion extends slightly under the gate. (Overlap capacitance)
  - C_{gb}: Gate to Body capacitance.
    - The gate electrode forms a parallel plate capacitor with channel.
  - C_{sb}: Source to Body capacitance.
    - Depletion capacitance of the reverse-biased *pn* junction (Body to Source).
  - C_{db}: Drain to Body capacitance.
    - Depletion capacitance of the reverse-biased *pn* junction (Body to Drain).
- Gate capacitive effect (C_{gs}, C_{gd}, C_{gb})
  - Triode
    - The gate-channel capacitance is WLC_{ox}
    - Model

$$C_{gs} = C_{gd} = \frac{1}{2} WLC_{ox} + WL_{ov}C_{ox} \tag{6.15}$$

  - Saturation
    - The gate-channel capacitance is $\frac{2}{3}WLC_{ox}$.

* Model

$$\begin{aligned} C_{gs} &= \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox} \\ C_{gd} &= WL_{ov}C_{ox} \end{aligned} \tag{6.16}$$

- Cut-off
  * The gate-body capacitance is WLC_{ox}.
  * Model

$$\begin{aligned} C_{gs} &= C_{gd} = WL_{ov}C_{ox} \\ C_{gb} &= WLC_{ox} \end{aligned} \tag{6.17}$$

- Depletion layer capacitance (C_{sb}, C_{db})
  - Junction capacitances from the bottom side and the side walls of the diffusion.
  - Source to body depletion capacitance C_{sb} (assume small signal)
    * C_{sb0}: The capacitance with zero voltage.
    * V_0: Junction built-in voltage.

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}} \tag{6.18}$$

  - Source to body depletion capacitance C_{db} (assume small signal)
    * C_{db0}: The capacitance with zero voltage.
    * V_0: Junction built-in voltage.

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{dB}}{V_0}}} \tag{6.19}$$

- Capacitance effects must be considered when the MOSFET is operated at high frequency.

6.3.3 Temperature Effect

- i_D decreases as temperature increases.
- Both V_t and k' are temperature sensitive.
  - V_t decreases by about $2mV$ for every 1 °C rise in temperature.
  - k' decreases with temperature and its effect is a dominant one.

6.3.4 Summary

- The saturation region is used for the operation of amplifier.

- The triode and cut-off regions are used for the operation of switch.

7

Bipolar Junction Transistor (BJT)

- A three-terminal device that uses the voltage of the two terminals to control the current flowing in the third terminal.
  - The basis for amplifier design.
  - The basis for switch design.
  - The basic element of high speed integrated digital and analog circuits.
- Applications
  - Discrete-circuit design.
  - Analog circuits.
    - High frequency application such as radio frequency analog circuit.
  - Digital circuits.
    - High speed digital circuit such as emitter coupled circuit (ECC).
    - Bi-CMOS (Bipolar+CMOS) circuits that combines the advantages of MOSFET and bipolar transistors.
      - MOSFET: high-input impedance and low-power.
      - Bipolar transistors: high-frequency-operation and high-current-driving capabilities.
- Circuit symbol
  - The arrowhead on the emitter implies the polarity of the emitter-base voltage.
    - NPN: $v_{BE} > 0$.
    - PNP: $v_{EB} > 0$.

7.1 Structure

7.1.1 NPN Transistor

- Figure 7.2 depicts a simplified NPN transistor.
  - Emitter (E): heavily doped n-type region.
  - Base (B): lightly doped p-type region.
  - Collector (C): heavily doped n-type region.
  - Two diodes connected in series with opposite directions.
    - EBJ: Emitter-Base junction.

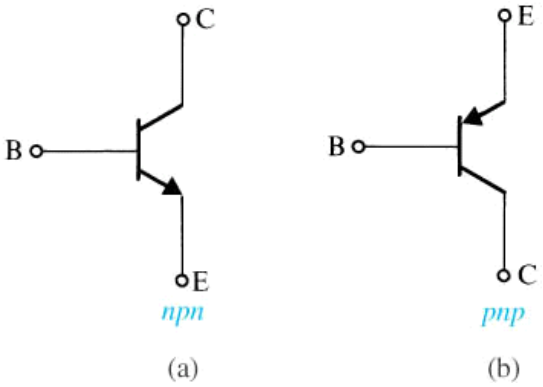


Figure 7.1: Circuit symbols of (a) NPN and (b) PNP transistors.

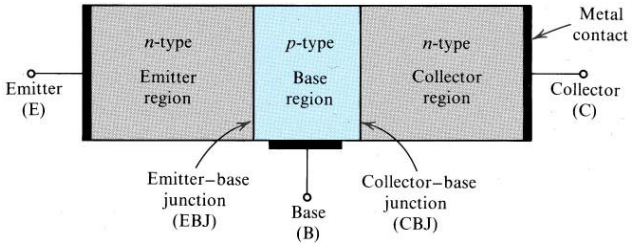


Figure 7.2: A simplified structure of the NPN transistor.

    - ∗ CBJ: Collector-Base junction.
- Figure 7.3 shows the cross-section view of an NPN transistor.
  - The NPN transistor has asymmetrical structure.
  - α and β parameters are different for forward active and reverse active modes.
- Modes of operations
  - Cutoff
    - ∗ EBJ (Reverse), CBJ (Reverse)
    - ∗ $v_{BE} < 0$, $v_{CB} > 0$.
  - Active (refer to Figure 7.7)
    - ∗ EBJ (Forward), CBJ (Reverse)
    - ∗ $v_{BE} > 0$, $v_{CB} > 0$.
  - Reverse Active
    - ∗ EBJ (Reverse), CBJ (Forward)
    - ∗ $v_{BE} < 0$, $v_{CB} < 0$.
  - Saturation
    - ∗ EBJ (Forward), CBJ (Forward)
    - ∗ $v_{BE} < 0$, $v_{CB} < 0$.

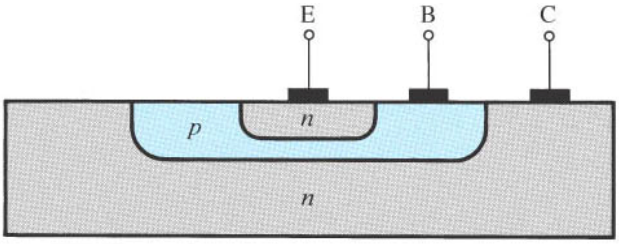


Figure 7.3: Cross-section of an NPN BJT.

- Figure 7.4 shows the voltage polarities and current flow in the NPN transistor biased in the active mode.

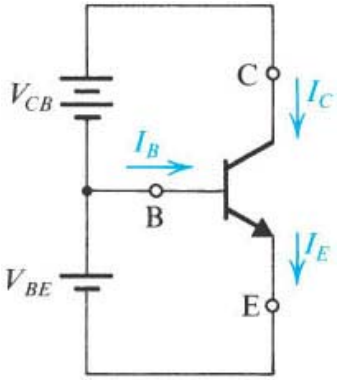


Figure 7.4: Voltage polarities and current flow in the NPN transistor biased in the active mode.

7.1.2 PNP Transistor

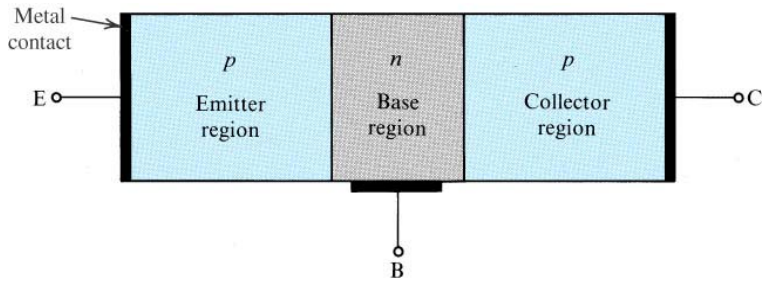


Figure 7.5: A simplified structure of the PNP transistor.

- Figure 7.5 depicts a simplified PNP transistor.
  - Emitter (E): heavily doped p-type region.

  - Base (B): lightly doped n-type region.
  - Collector (C): heavily doped p-type region.
  - Two diodes connected in series with opposite directions.
    * EBJ: Emitter-Base junction.
    * CBJ: Collector-Base junction.
- Modes of operations
  - Cutoff
    * EBJ (Reverse), CBJ (Reverse)
    * $v_{EB} < 0$, $v_{BC} < 0$.
  - Active (refer to Figure 7.7)
    * EBJ (Forward), CBJ (Reverse)
    * $v_{EB} > 0$, $v_{BC} > 0$.
  - Reverse Active
    * EBJ (Reverse), CBJ (Forward)
    * $v_{EB} < 0$, $v_{BC} < 0$.
  - Saturation
    * EBJ (Forward), CBJ (Forward)
    * $v_{EB} > 0$, $v_{CB} > 0$.
- Figure 7.6 shows the voltage polarities and current flow in the PNP transistor biased in the active mode.

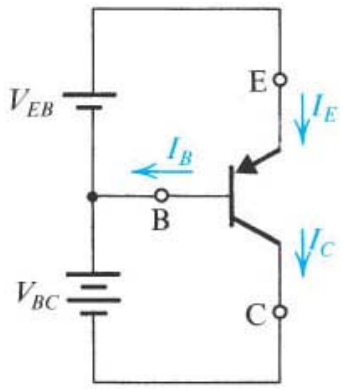


Figure 7.6: Voltage polarities and current flow in the PNP transistor biased in the active mode.

7.2 Operations of NPN Transistor

7.2.1 Active Mode

- Emitter-Base Junction

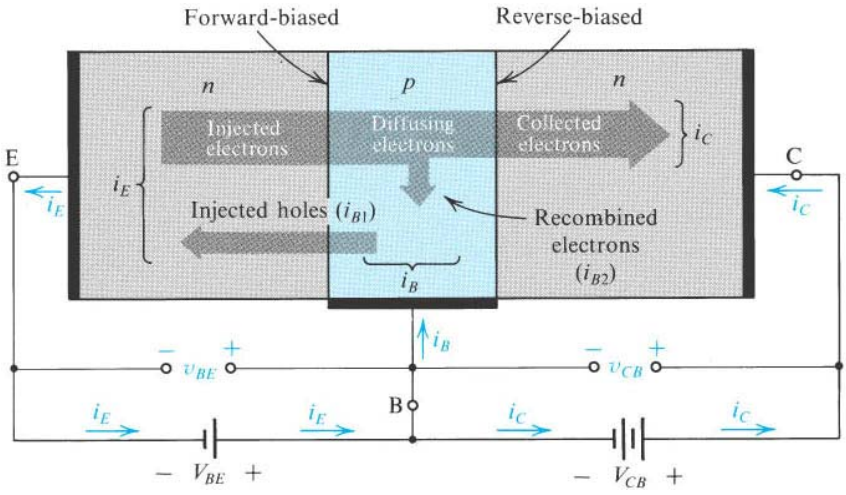


Figure 7.7: Current flow in an NPN transistor to operate in the active mode.

- Forward bias, $v_{BE} > 0$.
- Electrons in the emitter region are injected into the base causing a current i_{E1}.
- Holes in the base region are injected into the emitter region causing a current i_{E2}.
  - Generally, $i_{E1} >> i_{E2}$.

$$i_E(t) = i_{E1} + i_{E2} \tag{7.1}$$

- Base region
  - Figure 7.8 depicts the concentration of minority carriers (electrons) in the base region.
  - Tapered concentration causes the electrons to diffuse through the base region toward the collector.
    - Some of the electrons may combine with the holes causing a concave shape of the profile.
    - The recombination process is quite small due to lightly doped and thin base region.

$$n_p(0) = n_{p0} e^{v_{BE}/V_T} \tag{7.2}$$

  - Diffusion current I_n (flowing from right to the left) is proportional to the slope of the concentration profile.
    - A_E is the cross-sectional area of the base-emitter junction.
    - D_n is the electron diffusivity in the base region.
    - W is the effective width of the base.

$$I_n = A_E q D_n \frac{dn_p(x)}{dx} = -A_E q D_n \frac{n_p(0)}{W} \tag{7.3}$$

- Collector-Base Junction
  - Reverse bias, $v_{BC} > 0$.
  - The electrons near the collector side are swept into the collector region causing zero concentration at the collector side.

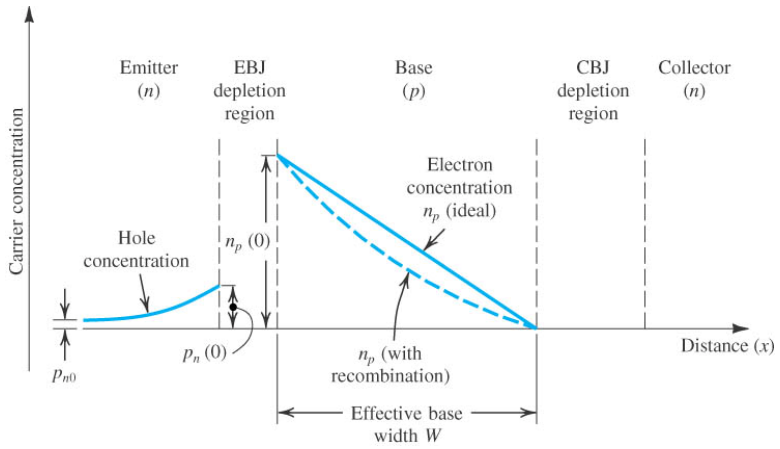


Figure 7.8: Profiles of minority carrier concentrations in the base and in the emitter of an NPN transistor.

- Collector current, i_C.
  - Most of the diffusing electrons will reach the collector region, i.e., $i_C = -I_n$.
    - Only a very small percentage of electrons are recombined with the holes in the base region.
  - As long as $v_{CB} > 0$, i_C is independent of v_{CB}.
    - The electrons that reach the collector side of the base region will be swept into the collector as collector current.

$$\begin{aligned} i_C &= -I_n \\ &= A_E q D_n \frac{n_p(0)}{W} \\ &= \frac{A_E q D_n n_{p0}}{W} e^{v_{BE}/V_T} \\ &= \frac{A_E q D_n n_i^2}{W N_A} e^{v_{BE}/V_T} \\ &= I_S e^{v_{BE}/V_T} \end{aligned} \tag{7.4}$$

  - Saturation current (also known as scale current) $I_S = (A_E q D_n n_i^2)/(W N_A)$
    - A strong function of temperature.
    - Proportional to the cross-sectional area of the base-emitter junction.
    - Inverse proportional to the base width W.
- Base current i_B

- i_B is composed of two currents.
  - The holes injected from the base region into the emitter region.

$$i_{B1} = \frac{A_E q D_p n_i^2}{N_D L_p} e^{v_{BE}/V_T} \tag{7.5}$$

  - The holes that have to be supplied by the external circuit due to the recombination.
    - τ_b is the average time for a minority electron to recombine with a majority hole.

$$i_{B2} = \frac{1}{2} \frac{A_E q W n_i^2}{\tau_b N_A} e^{v_{BE}/V_T} \tag{7.6}$$

- Formulation of i_B in terms of i_C.
  - I_S is the saturation current of i_C (refer to Eq.(7.4))
  - $\beta = 1/\left(\frac{D_p}{D_n}\frac{N_A}{N_D}\frac{W}{L_p} + \frac{1}{2}\frac{W^2}{D_n \tau_b}\right)$ is a constant (normally in the range $50 \sim 200$) for a given transistor.
  - β is mainly influenced by (1) the width of the base region, and (2) the relative dopings of the base region and the emitter region $\frac{N_A}{N_D}$.
    - To achieve high β values, the base should be thin (W small) and lightly doped, and the emitter heavily doped.

$$\begin{aligned} i_B &= i_{B1} + i_{B2} \\ &= I_S\left(\frac{D_p}{D_n}\frac{N_A}{N_D}\frac{W}{L_p} + \frac{1}{2}\frac{W^2}{D_n \tau_b}\right) e^{v_{BE}/V_T} \\ &= \left(\frac{D_p}{D_n}\frac{N_A}{N_D}\frac{W}{L_p} + \frac{1}{2}\frac{W^2}{D_n \tau_b}\right) i_C \\ &= \frac{1}{\beta} \times i_C \end{aligned} \tag{7.7}$$

- Emitter current i_E
  - From KCL, the i_E and i_C can be related as follows:

$$\begin{aligned} i_E &= i_B + i_C \\ &= \frac{1}{\beta} i_C + i_C \\ &= \frac{1+\beta}{\beta} \times i_C \\ &= \frac{1}{\alpha} \times i_C \\ &= \frac{1}{\alpha} \times I_s e^{v_{BE}/V_T} \end{aligned} \tag{7.8}$$

  - $\alpha = \beta/(1+\beta) \simeq 1$ is a constant for a given transistor.

    * Small change in α corresponds to large changes in β.
- Recapitulation
  - Configuration
    * EBJ (Forward), CBJ (Reverse)
  - Relationship between i_C, i_B, and i_E.
    * $i_C = \beta \times i_B$.
      · β (normally in the range 50∼200) is a constant for a given transistor.
    * $i_C = \alpha \times i_E$.
      · α ($\beta/(1+\beta) \precsim 1$) is a constant for a given transistor.
    * i_B, i_C, and i_E are all controlled by v_{BE}.

$$\begin{aligned} i_C &= I_S e^{v_{BE}/V_T} \\ i_B &= \frac{1}{\beta} I_S e^{v_{BE}/V_T} \\ i_E &= \frac{1}{\alpha} I_S e^{v_{BE}/V_T} \end{aligned} \tag{7.9}$$

  - Figure 7.9 depicts the large signal equivalent model of the NPN transistor.
    * In Figure 7.9 (a), i_C behaves as a voltage (v_{BE}) controlled current source.

$$i_C + i_B = i_E = \frac{1}{\alpha} i_C \tag{7.10}$$

    * In Figure 7.9 (b), i_C behaves as a current (i_E) controlled current source.

$$\begin{aligned} & i_C + i_B = i_E \\ \Rightarrow \quad & \alpha i_E + i_B = i_E \end{aligned} \tag{7.11}$$

    * The diode D_E represents the forward base-emitter junction.

7.2.2 Reverse Active Mode

- The α and β in the reverse active mode are much lower than those in the forward active mode.
  - α_R is in the range of 0.01 to 0.5.
    * In forward active mode, the collector virtually surrounds the emitter region.
      · Electrons injected into the thin base region are mostly captured by the collector.
    * In reverse active mode, the emitter virtually surrounds the collector region.
      · Electrons injected into the thin base region are partly captured by the

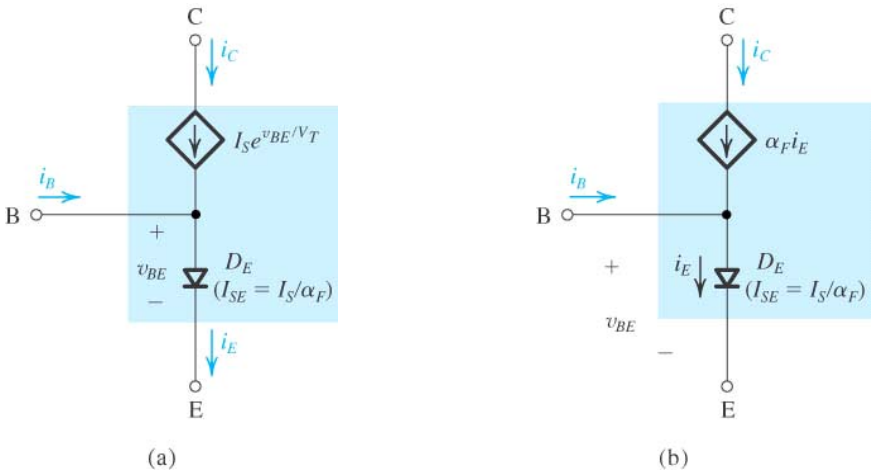


Figure 7.9: Large signal equivalent model of the NPN BJT operating in the forward active mode.

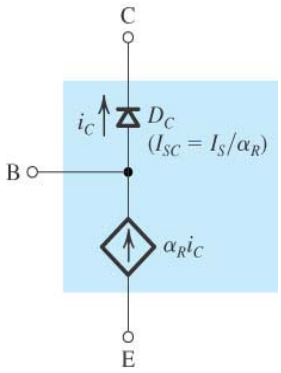


Figure 7.10: Large signal equivalent model of the NPN BJT operating in the reverse active mode.

collector.

  - β_R is in the range of 0.01 to 1.
- CBJ has a much larger area than EBJ.
  - The diode D_C denotes the forward base-collector junction.
  - The diode D_C has larger scale current (I_{SC}) than D_E does.
    - The diode D_C has lower voltage drop when forward biased.

7.2.3 Ebers-Moll (EM) Model

- A composite model that can be used to predict the operations of the BJT in all possible modes.
  - Combine Figure 7.9 (b) and Figure 7.10.
- α and β

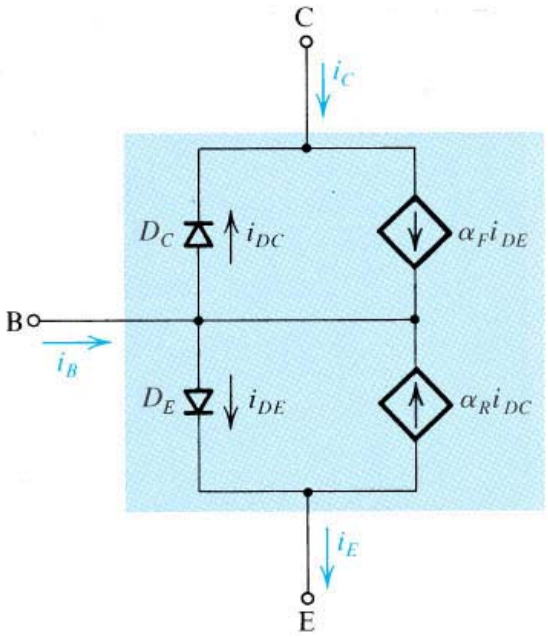


Figure 7.11: Ebers-Moll model of the NPN transistor.

  - α_F and β_F denotes the parameters in forward active mode.
  - α_R and β_R denotes the parameters in reverse active mode.
- Equivalent saturation current I_{SE} and I_{SC}
  - From Figure 7.9 (b) and Figure 7.10, I_{SE} and I_{SC} are the equivalent saturation currents at the EBJ and CBJ, respectively.

$$\begin{aligned} I_{SE} &= \frac{1}{\alpha_F} I_S \\ I_{SC} &= \frac{1}{\alpha_R} I_S \\ \Rightarrow \quad \alpha_F I_{SE} &= \alpha_R I_{SC} = I_S \end{aligned} \tag{7.12}$$

- i_C, i_B, and i_E in the EM model

$$\begin{aligned} i_E &= i_{DE} - \alpha_R i_{DC} \\ i_C &= -i_{DC} + \alpha_F i_{DE} \\ i_B &= (1-\alpha_F) i_{DE} + (1-\alpha_R) i_{DC} \end{aligned} \tag{7.13}$$

  - $i_{DE} = I_{SE}\left(e^{v_{BE}/V_T} - 1\right)$.
  - $i_{DC} = I_{SC}\left(e^{v_{BC}/V_T} - 1\right)$.

- By Eq. (7.12),

$$\begin{aligned} i_E &= \frac{I_S}{\alpha_F}(e^{v_{BE}/V_T}-1) - I_S(e^{v_{BC}/V_T}-1) \\ i_C &= I_S(e^{v_{BE}/V_T}-1) - \frac{I_S}{\alpha_R}(e^{v_{BC}/V_T}-1) \\ i_B &= \frac{I_S}{\beta_F}(e^{v_{BE}/V_T}-1) + \frac{I_S}{\beta_R}(e^{v_{BC}/V_T}-1) \end{aligned} \tag{7.14}$$

  - $\beta_F = \alpha_F/(1-\alpha_F)$.
  - $\beta_R = \alpha_R/(1-\alpha_R)$.

7.2.4 Saturation Mode

- CBJ is in forward bias, i.e., $v_{BC} > 0.4V$.
  - CBJ has larger junction area than EBJ.
    - CBJ has larger saturation current I_S and lower cut-in voltage than EBJ.
    - In forward bias,
      - The voltage drop across CBJ is $0.4V$.
      - The voltage drop across EBJ is $0.7V$.
  - As v_{BC} is increased, i_C will be decreased and eventually reach zero.

$$i_C \simeq I_S e^{v_{BE}/V_T} - \frac{I_S}{\alpha_R} e^{v_{BC}/V_T} \tag{7.15}$$

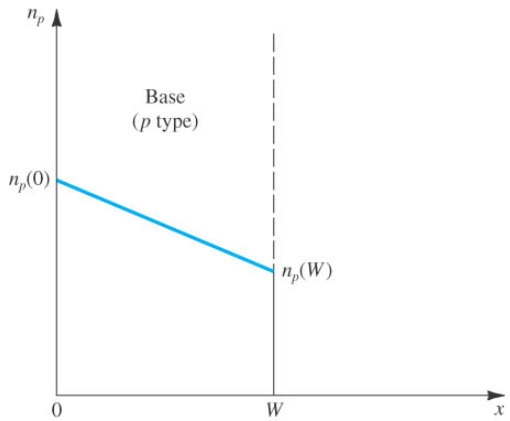


Figure 7.12: Concentration profile of the minority carriers in the base region of an NPN transistor.

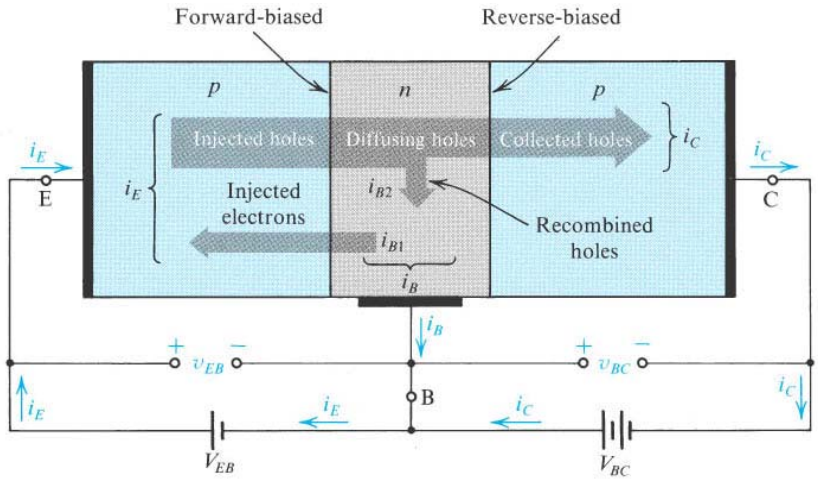


Figure 7.13: Current flow in a PNP transistor biased to operate in the active mode.

7.3 Operations of PNP Transistor

7.3.1 Active Mode

- Current in a PNP transistor is mainly conducted by holes.
- Emitter-Base Junction
  - Forward bias, $v_{EB} > 0$.
  - Holes in the emitter region are injected into the base causing a current i_{E1}.
  - Electrons in the base region are injected into the emitter region causing a current i_{E2}.
    - Generally, $i_{E1} >> i_{E2}$.

$$i_E(t) = i_{E1} + i_{E2} \tag{7.16}$$

- Base region
  - Tapered concentration causes the holes to diffuse through the base region toward the collector.
    - Some of the holes may combine with the electrons.
    - The recombination process is quite small due to lightly doped and thin base region.
- Collector-Base Junction
  - Reverse bias, $v_{BC} > 0$.
  - The holes near the collector side are swept into the collector region causing zero concentration at the collector side.
- Collector current, i_C.
  - Most of the diffusing holes will reach collector region.
    - Only a very small percentage of holes are recombined with the electrons

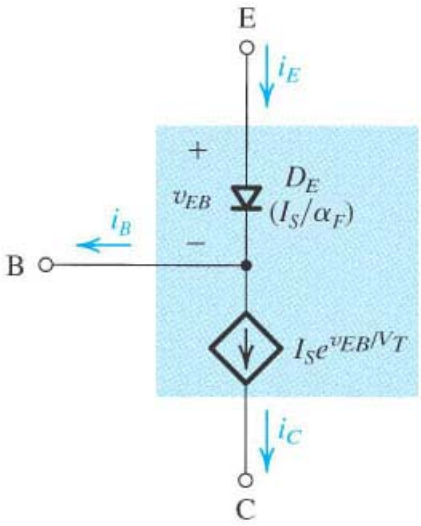


Figure 7.14: Large signal equivalent model of the PNP BJT operating in the forward active mode.

in the base region.

- As long as $v_{BC} > 0$, i_C is independent of v_{BC}.
  - The holes that reach the collector side of the base region will be swept into the collector as collector current.

- Base current i_B
  - i_B is composed of two currents.
    - The electrons injected from the base region into the emitter region.
    - The electrons that have to be supplied by the external circuit due to the recombination.

- Emitter current i_E
  - From KCL, the i_E and i_C can be related as follows:

$$\begin{aligned} i_E &= i_B + i_C \\ &= \frac{1}{\beta} i_C + i_C \\ &= \frac{1+\beta}{\beta} \times i_C \\ &= \frac{1}{\alpha} \times i_C \\ &= \frac{1}{\alpha} \times I_s e^{v_{EB}/V_T} \end{aligned} \tag{7.17}$$

    - $\alpha = \beta/(1+\beta) \simeq 1$ is a constant for a given transistor.
    - Small change in α corresponds to large changes in β.

- Figure 7.14 depicts the large signal equivalent model of the PNP transistor.

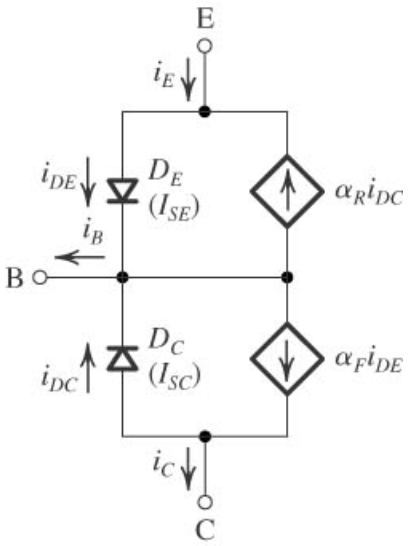


Figure 7.15: Ebers-Moll model of the PNP transistor.

- Figure 7.15 shows the EM model of the NPN transistor.

7.3.2 Reverse Active Mode

- Similar to NPN transistor.

7.3.3 Saturation Mode

- Similar to NPN transistor.

7.3.4 Summary of the i_C, i_B, i_E Relationships in Active Mode

- NPN transistor

$$\begin{aligned} i_c &= I_s e^{v_{BE}/V_T} \\ i_B &= \frac{I_s}{\beta} e^{v_{BE}/V_T} \\ i_E &= \frac{I_s}{\alpha} e^{v_{BE}/V_T} \end{aligned} \tag{7.18}$$

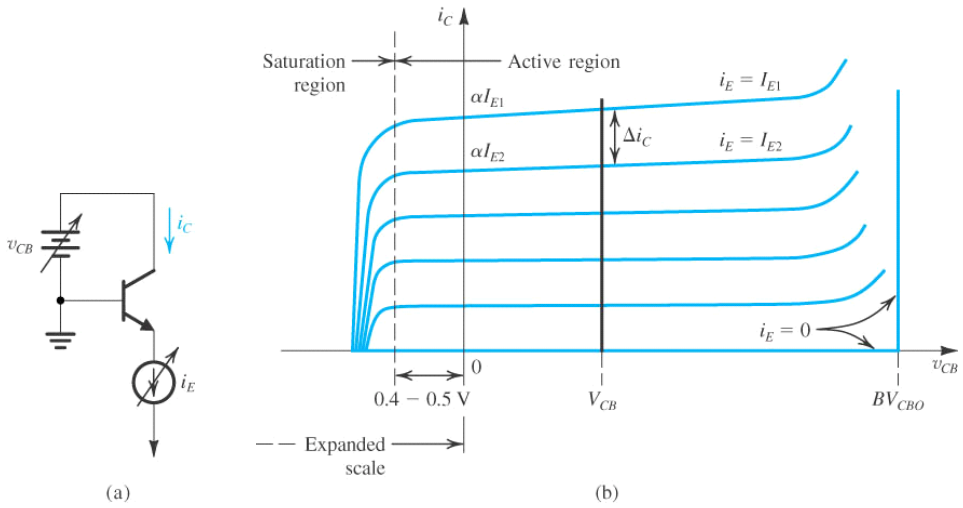


Figure 7.16: The $i_C - v_{CB}$ characteristics of an NPN transistor.

$$\begin{aligned} i_C &= \alpha i_E \\ i_C &= \beta i_B \\ i_B &= (1-\alpha) i_E = \frac{i_E}{1+\beta} \\ i_E &= (1+\beta) i_B \end{aligned} \tag{7.19}$$

- PNP transistor.
  - The v_{BE} in Eq. (7.18) is replaced by v_{EB}.

7.4 The $i - v$ Characteristics of NPN Transistor

7.4.1 Common Base ($i_C - v_{CB}$)

- Figure 7.16 depicts the i_C versus v_{CB} for various i_E, which is also known as the common-base characteristics.
  - Input port: emitter and base terminals.
    - Input current i_E.
  - Output port: collector and base terminals.
    - Output current i_C.
  - The base terminal serves as a common terminal to both input port and output port.
- Active Region ($v_{CB} \geq -0.4V$)
  - i_C depends slightly on v_{CB} and shows a small positive slope.

  - i_C shows a rapid increase, known as breakdown phenomenon, for a relatively large value of v_{CB}.
  - Each $i_C - v_{CB}$ curve intersects the vertical axis at a current level equal to αI_E.
    * Total or large-signal α (common-base current gain)
      · $\alpha = i_C/i_E$, where i_C and i_E denote the total collector and emitter currents, respectively.
    * Incremental or small-signal α
      · $\alpha = \Delta i_C/\Delta i_E$.
    * Usually, the values of incremental and total α differs slightly.
- Saturation Region ($v_{CB} < -0.4V$)
  - CBJ is forward biased.
  - The EM model can be used to determine the v_{CB} at which i_C is zero.

7.4.2 Common Emitter ($i_C - v_{CE}$)

- Figure 7.17 depicts the i_C versus v_{CE} for various v_{BE}, which is also known as the common-emitter characteristics.
  - Input port: base and emitter terminals.
    * Input current i_B.
  - Output port: collector and emitter terminals.
    * Output current i_C.
  - The emitter terminal serves as a common terminal to both input port and output port.
- Active Region ($v_{CB} \geq -0.4V$)
  - i_C increases as the v_{CE} is increased, which is known as Early Effect.
    * At a given v_{BE}, increasing v_{CE} increases the width of the depletion region of the CBJ.
    * The effective base width W is decreased.
    * As shown in Eq. (7.4), I_S is inversely proportional to the base width W.
  - When extrapolated, the characteristics line meet at point on the negative v_{CE} (normally in the range of 50V to 100V), $-V_A$.
    * V_A is a constant for a given transistor.
- Large signal equivalent circuit model in active mode.
  - The linear dependency of i_C on v_{CE} can be formulized as follows:

$$i_C = I_S e^{v_{BE}/V_T}(1 + \frac{v_{CE}}{V_A}) = I_C(1 + \frac{v_{CE}}{V_A}) \tag{7.20}$$

  - The output resistance looking into the collector-emitter terminals.
    * Inversely proportional to the collector current I_C without considering Early effect.

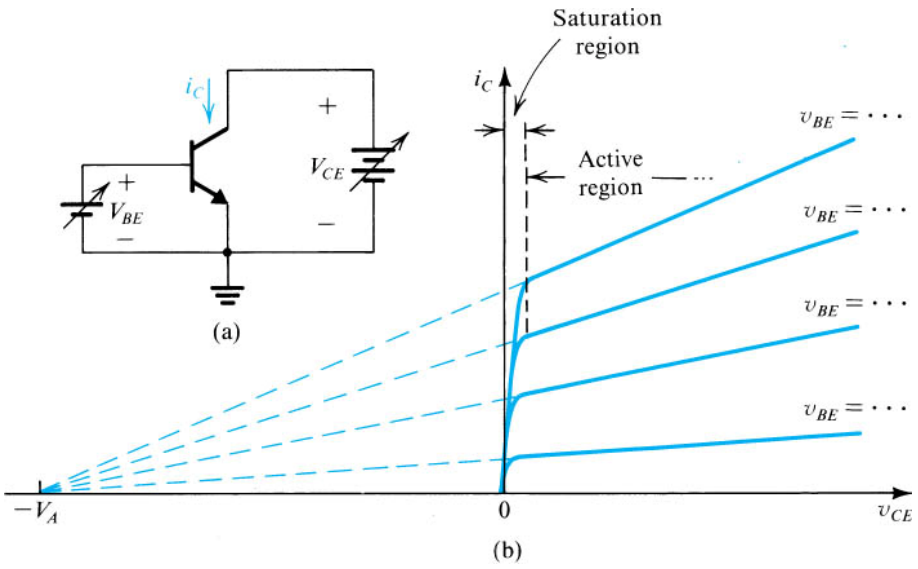


Figure 7.17: The $i_C - v_{CE}$ characteristics of the BJT.

* Controlled by v_{BE}.

$$\Delta i_C = I_S e^{v_{BE}/V_T}\left(\frac{\Delta v_{CE}}{V_A}\right) \tag{7.21}$$
$$\Rightarrow \quad r_o = \frac{\Delta v_{CE}}{\Delta i_C} = \frac{V_A}{I_C}$$

– Figure 7.18 depicts the large signal equivalent circuit model of an NPN BJT in the active mode and with the common emitter configuration.
  * Figure 7.18 (a), voltage v_{BE} controls the collector current source.
  * Figure 7.18 (b), the base current i_B controls the collector current source $\beta \times i_B$.
– Large signal or DC β
  * The ratio of total current in the collector to the total current in the base, which represents the ideal current gain (where r_o is not present) of the common-emitter configuration.

$$\beta_{dc} = \frac{i_C}{i_B}\Big|_{v_{CE}=\text{constant}} \tag{7.22}$$

  * β is also known as the common-emitter current gain.
– Incremental or AC β
  * Short-circuit common-emitter current gain.
  * AC β and DC β differ approximately 10% to 20%.

$$\beta_{ac} = \frac{\Delta i_C}{\Delta i_B}\Big|_{v_{CE}=\text{constant}} \tag{7.23}$$

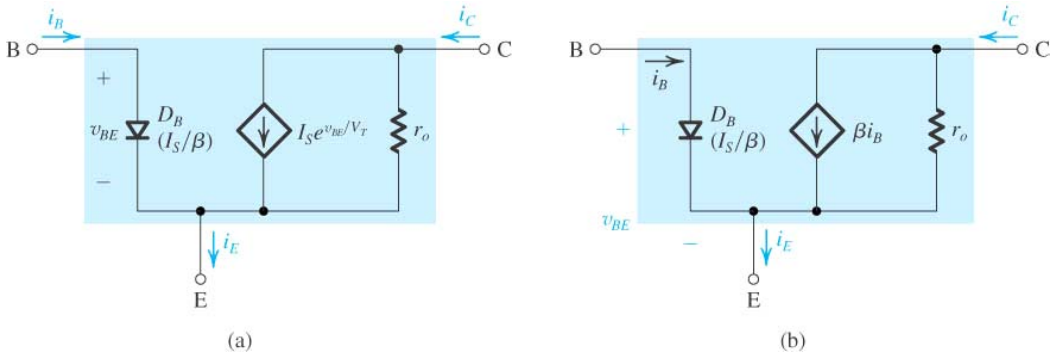


Figure 7.18: Large signal equivalent circuit model of an NPN BJT operating in the active mode and with common-emitter configuration.

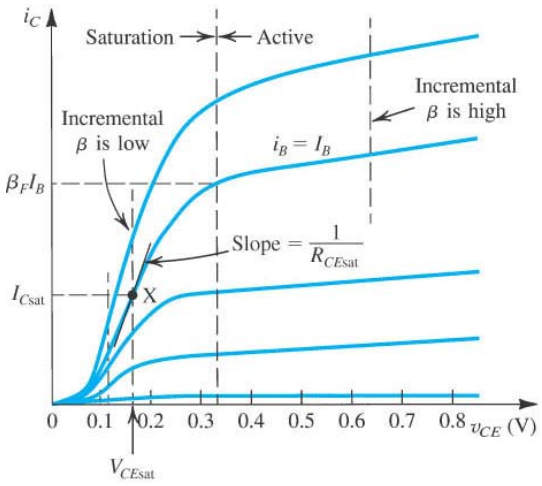


Figure 7.19: An expanded view of the common-emitter characteristic in the saturation region.

- Saturation Region ($v_{CB} < -0.4V$)
  - Figure 7.19 depicts an expanded view of the common-emitter characteristic in the saturation region.
  - Analytical expressions of $i_C - v_{CE}$ using EM model.
    * $v_{BE} = v_{CE} + v_{CB}$.

$$\begin{aligned} i_C &\simeq I_S(e^{v_{BE}/V_T}) - \frac{I_S}{\alpha_R}(e^{v_{BC}/V_T}) \\ I_B &\simeq \frac{I_S}{\beta_F}(e^{v_{BE}/V_T}) + \frac{I_S}{\beta_R}(e^{v_{BC}/V_T}) \end{aligned} \tag{7.24}$$

$$i_C \simeq (\beta_F I_B)\left(\frac{e^{v_{CE}/V_T} - \frac{1}{\alpha_R}}{e^{v_{CE}/V_T} - \frac{\beta_F}{\beta_R}}\right) \tag{7.25}$$

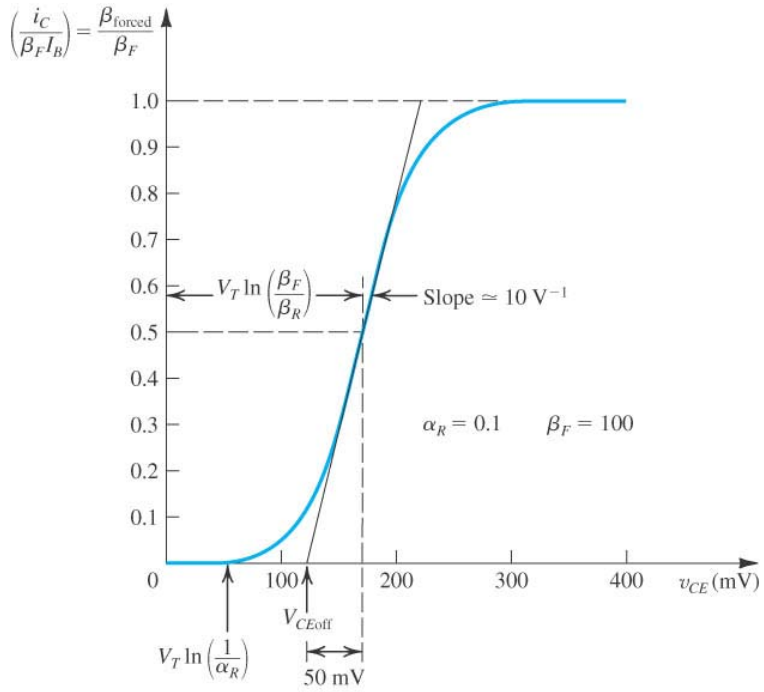


Figure 7.20: Plot of normalized i_C versus v_{CE} for an NPN transistor with $\beta_F = 100$ and $\alpha_R = 0.1$.

- Large signal equivalent circuit model in saturation mode.
  - The saturation transistor exhibits a low collector-to-emitter resistance R_{CEsat}.

$$R_{CEsat} = \frac{\partial v_{CE}}{\partial i_C}|_{i_B=I_B, i_C=I_C} \simeq 1/10\beta_F I_B \tag{7.26}$$

  - At the collector side, the transistor is modeled as a resistance $R_{CE_{sat}}$ in series with a battery v_{CEoff} as shown in Figure 7.21 (c).
    - V_{CEoff} is typically around $0.1V$.
    - V_{CEsat} is typically around $0.1 \sim 0.3V$.

$$V_{CEsat} = V_{CEoff} + I_{Csat} R_{CEsat} \tag{7.27}$$

  - For many applications, the even simpler model shown in Figure 7.21 is used.

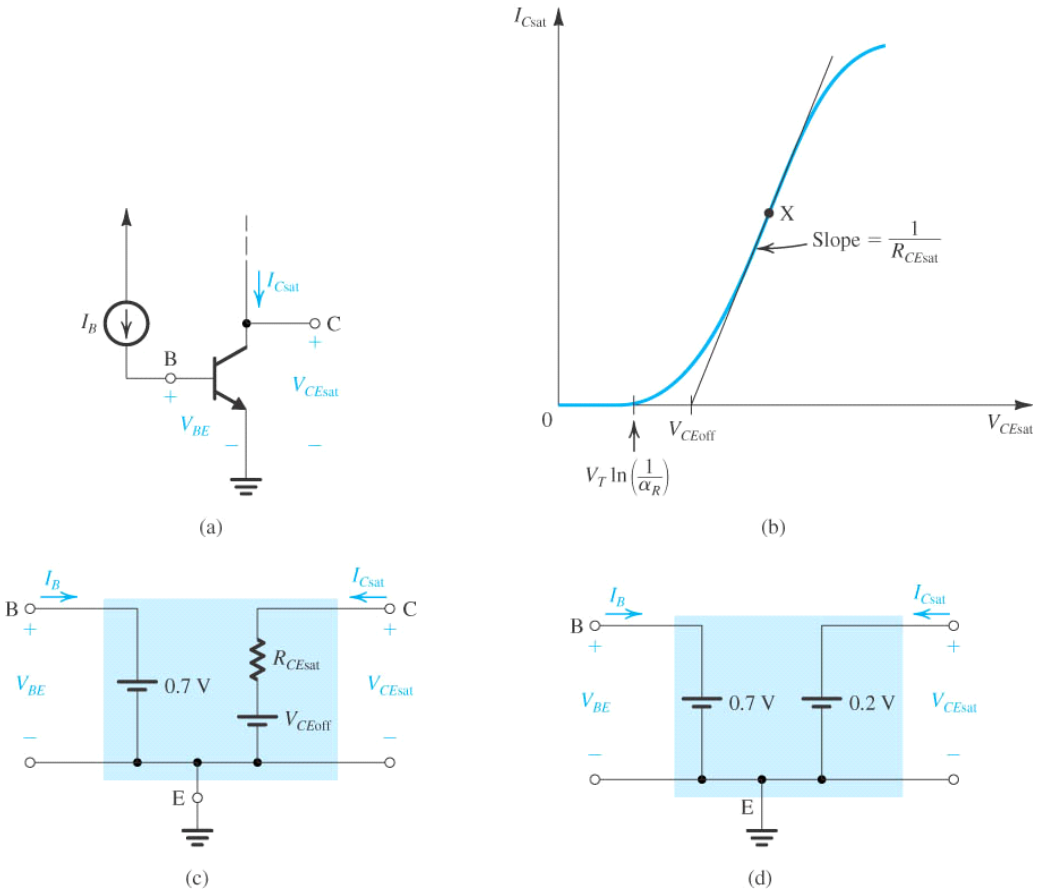


Figure 7.21: Equivalent circuit representation of the saturated transistor.