Baskent University, Faculty of Engineering
BME 222 – Electronics (Spring Semester 2004/2005)
Midterm – April 9, 2005

Student Name____________________________________

Faculty No: ____________________________________

1. Signals applied to the circuit of Fig. 1 are shown. Define and plot the output signal V_0, assuming ideal diodes.

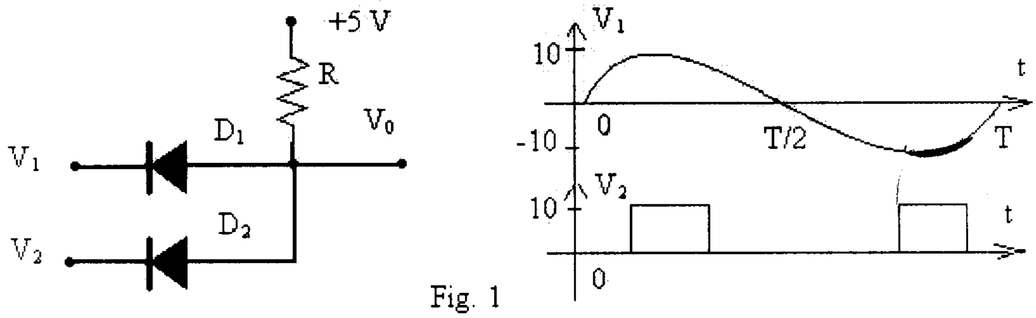


Fig. 1

2. Find the values of **I** and **V** for the circuit of Fig.2 assuming that the diodes are ideal.

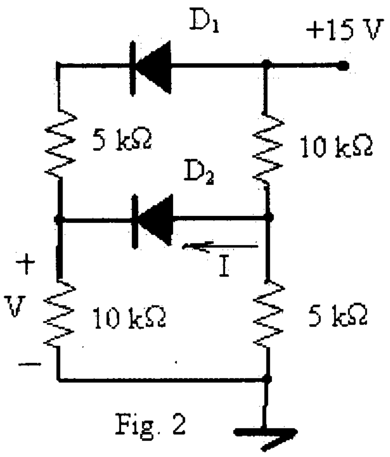


Fig. 2

3. The circuit shown in Fig.3 has a **20 V** peak sinusoidal input signal. Determine V_{C1}, V_{C2}, V_{C3} and V_{C4} for the circuit. Assume that the diodes are ideal.

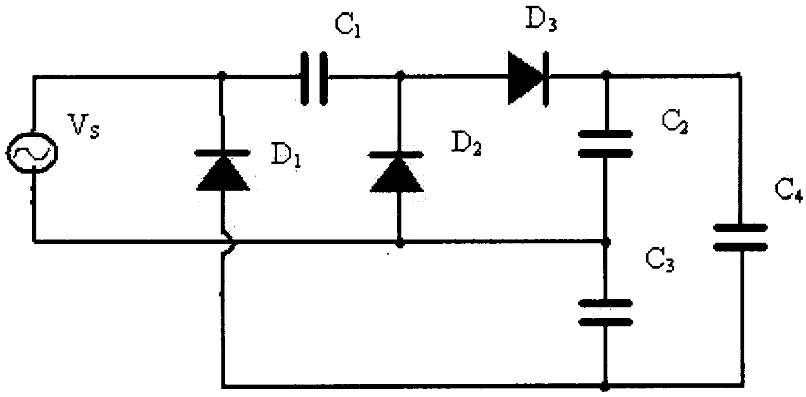


Fig. 3

4. Determine the range of V_i that will maintain the Zener diode of Fig. 4 in the "ON" state. (**V_Z = 10 V**, **I_{ZM} = 20 mA**).

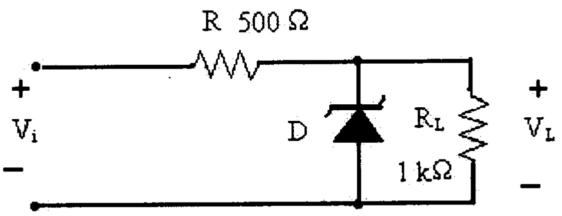
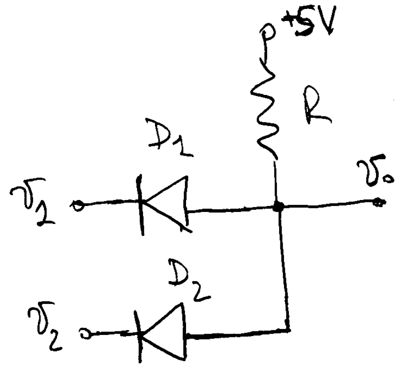


Fig.4

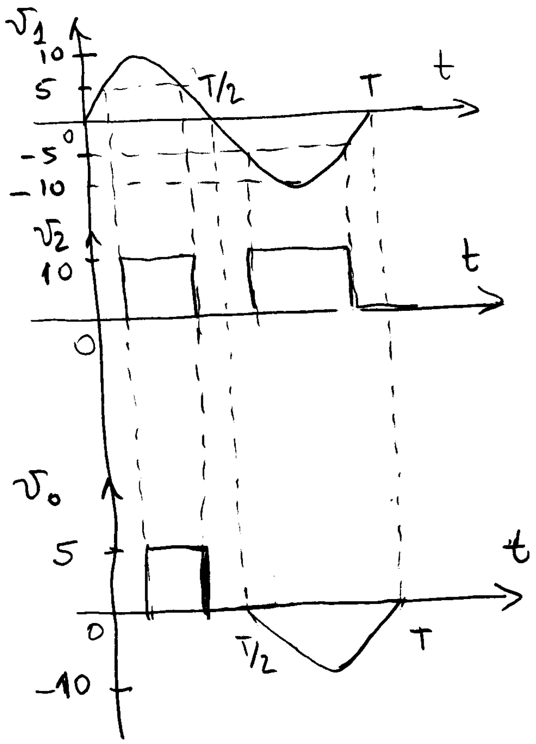
5. Calculate the voltage gain (**$A_V = V_o/V_i$**) for the common base network, if ac input resistance **R_i = 50 Ω**, ac output resistance **R_o = 500 kΩ** and load resistance **R_L = 2 kΩ**. Assume, that α = **1**.

20 points (each 4 points).

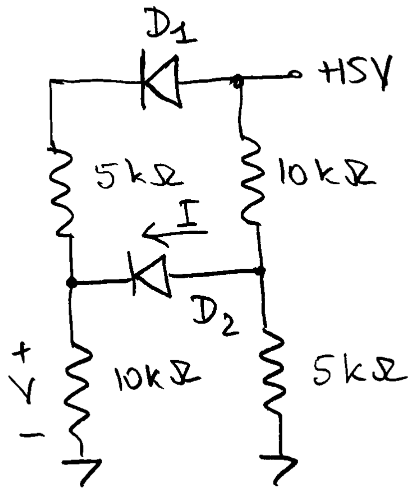
Good Luck!



1 Signals applied to the circuit of Fig. 1 are shown. Define and plot the output signal, assuming ideal diodes.



Solution:

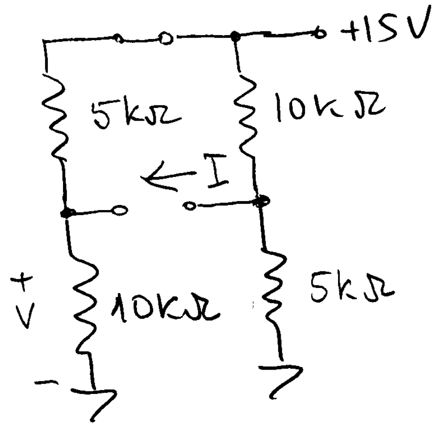


2. Find the values of I and V for the circuit of Fig. 2 assuming that the diodes are ideal.

Solution

Voltage source of +15V opens D_1 and due to the current in voltage divider stabilize V = +10 V.

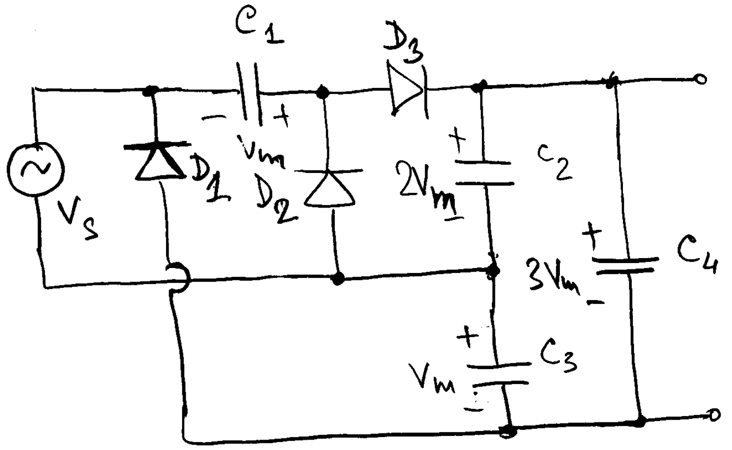
From the other side there is voltage 5V across resistor of 5 kΩ. The D_2 is in "OFF" state, then equivalent circuit is of form shown, and current I = 0 mA



Answers:

V = 10 V

I = 0 A



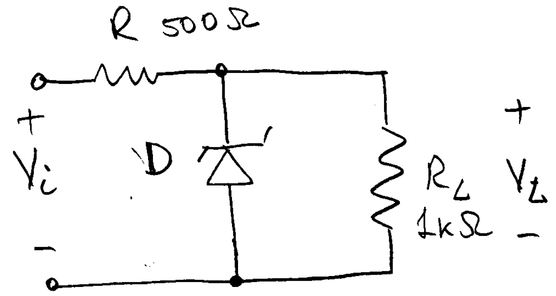
3. The circuit shown in Fig. 3 has a 20 V peak input signal. Determine V_{C1}, V_{C2}, V_{C3} and V_{C4} for the circuit. Assume that the diodes are ideal.

Solution

a). When acts negative half-wave of the input signal, capacitors C_1 and C_3 charges up to $V_m = 20$ V through D_2 and D_1 respeetively with polarity shown.

b). When acts positive half-wave of the input signal, C_2 charges through D_3 up to $2V_m = 40$ V.

c). Because C_2 and C_3 are in series and this branch is in parallel to C_4, total output voltage is $V_m + 2V_m = 3V_m = 3 \cdot 20 = 60$ V



4. Determine the range of V_i that will maintain the Zener diode of Fig. 4. in the "ON" state.
($V_Z = 10\,V$, $I_{ZM} = 20\,mA$)

Solution

$$V_{i\,min} = \frac{R_L + R}{R_L} V_Z = \frac{(1+0.5)\cancel{10^3}}{1 \cdot \cancel{10^3}} \cdot 10 = 15\ V$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{10}{1 \cdot 10^3} = 10\,mA$$

$$I_{R\,max} = I_{ZM} + I_L = 20 + 10 = 30\ mA$$

$$V_{i\,max} = I_{R\,max} \cdot R + V_Z = 30 \cdot 0.5 \cdot 10^{-3} \cdot 10^3 + 10 =$$

$$= 15 + 10 = 25\ V$$

5. Calculate the voltage gain ($A_v = V_o / V_i$) for the common base network, if $R_i = 50\,\Omega$, $R_o = 500 k\Omega$ and $R_L = 2\,k\Omega$. Assume that $\alpha = 1$.

Solution

1. Input current is

$$I_i = \frac{V_i}{R_i} = \frac{V_i}{50} \text{ A}$$

2. Assuming $\alpha = 1$, then $I_{out} = I_{input}$ and

$$V_o = I_o \cdot R_L = I_i R_o = \frac{V_i}{50} 2 \cdot 10^3$$

$$= 40 V_i \text{ V}$$

3. Voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{40 V_i}{V_i} = 40$$