Başkent University
Department of Electrical and Electronics Engineering
EEM 214 Electronics I
Experiment 9

COMMON-SOURCE JFET AMPLIFIER

Aim:

1. To evaluate the common-source amplifier using the small signal equivalent model.
2. To learn what effects the voltage gain.

Theory:

A self-biased n-channel JFET with an AC source capacitively coupled to the gate is shown in Figure 1-a.The resistor, RG, serves for two purposes: it keeps the gate at approximately 0 V dc (because IGSS is extremely small), and its large value (usually several megohms) prevents loading of the ac signal source. The bias voltage is created by the drop across RS. The bypass capacitor, C2, keeps the source of the FET effectively at ac ground.

The signal voltage causes the gate-to-source voltage to swing above and below its Q-point value, causing a swing in drain current. As the drain current increases, the voltage drop across RD also increases, causing the drain voltage to decrease. The drain current swings above and below its Q-point value in-phase with the gate-to-source voltage. The drain-to-source voltage swings above and below its Q-point value 180° out-of-phase with the gate-to-source voltage, as illustrated Figure 1-b.

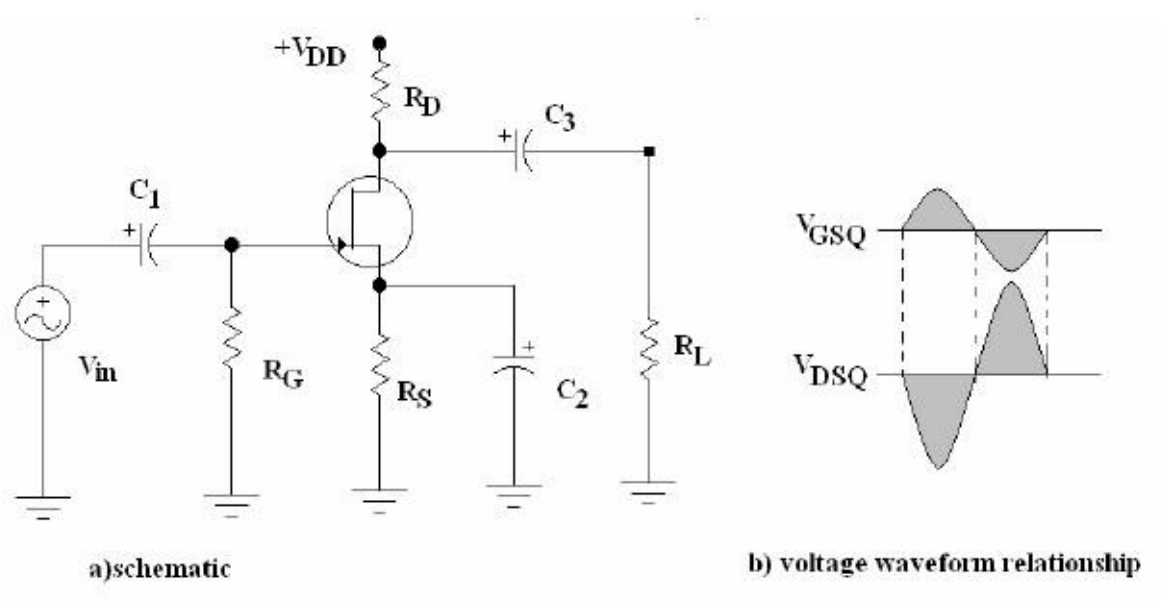
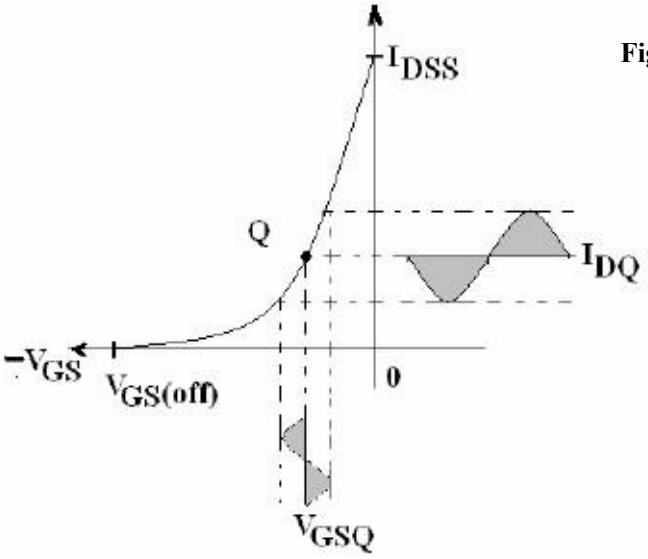


Figure 1

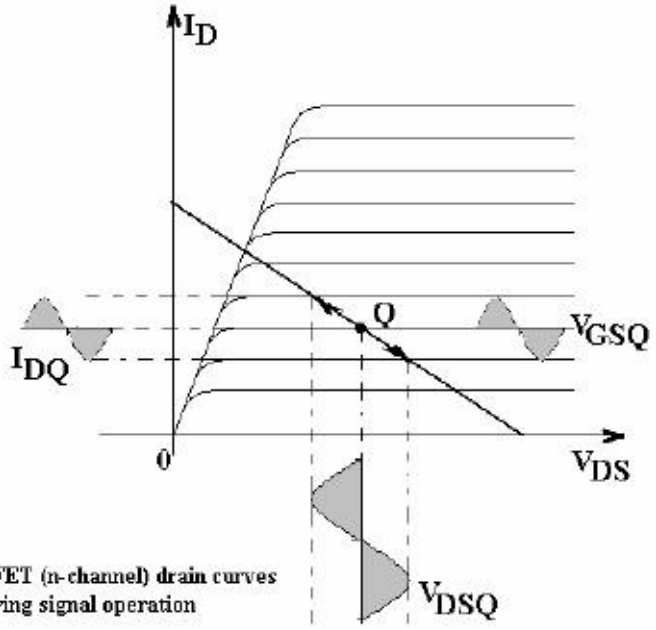
The operation just described for an n-channel JFET can be illustrated graphically on both the transfer characteristic curve and the drain characteristic curve in Figure 2. Figure 2-a shows how a sinusoidal variation, Vgs, produces a corresponding variation in Id. As Vgs swings from the Q point to a more negative value, Id decreases from its Q-point value. As Vgs swings to a less negative value, Id increases. Figure 2-b shows a view of the same operation using the drain curves. The signal at the gate drives the drain current equally above and below the Q

point on the load line, as indicated by the arrows. Lines projected from the peaks of the gate voltage across to the ID axis and down to the VDS axis indicate the peak-to-peak variations of the drain current and drain-to-source voltage, as shown.



a) JFET (n-channel) transfer characteristic curve showing signal operation

Figure 2



b) JFET (n-channel) drain curves showing signal operation

Small signal model of JFET is identical to that of the MOSFET in Figure 3. Here, g_m is given by

$$g_m = 1 - \frac{2 I_{DSS} V_{GS}}{|Vp| Vp}$$

or alternatively by

$$g_m = \frac{2 I_{DSS}}{|Vp|} \sqrt{\frac{I_D}{I_{DSS}}}$$

where V_{GS} and I_D are the DC bias quantities, and

$$r_O = \frac{|V_A|}{I_D} \quad \text{and} \quad g_{mo} = -2 I_{DSS} / Vp$$

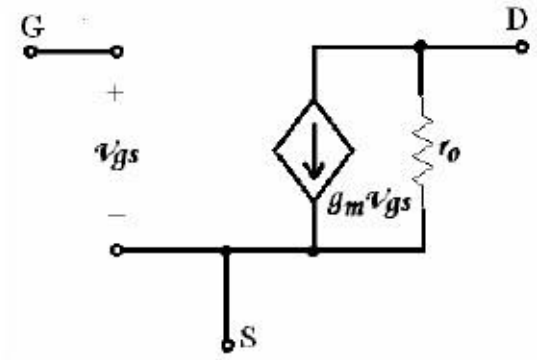


Figure 3

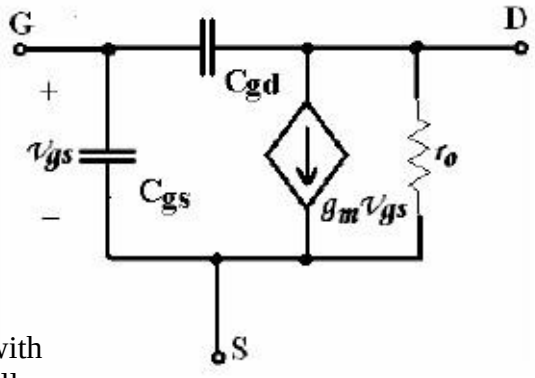


Figure 4

At high frequencies, the equivalent circuit of Figure 4 applies with Cgs and Cgd being both depletion capacitances. Typically, Cgs=1..3 pF, Cgd=0.1..0.5 pF and fT=20..100 MHz; and also there is a knowledge about the following:

$A_V = g_m (R_D // R_L)$ ....(R_s bypass)
$A_V = g_m R_d / (1 + g_m R_s)$, $R_d = (R_D // R_L)$ .....(normally)
$I_D = 2 I_{DSS} [(R s g_{mo}+1) - (2 R s g_{mo}+1)^{1/2}] / (R s g_{mo})^2$

For the n-channel JFET current-voltage characteristics described as follows:

Cutoff : VGS≤Vp, iD=0
Triode region : Vp≤VGS≤0, VDS≤VGS-Vp

$$i_D = I_{DSS} \left(2 \left(1 - \frac{V_{GS}}{V_p} \right) \left(\frac{V_{DS}}{-V_p} \right) - \left(\frac{V_{DS}}{V_p} \right)^2 \right)$$

Saturation reg.: Vp≤VGS≤0, VDS≥VGS-Vp
(pinch-off)

$$iD = IDSS1 - \left(\frac{VGS}{Vp} 2 \right) (1 + \lambda VDS)$$

λ is the inverse of the Early voltage; λ=1/VA . VA and λ are positive for n-channel devices.

Preliminary Work:

A. Find the values of ID, VGS and VDS and find gm in the circuit of Figure 7 then fill the Table 1 in the report to compare the measured ones.

B. In questions 2 to 5, let the n-channel JFET have Vp= -4V and IDSS=10mA, and unless otherwise specified assume that in pinch-off (saturation) the output resistance is infinite.

1. For VGS= -2V, find the minimum VDS for the device to operate in pinch-off. Calculate iD for VGS= -2V and VDS= 3V.

2. For small VDS, calculate the value of rDS at VGS= 0V and at VGS= -3V.

3. If VA= 100V, find the JFET output resistance rO when operating in pinch-off at a current of 1 mA, 2.5 mA and 10 mA.

C.

1. The JFET in the circuit of Figure 5 has Vp= -3V, IDSS= 9 mA, and λ=0. Find the values of all resistors so that VG= 5V, ID= 4 mA, and VD= 11V. Design for 0.05 mA in the voltage divider.

2. For the JFET circuit designed in question 6, let an input signal vi be capacitively coupled to the gate, a large bypass capacitor be connected between the source and ground, and the output signal vO be taken from the

drain through a large coupling capacitor. The resulting common-source amplifier is shown in Figure 6. Calculate gm and rO (assuming VA= 100V). Also find Ri,AV=vO/vi, and RO.

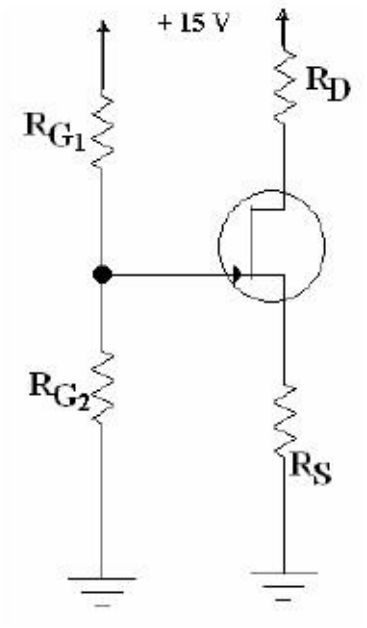


Figure 5

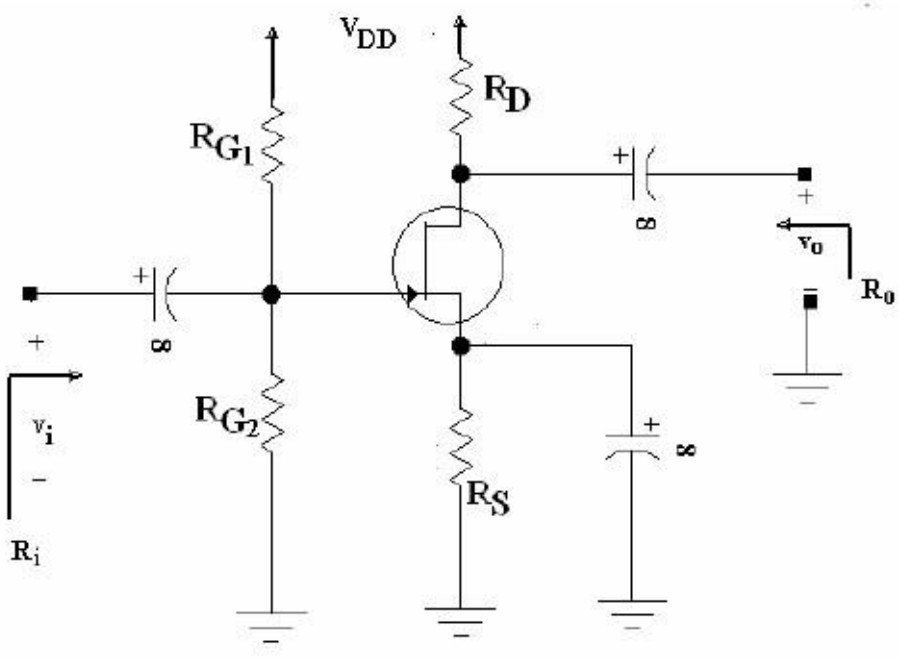


Figure 6

Procedure:

1. Construct the circuit in Figure 7:

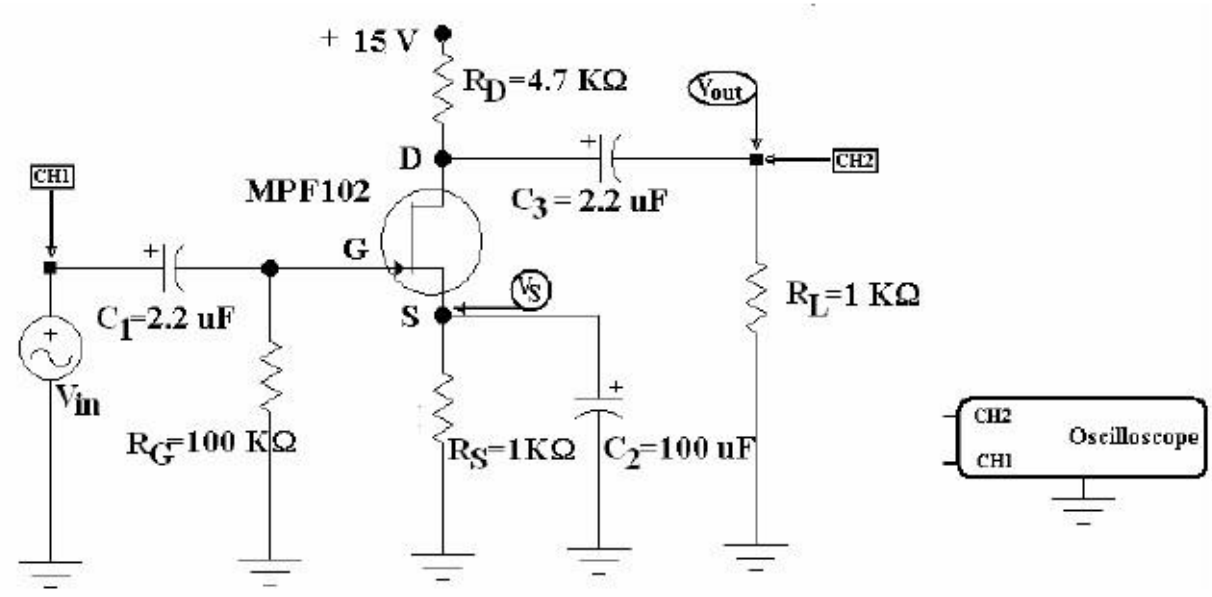


Figure 7

2. Measure the values of ID, VGS and VDS and find gm then fill the Table 1 in report part with your calculated values and compare the results.

3. With oscillator, obtain a 5 KHz signal with 0.5 Vpp and connect to the circuit as Vin, observe the Vout signal and find the voltage gain.

4. Measure the AC voltage at source point of FET as VS and write some comments on this occurence.

5. Reduce the RL and find the voltage gain.

6. Reduce the capacitor and find the voltage gain. (!Never ask “which capacitor?”!)

7. Draw all graphs for Vin and Vout, indicate the phase differences if they exist.

Equipment List:

- MPF102 FET transistor or equivalent
- DC power supply (15 V)
- Capacitors : 2*2.2 µF, 1*100 µF
- Resistors: 2*1 kΩ, 1*4.7 KΩ, 1*100 KΩ
- Oscilloscope

References:

Microelectronic Circuits, Fourth Edition, Sedra&Smith, FET Small Signal Analysis

Electronic Devices, Third Edition, Floyd, JFET Amplifers

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REPORT:

2.

TABLE 1

parameter	measured	calculated
I_D		
V_{GS}		
V_{DS}		
g_m		

3.

A_V=

4.

.....
.....
.....
.....

5.

A_V= ***(reduced R_L)***

6.

A_V= ***(reduced C_{bypass})***

Drawings for 3, 5, 6: (Draw in different colors for Vin and Vout)

Student ID # :
Name: