Başkent University
Department of Electrical and Electronics Engineering
EEM 311 Electronics II
Experiment 2

TWO STAGE AMPLIFIER CIRCUIT

Aim:

The aim the experiment is to investigate the two stage amplifier circuit.

Theory :

In most situations single transistor amplifiers cannot meet all the given specifications. Combination of a voltage gain, input resistance and output resistance cannot be met simultaneously

Multistage amplifiers are made up of single transistor amplifiers connected in cascade. The first stage usually provides a high input impedance to minimize loading the source (transducer). The middle stages usually account for most of the desired voltage gain. The final state provides a low output impedance to prevent loss of signal (gain), and to be able to handle the amount of current required by the load. In analyzing multistage amplifiers, the loading effect of the next stage must be considered since the input impedance of the next stage acts as the load for the current stage. Therefore the ac analysis of a multistage amplifier is usually done starting with the final stage. The individual stages are usually coupled by either capacitor or direct coupling. Capacitor coupling is most often used when the signals being amplified are ac signals. In capacitor coupling the stages are separated by a capacitor, which blocks the dc voltages between each stage. This dc blocking prevents the bias point of each stage from being upset.

The JFET CS - BJT CE cascade two-stage amplifier in Fig.1 is a good multistage configuration because the CS and CE amplifiers together provide some very desirable characteristics. JFET CS amplifier has a gain usually less than 10. Because of the high input impedance and low noise, JFET is usually used as the first stage in a multi-stage amplifier to pick up weak input signals. The BJT CE amplifier makes up the second stage and has the characteristics of high input impedance, low output impedance and high voltage gain.

The total gain of the two-stage amplifier is the product of the gains of the individual JFET CS and BJT CE amplifier :

$$A_{v-overall} = A_{v-\ firststage} \times A_{v-\text{second}stage}$$

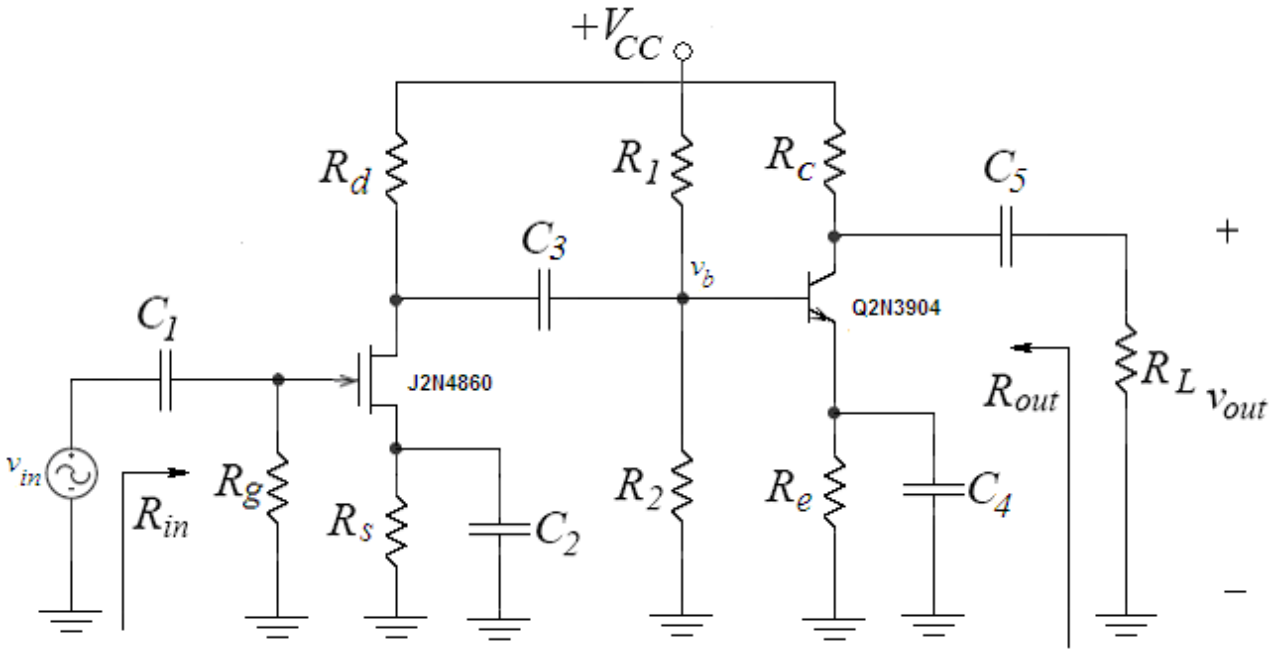

+VCC
Rd
R1
Rc
C5
C3
vb
+
C1
Q2N3904
J2N4860
Rout
RL
vout
vin
Rg
Rin
Rs
C2
R2
Re
C4
–

figure1

Preliminary Work:

Review the sections 4.12, 13.7.6, 15.1 through 15.2 from the Course Book.

In laboratory you will construct the circuit in Fig.1 using the transistors 2N3904 and 2N4860 and following values ;

V_{CC}	R_L	C_1=C_5	C_2=C_4	C_2
12 V	100 kΩ	10 µF	100 µF	22 µF

R_g	R_d	R_s	R_1	R_2	R_c	R_e
1 MΩ	1 kΩ	330 Ω	30 kΩ	47 kΩ	1 kΩ	2.2 kΩ

Assume the 2N3904 has a β =100, $V_{BE(ON)}$ = 0.7V and V_A = 100V. Use the emission coefficient as n = 1. (You can download data sheet 2N3904.pdf from course web page). The Pin Diagram of the 2N3904 is in Fig.2

The 2N4860 JFET used in this experiment is an n-channel JFET. The data sheet lists the typical value of V_p as -3V. The typical value of the drain to source saturation current (I_{DSS}) is 50 mA. (You can download data sheet 2N4860.pdf from course web page). The Pin Diagram of the 2N4860 is in Fig.3

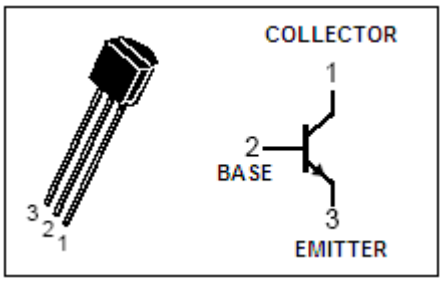


figure2

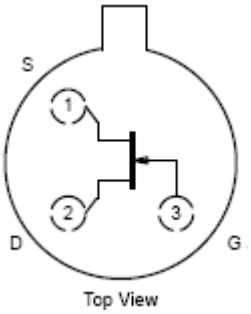


figure3

1. Make the DC analysis of the circuit given in the Fig.1;

a. Find the Q point of the JFET (I_D and V_{DS}) and its operation region
b. Find the Q point of the BJT (I_C and V_{CE}) and its operation region

2. Make the AC analysis of the circuit given in the Fig.1;

a. Draw the small signal AC equivalent of the circuit.

b. Find the voltage gains of each stage and the overall gain $A_{v\text{-}overall}$.

c. Find the input impedance R_{in}, and the output impedance R_{out} .

d. Calculate the largest value of the v_{in} that does not vioalate the small signal assumption.

e. Calculate the peak-to-peak maximum undistorted voltage swing at the output.

3) Simulate the current mirror using PSPICE. You will need to use a models for the J2N4860 and Q2N3904 transistors. The J2N4860 can be found in the JFET.LIB library and Q2N3904 can be found in the BIPOLAR.LIB library

a. Construct your circuit in Fig1. in Pspice

b. Bias simulation. Simulate the circuit of Fig.1. Do a BIAS simulation and find the **DC voltages at each node (V_D, V_G, V_S, V_B, V_C, V_E)** and **currents I_D, I_C, I_E, I_B.** Compare the results with the one you calculated in preliminary work part1.

c. Next, do a transient simulation. Use as input signal a sinusoidal source (V_{sin}) of 1 kHz frequency and amplitude of 0.1mVpeak. Find the **input voltage, output voltage and the voltage at v_b**. What are the **first stage, second stage, and overall voltage gain**? Compare the simulation results with your hand calculations.

d. Summarize the **simulation results in table** in table form and hand it in together with the calculations and the **simulation print-outs**. Label each graph clearly.

Experimental Work:

Before constructing the circuit,

- Verify the values of the resistors that you are going to use by measuring their resistances with a multimeter. Make sure that all resistors are within 2% of their marked values. This will assure that your current measurements are accurate

- Prepare the power supply for V_{CC} to ensure a DC voltage of 12V and adjust the function generator for a voltage level of approximately $1mV_{peak}$ at a frequency of 1kHz.

Construct the amplifier circuit using the values indicated in the preliminary work section.

1. Ground v_{in}. Measure and record V_G, V_D, V_S, V_B, V_C, V_E compare these with your calculations. Using the measured bias voltages calculate the bias current I_D and I_C. Compare these values with those calculated in the Preliminary work.

$V_G =$ $V_B =$
$V_D =$ $V_C =$
$V_S =$ $V_E =$

2. Apply a small signal input of $0.1mV_{peak}$ with a frequency of 1kHz at the gate of JFET (i.e. $v_{in}= 0.1mV_{peak}$). Use a voltage divider as shown in Fig.4 below. Observe the input output voltage waveforms and the voltage waveform at v_b on the oscilloscope. Calculate the first stage, secod stage and overall voltage gain of the amplifier and compare with your calculations in preliminary work. (R_1=8.2k, R_2=1k)

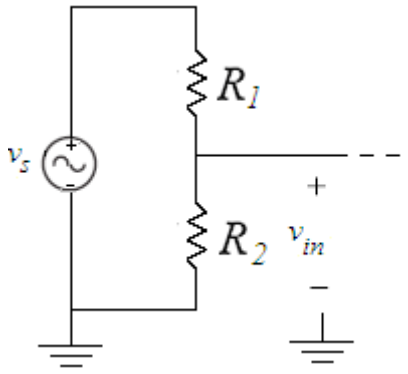
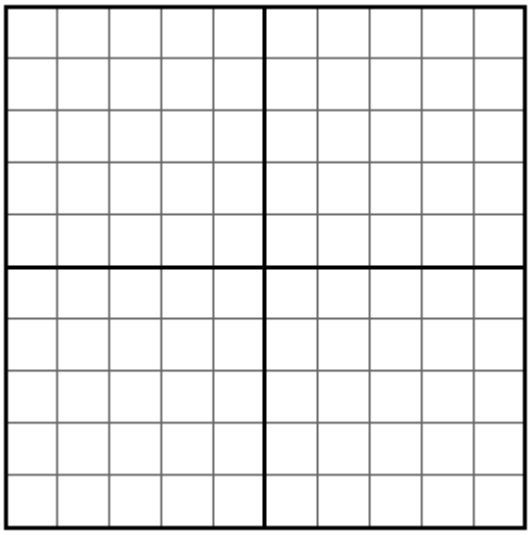
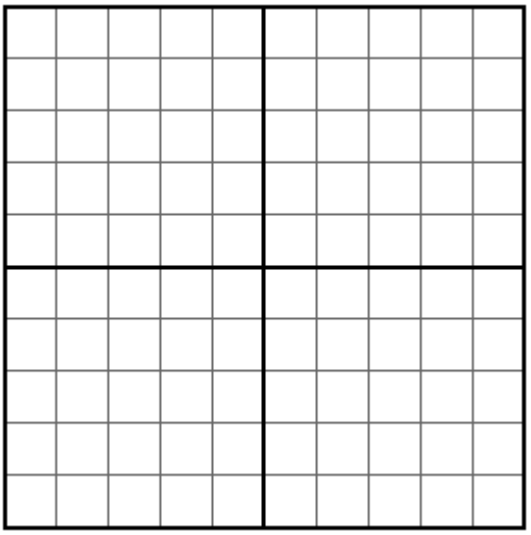


figure4

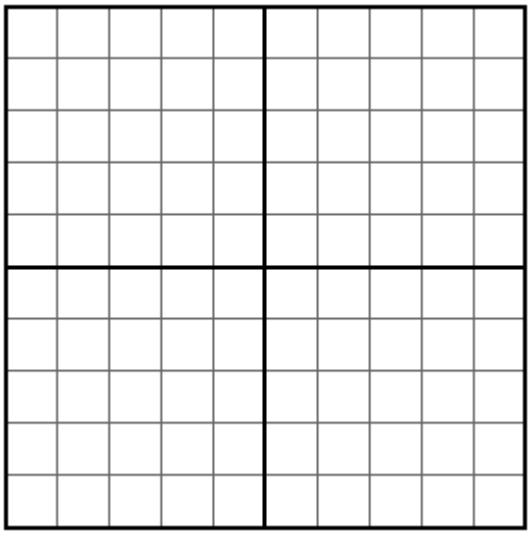
v_{in}



v_{out}



v_b



$A_{v\text{-}firststage}$ =
$A_{v\text{-}secondstage}$ =
$A_{v\text{-}overall}$ =

3. Determine the maximum peak-to-peak undistorted output voltage swing: Gradually increase the input signal amplitude and observe the onset of distortion at the output. Measure the peak-to-peak maximum undistorted output voltage swing. Compare this with your calculations.

$v_{out,undistorted\ max}$ =

4. Measure the input impedance R_{in} using method at the previous experiment.(R_x=500k)

R_{in} =

5. Measure the output impedance R_{out} using method at the previous experiment. (R_x=1k)

R_{out} =

6. Compare the input impedance, and output impedance at 1kHz with that obtained in the Preliminary work.

Experiment Instruments:	**Experiment Components:**
• Breadboard • Oscilloscope • Signal Generator • Multimeter • DC Power Source	1 2N4860 1 2N3904 4 1 kΩ 1 1 MΩ 1 100 kΩ 1 500kΩ 1 8.2 kΩ 1 30 kΩ 1 47 kΩ 1 2.2 kΩ 1 330 Ω 2 10 μF 2 100 μF 1 22 μF

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Experiment Results

Part1	V_G = V_B = V_D = V_C = V_S = V_E =	
Part2	$A_{v\text{-}firststage}$ = $A_{v\text{-}secondstage}$ = $A_{v\text{-}overall}$ =	
Part3	$v_{out,undistorted}$ =	
Part4	R_{in} =	
Part5	R_{out} =	

Student Name :

Signature…….……