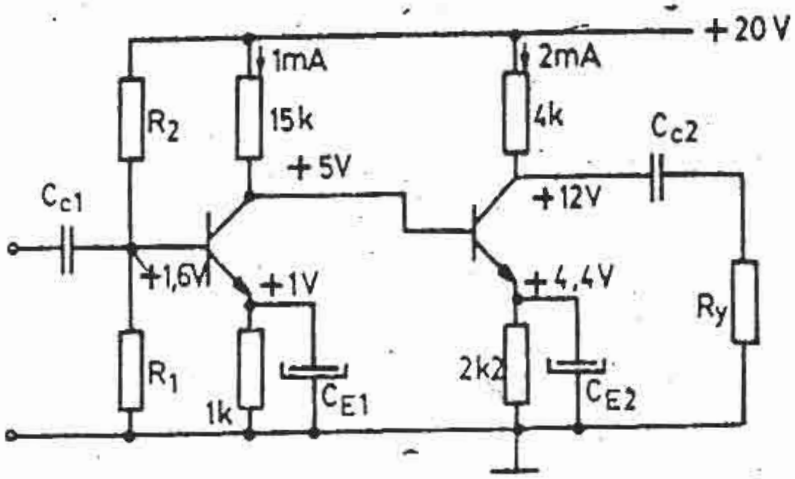
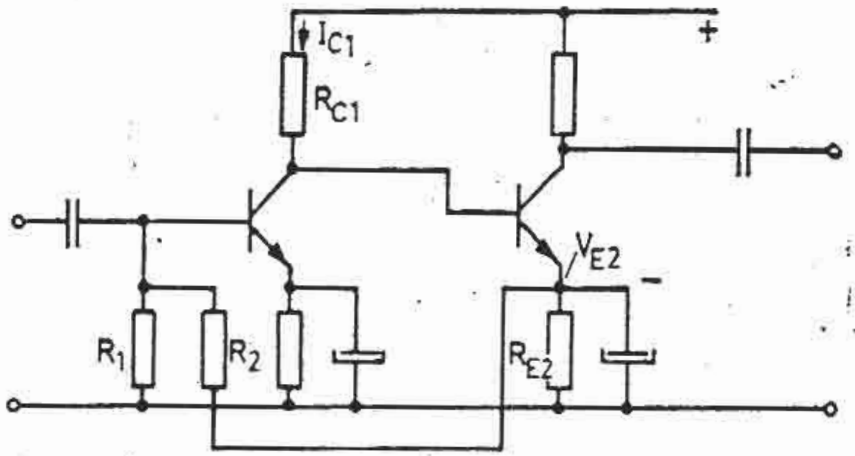
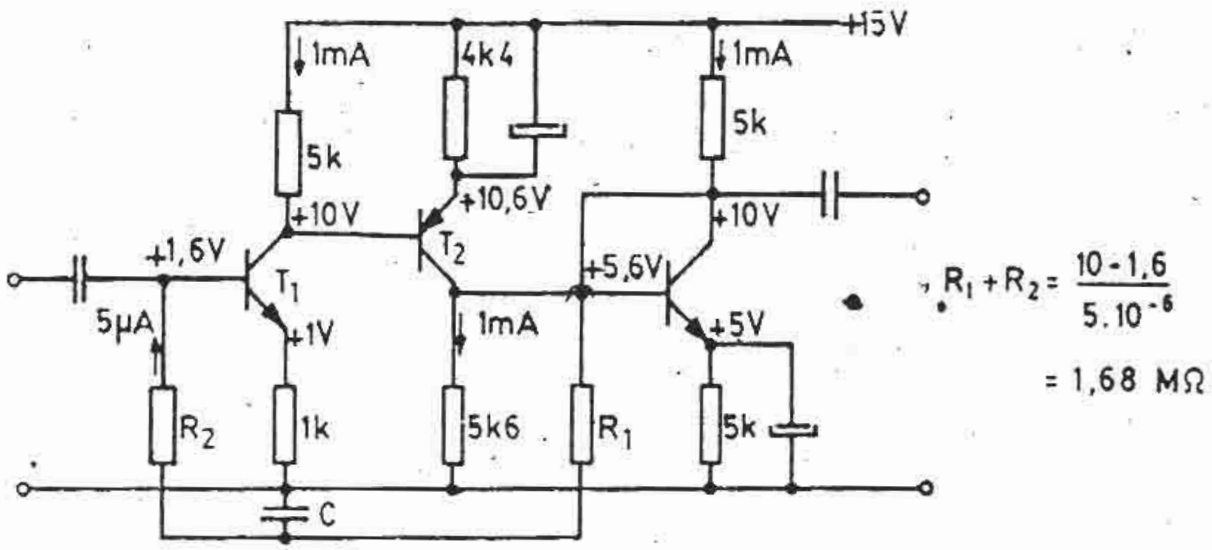


Şekil 6.1. Katları doğrudan doğruya bağlanmış iki katlı bir değişken işaret kuvvetlendiricisi.



Şekil 6.2. Doğru gerilim geribeslemesi ile çalışma noktalarının kararlılığının sağlanması.



$$R_1 + R_2 = \frac{10 - 1,6}{5.10^{-6}}$$

$$= 1,68\ M\Omega$$

Şekil 6.3. Üç katlı, doğrudan doğruya bağlamalı değişken işaret kuvvetlendiricisi.

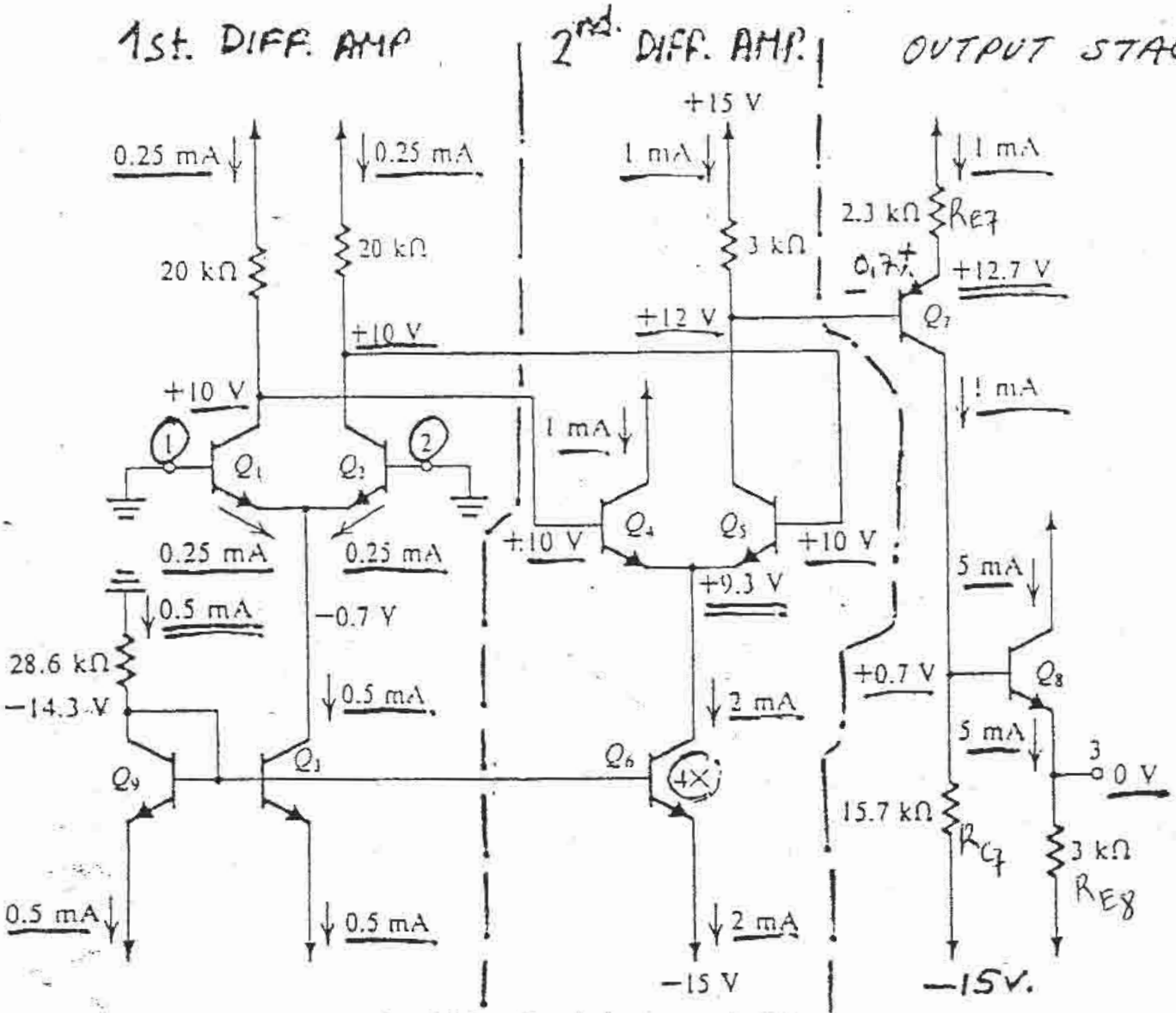


Fig. 6.24 Circuit for Example 6.3.

↑
SHIFTS THE dc LEVEL OF THE OUTPUT SIGNAL.

Terminals 1 & 2 : INPUT
Terminal 3 : OUTPUT

$A_v = -\frac{R_C}{r_e + R_E}$

AC- Analysis

$r_{e_1} = \frac{26mV}{0.25mA} = 104\Omega$ $\quad r_{e_2} = \frac{26mV}{1mA} = 26\Omega$ $\quad \beta = 100$

$r_{e_7} = \frac{26mV}{1mA} = 26\Omega$ $\quad r_{e_8} = \frac{26mV}{5mA} = 5.2\Omega$

$$A_{V1} = -\frac{R_{C1} // r_{\pi 2}}{r_{e_1}} \cong -\frac{R_{C1} // \beta r_{e_2}}{r_{e_1}} = -\frac{20k // 2.6k}{104\Omega} = -22.1$$

↳ differential output and $r_{\pi 2}$ = Bir sonraki katın giriş direncinin yaklaşık $\cong \beta r_{e_2}$

$$A_{V2} = -\frac{R_{C2} // R_{in7}}{2r_{e_7}} = -\frac{3k // 230k}{2 \times 26} \cong -57$$

see 15.97 solution $\frac{g_m}{2} = \frac{1}{2r_e}$

↳ Not differential output, Single output from Q5-collector.

$R_{in7} = r_{\pi 7} + (\beta+1) R_{E7} \cong \beta R_{E7} = 100 \times 2.3k = 230k$

$$A_{V7} = \frac{V_{c7}}{V_{b7}} = -\frac{R_{C7} // R_{in8}}{r_{e7} + R_{E7}} = -\frac{15.7 // 300k}{(26 + 2300)\Omega} = -6.4$$

↳ Unbypassed C-E amplifier where $R_{in8} = r_{\pi 8} + (\beta+1) R_{E8} \cong \beta R_{E8} = 300k$

$$A_{V8} = \frac{V_{e8}}{V_{c7}} = \frac{R_{E8}}{r_{e8} + R_{E8}} = \frac{3000}{5.2 + 3000} = 0.998$$ | C-C gain

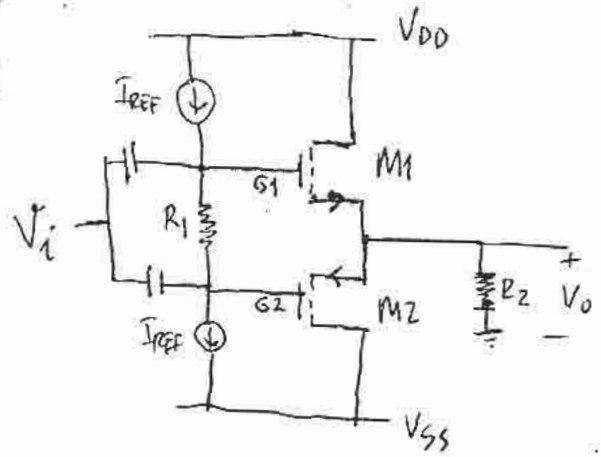
---

$$A_{V\text{-overall}} = (-22.1) \times (-57) \times (-6.4) \times (0.998) \cong -8046$$

$$A_{V\text{-overall}} \cong -8046$$

Fiyalde Başarılar MD

FET Push-pull amplifiers



Design Example.

Design the circuit for

$I_{D1} = I_{D2} = 4mA$ using

$K_n = K_p = 832\ \mu A/V^2$

$V_T = 1V$, $V_p = -1V$, $I_{REF} = 2mA$

$$I_{D_1} = \frac{K_n}{2}(V_{GS_1} - V_T)^2$$

$$I_{D_2} = \frac{K_p}{2}(V_{SG_2} + V_p)^2$$

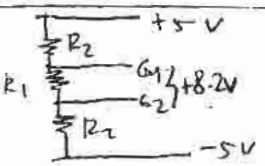
$$V_{GS1} = V_{SG2} = 4.1\ V$$

$V_{R1} = V_{GS1} + V_{SG2} = 8.2V \Rightarrow R_1 = \frac{V_{R1}}{I_{REF}} = \frac{8.2V}{2mA} =$

$R_1 = 4.1K$ can be used

If $V_{DD} = 5V$ $V_{SS} = -5V$

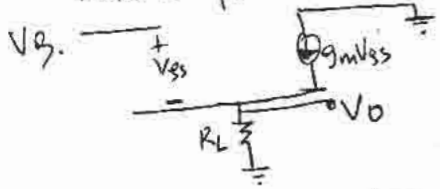
$V_{DD} - V_{SS} = 5 - (-5) = 10V$



$\frac{R_1}{R_1 + 2R_2} \cdot 10V = 8.2\ V = V_{G1-G2}$ can be used as a design criteria.

AC Analysis of FET push-pull

Since each FET is a common source amplifier, in its active period, common source model can be used.



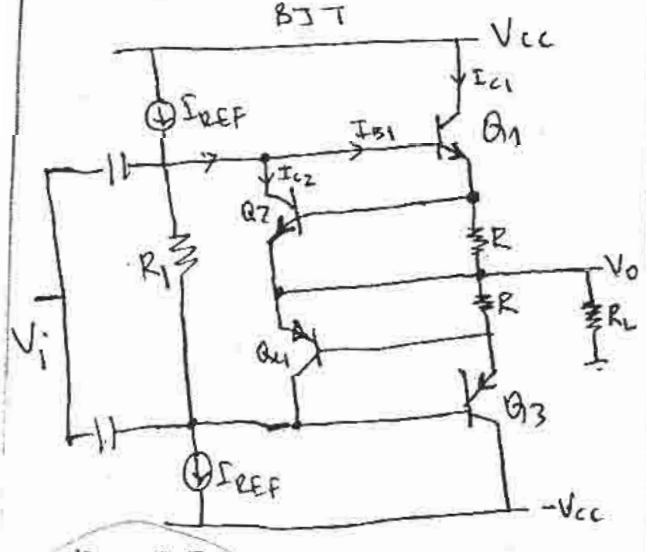
$V_g = V_{ss} + g_m V_{gs} R_L$

$V_o = g_m V_{gs} R_L$

$$\frac{V_o}{V_g} = A_v = \frac{g_m R_L}{1 + g_m R_L}$$

SHORT CIRCUIT PROTECTION IN PUSH-PULL AMPLIFIERS [CURRENT LIMITATIONS]

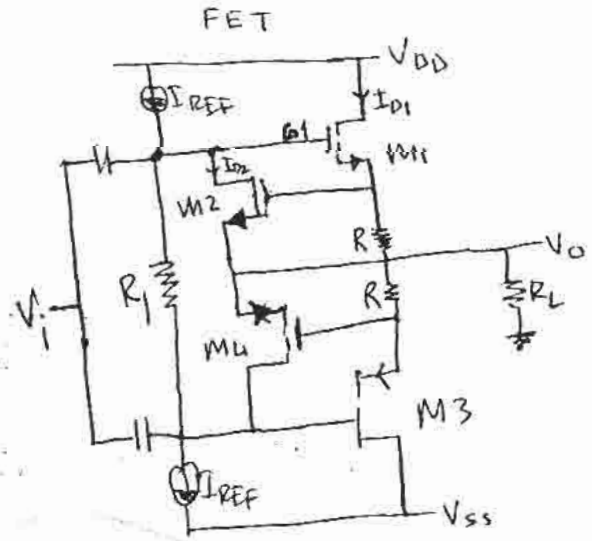
BJT



$R = \frac{0.7}{I_{MAX}}$

When I_{C1} exceeds $0.7V\ (I_{MAX})$ Q_2 becomes ON and steals the current I_{B1}, hence does not allow I_{C1} to increase

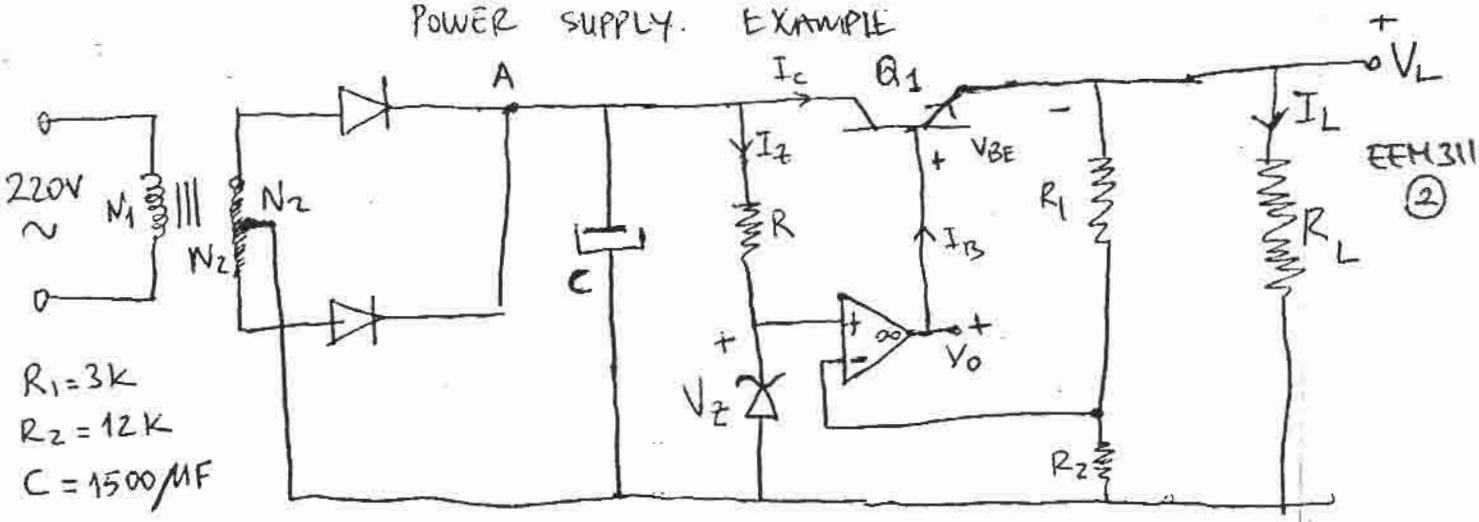
FET



$R = \frac{V_{TZ}}{I_{MAX}}$

When I_{D1} exceeds (I_{MAX}), $V_R > V_{TZ}$ M2 becomes ON, and steals the current on R_1 which gives the bias of V_{G1}.

POWER SUPPLY. EXAMPLE



EEM311 ②

$R_1 = 3K$
$R_2 = 12K$
$C = 1500\mu F$

$\beta_1 = 40$ $\quad P_{TOT} = 8W$ $\quad I_{CMAX} = 1A$ $\quad V_{CESAT} < 1V$ } BJT

$V_Z = 12V$ $\quad P_{TOT} = 240mW$ $\quad I_{Zmin} = 2mA$ } Zener Diode

$I_{BMAX} = 20mA$ (maximum available output current for OPAMP)

---

a) $V_L = ?$ (as a function of V_Z)

b) $I_L \gg I_Z$ or $I_C \gg I_Z \Rightarrow V_{AC} = ?$ ripple on A = ?

c) $P_{Lmax} = ?$ $\quad R_{Lmin} = ?$ $\quad I_{LMAX} = ?$

d) $R_{MAX} = ?$ for $V_A = V_{Amin}$ (for sudden supply loss)

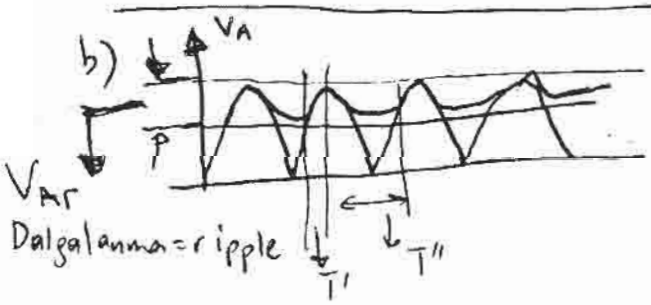
---

a) $V_O - V_{BE} = V_L$ and $V_Z = \frac{R_2}{R_1+R_2} V_L \Rightarrow V_L = \frac{R_1+R_2}{R_2} V_Z$

$V_L = \frac{15K}{12K} \cdot 12V = 15V$ stable regulator output voltage

---

b)



T' → Charging time for capacitance

T'' → Discharging time for capacitance.

$T'' \gg T'$ $\quad T' + T'' = T = \frac{1}{2f} \Rightarrow T'' \simeq \frac{1}{2f}$ (T: signal period.)

Capacitance: $\Delta Q_1 = \Delta Q_2$ (charge differences are identical for T' and T'')

$C V_{AC} = I_L T'' = I_L T = I_L \frac{1}{2f} \Rightarrow V_{AC_{p-p}} \simeq I_L \frac{1}{2fC}$

$f = 50Hz$ $\quad C = 1500\mu F \rightarrow V_{AC(max)} = \frac{I_{Lmax}}{0.15}$

$\rightarrow V_{AC(max)_{p-p}} \simeq 5.33V$ (peak to peak)

---

c) $I_{LMAX} = I_{BMAX} \cdot \beta_1 = 20mA \cdot 40 = 0.8A \rightarrow V_{AC(peak)} \simeq 2.6V = 2.665$

$P_{LMAX} = I_{LMAX} \cdot V_L = 15 \cdot 0.8 = 12W$

$P_{LMAX} = R_{Lmin} I^2_{LMAX} = 0.64 R_{Lmin} = 12W \rightarrow$

$R_{Lmin} \simeq 20\Omega$ OR exactly $R_{Lmin} = 18.75\Omega$

output of regulator $15 \mp 2.6V$ roughly.

POWER SUPPLY EXAMPLE

d) $V_{Amin} = V_L + V_{CEmin} = 15 + 1 = 16\,V$

↓ no distortion → $V_{CESAT} < 1$

$$\frac{V_{Amin} - V_Z}{R} \geq I_{Zmin} \Rightarrow R \leq \frac{V_{Amin} - V_Z}{I_{Zmin}}$$

$$R_{MAX} = \frac{V_{Amin} - V_Z}{I_{Zmin}} = \frac{16 - 12}{2mA} = \frac{4V}{2mA} = 2K\Omega$$

$$R \leq 2K\Omega = 2000\,\Omega$$

Geri Besleme	series-shunt Seri-gerilim	series-series Seri-akım	shunt-series Paralel-akım	shunt-shunt Paralel-gerilim
Örnek (xF)	Gerilim	Gerilim	Akım	Akım
Giriş devresi	$V_o = 0$	$I_o = 0$	$I_o = 0$	$V_o = 0$
Çıkış "	$I_i = 0$	$I_i = 0$	$V_i = 0$	$V_i = 0$
İşaret kaynağı	Thevenin	Thevenin	Norton	Norton
$\beta = \frac{x_f}{x_o}$	$\frac{V_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$	$\frac{I_f}{V_o}$
$A = \frac{x_o}{x_i}$	$A_V = \frac{V_o}{V_i}$	$G_M = \frac{I_o}{V_i}$	$A_I = \frac{I_o}{I_i}$	$R_M = \frac{V_o}{I_i}$
$D = 1 + \beta A$	$1 \mp \beta A_V$	$1 \mp \beta G_M$	$1 \mp \beta A_I$	$1 \mp \beta R_M$
A_f	$A_{Vf} = \frac{A_V}{D}$	$G_{Mf} = \frac{G_M}{D}$	$A_{If} = \frac{A_I}{D}$	$R_{Mf} = \frac{R_M}{D}$
R_{if}	$R_i \cdot D$	$R_i \cdot D$	$\frac{R_i}{D}$	$\frac{R_i}{D}$
R_{of}	$\frac{R_o}{1 + \beta A_V}$	$R_o(1 \mp \beta G_m)$	$R_o(1 \mp \beta A_i)$	$\frac{R_o}{1 \mp \beta R_m}$
R'_{of}	$\frac{R_o'}{D}$	$R_o' \cdot \frac{1 \mp \beta G_m}{D}$	$R_o' \cdot \frac{1 \mp \beta A_i}{D}$	$\frac{R_o'}{D}$

* Tranzistörün kesim frekansı (hfe = 1 'e düştüğü yer) $f_T = \frac{1}{2\pi r_e (C_i + C_r)}$

* Yüksek frekanslar:
  - $f_2 \cdot t_r = 0{,}35$ — RC bağlamalı kuvvetlendirici devrelerde cevap
  - $t_r = 2{,}2\,RC$ (yükselme süresi)
  - $f_{2n} \cdot t_{rn} \geq 0{,}35$
  - $f_{2n} = f_2 \sqrt{2^{1/n} - 1}$ — n: Küçük sayısı
  - $t_{rn} \cong 1{,}1 \sqrt{t_{r_1}^2 + t_{r_2}^2 + \dots}$
  - $t_{rn} = 1{,}1 \sqrt{n}\, t_r$ (tr'ler eşit ise)

Alçak frekanslarda:

Failure:

$$\delta(\%) = 100 \frac{\Delta V}{V_0} = \frac{t_1}{\tau'} \cdot 100 = 100 \frac{t_1}{(R_1 + R_2)C} = 100\, t_1 \cdot f_1 \cdot 2\pi$$

$t_1 = \frac{T}{2} = \frac{1}{2f}$, $\delta = \frac{1}{2 f \tau}$

n kat varsa

$$T_n = t_1 \left(\frac{1}{\tau_1'} + \frac{1}{\tau_2'} + \dots \right) = t_1 \frac{n}{\tau'} \qquad (\tau_1' = \tau_2' = \dots)$$

Note 1: EITHER $A > 0$ and SUBTRACTION ($-$) IS USED AT THE INPUT OR $A < 0$ AND ADDITION IS USED AT THE INPUT FOR NEGATIVE FEEDBACK

AT THE SECOND CASE $A_f = A/(1 - A \cdot f)$ WHERE $A < 0$

Note 2:

VOLTAGE SAMPLING at the output, makes the output closer to IDEAL VOLTAGE SOURCE, Hence output resistance decreases.

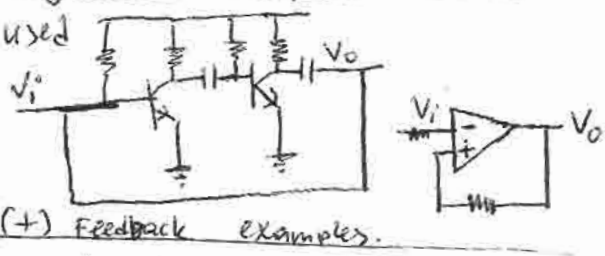
CURRENT SAMPLING at the input, makes the output closer to IDEAL CURRENT SOURCE, Hence output resistance increases

VOLTAGE COMPARISON at the input, makes the voltage from the source BETTER APPLIED TO AMPLIFIER by increasing input impedance (ideal Voltage Amplifier)

CURRENT COMPARISON at the input, makes the current from the source BETTER APPLIED TO AMPLIFIER By decreasing input impedance.

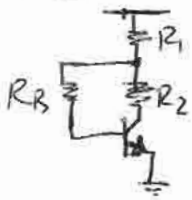
Note 3: Positive feedback should not be used

It causes undesired oscillations and/or INSTABILITY. Any very small variation is "feedback" with amplification.



(+) Feedback examples.

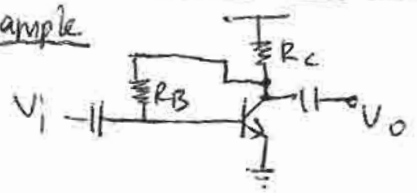
Note 4: Feedback connections cannot be limited only to 4 types "series-shunt, shunt-series, shunt-shunt, series-series". These are only the types that are EASY for calculation. Hence in the design they are PREFERRED.



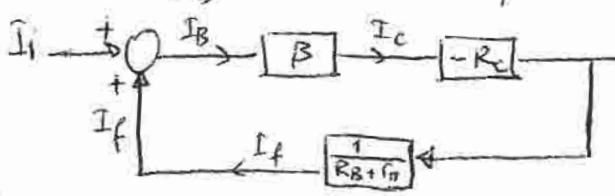
In the circuit given on the right, if $R_2 \ll R_1$ the circuit is VOLTAGE SAMPLING

Note 5: We should first divide the circuit into two as "forward gain without feedback" block, and "feedback gain" block. When finding forward gain, loading effect of feedback circuit should also be considered.

Example



Assume $R_B \gg R_C$. Then feedback block diagram is



$A = -\beta R_C$

$A = \frac{V_o}{I_i}$ {NO Feedback

$f = -\beta R_C \cdot \frac{1}{R_B + r_\pi} \simeq -\frac{\beta R_C}{R_B} \Rightarrow A_f = \frac{V_o}{I_i} = \frac{A}{1 - Af} \simeq -\frac{\beta R_C}{1 + \beta R_C / R_B} \simeq -\frac{\beta R_C R_B}{R_B + \beta R_C}$

$Z_i = r_\pi \qquad Z_o = r_o \leftarrow$ NO feedback

$Z_{if} = \frac{Z_i}{1 - Af} \simeq \frac{r_\pi}{1 + \frac{\beta R_C}{R_B}}$, $Z_{of} = \frac{Z_o}{1 - Af} \simeq \frac{r_o}{1 + \frac{\beta R_C}{R_B}}$ } WITH FEEDBACK

A_f

It is interesting to note that the use of feedback, while resulting in a lowering of voltage gain, has provided an increase in B and in the upper 3-dB frequency particularly. In fact, the product of gain and frequency remains the same so that the gain-bandwidth product of the basic amplifier is the same value for the feedback amplifier. However, since the feedback amplifier has lower gain, the net operation was to *trade* gain for bandwidth (we use bandwidth for the upper 3-dB frequency since typically $f_2 \gg f_1$).

Gain Stability with Feedback

In addition to the β factor setting a precise gain value, we are also interested in how stable the feedback amplifier is compared to an amplifier without feedback. Differentiating Eq. (17.2) leads to

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1 + \beta A|}\left|\frac{dA}{A}\right| \tag{17.8}$$

$$\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \qquad \text{for } \beta A \gg 1 \tag{17.9}$$

This shows that magnitude of the relative change in gain $\left|\frac{dA_f}{A_f}\right|$ is reduced by the factor $|\beta A|$ compared to that without feedback $\left(\left|\frac{dA}{A}\right|\right)$.

EXAMPLE 17.2

If an amplifier with gain of -1000 and feedback of $\beta = -0.1$ has a gain change of 20% due to temperature, calculate the change in gain of the feedback amplifier.

Solution

Using Eq. (17.9), we get

$$\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| = \left|\frac{1}{-0.1(-1000)}(20\%)\right| = \mathbf{0.2\%}$$

The improvement is 100 times. Thus, while the amplifier gain changes from $|A| = 1000$ by 20%, the gain with feedback changes from $|A_f| = 100$ by only 0.2%.

17.3 PRACTICAL FEEDBACK CIRCUITS

Examples of practical feedback circuits will provide a means of demonstrating the effect feedback has on the various connection types. This section provides only a basic introduction to this topic.

Voltage-Series Feedback

Figure 17.7 shows an FET amplifier stage with voltage-series feedback. A part of the output signal (V_o) is obtained using a feedback network of resistors R_1 and R_2. The feedback voltage V_f is connected in series with the source signal V_s, their difference being the input signal V_i.

Without feedback the amplifier gain is

$$A = \frac{V_o}{V_i} = -g_m R_L \tag{17.10}$$

where R_L is the parallel combination of resistors:

$$R_L = R_D R_o (R_1 + R_2) \tag{17.11}$$

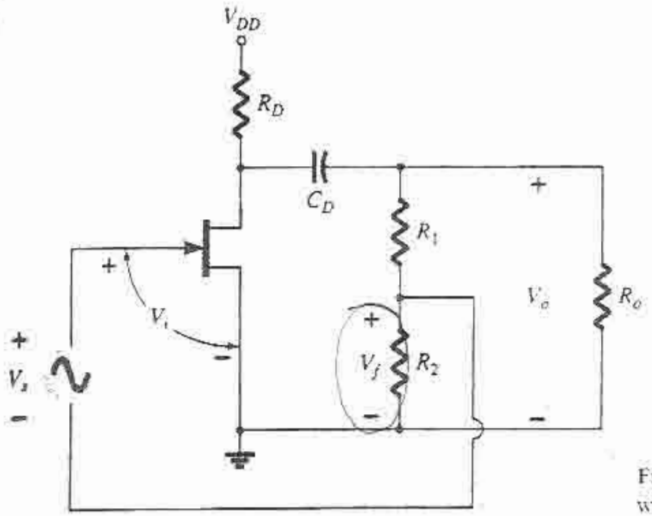


Figure 17.7 FET amplifier stage with voltage-series feedback.

The feedback network provides a feedback factor of

$$\beta = \frac{V_f}{V_o} = \frac{-R_2}{R_1 + R_2} \tag{17.12}$$

Using the values of A and β above in Eq. (17.2), we find the gain with negative feedback to be

$$A_f = \frac{A}{1 + \beta A} = \frac{-g_m R_L}{1 + [R_2 R_L/(R_1 + R_2)]g_m} \tag{17.13}$$

If $\beta A \gg 1$, we have

$$\boxed{A_f \cong \frac{1}{\beta} = -\frac{R_1 + R_2}{R_2}} \tag{17.14}$$

EXAMPLE 17.3

Calculate the gain without and with feedback for the FET amplifier circuit of Fig. 17.7 and the following circuit values: $R_1 = 80\ \text{k}\Omega$, $R_2 = 20\ \text{k}\Omega$, $R_o = 10\ \text{k}\Omega$, $R_D = 10\ \text{k}\Omega$, and $g_m = 4000\ \mu\text{S}$.

Solution

$$R_L \cong \frac{R_o R_D}{R_o + R_D} = \frac{10\ \text{k}\Omega\,(10\ \text{k}\Omega)}{10\ \text{k}\Omega + 10\ \text{k}\Omega} = 5\ \text{k}\Omega$$

Neglecting 100 kΩ resistance of R_1 and R_2 in series

$$A = -g_m R_L = -(4000 \times 10^{-6}\ \mu\text{S})(5\ \text{k}\Omega) = \mathbf{-20}$$

The feedback factor is

$$\beta = \frac{-R_2}{R_1 + R_2} = \frac{-20\ \text{k}\Omega}{80\ \text{k}\Omega + 20\ \text{k}\Omega} = -0.2$$

The gain with feedback is

$$A_f = \frac{A}{1 + \beta A} = \frac{-20}{1 + (-0.2)(-20)} = \frac{-20}{5} = \mathbf{-4}$$

A_f

Figure 17.8 shows a voltage-series feedback connection using an op-amp. The gain of the op-amp, A, without feedback, is reduced by the feedback factor

$$\beta = \frac{R_2}{R_1 + R_2} \tag{17.15}$$

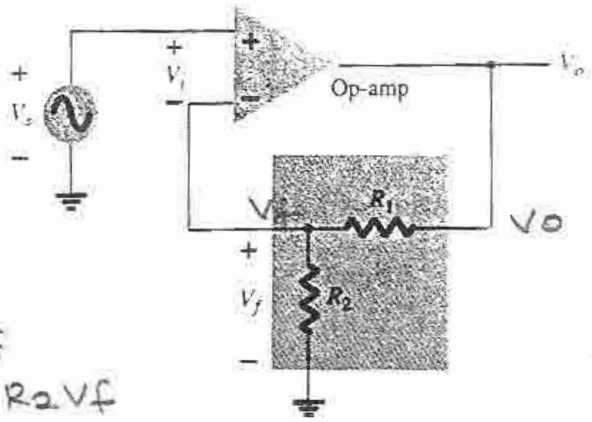


Figure 17.8 Voltage-series feedback in an op-amp connection.

EXAMPLE 17.4

Calculate the amplifier gain of the circuit of Fig. 17.8 for op-amp gain $A = 100{,}000$ and resistances $R_1 = 1.8\ \text{k}\Omega$ and $R_2 = 200\ \Omega$.

Solution

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{200\ \Omega}{200\ \Omega + 1.8\ \text{k}\Omega} = 0.1$$

$$A_f = \frac{A}{1 + \beta A} = \frac{100{,}000}{1 + (0.1)(100{,}000)}$$

$$= \frac{100{,}000}{10{,}001} = 9.999$$

Note that since $\beta A \gg 1$,

$$A_f \cong \frac{1}{\beta} = \frac{1}{0.1} = \mathbf{10}$$

The emitter-follower circuit of Fig. 17.9 provides voltage-series feedback. The signal voltage, V_s, is the input voltage, V_i. The output voltage, V_o, is also the feedback

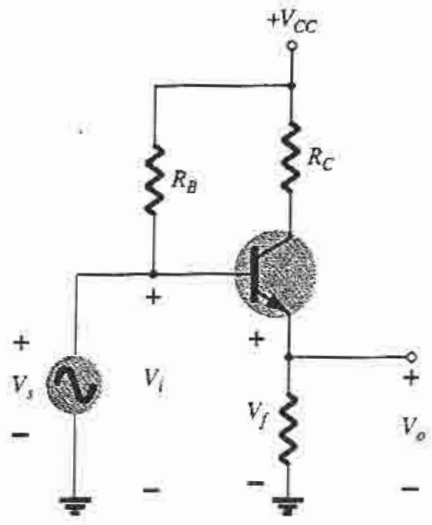


Figure 17.9 Voltage-series feedback circuit (emitter-follower).

A_f

voltage in series with the input voltage. The amplifier, as shown in Fig. 17.9, provides the operation *with* feedback. The operation of the circuit without feedback provides $V_f = 0$, so that

$$A = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_E}{V_s} = \frac{h_{fe} R_E (V_s/h_{ie})}{V_s} = \frac{h_{fe} R_E}{h_{ie}}$$

and

$$\beta = \frac{V_f}{V_o} = 1$$

The operation with feedback then provides that

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A} = \frac{h_{fe} R_E / h_{ie}}{1 + (1)(h_{fe} R_E / h_{ie})}$$

$$= \frac{h_{fe} R_E}{h_{ie} + h_{fe} R_E}$$

For $h_{fe} R_E \gg h_{ie}$,

$$A_f \cong 1$$

Current-Series Feedback = Series-series Akım örnekleme

Another feedback technique is to sample the output current (I_o) and return a proportional voltage in series with the input. While stabilizing the amplifier gain, the current-series feedback connection increases input resistance.

Figure 17.10 shows a single transistor amplifier stage. Since the emitter of this stage has an unbypassed emitter, it effectively has current-series feedback. The current through resistor R_E results in a feedback voltage that opposes the source signal applied so that the output voltage V_o is reduced. To remove the current-series feedback, the emitter resistor must be either removed or bypassed by a capacitor (as is usually done).

(Voltaj girişi, akım geri besleme)

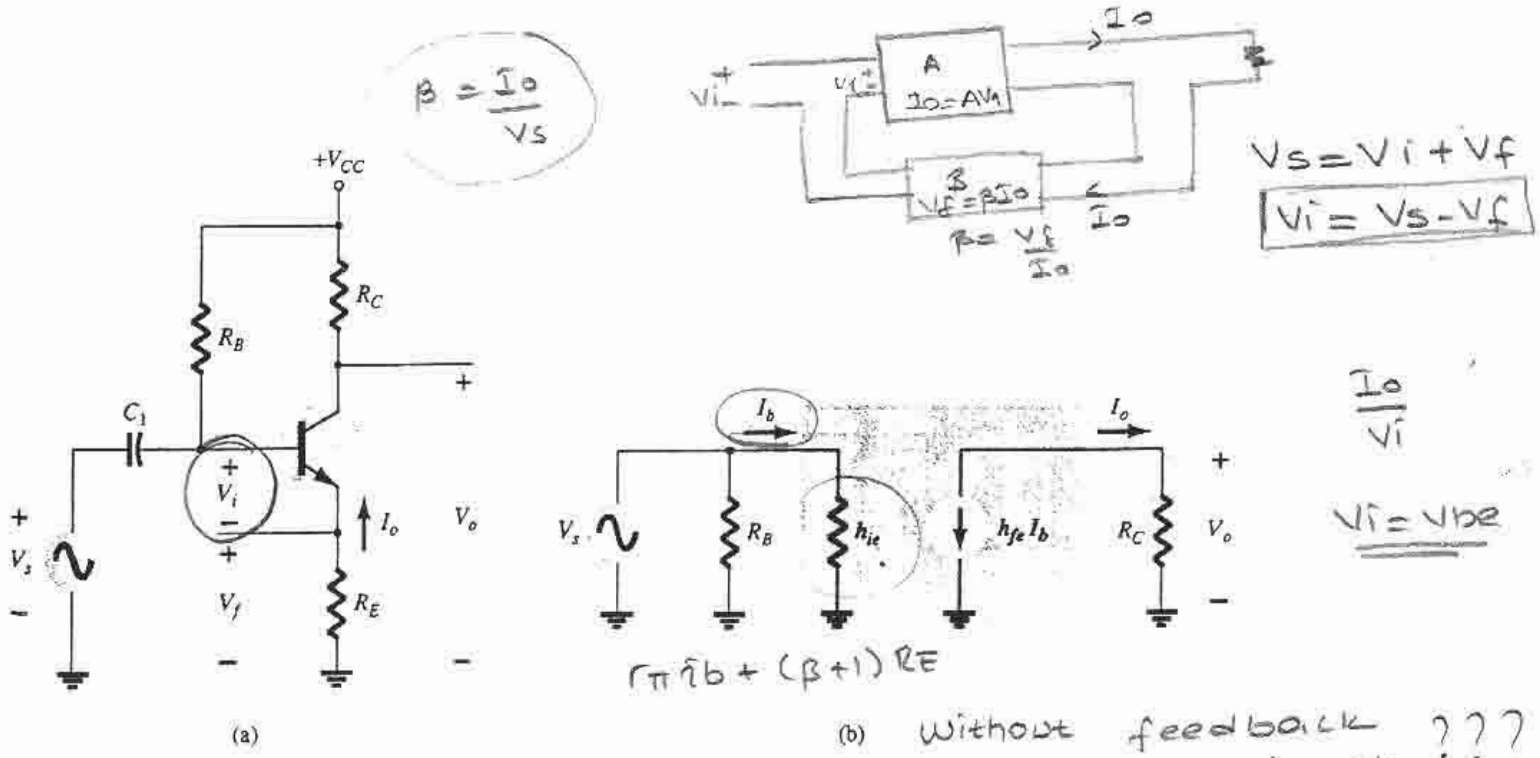


Figure 17.10 Transistor amplifier with unbypassed emitter resistor (R_E) for current-series feedback: (a) amplifier circuit; (b) ac equivalent circuit without feedback.

A_f

WITHOUT FEEDBACK

Referring to the basic format of Fig. 17.2a and summarized in Table 17.1, we have

$$A = \frac{I_o}{V_i} = \frac{-I_b h_{fe}}{I_b h_{ie} + R_E} = \frac{-h_{fe}}{h_{ie} + R_E} \tag{17.16}$$

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_E}{I_o} = -R_E \tag{17.17}$$

The input and output impedances are

$$Z_i = R_B \| (h_{ie} + R_E) \cong h_{ie} + R_E \tag{17.18}$$

$$Z_o = R_C \tag{17.19}$$

WITH FEEDBACK

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} = \frac{-h_{fe}/h_{ie}}{1 + (-R_E)\left(\dfrac{-h_{fe}}{h_{ie} + R_E}\right)} \cong \frac{-h_{fe}}{h_{ie} + h_{fe} R_E} \tag{17.20}$$

The input and output impedance is calculated as specified in Table 17.2.

$$Z_{if} = Z_i (1 + \beta A) \cong h_{ie}\left(1 + \frac{h_{fe} R_E}{h_{ie}}\right) = h_{ie} + h_{fe} R_E \tag{17.21}$$

$$Z_{of} = Z_o (1 + \beta A) = R_C\left(1 + \frac{h_{fe} R_E}{h_{ie}}\right) \tag{17.22}$$

The voltage gain (A) with feedback is

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_C}{V_s} = \left(\frac{I_o}{V_s}\right) R_C = A_f R_C \cong \frac{-h_{fe} R_C}{h_{ie} + h_{fe} R_E} \tag{17.23}$$

EXAMPLE 17.5 Calculate the voltage gain of the circuit of Fig. 17.11.

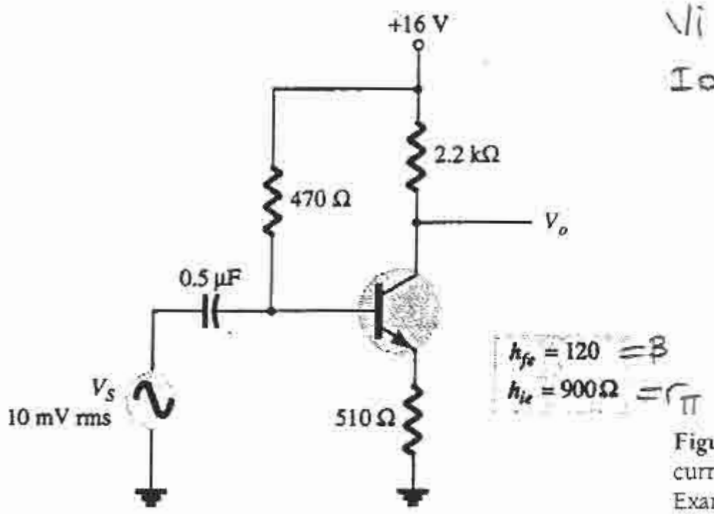


Figure 17.11 BJT amplifier with current-series feedback for Example 17.5

Solution

Without feedback,

$$A = \frac{I_o}{V_i} = \frac{-h_{fe}}{h_{ie} + R_E} = \frac{-120}{900 + 510} = -0.085$$

$$\beta = \frac{V_f}{I_o} = -R_E = -510$$

The factor $(1 + \beta A)$ is then

$$1 + \beta A = 1 + (-0.085)(-510) = 44.35$$

The gain with feedback is then

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} = \frac{-0.085}{44.35} = -1.92 \times 10^{-3}$$

and the voltage gain with feedback A_{vf} is

$$A_{vf} = \frac{V_o}{V_s} = A_f R_C = (-1.92 \times 10^{-3})(2.2 \times 10^3) = \mathbf{-4.2}$$

Without feedback ($R_E = 0$), the voltage gain is

$$A_v = \frac{-R_C}{r_e} = \frac{-2.2 \times 10^3}{7.5} = \mathbf{-293.3}$$

Voltage-Shunt Feedback

The constant-gain op-amp circuit of Fig. 17.12a provides voltage-shunt feedback. Referring to Fig. 17.2b and Table 17.1 and the op-amp ideal characteristics $I_i = 0$, $V_i = 0$, and voltage gain of infinity, we have

$$A = \frac{V_o}{I_i} = \infty \tag{17.24}$$

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_o} \tag{17.25}$$

The gain with feedback is then

$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i} = \frac{A}{1 + \beta A} = \frac{1}{\beta} = -R_o \tag{17.26}$$

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback,

$$A_{vf} = \frac{V_o}{I_s}\frac{I_s}{V_1} = (-R_o)\frac{1}{R_1} = \frac{-R_o}{R_1} \tag{17.27}$$

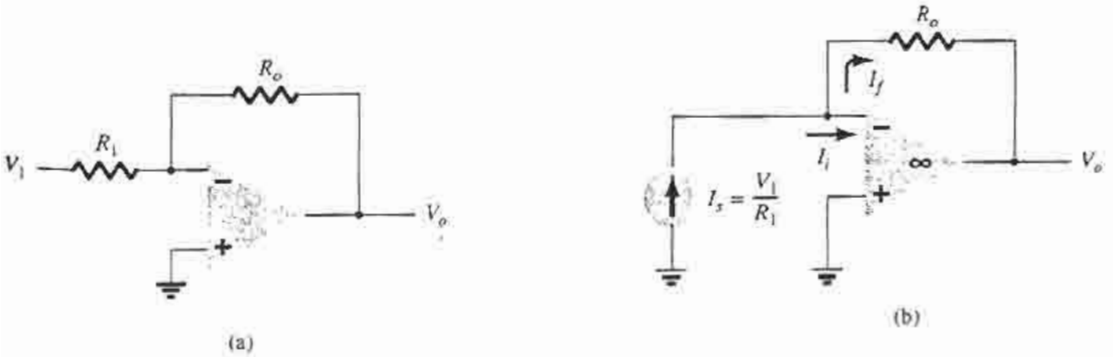


Figure 17.12 Voltage-shunt negative feedback amplifier: (a) constant-gain circuit; (b) equivalent circuit.

A_f

The circuit of Fig. 17.13 is a voltage-shunt feedback amplifier using an FET with no feedback, $V_f = 0$.

$$A = \frac{V_o}{I_i} \cong -g_m R_D R_S \tag{17.28}$$

The feedback is

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_F} \tag{17.29}$$

With feedback, the gain of the circuit is

$$A_f = \frac{V_o}{I_s} = \frac{A}{1 + \beta A} = \frac{-g_m R_D R_S}{1 + (-1/R_F)(-g_m R_D R_S)}$$

$$= \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S} \tag{17.30}$$

The voltage gain of the circuit with feedback is then

$$A_{vf} = \frac{V_o}{I_s}\frac{I_s}{V_s} = \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S}\left(\frac{1}{R_S}\right)$$

$$= \frac{-g_m R_D R_F}{R_F + g_m R_D R_S} = (-g_m R_D)\frac{R_F}{R_F + g_m R_D R_S} \tag{17.31}$$

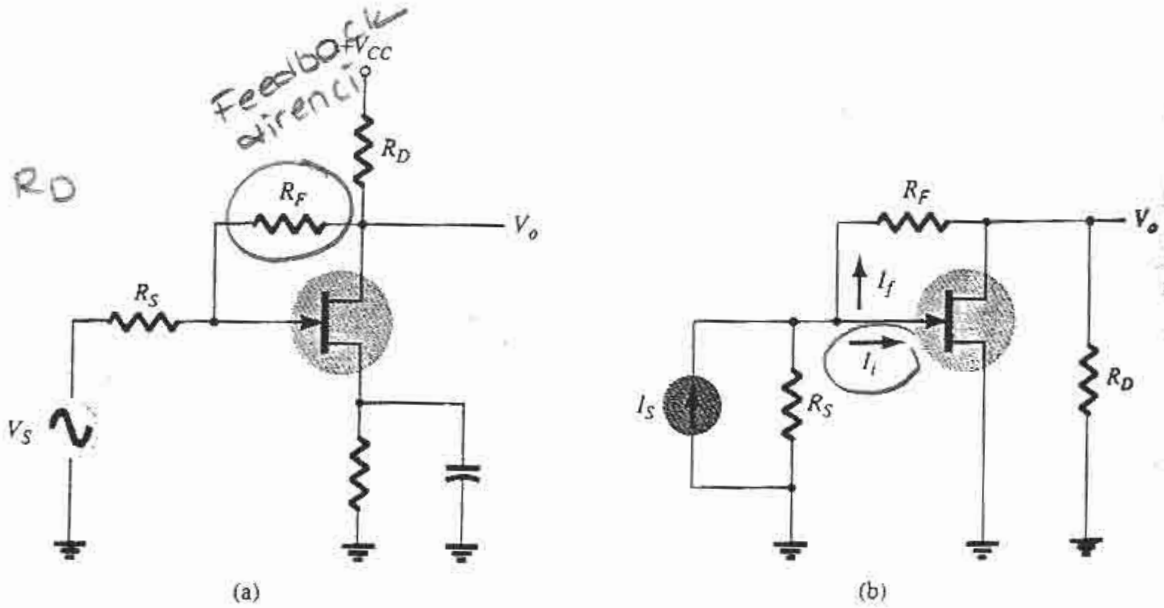


Figure 17.13 Voltage-shunt feedback amplifier using an FET: (a) circuit; (b) equivalent circuit.

EXAMPLE 17.6

Calculate the voltage gain with and without feedback for the circuit of Fig. 17.13a with values of $g_m = 5$ mS, $R_D = 5.1$ kΩ, $R_S = 1$ kΩ, and $R_F = 20$ kΩ.

Solution

Without feedback, the voltage gain is

$$A_v = -g_m R_D = -(5 \times 10^{-3})(5.1 \times 10^3) = \mathbf{-25.5}$$

h feedback the gain is reduced to

$$A_{vf} = (-g_m R_D)\frac{R_F}{R_F + g_m R_D R_S}$$

$$= (-25.5)\frac{20 \times 10^3}{(20 \times 10^3) + (5 \times 10^{-3})(5.1 \times 10^3)(1 \times 10^3)}$$

$$= -25.5(0.44) = \mathbf{-11.2}$$

'.4 FEEDBACK AMPLIFIER—PHASE AND FREQUENCY CONSIDERATIONS

far we have considered the operation of a feedback amplifier in which the feed-ck signal was *opposite* to the input signal—negative feedback. In any practical cir-it this condition occurs only for some mid-frequency range of operation. We know it an amplifier gain will change with frequency, dropping off at high frequencies om the mid-frequency value. In addition, the phase shift of an amplifier will also ange with frequency.

If, as the frequency increases, the phase shift changes then some of the feedback gnal will *add* to the input signal. It is then possible for the amplifier to break into cillations due to positive feedback. If the amplifier oscillates at some low or high equency, it is no longer useful as an amplifier. Proper feedback-amplifier design re-uires that the circuit be stable at *all* frequencies, not merely those in the range of in-rest. Otherwise, a transient disturbance could cause a seemingly stable amplifier to ıddenly start oscillating.

lyquist Criterion

ı judging the stability of a feedback amplifier, as a function of frequency, the βA roduct and the phase shift between input and output are the determining factors. One f the most popular techniques used to investigate stability is the Nyquist method. A lyquist diagram is used to plot gain and phase shift as a function of frequency on a omplex plane. The Nyquist plot, in effect, combines the two Bode plots of gain ver-us frequency and phase shift versus frequency on a single plot. A Nyquist plot is sed to quickly show whether an amplifier is stable for all frequencies and how sta-le the amplifier is relative to some gain or phase-shift criteria.

As a start, consider the *complex plane* shown in Fig. 17.14. A few points of var-ous gain (βA) values are shown at a few different phase-shift angles. By using the

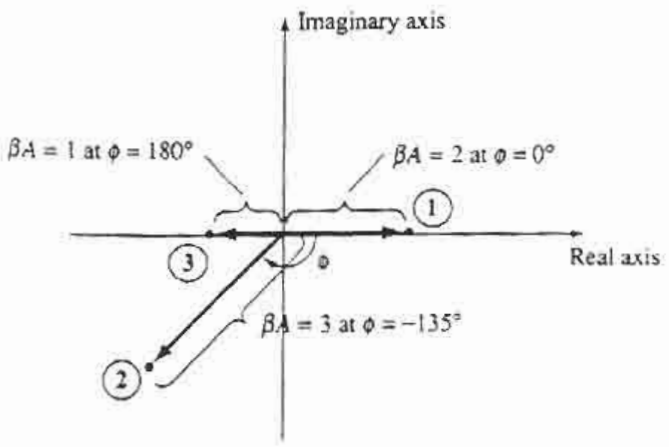
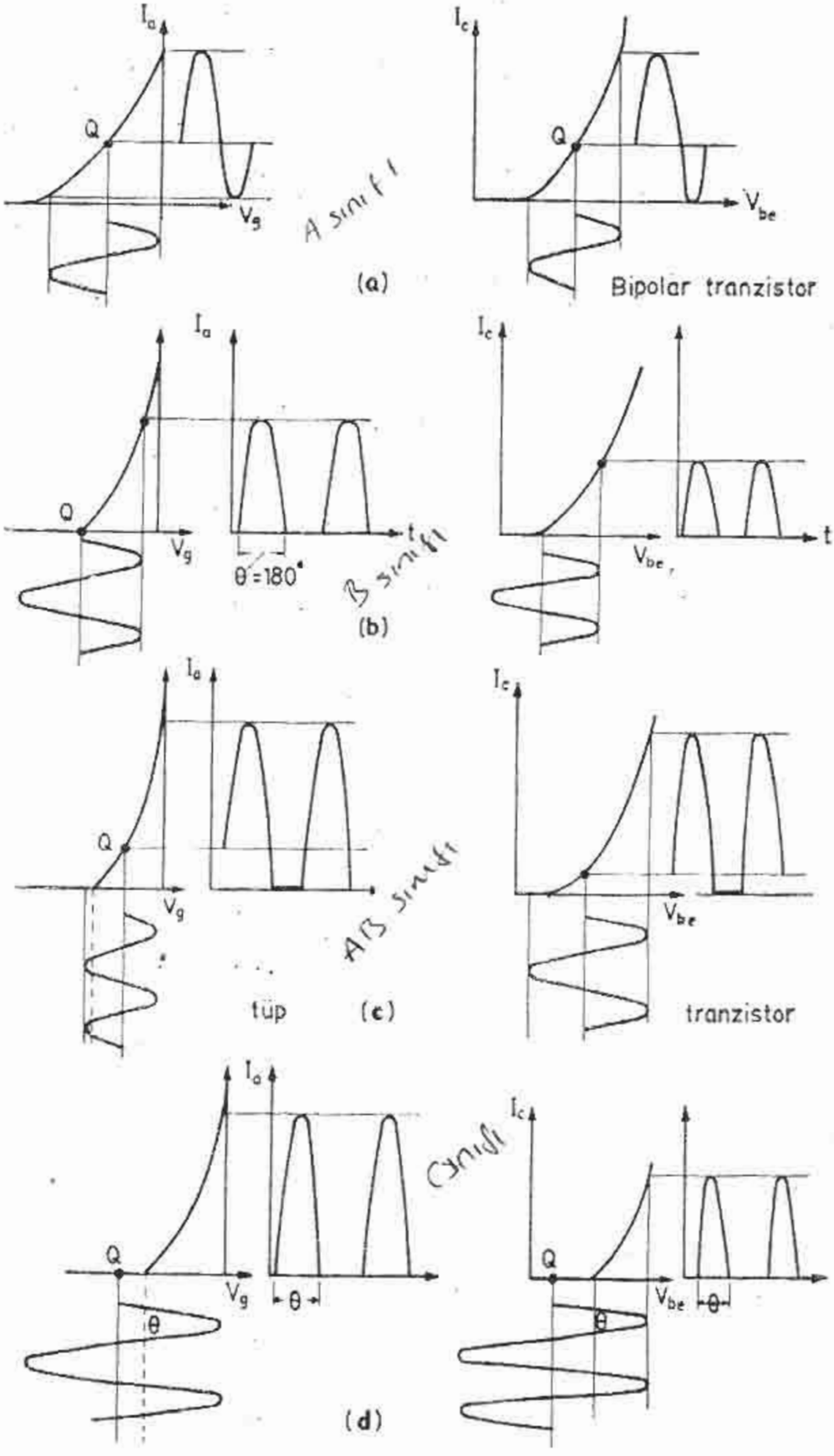


Figure 17.14 Complex plane showing typical gain-phase points.

POWER AMPLIFIERS.

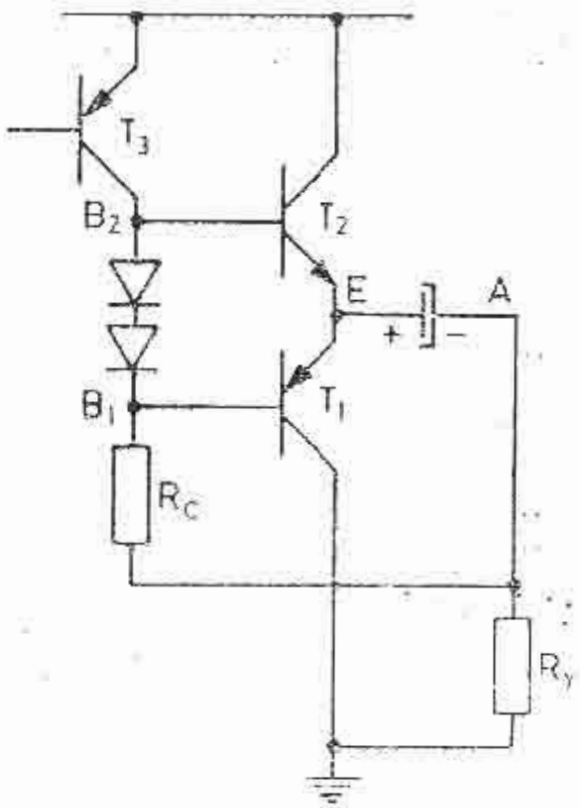
EEM 311

GÜÇ KUVVETLENDİRİCİLERİ



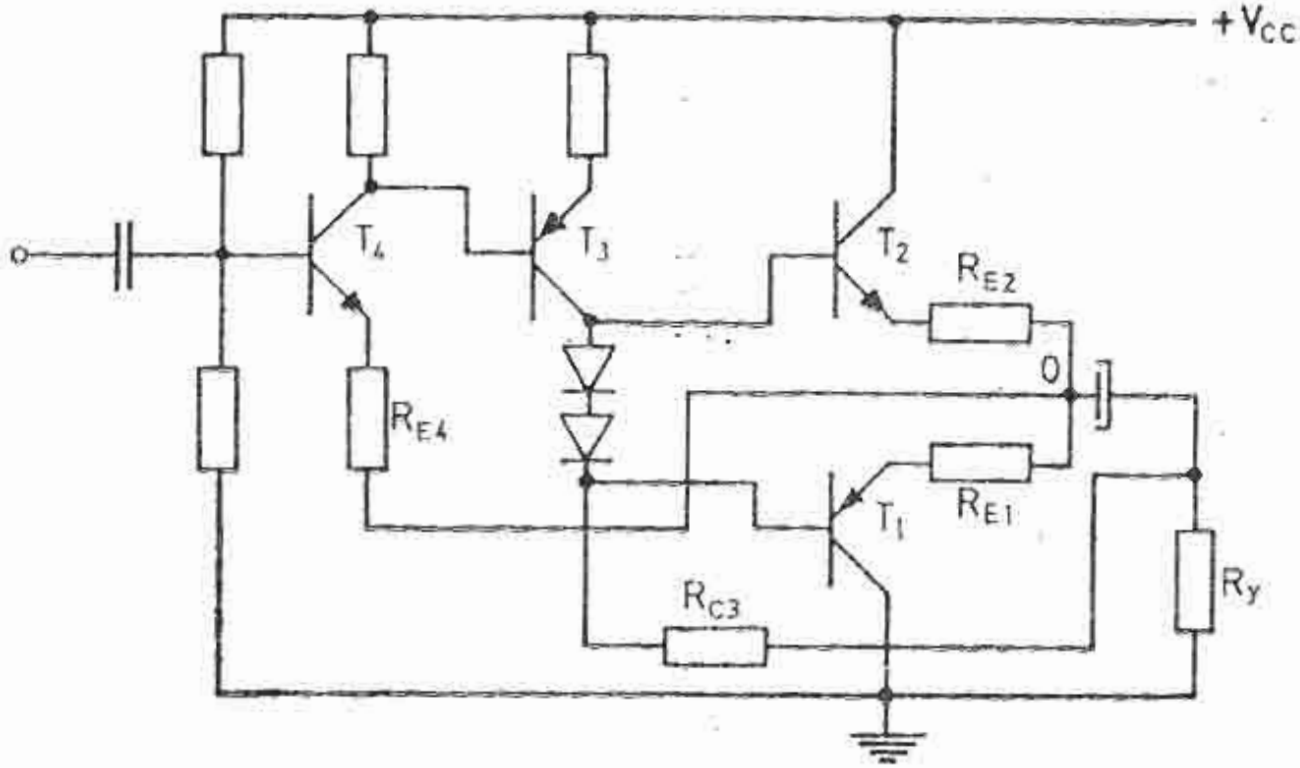
Şekil 8.1. Tüplü ve tranzistorlu kuvvetlendiricilerde çalışma sınıfları.
(a) A sınıfı, (b) B sınıfı, (c) AB sınıfı, (d) C sınıfı.

girer, T_1 in akımı artar. T_1 in gerilim kazancı yaklaşık olarak 1'e eşit olduğundan A noktasının gerilimi v_{B1}'i izler ve bu yüzden R_c üzerindeki değişken gerilim düşümü yaklaşık olarak sıfır olur. Böylece yukarda anlatılmış olan sınırlama etkisi ortadan kalkar. Negatif yarıperyotta T_3'ün akımı artar; B_2 noktasının gerilimi yükselir. T_2 iletime T_1 kesime girer. T_3'ün yükü Şekil 8.25. deki devrede T_2'nin girişi ile diyotlar ve R_c'nin oluşturduğu kolun paralel eşdeğeridir. Şekil 8.26. daki devrede ise $v_{B1} \approx v_A$ olduğundan diyotlar ve R_c üzerinden akan akım çok küçüktür. Böylece T_3'ün yükü önemli ölçüde azalmış olur. Şekil 8.26. daki devreye *sürüklemeli devre* («bootstrap» devresi) denir ve transformatörsüz çıkış katlarında sürülme problemini önemli ölçüde kolaylaştırdığından çok kullanılır.



Şekil 8.26. Eşlenik tranzistorlu çıkış katının «bootstrap» düzeni kullanılarak sürülmesi.

B sınıfı transformatörsüz bir çıkış katında çıkış işaretinin iki yöne doğru değişim alanının eşit olabilmesi için yükün üst ucunun sükûnet geriliminin, V_{CC}'nin tam yarısına eşit olması gerekir. Bu eşitliğin sağlanması yalnızca kullanılan tranzistorların özeliklerinin benzerliğine bırakılmaz ve genellikle Şekil 8.27 deki gibi bir doğru akım geribeslemesi düzeninden yararlanılır. Devrede T_3 sürücü tranzistorunun önündeki gerilim kuvvetlendirme katının (T_4'ün) emetör direncinin alt ucu 0 noktasına (orta noktaya) bağlanmış ve T_4'ün baz bölücü dirençleri, sükûnetteki



Şekil 8.27. Doğru akım geribeslemesi ile orta noktasının kararlılığı sağlamış olan bir B sınıfı kuvvetlendirici.

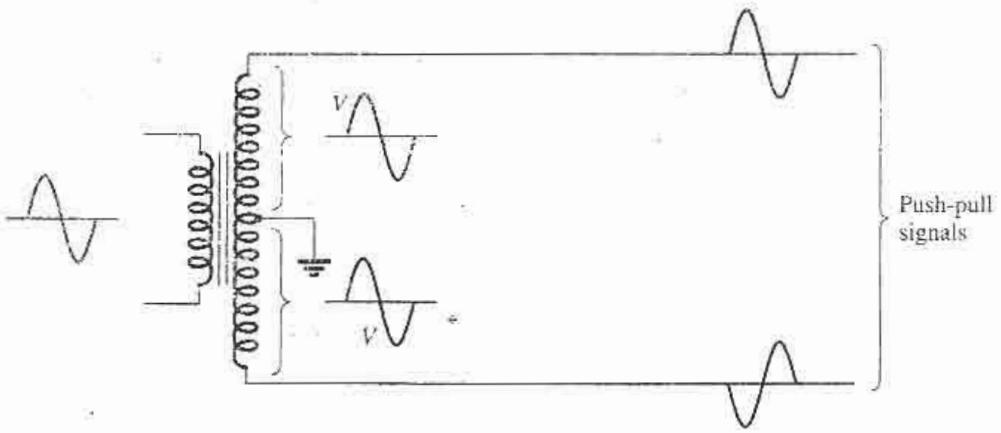
emetör gerilimi $V_{E4}=(V_{CC}/2)+R_{E4}\cdot I_{EQ4}$ olacak şekilde hesaplanmıştır. Çıkıştaki T_1 ve T_2 tranzistorları arasındaki gerilim bölüşümü herhangi bir nedenle bozulsa (örneğin 0 noktasının gerilimi olması gereken $V_{CC}/2$ değerinden daha küçük bir değere düşse), bunun sonucunda T_4'ün akımı artacak, T_3'ün bazının gerilimi düşeceğinden (baz-emetör gerilimi yükseleceğinden) akımı artacak ve T_2'nin bazının bağlı olduğu B_2 noktasının gerilimi yükselecektir. T_2'nin emetör gerilimi baz gerilimini —aşağı yukarı sabit bir farkla— izleyeceğinden T_2'nin emetör gerilimi (yani 0 orta noktasının gerilimi) artacaktır. Orta nokta geriliminde meydana geldiğini varsaydığımız bir değişmenin bu şekilde kendi kendini karşılayan (kompanze eden) bir etki doğurması, çıkış tranzistorları arasındaki gerilim bölüşümünün devamlı olarak kontrol edilmesi ve herhangi bir sebepten meydana gelebilecek dengesizliklerin otomatik olarak giderilmesi demektir.

Devreye R_{C3} direnci yardımı ile sürüklenme uygulanmıştır. Ayrıca görüldüğü gibi T_1 ve T_2 çıkış tranzistorlarının emetörlerine birer direnç bağlanmıştır. Çıkış tranzistorlarının ısıl kararlılığına yardımcı olmak üzere konulmuş olan bu dirençler —çıkış gücünün çok düşmemesi için— küçük değerli seçilirler. Pratikte bu dirençleri, tranzistordan maksimum akım akarken direncin uçlarında V_{CC} nin 1/10'undan daha küçük bir gerilim düşecek şekilde seçmek uygun olur.

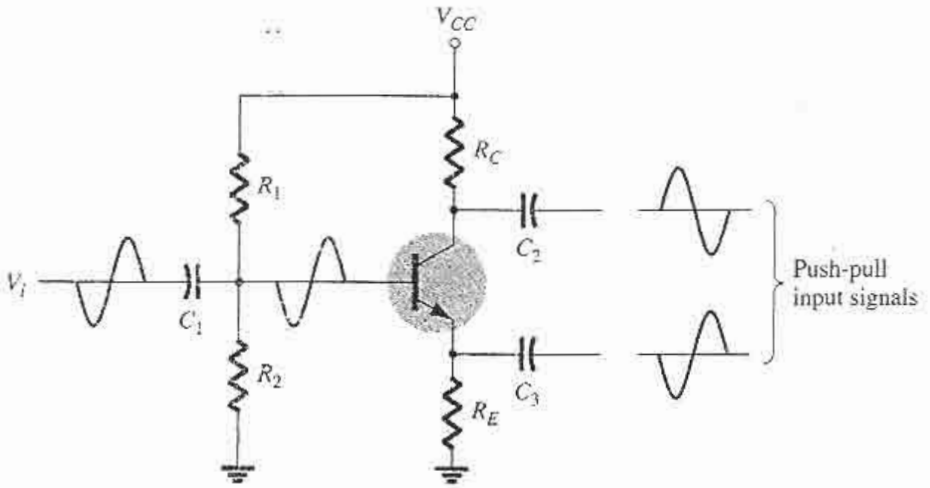
P_L

circuit then providing two different output stages, each operating for one-half the cycle. If the input is in the form of two opposite polarity signals, two similar stages could be used, each operating on the alternate cycle because of the input signal. One means of obtaining polarity or phase inversion is using a transformer, the transformer-coupled amplifier having been very popular for a long time. Opposite polarity inputs can easily be obtained using an op-amp having two opposite outputs or using a few op-amp stages to obtain two opposite polarity signals. An opposite polarity operation can also be achieved using a single input and complementary transistors (*npn* and *pnp*, or *n*MOS and *p*MOS).

Figure 15.14 shows different ways to obtain phase-inverted signals from a single input signal. Figure 15.14a shows a center-tapped transformer to provide opposite



(a)



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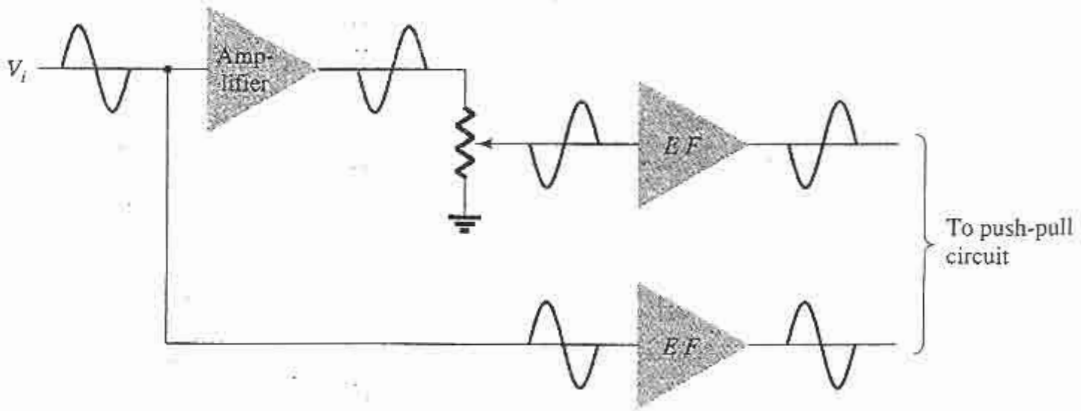


(c)

Figure 15.14 Phase-splitter circuits.

phase signals. If the transformer is exactly center-tapped, the two signals are exactly opposite in phase and of the same magnitude. The circuit of Fig. 15.14b uses a BJT stage with in-phase output from the emitter and opposite phase output from the collector. If the gain is made nearly 1 for each output, the same magnitude results. Probably most common would be using op-amp stages, one to provide an inverting gain of unity and the other a noninverting gain of unity, to provide two outputs of the same magnitude but of opposite phase.

Transformer-Coupled Push–Pull Circuits

The circuit of Fig. 15.15 uses a center-tapped input transformer to produce opposite polarity signals to the two transistor inputs and an output transformer to drive the load in a push-pull mode of operation described next.

During the first half-cycle of operation, transistor Q_1 is driven into conduction whereas transistor Q_2 is driven off. The current I_1 through the transformer results in the first half-cycle of signal to the load. During the second half-cycle of the input signal, Q_2 conducts whereas Q_1 stays off, the current I_2 through the transformer resulting in the second half-cycle to the load. The overall signal developed across the load then varies over the full cycle of signal operation.

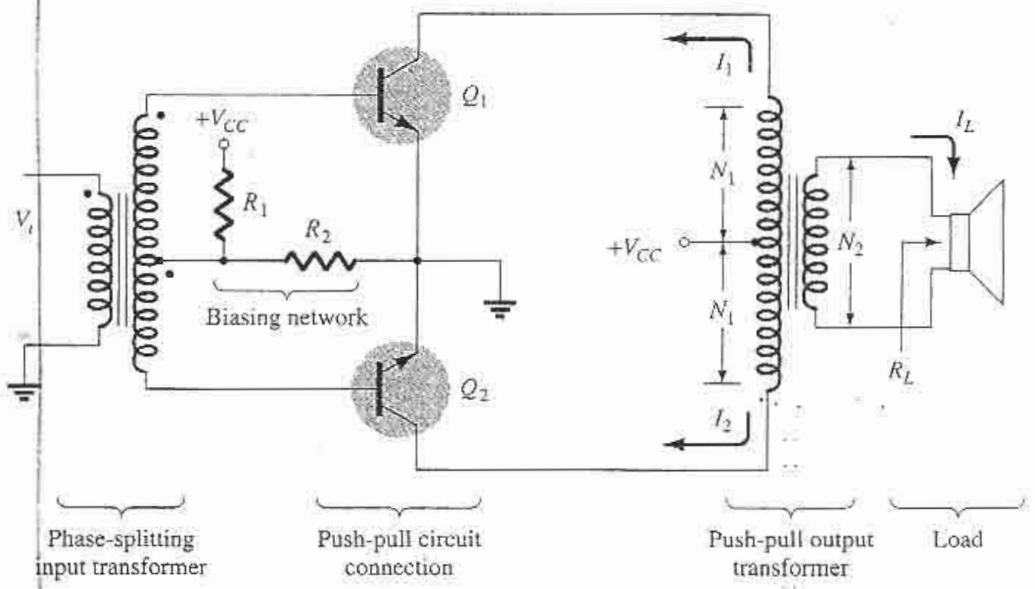


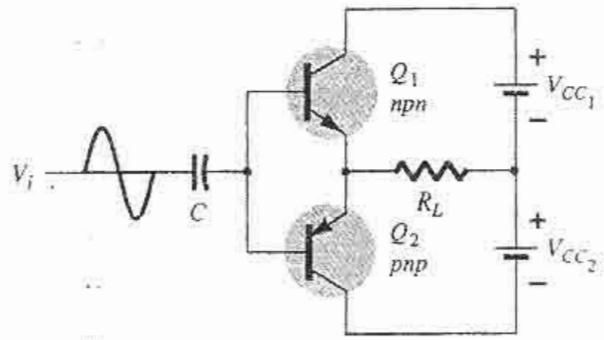
Figure 15.15 Push-pull circuit

Complementary-Symmetry Circuits

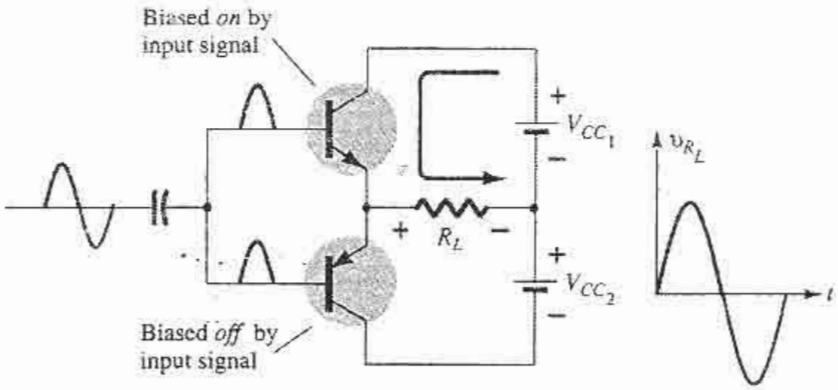
Using complementary transistors (*npn* and *pnp*) it is possible to obtain a full cycle output across a load using half-cycles of operation from each transistor, as shown in Fig. 15.16a. While a single input signal is applied to the base of both transistors, the transistors, being of opposite type, will conduct on opposite half-cycles of the input. The *npn* transistor will be biased into conduction by the positive half-cycle of signal, with a resulting half-cycle of signal across the load as shown in Fig. 15.16b. During the negative half-cycle of signal, the *pnp* transistor is biased into conduction when the input goes negative, as shown in Fig. 15.16c.

During a complete cycle of the input, a complete cycle of output signal is developed across the load. One disadvantage of the circuit is the need for two separate voltage supplies. Another, less obvious disadvantage with the complementary circuit is shown in the resulting crossover distortion in the output signal (see Fig. 15.16d). *Crossover distortion* refers to the fact that during the signal crossover from positive to negative (or vice versa) there is some nonlinearity in the output signal. This results from the fact that the circuit does not provide exact switching of one transistor off and the other on at the zero-voltage condition. Both transistors may be partially off

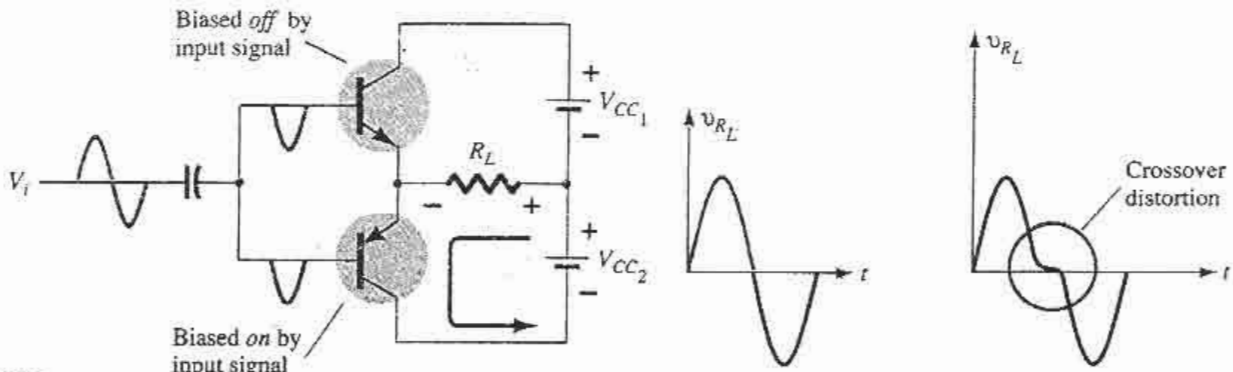
P_L



(a)



(b)



(c) (d)

Figure 15.16 Complementary-symmetry push-pull circuit.

so that the output voltage does not follow the input around the zero-voltage condition. Biasing the transistors in class AB improves this operation by biasing both transistors to be on for more than half a cycle.

A more practical version of a push-pull circuit using complementary transistors is shown in Fig. 15.17. Note that the load is driven as the output of an emitter-follower so that the load resistance of the load is matched by the low output resistance of the driving source. The circuit uses complementary Darlington-connected transistors to provide higher output current and lower output resistance.

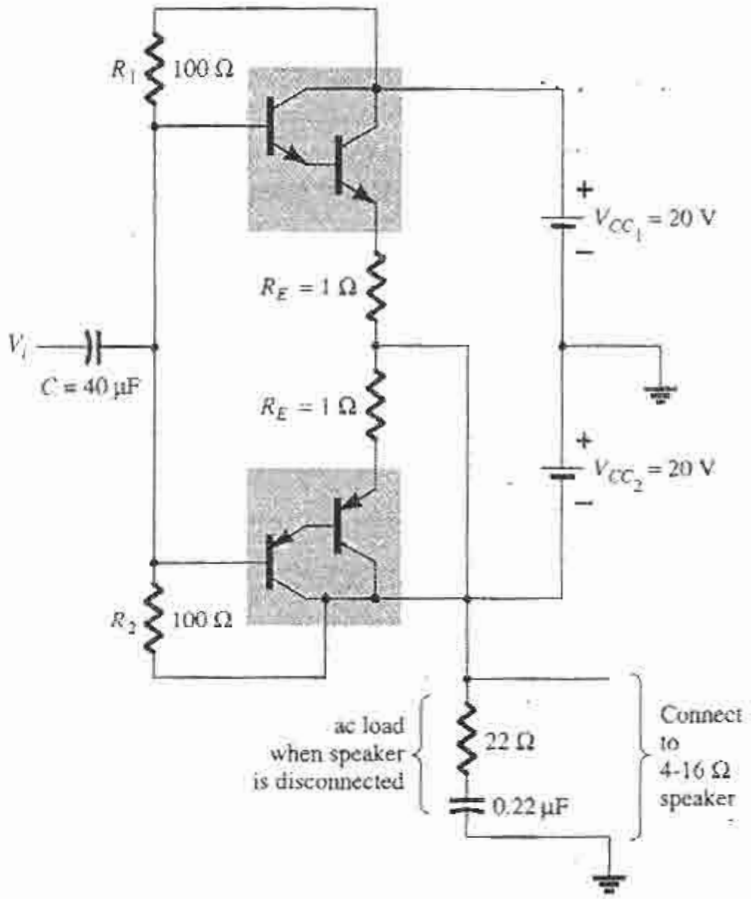


Figure 15.17 Complementary-symmetry push-pull circuit using Darlington transistors.

Quasi-Complementary Push–Pull Amplifier

In practical power amplifier circuits, it is preferable to use *npn* transistors for both high-current-output devices. Since the push-pull connection requires complementary devices, a *pnp* high-power transistor must be used. A practical means of obtaining complementary operation while using the same, matched *npn* transistors for the output is provided by a quasi-complementary circuit, as shown in Fig. 15.18. The push-pull op-

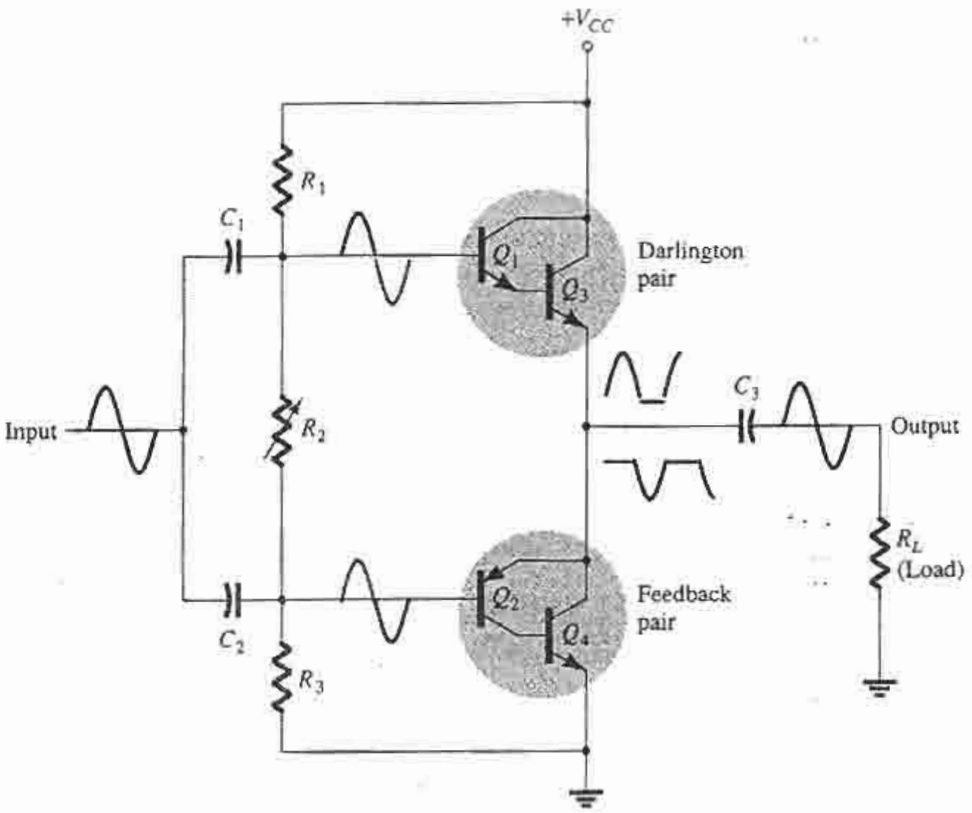


Figure 15.18 Quasi-complementary push-pull transformerless power amplifier.

P_L

eration is achieved by using complementary transistors (Q_1 and Q_2) before the matched *npn* output transistors (Q_3 and Q_4). Notice that transistors Q_1 and Q_3 form a Darlington connection that provides output from a low-impedance emitter-follower. The connection of transistors Q_2 and Q_4 forms a feedback pair, which similarly provides a low-impedance drive to the load. Resistor R_2 can be adjusted to minimize crossover distortion by adjusting the dc bias condition. The single input signal applied to the push-pull stage then results in a full cycle output to the load. The quasi-complementary push-pull amplifier is presently the most popular form of power amplifier.

EXAMPLE 15.10

For the circuit of Fig. 15.19, calculate the input power, output power, and power handled by each output transistor and the circuit efficiency for an input of 12 V rms.

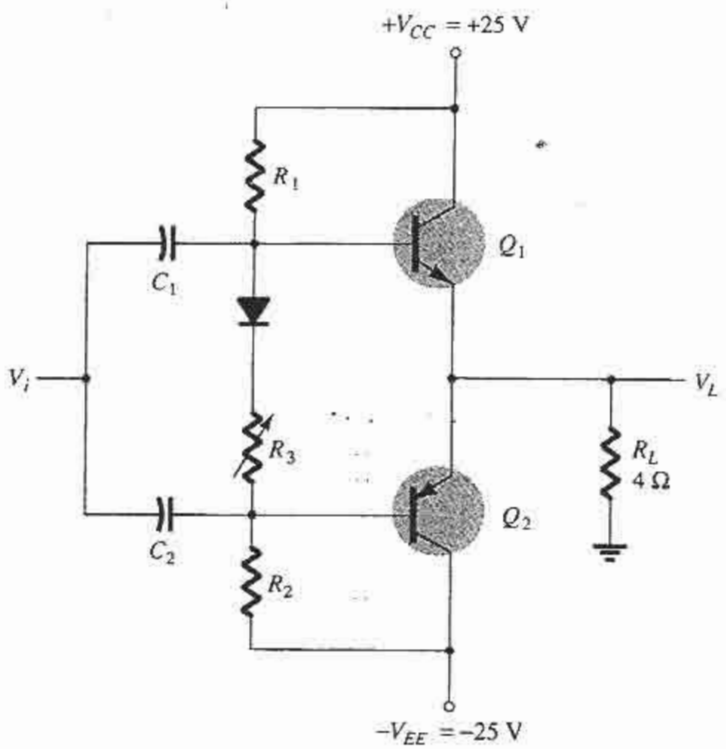


Figure 15.19 Class B power amplifier for Examples 15.10–15.12.

Solution

The peak input voltage is

$$V_i(\text{p}) = \sqrt{2}\, V_i\,(\text{rms}) = \sqrt{2}\,(12\text{ V}) = 16.97\text{ V} \approx 17\text{ V}$$

Since the resulting voltage across the load is ideally the same as the input signal (the amplifier has, ideally, a voltage gain of unity),

$$V_L(\text{p}) = 17\text{ V}$$

and the output power developed across the load is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(17\text{ V})^2}{2(4\ \Omega)} = \mathbf{36.125\ W}$$

The peak load current is

$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{17\text{ V}}{4\ \Omega} = 4.25\text{ A}$$

from which the dc current from the supplies is calculated to be

$$I_{\text{dc}} = \frac{2}{\pi} I_L(\text{p}) = \frac{2(4.25\text{ A})}{\pi} = 2.71\text{ A}$$

so that the power supplied to the circuit is

$$P_i(\text{dc}) = V_{CC}I_{dc} = (25\text{ V})(2.71\text{ A}) = \mathbf{67.75\text{ W}}$$

The power dissipated by each output transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{P_i - P_o}{2} = \frac{67.75\text{ W} - 36.125\text{ W}}{2} = \mathbf{15.8\text{ W}}$$

The circuit efficiency (for the input of 12 V, rms) is then

$$\%\,\eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125\text{ W}}{67.75\text{ W}} \times 100\% = \mathbf{53.3\%}$$

EXAMPLE 15.11

For the circuit of Fig. 15.19, calculate the maximum input power, maximum output power, input voltage for maximum power operation, and the power dissipated by the output transistors at this voltage.

Solution

The maximum input power is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi R_L} = \frac{2(25\text{ V})^2}{\pi 4\,\Omega} = \mathbf{99.47\text{ W}}$$

The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(25\text{ V})^2}{2(4\,\Omega)} = \mathbf{78.125\text{ W}}$$

[Note that the maximum efficiency is achieved:]

$$\%\,\eta = \frac{P_o}{P_i} \times 100\% = \frac{78.125\text{ W}}{99.47\text{ W}}100\% = 78.54\%$$

To achieve maximum power operation the output voltage must be

$$V_L(\text{p}) = V_{CC} = 25\text{ V}$$

and the power dissipated by the output transistors is then

$$P_{2Q} = P_i - P_o - 99.47\text{ W} - 78.125\text{ W} = \mathbf{21.3\text{ W}}$$

EXAMPLE 15.12

For the circuit of Fig. 15.19, determine the maximum power dissipated by the output transistors and the input voltage at which this occurs.

Solution

The maximum power dissipated by both output transistors is

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} = \frac{2(25\text{ V})^2}{\pi^2 4\,\Omega} = \mathbf{31.66\text{ W}}$$

This maximum dissipation occurs at

$$V_L = 0.636V_L(\text{p}) = 0.636(25\text{ V}) = \mathbf{15.9\text{ V}}$$

Notice that at $V_L = 15.9$ V the circuit required the output transistors to dissipate 31.66 W, while at $V_L = 25$ V they only had to dissipate 21.3 W.)
