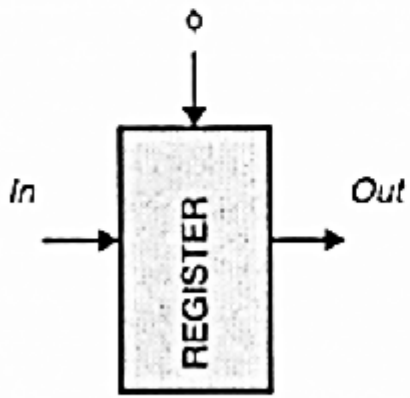
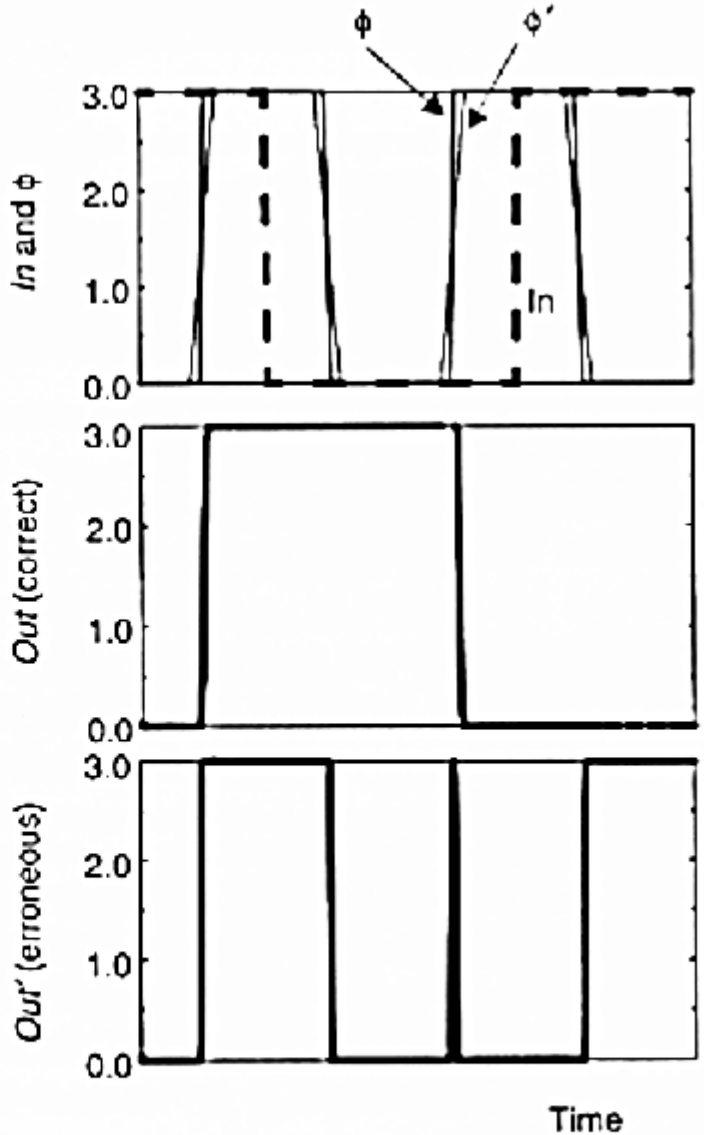
(a) Ideal clock waveform

(b) More realistic clock waveform

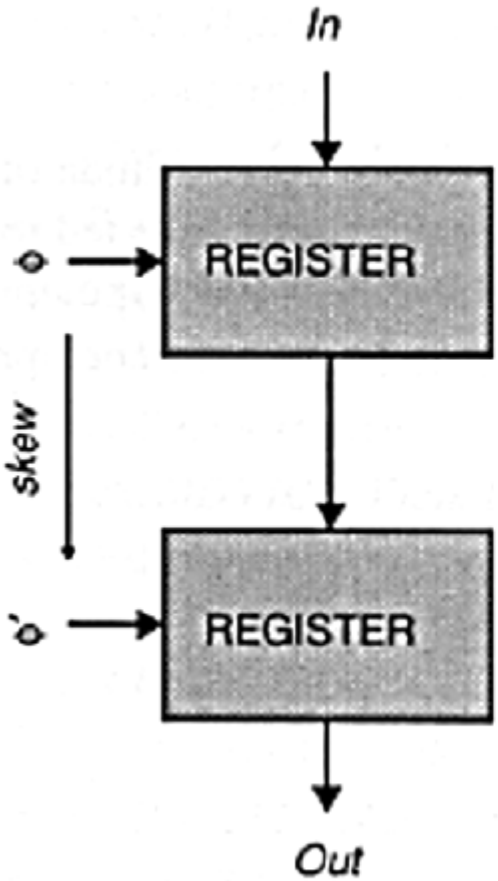


(c) Register module and its connections

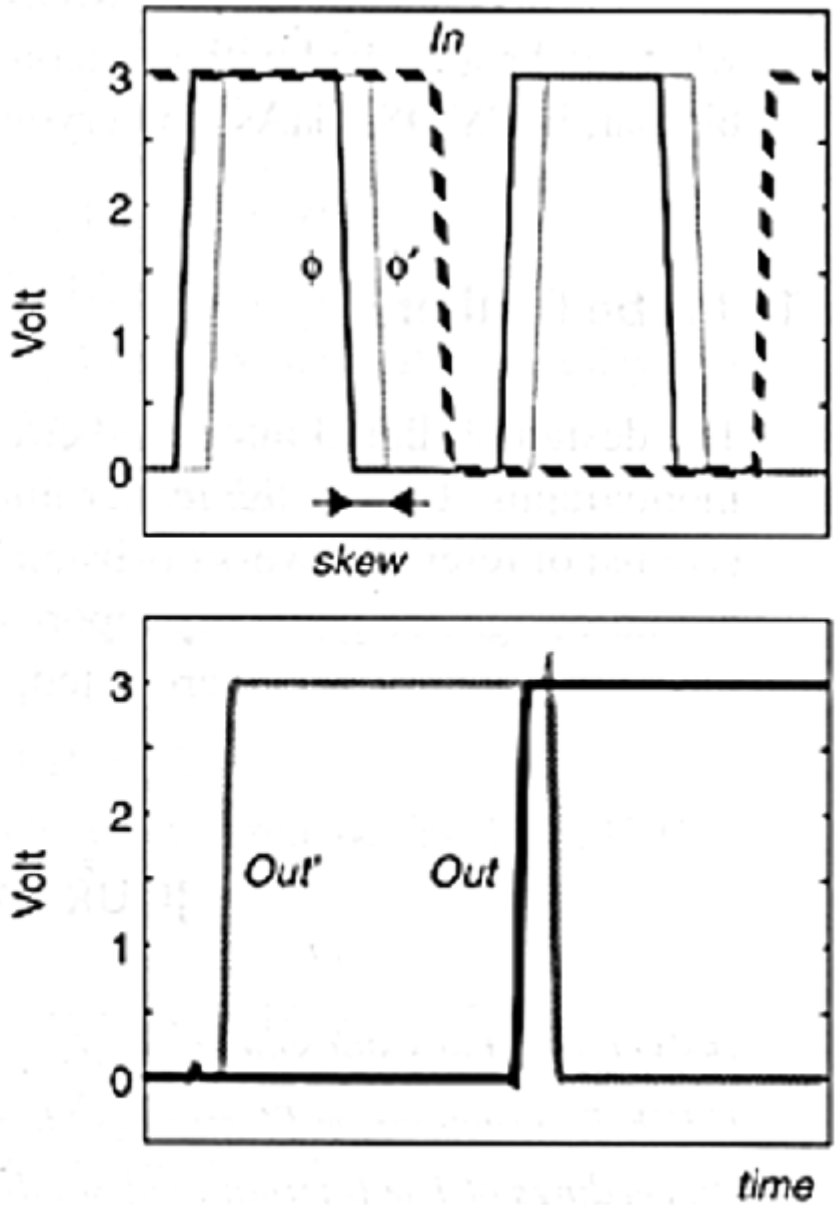


(d) Simulated waveforms

Figure 1.6 Reduced clock slopes can cause a register circuit to fail.

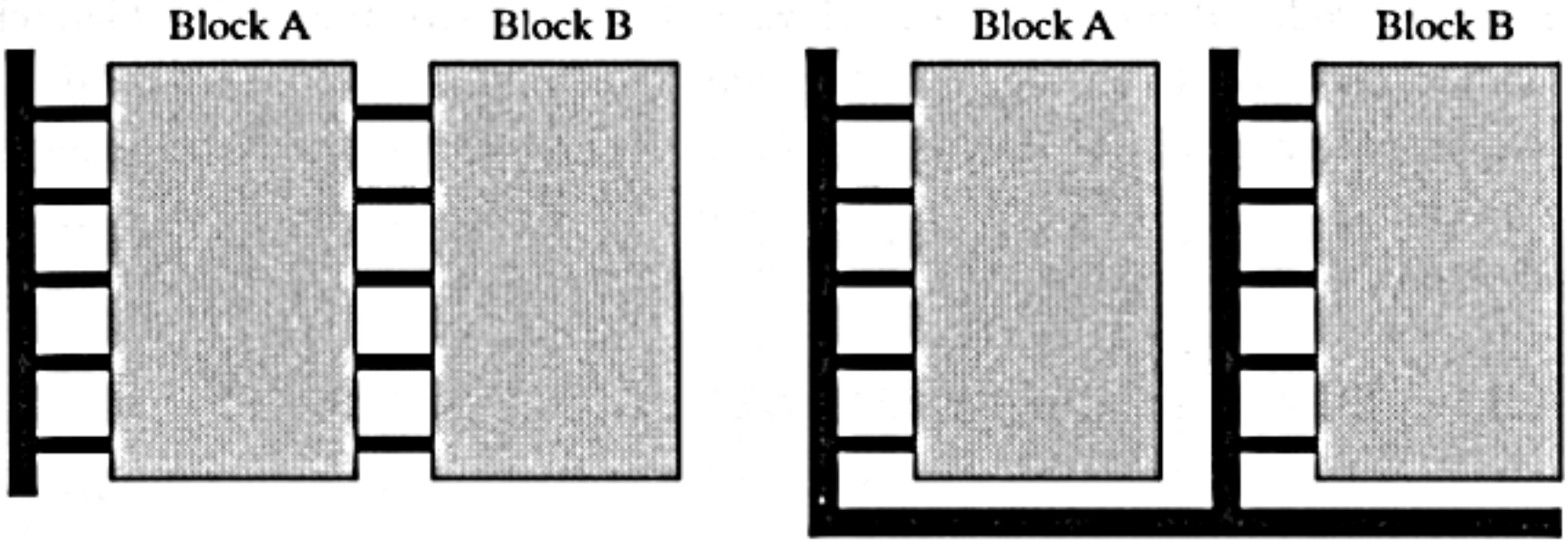


(a) Two cascaded registers



(b) Simulated waveforms

Figure 1.7 Impact of clock misalignment.



(a) Routing through the block

(b) Routing around the block

For a current of 100 A, a wire resistance of 1.25 mΩ leads to a 5% drop in supply voltage (2.5 V supply)! On the other hand, current demand can change from zero to this peak value within 1nsec which leads to a current variation of 100GA/sec!

Fundamental Design Metrics

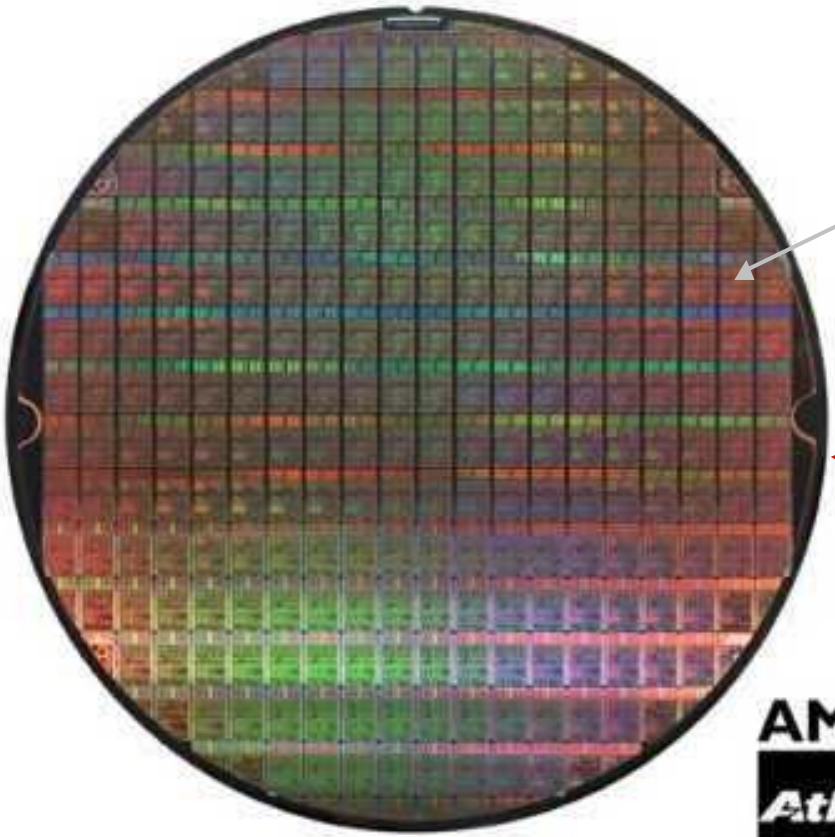
- Functionality
- Scalability
- Cost
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test
- Reliability, robustness
  - Noise margins
  - Noise immunity
- Performance
  - Speed (delay)
  - Power consumption; energy
- Time-to-market

Cost of Integrated Circuits

- NRE (non-recurring engineering) costs
  - Fixed cost to produce the design
    - design effort
    - design verification effort
    - mask generation
  - Influenced by the design complexity and designer productivity
  - More pronounced for small volume products
- Recurring costs – proportional to product volume
  - silicon processing (also proportional to chip area)
  - Parts
  - assembly (packaging)
  - test

$$\text{cost per IC} = \text{variable cost per IC} + \frac{\text{fixed cost}}{\text{volume}}$$

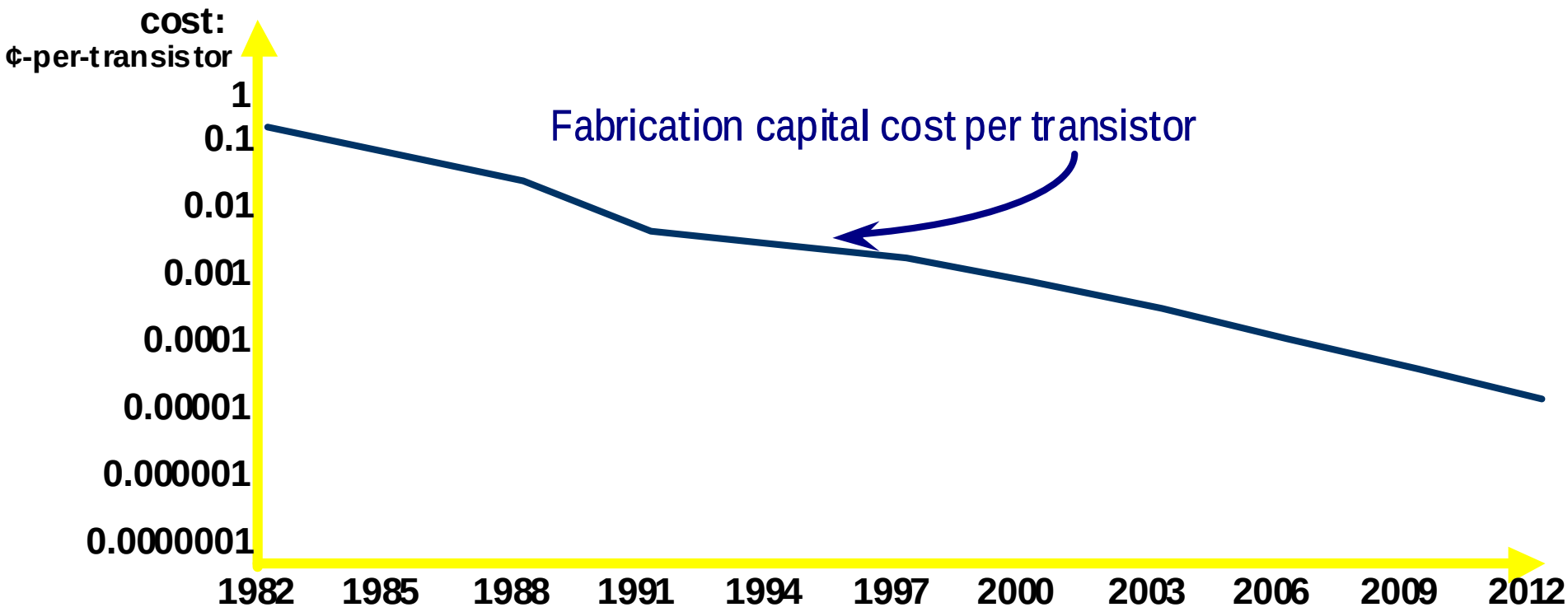
Die Cost



Going up to 12" (30cm)

From http://www.amd.com

Cost per Transistor

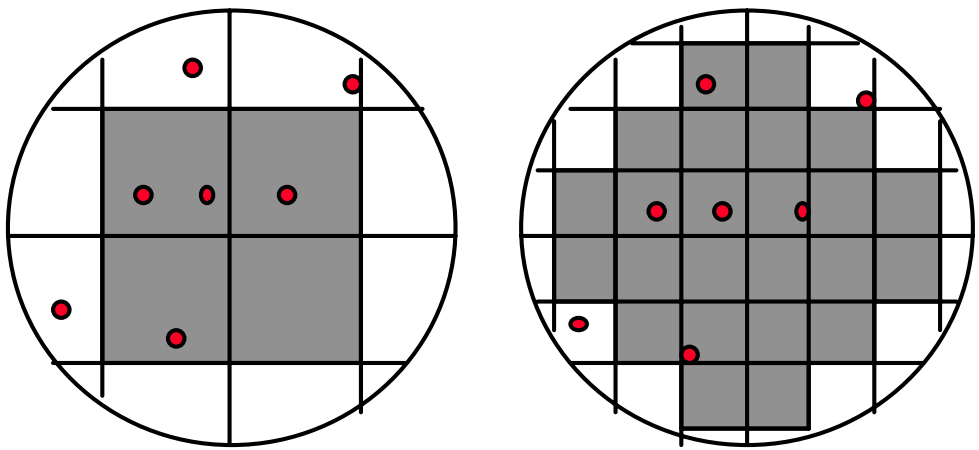


Recurring Costs

$$\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}$$

$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}$$

$$\text{dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$



$$\text{die yield} = (1 + (\text{defects per unit area} \times \text{die area})/\alpha)^{-\alpha}$$

die yield (%) = No. of good chips per wafer x 100 / Total number of chips per wafer

α is a parameter that depends upon the complexity of the manufacturing process and is roughly proportional to the number of masks.

$\alpha = 3$ (a good estimate for today's complex CMOS processes)

A value between 0.5 - 1 defects per cm^2 is typical these days.

$$\text{die cost} = f(\text{die area})^4$$

- Smaller gate → higher integration density → smaller die size
- Smaller gate → faster
  - less energy
  - less gate capacitance

Yield Example

- Example
  - wafer size of 12 inches, die size of 2.5 cm^2, 1 defects/cm^2, $\alpha = 3$ (measure of manufacturing process complexity)
  - 252 dies/wafer (remember, wafers round & dies square)
  - die yield of 16%
  - 252 x 16% = only 40 dies/wafer die yield !

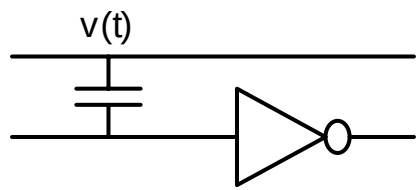
Examples of Cost Metrics (1994)

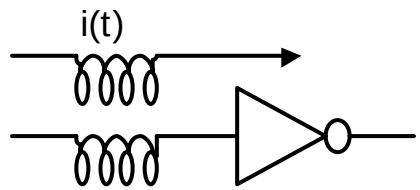
Chip	Metal layers	Line width	Wafer cost	Defects /cm^2	Area (mm^2)	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486DX2	3	0.80	$1200	1.0	81	181	54%	$12
PowerPC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super SPARC	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Reliability

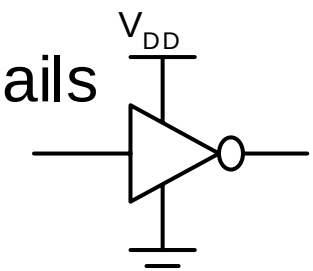
Noise in Digital Integrated Circuits

- Noise – unwanted variations of voltages and currents at the logic nodes
- from two wires placed side by side
  - capacitive coupling
    - voltage change on one wire can influence signal on the neighboring wire
    - cross talk
  - inductive coupling
    - current change on one wire can influence signal on the neighboring wire





- from noise on the power and ground supply rails
  - can influence signal levels in the gate



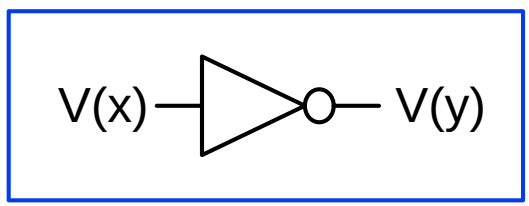
Static Gate Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.
- Digital circuits perform operations on Boolean variables

$$x \in \{0,1\}$$

- A logical variable is associated with a *nominal voltage level* for each logic state

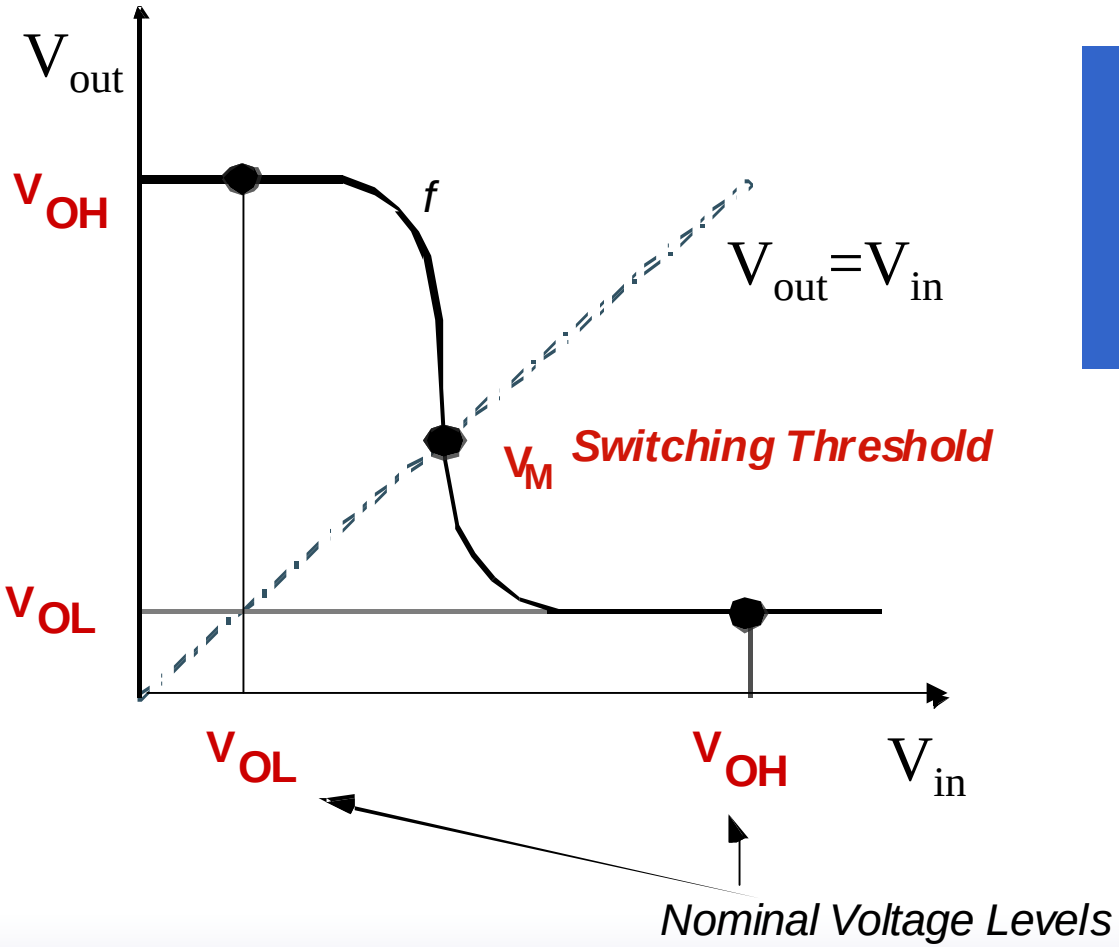
$$1 \Leftrightarrow V_{OH} \text{ and } 0 \Leftrightarrow V_{OL}$$



$$V_{OH} = (\overline{V_{OL}})$$
$$V_{OL} = (\overline{V_{OH}})$$

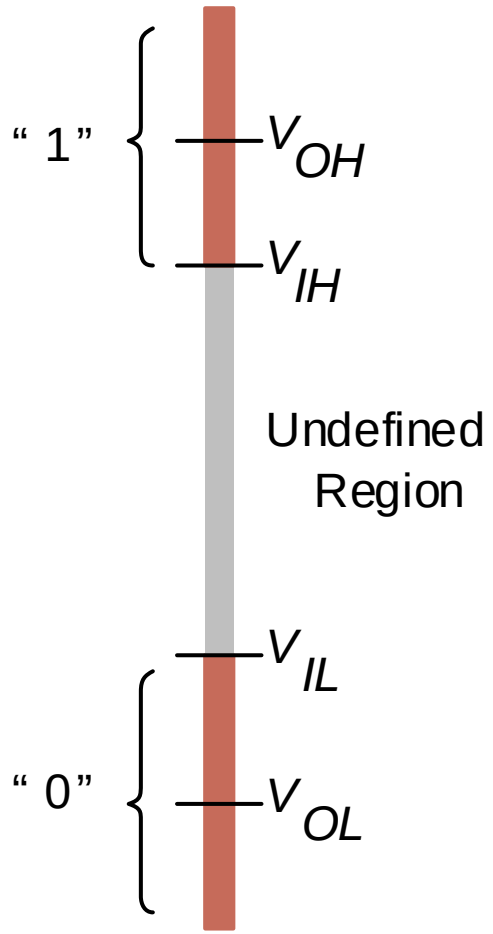
- Difference between V_{OH} and V_{OL} is the logic or *signal swing* V_{sw}

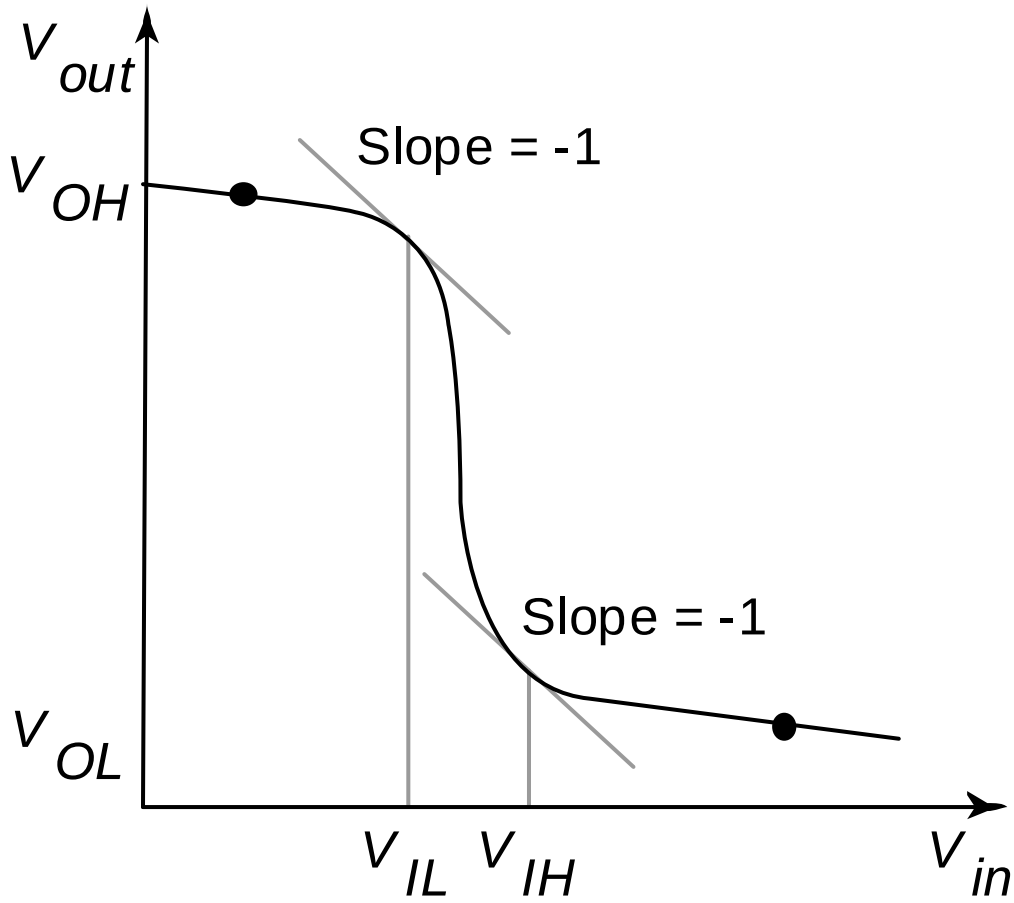
DC Operation
Voltage Transfer Characteristic



VOH = *f*(VOL)
VOL = *f*(VOH)
VM = *f*(VM)

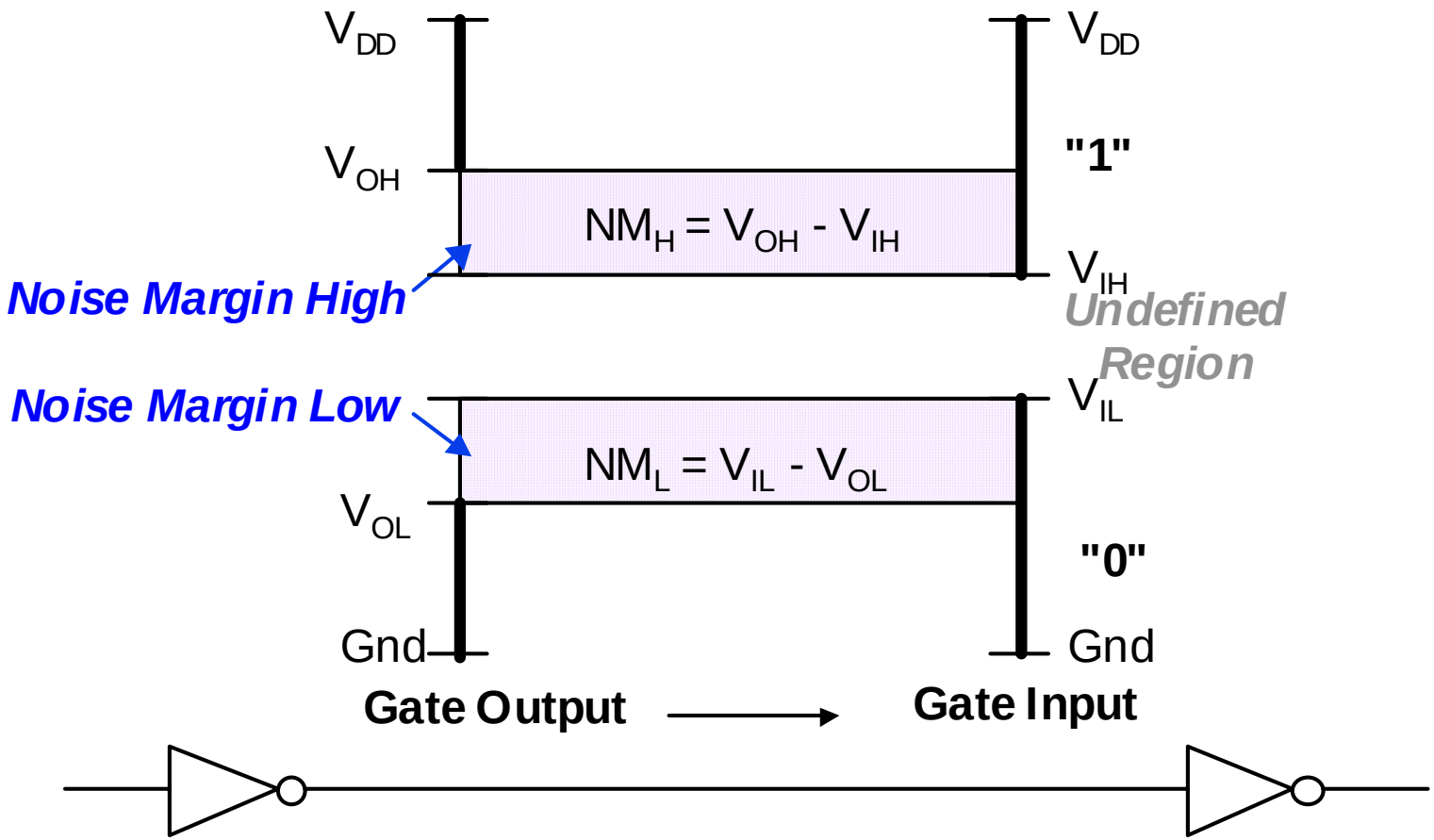
Mapping between analog and digital signals





Noise Margins

- For robust circuits, want the “0” and “1” intervals to be as large as possible



- Large noise margins are desirable, but not sufficient …

Noise Immunity

- Noise margin expresses the ability of a circuit to overpower a noise source
  - noise sources: supply noise, cross talk, interference, offset
- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- *Noise immunity* expresses the ability of the system to process and transmit information correctly in the presence of noise (reject a noise source)
- For good noise immunity, the signal swing (i.e., the difference between V_{OH} and V_{OL}) and the noise margin have to be large enough to overpower the impact of fixed sources of noise

Assuming $V_{NM}=V_{SW}/2$

$$V_{NM} = \frac{V_{sw}}{2} \geq \sum_i f_i V_{Nfi} + \sum_j g_j V_{sw}$$

Given a set of noise sources, we can derive the minimum signal swing necessary for the system to be operational

$$V_{sw} \geq \frac{2\sum_i f_i V_{Nfi}}{1-2\sum_j g_j}$$

f = transfer function from noise to signal node

V_{Nf} = amplitude of noise (fixed) source

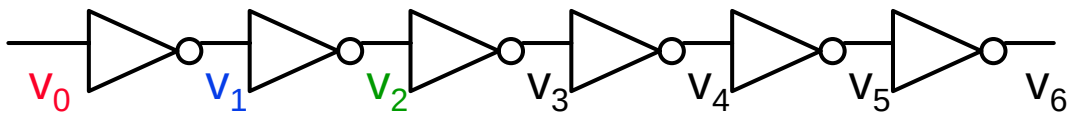
gV_{SW} = Noise proportional to the signal swing

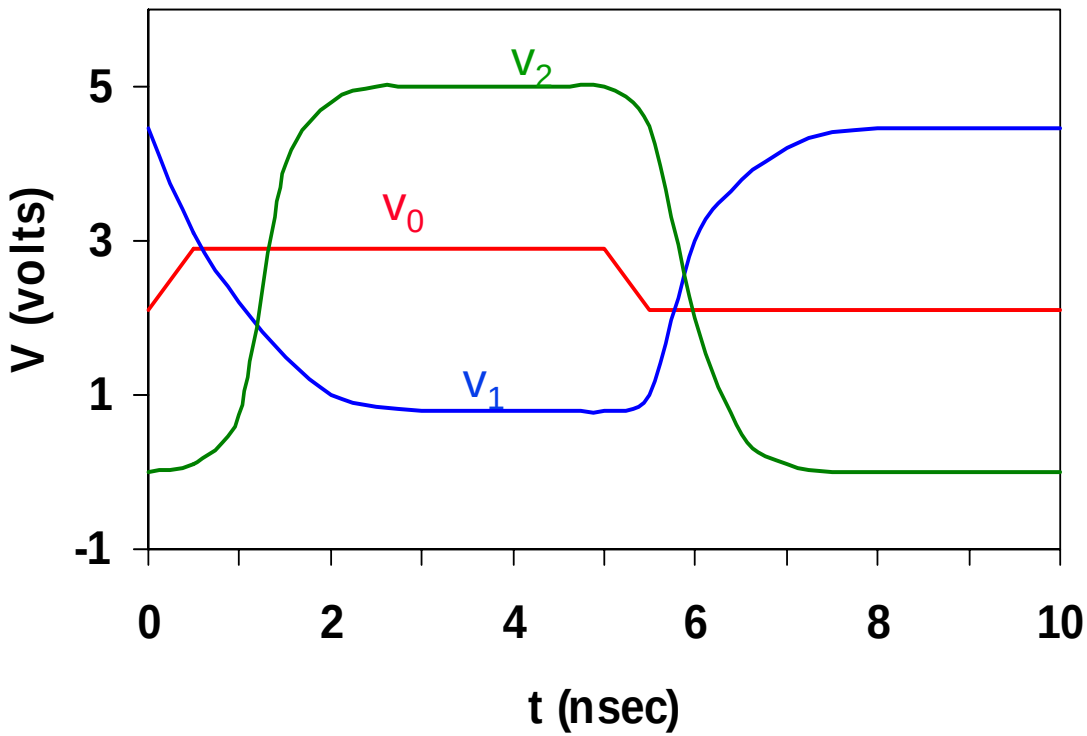
Key Metrics & Reliability Properties

- Noise immunity is the more important metric – the capability to suppress noise sources
- A gate must be *undirectional*: changes in an output level should not appear at any unchanging input of the same circuit
  - In real circuits *full* directivity is an illusion (e.g., due to capacitive coupling between inputs and outputs)
- *output impedance* of the driver and *input impedance* of the receiver
  - ideally, the output impedance of the driver should be zero
  - input impedance of the receiver should be infinity

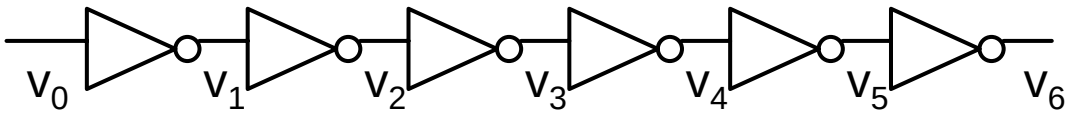
The Regenerative Property

- A gate with regenerative property ensure that a disturbed signal converges back to a nominal voltage level

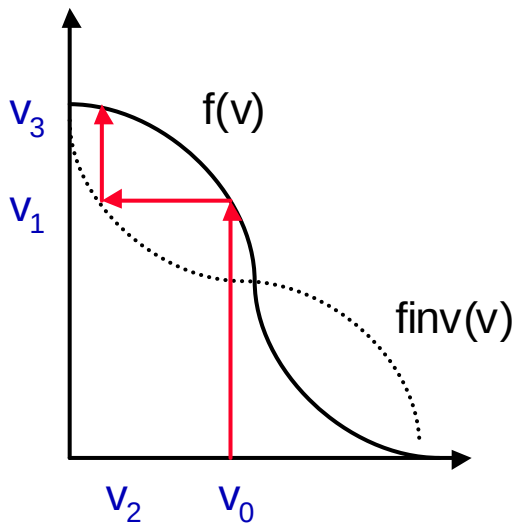




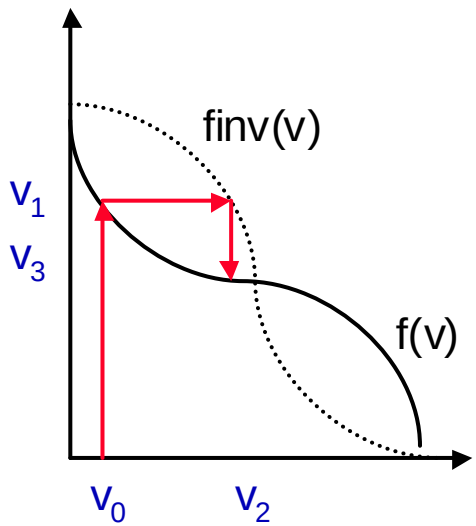
Conditions for Regeneration



$v_1 = f(v_0) \Rightarrow v_1 = finv(v_2)$



Regenerative Gate

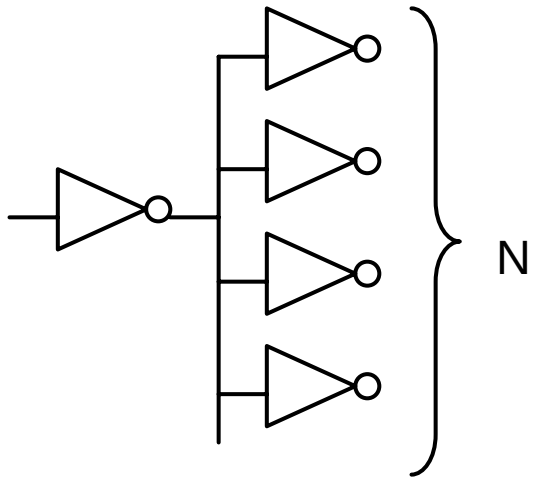


Nonregenerative Gate

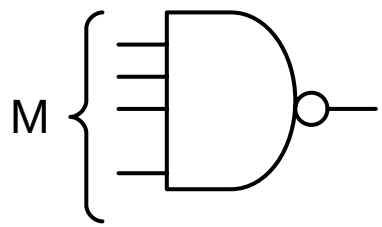
- To be regenerative, the VTC must have a transient region with a gain greater than 1 (in absolute value) bordered by two valid zones where the gain is smaller than 1. Such a gate has two stable operating points.

Fan-In and Fan-Out

- Fan-out – number of load gates connected to the output of the driving gate
  - gates with large fan-out are slower

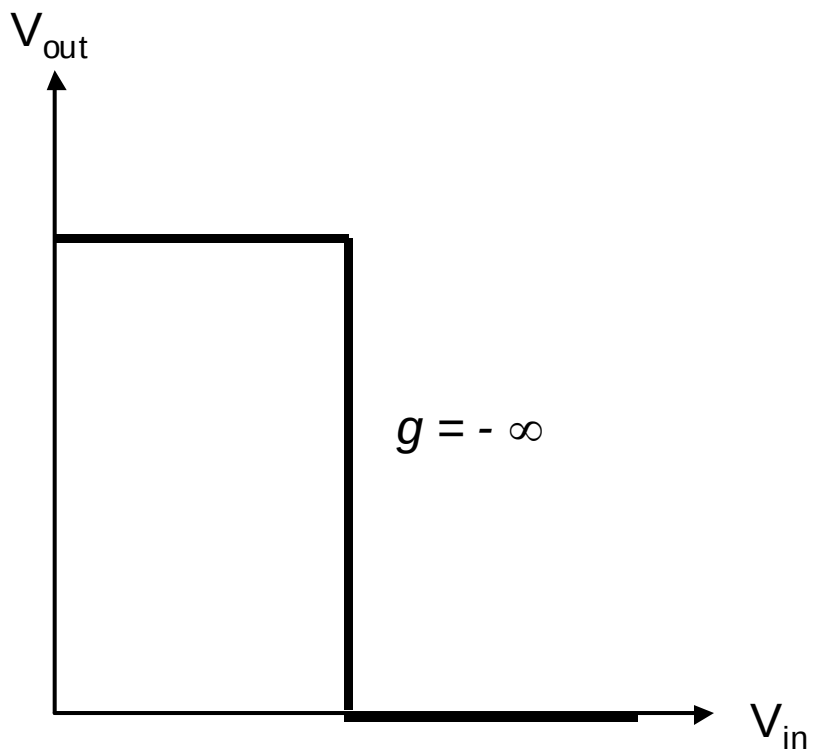


- Fan-in – the number of inputs to the gate
  - gates with large fan-in are bigger and slower



The Ideal Inverter

- The ideal gate should have
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, resp.



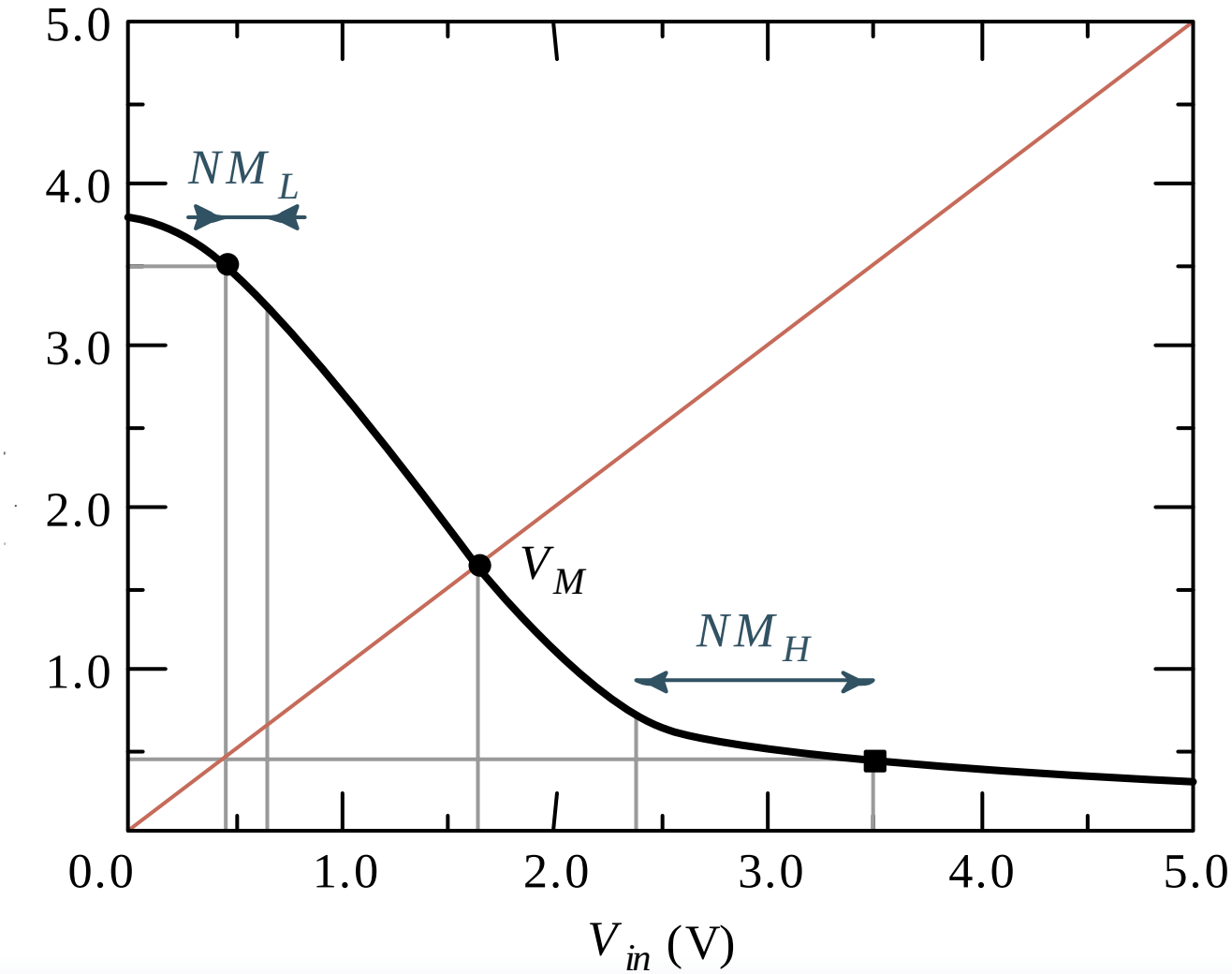
$R_i = \infty$

$R_o = 0$

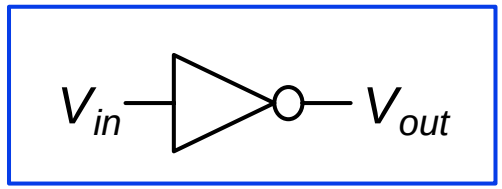
Fanout = ∞

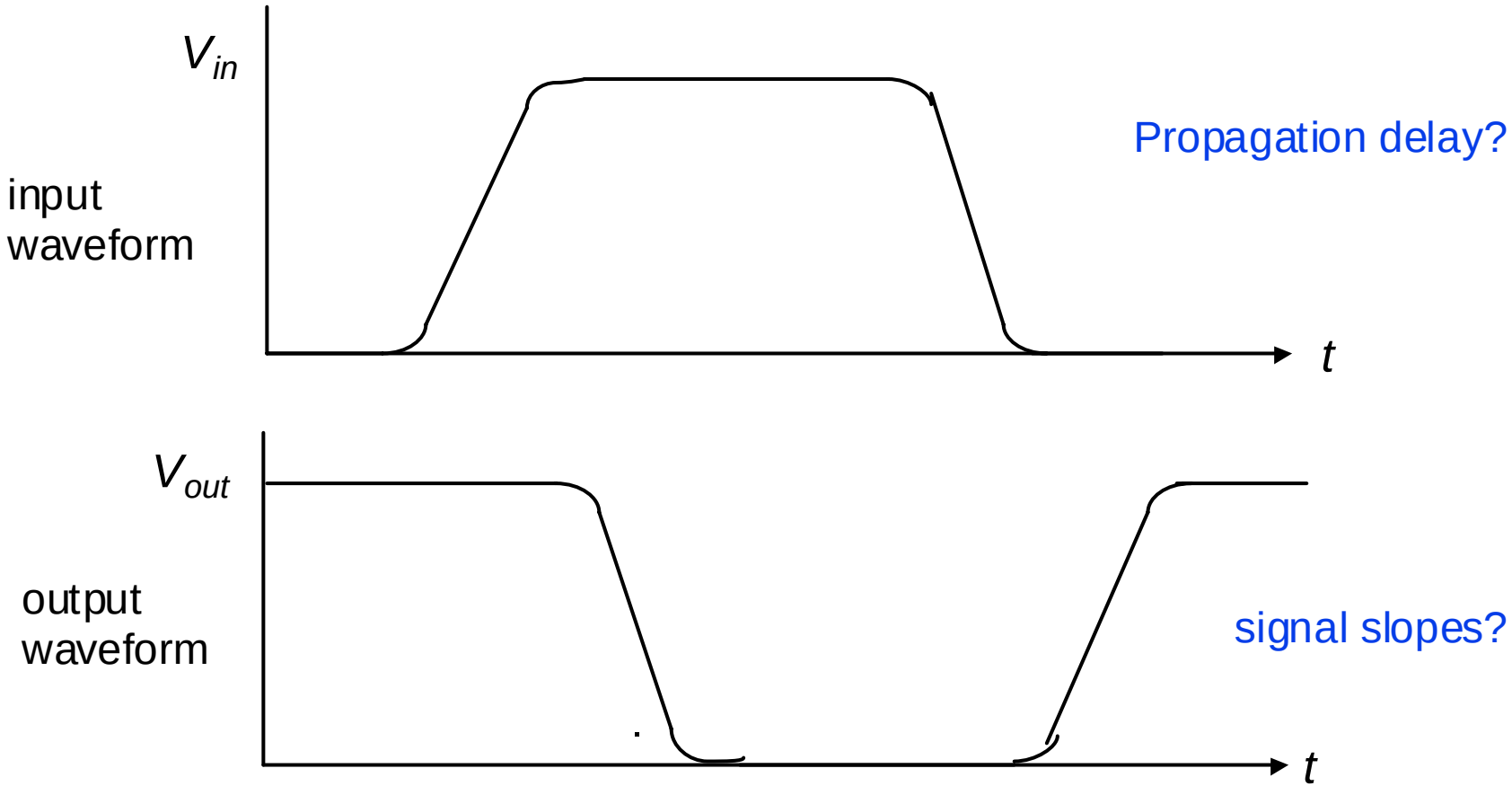
$NM_H = NM_L = VDD/2$

An Old-time Inverter

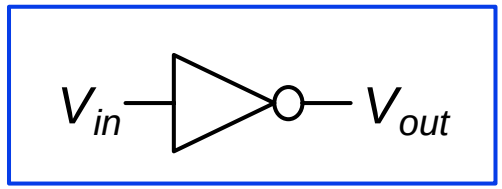


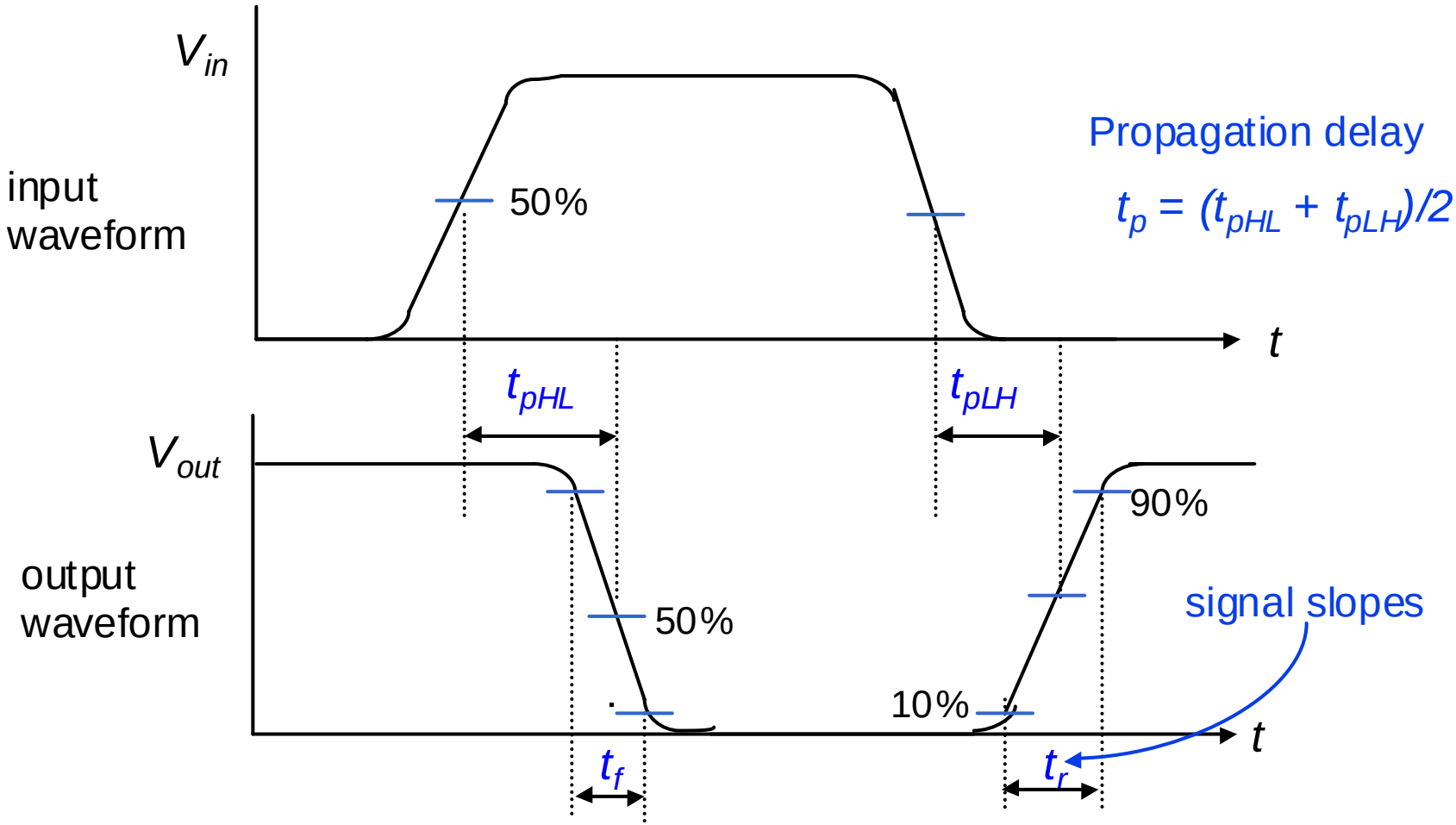
Delay Definitions



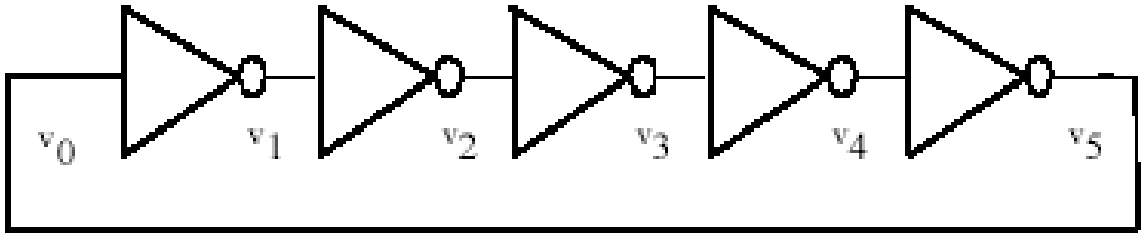


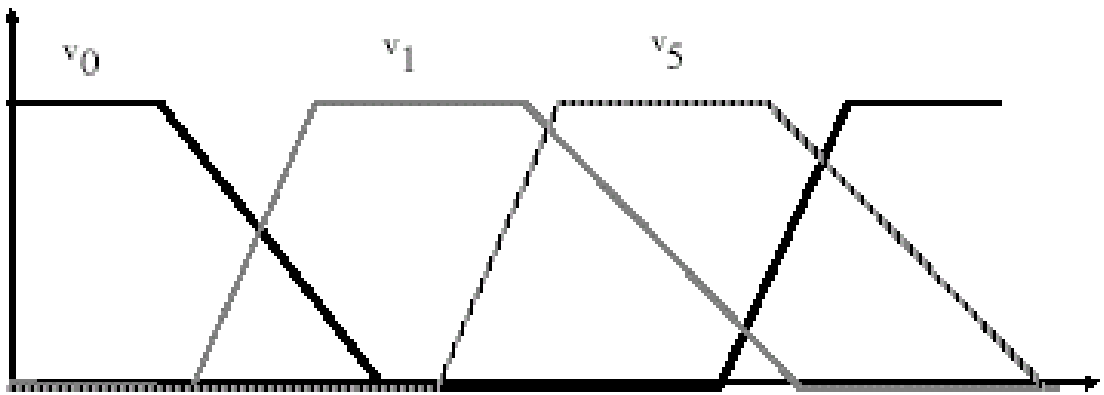
Delay Definitions





Ring Oscillator



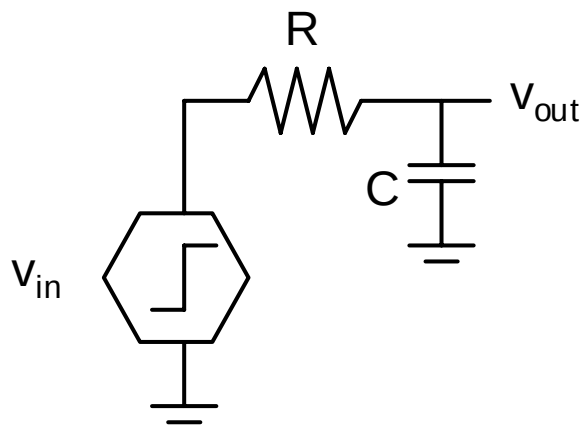


$$T = 2 \times t_p \times N$$

$$2Nt_p >> t_f + t_r$$

Modeling Propagation Delay

- Model circuit as first-order RC network



$$v_{out}(t) = (1 - e^{-t/\tau})V$$

where $\tau = RC$

Time to reach 50% point is

$t = \ln(2)\,\tau = 0.69\,\tau$

Time to reach 90% point is

$t = \ln(9)\,\tau = 2.2\,\tau$

- Matches the delay of an inverter gate

Power Dissipation

- Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

- supply line sizing (determined by peak power)

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

- battery lifetime (determined by average power dissipation)

Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}(t)dt$$

- packaging and cooling requirements

Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related
- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors
  - the faster the energy transfer (higher power dissipation) the faster the gate
- For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant
  - Power-delay product (PDP) – energy consumed by the gate per switching event : $P_{av} \times t_p$
- An ideal gate is one that is fast and consumes little energy, so the ultimate quality metric is
  - Energy-delay product (EDP) = PDP $\times t_p$

Power and Energy Dissipation

- Two important components: static and dynamic

$$E\ (\text{joules}) = C_L V_{dd}^2 P_{0\to1} + t_{sc} V_{dd} I_{peak} P_{0\to1} + V_{dd} I_{leakage}$$

$$f_{0\to1} = P_{0\to1} * f_{clock}$$

$$P\ (\text{watts}) = C_L V_{dd}^2 f_{0\to1} + t_{sc} V_{dd} I_{peak} f_{0\to1} + V_{dd} I_{leakage}$$

$$PDP = C_L V_{dd}^2 f_{0\to1} t_p$$

$$E_{0\to1} = \int_0^T P(t)dt = V_{dd}\int_0^T i_{supply}(t)dt = V_{dd}\int_0^{Vdd} C_L dV_{out} = C_L \bullet V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t)dt = \int_0^T V_{out} i_{cap}(t)dt = \int_0^{Vdd} C_L V_{out} dV_{out} = \frac{1}{2} C_L \bullet V_{dd}^2$$