EEM312 Laboratory

- Today:
  - About the labs
  - Overview of Spice3

EEM312 Laboratory

- Lab assistants are:
  Engin Çiftçi & Hasan Hatipoglu
- Labs are divided into two section. Verify your section as soon as possible.
- Lab homepage:
  http://www.baskent.edu.tr/~engcif
- Lab rules
- Lab syllabus

EEM312 Laboratory

- About Upload: Your initial password is <please ask your lab. assistant>
- You have to upload a word document others types are not allowed
- File name must be changed as

  94130045V02.doc

  and uploaded to the proper folder

  Why need versioning?

EEM312 Laboratory

- Contents of the lab
  - Rise time, fall time, noise margin and delay measurements both in HW and SW labs
  - Datasheet comparisons with the real measurements
  - Regenerative property of logic gates
  - Ring oscillators
  - Diodes and diode based logic gates
  - MOSFET models
  - Mosfets and measurements and comparisons
  - NMOS PMOS CMOS comparisons
  - Power dissipation of inverters
  - Domino logic implementation in Spice
  - Pass transistors logic implementations
  - Transmission gates and logics

Spice3

Circuit Simulation Program

INTRODUCTION

- **WinSpice3** is a general-purpose circuit simulation program for non-linear DC, non-linear transient, and linear AC analyses
- Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, lossless and lossy transmission lines, switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs

INTRODUCTION

- Installation:
  - You may download program at

http://www.winspice.com

http://www.baskent.edu.tr/~engcif

follow the links for the related materials: Academia→eem312

- Features:

  Unlimited ☺

  Has no schematic editor ☹

  Supporting the BSIM3 BSIM4 models

  Windows version of SPICE3F4

TYPES OF ANALYSIS

- DC Analysis
- AC Small-Signal Analysis
- Transient Analysis
- Pole-Zero Analysis
- Small-Signal Distortion Analysis
- Sensitivity Analysis
- Noise Analysis
- Analysis At Different Temperatures

CIRCUIT DESCRIPTION

- The first line in the input file must be the title, and the last line must be ".END"
- An element line that contains the element name, the circuit nodes to which the element is connected, and the values of the parameters that determine the electrical characteristics of the element specifies each element in the circuit

CIRCUIT DESCRIPTION

- A number field may be an integer field (12, -44), a floating point field (3.14159), either an integer or floating point number followed by an integer exponent (1e-14, 2.65e3), or either an integer or a floating point number followed by one of the following scale factors:
  - T = 10^{12}
  - G = 10^{9}
  - Meg = 10^{6}
  - K = 10^{3}
  - mil = 25.4^{-6}
  - m = 10^{-3}
  - u (or M) = 10^{-6}
  - N = 10^{-9}
  - p = 10^{-12}
  - f = 10^{-15}
- Letters immediately following a number that are not scale factors are ignored, and letters immediately following a scale factor are ignored.

CIRCUIT DESCRIPTION

- The title line must be the first in the input file.
- “.END” line must always be the last in the input file.
- Comments:
  * <any comment>

CIRCUIT DESCRIPTION

- **.MODEL: Device Models**

  .MODEL MNAME TYPE(PNAME1=PVAL1 PNAME2=PVAL2 ...)

  Ex: NPN Transistor

  .MODEL MOD1 NPN (BF=50 IS=1E-13 VBF=50)

- TYPES
  - A set of device model parameters is defined on a separate ".MODEL" line and assigned a unique model name.
  - For these more complex device types, each device element line contains the device name, the nodes to which the device is connected, and the device model name.

CIRCUIT DESCRIPTION

- **R** Semiconductor resistor model
- **C** Semiconductor capacitor model
- **SW** Voltage controlled switch
- **VSWITCH** Voltage controlled switch
- **CSW** Current controlled switch
- **ISWITCH** Current controlled switch
- **URC** Uniform distributed RC model
- **LTRA** Lossy transmission line model
- **D** Diode model
- **NPN** NPN BJT model
- **PNP** PNP BJT model
- **NJF** N-channel JFET model
- **PJF** P-channel JFET model
- **NMOS** N-channel MOSFET model
- **PMOS** P-channel MOSFET model
- **NMF** N-channel MESFET model
- **PMF** P-channel MESFET model

CIRCUIT DESCRIPTION

Extra information for descriptions:

.SUBCKT subnam N1 <N2 N3 ...>

.ENDS <SUBNAM>

.INCLUDE filename

.LIB filename

CIRCUIT ELEMENTS AND MODELS

Simple Resistors

RXXXXXXX N1 N2 VALUE

Ex:

R1 1 2 100

RC1 12 17 1K

Semiconductor Resistors

RXXXXXXX N1 N2 <VALUE> <MNAME> <L=LENGTH> <W=WIDTH> <TEMP=T>

Ex:

RLOAD 2 10 10K

RMOD 3 7 RMODEL L=10u W=1u

- TEMP value is the temperature at which this device is to operate, and overrides the temperature specification on the .OPTION control line.

CIRCUIT ELEMENTS AND MODELS

- **Semiconductor Resistors**
  - **If value is defined**
    - it overrides the geometric information and defines the resistance
    - **If MNAME is also defined**
      - Resistance may be calculated from the process information in the model MNAME and the given LENGTH and WIDTH
  - **If value is not defined**
    - MNAME and LENGTH must be specified

CIRCUIT ELEMENTS AND MODELS

- **Semiconductor Resistor Model (R)**

$$R=RSH((L-NARROW)/(W-NARROW))$$

$$R(T)=R(T_0)[1+TC1(T-T_0)+TC2(T-T_0)^2]$$

name	parameter	units	default	example
TC1	1st order Temp. coefficient	? /°C	0.0	
TC2	2nd order Temp. coefficient	? /°C^2	0.0	
RSH	sheet resistance	? /square		50
DEFW	default width	meters	1e-6	2e-6
NARROW	narrowing due to side etching	meters	0.0	1e-7
TNOM	parameter measurement temperature	°C	27	50

CIRCUIT ELEMENTS AND MODELS

Simple Capacitors

CXXXXXXX N+ N- VALUE <IC=initial_condition>

EX:

CBYP 13 0 1UF

COSC 17 23 10U IC=3V

Semiconductor Capacitors

CXXXXXXX N1 N2 <VALUE> <MNAME> <L=LENGTH> <W=WIDTH> <IC=VAL>

EX:

CLOAD 2 10 10P

CMOD 3 7 CMODEL L=10u W=1u

CIRCUIT ELEMENTS AND MODELS

- **Semiconductor Capacitors**
  - **If value is defined**
    - it overrides the geometric information and defines the resistance
    - **If MNAME is also defined**
      - Resistance may be calculated from the process information in the model MNAME and the given LENGTH and WIDTH
  - **If value is not defined**
    - MNAME and LENGTH must be specified

CIRCUIT ELEMENTS AND MODELS

- **Semiconductor Capacitor Model (C)**

CAP=CJ(LENGTH-NARROW)(WIDTH-NARROW)+*CJSW*(LENGTH+WIDTH-2NARROW)

name	parameter	units	default	example
TNOM	parameter measurement temperature	°C	27	50
TC1	first order temperature coefficient	&/°C	0.0	
TC2	second order temperature coefficient.	&/°C2	0.0	
VC1	first order voltage coefficient	volt-1	0.0	
VC2	second order voltage coefficient.	volt-2	0.0	
CJ	junction bottom capacitance	F/meters2		5,00E-05
CJSW	junction side wall capacitance	F/meters		2,00E-11
DEFW	default device width	meters	1,00E-06	2,00E-06
NARROW	narrowing due to side etching	meters	0.0	1,00E-07

CIRCUIT ELEMENTS AND MODELS

- **Inductors**

LYYYYYYY N+ N- VALUE <IC=initial condition>

EX:

LLINK 42 69 1UH

LSHUNT 23 51 10U IC=15.7MA

- **Coupled (Mutual) Inductors**

KXXXXXXX LYYYYYYY LZZZZZZZ VALUE

EX:

K43 LAA LBB 0.999

KXFRMR L1 L2 0.87

- Coefficient of coupling must be greater than 0 and less than or equal to 1.
- Using the 'dot' convention, place a 'dot' on the first node of each inductor.

CIRCUIT ELEMENTS AND MODELS

- **Voltage Controlled Switch**
  SXXXXXXX N+ N- NC+ NC- MODEL <ON><OFF>
  N± are terminal nodes, NC± are control nodes
  EX:
  s1 1 2 3 4 switch1 ON
  s2 5 6 3 0 sm2 off
  Switch1 1 2 10 0 smodel1
- **Current Controlled Switch**
  WYYYYYYY N+ N- VNAM MODEL <ON><OFF>
  EX:
  w1 1 2 vclock switchmod1
  W2 3 0 vramp sm1 ON
  wreset 5 6 vclck lossyswitch OFF
- For model parameters see manual

CIRCUIT ELEMENTS AND MODELS

- **Voltage And Current Sources**

```
VXXXXXXX N+ N- <<DC> DC/TRAN VALUE>
                   <AC <ACMAG <ACPHASE>>>
                   <DISTOF1 <F1MAG <F1PHASE>>>
                   <DISTOF2 <F2MAG <F2PHASE>>>

IXXXXXXX N+ N- <<DC> DC/TRAN VALUE>
                   <AC <ACMAG <ACPHASE>>>
                   <DISTOF1 <F1MAG <F1PHASE>>>
                   <DISTOF2 <F2MAG <F2PHASE>>>
```

EX:

```
VCC 10 0 DC 6
VIN 13 2 0.001 AC 1 SIN(0 1 1MEG)
ISRC 23 21 AC 0.333 45.0 SFFM(0 1 10K 5 1K)
VMEAS 12 9
VCARRIER 1 0 DISTOF1 0.1 -90.0
VMODULATOR 2 0 DISTOF2 0.01
IIN1 1 5 AC 1 DISTOF1 DISTOF2 0.001
```

CIRCUIT ELEMENTS AND MODELS

- DC/TRAN is the DC and transient analysis value of the source. If the source value is zero both for DC and transient analyses, this value may be omitted. If the source value is time-invariant (e.g., a power supply), then the value may optionally be preceded by the letters DC.

- ACMAG is the AC magnitude and ACPHASE is the AC phase. The source is set to this value in the AC analysis. If ACMAG is omitted following the keyword AC, a value of unity is assumed. If ACPHASE is omitted, a value of zero is assumed. If the source is not an AC small-signal input, the keyword AC and the AC values are omitted.

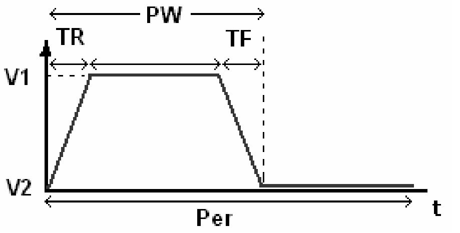
- DISTOF1 and DISTOF2 are the keywords that specify that the independent source has distortion inputs at the frequencies F1 and F2 respectively (see the description of the .DISTO control line). An optional magnitude and phase may follow the keywords. The default values of the magnitude and phase are 1.0 and 0.0 respectively.

CIRCUIT ELEMENTS AND MODELS

- **Pulse**

  PULSE(V1 V2 TD TR TF PW PER)

  EX:



VIN 3 0 PULSE(-1 1 2NS 2NS 2NS 50NS 100NS)

parameter	**default value**	**units**
V1 (initial value)		Volts or Amps
V2 (pulsed value)		Volts or Amps
TD (delay time)	0.0	seconds
TR (rise time)	TSTEP	seconds
TF (fall time)	TSTEP	seconds
PW (pulse width)	TSTOP	seconds
PER(period)	TSTOP	seconds

CIRCUIT ELEMENTS AND MODELS

- **Sinusoidal**

  SIN(VO VA FREQ TD THETA)

  EX:

  VIN 3 0 SIN(0 1 100MEG 1NS 1E10)

parameters	**default value**	**units**
VO (offset)		Volts or Amps
VA (amplitude)		Volts or Amps
FREQ (frequency)	1/TSTOP	Hz
TD (delay)	0.0	seconds
THETA (damping factor)	0.0	1/seconds

CIRCUIT ELEMENTS AND MODELS

- **Transistors And Diodes**

- The model for the BJT is based on the integral-charge model of Gummel and Poon; however, if the Gummel-Poon parameters are not specified, the model reduces to the simpler Ebers-Moll model. In either case, charge-storage effects, ohmic resistances, and a current-dependent output conductance may be included.

- The diode model can be used for either junction diodes or Schottky barrier diodes. The JFET model is based on the FET model of Shichman and Hodges.

CIRCUIT ELEMENTS AND MODELS

- Six MOSFET models are implemented: MOS1 is described by a square-law I-V characteristic, MOS2 is an analytical model, while MOS3 is a semi-empirical model; MOS6 is a simple analytic model accurate in the short-channel region; MOS4 and MOS5 are the BSIM (Berkeley Short-channel IGFET Model) and BSIM2. MOS2, MOS3, and MOS4 include second-order effects such as channel length modulation, sub threshold conduction, scattering-limited velocity saturation, small-size effects, and charge-controlled capacitances.

CIRCUIT ELEMENTS AND MODELS

- **Junction Diodes**

DXXXXXXX N+ N- MNAME <AREA> <OFF> <IC=VD(initial condition)> <TEMP=T>

EX:

DBRIDGE 2 10 DIODE1

DCLMP 3 7 DMOD 3.0 IC=0.2

CIRCUIT ELEMENTS AND MODELS

- **Diode Model (D)**
  - The DC characteristics of the diode are determined by the parameters **IS** and **N**. An ohmic resistance, **RS**, is included
  - Charge storage effects are modeled by a transit time, **TT**, and a non-linear depletion layer capacitance which is determined by the parameters **CJO**, **VJ**, and **M**
  - Reverse breakdown is modelled by an exponential increase in the reverse diode current and is determined by the parameters **BV** and **IBV**

For model parameters see manual

CIRCUIT ELEMENTS AND MODELS

- **Bipolar Junction Transistors (BJTs)**

QXXXXXXX NC NB NE <NS> MNAME <AREA> <OFF> <IC=VBE, VCE> <TEMP=T>

EX:

Q23 10 24 13 QMOD IC=0.6, 5.0

Q50A 11 26 4 20 MOD1

CIRCUIT ELEMENTS AND MODELS

- The DC model is defined by the parameters **IS**, **BF**, **NF**, **ISE**, **IKF**, and **NE** which determine the forward current gain characteristics, **IS**, **BR**, **NR**, **ISC**, **IKR**, and **NC** which determine the reverse current gain characteristics, and **VAF** and **VAR** which determine the output conductance for forward and reverse regions.

- Three ohmic resistances **RB**, **RC**, and **RE** are included, where **RB** can be highly current dependent. Base charge storage is modelled by forward and reverse transit times, **TF** and **TR**, the forward transit time **TF** being bias dependent if desired.

- **CJE**, **VJE**, and **MJE** determine non-linear depletion layer capacitances for the B-E junction, **CJC**, **VJC**, and **MJC** for the B-C junction and **CJS**, **VJS**, and **MJS** for the C-S (Collector-Substrate) junction.

For model parameters see manual

CIRCUIT ELEMENTS AND MODELS

- **Junction Field-Effect Transistors (JFETs)**

JXXXXXXX ND NG NS MNAME <AREA> <OFF> <IC=VDS, VGS> <TEMP=T>

EX:

J1 7 2 3 JM1 OFF

CIRCUIT ELEMENTS AND MODELS

- **JFET Models (NJF/PJF)**
  - LEVEL=1 -> Shichman-Hodges
  - LEVEL=2 -> Parker-Skellern FET model
- In both models, the DC characteristics are defined by the parameters **VTO** and **BETA**, which determine the variation of drain current with gate voltage, **LAMBDA**, which determines the output conductance, and **IS**, the saturation current of the two gate junctions. Two ohmic resistances, **RD** and **RS**, are included.

CIRCUIT ELEMENTS AND MODELS

- **MOSFETs**

```
MXXXXXXX ND NG NS NB MNAME <L=VAL> <W=VAL> <AD=VAL> <AS=VAL>
        <PD=VAL> <PS=VAL> <NRD=VAL> <NRS=VAL> <OFF>
        <IC=VDS, VGS, VBS> <TEMP=T>
```

Ex:

```
M1 24 2 0 20 TYPE1
M31 2 17 6 10 MODM L=5U W=2U
M1 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U PS=40U
```

- **PD** and **PS** are the perimeters of the drain and source junctions
- **NRD** and **NRS** designate the equivalent number of squares of the drain and source diffusions

CIRCUIT ELEMENTS AND MODELS

- **MOSFET Models (NMOS/PMOS)**

  SPICE provides four MOSFET device models, which differ in the formulation of the I-V characteristic. The variable LEVEL specifies the model to be used:

- LEVEL=1 Shichman-Hodges
- LEVEL=2 MOS2
- LEVEL=3 MOS3, a semi-empirical model
- LEVEL=4 BSIM1
- LEVEL=5 BSIM2
- LEVEL=6 MOS6
- LEVEL=8 BSIM3
- LEVEL=9 B3SOI
- LEVEL=14 BSIM4
- LEVEL=44 EKV from Ecole Polytechnique Federale de Lausanne
- LEVEL=49 BSIM3 (same as LEVEL=8 for HSPICE compatibility)

CIRCUIT ELEMENTS AND MODELS

- *** Level 3 SPICE model for CMOS14TB 0.5 um**

```
.MODEL CMOSN5 NMOS LEVEL=3 PHI=0.700000
+ TOX=9.6000E-09 XJ=0.200000U TPG=1
+ VTO=0.7118 DELTA=2.3060E-01 LD=2.9830E-08 KP=1.8201E-04
+ UO=506.0 THETA=1.9090E-01 RSH=1.8940E+01 GAMMA=0.6051
+ NSUB=1.4270E+17 NFS=7.1500E+11 VMAX=2.4960E+05 ETA=2.5510E-02
+ KAPPA=1.8530E-01 CGDO=9.0000E-11 CGSO=9.0000E-11
+ CGBO=3.7295E-10 CJ=6.02E-04 MJ=0.805 CJSW=2.0E-11
+ MJSW=0.761 PB=0.99
```

*** Level 3 SPICE model for CMOS14TB 0.5 um**

```
.MODEL CMOSP5 PMOS LEVEL=3 PHI=0.700000
+ TOX=9.6000E-09 XJ=0.200000U TPG=-1
+ VTO=-0.9016 DELTA=4.2020E-01 LD=4.3860E-08 KP=4.1582E-05
+ UO=115.6 THETA=3.7990E-02 RSH=9.0910E-02 GAMMA=0.4496
+ NSUB=7.8780E+16 NFS=6.4990E+11 VMAX=2.3130E+05 ETA=2.8580E-02
+ KAPPA=9.9270E+00 CGDO=9.0000E-11 CGSO=9.0000E-11
+ CGBO=3.6835E-10 CJ=9.34E-04 MJ=0.491 CJSW=2.41E-10
+ MJSW=0.222 PB=0.90
```

Analyses

- **.TRAN: Transient Analysis**

  .TRAN TSTEP TSTOP <TSTART <TMAX>>

  EX:

  .TRAN 1NS 100NS

  .TRAN 1NS 1000NS 500NS

  .TRAN 10NS 1US

- **TSTEP** is the printing or plotting increment for line printer output. For use with the post processor,**TSTEP** is the suggested computing increment.

- **TSTOP** is the final time, and **TSTART** is the initial time. If **TSTART** is omitted, it is assumed to be zero. The transient analysis always begins at time zero. In the interval <zero, TSTART>, the circuit is analysed (to reach a steady state), but no outputs are stored. In the interval <TSTART, TSTOP>, the circuit is analysed and outputs are stored.
- **TMAX** is the maximum step size that **WinSpice3**

BATCH OUTPUT

- **.PLOT**
  .PLOT PLTYPE OV1 <(PLO1, PHI1)> <OV2 <(PLO2, PHI2)> ... OV8>
  EX:
  - .PLOT DC V(4) V(5) V(1)
  - .PLOT TRAN V(17, 5) (2,5) I(VIN) V(17) (1,9)
  - .PLOT AC VM(5) VM(31, 24) VDB(5) VP(5)
  - .PLOT DISTO HD2 HD3(R) SIM2
  - .PLOT TRAN V(5,3) V(4) (0,5) V(7) (0,10)
- V(N1<,N2>)
  - V magnitude (same as VM below)
  - VR real part
  - VI imaginary part
  - VM magnitude
  - VP phase (in radians or degrees - see the **units** variable description)
  - VDB 20 log10(magnitude)

BATCH OUTPUT

- I(VXXXXXXX)

  Specifies the current flowing in the independent voltage source named VXXXXXXX

  - I magnitude (same as IM below)
  - IR real part
  - II imaginary part
  - IM magnitude
  - IP phase (in radians or degrees - see the **units** variable description)
  - IDB 20 log10(magnitude)
- Question:

  How do we measure a current flowing in a branch?

Thank you

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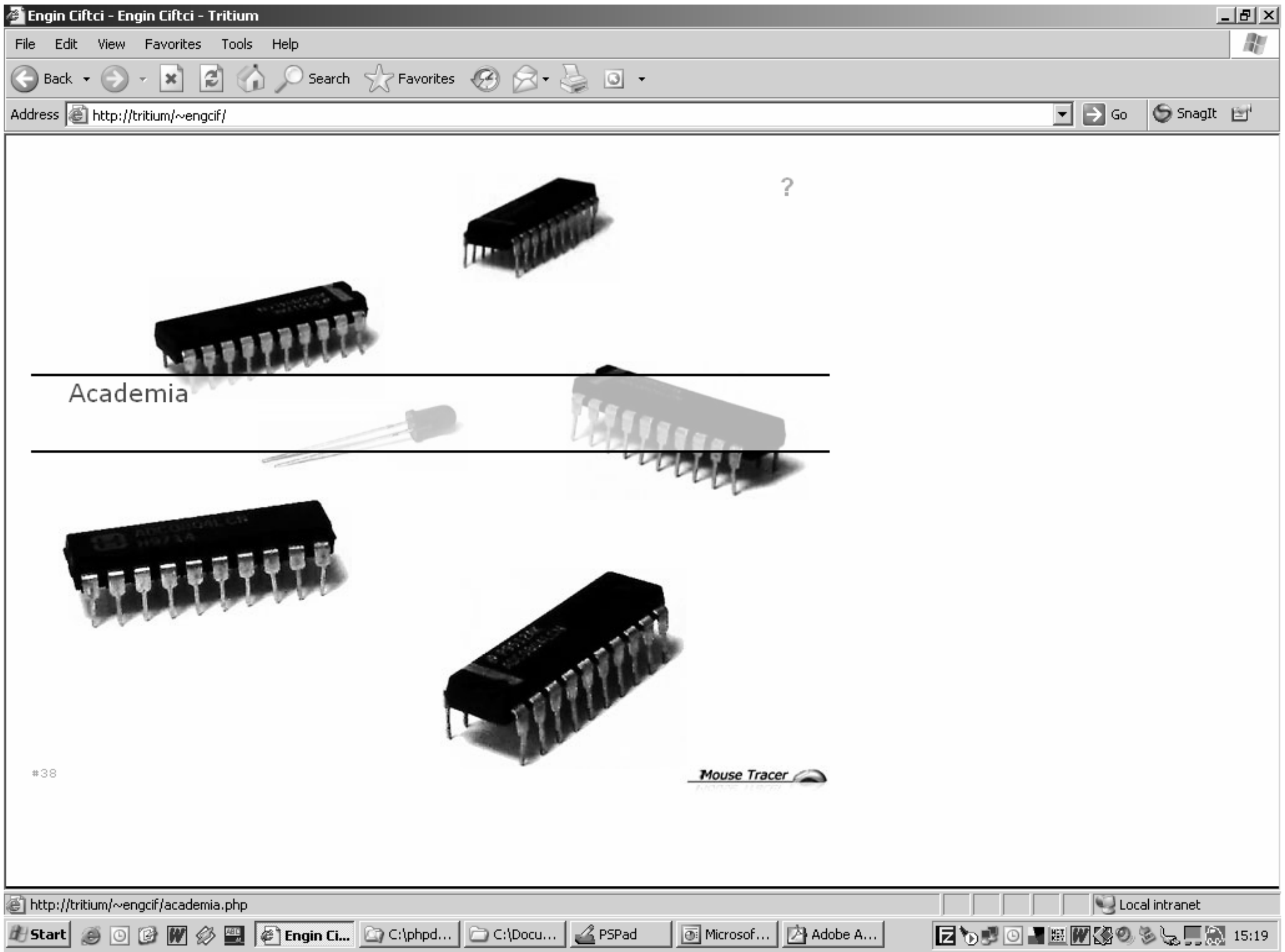

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Academia

Current courses:

2004-2005 (Spring)	Lecture Code	Description
	EEM214	Electronics I
	EEM312	Digital Electronics
	EEM412	Introduction to VLSI Design II

Assisted courses in previous semesters:

Year/Semester	Lecture Code	Description
2004-2005 (Fall)	EEM211	Digital Logic Design
	EEM411	Introduction to VLSI Design
	EEM491	Final Project
2003-2004 (Spring)	EEM312	Digital Electronics
	EEM412	VLSI Design II
	EEM474	Power Electronics
2003-2004 (Fall)	EEM211	Digital Logic Design
	EEM411	Introduction to VLSI Design
	EEM461	Process Control
2002-2003 (Spring)	EEM332	Microprocessors

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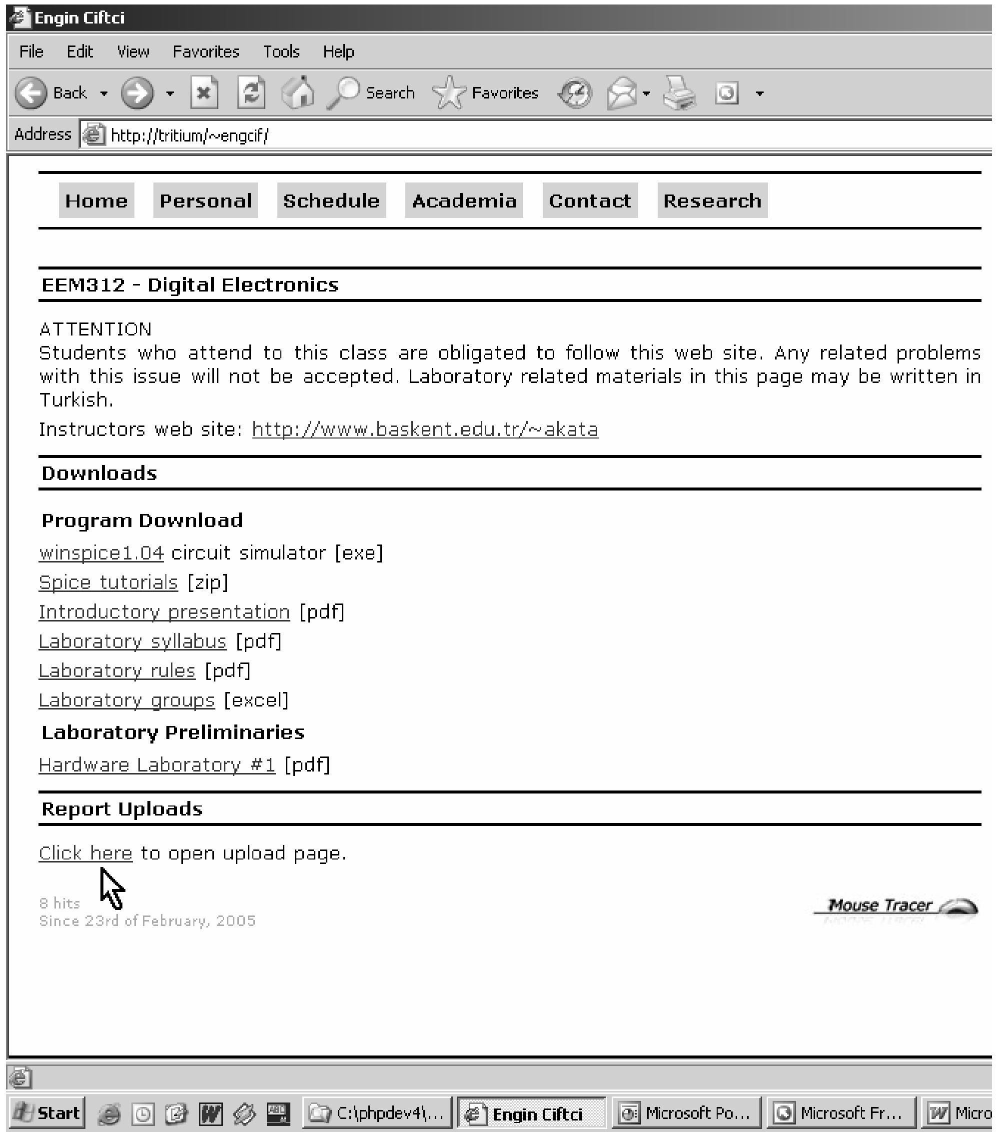

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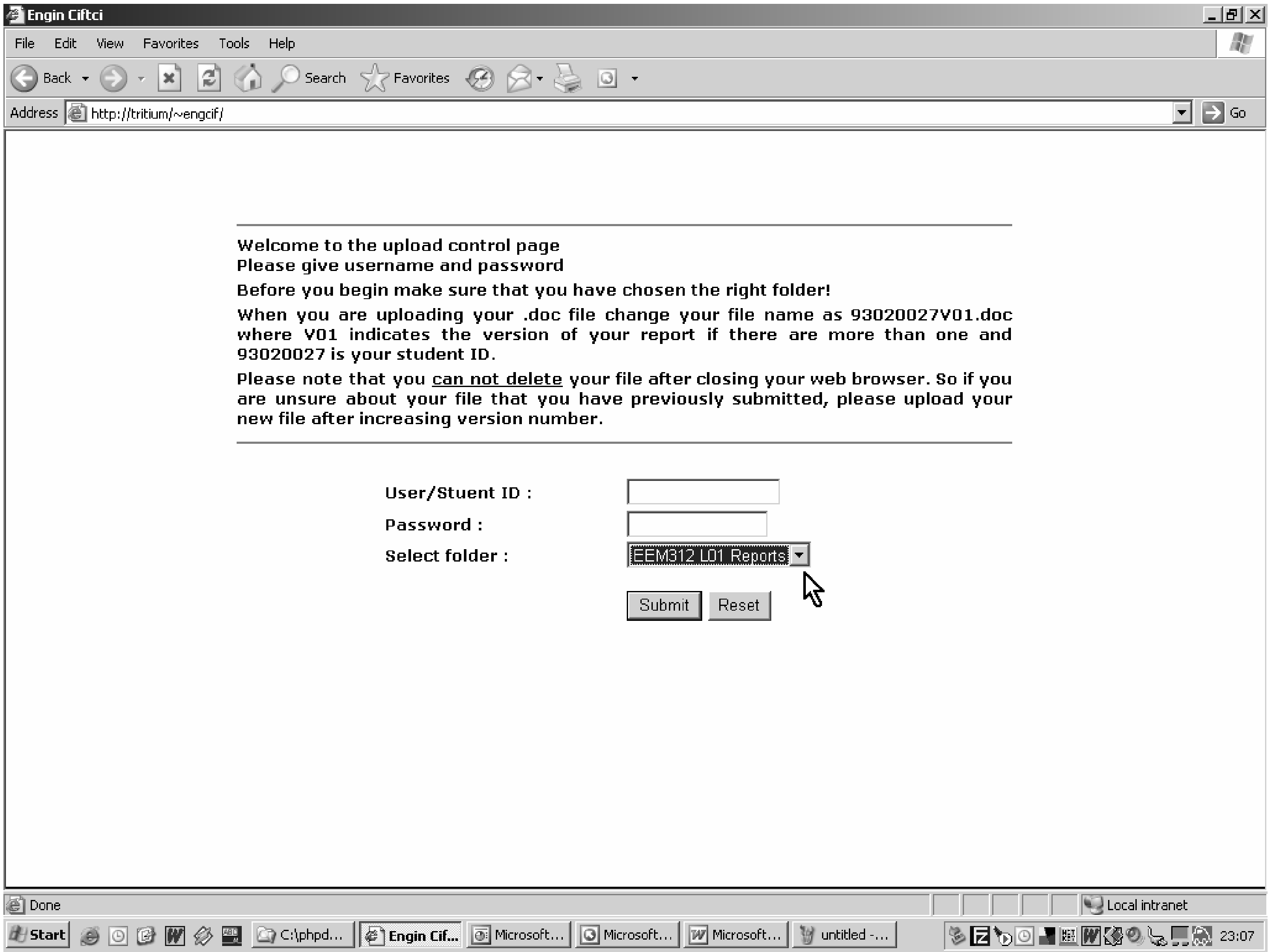

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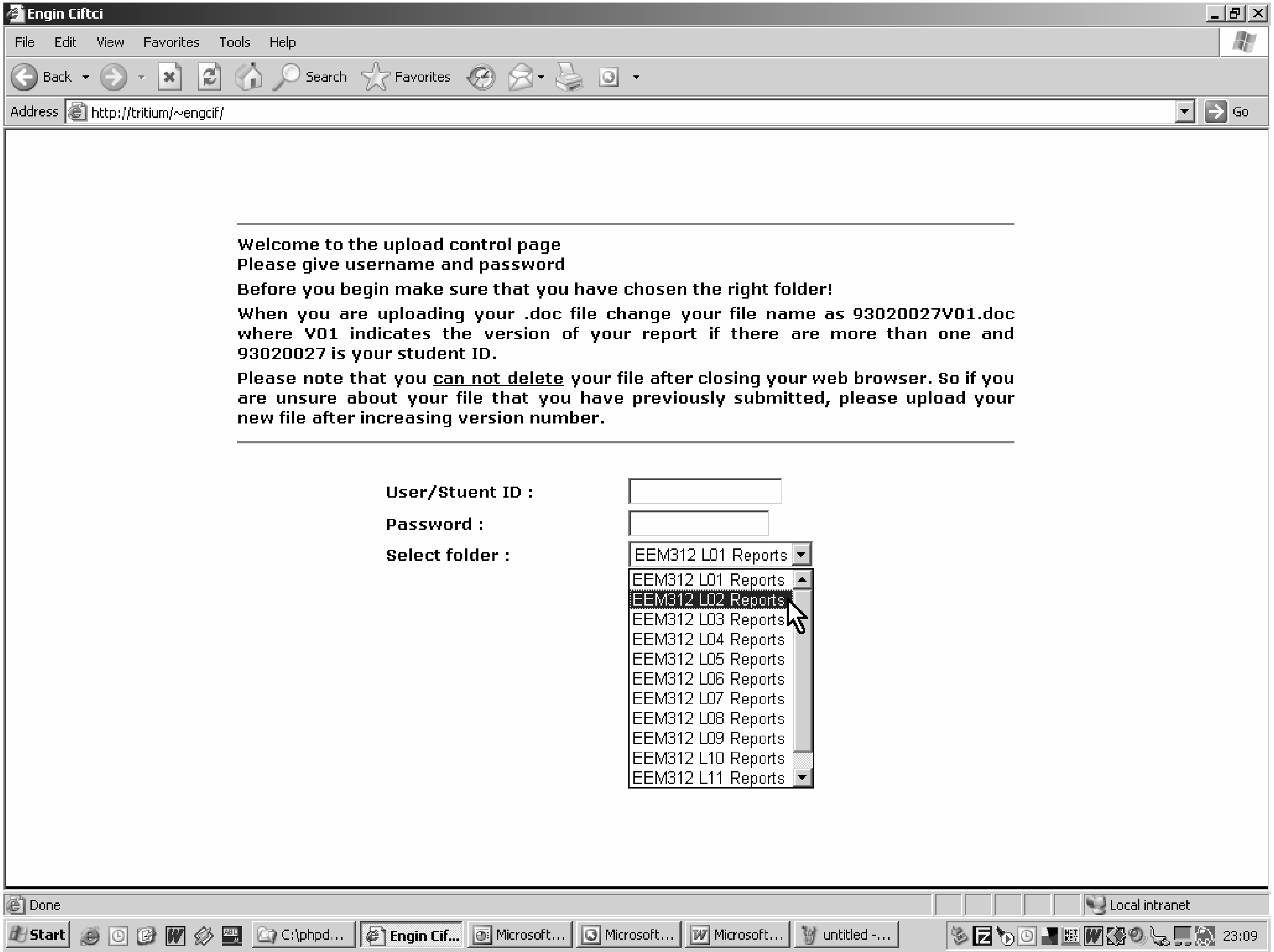

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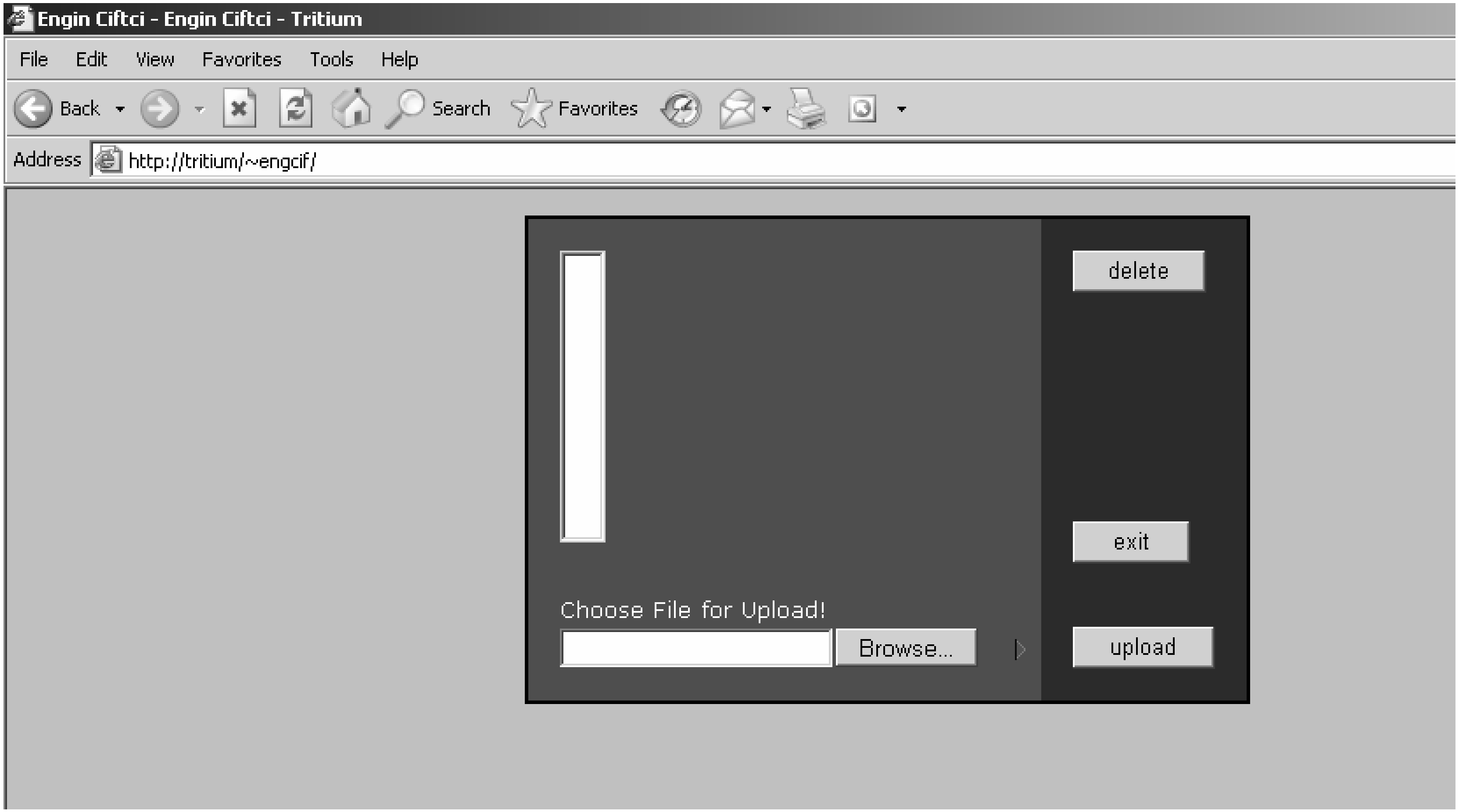

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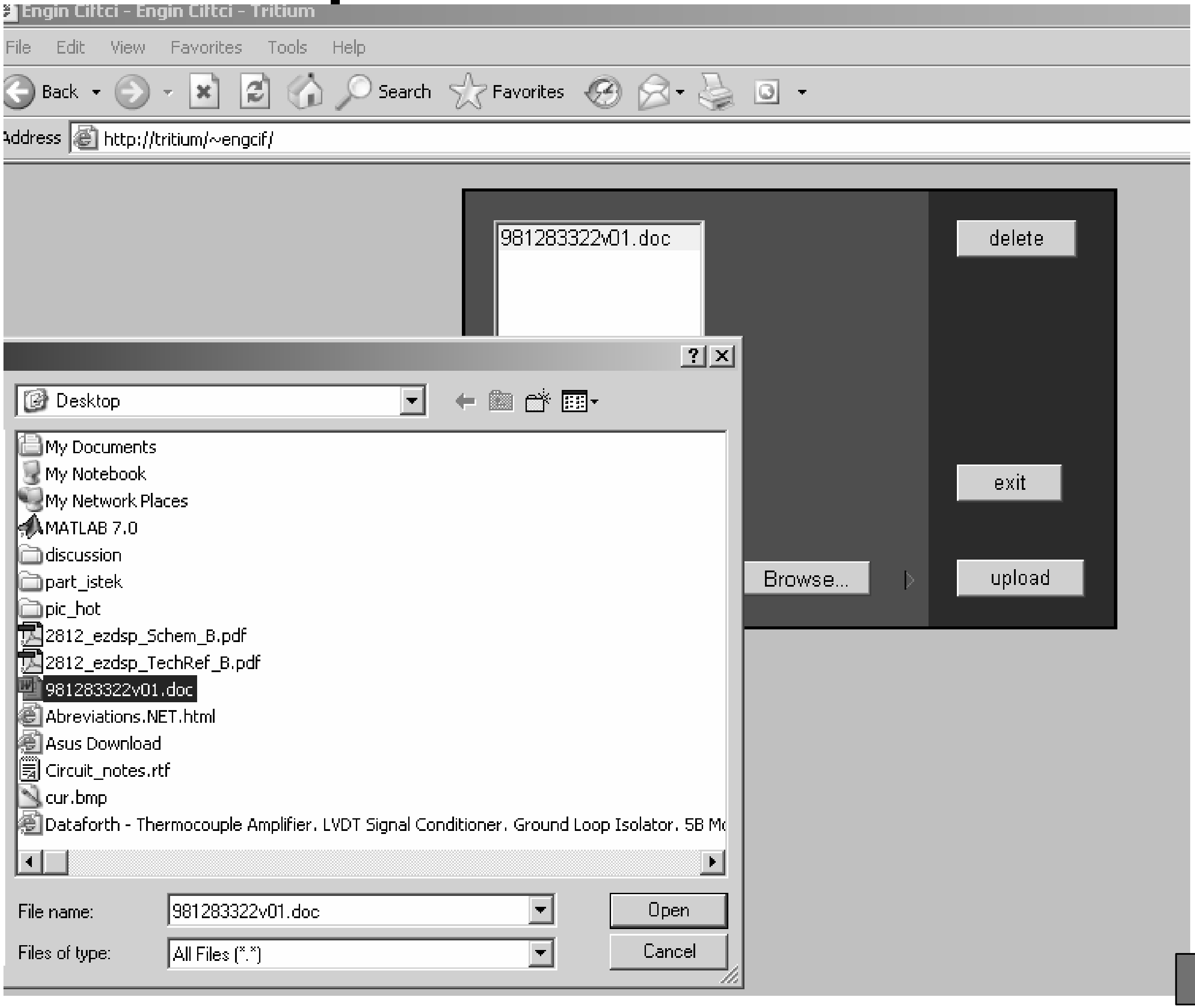

PULSE