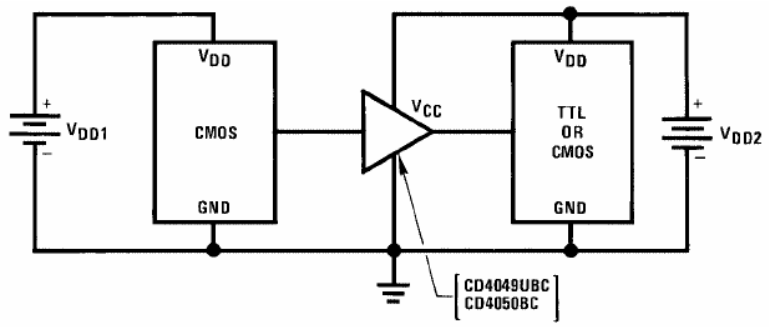
BAŞKENT ÜNİVERSİTESİ
Mühendislik Fakültesi - Elektrik-Elektronik Mühendisliği Bölümü
EEM 312 – Sayısal Elektronik
Donanım Laboratuvarı

Deney No: D2
Deney Adı: Entegre devre tersleyici ölçümleri
Amaç:

- Veri kitabı kullanımı
- Veri kitabında yer alan verilerin deneysel olarak gözlenmesi ve kıyaslanması

Ön Çalışma:

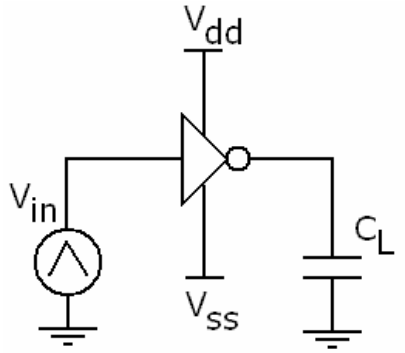
1. Ekte iki adet veri kitabı verilmiştir. Verilen veri kitaplarını inceleyin ve aşağıdaki soruları cevaplayın;
    a. Entegreler hangi mantık ailesinin (logic family) elemanıdır?
    b. Veri kitabında her bir entegrenin hangi özellikleri ön plana çıkarılmıştır ya da vurgulanmıştır?
    c. Hangi entegre 5V'luk besleme gerliminde çalışabilmektedir?
    d. Hangi entegre 5V'luk besleme geriliminde çıkışı için düşük tr, tf değerine sahiptir?
    e. Bu iki entegreyi birbirine doğrudan bağlayarak bir tane tampon (buffer – non invering buffer) yapmak mümkün müdür? Eğer mümkün ise hangisi tamponun girişinde kullanılmalıdır ya da sıralama yapmak gerekir mi?
    f. Aşağıdaki şekilde veri kitabında verilen bir CD4050'nin örnek uygulaması görülmektedir. CD4050 ya da CD4049'un buradaki kullanılış amacı nedir, açıklayınız.



Laboratuvar Çalışması:

1. Laboratuarda size verilen entegre hangi mantık ailesine girmektedir. Tam parça numarasını ve **özelliklerini** raporunuza yazın.

2. Laboratuardaki sinyal üreticilerini 5V max 0V min değerlerine sahip 1KHz'lik üçgen dalga verecek biçimde ayarlayın. Daha sonra size verilen entegre paketi içerisindeki bir tersleyiciyi (inverter) şekil-1'deki gibi başlayın. C_L kapasitörünü 10pF alın. Vdd ve Vss arasına deşiğken güç kaynağını kullanarak 5V DC uygulayın.



Şekil 1 – Tersleyici

Osiloskop'u bağlamadan önce zaman dilimi ayarlarını ve voltaj seviyesi ayarlarını girişteki sinyali ölçebilecek biçimde ayarlayın. Her iki kanalı da DC'değer ölçecek şekilde ayarlamayı unutmayın. Osiloskop girişlerini doğru çarpana ayarlamaya dikkat edin. Osiloskop'un birinci kanalını Vin'e ikinci kanalını ise C_L kapasitörüne bağlayın. Daha sonra osiloskobu X-Y moduna alarak çıkışı gözlemleyin. Bu grafiği kullanarak V_{OH} V_{OL} V_{IL} V_{IH} değerlerini ölçebilir misiniz? Girişteki Vin kaynağını ayarlanabilir bir voltaj kaynağı ile değiştirerek öçümlerinizi kolaylaştırabilirsiniz. Kuruduğunuz düzenekte tablo-1'de verilen parametreleri ölçerek elde edin ve bu değerleri veri kitabında verilen değerler ile karşılaştırarak kıyaslayın ve raporunuzda tartışın.

Tablo 1 – DC karakter ölçümleri

VOL	
VOH	
VIL	
VIH	
NMH	
NML	

3. Kurulan düzenekte bu kez sinyal üreticisini 1KHz'lik 0-5V'luk kare dalga verecek bir biçimde yeniden ayarlayın. Osiloskop'u giriş ve çıkış sinyallerini elde edecek biçimde yeniden ayarlayın ve zaman ekseninde her iki sinyali gözlemleyecek bir biçime getirin. Osiloskop'un üzerindeki ölçüm menüsünü kullanarak aşağıdaki değerleri ölçerek elde edin ve bu değerleri veri kitabında verilen değerler ile karşılaştırarak kıyaslayın, raporunuzda tartışın.

Tablo 2 – Zaman ölçümleri

tr	
tf	
tpHL	
tpLH	
td	

Değerlendirme:

Değerlendirme ile ilgili bilgileri ilgili web sayfasında bulabilirsiniz. Raporlarınızı laboratuar web sayfasına teslim süresinden önce yüklemeniz gerekmektedir. Yükleme ile ilgili detaylar web sayfasında yer almaktadır

http://www.baskent.edu.tr/~engcif

EK1

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised April 2002

CD4049UBC • CD4050BC
Hex Inverting Buffer • Hex Non-Inverting Buffer

General Description

The CD4049UBC and CD4050BC hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at V_{DD} = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

- Wide supply voltage range: 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current “sink” or “source” driver
- CMOS HIGH-to-LOW logic level converter

Ordering Code:

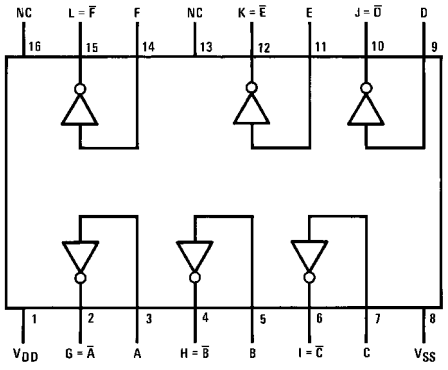
Order Number	Package Number	Package Description
CD4049UBCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4049UBCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4050BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4050BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagrams

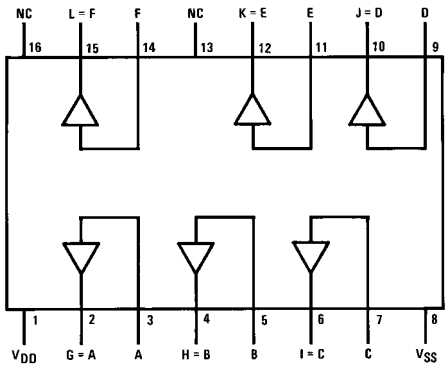
Pin Assignments for DIP

CD4049UBC



Top View

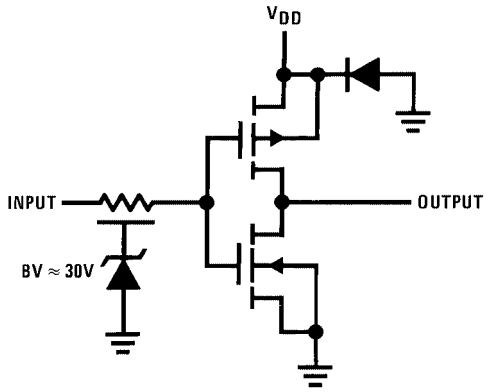
CD4050BC



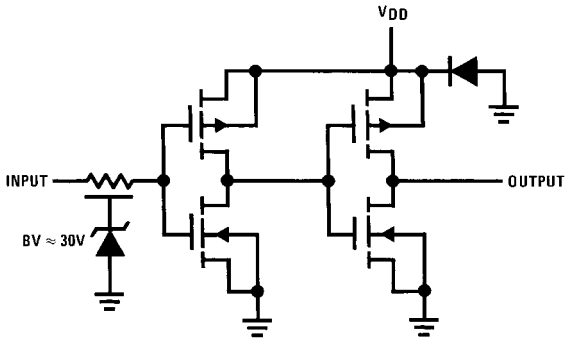
Top View

Schematic Diagrams

CD4049UBC
1 of 6 Identical Units



CD4050BC
1 of 6 Identical Units



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to +18V
Voltage at Any Output Pin (V_{OUT})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to 15V
Voltage at Any Output Pin (V_{OUT})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4049UBC, CD4050BC	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		30	
		V_{DD} = 10V		2.0		0.01	2.0		60	µA
		V_{DD} = 15V		4.0		0.03	4.0		120	
V_{OL}	LOW Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 µA								
		V_{DD} = 5V		0.05		0	0.05		0.05	
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	
V_{OH}	HIGH Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V,								
		$\|I_O\|$ < 1 µA								
		V_{DD} = 5V	4.95		4.95	5		4.95		
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	
V_{IL}	LOW Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4050BC Only)	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$ < 1 µA								
	(CD4049UBC Only)	V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		
I_{OL}	LOW Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 0.4V	5.6		4.6	5		3.2		
		V_{DD} = 10V, V_O = 0.5V	12		9.8	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	35		29	40		20		
I_{OH}	HIGH Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
	(Note 4)	V_{DD} = 5V, V_O = 4.6V	−1.3		−1.1	−1.6		−0.72		
		V_{DD} = 10V, V_O = 9.5V	−2.6		−2.2	−3.6		−1.5		mA
		V_{DD} = 15V, V_O = 13.5V	−8.0		−7.2	−12		−5		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Continued)

Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 5)

CD4049UBC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		30	65	
	HIGH-to-LOW Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	
t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		45	85	
	LOW-to-HIGH Level	$V_{DD} = 10V$		25	45	ns
		$V_{DD} = 15V$		20	35	
t_{THL}	Transition Time	$V_{DD} = 5V$		30	60	
	HIGH-to-LOW Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	
t_{TLH}	Transition Time	$V_{DD} = 5V$		60	120	
	LOW-to-HIGH Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	
C_{IN}	Input Capacitance	Any Input		15	22.5	pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Note 6)

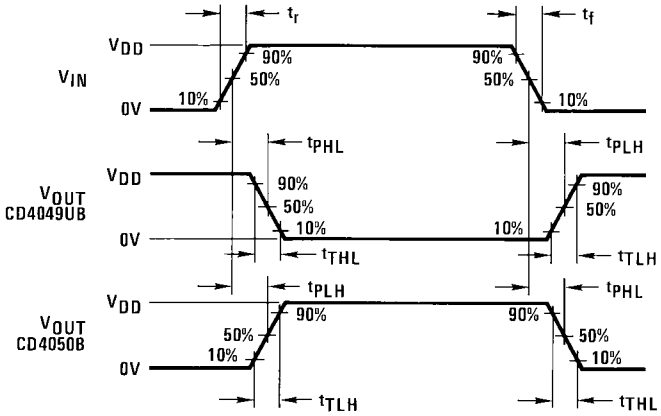
CD4050BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		60	110	
	HIGH-to-LOW Level	$V_{DD} = 10V$		25	55	ns
		$V_{DD} = 15V$		20	30	
t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		60	120	
	LOW-to-HIGH Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	
t_{THL}	Transition Time	$V_{DD} = 5V$		30	60	
	HIGH-to-LOW Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	
t_{TLH}	Transition Time	$V_{DD} = 5V$		60	120	
	LOW-to-HIGH Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

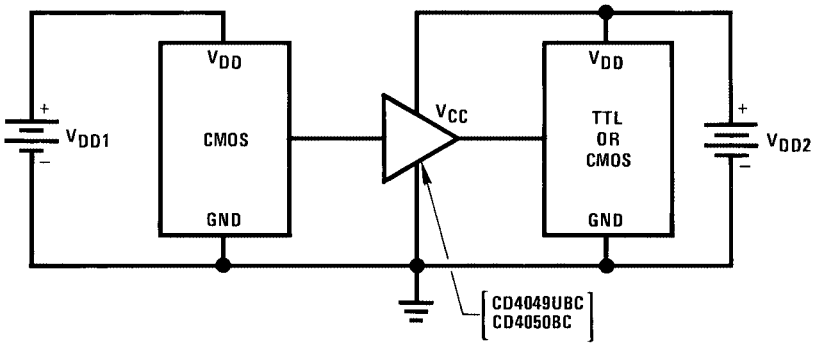
Note 6: AC Parameters are guaranteed by DC correlated testing.

Switching Time Waveforms



Typical Applications

CMOS to TLL or CMOS at a Lower V_{DD}



$V_{DD1} \geq V_{DD2}$

In the case of the CD4049UBC the output drive capability increases with increasing input voltage.
E.g., If V_{DD1} = 10V the CD4049UBC could drive 4 TTL loads.

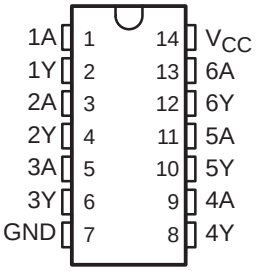
EK2

- **Dependable Texas Instruments Quality and Reliability**

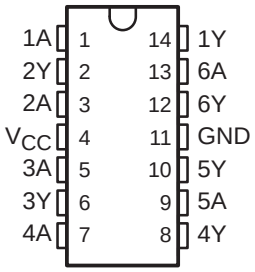
description/ordering information

These devices contain six independent inverters.

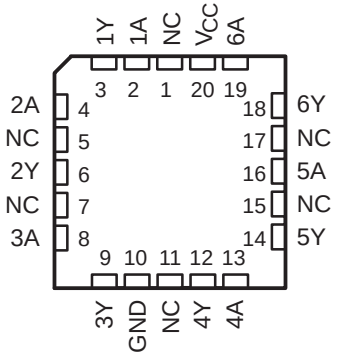
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

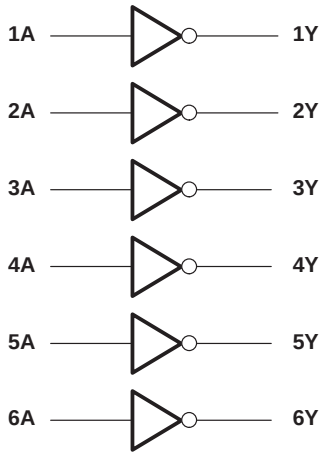
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP − N	Tube	SN7404N	SN7404N
		Tube	SN74LS04N	SN74LS04N
		Tube	SN74S04N	SN74S04N
	SOIC − D	Tube	SN7404D	7404
		Tape and reel	SN7404DR	
		Tube	SN74LS04D	LS04
		Tape and reel	SN74LS04DR	
		Tube	SN74S04D	S04
		Tape and reel	SN74S04DR	
	SOP − NS	Tape and reel	SN7404NSR	SN7404
		Tape and reel	SN74LS04NSR	74LS04
		Tape and reel	SN74S04NSR	74S04
	SSOP − DB	Tape and reel	SN74LS04DBR	LS04
−55°C to 125°C	CDIP − J	Tube	SN5404J	SN5404J
		Tube	SNJ5404J	SNJ5404J
		Tube	SN54LS04J	SN54LS04J
		Tube	SN54S04J	SN54S04J
		Tube	SNJ54LS04J	SNJ54LS04J
		Tube	SNJ54S04J	SNJ54S04J
	CFP − W	Tube	SNJ5404W	SNJ5404W
		Tube	SNJ54LS04W	SNJ54LS04W
		Tube	SNJ54S04W	SNJ54S04W
	LCCC − FK	Tube	SNJ54LS04FK	SNJ54LS04FK
		Tube	SNJ54S04FK	SNJ54S04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

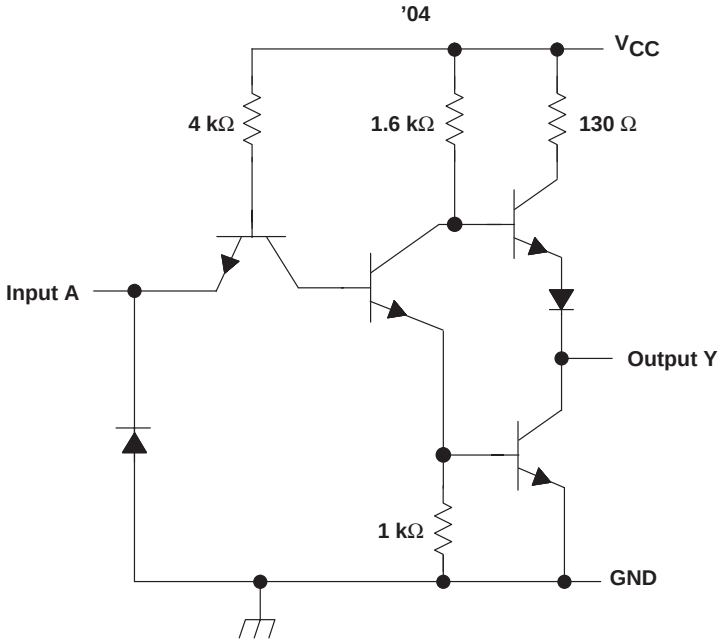
INPUT A	OUTPUT Y
H	L
L	H

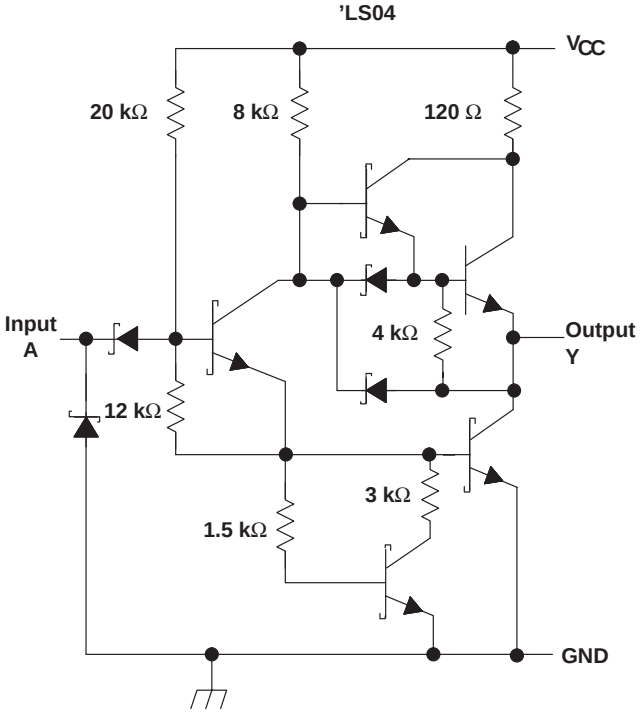
logic diagram (positive logic)

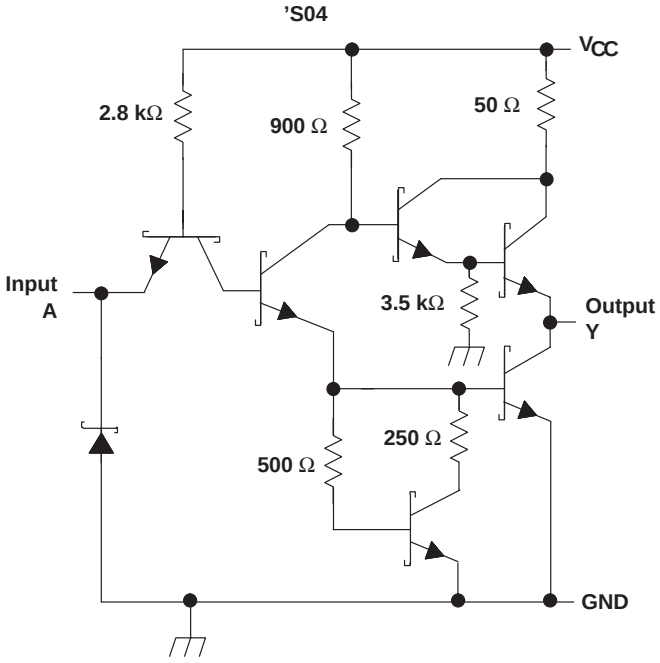


$Y = \overline{A}$

schematics (each gate)







Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: '04, 'S04 . . . . . 5.5 V
'LS04 . . . . . 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			SN5404			SN7404			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}¶	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			6	12		6	12	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			18	33		18	33	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5404 SN7404			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 400 Ω, C_L = 15 pF		12	22	ns
t_{PHL}					8	15	

recommended operating conditions (see Note 3)

		SN54LS04			SN74LS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS04			SN74LS04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4			0.4	V
			I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS04 SN74LS04			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

recommended operating conditions (see Note 3)

		SN54S04			SN74S04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

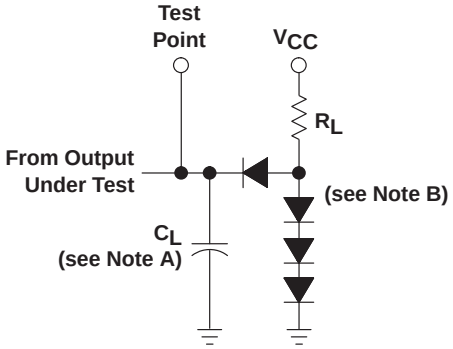
PARAMETER	TEST CONDITIONS†			SN54S04			SN74S04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			15	24		15	24	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			30	54		30	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

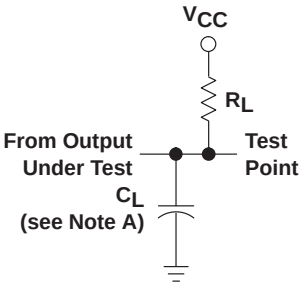
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54S04 SN74S04			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 15 pF		3	4.5	ns
t_{PHL}						3	5	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 50 pF		4.5		ns
t_{PHL}						5		

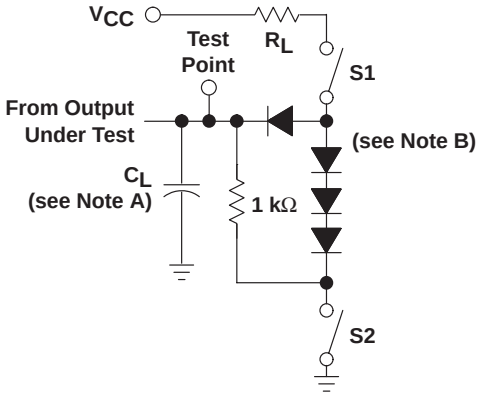
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES



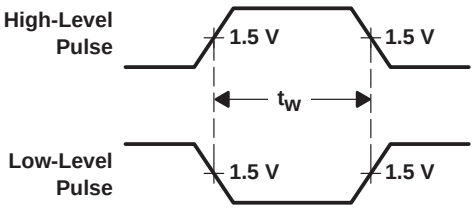
**LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS**



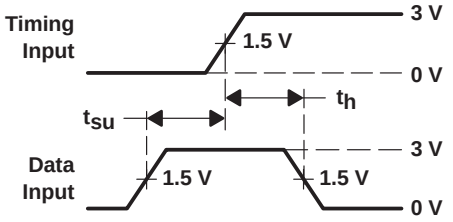
**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**



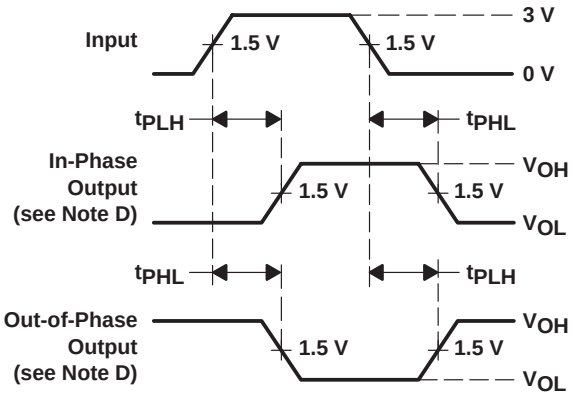
**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**



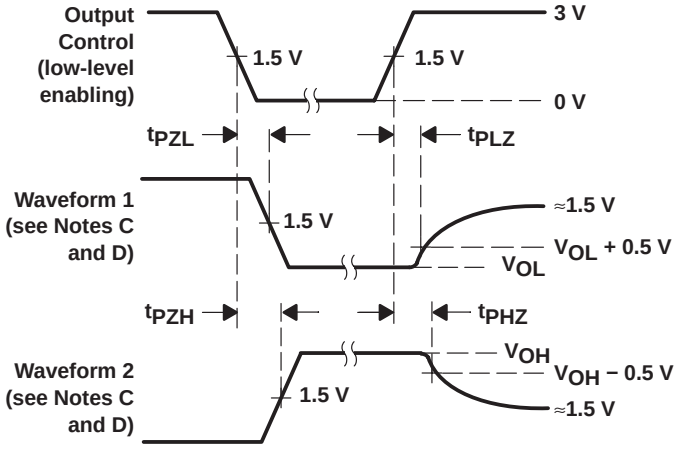
**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

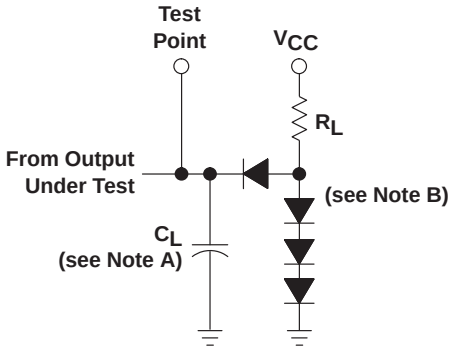


**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

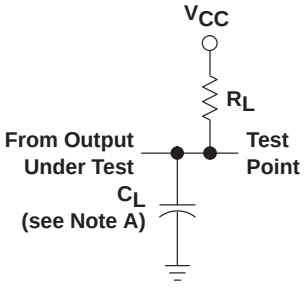
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

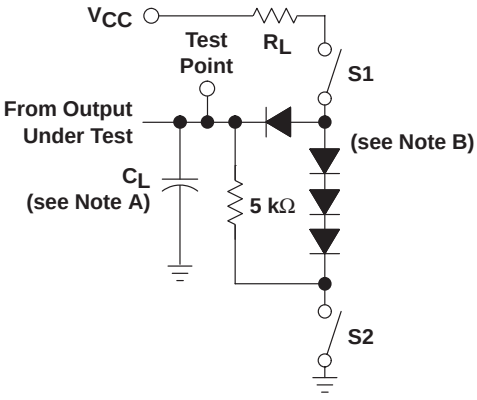
PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



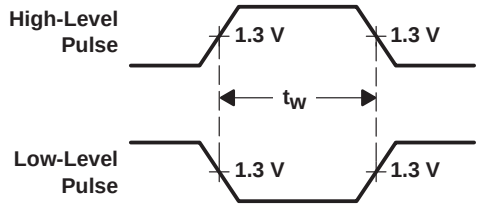
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



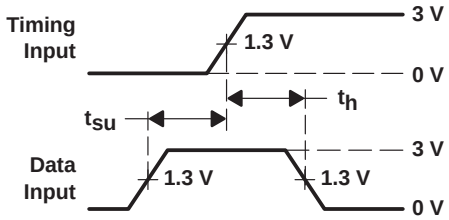
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



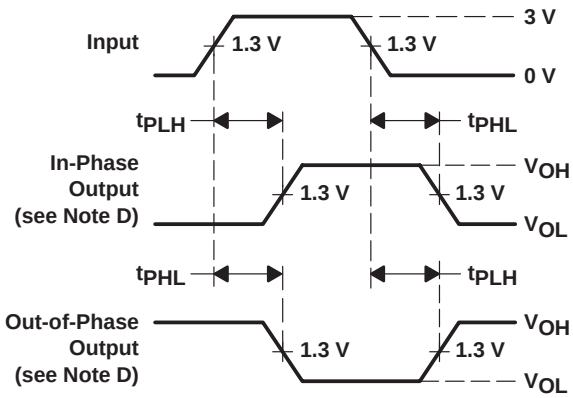
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



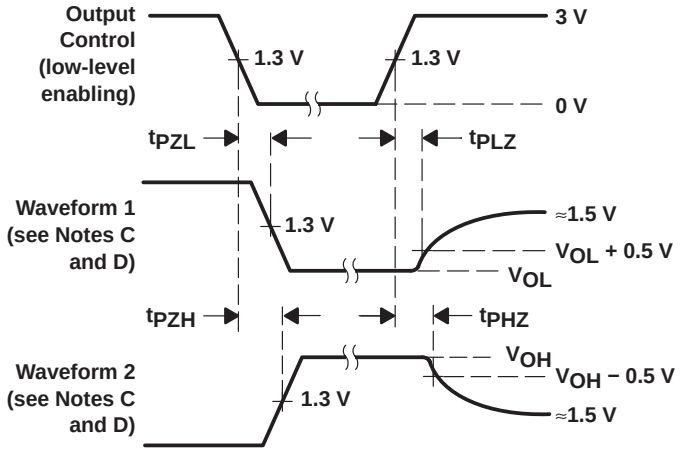
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.
G. The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms