Digital Integrated Circuits

A Design Perspective (2’nd edition - 2003)

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Transistor Revolution

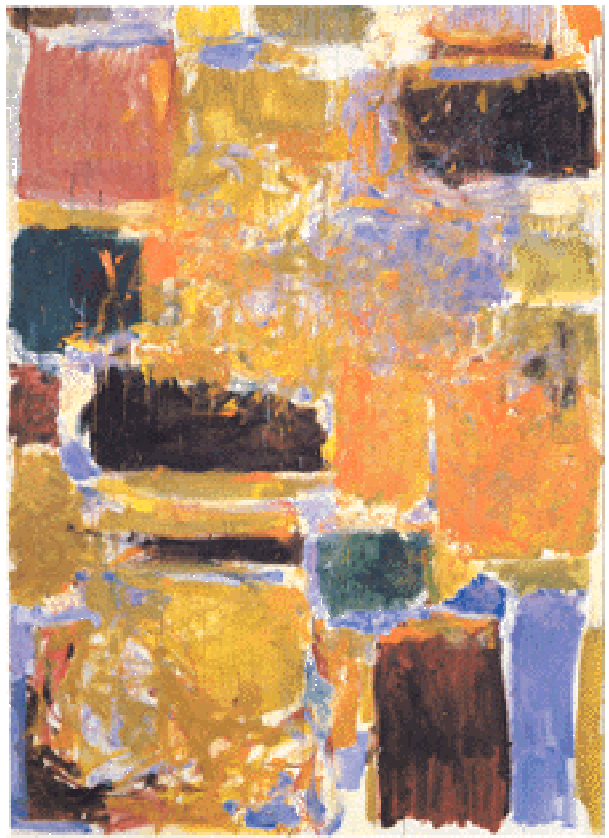
- Transistor –Bardeen (Bell Labs) in 1947
- Bipolar transistor – Schockley in 1949
- First bipolar digital logic gate – Harris in 1956
- First monolithic IC – Jack Kilby in 1959
- First commercial IC logic gates – Fairchild 1960
- TTL – 1962 into the 1990’s
- ECL – 1974 into the 1980’s

MOSFET Technology

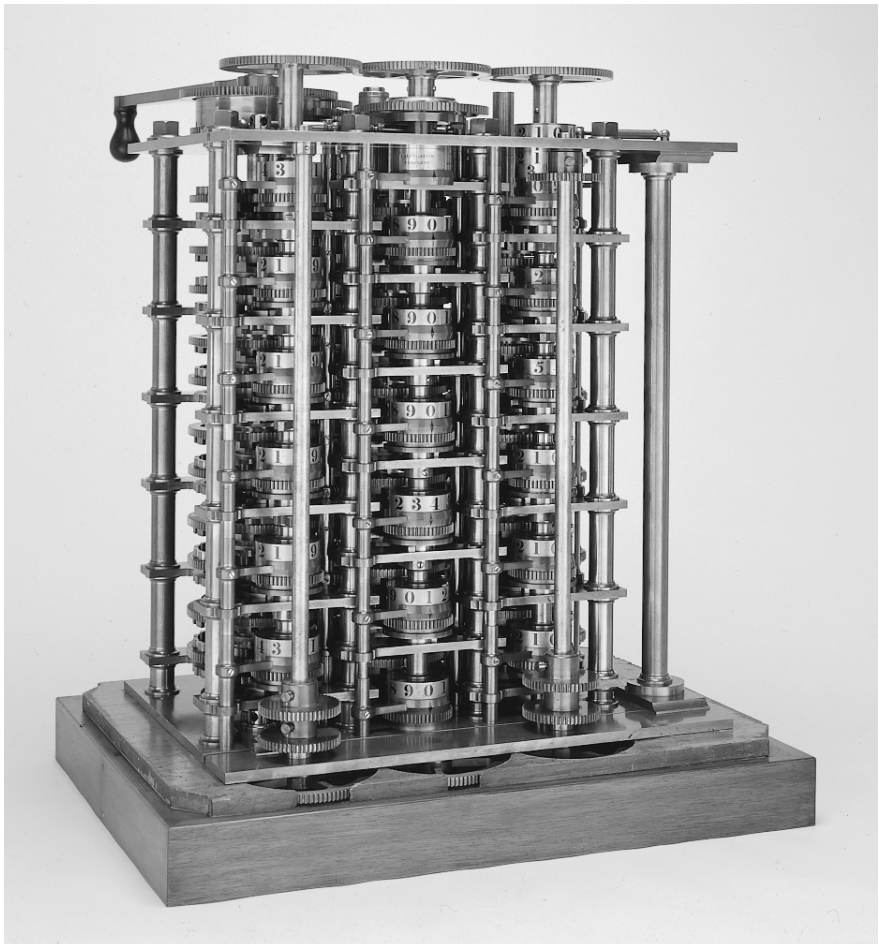
- MOSFET transistor - Lilienfeld (Canada) in 1925 and Heil (England) in 1935
- CMOS – 1960's, but plagued with manufacturing problems
- PMOS in 1960's (calculators)
- NMOS in 1970's (4004, 8080) – for speed
- CMOS in 1980's – preferred MOSFET technology because of power benefits
- BiCMOS, Gallium-Arsenide, Silicon-Germanium
- SOI, Copper-Low K, …

Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?



The First Computer

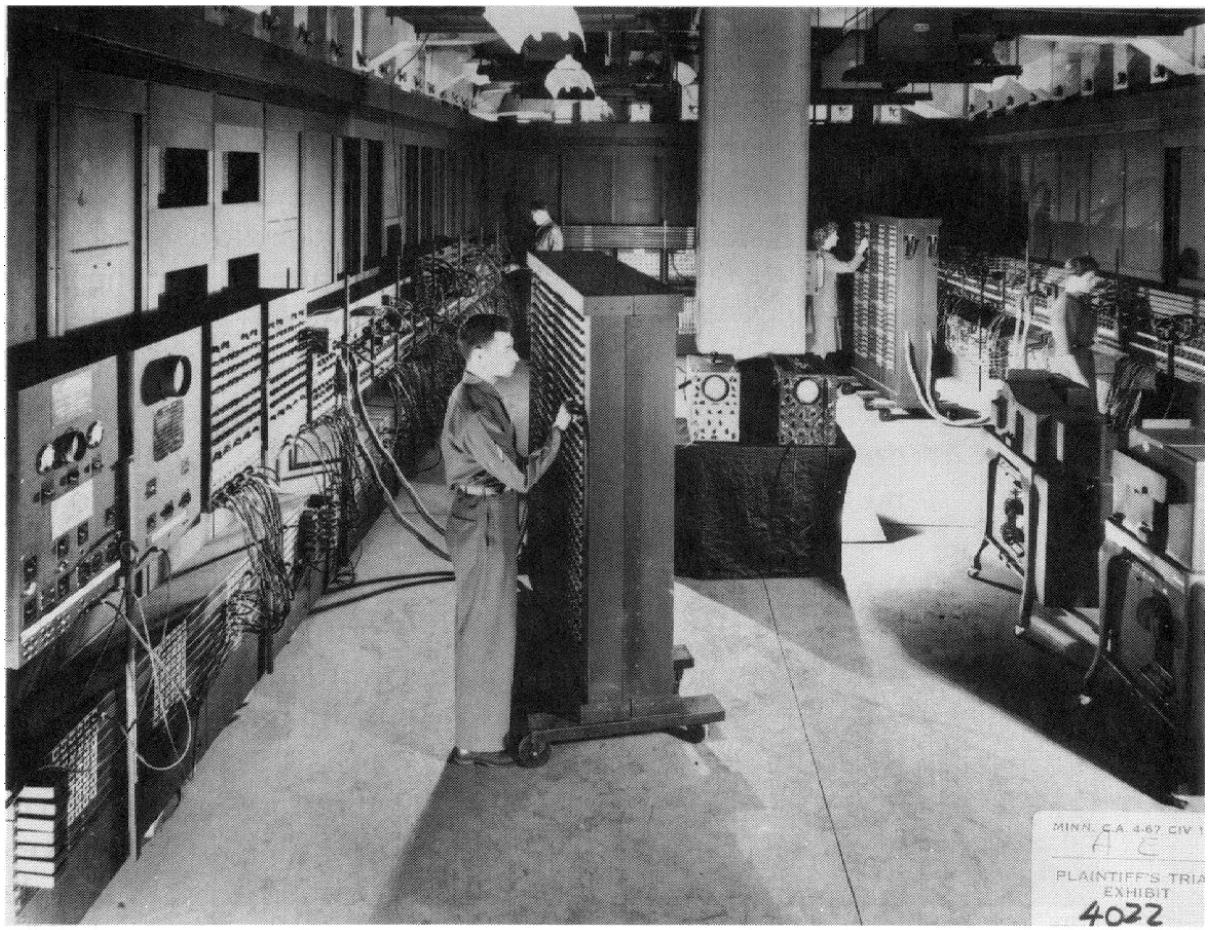


The Babbage Difference Engine (1832)

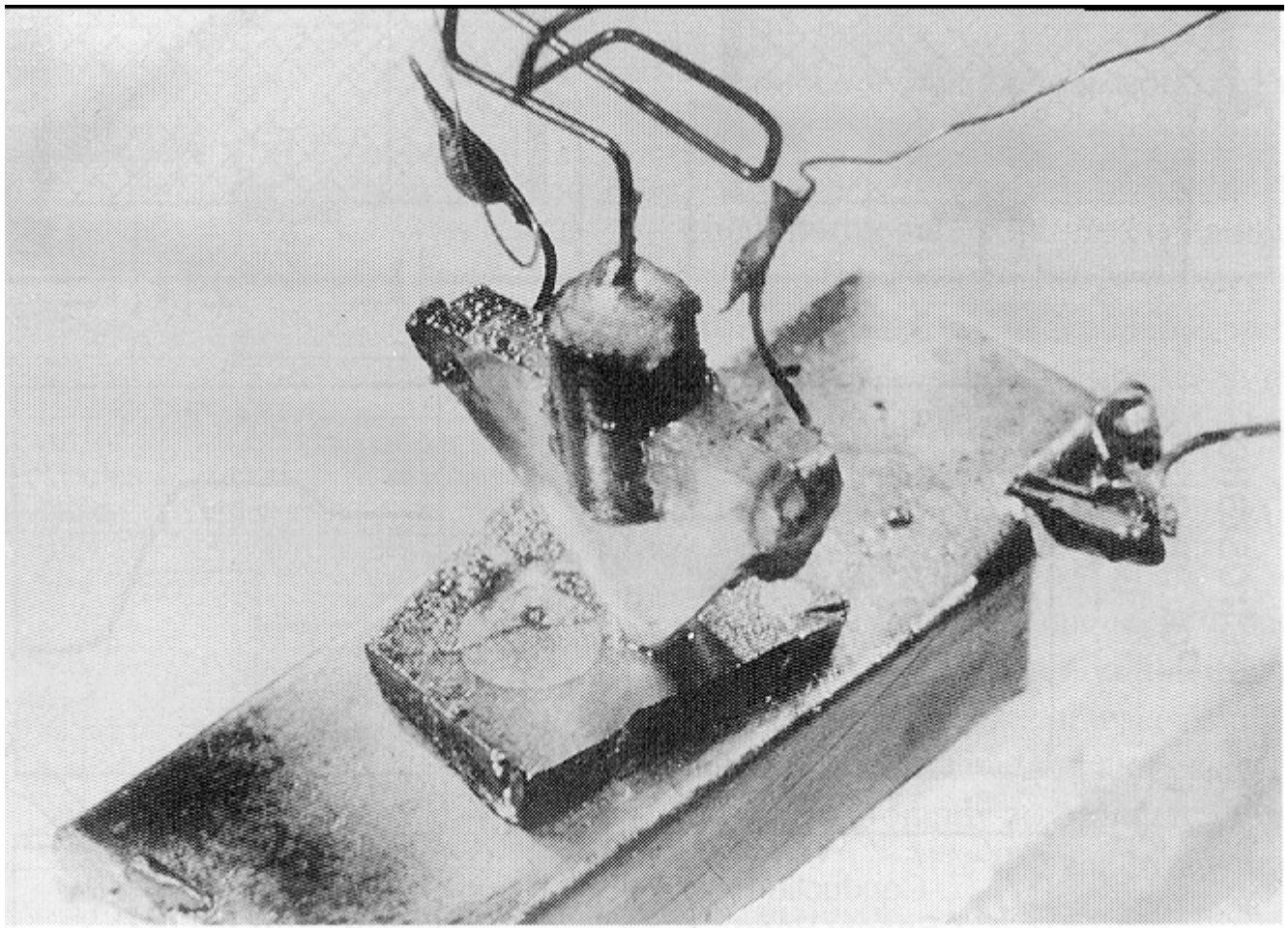
25,000 parts

cost: £17,470

ENIAC - The first electronic computer (1946)

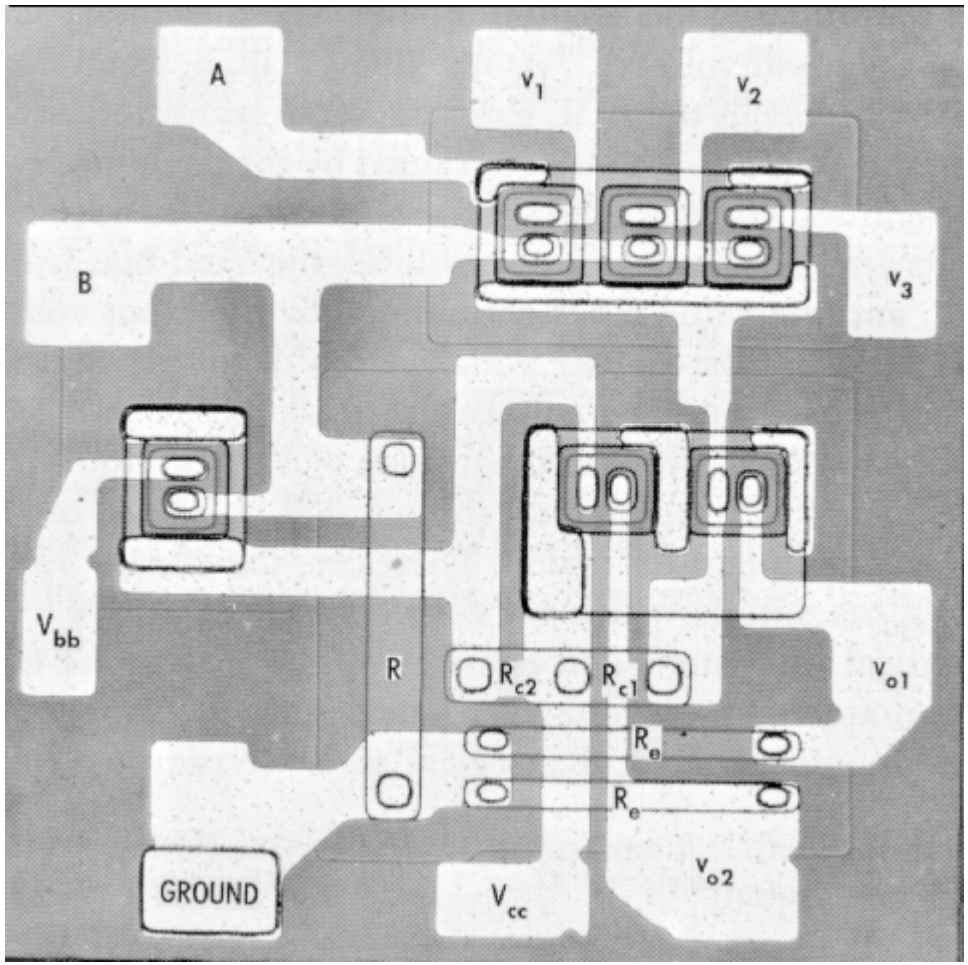


The Transistor Revolution



First transistor
Bell Labs, 1948

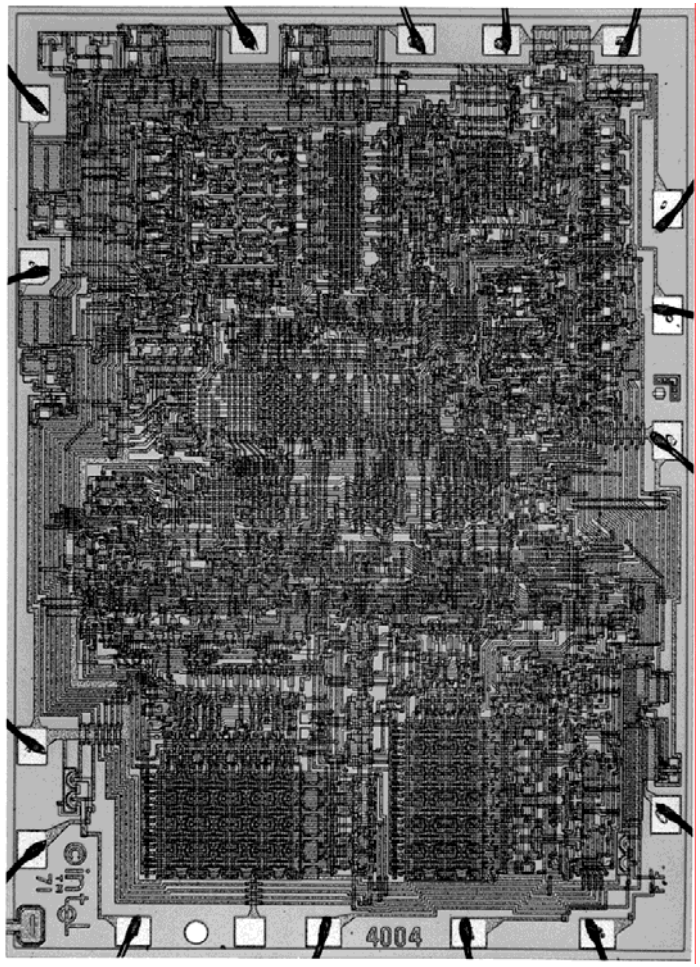
The First Integrated Circuits



Bipolar logic
1960's

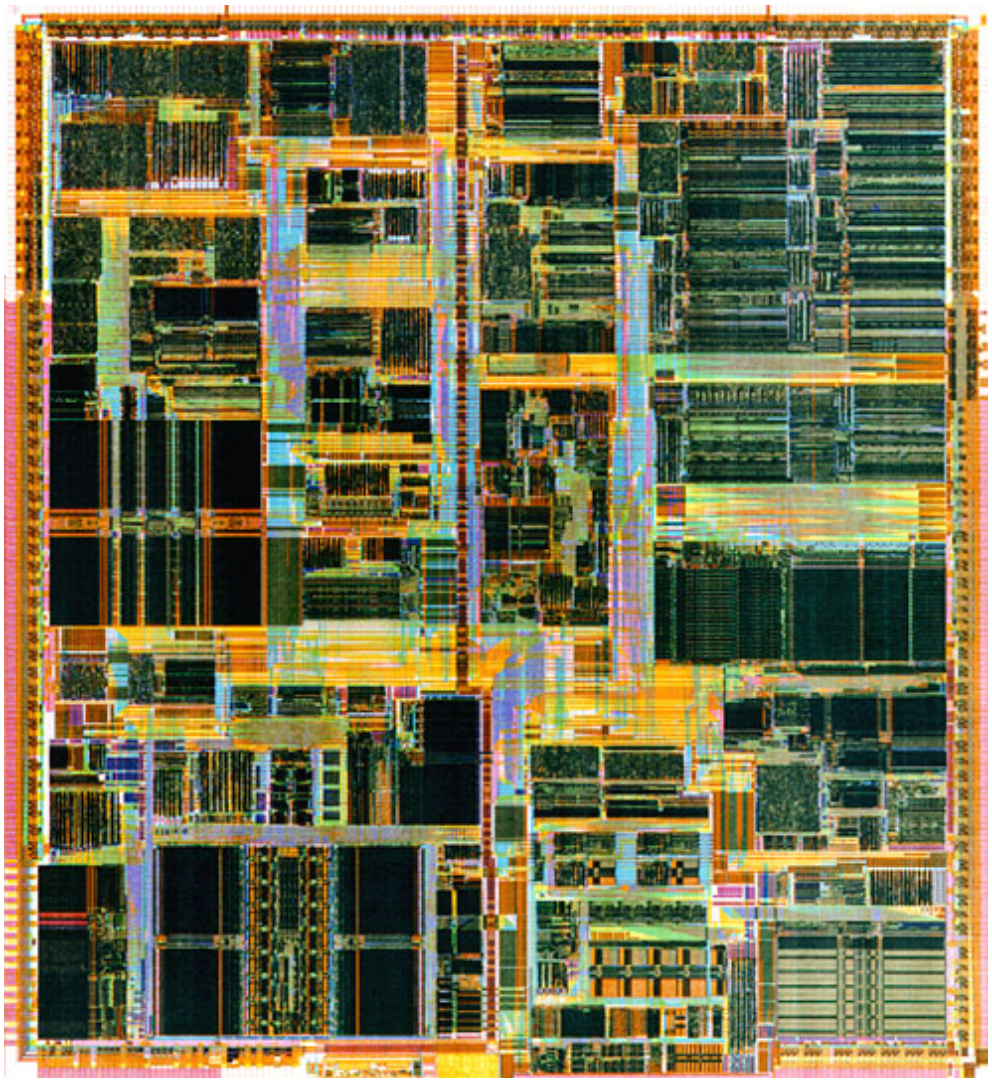
ECL 3-input Gate
Motorola 1966

Intel 4004 Micro-Processor



1971
1000 transistors
1 MHz operation

Intel Pentium (IV) microprocessor



2001

42 million transistors

2 GHz operation

0.13μ process

55 million transistors

2.4GHz clock

145mm^2

Moore's Law

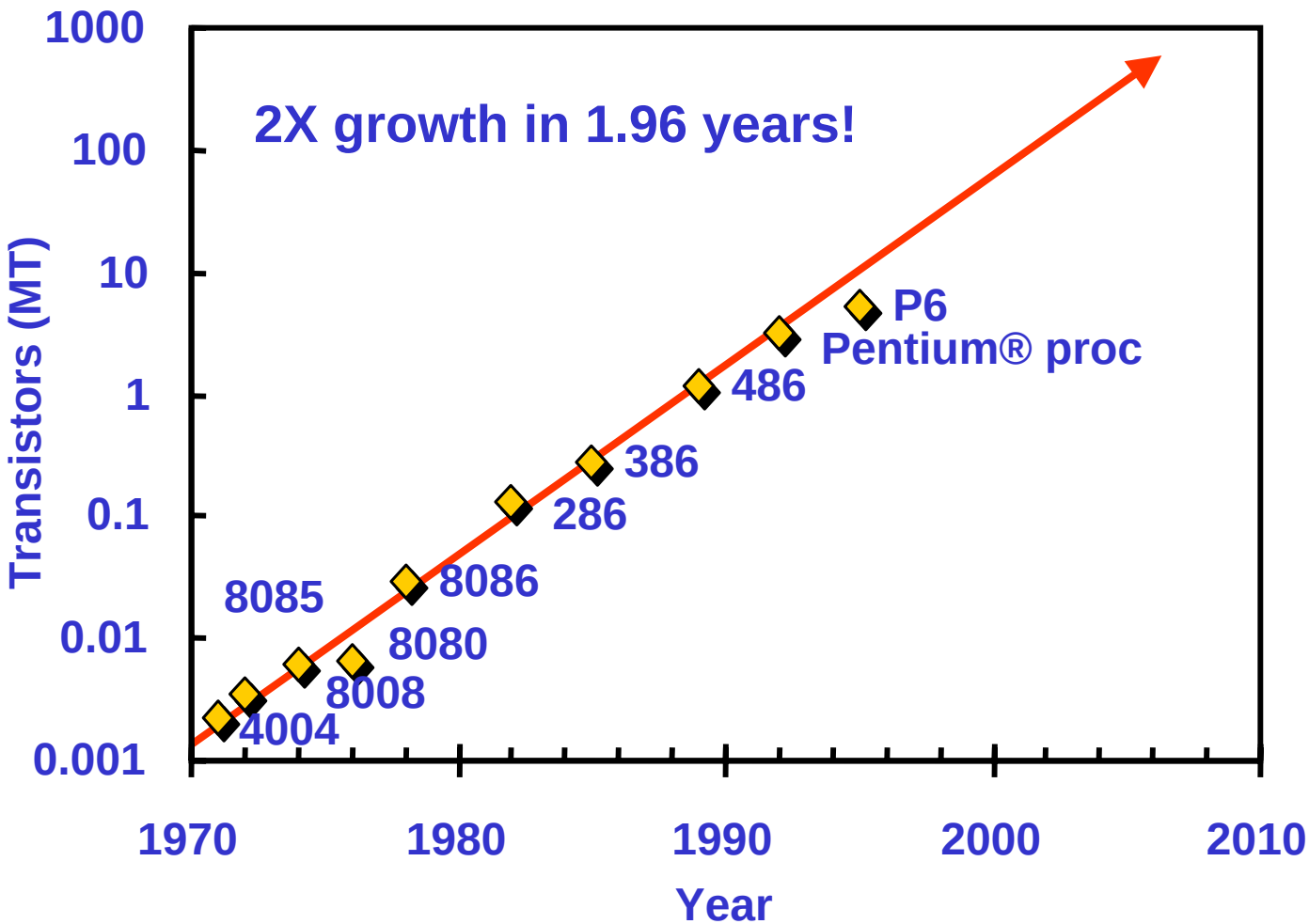
- In 1965, Gordon Moore predicted that the number of transistors that can be integrated on a die would double every 18 to 14 months (i.e., grow exponentially with time).
- Amazingly visionary – million transistor/chip barrier was crossed in the 1980's.
  - 2300 transistors, 1 MHz clock (Intel 4004) - 1971
  - 16 Million transistors (Ultra Sparc III)
  - 42 Million, 2 GHz clock (Intel P4) - 2001
  - 140 Million transistor (HP PA-8500)

State-of-the Art: Lead Microprocessors

Processor	Alpha 21264B	AMD Athlon	HP PA-8600	IBM Power3-II	Intel Pentium III	Intel Pentium 4	MIPS R12000	Sun Ultra-II	Sun Ultra-III
Clock Rate	833MHz	1.33GHz	552MHz	450MHz	1.0GHz	1.7GHz	400MHz	480MHz	900MHz
Cache (I/D/L2)	64K/64K	64K/64K/256K	512K/1M	32K/64K	16K/16K/256K	12K/8K/256K	32K/32K	16K/16K	32K/64K
Issue Rate	4 issue	3 x86 instr	4 issue	4 issue	3 x86 instr	3 ROPs	4 issue	4 issue	4 issue
Pipeline Stages	7/9 stages	9/11 stages	7/9 stages	7/8 stages	12/14 stages	22/24 stages	6 stages	6/9 stages	14/15 stages
Out of Order	80 instr	72ROPs	56 instr	32 instr	40 ROPs	126 ROPs	48 instr	None	None
Rename regs	48/41	36/36	56 total	16 int/24 fp	40 total	128 total	32/32	None	None
BHT Entries	4K x 9 bits	4K x 2 bits	2K x 2 bits	2K x 2 bits	≥ 512	4K x 2 bits	2K x 2 bits	512 x 2 bits	16K x 2 bits
TLB Entries	128/128	280/288	120 unified	128/128	32I/64D	128I/64D	64 unified	64I/64D	128I/512D
Memory B/W	2.66GB/s	2.1GB/s	1.54GB/s	1.6GB/s	1.06GB/s	3.2GB/s	539 MB/s	1.9GB/s	4.8GB/s
Package	CPGA-588	PGA-462	LGA-544	SCC-1088	PGA-370	PGA-423	CPGA-527	CLGA-787	1368 FC-LGA
IC Process	0.18µ 6M	0.18µ 6M	0.25µ 2M	0.22µ 6M	0.18µ 6M	0.18µ 6M	0.25µ 4M	0.29µ 6M	0.18µ 7M
Die Size	115mm^2	117mm^2	477mm^2	163mm^2	106mm^2	217mm^2	204mm^2	126mm^2	210mm^2
Transistors	15.4 million	37 million	130 million	23 million	24 million	42 million	7.2 million	3.8 million	29 million
Est mfg cost	$160	$62	$330	$110	$39	$100	$125	$70	$145
Power (max)	75W*	76W	60W*	36W*	30W	64W(TDP)	25W*	20W*	65W
Availability	1Q01	1Q01	3Q00	4Q00	2Q00	2Q01	2Q00	3Q0	4Q00

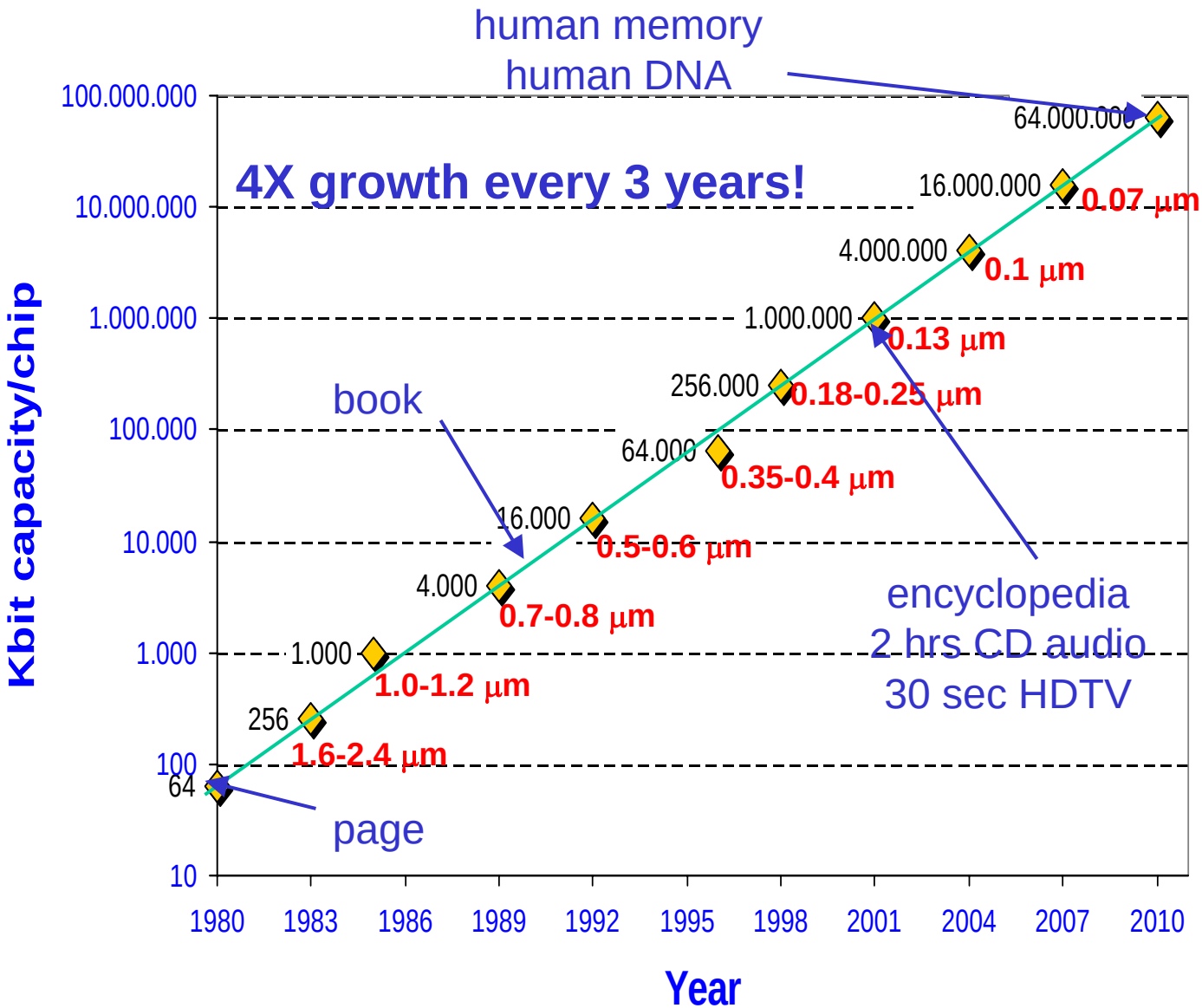
Moore's Law in Microprocessors

Transistors on lead microprocessors double every 2 years

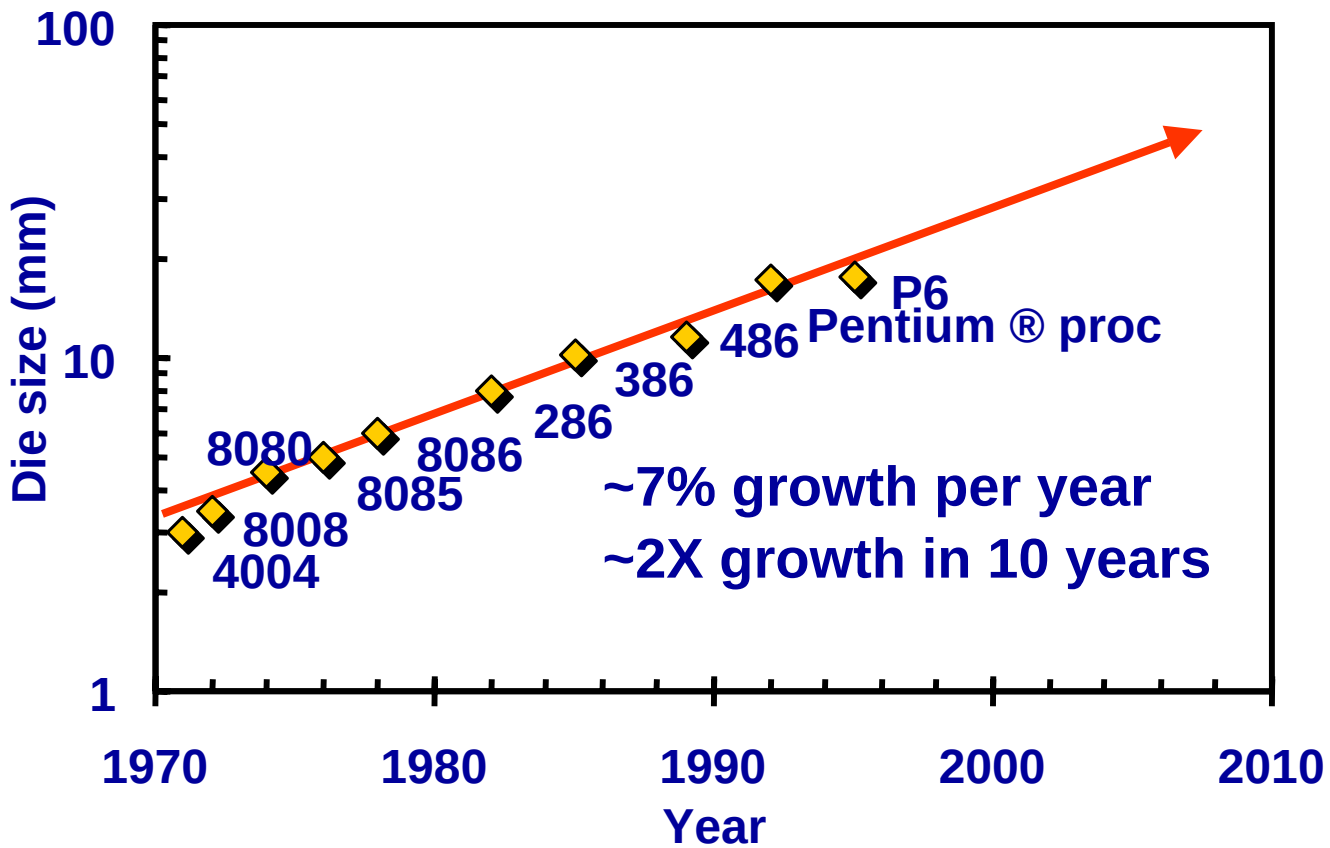


Courtesy, Intel

Evolution in DRAM Chip Capacity



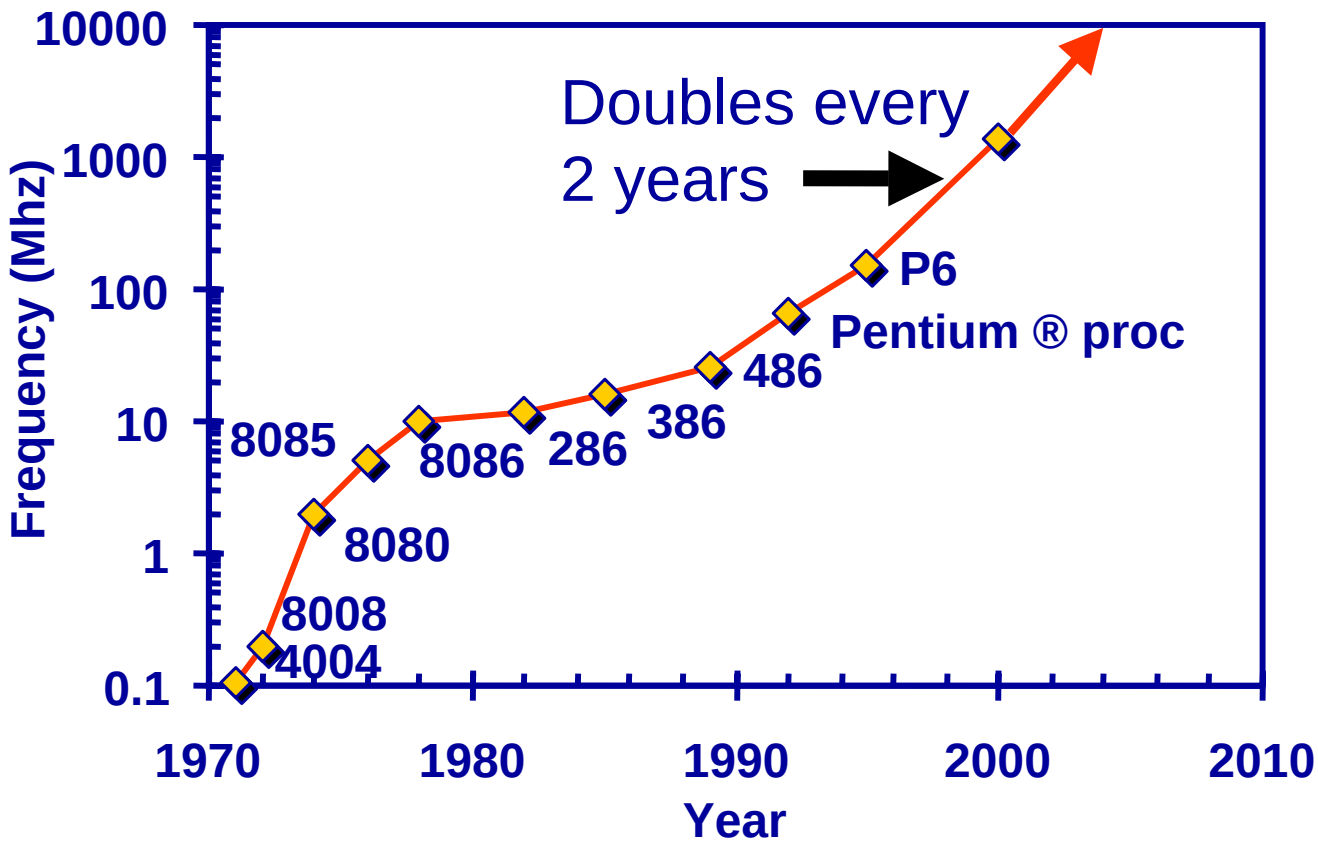
Die Size Growth



Die size grows by 14% to satisfy Moore's Law

Courtesy, Intel

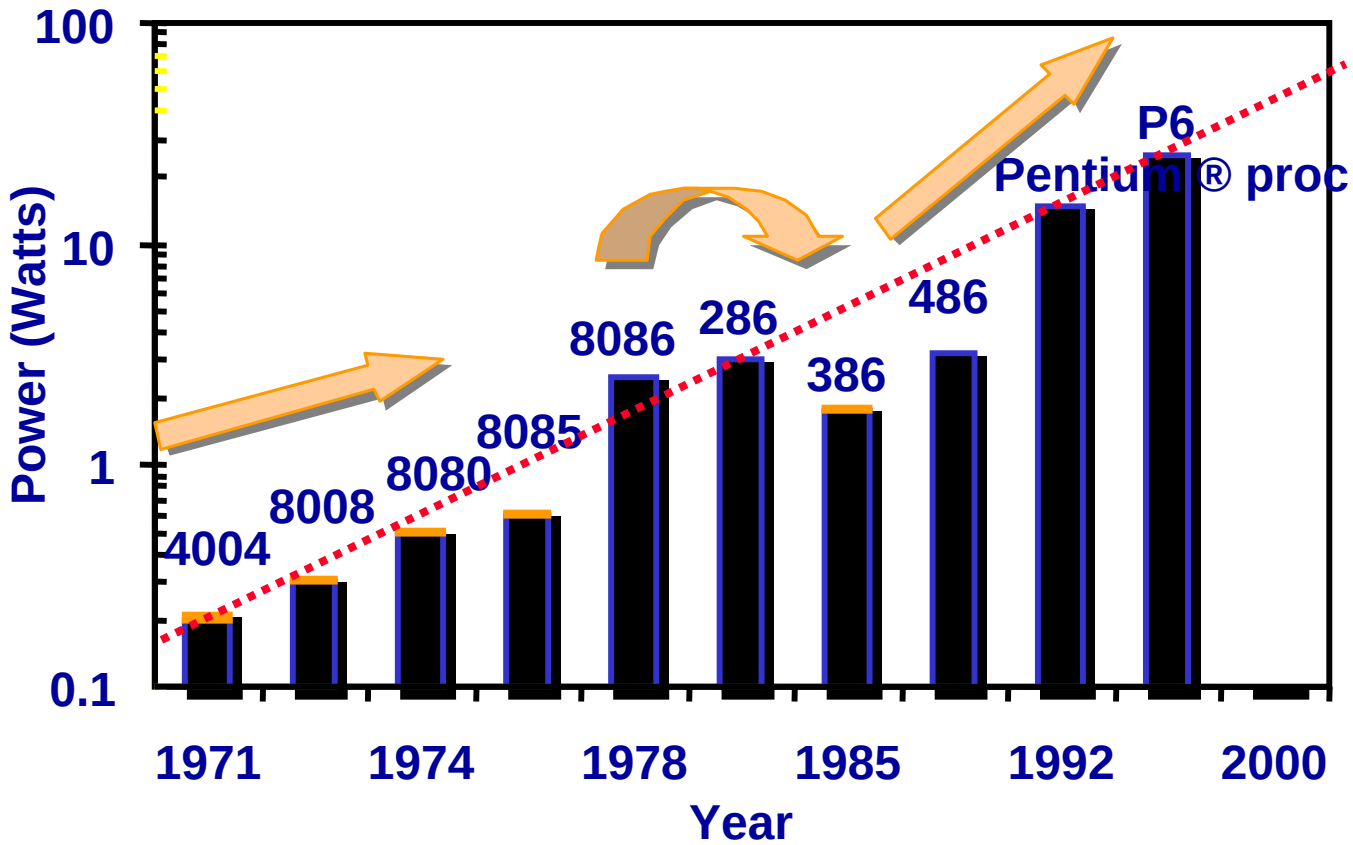
Clock Frequency



Lead Microprocessors frequency doubles every 2 years

Courtesy, Intel

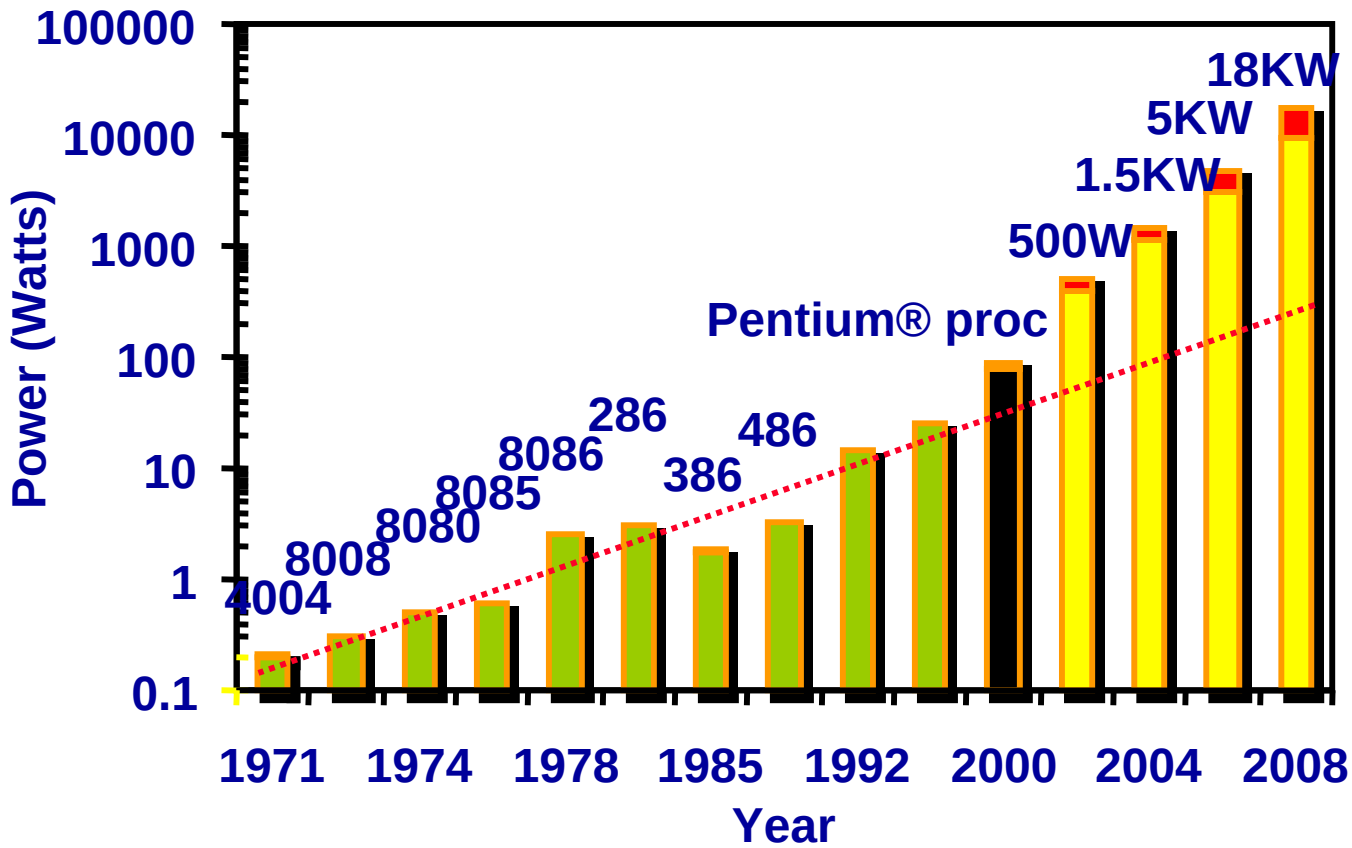
Power Dissipation



Lead Microprocessors power continues to increase

Courtesy, Intel

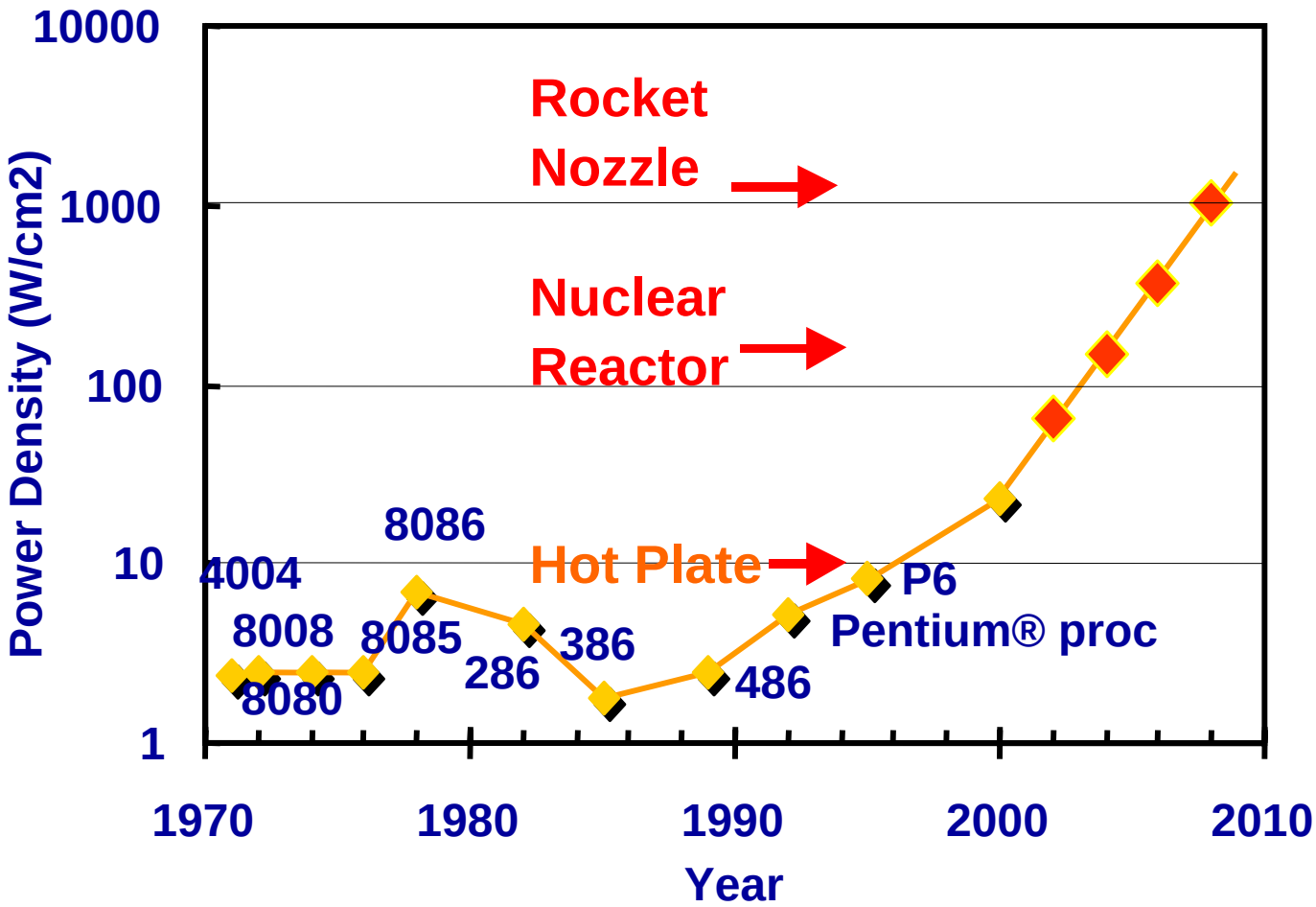
Power will be a major problem



Power delivery and dissipation will be prohibitive

Courtesy, Intel

Power Density

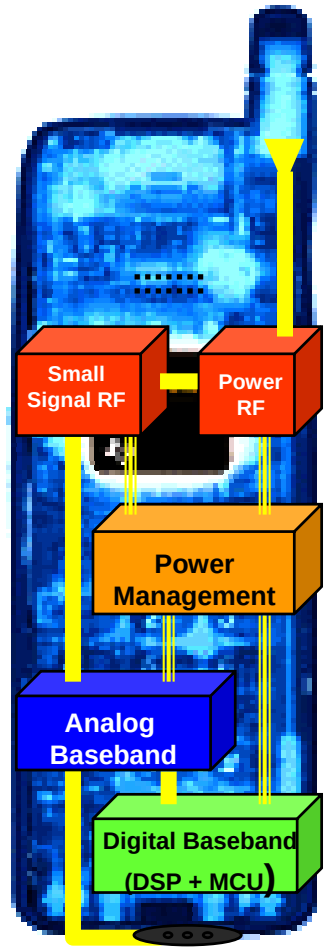


Power density too high to keep junctions at low temp

Courtesy, Intel

Not Only Microprocessors

Cell Phone

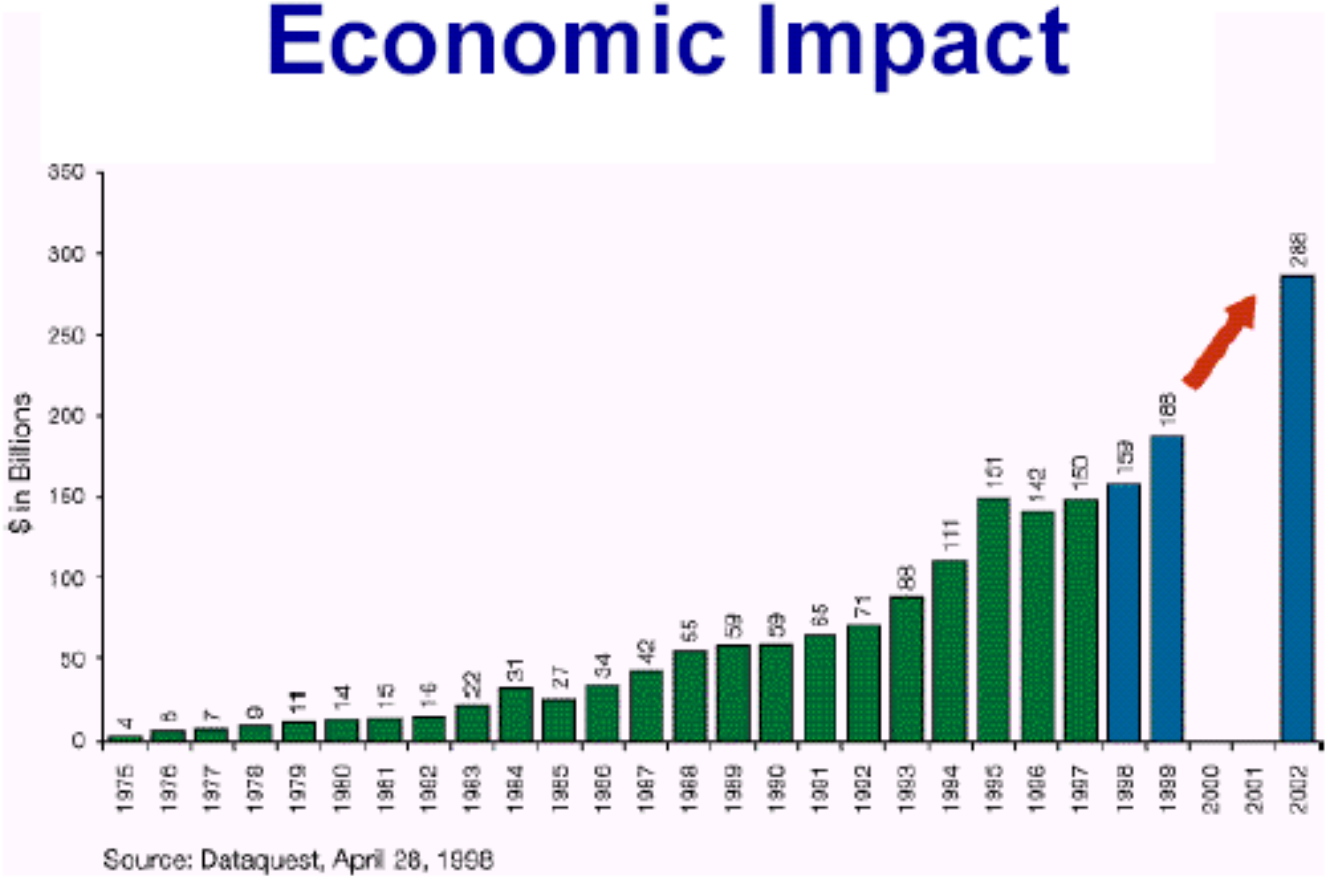


Digital Cellular Market (Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

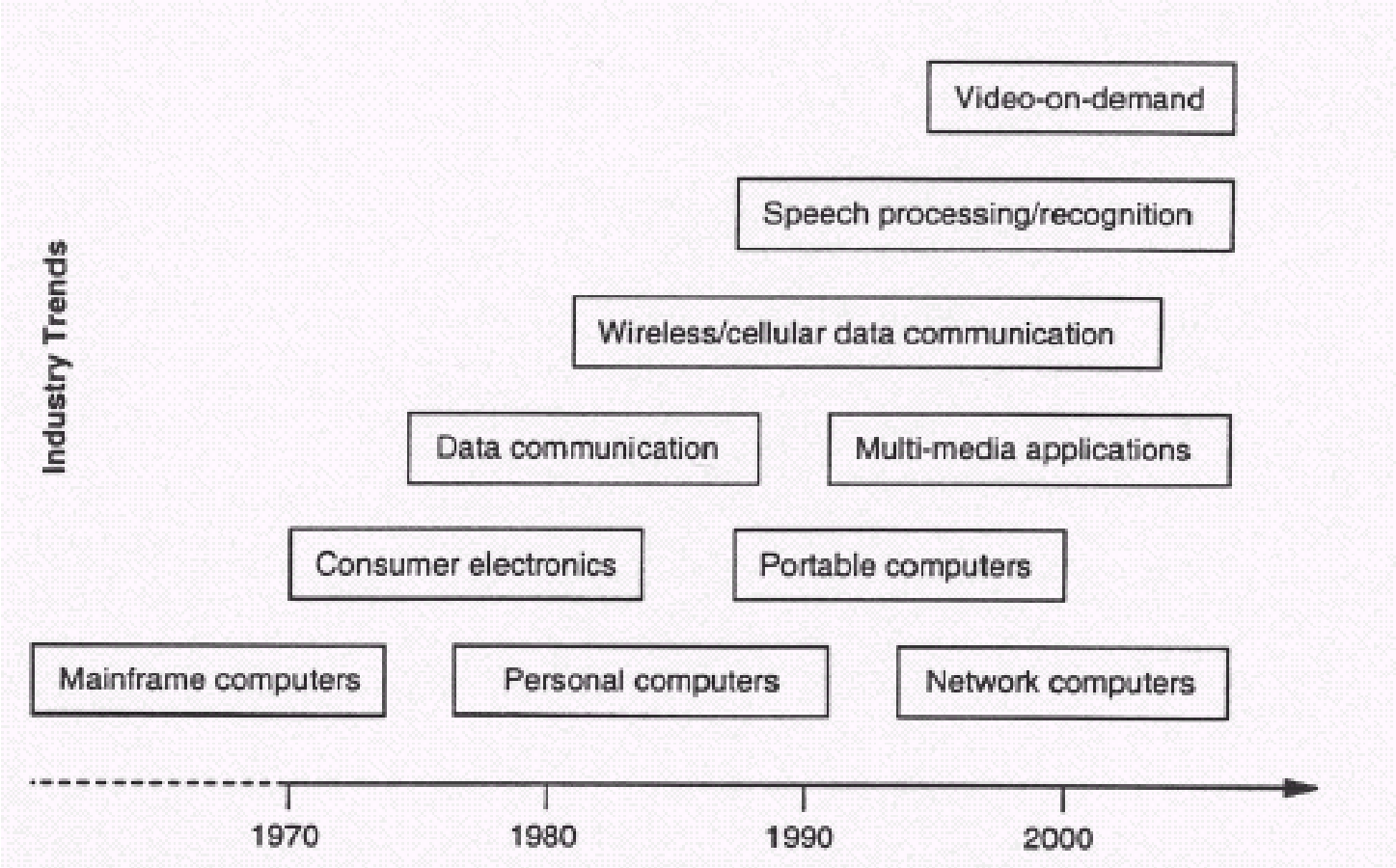
(data from Texas Instruments)

Economic Impact



As a result of the continuously increasing integration density and decreasing unit costs, the semiconductor industry has been one of the fastest growing sectors in the worldwide economy.

Industry Trends

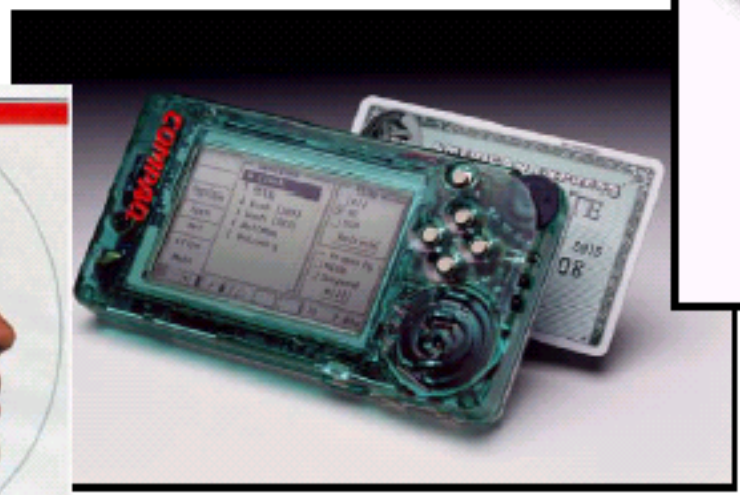


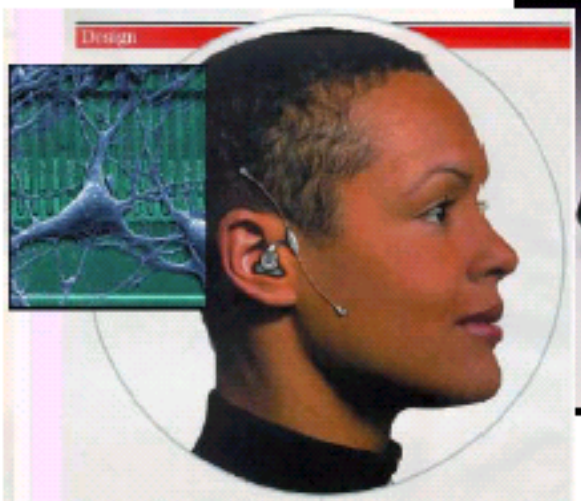
Large
Centralized
Expensive

Small / Portable
Distributed
Inexpensive

Industry Trends

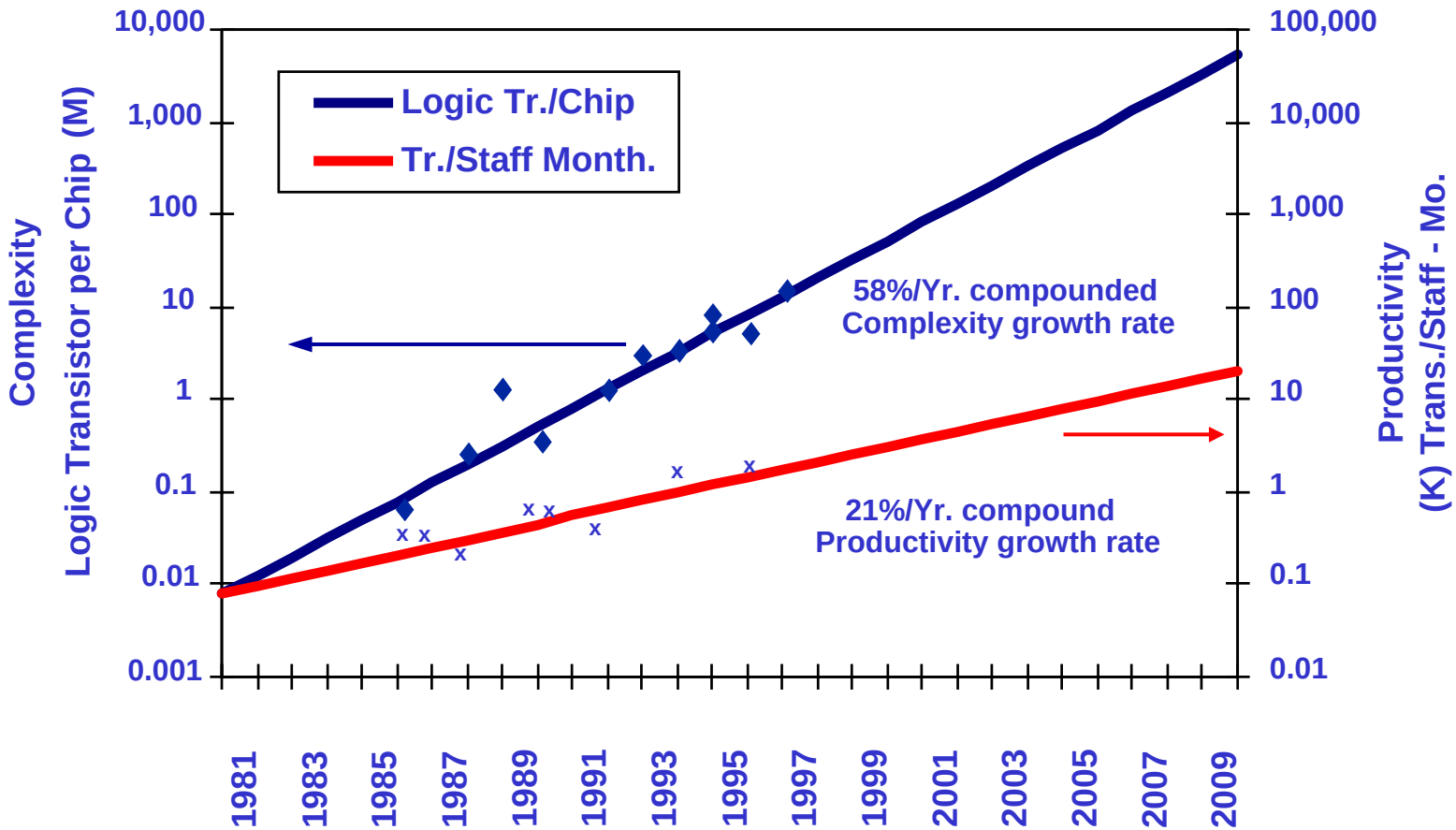
High performance
Low power dissipation
Wireless capability
etc…





More portable, wearable, and more powerful devices for ubiquitous and pervasive computing…

Design Productivity Trends



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Technology Directions: SIA Roadmap

Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Mtrans/cm^2	7	14-26	47	115	284	701
Chip size (mm^2)	170	170-214	235	269	308	354
Signal pins/chip	768	1024	1024	1280	1408	1472
Clock rate (MHz)	600	800	1100	1400	1800	2200
Wiring levels	6-7	7-8	8-9	9	9-10	10
Power supply (V)	1.8	1.5	1.2	0.9	0.6	0.6
High-perf power (W)	90	130	160	170	174	183
Battery power (W)	1.4	2.0	2.4	2.0	2.2	2.4

For Cost-Performance MPU (L1 on-chip SRAM cache; 32KB/1999 doubling every two years)

http://www.itrs.net/ntrs/publntrs.nsf

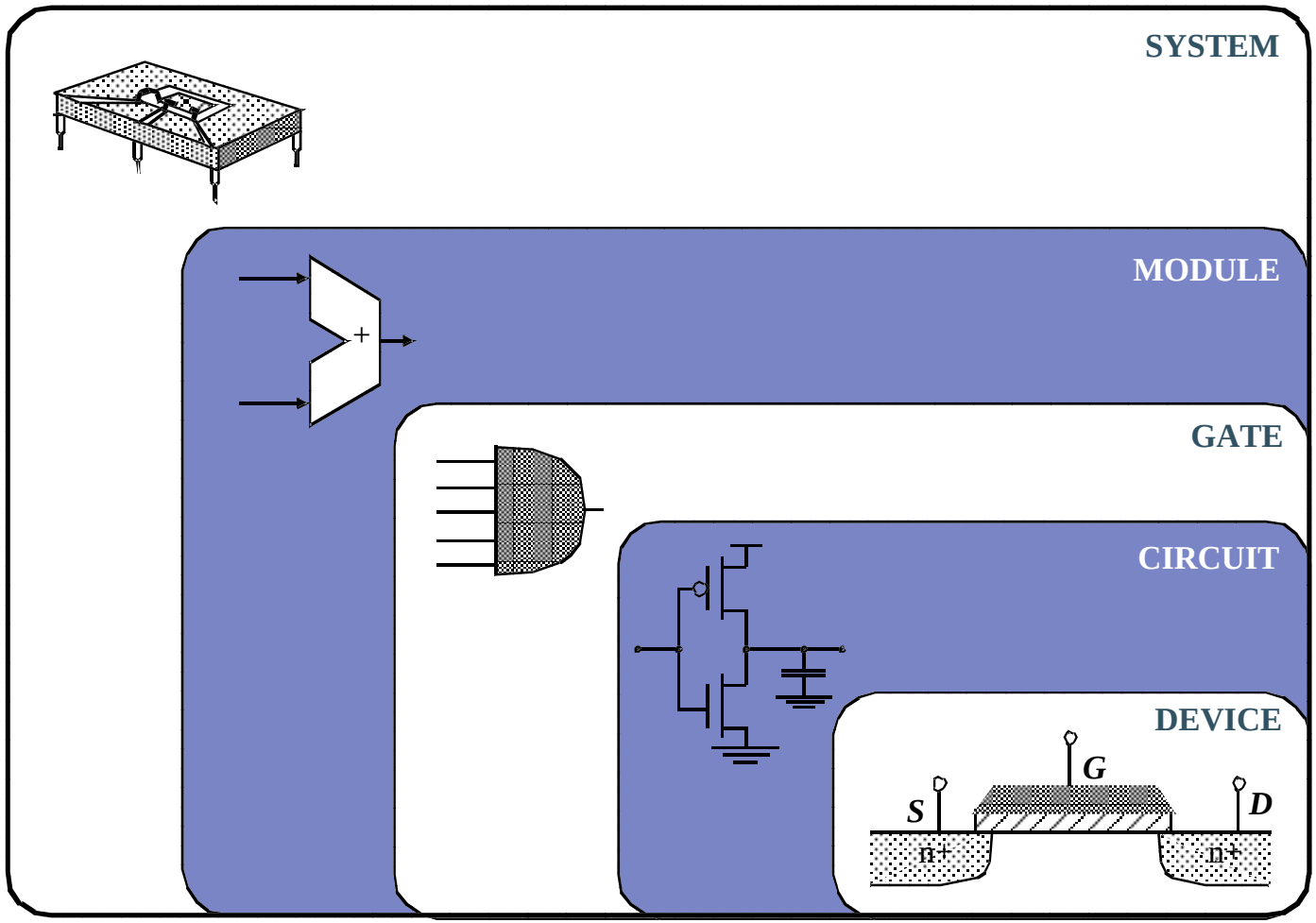
Increasing Function Density

YEAR	2002	2005	2008	2011	2014
TECHNOLOGY	130 nm	100 nm	70 nm	50 nm	35 nm
CHIP SIZE	400 mm^2	600 mm^2	750 mm^2	800 mm^2	900 mm^2
NUMBER OF TRANSISTORS (LOGIC)	**400 M**	**1 Billion**	**3 Billion**	**6 Billion**	**16 Billion**
DRAM CAPACITY	**2 Gbits**	**10 Gbits**	**25 Gbits**	**70 Gbits**	**200 Gbits**
MAXIMUM CLOCK FREQUENCY	1.6 GHz	2.0 GHz	2.5 GHz	3.0 GHz	3.5 GHz
MINIMUM SUPPLY VOLTAGE	1.5 V	1.2 V	0.9 V	0.6 V	0.6 V
MAXIMUM POWER DISSIPATION	130 W	160 W	170 W	175 W	180 W
MAXIMUM NUMBER OF I/O PINS	2500	4000	4500	5500	6000

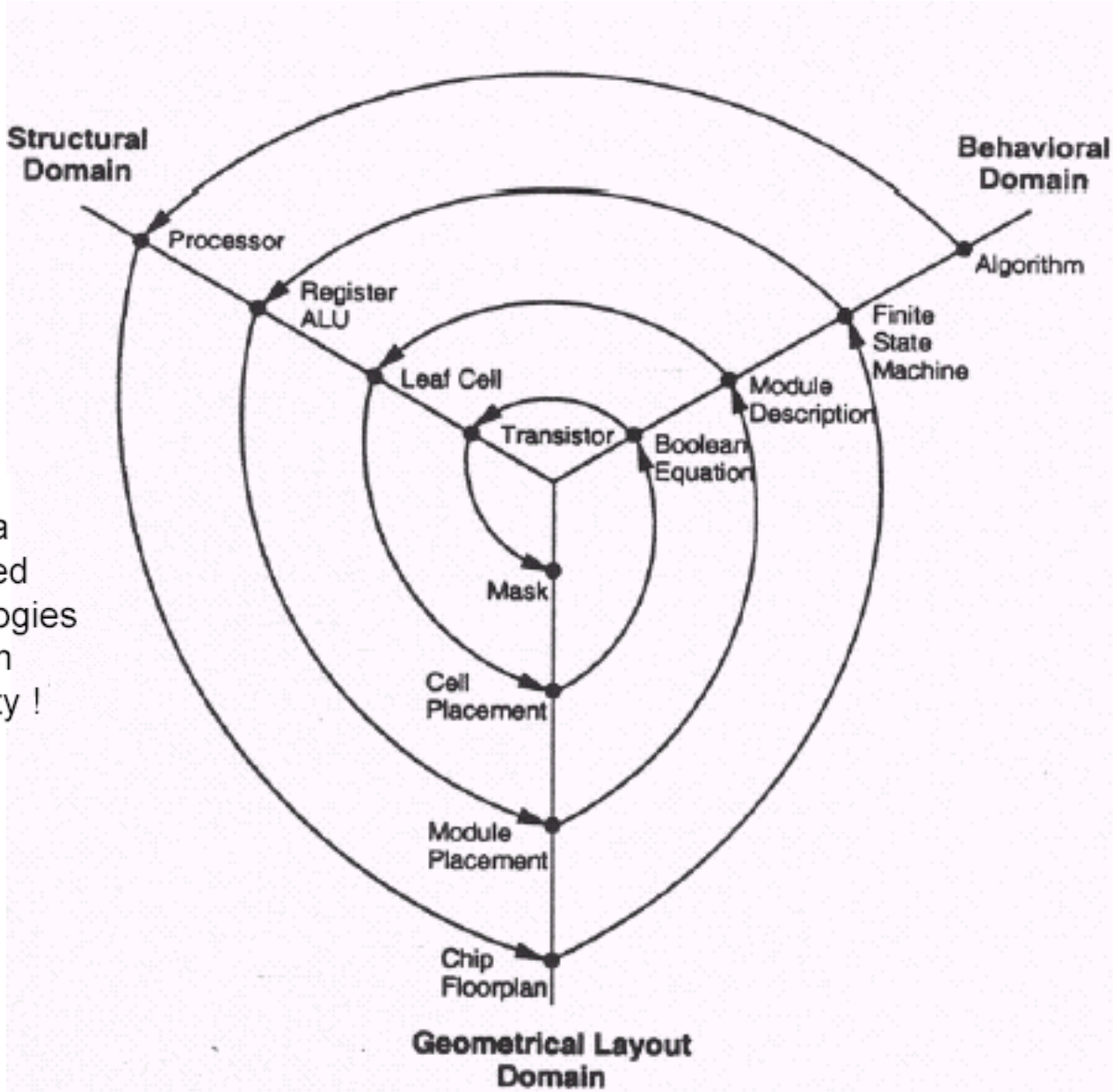
Why Scaling?

- Technology shrinks by ~0.7 per generation
- With every generation can integrate 2x more functions on a chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels



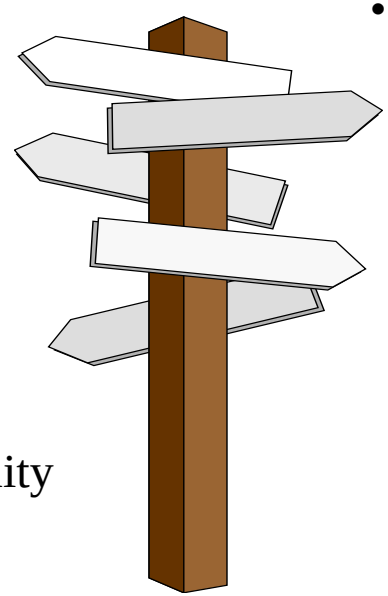
The Y-Chart



Notice: There is a need for structured design methodologies to handle the high level of complexity !

Major Design Challenges

- Microscopic issues
  - ultra-high speeds
  - power dissipation and supply rail drop
  - growing importance of interconnect
  - noise, crosstalk
  - reliability, manufacturability
  - clock distribution



- Macroscopic issues
  - time-to-market
  - design complexity (millions of gates)
  - high levels of abstractions
  - reuse and IP, portability
  - systems on a chip (SoC)
  - tool interoperability

Year	Tech.	Complexity	Frequency	3 Yr. Design Staff Size	Staff Costs
1997	0.35	13 M Tr.	400 MHz	210	$90 M
1998	0.25	20 M Tr.	500 MHz	270	$120 M
1999	0.18	32 M Tr.	600 MHz	360	$160 M
2002	0.13	130 M Tr.	800 MHz	800	$360 M

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