BME – 231 DIGITAL LOGIC DESIGN – EXPERIMENT 9 Counters and Shift Registers

Purpose:

- 1. Design a chronometer.
- 2. Design a bi-directional counter
- 3. Make a Shift Register with D flip flops and demonstrate it.

Preliminary Work:

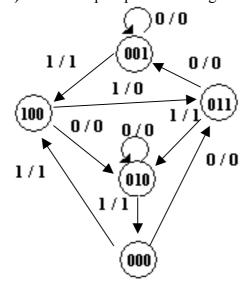
- 1. Read chapter 6 and 7 of textbook.
- **2.** A sequential circuit with two D flip-flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations:

$$A(t+1)=x'y+xA$$

$$B(t+1)=x'B+xA$$

$$z=B$$

- a) Draw the logic diagram of the circuit
- **b)** Derive the state table
- c) Derive the state diagram
- **3.** A sequential circuit has three flip-flops, A, B, C; one input, x; and one output, y. The state diagram is shown below. The circuit is to be designed by treating the unused states as don't care conditions. The final circuit must be analyzed to ensure that it is self correcting!
 - a) Use D flip flops in the design
 - **b)** Use JK flip flops in the design



- **4.** Design a chronometer which counts up seconds and shows seconds and minutes in 7 segment display (Hint: clock pulses CP are available with square wave generator, you must fix it to 5 V and 1 Hz for 1 second).

 It must count from 0:00 to 1:59 in displays! (2 minute chronometer [⊕])
- **5.** Design a bi-directional counter which counts 0, 2, 4, 6, 0, 2, ...for input x=0 (up counter) and counts 6, 4, 2, 0, 6, 4, ... for input x=1 (down counter). display (Hint: clock pulses CP are available with square wave generator, you must fix it to 5 V and 1 Hz)
- **6.** Design a 4-bit bi-directional shift register with parallel load. You must use D flip flops and your design handles 3 operations:
 - a) Shift right
 - **b)** Shift left
 - c) Parallel Load

(Hint: Your textbook includes a solution for this and clock pulses CP are available with square wave generator, you must fix it to 5 V and 1 Hz)

Experimental Work:

Construct any two of your designs for preliminary work 4, 5, 6 in EWB and simulate it