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Computer Organization
and Architecture
7th Edition

Chapter 5

Internal Memory

Semiconductor Memory Types

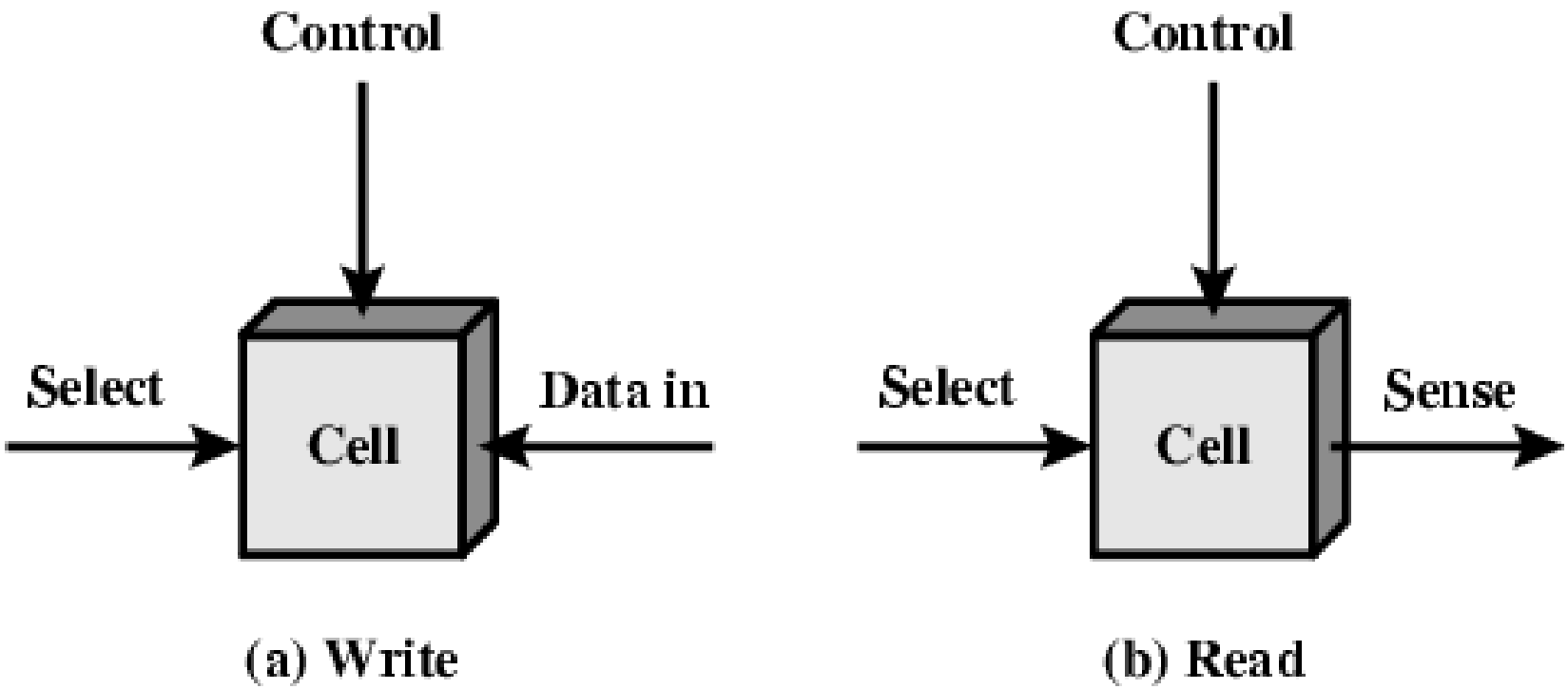
Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

Semiconductor Memory

- RAM
  - —Misnamed as all semiconductor memory is random access
  - —Read/Write
  - —Volatile
  - —Temporary storage
  - —Static or dynamic

Memory Cell Operation

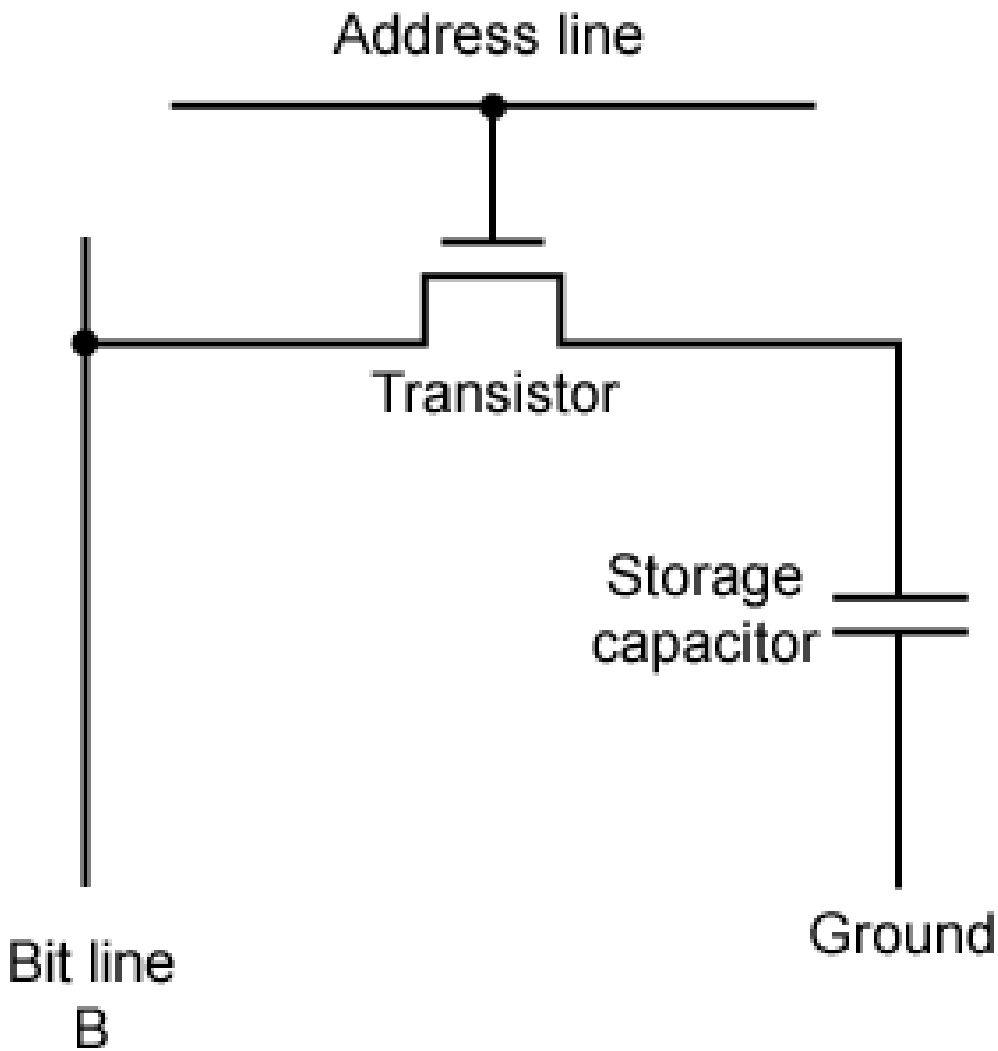
- Capable of being written into (at least once) to set the state (0 or 1)
- Capable of being read to sense the state



Dynamic RAM

- Bits stored as charge in capacitors
- Charges leak
- Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Main memory
- Essentially analogue
  - Level of charge determines value

Dynamic RAM Structure



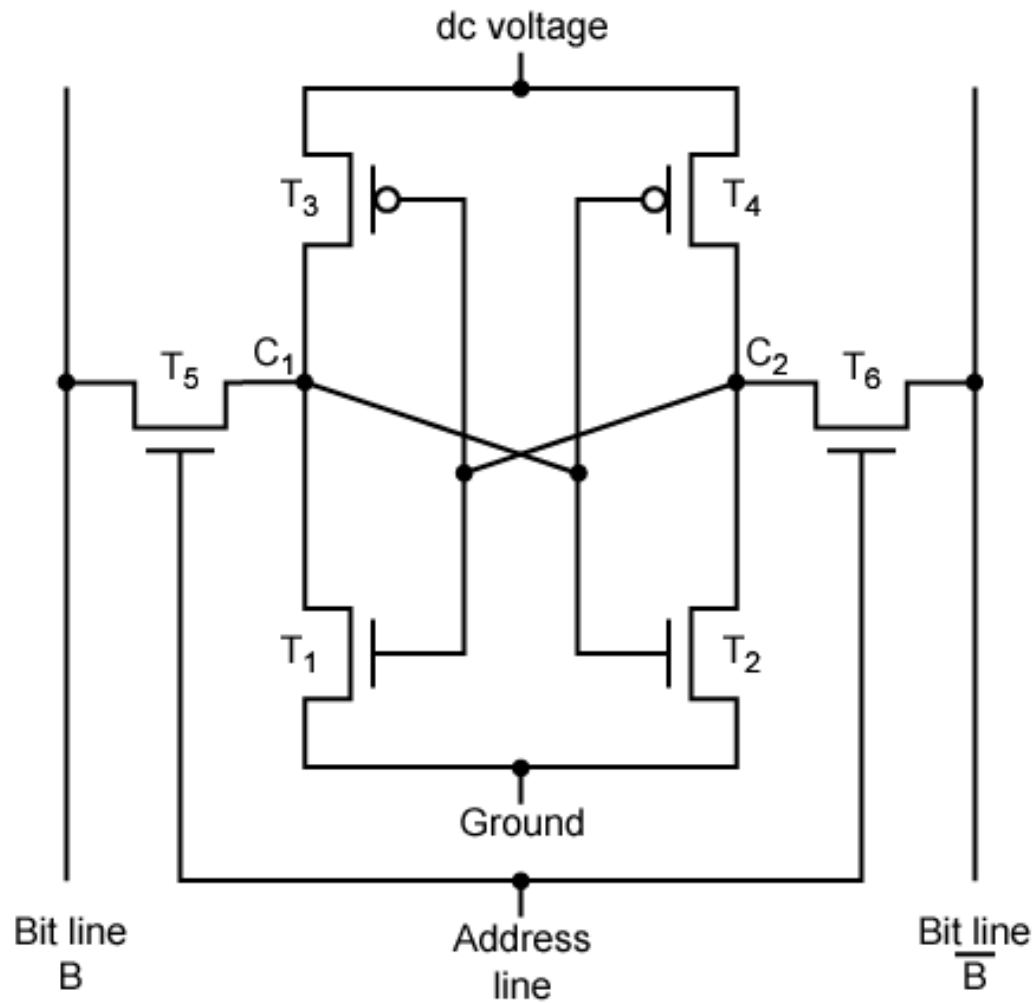
DRAM Operation

- Address line active when bit read or written
  - Transistor switch closed (current flows)
- Write
  - Voltage to bit line
    - High for 1 low for 0
  - Then signal address line
    - Transfers charge to capacitor
- Read
  - Address line selected
    - transistor turns on
  - Charge from capacitor fed via bit line to sense amplifier
    - Compares with reference value to determine 0 or 1
  - Capacitor charge must be restored

Static RAM

- Bits stored as on/off switches
- No charges to leak
- No refreshing needed when powered
- More complex construction
- Larger per bit
- More expensive
- Does not need refresh circuits
- Faster
- Cache
- Digital
  - Uses flip-flops

Stating RAM Structure



Static RAM Operation

- Transistor arrangement gives stable logic state
- State 1
  - —C_1 high, C_2 low
  - —T_1 T_4 off, T_2 T_3 on
- State 0
  - —C_2 high, C_1 low
  - —T_2 T_3 off, T_1 T_4 on
- Address line transistors T_5 T_6 is switch
- Write – apply value to B & compliment to B
- Read – value is on line B

SRAM v DRAM

- Both volatile
  - —Power needed to preserve data
- Dynamic cell
  - —Simpler to build, smaller
  - —More dense
  - —Less expensive
  - —Needs refresh
  - —Larger memory units
- Static
  - —Faster
  - —Cache

Read Only Memory (ROM)

- Permanent storage
  - Nonvolatile
- Microprogramming (see later)
- Library subroutines
- Systems programs (BIOS)
- Function tables

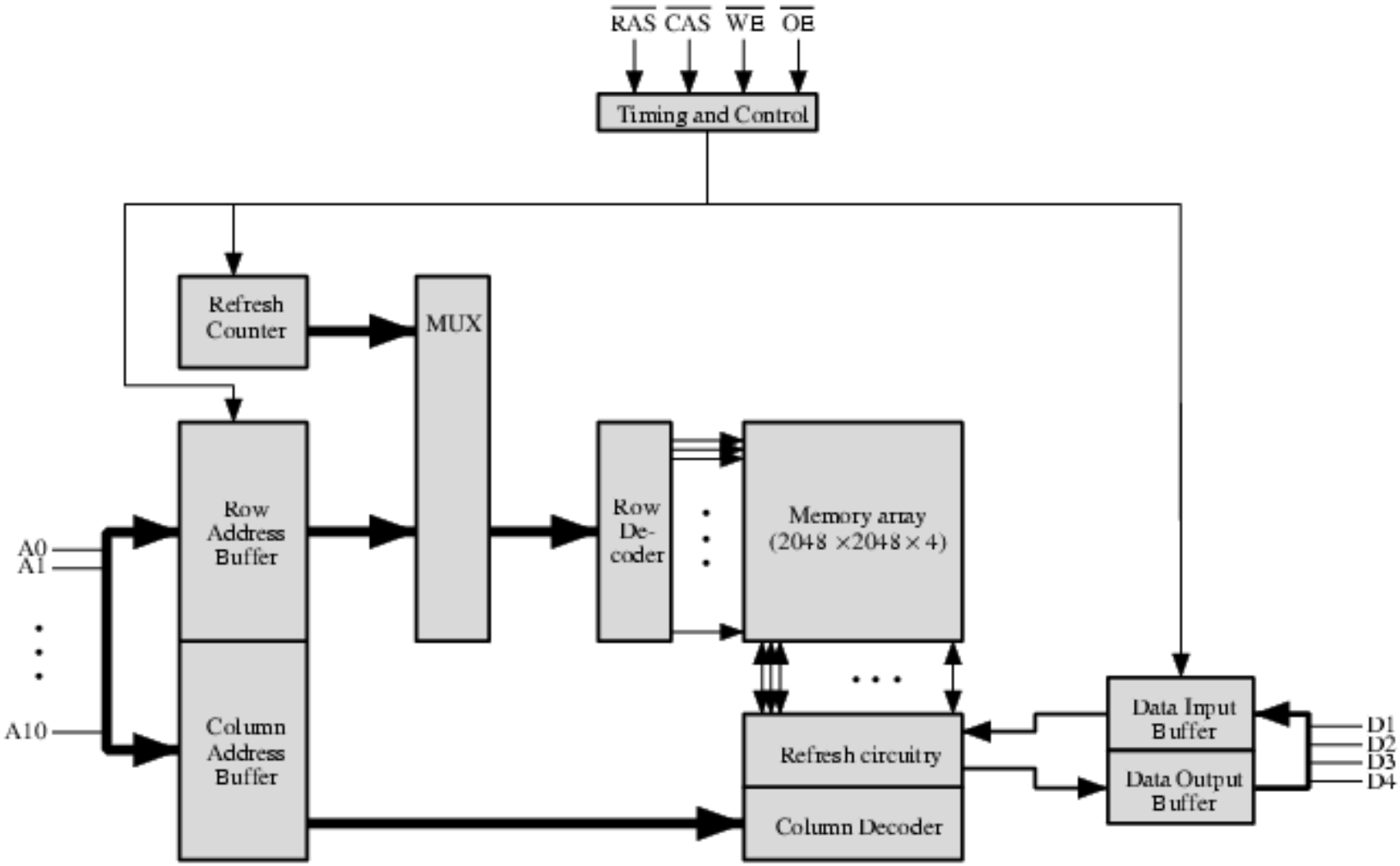
Types of ROM

- Written during manufacture
  - Very expensive for small runs
- Programmable (once)
  - PROM
  - Needs special equipment to program
- Read “mostly”
  - Erasable Programmable (EPROM)
    - Erased by UV
  - Electrically Erasable (EEPROM)
    - Takes much longer to write than read
  - Flash memory
    - Erase whole memory (or a block of) electrically

Organisation in detail

- A 16Mbit chip can be organised as 1M of 16 bit words
- A bit per chip system has 16 lots of 1Mbit chip with bit 1 of each word in chip 1 and so on
- A 16Mbit chip can be organised as a 2048 x 2048 x 4bit array
  - Reduces number of address pins
    - Multiplex row address and column address
    - 11 pins to address ($2^{11}=2048$)
    - Adding one more pin doubles range of values so x4 capacity

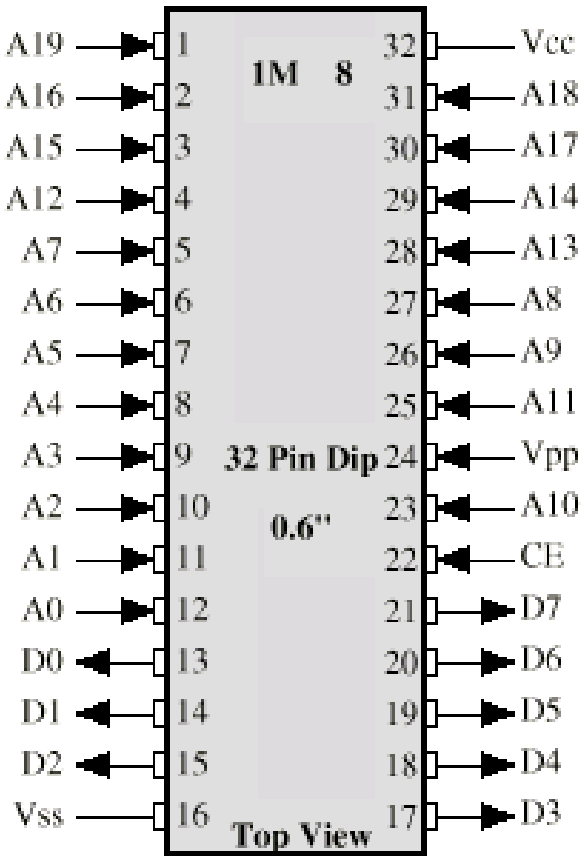
Typical 16 Mb DRAM (4M x 4)



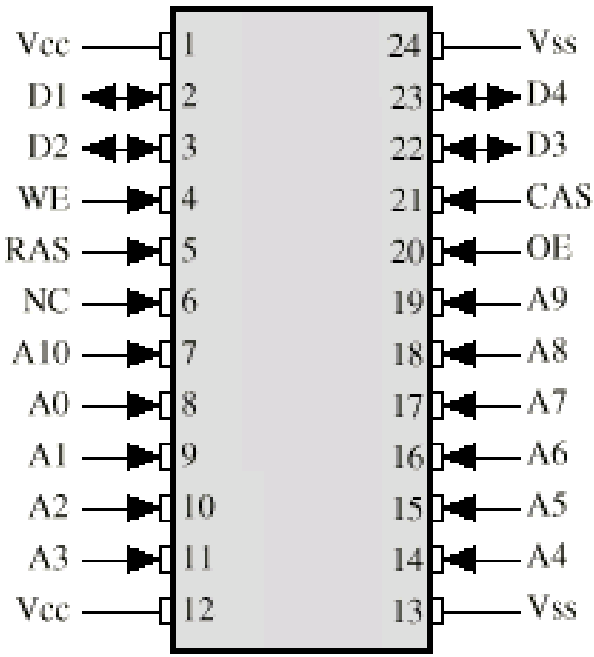
Refreshing

- Refresh circuit included on chip
- Disable chip
- Count through rows
- Read & Write back
- Takes time
- Slows down apparent performance

Packaging

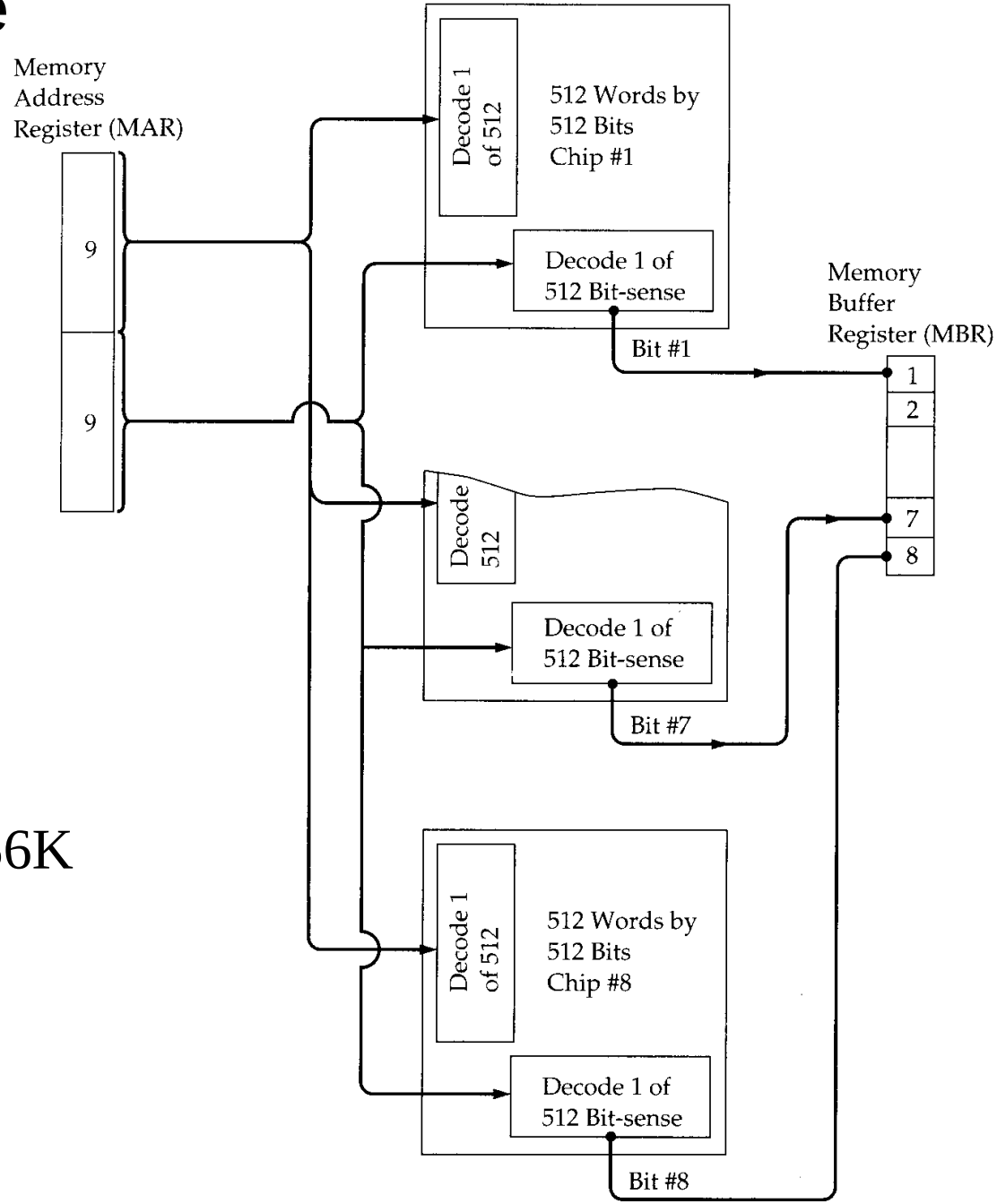


(a) 8 Mbit EPROM



(b) 16 Mbit DRAM

256kByte Module Organisation

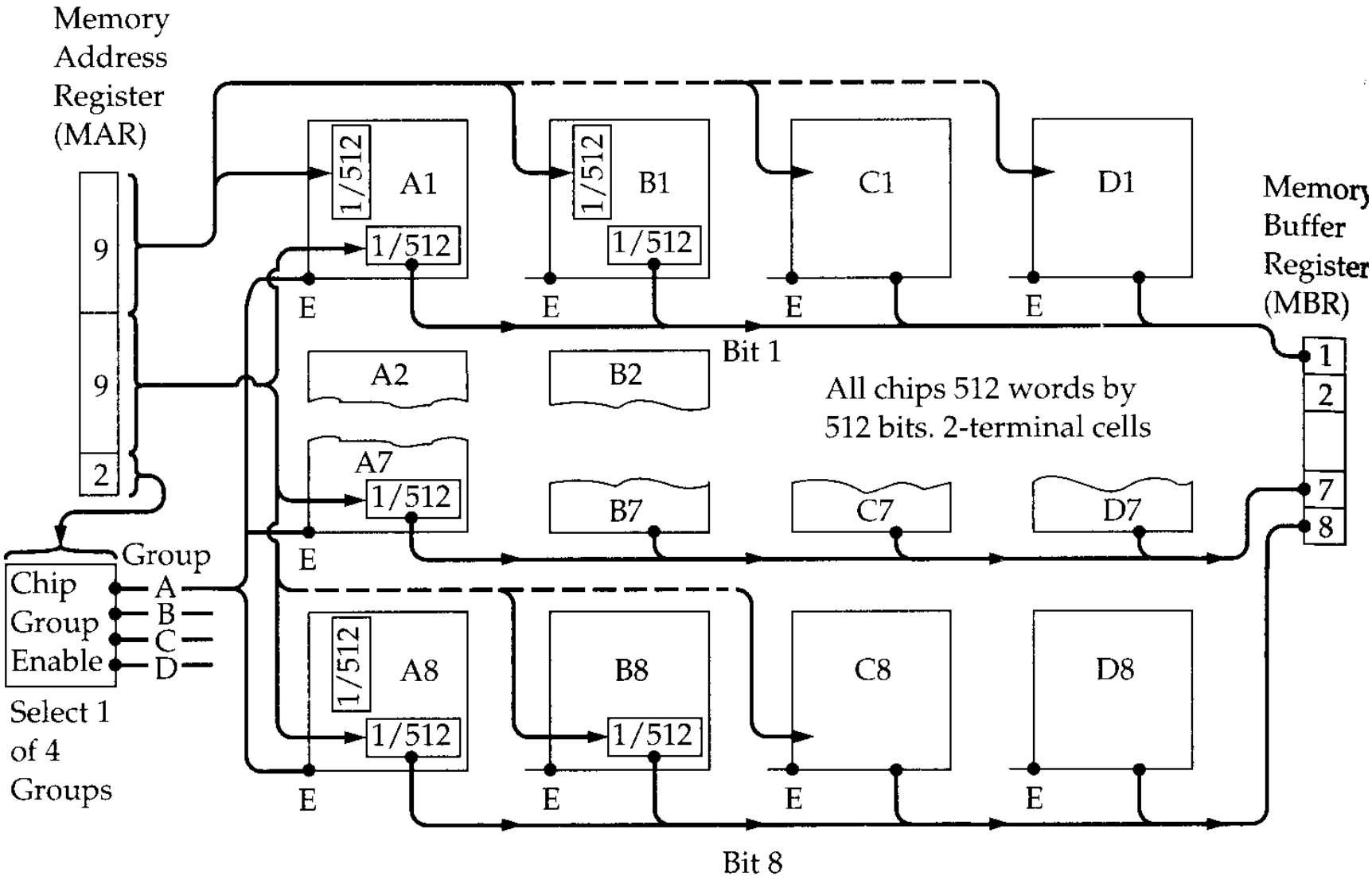


$2^{18} = 262,144 = 256K$

$2^{9} = 512$

$512 \times 512 = 262,144 = 256K$

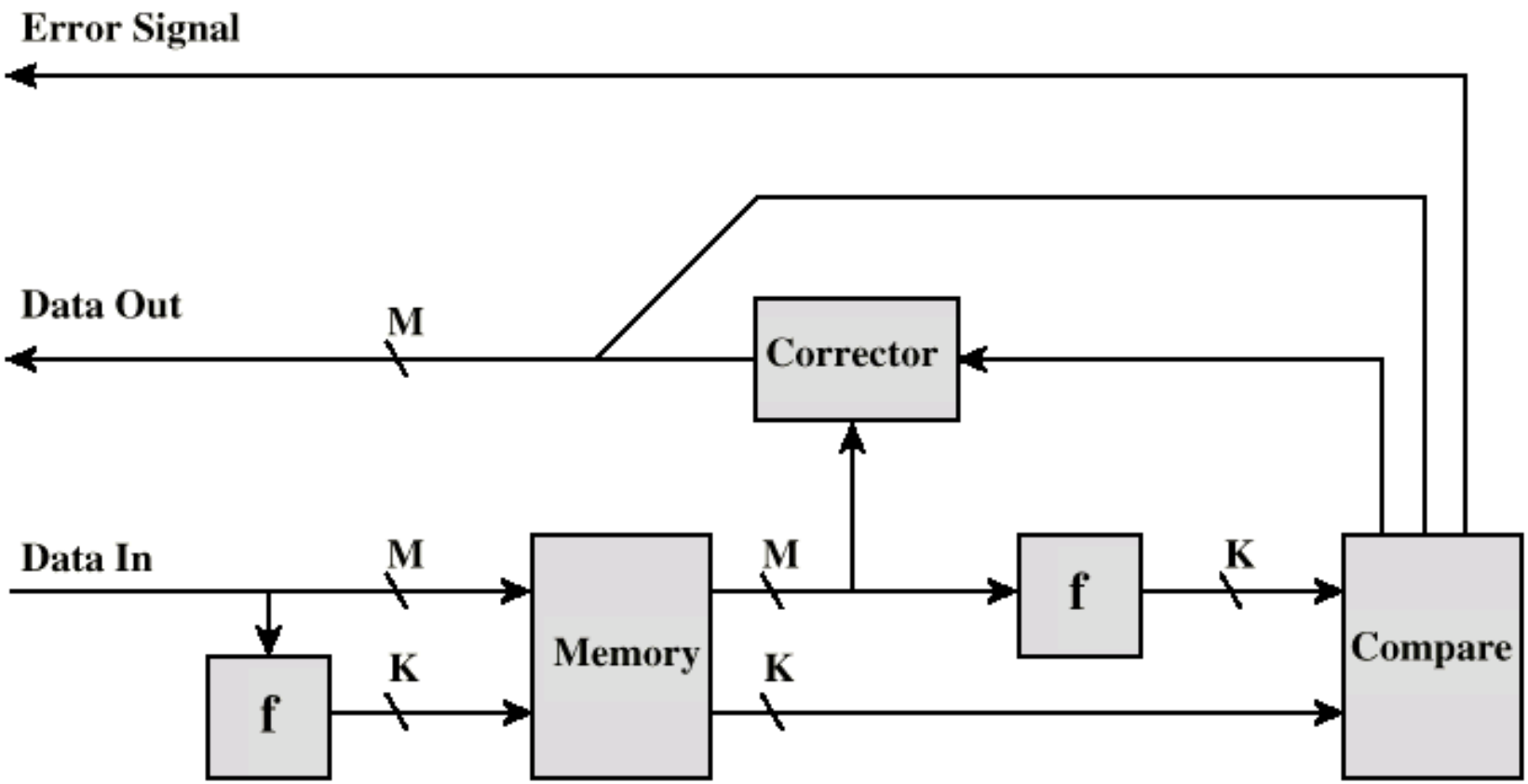
1MByte Module Organisation



Error Correction

- Hard Failure
  - Permanent defect (stuck at 0 or 1)
- Soft Error
  - Random, non-destructive
  - No permanent damage to memory
- Detected using Hamming error correcting code

Error Correcting Code Function



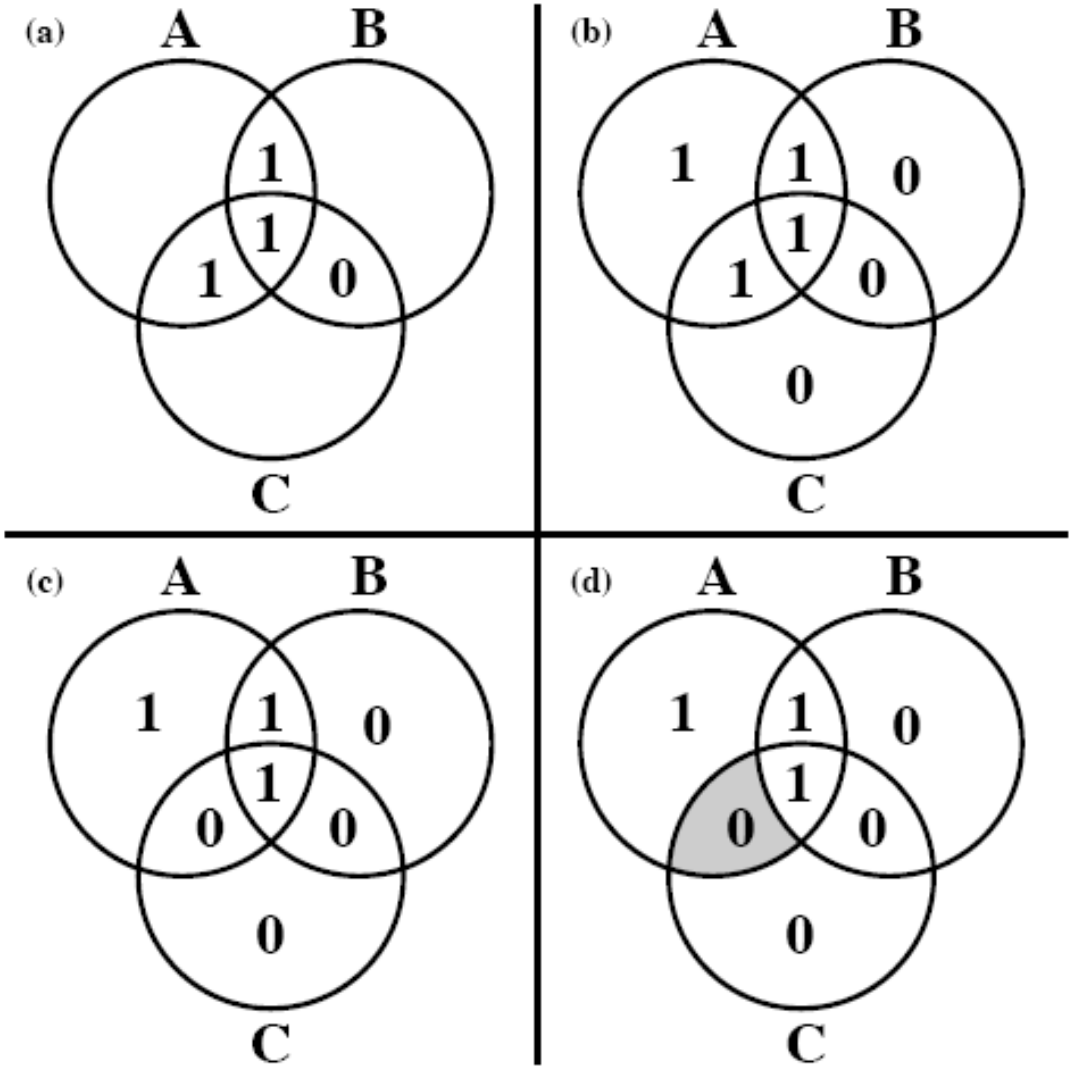


Figure 5.8 Hamming Error-Correcting Code

Table 5.2 Increase in Word Length with Error Correction

	Single-Error Correction		Single-Error Correction/ Double-Error Detection	
Data Bits	Check Bits	% Increase	Check Bits	% Increase
8	4	50	5	62.5
16	5	31.25	6	37.5
32	6	18.75	7	21.875
64	7	10.94	8	12.5
128	8	6.25	9	7.03
256	9	3.52	10	3.91

Advanced DRAM Organization

- Basic DRAM same since first RAM chips (1970's)
- Enhanced DRAM
  - Contains small SRAM as well
  - SRAM holds last line read (c.f. Cache!)
- Cache DRAM
  - Larger SRAM component
  - Use as cache or serial buffer

Table 5.3 Performance Comparison of Some DRAM Alternatives

	Clock frequency (MHz)	Transfer rate (GB/s)	Access time (ns)	Pin count
SDRAM	166	1.3	18	168
DDR	200	3.2	12.5	184
RDRAM	600	4.8	12	162

Synchronous DRAM (SDRAM)

- Access is synchronized with an external clock
- Address is presented to RAM
- RAM finds data (CPU waits in conventional DRAM)
- Since SDRAM moves data in time with system clock, CPU knows when data will be ready
- CPU does not have to wait, it can do something else
- Burst mode allows SDRAM to set up stream of data and fire it out in block
- DDR-SDRAM sends data twice per clock cycle (leading & trailing edge)

SDRAM

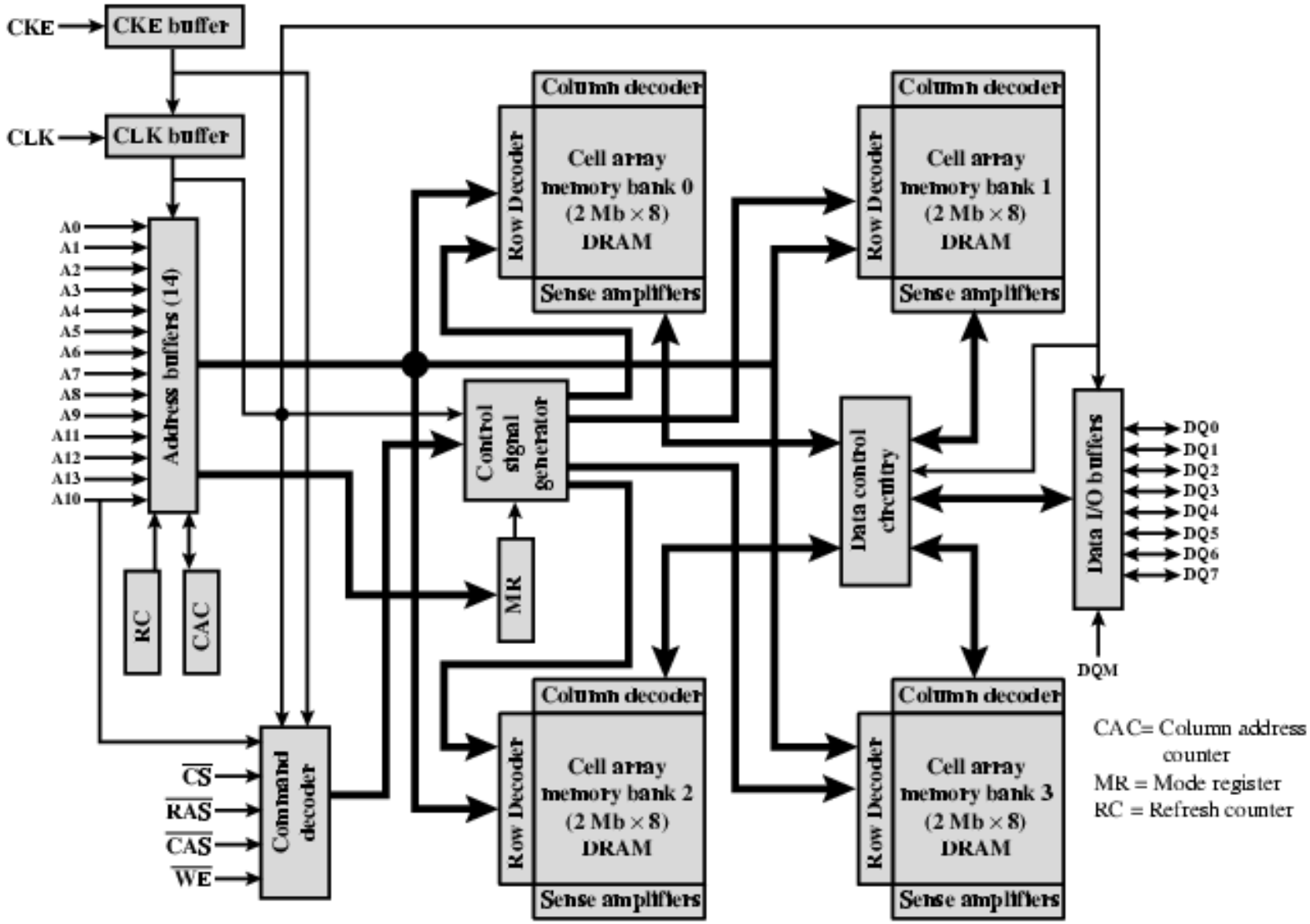

CKE
CKE buffer
CLK
CLK buffer
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A11
A12
A13
A10
Address buffers (14)
RC
CAC
MR
Control signal generator
Column decoder
Row Decoder
Cell array memory bank 0 (2 Mb × 8) DRAM
Sense amplifiers
Column decoder
Row Decoder
Cell array memory bank 1 (2 Mb × 8) DRAM
Sense amplifiers
Data control circuitry
Data I/O buffers
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQM
Column decoder
Row Decoder
Cell array memory bank 2 (2 Mb × 8) DRAM
Sense amplifiers
Column decoder
Row Decoder
Cell array memory bank 3 (2 Mb × 8) DRAM
Sense amplifiers
CS
RAS
CAS
WE
Command decoder
CAC= Column address counter
MR = Mode register
RC = Refresh counter

Table 5.4 SDRAM Pin Assignments

A0 to A13	Address inputs
CLK	Clock input
CKE	Clock enable
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQ0 to DQ7	Data input/output
DQM	Data mask

SDRAM Read Timing

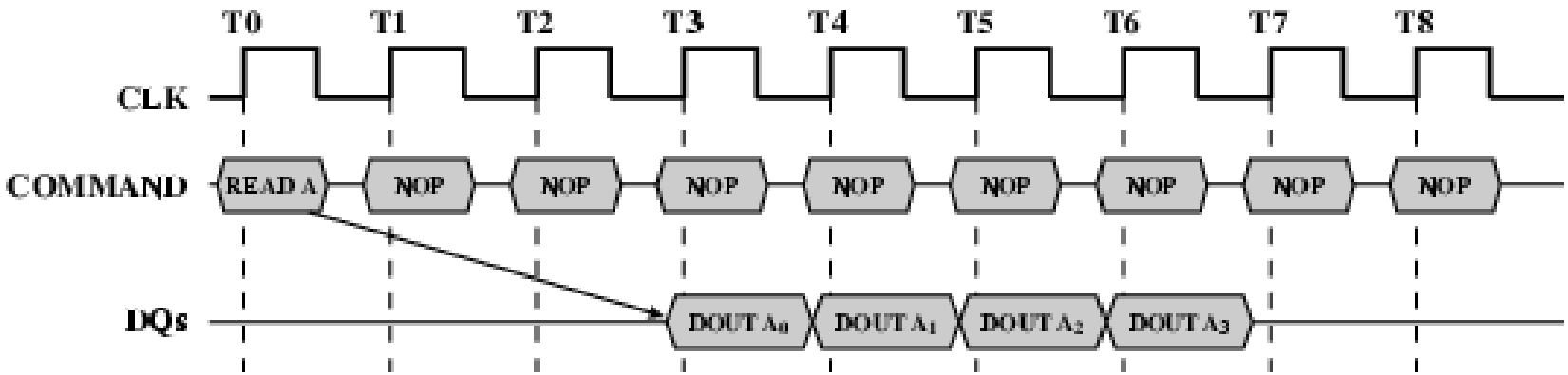
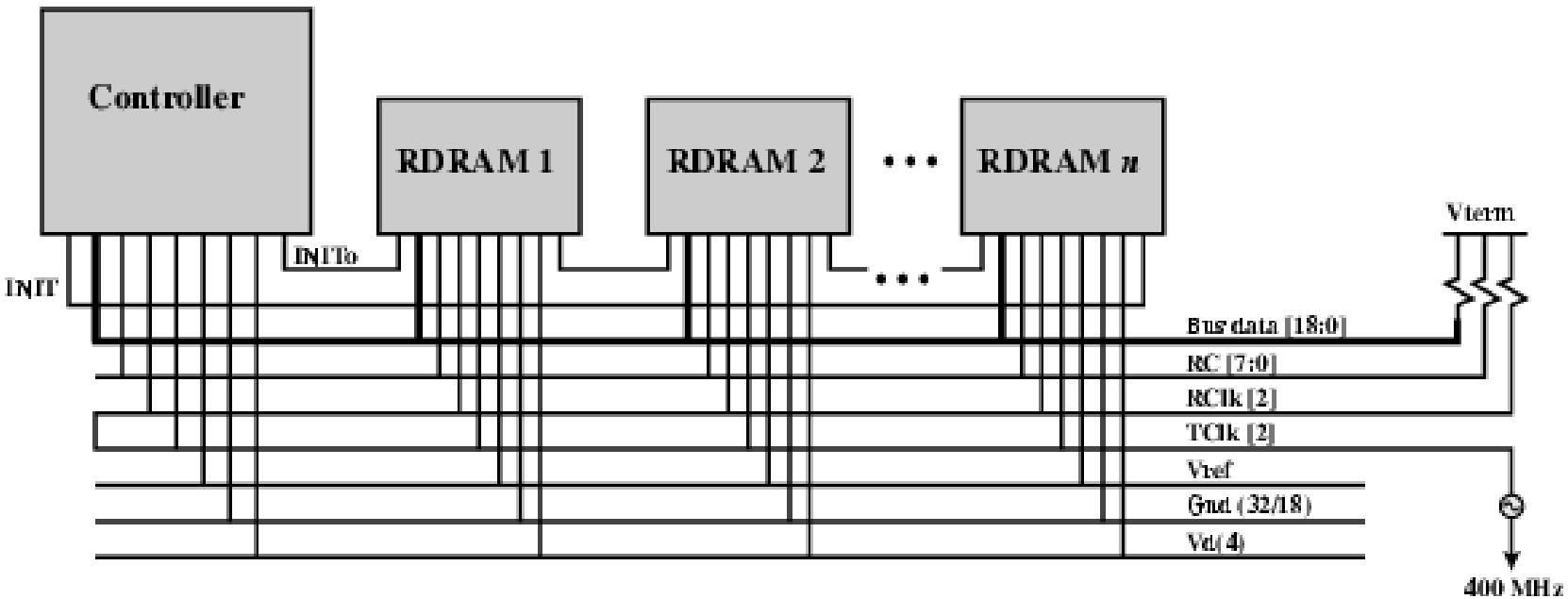


Figure 5.13 SDRAM Read Timing (Burst Length = 4, $\overline{\text{CAS}}$ latency = 2)

RAMBUS

- Adopted by Intel for Pentium & Itanium
- Main competitor to SDRAM
- Vertical package – all pins on one side
- Data exchange over 28 wires < 12cm long
- Bus addresses up to 320 RDRAM chips at 1.6Gbps
- Asynchronous block protocol
  - 480ns access time
  - Then 1.6 Gbps

RAMBUS Diagram



DDR SDRAM

- SDRAM can only send data once per clock
- Double-data-rate SDRAM can send data twice per clock cycle
  - Rising edge and falling edge

Cache DRAM

- Mitsubishi
- Integrates small SRAM cache (16 kb) onto generic DRAM chip
- Used as true cache
  - 64-bit lines
  - Effective for ordinary random access
- To support serial access of block of data
  - E.g. refresh bit-mapped screen
    - CDRAM can prefetch data from DRAM into SRAM buffer
    - Subsequent accesses solely to SRAM

Reading

- The RAM Guide
- RDRAM