William Stallings
Computer Organization and Architecture
7th Edition

Chapter 2
Computer Evolution and Performance

History of Computers

- Mechanical Era (1600s-1940s)
  - Wilhelm Schickhard (1623)
    - » Astronomer and mathematician
    - » Automatically add, subtract, multiply, and divide
  - Blaise Pascal (1642)
    - » Mathematician
    - » Mass produced first working machine (50 copies)
    - » Could only add and subtract
    - » Maintenance and labor problems
  - Gottfried Liebniz (1673)
    - » Mathematician and inventor
    - » Improved on Pascal's machine
    - » Add, subtract, multiply, and divide

- Charles Babbage (1822)
  - Mathematician
  - "Father of modern computer"
  - Wanted more accuracy in calculations
  - Difference engine
    - Government / science agreement
    - Automatic computation of math tables
  - Analytic engine
    - Perform any math operation
    - Punch cards
    - Modern structure: I/O, storage, ALU
    - Add in 1 second, multiply in 1 minute
  - Both engines plagued by mechanical problems
- George Boole (1847)
  - Mathematical analysis of logic
  - Investigation of laws of thought

- Herman Hollerith (1889)
  - » Modern day punched card machine
  - » Formed Tabulating Machine Company (became IBM)
  - » 1880 census took 5 years to tabulate
  - » Tabulation estimates
    - ◆ 1890: 7.5 years
    - ◆ 1900: 10+ years
  - » Hollerith's tabulating machine reduced the 7.5 year estimate to 2 months
- Konrad Zuse (1938)
  - » Built first working mechanical computer, the Z1
  - » Binary machine
  - » German government decided not to pursue development -- W.W.II already started
- Howard Aiken (1943)
  - » Designed the Harvard Mark I
  - » Implementation of Babbage's machine
  - » Built by IBM

The Electronic Era

- Generation 1 (1945 - 1958)
  - ENIAC
    - » Developed for calculating artillery firing tables
    - » Designed by Mauchly and Echert of the University of Pennsylvania
    - » Generally regarded as the first electronic computer
      - Colossus probably the first, but was classified until recently
    - » BIG!
      - 18,000 tubes
      - 70,000 resistors
      - 10,000 capacitors
      - 6,000 switches
      - 30 x 50 feet
      - 140 kW of power
    - » Decimal number system used
    - » Programmed by manually setting switches

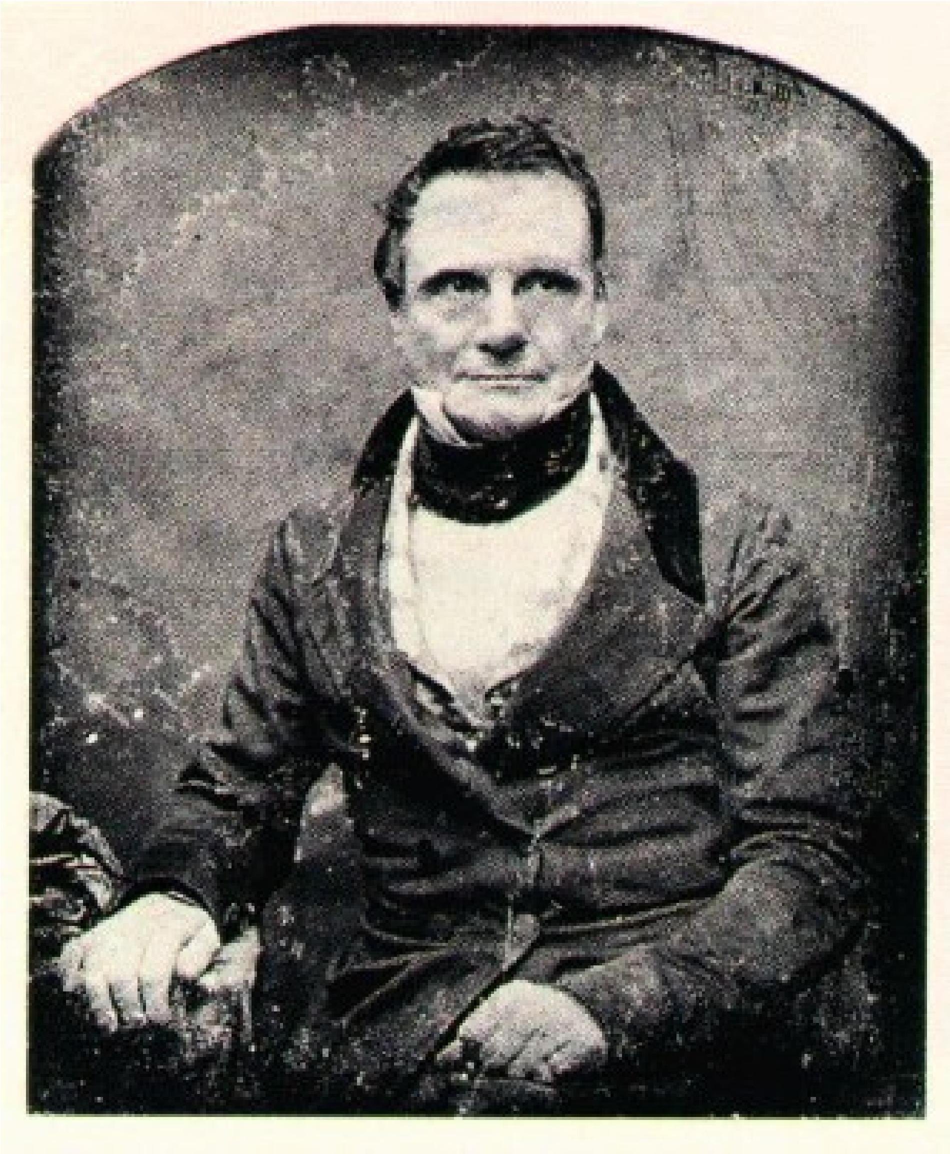
- IAS (Institute for Advanced Studies)
  - » von Neumann and Goldstine
  - » Took idea of ENIAC and developed concept of storing a program in the memory
  - » This architecture came to be known as the "von Neumann" architecture and has been the basis for virtually every machine designed since then
  - » Features
    - ◆ Data and instructions (programs) are stored in a single read-write memory
    - ◆ Memory contents are addressable by location, regardless of the content itself
    - ◆ Sequential execution
- Lots of initial and long-term fighting over patents, rights, credits, firsts, etc.

- Generation 2 (1958 - 1964)
  - Technology change
  - Transistors
  - High level languages
  - Floating point arithmetic
- Generation 3 (1964 - 1974)
  - Introduction of integrated circuits
  - Semiconductor memory
  - Microprogramming
  - Multiprogramming
- Generation 4 (1974 - present)
  - Large scale integration / VLSI
  - Single board computers
- Generation 5 (? - ?)
  - VLSI / ULSI
  - Computer communications networks
  - Artificial intelligence
  - Massively parallel machines

Summary of Generations

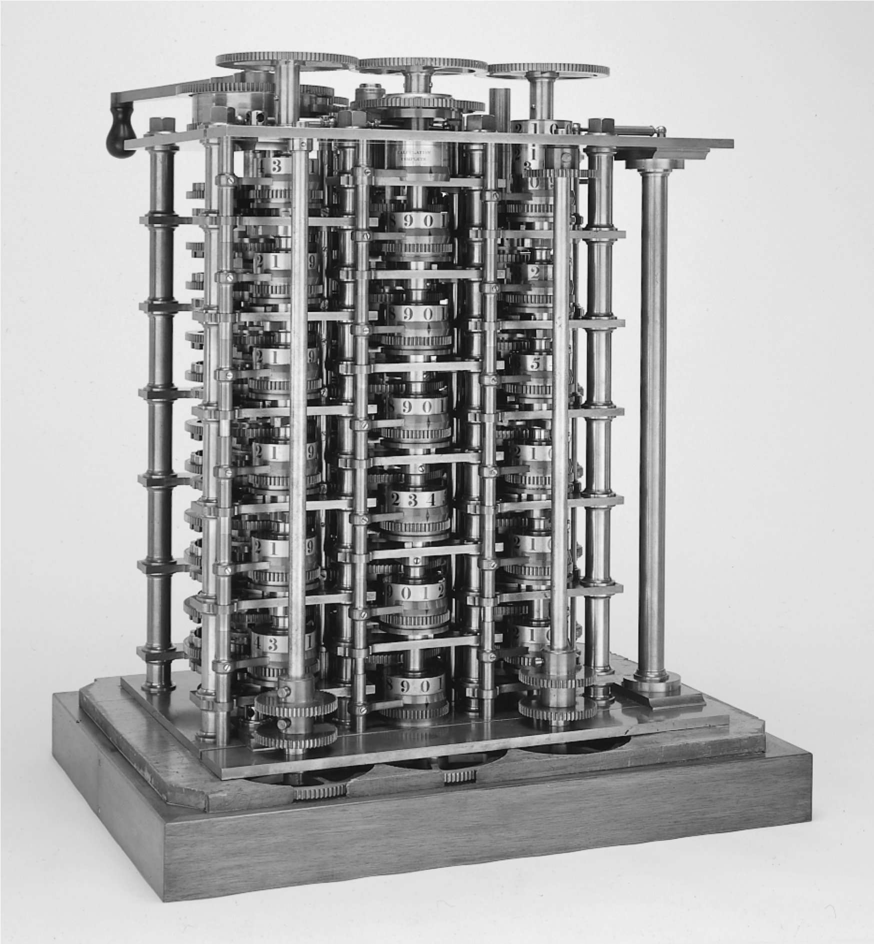
Generation	Example Machines	Hardware	Software	Performance
1	ENIAC, UNIVAC I, IBM 700	Vacuum tubes, magnetic drums	Machine code, stored programs	2 Kb memory, 10 KIPS
2	IBM 7094	Transistors, core memory	High level languages	32 Kb memory, 200 KIPS
3	IBM 360 370, PDP 11	ICs, semiconductor memory, microprocessors	Timesharing, graphics, structured programming	2 Mb memory, 5 MIPS
4	IBM 3090, Cray XMP, IBM PC	VLSI, networkes, optical disks	Packaged programs, object-oriented languages, expert systems	8 Mb memory, 30 MIPS
5	Sun Sparc, Intel Paragon	ULSI, GaAs, parallel systems	Parallel languages symbolic processing, AI	64 Mb memory, 10 GFLOPS

Charles Babbage (1791-1871)



Construction of a machine called "Difference Engine."

The First Computer



The Babbage Difference Engine (1832)

25,000 parts

cost: £17,470

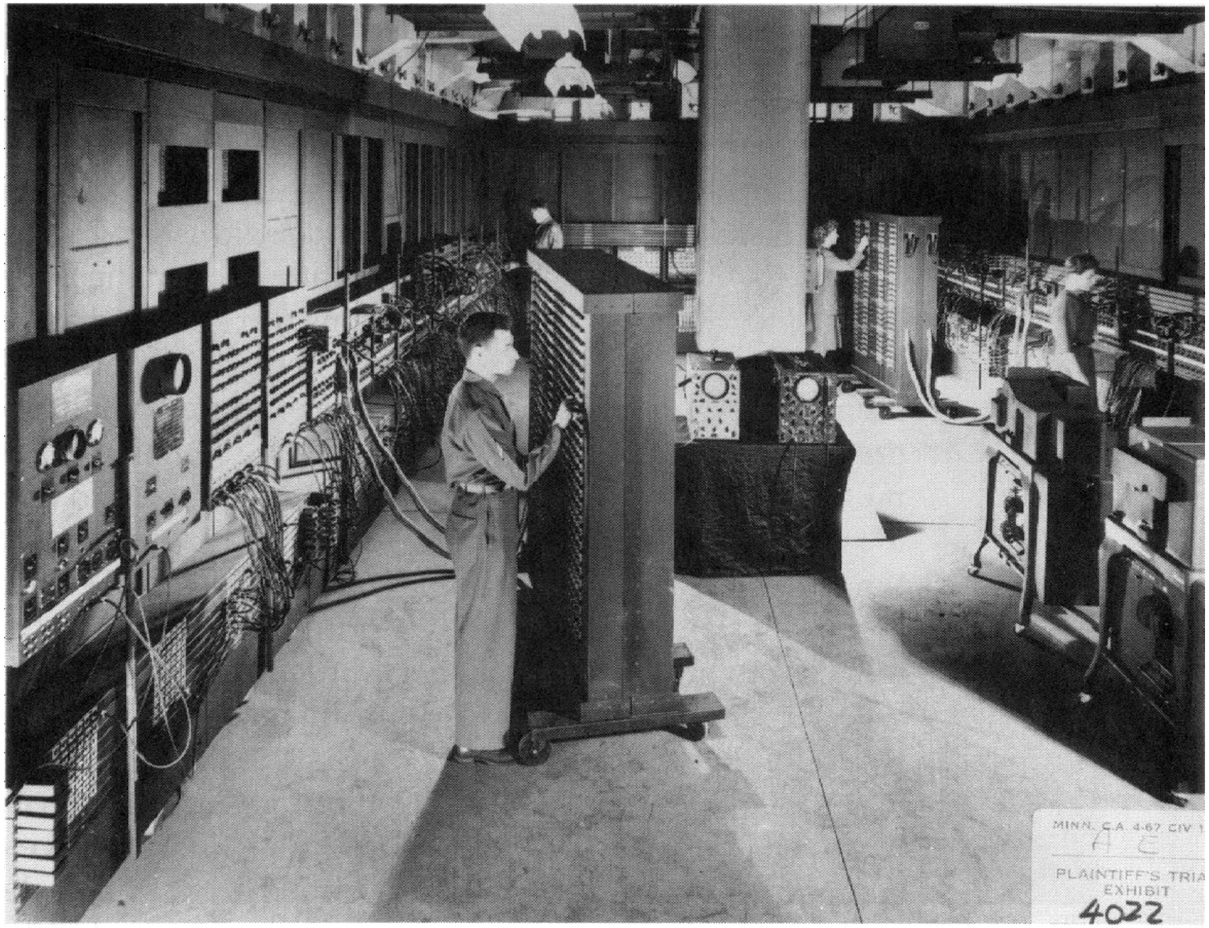
ENIAC - background

- Electronic Numerical Integrator And Computer
- Eckert and Mauchly
- University of Pennsylvania
- Trajectory tables for weapons
- Started 1943
- Finished 1946
  - Too late for war effort
- Used until 1955

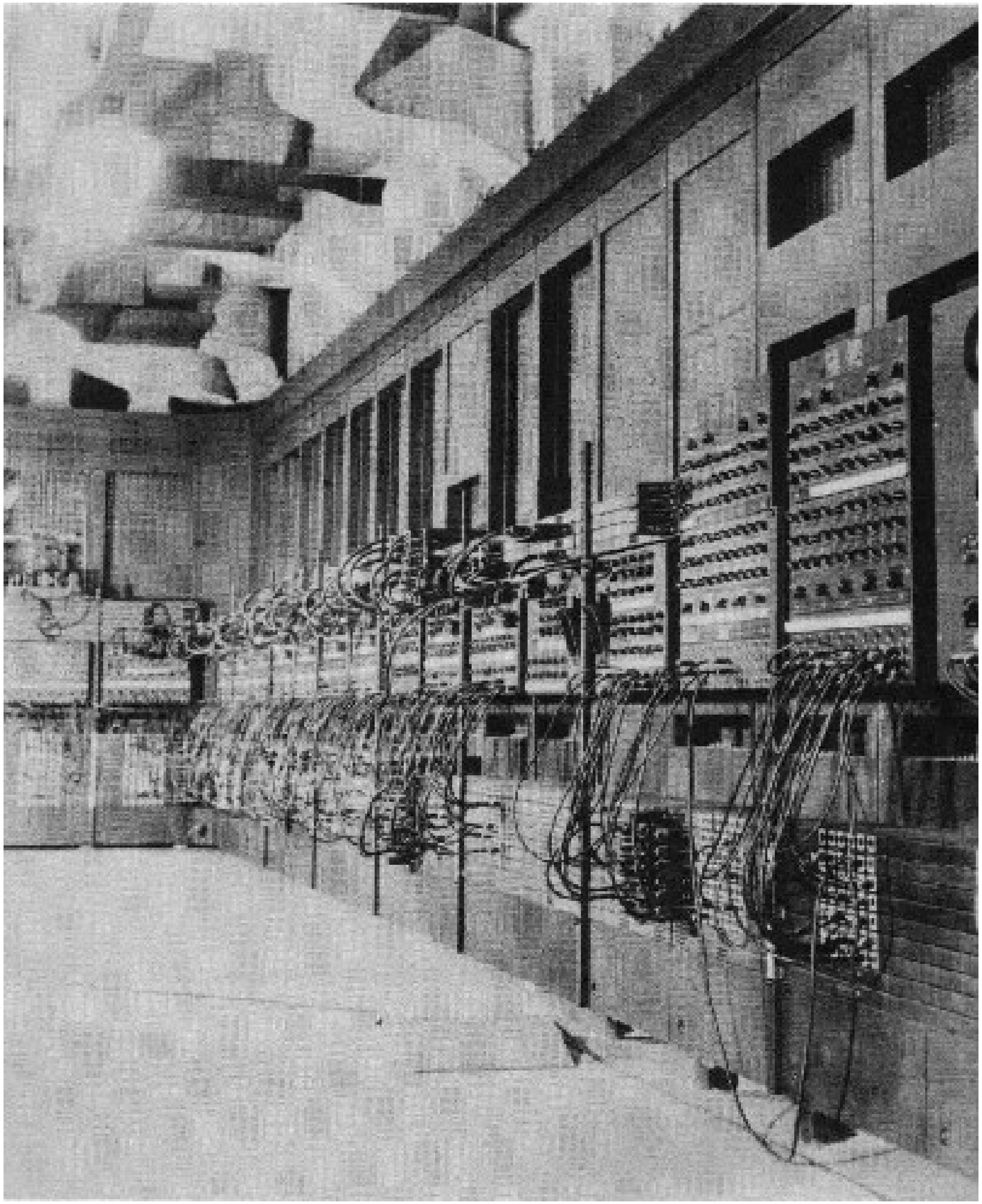
ENIAC - details

- Decimal (not binary)
- 20 accumulators of 10 digits
- Programmed manually by switches
- 18,000 vacuum tubes
- 30 tons
- 15,000 square feet
- 140 kW power consumption
- 5,000 additions per second

ENIAC - The first electronic computer (1946)



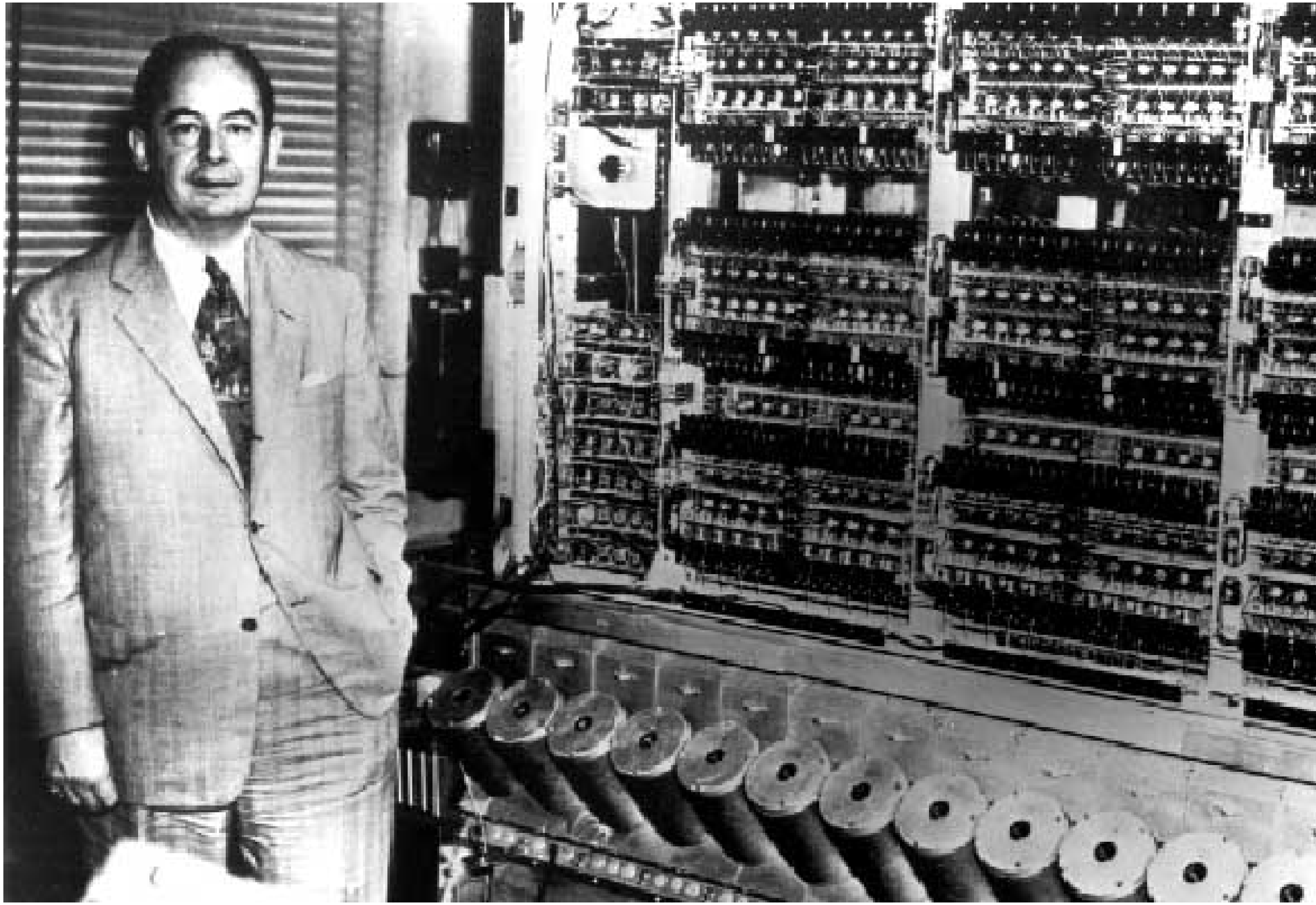
ENIAC



von Neumann/Turing

- Stored Program concept
- Main memory storing programs and data
- ALU operating on binary data
- Control unit interpreting instructions from memory and executing
- Input and output equipment operated by control unit
- Princeton Institute for Advanced Studies
  - IAS
- Completed 1952

von Neumann

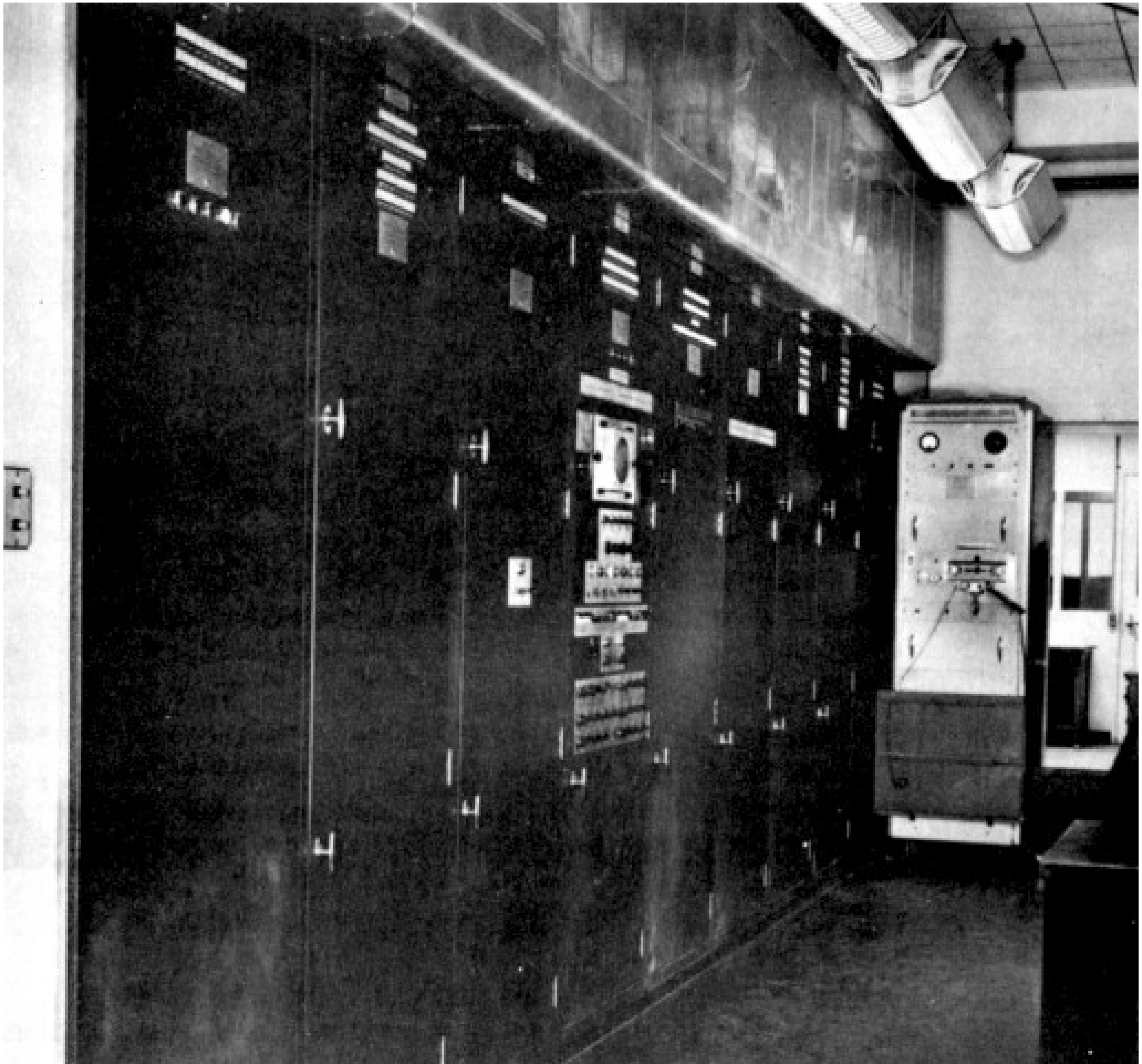


Von Neumann with the first Institute computer

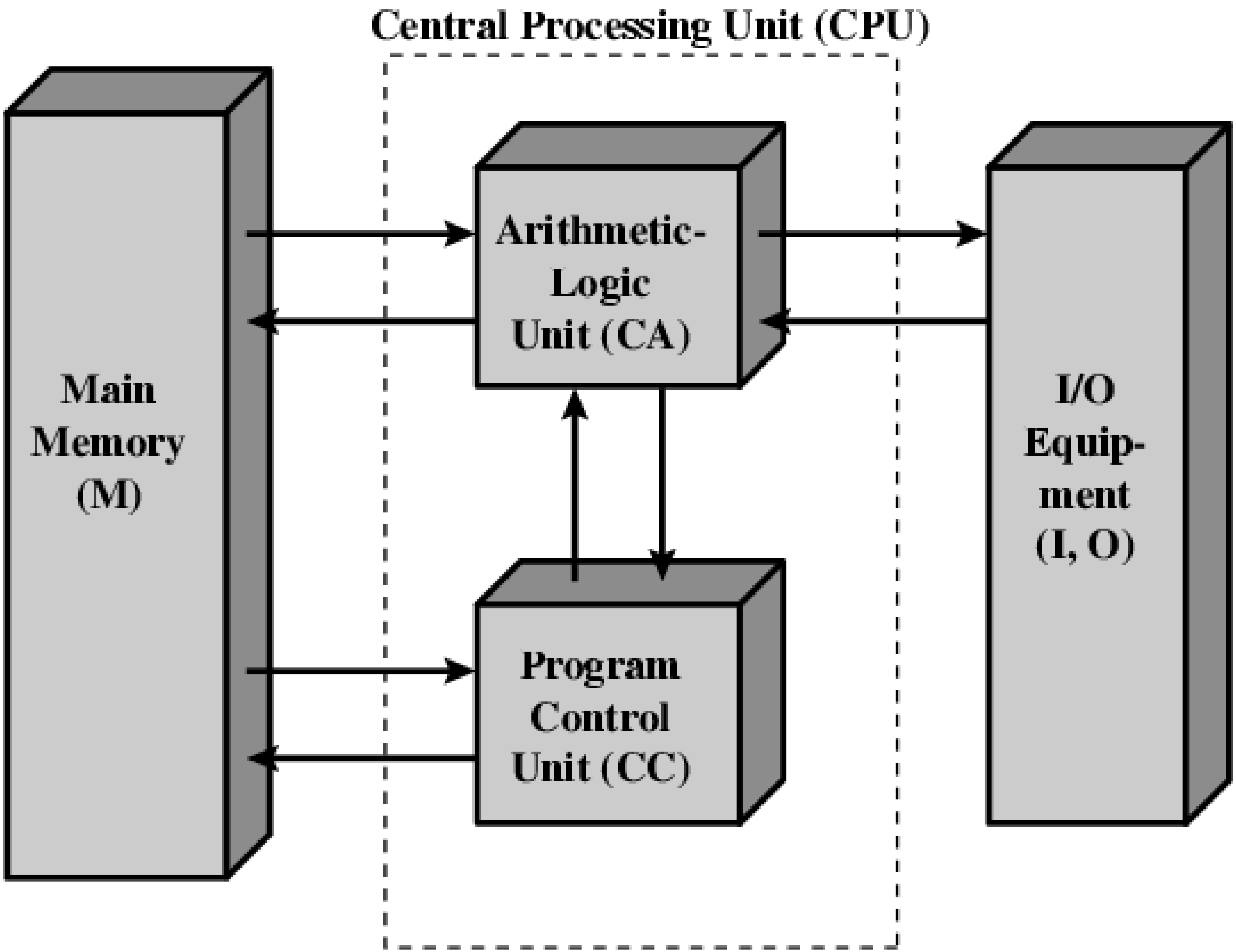
Alan Turing

EDVAC

Electronic Discrete Variable Computer



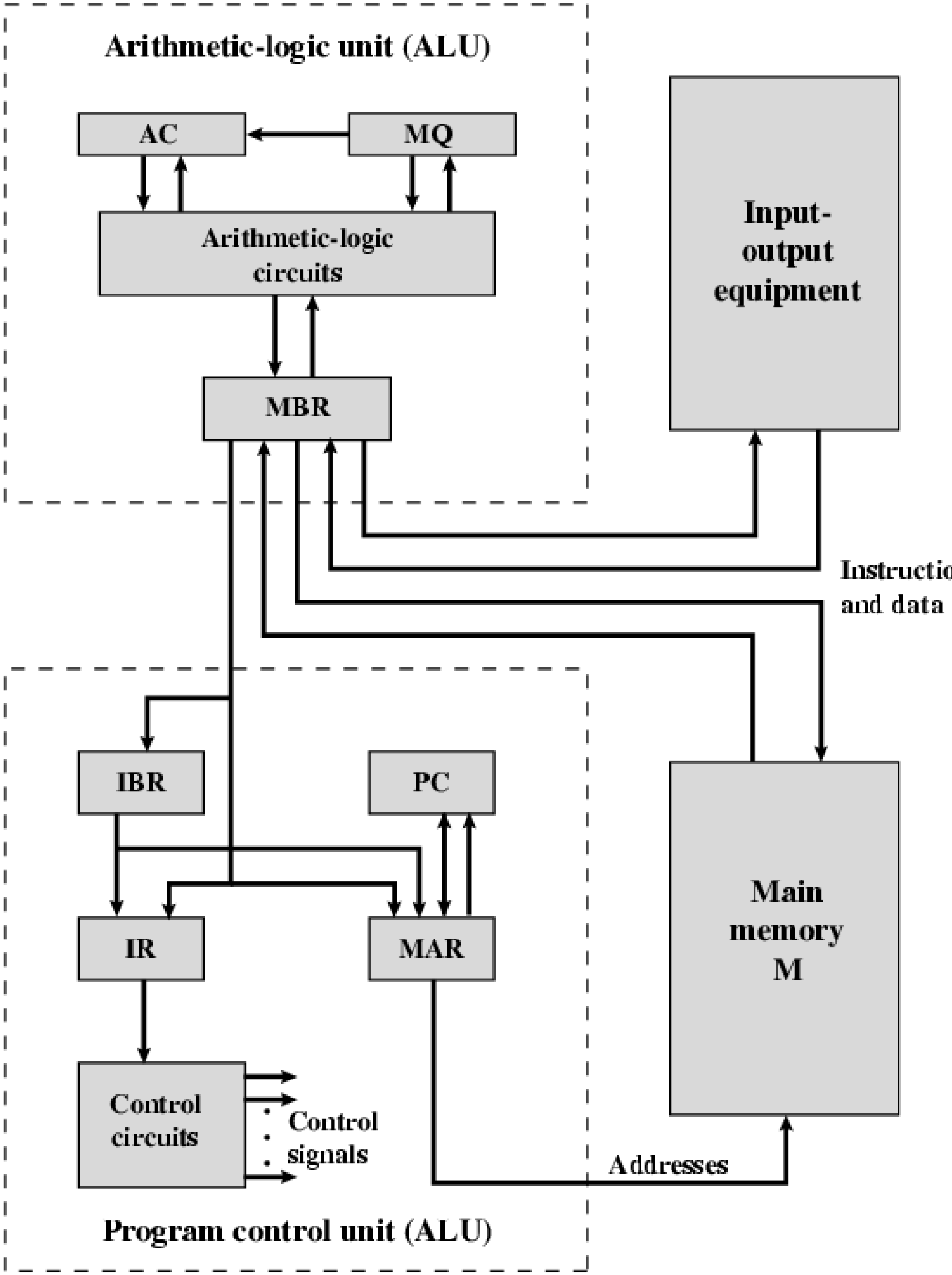
Structure of von Neumann machine



IAS - details

- 1000 x 40 bit words
  - Binary number
  - 2 x 20 bit instructions
- Set of registers (storage in CPU)
  - Memory Buffer Register
  - Memory Address Register
  - Instruction Register
  - Instruction Buffer Register
  - Program Counter
  - Accumulator
  - Multiplier Quotient

Structure of IAS – detail



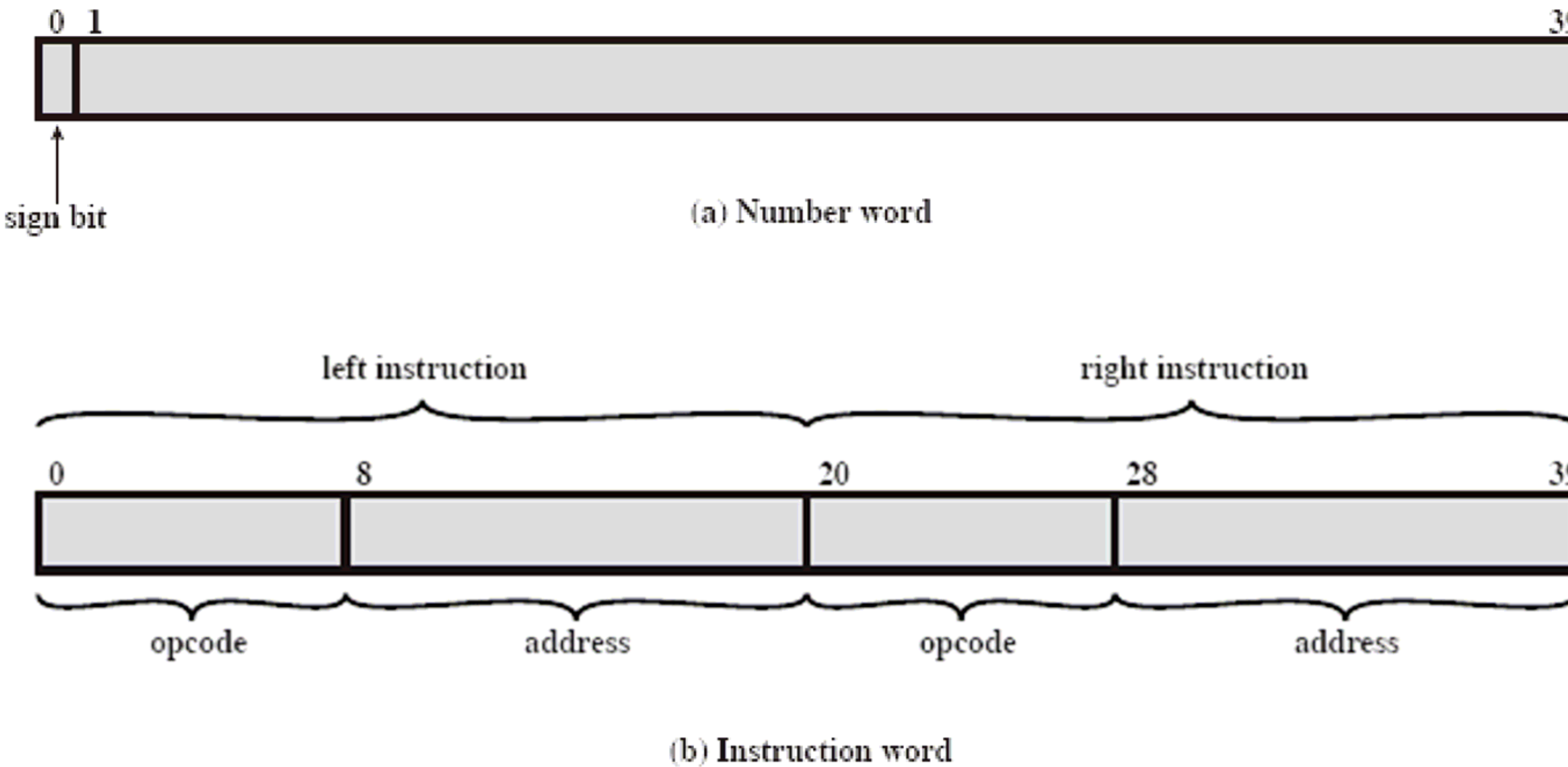


Figure 2.2 IAS Memory Formats

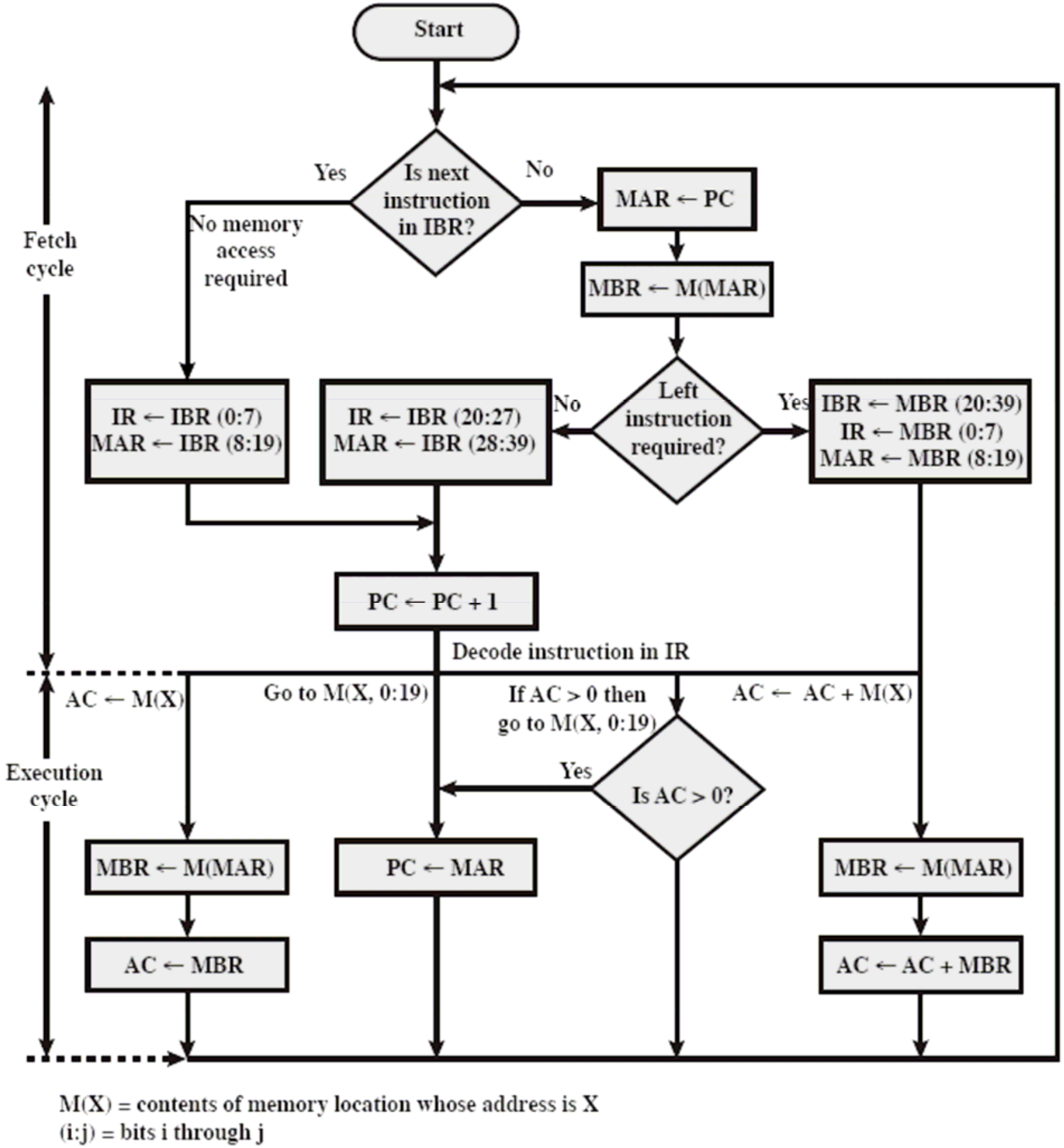
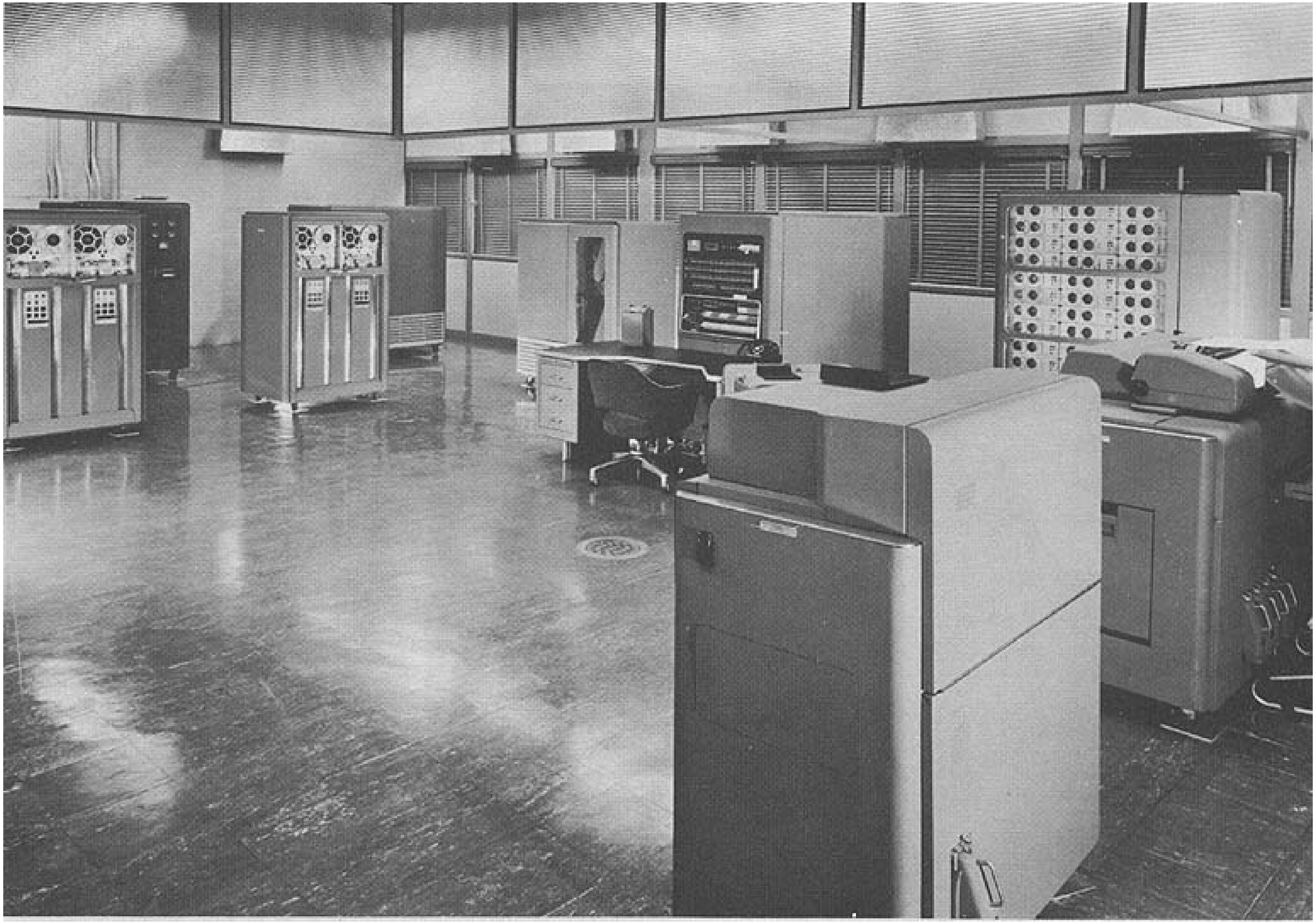


Figure 2.4 Partial Flowchart of IAS Operation

Vacuum tubes

UNIVAC II

IBM 701



IBM 7030 (1961)

DEC PDP-1 (1960)

Estimated cost=$120,000

IBM 360 Family

PDP-11 (1973)

VAX-11 (1981)

Micro VAX

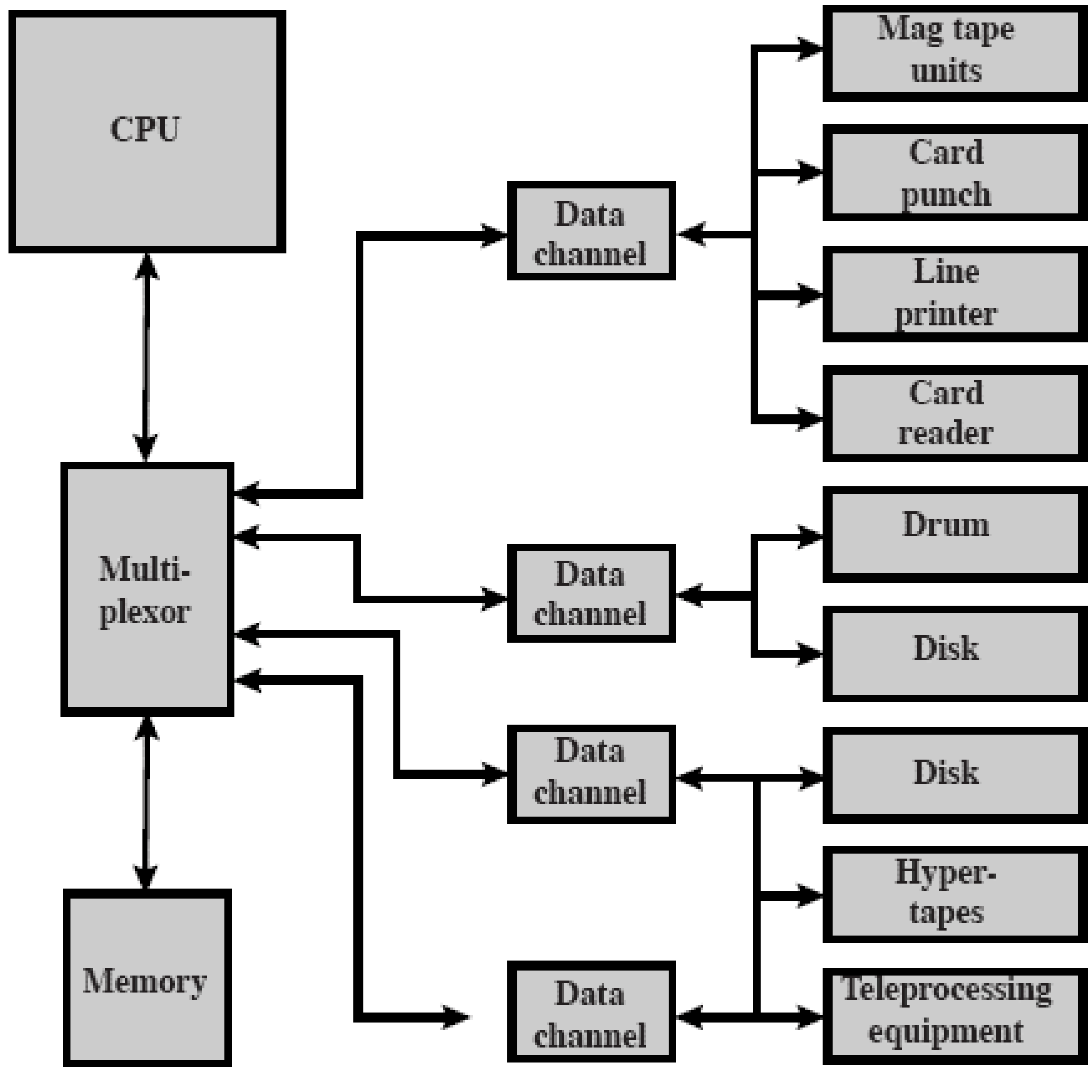


Figure 2.5 An IBM 7094 Configuration

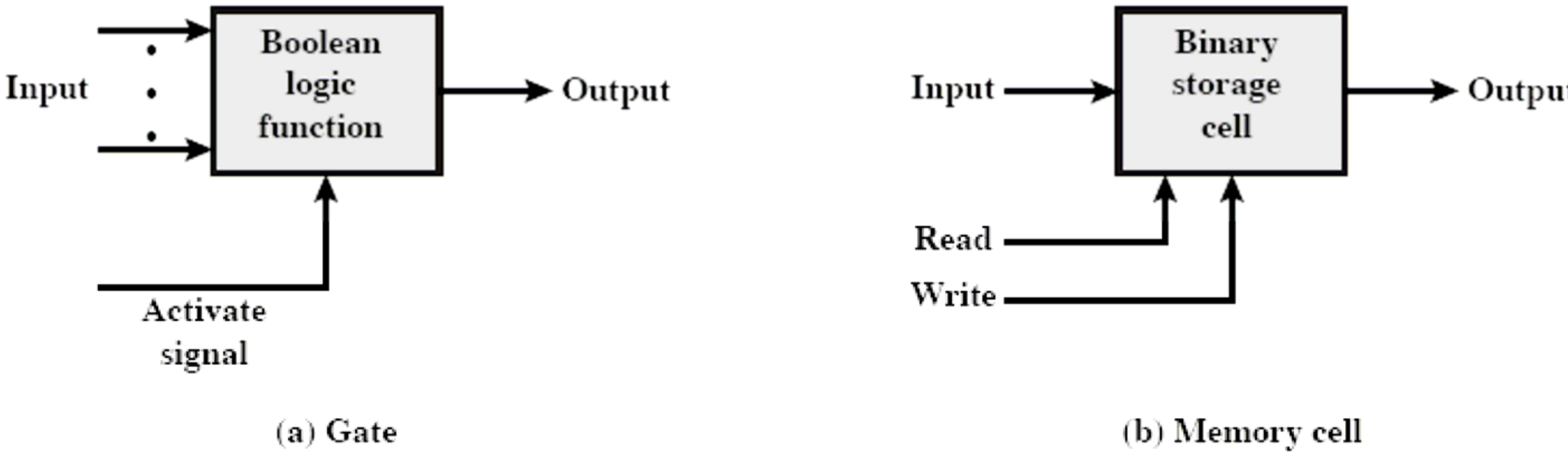


Figure 2.6 Fundamental Computer Elements

Commercial Computers

- 1947 - Eckert-Mauchly Computer Corporation
- UNIVAC I (Universal Automatic Computer)
- US Bureau of Census 1950 calculations
- Became part of Sperry-Rand Corporation
- Late 1950s - UNIVAC II
  - Faster
  - More memory

IBM

- Punched-card processing equipment
- 1953 - the 701
  - IBM's first stored program computer
  - Scientific calculations
- 1955 - the 702
  - Business applications
- Lead to 700/7000 series

Transistors

- Replaced vacuum tubes
- Smaller
- Cheaper
- Less heat dissipation
- Solid State device
- Made from Silicon (Sand)
- Invented 1947 at Bell Labs
- William Shockley et al.

Transistor Based Computers

- Second generation machines
- NCR & RCA produced small transistor machines
- IBM 7000
- DEC - 1957
  - Produced PDP-1

Microelectronics

- Literally - “small electronics”
- A computer is made up of gates, memory cells and interconnections
- These can be manufactured on a semiconductor
- e.g. silicon wafer

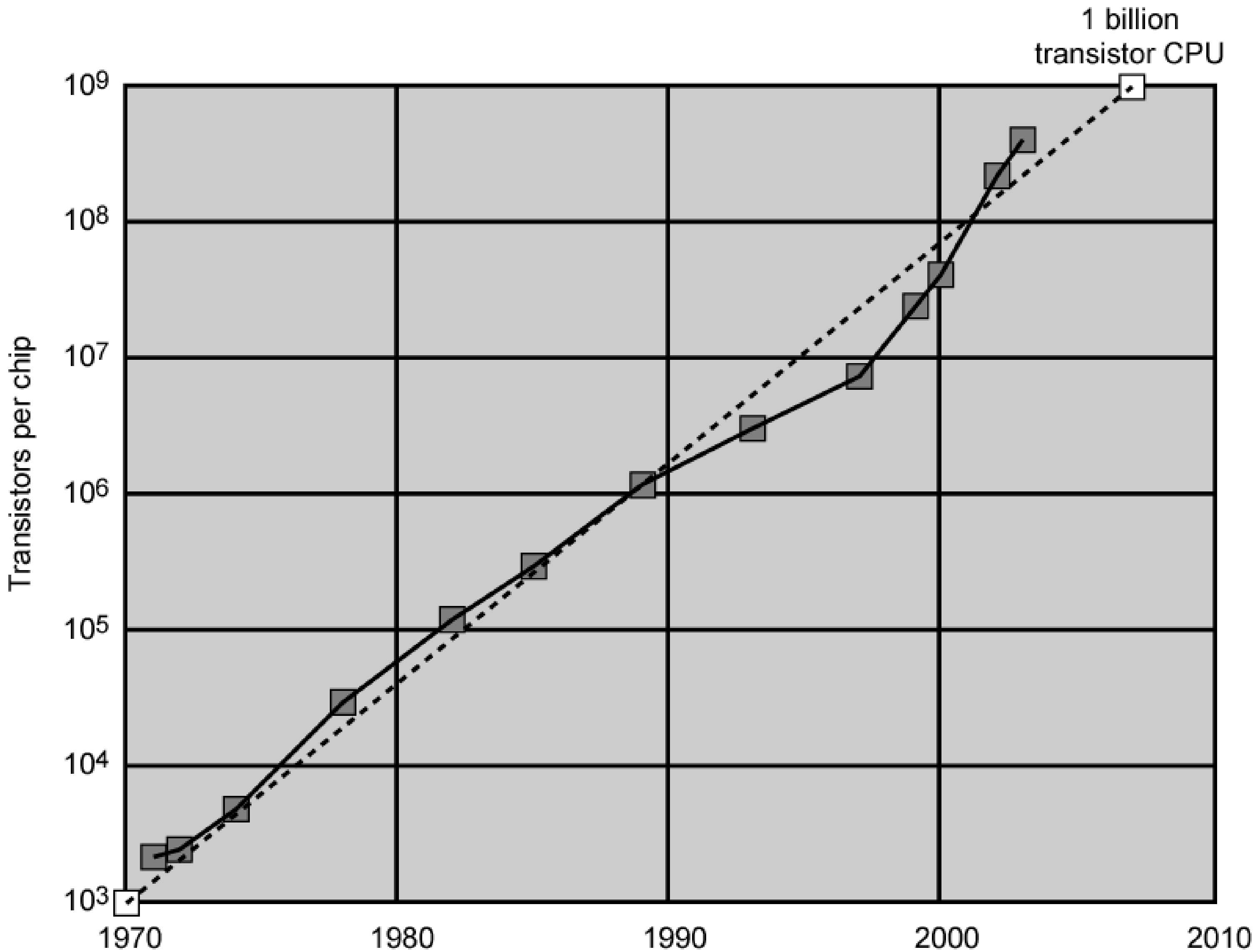
Generations of Computer

- Vacuum tube - 1946-1957
- Transistor - 1958-1964
- Small scale integration - 1965 on
  - Up to 100 devices on a chip
- Medium scale integration - to 1971
  - 100-3,000 devices on a chip
- Large scale integration - 1971-1977
  - 3,000 - 100,000 devices on a chip
- Very large scale integration - 1978 -1991
  - 100,000 - 100,000,000 devices on a chip
- Ultra large scale integration – 1991 -
  - Over 100,000,000 devices on a chip

Moore's Law

- Increased density of components on chip
- Gordon Moore – co-founder of Intel
- Number of transistors on a chip will double every year
- Since 1970's development has slowed a little
    - Number of transistors doubles every 18 months
- Cost of a chip has remained almost unchanged
- Higher packing density means shorter electrical paths, giving higher performance
- Smaller size gives increased flexibility
- Reduced power and cooling requirements
- Fewer interconnections increases reliability

Growth in CPU Transistor Count



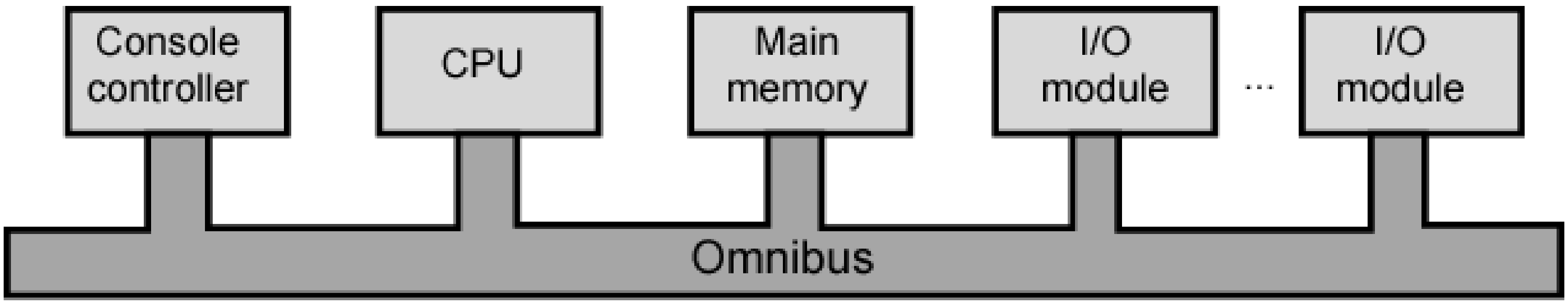
IBM 360 series

- 1964
- Replaced (& not compatible with) 7000 series
- First planned “family” of computers
  - Similar or identical instruction sets
  - Similar or identical O/S
  - Increasing speed
  - Increasing number of I/O ports (i.e. more terminals)
  - Increased memory size
  - Increased cost
- Multiplexed switch structure

DEC PDP-8

- 1964
- First minicomputer (after miniskirt!)
- Did not need air conditioned room
- Small enough to sit on a lab bench
- $16,000
  - $100k+ for IBM 360
- Embedded applications & OEM
- BUS STRUCTURE

DEC - PDP-8 Bus Structure



Semiconductor Memory

- 1970
- Fairchild
- Size of a single core
  - i.e. 1 bit of magnetic core storage
- Holds 256 bits
- Non-destructive read
- Much faster than core
- Capacity approximately doubles each year

Intel

- 1971 - 4004
  - First microprocessor
  - All CPU components on a single chip
  - 4 bit
- Followed in 1972 by 8008
  - 8 bit
  - Both designed for specific applications
- 1974 - 8080
  - Intel's first general purpose microprocessor

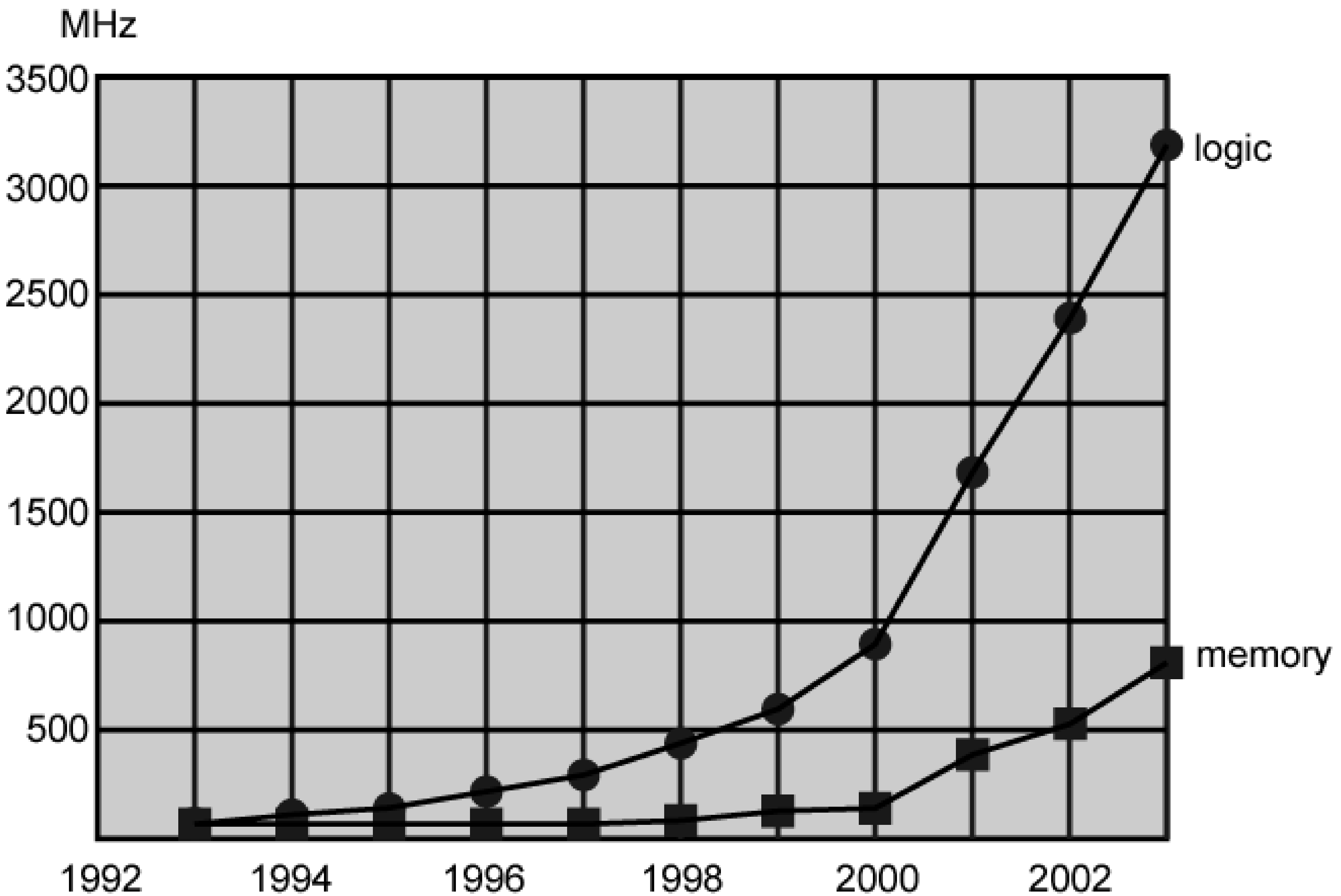
Speeding it up

- Pipelining
- On board cache
- On board L1 & L2 cache
- Branch prediction
- Data flow analysis
- Speculative execution

Performance Balance

- Processor speed increased
- Memory capacity increased
- Memory speed lags behind processor speed

Logic and Memory Performance Gap



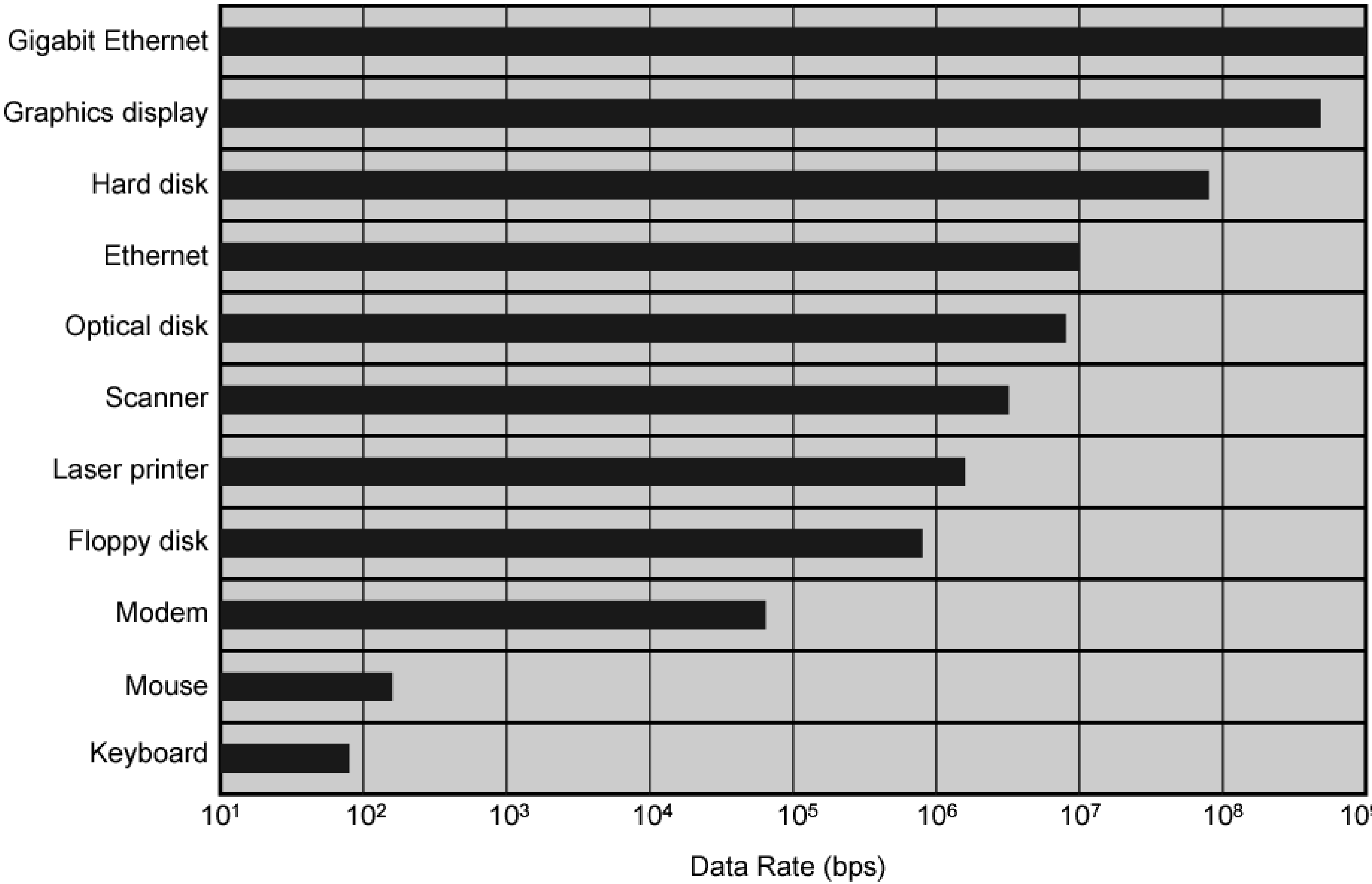
Solutions

- Increase number of bits retrieved at one time
  - Make DRAM “wider” rather than “deeper”
- Change DRAM interface
  - Cache
- Reduce frequency of memory access
  - More complex cache and cache on chip
- Increase interconnection bandwidth
  - High speed buses
  - Hierarchy of buses

I/O Devices

- Peripherals with intensive I/O demands
- Large data throughput demands
- Processors can handle this
- Problem moving data
- Solutions:
  - Caching
  - Buffering
  - Higher-speed interconnection buses
  - More elaborate bus structures
  - Multiple-processor configurations

Typical I/O Device Data Rates



Key is Balance

- Processor components
- Main memory
- I/O devices
- Interconnection structures

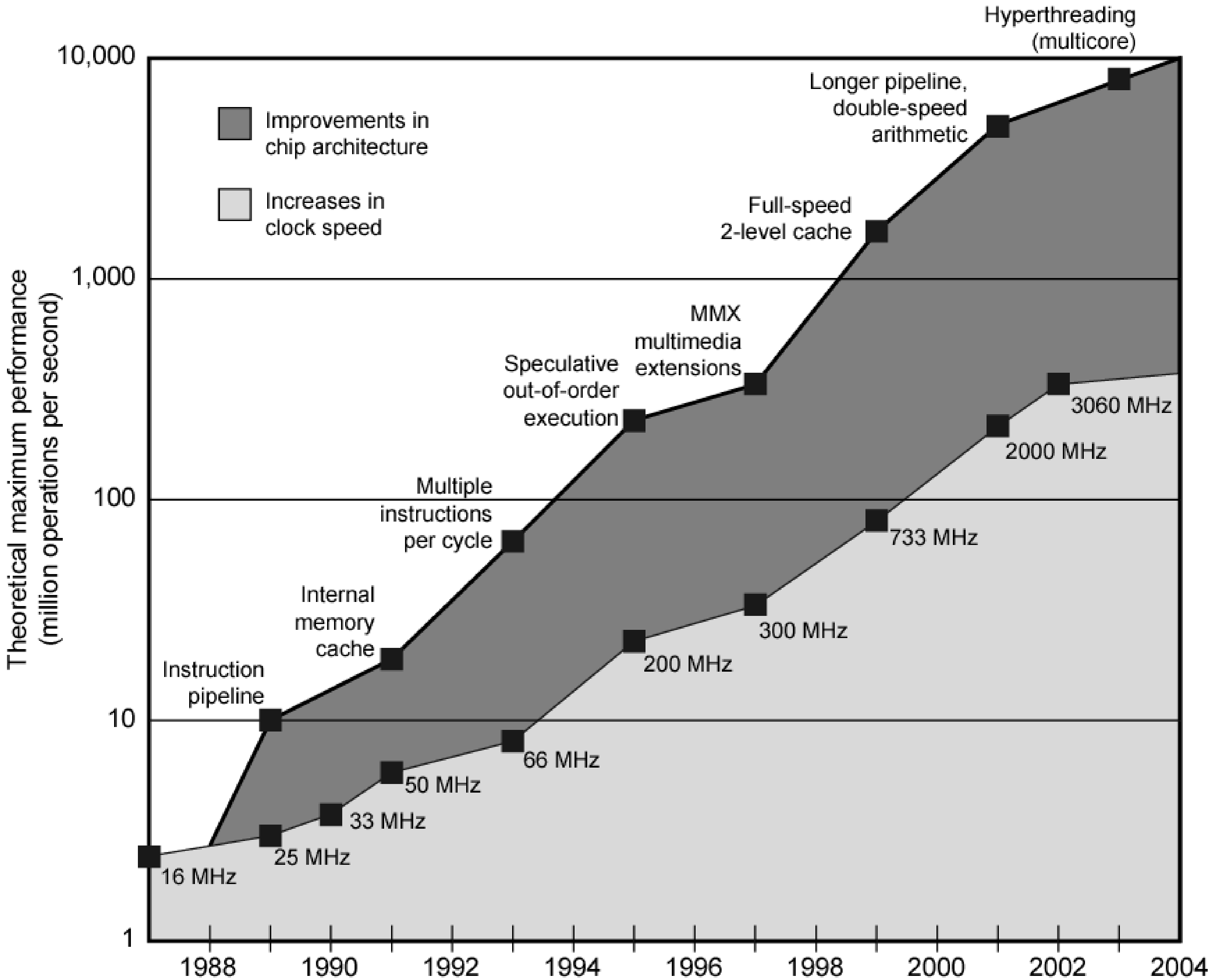
Improvements in Chip Organization and Architecture

- Increase hardware speed of processor
  - Fundamentally due to shrinking logic gate size
    - More gates, packed more tightly, increasing clock rate
    - Propagation time for signals reduced
- Increase size and speed of caches
  - Dedicating part of processor chip
    - Cache access times drop significantly
- Change processor organization and architecture
  - Increase effective speed of execution
  - Parallelism

Problems with Clock Speed and Logic Density

- Power
  - Power density increases with density of logic and clock speed
  - Dissipating heat
- RC delay
  - Speed at which electrons flow limited by resistance and capacitance of metal wires connecting them
  - Delay increases as RC product increases
  - Wire interconnects thinner, increasing resistance
  - Wires closer together, increasing capacitance
- Memory latency
  - Memory speeds lag processor speeds
- Solution:
  - More emphasis on organizational and architectural approaches

Intel Microprocessor Performance



Increased Cache Capacity

- Typically two or three levels of cache between processor and main memory
- Chip density increased
  - More cache memory on chip
    - Faster cache access
- Pentium chip devoted about 10% of chip area to cache
- Pentium 4 devotes about 50%

More Complex Execution Logic

- Enable parallel execution of instructions
- Pipeline works like assembly line
  - Different stages of execution of different instructions at same time along pipeline
- Superscalar allows multiple pipelines within single processor
  - Instructions that do not depend on one another can be executed in parallel

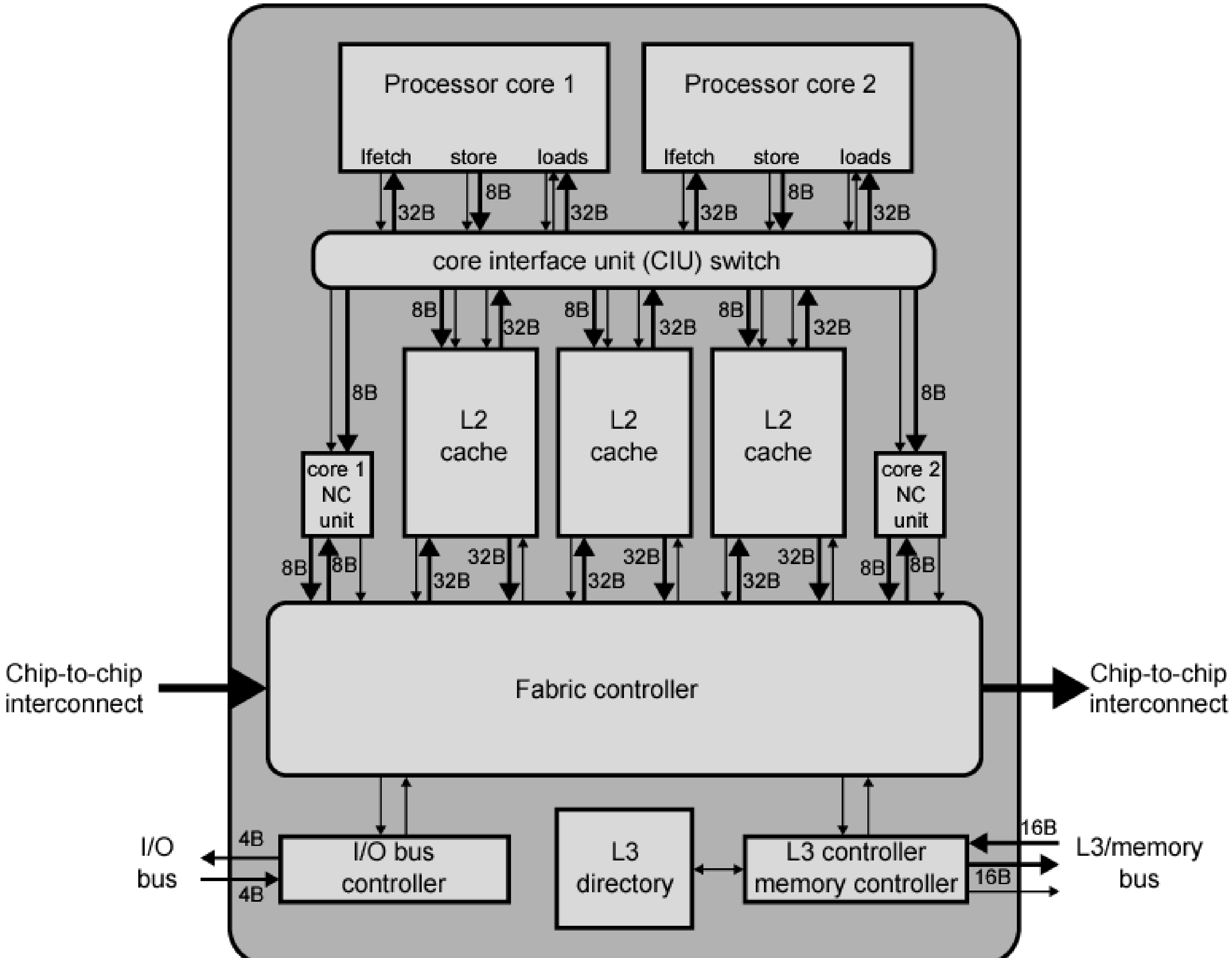
Diminishing Returns

- Internal organization of processors complex
  - Can get a great deal of parallelism
  - Further significant increases likely to be relatively modest
- Benefits from cache are reaching limit
- Increasing clock rate runs into power dissipation problem
  - Some fundamental physical limits are being reached

New Approach – Multiple Cores

- Multiple processors on single chip
  - Large shared cache
- Within a processor, increase in performance proportional to square root of increase in complexity
- If software can use multiple processors, doubling number of processors almost doubles performance
- So, use two simpler processors on the chip rather than one more complex processor
- With two processors, larger caches are justified
  - Power consumption of memory logic less than processing logic
- Example: IBM POWER4
  - Two cores based on PowerPC

POWER4 Chip Organization



NC = noncacheable

Pentium Evolution (1)

- 8080
  - first general purpose microprocessor
  - 8 bit data path
  - Used in first personal computer – Altair
- 8086
  - much more powerful
  - 16 bit
  - instruction cache, prefetch few instructions
  - 8088 (8 bit external bus) used in first IBM PC
- 80286
  - 16 Mbyte memory addressable
  - up from 1Mb
- 80386
  - 32 bit
  - Support for multitasking

Pentium Evolution (2)

- 80486
  - sophisticated powerful cache and instruction pipelining
  - built in maths co-processor
- Pentium
  - Superscalar
  - Multiple instructions executed in parallel
- Pentium Pro
  - Increased superscalar organization
  - Aggressive register renaming
  - branch prediction
  - data flow analysis
  - speculative execution

Pentium Evolution (3)

- Pentium II
  - MMX technology
  - graphics, video & audio processing
- Pentium III
  - Additional floating point instructions for 3D graphics
- Pentium 4
  - Note Arabic rather than Roman numerals
  - Further floating point and multimedia enhancements
- Itanium
  - 64 bit
  - see chapter 15
- Itanium 2
  - Hardware enhancements to increase speed
- See Intel web pages for detailed information on processors

PowerPC

- 1975, 801 minicomputer project (IBM) RISC
- Berkeley RISC I processor
- 1986, IBM commercial RISC workstation product, RT PC.
  - Not commercial success
  - Many rivals with comparable or better performance
- 1990, IBM RISC System/6000
  - RISC-like superscalar machine
  - POWER architecture
- IBM alliance with Motorola (68000 microprocessors), and Apple, (used 68000 in Macintosh)
- Result is PowerPC architecture
  - Derived from the POWER architecture
  - Superscalar RISC
  - Apple Macintosh
  - Embedded chip applications

PowerPC Family (1)

- 601:
  - Quickly to market. 32-bit machine
- 603:
  - Low-end desktop and portable
  - 32-bit
  - Comparable performance with 601
  - Lower cost and more efficient implementation
- 604:
  - Desktop and low-end servers
  - 32-bit machine
  - Much more advanced superscalar design
  - Greater performance
- 620:
  - High-end servers
  - 64-bit architecture

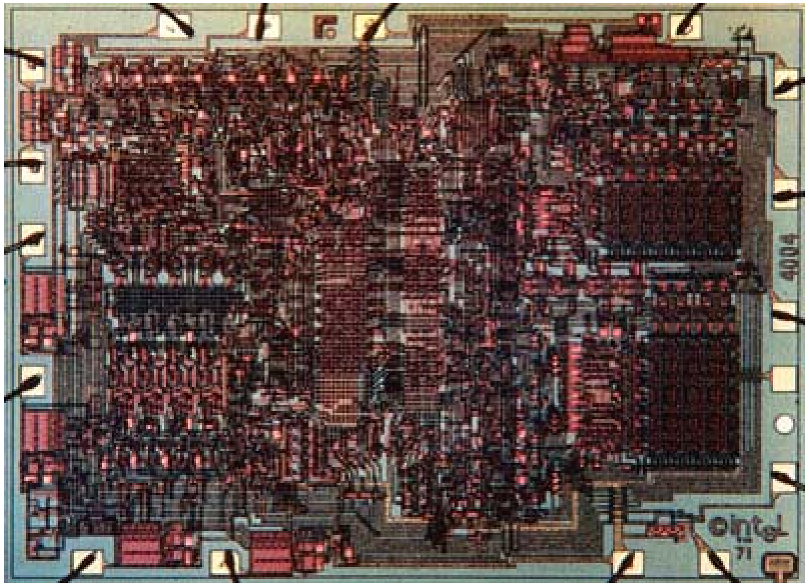
PowerPC Family (2)

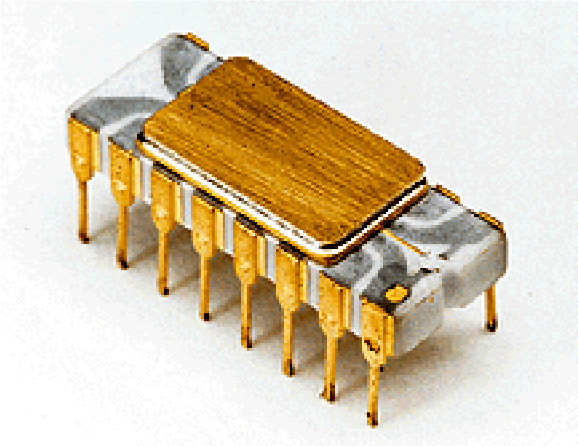
- 740/750:
  - Also known as G3
  - Two levels of cache on chip
- G4:
  - Increases parallelism and internal speed
- G5:
  - Improvements in parallelism and internal speed
  - 64-bit organization

Internet Resources

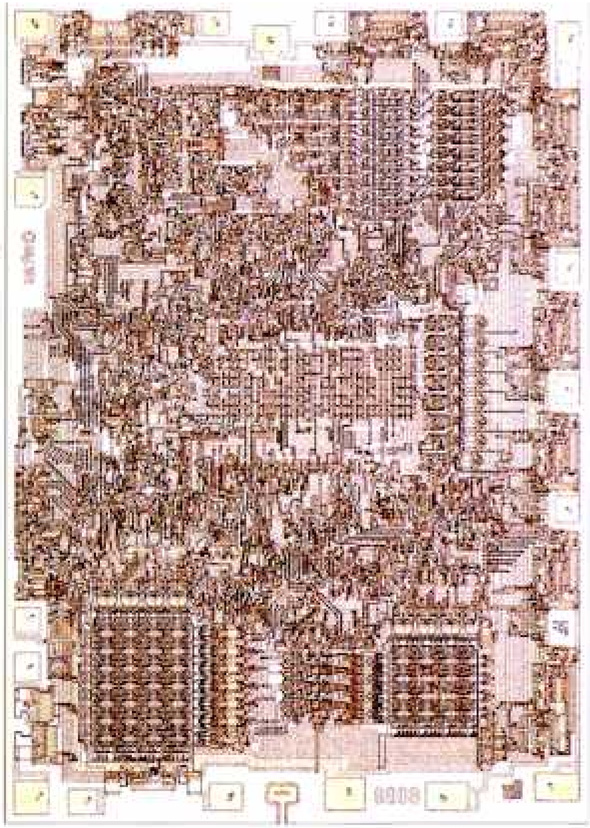
- http://www.intel.com/
  - Search for the Intel Museum
- http://www.ibm.com
- http://www.dec.com
- Charles Babbage Institute
- PowerPC
- Intel Developer Home

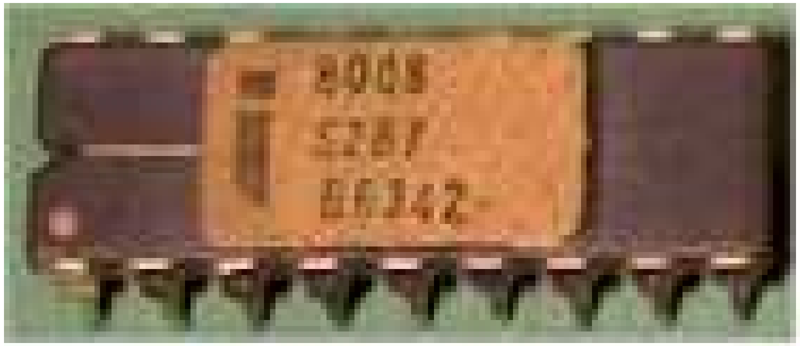
INTEL 4004



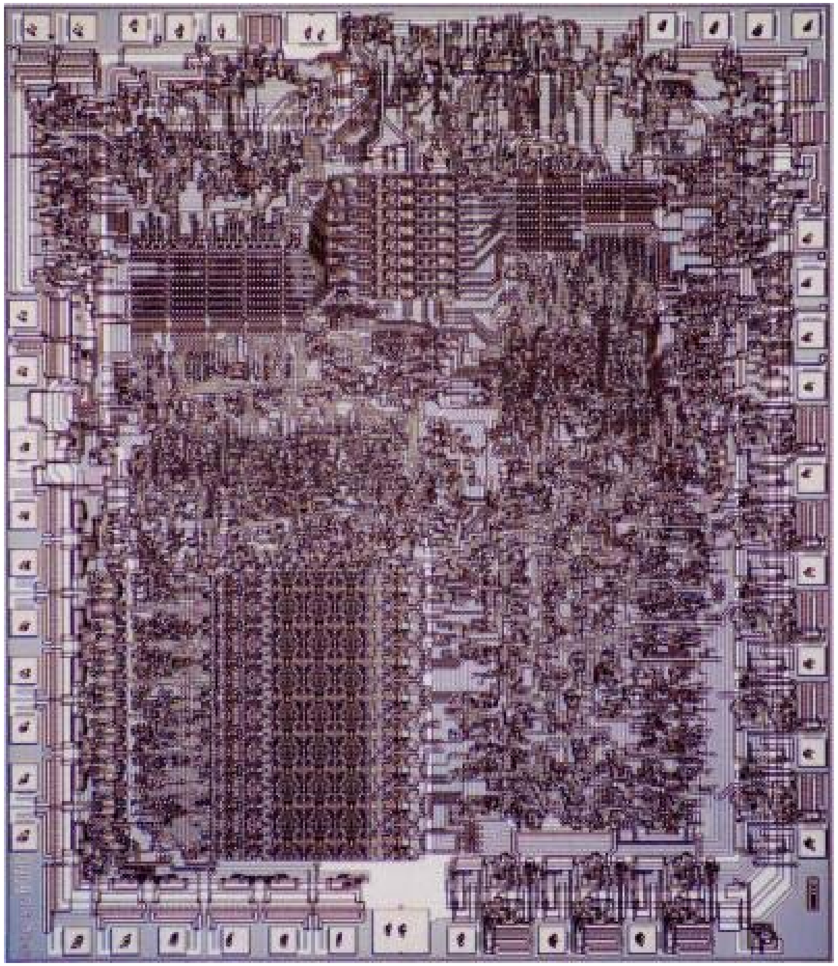


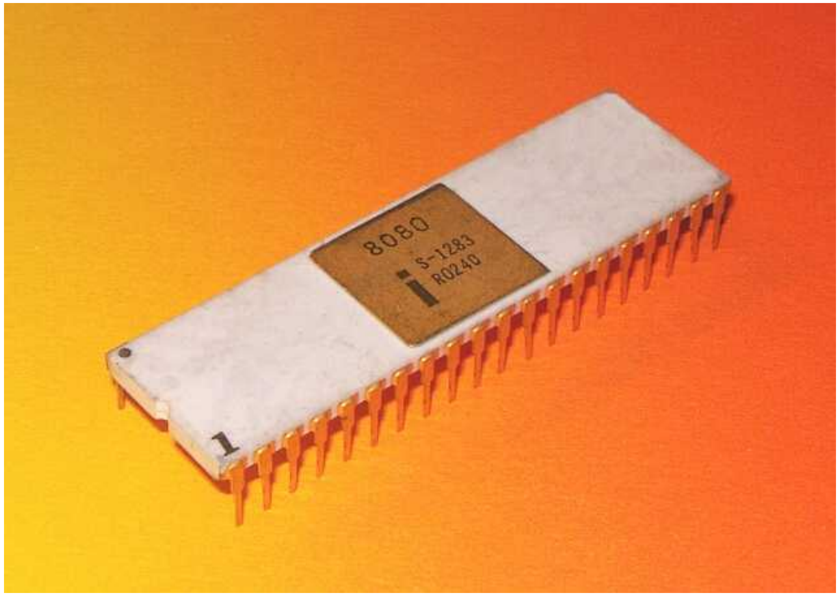
INTEL 8008



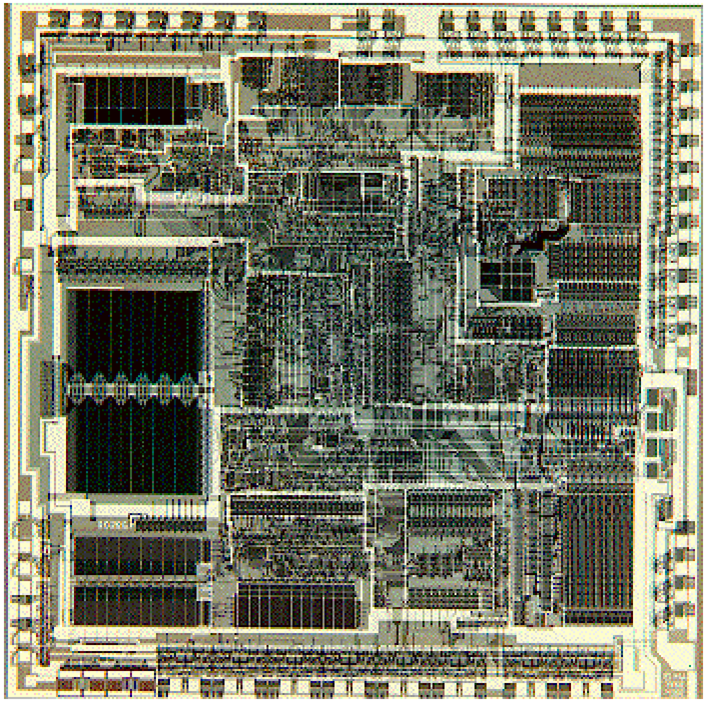


INTEL 8080

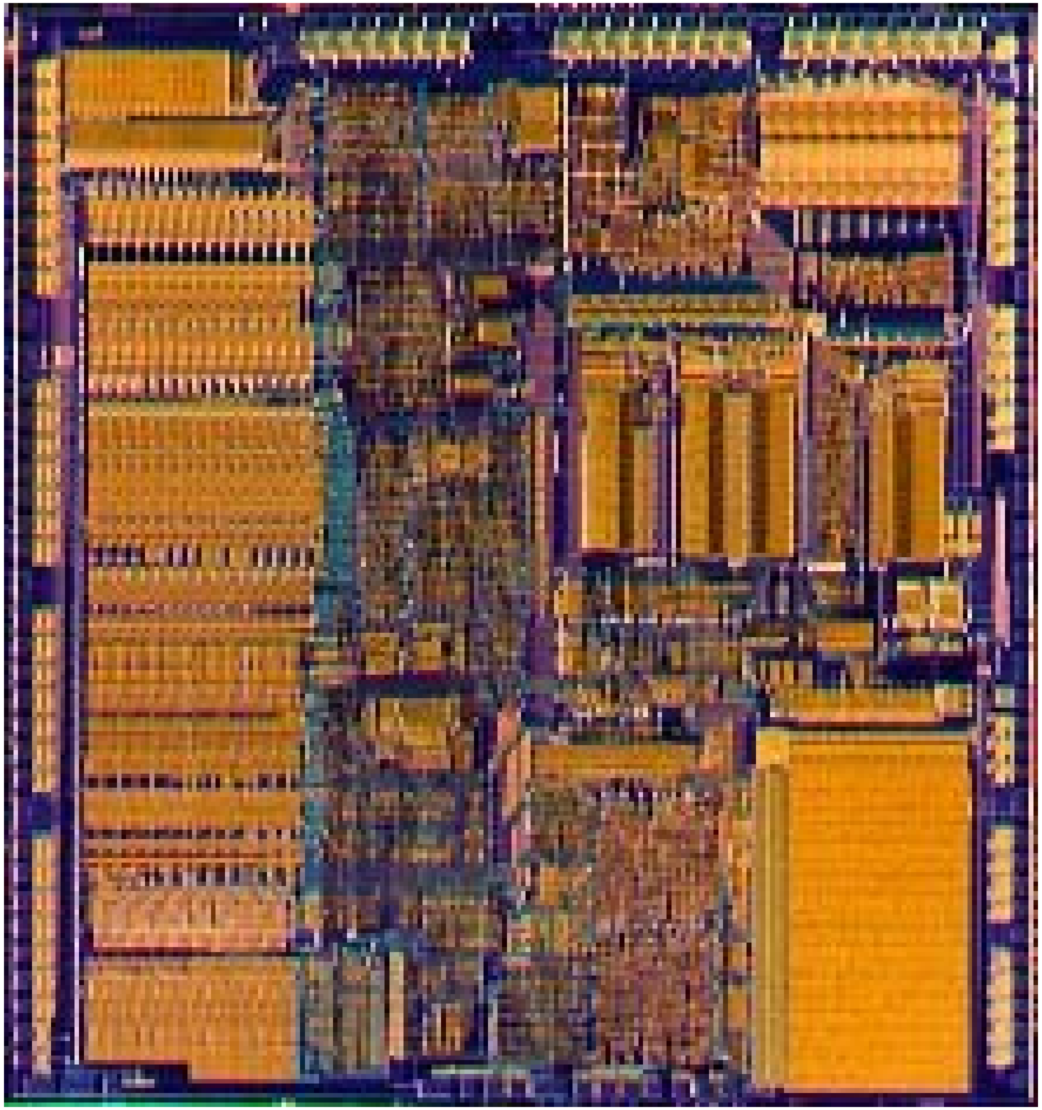


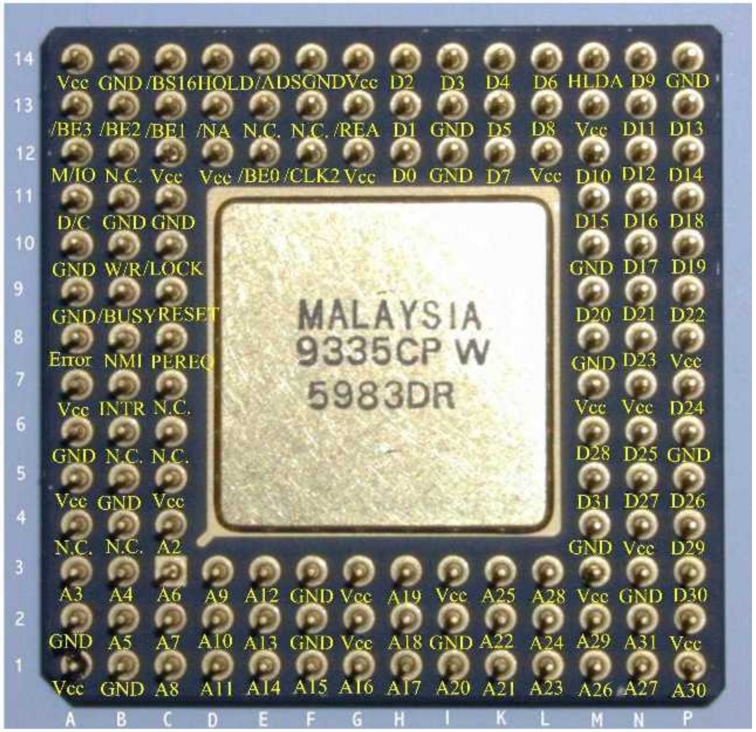


INTEL 80286



INTEL 80386

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13
/BE3 /BE2 /BE1 /NA N.C. N.C. /REA D1 GND D5 D8 Vcc D11 D13
12
M/IO N.C. Vcc Vcc /BE0 /CLK2 Vcc D0 GND D7 Vcc D10 D12 D14
11
D/C GND GND D15 D16 D18
10
GND W/R /LOCK GND D17 D19
9
GND /BUSY RESET D20 D21 D22
8
Error NMI PEREQ GND D23 Vcc
7
Vcc INTR N.C. Vcc Vcc D24
6
GND N.C. N.C. D28 D25 GND
5
Vcc GND Vcc D31 D27 D26
4
N.C. N.C. A2 GND Vcc D29
3
A3 A4 A6 A9 A12 GND Vcc A19 Vcc A25 A28 Vcc GND D30
2
GND A5 A7 A10 A13 GND Vcc A18 GND A22 A24 A29 A31 Vcc
1
Vcc GND A8 A11 A14 A15 A16 A17 A20 A21 A23 A26 A27 A30
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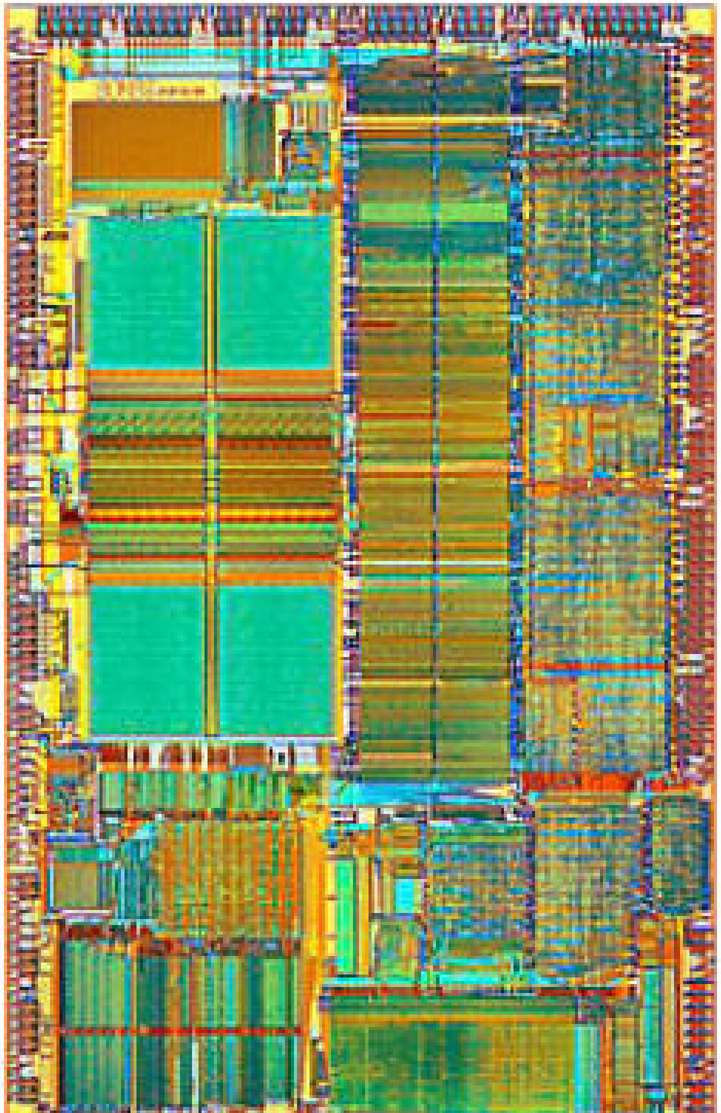
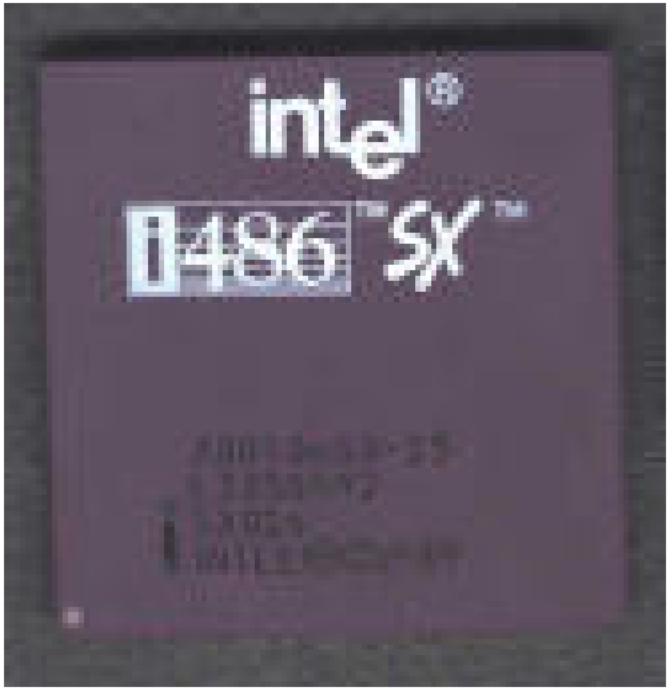
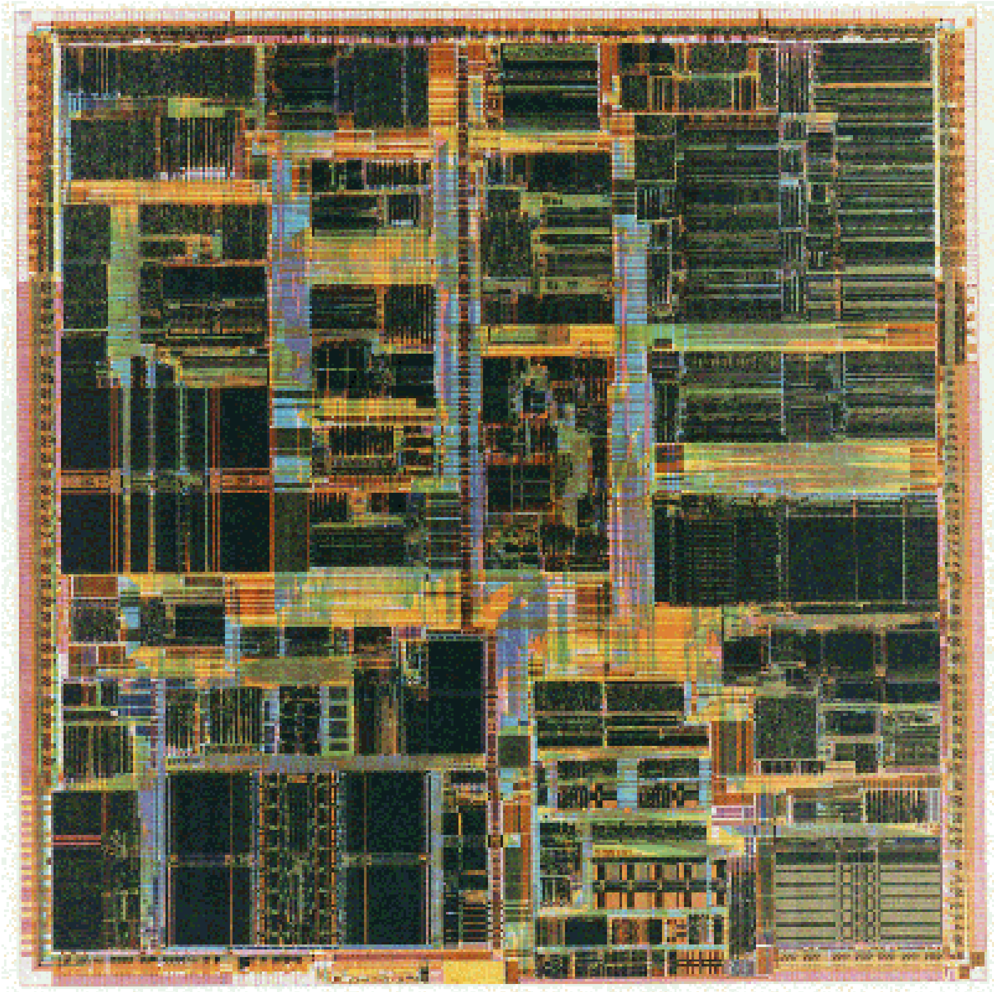
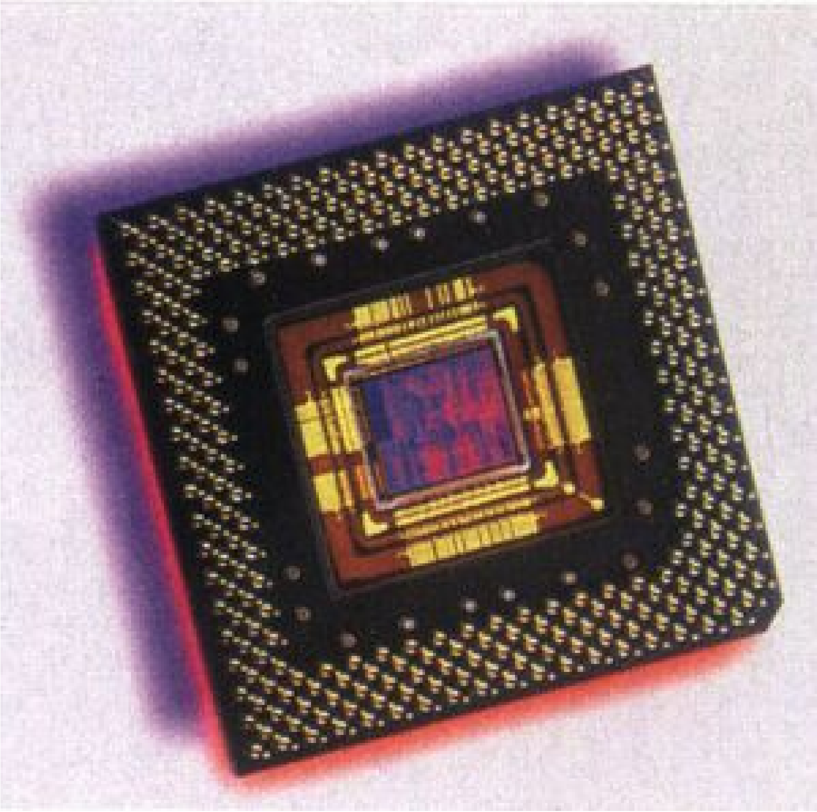
INTEL 80486



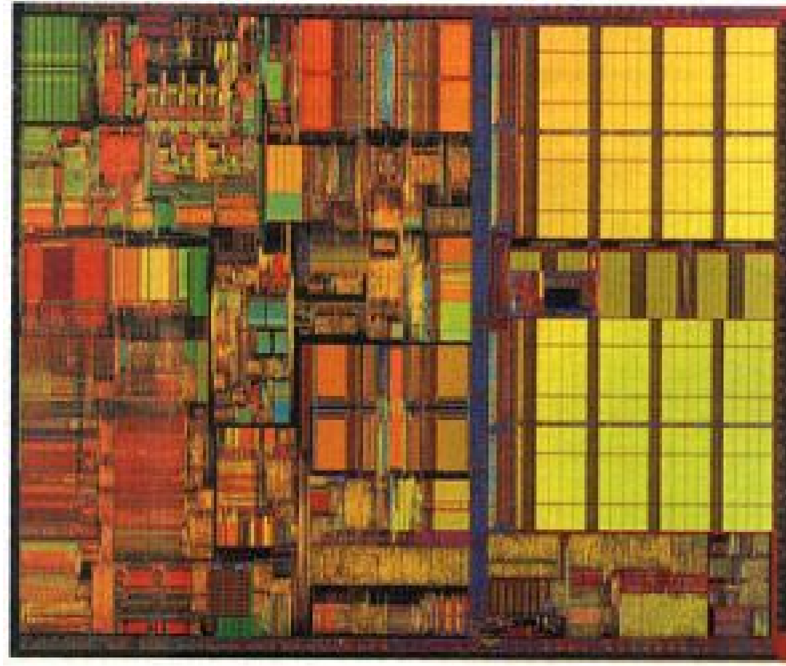


Pentium

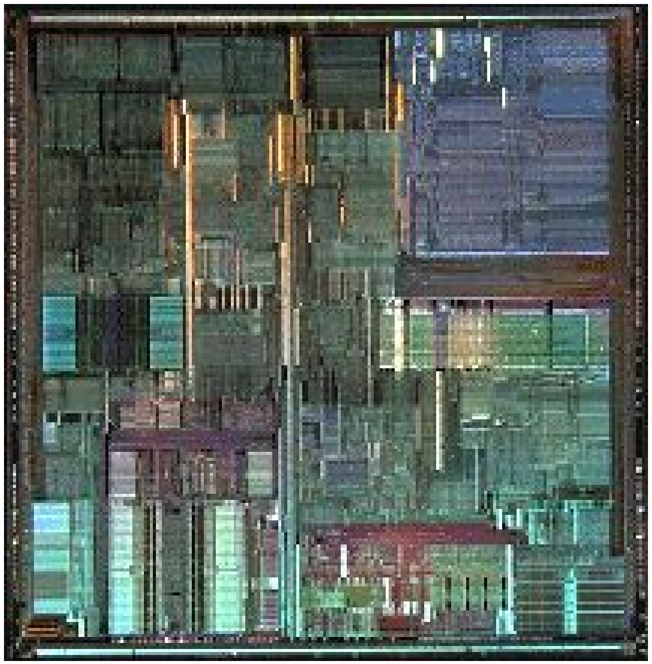




More Pentium

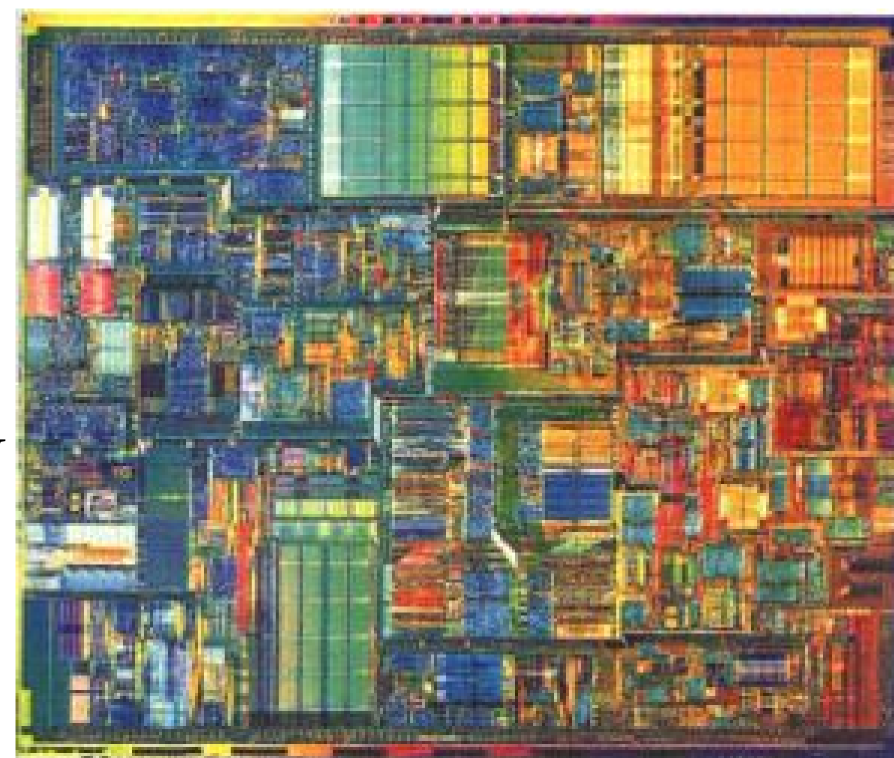


III



Pro

IV



Itanium