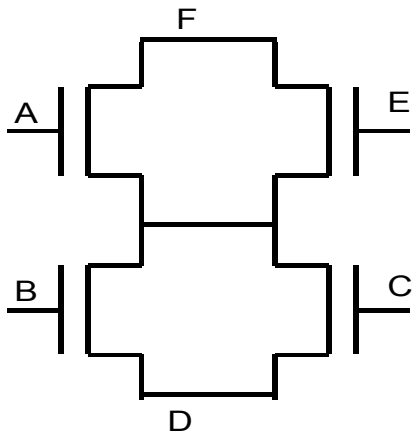
EEM411 DERSİ FİNAL SINAV ÇÖZÜMLERİ

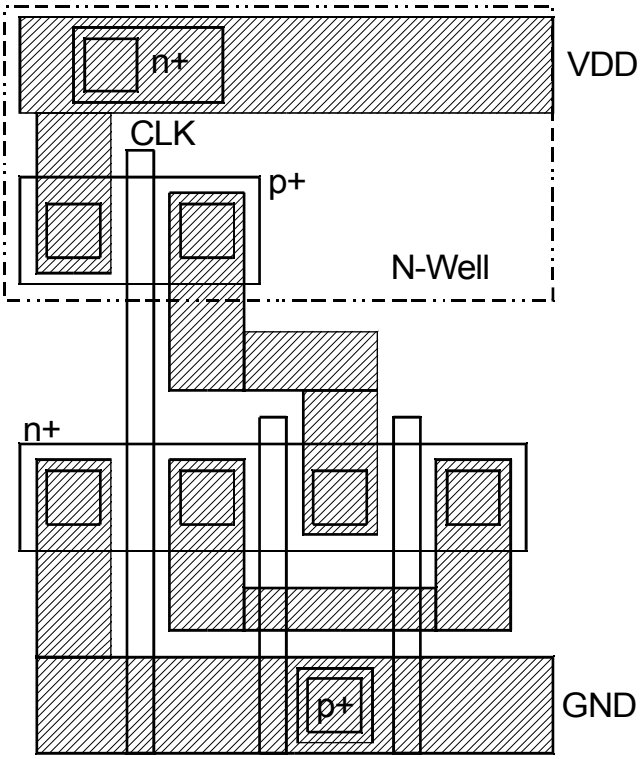
1) (11p) CMOS IC üretim süreci soruları. Aşağıdaki boşlukları bir sözcük ya da sayı ile doldurunuz. Bir yanlış bir doğruyu silmektedir.
   - VDD ve GND bağlantılı tümleşikdevrede P-Well **GND** hattına bağlanır.
   - Metal-4 maskesi uygulanmadan önce **VIA** maskesi uygulanır.
   - Aktif maske altında **FOX** bulunmaz.
   - MOSFET kanal genişliği (channel width) **ACTIVE** maskesi ile belirlenir.
   - Poly ile difüzyon bağlantısını **METAL** maskesi sağlar.
   - N+ koruma halkası (guard ring) **N** kuyusu (well) içindedir.
   - İki metal bağlantısını **VIA** maskesi sağlar.
   - J=2mA/μm olan metal 100μm uzunluğunda ve 20μm genişliğinde ise toplam **40** mA akım geçirebilir.
   - Cja=10fF/μm2, Cjp=20fF/μm olan n+ difüzyon 60μm uzunluğunda ve 10μm genişliğinde ise toplam **8.8** pF kapasite değerindedir.
   - Rs=30Ω/kare olan poly 100μm uzun ve 30μm genişliğinde ise toplam **100Ω** direnç değerindedir.
   - Koruma halkası (guard ring) **GENİŞ** MOSFET'lerde kullanılmalıdır.
   - "Latch-up" sorununun oluşum nedeni CMOS sürecinde oluşan **BJT** yapılardır.
   - Bir kütüphanede bulunan standart hücrelerin **YÜSEKLİĞİ** aynıdır.
   - Standart hücre seriminde (standard-cell layout) bitişik bağlantı kanalları arasında bağlantıyı **FEEDTHROUGH** hücresi sağlar.
   - 1000μm uzunluğundaki metal teldeki sinyal gecikmesi **0.019** ns'dir. Rw=0.1Ω/μm, Cw=0.5fF/μm verilmiştir.

2) Yazım hatası nedeniyle sınav soru kağıdında 2 numaralı soru yer almamıştır. Toplam soru sayısı da 19 yerine 18 olmuştur.

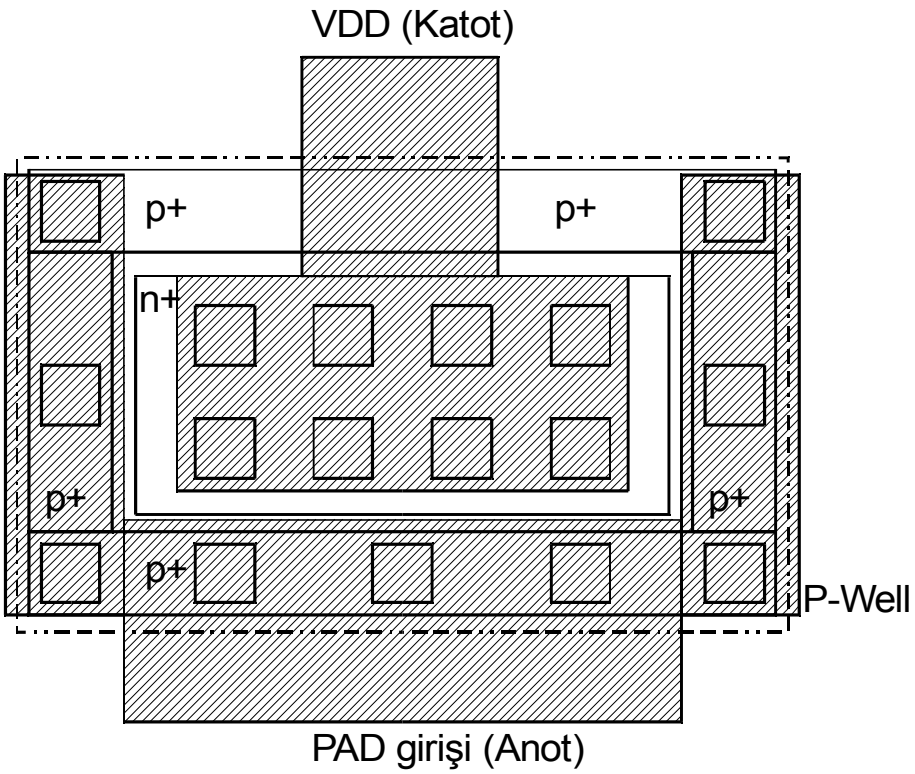
3) (5p)



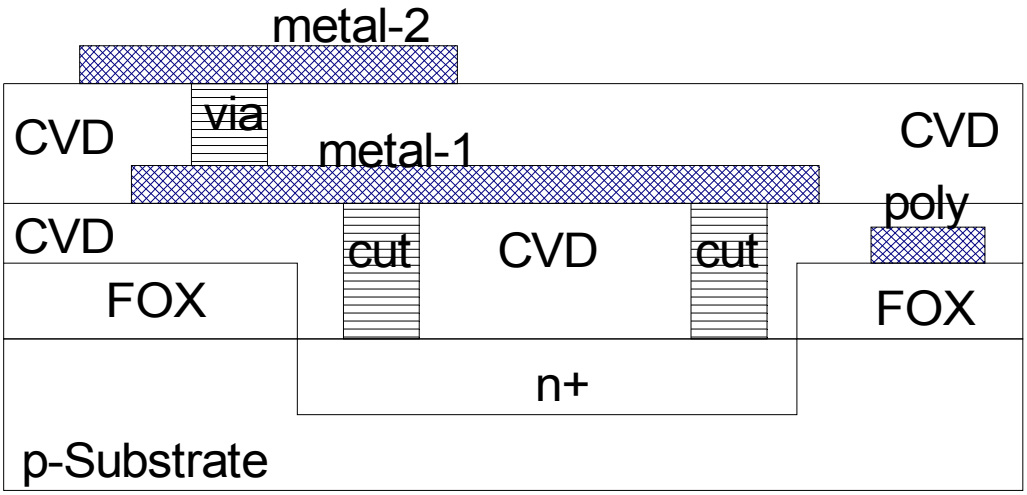
4) (5p)


n+
VDD
CLK
p+
N-Well
n+
p+
GND

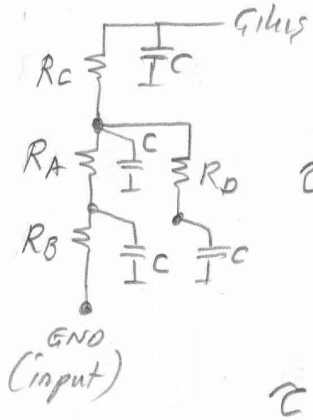
5) (3p)


VDD (Katot)
p+
p+
n+
p+
p+
p+
P-Well
PAD girişi (Anot)

6) (5p)


metal-2
via
CVD
metal-1
CVD
poly
CVD
cut
CVD
cut
FOX
FOX
n+
p-Substrate

7)



En kötü durum: M_E = OFF

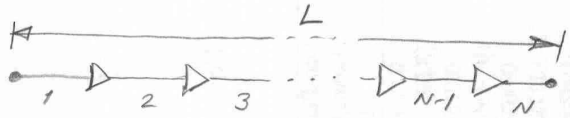
$$\tau = C(R_B) + C(R_B+R_A) + C(R_B+R_A) + C(R_B+R_A+R_C)$$

$$= RC + 2RC + 2RC + 3RC$$

$$\tau = 8RC = 800\ psec.$$

$$\Rightarrow t_p = 0.69\,\tau \cong 550\ psec.$$

8)



$$t_{d_1} = 0.38\frac{RC}{N^2} = \frac{380}{N^2}\ nsec$$

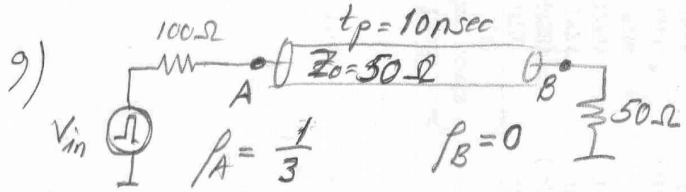
$$t_{d_1} = t_{d_2} = \cdots = t_{d_N}$$

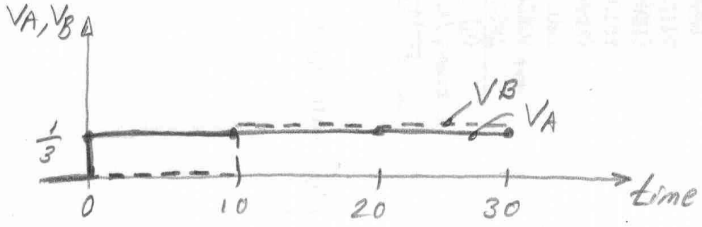
$$t_{d_{toplam}} = N\frac{380}{N^2} + (N-1)\,0.5 = \left(\frac{380}{N} + \frac{N}{2} - 0.5\right) nsec$$

$$\frac{\partial t_{d_{toplam}}}{\partial N} = 0 = -\frac{380}{N^2} + \frac{1}{2} \Rightarrow \frac{380}{N^2} = \frac{1}{2}$$

$$\Rightarrow N^2 = 760 \Rightarrow N \cong 27.6 \Rightarrow \text{Choose } N = 28 \text{ for minimum delay.}$$

9)





@ $t = 0^+$: $V_{in} = 1V$

$$V_A = \frac{Z_0}{Z_0+R_S} = \frac{1}{3}\ V$$

@ $t = 10ns$: $V_B = \frac{1}{3} + V_{reflected}$

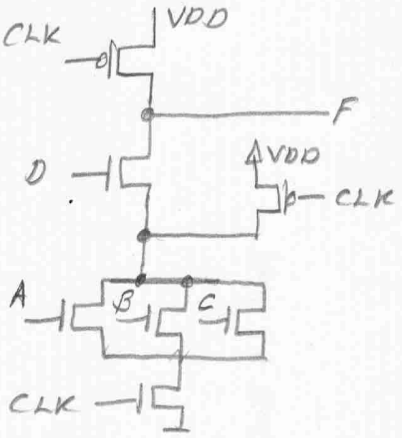
$$\rho_B \tfrac{1}{3} V = 0\ V$$

@ $t = 20ns$:

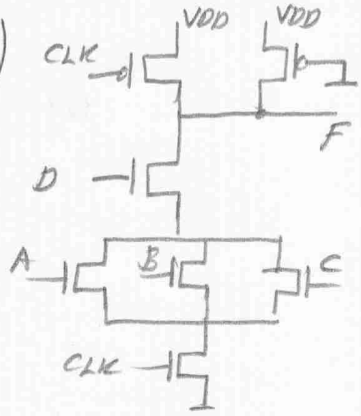
$V_A = V_{initial} + V_{incident} + V_{reflected}$

$$= \frac{1}{3} + \underbrace{\rho_B \tfrac{1}{3}}_{0} + \underbrace{\rho_B \tfrac{1}{3} \rho_A}_{0}$$

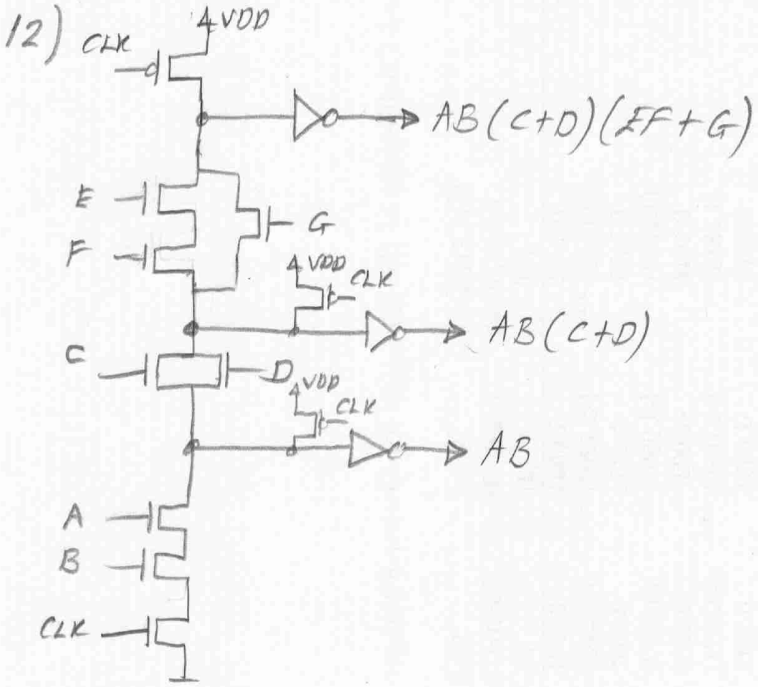
10)


CLK
VDD
F
D
VDD
CLK
A
B
C
CLK

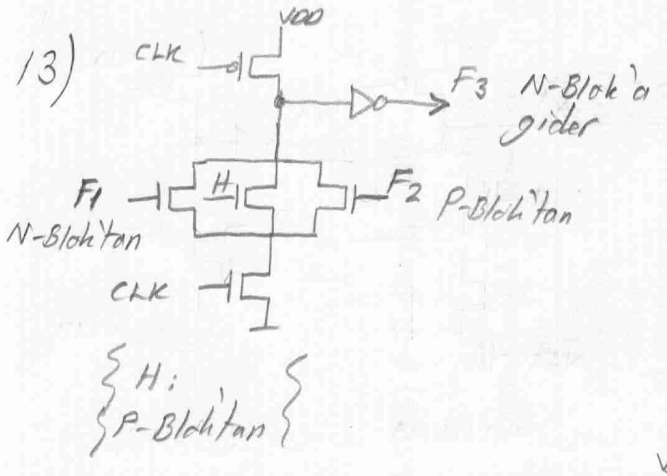
11)

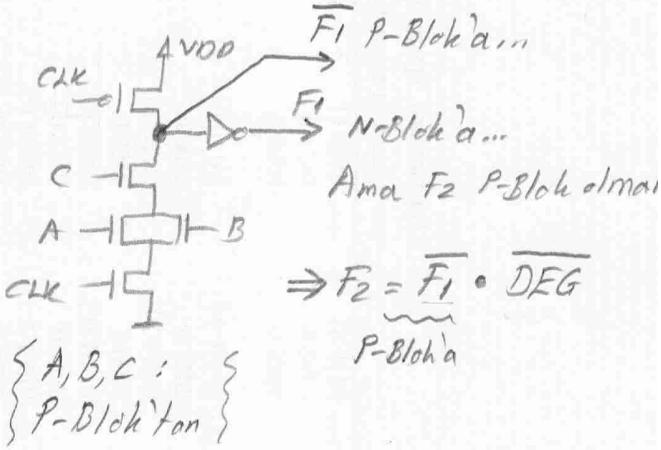

CLK
VDD
VDD
F
D
A
B
C
CLK

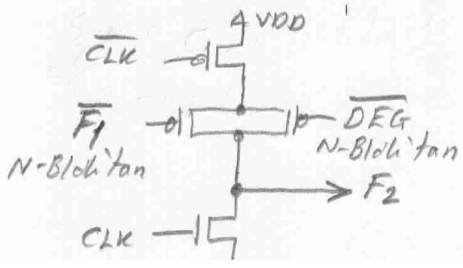
12)

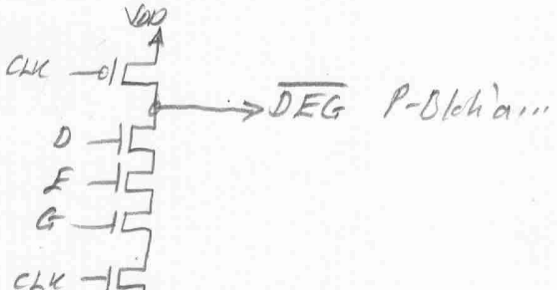

CLK
VDD
AB(C+D)(EF+G)
E
F
G
VDD
CLK
AB(C+D)
C
D
VDD
CLK
AB
A
B
CLK

13)

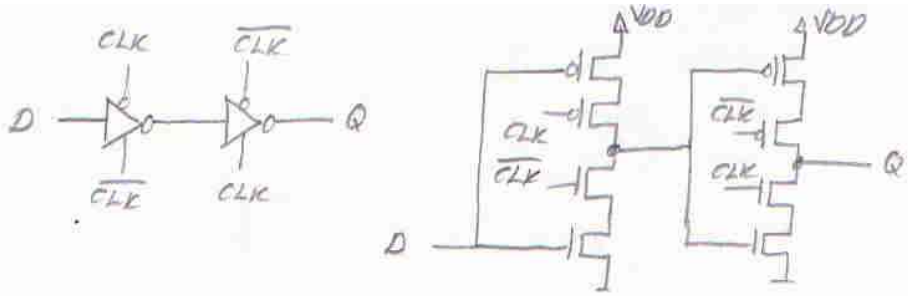

CLK
VDD
F3 N-Blok'a gider
F1
N-Blok'tan
H
F2
P-Blok'tan
CLK
{H: P-Blok'tan}


F1 P-Blok'a...
CLK
VDD
F1
N-Blok'a...
C
A
B
CLK
Ama F2 P-Blok olmalı
⇒ F2 = F1 • DEG
P-Blok'a
{A, B, C : P-Blok'tan}

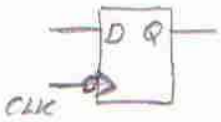

CLK
VDD
F1
DEG
N-Blok'tan
N-Blok'tan
F2
CLK

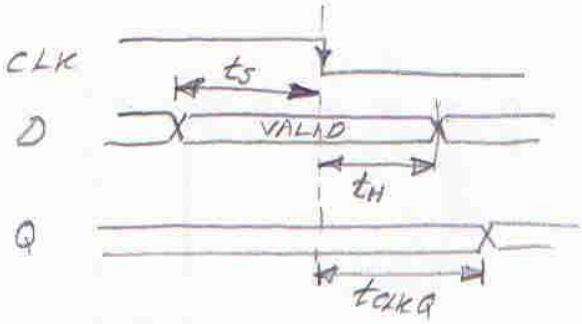

VDD
CLK
DEG P-Blok'a...
D
E
G
CLK

14)



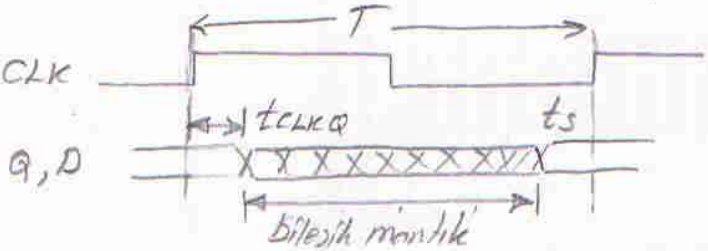
15)





t_S : set-up time
t_H : hold time
t_{CLK-Q} : clock to Q delay.

16)

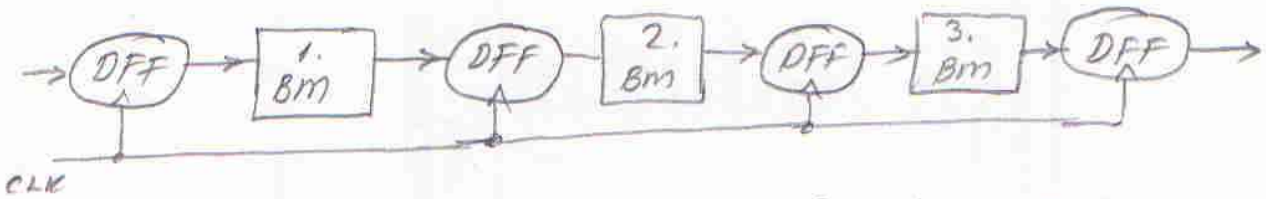


$t_S = 10ns.$
$t_{CLKQ} = 15ns$

$$\Rightarrow T_{min} = t_{CLKQ} + 100ns + t_S = 125ns.$$

$$\Rightarrow f_{CLK_{max}} = \frac{1}{T_{min}} = 8\,MHz.$$

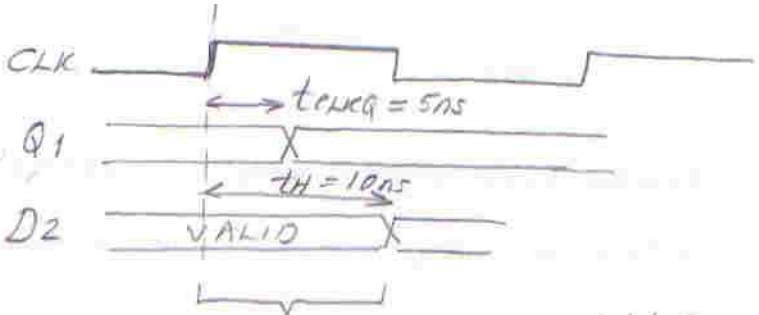
17)



$$\Rightarrow T'_{min} = t_{CLKQ} + \max\{30ns, 50ns, 20ns\} + t_S = 75ns.$$

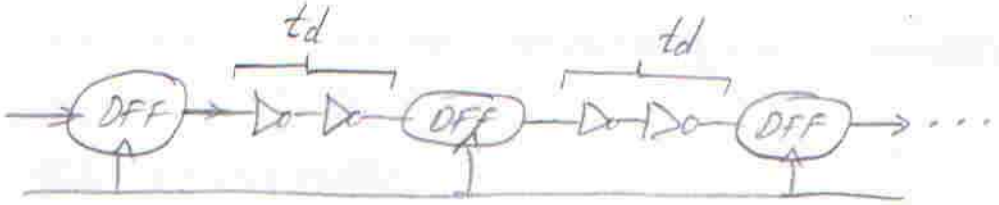
$$\Rightarrow f'_{CLK_{max}} = \frac{1}{T'_{min}} \cong 13.3\,MHz$$

18)



Ama $D_2 = Q_1$! ⇒ Hold time uyumsuz

19)



$t_{d_{min}} = 5ns$