Chapter 2

Practical Transducers

In the last chapter we examined the physics of a Hall-effect transducer and related its performance to physical characteristics and materials properties. While this level of detail is essential for someone designing a Hall-effect transducer, it is not necessary for someone attempting to design with an already existing and adequately characterized device.

2.1 Key Transducer Characteristics

What are the key characteristics of a Hall-effect transducer that should be considered by a sensor designer? For the vast majority of applications, the following characteristics describe a Hall-effect transducer's behavior to a degree that will allow one to design it into a larger system.

- Sensitivity
- Temperature coefficient (tempco) of sensitivity
- Ohmic offset
- Temperature coefficient of ohmic offset
- Linearity
- Input and output resistance
- Temperature coefficient of resistance
- Electrical output noise

Sensitivity

Transducer sensitivity, or gain, was the major focus of much of the last chapter, in which we analyzed the device physics. From a designer's standpoint, more sensitivity is usually a good thing, as it increases the amount of signal available to work with. A

sensor that provides more output signal often require simplers and less expensive support electronics than one with a smaller output signal.

Because the sensitivity of a Hall-effect transducer is dependent on the amount of current used to bias it, the sensitivity of a device needs to be described in a way that takes this into account. Sensitivity can be characterized in two ways:

1. Volts per unit field, per unit of bias current (V/B × I)
2. Volts per unit field, per unit of bias voltage (1/B)

Since a Hall-effect transducer is almost always biased with a constant current, the first characterization method provides the most detailed information. Characterizing by bias voltage, however, is also useful in that it quickly tells you the maximum sensitivity that can be obtained from that transducer when it is used in a bias circuit operating from a given power-supply voltage.

Temperature Coefficient of Sensitivity

Although a Hall-effect transducer has a fairly constant sensitivity when operated from a constant current source, the sensitivity does vary slightly over temperature. While these variations are acceptable for some applications, they must be accounted for and corrected when a high degree of measurement stability is needed. Figure 2-1 shows the variation in sensitivity for an F.W. Bell BH-200 instrumentation-quality indium-arsenide Hall-effect transducer when biased with a constant current. The mean temperature coefficient of sensitivity of this device is about –0.08%/°C.

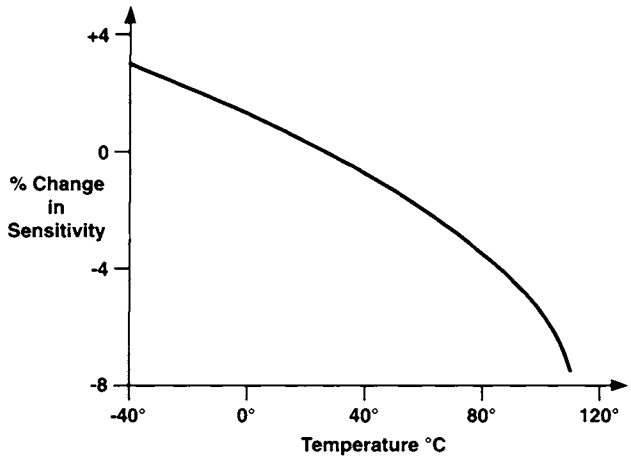

Figure 2-1: Sensitivity vs. temperature for BH-series Hall transducer under constant current bias (after [Bell]).

When operating a Hall-effect transducer from a constant-voltage bias source, one will obtain sensitivity variations over temperature considerably greater than those obtained when operating the device from a constant-current bias source. For this reason constant-current bias is normally used when one is concerned with the temperature stability of the sensor system. For the BH-200 device described above, constant-voltage bias would result in a temperature coefficient of sensitivity of approximately –0.2%/°C.

Ohmic Offset

Because we live in an imperfect world, we can't expect perfection in our transducers. When a Hall-effect transducer is biased, a small voltage will appear on the output even in the absence of a magnetic field. This offset voltage is undesirable, because it limits the ability of the transducer to discriminate small steady-state magnetic fields. A number of effects conspire to create this offset voltage. The first is alignment error of the sense contacts, where one is further "upstream" or "downstream" in the bias current than the other. Inhomogeneities in the material of the transducer can be another source. These effects are illustrated in Figure 2-2. Finally, the semiconductor materials used to make Hall-effect transducers are highly piezoresistive, meaning that the electrical resistance of the material changes in response to mechanical distortion. This causes most Hall-effect transducers to behave like strain gauges in response to mechanical stresses imposed on them by the packaging and mounting.

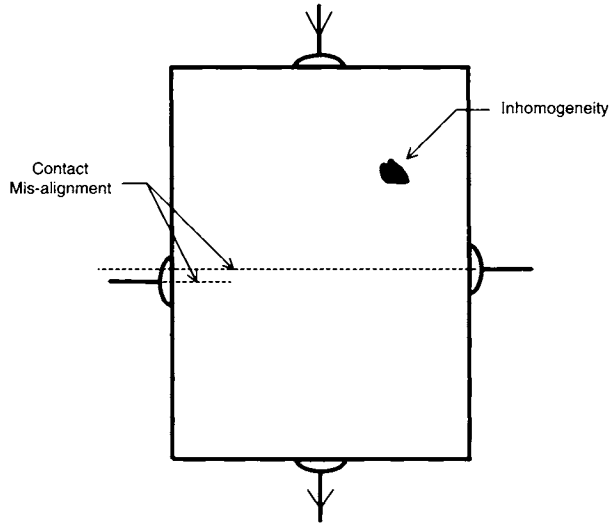

Figure 2-2: Ohmic offsets result from misalignment of the sense contacts and inhomogeneities in the material.

Although offset is usually expressed in terms of output voltage for a given set of bias conditions, it also needs to be considered in terms of magnetic field units. For example, compare a transducer with 500 μV of offset and a sensitivity of 100 μV/gauss, to a second transducer with 200 μV of offset but only 10 μV/gauss of sensitivity. The first transducer has a 5-gauss offset while the latter has an offset of 20 gauss, in addition to having a much lower sensitivity. For applications where low magnetic field levels are to be measured, the first sensor would tend to be easier to use, both because it provides a higher sensitivity and also because it provides a lower offset error when considered in terms of the quantity being measured, namely magnetic field.

Temperature Coefficient of Ohmic Offset

Like sensitivity, the offset of a transducer will drift over temperature. Unlike sensitivity, however, the offset drift will tend to be random, varying from device to device, and is not generally predictable. Some offset drift results from piezoresistive effects in the transducer. As temperature varies, uneven expansion of the materials used to fabricate a transducer will induce mechanical stresses in the device. These stresses are then sensed by the Hall-effect transducer. In general, devices with larger initial offsets also tend to have higher levels of offset drifts. While there are techniques for minimizing offset and its drift, precision applications often require that each transducer be individually characterized over a set of environmental conditions and a compensation scheme be set for that particular transducer.

Linearity

Because Hall-effect transducers are fundamentally passive devices, much like strain gauges, the output voltage cannot exceed the input voltage. This results in a roll-off of sensitivity as the output voltage approaches even a small fraction of the bias voltage. In cases where the Hall voltage is small in comparison to the transducer bias voltage, Hall sensors tend to be very linear, with linearity errors of less than 1% over significant operating ranges. When constructing instrumentation-grade sensors, which are expected to measure very large fields such as 10,000 or even 100,000 gauss, it is often desirable to use low sensitivity devices that do not easily saturate.

Input and Output Resistances

These parameters are of special interest to the circuit designer, as they influence the design of the bias circuitry and the front-end amplifier used to recover the transducer signal. The input resistance affects the design of the bias circuitry, while the output resistance affects the design of the amplifier used to detect the Hall voltage. Although it is possible to design a front-end amplifier with limited knowledge of the resistance of the signal source that will be feeding it, it may be far from optimal from either performance

or cost standpoints, compared to an amplifier designed in light of this information.

For low-noise applications, the output resistance is of special interest, since one source of noise, to be discussed later, is dependent on the output resistance of the device. A simple electrical model describing a Hall-effect transducer from a circuit-interface standpoint is presented later on in Chapter 3.

Temperature Coefficient of Resistance

The temperature coefficient of the input and output resistances will either be identical, or match very closely. Knowing the temperature variation of the input resistance is useful when designing the current source used to bias the transducer. For transducers biased with a constant current source, the bias voltage will be proportional to the transducer's resistance. A bias circuit designed to drive a transducer with a particular resistance at room temperature may fail to do so at hot or cold extremes if variations in transducer resistance are not anticipated. For practical transducers the temperature coefficient of resistance can be quite high, often as much as 0.3%/°C. Over an automotive temperature range (–50° to +125°C) this means that the input and output resistances can vary by as much as 30% from their room temperature values.

Noise

In addition to providing a signal voltage, Hall-effect transducers also present electrical noise at their outputs. For now we will limit our discussion to sources of noise actually generated by the transducer itself, and not those picked up from the outside world or developed in the amplifier electronics.

The most fundamental and unavoidable of electrical noise sources is called Johnson noise, and it is the result of the thermally induced motion of electrons (or other charge carriers) in a conductive material. It is solely a function of the resistance of the device and the operating temperature. Johnson noise is generated by any resistance (including that found in a Hall transducer), and is described by:

$$V_n = \sqrt{4kTRB} \qquad \textbf{(Equation 2-1)}$$

where k is Boltzmann's constant (1.38×10^{-23} K^{-1})
T is absolute temperature in °K
R is resistance in ohms
B is bandwidth in hertz

The bandwidth over which the signal is examined is an important factor in how much noise is seen. The wider the frequency range over which the signal is examined, the more noise will be seen.

The down side of Johnson noise is that it defines the rock-bottom limit of how small a signal can be recovered from the transducer. The two positive aspects are that it can be minimized by choice of transducer impedance, and that it is not usually of tremendous magnitude. A 1-kΩ resistor, for example, at room temperature (300°K) will only generate about 400 nanovolts RMS (root-mean-squared) of Johnson noise measured across a 10-kilohertz bandwidth.

Flicker noise, also known as $1/f$ noise, is often a more significant problem than Johnson noise. This type of noise is found in many physical systems, and can be generated by many different and unrelated types of mechanisms. The common factor, however, is the resultant spectrum. The amount of noise per unit of bandwidth is, to a first approximation, inversely proportional to the frequency; this is why it's also referred to as $1/f$ noise. Because many sensor applications detect DC or near-DC low-frequency signals, this type of noise can be especially troublesome. Unlike Johnson noise, which is intrinsic to any resistance regardless of how it was constructed, the flicker noise developed by a transducer is related to the specific materials and fabrication techniques used. It is therefore possible to minimize it by improved materials and processes.

The following sections describe the construction and characteristics of several types of Hall-effect transducers that are presently in common use.

2.2 Bulk Transducers

A bulk-type transducer is essentially a slab of semiconductor material with connections to provide bias and sense leads to the device. The transducer is cut and ground to the desired size and shape and the wires are attached by soldering or welding. One advantage of bulk-type devices is that one has a great deal of choice in selecting materials. Another advantage is that the large sizes of bulk transducers result in lower impedance levels and consequently lower noise levels than those offered by many other processes. Some key characteristics of an instrument-grade bulk indium-arsenide transducer (the F.W. Bell BH-200) are shown in Table 2-1.

Table 2-1: Key characteristics of BH-200 Hall Transducer

Characteristic	Value	Units
Nominal bias current	150	mA
Sensitivity at recommended bias current (Ibias = 150 mA)[1]	15	μV/G
Sensitivity (current referenced)[1]	100	μV/G•A
Temperature coefficient of sensitivity	–0.08	%/°C
Ohmic offset, electrical (maximum) – (Ibias = 150 mA)	±100	μV
Ohmic offset, magnetic (maximum)[1]	±7	gauss
Tempco of ohmic offset, electrical – (Ibias = 150 mA)	±1	μV/°C

(Continued)

Characteristic	Value	Units
Tempco of ohmic offset, magnetic[1]	±0.07	±gauss/°C
Max linearity error (over ±10 kilogauss)	±1	%
Input resistance (max)	2.5	Ω
Output resistance (max)	2	Ω
Temperature coefficient of resistance	0.15	%/°C

Note 1: These parameters estimated from manufacturer's data

2.3 Thin-Film Transducers

A thin-film transducer is constructed by depositing thin layers of metal and semiconductor materials on an insulating support structure, typically alumina (Al_2O_3) or some other ceramic material. Figure 2-3 provides an idealized structural view of a "typical" thin-film Hall-effect transducer. The thickness of the films used to fabricate these devices can be on the order of 1 μm or smaller.

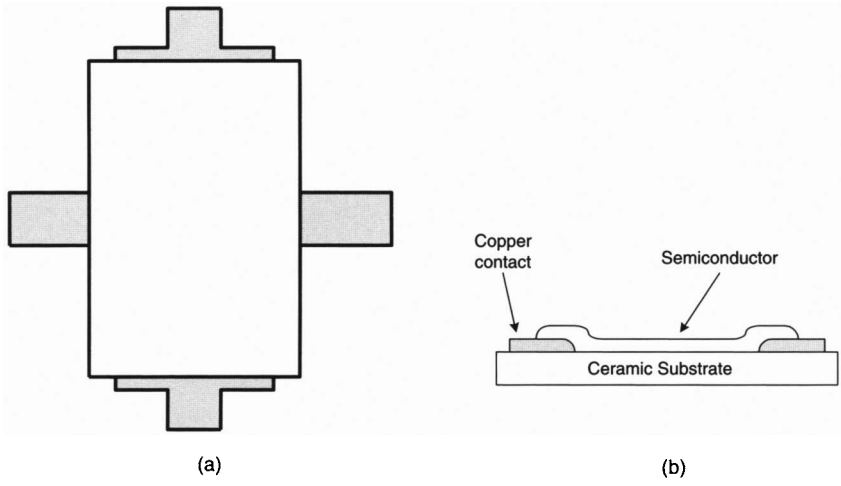

Figure 2-3: Schematic top (a) and cross-section (b) views of thin-film Hall-effect transducer.

The primary advantages of thin-film construction are:

- Flexibility in material selection
- Small transducer sizes achievable
- Thin Hall-effect transducers provide more signal for less bias current
- Photolithographic processing allows for mass production

Each layer is added to the thin-film device by a process that consists of covering the device with the film and selectively removing the sections that are not wanted, leaving the desired patterns. The details of the processing operations for each layer vary depending on the characteristics of the materials being used.

Film deposition is commonly accomplished through a number of means, the two most common being evaporation and sputtering. In evaporation, the substrate to be coated and a sample of the coating material are both placed in a vacuum chamber, as shown in Figure 2-4. The sample is then heated to the point where it begins to vaporize into the vacuum. The vapor then condenses on any cooler objects in the chamber, such as the substrate to be coated. Because the hot vapor in many cases will chemically react with any stray gas molecules, a substantially good vacuum is required to implement this technique. Vacuums of 10^{-6} to 10^{-7} torr (760 torr = 1 atmosphere) are commonly required for this type of process. The thickness of the deposited film is controlled by the exposure time.

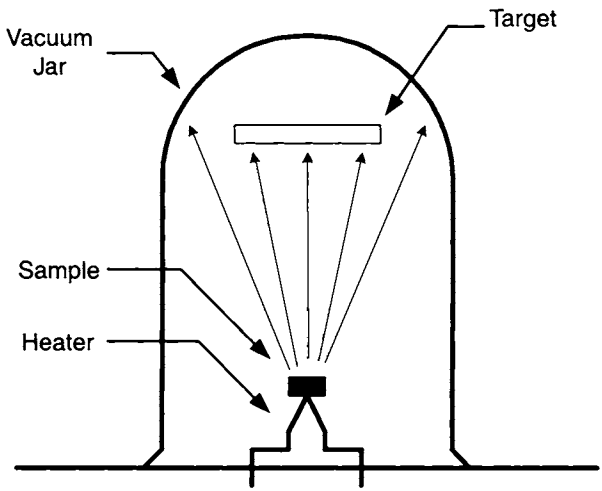

Figure 2-4: Schematic drawing of evaporative thin-film process.

Sputtering is another method for coating substrates with thin films. In sputtering, the sample coating material is not directly heated. Instead, an inert gas, such as argon, is ionized into a plasma by an electrical source. The velocity of the ions of the plasma is sufficient to knock atoms out of the coating sample (the target), at which point they can deposit themselves on the substrate to be coated. As in the case of an evaporative coating system, film thickness is controlled by exposure time. Figure 2-5 shows a schematic view of a sputtering system.

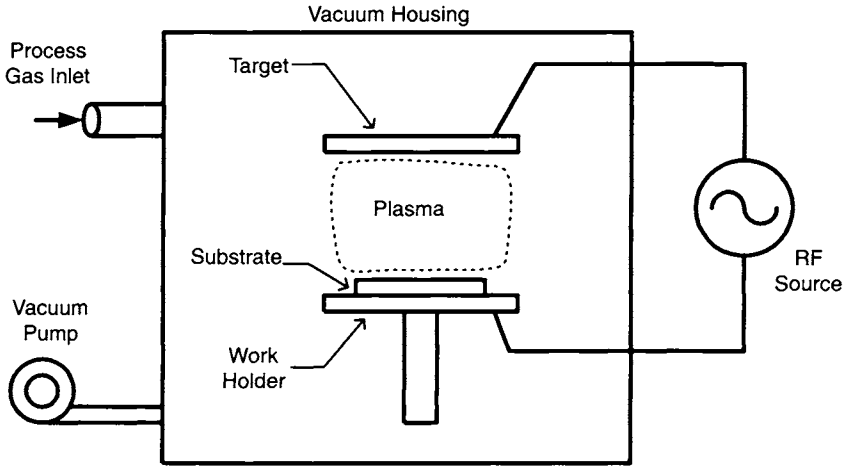

Figure 2-5: Sputtering method of thin-film deposition.

The principal advantage offered by sputtering over evaporation is that, because the coating material doesn't need to be heated to near its evaporation point, it is possible to make thin films with a much wider variety of materials than is possible by evaporation.

Once a material has been laid down in a thin film, it is then patterned with a photoresist material, exposed to a photographic plate carrying the desired pattern, and the photoresist is then developed, leaving areas of the substrate selectively exposed. The substrate is then etched, often by immersion in a suitable liquid solvent or acid. Alternatively, the substrate can be plasma-etched by a process related to sputtering. In either case, after the etching step is finished, the remaining photoresist is stripped and the substrate is prepared to receive the next layer of film or readied for final processing. The sequence of operations needed to process a layer of a thin film is summarized in Figure 2-6.

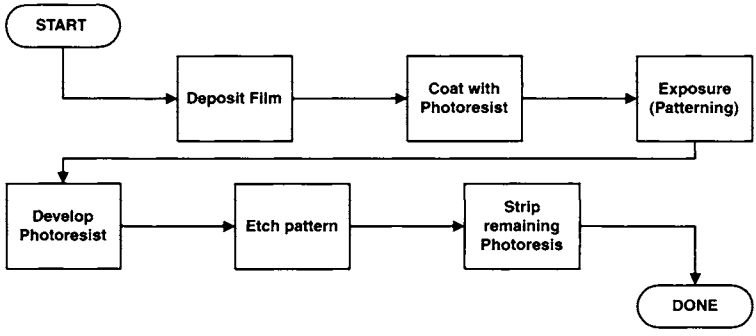

Figure 2-6: Thin-film processing sequence.

The HS-100 is an example of a commercial thin-film Hall transducer manufactured by F.W.Bell. This device is made with two thin-film layers, a metal layer to provide contacts to the Hall-effect element, and an indium-arsenide thin film that forms the Hall-effect transducer itself. In addition, solder bumps are deposited on the copper to provide connection points to the outside world. Wires may be soldered to these features, or the device may be placed face down on a printed circuit board or ceramic hybrid circuit, and reflow soldered into place.

Key specifications for the HS-100 transducer are listed in Table 2-2. The major improvements over bulk devices are in the area of sensitivity and supply current; the thin-film device is nearly as sensitive as the previously described bulk device (BH-200), and obtains this level of sensitivity with an order of magnitude less supply current needed. The BH-200 bulk device, however, is superior in the areas of offset error and drift over temperature. The principal advantage of the thin-film device is potentially lower cost. Thin-film processing techniques allow a great number of devices to be fabricated simultaneously and separated into individual units at the end of processing.

Table 2-2: Key characteristics of HS-100 Hall transducer

Characteristic	Value	Units
Nominal bias current	150	mA
Sensitivity at recommended bias current (Ibias = 10 mA)[1]	8	μV/gauss
Sensitivity (current referenced)[1]	800	μV/gauss•A
Temperature coefficient of sensitivity	–0.1	%/°C
Ohmic offset, electrical (maximum) (Ibias = 10 mA)	±6	mV
Ohmic offset, magnetic (maximum)[1]	±750	Gauss
Tempco of ohmic offset, electrical (Ibias = 10 mA)	±10	μV/°C
Tempco of ohmic offset, magnetic[1]	±1.25	±gauss/°C
Max linearity error (over ±10 kilogauss)	—	%
Input resistance (max)	160	Ω
Output resistance (max)	360	Ω
Temperature coefficient of resistance	0.1	%/°C

Note 1: These parameters estimated from manufacturer's data

2.4 Integrated Hall Transducers

Making a Hall-effect transducer out of silicon, using standard integrated circuit processing techniques, allows one to build complete sensor systems on a chip. The trans-

ducer bias circuit, the front-end amplifier, and in many cases application-specific signal processing can be combined in a single low-cost unit. The addition of electronics to the bare transducer allows sensor manufacturers to provide a very high degree of functionality and value to the end user, for a modest price. By simultaneously fabricating thousands of identical devices on a single wafer, it is possible to economically produce large numbers of high-quality sensors. Figure 2-7 shows an example of several hundred Hall-effect sensors on a silicon wafer, before being separated and individually packaged.

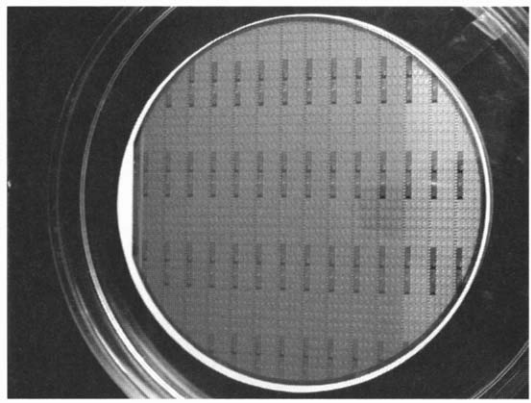

Figure 2-7: Hall-effect sensor ICs on a silicon wafer. *(Courtesy of Melexis USA.)*

While there are many layers and structures available in modern integrated circuit processes that can be exploited to fabricate Hall-effect transducers, we will illustrate the basics by considering one particular case. Because of the complexity of integrated circuit fabrication processes, we will not even attempt to describe them here. Interested readers will find good descriptions of how silicon ICs are made in [GRAY84]. For this example, we will consider what is known as an epitaxial Hall-effect transducer. We will begin by considering the structure of a related device, the epitaxial resistor.

Figure 2-8 shows top views and side views of an epitaxial resistor made with a typical bipolar process. The device is so named because it is built in the epitaxial N-type silicon layer. The raw wafer is usually of a P-type material, and the epitaxial layer is deposited on the surface of the wafer by a chemical vapor deposition (CVD) process, and can be doped independently of the raw wafer. P-type isolation walls are then implanted or diffused into the top surface of the epitaxial layer to form wells (isolated islands) of N-type material. Maintaining each of the wells at a positive voltage with respect to the P-type substrate causes the P-N junctions to be reverse-biased, thus electrically isolating the wells from each other. By providing this junction isolation, one can build independent circuit components such as resistors, transistors, and Hall-effect transducers, in a single, monolithic piece of silicon, using the wells as starting points. The overall depth of epitaxial layers can vary from 2–30 μm for commonly available IC processes.

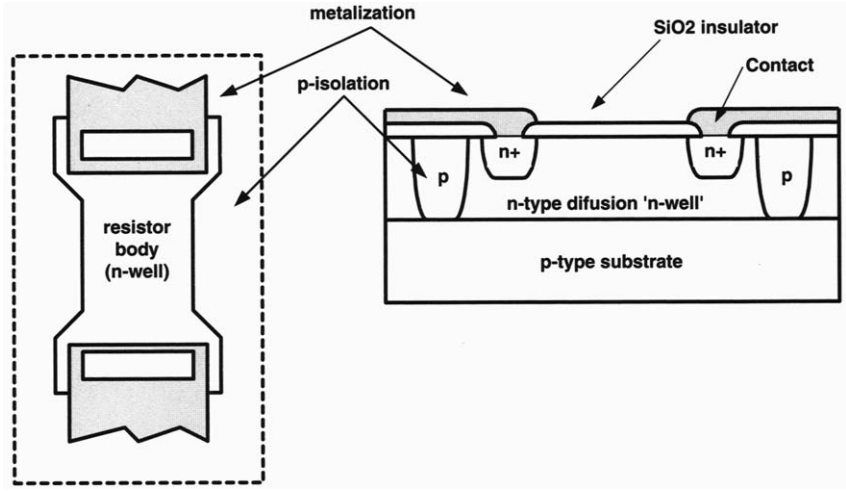

Figure 2-8: Structure of epitaxial resistor showing various layers.

In the case of an epitaxial resistor, the well defines the body of the component. The N-type material used typically has a resistance of about 2–5 kΩ when measured across the opposite edges of a square section. This allows one to readily construct resistors with values up to about 100 kΩ by building long, narrow resistor structures. The whole IC is then covered with an insulating layer of SiO_2 (silica glass), and holes called contact windows are then etched through this glass layer at specific points to allow for electrical contact to the underlying silicon. Finally a layer of aluminum is patterned on top of the SiO_2 to make to form the "wiring" for the IC, with the metal extending down through the contact windows to connect to the silicon. To get a good electrical contact with the aluminum, a plug of high concentration N-type material (somewhat confusingly referred to as "N+" material) is driven into the epitaxial resistor just under the contact areas before the SiO_2 is grown over the device.

"Epi" resistors, as they are commonly called, are easy to make in a bipolar process because they require no additional process steps beyond those required to make NPN transistors. Their performance characteristics, however, are fairly awful, at least when compared to the discrete resistors most electronic designers commonly use. Their absolute tolerance is on the order of ±30%, and they experience temperature coefficients of up to 0.3%/°C. In addition, the effective thickness of the reverse-biased P-N junction that isolates an epi resistor from the substrate varies with applied voltage. This has the effect of making the resistor's value dependent on the voltage applied at its terminals.

Despite the drawbacks of using the epitaxial layer when making resistors, it is quite useful for making Hall-effect transducers. Because the epitaxial layer is relatively thin (5 μm is thin from a macroscopic perspective), and usually made from

lightly ($N = 10^{15}/cm^3$) doped silicon, it is possible to make reasonably sensitive Hall-effect transducers that have modest power requirements.

Because IC manufacturers view the exact details of their processes as trade secrets and are thus not inclined to broadcast them to the world, we will present an example of a Hall device fabricated with a "generic" bipolar process. This will give a general idea of the performance one can expect from such a device. Figure 2-9 shows the details of this device.

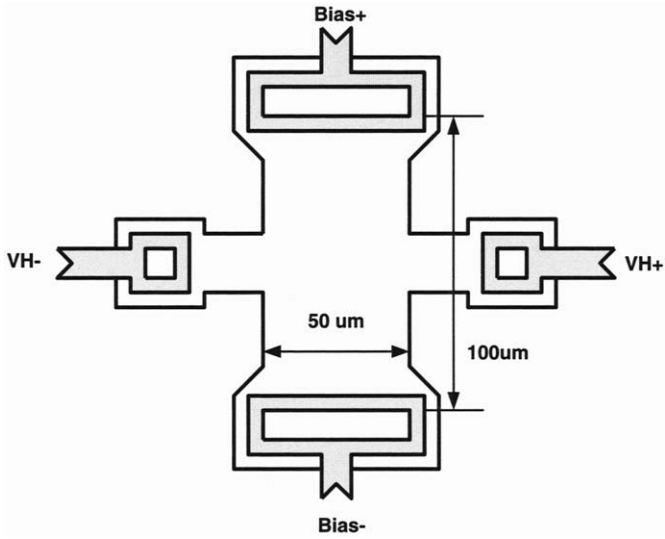

Figure 2-9: Integrated epitaxial Hall-effect transducer layout.

Note that the connections of the sense terminals are made by bringing out "ears" of epitaxial material from the body of the device and making metal contact at these points, instead of simply placing the sense contacts directly on the transducer. There are two reasons for doing this: the first is to maximize the sensitivity by ensuring that all the bias current flows between the sense terminals, and the second is to minimize ohmic offsets. Because the "ears" are fabricated in the same process step as the rest of the transducer, a high degree of alignment is naturally maintained. Metalization and contact windows, on the other hand, are fabricated in separate manufacturing steps, increasing the opportunities for contact misalignment.

For this transducer, the critical physical parameters are:

- Length = 200 μm
- Width = 100 μm
- Thickness (of epi layer) = 10 μm

- Carrier concentration = $3 \times 10^{15}/cm^3$ ($3 \times 10^{21}/m^3$)
- Bulk resistivity $\sigma = 2\ \Omega$-cm (0.02 Ω-m)

The sensitivity per unit of current and field can be calculated by using equation 1-10, yielding:

$$V_H = \frac{IB}{q_0 Nd} = \frac{1A \cdot 1T}{1.6\times10^{-19}C \cdot 3\times10^{21}m^{-3} \cdot 10^{-5}m} = 208V \qquad \textbf{(Equation 2-1)}$$

for 1 tesla at 1 ampere of bias, or 20.8 mV/G-A in cgs units. This is an amazingly high level of sensitivity. This sensor, however, will never operate at one ampere; 1 milliampere is a more realistic bias current. Even at 1 milliampere, however, this transducer will still provide 20 μV/gauss.

The next major question is that of input and output resistance. Because the bias current flows in a substantially uniform manner between the bias contacts, since the contacts extend across the width of the transducer, we can make a fairly good estimate of the input resistance by:

$$R_{in} = \sigma\frac{L}{W \cdot T} = 0.02\Omega \cdot m\frac{200\times10^{-6}m}{100\times10^{-6}m \cdot 10^{-5}m} = 4000\Omega \qquad \textbf{(Equation 2-2)}$$

It therefore requires 4V to bias the transducer with 1 mA.

Because of geometric factors, the output resistance cannot be as readily calculated as the input resistance. If one were to apply a voltage between the output terminals, the lines of current flow would not be parallel and uniform (and therefore amenable to back-of-envelope analysis). For purposes of designing a compatible front-end amplifier and noise calculations, one might assume that the resistance of the output is within a factor of two or three of that of the input.

Because the estimation of temperature sensitivities and ohmic offset is very difficult (if not impossible) even when one is working with a fully characterized process, we shall ignore them. Suffice it to say, however, that integrated Hall-effect transducers can be made with substantially good performance in these areas. For sake of comparison with the previous examples, Table 2-3 lists a few of the predicted and "guesstimated" characteristics of our hypothetical integrated transducer.

Table 2-3: Key characteristics of hypothetical silicon integrated Hall-effect transducer

Characteristic	Value	Units
Sensitivity at recommended bias current (Ibias = 1 mA)	20	μV/G
Sensitivity (current referenced)	20	mV/G•A

(Continued)

Characteristic	Value	Units
Temperature coefficient of sensitivity (for constant-current bias)	–0.1	%/°C
Ohmic offset, electrical (maximum) (Ibias = 1 mA)	±10	mV
Ohmic offset, magnetic (maximum)	±500	G
Max linearity error (over ±1 kilogauss)	1	%
Input resistance	4000	Ω
Output resistance	4000?	Ω
Temperature coefficient of resistance	0.3	%/°C

It is also possible to construct integrated Hall-effect transducers from gallium-arsenide, germanium, and other semiconductor materials for even better performance. Integrated processes based on these other materials, however, do not provide the wealth of electronic device types that can be cofabricated on silicon processes.

Silicon processes have another advantage: availability. High-quality Hall-effect transducers can be fabricated with many standard bipolar and CMOS integrated circuit processes with little or no modification. A number of semiconductor companies presently produce a vast array of Hall-effect integrated circuits.

Figure 2-10 shows an example of a silicon Hall-effect IC, containing a Hall-effect transducer and a number of other components such as transistors and resistors. The Hall-effect transducer is the square-shaped object in the center. The size of this IC is roughly 1.5 mm × 2 mm.

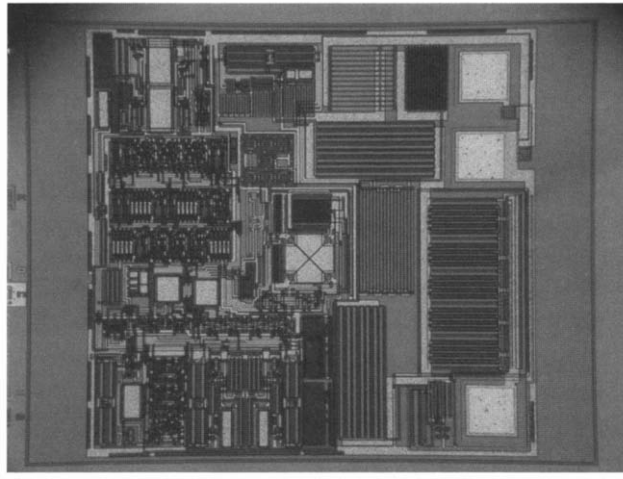

Figure 2-10: Silicon Hall-effect sensor IC with supporting electronics. *(Courtesy of Melexis USA.)*

2.5 Transducer Geometry

To this point, we have largely ignored the role of geometry in the construction of a Hall-effect transducer. The specific geometry used which device fabrication, however, can have a large impact on its performance and consequent suitability as a component.

The main factors that can be optimized by transducer geometry are sensitivity, offset, and power consumption. Let us examine the rectangular slab form as a starting point for improvements.

In the rectangular transducer form (Figure 2-11a), a uniform current sheet is established by bias electrodes that run the width of the device. Since the sensitivity is proportional to the total current passing between the sense electrodes, it would at first glance seem that by either making the sensor wider or shorter, more bias current could be driven through the device for a given bias voltage. More bias current does flow in these cases, but the wide bias electrodes form a low-resistance path to short-circuit the Hall voltage. For similar reasons, chaining multiple Hall transducers so that the bias terminals are connected in parallel and the output terminals are in series does not significantly increase the output sensitivity. For a rectangular transducer, maximum sensitivity for a given amount of power dissipation is achieved when the ratio of length to width is about 1.35 [Baltes94].

One method of avoiding end-terminal shorting is to use a cross pattern (Figure 2-11b). Because the input resistance rises rapidly with the lengthening of the cross, this geometry is not a particularly good one to use when trying to optimize sensitivity.

Another method of reducing end-terminal shorting is through the use of a diamond-shaped transducer (Figure 2-11c). In this device, all the terminals are essentially points, and the current spreads though the device in a nonuniform manner. Although the diamond shape is not optimal from a sensitivity standpoint, it offers other advantages; one of the major advantages is that the sense terminals out at the edges of of the current bias the transducer. In this respect the diamond shape works well; because the current flow at the sense corners of the diamond is low, the voltage gradient in the corners will also be low. This tends to reduce ohmic offset from contact misalignment effects.

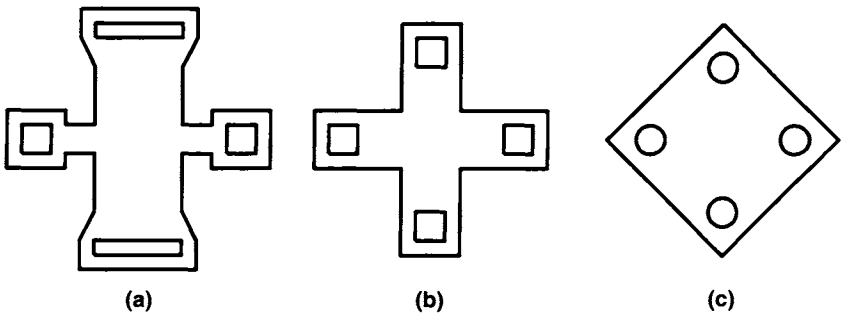

Figure 2-11: Common Hall transducer shapes: rectangle (a), cross (b), diamond (c),

2.6 The Quad Cell

In integrated Hall-effect transducers, where features can be defined with very high (submicron) resolutions, geometric flaws can be a minor source of output offset voltage. Three additional and significant sources of offset are:

- Process variation over the device
- Temperature gradients across the device in operation
- Mechanical stress imposed by packaging.

Process variations such as the amount and depth of doping can vary slightly over the surface of a wafer, leading to very slight nonuniformities between individual devices. In the case of some components, such as resistors, this effect is most readily seen as a degree of mismatch between two proximate and identical devices. In a device such as a Hall-effect transducer, this effect manifests itself as offset voltage errors. If the transducer is thought of as a balanced resistive bridge, as shown in Figure 2-12, inconsistencies appear as ΔR in one or more of the legs.

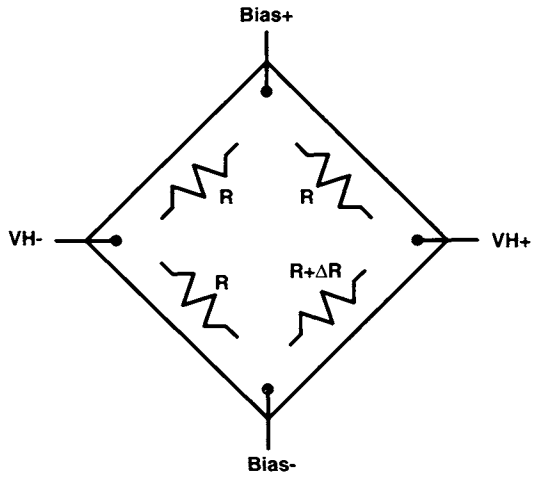

Figure 2-12: Transducer offset errors modeled as imbalanced resistive bridge.

When an integrated circuit is operating, the power dissipated in the device causes heating of the silicon die. Because most circuits dissipate more power in some parts than in others, the heating is not uniform. The resultant temperature differences can cause identical devices to behave differently, depending on where they are situated and their actual operating temperature. In some cases, in addition to being sensitive to their absolute temperature, a device may exhibit different behavior in response to temperature gradients appearing across it. While it may be difficult to believe that temperature gradients across a microscopic structure can be significant, consider that a matched

pair of devices with temperature coefficients of resistance on the order of 0.3%/°C only need differ in temperature by about 1/3°C to create a 0.1% mismatch.

Finally, silicon is a highly piezoresistive material, meaning its resistance changes when you mechanically deform it. While this effect is useful when making strain gauges, it is a nuisance when making magnetic sensors. Mechanical stresses in an IC come from a number of sources, but primarily result from the packaging. The silicon die, the metal leadframe, and the plastic housing all have slightly different thermal coefficients of expansion. As the temperature of the packaged IC is varied, this can result in enormous compressive and shear stresses being applied to the surface of the IC chip. In extreme cases this can actually result in damaging the IC chip, even to the extent of fracturing it. Additionally, the processes used for molding "plastic" packages around ICs tend to leave considerable residual stresses in the package after the overmolding material cools and sets.

The technique of "Quadding" [Bate79] offers substantial immunity to offset effects from the above three sources of offset. While these effects behave in very complicated ways, if one assumes that they behave either uniformly or linearly over very small regions of an IC, such as the transducer, one can use the offsets induced in one device to cancel out those induced in an adjacent device.

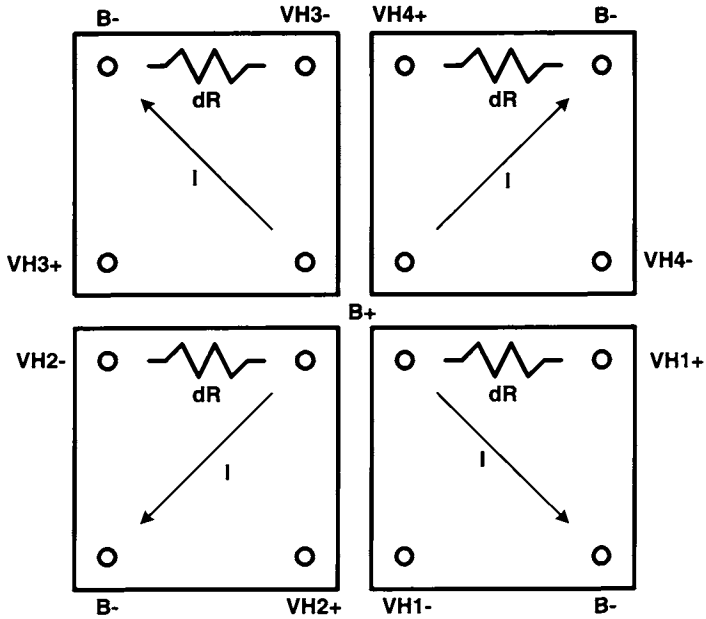

Figure 2-13: "Quad" transducer layout causes identical offsets to cancel each other out.

Figure 2-13 shows a Hall-effect transducer using a quadded layout. If one assumes that the effect causing the offset will create the offset equally in the four separate transducers, then the ΔR will occur in the same physical leg of each device, and will result in a ΔV in addition to the Hall voltage from that device. The individual voltages seen at the outputs of the individual devices will be:

$$V_1 = V_H + \Delta V$$
$$V_2 = V_H - \Delta V$$
$$V_3 = V_H + \Delta V$$
$$V_4 = V_H - \Delta V \qquad \textbf{(Equation 2-3)}$$

The transducers are then wired so that their signals are averaged. This results in an output signal of just V_H, with no offset error, at least in theory. In practice you still will get some offset voltage with a quadded transducer, but it will be an order of magnitude smaller than that obtained from a single device. Figure 2-14 shows how the devices can be wired in parallel. Similar wiring schemes have often been used because none of the wires cross, meaning that the transducer can be readily implemented in IC processes that only provide a single layer of metal for component interconnection.

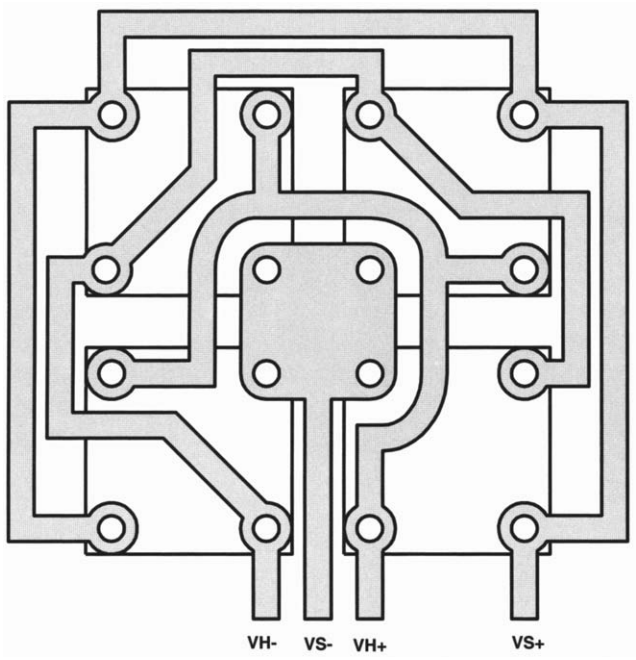

Figure 2-14: Parallel wiring structure for quadded Hall transducer.

2.7 Variations on the Basic Hall-Effect Transducer

Although most commercial Hall-effect devices employ the types of transducers previously described in this chapter, several variations on the basic technology have been developed that offer additional performance and capabilities. The two most significant of these technologies are the vertical Hall transducer and the incorporation of integrated flux concentrators.

One of the fundamental limitations of traditional Hall-effect transducers is that they provide sensitivity in only one axis—the one perpendicular to the surface of the IC on which they are fabricated. This means that to sense field components in more than one axis, one needs to use more than one sensor IC, and those sensor ICs must be individually mounted and aligned. For example, in order to realize a three-axis magnetic sensor with traditional Hall-effect transducers, three separate devices must be used, and the designer must try to align them along the desired sensing axis, all while trying to maintain close physical proximity. While this is not impossible, it can be difficult and expensive to implement such a sensor, especially if the transducers need to be physically close together.

The vertical Hall-effect transducer [Baltes94] is one means of providing multi-axis sensing capability on a single silicon die. Figure 2-15 shows the basic structure of this device.

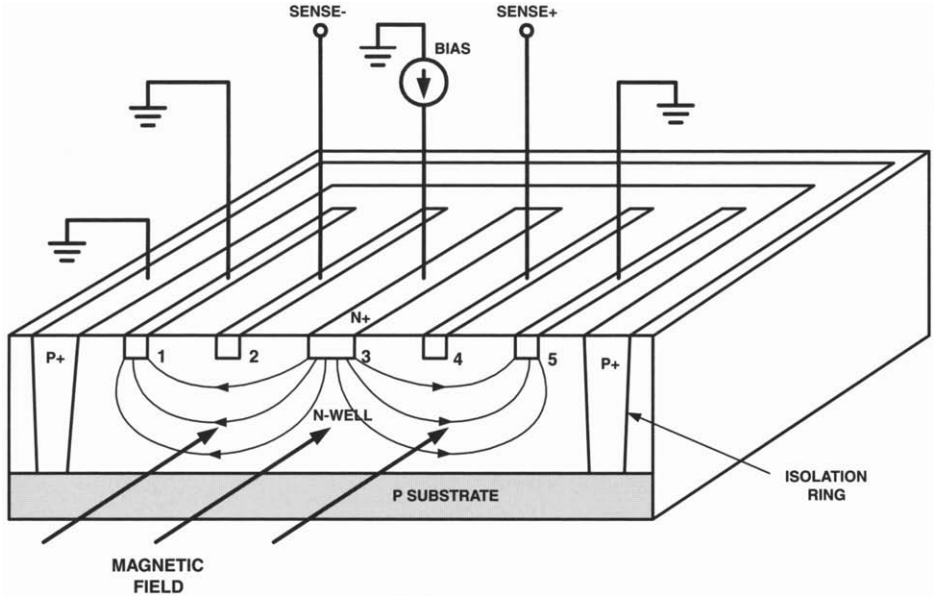

Figure 2-15: Vertical Hall-effect transducer (after Baltes et al.).

In the vertical Hall-effect transducer, bias current is injected into an N-well from a central terminal 3, and is symmetrically collected by ground terminals 1 and 5. The current path goes down from the central terminal, and arches across the IC and back up to the ground terminals. In the absence of an applied magnetic field, this current distribution results in equal potentials being developed at sense terminals 2 and 4.

When a magnetic field is applied across the face of the chip perpendicular to the current paths, Lorentz forces cause a slight shift in the current paths, as they do in a traditional Hall-effect transducer. This in turn causes a voltage differential to be developed across the sense terminals, which can then be amplified and subsequently processed into a usable signal level.

Because the vertical Hall-effect transducer, like its more traditional cousin, is sensitive to field in a single axis, it is possible to fabricate a two-axis sensor by placing a pair of these devices on a single silicon die by aligning their structures at 90° rotation to each other. Finally, one can also add a conventional Hall-effect transducer to the same die to obtain a third axis of sensitivity. In this way, it becomes possible to create a three-axis magnetic transducer on a single silicon die.

One disadvantage of the vertical Hall structure is that it lacks four-way symmetry. As will be seen in the next chapter, transducer symmetry can be exploited at the system level to reduce the effects of ohmic offset voltage errors.

Another structure that offers significant advantages is the Hall-effect transducer with *integrated magnetic flux concentrators* (IMCs) [Popovic01]. A magnetic flux concentrator is a piece of ferrous material, such as steel, that is used to direct or intensify magnetic flux towards a sensing element. External flux concentrators have long been used externally to direct and concentrate magnetic flux in Hall-effect applications. The novel aspect of the IMC is in fabricating the flux concentrator on the surface of the silicon die in extremely close proximity to the Hall-effect transducer, as shown in Figure 2-16.

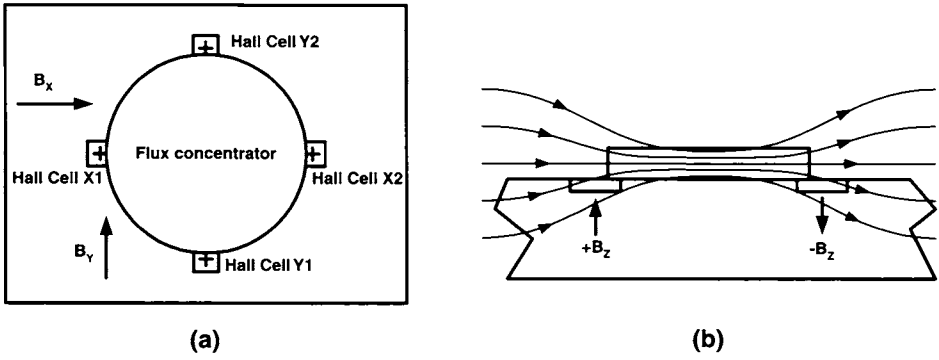

Figure 2-16: Integrated magnetic flux concentrator, top view (a) and side view (b).

The flux concentrator shown in Figure 2-16 would normally be implemented as a thin layer of a high-permeability magnetic alloy such as permalloy (a nickel-iron steel), which would be laid down on the IC surface with an evaporation or sputtering process. In the configuration shown, there are four Hall-effect transducers arranged around the periphery of the flux concentrator. The concentrator performs two functions. The first is to concentrate the field in its proximity (Figure 2-16b). This intensifies the field seen by the transducers and has the effect of increasing the transducers' effective sensitivity. The second function performed by the concentrator is to redirect the axis of the applied field from horizontal to vertical near the transducers. For example, a horizontally applied X field is mapped into a positive Z component at transducer X1 and a negative component at transducer X2. Note, however, that the transducers will still be sensitive to fields applied in the Z-axis despite the presence of the flux concentrator. By subtracting the outputs of the transducers (X2–X1, Y2–Y1), the effects of any Z-field components can be ignored. A microphotograph of an IMC Hall-effect transducer can be seen in Figure 2-17.

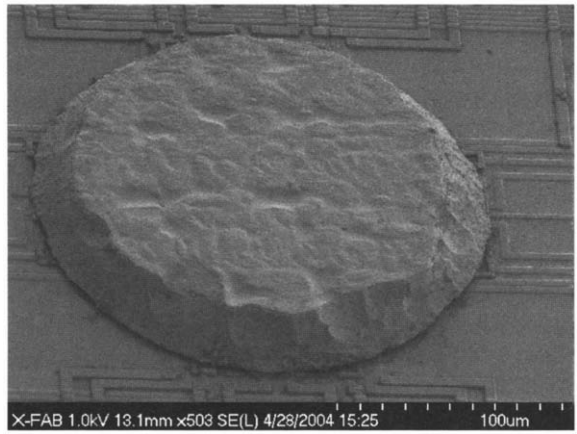

Figure 2-17: Microphotograph of IMC Hall-effect transducer. *(Courtesy Melexis USA.)*

Commercially available products utilizing IMC Hall-effect transducers have been developed by Sentron AG. Two typical devices are the CSA-1V-SO and the 2SA-10. The CSA-1V-SO is a single-axis device in an SOIC-8 package, while the 2SA-10 is a two-axis device. Both of these devices incorporate on-chip amplifier circuitry in addition to the transducer elements. The CSA-1V-SO provides a very high level of sensitivity, typically 30-mV output per gauss of applied field, and can sense fields over a range of approximately ±75 mV. Because of the device's high sensitivity and a sensing axis parallel to the SOIC package face, this device has potential for replacing magneto-resistive sensors in many applications. The 2SA-10 also is provided in an SOIC-8 package, and provides somewhat lower sensitivity (5-mV output per gauss of applied field), but

also offers two sensing axes, both parallel to the SOIC face. The primary application for this device is in sensing rotary position, where one simultaneously measures field strength in two axes, and resolves the two measurements into degrees of rotation.

2.8 Examples of Hall Effect Transducers

Table 2-4 lists a few examples of commercially available Hall-effect transducers. Keep in mind that these devices are intended for a variety of applications, so sensitivity alone should not be used to determine a particular transducer's suitability for a particular use.

Table 2-4: Examples of commercial Hall-effect transducers

Manufacturer	Device	Sensitivity	Material
F.W. Bell	HS-100	8μV/G @ 10 mA	Thin-Film Indium Arsenide
	BH-200	15μV/G @ 150 mA	Bulk Indium-Arsenide
Asahi-Kasei	HG-106C	100μV/G @ 6 mA	Gallium Arsenide
Sprague Electric[1]	UGN-3604	60μV/G @ 3 mA	Silicon (monolithic)

Note 1: This product was discontinued a long time ago, and is only mentioned here to provide an example of a silicon Hall-effect transducer's "typical" sensitivity..