Chapter 3

Transducer Interfacing

While it is possible to use a Hall-effect transducer as a magnetic measuring instrument with merely the addition of a stable power supply and a sensitive voltmeter, this is not a typical mode of application. More frequently the transducer is used in conjunction with electronics specially designed to properly bias it and perform some preprocessing of the resultant signals before presenting them to the end-user. The addition of application-specific electronics provides significant value by allowing the end-user to view the system as a black-box, without having to concern himself with the details of how the transducer is implemented. To differentiate a bare transducer from a transducer with support electronics, we will be referring to the latter as a sensor.

A minimal Hall-effect sensor (Figure 3-1) consists of three parts: a means of powering or biasing the transducer, the transducer itself, and an amplification stage. Because of the variety of applications in which Hall-effect sensors are employed, and their equally diverse functional requirements, there is no single "best way" to build even a minimal transducer interface. The "goodness" of any implementation is a function of how well it meets the requirements of a particular application. These requirements can include sensing accuracy, cost, packaging, power consumption, response time, and environmental compatibility. A $4,000 laboratory gaussmeter would not be a good (or even adequate) solution under the hood of a car, nor would a 20-cent commodity sensor IC be an especially good choice for many laboratory applications; each has its own application domain for which it is best suited.

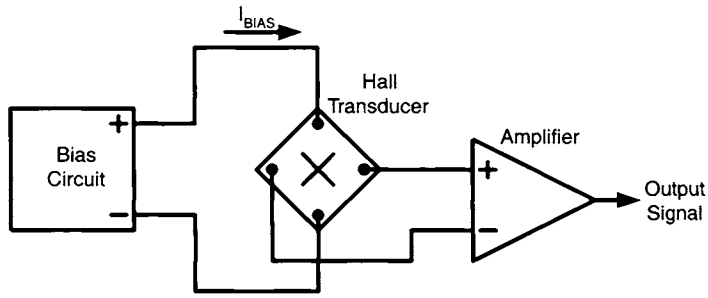

Figure 3-1: Minimal components of Hall-effect sensor system.

3.1 An Electrical Transducer Model

To design good interface circuitry for a transducer requires that one understand how the transducer behaves. While the first two chapters described the physics and construction of a number of Hall-effect transducers, there still remains the question of how it behaves as a circuit element. Carrier concentration, current density, and geometry describe the device from a physical standpoint, but what is needed is a model that describes how the device interacts with transistors, resistors, op-amps, and other components dear to the hearts of analog designers.

When confronted with an exotic component, such as a transducer, a good circuit designer will attempt to build a model to approximately describe that device's behavior, as seen by the circuits it will be connected to. For this reason, the model will usually be built from primitive electronic elements, and be represented in a highly symbolic (schematic) manner. The elements employed can include resistors, capacitors, inductors, voltage sources and current sources. There are several advantages inherent in this approach:

1) Circuit designers think in terms of electronic components and a good circuit-level model can allow a designer to understand the system. A great model can give a circuit designer the gut-level intuitive understanding of the system needed to produce first-rate work. Alternatively, a poor model can give a circuit designer gut-level feelings best resolved with antacids.
2) Simple circuit-level models often are analytically tractable. Deriving a set of closed-form analytic relationships can allow one to deliberately design to meet a set of goals and constraints, as opposed to designing through an iterative, generate-and-test procedure.

3) Circuits can be automatically analyzed on a computer, by a number of commercially available circuit simulation programs (e.g., SPICE). In the hands of a skilled designer, the use of these tools can result in robust and effective designs. Conversely, in the hands of unskilled designers, their use can result in mediocre designs reached by trial-and-error (also known as the *design by brute-force and ignorance* method).

Figure 3-2 shows the model that was initially presented in the last chapter. It consists of four resistors and two controlled voltage sources. This model describes the transducer's input and output resistances, as well as its sensitivity as a function of bias voltage.

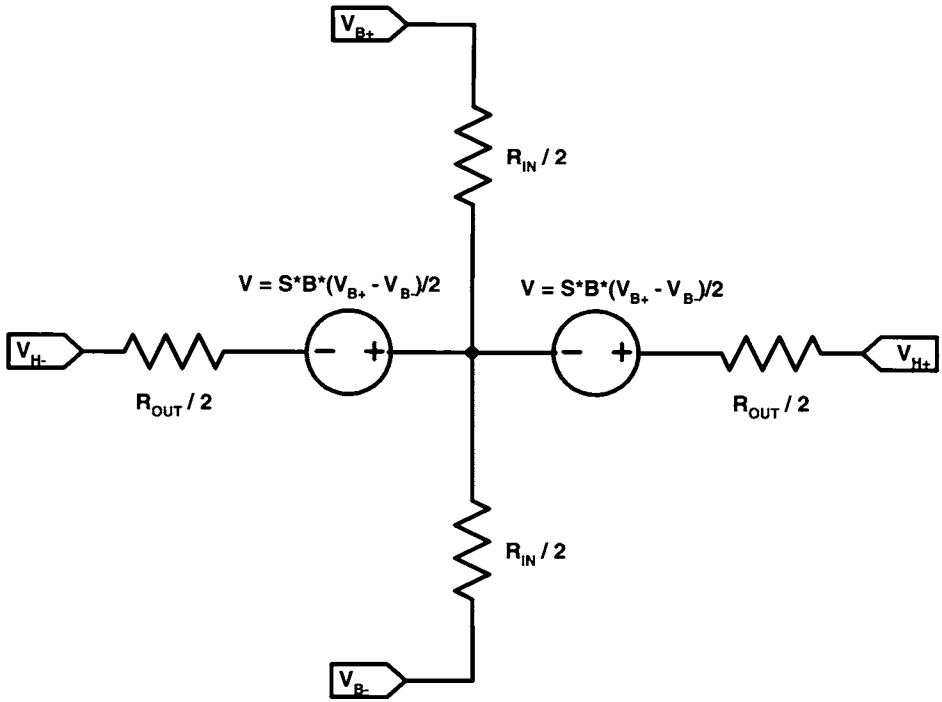

Figure 3-2: Hall-effect transducer simple electrical model.

The four resistors describe the input and output resistances of the transducer. In the case of a transducer with four-way symmetry, all of the resistors are equal. The voltage sources model the transducer's sensitivity or the gain, which is a linear function of the bias voltage and the applied magnetic field, The various variables and constants in this model are defined as follows:

V_{B+}, V_{B-}	Bias voltage
S	Sensitivity in $Vo/B * Vi$
B	Magnetic flux density
R_{IN}	Input resistance
R_{OUT}	Output resistance

Although this model is a gross simplification, it will exhibit enough of the electrical attributes of a transducer to be useful as an aid to designing interface circuits. The following are some of the major assumptions and limitations:

- Magnetic linearity; there are no saturation effects at high field.
- Temperature coefficients are ignored.
- There is no zero-flux offset.
- The resistance as measured between adjacent terminals is unimportant for many applications; modeling this correctly would unnecessarily complicate the model.
- A real Hall-effect sensor is a passive device; this model contains power-producing elements. We assume this additional power is small enough to ignore.
- The transducer is symmetric; the sense terminals are placed at the halfway point along the device.

3.2 A Model for Computer Simulation

The model presented in the last section can be adjusted so that it is suitable for simulation by SPICE (simulation program with integrated circuit emphasis) or another circuit simulation program. A few additional details need to be added both to make it more specific and to make it fit into SPICE's view of the world. Since SPICE doesn't directly handle magnetic field quantities, magnetic flux is represented by a voltage input to the model. SPICE also requires the user to define circuit topology by numbering each electrical node in the circuit. If you are using a graphical schematic-capture program to input your circuits, the computer numbers the nodes automatically. This can be a major convenience, especially when simulating large circuits. Figure 3-3 shows the SPICE-compatible circuit, with electrical nodes numbered.

The major adjustments to the model are to provide user control of an applied magnetic field. This is what node 5 and resistor RB are for. When a connected circuit presents a voltage to node 5, that voltage is interpreted as gauss input to the sensor. The resistor to ground is merely to guarantee that the node has a path to ground. This is done for reasons of numerical stability; it doesn't have any function in the circuit other than to make the circuit easier for SPICE to simulate.

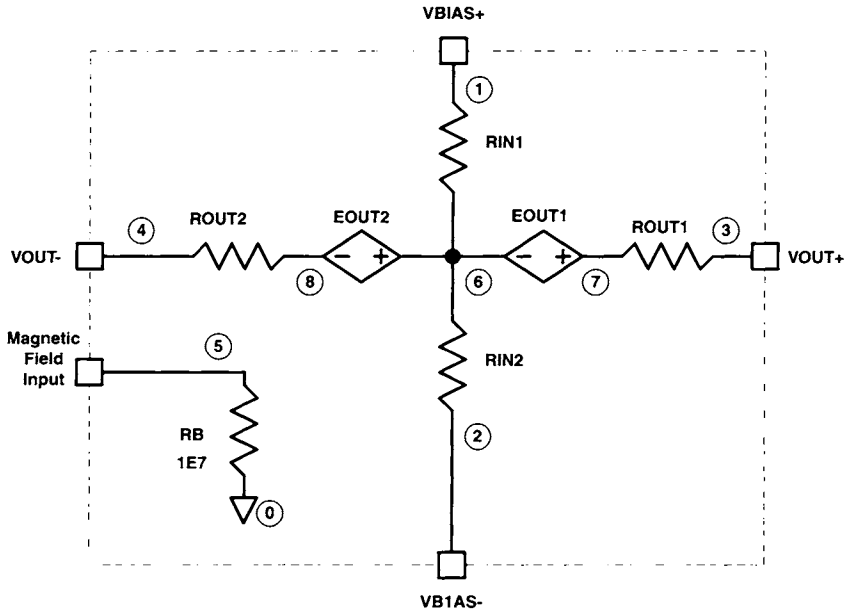

Figure 3-3: Electrical model adapted for SPICE.

This schematic can now be translated into the SPICE language, and packaged as a subcircuit. Because of the number of commercial varieties of SPICE that have evolved over the past few years, we will be using a minimal set of features, so as to provide a least-common-denominator model. In keeping with this philosophy, the controlled sources (EOUT1 and EOUT2) are modeled as multidimensional polynomial functions of V5 and V1–V2. Some versions of SPICE will simply let you specify the source's gain algebraically (e.g., V(5) * (V(1)–V(2))) but this feature is not uniformly supported.

The subcircuit's user I/O ports are:

Nodes 1, 2: bias connections (+ and –)
Nodes 3,4: output connections (+ and –)
Node 5: magnetic field input (1 gauss/Volt)

To finish this example and make this a complete model, we will use some of the parameters of the F.W. Bell BH-200 transducer:

- Sensitivity = 40 μVo/G–V_{in}
- R_{in} = 2.5Ω
- R_{out} = 2Ω

The resultant SPICE code is shown in Listing 3-1:

Listing 3-1: Simple SPICE model for BH200 Hall-effect transducer.

```
* EXAMPLE OF SIMPLE HALL-EFFECT TRANSDUCER MODEL FOR SPICE
*
.SUBCKT       HALL1 (1 2 3 4 5)
* HALL EFFECT TRANSDUCER SUBCIRCUIT
* EACH RIN LEG HAS HALF OF 2.5 OHM INPUT RESISTANCE
RIN1   1 6 1.25
RIN2   2 6 1.25
* EACH ROUT LEG HAS HALF OF 2 OHM OUTPUT RESISTANCE
ROUT1  7 3 1.00
ROUT2  8 4 1.00
* EACH SOURCE PROVIDES V5*(V1-V2)*GAIN/2
EOUT1  7 6 POLY(2) 5 0 1 2 0.0 0.0 0.0 0.0 20E-6
EOUT2  6 8 POLY(2) 5 0 1 2 0.0 0.0 0.0 0.0 20E-6
* LOAD FOR MAGNETIC INPUT (AS VOLTAGE) - KEEPS SPICE HAPPY
RB     5 0 1E7
.ENDS HALL1

**** TEST CIRCUIT ****
BIAS WITH 5V
VBIAS 1 0 5
* PROVIDE 1 MEG LOADS FROM OUTPUTS TO GND RL1 2 0 1E6 RL2 3 0 1E6
* DEFINE VMAG AS MAGNETIC FIELD INPUT
VMAG 4 0 0
* CALL HALL TRANSDUCER SUBCIRCUIT
X1 1 0 2 3 4 HALL1
* SWEEP MAGNETIC FIELD FROM -1000 TO +1000 GAUSS IN 20 G STEPS
* AND OUTPUT RESULTS
.DC VMAG -1000 1000 20
.PRINT DC V(4), V(2), V(3)
.PLOT DC V(4), V(2), V(3)
.END
```

This SPICE model provides the following features:

- Input and output resistance
- A control for applied flux, via pin 5
- Output voltage, both as a function of bias voltage and applied field

To make for a simple illustration, we deliberately left a number of relatively useful features out of this model. Temperature coefficients of resistance and sensitivity,

for example, are not modeled in the above SPICE input file. SPICE is quite capable of simulating temperature-dependent behavior, provided one goes to the trouble to build an appropriate model. For many, if not most, purposes, however, the level of detail presented in this model will be sufficient for evaluating most of the circuits presented in this chapter. As with any computer model, your actual mileage may vary, depending on how you use (or abuse) it.

3.3 Voltage-Mode Biasing

One of the major dichotomies in the design of a Hall-effect sensor is the mode in which the transducer is biased. It can be driven by either a constant voltage source or a constant current source; both modes have their advantages and their disadvantages. We will first look at circuitry for biasing a transducer with a constant-voltage source.

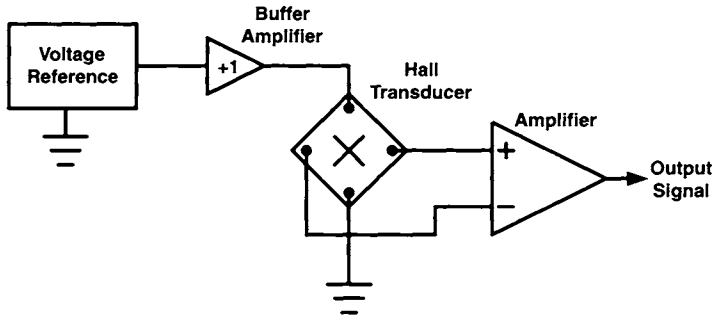

Figure 3-4: Voltage-mode Hall-effect sensor.

Figure 3-4 shows the basic arrangement of a voltage-biased Hall-effect sensor. There is a voltage reference, a buffer, the transducer, and an amplifier. One of the key features of this architecture is that, for most applications, the temperature coefficient of the transducer sensitivity will be sufficiently high that it must be compensated for. This can be done in one of two ways. The first is to make the voltage source temperature dependent so as to obtain a constant output level from the Hall-effect transducer. The second method is to make the gain of the amplifier temperature dependent, so it can compensate for the temperature-varying gain of the transducer signal. Although either method can be made to work, we will examine the case where the drive voltage is held constant over temperature.

A simple but workable bias circuit is shown in Figure 3-5a. A voltage reference, in this case a REF-02 type device, drives an op-amp follower to provide a stable voltage (+5V) to bias the Hall-effect transducer. When constructed from commonly available op-amps, such as the LM324 or TL081, this circuit can provide a few milliamperes of output drive, making it suitable for use with high input resistance transducers (R_{in} > 1 kΩ).

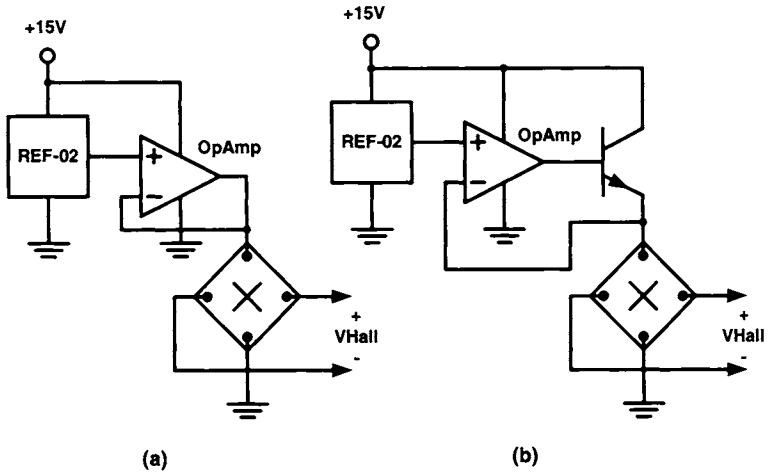

Figure 3-5: Voltage bias circuits for low current (a) and high current (b) transducers.

Bulk and thin-film transducers, however, can often require as much as 100–200 mA for optimal performance. To bias these devices, the driver circuit of Figure 3-5b can be used. The addition of the transistor to the output of the op-amp increases its effective output current capability. When using this circuit, there are a few issues to keep in mind. First is whether or not the transistor has sufficient current gain (referred to as beta or β). The maximum output current able to be drawn from the emitter of the transistor is limited to the maximum output current of the op-amp multiplied by the transistor's beta.

Another potential problem associated with this circuit is that of power dissipation in the transistor. For example, if the transducer draws 100 mA with only 0.2V of bias voltage, it only dissipates 20 mW. The drive transistor, however, if the collector is connected to a 5V supply, will dissipate nearly 500 mW of power. The maximum power dissipated in the transistor must be anticipated in the design, and should be a factor in selecting the transistor, as well as in determining what kind of additional heat-sinking is required, if any.

Finally, in either of the circuits of Figure 3-5, stability can become an issue, especially if the transducer is operated at the end of a length of cable. The addition of parasitic capacitance, or in some cases the additional transistor of Figure 3-5b, can cause the bias circuit to break out into oscillation. Because the stability of a given circuit is dependent on many variables, there is no simple one-size-fits-all fix. The circuit of Figure 3-6 shows one approach that is often useful when driving loads at the end of long cables. This circuit works by providing separate feedback paths from the cable load and the output of the op-amp. The exact values required for the components (R_F, C_F, R_O) surrounding the op-amp will depend on the details of the application and the opamp chosen. For a general-purpose op-amp such as the TL081, setting R_F to 100 kΩ, C_F to 100 pF, and R_O to 100Ω is a good starting point for experimentation in many cases.

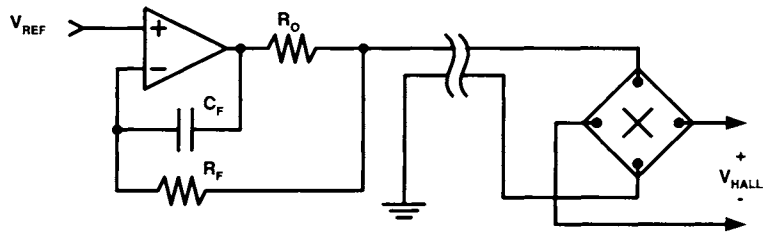

Figure 3-6: Circuit for driving capacitive loads.

All of the above bias circuits result in a small differential Hall output voltage riding on a fairly large common-mode voltage; specifically half the bias voltage. The common-mode signal is the average of the two output voltages, while the differential is the difference. In the case of a Hall-effect transducer, the differential signal is the one carrying the measurement information. While it is possible to measure a small differential signal riding on a large DC common-mode signal, signal recovery is easier if one doesn't have to deal with a large common-mode signal. The circuit of Figure 3-7 solves this problem by symmetrically biasing the transducer. If the transducer's sense terminals are halfway between the bias terminals, providing bias at +V and –V will result in zero common-mode output voltage. The Hall output voltage will in this case swing symmetrically about zero volts, for the case of ideally matched components. In reality this scheme will not completely eliminate common mode voltage from the transducer, but will reduce it to very low levels.

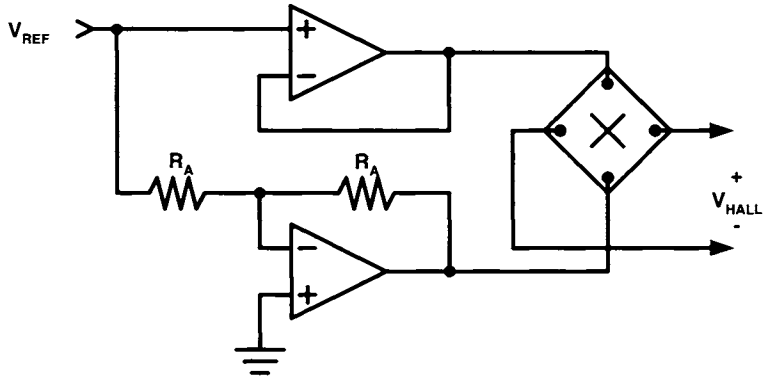

Figure 3-7: Symmetric bias circuit.

One problem frequently encountered when driving a Hall-effect transducer in constant-voltage mode is the voltage drops along long wires. This problem becomes especially acute when the load requires a significant amount of current. While one solution

is to simply use thicker wires, this is not always either feasible or desirable. Another option is the use of a force-sense bias circuit. In a force-sense type of bias circuit, four wires are used to provide the bias voltage to the transducer. Two of the wires are used to provide positive supply and return (the force leads), while the remaining two (the sense leads) are used to measure the voltage that is actually being provided to the transducer. Because there is an insignificant amount of current flowing down the sense leads, there is no significant voltage drop along them, and they can be used to accurately measure the transducer bias voltage. Figure 3-8 shows a force-sense bias circuit using a differential amplifier (Gain = 1) to measure the voltage across the transducer. This circuit will impress V_{REF} across the transducer bias terminals even if significant voltage drops (~1V) occur along the force leads.

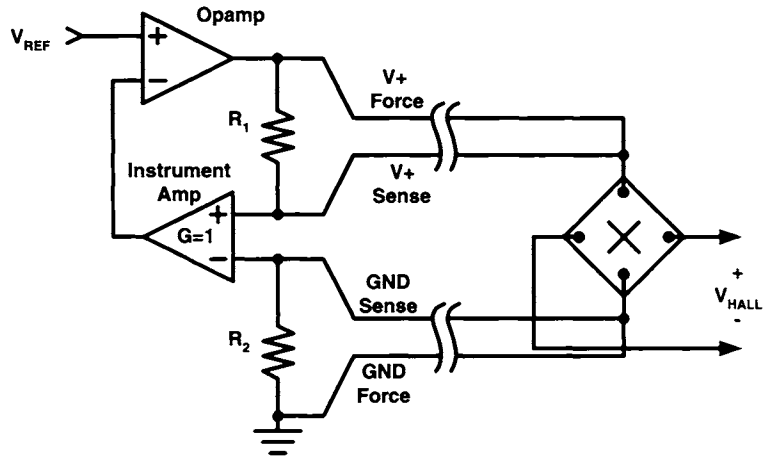

Figure 3-8: Force-sense bias circuit.

Resistors R_1 and R_2 are in this circuit to handle the condition where one of the sense leads is accidentally disconnected. If this situation should occur, the differential amplifier will still measure the voltage applied to the force lead. This prevents the op-amp from overdriving and possibly damaging the transducer in the event of a broken sense connection.

It is also possible to construct a force-sense bias circuit with a single opamp, as shown in Figure 3-9. Good performance in this circuit, however, is highly dependent on the degree to which the values of all the R_A resistors match each other.

Because force-sense techniques are normally employed when the transducer is some distance from the bias supply, stability again becomes an issue. The circuits of both Figures 3-8 and 3-9 would most likely require some modification in order to be successfully used in practice with commonly available op-amps and differential amplifiers.

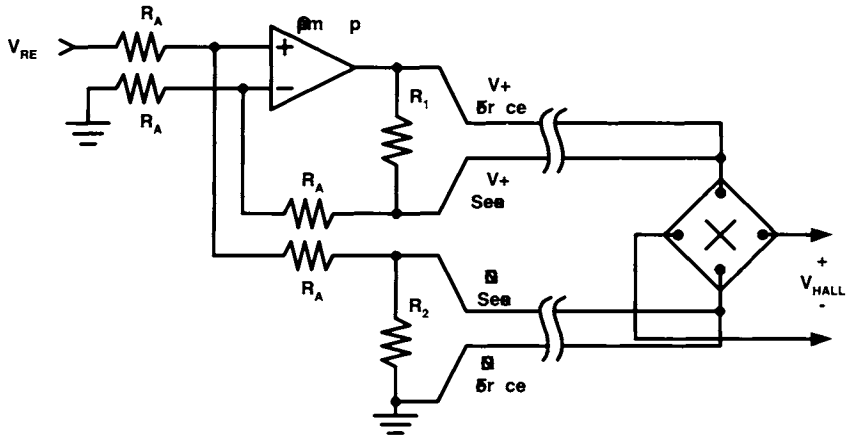

Figure 3-9: Force-sense circuit implemented with single op-amp.

3.4 Current-Mode Biasing

Another way to bias a Hall-effect transducer is to feed it with a constant current; this mode of operation results in a Hall output voltage with a temperature coefficient on the order of 0.05%/°C, as opposed to the 0.3%/°C obtained with constant-voltage biasing. For many applications, the tempco obtained with constant-current biasing is sufficiently low that no additional correction is necessary. An additional advantage is obtained when using long cable runs; because current does not "leak" out of wires to any appreciable degree under most circumstances, current-mode biasing doesn't normally require any kind of force-sense arrangement to be used in the bias supply.

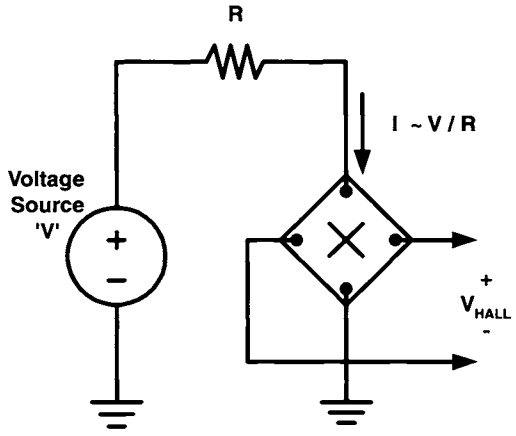

Figure 3-10: Brute-force constant-current bias circuit.

There are a number of ways to construct constant-current bias sources for a Hall-effect transducer. The simplest method is to use a high-value resistor (R) in series with a constant voltage source, as shown in Figure 3-10. While such an arrangement is easy to make and inexpensive, maintaining a stable bias current requires that the voltage source be much greater than the transducer bias voltage. While this arrangement can be useful with bulk-type transducers that often operate with a bias voltage of under a volt, it can require excessively large voltage sources when used with integrated devices that may require several volts of bias.

The use of active electronics allows for the construction of stable current sources that don't require stable high voltage supplies. Figure 3-11 shows three common circuit topologies.

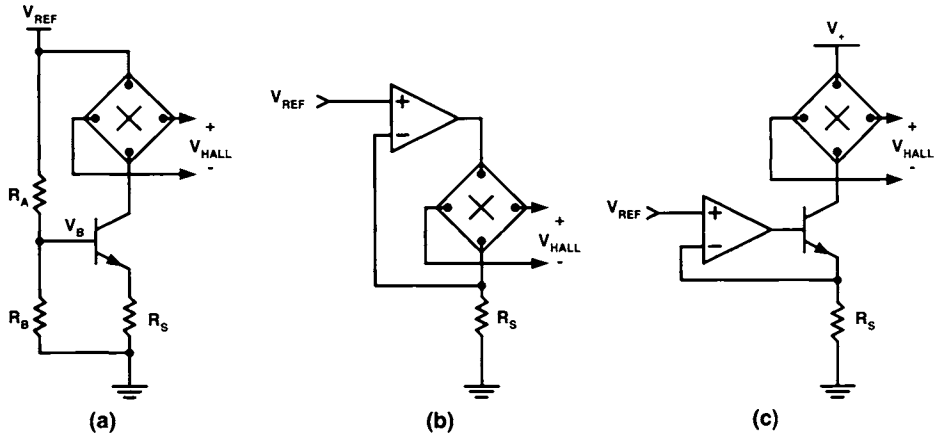

Figure 3-11: Constant current sources. Transistor (a) op-amp (b) op-amp with outboard transistor (c).

The circuit of Figure 3-11a works by setting a voltage at the base of the transistor, approximately determined by $V_B = V_{REF} \cdot R_B/(R_A + R_B)$. This results in an emitter voltage about 0.6V lower, which then sets the current through R_S. The load (transducer) in the collector doesn't significantly affect the amount of current pulled through the collector, assuming that the collector voltage is higher than the emitter voltage so that the transistor is not saturated. The collector current is approximately given by:

$$I_C \approx \frac{1}{R_S}\left(\left(\frac{V_{REF}R_B}{R_A + R_B}\right) - 0.6\right) \qquad \textbf{(Equation 3-1)}$$

This relation will hold substantially true if two conditions are met. The first is that the voltage across R_S is greater than 0.6V; this will minimize the effects of transistor V_{BE} variation (V_{BE} varies both over current and temperature, between individual transistors). The second condition is that $(R_S \cdot \beta) >> ((R_A \cdot R_B)/(R_A + R_B))$. If this condition is

violated the base will load down the R_A/R_B divider network and the output current may be significantly reduced.

The circuit in Figure 3-11b uses feedback to regulate current. By actively measuring the current passing through R_S, and consequently through the transducer, the opamp can adjust its output voltage to obtain the desired current. The current is given simply by V_{REF}/R_S, and if the op-amp has sufficient drive capabilities (current and voltage), the bias current will remain nearly constant over temperature. The output current drive capabilities of this circuit may be increased by adding a transistor to the output of the op-amp, in the manner similar to that shown previously in Figure 3-5b.

A third current source appears in Figure 3-11c. This circuit adds the active feedback control of an op-amp to the circuit of Figure 3-11a. The resultant current is approximately V_{REF}/R_S, with a small error (1–5%) resulting from base current feeding through the emitter and into the sense resistor. Adding feedback makes this circuit much less sensitive to variation in the transistor caused by both device-to-device differences and temperature effects, as compared to the circuit of Figure 3-11a.

One characteristic of all of the above circuits is that the transducer is "floating" with respect to ground, meaning that no terminal is grounded The transducer in Figures 3-11a and 3-11c is essentially "hanging" from the positive supply rail. The transducer of Figure 3-11b is floating at some indeterminate point in between ground and the positive supply rail. A circuit called a *Howland current source* can be used to supply current to a ground-referenced load. Figure 3-12 shows the Howland current source.

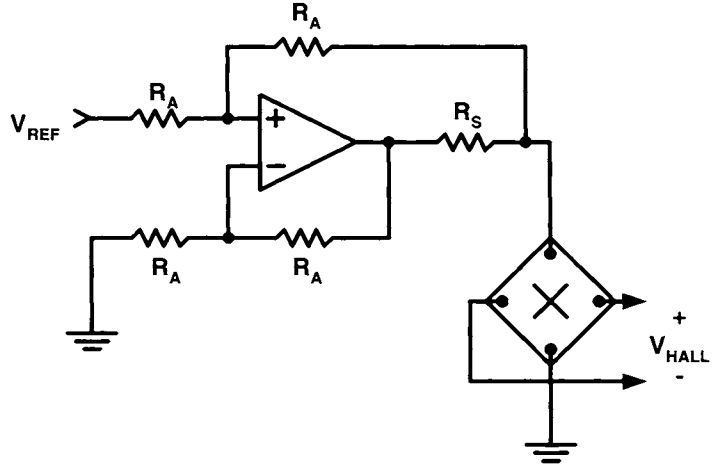

Figure 3-12: Howland current source.

To obtain good performance with a Howland current source, the R_A resistors must be well matched and significantly greater in value than the sense resistor R_S. The output current is given by V_{REF}/R_S.

3.5 Amplifiers

With the transducer properly biased, one obtains a small differential voltage signal from the output terminals, often riding on a large DC common mode signal. The job of the amplifier is to amplify this small differential signal while rejecting the large common-mode signal. The fundamental circuit to perform this task is the differential amplifier (Figure 3-13), also known as an instrumentation amplifier (or in-amp).

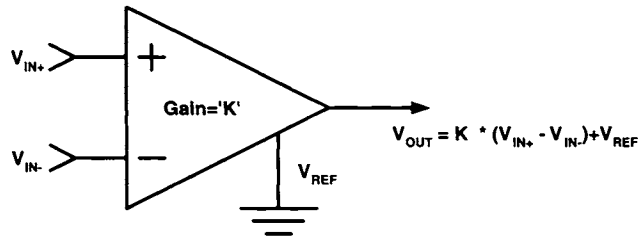

Figure 3-13: Instrumentation amplifier.

A typical differential amplifier has a positive and a negative input terminal and an output terminal. The schematic symbol unfortunately looks a lot like that for an op-amp, sometimes leading to a bit of confusion. Some differential amplifiers have an additional reference input terminal, to which the output voltage is referenced. For most applications, this terminal will be tied to ground. Ideally, the output voltage is the difference of the two input voltages. Because ideal devices are not yet available, you must make some trade-offs among various performance characteristics to get an amplifier that suits your needs. Some of the key parameters for differential amplifiers are:

- Differential Gain
- Gain Stability
- Input Offset Voltage
- Input Bias Current
- Common-Mode Rejection
- Bandwidth
- Noise

Differential gain is the gain by which the amplifier boosts the difference of the input signals. While there are monolithic instrumentation amplifiers that have fixed gains, this parameter is often user adjustable within wide limits, with ranges of 1000:1 commonly available.

Gain stability. One uses an instrumentation amp to get an accurate gain, and this is one of the features that differentiates them from the more common op-amp, which has a very large (>50,000) but not very well-controlled gain. Key gain-stability issues center around initial accuracy (% gain error) and stability over temperature (% drift/°C).

Input Offset Voltage. This is a small error voltage that is added to the differential input signal by the instrumentation amp. It results from manufacturing variations in the internal construction of the amplifier. The offset voltage is multiplied by the gain along with the signal of interest and can be a significant source of measurement error.

Input Bias Current. The inputs of the instrumentation amp will draw a small amount of input current. The amount is highly dependent on the technology used to implement the amplifier. Devices using bipolar transistors in their input stages tend to draw input currents in the range of nanoamperes, while those based on field-effect transistors (FETs) will tend to draw input bias currents in the picoampere or even femtoampere (10^{-15}) range. While FET-input instrumentation amps have lower bias currents than their bipolar counterparts, the input offset voltages are usually higher, meaning that a trade-off decision must be made to determine which technology to use for a given application.

Common-Mode Rejection. While the purpose of a differential amplifier is to amplify just the difference between the input signals, it also passes through some of the common-mode, or average, component of the input signal. The ability of a given amplifier to ignore the average of the two input signals is called the *common mode rejection ratio*, or CMRR. It is defined as the ratio between the differential gain (A_{Vd}) and the common-mode gain (A_{Vc}) and, like many other things electrical, is often expressed logarithmically in decibels:

$$CMRR = 20\log\left(\frac{A_{Vd}}{A_{Vc}}\right) \qquad \textbf{(Equation 3-2)}$$

Common-mode rejection ratios of 80–120 dB (10,000–100,000) can be easily obtained by using monolithic instrumentation amplifiers. Additionally, the CMRR for many devices increases as the gain increases.

Bandwidth. Unless you are only interested in very slowly changing signals, you will probably be concerned with the frequency response, or bandwidth, of the amplifier. This is commonly specified in terms of a gain-bandwidth product (GBP). In rough terms, gain-bandwidth product can be defined as the product of the gain and the maximum frequency at which you can achieve that gain. For many types of amplifiers, the GBP is roughly constant over a wide range of frequencies. For example, an amplifier with a 1-MHz GBP can provide 1 MHz of bandwidth at a gain of 1, or conversely only 1000 Hz of bandwidth at a gain of 1000. Figure 3-14 shows how the gain of this hypothetical 1-MHz GBP amplifier varies when set at various gains.

One caveat, however, is that an amplifier doesn't simply block signals past its frequency response; the response gracefully degrades. For precision applications, you will want to choose your bandwidth so that it is at least a factor of 5–10 greater than that of the signal you are interested in. So, for the case of an amplifier with a gain of 1000 amplifying signals with useful information up to about 1000 Hz, you might want to use an instrument amplifier with a GBP of 5 to 10 MHz to preserve signal integrity.

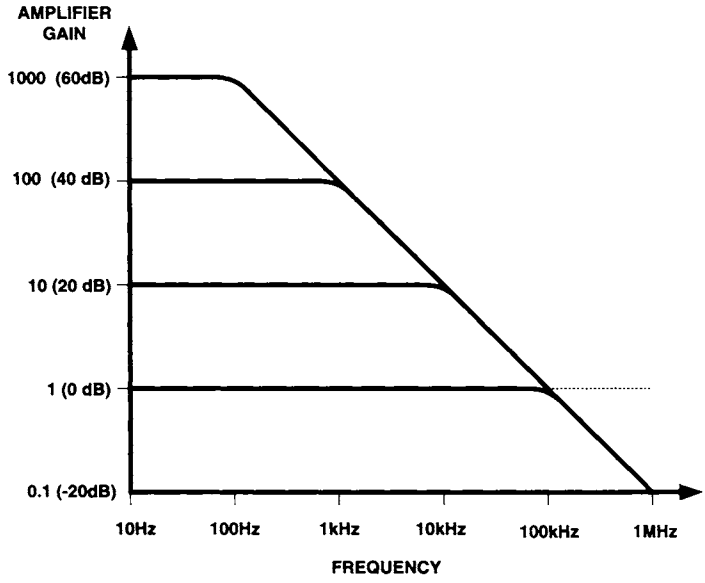

Figure 3-14: Instrumentation amplifier frequency response vs. gain.

Noise. In addition to noise from the transducer, an amplifier will add some noise of its own. Although the sources of amplifier noise are complex and beyond the scope of this text, it can be modeled as a noiseless amplifier, with both voltage and current noise sources at the input, as shown in Figure 3-15. Because the noise from the current source is converted into voltage by the source impedance, it also ultimately appears as voltage noise. For a given input impedance R_S, the total amplifier noise is given by:

$$v_{NT} = \sqrt{(v_N)^2 + (R_S i_N)^2} \qquad \textbf{(Equation 3-3)}$$

Noise is specified over a given bandwidth, and is usually given in terms of V$\sqrt{}$Hz for voltage noise and amperes/$\sqrt{}$hertz for current noise. As with the case of transducer noise, the larger the bandwidth examined, the more noise that will be seen. (See Figure 3-15.)

Different technologies provide varying trade-offs between the magnitude of the voltage and current noise sources. Bipolar input amplifiers tend to have low voltage noise and high current noise, whereas amplifiers using FET technology tend to have higher voltage noise and lower current noise. The choice of technology is complex and is dictated by both the technical requirements and the economics of an application. As a general rule of thumb, however, bipolar-input amplifiers tend to give better noise performance with low impedance transducers (<1 kΩ) while FET-input devices contribute

less noise when used with higher impedance sources. Table 3-1 lists the voltage and noise parameters of a few commonly available op-amps.

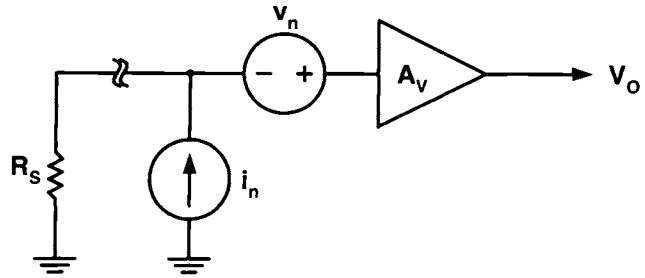

Figure 3-15: Noise model of amplifier.

Table 3-1: Typical noise performance of various operational amplifiers at 1 kHz.

Device	Technology	VN (nV/√Hz)	IN (pA/√Hz)
OP27	Bipolar	3	1
OP42	JFET	13	0.007
TLC272	CMOS	25	Not avail.

3.6 Amplifier Circuits

Although a number of techniques exist for constructing differential amplifiers, one of the simplest is to use an op-amp and a few discrete resistors as shown in Figure 3-16.

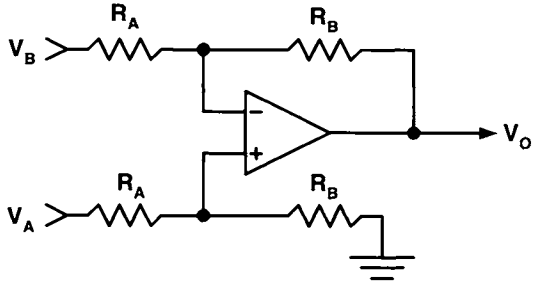

Figure 3-16: Differential amplifier.

This circuit provides an output voltage (with respect to ground) that is proportional to the difference in the input voltages. The output voltage is given by:

$$V_O = \frac{R_B}{R_A}(V_A - V_B) \qquad \textbf{(Equation 3-4)}$$

In the ideal case where the R_A resistors match, the R_B resistors match, and an "ideal" op-amp is used, the common mode gain is zero. In the more realistic case where the resistors do not match exactly, the common mode gain is a function of the mismatch; the greater the mismatch, the higher the common mode gain and the less effective the differential amplifier will be at rejecting common mode input signal. For a differential amplifier constructed with 1% precision resistors, one can expect a CMRR on the order of 40–60 dB (100–1000).

One characteristic of this differential amplifier is that its input impedance is determined by the R_A and R_B resistors. In situations where this circuit is used with a transducer with a comparable output impedance, severe gain errors can result from the amplifier loading down the transducer. One way around this problem is to buffer the inputs with unity-gain followers, as is shown in Figure 3-17a. This circuit can provide very high input impedances, especially when implemented with FET input op-amps.

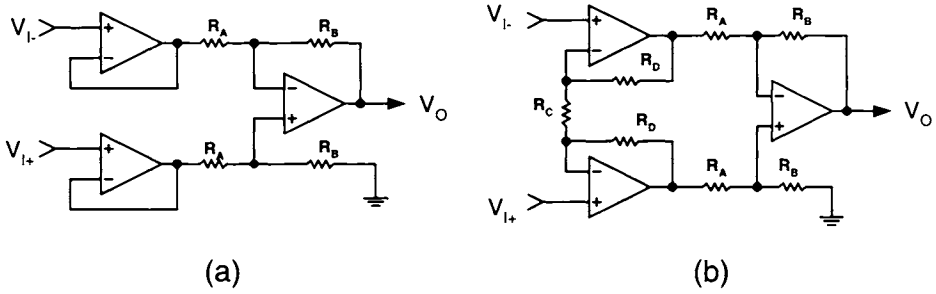

Figure 3-17: Three-op-amp differential amplifiers. Simple buffered (a) classical (b).

Figure 3-17b shows the "Classical" three-op-amp instrument amplifier. In this circuit, the input op-amps still provide high-impedance inputs, but they also provide an additional differential gain stage. The common mode gain of this first stage is unity, but the differential gain is given by:

$$A_{VD} = \frac{2R_D}{R_C} + 1 \qquad \textbf{(Equation 3-5)}$$

Note that there is only one R_C in the circuit. Making this resistance variable allows for a single-point adjustment of the amplifier's gain.

With the addition of the final stage, the differential gain of the complete instrumentation amplifier is given by:

$$A_{VD} = \frac{-R_B}{R_A}\left(\frac{2R_D}{R_C} + 1\right) \qquad \textbf{(Equation 3-6)}$$

The circuit of Figure 3-17b's use of two gain stages offers a number of significant advantages over the circuits of Figures 3-16 and 3-17a. First, it allows for the construction of a higher-gain instrument amplifier for a given range of resistor ratios. Next, by splitting the gain across two stages, it offers higher frequency response for a given gain. Finally, because of the differential gain provided in the first stage, it becomes possible to build amplifiers with much higher levels of common-mode rejection, especially at higher gains.

While there are several other ways to obtain differential amplifiers, perhaps the easiest is to simply buy them; a number of manufacturers presently supply very high-quality devices at reasonable prices. One example of such a device is the AD627. Figure 3-18 shows how the device can be hooked up. Only one external component, a resistor (R_G) to set gain, is necessary for operation. As with any precision analog circuit, local power supply bypassing (in this case provided by capacitor C_B) is usually a good idea.

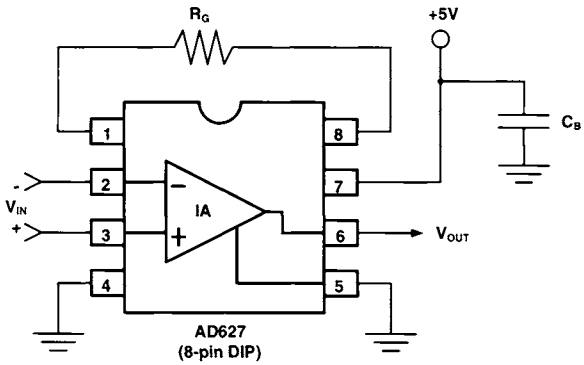

Figure 3-18: External connections for AD627 monolithic instrumentation amplifier.

Aside from component count reduction, the use of monolithic devices offers many performance advantages. Some of the key parameters of the AD627 ("A" version for 5V operation at 25°C) are listed in Table 3-2:

Table 3-2: Key parameters of AD627A instrumentation amplifier.

Parameter	Min	Typical	Max	Units
Input offset voltage	—	50	250	μV
Gain range	5	—	1000	—
Gain error (G=5)	—	0.03	0.10	%

(Continued)

Parameter	Min	Typical	Max	Units
Gain vs. temperature (G=5)	—	10	20	ppm/°C
Input current	—	3	10	nA
Gain-bandwidth product		400		kHz
Common-mode rejection	77	90	—	dB
Input voltage noise (G=100)		37		NV/√Hz

Designing an instrumentation amplifier with this level of performance using discrete op-amps and resistors would be a challenging project, especially at a cost less than or equal to that of the AD627. For many applications, using an off-the-shelf monolithic instrumentation amplifier will be the most cost-effective means of achieving a desired level of performance.

3.7 Analog Temperature Compensation

Although it is possible to make voltage sources, current sources, and amplifiers with a high degree of temperature stability, it is difficult to obtain this characteristic in a Hall-effect transducer. While the transducer provides a more constant gain over temperature when biased with a constant current (0.05%/°C) than with a constant voltage (0.3%/°C), many applications require higher levels of stability.

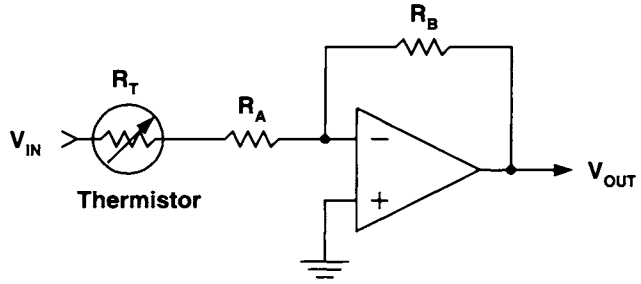

Figure 3-19: Temperature-compensated amplifier.

One method of increasing the temperature stability is to use an amplifier with a temperature dependent gain. Figure 3-19 shows one such implementation based on an op-amp and a thermistor, in an inverting configuration. As the temperature increases, the value of the thermistor decreases, causing the gain to rise. Because the temperature responses of most thermistors are highly nonlinear, it will often be impossible to obtain an exact desired gain-vs.-temperature response for any given combination of resistors and thermistors. The gain for this circuit as a function of temperature is given by:

$$G(T) = \frac{-R_B}{R_A + R_T(T)}$$ **(Equation 3-7)**

The best that can usually be done is to obtain an exact fit at two predetermined reference temperatures, with some degree of error at temperatures in-between. One procedure for designing this type of circuit, given a set of desired gains and a given thermistor, is as follows:

1) Determine the temperatures at which exact fit is desired (T_1, T_2)
2) Determine the gain at T_1 and T_2 (G_1, G_2)
3) Determine the resistance of the thermistor at T_1, T_2 (R_{T1}, R_{T2})
4) Calculate R_A by:

$$R_A = \frac{(G_2 R_{T2} - G_1 R_{T1})}{G_1 - G_2}$$ **(Equation 3-8)**

5) Calculate R_B by:

$$R_B = -G_1 (R_A + R_{T1})$$ **(Equation 3-9)**

The above procedure assumes that a positive temperature coefficient of gain is desired and the resistor has a negative temperature coefficient. Note that there will be some cases for which a viable solution doesn't exist (usually indicated by a negative value for R_A or R_B), and others for which the solution may be unacceptable (i.e., resistor values are too low or too high).

Example:
Design a circuit to provide a gain of –9 at 0°C and –11 at 50°C. The thermistor to be used has a resistance of 32.65 kΩ at 0°C and 3.60 kΩ at 50°C. (As a side note, this degree of resistance variation is not at all unusual in a thermistor; the device used in this example is a 10-kΩ (nominal @ 25°C) "J" curve device.)

$G_1 = -9$
$G_2 = -11$
$R_{T1} = 32.65\ \text{k}\Omega$
$R_{T2} = 3.60\ \text{k}\Omega$

(Equation 3-10)

$$R_A = \frac{(G_2 R_{T2} - G_1 R_{T1})}{(G_1 - G_2)} = \frac{(-11 \cdot 3.60\ \text{k}\Omega - (-9 * 32.65\ \text{k}\Omega))}{(-9 - (-11))} = 127\ \text{k}\Omega$$

$$R_B = -G_1\left(R_A + R_{T1}\right) = -\left(-9\right)\left(127\ \text{k}\Omega + 32.65\ \text{k}\Omega\right) = 1436\ \text{k}\Omega \quad \textbf{(Equation 3-11)}$$

Table 3-3 shows the gain of this circuit for several temperatures, and the departure from a straight-line fit (% error).

Table 3-3: Temperature compensated amplifier performance.

T (°C)	RT (kΩ)	Ideal Gain (straight-line)	Actual Gain (circuit)	Error %
–20	97.08	–8.2	–6.4	–22
–10	55.33	–8.6	–7.9	–8
0	32.65	–9	–9	0
10	19.90	–9.4	–9.8	4
20	12.49	–9.8	–10.3	5
30	8.06	–10.2	–10.6	4
40	5.33	–10.6	–10.8	2
50	3.60	–11	–11	0
60	2.49	–11.4	–11.1	–3
70	1.75	–11.8	–11.2	–5

Although temperature-compensated amplifiers can be useful in certain situations, they suffer from two principal drawbacks. The first is that, as the above example shows, it can be difficult to get the curve one really wants with available components. Although various series and parallel combinations of resistors and thermistors can be used to get more desirable temperature characteristics (with varying degrees of success), this also results in more complex design procedures, with the design process often deteriorating into trial-and-error.

The second drawback is a little more philosophical; the underlying physical mechanism responsible for transducer gain variation will rarely be the same as that underlying the temperature response of your compensated amplifier. In practice this means that you often can't design a compensation scheme that works well over the process variation seen in production. Any given compensation scheme may need to be adjusted on an individual basis for each transducer, or at least on a lot-by-lot basis in production. Since this adjustment process requires collection of data over temperature, it can be an expensive proposition with lots of room for error.

3.8 Offset Adjustment

While some systematic attempts can be made to temperature compensate the gain of a Hall-effect transducer, the ohmic offset voltage is usually random enough so that to make any significant reduction requires compensation of devices on an individual basis. Moreover, since the drift of the ohmic offset will also usually have an unpredictable component, one will often only try to null it out at a single temperature (such as 25°C).

The simplest method of offset adjustment is shown in Figure 3-20; it uses a manual potentiometer to null out the offset of the Hall-effect transducer. The potentiometer is used to set a voltage either positive or negative with respect to the output sense terminal, and a high-value resistor (R_A) sets an offset current into or out of the transducer. It is therefore possible to null out either positive or negative offsets with this scheme.

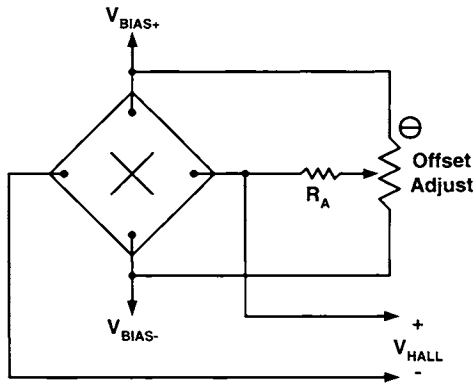

Figure 3-20: Manual offset adjustment using potentiometer.

An adjustment made in this manner is relatively stable over temperature, particularly if the temperature coefficient of resistance of R_A can be made similar to that of the transducer output. Another feature of this trim method is that it can be used regardless of whether the transducer is biased from a constant current or a constant voltage source. The amount of trim current injected through R_A will be proportional to the bias voltage, and will thus track the transducer's ohmic offset over variations in bias voltage.

Offset adjustment can also be made at the amplifier. When performing offset correction in the amplifier circuitry, an important consideration is that the transducer's offset voltage will be proportional to the voltage across its drive terminals. The input offset voltage of the amplifier, however, will be independent of sensor bias conditions. In the case of a transducer being operated from a constant bias voltage, both offsets can be approximately corrected through one adjustment. Because Hall-effect transducers are

more typically biased with a constant current source, the transducer bias voltage will change as a function of temperature. There are several approaches to dealing with these two independent offset error sources. The first is to get an amplifier with an acceptably low input offset specification and simply ignore its input offset voltage. A circuit to perform an adjustment of transducer offset is shown in Figure 3-21. This circuit measures the actual bias voltage across the transducer and generates proportional positive and negative voltage references based on the bias voltage. The potentiometer allows one to add an offset correction to the amplified sensor signal. Since this correction will be proportional to the transducer bias voltage, it will track changes in transducer offset resulting from bias variation over temperature.

If a separate offset adjustment were added to correct for input voltage offset of the instrumentation amplifier, the offset adjustment process would need to be performed as a two-stage process. First the amplifier inputs would need to be shorted together and the amplifier offset adjusted, for zero output voltage. Next, the short would be removed, and the Hall-offset adjust would be used to trim out the remaining offset.

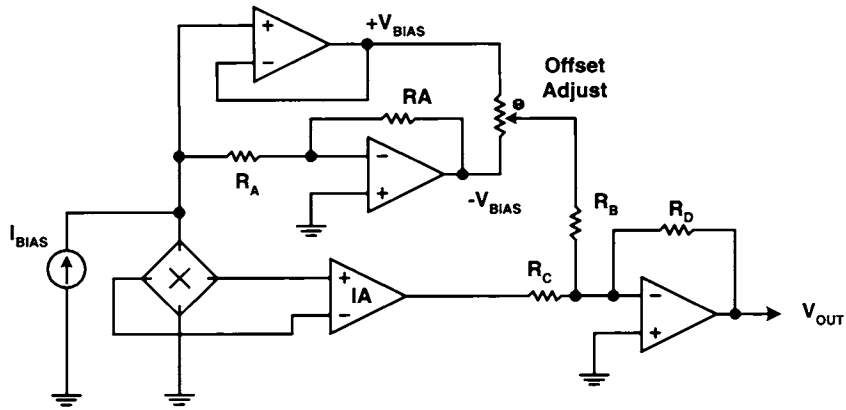

Figure 3-21: Correcting transducer offset at the amplifier.

3.9 Dynamic Offset Cancellation Technique

In addition to removing zero-flux ohmic offset by manually trimming it out, an elegant method exists that exploits a property of the Hall-effect transducer to reduce system offset.

A four-way symmetric Hall-effect transducer can be viewed as a Wheatstone bridge. Ohmic offsets can be represented as a smali ΔR, as shown in Figure 3-22a. When bias current is applied to the drive terminals, the output voltage appearing at the sense terminals is $V_H + V_E$, where V_H is the Hall voltage and V_E is the offset error voltage.

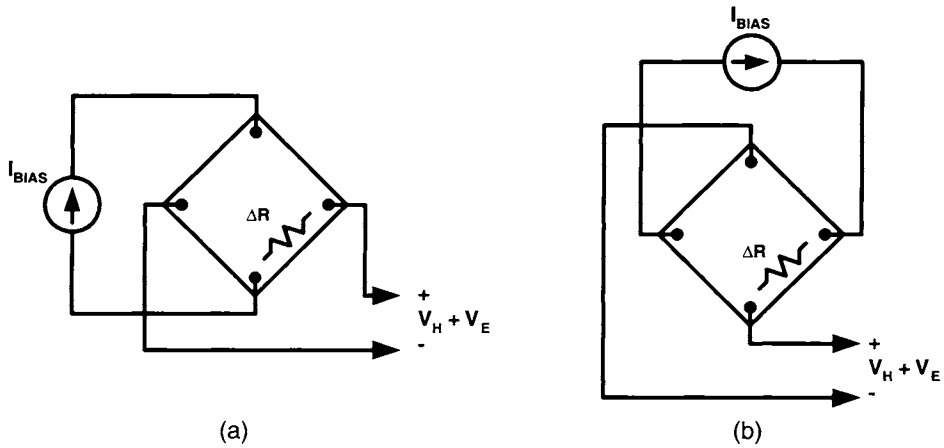

Figure 3-22: Effects of rotating bias and sense terminals on output.

Now consider what happens if we take the transducer and reconnect the bias and sense terminals, as shown in Figure 3-22b. All of the terminal functions have been rotated clockwise by 90°. The sense terminals are now connected to bias voltage, and the former drive terminals are now used as outputs. Because the transducer is symmetric with rotation, we should expect to see, and do see, the same Hall output voltage.

The transducer, however, is not symmetric with respect to the location of ΔR. In effect, this resistor has moved from the lower right leg of the Wheatstone bridge to the upper right leg, resulting in a polarity inversion of the ohmic offset voltage. The total output voltage is now $V_H - V_E$. One way to visualize this effect is to see the Hall voltage as rotating in the same direction as the rotation in the bias current, while the ohmic offset rotates in the opposite direction.

If one were to take these two measurements to obtain $V_H + V_E$ and $V_H - V_E$, one can then simply average them to obtain the true value of V_H. For this technique to work, the only requirement on the Hall-effect transducer is that it be symmetric with respect to rotation.

It is possible to build a circuit that is able to perform this "plate-switching" function automatically. By using CMOS switches, one can construct a circuit that can rotate the bias and measurement connections automatically. Such a circuit is shown in Figure 3-23. An oscillator provides a timing signal that controls the switching. When the clock output is LOW, the switches A,B,E, and F close, and switches C,D,G, and H open. This places the transducer in a configuration that outputs $V_H + V_E$. When the clock goes HIGH, switches C,D,G,H close, while the remaining switches open. This outputs $V_H - V_E$.

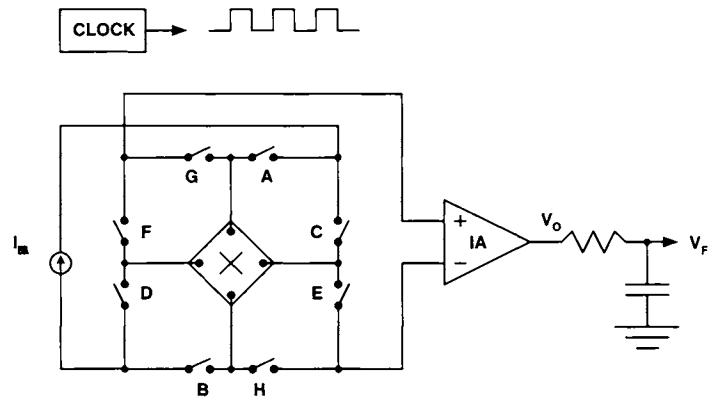

Figure 3-23: Switching network and output filter for auto-nulling offset voltage.

The output signal produced by the transducer and this periodic switching network next needs to be amplified and averaged. While there are several ways of averaging the signal over time, the simplest is through the use of a low-pass filter. Examples of signals present at various stages of this network are shown in Figure 3-24.

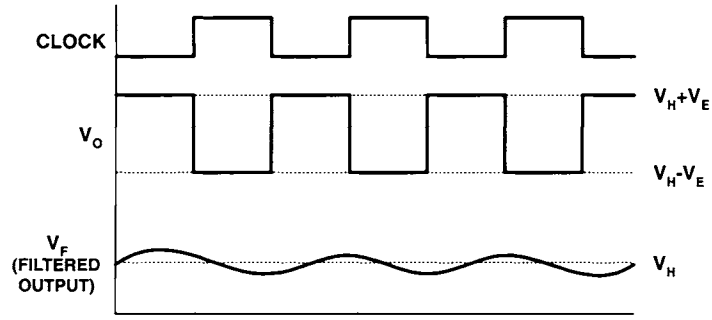

Figure 3-24: Auto-nulling circuit waveforms.

This technique is used, with suitable modifications, in many modern Hall-effect integrated circuits. It is often referred to by the terms *plate-switching*, *auto-nulling*, and *chopper-stabilization*. When properly implemented, it can reduce the effective ohmic offset of a given transducer by nearly two orders of magnitude. Additionally, since the offset is being cancelled out dynamically, it is very temperature stable. This technique can also be employed in the construction of the digital-output Hall-effect ICs, resulting in highly sensitive devices with low and temperature-stable operate (turn-on) and release (turn-off) points.