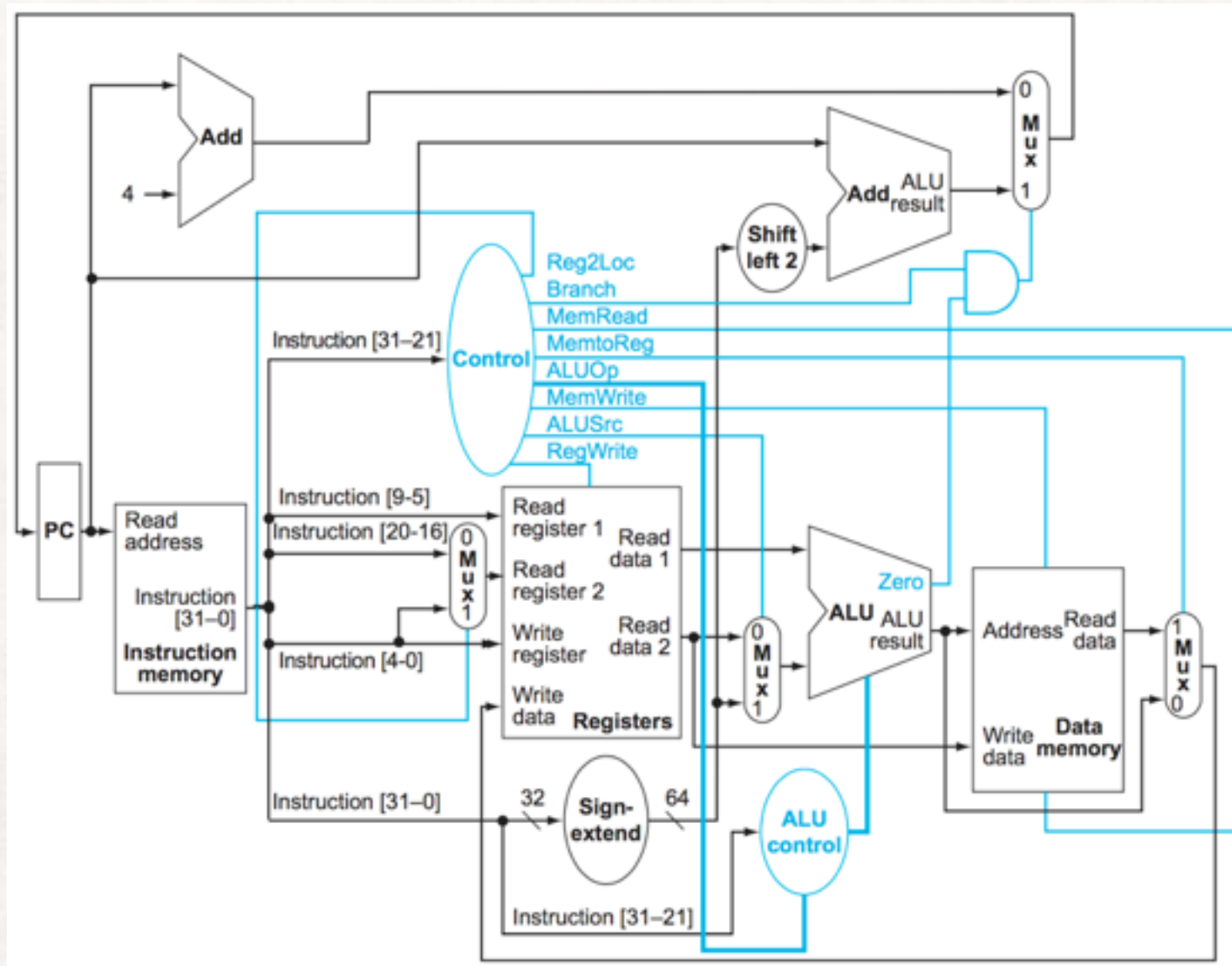


# ARM DATAPATH CONTROL SIGNALS



What are the control signals for

ADD X9, X9, X10

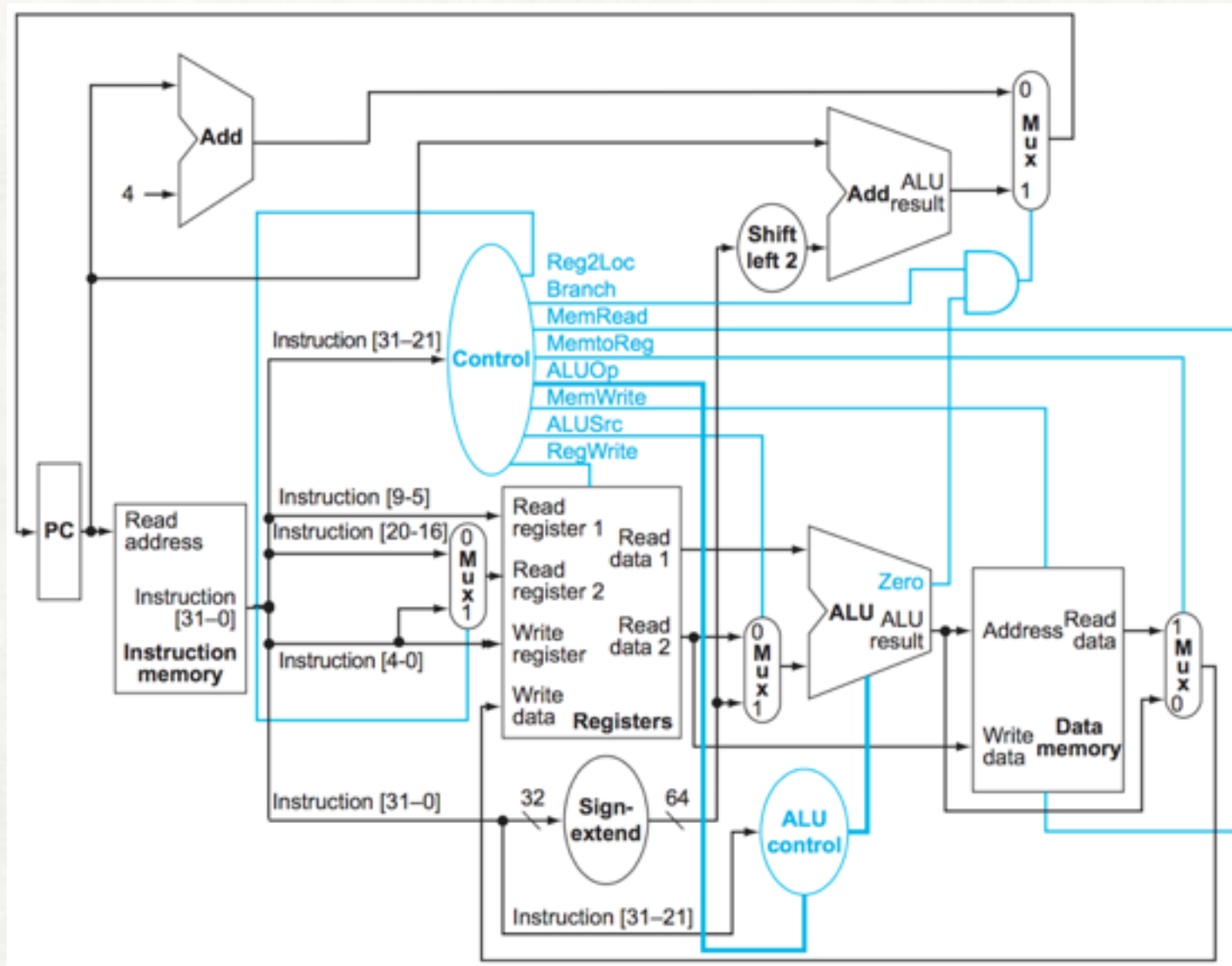
## CORE INSTRUCTION FORMATS

R	opcode		Rm	shamt		Rn	Rd	
	31	21 20	16 15	10 9	5 4	0		
I	opcode		ALU immediate			Rn	Rd	
	31	22 21	10 9			5 4	0	
D	opcode		DT_address		op	Rn	Rt	
	31	21 20	12 11 10 9		5 4	0		
B	opcode	BR_address						
	31	26 25	0					
CB	Opcode	COND_BR_address					Rt	
	31	24 23	5 4					0
IW	opcode		MOV_immediate				Rd	
	31	21 20	5 4				0	

Reg2Loc  
Branch  
MemRead  
MemtoReg  
ALUOp  
MemWrite  
ALUSrc  
RegWrite

Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

# ARM DATAPATH CONTROL SIGNALS



What are the control signals for

ADD X9, X9, X10

## CORE INSTRUCTION FORMATS

R	opcode	Rm	shamt	Rn	Rd
	31	21 20	16 15	10 9	5 4 0
I	opcode	ALU immediate		Rn	Rd
	31	22 21	10 9		5 4 0
D	opcode	DT address		op	Rn
	31	21 20	12 11 10 9	5 4	0
B	opcode	BR address			
	31	26 25	0		
CB	Opcode	COND_BR address			Rt
	31	24 23	5 4	0	
IW	opcode	MOV immediate			Rd
	31	21 20	5 4	0	

Reg2Loc 0

Branch 0

MemRead 0

MemtoReg 0

ALUOp 10

MemWrite 0

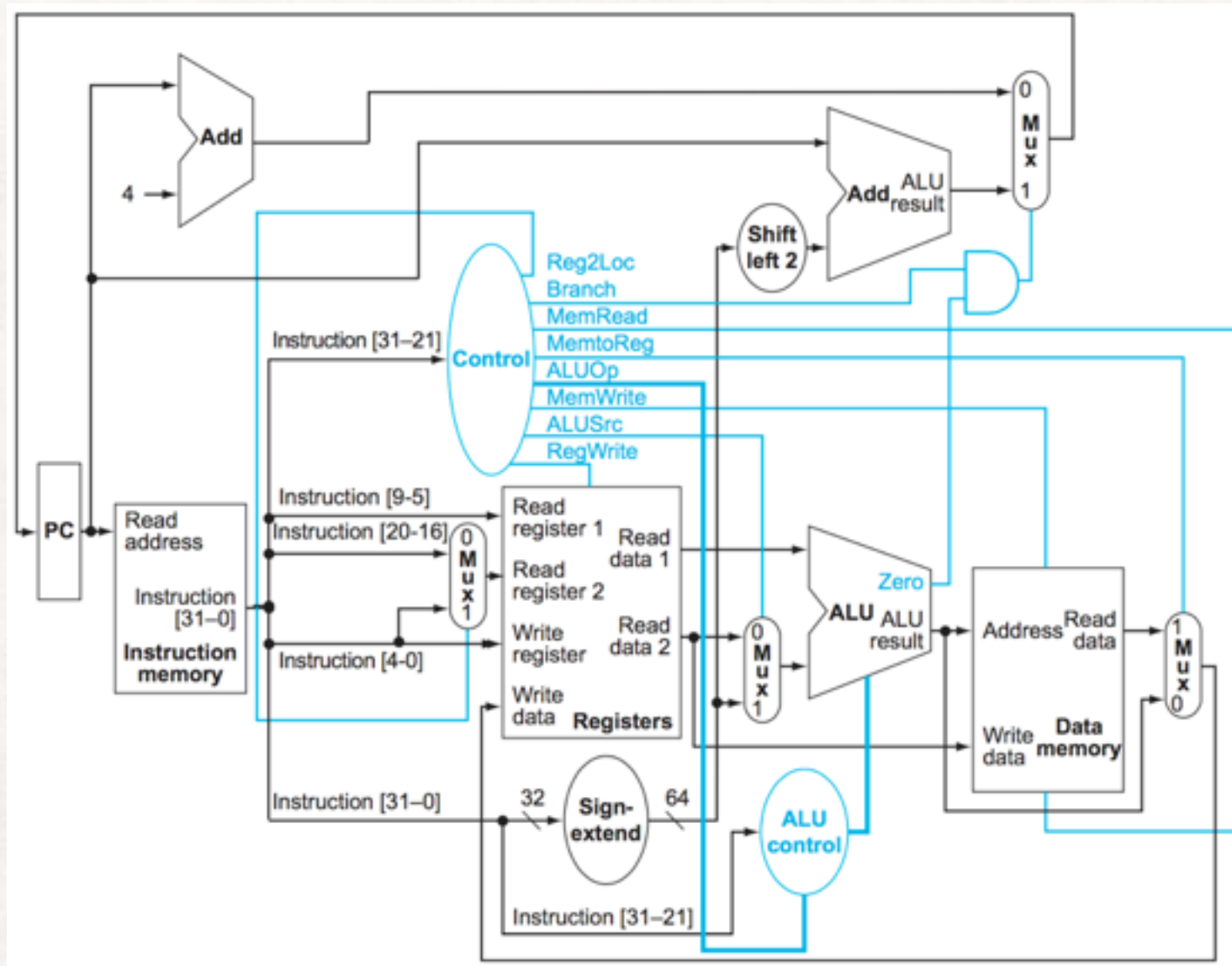
ALUSrc 0

RegWrite 1

Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001



# ARM DATAPATH CONTROL SIGNALS



What are the control signals for

CBZ X9, #4

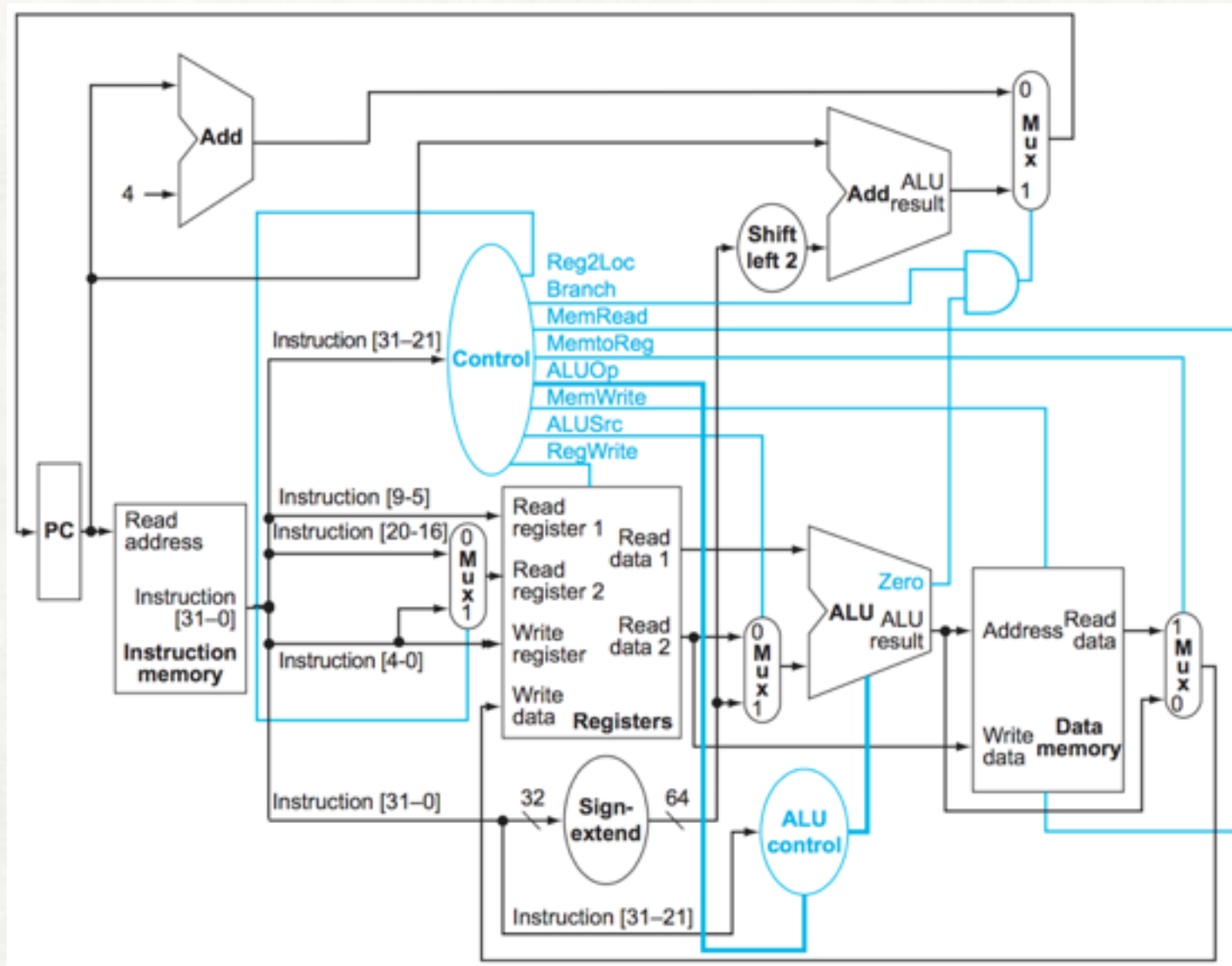
## CORE INSTRUCTION FORMATS

R	opcode		Rm	shamt		Rn	Rd	
	31	21 20	16 15	10 9	5 4	0		
I	opcode		ALU immediate			Rn	Rd	
	31	22 21	10 9			5 4	0	
D	opcode		DT_address		op	Rn	Rt	
	31	21 20	12 11 10 9		5 4	0		
B	opcode	BR_address						
	31	26 25	0					
CB	Opcode	COND_BR_address					Rt	
	31	24 23	5 4					0
IW	opcode		MOV_immediate				Rd	
	31	21 20	5 4				0	

Reg2Loc  
Branch  
MemRead  
MemtoReg  
ALUOp  
MemWrite  
ALUSrc  
RegWrite

Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

# ARM DATAPATH CONTROL SIGNALS



What are the control signals for  
CBZ X9, #4

## CORE INSTRUCTION FORMATS

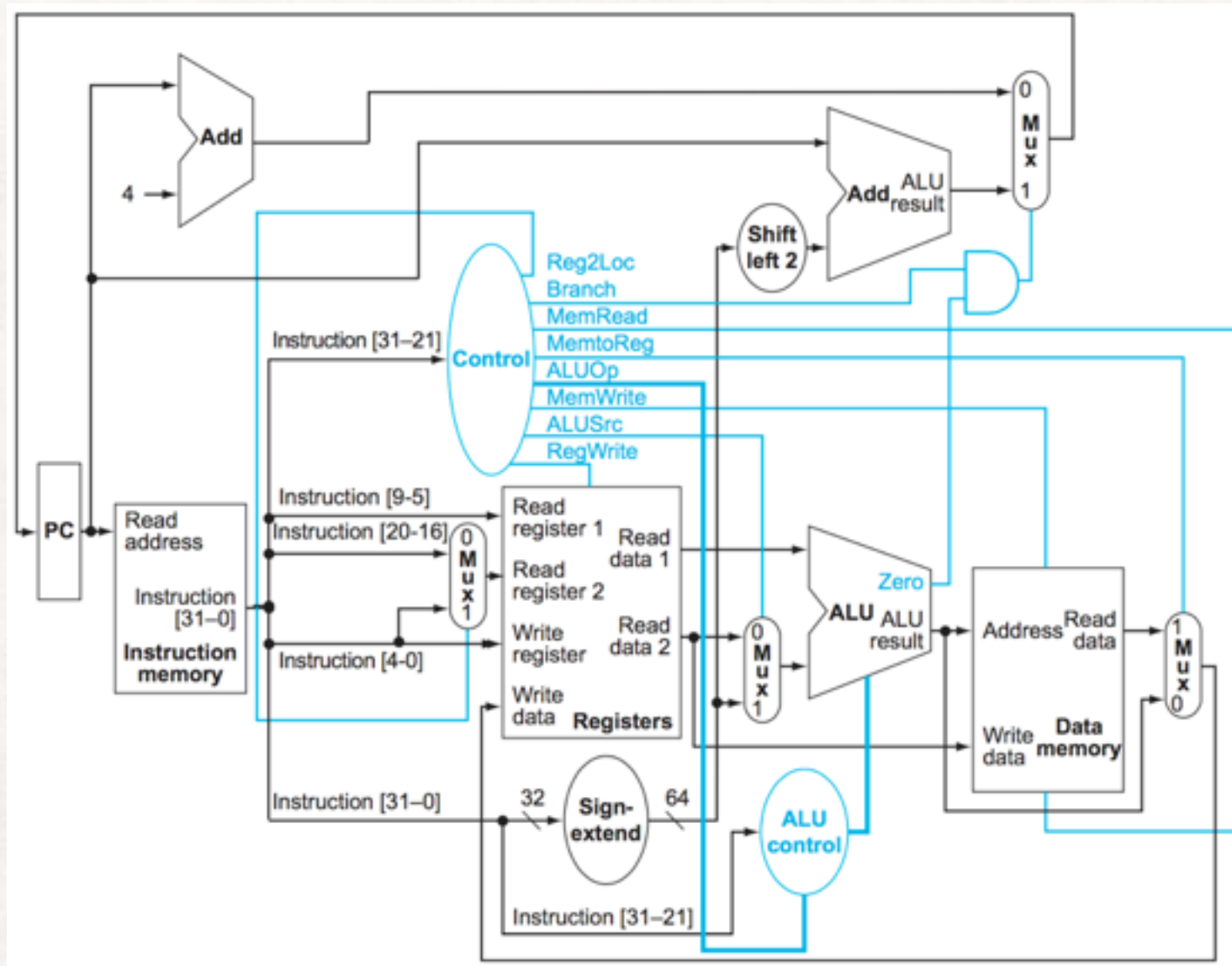
R	opcode	Rm	shamt	Rn	Rd
	31	21 20	16 15	10 9	5 4 0
I	opcode	ALU immediate		Rn	Rd
	31	22 21		10 9	5 4 0
D	opcode	DT address		op	Rn Rt
	31	21 20		12 11 10 9	5 4 0
B	opcode	BR address			
	31	26 25			
CB	Opcode	COND_BR address			Rt
	31	24 23			5 4 0
IW	opcode	MOV immediate			Rd
	31	21 20			5 4 0

Reg2Loc 1  
Branch 1  
MemRead 0  
MemtoReg x  
ALUOp 01  
MemWrite 0  
ALUSrc 0  
RegWrite 0

Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001



# ARM DATAPATH CONTROL SIGNALS



# What are the control signals for

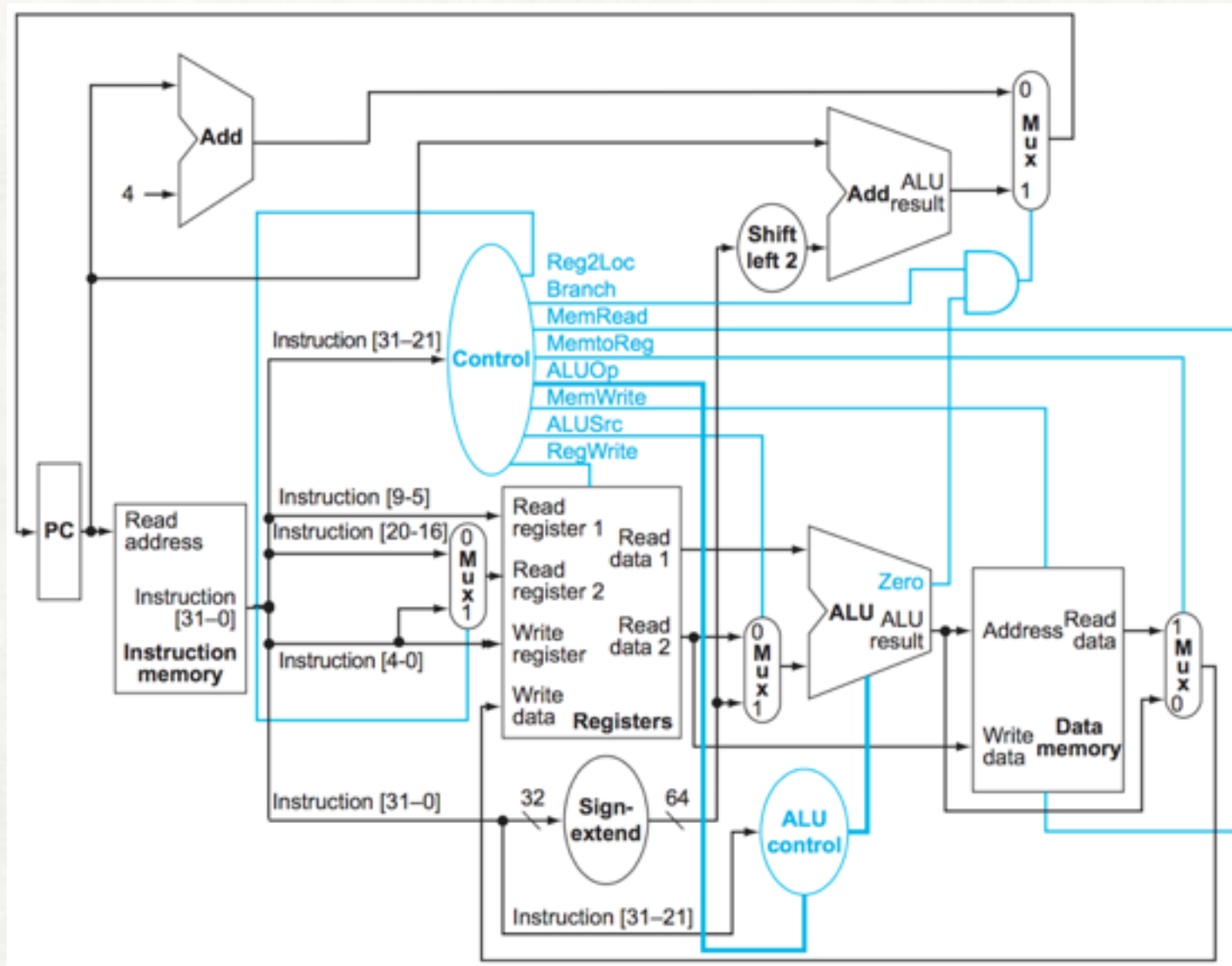
## STUR X9, [X10, #8]

CORE INSTRUCTION FORMATS									
<b>R</b>	opcode		Rm	shamt		Rn	Rd		
	31	21 20	16 15	10 9		5 4	0		
<b>I</b>	opcode		ALU immediate			Rn	Rd		
	31	22 21	10 9		5 4	0			
<b>D</b>	opcode		DT_address		op	Rn	Rt		
	31	21 20	12 11		10 9	5 4	0		
<b>B</b>	opcode	BR_address							
	31	26 25	0						
<b>CB</b>	Opcode	COND BR_address					Rt		
	31	24 23	5 4				0		
<b>IW</b>	opcode		MOV_immediate				Rd		
	31	21 20	5 4				0		

Reg2Loc  
Branch  
MemRead  
MemtoReg  
ALUOp  
MemWrite  
ALUSrc  
RegWrite

Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

# ARM DATAPATH CONTROL SIGNALS



What are the control signals for  
STUR X9, [X10, #8]

## CORE INSTRUCTION FORMATS

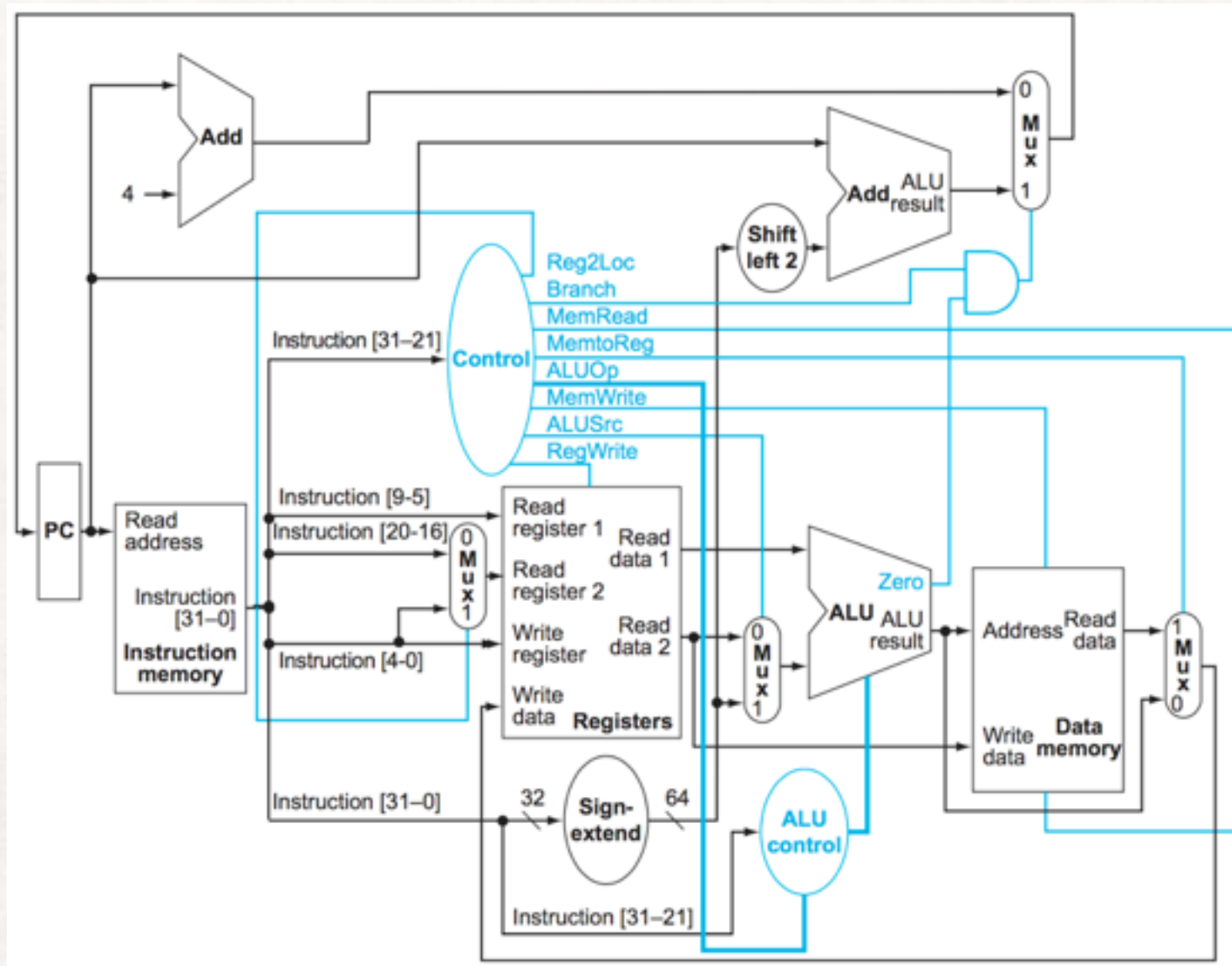
R	opcode	Rm	shamt	Rn	Rd
	31	21 20	16 15	10 9	5 4 0
I	opcode	ALU immediate		Rn	Rd
	31	22 21	10 9		5 4 0
D	opcode	DT address		op	Rn
	31	21 20	12 11 10 9	5 4	0
B	opcode	BR address			
	31	26 25	0		
CB	Opcode	COND_BR address			Rt
	31	24 23	5 4	0	
IW	opcode	MOV immediate			Rd
	31	21 20	5 4	0	

Reg2Loc 1  
Branch 0  
MemRead 0  
MemtoReg x  
ALUOp 00  
MemWrite 1  
ALUSrc 1  
RegWrite 0

Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001



# ARM DATAPATH CONTROL SIGNALS



What are the control signals for

LDUR X9, [X10, #8]

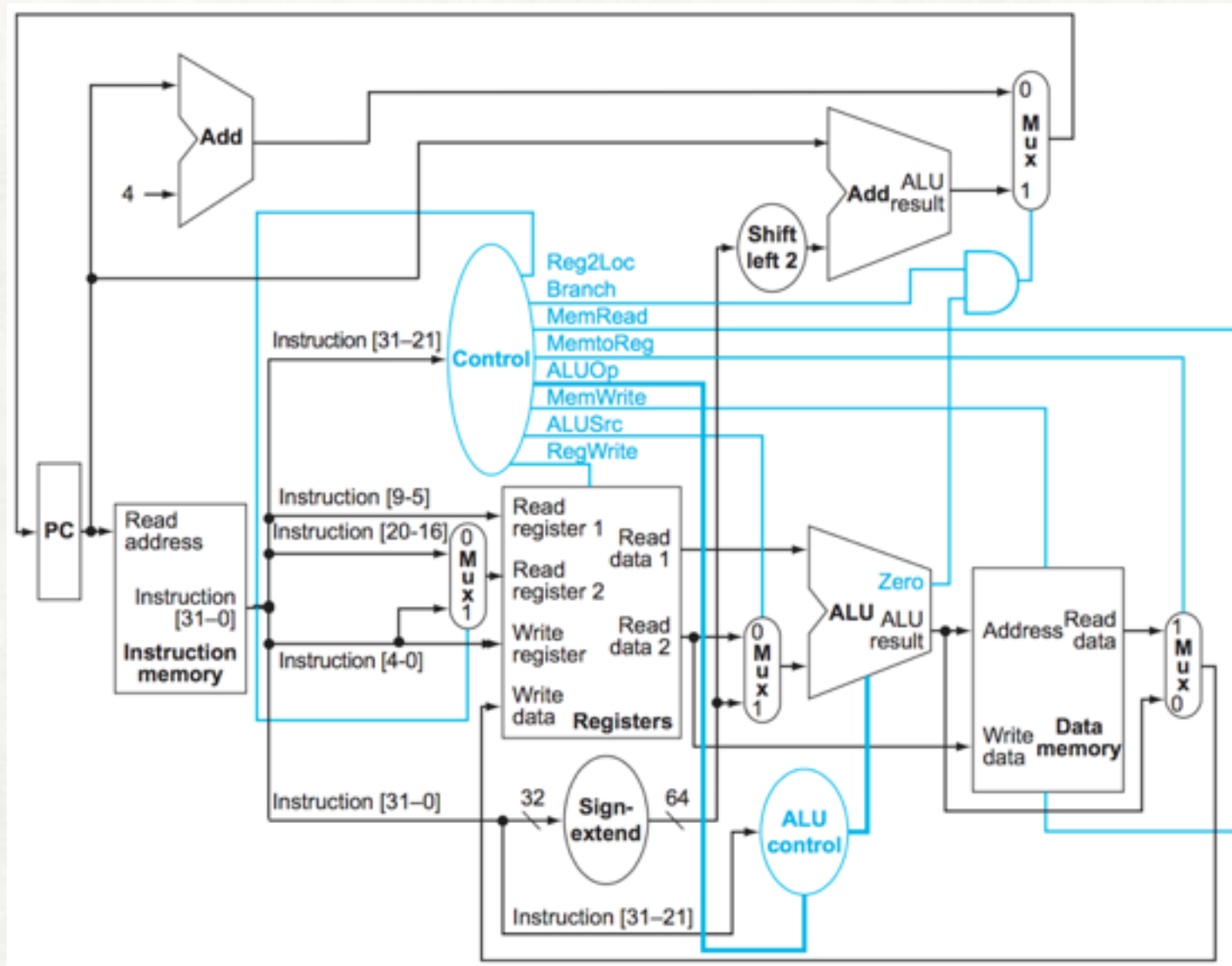
## CORE INSTRUCTION FORMATS

R	opcode	Rm	shamt	Rn	Rd
	31	21 20	16 15	10 9	5 4 0
I	opcode	ALU immediate		Rn	Rd
	31	22 21		10 9	5 4 0
D	opcode	DT_address	op	Rn	Rt
	31	21 20	12 11 10 9	5 4	0
B	opcode	BR address			
	31	26 25	0		
CB	Opcode	COND BR address			Rt
	31	24 23		5 4	0
IW	opcode	MOV immediate			Rd
	31	21 20		5 4	0

Reg2Loc  
Branch  
MemRead  
MemtoReg  
ALUOp  
MemWrite  
ALUSrc  
RegWrite

Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

# ARM DATAPATH CONTROL SIGNALS



What are the control signals for

LDUR X9, [X10, #8]

## CORE INSTRUCTION FORMATS

R	opcode	Rm	shamt	Rn	Rd
	31	21 20	16 15	10 9	5 4 0
I	opcode	ALU immediate		Rn	Rd
	31	22 21	10 9		5 4 0
D	opcode	DT address		op	Rn Rt
	31	21 20	12 11 10 9	5 4	0
B	opcode	BR address			
	31	26 25	0		
CB	Opcode	COND_BR address			Rt
	31	24 23	5 4	0	
IW	opcode	MOV immediate			Rd
	31	21 20	5 4	0	

Reg2Loc x  
Branch 0  
MemRead 1  
MemtoReg 1  
ALUOp 00  
MemWrite 0  
ALUSrc 1  
RegWrite 1

Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001