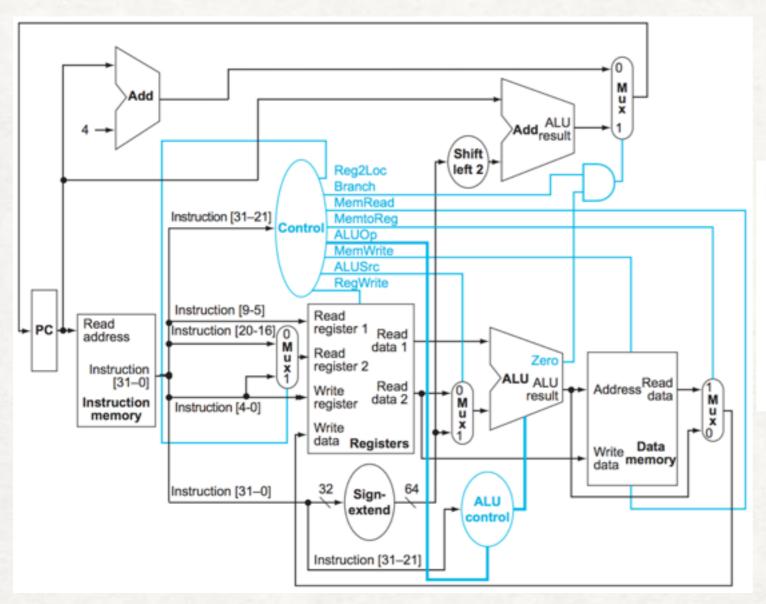


Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control Input
LDUR	00	load register	XXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

What are the control signals for

ADD X9, X9, X10

R	opcode		Rm	shan	nt	Rn		Rd	
	31	21 20	0 16	15	10 9		54		(
Ι [opcode		ALU i	mmediate		Rn		Rd	
	31	22 21			10 9		54		(
D [opcode		DT a	ddress	op	Rn		Rt	
	31	21 20)	1:	2 11 10 9		54		(
в [opcode			BR :	address				
	31 26 25	5							-
CB [Opcode		CONI	D BR add	ress			Rt	
	31 24 23	;					54		-
IW [opcode			MOV in	mediate			Rd	
	31	21 20)				54		-



Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control Input
LDUR	00	load register	XXXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

What are the control signals for

ADD X9, X9, X10

R	opcode		Rm	shamt		Rn		Rd	
	31	21 20	16 15		109		54		(
Į.	opcode		ALU imn	nediate		Rn		Rd	
	31	22 21			109		54		
D	opcode	1	DT addr	ess	op	Rn		Rt	
	31	21 20		12	11 10 9		54		
В	opcode			BR_ad	dress				
	31 26 2	5							
CB	Opcode		COND E	3R addre	ss			Rt	
	31 24 2	3					54		
W	opcode		M	fOV imn	rediate			Rd	
	31	21 20					5.4		

Reg2Loc 0

Branch 0

MemRead 0

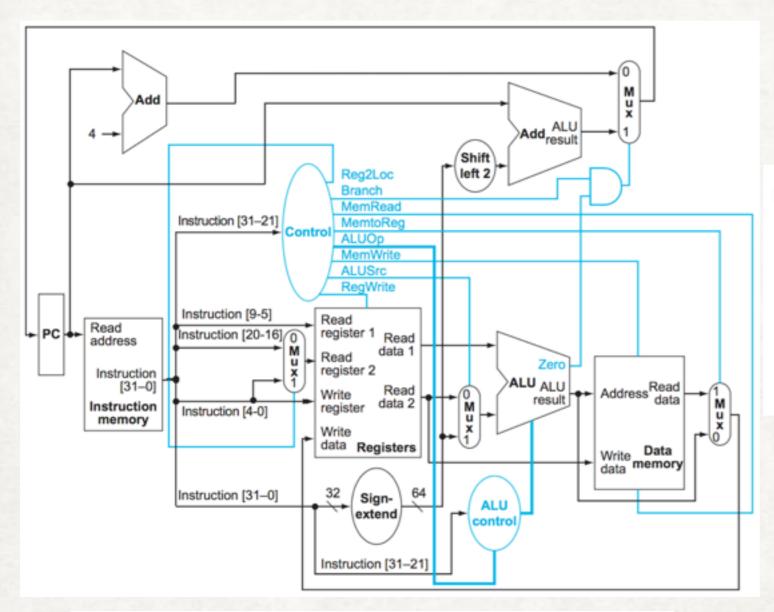
MemtoReg 0

ALUOp 10

MemWrite 0

ALUSrc 0

RegWrite 1

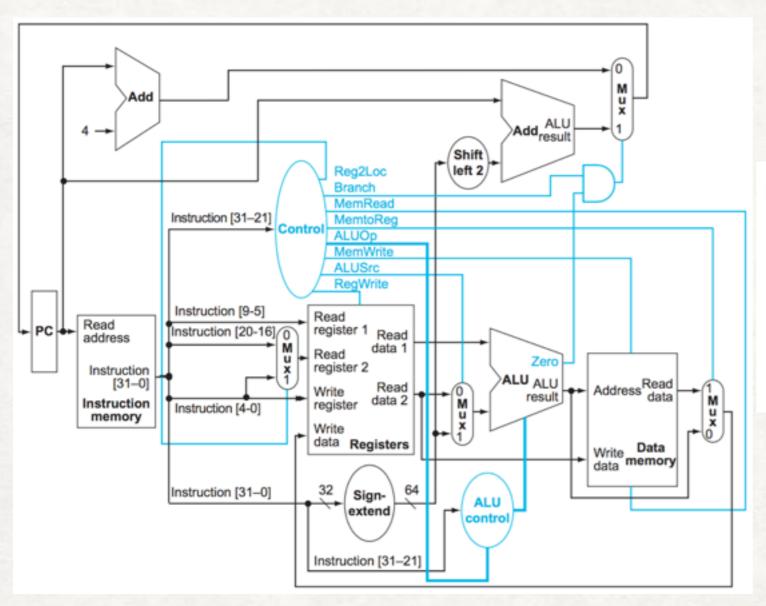


Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

What are the control signals for

CBZ X9, #4

3	opcode		Rm	shamt		Rn	Rd	
	31	21 20	16 1	5	109	5	5 4	
	opcode		ALU im	mediate		Rn	Rd	
	31	22 21			109	5	5.4	
	opcode		DT add	dress	op	Rn	Rt	
	31	21 20		12	11 10 9	5	4	
	opcode			BR ac	ldress			
	31 26 2:	5						
В	Opcode		COND	BR addre	:ss		Rt	
	31 24 23	3				5	5.4	
V	opcode			MOV imr	nediate		Rd	
	31	21 20				5	5.4	



Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

What are the control signals for

CBZ X9, #4

e opcode		Rm	S	hamt		Rn			Rd	
31	21	20	16 15		109		5	4		(
opcode		ALU	immedi	ate		Rn			Rd	
31	22 21				109		5	4		(
opcode		DT	address	О	р	Rn			Rt	
31	21	20		12 11	109		-5	4		-
opcode			В	R_addr	ess					
31	26 25									
B Opcode		CO	ND BR	address					Rt	
31	24 23						5	4		
W opcode			MOV	immed	fiate				Rd	
31	21	20					- 5	4		

Reg2Loc 1

Branch 1

MemRead 0

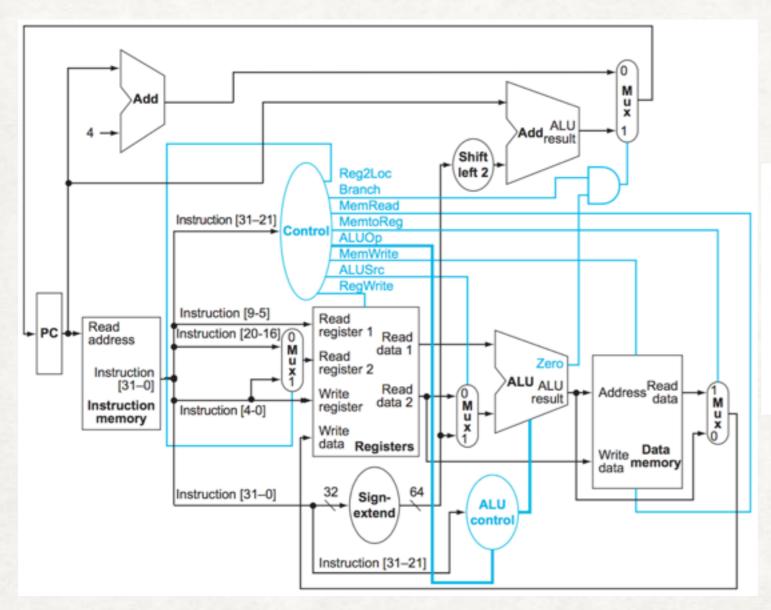
MemtoReg x

ALUOp 01

MemWrite 0

ALUSrc 0

RegWrite 0

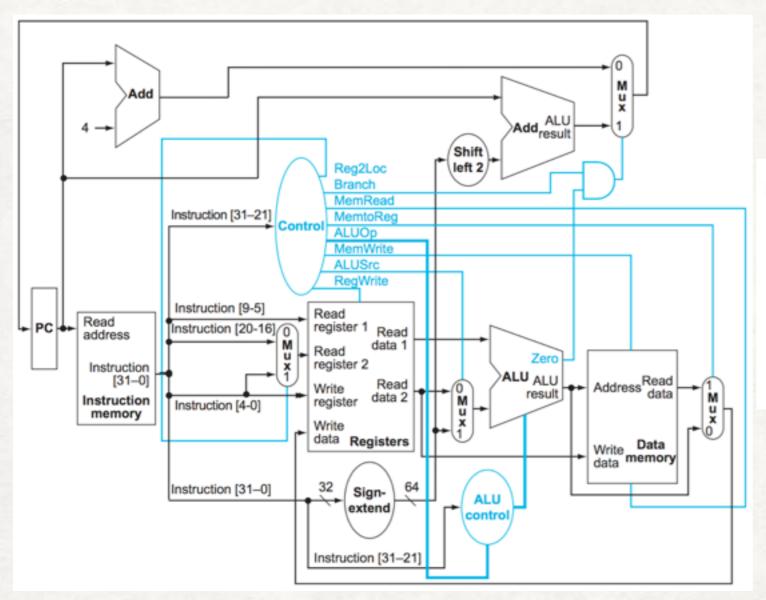


Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

What are the control signals for

STUR X9, [X10, #8]

R	opcode		Rm	sha	amt	Rn		Rd	
	31	21 2	0 16	15	10	9	5 4		
I.	opcode		ALU it	nmediat	e	Rn		Rd	
	31	22 21			10	9	54		
D	opcode		DT_ac	ldress	op	Rn		Rt	
	31	212	0		12 11 10	9	54		
В	opcode			BR	_address				
	31 26	25							
CB	Opcode		COND	BR ad	ldress			Rt	
	31 24	23					5 4		
W	opcode			MOV_i	immedia	te		Rd	
	31	21.2	0				54		



Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

What are the control signals for

STUR X9, [X10, #8]

R	opcode		Rm	shamt		Rn		Rd	
	31	21 20	16 15	5	109		54		(
L	opcode		ALU imr	nediate		Rn		Rd	
	31	22 21			109		54		(
D	opcode		DT add	ress	op	Rn		Rt	
	31	21 20		12	11 10 9		54		(
В	opcode			BR_ad	dress				
	31 26 2	5							(
CB	Opcode		COND	BR_addre	ss			Rt	
	31 24 2	3					54		(
W	opcode		N	4OV_imn	nediate			Rd	
	31	21 20					54		(

Reg2Loc 1

Branch 0

MemRead 0

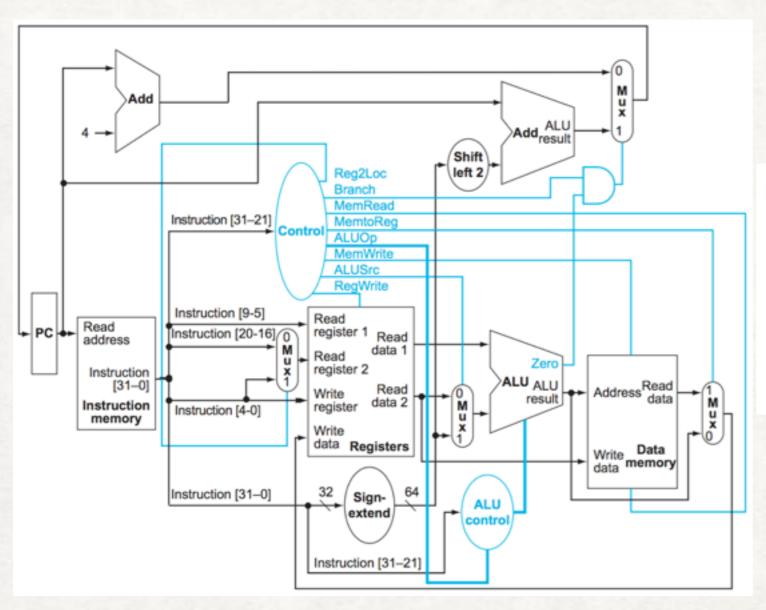
MemtoReg x

ALUOp 00

MemWrite 1

ALUSrc 1

RegWrite 0

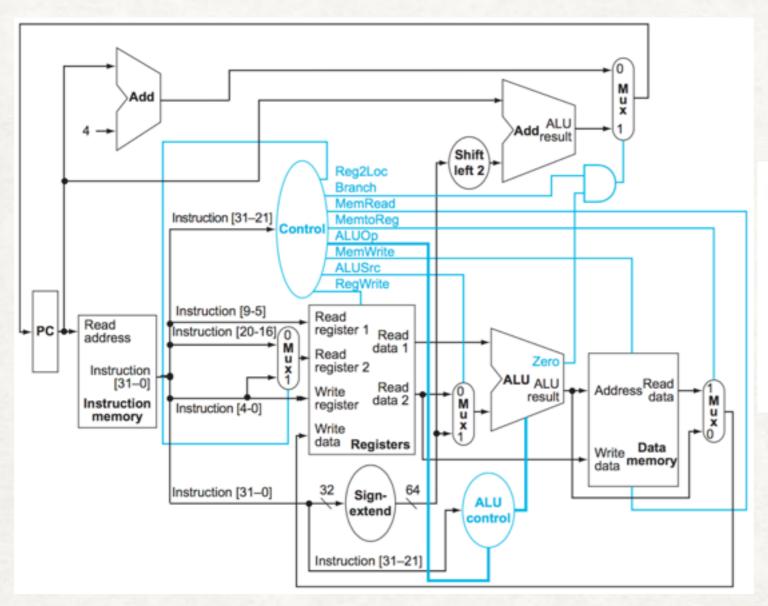


Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

What are the control signals for

LDUR X9, [X10, #8]

R	opcode		Rm	shan	nt	Rn		Rd	
	31	21.20	0 16	15	109		54		(
[opcode		ALU immediate			Rn		Rd	
	31	22 21			109		54		-
D	opcode		DT a	ddress	op	Rn		Rt	
	31	21.20)	12	2 11 10 9		54		
3	opcode	BR address							
	31 262	5							
В	Opcode	COND BR address						Rt	
	31 242	3					54		
w	opcode			MOV im	mediate			Rd	
	31	21.20)				54		



Instruction	ALUOp	Instruction operation	Opcode field	Desired ALU action	ALU control input
LDUR	00	load register	XXXXXXXXXXXXX	add	0010
STUR	00	store register	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	add	0010
CBZ	01	compare and branch on zero	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	pass input b	0111
R-type	10	ADD	10001011000	add	0010
R-type	10	SUB	11001011000	subtract	0110
R-type	10	AND	10001010000	AND	0000
R-type	10	ORR	10101010000	OR	0001

What are the control signals for

LDUR X9, [X10, #8]

R	opcode		Rm	sham	nt	Rn		Rd	
	31	21 20	16	15	109		54		(
I	opcode		ALU immediate		Rn			Rd	
	31	22 21			109		54		(
D	opcode		DT ac	ldress	op	Rn		Rt	
	31	21 20		12	11 10 9		54		(
В	opcode	BR address							
	31 26 2:	5							(
CB	Opcode	COND BR address						Rt	
	31 24 2	3					54		(
IW	opcode			MOV im	mediate			Rd	
	31	21 20					54		- (

Reg2Loc x
Branch 0
MemRead 1
MemtoReg 1
ALUOp 00
MemWrite 0
ALUSrc 1
RegWrite 1