# Vyshak Suresh

**P:** (346) 438-0410 LinkedIn **E:** vyshaksureshh@gmail.com

Design and Analysis | Schematic Diagrams | Scheduling |Digital Circuit Design | FPGA / ASIC Design / Verification
Verilog | Scripting| Research Skills | Simulation | Azure | Linux | Troubleshooting

**RTL Design Engineer / (FPGA/ASIC) Verification Engineer**

**Education:**

- **University of Houston, Houston, TX:** Master of Science in Computer and System Engineering **Anticipated May 2023**
- **Relevant Coursework:** Advanced Computer Architecture, VLSI Design, Hardware Verification, and Advanced Hardware Design
- **Govt. Model Engineering College, India:** Bachelor of Science in Electrical and Electrical Engineering **Aug 2020**
- **Relevant Coursework:** Digital System Design, Embedded system, Logic Circuit Design, Analog Integrated Circuits, and Microprocessors

**Certifications:**

- **System Verilog for Verification**, Covering Language Constructs, Functional Coverage, and Class-based verification, Maven Silicon
- **VLSI Design Methodologies,** Covering Verilog RTL coding, Digital Electronics, Quartus Prime, and ModelSim
- **Completed Python (Data Collection and Processing, Functions, Dictionaries, Files),** The University of Michigan, Coursera
- **Embedded Systems and Hardware Design,** SMEC Labs Kerala, India

**Technical Skills:**

- **OS:** Windows, Linux **| Abilities:** Electrical Engineering, Computer Engineering
- **Tools:** Intel Quartus Prime, Model Sim, Visual Code, GIT
- **Languages:** Verilog HDL, Python, Assembly code, System Verilog
- **Technologies:** Digital Design, FPGA, RTL Design, Hardware Design, IC Fabrication, ASIC design/ASIC verification, Test Bench Creation
- **Interpersonal Skills:** Strong Internet Research, Excellent Verbal, Written and Quantitative Skills, Time Management and Prioritization Abilities, Effective Presentation, Team Player, Leadership and Negotiation Skills

**Work Experience**

**IOT Intern| Infox Technologies, India** **June 2019 - July 2019**

- Controlled and operated 5+ IOT devices, including Arduino Uno, mastering the technical fundamentals of IOT.
- Gained in-depth working knowledge and hands-on experience in IOT-related technologies and fields.

**Others**

**Verification of Dual Port RAM using System Verilog Test bench Environment** **Jan 2023**

- Designed and verified 4096x64 Dual Port RAM by creating a test bench environment from scratch using System Verilog.
- Demonstrated expertise in ASIC design and verification methodologies, including functional coverage techniques.
- Implemented multiple interfaces, generator, drivers, monitors, reference models, and a scoreboard in the test bench Environment using advanced System Verilog coding techniques.

**RTL Design of Round Robin Arbiter** **Jan 2023**

- Designed a Round Robin Arbiter/Scheduler in Verilog with four request signals and four grant signals.
- Assigned a 4-clock cycle time slice to each request, ensuring efficient resource allocation.
- Guaranteed system stability by shifting the grant signal to other requests in the event of a request stopping within the allotted time.

**RTL Design of Voter Machine** **Dec 2022**

- Developed RTL design of a voting machine using Verilog that accepts input from buttons and casts votes.
- Validated the DUT's functionality using a test bench, achieving 100% coverage and ensuring proper device operation.
- Analyzed multiple signal flows and waveforms using Model Sim and synthesized the RTL design using Quartus Prime.

**Pipeline Implementation of a RISC Processor design** **Jan 2022**

- Devised and implemented a small subset of the MIPS32processor's instruction pipeline designs.
- Organized relevant instructions into micro-operations & segregated tasks into several pipeline stages with buffers to make a design.
- Implemented and took into account the case of pipeline hazards.
- Formulated and debugged a Test bench in Verilog ensuring 100%accuracy in results.

**Cache Test Bench Evaluation using SPEC2000 Benchmark** **Jan 2021**

- Evaluated performance and tradeoff analysis of results using bar graphs.3
- Tested 5 different standard processor SPEC2000 benchmarks, including MESA, GCC, GALGEL, etc.
- Assessed the effects of changing parameters like block size, associativity of blocks, and data and instruction cache size on a set of cache configurations, such as IPC and miss rate using the open-source software tool Simple Scalar.