VE370 Lab3 Report

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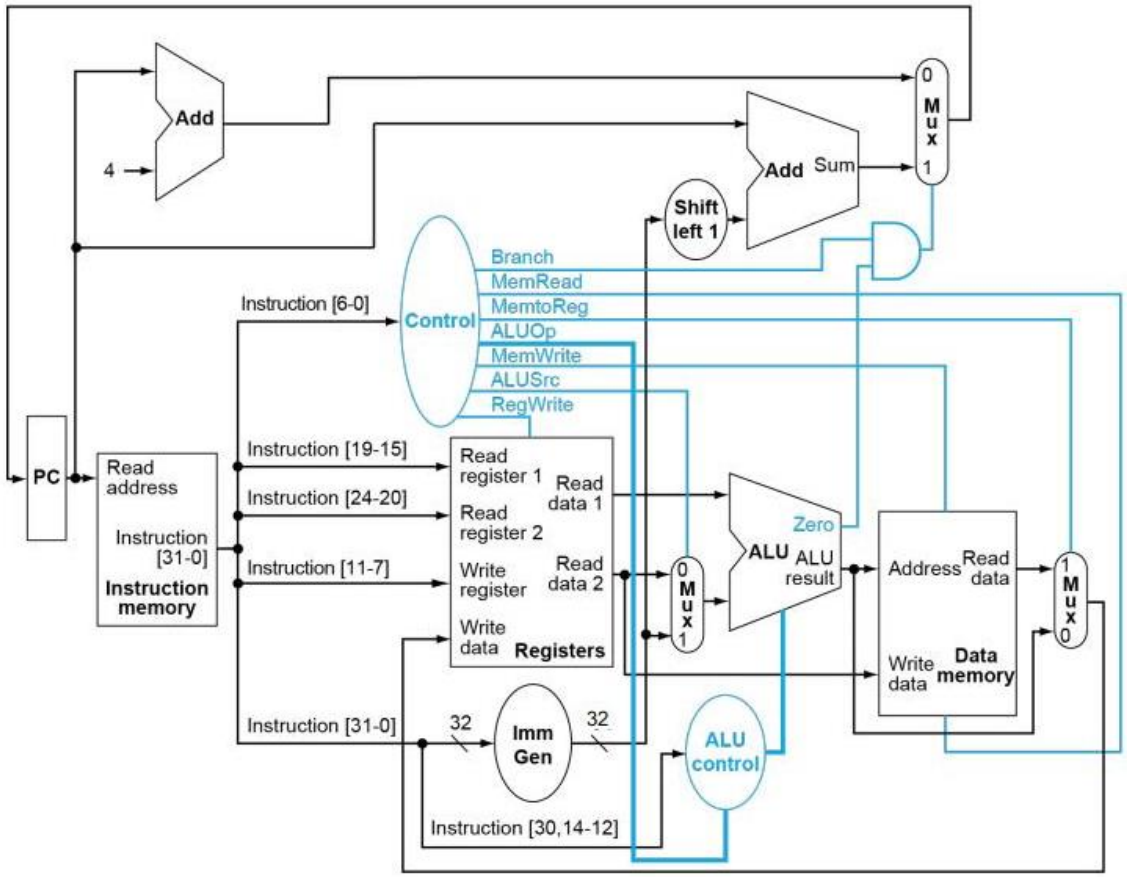
General Description

Firstly, my overall modeling and implementation of the processor is under the guidance of the picture below[[1]]:



Specifically, I have implemented RISC-V instructions including:

- The arithmetic-logical instructions add, addi, sub, and, and or
- The memory-reference instructions lw and sw
- The branch instructions beq and bne

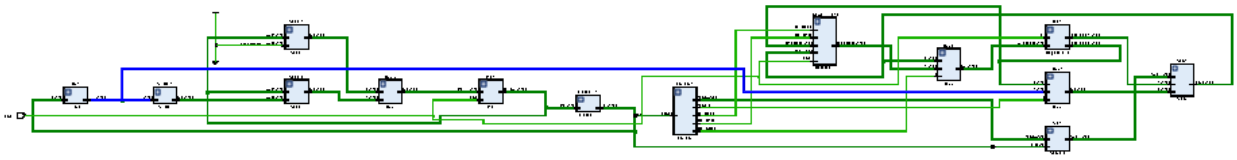
For control signals:

Instruction	RegWrite	ALUsrc	ALUop	Aluctrl	Branch	MemWrite	MemRead	MemtoReg
add	1	0	10	0010	0	0	0	0
addi	1	1	00	0010	0	0	0	0
sub	1	0	10	0110	0	0	0	0
and	1	0	10	0000	0	0	0	0
or	1	0	10	0001	0	0	0	0
lw	1	1	00	0010	0	0	1	1
sw	0	1	00	0010	0	1	0	0
beq	0	0	01	0110	1	0	0	0

Instruction	RegWrite	ALUsrc	ALUop	Aluctrl	Branch	MemWrite	MemRead	MemtoReg
bne	0	0	01	0111	1	0	0	0

RTL schematic of my Verilog model

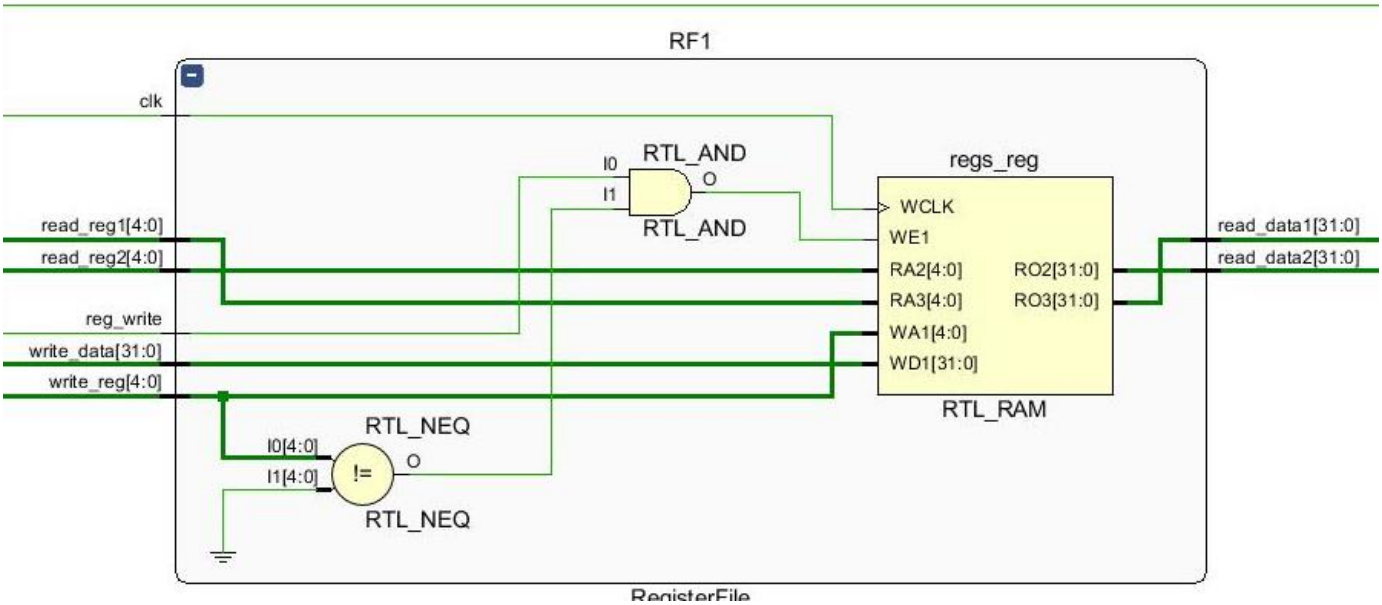
This is my RTL schematic of Verilog model generated with Xilinx Vivado software:[[2]]



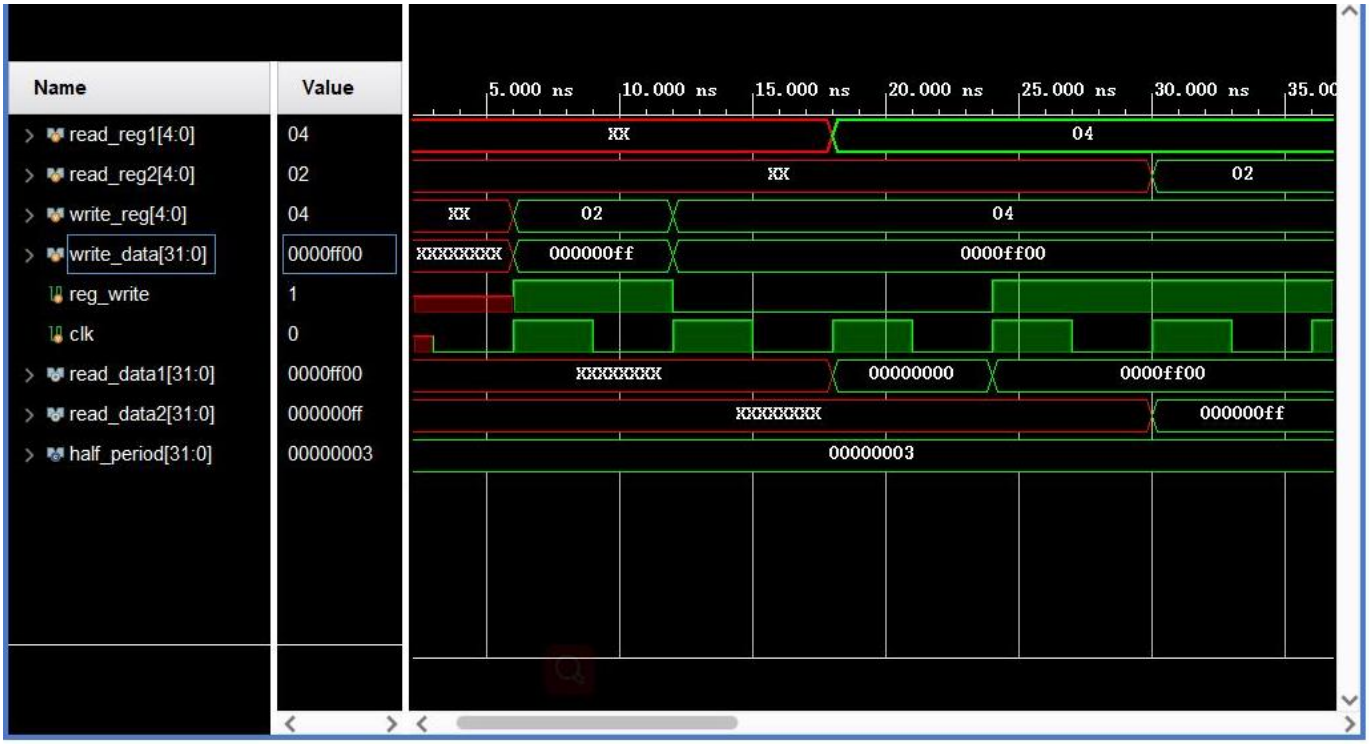
Simulations

Register File

The detailed design:

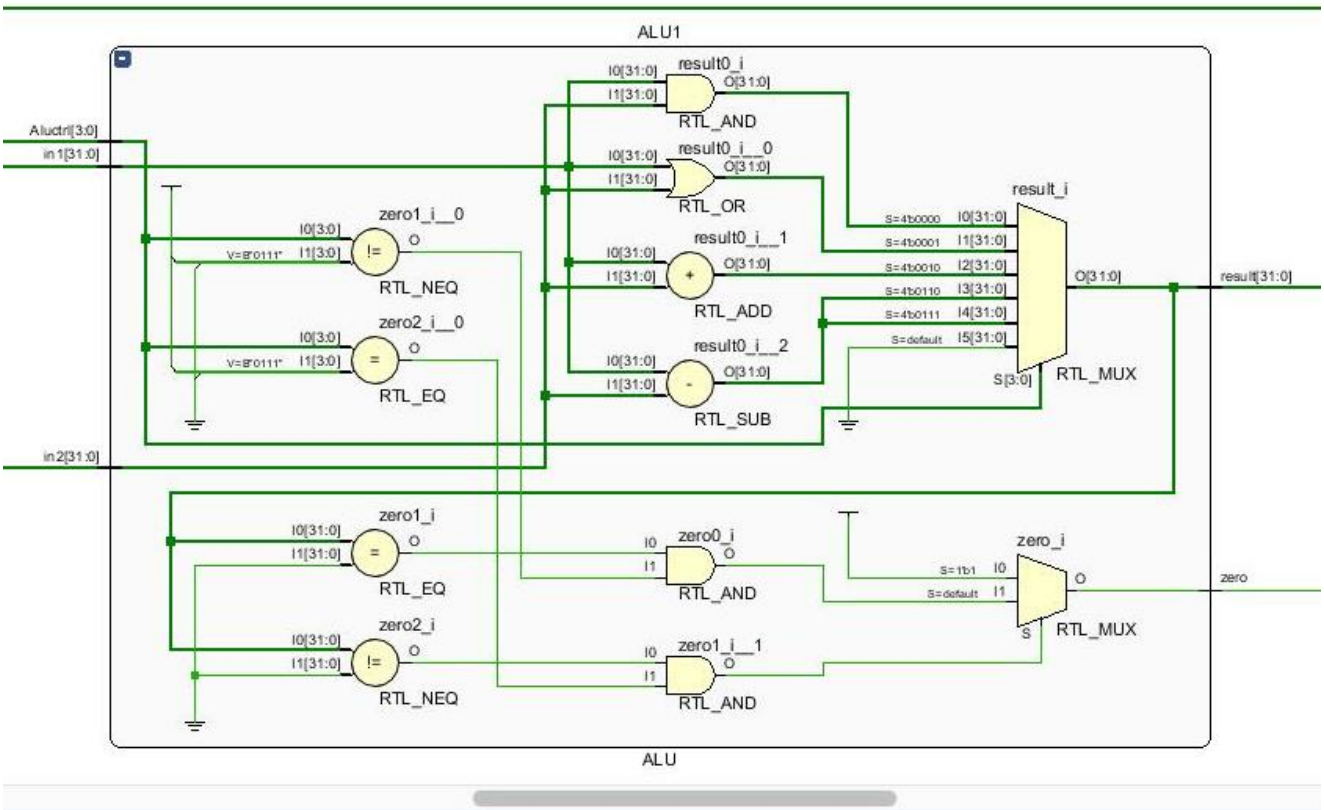


Simulation result:

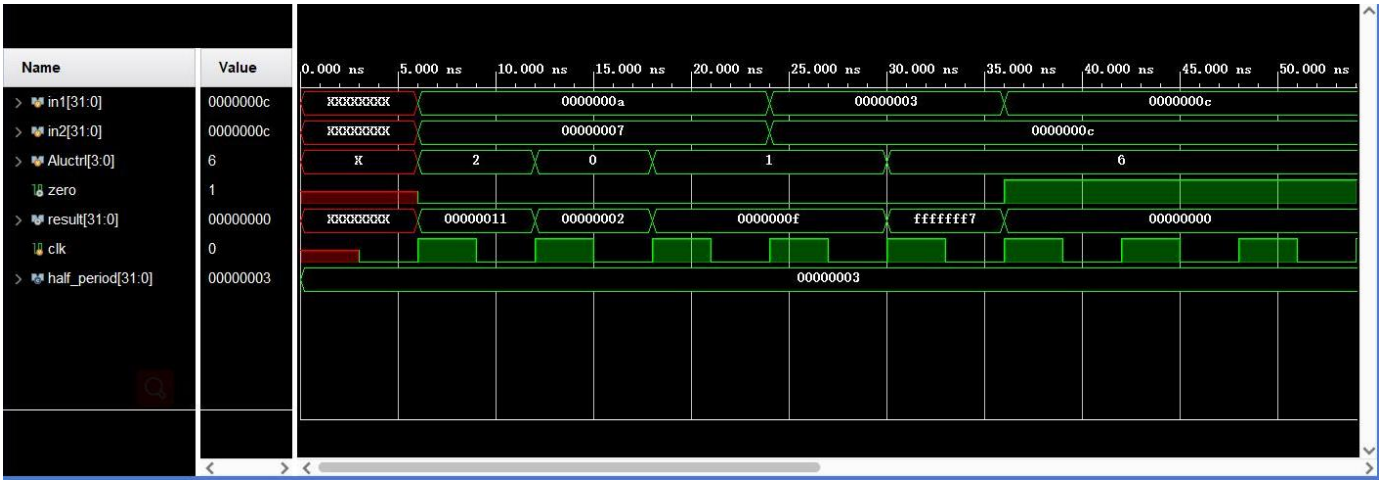


32-bit ALU

The detailed design:

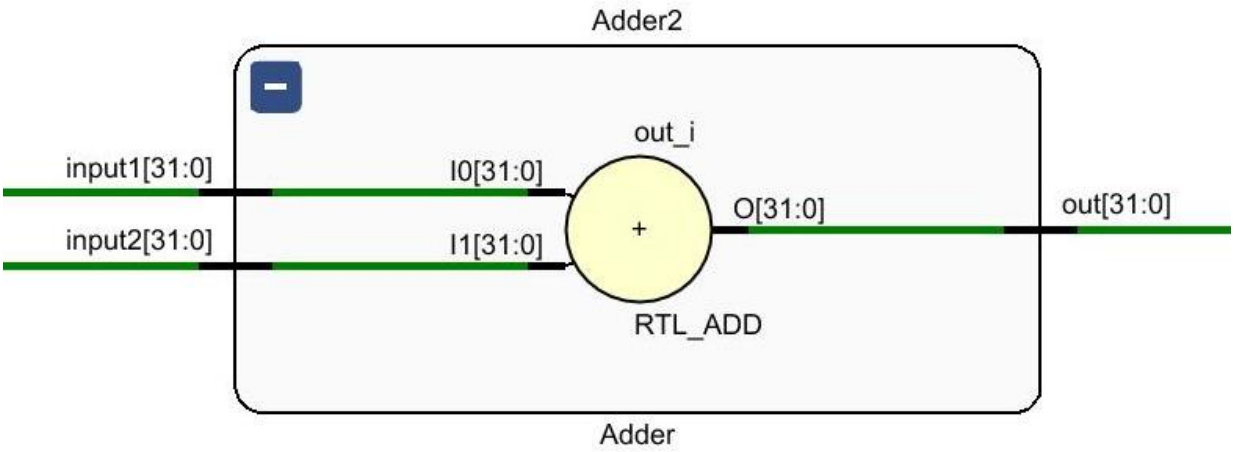


Simulation result:

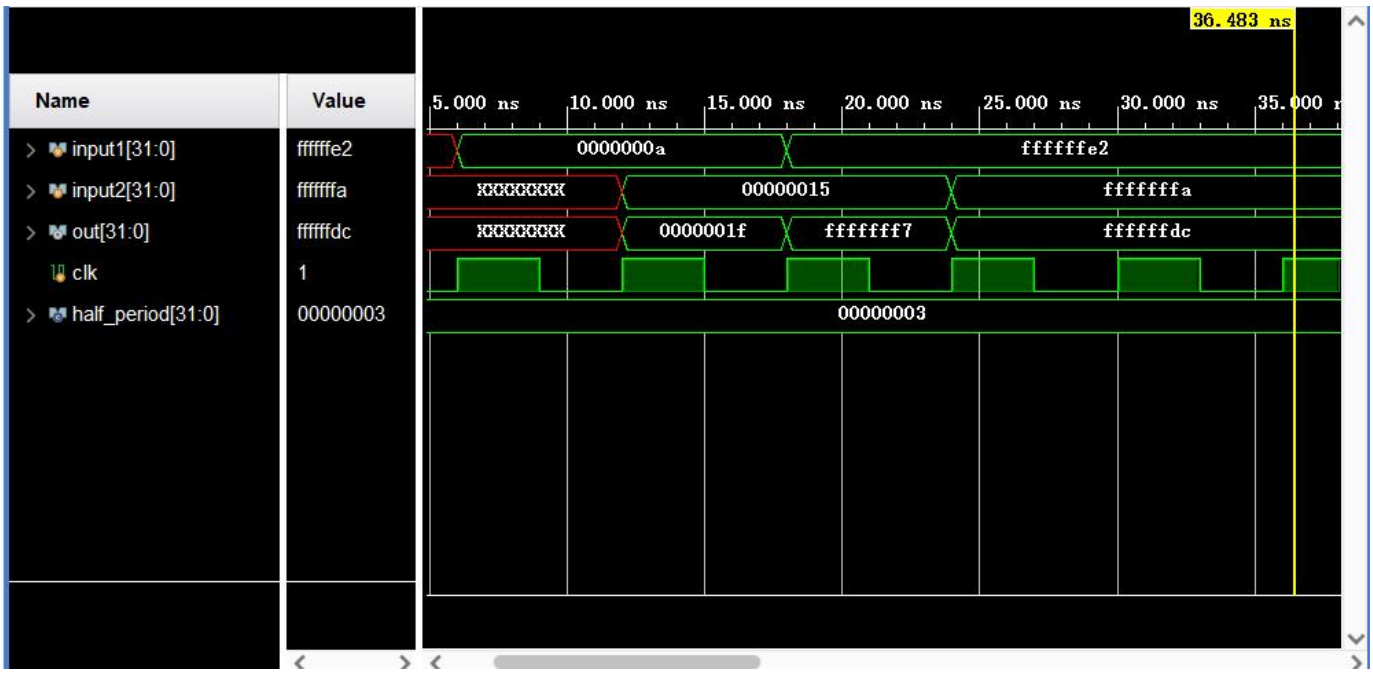


32-bit Adder

The detailed design:

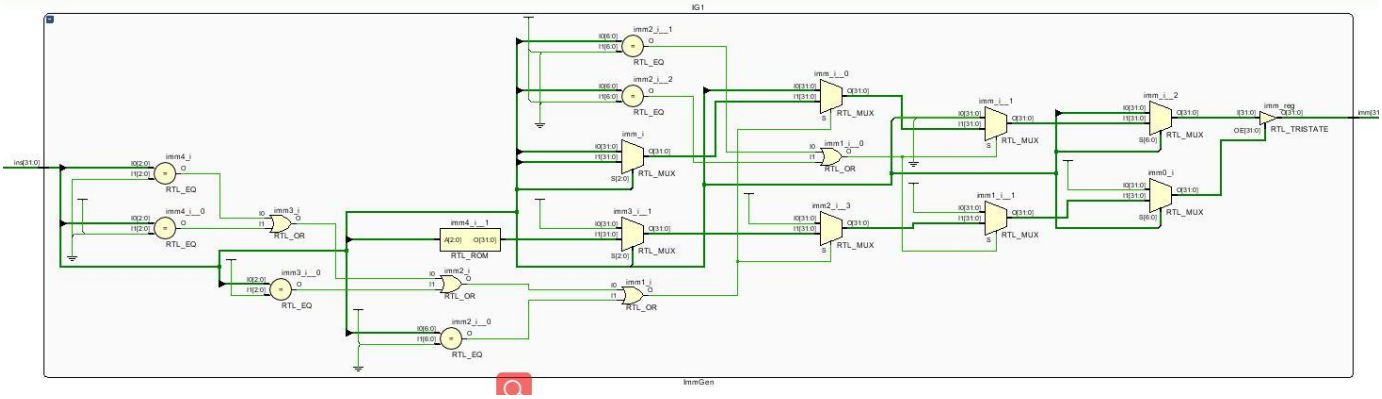


Simulation result:

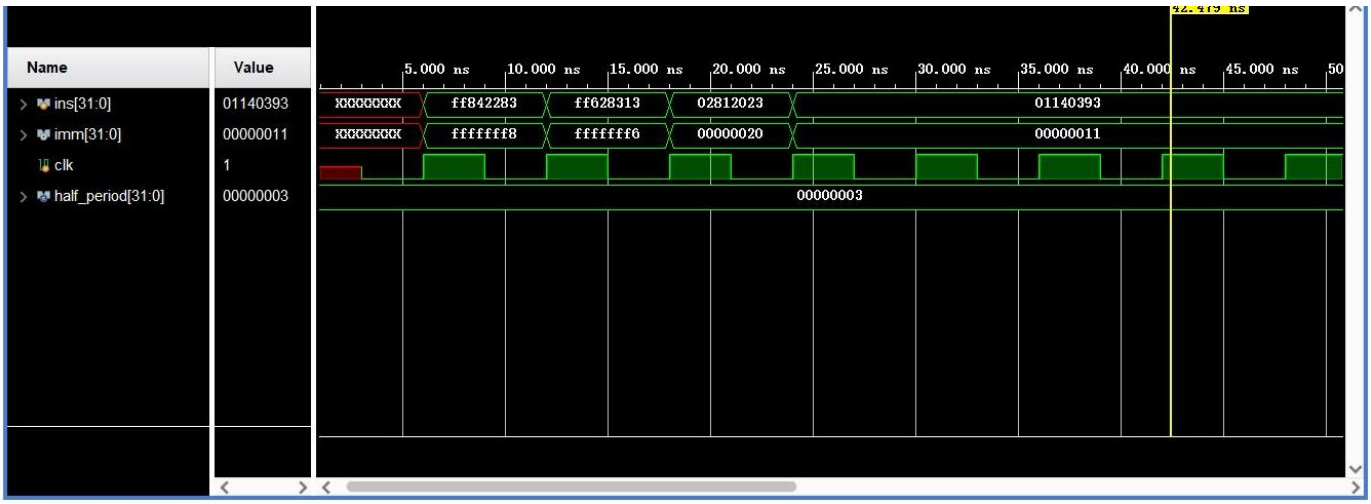


Immediate Generator

The detailed design:

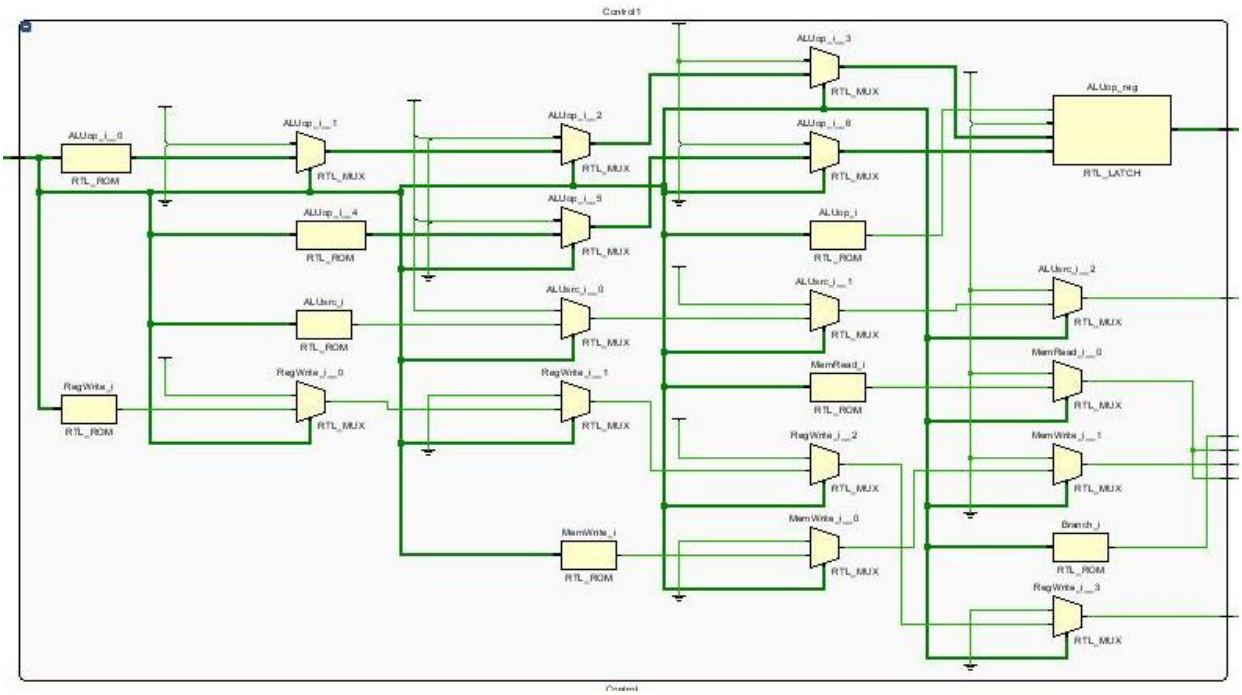


Simulation result:

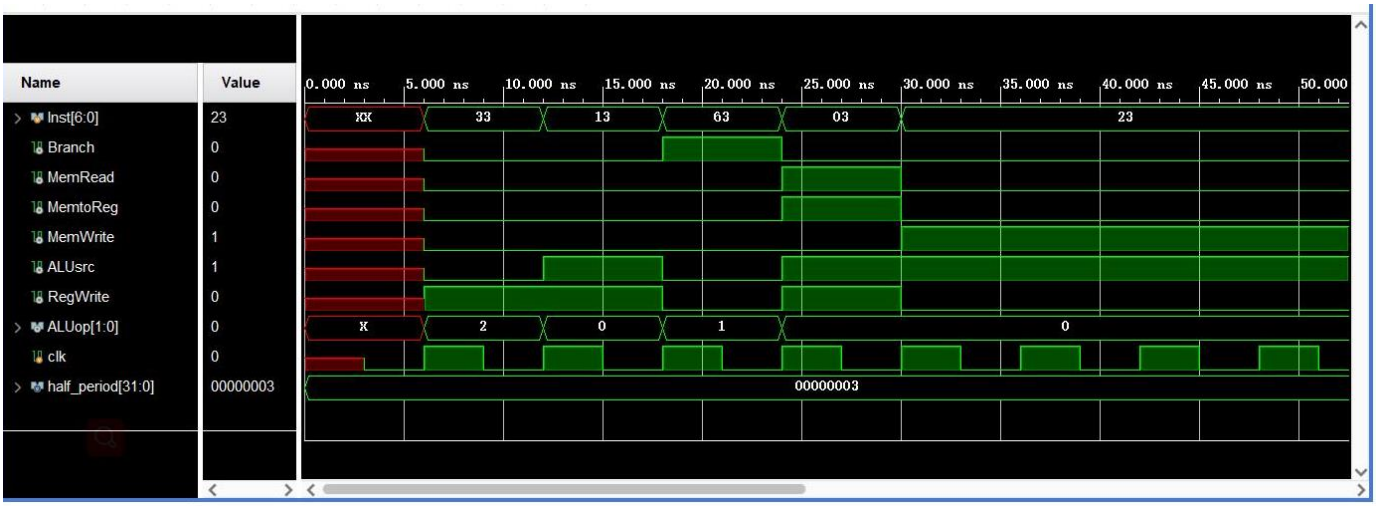


Control Unit

The detailed design:

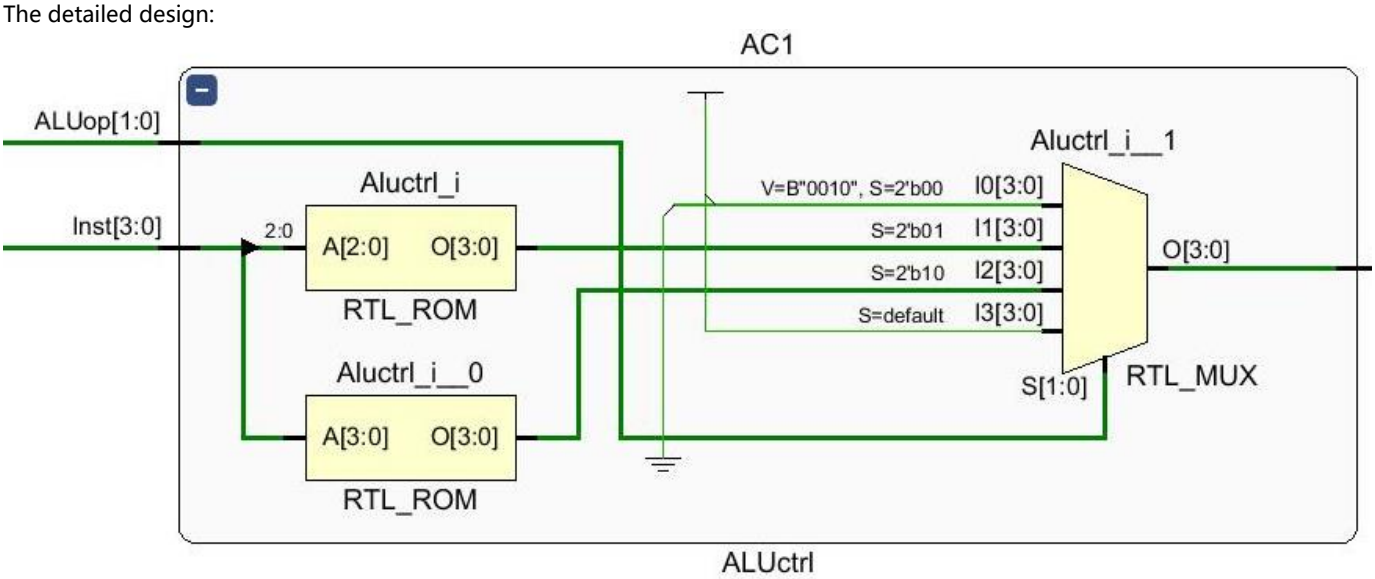


Simulation result:

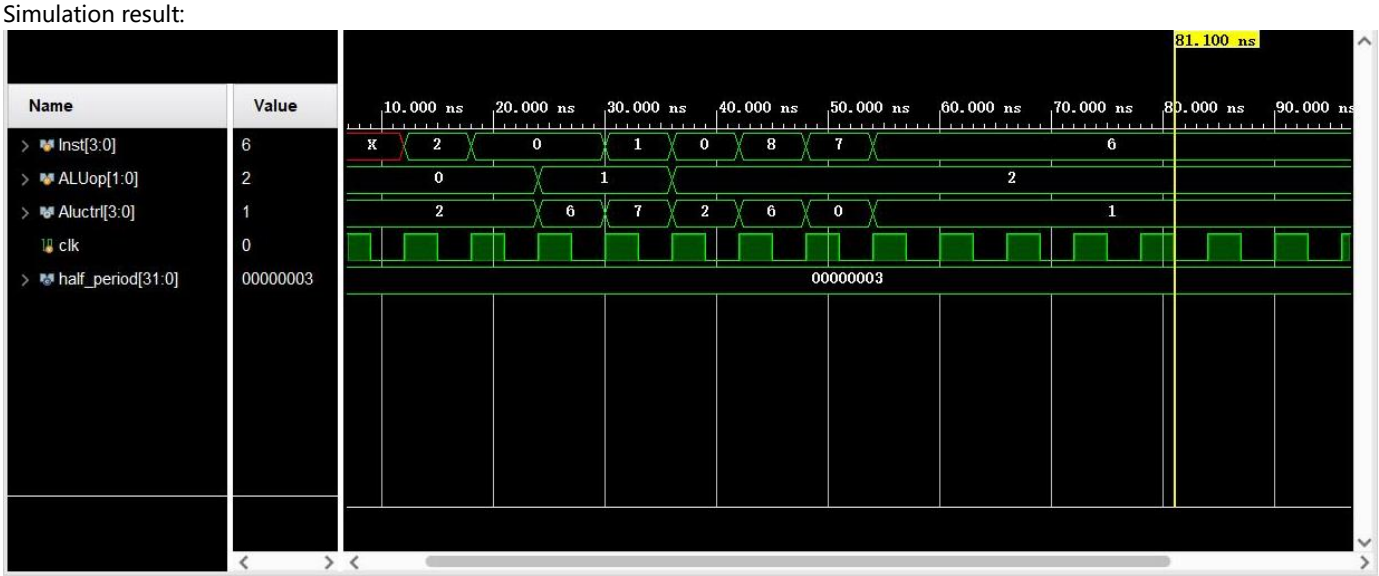


ALU control

The detailed design:

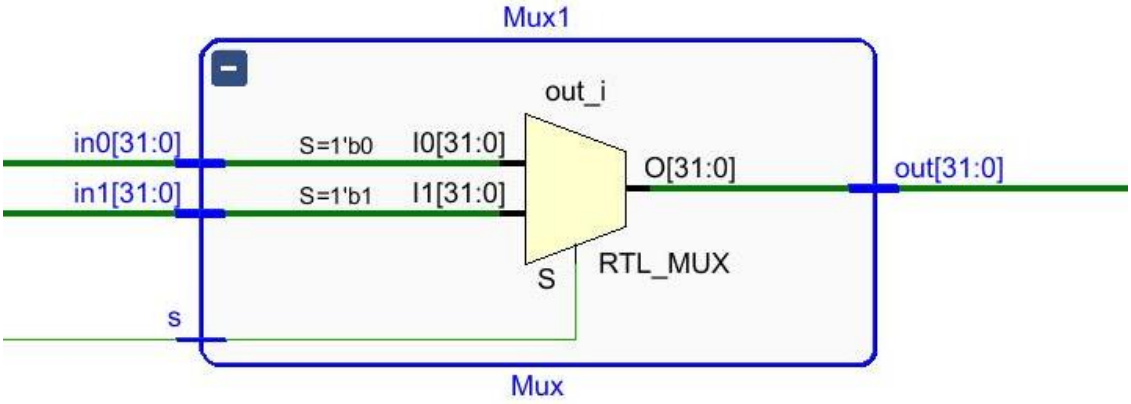


Simulation result:



2-to-1 MUX

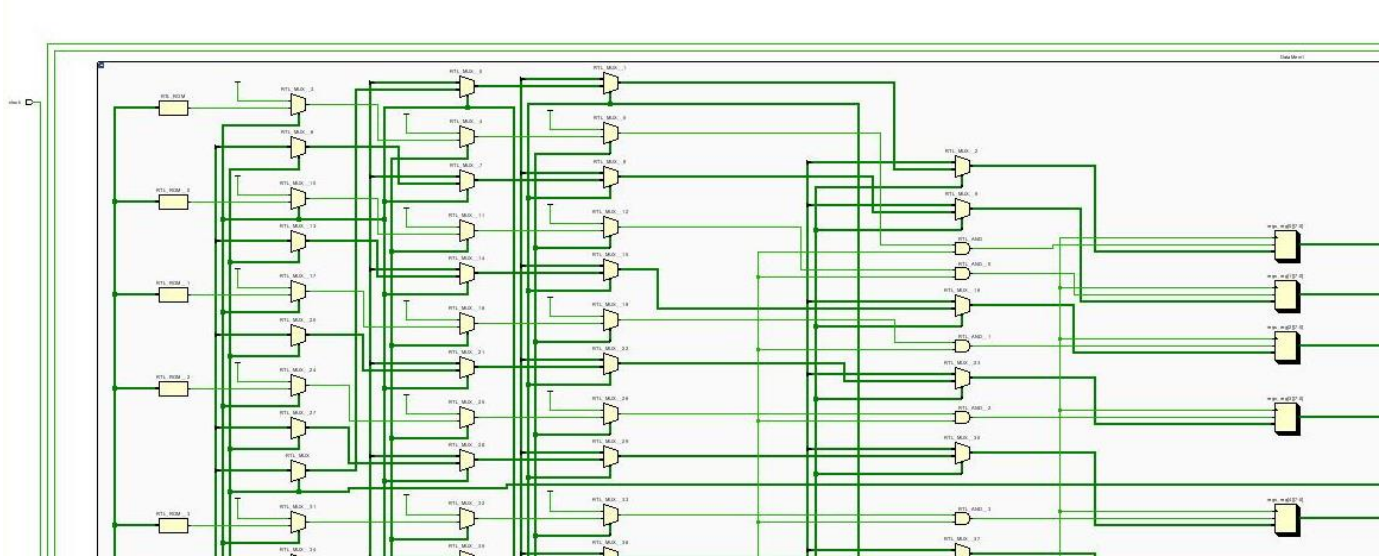
The detailed design:



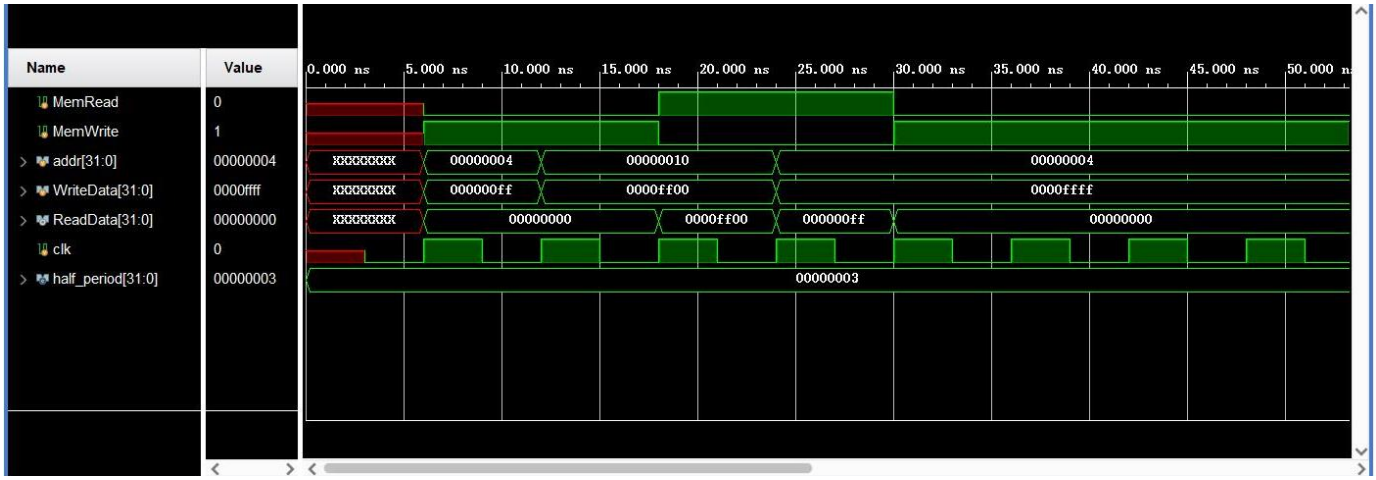
Simulation result:

Data Memory

Part of the detailed design(the whole schematic is too large):



Simulation result:



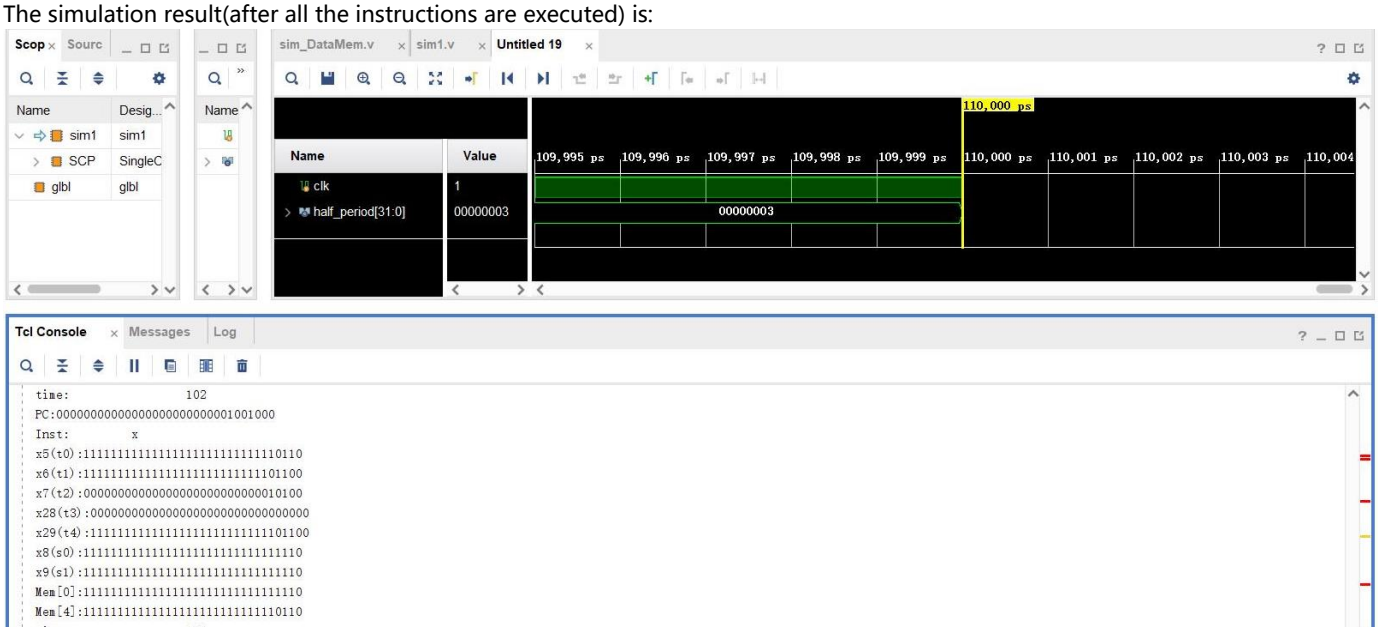
Simulation Results for Test Instructions

A testcase of instructions are given: (with analysis and wanted answers)

```
        addi t0 x0 -10 #t0=-10
        add t1 t0 t0 #t1=-20
        sub t2 t0 t1 #t2=10
        and t3 t1 x0 #No change
        or t4 t1 t0 #t4=-2
        sw t4 0(x0) #Mem[0]=-2
        sw t0 4(x0) #Mem[4]=-10
        beq t0 x0 L1 #No change
        add t4 t1 x0 #t4=-20
L1:     bne t1 t4 error1 #No change
        bne t1 t3 L2 #No change, go to L2
error1: add t2 x0 x0
L2:     lw s0 0(x0) #s0=-2
        lw s1 4(x0) #s1=-10
        addi s1 s1 8 #s1=-2
        beq s0 s1 L3 #No change, go to L3
error2: add t2 x0 x0
L3:     add t2 t2 t2 #t2=20
```

Note that in this test cases

The simulation result(after all the instructions are executed) is:



We can see that after executing all the instructions, t0=-10, t1=-20, t2=20, t3=0, t4=-20, s0=-2, s1=-2, Mem[0]=-2, Mem[4]=-10. All the corresponding components work as expected.

For detailed verification, all the outputs in the vivado window are as follows, and they correspond to the wanted answers:

```
time:                   6
PC:00000000000000000000000000000000
Inst:4284482195
x5(t0):00000000000000000000000000000000
x6(t1):00000000000000000000000000000000
x7(t2):00000000000000000000000000000000
x28(t3):00000000000000000000000000000000
x29(t4):00000000000000000000000000000000
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:00000000000000000000000000000000
Mem[4]:00000000000000000000000000000000
time:                  12
PC:00000000000000000000000000000100
Inst:   5407539
x5(t0):11111111111111111111111111110110
x6(t1):00000000000000000000000000000000
x7(t2):00000000000000000000000000000000
x28(t3):00000000000000000000000000000000
x29(t4):00000000000000000000000000000000
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:00000000000000000000000000000000
Mem[4]:00000000000000000000000000000000
time:                  18
PC:00000000000000000000000000001000
Inst:1080198067
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000000000
x28(t3):00000000000000000000000000000000
x29(t4):00000000000000000000000000000000
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:00000000000000000000000000000000
Mem[4]:00000000000000000000000000000000
time:                  24
PC:00000000000000000000000000001100
Inst:    228915
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):00000000000000000000000000000000
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:00000000000000000000000000000000
Mem[4]:00000000000000000000000000000000
time:                  30
PC:00000000000000000000000000010000
Inst:   5467827
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):00000000000000000000000000000000
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:00000000000000000000000000000000
Mem[4]:00000000000000000000000000000000
time:                  36
PC:00000000000000000000000000010100
Inst:  30416931
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111111110
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:00000000000000000000000000000000
Mem[4]:00000000000000000000000000000000
time:                  42
PC:00000000000000000000000000011000
Inst:   5251619
x5(t0):11111111111111111111111111110110
```

```
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111111110
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:11111111111111111111111111111110
Mem[4]:00000000000000000000000000000000
time:                   48
PC:00000000000000000000000000011100
Inst:    164963
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111111110
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
time:                   54
PC:00000000000000000000000000100000
Inst:    200371
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111111110
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
time:                   60
PC:00000000000000000000000000100100
Inst:  30610531
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111101100
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
time:                   66
PC:00000000000000000000000000101000
Inst:  29561955
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111101100
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
time:                   72
PC:00000000000000000000000000110000
Inst:      9219
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111101100
x8(s0):00000000000000000000000000000000
x9(s1):00000000000000000000000000000000
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
time:                   78
PC:00000000000000000000000000110100
Inst:   4203651
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111101100
x8(s0):11111111111111111111111111111110
```

```
x9(s1):00000000000000000000000000000000
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
time:                   84
PC:00000000000000000000000000111000
Inst:   8684691
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111101100
x8(s0):11111111111111111111111111111110
x9(s1):11111111111111111111111111110110
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
time:                   90
PC:00000000000000000000000000111100
Inst:   9700451
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111101100
x8(s0):11111111111111111111111111111110
x9(s1):11111111111111111111111111110110
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
time:                   96
PC:00000000000000000000000001000100
Inst:   7570355
x5(t0):11111111111111111111111111110110
x6(t1):11111111111111111111111111101100
x7(t2):00000000000000000000000000001010
x28(t3):00000000000000000000000000000000
x29(t4):11111111111111111111111111101100
x8(s0):11111111111111111111111111111110
x9(s1):11111111111111111111111111110110
Mem[0]:11111111111111111111111111111110
Mem[4]:11111111111111111111111111110110
```

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1. This picture is taken from VE370 T5 slides ↩
2. For a clear version, see schematic.pdf in source file. ↩