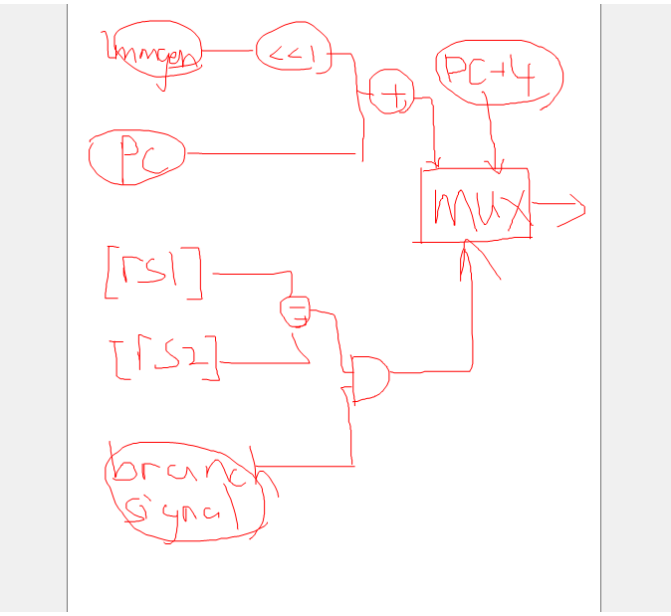
Final RC Answer

Stall

1. Normally, `beq` need **3** nops behind if the **branch decision unit (“and” logic gate)** is in MEM
2. Move from MEM to ID, we only need 1 nops.
3. What do we add?



Assume branch not taken

▼ **Exercise.** Write the condition of “IF.Flush = 1”.

Ans: “branch==1” for stall; “branch==1 && “=”output==1” for assume not

▼ **Exercise.** Write the condition of “PC = PC + 4” if `beq` detected in ID stage.

Ans: “branch==0 || “=”output≠1” for assume not; never for stall

Relevant Issues

1. performance

Exercise. If we want to support `jalr` instruction in pipeline, we identify it in ID stage. However, we can choose to put calculation unit in EX stage, or move it to ID stage. Which stage is definitely longer? Which stage could be longer? Which one is better?

Ans: WB; EX or ID; Hard to say.

2. If only one → forwarding path See P19

   Forward1 = 1, when

   1. branch in ID
   2. data in MEM
   3. MEM.rd == ID.rs1/2
   4. MEM.RegWrite == 1

Exercise. How many instructions should be in between `lw x4 ...` and `beq x4 ...` ? What forwarding path should be used when there is not enough instructions in between?

Ans: 2. No forwarding path, just delays.

Exercise. How to add stall in a current time stage diagram? HW6Q3

Ans: push everything below right.

Exercise. Draw the FSM for 2-bit predictor.

Ans:

Exercise. Use the example below to explain why 2-bit predictor is better than 1-bit.

Ans: Inner loop. 1-bit: first and last iteration.

Exercise. Is 2-bit predictor always better than 1-bit? If so, prove it, if not make a counter example.

Ans. T T T F F F