ECE3700J Mid RC
Data Hazard

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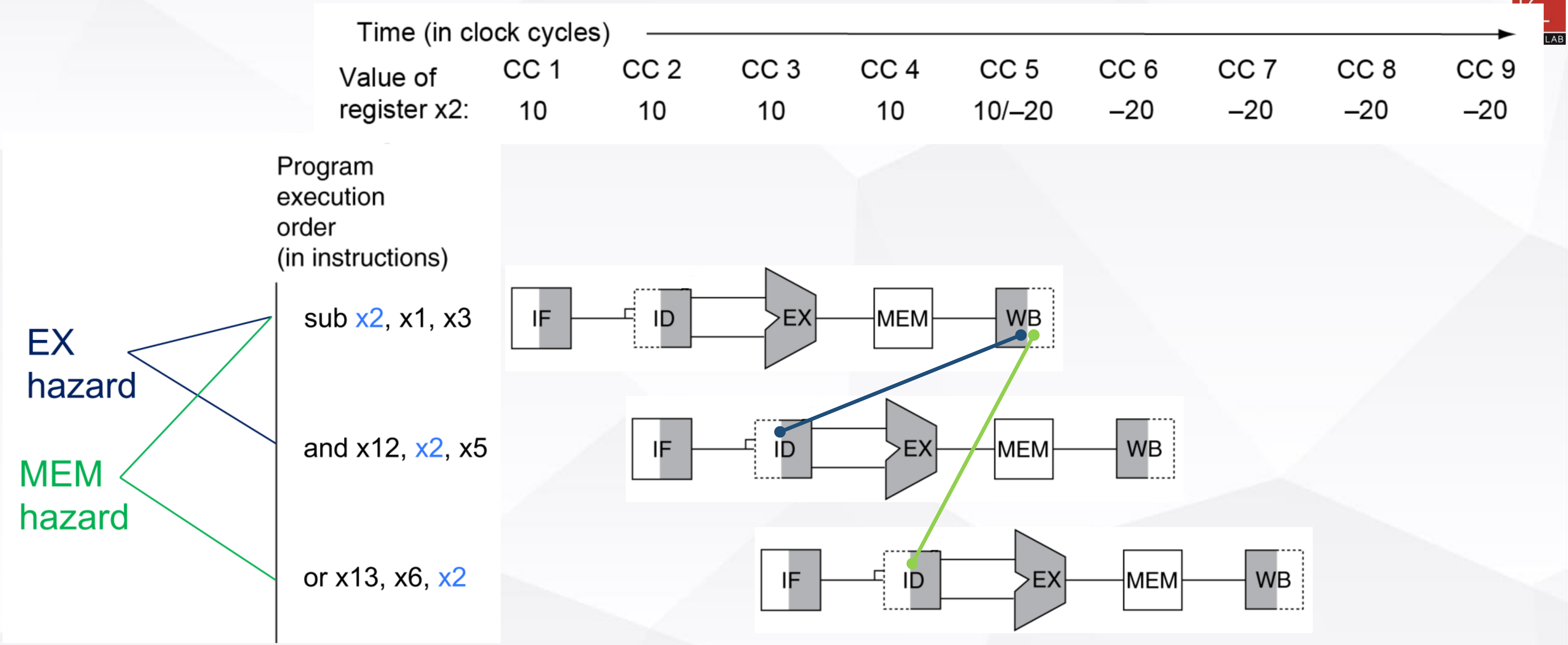
Data Hazard in ALU Instructions



Time (in clock cycles)

	CC 1	CC 2	CC 3	CC 4	CC 5	CC 6	CC 7	CC 8	CC 9
Value of register x2:	10	10	10	10	10/–20	–20	–20	–20	–20

Program execution order (in instructions)

sub x2, x1, x3

and x12, x2, x5

or x13, x6, x2

EX hazard

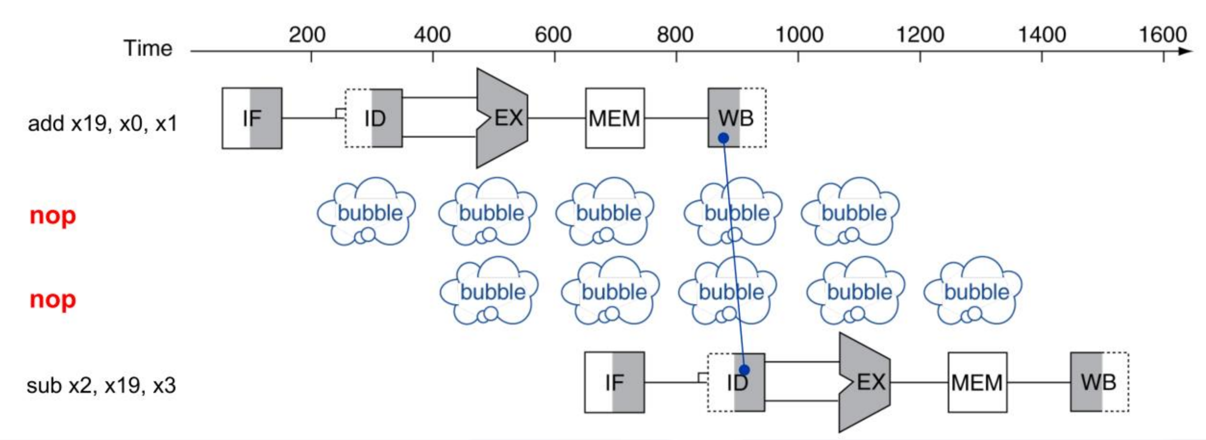
MEM hazard

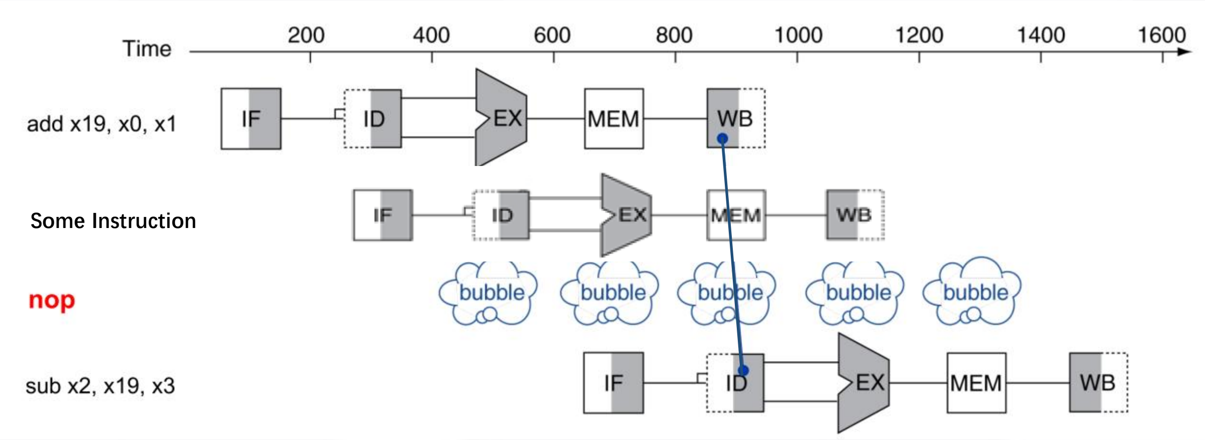
Solution with adding NOP/Stall

```
nop   # no operation, pseudo-instruction
      # addi x0, x0, 0
```

EX Hazard: +2 NOP

MEM Hazard: +1 NOP

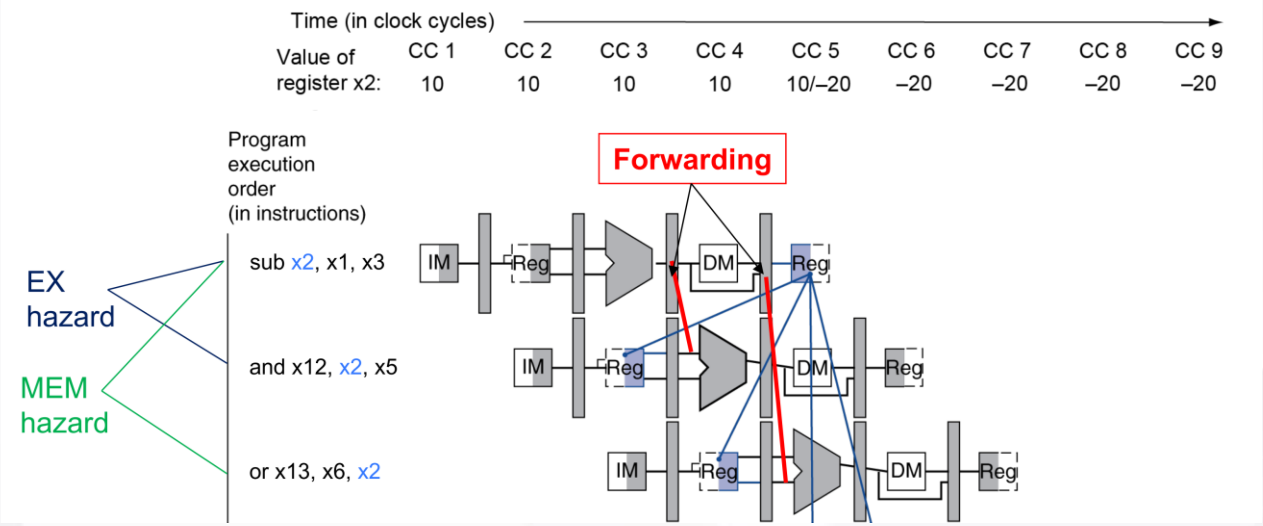




Solution with forwarding

Forwarding Unit

Forwarding Scheme



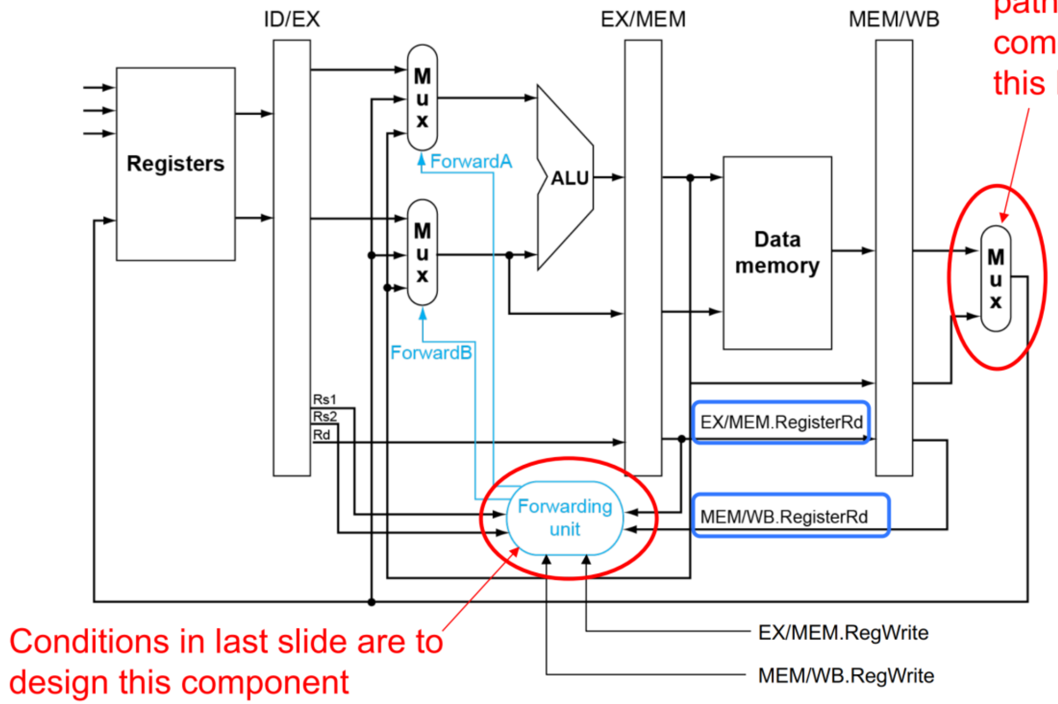
Time (in clock cycles)

Value of register x2:	CC 1	CC 2	CC 3	CC 4	CC 5	CC 6	CC 7	CC 8	CC 9
	10	10	10	10	10/–20	–20	–20	–20	–20

Forwarding Paths

Forwarding Unit in **EX** stage

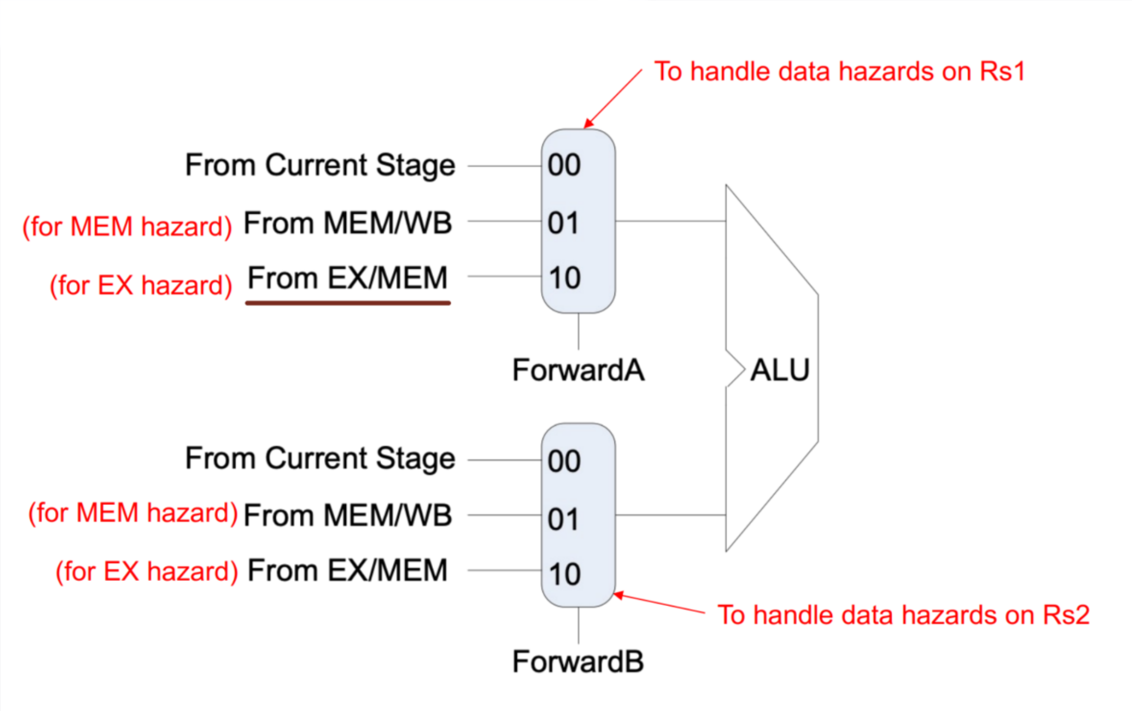
MEM/WB forwarding path actually comes from this MUX



Conditions in last slide are to design this component

Solution with forwarding

Forwarding detection and MUXes



To handle data hazards on Rs1

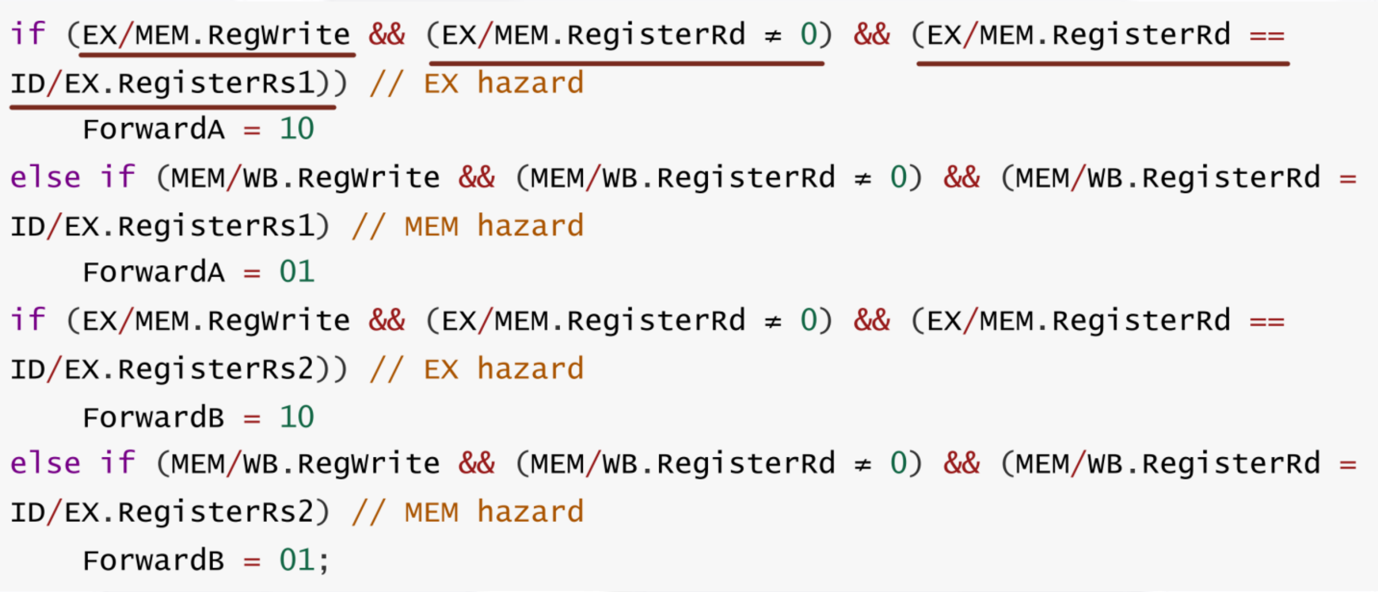
(for MEM hazard)

(for EX hazard)

(for MEM hazard)

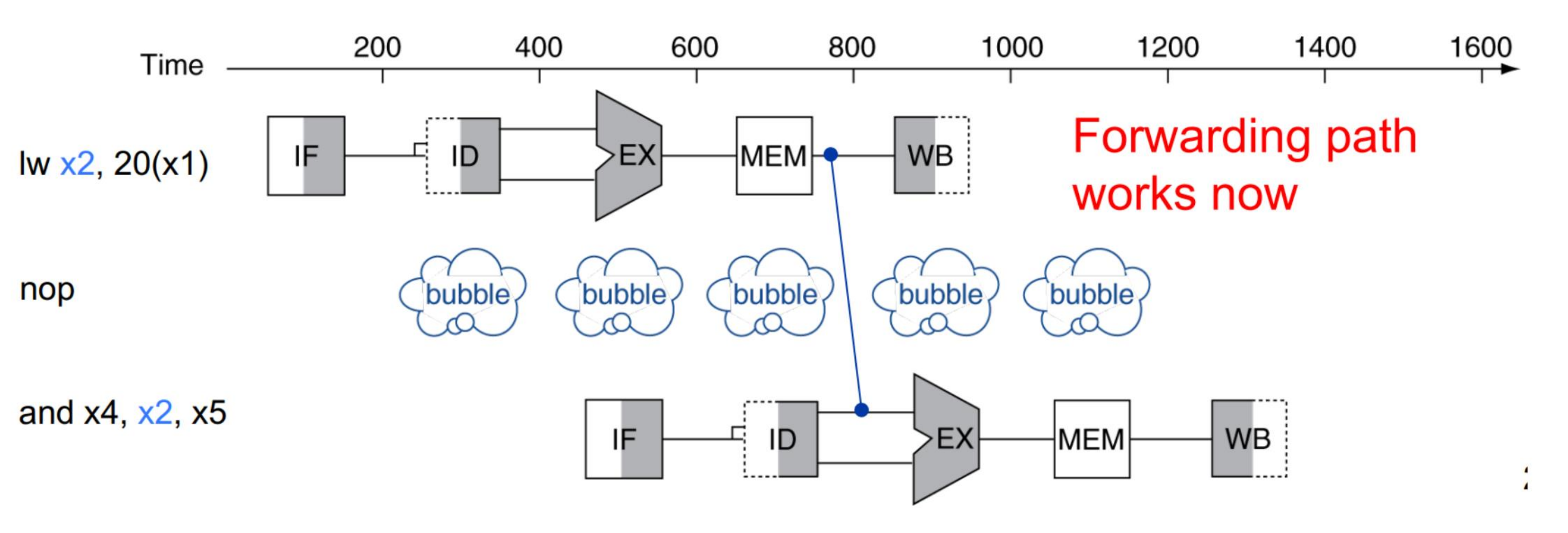
(for EX hazard)

To handle data hazards on Rs2



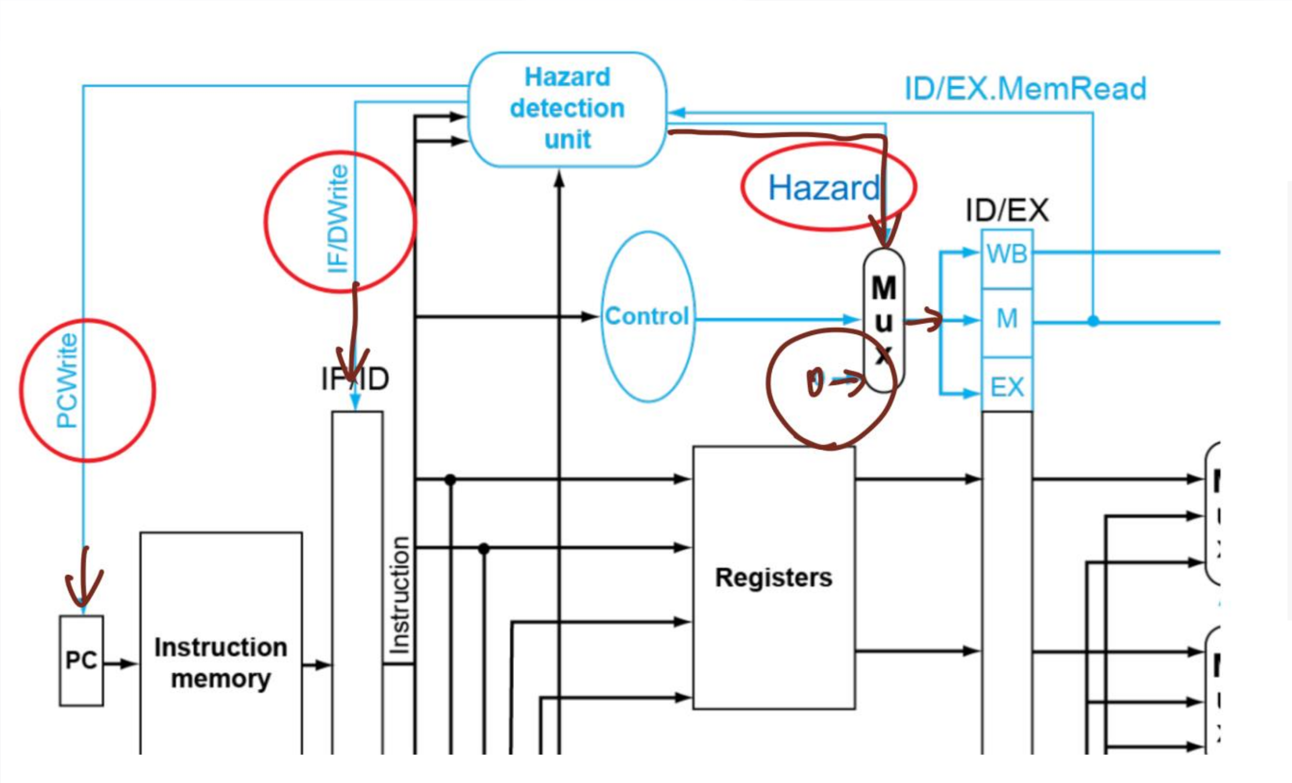
```
if (EX/MEM.RegWrite && (EX/MEM.RegisterRd ≠ 0) && (EX/MEM.RegisterRd ==
ID/EX.RegisterRs1)) // EX hazard
    ForwardA = 10
else if (MEM/WB.RegWrite && (MEM/WB.RegisterRd ≠ 0) && (MEM/WB.RegisterRd =
ID/EX.RegisterRs1) // MEM hazard
    ForwardA = 01
if (EX/MEM.RegWrite && (EX/MEM.RegisterRd ≠ 0) && (EX/MEM.RegisterRd ==
ID/EX.RegisterRs2)) // EX hazard
    ForwardB = 10
else if (MEM/WB.RegWrite && (MEM/WB.RegisterRd ≠ 0) && (MEM/WB.RegisterRd =
ID/EX.RegisterRs2) // MEM hazard
    ForwardB = 01;
```

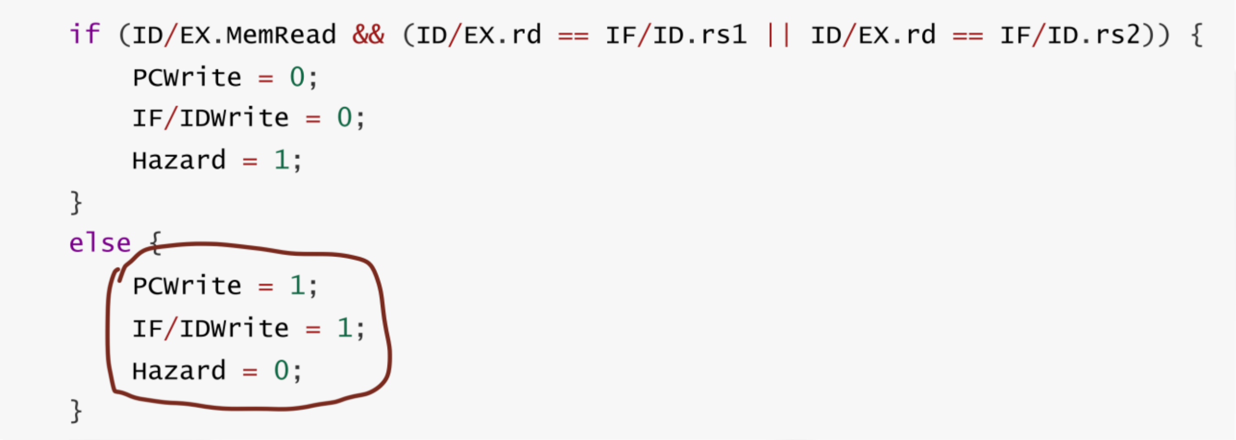
Load-use Data Hazard



Forwarding path works now

Load-use Data Hazard





```
if (ID/EX.MemRead && (ID/EX.rd == IF/ID.rs1 || ID/EX.rd == IF/ID.rs2)) {
    PCWrite = 0;
    IF/IDWrite = 0;
    Hazard = 1;
}
else {
    PCWrite = 1;
    IF/IDWrite = 1;
    Hazard = 0;
}
```

Very Important !!! (Slide 31-37)

CC1

PC Write	IF/ID Write	Hazard	ID/EX. MemRead	IF/ID .Rs1	IF/ID .Rs2	ID/EX. Rd
1	1	x	x	x	x	x

lw x2, 20(x1)

CC2

PC Write	IF/ID Write	Hazard	ID/EX. MemRead	IF/ID. Rs1	IF/ID. Rs2	ID/EX. Rd
1	1	x	x	1	20	x

and x4,x2,x5   lw x2, 20(x1)

CC3

PC Write	IF/ID Write	Hazard	ID/EX. MemRead	IF/ID. Rs1	IF/ID. Rs2	ID/EX. Rd
0	0	1	1	2	5	2

or x8,x2,x6   and x4,x2,x5   lw x2, 20(x1)

CC4

PC Write	IF/ID Write	Hazard	ID/EX. MemRead	IF/ID. Rs1	IF/ID. Rs2
1	1	0	0	2	5

or x8,x2,x6   and x4,x2,x5   nop (and)   lw x2, 20(x1)

CC4

ID/EX.Rs1	ID/EX.Rs2	ID/EX.Rd	EX/MEM.Rd	MEM/WB.Rd
2	5	4	2	x

EX/MEM.RegWrite	MEM/WB.RegWrite	ForwardA	ForwardB
1	x	10	00

or x8,x2,x6   and x4,x2,x5   nop (and)   lw x2, 20(x1)

Fake EX hazard

CC5

PC Write	IF/ID Write	Hazard	EX/MEM. MemRead	EX/MEM. MemWrite
1	1	0	0	0

No effective operation

add x9,x4,x2   or x8,x2,x6   and x4,x2,x5   nop (and)   lw x2, 20(x1)

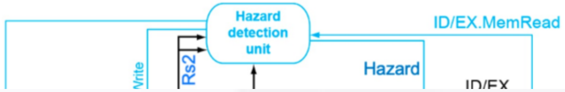
CC5

ID/EX.Rs1	ID/EX.Rs2	ID/EX.Rd	EX/MEM.Rd	MEM/WB.Rd
2	5	4	4	2

EX/MEM.RegWrite	MEM/WB.RegWrite	ForwardA	ForwardB
0	1	01	00

add x9,x4,x2   or x8,x2,x6   and x4,x2,x5   nop   lw x2, 20(x1)

MEM Hazard



TIPS

- Slide and homework are VERY Important!
- Understand how processor functions at different stages (Your Vivado Labs can help you well)
- Be careful

TIPS

Thank You and Good Luck :D