JOINT INSTITUTE
交大密西根学院

ECE3700J Introduction to Computer Organization

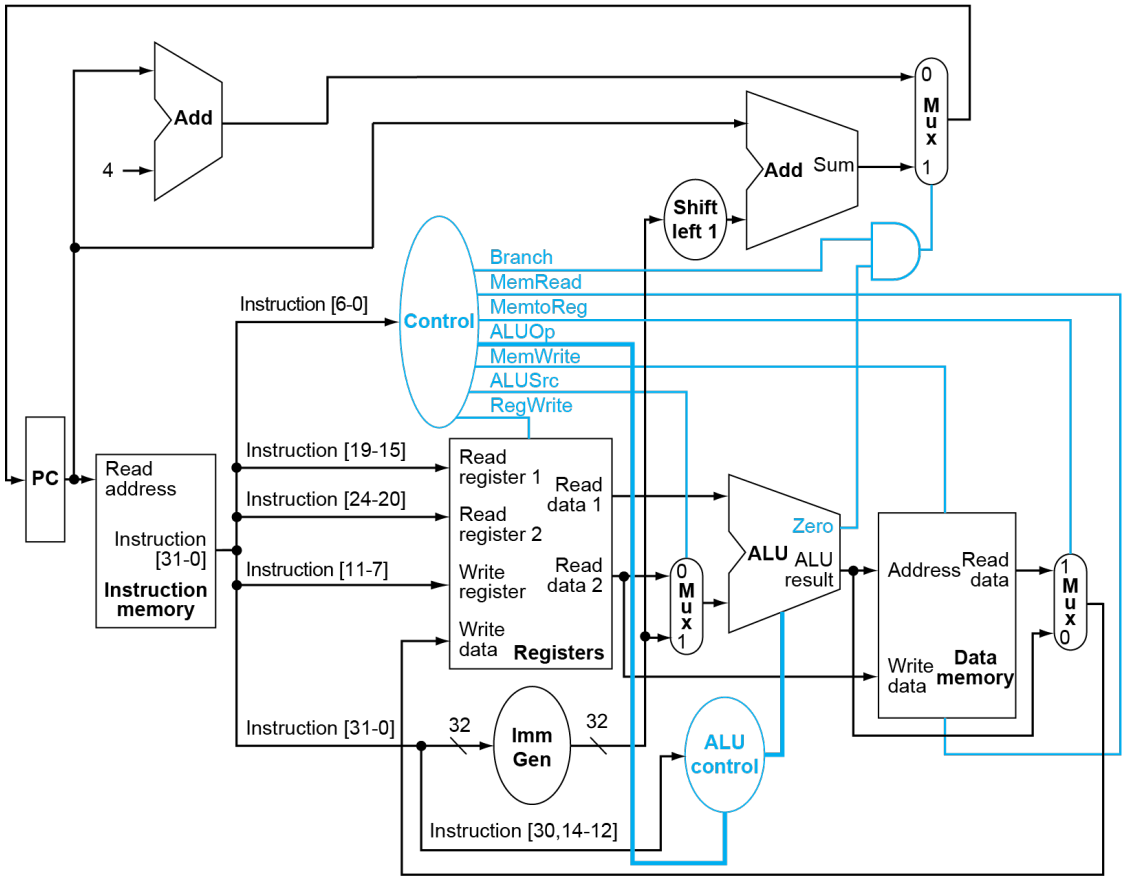
Homework 3

Assigned: October 10, 2023

Due: 2:00pm on October 17, 2023

Submit a PDF file on Canvas

Following questions refer to the figure below.



1. (30 points) Given RISC-V assembly instruction sequence:

```
Loop:
      slli x10, x22, 2
      add  x10, x10, x25
      lw   x9, 0(x10)
      bne  x9, x24, Exit
      addi x22, x22, 1
      beq  x0, x0, Loop
Exit: …
```

Assuming the memory location of the first instruction (`slli`) is 0x1000F400, what are the values of the control signals in the table when each of the instructions is executed?

Ctrl Signals / Instruction	Branch	MemRead	MemtoReg	ALUOp	MemWrite	ALUSrc	RegWrite	Zero	PC	ImmGen Output
`add`										
`lw`										
`beq`										

2. (20 points) When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get "broken" and always read a logical 0 or logical 1. These are often called a "stuck-at-0" fault or "stuck-at-1" fault, respectively.
   (1) Which instructions fail to operate correctly if the MemtoReg wire is stuck-at-0? (5 points)
   (2) Which instructions fail to operate correctly if the ALUSrc wire is stuck-at-0? (5 points)
   (3) Which instructions fail to operate correctly if the MemRead wire is stuck-at-1? (5 points)
   (4) Which instructions fail to operate correctly if the RegWrite wire is stuck-at-1? (5 points)

NOTE: the following problems are optional and won't be graded.

3. Given following assembly instruction:
   `sw rs2, imm12(rs1)`

   (1) Which resources (blocks) perform a useful function for this instruction? (3 points)
   (2) Which resources (blocks) produce no output for this instruction? Which resources produce output that is not used? (7 points)

4. Consider the following instruction mix:

R-type	**I-type (non-load)**	**Load**	**Store**	**Branch**	**Jump**
30%	18%	25%	15%	10%	2%

   (1) What fraction of all instructions use data memory? (3 points)
   (2) What fraction of all instructions use instruction memory? (2 points)
   (3) What fraction of all instructions use the sign extend? (5 points)

5. Problems in this exercise assume that the logic blocks used to implement a processor's datapath have the following latencies:

I-Mem / D-Mem	Register File	Mux	ALU	Adder	Single gate	Register Read	Register Setup	Sign extend	Control
250 ps	200 ps	25 ps	200 ps	170 ps	5 ps	30 ps	20 ps	30 ps	150 ps

In above table, "Register Read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register Setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

(1) What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)? (5 points)
(2) What is the latency of lw? (5 points)
(3) What is the latency of sw? (5 points)
(4) What is the latency of beq? (5 points)
(5) What is the latency of an arithmetic, logical, or shift I-type (non-load) instruction? (5 points)
(6) What is the minimum clock period for this CPU? (5 points)

6. Modify the single-cycle processor datapath to support the `auipc` instruction.