HW5

1. (1) /

(2) In Hazard-detection Unit, insert nop when branch==1.
Move addr adder, comparator, branch logic to ID stage.

(3) Identified: ~~ID stage~~. IF stage >no nop.
Calculated: ~~ID stage~~. IF stage.
The IF stage is longer., maybe affect the clk cycle time.

2.

	1	2	3	4	5	6	7	8	9	10
lw	IF	ID	EX	MEM	WB					
lw		IF	ID	EX	MEM	WB				
add (nop)			IF	ID	bubble	bubble	bubble			
add				IF	ID	EX	MEM	WB		
addi					IF	ID	EX	MEM	WB	
bne						IF	ID	EX	MEM	WB

The second iteration is exactly the same.

3. (1) jal: no extra CPI. Since it's executing in IF stage.
(2) 45% · 30% = 15%. extra CPI. due to always-taken.
(2) jal: no extra CPI.
20% · 30% = 6% extra CPI when 2-bit.

4. (1) only first 2 T. $\frac{2}{6} = 33.3\%$
(2) only ≥ NT is mispredicted $\frac{4}{6} = 66.7\%$
(3) Use ~~Final~~ FSM
Input: Clk (hidden below), Control signal S.
Output: prediction (w)