JOINT INSTITUTE
交大密西根学院

ECE3700J Introduction to Computer Organization

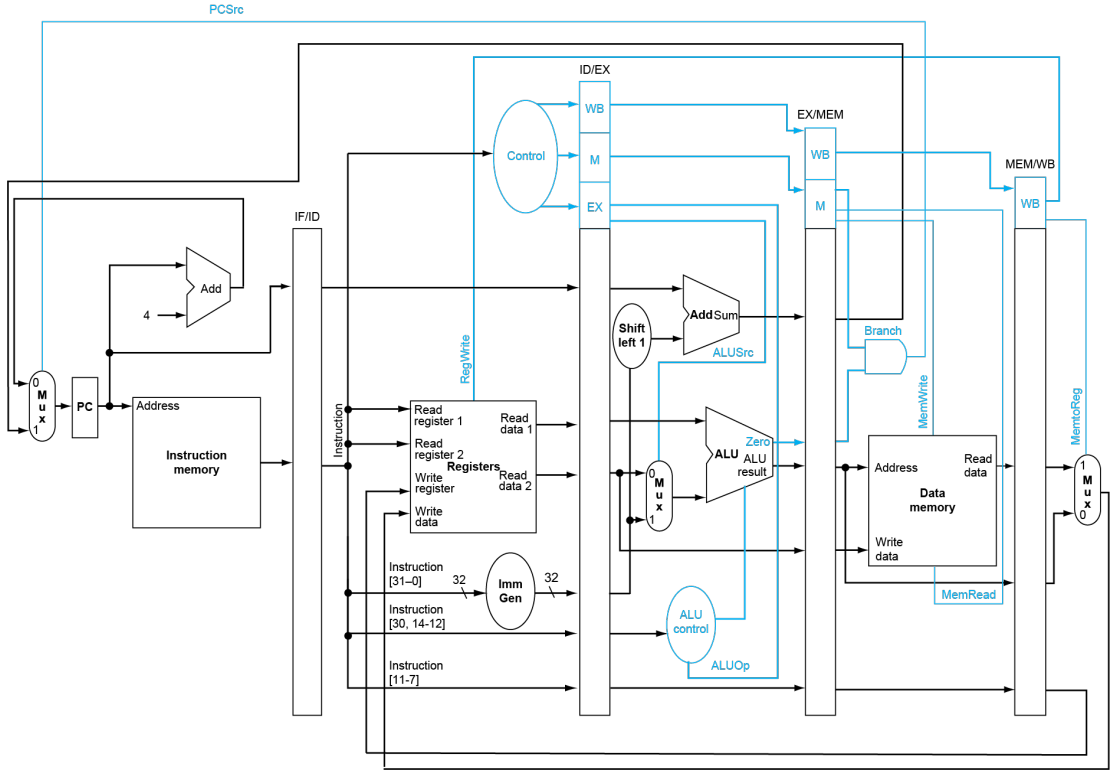
Homework 4

Assigned: October 17, 2023

Due: 2:00pm on October 24, 2023

Submit a PDF file on Canvas

Refer to the following figure for homework problems



1. (21 points) Given this instruction:
   `addi x10, x11, -4`

   As the instruction goes through the pipeline, what will be stored in the pipeline registers:
   IF: what's in PC
   ID: what's in IF/ID
   EX: what's in ID/EX?
   MEM: what's in EX/MEM
   WB: what's in MEM/WB?

2. (20 points) Assume that individual stages of the RISC-V pipelined datapath have the following latencies:

IF	ID	EX	MEM	WB
250 ps	200 ps	250 ps	300 ps	150 ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU/Logic	Jump/Branch	Load	Store
30%	20%	30%	20%

(1) What is the clock cycle time? (2 points)
(2) What is the execution time of a sw instruction in the pipelined processor? (3 points)
(3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor? (5 points)
(4) Using the processor to run a program of 1,000 instructions, what is the total execution time? What is the average CPI? (10 points)

3. (9 points) If we change load/store instructions to use a register (without an offset) as the address, these instructions no longer need to use the ALU. As a result, the MEM and EX stages can be overlapped and the pipeline has only four stages.
(1) How will the reduction in pipeline depth affect the cycle time? (3 points)
(2) How might this change improve the performance of the pipeline? (3 points)
(3) How might this change degrade the performance of the pipeline? (3 points)