ECE3700J
Course Introduction

Instructional Support

- **Instructor:** Gang Zheng, Ph.D.
- **Office:** JI New Building 400E
- **Contact:** (021) 3420-6765 x4005, gzheng@sjtu.edu.cn
- **Classroom:** SY317
- **Office Hours:** W 4:00 – 6:00pm / Th 10:00am – noon, in office and on Feishu, or by appointment
- **TAs:** Mr. RUAN Renjian, renjianruan967@sjtu.edu.cn
  Mr. XU Weiqing, sjtu_xwq@sjtu.edu.cn
  Mr. XU Haomiao, xhm_sjtu20@sjtu.edu.cn
- **Recitation:** once a week, discussing past HW problems
- **TA Office Hours:** TBD

What will be taught?

- Assembly language
- What's the correspondence between different levels of languages: C/C++, assembly, and machine language?
- How computers execute programs?
- How to design a processor as a digital system?
- What are the difficulties and tricks in the design of a CPU? How to resolve? How to improve performance?
- How memory works as part of a computer, and how is it organized?
- How processor, memory, and I/O devices work together as a computer?

What Are You Expected to Do?

- Write an assembly language program, translate the program into binary code, and trace execution of the program.
- Model a processor using hardware description languages (HDLs).
- Be able to identify and resolve potential data and control hazards in the Instruction Set Architecture (ISA)
- Understand memory hierarchy including cache, main memory, hard disk, and how data is stored, understand memory hits and misses
- Understand the memory mapped I/O concept and how I/O devices interface to the CPU
- Be able to use library and internet resources for literature review to learn contemporary issues, technologies, and future development trends in computing

Textbook

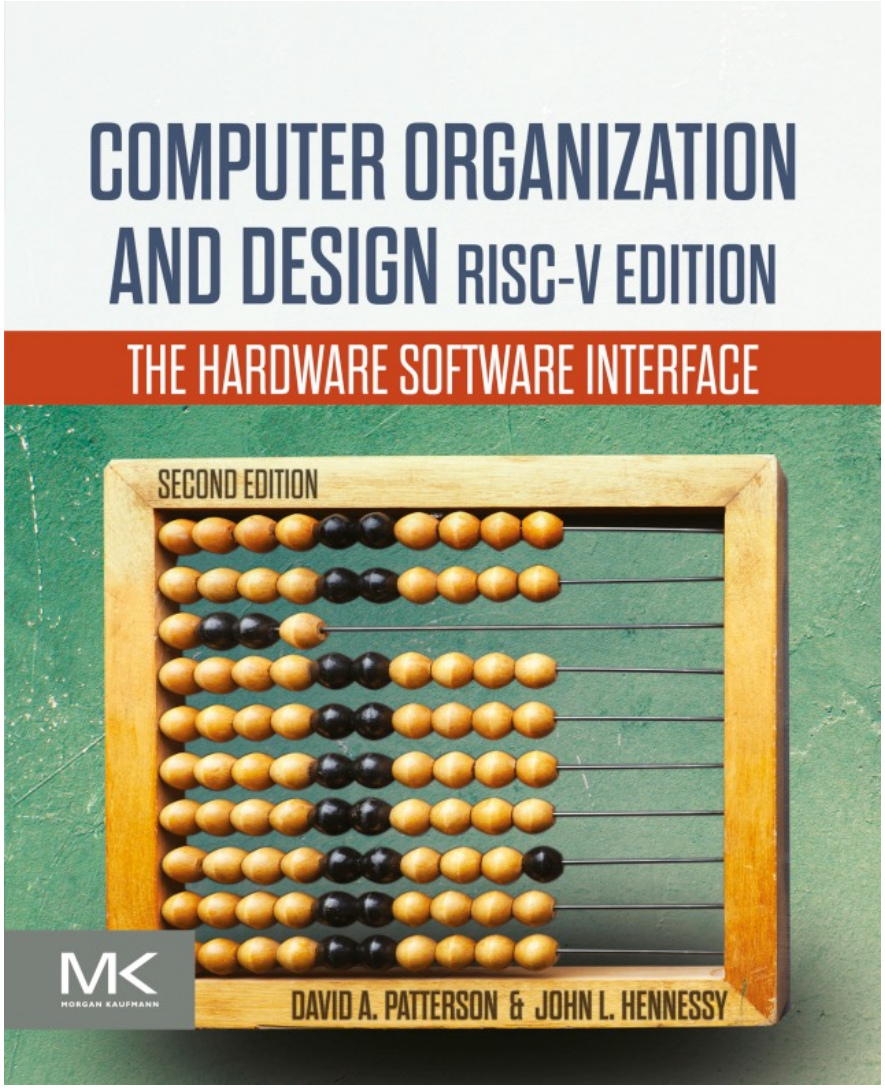
David Patterson and John Hennessy

Computer Organization and Design RISC-V Edition, 2nd edition

Morgan Kaufmann, 2020,

ISBN-10: 0128203315

ISBN-13: 978-0128203316



Tentative Schedule

Week	Date	Topics	Labs
1	9/12	Course Introduction, introduction to computer	
	9/14	Assembly: operations and operands	
2	9/19	operations and operands	Lab 1. RISC-V Assembly
	9/21	Assembly: function and function call	
3	9/26	**(online)** Assembly: function and function call	Lab 2. Assembly Programming
	9/28	**(online)** Assembly: instruction encoding	
4	10/3	**No Class (National Holiday)**	
	10/5	**No Class (National Holiday)**	
5	10/10	CPU: single cycle processor	Lab 3. Single Cycle Processor
	10/12	CPU: pipelined processor	
6	10/17	CPU: pipelined processor	
	10/19	CPU: data hazards	
7	10/24	CPU: data hazards	
	10/26	CPU: data hazards	
8	10/31	**Midterm Exam**	Lab 4. Pipelined Processor
	11/2	CPU: control hazards	
9	11/7	CPU: control hazards	
	11/9	Memory: cache	
10	11/14	Memory: cache	Lab 5. Resolving Hazards
	11/16	Memory: cache	
11	11/21	Memory: cache	Lab 6. Cache Memory
	11/23	Memory: virtual memory	
12	11/28	Memory: virtual memory	
	11/30	Memory: virtual memory	
13	12/5	I/Os and interfaces	Lab 7. Virtual Memory
	12/7	Discussion & Review	
14	TBD	**Final Exam**	

Course Policies

- **Honor Code:**
  - Honor Code of the Joint Institute
  - https://www.ji.sjtu.edu.cn/academics/academic-integrity/honor-code/
- **Test:**
  - Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.
- **Attendance:**
  - Attendance to the lectures is required, will be recorded randomly
  - Attendance to all lab sessions is required

Course Policies

- **Individual Assignments:**
  - Homework, Lab 1, 2, & 3, literature review report
  - OK to discuss lecture topics and help each other understand the project/homework requirements better
  - NOT OK for copying
- **Group Assignments:**
  - Labs 4 ~ 7
  - One submission, shared grade, except for peer evaluation part
  - Individual oral examination
- **Submission:**
  - Electronic submission on Canvas before deadline

Assessment Methods

- **Homework:**
  - About 8 homework assignments
- **Examination:**
  - Two paper-based examinations.
  - The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.
- **Laboratories:**
  - 7 labs
  - Labs 1-3 are individual work
  - Labs 4-7 are team work, 3 students per team, randomly grouped

Assessment Methods

- **Literature Review:**
  - Choose an interesting topic related to **performance improvement**
  - search literatures to review, write a review report
- **Participation:**
  - effective contribution on Piazza: effective posts, instructor's endorsement, answers, follow-ups, replies, etc.
  - Classroom interaction with the instructor and other students
  - Effective visit to office hours of the instructor and TA
  - active participation in team-based labs

Grading Policy

Attendance & Participation	2%
Midterm Exam	25%
Final Exam	25%
Lab */**	38%
Literature Review Report *	5%
Homework *	5%
Total	**100%**

*Individual assignments

**Group assignments

Note: final letter grades may be curved

Join the Class Feishu Group

Only members of this organization can join this group

This QR code is valid for 7 days (before 9/18)

- **For**
  - Occasional online Lectures
  - Office hours
  - Emergency notice
  - Discussions of course logistics
- **Not For**
  - Official announcement (Canvas)
  - Resource sharing (Canvas)
  - Tech questions and discussions (Piazza)