JOINT INSTITUTE
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ECE3700J Introduction to Computer Organization

Homework 7

Assigned: October November 22, 2022

Due: 2:00pm on November 29, 2022

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1. (20 points) For a 2-way set associative cache with a 32-bit address and write back mechanism, the partition of the 32 bits are as follows:
   - Offset: bit 6 to 0
   - Index: bit 11-7

   (1) What is the size of the cache? (5 points)

   The cache has 2^5=32 sets → 64 blocks.

   Word offset has 7-2=5 bits. Thus there are 32words per block.

   Thus the cache has 32*64*32+(1+1+20)*64=66944 bits=8368 bytes

   Starting from power on, the following byte addresses were used to access the cache memory: 0, 4, 20, 136, 232, 164, 1024, 30, 140, 3100, 176, 2180

   (2) What is the hit ratio? (5 points)

   0-miss
   4-hit
   20-hit
   136-miss
   232-hit
   164-hit
   1024-miss
   30-hit
   140-hit
   3100-miss
   176-hit
   2180-miss
   Hit ratio: 7/12=58.33%

   (3) Show the final state of the cache, with each valid line represented as <index, tag, data>. (10 points)

   The offsets below are word address.

   <0, 0, Mem[0]-Mem[31]>

   <1, 0, Mem[32]-Mem[63]>

   <8, 0, Mem[256]-Mem[287]>

<17, 0, Mem[544]-Mem[575]>

<24, 0, Mem[768]-Mem[799]>

2. (20 points) In general, cache access time is proportional to its capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for caches attached to each of two processors, P1 and P2.

	Size	Miss Rate	Hit Time
P1	16KB	4.3%	1.18 ns
P2	32KB	2.7%	2.22 ns

(1) Assuming that the cache hit time determines the cycle times for P1 and P2, what are their respective clock rates? (5 points)

P1: 1/1.18ns=0.847GHz

P2: 1/2.22ns=0.450GHz

(2) What is the AMAT for P1 and P2? AMAT (Average Memory Access Time) is defined as follows: AMAT = Hit time + Miss rate × Miss penalty (5 points).

P1: AMAT=1.18ns+4.3%*70ns=4.19ns

P2: AMAT=2.22ns+2.7%*70ns=4.11ns

(3) Assuming a base CPI of 1.0 without any memory stalls, what is the actual CPI for P1 and P2? Which processor is faster? (10 points)

P1: CPI=1.0+36%*4.19/1.18=2.28

P2: CPI=1.0+36%*4.11/2.22=1.56

P2 takes little CPI

P1: CPI*TC=2.28*1.18ns=2.69ns

P2: CPI*TC=1.56*2.22ns=3.46ns

For same amount of instructions, P1 is faster.

3. (60 points) Given the following byte addresses for memory access:

3, 180, 43, 3, 191, 89, 190, 14, 181, 44, 186, 252

(1) Show the final cache contents for a 3-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference identify the index bits, the tag bits, the offset bits, and if it is a hit or a miss. (20 points)

24/(3*2)=4sets, Index: 2bits. Word offset: 1bit. Byte offset: 2bits.

	3	180	43	3	191	89	190	14	181	44	186	252
Index	0	10	1	0	11	11	11	1	10	1	11	11
Tag	0	101	1	0	101	10	101	0	101	1	101	111
Offset	011	100	011	011	111	001	110	110	101	100	010	100
Hit/miss	miss	miss	miss	hit	miss	miss	hit	miss	hit	hit	hit	miss

Final state below: <index, tag, data(two words)>

<00, 0, Mem[0], Mem[1]>

<01, 0, Mem[2], Mem[3]>

<01, 1, Mem[10], Mem[11]>

<10, 101, Mem[44], Mem[45]>

<11, 101, Mem[46], Mem[47]>

<11, 10, Mem[22], Mem[23]>

<11, 111, Mem[62], Mem[63]>

(2) Show the final cache contents for a fully associative cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference identify the index bits, the tag bits, and if it is a hit or a miss. (20 points)

	3	180	43	3	191	89	190	14	181	44	186	252
Tag	0	101101	1010	0	101111	10110	101111	11	101101	1011	101110	111111
Offset	11	00	11	11	11	01	10	10	01	00	10	00
Hit/miss	miss	miss	miss	hit	miss	miss	hit	miss	hit	miss	miss	miss

Final state below: <tag, data>

<0, Mem[0]>

<101101, Mem[45]>

<111111, Mem[63]>

<101111, Mem[47]>

<10110, Mem[22]>

<11, Mem[3]>

<1011, Mem[11]>

<101110, Mem[46]>

(3) What is the miss rate for a fully associative cache with two-word blocks and a total size of 8 words, using LRU replacement? What is the miss rate using MRU (most recently used) replacement? Finally what is the best possible miss rate for this cache, given any replacement policy? (20 points)

LRU:

	3	180	43	3	191	89	190	14	181	44	186	252
Tag	0	10110	101	0	10111	1011	10111	1	10110	101	10111	11111
Offset	011	100	011	011	111	001	110	110	101	100	010	100
Hit/miss	miss	miss	miss	hit	miss	miss	hit	miss	miss	miss	hit	miss

Miss rate=9/12=0.75

MRU miss rate: Also 3 hits (0, 10110, 101): 0.75

Best possible miss rate: 7/12=0.58 (Always replace the one will not be used)