JOINT INSTITUTE
交大密西根学院

ECE3700J Introduction to Computer Organization

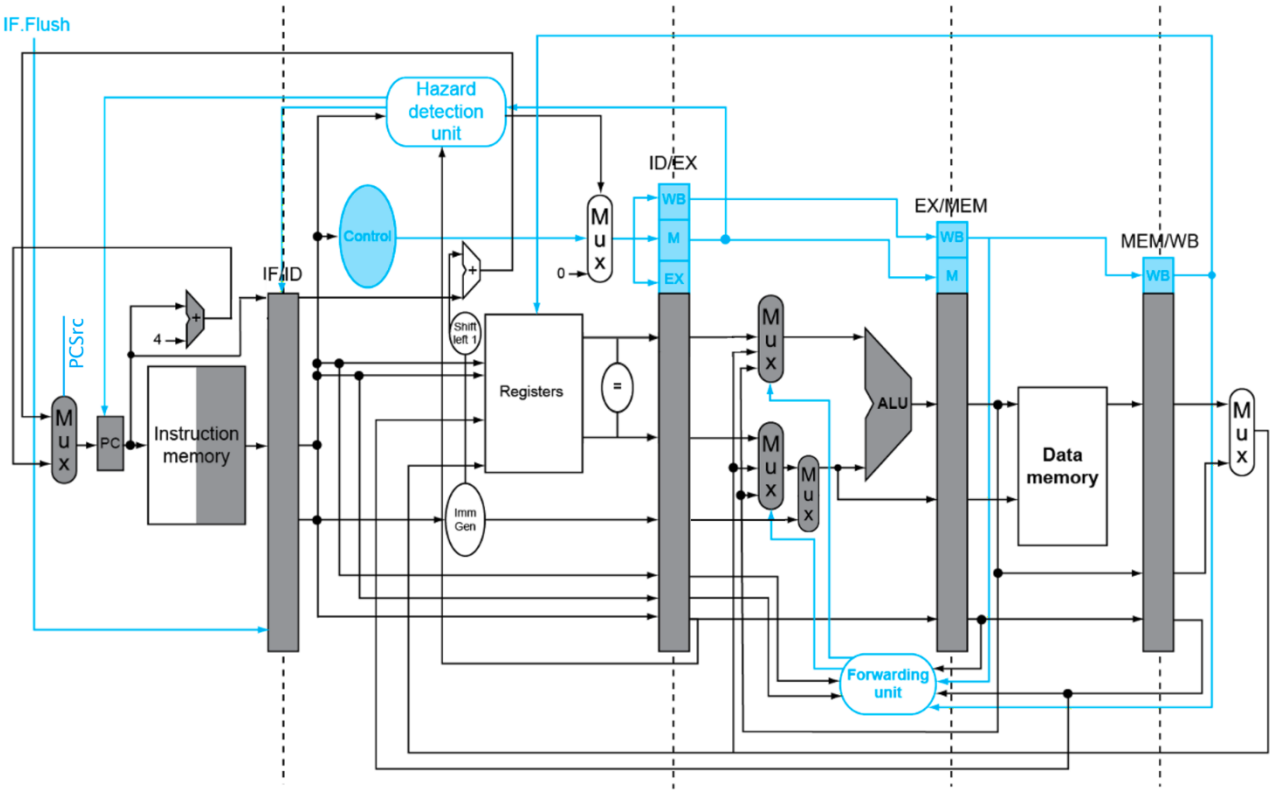
Homework 6

Assigned: November 7, 2023

Due: 2:00pm on November 14, 2023

Submit a PDF file on Canvas

1. (30 points) One of the solutions to control hazard is to always stall the instruction following the branch or jump instruction by inserting nop instructions. Using the following diagram as a reference:



(1) How can the stall be implemented in hardware rather than in software? (15 points)

(2) If the above pipeline is modified to support jalr instruction, which would be the earliest stage the jump instruction is identified and jump target is calculated? In that case, how many stalls would have to be inserted? How would the clock cycle time be affected? (15 points)

2. (20 points) The importance of having a good branch predictor depends on how often conditional branches are executed. Together with branch predictor accuracy, this will

determine how much time is spent flushing due to mispredicted branches. In this exercise, assume that the breakdown of dynamic instructions into various instruction categories is as follows:

R-type	branch	jal	lw	sw
40%	20%	10%	15%	15%

Also, assume the following branch predictor accuracies:

Always-Taken	Always-Not-Taken	2-Bit Dynamic
35%	65%	85%

(1) Stall cycles due to mispredicted branches and jumps increase the CPI. What is the extra CPI due to jumps? What is the extra CPI due to mispredicted branches with the always-not-taken predictor? Assume that branch outcomes are determined in the ID stage and that there are no data hazards, and that no delay slots are used. (10 points)

(2) Repeat (1) for the 2-bit predictor. (10 points)

NOTE: the following problems are optional and won't be graded.

3. Consider the following loop.

```
LOOP: lw x10, 0(x13)
      lw x11, 8(x13)
      add x12, x10, x11
      addi x13, x13, 16
      bne x12, x13, LOOP
```

Assume that perfect branch prediction is used (no stalls due to control hazards), that there are no delay slots, that the pipeline has full forwarding support, and that branches are determined in the ID stage. Show a pipeline execution (multicycle) diagram for the first two iterations of this sequence of instructions. Hint: unfold the loop first. Hint : you may use Excel to show the execution diagram.

4. Given following repeating pattern of a branch instruction: T, T, NT, NT, NT, T. (T: taken, NT: not taken)

(1) What is the steady-state accuracy of a 1-bit dynamic predictor if this pattern is repeated forever?

(2) What is the steady-state accuracy of a 2-bit dynamic predictor (as on Slide 28 of Topic 8) if this pattern is repeated forever?

(3) Design a predictor that would achieve a perfect accuracy if this pattern is repeated forever. You predictor should be a sequential circuit with one output that provides a prediction (1 for taken, 0 for not taken) and no inputs other than the clock and the control signal that indicates that the instruction is a conditional branch.

5. Which levels and concepts of a memory hierarchy are analogous to these frozen food storage mechanisms and events?
   a. The refrigerator in the kitchen
   b. Frozen food freezers at a grocery store
   c. Suppliers of frozen food for the grocery store
   d. Getting food from the refrigerator to cook
   e. Time it takes to get food from the refrigerator
   f. Chances of not finding the desired food in the refrigerator
   g. Putting cooked food into the refrigerator
   h. Getting new food from the grocery store to put in the refrigerator
   i. Time taken to get new food from the grocery store
   j. Finding a short cut to the grocery store to get new food