JOINT INSTITUTE
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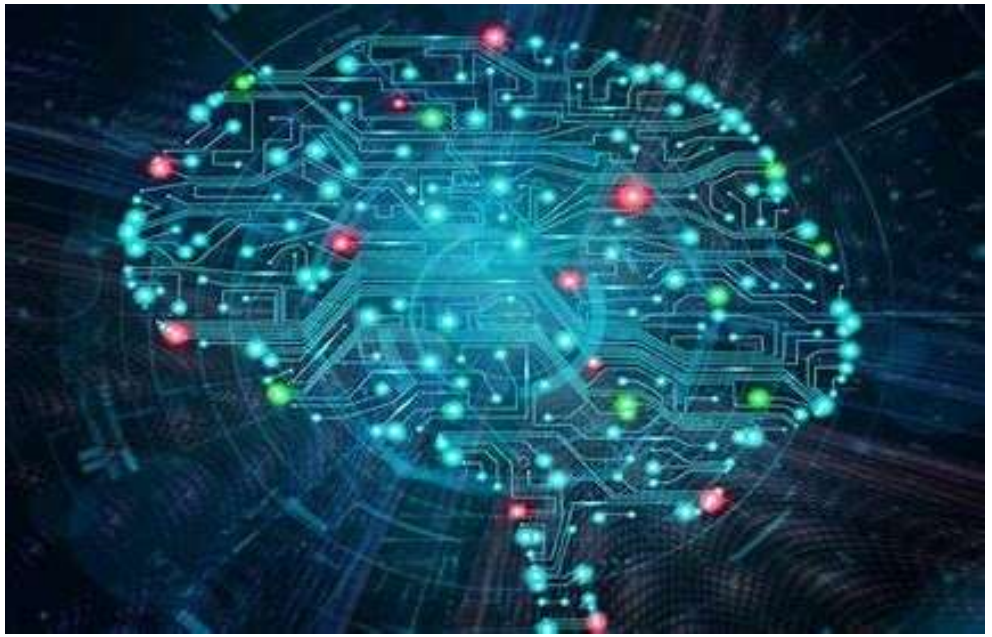
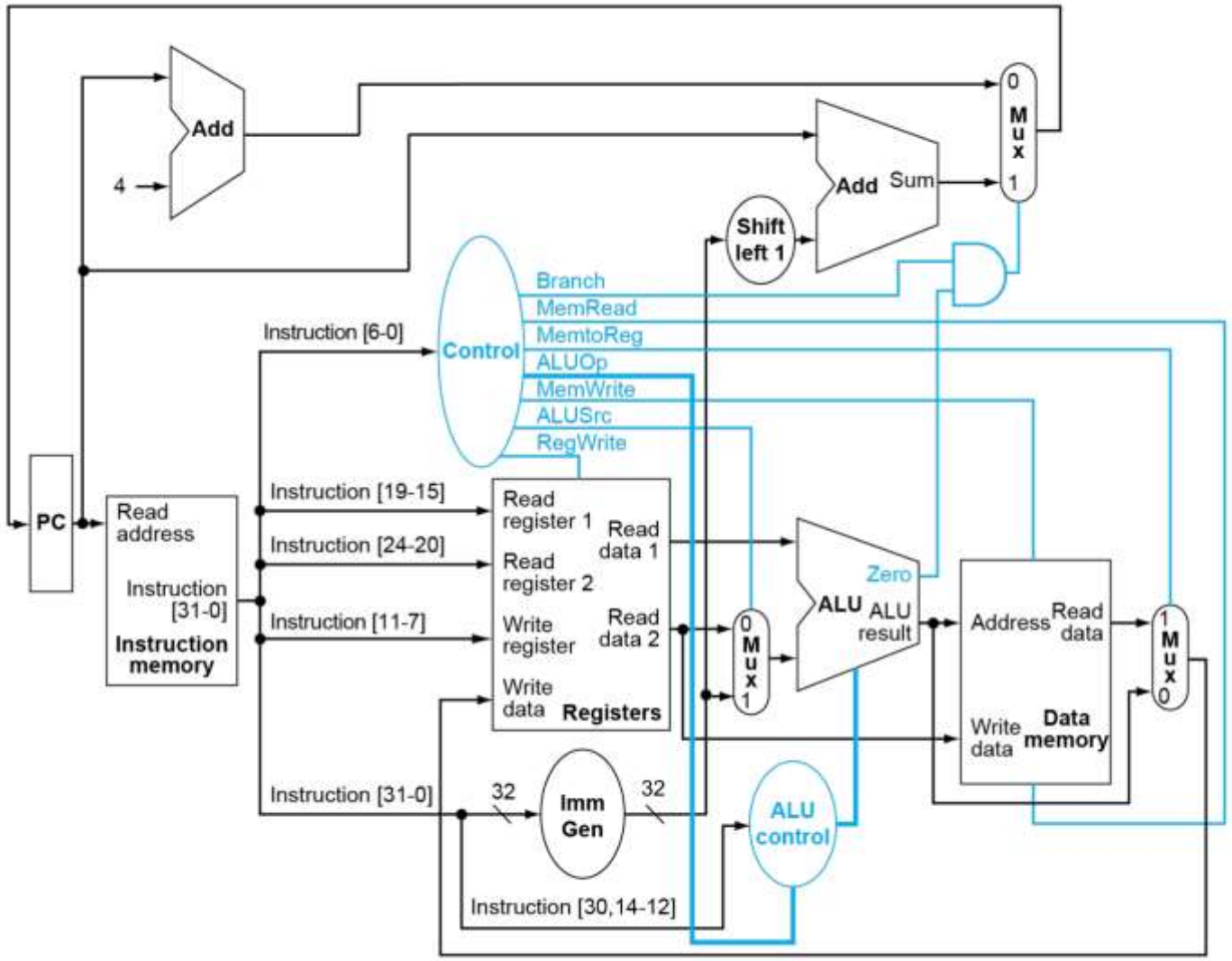
RC4



ECE3700J Intro to Computer Organization

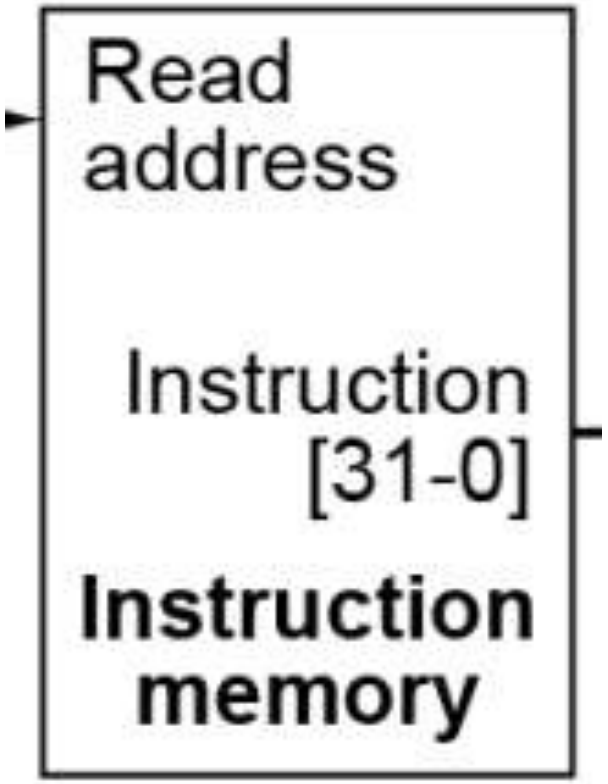
2023.10.17

Single Cycle Processor




```
1  .text
2  main:
3      addi x10, x0, 100
4      sw x10, 100(x0)
5      lw x11, 0(x10)
6      add x12, x11, x10
7      addi x8, x0, 200
8      beq x12, x8, Exit
9  Wrong_Exit:
10     addi x13, x0, 1
11 Exit:
12     add x0, x0, x0
```

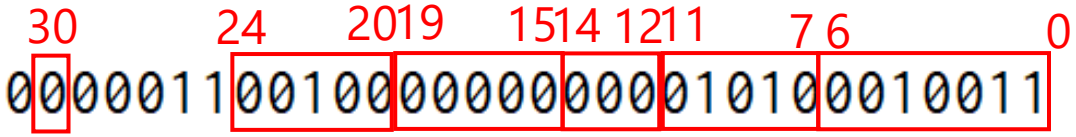
Single Cycle Processor

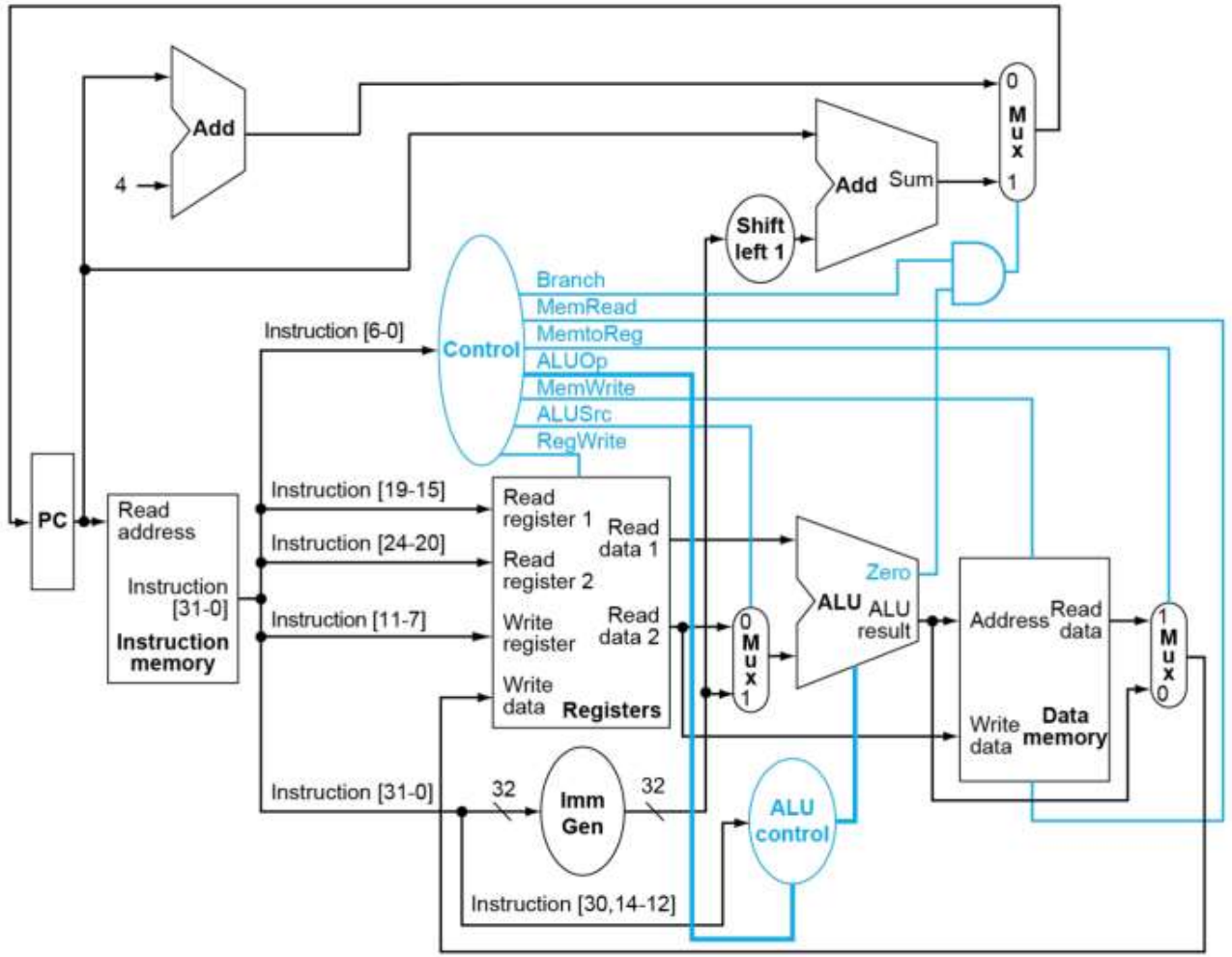



```
3     addi x10, x0, 100
4     sw x10, 100(x0)
5     lw x11, 0(x10)
6     add x12, x11, x10
7     addi x8, x0, 200
8     beq x12, x8, Exit
10    addi x13, x0, 1
12    add x0, x0, x0
```

Single Cycle Processor

```
3    addi x10, x0, 100
```





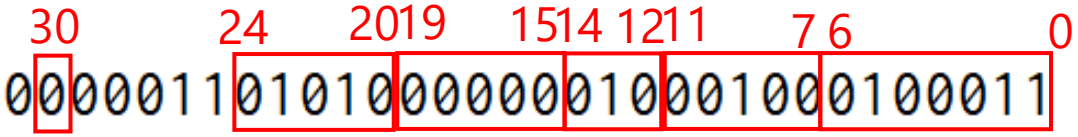
Branch = 0
MemRead = 0
MemToReg = 0
ALUOp = X
MemWrite = 0
ALUSrc = 1
RegWrite = 1

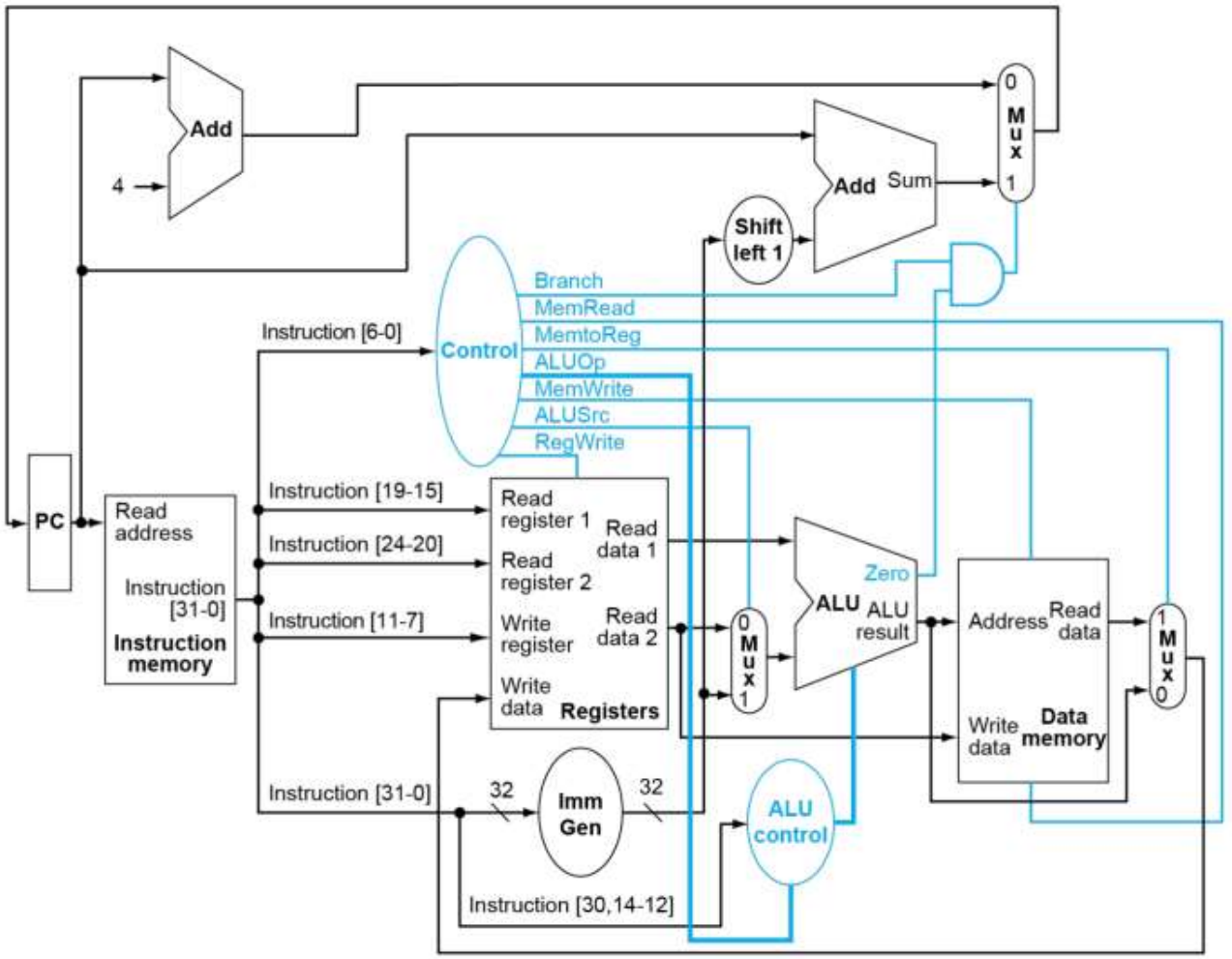
PC = 0x00

Immediate num
= 000001100100
= 4+32+64
= 100

Single Cycle Processor

4 `sw x10, 100(x0)`





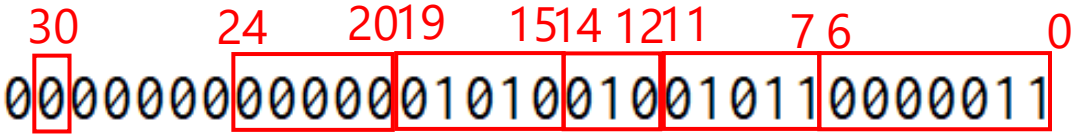
Branch = 0
MemRead = 0
MemToReg = 0
ALUOp = 00
MemWrite = 1
ALUSrc = 1
RegWrite = 0

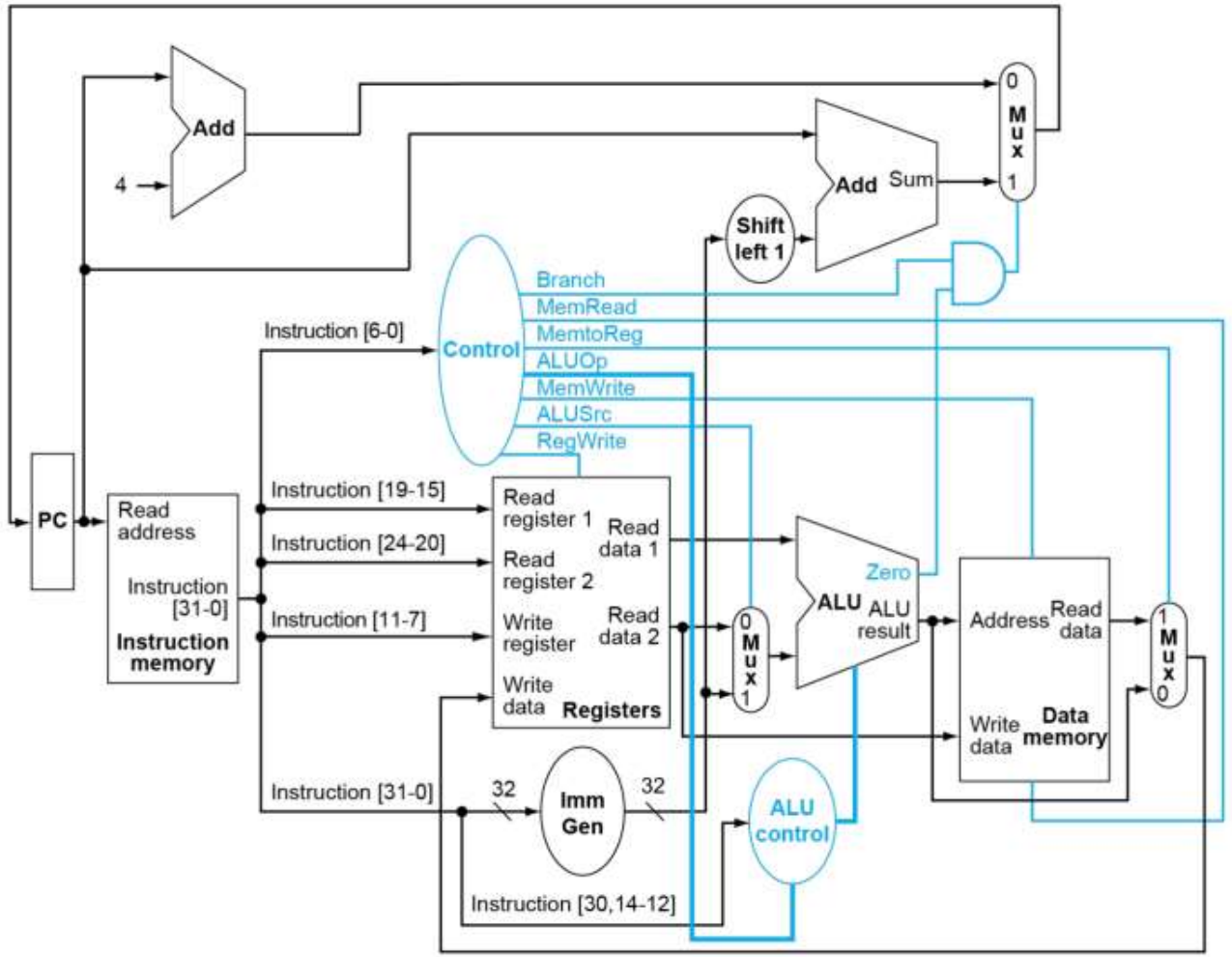
Immediate num
= 000001100100
= 4+32+64
= 100

PC = 0x04

Single Cycle Processor

```
5    lw x11, 0(x10)
```





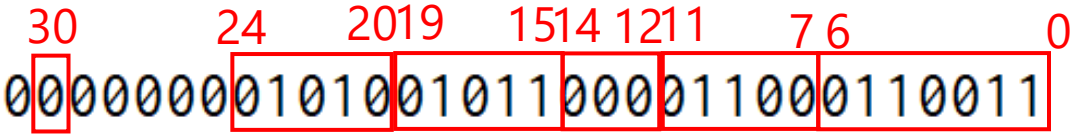
Branch = 0
MemRead = 1
MemToReg = 1
ALUOp = 00
MemWrite = 0
ALUSrc = 1
RegWrite = 1

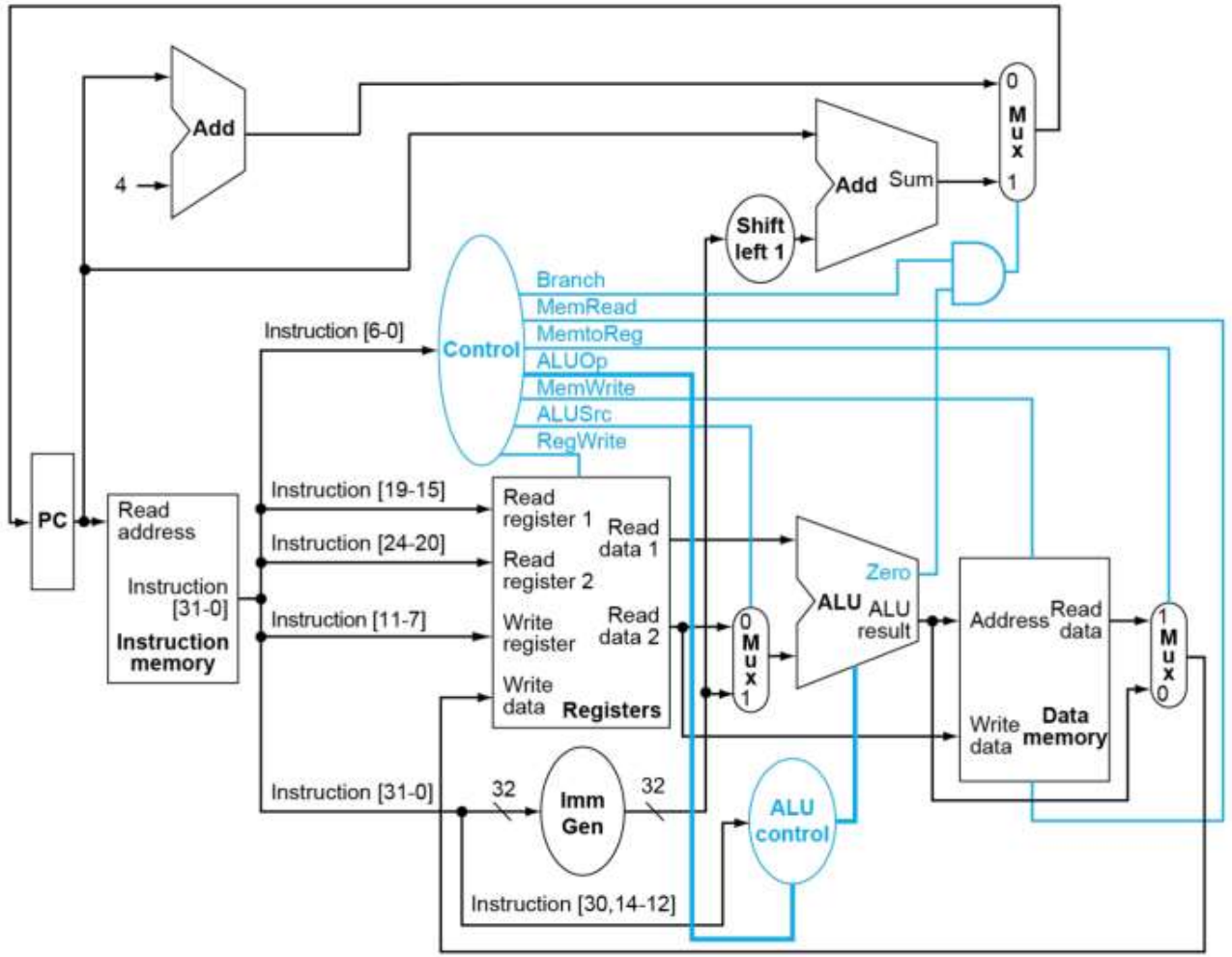
Immediate num
= 000000000000
= 0

PC = 0x08

Single Cycle Processor

6 `add x12, x11, x10`





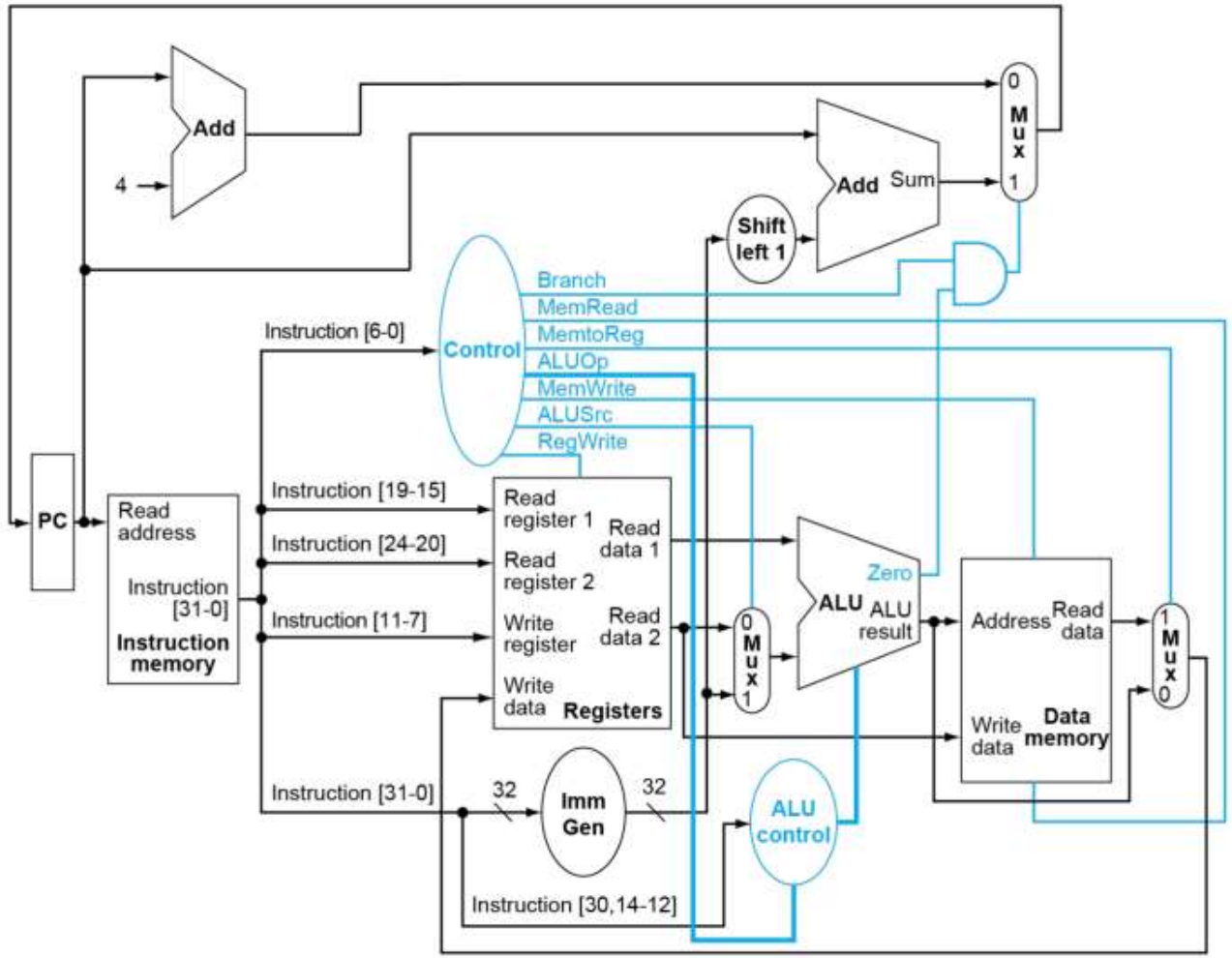
Branch = 0
MemRead = 0
MemToReg = 0
ALUOp = 10
MemWrite = 0
ALUSrc = 0
RegWrite = 1

PC = 0x0C

Single Cycle Processor

```
7    addi x8, x0, 200
```

```
30      24      2019     1514 1211     7 6          0
0000110 01000 00000 000 01000 0010011
```



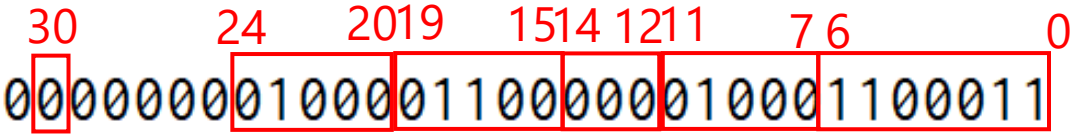
Branch = 0
MemRead = 0
MemToReg = 0
ALUOp = X
MemWrite = 0
ALUSrc = 1
RegWrite = 1

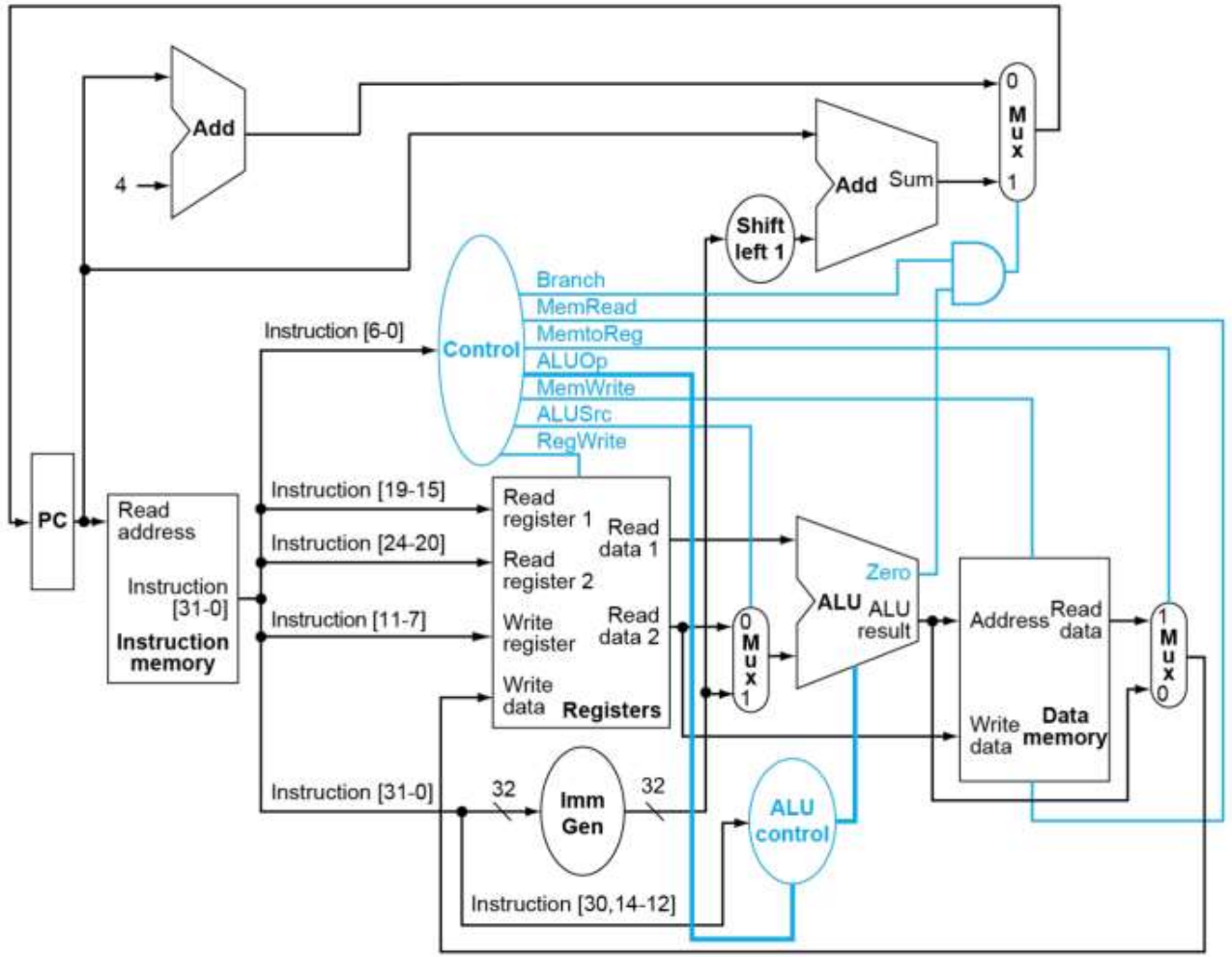
Immediate num
= 000011001000
= 8+64+128
= 200

PC = 0x10

Single Cycle Processor

```
8        beq x12, x8, Exit
```





Branch = 1
MemRead = 0
MemToReg = 0
ALUOp = 01
MemWrite = 0
ALUSrc = 0
RegWrite = 0
Zero = 1

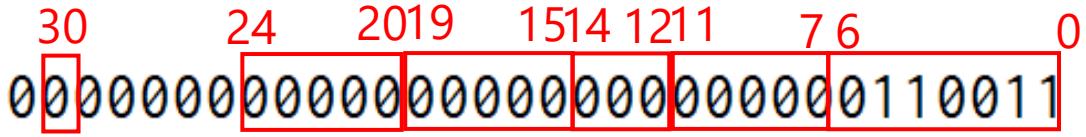
Immediate num
=000000000100
= 4

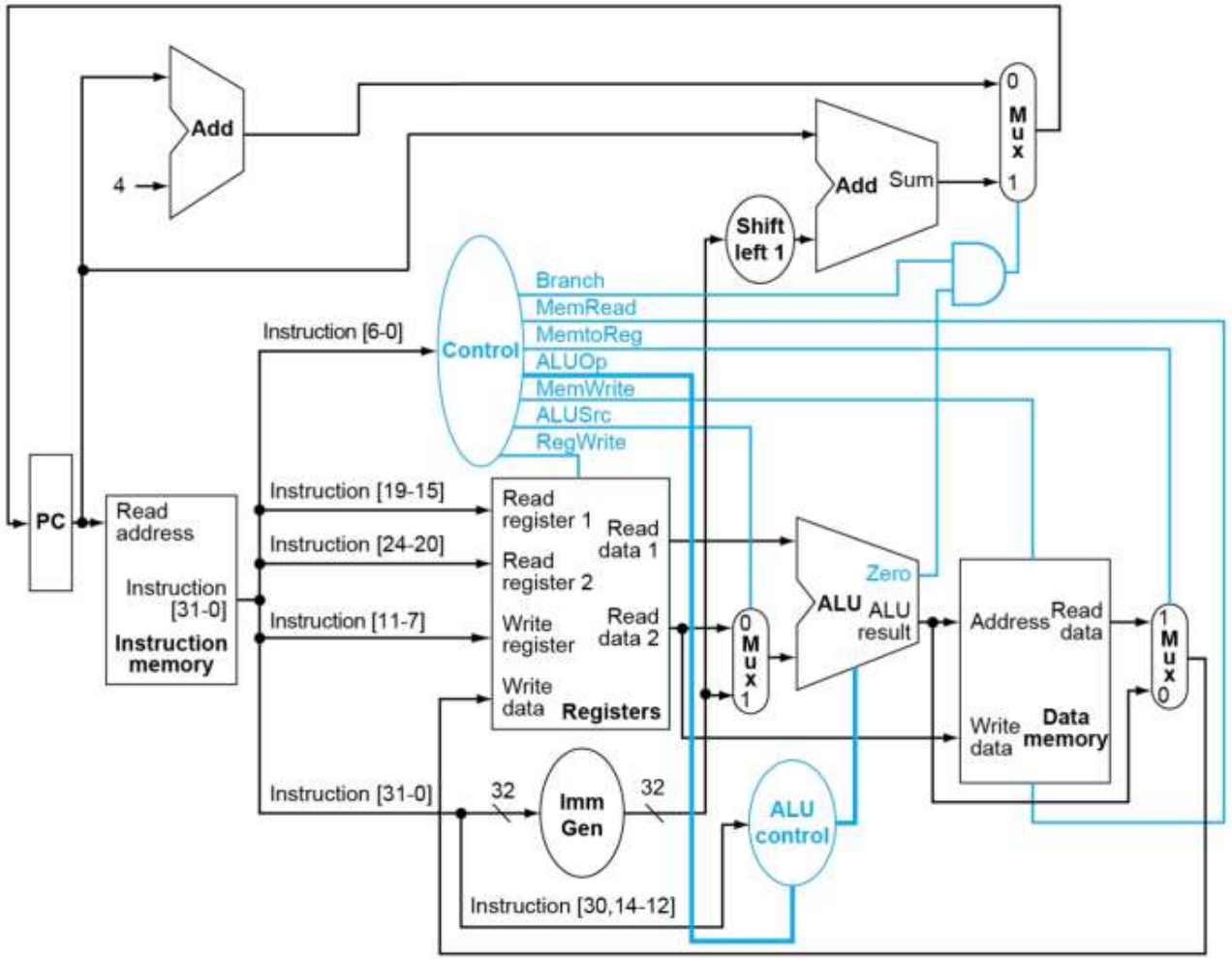
PC = PC + 4 * 2 =
0x1C

PC = 0x14

Single Cycle Processor

12 `add x0, x0, x0`





Branch = 0
MemRead = 0
MemToReg = 0
ALUOp = 10
MemWrite = 0
ALUSrc = 0
RegWrite = 1

PC = 0x1C

That's all for today's RC