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ECE3700J Introduction to Computer Organization

Homework 4

Assigned: October 20, 2022

Due: 2:00pm on November 1, 2022

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1. (15 points) Given this instruction:  
sw x5, -4(x2)

As the instruction goes through the pipeline, what will be stored in the pipeline registers:

IF: what's in PC

The address of this instruction.

ID: what's in IF/ID

The address of this instruction, and the instruction itself.

EX: what's in ID/EX?

Note that the binary code for this instruction is 1111110010100010010111000100011

1. Control signals:

- a) ALUop: 00
- b) ALUsrc: 1
- c) Branch: 0
- d) Memread: 0
- e) Memwrite: 1
- f) MemtoReg: 0
- g) RegWrite: 0

2. PC(the address of this instruction)

3. ReadData1: the data in x2

4. ReadData2: the data in x5

5. Immediate number: 0xFFFF\_FFFC

6. Instruction[30,14-12]=I[30]+funct3=1010

7. Instruction[11-7]=rd=11100 (not used)

MEM: what's in EX/MEM

1. Control signals:

- a) Branch: 0
- b) Memread: 0
- c) Memwrite: 1
- d) MemtoReg: 0
- e) RegWrite: 0

2. PC(the address of this instruction) + immediate\*2

3. Zero

4. ALUresult = (the data in x2) - 4

5. Instruction[11-7]=rd=11100 (not used)

WB: what's in MEM/WB?

1. Control signals:

- a) MemtoReg: 0

b) RegWrite: 0

2. Instruction[11-7]=rd=11100 (not used)

3. ReadData: the data in memory[(the data in x2) - 4] (not used)

4. ALUresult: (the data in x2) - 4

2. (20 points) Assume that individual stages of the RISC-V pipelined datapath have the following latencies:

IF	ID	EX	MEM	WB
300 ps	150 ps	250 ps	300 ps	150 ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU/Logic	Jump/Branch	Load	Store
45%	15%	20%	20%

- (1) What is the clock cycle time? (2 points)

$T_c = 300\text{ps}$

- (2) What is the execution time of a sw instruction in the pipelined processor? (3 points)

$T = 5 * T_c = 1500\text{ps}$

- (3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor? (5 points)

IF or MEM stage

New clock cycle time is still 300ps.

- (4) Using the processor to run a program of 1,000 instructions, what is the total execution time? What is the average CPI? (10 points)

$CPI = (1000 + 4) / 1000 = 1.004$

Total execution time =  $IC * CPI * T_c = 1000 * 1.004 * 300\text{ps} = 301200\text{ps}$

3. (10 points) Assume that x11 is initialized to 11 and x12 is initialized to 12. Suppose you executed the code below on a pipelined processor that does not handle data hazards at all.

L1: addi x11, x12, 5

L2: add x13, x12, x11

L3: addi x14, x11, 15

- (1) Indicate data dependencies, if any, in above instruction sequence. (which register between which instructions) (5 points)

x11: L1 and L2, L1 and L3

- (2) What would the final values of registers x13 and x14 be? (5 points)

X13: 23

X14: 26

4. (30 points) Given the following instructions:

L1: addi x8, x0, 1000

L2: sw x18, -12(x8)

L3: lw x3, 8(x18)

L4: add x6, x3, x3



L5: or x8, x9, x6

- a) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)

L1: addi x8, x0, 1000

NOP

NOP

L2: sw x18, -12(x8) //L1, EX hazard

L3: lw x3, 8(x18)

NOP

NOP

L4: add x6, x3, x3 //L3, load-use hazard

NOP

NOP

L5: or x8, x9, x6 // L4, EX hazard

Total: 11 clock cycles.

- b) Assume there is ALU-ALU forwarding. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)

L1: addi x8, x0, 1000

L2: sw x18, -12(x8)

L3: lw x3, 8(x18)

NOP

NOP

L4: add x6, x3, x3 //L3, load-use hazard

L5: or x8, x9, x6

Total: 7 clock cycles.

- c) Assume there is full forwarding. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)

L1: addi x8, x0, 1000

L2: sw x18, -12(x8)

L3: lw x3, 8(x18)

NOP

L4: add x6, x3, x3 //L3, Mem hazard

L5: or x8, x9, x6

Total: 6 clock cycles.

5. (25 points) Given this assembly instruction sequence executed by the pipelined processor:

sub x6, x2, x1

lw x3, 8(x6)

lw x2, 0(x6)

or x3, x5, x3

sw x3, 0(x5)

- a) If the processor has forwarding, but we forgot to implement the hazard detection unit, what happens when this code executes? (5 points)

It will run correct since the forwarding unit has eliminated all the hazards.

- b) If there is forwarding, for the first five cycles during the execution of this code, specify which signals are asserted in each cycle by hazard detection and forwarding units. (10 points)

sub x6, x2, x1: No asserted signals



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lw x3, 8(x6): ForwardA=10
lw x2, 0(x6): ForwardA=01
or x3, x5, x3: ForwardB=01
sw x3, 0(x5): ForwardB=10
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- c) If there is no forwarding, what new inputs and output signals do we need for the hazard detection unit? Using this instruction sequence as an example, explain why each signal is needed. (10 points)

New input signals: ID/EX.RegWrite, ID/EX.RegRd, EX/MEM.RegWrite, EX/MEM.RegRd

No new output signals

L1: sub x6, x2, x1

L2: lw x3, 8(x6)

L3: lw x2, 0(x6)

L4: or x3, x5, x3

L5: sw x3, 0(x5)

Reasons: ID/EX.RegWrite and ID/EX.RegRd are for EX hazard, for example, x6 between L1 and L2, x3 between L4 and L5. EX/MEM.RegWrite and EX/MEM.RegRd are for MEM hazard, for example, x6 between L1 and L3, x3 between L2 and L4.