ECE3700J Introduction to Computer Organization
Lab 3 – Single Cycle Processor

Purpose

This lab is intended to help you have a better understanding of RISC-V 32-bit single cycle architecture as well as how different format of instructions are executed by the processor. Although single-cycle design is not commonly adopted in modern processors, it lays a good basis for more advanced CPU designs. The individual elements you will model in this lab will be reused in the designs of future labs. Therefore, having each element modeled separately and verified individually is critical to completion of the future labs.

Tasks

In this lab, every student models a single cycle processor in Verilog HDL that executes a subset of RISC-V instructions including:

- The arithmetic-logical instructions `add`, `addi`, `sub`, `and`, and `or`
- The memory-reference instructions `lw` and `sw`
- The branch instructions `beq` and `bne`

Your modules must be simulated with a Verilog simulator of your choice and synthesized by using Xilinx synthesis tool. This means your Verilog code must be **synthesizable**. A simple RISC-V assembly testing program will be provided to verify that the processor can execute those instructions continuously and correctly.

FPGA hardware implementation is NOT required.

Deliverables

- **Demonstration –** Every student should demonstrate to the teaching group the following before your lab session ends:
  1) Simulation results of the top-module of your design
  2) RTL schematic of your Verilog model generated with Xilinx Vivado software.

- **Lab report** – The lab report should be a written report including:
  1) Brief description of all aspects of the modeling and implementation of the processor;
  2) Screen shots of simulation results for individual modules: Register File, 32-bit ALU, 32-bit Adder, Immediate Generator, Control Unit, ALU Control, 2-to-1 MUX, Instruction Memory, and Data Memory.
  3) Screen shots and brief explanations of simulation results for each type of instruction (`add`, `addi`, `lw`, `sw`, and `beq`).
  4) RTL schematic of your Verilog model generated with Xilinx Vivado software;

- **Source Files –** All your Verilog source files and any other supporting files should be submitted as appendix to the lab report.

This is an individual assignment. Your work must be submitted electronically to Canvas before the specified due date. Late submission will result in 0 point for the corresponding deliverables. Source code must be submitted before a grade for this lab can be assigned.

This is a 3-week lab. The full score for this lab is 500 points. All required documents should be submitted on Canvas before **22:00pm, October 28, 2023**.

Grading

- Lab report: 40%
- Demonstration and oral examination: 40%
- Source files: 20%