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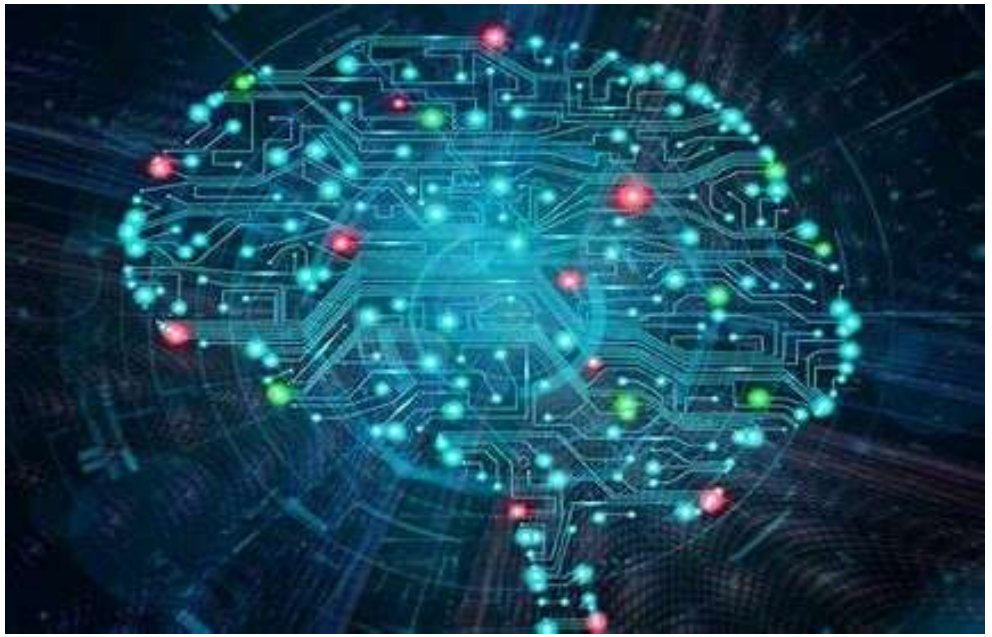
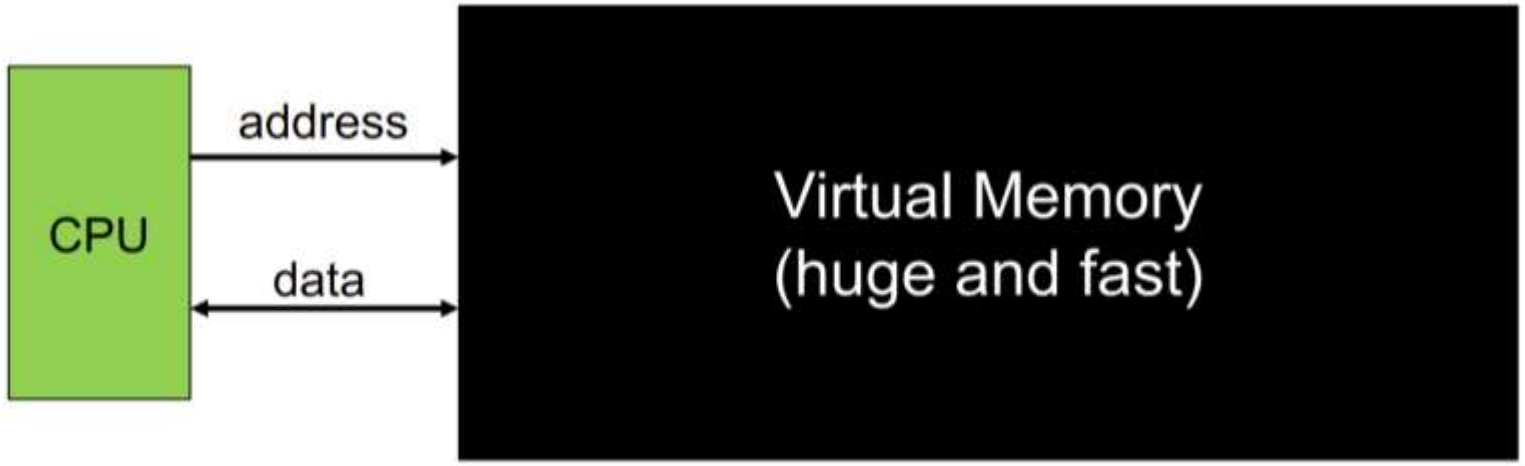
Final RC



ECE3700J Intro to Computer Organization

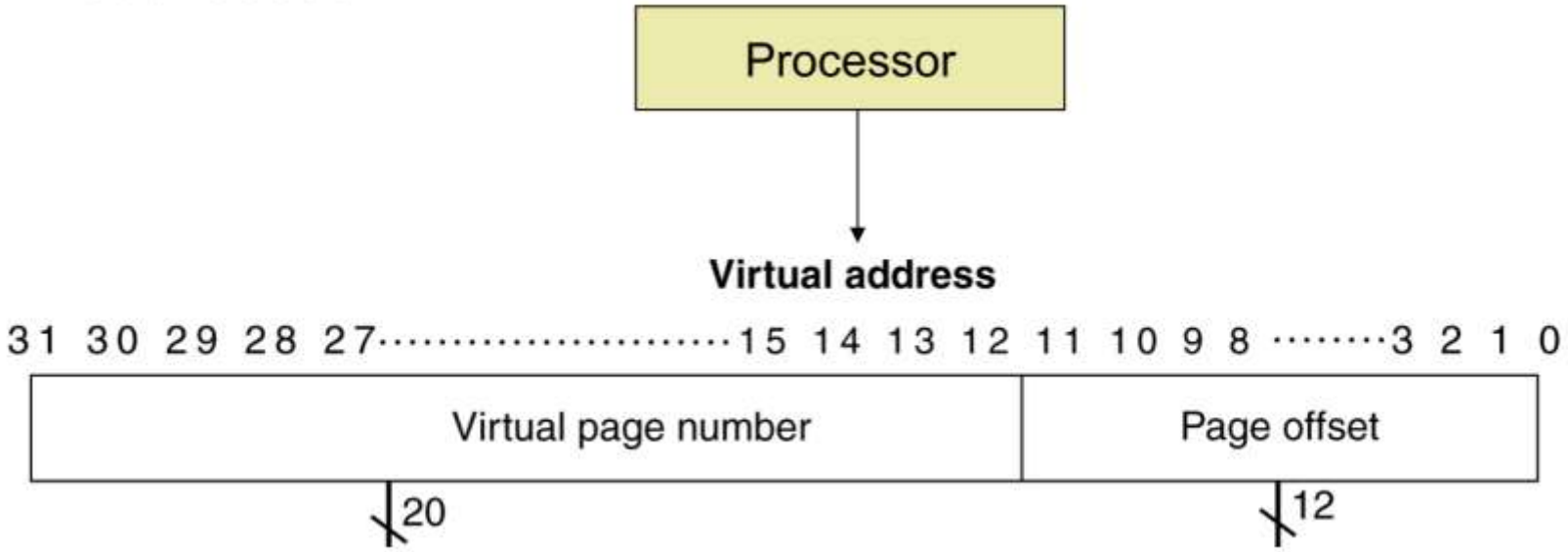
2023.12.9

Virtual Memory



- **Black box**
- **The CPU provides the address and virtual memory provides the data.**

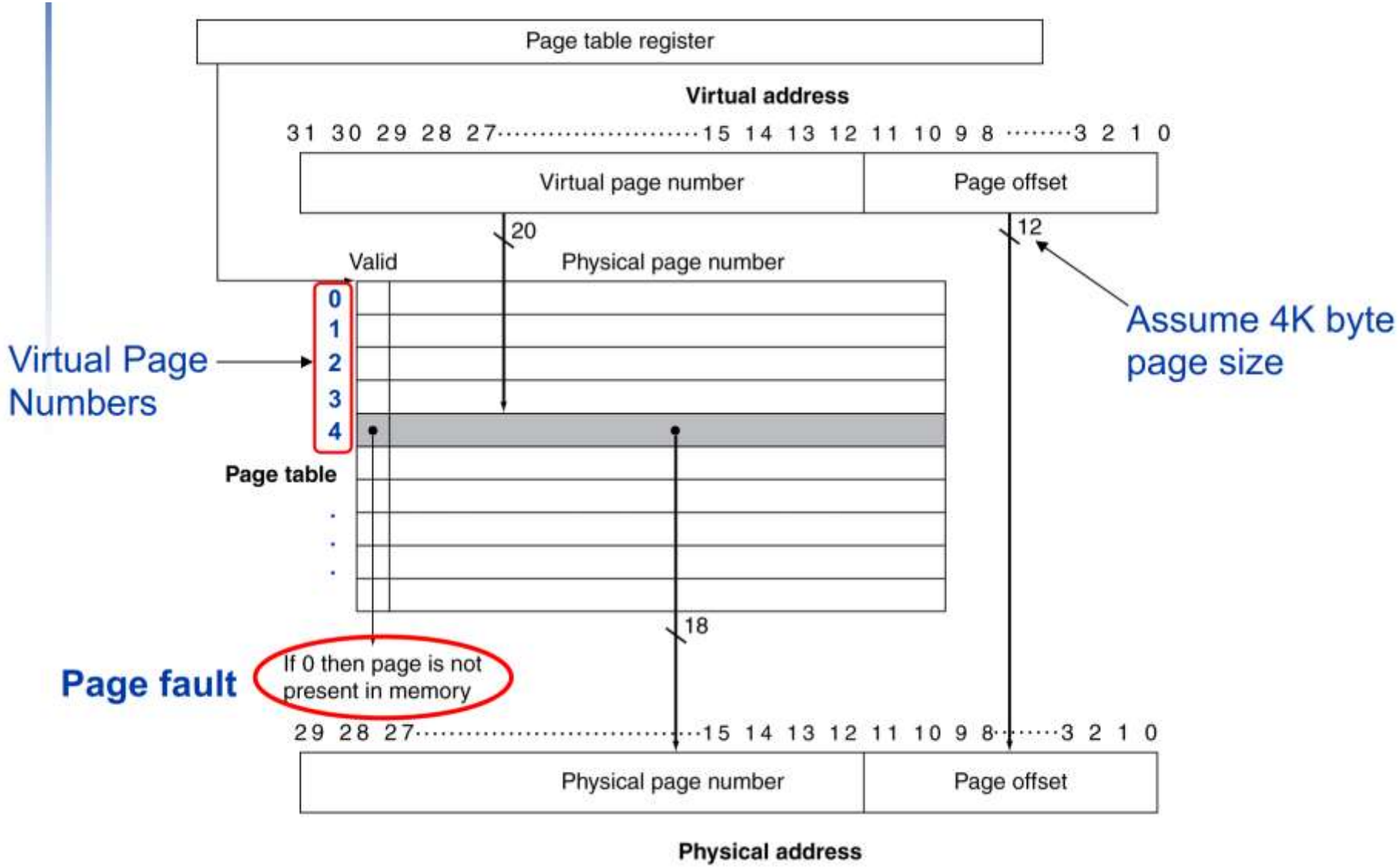
Virtual Memory



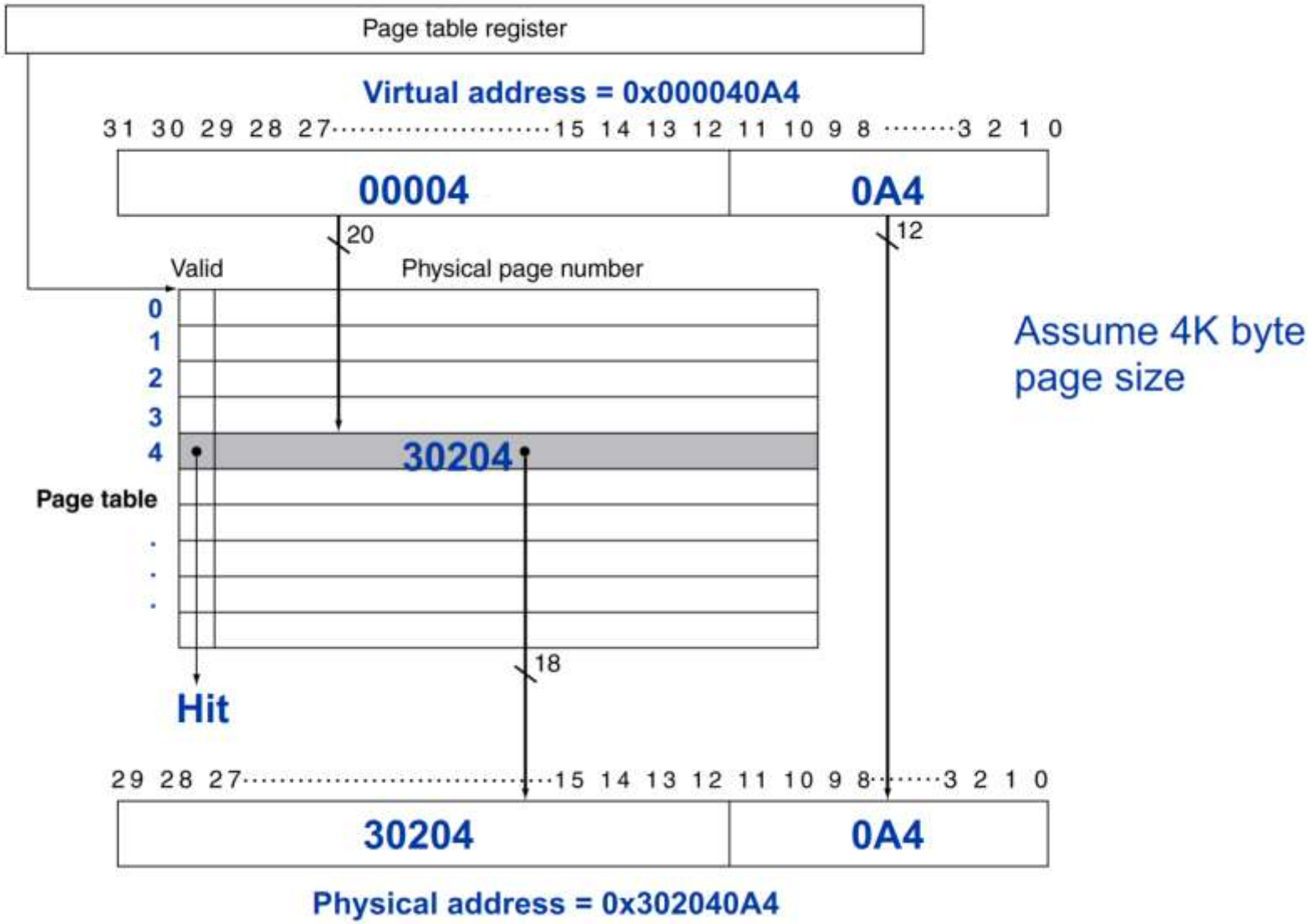
- **The addresses provided by the processor are all virtual address**
- **The length of page offset depends on the size of the page.**

Let the length to be **L**, then the size of the page should be 2^L. 1K = 10bits, 1M = 20bits, 1G = 30bits

Virtual Memory



Virtual Memory



Assume 4K byte page size

Exercise 1

- Given
  - 4KB page size, 16KB physical memory, LRU replacement
  - Virtual address: byte addressable, 20 bits (how many bytes?)
  - Page table for program A stored in page #0 of physical memory, starting at address 0x0100, assume only 2 valid entries in page table:
    - Virtual page number 0 => physical page number 1
    - Virtual page number 1 => physical page number 2
- Show physical memory including page table
- Complete following table

Virtual Address	Virtual page number	Page fault?	Physical Address
0x00F0C			
0x01F0C			
0x20F0C			
0x00100			
0x00200			
0x30000			
0x01FFF			
0x00200			

Exercise 1

	VPN	Page fault	Physical Addr
0x00F0C	0x00	n	0x1F0C
0x01F0C	0x01	n	0x2F0C
0x20F0C	0x20	y	0x3F0C
0x00100	0x00	n	0x1100
0x30000			

PM

0	Page table		page table	v	PPN
1	0		0	1	1
2	1		1	1	2
3	20		...	0	
			20	1	3
			...	0	
			30	0	
			...	0	

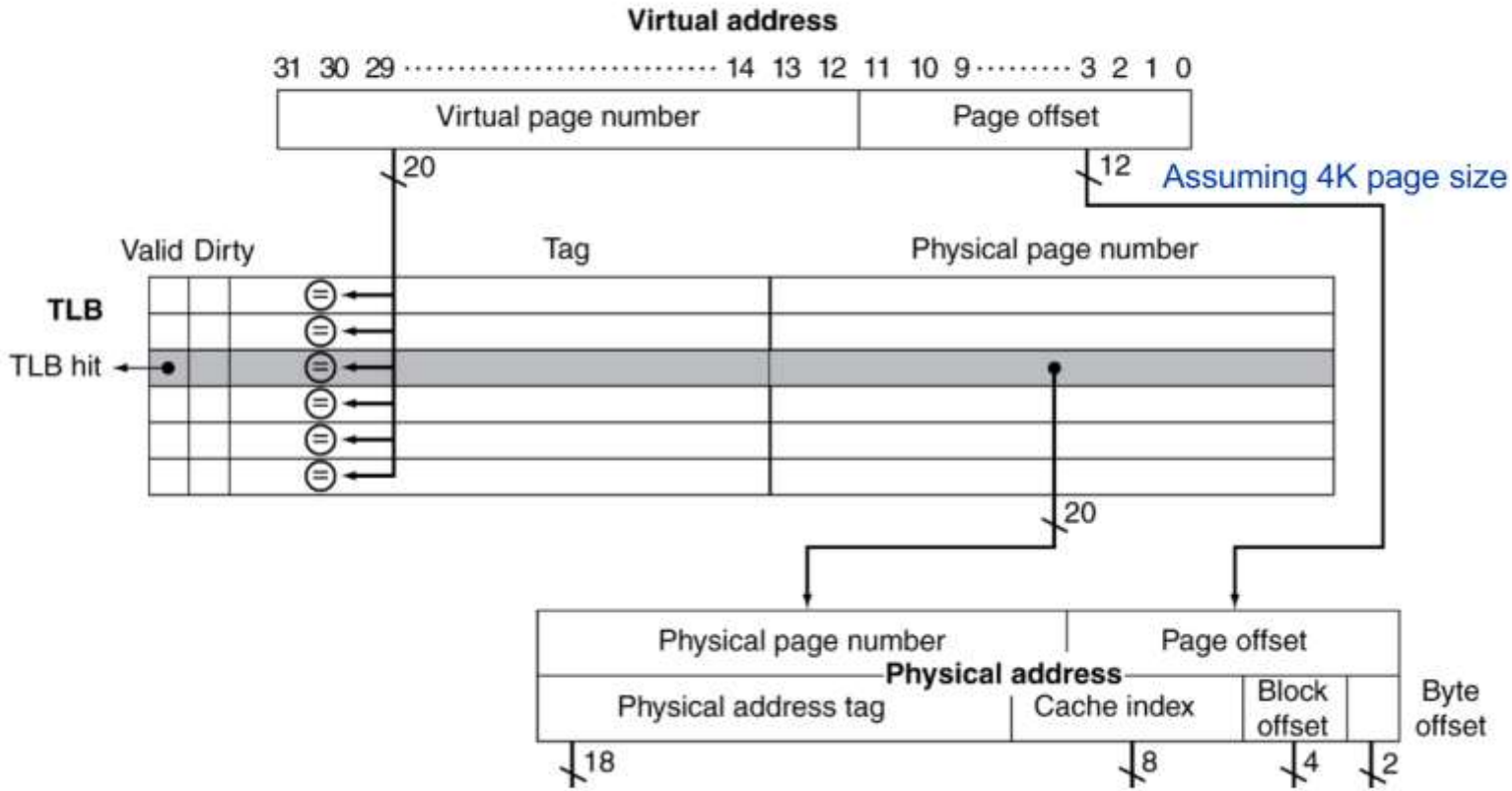
	VPN	Page fault	Physical Addr
0x00F0C	0x00	n	0x1F0C
0x01F0C	0x01	n	0x2F0C
0x20F0C	0x20	y	0x3F0C
0x00100	0x00	n	0x1100
0x30000	0x30	y	0x2000

PM

0	Page table		page table	v	PPN
1	0		0	1	1
2	30		1	1	2
3	20		...	0	
			20	1	3
			...	0	
			30	1	2
			...	0	

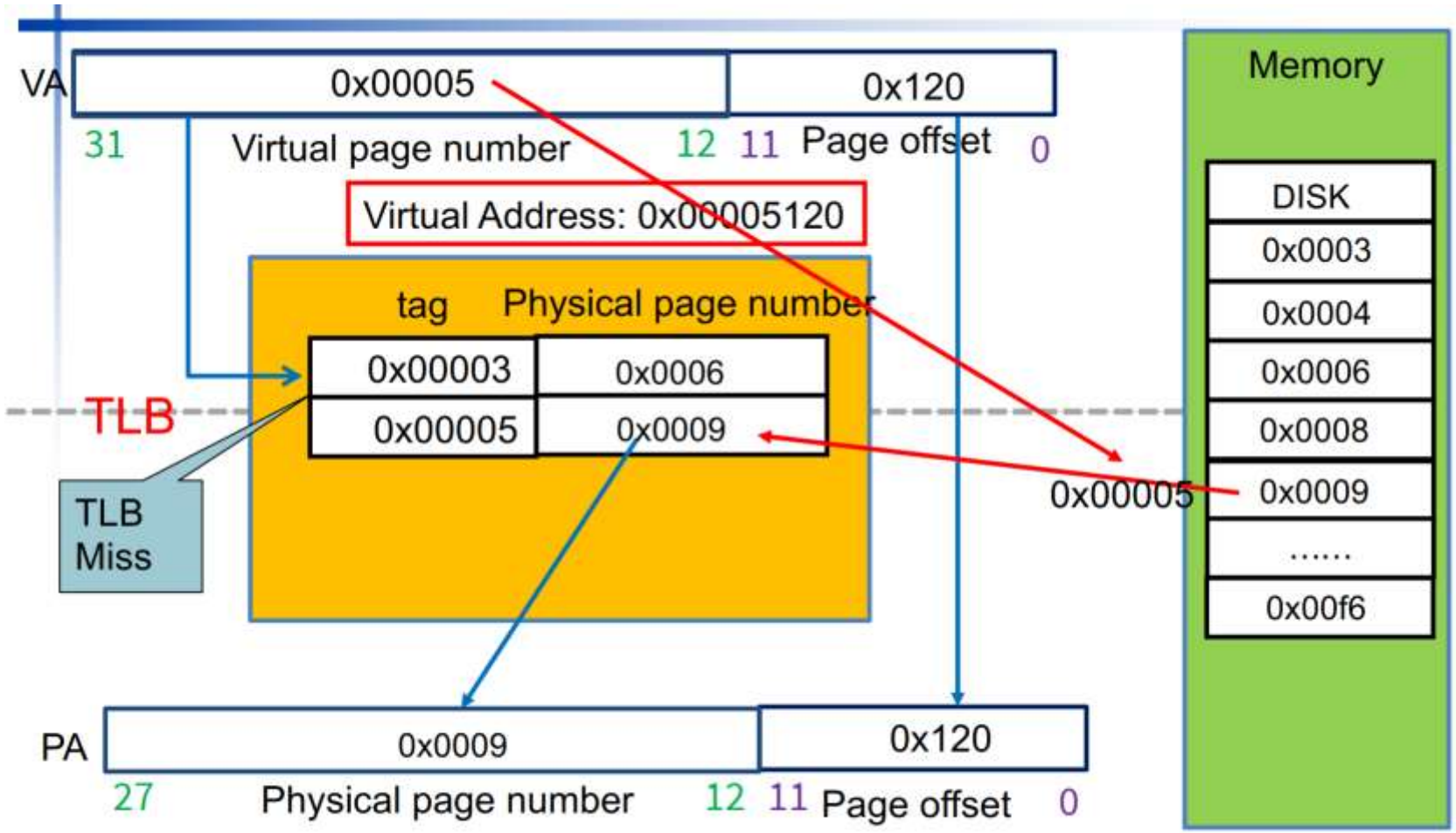
TLB

Virtual page number is the Tag that is compared with all Tag fields of TLB because of full associativity of TLB (only 1 set)

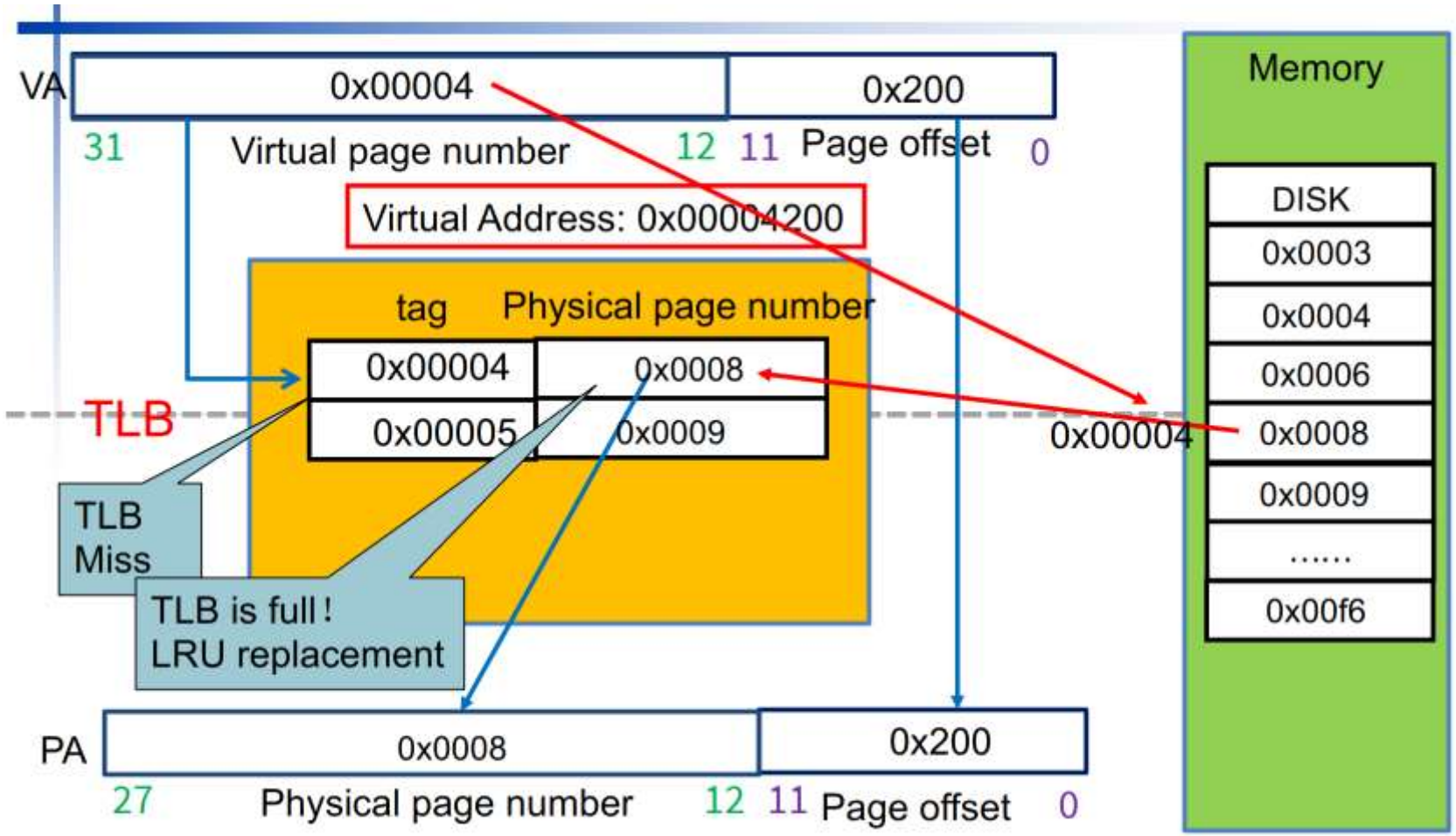


To access physical memory

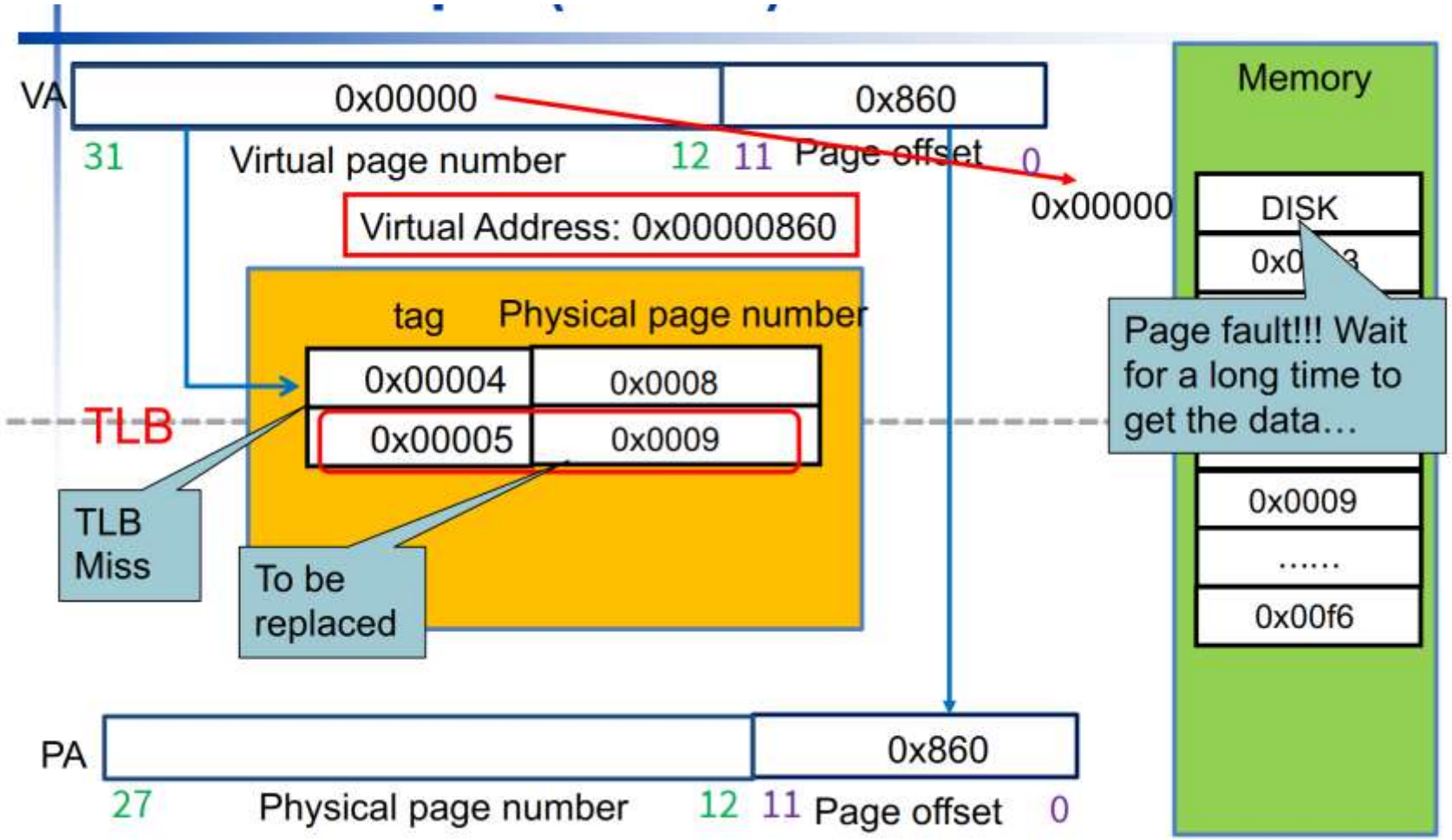
TLB


VA
0x00005
0x120
31
Virtual page number
12 11
Page offset
0
Virtual Address: 0x00005120
tag
Physical page number
0x00003
0x0006
0x00005
0x0009
TLB
TLB Miss
PA
0x0009
0x120
27
Physical page number
12 11
Page offset
0
Memory
DISK
0x0003
0x0004
0x0006
0x0008
0x0009
.....
0x00f6
0x00005

TLB


VA
0x00004
0x200
31
Virtual page number
12
11
Page offset
0
Virtual Address: 0x00004200
tag
Physical page number
0x00004
0x0008
0x00005
0x0009
TLB
TLB Miss
TLB is full !
LRU replacement
0x00004
Memory
DISK
0x0003
0x0004
0x0006
0x0008
0x0009
.....
0x00f6
PA
0x0008
0x200
27
Physical page number
12
11
Page offset
0

TLB


VA
0x00000
0x860
31
Virtual page number
12 11
Page offset
0
Virtual Address: 0x00000860
tag
Physical page number
0x00004
0x0008
0x00005
0x0009
TLB
TLB Miss
To be replaced
PA
0x860
27
Physical page number
12 11
Page offset
0
Memory
0x00000
DISK
Page fault!!! Wait for a long time to get the data…
0x0009
.....
0x00f6

Exercise 2

- Given
  - 4KB page, 16KB physical memory, 4-word blocks, LRU replacement
  - Virtual address: byte addressable, 20 bits (how many bytes?)
  - Page table for program A stored in page #0 of physical memory, starting at address 0x0100, assume only 2 valid entries in page table:
    - Virtual page number 0 => physical page number 1
    - Virtual page number 1 => physical page number 2
  - Fully associative TLB, 2 entries; 4-way associative cache,
- Show how the physical address is used to access a 512-byte cache
- Show the memory structure, complete following table

Virtual Address	Virtual page number	TLB miss?	Page fault?	Physical Address	Cache Hit?	Cache Set Index
0x00F0C						
0x01F0C						
0x20F0C						
0x00100						
0x00200						
0x30000						
0x01FFF						
0x00200						

Exercise 2

	VPN	TLB miss	Page fault	Physical Addr	cache hit	cache set index
0x00F0C	0x00	y	n	0x1F0C	n	000
0x01F0C	0x01	y	n	0x2F0C	n	000

	PM
0	page table
1	vpn0
2	vpn1
3	

TLB	tag	PPN
	0	1
	1	2

cache	word0	word1	word2	word3
0	0x1F00	0x1F04	0x1F08	0x1F0C
	0x2F00	0x2F04	0x2F08	0x2F0C
1				

Exercise 2

	VPN	TLB miss	Page fault	Physical Addr	cache hit	cache set index
0x00F0C	0x00	y	n	0x1F0C	n	000
0x01F0C	0x01	y	n	0x2F0C	n	000
0x20F0C	0x20	y	y	0x3F0C	n	000

	PM	TLB	tag	PPN
0	page table		20	3
1	vpn0		1	2
2	vpn1			
3	vpn20			

cache	word0	word1	word2	word3
0	0x1F00	0x1F04	0x1F08	0x1F0C
	0x2F00	0x2F04	0x2F08	0x2F0C
	0x3F00	0x3F04	0x3F08	0x3F0C
1				

Exercise 2

	VPN	TLB miss	Page fault	Physical Addr	cache hit	cache set index
0x00F0C	0x00	y	n	0x1F0C	n	000
0x01F0C	0x01	y	n	0x2F0C	n	000
0x20F0C	0x20	y	y	0x3F0C	n	000
0x00100	0x00	y	n	0x1100	n	000

	PM	TLB	tag	PPN
0	page table		20	3
1	vpn0		0	1
2	vpn1			
3	vpn20			

cache		word0	word1	word2	word3
	0	0x1F00	0x1F04	0x1F08	0x1F0C
		0x2F00	0x2F04	0x2F08	0x2F0C
		0x3F00	0x3F04	0x3F08	0x3F0C
		0x1100	0x1104	0x1108	0x110C
	1				

That's all for My Part